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**THE IMPACT OF
MICROCOMPUTERS ON AVIATION:
A TECHNOLOGY FORECASTING
AND ASSESSMENT STUDY**

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**VOLUME I: UNCONSTRAINED FORECASTS OF
MICROCOMPUTER TECHNOLOGY**

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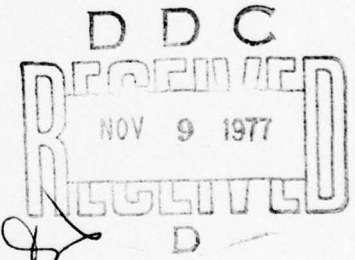
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**September 1977
FINAL REPORT**



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**U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION**

Office of Aviation Policy

Policy Development Division

System Concepts Branch

Washington, D.C. 20591

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CHAPTER ONE

INTRODUCTION

Microcomputers* are fast emerging as the technology of the 1970's. They are finding their way into everything from televisions to washing machines, microwave ovens to automobiles, and pocket calculators to aviation avionics. It now appears that few fields of human endeavor will remain untouched by this rapidly advancing technology and some social historians are suggesting that the inexpensive microcomputer may well rank as the third major cultural invention of the twentieth century, following the automobile and the television.

Microcomputers are indeed a technology under very rapid development; their costs, weights, and sizes are decreasing drastically while their computing capabilities, versatility and reliability are increasing at almost the same rate. These revolutionary changes can have a tremendous impact on the National Aviation System (NAS), including all the salient aspects of energy efficiency, air traffic control, safety, and environmental protection. It was considered imperative that the possible impact of microcomputers on NAS be assessed, so that the Federal Aviation Administration (FAA) could begin formulating appropriate policies in anticipation of, not in reaction to, the subject revolutionary changes.

*For a detailed explanation of terms, see the glossary on page 293.

In recognition of the major impact which microcomputers may have on society in general, and aviation in particular, the Federal Aviation Administration, Office of Aviation Policy, Policy Development Division, System Concepts Branch, has funded this study consistent with the goals of its Technology Forecasting and Assessment Program. The study has as its main objective the assessment of the impact of microcomputers on the National Aviation System (NAS). The time horizon of the impact assessment is 1976 to 2000 A.D. The impact will be assessed with respect to the important goals of the NAS, specifically, those referred to as the "S3E" goals (Safety, Energy, Environment, Economics). Another objective of the study is to identify the policy implications accompanying the impacts.

A primary purpose of the Technology Forecasting and Assessment (TF&A) Program within the Federal Aviation Administration, Office of Aviation Policy (AVP) is to anticipate certain rapid technological changes that may have profound impact and policy implications for the NAS. The Onyx Corporation had the privilege of assisting the Policy Development Division, System Concepts Branch, within AVP, in defining the scope and the urgent tasks for its TF&A Program. One of the urgent tasks identified and presented in the final project briefing in December 1975, and later expanded in the final report [1], was the potential impact of microcomputers on the NAS.

The problem addressed by the subject study stemmed from the drastically changing needs of the NAS on the one hand, and the

opportunities accompanying the rapid advances in microcomputers on the other. In the NAS, as in other modes of transportation, "S3E" has become a major challenge to Federal agencies in a search for definitive new policies and technological alternatives that will help attain all these important goals simultaneously.

From the standpoint of methodology, the study has used a mix of "exploratory forecasting" and "normative forecasting." In exploratory forecasting, the future advances in microcomputers were projected assuming a "surprise free-unconstrained" economy. Although special attention was given to those advances which were particularly relevant to the NAS, the projections were by and large independent of the needs of NAS. In normative forecasting, the NAS "S3E" goals in the context of five alternative aviation scenarios were used as the basis to project, under "constrained" conditions, the impact of microcomputers on the NAS.

The study report consists of two volumes. This volume includes the Technological Forecast for microcomputers over the designated time horizon and Volume II includes the technology assessment of the forecasted developments.

CHAPTER TWO

TECHNOLOGY DEFINITION AND

STATE-OF-THE-ART

I. Introduction

Although the primary thrust of this study is the future capabilities of microcomputers, a summary of the current state-of-the-art in microcomputer technology provides a concrete point of departure for the following chapters. Also, a precise definition of microcomputer technology and an identification of the technological trends and characteristics having particular importance to the FAA and aviation would be useful. This chapter provides this background information for each of the hardware and software areas in Sections II and III below, respectively. The hardware technological forecasts then follow in Chapters Three, Four and Five, and the software forecasts in Chapter Six.

II. Microcomputer Hardware

A. Historical Development of Integrated Electronics

In dealing with microcomputer hardware, it is appropriate to deal first with technology in more general terms, since the speed, power, and size of a given technology will largely determine the speed, power, chip complexity, and cost of a microprocessor, memory, or any other circuit function realized. At the present time (1976) there are several competing technologies

which are recognized as being appropriate for large scale integration (LSI). Each of these will be considered in some detail in this section.

Historically, solid state electronics began with the invention of the transistor at Bell Telephone Laboratories in 1947. During the decade of the 1950's, the bipolar transistor structure was refined and transistorized circuits rapidly replaced vacuum tubes in a wide variety of applications. About 1960, batch-fabrication and miniaturization was extended to the circuit level with the development of the planar process for integrated circuits. This was based on the use of photoengraving, particularly in silicon dioxide, to define the circuit components in a single monolithic substrate. The decade of the 1960's concentrated on the development of technology. The art of photolithography was extended, ion implanatation and diffusion were introduced and refined for implementing the doping process, and a variety of metal interconnect schemes were investigated. Epitaxy was also developed during this period.

Three driving factors motivated these developments in technology: achieving lower cost, higher speed, and higher performance. The drive toward lower cost concentrated on reducing device size and on simplifying

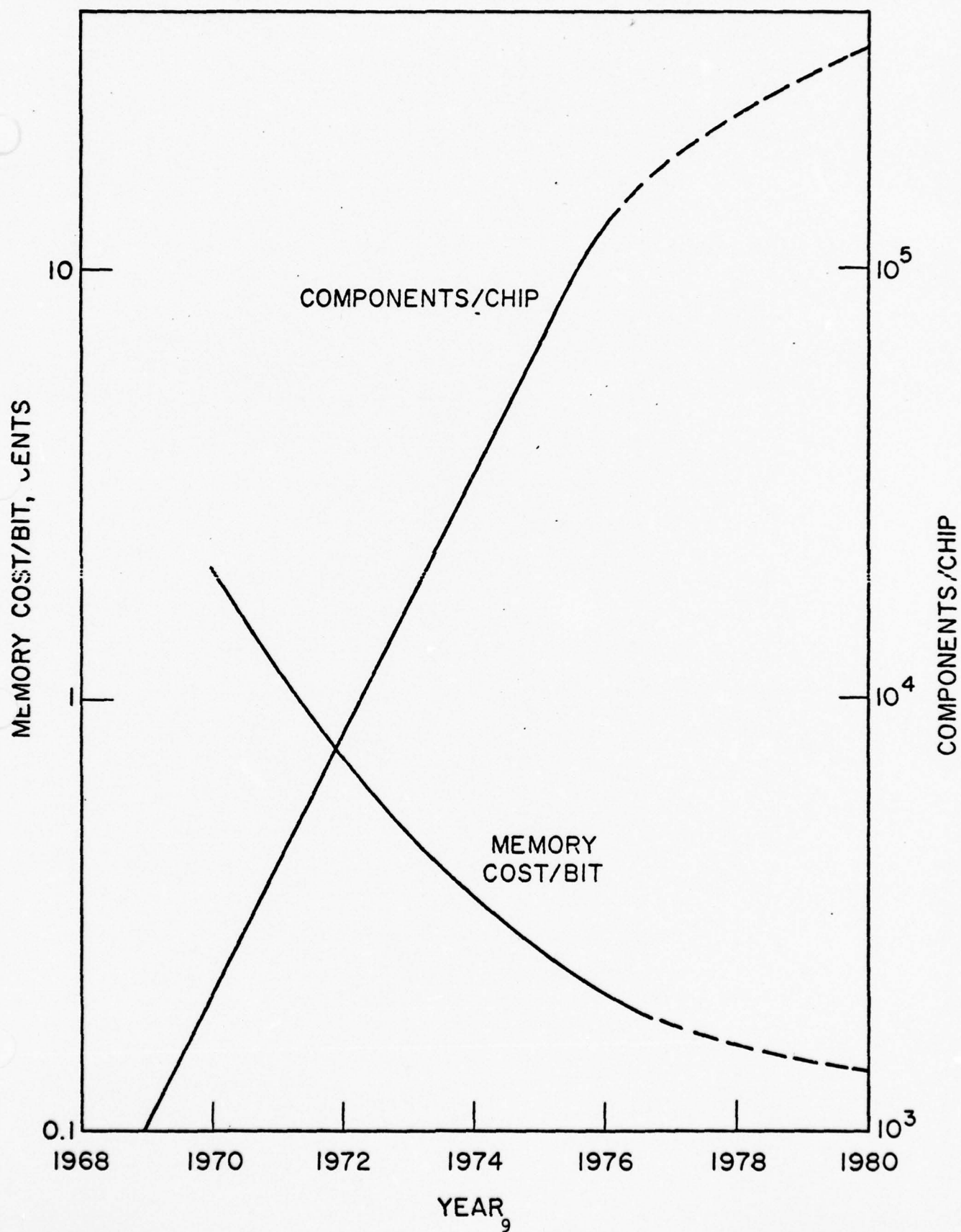
the fabrication sequence to put more functions on a chip and attain higher yields. During the first half of the 1960's, the technology rested entirely on the junction isolated bipolar transistor. About 1965, metal-oxide-silicon (MOS) transistor circuits were introduced for digital applications. Although slower than bipolar circuits, they were also denser and simpler to fabricate. The latter half of the 1960's saw intensive work on MOS processes in order to control turn-on thresholds and enhance speed. Bipolar technology experimented with a variety of new structures which were more dense and simpler to fabricate. Most of these attempted to replace junction isolation or at least reduce the capacitance of the isolating junction. This generally led to higher speed along with lower cost so that although MOS preserved its cost advantage, bipolar structures maintained their speed advantage. The diversity of approaches and the number of companies involved in developing integrated electronics had a strong influence on the rapid pace with which developments occurred.

Although most applications were digital, from 1965 on an increasing number of linear integrated circuits (IC) were introduced. Monolithic operational amplifiers were the first major linear circuit function to be integrated. Later, phase-locked loops, digital-to-

analog and analog-to-digital converters followed. These developments motivated activity aimed at achieving high performance levels--low temperature coefficients, high accuracy, etc. Many structures at first used thin film passive components in hybrid assemblies; however, the trend has been increasingly toward monolithic structures for lower cost while preserving performance by sophisticated circuit design and, in some cases, the use of thin film components on the silicon itself.

Figure 1 shows the ability to pack electronic components on a single chip (die) while maintaining acceptable yields. The number of components has been doubling every year and in the near term is expected to continue doubling about every two years. At the same time, the cost per function (in this case, per bit of memory) has been declining rapidly. It is this combination of increased functional complexity and decreased functional cost which is causing the rapid proliferation of electronics into many formerly non-electronic areas. It is the purpose of this study to assist the FAA in planning policy which will allow the aviation community take maximum advantage of this expanding technology during the coming decade.

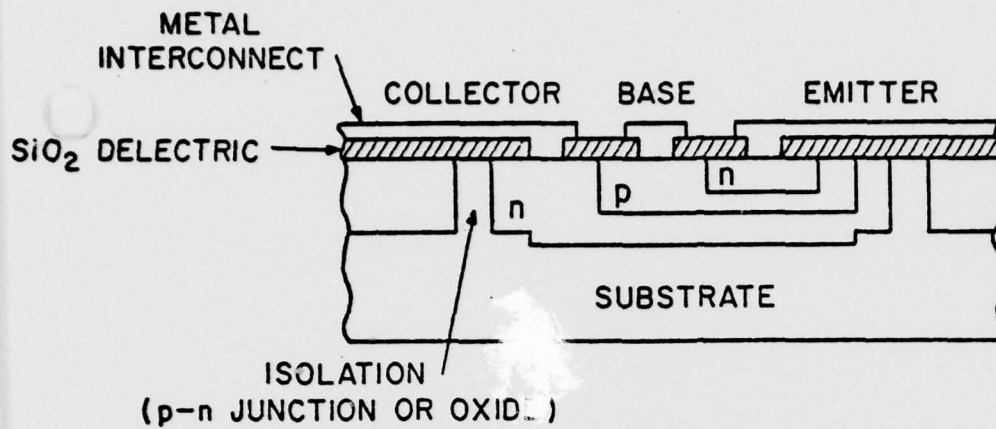
FIGURE 1: TRENDS IN ELECTRONICS
COMPONENT DENSITIES



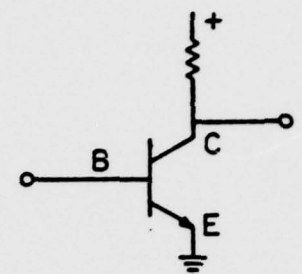
B. Present State-of-the-Art

As a basis for the unconstrained technology forecasts it is essential to first briefly review the present state-of-the-art. As indicated above, present integrated circuits are formed via a series of photoengraving operations which control the selective introduction of dopants such as boron (p-type) and phosphorous (n-type) into the silicon lattice to form diodes, resistors and transistors. The implementation of logic with these comments depends on the realization of an electronic switch (e.g., a device in which the application of a small current at one terminal controls the flow of a larger current between two other terminals), and for the last ten years, the two ways of doing this in silicon have competed. Figure 2 shows cross sections of the two approaches: the charge controlled bipolar transistor and the voltage controlled unipolar MOS transistor. The bipolar (positive and negative charge carriers) transistor bases its operation on the fact that a positive voltage applied to the base relative to the emitter causes electrons to be injected from the heavily doped emitter into the base. Once injected, the carriers diffuse to the reverse biased collector where they constitute collector current. The only charge which flows in the external base lead is that necessary to make up for electrons which recombine before they reach the collector. Thus, a relatively small base current can control a

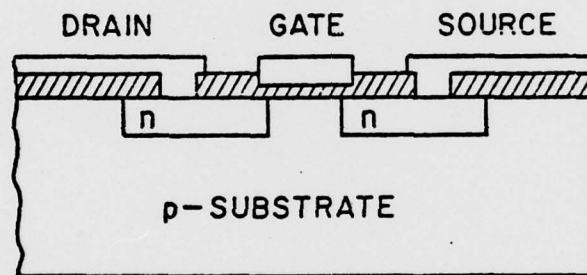
FIGURE 2: THE TWO CURRENT METHODS OF LOGIC IMPLEMENTATION



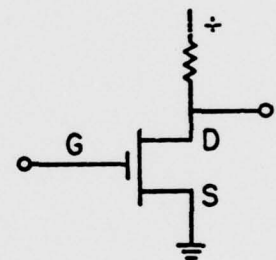
BIPOLAR (npn) TRANSISTOR



BIPOLAR INVERTER



MOS TRANSISTOR



nMOS INVERTER

large collector-emitter current. The on-resistance from collector to emitter when used as a switch is typically less than 100 ohms while the off-resistance is many megohms.

The MOS switch is based on a different phenomenon. With no voltage applied to the gate, no conducting path from drain to source exists and the switch is off. When a positive voltage is applied to the gate, however, holes are repelled from the surface and electrons are attracted. When the gate voltage rises above a threshold determined by the channel doping and gate dielectric thickness, the silicon surface under the gate electrode inverts to n-type, forming a conducting path from drain to source with an on-resistance from several hundred to several thousand ohms depending on the applied gate voltage and the size of the device.

Details of fabrication, design, and operation can be found in the literature [18]. For the purposes here only the basic differences will be indicated so that an accurate assessment of future developments and fundamental limits can be made.

As indicated above, efforts during the late 1960's to reduce the size and parasitic capacitance associated with the isolation areas between devices led to shallower and faster device structures, often employing SiO₂ sidewall or even all around isolation from the

substrate. The early advantages of MOS in terms of device size and process simplicity were traded to some degree in an effort to improve the performance of these devices. MOS and bipolar approaches are probably closer now than ever as bipolar has become more dense and MOS has become faster. Both technologies are continuing to evolve rapidly.

Figure 2 shows a basic inverter implemented with bipolar and MOS switches. The different LSI technologies differ in the device structures used for the driver (switch) device and the load. Most technologies use a second transistor as an active load device, both because the transistor requires less area than would a resistor of comparable value and because the nonlinear properties of the active load can be used to optimize the power and speed of the gate. In integrated injection logic (I²L) [12], the most promising of the bipolar approaches, a lateral pnp transistor is used as a load. In p-channel and n-channel MOS, both enhancement and depletion loads have been used [22], while in complementary MOS (CMOS) the load is a pMOS device while the driver is nMOS. Since in CMOS, either the driver or the load is always off, the quiescent power dissipation of this technology is virtually negligible.

Table 1 compares the major LSI technologies in terms of their process complexity and required gate areas

TABLE 1: APPROXIMATE PROCESS COMPLEXITY AND
SIZE OF THE LSI TECHNOLOGIES

	TTL	I ² L	pMOS	nMOS	CMOS
Mask Steps	7	5	4	6	6
Number of Diffusions	4	3	1	3	3
Gate Area (mil ²)	20	5	10	6	20

[27,29]. I²L with its merged transistor structure has the smallest gate size, followed closely by nMOS. Both transistor-transistor logic (TTL) and CMOS require more area due to the number and complexity of the devices used to realize a gate. It should be noted that production line widths (5 to 7 μm) and alignment tolerances (2 μm) have not changed greatly over the past five years, and size reductions have generally come from structural changes in the devices rather than from simple scaling of dimensions. All of these technologies have been used for microprocessors. It should be noted that on a typical microprocessor chip, half or more of the chip area is inactive, i.e., used to support the interconnect wiring but not part of an active gate, so that differences in gate area may not translate directly to differences in chip size.

A semiconductor technology not shown in these comparisons is emitter coupled logic (ECL), a bipolar family. This structure is now being used for high speed computers, but its power levels preclude high levels of integration on a single chip. Thus its use in microcomputers is doubtful. TTL as used in these comparisons is the low power Schottky version (LSTTL) since this represents the best present tradeoff among speed, density, and power for microcomputer applications of all the TTL versions available. It is likely that new

technologies will evolve during the next decade and that some of those listed will be replaced. For this reason, after discussing the criteria by which technology will be assessed, each of the present technologies will be individually assessed in terms of future potential. Then the criteria will be forecast in terms of the performance available from any available technology. The criteria for forecasting and assessment will be:

- 1) Cost per function
- 2) Reliability
- 3) Speed
- and 4) Power

Each of these will now be examined as a basis for the forecasts.

C. Cost in LSI Circuits

During the past five years, the cost per function has declined at a rate of from 20 to 50 percent per year or more. In discussing cost here, the focus will be on the levels which can be achieved in high volume production, given sufficient product life to fine tune the processing and optimize yield.

The cost of an integrated circuit is composed of the cost of the processed die together with the cost of packaging and testing the completed unit. The cost of

processing a silicon wafer is virtually independent of wafer size and a present cost of \$30 per wafer is assumed. The number of dice per wafer, neglecting edge drop out, is

$$N = \frac{\text{wafer area}}{\text{die area}} = \frac{\pi D^2}{4A} , \quad (1)$$

where D is the wafer diameter and A is the die area.

It is now assumed that the primary yield limiting mechanism is the presence of defects on the masks (or in the photoresist) which limit the yield from each photoengraving operation. The yield of die which pass visual inspection, neglecting die breakage or loss due to non-mask related sources, is [11]

$$Y_p = (1 + FA)^{-n} , \quad (2)$$

where F is the defect density per mask and n is the number of masking operations per wafer. Then the cost of a potentially good die is

$$\text{cost/die} = \frac{\$30}{NY_p} \quad (3)$$

To this cost must be added the cost of testing, T , and packaging, P . A cost of \$0.30/die for testing and a package cost of \$0.15 for plastic or \$0.82 for ceramic is assumed. A final test yield, Y_F , of 0.8 is also assumed. Then, the approximate cost per package circuit is

$$\text{cost/DIP} = \left[\frac{\$30}{NY_p} + T + P \right] \left[\frac{1}{Y_F} \right] . \quad (4)$$

Figure 3 shows cost as a function of die area with the process complexity (masking steps) as a parameter. For 3 inch wafers and 10 defects per square inch, the final circuit cost is dominated by packaging and testing below die areas of approximately 20 K mil². Most present 4K-bit Random Access Memories (RAMs) fall in the 20 to 30 K mil² range so that assembly, packaging and testing can be expected to play an important role in the final cost of these units. Many microcomputers are in the 30 to 40 K mil² range, where die cost and process complexity remain more important. Figure 3 also shows the estimated cost of a single chip function requiring 20 K mil² of silicon in nMOS, assuming a 50 percent overhead at this density for lead routing. The data in Table 1 was used to estimate the cost in other technologies.

Figure 4 shows the packaged cost per unit area as a function of die size. A 3 inch wafer, 6 mask process, 10 mask defects per square inch, and a ceramic package is assumed nominal, and single deviations are examined in terms of their effect on cost. For large systems, it is clearly more cost effective to implement the required functions in a few large die rather than in many smaller chips. For example, a system requiring a 40 K mil² of silicon in a given technology would cost approximately \$3 as a single LSI chip. As

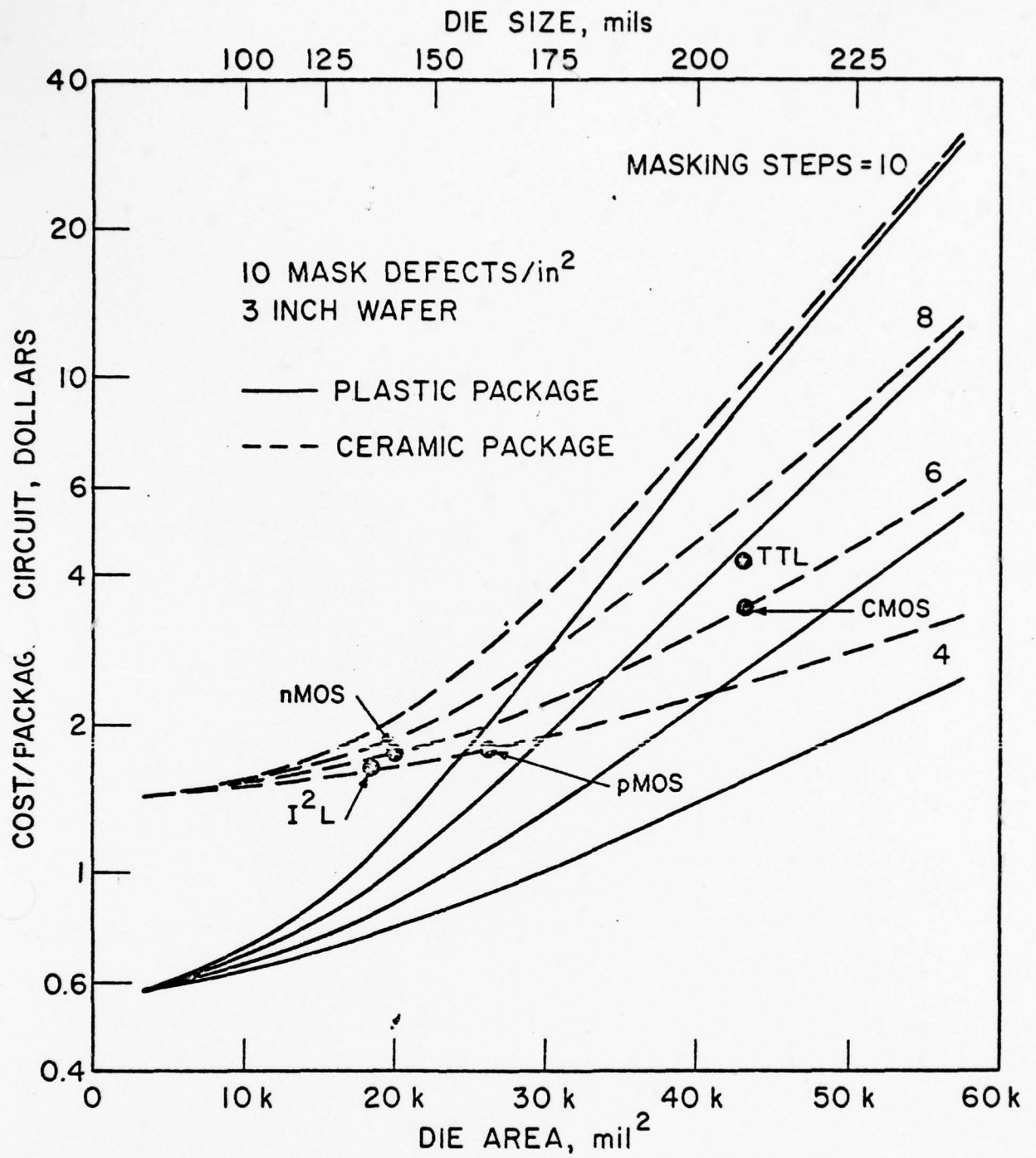
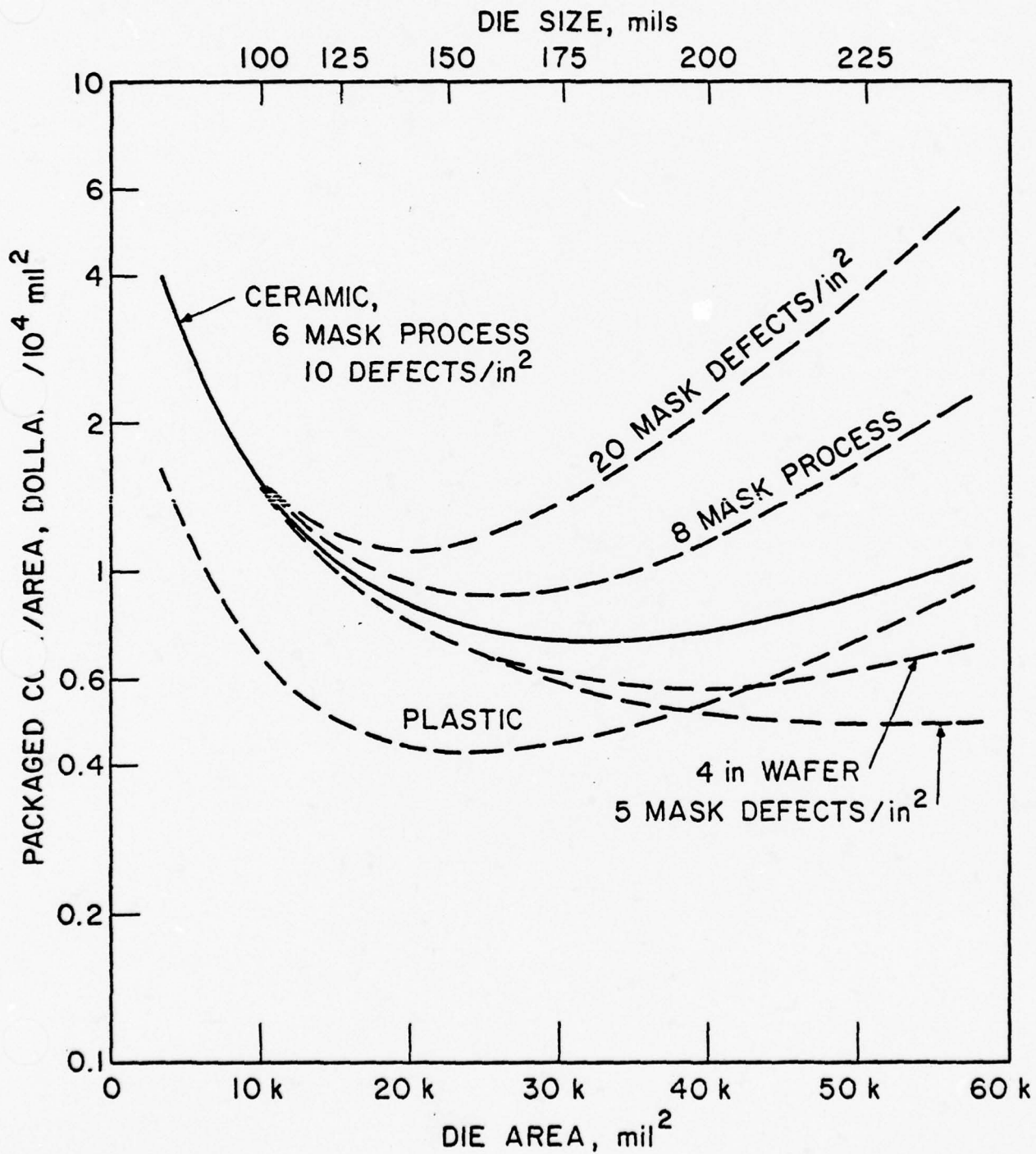


FIGURE 3: COST AS A FUNCTION OF DIE AREA

FIGURE 4: PACKAGED COST PER UNIT AREA AS A FUNCTION OF DIE SIZE



four 10 K mil² chips, the system cost would be \$6. Any increased testing and package cost for the larger chip (not included) would be at least partially offset by the lower cost associated with mounting the single DIP. Recent activity in projection printing (to achieve lower defect densities) and the trend to larger wafers support the use of larger, more complex chips in future LSI systems. The objective costs given in these figures indicate that given sufficient time to fine tune a product line, the cost of such systems will be extremely low. Microprocessors are available today at less than \$10 in volume.

D. Reliability

High reliability is essential in virtually all applications of electronics in aviation. In addition to extensive work to minimize failures at the chip level, work on applying redundancy through the use of distributed and duplicated control is one approach being investigated to ensure system reliability in the face of imperfect reliability at the chip level.

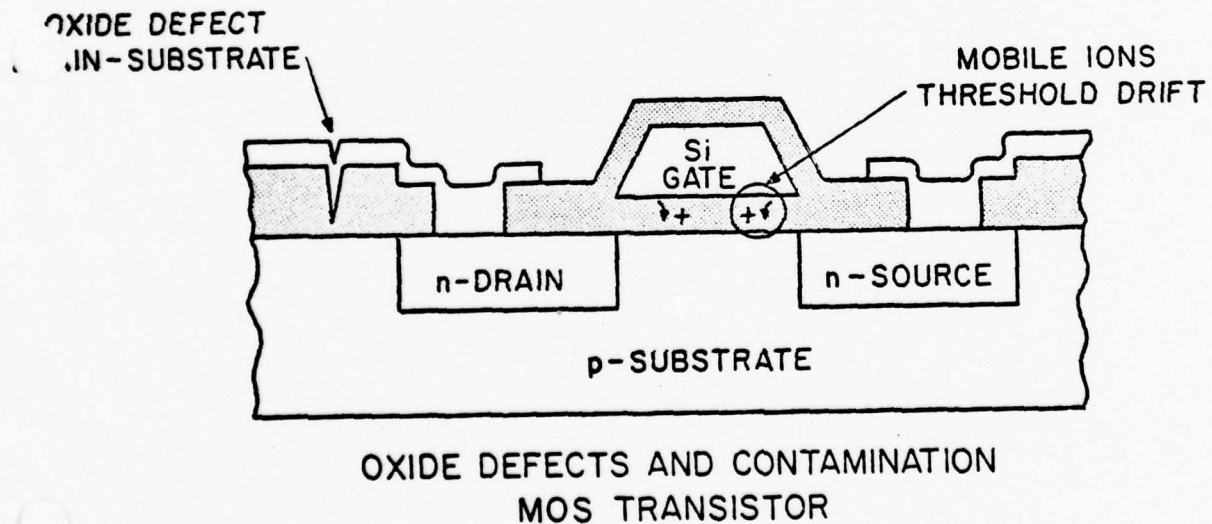
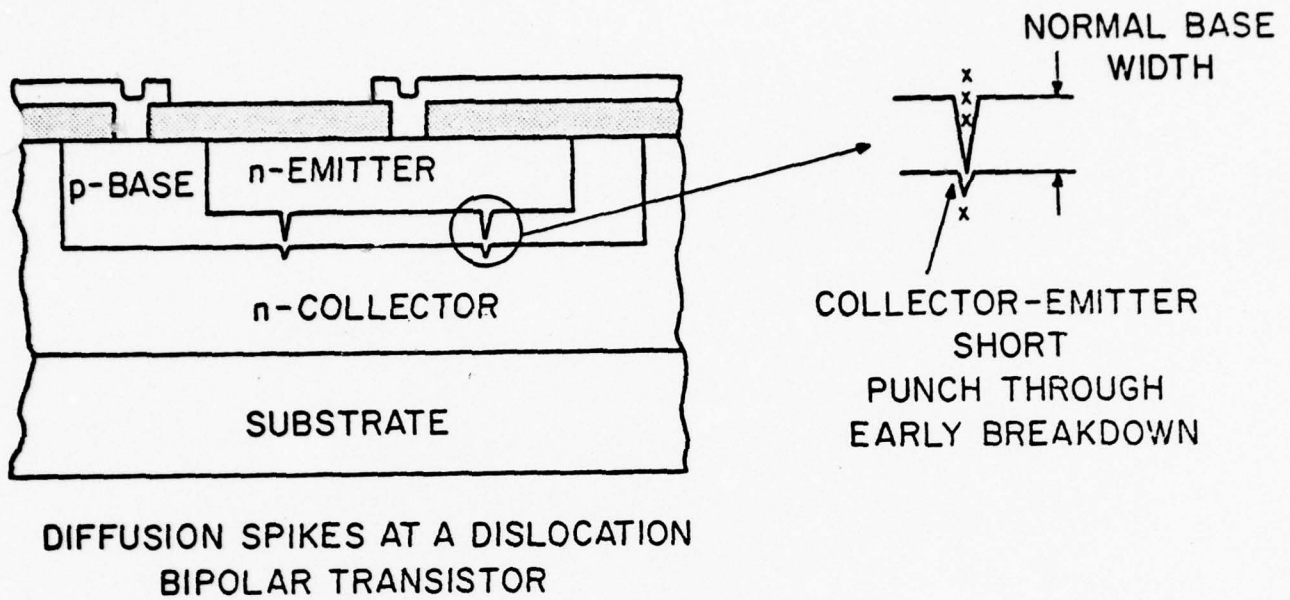
In the past, on-chip failures in integrated electronics have been frequently of less significance than off-chip failures, e.g., at bonds or associated with external leads. As more and more of the system is integrated on a single monolithic die, however, the chip related

failures become more significant as system reliability improves. The failure mechanisms in LSI are diverse and include metalization problems, diffusion and bulk related phenomena and surface or oxide defects.

Two important failure mechanisms for bipolar and MOS-LSI are illustrated in Figure 5. The thin base layer on which bipolar devices depend is achieved only with careful control and uniformity in the diffusion process. Although this control is usually achieved readily, the presence of stacking faults and dislocations in the silicon lattice can enhance local diffusion, producing diffusion spikes. Such spikes can cause emitter-collector shorts or otherwise distort the electrical characteristics causing the device to fail under stress. The susceptibility of bipolar LSI to such failures is a concern, and the ability of I²L-LSI to achieve high density with high production yields has yet to be proven.

A large fraction of MOS failures are related to oxide problems, while diffusion phenomena are less important. These oxide problems include pinholes, partial pinholes, dielectric faults, and contamination problems arising from impurities in the gate oxide. Ultra-clean processing and a variety of high temperature bias and stress tests are required to minimize such failures,

FIGURE 5: FAILURE MECHANISMS FOR
BIPOLAR AND MOS-LSI



some of which have activation energies as low as 0.3 eV [41]. Metallization failures related to electromigration or cracking have been minimized by careful attention to maintaining low current densities and proper oxide step contours, respectively [28]. Manufacturer reported failure rates for both MOS and bipolar circuits, including 4K dynamic MOS RAMs, are now well under 0.1 percent/1000 hours at 70°C and 90 percent confidence level. Stated differently, 90 percent of such components would survive for more than 100 years at 70°C. Details concerning extrapolations based on accelerated aging are given in the literature. The significance of testing in achieving high reliability (and cost) cannot be overemphasized. Pattern sensitivity in many LSI circuits does much to complicate the testing problem. Apart from differences between MOS and bipolar failure mechanisms, there are differences among the MOS families. N-channel MOS is generally more susceptible to contamination problems than p-channel due to the lower threshold and positive control voltage in n-MOS, which enhance the effects of mobile positive ions in the gate. Although early CMOS failure rates were higher than for other technologies, recent reports on CMOS static RAMs indicate failure rates lower than nMOS and under 0.05 percent per 1000 hours at 70°C.

The wide temperature extremes, relatively poor voltage regulation, and the presence of serious electrical noise in the airborne environment can combine to cause soft failures, degrading system reliability. Only CMOS is routinely specified over the full military temperature range (-55 to $+125^{\circ}\text{C}$). Logic thresholds in bipolar circuits are related to the voltage across a forward biased diode, which decreases at $2\text{ mV}/^{\circ}\text{C}$. In CMOS, the p-channel and n-channel thresholds track each other so that the input threshold variation is typically less than 5 percent over the military range, whereas bipolar thresholds may vary by 30 percent or more. On the other hand, MOS propagation delays are more sensitive to temperature and can vary by 30 percent from their nominal values over the military range. For clocked systems, this sets a limit on useable clock rates. Junction reverse leakage, which doubles every 11°C in silicon, can affect both bipolar and MOS circuits, especially those utilizing dynamic logic.

Immunity to voltage transients and supply voltage variation is important and depends on the technology chosen. CMOS is probably the best of technologies in these regards, with a noise immunity of nearly half the supply voltage and a wide tolerance to supply voltage variations. Noise immunity depends on the efficiency of the coupling path and on the noise source

and is enhanced by using a slower technology. On-chip coupling is typically less important than coupling to the input leads, which depends on the output impedance levels of the drivers and the sensors. Isolation from power supply transients can be improved by operating from secondary batteries where possible, and this approach is enhanced when system power levels are low.

E. Speed and Power in LSI Circuits

Speed and power can be treated together since in both MOS and bipolar circuits, speed can be traded for low power and vice versa. The power-speed (power-delay) product is a widely used figure of merit in comparing different technologies.

Speed in either bipolar or MOS technology is related to the delay given by the product of node capacitance and node resistance. The resistance (conductance) is, in turn, given by the conductance (or transconductance) of the device. The change in output current for a given change in input voltage, i.e., the transconductance, for a high-frequency bipolar transistor can be expressed as

$$g_{ml} = \frac{\partial I_c}{\partial V_{be}} = \frac{qI_c}{kT} , \quad (5)$$

where q is the electronic charge, k is Boltzmann's constant and T is the temperature in degrees Kelvin.

For an MOS device, the transconductance can similarly be approximated as

$$g_{m2} = \frac{\partial I_D}{\partial V_G} = \left[\frac{2\mu\epsilon_{ox}}{t_{ox}} \right] \left[\frac{Z}{L} \right] I_D^{1/2}, \quad (6)$$

where μ is the carrier mobility, ϵ_{ox} and t_{ox} are the dielectric constant and thickness of the gate oxide, and Z/L is the width-to-length ratio in the channel. Putting in numbers which are representative of present LSI devices at room temperature, the bipolar device had $g_{m1} = 40 I_C$, whereas $g_{m2} = 0.02 I_D^{1/2}$ (nMOS), so that at 100 μA the bipolar transconductance is higher by a factor of 20.

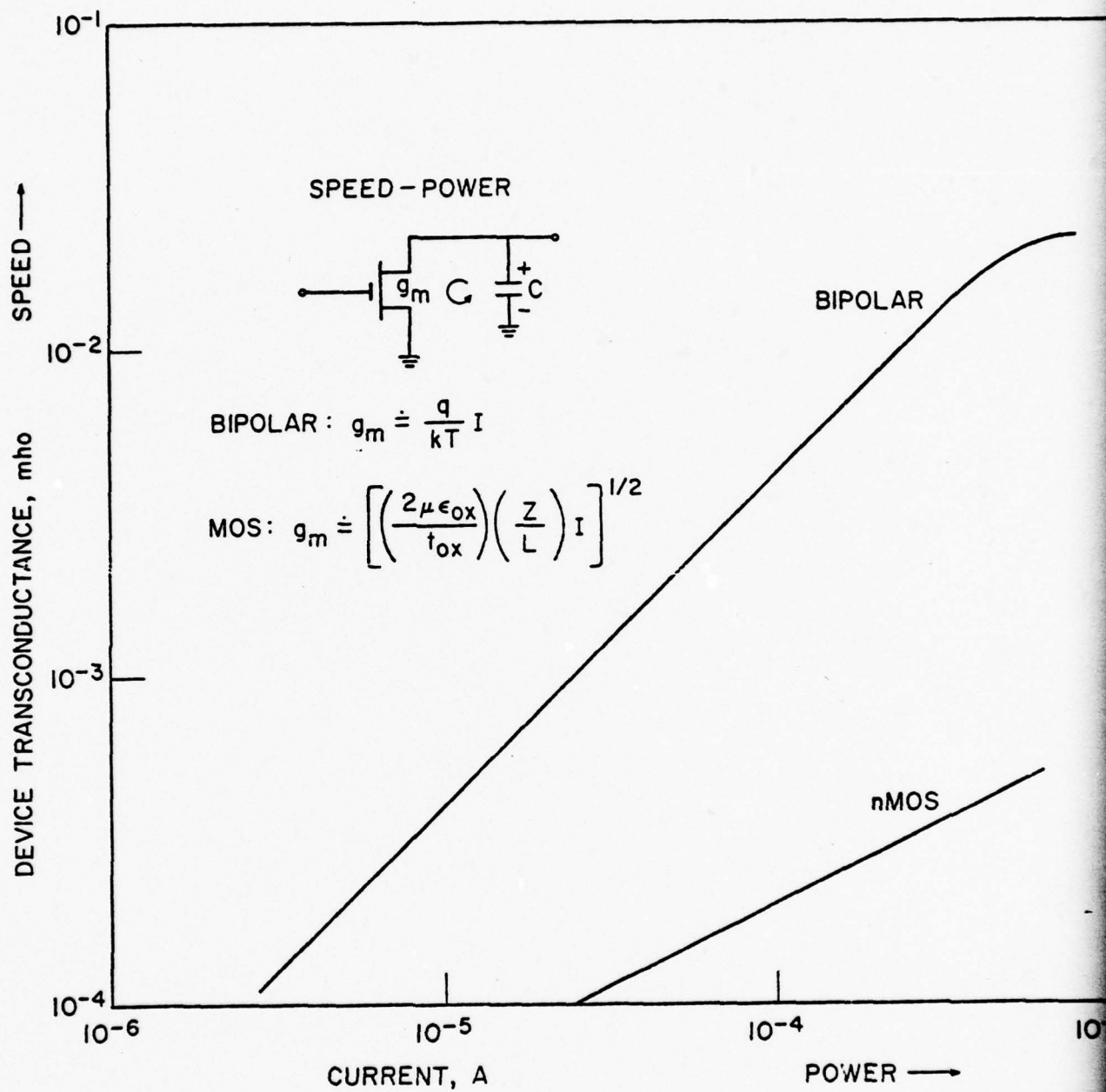
Node capacitance is a function of device area, dielectric thicknesses, substrate doping, and interconnecting line widths. In present LSI, node capacitances are generally well under 1 pf. The greater transconductance of the bipolar device gives bipolar circuits a speed advantage over MOS circuits of similar area and current level. The required voltage swing is several times greater in present MOS, increasing the speed differential. The lower transconductance (and conductance) of the MOS switch is perhaps most noticeable in the limited off-chip drive capability of these technologies. For on-chip functions, where current levels and node capacitance remain low, the speed differential between the

bipolar and MOS approaches is reduced. Figure 6 shows transconductance versus current for typical MOS and bipolar devices.

As the size of the LSI device and its interconnections is reduced, node capacitance can be expected to decrease. Dielectric thickness will probably change relatively little so that capacitance per unit area will remain relatively constant. For an MOS device, the conductance will remain relatively constant. For an MOS device, the conductance will vary with (Z/L) and with current level. At a fixed current level, reductions in device linear dimensions should therefore be expected to increase speed proportional to the reduction in node capacitance. For submicron channel lengths, however, velocity saturation of carriers in high-field portions of the channel can decrease the effective channel mobility so that further increases in speed imply a reduction in operating voltage and thresholds. Future MOS-LSI will make more extensive use of ion implantation for low-threshold device fabrication.

For a bipolar device, the approximation of an RC^+ limitation on speed is valid only so long as these delays dominate over space-charge transit time delays in the collector and minority transport diffusion times in the thin base region. At present these

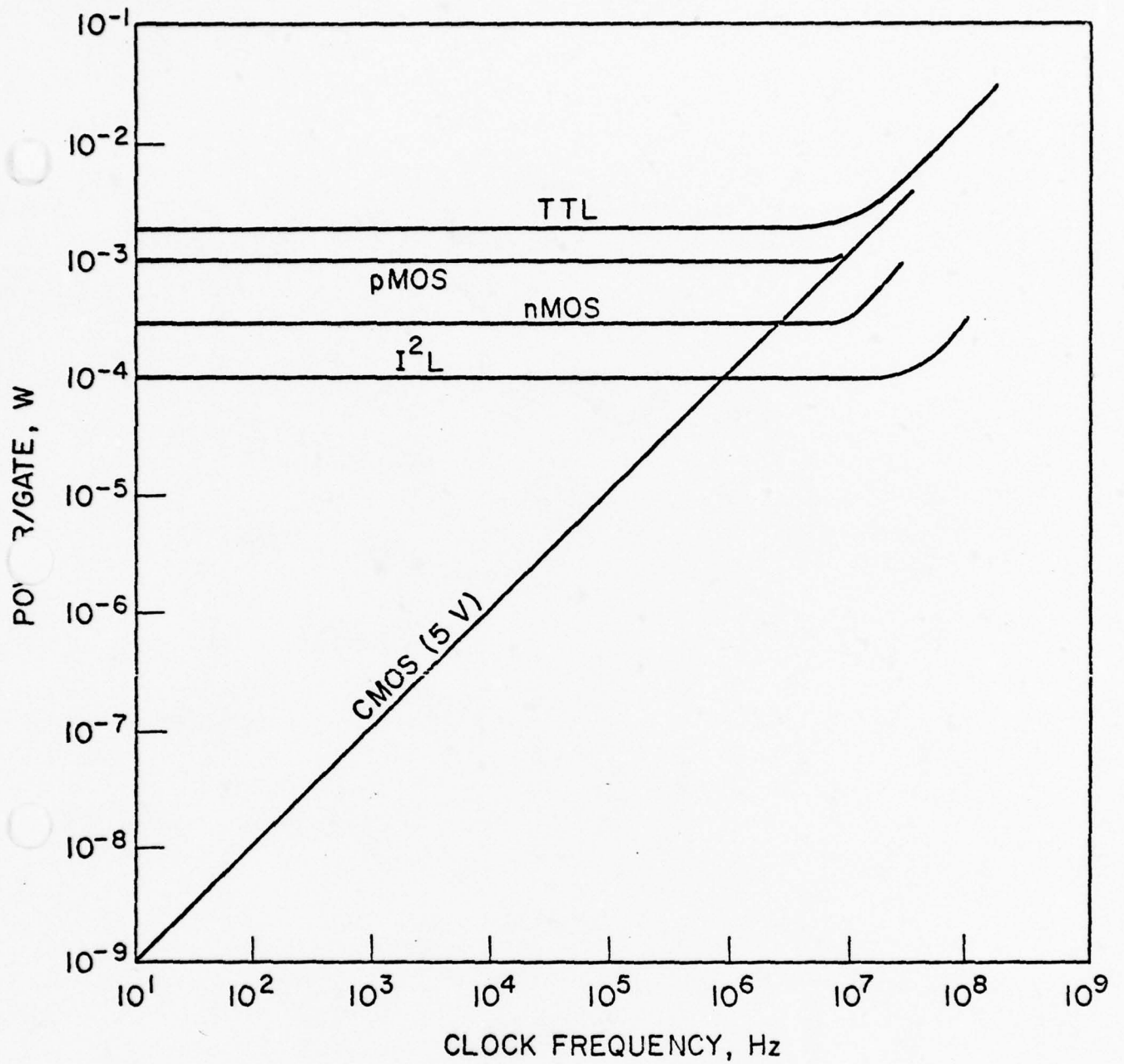
FIGURE 6: TRANSCONDUCTANCE VERSUS CURRENT FOR MOS AND BIPOLAR DEVICES



are roughly comparable in many device structures. As device size decreases, node capacitance can be expected to decrease with device area. At a given current level, however, transconductance (resistance) will remain roughly constant. With the associated increase in speed, base transit delay can be expected to become important. This delay is proportional to the square of the base width. The minimization of base width is limited by nonuniformities associated with the doping process. It is unlikely that this parameter will decrease by more than a factor of four or five below present levels, which means base transit delays will be important for future bipolar LSI and may reduce the speed advantage of the bipolar technologies relative to MOS.

The power of a gate is proportional to the current level at a fixed supply voltage. Figure 7 shows the power dissipation for each of the LSI technologies as a function of clock (switching) frequency, while Table 2 shows the static power and power delay product. Primarily due to the higher mobility of electrons relative to holes, nMOS is faster than pMOS. Schottky-TTL is very fast but consumes relatively high power so that power dissipation can be a limiting factor in LSI chip designs using this technology. As clock frequency increases, the dynamic power associated with

FIGURE 7: POWER DISSIPATION FOR
LSI TECHNIQUES



charging and discharging node capacitance eventually becomes dominant. This is most noticeable for CMOS, where static power dissipation is virtually negligible.

Included in Table 2 are typical instruction cycle times (register-register add times) and power levels for microprocessors realized in each technology. As should be expected, there is a strong correlation between processor performance and gate performance.

III. Microcomputer Software

It has been barely thirty years since the digital computer was born in the middle 1940's, and only twenty since it came into practical use. These twenty years have been an expansion of computer technology and applications that is virtually unprecedented in industrial history. Yet the computer age is still in its infancy and, like the first inventors of the steam engines which led to the industrial revolution, at this point we have neither the imagination nor the foresight to realize what the full effects of the new computer technology will ultimately be.

It is possible, however, to point to several trends and forces at work today, all of which indicate that computers will play an increasingly vital role in the future technologies of the industrialized nations, and will enter more and more directly into the

TABLE 2: PERFORMANCE CHARACTERISTICS FOR
THE LSI TECHNOLOGIES

	TTL	I ² L	pMOS	nMOS	CMOS
Static Power/gate (mW)	2	<0.1	0.5 - 2	0.1 - 0.3	<0.01
Power-delay product (pJ)	10 - 20	<1	200	10 - 20	0.3 - 2
CPU In- struction Cycle (μs)	0.1 - 0.2	0.7 - 1	4 - 12	2 - 5	2 - 6
CPU Power (w)	1 - 3	0.1 - 0.2	0.5 - 1.5	0.2 - 1	0.01

life of each of their citizens. These trends and forces are:

- 1) "Computer hardware is becoming less expensive and more powerful every day."

The continuing decrease in hardware costs and increases in its capability is making it possible to employ computer technology in applications that were undreamed of only two or three years ago.

- 2) "The surrounding technologies require ever increasing amounts of information processing capability."

Developing technologies embedded in an expanding population have an insatiable appetite for information. Every new system, from manufacturing to banking to air traffic control, presents new demands for the generation, storage, transmission, and transformation of various types of data. Digital computers are at present the only way to fulfill these needs.

- 3) "Each successful new application of computer technology breeds more new applications."

As each new application area is brought under control through the use of computers, new

refinements and capabilities in that same area immediately suggest themselves, continuously increasing both system size and complexity. In addition, each application acquaints more people with the power versatility of the digital computer, and suggests further applications in their own particular fields. The "intelligent" sewing machines and ovens of today provide a small indication of what the future will bring.

In the midst of this proliferation of computer technology lies computer software. Briefly, the term software refers to all the programs and their associated documentation that are used on a computer, as opposed to hardware, which is the computer itself and its peripheral equipment. It is the software which tells the computer what to do and which gives purpose and form to the raw computing power of the hardware. In any information processing system, the software component is at least as important as the hardware; without it, the machines are nothing but worthless collections of electronics.

In one important sense, cost, software is vastly more important than hardware. In a 1973 study of command and control information processing trends both now

and in the future (Boehm, 1973, 1974, Kosy, 1974 - These reports will be referred to as "CCIP-85" in the remainder of the study.), U.S. Air Force estimated that software comprised 70% of total automatic data processing system costs in 1973, and projected that it would comprise 90% of the cost by 1980. Moreover, it was estimated that over \$10 billion per year was then being spent in the U. S. on software, or over 1% of the gross national product.

It is apparent, then, that the present and future importance of computer software cannot be over emphasized. It is a vital component of a technology upon which an information choked society is becoming increasingly dependent, and it is a huge industry, employing thousands of people and circulating billions of dollars each year.

The forecasts of software parameters is reserved to Chapter Six; however, the criticality of software, particularly with regard to total system cost, should now be apparent.

CHAPTER THREE

AN UNCONSTRAINED TECHNOLOGICAL FORECAST OF MICROCOMPUTER MEMORY AND COMPONENT HARDWARE

I. Introduction

The current state-of-the-art in microcomputer hardware technology discussed in the previous chapter showed an industry subject to incredible dynamic change. This chapter endeavors to forecast the developments in microcomputer hardware to the year 2000. The forecasts presented below reveal a continuation of the dynamic momentum of the past few years through the rest of this century. The implications for society alone are enormous; however, the implications for aviation are equally portentous. The approach of this chapter is to provide an "unconstrained" technological forecast. This means, essentially, that the characteristics of the electronics industry are not expected to radically differ and that current trends are presumed to continue into the future. This is not meant to imply, however, that the forecasts below are the results of simple trend extrapolation. A number of different technology forecasting techniques have been synthesized with informed judgement collected directly from those people at the boundaries of present-day research to provide the forecasts.

Section II presents the assumptions for the forecast, Section III presents forecasts for integrated electronics in

general, Section IV provides the microcomputer forecast, Section V the memory forecast and Section VI the conclusions of the hardware technological forecast.

II. Assumptions for Unconstrained Technology Forecasts

There are several broad assumptions on which the unconstrained forecasts rest. These are discussed as follows:

1. Electronic markets will continue to expand, providing economic motivation for new products and the continued development of technology
2. Electronics and the electronics industry will continue to be regarded as of benefit to society.
3. The electronics industry will remain diverse and competitive, with a minimum of government regulation and no market domination by any one company.
4. The development of integrated electronics continues in an evolutionary manner with no revolutionary developments to change its basic form abruptly.*
5. New, but known, technologies such as X-ray lithography are developed to permit the continued evolution of electronics. Processing materials continue to be readily available.

It is highly likely that all of these assumptions will be true, at least through the 1980's. Integrated electronics

*As will be discussed in Volume II, Chapter Two, optical computing is expected to become practical toward the Year 2000. However, the change is likely to be evolutionary. A hybrid of optical and solid-state electronic hardware, rather than purely optical computing, will be the most advanced basic form of computers at the beginning of the next century.

is just beginning to penetrate the consumer market, and the cost effectiveness of electronic control is causing its adoption in many formerly non-electronic industries (e.g., in the automobile). This growth in electronic markets will likely continue at an increasing pace. If computer automation became widely regarded as a threat to the job market or if government regulation in operating practices (safety, pollution, etc.) became excessive, the pace of development could be slowed. Both are unlikely, and electronics at present is certainly one of the cleanest (and safest) industries.

One of the reasons for the rapid pace of technology is the fierce competition between companies in the industry. The continued prominence of a variety of companies, competing for the market, is essential to the continued growth of the industry. Domination by any one company or removal of any major part of the industry from the private sector could seriously slow progress. These developments are regarded as possible but unlikely.

Integrated electronics has been evolving for more than ten years. New techniques and device structures have been developed but no radical and fundamental discoveries have occurred to change the development of the technology. Since radical, new developments can only be conjectured, but cannot be forecast, the assumption of continued technological evolution is made. Non-electronic discoveries appear

unlikely to alter the development of electronics, and new discoveries in electronic materials would only speed the development of technology beyond that forecast. It is assumed that supporting techniques such as submicron lithography will be widely available for production by the mid-80's or before, and that materials continue to be available as needed in device processing.

In forecasting future developments in semiconductor electronics, it is important to recognize that this is still a very young and extremely dynamic industry. Integrated circuits are only about 15 years old, and the growth rate at present makes forecasts difficult. Beyond 1990, it is possible that radically new approaches (beyond optical computing) which have not been conceived today will be developed. Therefore, the forecasts presented here are probably conservative for the 1990's and, possibly, for the 1980's as well.

A. Assumed Developments in Present Silicon LSI Technologies

1. Low Power Schottky Transistor-Transistor Logic (LSTTL)

Developed about 1970, this technology offers the best present performance for high speed (5 nsec propagation delay) digital systems. As other bipolar and MOS technologies develop and achieve faster speeds, the use of LSTTL in LSI will decrease. The best features of the technology (Schottsky diodes, dielectric sidewall isolation, walled emitters, etc.) will be adopted by other device structures having lower power levels and allowing denser LSI structures.

The use of LSTTL, as it is now known, is not likely for LSI beyond 1980.

2. Integrated Injection Logic (I^2L)

Integrated injection logic, developed during the early 1970's and still evolving, will become a major factor in dense, high-speed circuits, continuing the speed-density race with MOS. It will be a major factor in replacing LSTTL. The most important feature of I^2L is its departure from discrete circuit concepts through the use of merged device structures. The merged device approach will continue, providing significant increases in density for both bipolar and MOS. Non-binary logic using merged device structures is being explored using I^2L structures now [13], and if successful could increase the effective density and speed of arithmetic functions by orders of magnitude by the mid 1980's.

3. P-channel MOS Technology (pMOS)

This technology, developed around 1965, is the simplest of the LSI technologies and was used for the first microprocessor in 1971. It exhibits high yield and low cost but also a relatively high power per gate and low speed. In 1976 it is being used only in applications where lowest cost is essential, and it is not expected to be used in LSI designs in the post-1978 period.

4. N-channel MOS Technology (nMOS)

This technology has a basic speed advantage over pMOS due to the higher mobility of electrons in the silicon lattice as compared with holes. The lower threshold also permits higher speed but requires greater cleanliness in processing than does pMOS. N-channel (nMOS) is the most widely used technology for microprocessors and will continue as a major LSI technology well into the 1980's. As device size decreases and thresholds are reduced, speed will increase and power will decrease. There is probably an order of magnitude in speed and two orders of magnitude in density remaining in the technology as now known. Two variations of n-channel technology known to produce higher speed or density which are now being developed deserve special mention:

a. Short-Channel Structures (DMOS and VMOS)

During the 1971-74 period, two structures were developed which are beginning to see application in production circuits. Both structures allow submicron channel lengths to be realized using masking line widths of 5 to 10 μm . DMOS [44] is a lateral MOS structure consisting of a two-part channel region. A normally-on (depletion type) channel is in series with a submicron

normally-off channel which controls device speed. The submicron channel is realized as the distance between successive p-type and n-type diffusions as in the formation of a bipolar device. Propagation delays less than 500 psec have been obtained in DMOS logic. VMOS is similar to DMOS except that current flow is vertical rather than lateral to the plane of the wafer. An anisotropically etched slot is cut through the p- and the n-diffusions so that the junction is exposed to the gate contact. This results in higher conductance for the same device area although the source in present structures is constrained to be the common substrate.

Both DMOS and VMOS offer enhanced speed through their short channel lengths. As such, they can be expected to permit the early introduction of high-speed MOS circuits in the late 1970's and early 1980's. With the application of electron-beam lithographic techniques in production by the mid 1980's, their subsequent use is less certain in high speed LSI.

b. Charge-Transfer Devices (CCDs and BBDs)

Charge-transfer devices [2, 3, 4] in the form of charge-coupled devices (CCDs) and

bucket-brigade devices (BBDs) made their appearance about 1970. They are being developed for three application areas: imaging, analog signal processing, and memory. The last area is the most significant for this study, and CCD memories, operating as line addressed or block addressed serial stores, are approximately four times as dense as nMOS RAM. Serial CCD devices at the 64 K-bit/chip level are expected in 1977. CCD structures will continue to be important for serial bulk storage, replacing drum and disc memories, and may well evolve into structures for high density RAM as well.

5. Complementary MOS (CMOS)

As a logic technology, CMOS has many advantages, including low power, moderately high speed, and a high immunity to environmental conditions (noise pickup, power supply variations, temperature, etc.). Its principal disadvantage has been the relatively large area required per gate. Gate areas have been decreasing rapidly, however, and dynamic clocked-CMOS (C^2 MOS) has been further increasing the functional densities which can be achieved[34]. As technology evolves, the significance of the density penalty in CMOS may be reduced. The degree with which this technology will succeed in LSI will

depend on demand for it in the marketplace. If adopted by, for example, the automotive industry, the economic incentive to develop it fully would be present.

III. Unconstrained Technology Forecasts for Integrated Electronics

Section II has reviewed the historical development of semiconductor technology and the present state of the art. Factors contributing to cost, reliability, power, and speed were discussed, and the assumptions on which the forecasts rest were delineated. Finally, short comparative forecasts were given for each of the major technologies for present large scale integration. In this section forecasts for cost, speed, power, and reliability will be given. The first three parameters will be treated at the gate level, while reliabilities will refer to the entire LSI chip. In dealing with cost, 1975 dollars are used throughout this report. The parameters are forecast in terms of the performance achievable with any LSI technology since in terms of the user, the technology is relatively unimportant except in terms of the performance levels achieved.

A. Cost Per Packaged Gate (1970-2000)

Over the past decade, the binary logic gate has been the basic building block of digital circuits. As density has increased, gates have become increasingly difficult to identify physically, but have remained the basic circuit entity. The cost per packaged gate is related

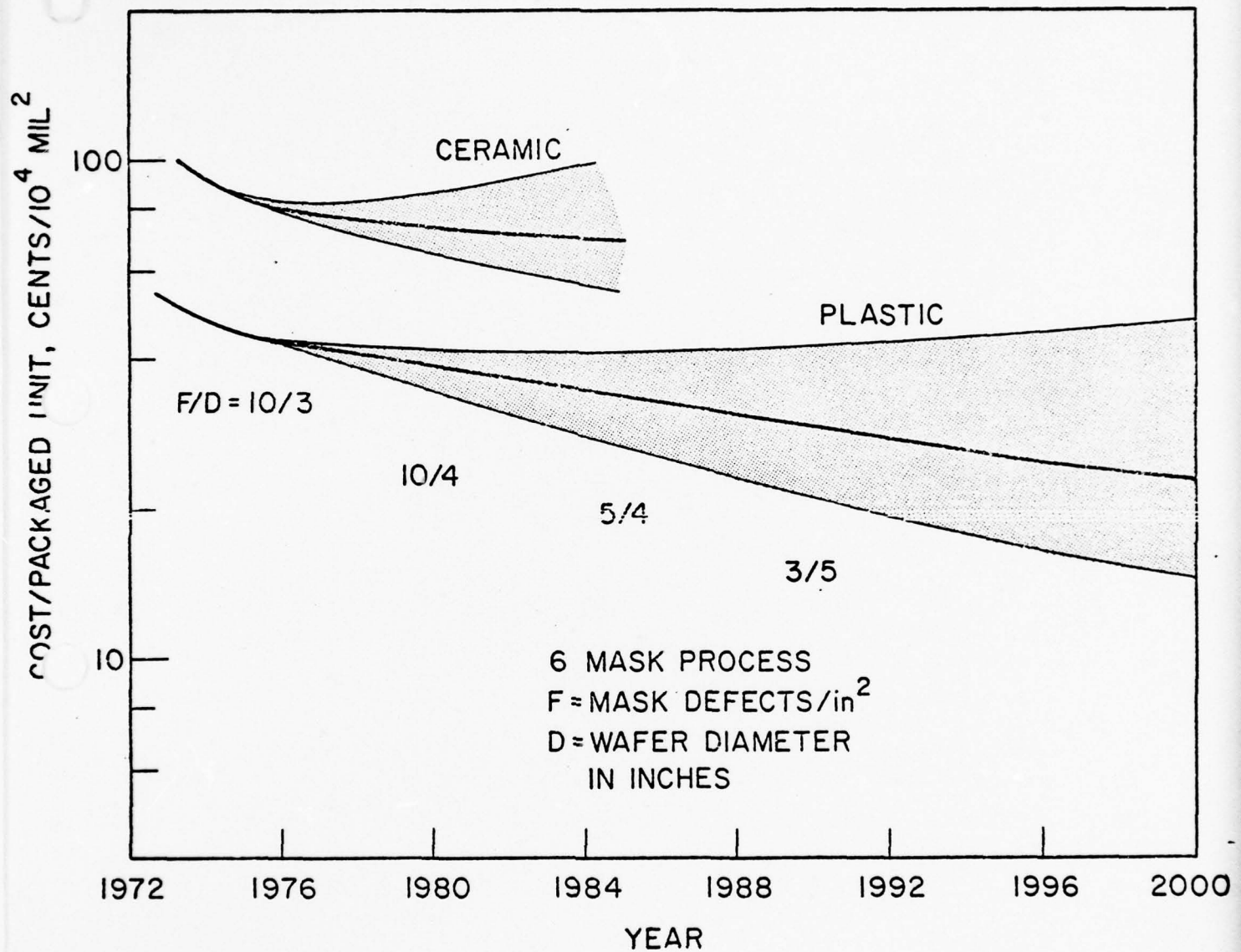
to the cost per circuit (or per unit silicon area) as well as the gate size and density. These two parameters are forecast separately and then taken together to form the cost per packaged gate. It is assumed that the system to be integrated is large enough that optimum chip sizes (lowest cost per unit area) can be used.

1. Packaged Circuit Cost Vs. Time (Figure 8)

The cost of a packaged circuit is composed of the cost of the processed die (silicon), the testing cost and the cost of encapsulation and packaging.

Die Cost: For a given die size, die cost is expected to decline slowly in the future, partly due to increased wafer sizes. It is assumed that the chip die size is at the most cost effective point and that this size will increase from 20K square mils (1975) to 35K square mils (1980) and to at least 80K square mils in 1990. The cost of fabricating a wafer will decrease due to increased process automation but will increase due to rising labor costs and more expensive equipment and supplies. Wafer process cost will increase from \$30 in 1975 to \$35 in 1980 and \$50 in 1990. Wafer size will increase from 3 inches (1975) to 4 inches (1980) and 5 inches by 1990. The use of improved masks, projection printing, and later, X-ray lithography will reduce defect densities, maintaining yield in the 20 to 30 percent range and allowing the cost per unit area of

FIGURE 8: FORECAST OF PACKAGED CIRCUIT COST



processed silicon to decrease from about 13 cents (per 10K square mils) in 1975 to 9 cents in 1990. The mask defect density/wafer diameter (F/O) ratio in Figure 8 shows the reduction in mask defects per square inch as wafer diameter increases overtime.

Testing Cost: Increased testing automation and the inclusion of diagnostic circuitry on the chip will only partially offset the increased cost of testing an increasingly complex die. An increase in testing cost from 30 cents (1975) to 54 cents (1985) and 75 cents (1990) is forecast for RAM. The testing cost for more complex units (e.g., microcomputers) will be somewhat higher.

Packaging Cost: Automated die attach and lead attach will become widespread by the early 1980's causing a drop in this component of packaging cost. Further reductions will be difficult and prices will subsequently rise due to increasing materials and tooling costs. Package materials will increase in cost, especially precious metals. Improvements in package forming will act to balance some of the increases in materials costs. Improved plastics and molding techniques will permit increased use of plastic packages with a shift from metal-lid ceramic to plastic and "cerdip" packages. Plastic packaging costs will

increase from 15 cents (1975) to 24 cents (1985) and will rise to 35 cents by 1990 as package size continues to grow.

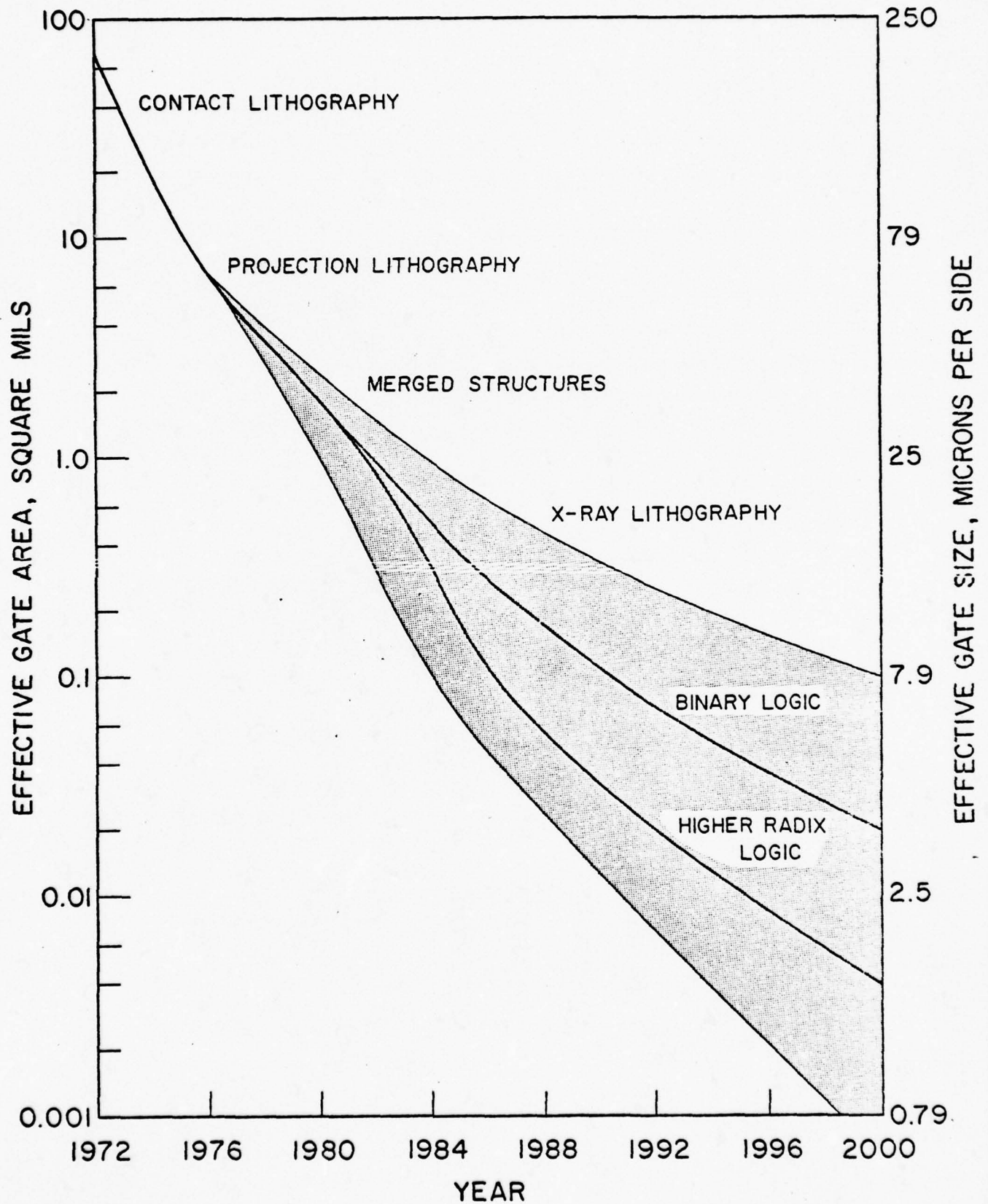
The cost per 10K square mils of processed, packaged silicon is expected to decline slowly from 44 cents (1975) to 28 cents in 1990. As was the case from 1965 to 1975, the most dramatic reductions in cost perfunction will come from increased functional density and larger chip size.

2. Gate Density Vs. Time (Figure 9)

The density of gates is dependent on lithographic dimensions, device structure, and operating depletion layer thicknesses in the substrate material. Production line widths have gradually decreased from 10-12 μm in the late 1960's to 5-6 μm in the mid 1970's. Hard contact printing has given way to soft contact systems and scanning projection printing is gaining rapidly in commercial acceptance. Lower defect densities and longer mask life permit higher quality masks to be used, and line widths are expected to decrease to 3-4 μm by 1980. Electron-beam and X-ray systems for device lithography are both under exploratory development and by 1985 should reduce production line widths to 1-1.5 μm .

The use of merged device structures and an emphasis on basic charge transport in the silicon crystal will increase throughout the next decade. This trend will

FIGURE 9: FORECAST OF GATE DENSITY



continue to reduce gate size through changes in device structure, with factors 20-30 percent per year in increased gate density through 1982, and about half subsequently from this source. New modes of submicron device operation may well continue the evolution in device structure into the mid 80's and 90's. A reduction in lithographic dimensions permits a corresponding reduction in device size only so long as depletion layer widths can also be reduced in size. These layer thicknesses depend on doping levels and operating voltage levels. The increased use of ion implantation for selectively doping the substrate to allow reduced operating voltage and narrower depletion layer thicknesses will be of increasing importance. By the late 1980's, we should be approaching the limits on device size as defined by Hoeneisen and Mead [24, 25].

The focus on the binary gate as the basic circuit building block may not be appropriate after the early 80's. Charge transfer devices are now handling analog signals with very low loss and dispersion, and the use of non-binary logic or discrete-analog signal processing is not out of the question by the mid 1980's. There are diverse opinions on this in the industry now, but at least one company is nearing production on four-level logic structures [15]. In a

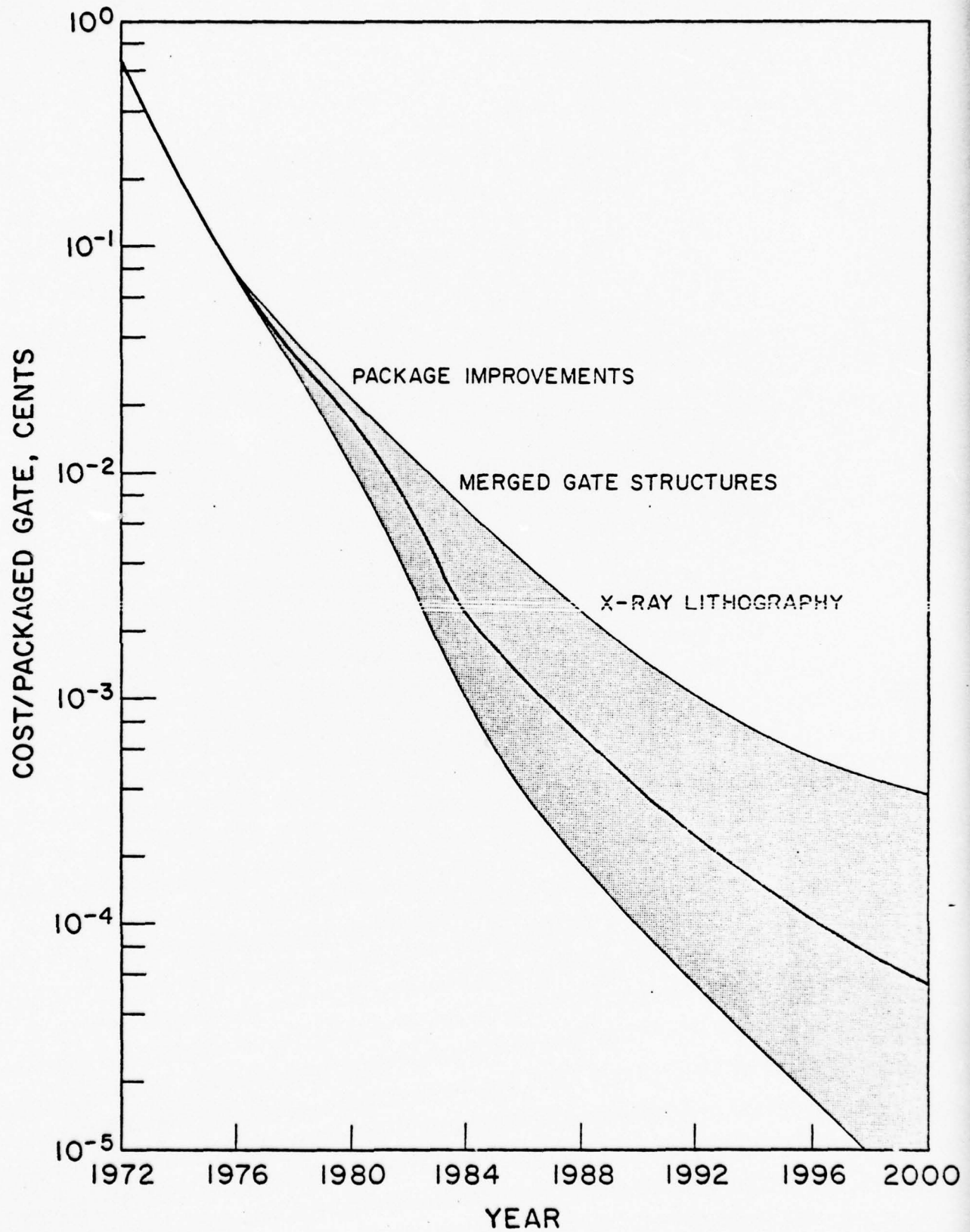
large machine, this could result in a significant improvement in effective gate density. By the mid 80's such improvements due to higher radix (non-binary) structures are expected.

Figure 9 shows gate area versus time. An area penalty of 50 percent is assumed for lead routing. In 1975 we were fabricating logic structures with 5-10 square mils per gate. As seen in the figure, improvements in gate density are expected to continue, with effective gate area shrinking to about 2 square mils in 1980, and 0.1 square mils by the early 1990's. Gate structures are still several microns on a side, well above any basic limit. Certainly, the problem of what to put on the chip will soon be more significant in most cases than how to do it. An expanding market in very large (by present standards) electronic systems is important in achieving the forecast levels.

3. Cost Per Packaged Gate Vs. Time (Figure 10)

Taking Figures 8 and 9, the cost per packaged gate is shown as a function of time in Figure 10. The constant or slowly falling cost of packaged silicon combined with the dramatic decreases in gate area, results in further dramatic cost reductions on a per gate basis for future LSI systems. While cost per chip will remain relatively constant and even increase somewhat as chip size increases, the functional complexity

FIGURE 10: FORECAST OF COST PER PACKAGED GATE



(gates/chip) can be expected to increase in accordance with Figure 9. This has enormous implications on the cost, size, and sophistication of future data processing.

B. Reliability

Present reliability levels on LSI components, including the 8080 microprocessor, are about 99.95 percent per 1000 hours at 90 percent confidence level and 70°C. The reliability of any LSI part improves significantly during the first two or three years of production as failure mechanisms are identified and eliminated. As component complexity increases new failure modes will undoubtedly arise and subsequently be corrected. Narrower line widths will require lower currents to avoid metal migration; however, device operating currents are expected to remain well below the critical levels. Little change in component reliability is seen below the 99.99 percent per 1000 hour levels (90 percent confidence, 70°C) which will be achieved by 1980. Extensive and special testing programs might do somewhat better but at greatly added expense. With increases in component complexity, however, these reliability levels are of great significance in future LSI circuits. Stated a different way, if we look at a computer such as the PDP-10, with about 10^4 gates, in LSI technology of the mid 80's, 90 percent of such machines would still be functioning after 1000 years

of operation at 70°C. Again, this level of reliability is possible during the 80's, assuming the component has been in production for several years and that extrapolations based on accelerated testing are accurate. These reliability levels are satisfactory for most applications. In situations where failures cannot be tolerated, redundancy will be used. Some fault detecting/correcting circuits will be built into the LSI circuits of the 80's.

Soft failure mechanisms (temperature effects, pattern sensitivity, requirements on power supply regulation, etc.) and operating limitations will continue to complicate the testing problem. It is doubtful that any significant changes will occur in the operating temperature range of LSI circuits. As densities increase and operating current levels and node capacities decrease, the high temperature operating limit may be difficult to maintain and could decrease. Low temperature limits are less of a problem, partly due to the heat generated by the circuit itself. As MOS thresholds are reduced and shallower device structures are used, it is also likely that operating voltage ranges will be reduced. The tightening of these operating temperature and voltage ranges should have little effect on ground-based data processing applications, but could complicate the

sensor/actuator interface in instrumentation and control applications. Sensors are discussed in a subsequent section.

C. Speed and Power in LSI Circuits

The dramatic increase in gate density forecast in Figure 9 will be possible only if accompanied by a comparable decrease in the power per gate. Package limitations are expected to continue to limit the power dissipation per package to a few watts. As gate area decreases, the node capacitance in logic arrays will decrease similarly. At a constant rate, the power will drop on a per gate basis but remain relatively constant per unit area. In MOS, from one to two orders of magnitude in power exist before package limitations will force on-chip power gating or limit development. Hence, to a large extent, there are two orders of magnitude improvement in speed possible as sizes decrease. Decreased operating voltages should roughly compensate for larger chip areas. In I^2L , an order of magnitude or less in power exists before power gating is required although a significant speed advantage over MOS already exists. However, as power is traded for speed, the base transit time, which is largely independent of power, may become limiting. Another order of magnitude in speed is probably possible before transit time delays slow further progress in silicon. Therefore, both MOS

and bipolar technologies are expected to mirror improvements in gate area with improved speed down to levels of about 0.5 nsec/gate and then become relatively more constant with time. Power per unit area is being traded here for speed per gate. Figures 11 and 12 show the expected power per gate at constant speed and speed (delay) per gate at constant power versus time.

Much progress has been made recently in logic based on new materials and effects. Gallium arsenide logic gates have exhibited delays less than 0.1 nsec and Josephson junction devices have shown delays less than 0.2 nsec with power-delay products of 0.004 pJ [27, 28]. It is unlikely that there will be sufficient motivation to apply these devices in LSI before 1990, although applications in high speed interface circuits are likely during the 1980's. During the 1990's their use is likely in extending the performance of LSI systems below 0.5 nsec.

IV. Unconstrained Microcomputer Forecasts

The general capabilities of future integrated electronics were forecast in the last section in terms of cost, reliability, speed, and power. In this section we will examine the application of this technology to microcomputers, forecasting parameters such as cost, speed (instruction cycle), word length, power, and reliability. The distinction between

FIGURE 11: FORECAST OF POWER PER GATE AT CONSTANT SPEED

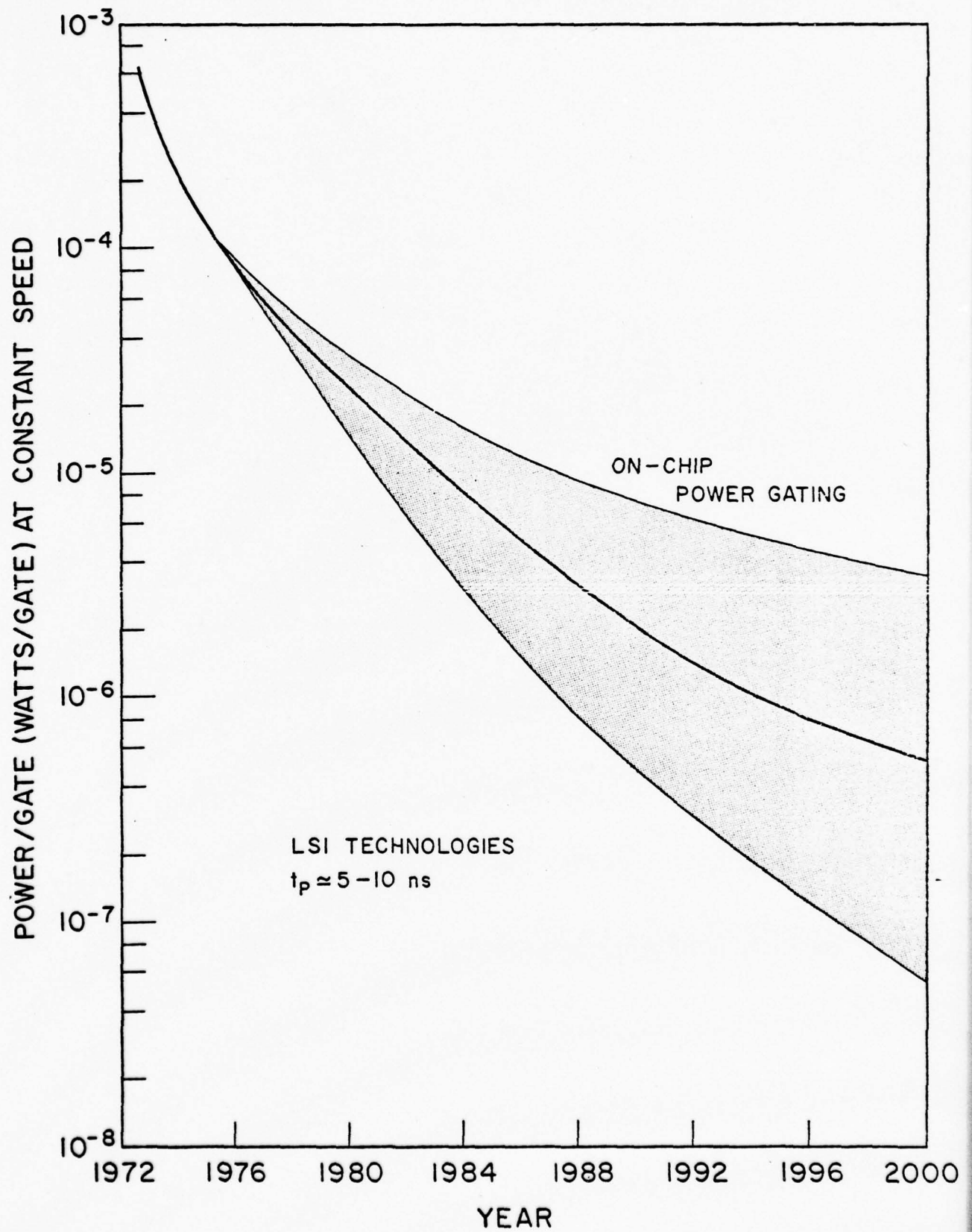
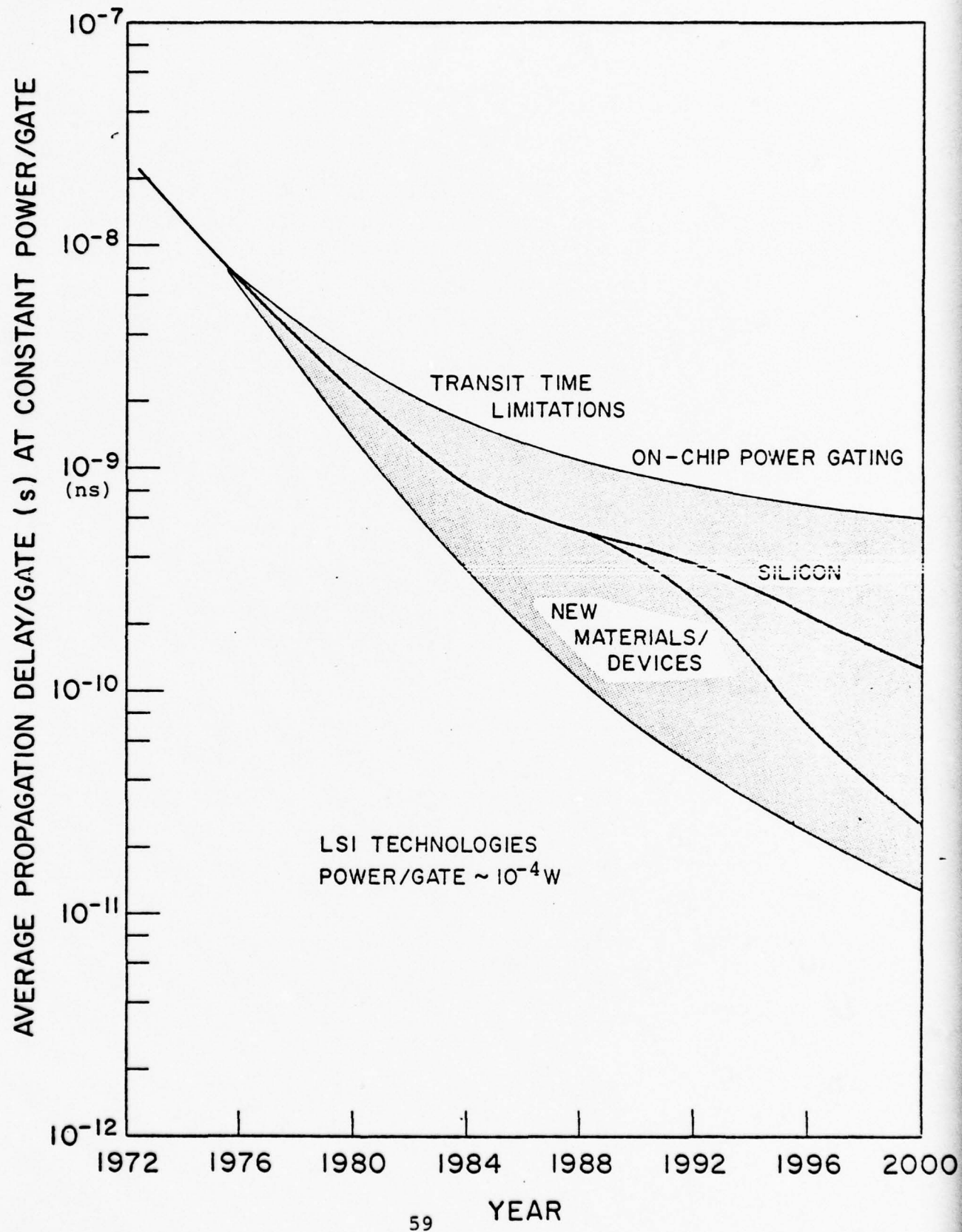


FIGURE 12: FORECAST OF SPEED PER GATE AT CONSTANT POWER



microcomputers and minicomputers is expected to become increasingly difficult. In general, microcomputers will consist of one or a few LSI chips, have limited I/O, and will be applied primarily in dedicated applications. Minicomputers will have more flexible I/O, will be general purpose in nature, but will be built around microcomputers (or possibly networks of them). In terms of performance, microcomputers will soon replace present minicomputers, while minicomputers will replace present macrocomputers. For example, the PDP-8 CPU is now available on a single chip and larger computers, such as the PDP-11, are expected to follow suit.

There are two classes of microcomputer applications: data processing, and control/instrumentation. Since the latter will constitute a majority of the airborne applications, it is appropriate to define the components of a microcomputer-based control system briefly before discussing specific forecasts.

Figure 13 shows a typical control system which interacts with the aircraft via the sensors and actuators shown. Both digital-output sensors (event-type, pulse-rate encoded, etc.) and analog-output sensors are shown. The analog sensors interface to the processor via an analog multiplexer (MUX) and analog-to-digital converter (ADC) while the digital sensors interface through level-shifting buffers and counters. Similarly, the actuators are driven by digital-to-analog converters (DAC) and demultiplexers as shown. The control

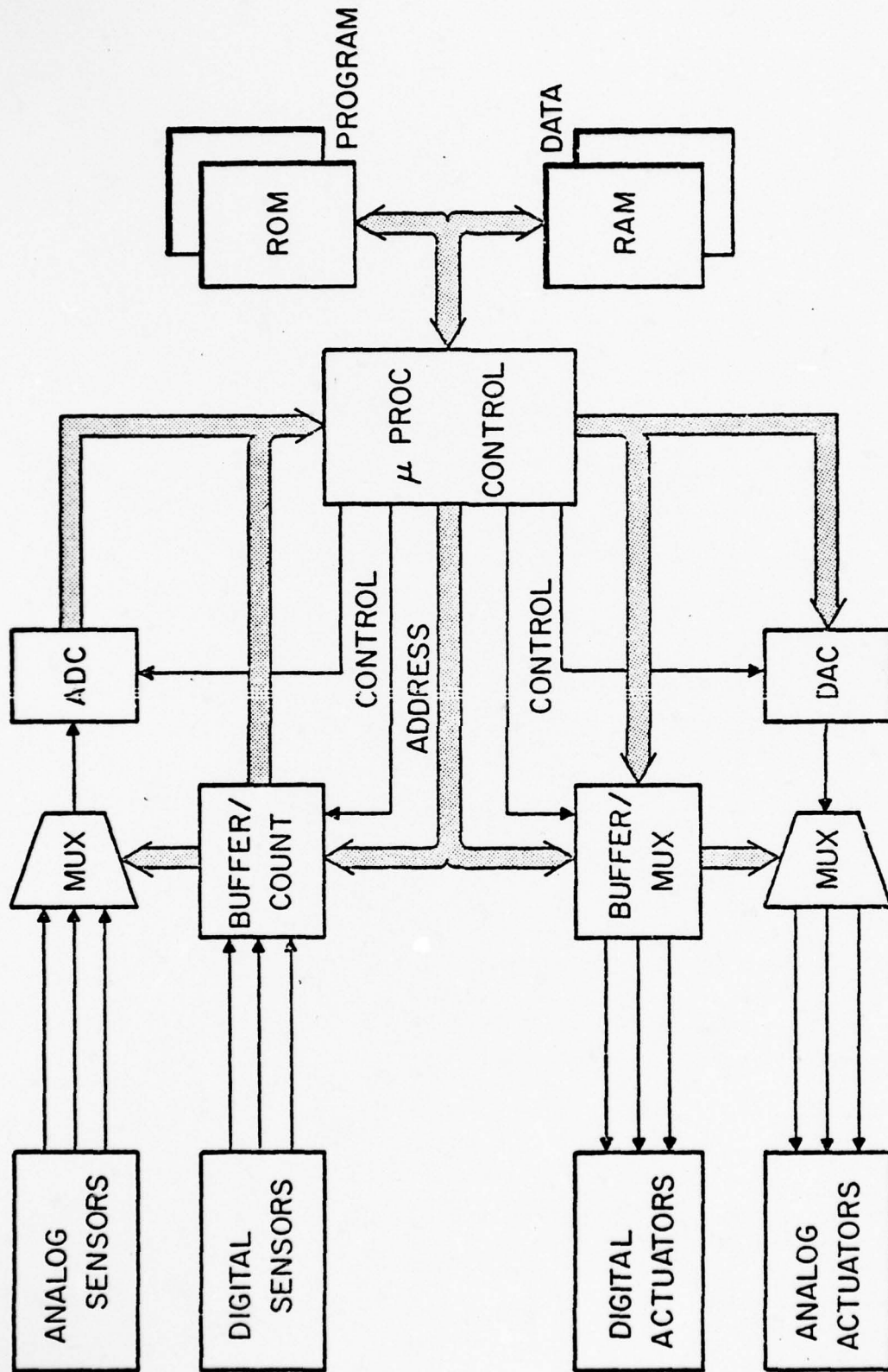


FIGURE 13: ELECTRONIC CONTROL SYSTEM

logic consists of one or more microprocessors whose operation is controlled by a program of instructions stored in read-only memory (ROM) and which uses random access memory (RAM) for temporary storage of data. The processor samples the sensor outputs periodically or on demand, interpreting the results, and modifying the aircraft operation as needed through the actuators.

The block diagram of a typical microprocessor is shown in Figure 14. An instruction cycle is composed of several clock periods during which the processor transmits the address of the next instruction from the program counter to memory, receives the instruction from memory, decodes it, and finally executes the instruction using the Arithmetic Logic Unit (ALU) to perform computations on the binary data. More than two-dozen different microprocessors are now available [27] with word lengths of 4, 8, 12 and 16 bits. Most recognize 50 to 100 different instructions and contain several thousand transistors.

Table 2 of the previous chapter showed typical instruction cycles and power levels for present processors. One to three instruction cycles are typically required to specify a sensor and read its data into the accumulator for subsequent processing. Many sophisticated control operations can be handled with less than 1000 instructions.

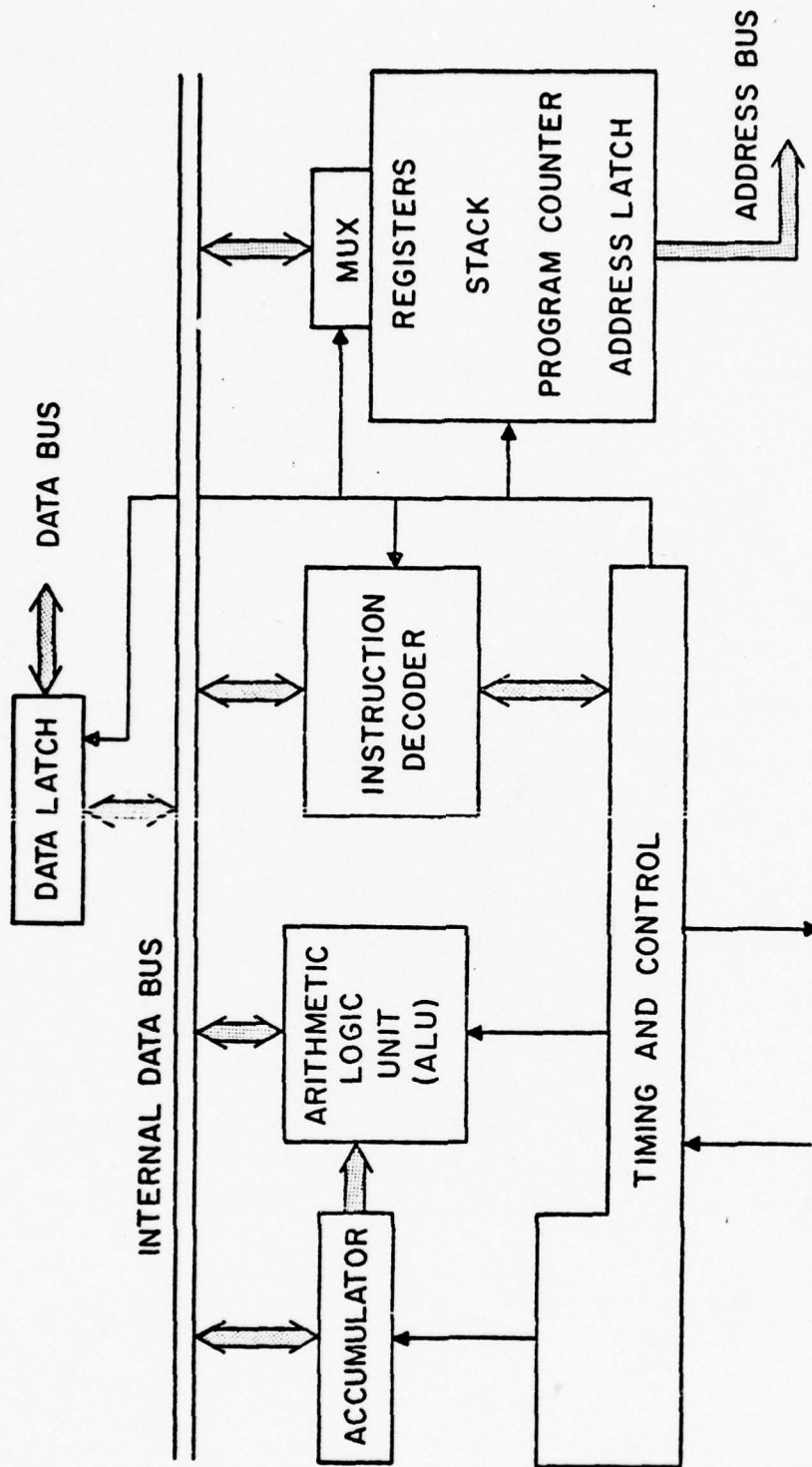
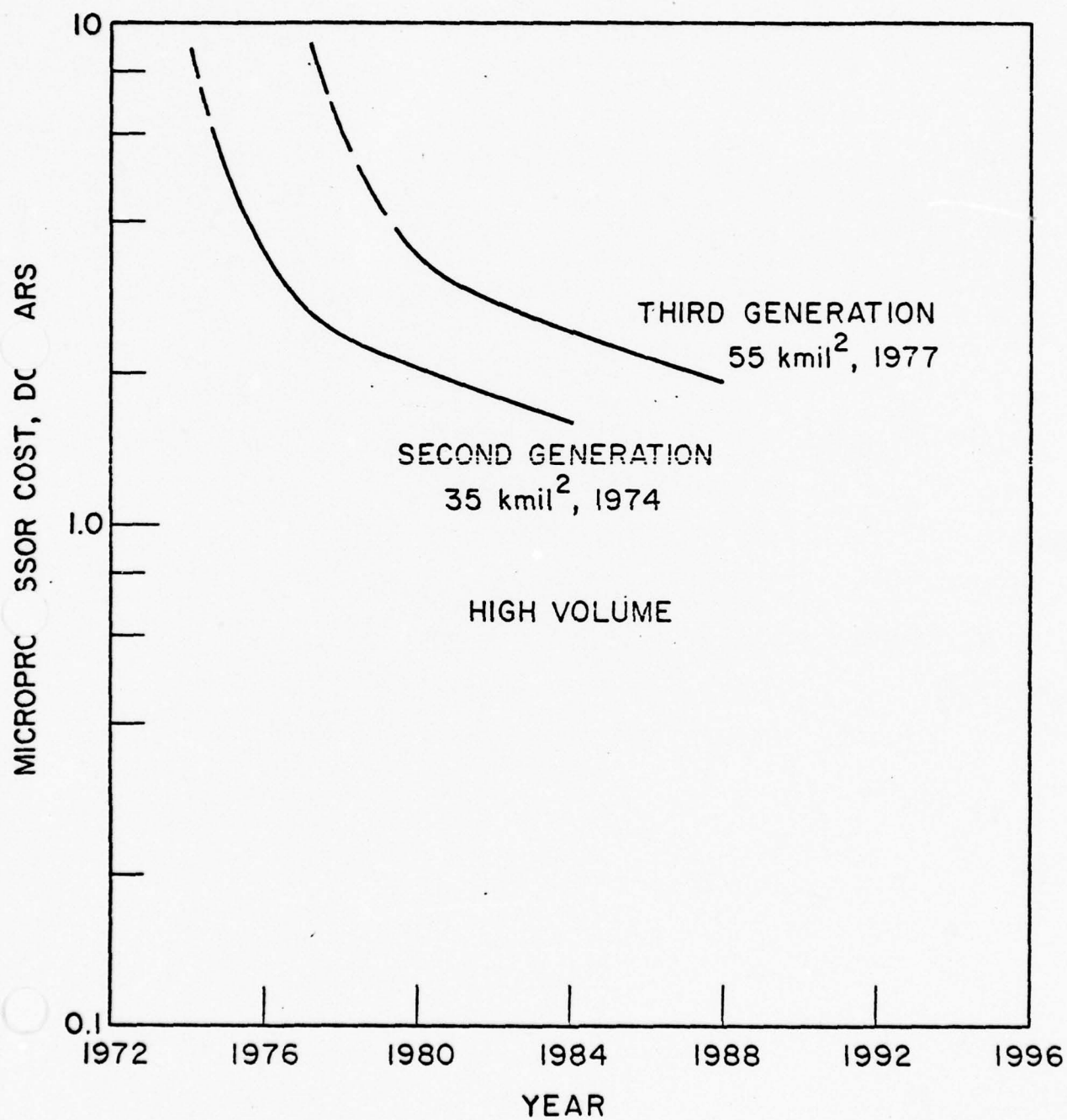


FIGURE 14: BLOCK DIAGRAM OF TYPICAL MICROPROCESSOR

A. Microcomputer Cost

Most first- and second-generator microprocessors are in the 30K to 40K square mil range in chip area. Third generation designs, containing significant amounts of memory on-chip (e.g., microcomputers with 8K bits of ROM and 1K bits of RAM) are expected in the 1977-78 time frame with chip sizes in the range of 50K to 60K square mils. Given at least three years in production so that mask limited yields are approached and by 1980 such microcomputers should exhibit a high volume price of less than four dollars. By 1985, with an improved plastic package, the same processor in high volume (excluding marketing and distribution costs) should be near two dollars. Figure 15 summarizes the objective cost of such a third-generation microcomputer versus time. The time duration of these curves reflects an expected production life of about ten years for these microcomputers. It is clear that the low cost of these elements can have enormous impact, particularly in entirely new areas, e.g., performance computers, automation of maintenance, etc. The cost of a packaged electronic system will increasingly reside in the chassis, I/O connectors, and those portions of the system which do not use high-volume digital components. Although the packaged system cost may continue to exceed the LSI DIP cost by one to two orders of magnitude, the system cost will nonetheless drop significantly by virtue of reduced chassis size.

FIGURE 15: FORECAST OF COST OF THIRD-GENERATION MICROCOMPUTER



The low cost of digital LSI microcomputers requires that new design and organizational concepts be developed for next generation systems. Emphasis on the minimization of custom circuits and the development of microprocessor-compatible sensors will be important for instrumentation. The use of a microcomputer to save system interconnect wiring cost through sophisticated multiplexing arrangements is certainly increasingly feasible.

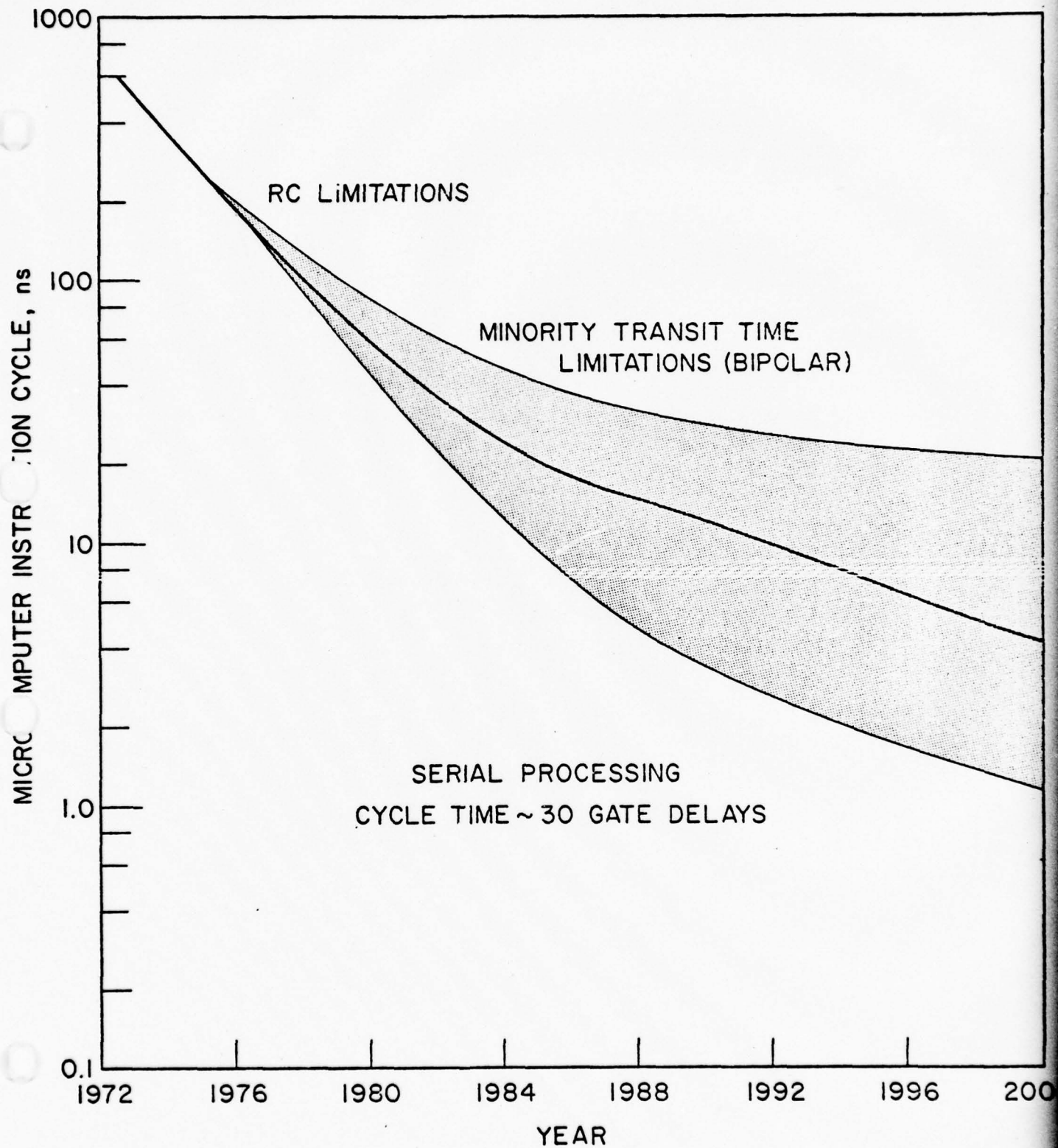
B. Microcomputer Speed (Instruction Cycle)

The instruction cycle (register-register add time) of a microprocessor is typically composed of several clock periods, each of which is several logic delays long. The resulting cycle time is typically 20 to 40 times the individual gate delay for a serial processor. Figure 16 shows the instruction cycle time forecast versus time. In the near term the indicated speeds will be attained only with bipolar technologies; however, by the mid 80's, MOS technology could match or exceed the bipolar approach. By 1980, processors with cycle times less than 100 nsec should be achievable, while by 1985, this could drop to 20 nsec or less. The results of parallel processing architectures are mentioned in a later section.

C. Microcomputer Word Length

The first microprocessor, available in 1972, was a 4-bit machine. It was quickly followed by an 8-bit machine and in 1976, microprocessors were available with word

FIGURE 16: FORECAST OF INSTRUCTION CYCLE TIME

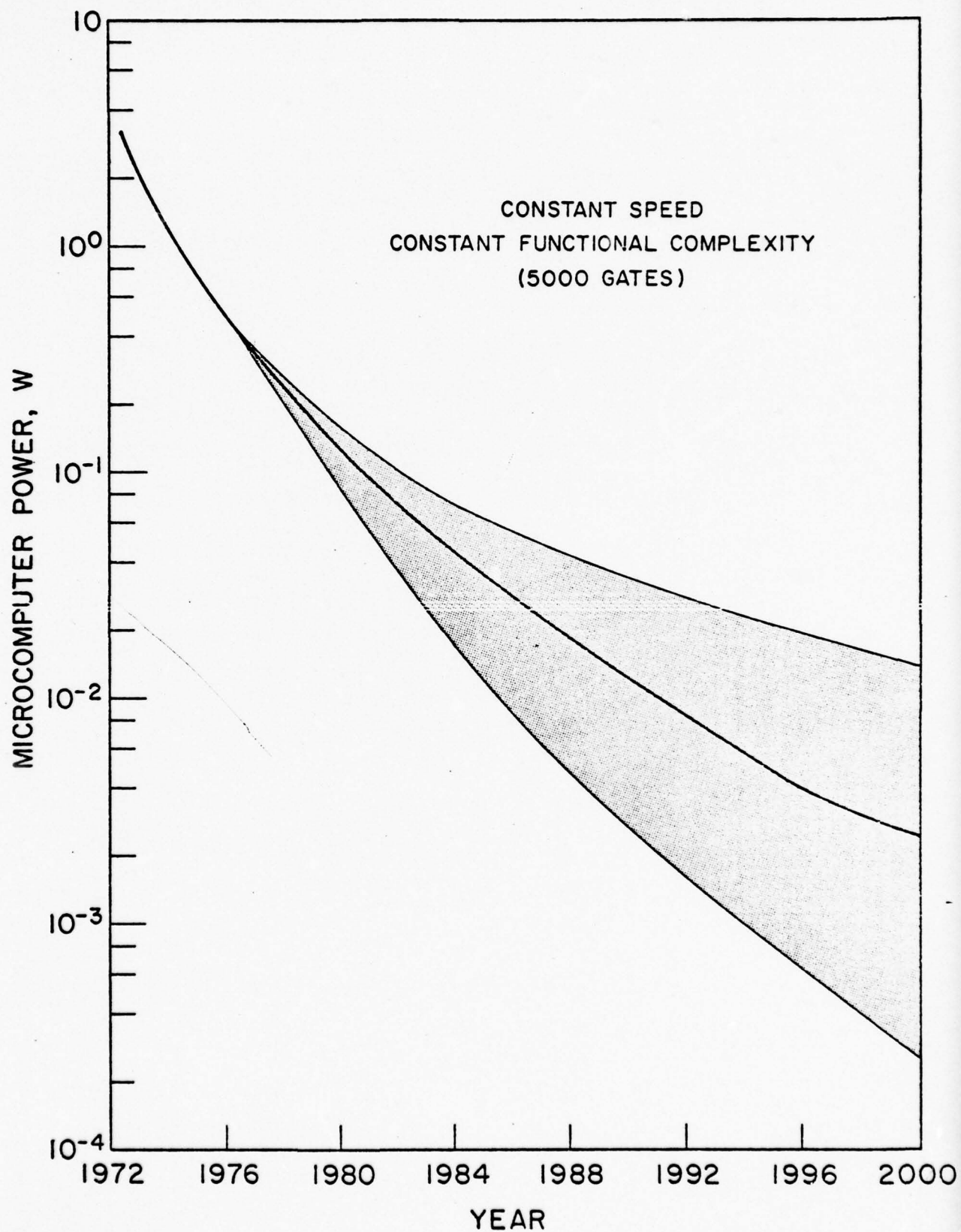


lengths of 4, 8, 12 and 16 bits. There does not appear to be strong motivation in the industry to develop longer word lengths, but by the early 1980's, machines having 32-bit word lengths should be available. Longer word lengths are doubtful, except possibly by paralleling chips (bit slicing). Although little standardization in word length is discernable yet, some standardization on 8, 16 and 32 bits is likely by the early 80's.

D. Microcomputer Power

Microcomputer power can be expected to closely mirror power per gate for a given function at constant speed. The power for a second or third generation microcomputer having 5000 gates, each active 1/2 of the time and each biased to dissipate 0.2 mw when active is about 0.5 watts using 1976 technology. As Figure 17 shows, if we accept 1976 performance levels (i.e., speed), the power of a given microcomputer (redesigned each year to realize higher density) should have decreased an order of magnitude by 1984 and should fall another order of magnitude by the mid 1990's. Practically, this will not occur, since the life of any given product will be well under 10 years, and each new product generation will likely offer higher speed as well as lower power. Nevertheless, the power per function will drop dramatically over the next 25 years.

FIGURE 17: FORECAST OF MICROCOMPUTER POWER REQUIREMENTS



E. Microcomputer Reliability

The subject of reliability has already been discussed at the chip level, and that discussion should be applicable to future microcomputers. Reliability levels approaching 99.99 percent per 1000 hours at 90 percent confidence level and 70°C should be attained by the early 80's. Redundancy will be applied in many system applications where failures cannot be tolerated with little affect on system cost. Fault detection and even fault correction are possible microcomputer features by the mid-to-late 1980's.

V. Unconstrained Memory Forecasts

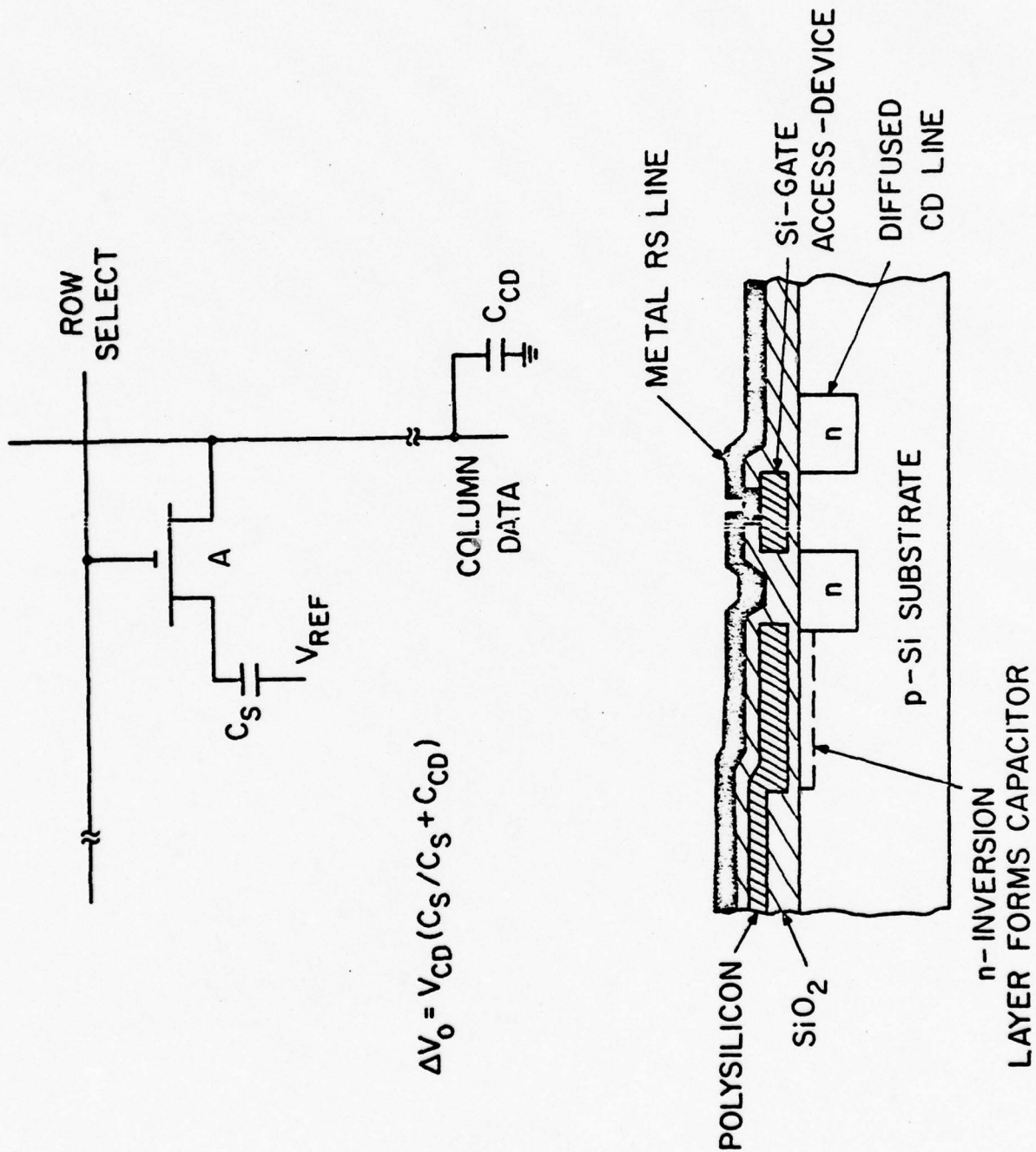
The success of microcomputers as well as their ability to evolve as forecast depends on the availability of memory which is compatible in terms of speed, power, cost, and reliability. There are several types of memory which can be considered, including random access memory (RAM), read-only memory (ROM) and electronically-alterable read-only memory (EAROM), and bulk storage devices. In this study emphasis will be placed on those memory structures which appear most closely compatible with microprocessors. Section A deals with semiconductor RAM, while B discusses read-only memory technology. The final section, C, comments on two other memory types--electron-beam addressed memories (EBAM's) and magnetic bubble memories.

A. Semiconductor Random Access Memory (RAM)

There are two basic types of RAM--static and dynamic. In a static RAM, the storage cell is a four-transistor flip-flop with an access transistor to each side. Once written, such a cell will retain data indefinitely so long as power to the chip is not interrupted. Such a memory is simple to operate but requires six transistors per bit of storage. The dynamic RAM, introduced about 1970, trades complexity in the peripheral chip circuitry for a simpler cell. The cell has evolved to a single transistor per bit design as shown in Figure 18. Information is stored on the capacitor shown. To write, the column data line is forced to the level corresponding to the information to be stored, while the row select line is pulsed, turning on the access transistor and charging (or discharging) the storage capacitor. To read, the column data line is precharged high and then left to float while the access transistor is turned on. Charge will redistribute between the column line capacitance and the storage cell, and the voltage on the column line will drop if a low level has been stored in the cell (C_S). The voltage excursion on the column data line is the precharge level times the ratio of C_S to C_D .

$$\Delta V_O = V_{CD} \frac{C_S}{C_D} .$$

FIGURE 18: DYNAMIC RAM STORAGE CELL



4030 - TYPE IX-1Y CELL

As the cell array becomes more dense and column length expands, C_S decreases while C_D increases so that the voltage available for detection decreases. Thus, sensitive differential sense amplifiers are important for larger RAMs.

The complete memory chip is shown in Figure 19. An address is presented to the chip along with chip select and read/write control signals. All address decoding and critical timing operations are performed on-chip as shown. From the terminals, the chip appears much like the static RAM with one exception. Since information storage is in the form of charge on a capacitor, the retention time for data is finite in the face of leakage from the storage node. As a result, normal memory operation must be interrupted periodically for a refresh cycle, in which all of the storage locations are read and rewritten to renew the stored charge. The refresh period is of the order of one percent of real time. Since any read operation is destructive of the stored charge, a read is normally followed by a write of the same data.

Figure 20 shows the number of bits per chip of memory as a function of time during this decade. Static RAM has remained about a factor of four less dense than dynamic RAM due to the larger cell required. Dynamic

FIGURE 19:

MEMORY CHIP ORGANIZATION

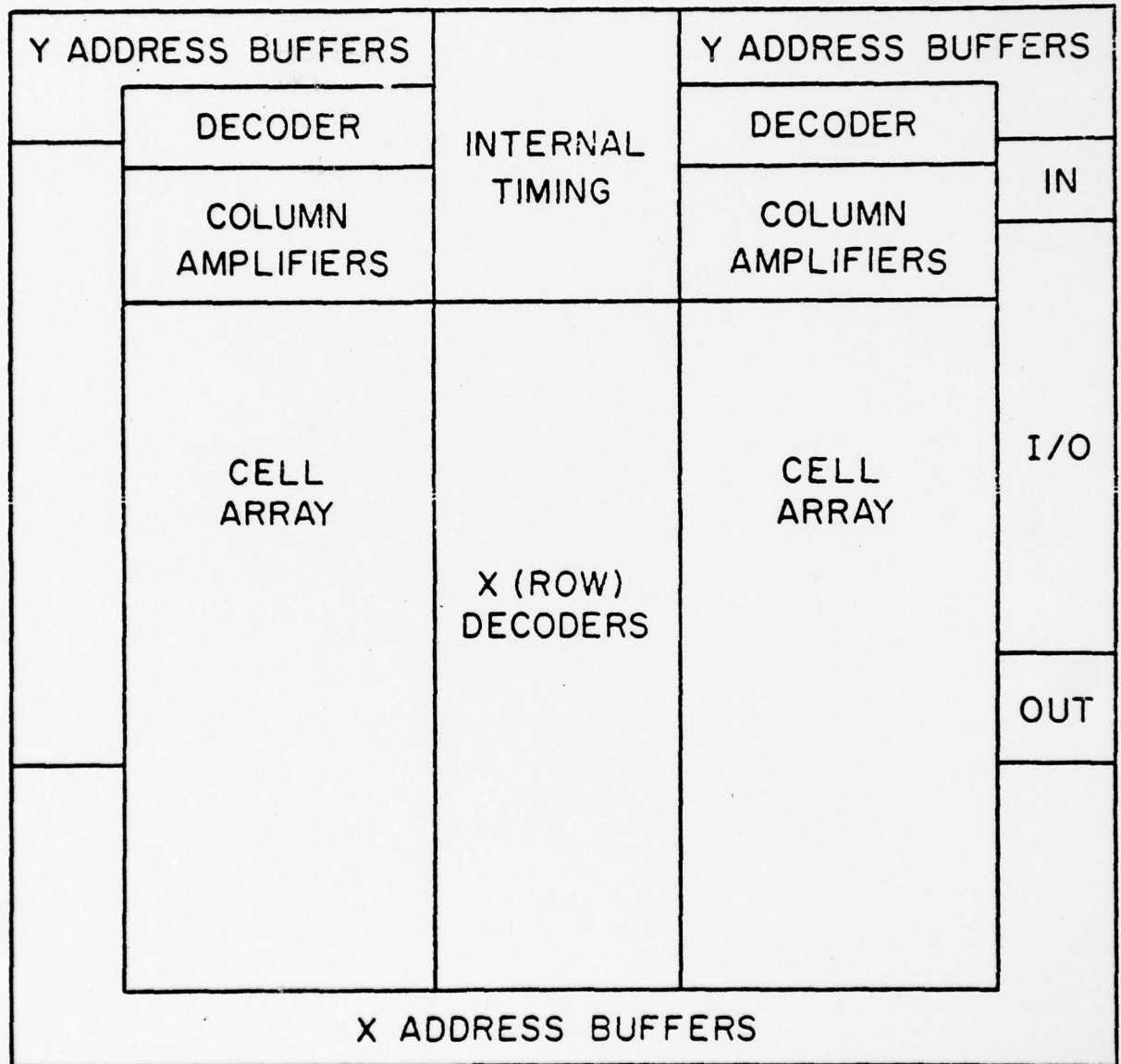
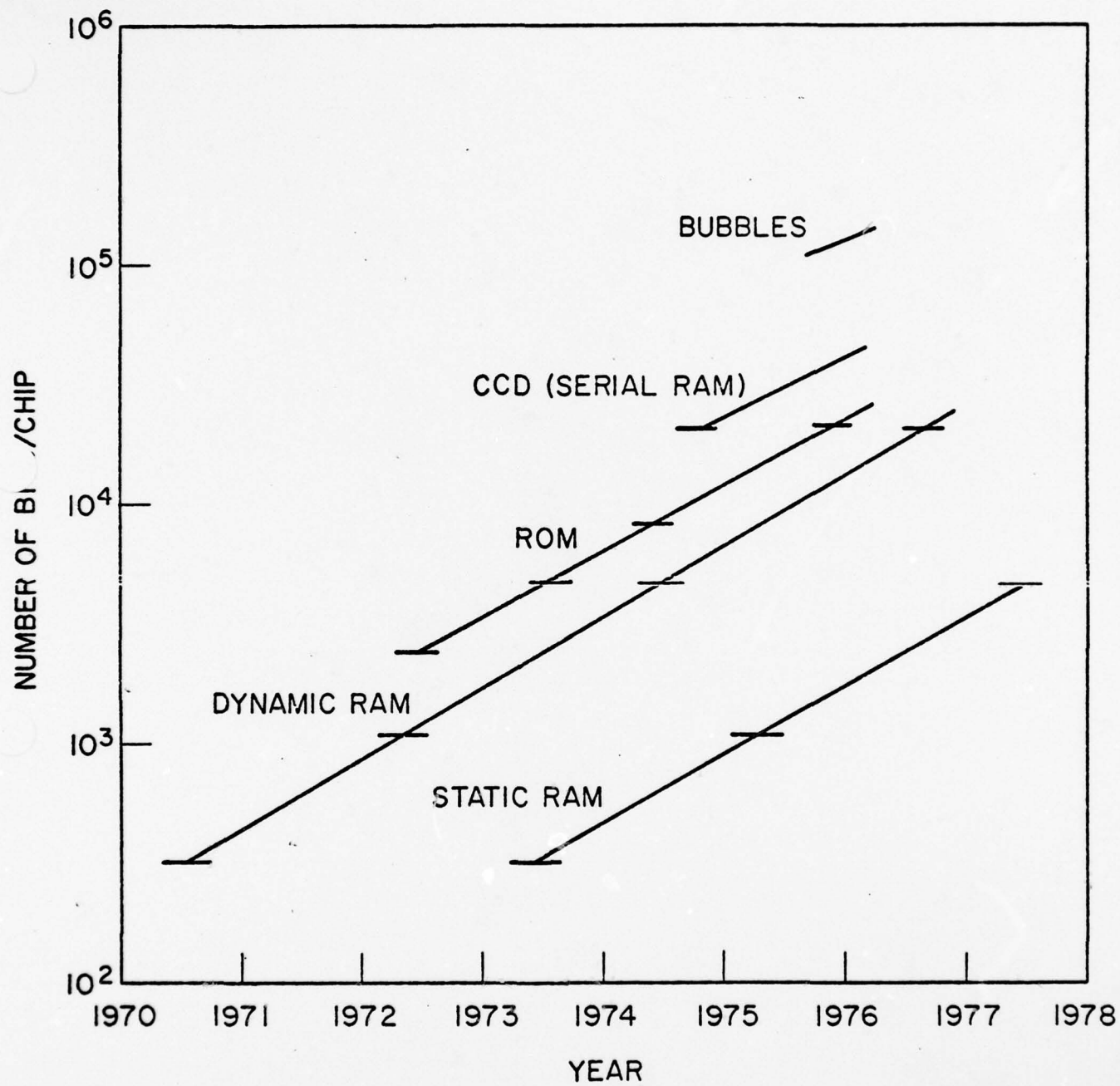


FIGURE 20: NUMBER OF BITS PER CHIP OF MEMORY IN THE 1970'S



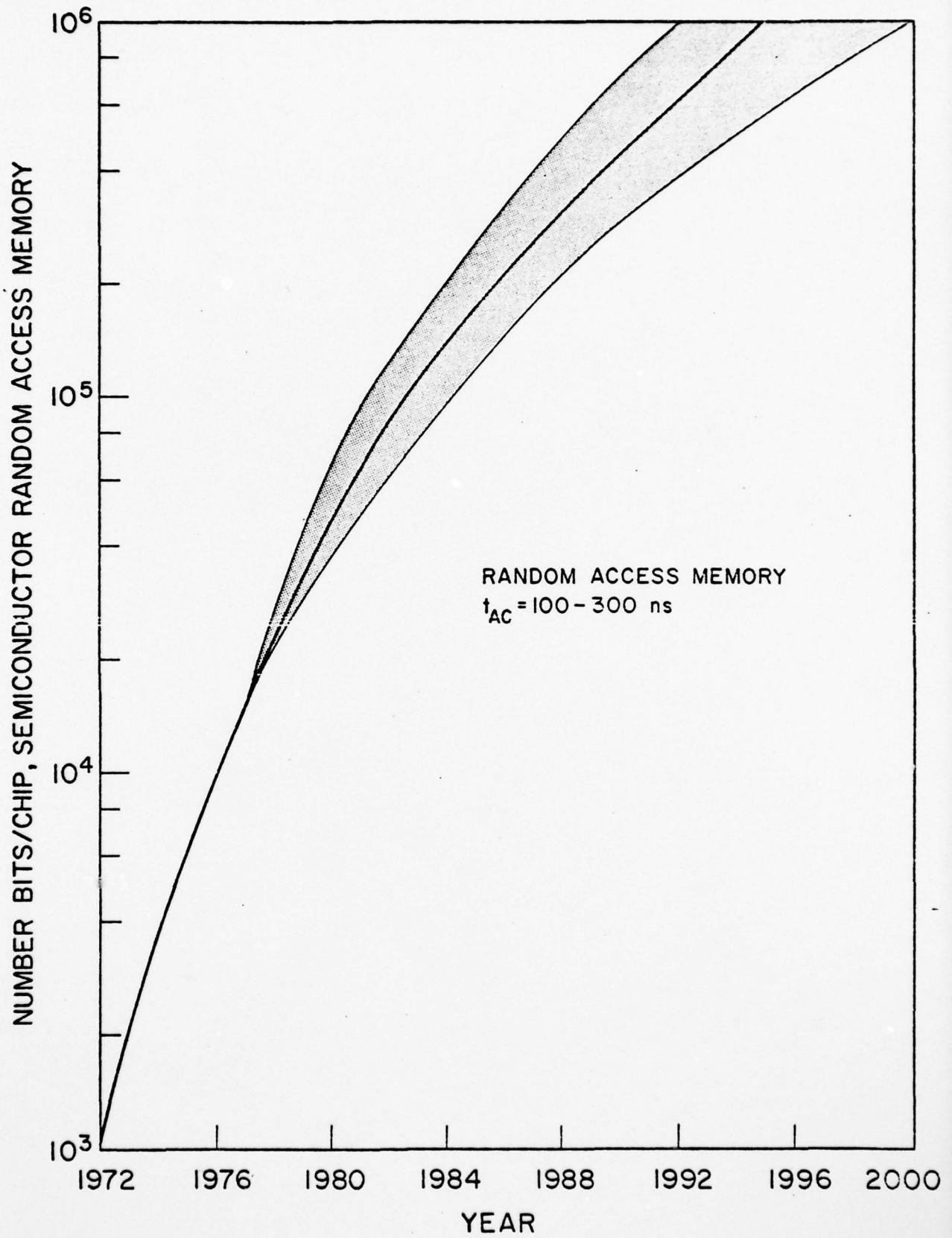
RAM has been roughly doubling every year in terms of bit capacity. The evolution from 1K bits/chip to 4K bits/chip was accomplished by going from a three-transistor cell to a single transistor cell (Figure 18). Further evolution is forecast in Figure 21 and is summarized below:

1. Memory Development (Figure 21)

Number of Bits Per Chip 1970-2000

- 16K - Present state-of-the-art; in full production in 1977; double-poly silicon gate process, single transistor per bit. Chip size about 180 X 200 mils with cell 30 μ m X 30 μ m. Size reductions with iteration.
- 64K - Smaller cell, projection printed with visible light, stacked double poly (possibly modified) CCD) design with larger chip size, chip size 200 X 230 mils with a cell about 18 X 20 μ m.
- 128K - Some cell simplification, larger chip, enhanced sensitivity in the sense amplifiers, discretionary wiring for redundancy and yield enhancement. Chip size is approaching a limit at 320 mils. Chip size 320 X 280 mils, 18 X 18 μ m cells.
- 256K - Cell density increases as electron-beam printing is used. Low voltage, low power designs and enhanced on-chip redundancy.

FIGURE 21: FORECAST OF DEVELOPMENTS IN MICROCOMPUTER MEMORY



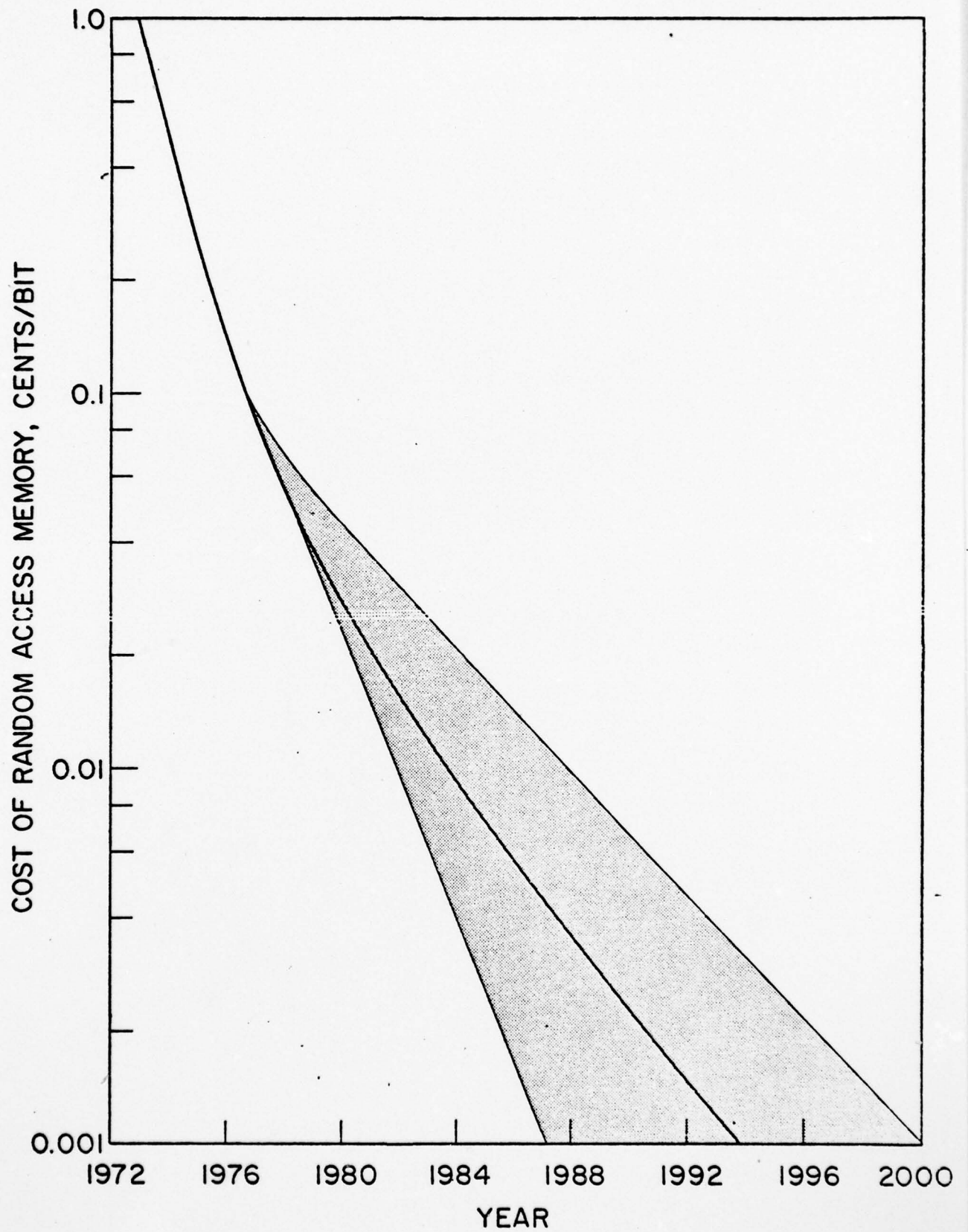
512K - X-ray lithography with further reduced cell sizes. Chip size 320 X 280 mils; cell size 8 X 10 μ m.

1M - Possible use of optically addressed dynamic storage for further increased density. Likelihood of new materials and storage mechanisms which could increase storage still further. Motivation for entire systems may focus efforts away from bit density as prime design motivation.

2. Cost Per Bit of Random Access Memory (Figure 22)

The cost per bit of random access memory has been declining rapidly since 1971 (5 cents per bit) and reached levels below 0.3 cents per bit in 1975. Further cost reductions are forecast and RAM should reach 0.01 cents per bit by 1984. In the period 1971-75, cost per bit dropped by a factor of two every year. From 1976 through the early 1980's the cost per bit should decline by a factor of two every two years and subsequently will decline still more slowly. This reflects the increased bit densities and larger chips on the one hand, and the increased area cost of silicon on the other. In predicting the memory cost, it is assumed that the chip yield becomes defect limited approximately two years after product introduction, allowing time for several design

FIGURE 22: FORECAST OF COST PER BIT OF RAM



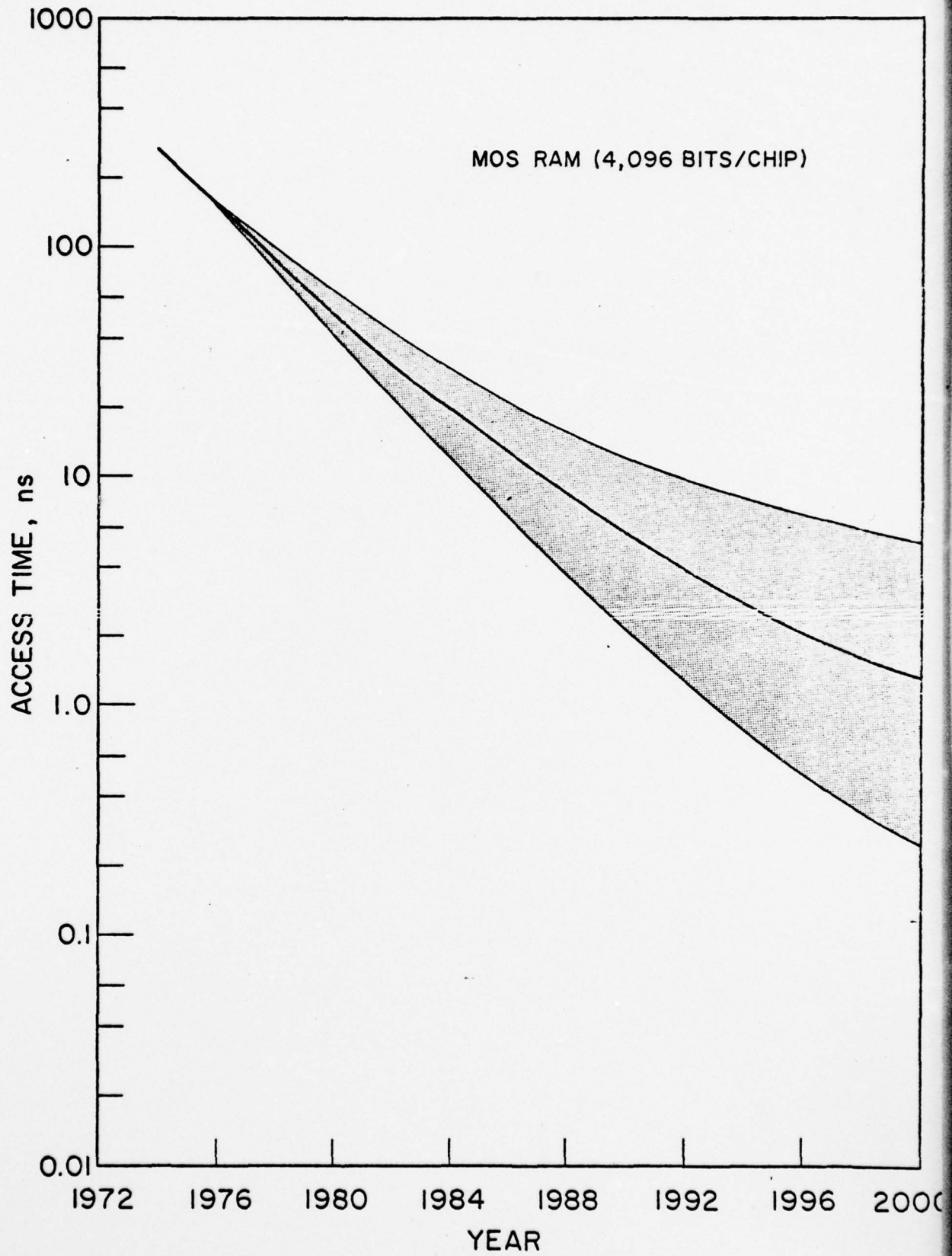
iterations. The forecast assumes an evolutionary development in random access memory and fundamentally new approaches to memory could speed cost reductions considerably. Similarly, the forecast assumes that the needed developments in X-ray lithography and sense amplifier design will occur by the mid 1980's so that memory evolution can continue. Serial and read-only memory technologies will evolve in a similar manner, exhibiting from two to four times the density of RAM and from one-half to one-fourth the cost. Block oriented CCD RAM's will merge the random access and serial approaches and will be widely used in the 1980's. By the 1990's it is likely that new memory approaches (e.g., optical stores) will be applied.

3. Random Access Memory Speed (Figure 23)

(Access Time)

Access time will be used as a measure of memory speed. Access time is defined as the delay between the presentation of a stable address at the chip and the appearance of valid data out at the output. Thus access time is related to the on-chip logic delays and especially to the capacitance of the row and column lines. As the cell size decreases, the storage capacitance will decrease. The resistance of the access switch will remain roughly constant so long as the

FIGURE 23: FORECAST OF RAM ACCESS TIME



channel length can be scaled appropriately. Hence, charge redistribution times will decrease. For fixed memory capacity, the line capacities will decrease with reduced dimensions and higher overall speed will result. On the other hand, if memory capacity is allowed to grow, then access time will remain roughly constant (Figure 20) unless new internal organizations are developed. Such developments are likely, and large RAM's may be organized internally as a series of smaller RAM's. Figure 23 forecasts the speed of a 4K-bit dynamic RAM versus time and reflects the improvement forecast in gate delays and reduced node capacitance. Comparing Figure 23 with Figure 16, the access time for RAM will stay well ahead of the instruction cycle time for memories at the 4K-bit level. Larger memories, perhaps built around several 4K-bit blocks, will decrease in access time at a slightly slower rate, due to the additional delay stages introduced by chip partitioning. In any case, improvements in memory access time should allow the forecast improvements in microcomputer instruction cycle to be fully utilized.

4. Random Access Memory Power

Dynamic MOS RAM as well as static CMOS RAM draws virtually no quiescent power in the storage array

itself since the only DC current flow is due to leakage. In CMOS, quiescent dissipation levels of less than 10^{-8} watts/bit have been achieved. Most of the power dissipated in such memories is dynamic, i.e., associated with charging or discharging node capacitance. Since for a fixed chip size, the capacitance will remain approximately constant, the power per chip will remain roughly constant. The power per bit will therefore decrease in accordance with Figure 21 for a constant clock frequency. As clock frequency is increased to achieve higher speed, power per chip will increase proportional to clock frequency. The reduction of operating voltage levels, use of low power technologies, chip partitioning, and on-chip power gating should allow the power to be held within package limits while memory speed and capacity is increased.

5. RAM Reliability

The previous discussion of reliability is applicable to memories and will not be repeated here.

B. Read-Only Memory (ROM and EAROM)

Semiconductor random access memory is volatile, i.e., information is lost if the supply voltage is interrupted. While this is acceptable for many data applications, it is far less acceptable for program storage. Read-only memory, as its name implies, can only be read. In its

simplest form, information is written via the mask pattern used at manufacture. Thus, a single transistor (with no storage capacitor) can be used per bit. The cell area is reduced by roughly half, while the peripheral circuitry is simplified as well. The resulting mask-encoded ROM is two-to-four-times more dense than RAM (Figure 21) and should remain so throughout the 1980's. Access times are expected to parallel RAM access times, and since the read operation is non-destructive, access time and cycle time for ROM are the same.

Mask encoding of the stored data is permanent and precludes subsequent program modifications. This can be circumvented using electronically-alterable ROM. The first such device was announced in 1971 and used a floating silicon gate to store charge. Erasure was by irradiation with ultraviolet light, and writing was via avalanche-induced tunneling of charge through the oxide. A single transistor was the storage element. Double-dielectric structures are also in use for the semi-permanent nonvolatile storage of information and will replace mask encoded ROM's in many applications. Microcomputers with at least 8K-bits of alterable ROM on-chip are now a reality. Storage for well over 100 years at 100°C has been forecast on the basis of accelerated high temperature aging.[17]

C. Bulk Storage Devices

In addition to the ROM and RAM already mentioned, other approaches to memory also deserve mention. Magnetic bubbles [16] have been in development for several years and are approaching production for a number of systems. Present chip capacities are about 100K, exceeding charge semiconductor memories (CCDs) by a factor of two. However, access time for these serial memories are as much as an order of magnitude slower than for CCDs, falling in the range of a few milliseconds. The prime advantage of bubble memories are their nonvolatility. Bubble memories will be important in replacing disc memories for data processing applications but will not have a major affect on systems having storage capacity less than one megabit. The latter encompasses most microprocessor-based systems. A data base for a movable map display is one possible application for a bubble memory on-board an aircraft.

Electron-beam addressed memory systems (EBAMS) replace the X-Y access scheme on the memory chip with an electron-beam addressing scheme off-chip so that the cell is considerably simplified. High density and low cost per bit result but an electron tube and its associated circuitry is required. Applications of this technology will be primarily in very large memories of more than 10 megabits. Thus the impact on microprocessor-based systems is expected to be minimal.

VI. Conclusions

In order to take advantage of the rapidly increasing capability of integrated electronics, new concepts in the design and organization of electron systems will be required. In some instrumentation and control applications, we are approaching the time when the cost of digital control may well be less than not only the system sensors, but the hookup wire itself. Microcomputers will be used much as latches are used today--as building blocks for larger systems. Careful thinking should be applied to all areas within FAA jurisdiction regarding automation, particularly in maintenance areas. The most important impacts will come through entirely new applications for integrated electronics. Cost, speed, power, and reliability will all be important.

In data processing, we have already seen hand-held electronic calculators evolve to the point where they are capable of performing functions which a few years ago were reserved for minicomputers. Some minicomputers such as the PDP-8 have already seen their CPUs reduced to a single chip and it is generally felt that most 1975 minicomputer-CPU's will be realizable on a single chip by 1980. By 1985, large machines (by today's standards) are expected to follow suit. The prospect of a processor composed of 10^4 gates, 64K-bits of RAM, and 128K-bits of ROM on a single chip is very real for 1985.

CHAPTER FOUR

AN UNCONSTRAINED TECHNOLOGICAL FORECAST OF PERIPHERAL HARDWARE AND DISPLAY TECHNOLOGY

I. Introduction

In previous chapters, impressive progress has been forecast for microcomputers throughout the remainder of this century. This progress will impact electronic systems in terms of complexity, cost, speed, power, and reliability and will permit the introduction of sophisticated electronics into both ground-based and airborne aviation systems. For large ground-based systems intended for ATC or administrative computing, the number of system parts in addition to the computer itself is not large, and the impact on system capabilities can be assessed from the microcomputer forecasts almost directly. However, for airborne systems the impact of advances in microcomputers could be severely muted unless these advances are accompanied by progress in the peripheral hardware necessary to implement an instrumentation or control system. In this chapter the progress in the peripheral hardware area will be discussed, 'peripheral' being interpreted as functionally and physically separate from the microcomputer itself. Progress in interface electronics, sensors, and displays will be described. These areas are of prime importance in determining the cost, speed, and feasibility of an airborne instrumentation system. The approaches in these peripheral areas are more diverse than in microcomputers

and no attempt to be highly comprehensive or detailed will be made. Rather, an overview of recent and anticipated progress in these areas will be given together with references to more detailed discussions. The significance of peripheral hardware is placed in further perspective in Chapter Five, where specific ground-based and airborne electronic systems are analyzed and forecast.

II. Interface Electronics

A. Peripheral Functions in Microcomputer Systems

Progress in single-chip highly-integrated microcomputers is dramatically reducing the cost and increasing the computing power of electronic systems. As has been suggested, the developments forecasted for microcomputers can be interpreted almost directly in terms of increased performance for computing equipment. However, in the instrumentation area, where the most significant microcomputer impacts will likely be made, a variety of electronic components are required in addition to the microcomputer itself for system implementation. These peripheral circuits and devices are required to interface the microcomputer with other machines and with the analog world.

The elements required in this peripheral interface area at present include a large and diverse array of components ranging from line drivers, multiplexers, level

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shifters, and data converters which are required to change the strength, origin, and format of the analog or digital signals, to the input/output devices (sensors and actuators) required to interface between the electronic system and the physical world. From a circuit standpoint, many of these devices require a mix of both analog and digital functions, and this has tended to keep them physically as well as functionally separate from the processor. The sensor/actuator area is frequently interdisciplinary and highly specific to a given application, restricting its suitability for high-volume batch production.

As the capability to produce low-cost LSI circuits has developed, the number of separate interface circuits required for system implementation has dropped rapidly, and there has been an increasing effort to define and develop standard interface elements for many machine-machine interfaces. Familiar examples are the programmable interface elements (PIEs) and universal asynchronous receiver-transmitters (UARTs) now available with most microprocessor chip families. In the past five years, the number of small and medium complexity packaged circuits required for microcomputer system implementation has decreased by roughly an order of magnitude, dropping from thirty or more in 1972 to three or four in 1977. These peripheral functions will

likely become still more consolidated and standardized in the future, and many will become an integral part of the microcomputer chip itself. Exceptions are circuits required to operate at high voltage or power in order to interface with I/O devices, and circuits requiring special technologies for their implementation. The former class of circuits will be discussed in connection with comments on sensors which are presented in Section III below, while the latter category is illustrated in the discussion of analog-to-digital and digital-to-analog converters which follows. As for the other miscellaneous circuits mentioned above, they will become more and more highly integrated and will continue to have a decreasing role in system cost and performance.

B. Analog-to-Digital/Digital-to-Analog Converters

The area of analog-to-digital and digital-to-analog converters has recently been the focus of a great deal of work in the electronics industry and is a key element in the implementation of a variety of electronic systems. The role of these converters in interfacing between the digital processor and the analog I/O devices was illustrated in Figure 13. The requirements on such converters include high speed, high accuracy, and low cost, and efforts to satisfy these requirements have motivated the joining of high precision analog technology with a batch-process production environment.

1. Conversion Techniques and Tradeoffs

Consider first the simple current-mode digital-to-analog converter (DAC) illustrated in Figure 24.

A signal voltage represented as a digital n-bit word, resulting perhaps from a digital computation, is to be converted into an analog form. Each bit of the digital representation is used to control a switch which directs current from a reference level into either the summing node of an operational amplifier or into ground. Since the summing node is at a virtual ground, the circuit avoids RC time constants and voltage settling problems and develops an output voltage

$$e_o = -V_{REF} (1/2 e_1 + 1/4 e_2 + 1/8 e_3 + \dots + 2^{-n} e_n)$$

where e_i , the i^{th} input bit, is either 0 or 1 depending on the input binary word. This relatively simple approach to digital-to-analog conversion has been used for most DAC applications. The output voltage can represent the desired analog signal to within one-half of the least significance bit (LSB) ($\pm 1/2$ LSB) so that the resolution of the converter is

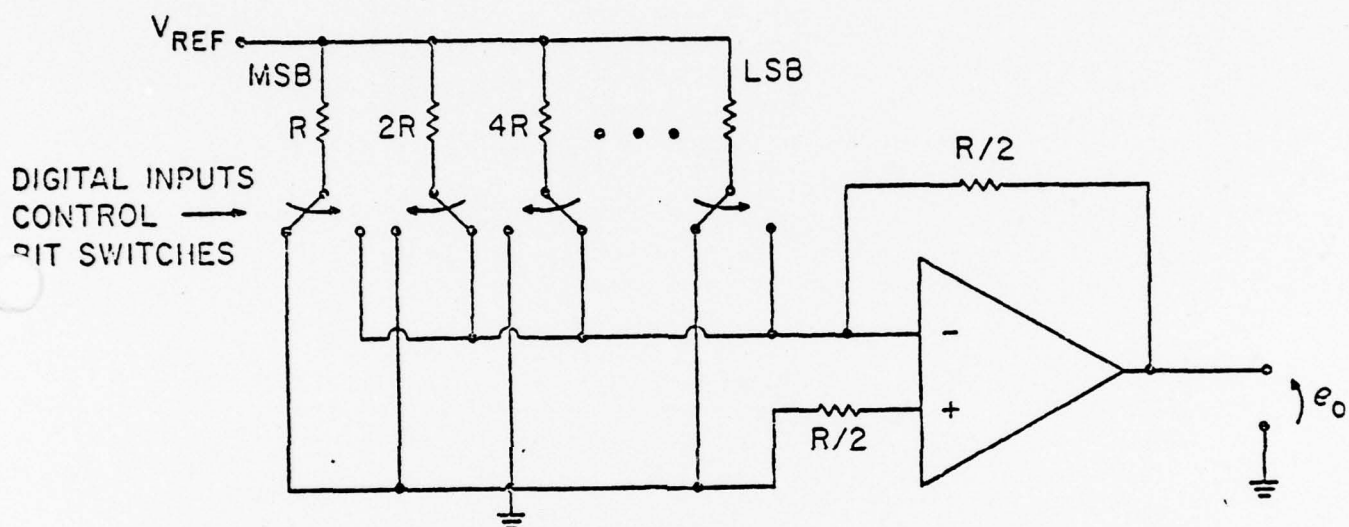
$$\text{Resolution} = \pm 1/2 \text{ L.S.B.} = \pm 1/2^n + 1$$

For an eight-bit converter ($n=8$) we have 256 possible output levels and a resolution of ± 1 part in 512.

For twelve bits (the present state-of-the-monolithic-

art), the resolution is 1 part in 8192 (nearly \pm 0.01 percent). Achieving this resolution in a batch process has presented a formidable challenge to the industry which has been met to a considerable degree.

The realization of the DAC shown functionally in Figure 24 as a monolithic chip involves the realization of four key elements in precise and stable form: 1) the resistive ladder network, which weights the respective currents in a binary fashion, 2) the bit switches, 3) the summing amplifier, and 4) the voltage reference. The ladder network has been a prime focus for work, since the relative scaling of the resistors determines the resolution and relative accuracy of the DAC. Both binarily-weighted and R-2R ladder networks have been used employing diffused, ion-implanted, or thin-film resistor technologies [1,2]. Thin-film Si-Cr resistors have been used for many high-accuracy DACs and have exhibited absolute and tracking temperature coefficients of -30 ppm/ $^{\circ}$ C and ± 1 ppm/ $^{\circ}$ C, respectively [2]. Ladder networks for converters having accuracies greater than eight bits must be trimmed, and laser trimming [3] has proved a valuable production technique in the realization of high performance DACs. The selective shorting Zener diodes to allow permanent one-time adjustment of ladder accuracy is a second



INPUT: 011 ...

OUTPUT: $-V_{REF}(1/4 + 1/8 + \dots) = e_0$

FIGURE 24: A CURRENT-MODE DIGITAL-TO-ANALOG CONVERTER

technique now in use [4].

The monolithic bit switches used to steer the bit currents in the DAC must be carefully designed to maintain the accuracy of the ladder over the operating voltage and temperature range of the part. Both the binary attenuation of equal currents and the binary weighting of bit currents are used [1] as well as combinations of the two approaches. Similarly, the summing amplifier represents an analog component whose dynamic response and linearity are important in achieving high performance from the converter.

The voltage reference represents a final element whose stability is crucial to the absolute accuracy and stability of the DAC. These references in the past have been separate from the DAC chip but their integration as part of the monolithic DAC is increasingly feasible. Recent developments in band-gap [5] and buried Zener [6] voltage references, some using on-chip heaters to stabilize the chip temperature in the face of ambient temperature fluctuations, have produced references stable to better than 0.5 ppm/°C in the ambient. A variety of monolithic self-contained DACs should be available at the twelve-bit level by 1980. Comments on anticipated accuracy, speed, and cost will be given in the sections below. The integration of the DAC on the processor chip

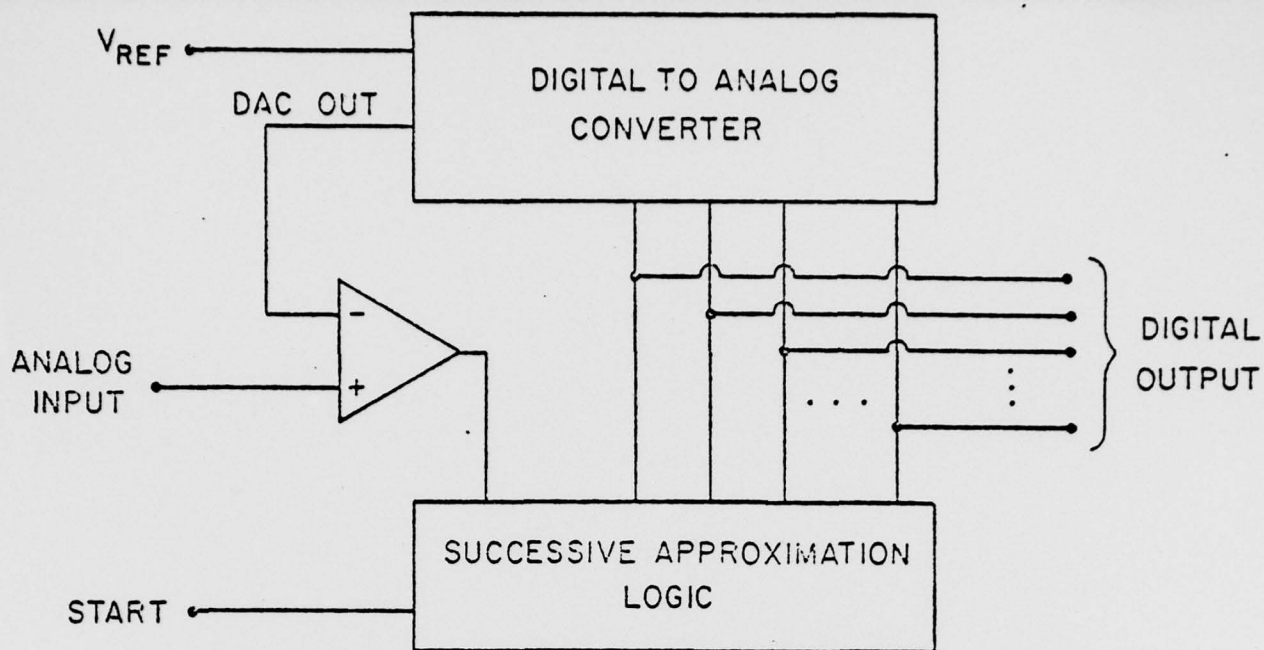
itself is a possibility by the early 1980's in microcomputers aimed at the control area.

While most digital-to-analog converters are derived from a common resistive-ladder approach such as that shown in Figure 24, the approaches used for analog-to-digital conversion (ADC) have been diverse [7]. The approaches have ranged from open-loop techniques such as analog-to-frequency, analog-to-pulse width, and simultaneous (parallel) conversion to closed-loop techniques such as ramp-and-counter, successive approximation, and dual or triple-ramp methods. Each technique represents a slightly different compromise among speed (conversion time), accuracy (number of bits), and complexity (cost). Simultaneous converters have operated at speeds in excess of 100 MHz [8] but are limited in accuracy to less than six bits by the required circuit complexity. They are also very expensive. Dual ramp converters require relatively modest complexity but are also relatively slow, with 2^{n+1} clock cycles required for an n-bit conversion. For a 5MHz clock, the conversion time is more than 400 μ sec for a ten-bit ADC. Such converters are widely used in digital panel meters.

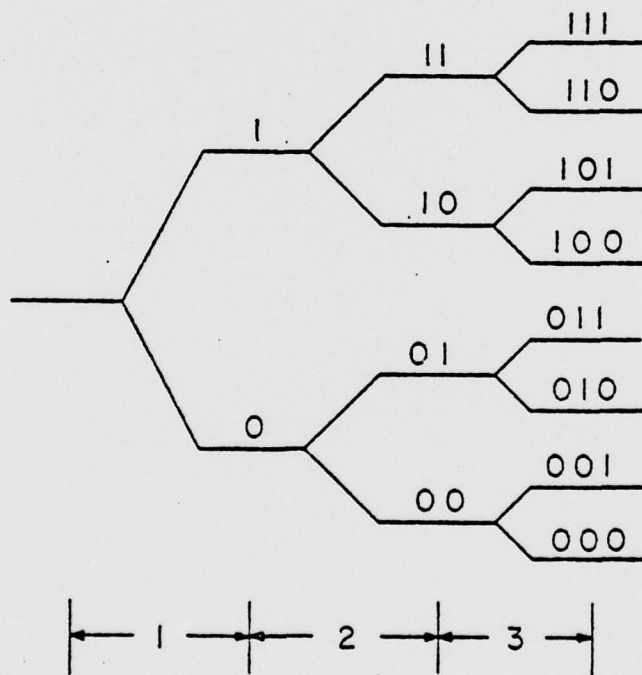
The successive approximation technique represents a tradeoff among speed, accuracy, and complexity which is appropriate for many instrumentation

applications. This technique is shown in Figure 25. An analog signal is presented to the converter and a START signal from the processor initiates the conversion process. The most significant bit (MSB) is set to one and the other bits are set to zero, defining a level at half of full scale. These bit settings are used as inputs to a DAC, which produces the selected analog level. This level is compared with the analog input, and if the input is greater, the MSB remains set at one; if not, the MSB is set to zero. The next-most significant bit is next set to one and the analog signal generated is again compared with the analog input to determine the proper next-most significant bit setting. Successively, each remaining bit is set to one, the input is tested, and the proper bit state is determined. Thus the successive approximation ADC requires a DAC, a comparator, and some sequencing logic. The conversion time is equal to n DAC conversion times plus n comparator delays for an n -bit ADC. In present technology this corresponds to 20-40 μ sec for 10 bits.

The ADC area has been extremely active during the past five years. With the introduction of monolithic designs to replace earlier hybrid circuits, prices have fallen by nearly an order of magnitude. Fully dozens of different approaches have been tried and



(a) Converter Block Diagram



(b) Successive Approximation Sequence

FIGURE 25: ANALOG-TO-DIGITAL CONVERSION USING THE SUCCESSIVE APPROXIMATION TECHNIQUE

and innovation in this area continues. Approaches using switched-capacitor arrays [9,10] have conserved chip area and appear compatible with integration on the microcomputer chip itself. This will probably occur by the early 1980's. The diversity of approaches to analog-to-digital conversion makes forecasts of future performance difficult; however, general trends are discussed in the sections below for converters having conversion times below 40 μ sec and accuracies of ten to twelve bits. Since DACs are a component part of at least one such form of ADC, they are not forecast separately.

2. Accuracy

The accuracy of monolithic data converters has improved dramatically in the past five years. The discussion here is restricted to monolithic converters, as opposed to hybrid modules, due to their greater compatibility (in size and cost) with microcomputer systems. Digital-to-analog converters evolved from six-bit designs, announced in 1971 [11] to ten-bits in 1973 [1], and in 1977 attained twelve-bits (\pm one part in 8192 resolution) in monolithic form. Analog-to-digital converters have improved in accuracy in a similar fashion. ADCs capable of resolving at the sixteen-bit level have been reported [12], although these converters are not in fully monolithic form and are very slow

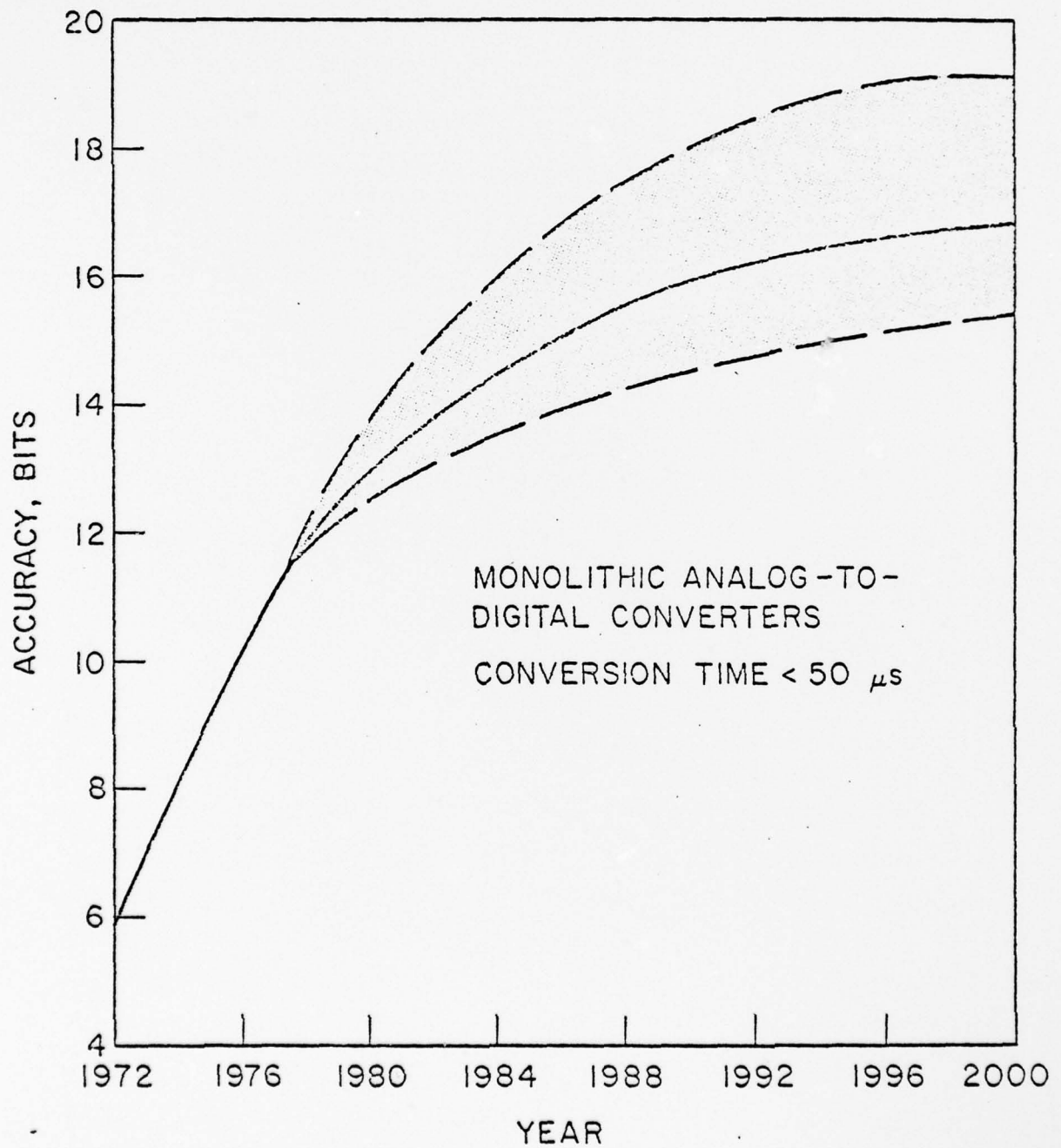
(one second conversion time). For successive-approximation ADCs with conversion times less than 100 μ s, we are now at the ten to twelve-bit level in accuracy.

Figure 26 shows the likely growth in converter accuracy (number of bits) for the remainder of this century. A converter offering speed comparable to today's successive approximation ADCs is assumed although beyond the very near term (1980) it is probable that some alternative technique may be used. In view of the extreme stability required as accuracy and resolution increase and the difficulty in maintaining stability over temperature, the growth in available accuracy is expected to slow considerably in the future, with fourteen-bits available in the early 80's and relatively little subsequent progress. As microprocessor capabilities improve, however, it is possible that recalibration within the end system may ease some of the stability requirements in achieving high-accuracy conversion. A second factor slowing growth may well be the market demand for such high accuracies.

3. Speed

The speed (conversion time) of an ADC depends strongly on the conversion technique employed, and it is likely that a number of new techniques will be used in the future. If successive approximation is selected

FIGURE 26: ANTICIPATED ACCURACY FOR MONOLITHIC ANALOG-TO-DIGITAL CONVERTERS



as representative of a present technique popular for many instrumentation and control applications, we can, however, forecast anticipated improvements in conversion time for this approach. As noted above, conversion time for fixed accuracy (taken here as ten bits), will depend on speed improvements in the DAC, sequencing logic, and the comparator. As node capacitance decreases with reduced lithographic dimensions and, perhaps, with the application of dielectric isolation, speed improvements can be anticipated in all areas, resulting in the conversion time forecast shown in Figure 27. Greater improvements are anticipated in speed than in accuracy for these converters, and speed is expected to be a more sensitive function of conversion technique. For the successive approximation approach, speed is a linear function of the desired accuracy (number of bits), and at the ten-bit level, much of the present cost penalty as compared with slower techniques should soon disappear.

4. Converter Costs

The cost of a converter is directly related to its yield at a given accuracy level. Many present converters are marketed in several resolution ranges; the less accurate are 'short-cycled' in operation to omit the LSB conversion cycles. Cost also varies with chip complexity (size and yield) and hence

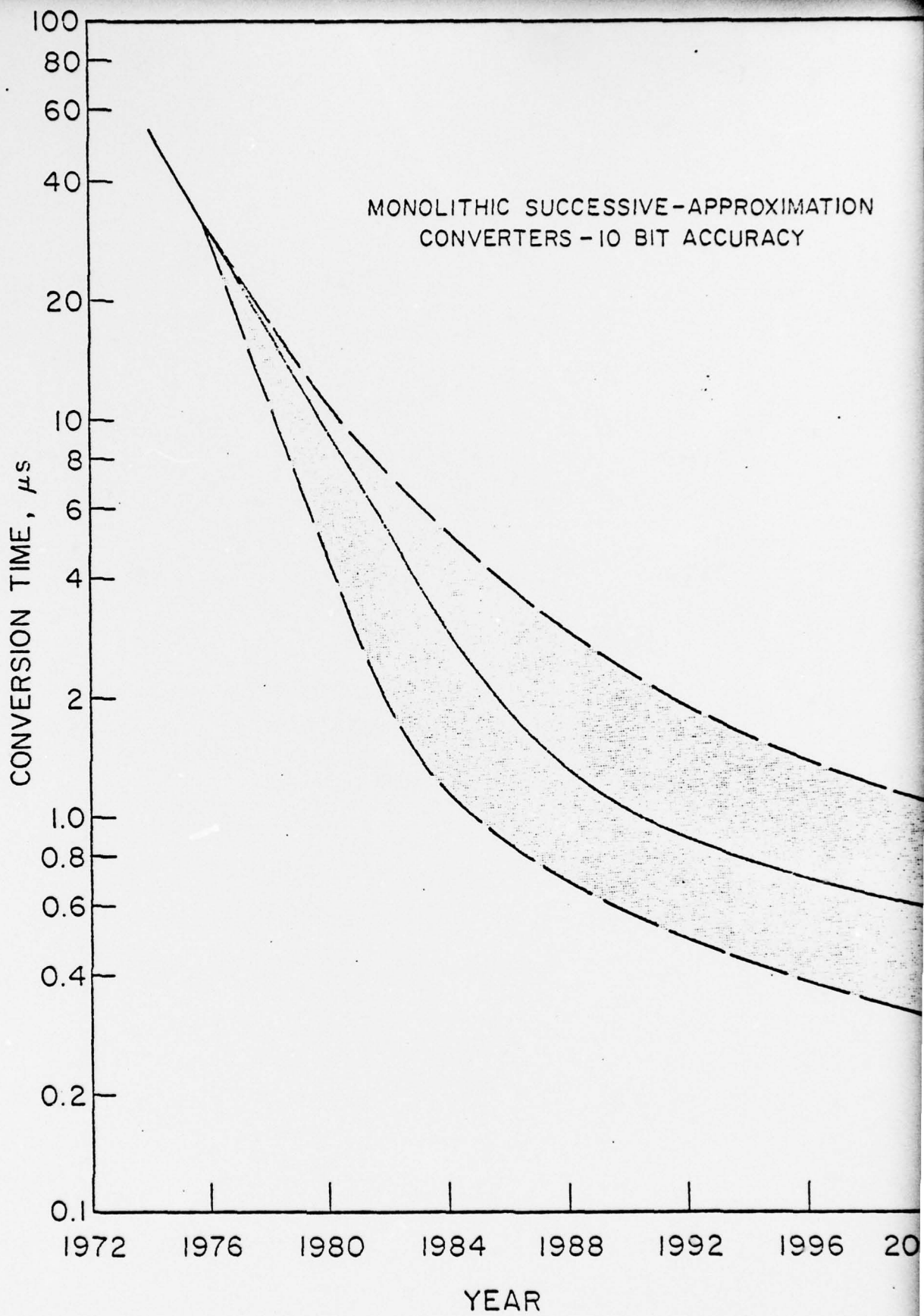


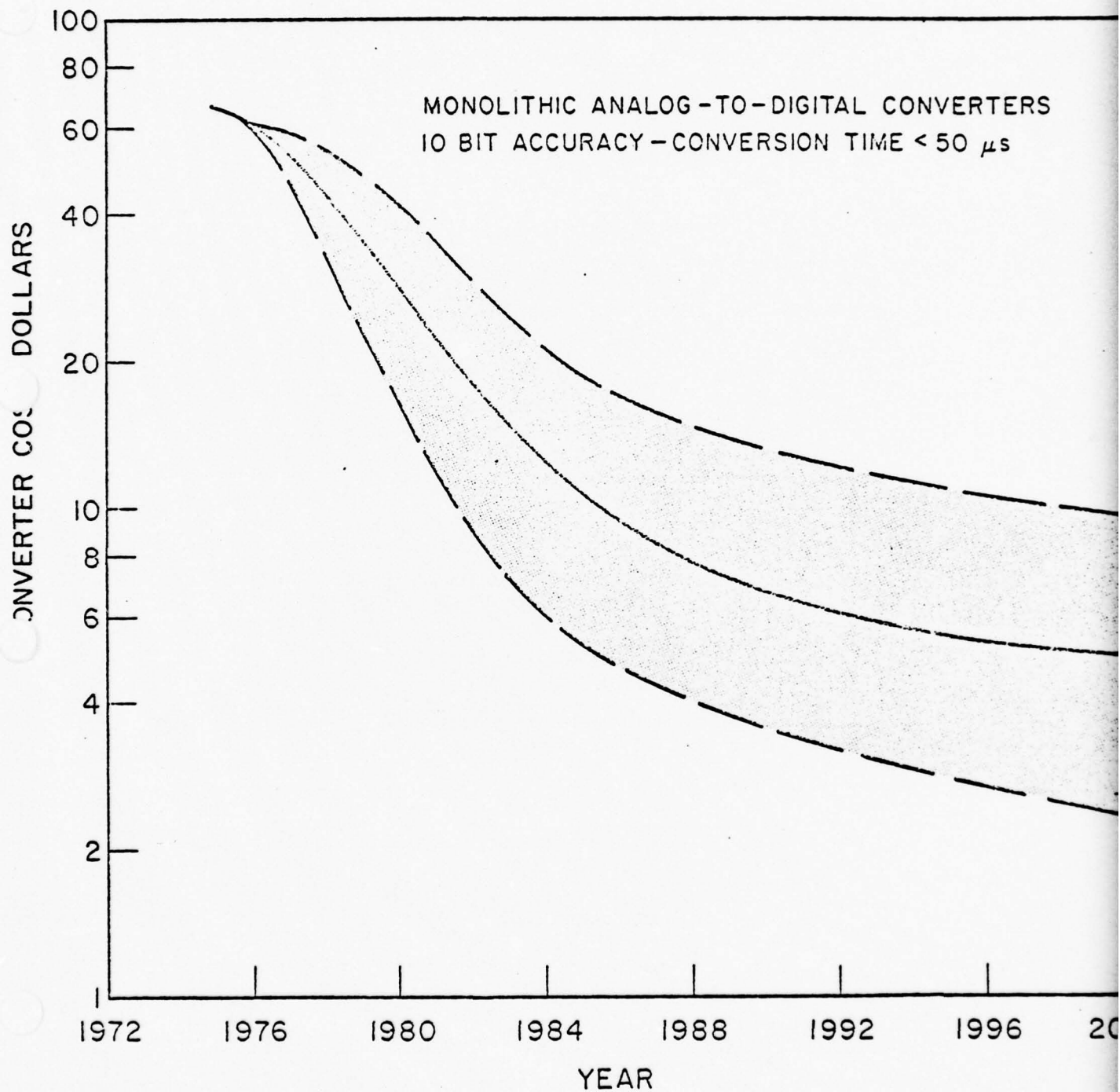
FIGURE 27: CONVERSION TIME FOR SUCCESSIVE APPROXIMATION
ANALOG-TO-DIGITAL CONVERTERS

again differs widely among different conversion techniques. Figure 28 shows the anticipated cost of a successive-approximation ten-bit converter over time. While present ADCs of this type are relatively expensive compared with microprocessors, prices should drop below the ten dollar level during the early 1980's. In the near-term at least, prices should change by a factor of roughly two for every two-bits of resolution added or deleted from the converter. Allowing conversion times in the millisecond range, ADCs are available today at less than ten dollars.

5. Summary

The analog-to-digital converter is probably the most significant peripheral interface component for next-generation instrumentation systems. A wide number of designs are now available at the eight and ten-bit levels, offering a wide range of conversion times and chip complexities. Future progress extending resolution beyond the twelve-bit level will be relatively slow as a result of both market demand and the extremely high component match and stability required. Resolution levels should nevertheless reach sixteen bits during the 1980's, probably using new conversion techniques and possibly using sophisticated microprocessors to ease the stability requirements on the converter. At the eight-bit and possibly ten-bit

FIGURE 28: ANTICIPATED DECLINE IN ADC
COST AS A FUNCTION OF TIME



levels, ADCs will be part of the microcomputer chip by the early 1980's or before.

Conversion time will show steady improvement as smaller dimensions and improved processes are employed; however, conversion time will continue to be comparable to several microcomputer instruction cycles. Cost will decline relatively slowly at a given resolution level, particularly at ten-bits and above where extensive testing and trimming is required. At ten-bits, converter cost comparable to that of the microcomputer chip is expected, while for higher accuracy the converter cost could be several times that of the microcomputer.

III. Sensors and Actuators

A. Factors Motivating and Constraining Sensor Development

An increasing number of electronic systems are being designed to interface with non-electronic systems, and here the input and output functions are provided by sensors and actuators, respectively. In many important areas such as automotive and medical electronics, the development of appropriate sensors and actuators is the key to the application of electronic instrumentation and control. In the following discussion, the term 'sensor' will be used to include both sensors and actuators.

Performance requirements for sensors are frequently very demanding and necessarily equal or exceed those placed on the data converter. Since the sensor represents the interface with the system being monitored or controlled, performance requirements tend to be varied and not easily met by batch-processed structures. Packaging problems are often severe and the environmental conditions under which the sensor must operate are typically far from ideal. Image sensors represent probably the most developed solid state sensor area and together with temperature sensors represent parameters most easily coupled with via a nearly-conventional package. Encapsulation becomes more of a problem with pressure and force sensors, and is still more difficult with chemical concentration and other 'wet' monitoring devices.

Solutions to sensor problems have involved a very wide range of approaches and technology. The resulting sensors have been primarily high-cost, low volume, custom devices. The high cost has helped to hold the volume down and vice versa. The market for solid-state sensors in this country in 1971 was about 85 million dollars (1971 dollars), increasing to just over 120 million in 1975 (1975 dollars) and expected to reach nearly 150 million in 1978 (1975 dollars)[53]. Sensors represent an increasingly important component of system cost and frequently limit the performance levels which can be achieved.

There is a clear need for improved sensors, and yet progress in this area has been disappointingly slow.

One major factor constraining sensor developments has been the interdisciplinary nature of the problems involved. Successful sensor development often involves combinations of new materials, new techniques, and in depth understanding of a non-electrical system. These factors, especially the last, have caused many of the component manufacturers to avoid the sensor area, while the system manufacturers have frequently lacked expertise in the first two areas. The result has been very little real progress in sensors. Several university laboratories have attempted to perform the necessary research and development with some success, but, for the most part, sensors remain expensive, low-volume, individually-tuned devices. This situation may change, however, as an increasing number of system manufacturers become involved with device fabrication and as the decreasing cost of digital computation and control circuitry applies more and more pressure for developments in the sensor area. The existence of low-cost microprocessors is also changing the emphasis in sensors from linearity and absolute stability to reproducibility and predictability.

A challenge facing the industry is the development of low-cost, batch-fabricated, reliable sensors of

sufficiently wide operating range to overcome much of the diversity in present sensing approaches. There are indications that this may be possible for many applications using integrated silicon sensors, combining the precision analog techniques evidenced in data converters with transduction phenomena in silicon. Transducing mechanisms in silicon are known for pressure, strain (force), acceleration, temperature, and radiation (infrared, visible, gamma). Silicon-based devices have also shown promise as sensors for gas and ion concentrations. In addition to its versatility, silicon is probably better understood relative to its properties and processing than any other material. Its use as a basis for transducer fabrication raises the possibility of also integrating a limited amount of circuitry on the sensor to condition the output signal prior to transmission to the microprocessor. This ability is especially attractive in vehicular systems [13] where noise immunity is important and where it may be necessary to compensate the sensor response for sensitivity to secondary variables (e.g., temperature) capable of interfering with the parameter being measured. It is by no means clear how the electronic circuitry should be partitioned between the sensor and the (possibly remote) instrumentation package, but in many situations, circuitry on the sensor itself appears very attractive. Encoding analog data in a quasi-digital format such as FM

at the sensor, for example, would permit multiplexing multiple sensors on a common pair of leads, decreasing lead counts and increasing system reliability.

Integrated silicon sensors are under development in a number of university and industrial laboratories. In the past, industrial efforts have sometimes been unsuccessful and frequently frustrating due partly to the interdisciplinary aspects of these problems. Universities are more ideally suited to such problems but require sufficient external funding to allow such problems to be pursued. Although the aviation industry will have little influence on the development of microcomputers or data converters, it is believed that a significant impact on future airborne instrumentation might be derived from its support of specific programs in this sensor area.

All sensing problems can certainly not be satisfied via integrated silicon sensors. The relatively low maximum operating temperature of silicon devices (150-200°C) alone precludes many applications. However, it appears that many sensing problems are solvable using either integrated silicon sensors or an appropriate marriage of silicon circuit technology and a non-silicon transducer material.

In silicon, solid state image sensors are undoubtedly the most highly-developed sensing example, offering both

linear and area arrays capable of approaching TV-quality imaging. Silicon temperature sensors were introduced about 1972 for the low-cost low-to-medium temperature range. Pressure sensors are slowly improving in performance and appear nearly ready for a number of high-performance, low-cost applications. Silicon pressure sensors are discussed more fully in the sections below.

The further development of solid state sensors and actuators for microcomputer-based instrumentation and control systems is essential. However, based on past developments in the sensor area, it is difficult to predict how or when these developments will occur. Some continued government funding may be necessary to solve key problems in this area.

B. Pressure Sensors: A Specific Example

Pressure represents one of the most important parameters which must be transduced for processing by electronic systems, and the demand for reliable pressure sensors has proved one of the most difficult to satisfy at low cost. Applications are widespread in medical instrumentation, construction, and industrial process control as well as in transportation. In the automotive area alone, there are more than a dozen different applications for pressure sensors on the automobile [14], ranging from transducers which monitor brake line or tire pressure for operating safety to those sensors of manifold and

barometric pressure necessary for real-time engine control and its associated fuel economy. In aviation there are many similar applications as well as many others unique to flight.

Just as there are a wide variety of applications, presently available transducers take a number of forms. They generally consist of a diaphragm, which moves in response to pressure, and a transducing structure which is driven by the diaphragm and which produces an electrical output in response to pressure. In many applications, stability is a serious problem and the cost of the sensors used is high. High cost, in turn, limits the usage of such sensors. In medical applications, high cost must sometimes be tolerated, as in present catheter-tip pressure sensors which cost hundreds of dollars each. In automotive applications, high cost is the primary factor precluding the use of solid-state pressure sensors and forcing the continued use of mechanical sensors. In airborne equipment, sensitivity to cost lies somewhere between these two extremes.

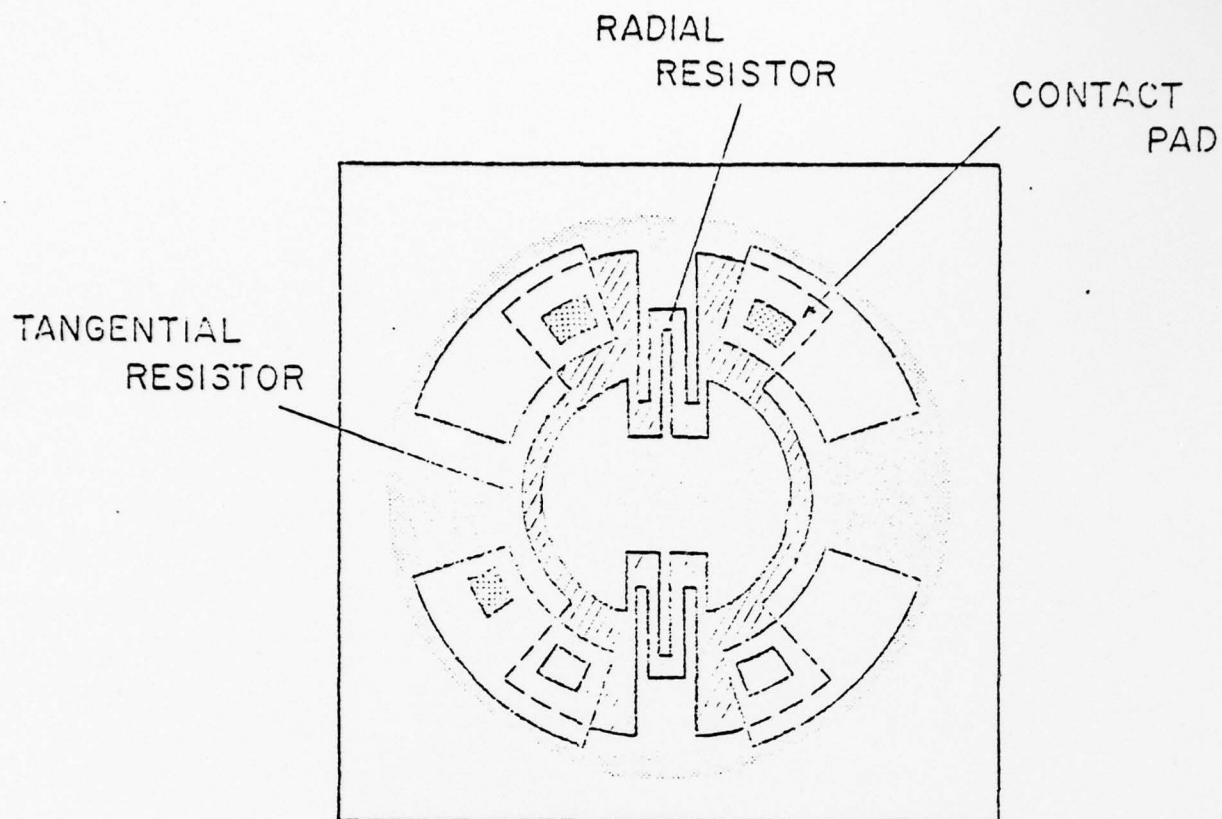
A number of desirable operating characteristics for next-generation pressure sensors can be identified, including 1) low cost (batch fabrication), 2) small size, 3) high accuracy, 4) wide dynamic range, 5) high stability, and 6) compatible output format (e.g., frequency modulation (FM) as opposed to straight analog).

A number of approaches to fulfilling these goals are possible, the most promising of which is the integrated silicon sensor fabricated using integrated-circuit batch processing techniques. The highly-developed state of silicon technology coupled with the possibility of including a limited amount of signal processing circuitry on the same chip with the transducer makes the approach a logical choice for low-cost sensor realization.

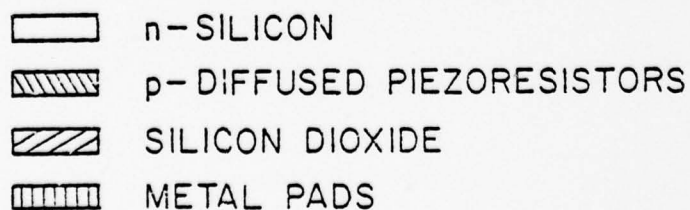
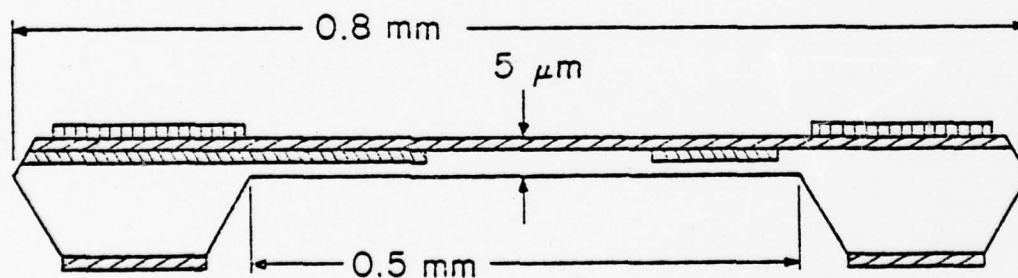
Historically, there are several pressure-sensitive effects in silicon which have been used for pressure transducers. Although no piezoelectric effect is observable, both the strain-induced changes in the electrical properties of p-n junctions [15] and the piezoresistive effect [16] have been widely used for several years. The piezo-junction effect, frequently observed as a change in reverse diode current with pressure, is a bandgap effect and measurable changes require stress levels approaching the fracture stress of silicon. This leads to instabilities and long-term drift in such sensors and is no longer widely used. The piezoresistive effect, on the other hand, is observable at lower stress levels and is the result of the change in carrier mobility with stress.

To produce observable effects with small pressures, some kind of pressure magnification scheme must be employed. Most present transducers utilize the piezoresistive effect combined with a thin diaphragm for coupling the

external pressure to the transducing element. A typical transducer of this type is shown in Figure 29. Early devices of this type were formed entirely from a thin silicon membrane, whose edges were clamped by the package but which lacked a thick supporting rim. The difficulties associated with processing and handling such thin silicon membranes precluded batch processing and kept yields very low. As chemical etching techniques developed, the feasibility of selectively etching diaphragms in wafers of normal thickness improved, and structures of the type shown were demonstrated [17]. The piezoresistive elements are diffused into the thin silicon diaphragm and are oriented with respect to the crystallographic axes in accordance with known design considerations [17]. The diaphragm is formed by etching and is supported by the thick rim, which is an integral part of the structure. The resistors are interconnected to form a full bridge. This structure is capable of batch processing and acceptable yields and is consistent with meeting the design goals mentioned earlier. In 1973, a commercial pressure sensor was announced by National Semiconductor based on these techniques [18]. This was a hybrid configuration, consisting of a monolithic transducer chip (Figure 29), a thick film resistor network for trimming the zero point and temperature sensitivity, and several active integrated circuit chips to implement temperature compensation and signal conditioning. The relatively large



(a) Top View



(b) Cross-section

(b)

FIGURE 29: A THIN-DIAPHRAGM PIEZORESISTIVE SILICON PRESSURE SENSOR FABRICATED USING INTEGRATED CIRCUIT BATCH PROCESSING TECHNIQUES. Diaphragm shape can be circular, square, or rectangular.

chip count and variety of technologies used made this approach relatively expensive (more than \$50 in small quantities) and precluded most low-cost applications, including the automotive. A low-cost, monolithic, pressure sensor meeting the goals above has yet to be developed. Most approaches now center on structures similar to that shown in Figure 30, where the transducer chip, perhaps also containing signal conditioning electronics, is sealed to a thick silicon support. The support absorbs mismatches between the thermal expansion of silicon and the package, minimizing package-induced drift in the transducer. An electrostatic or alloy seal results in an absolute sensor. Square diaphragms are used instead of circular ones due to their greater compatibility with anisotropic etching. Major problems yet to be solved include an understanding of the basic instability mechanisms in such sensors and the use of monolithic circuitry to provide drift-free signal conditioning while easing the testing and calibration of the devices.

IV. Display Technologies and the Man-Machine Interface

In most systems, the task to be performed or the result obtained is ultimately supplied by or presented to man. The dominant mode of presenting complex results is via the visual display, either in character or graphic form, and it will play an important role in airborne instrumentation.

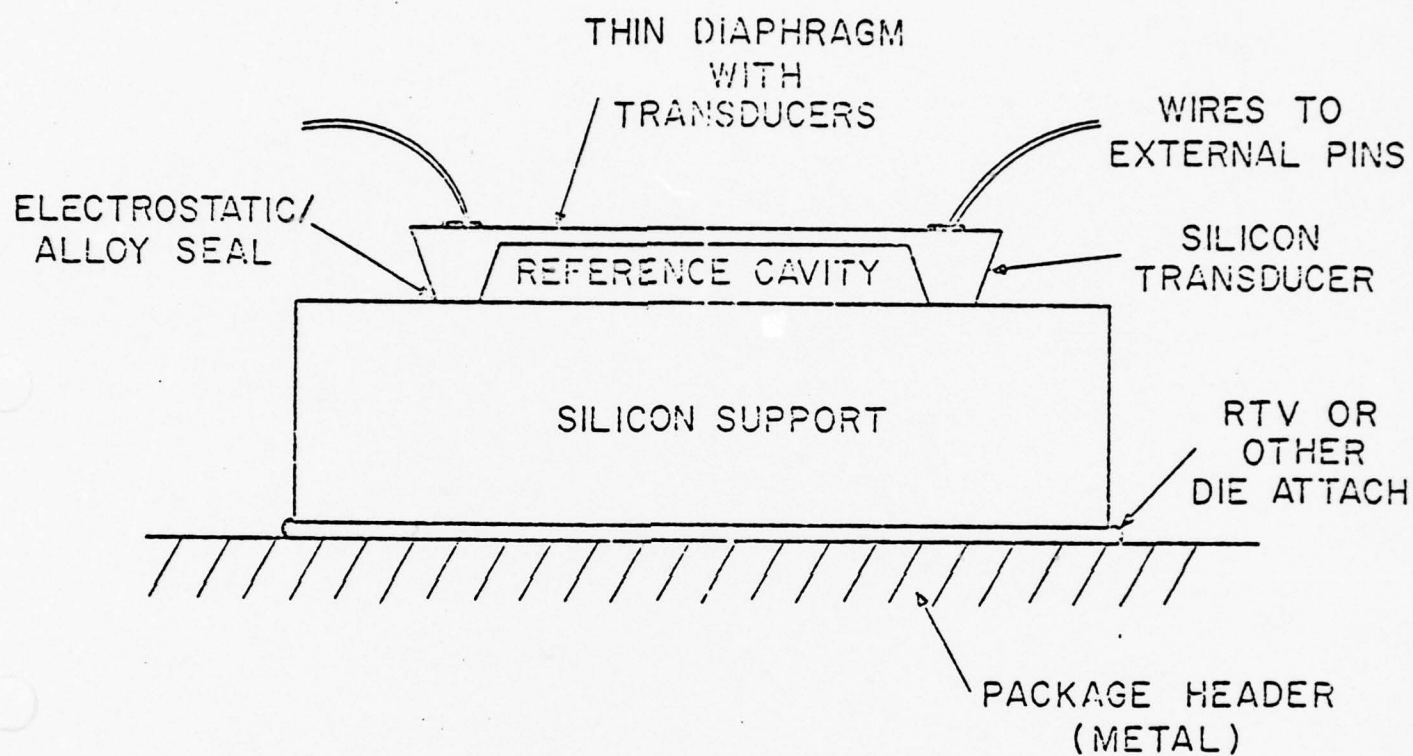


FIGURE 30: MOUNTING ARRANGEMENT FOR AN INTEGRATED SOLID STATE PRESSURE SENSOR

In this section, present activities in the display area will be summarized, followed by a short description of auditory (voice) input-output communication between man and machine.

A. Display Technologies

The display area has been extremely active during the past five years, with a number of competing technologies in exploratory development. The diversity and number of these approaches suggests some fragmentation of effort which, hopefully, will be resolved soon as the most promising approaches become evident. For aircraft and ATC applications, there is a need for both character (alphanumeric) and imaging displays with the following characteristics:

- 1) high reliability
- 2) low cost
- 3) small size
- 4) light weight
- 5) low input power
- 6) easy interfacing with digital drive circuitry
- 7) low luminance noise
- 8) suitable brightness under varying conditions of ambient lighting.

Some of the technologies under present development are primarily for character displays while some are for panel imaging. Since the requirements in these areas differ, they are discussed separately following a

description of the present competing technologies. For more comprehensive, in depth discussions of displays, the reader is referred to several recent reviews [19, 21, 27]. It should be emphasized that the aircraft market for displays will not have a significant impact on the development of display technologies, which will be oriented toward entertainment (including video games), and possibly toward automotive applications.

1. The Cathode Ray Tube (CRT)

Although the CRT is among the oldest of the display devices, it is unmatched in cost and quality for many applications and remains the standard to which all other displays are compared. The CRT is a vacuum device in which an electron-beam is deflected over a screen coated with a luminescent phosphor. The beam deflection, which is controlled by the input video signal, can be operated in either a raster-scan or random-access mode. In raster scan, the beam sweeps the entire display area line by line. This mode is preferred for complex displays and TV-type imaging. The random access mode directs the beam only to those parts of the screen where information is to be written, and is preferred for limited graphics and for character displays. In either case, the high peak brightness and relatively long persistence of the phosphor permits a high average brightness at scan rates of 1/30 second or

faster. This is important for cockpit displays, where ambient light can approach 10^5 lm/m². Tube phosphors have high uniformity and good dynamic range. Both black-and-white and color tubes are available, and a great deal of work on each tube continues. Efforts in black-and-white CRTs have recently concentrated on improving deflection sensitivity and on improving the writing speed. For high-resolution applications, tubes having diameters of 11 inches and resolution exceeding 40 lines/mm are available [22].

For airborne applications, the advantages of the CRT include widespread availability, high brightness, relatively simple drive requirements, and low cost. Its disadvantages include its relatively large size and weight, and the high voltage required for its operation. The CRT has a strong place in display technology and handles most jobs very well. In spite of developments in alternative technologies, the CRT continues to supply tough competition and is expected to be widely used for another decade or more.

2. The Light-Emitting Diode (LED)

Next to the CRT and perhaps the incandescent light, the LED is probably the most familiar and widely used display device. The diode here is formed in gallium phosphide (GaP), gallium arsenide (GaAs), or gallium arsenide phosphide (GaAsP) crystals formed epitaxially.

Red LEDs were the first to be widely available, but have now been joined by yellow and green devices. Recent work has centered on techniques for achieving improved efficiency and alternative colors. In GaP a major focus remains on the development of nitrogen-doped diodes for green-yellow emission, resulting in the maximum contrast as perceived by the human eye. Efficiencies, reproducibility, and uniformity are improving, and some progress using GaN diodes emitting in the blue has been reported.

LEDs continue to dominate the calculator market in spite of the relatively high current levels required to produce acceptable intensity. Several millamperes per segment is typically required. The diodes voltages required are in the range of a few volts or less so that LEDs interface well with many IC techniques, especially bipolar. Material quality is increasing, and costs are decreasing so that this technology promises to continue to enjoy wide use for some time.

3. Gas-Plasma Devices (GPD)

These devices have been undergoing intense development and are probably the most serious competition for the CRT in large panel displays. The device consists of parallel front and back plates containing orthogonal conductors. The space between the plates is typically neon mixed with an inert gas such as nitrogen. When a high voltage (150-200 volts) is

applied between the electrodes, a visible plasma discharge occurs. Both ac and dc operating modes are possible, and much recent work has concentrated on addressing techniques. Matrix addressing of some sort is typically employed so that each display element is at the intersection of a row and column. A sharp excitable threshold is essential and is present in this device. DC panels have no intrinsic memory but are preferred for TV applications due to the relative ease with which intensity can be varied.

The resolution limit of GPD displays is thought to be about four lines per millimeter and present resolution is about half that. Although most displays are red or orange in color, blue and green have also been reported. At least one 512 x 512 element panel is now available. At the present time, luminance levels are still relatively low and costs are high, partly due to the high drive voltages required. This technology should be watched closely as it develops for possible application in airborne displays.

4. Electroluminescent Devices (ELD)

This device consists of parallel electrodes, one of which is transparent, and an electroluminescent phosphor separating them to form a capacitor. When a high voltage is applied between the electrodes

(several hundred volts), the phosphor emits light. These displays are limited to a single color and typically operate in an ac mode. Thin-film transistor networks and capacitors provide the necessary threshold control and memory at each phosphor element, and the development of such large-area thin film circuitry is an important part of the development of this and several other display technologies [23,24].

These displays are still very exploratory, and have disadvantages in their high operating voltage and relatively short life (20,000 hours). Arrays containing 12,000 elements, contrast ratios greater than 50:1, and power consumption below one watt have been demonstrated [24].

5. Liquid Crystal Displays (LCD)

This is the first example of a passive display, i.e., one that does not emit light but rather controls the passage of light through the display. The liquid crystal material possesses a phase, in addition to the normal solid and liquid-isotropic phases, in which the material flows like a fluid but exhibits an anisotropic crystalline state. Materials forming this nematic liquid crystalline phase from -10°C to $+80^{\circ}\text{C}$ have been developed and are commercially available.

The liquid crystal material is usually contained

between two closely-spaced (less than 25 microns) plates, both of which are coated on the inside with a conductive film. The optic axis is aligned by specially treating the electrode surfaces. The front conductive film is etched corresponding to the pattern to be displayed and is transparent. The back film is either transparent or opaque and reflective, depending on whether the LCD is to be operated in a reflecting or a transmitting mode. In the latter case, a light source is mounted behind the display.

The electro-optical phenomena are of two types and occur when a voltage of a few volts is applied across the conductive films. In the first category, alignment of the LC molecules occurs via purely dielectric forces and therefore requires no appreciable current. Most research has been directed at these LC types due to their very low power and potential in electronic watch applications. In one dielectric effect (the so-called 'deformation of aligned phases' or DAP effect), uniformly-aligned nematic crystals are deformed under the influence of an applied electric field, changing the optical transmission of the film. The second type of phenomena are the so-called dynamic scattering types, in which reorientation of the LC occurs via electrohydrodynamic effects and which require an electric current.

Liquid crystal displays require only low voltages and very low currents in operation and have contrast which is relatively independent of ambient light level. However, viewing angle affects the perceived contrast and the response time is slow (100 msec), making drive of LCD matrices difficult. They are a strong contender for some character displays.

6. Electrochromic Displays (ECD)

Like LCDs, electrochromic displays are passive devices. As in other devices, ECDs employ parallel transparent plates on which appropriate electrode structures have been formed. The electrochromic material between the plates changes color under the application of a few volts between opposing electrodes and hence changes the color of the display. Contrast is excellent and wide viewing angles are permitted [25]. Both solid and liquid EC materials are being investigated and results are very promising; however, this area is still relatively new and much work is still proprietary. Response times are slow, in the range of 100 msec.

7. Electrophoretic Displays (EPD)

These displays use still a different electro-optical material. Here, pigment particles of one color are suspended in a liquid of another color. The pigment particles carry a charge, so that when exposed to an applied field, they move to the transparent surface

electrode or away from the surface, depending on the polarity. Since the pigment scatters light when at the surface, it has the ability to change the perceived color of the display. Like ECDs, EPDs operate at relatively low voltages. They are also very slow and there is concern regarding the long-term reliability of the structure. These displays are at a relatively early stage of development, but their suitability for airborne applications appears doubtful.

8. Ferroelectric Ceramic Displays (FCED-PLZT)

These displays use a transparent ceramic material-La-doped lead zirconate-titanate. The electro-optical effect here is either electronically-controlled light scattering or electronically-controlled birefringence, depending on ceramic grain size. In both cases, the applied electric field orients the ferroelectric domains, changing the optical properties of the material. Drive voltages here are higher (e.g., 40 volts) and the material must be excited transverse to the direction of transmission, causing fabrication difficulties. Poor contrast and stress-induced cracking are also concerns.

A brief comparative summary of these display materials is shown in Table 3. Comments on the suitability of these approaches for applications in aviation are given below.

Material	Present Resolution (lines/cm)	Ultimate Resolution (lines/cm)	Intrinsic Contrast	Response Time	Drive Requirements	Temperature Range, °C
LED	20	40	50:1	0.1μsec	1.4 - 4.5V 1.5 A/cm	wide
GPD	20	40	50:1*	1-10μsec	170 V. ² 160mA/cm	wide
ELD	8	40	50:1*	—	200-600 V. ² 30mA/cm	wide
LCD	40	100	15:1 to 50:1	20-200 msec.	5 V. ² 1μW/cm	-10 to +80
ECD	—	—	can be high [21]	100-500 msec.	<5 V. High Current	-20 to +70
EPD	—	—	20:1 to 40:1	~ 100 msec.	10-30 V. Low Current	-15 to +50
FCD/ PLZT	—	—	100:1	1-100μsec	30-50 V. microamps	—

* Time averaged.

TABLE 3: COMPARATIVE SUMMARY OF DISPLAY MATERIALS [19].

B. Alphanumeric Character Displays

Two general classes of displays will be considered: alpha-numeric character displays and TV-type imaging displays. If an imaging display is present in a system, it will undoubtedly be used for character display as well; however, it is likely that even in such systems, auxiliary alphanumeric displays will be required. These statements apply to both ground-based and airborne equipment.

For alphanumeric displays, low operating voltage and compatibility with relatively standard IC technologies is important. High contrast is also important, especially under conditions of varying and sometimes high ambient lighting as in a cockpit. Light-emitting diodes and liquid crystal displays are certainly the most highly developed technologies at present for alphanumeric displays, and this is their main area of application. LCDs have advantages in the low currents required and in the relative insensitivity of their contrast to ambient lighting variations, although contrast is viewing-angle sensitive. LEDs produce a sharper, more attractive display at present and the development of high efficiency yellow displays should enhance their attractiveness for aircraft use. Both LEDs and LCDs are widely available now and will be widely used during the 1980s. Prices, which are presently several dollars per character, should decline slowly as manufacturing techniques improve.

As for the other display techniques, none appears to offer significant advantages over LEDs and LCDs for general alphanumeric character displays.

C. Imaging Displays

The dominant technology for imaging-type displays continues to be the CRT, which combines high resolution, large display area, high contrast, and high brightness with low cost. The high beam voltage and relatively high ratio of tube depth to tube diameter are disadvantages. Efforts at developing new flat panel displays are aimed at overcoming these two disadvantages but all appear to require significant tradeoffs in other areas, e.g., resolution or cost. The gas plasma displays are undoubtedly the most developed and appear the most promising. The fast response and sharp device threshold simplifies drive requirements and the display permits a wide viewing angle. Reliability and lifetime are potentially better than for CRTs. Cost is still significantly above the CRT but should decline significantly as the technology matures. These displays are receiving substantial support from the TV industry. Display panels less than one-inch thick have been demonstrated using GPDs and this is important to the avionics industry. Drive voltage is reduced from several thousand volts for a CRT to less than 200 volts for the GPD; however, this is still too high for direct drive by most semiconductor technologies.

Many of the newer display technologies are not sufficiently mature to warrant comments on their potential for aircraft applications. Some are being developed in matrix form, but none appear to offer significant advantages over CRTs and GPDs for large area imaging displays. For small area imaging in portable equipment, LCD matrices are being pursued as well. More than one individual contacted during this study expressed serious doubt that any of the new displays offer any significant overall advantage over the CRT.

CRT displays will certainly continue to dominate the image display area for the next several years. GPDs will possibly become practical for aircraft applications by 1985 or before, when reduced resolution may be an acceptable trade for reduced size and weight. Motivated by the entertainment market and by the proliferation of data terminals for electronic systems, the display area promises to be very active during the next decade and should be watched closely by aviation.

D. The Auditory (Voice) Computer Interface

The dominant form of man-machine interface will likely continue to be the interactive terminal, consisting of a microcomputer-controlled imaging display (CRT) and a keyboard. In addition to this mode, however, it is of

interest to consider interaction via the other dominant sense - hearing. Simple auditory devices such as buzzers and tones will undoubtedly continue to be used for warnings and other signaling. They are inexpensive and familiar in these applications. For more complicated interaction, computer-generated voice output has been developed to the point where it is now practical for many applications. As microcomputer and memory costs decline, voice output should be practical for airborne avionics. At present, phrases are stored digitally in memory for recall by the processor. As this technology advances, storage of individual words may be feasible so that phrases may be synthesized directly by the machine. Voice output systems should be practical for avionics during the 1980s.

Voice input to computers is a more difficult problem, involving computer recognition of specific words in the face of regional accents and differences in pitch. Systems have been developed which recognize digits and a few words, but the cost is still very high and vocabularies are very limited. The first commercial systems were installed at Owens-Illinois, United Airlines, and TWA in 1973 and about 175 units are in service today [26]. Limited-vocabulary systems may be available for air traffic control by the mid-to-late 1980s, but it is unlikely that voice-entry systems will be available for airborne applications before the 1990s.

CHAPTER FIVE

AN UNCONSTRAINED TECHNOLOGICAL FORECAST OF MICROCOMPUTER SYSTEMS

I. Introduction

In the preceding chapters, the forecasts have treated large scale integration (LSI) at the component level, examining microprocessors, memory and some input-output devices.

Dramatic improvements in the speed, power, size, weight, and cost of microcomputers have been projected. In this chapter, the impact of these developments on LSI systems will be discussed. It is at the system level where component improvements impact the user and it is at this level where the real impact must be measured.

Microcomputers will certainly find wide application in many diverse areas. In fact, as mentioned earlier, the continued expansion of electronic markets is essential to the realization of the forecast growth. Although applications will be of many types, they have been divided into two broad categories--applications in instrumentation and control, and applications in data processing. Instrumentation applications can be expected to be the more numerous, and in these applications low cost, low power and small size will be important, while high speed will not be a major driving force. Single-chip microcomputers will find wide application in a variety of consumer, medical, industrial, automotive, and avionics instrumentation. Data processing applications will

apply microcomputers in many (probably most) applications now involving minicomputers and LSI will drastically change the characteristics of such equipment. On the low end, hand-held calculators will improve to the level of present minicomputers, while on the high end relatively large machines will be reduced in size and cost to the level of present minicomputers. In high-end microcomputers, market volumes will be lower (although much larger than present large computer market volumes) and speed will be an important driving factor on the technology.

In order to assess the impact of LSI on these two application areas, two microcomputer systems will be defined and their technological evolution will be forecast over the remainder of this century. The first system, which will illustrate microcomputer applications in instrumentation and control, will owe its feasibility to LSI microcomputer technology but will be heavily dependent for its evolution on a much broader range of technological developments. Such systems will have a revolutionary impact on airborne avionics, on automated maintenance activities, and on transportation in general. The second system, which will illustrate a relatively large, ground-based data processing facility, will show the impact of LSI technology on these more conventional computing applications.

In the following forecasts, no attempt to completely design the system is made; however, they are defined in block

diagram form, and their major components are identified. The forecasts then show the relative significance of the system component parts and how the dominant components are expected to change the system features over time.

II. Microcomputer Applications in Instrumentation and Control

A. Specifications for an On-Board System

Microcomputer-based systems will likely find numerous applications in on-board (airborne) instrumentation and control systems. As an illustration of one such system, the following functions are identified for possible inclusion:

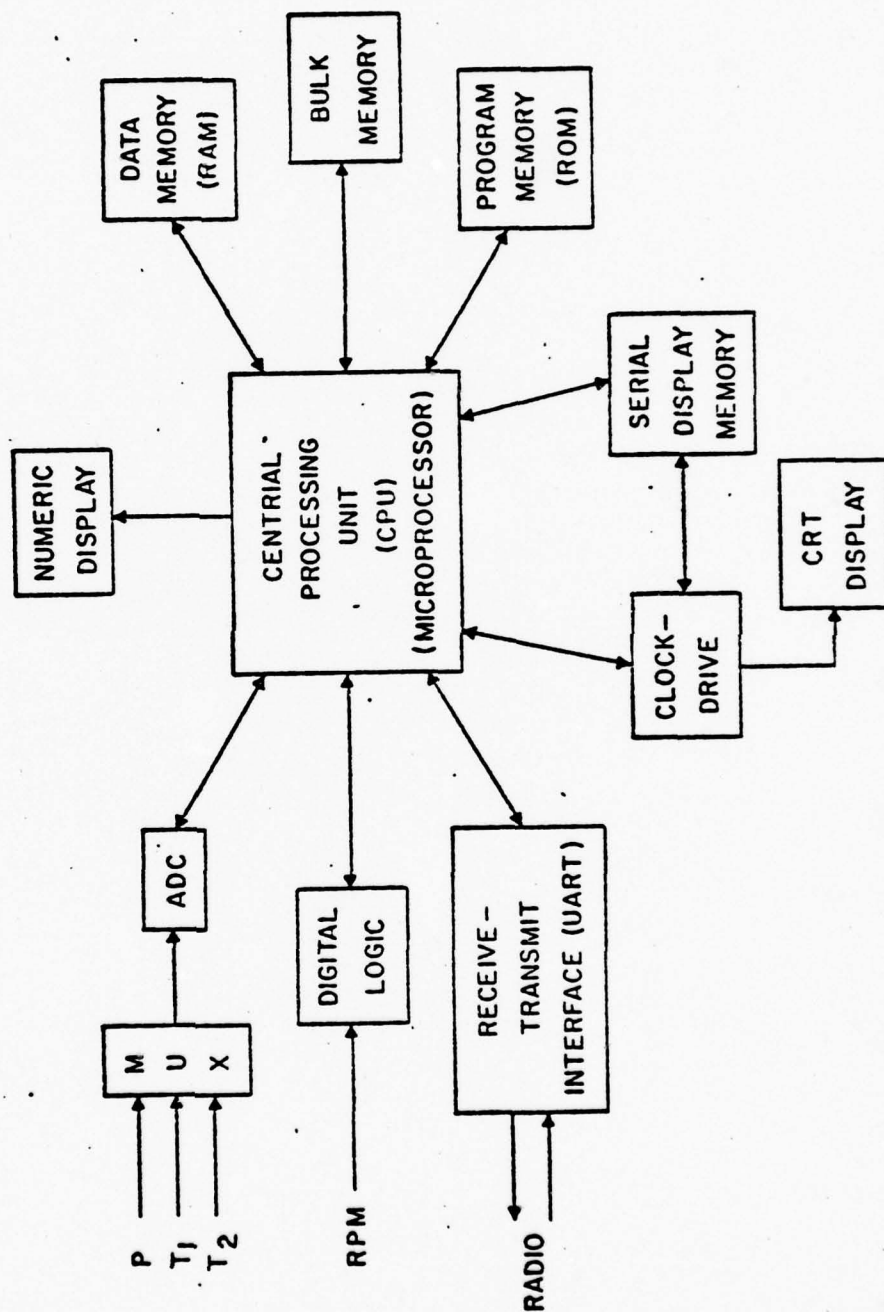
1. Altitude Measurement and Display. A number of altitude measurement techniques are possible. It is assumed that the system periodically measures barometric pressure, corrects it for the local reference pressure (received periodically over a data link from the ground), computes altitude, and displays the information on a numeric display. The system is completely automatic and requires no pilot involvement. Altitude information is updated as required (once per second or as selected).
2. Rate of Climb Measurement and Display. Using the altitude information, the system computes rate of climb (descent) and displays the information for the pilot. Analog or numeric display is possible; here numeric form is assumed.

3. Computation and Display of Optimum Power/Fuel Settings. Using measurements of engine rpm, outer air temperature, and engine manifold temperature, the system will compute the optimum power/fuel settings for the engine using manufacturer's engine data stored in the system memory. This information will be presented in numerical or graphical form to the pilot on a CRT-type display console.
4. Flight Diagnostics. A variety of operating data (engine time, temperature, fuel consumption, etc.) will be recorded during flight for automatic readout on landing as an aid to aircraft maintenance personnel.
5. Display of Operating Parameters. Many of the gauges used to display operating parameters (oil pressure, hydraulic pressure, etc.) could be removed and placed in memory for CRT as needed. Warning lights would identify problems. Display formats might vary but could show the present gauge format with a numeric readout beneath.
6. Sector Map/Aircraft Position. With the filing of a flight plan, the pilot might receive a disk or cassette containing updated weather and terrain information along his proposed route, including way points and airports. This information could be displayed on a CRT during flight with the aircraft position identified. Expansion of the sector map by quadrant would also be possible.

7. Landing Display. For IFR landings, the CRT could be used to display a simulated landing approach. Display data would be stored on-board in memory and moved to indicate aircraft position via an air-ground data link.

These functions are intended to indicate several general areas where airborne microcomputer-based instrumentation might be applied. Each area could be expanded or modified (and might need to be), and might serve as a total system in itself. Nevertheless, these functions are illustrative and sufficient to define the system shown in Figure 31. Three sensors (barometric pressure plus outer air and engine temperature) are read into the microcomputer via the analog multiplexer (MUX) and analog-to-digital converter (ADC) shown. Engine speed (in pulse rate digital form) is interfaced via a digital counter gated by the processor. Numeric information is displayed on an alpha-numeric (or numeric) display (altitude, rate of climb), while aircraft operating parameters, sector maps, and landing displays are displayed on a CRT. This display is assumed to use a CRT (cathode-ray tube) at least in the near term, but might be replaced by a flat panel (gas plasma) display in the future. This display will be assumed to operate in a raster scan mode and consist of a matrix of 512 lines of 512 points per line (262,144 elements per display). The screen is refreshed at a rate from 30 to 60 times

FIGURE 31: GENERAL AIRBORNE MICROCOMPUTER-BASED INSTRUMENTATION AND CONTROL SYSTEM



per second to avoid noticeable flicker. A serial refresh memory containing 262,144 bits controls the display on a point-by-point basis. Data for the display is obtained from a bulk memory under control of the microcomputer. The display can be modified on a line-by-line basis by the microcomputer. The data memory (RAM) and program memory (ROM) along with the microprocessor (CPU) will be assumed to make up the microcomputer. Interface with the ground is via an asynchronous receive-transmit interface and the aircraft radio (not shown).

This system exemplifies a fairly general airborne system which in this case is heavily involved in input-output operations and which involves a wide range of peripheral hardware.

The estimated memory requirements (in eight-bit bytes) by function are presented in Table 4.

A requirement for approximately 8K-bytes (65K-bits) of program memory (ROM), 512-bytes (4K-bits) of data RAM, and 512K-bytes (4 M-bytes) of bulk memory storage is estimated. These requirements are approximate and in some cases assume a system of "bare-bones" complexity. For example, the sector map is not moveable but has rather a fixed orientation (e.g., north-up). Work to more precisely define the system requirements for fixed and moveable map display systems is now underway at

TABLE 4: AIRBORNE SYSTEM MEMORY REQUIREMENTS
(8 bit-bytes)

	<u>RAM</u>	<u>ROM</u>	<u>Bulk Storage</u>
1. Altitude measurement, correction, and display	16	300	----
2. Rate of climb measurement	16	100	----
3. Optimum Power/Fuel Settings	96	1900	16K
4. Flight Diagnostics	64	1000	----
5. Operating Parameters Display (4)	16	1000	40K
6. Sector Map, fixed orientation, eight sectors stored	64	1000	256K
7. Landing Display	64	1000	50K
Miscellaneous routines	150	1500	100K
	<u>486</u>	<u>7800</u>	<u>462K</u>

NASA's Ames Research Center. In view of the need for and requirements of such systems, this work is important to future avionics as the present system will illustrate. With the system defined, proceeding to forecast its characteristics as a function of the technology used (e.g., 1985-technology) follows.

B. Unconstrained Forecast of System Characteristics

1. System Speed

In dealing with microcomputers as components, instruction cycle time (register-register add time) was a convenient measure of system speed. In dealing with a system, however, this measure may not be appropriate. In particular, with an instrumentation or control system it is important to measure speed in terms of the operations the system must perform. Accordingly, defined for this system are three measures of system speed: 1) time for a complete display (CRT) update; 2) time for interfacing with the ground (I/O); and 3) time for reading and interpreting an analog sensor. These measures will serve to identify the cost in real time of each type of function.

a) Time for Display Update/Change

The serial refresh memory autonomously rewrites the CRT 30 times per second or more. To change any particular line, e.g., to display a gauge, the line information is transferred from bulk

memory to refresh memory directly, following initial access (addressing) by the CPU and designation of the block of data (number of bits) to be transferred. A bulk data transfer then requires the CPU to designate the initial and final addresses for the transfer and to enable the transfer circuitry. The initial bit is accessed and successive bits are transferred in serial. The bulk transfer time will then be composed of CPU time, bulk memory initial access time, and bulk transmission time. This process assumes minimal CPU involvement, which is feasible for fixed orientations and fixed formats. As the CPU speed increases, it could take a more active role and some encoding of the bulk data could be used to effectively extend the system capabilities.

If instead of a bulk transfer to alter the entire screen, only a message is to be added, then only approximately 10 lines (5120 bits) must be altered in the refresh memory. First, the line to be altered is defined, and it is then written on a bit-by-bit basis. Characters and standard messages are assumed formatted in ROM to be called as needed. Line information is stored in a small parallel/serial-in, serial-out cache memory

for formatting and subsequent transmission to the refresh memory. For a typical line, it is assumed that one random access of the bulk memory is required (for messages). Other character storage is assumed to reside in ROM. A total of 12 characters or character blocks is assumed per line, each requiring approximately 50 CPU instruction cycles for formatting. Line transfer time thus is composed of one bulk memory access (or none if all messages are in ROM), 600 CPU cycle times, one serial refresh memory access time, and the time to transfer 512 bits serially into the refresh memory.

The microcomputer assumed for this system will use MOS technology, making it slower but also lower in power, size, and cost. After 1985, its speed should be comparable to the speed (instruction cycle time) forecast in Chapter Three for bipolar devices. For the bulk memory, a disk system is assumed initially, to be replaced by magnetic bubbles in the early 1980's. A serial charge-coupled (CCD) memory which is line or block addressable is assumed for the refresh display memory. It is noted that for a complete screen refresh 30 times per second, 262,144 bits in 33 msec or 126 nsec/bit is required, neglecting retrace times for the beam.

This is very fast in 1975 terms but should be available by 1980 and would allow complete digital beam control. A vector-scan (randomly addressable) CRT design would have some advantages for character display but disadvantages for some cockpit visual simulations. In 1975 technology using a small, relatively fast disk and an MOS processor having a 2.5μ sec instruction cycle and requiring 100 instructions for a bulk transfer, it is anticipated that a 10 msec (millisecond) disk access, 0.25 msec of CPU time, and 520 msec for bulk transfer of 262K-bits is required. For a line transfer, a disk access of 10 msec, 1.5 msec of CPU time to format 12 messages or characters per line, a refresh memory access of 0.1 msec, and a transfer time for 512 bits from cache memory to refresh memory of 0.5 msec at 1 M(mega)bit/sec writing rate is expected. Thus, the bulk transfer time for 512 lines (one display) is 530 msec and the line transfer time is 12.1 msec. Bulk transfer is limited by achievable bit rates from the bulk memory, while line transfer is dominated by the access time of the bulk memory. In neither case is the expected CPU time very significant, partly due to the semi-autonomous way the transfers are implemented. Table 5 presents forecasts of the

TABLE 5: FORECASTS OF ACHIEVABLE TRANSFER
SPEEDS FOR AIRBORNE SYSTEM

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Bulk memory access	10m	1m	0.2m	0.075m	0.02m
CPU instruction cycle	2.5 μ	0.4 μ	0.067 μ	0.015 μ	0.005 μ
Refresh access	0.1m	0.025m	0.005m	0.001m	0.001m
Serial bit rates (bits/sec) (from bulk memory)	0.5M	5M	12M	20M	40M
Bulk Transfer	530m	53m	25m	25m	25m
Line Transfer	12m	1.4m	0.3m	0.14m	0.06m
Message Transfer	120m	14m	3.0m	1.4m	0.6m

NOTE: all times in seconds

achievable speed for bulk (full screen) transfer, line transfer, and message transfer (10 line transfers) until the year 2000.

From the late 1980's on, the speeds for bulk transfer, and increasingly for line transfer, are limited by the required refresh rate for the display. This is assumed to be at a bit rate of about 10Mbits/sec, which is consistent with a refresh rate of 40 times per second. In other words, more speed is available than can be used in terms of bit rates after 1985. CPU time is a minor factor in both operations.

b) Time for Ground Interface

This factor will reflect the time required for the processor to handle data, including the time for data formatting, parity checks, and recording or displaying the data. The speed of external logic is expected to exceed that of the CPU so that CPU execution time will be dominant. Limitations imposed by the ground-to-air communications link are not included in these considerations. It is estimated that at least 20 instruction cycles, on the average, are required to format, interpret, and act on (or store) a byte of data from or to the ground. Messages might be temporarily stored in a

holding register prior to transmission, and a suitable 'hand-shaking' algorithm is assumed present to ensure an efficient interface. Based on the estimate of 20 instructions, the data rates listed in Table 6 are forecast as limited by the processor.

After 1985, the distinction between bipolar and MOS technologies has been dropped; the leading technologies at that time may well be merges of these two approaches. Overall, a speed increase of a factor of 50 is predicted over the next 25 years. In real terms, most messages (coordinates, landing data, weather information, on-board diagnostics, etc.) would constitute less than 100 bytes of code so that bytes per second divided by roughly a factor of 100 would represent a typical message rate for the processor. In 1975 this corresponded to message times of 0.5 msec and 5 msec, decreasing to 50 μ sec and 133 μ sec by 1985 and to 10 μ sec by 2000. In the near term, temporary holding registers to buffer the data transmission interface would likely be required to avoid interrupting the processor's duties for excessive periods of time and to avoid excessive commitments of ground-based equipment.

TABLE 6: AIR-GROUND DATA RATE
(bytes/sec) FORECASTS
FOR AIRBORNE SYSTEM

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Bipolar Processor	200K	830K	2M	3.3M	10M
MOS Processor	20K	130K	750K	3.3M	10M

c) Sensor Read Time

Air-ground communication is not expected to be frequent and would not consume significant amounts of real time except perhaps during takeoffs and landings. Visual updating of the display is also expected to be time consuming in real time primarily during takeoffs and landings. Thus, the load on the processor from the first two functions is highly nonuniform, and the processor must be capable of handling peak load (e.g., during landings). Reading and interpreting various sensors to monitor on-board systems will be more uniform over the time of a flight but significant real time will be available for other functions as well during flight. Sensor read time will depend on the type of sensor to be read. Analog-output sensors will require analog-to-digital conversion whereas digital-output sensors can be processed by digital logic, e.g., counting. The two functions will be treated separately.

For the present system, the pressure and temperature sensors are representative of sensors having an analog output. In order to read a given sensor, the processor sends the sensor address to the analog multiplexer to select the appropriate channel. After the voltage at the input to the converter has settled, the processor initiates a

conversion cycle, after which data is available in digital form to the processor for interpretation and display. The total read time, including processor interpretation and correction, is composed of CPU time and data conversion time.

It is estimated that to address the multiplexer, control the converter, correct the data for sensor nonlinearities or offsets, and display the data numerically would require on the order of 50 instruction cycles using a simple look-up table for sensor nonlinearities. Conversion time will depend on the desired accuracy and for this application, 10-bit accuracy is assumed sufficient (0.1%). A monolithic converter is assumed. The resulting read time for analog sensors is given in Table 7.

The total times allocated to a read operation assume that the processor idles while waiting for the ADC to respond. The discrepancy between instruction cycle time and conversion time is expected to grow, partly as the result of analog settling times and response times. Nevertheless, an improvement of nearly 200 times is expected in read time. While the read time for three sensors is not significant for these variables, the frequency with which read operations can be

TABLE 7: ANALOG SENSOR READ TIME
FORECASTS OR AIRBORNE SYSTEM

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
CPU time (μ sec)	125	20	4	0.8	0.25
Conversion time (μ sec)	40	10	2	1	0.6
	<hr/>	<hr/>	<hr/>	<hr/>	<hr/>
Total read (μ sec)	165	30	6	1.8	.85

performed is directly related to the ability of the system to follow time-varying parameters in real time. A signal having a 10 kHz bandwidth can be reproduced only if the read (sample) time is less than 50μ sec. Thus the read time determines the signal bandwidths which can be followed.

For a digital (e.g., time-analog or FM) output sensor, the sense parameter is transmitted as a pulse rate. The rate is determined either by timing a fixed number of counts or counting over a fixed time interval. Engine rpm is an example of a parameter which naturally lends itself to this type of encoding. Much of this approach can be handled by dedicated logic separate from the processor; the "conversion rate" is a function of the desired accuracy and the sensor output frequency. For 10-bit accuracy ($\pm 0.05\%$ of full scale), at least 1000 counts are required. If the maximum transmission rate from the sensor to the processor is 5 million counts/sec, then we require 200μ sec to accumulate 1000 counts (full scale). The processor is expected to require about 50 instruction cycles to process the data as for the analog sensors. In this case the processor would not wait for the counts to be accumulated so that in terms of CPU time, the sensor read times for these

two types of sensors are comparable. In terms of the ability to follow a signal in real time, the analog format has speed advantages, with the maximum bandwidth limited by the bandwidth of the interconnecting bus.

d) Concluding Comments on System Speed

Examining the three measures of system speed which have been described, none occupies significant processor real time during flight unless the sensor interrogation rates or display update rates are in the kilohertz range. Expected loads during flight can be handled by present as well as future systems. Future improvements in system speed can be used to eliminate peripheral circuitry, allowing more direct processor control of functions. Particularly for in-flight operations involving primarily computational activities, there is plenty of room for additional features in the present system. Plotting aircraft position and displaying it continuously on the fixed sector map could be accommodated easily, and by the mid-80's moveable map displays should be possible using existing microcomputers. It is concluded that speed will not be a barrier to sophisticated electronic systems for on-board instrumentation and control applications. Figure 32 summarizes the speed performance of this system as a function of time.

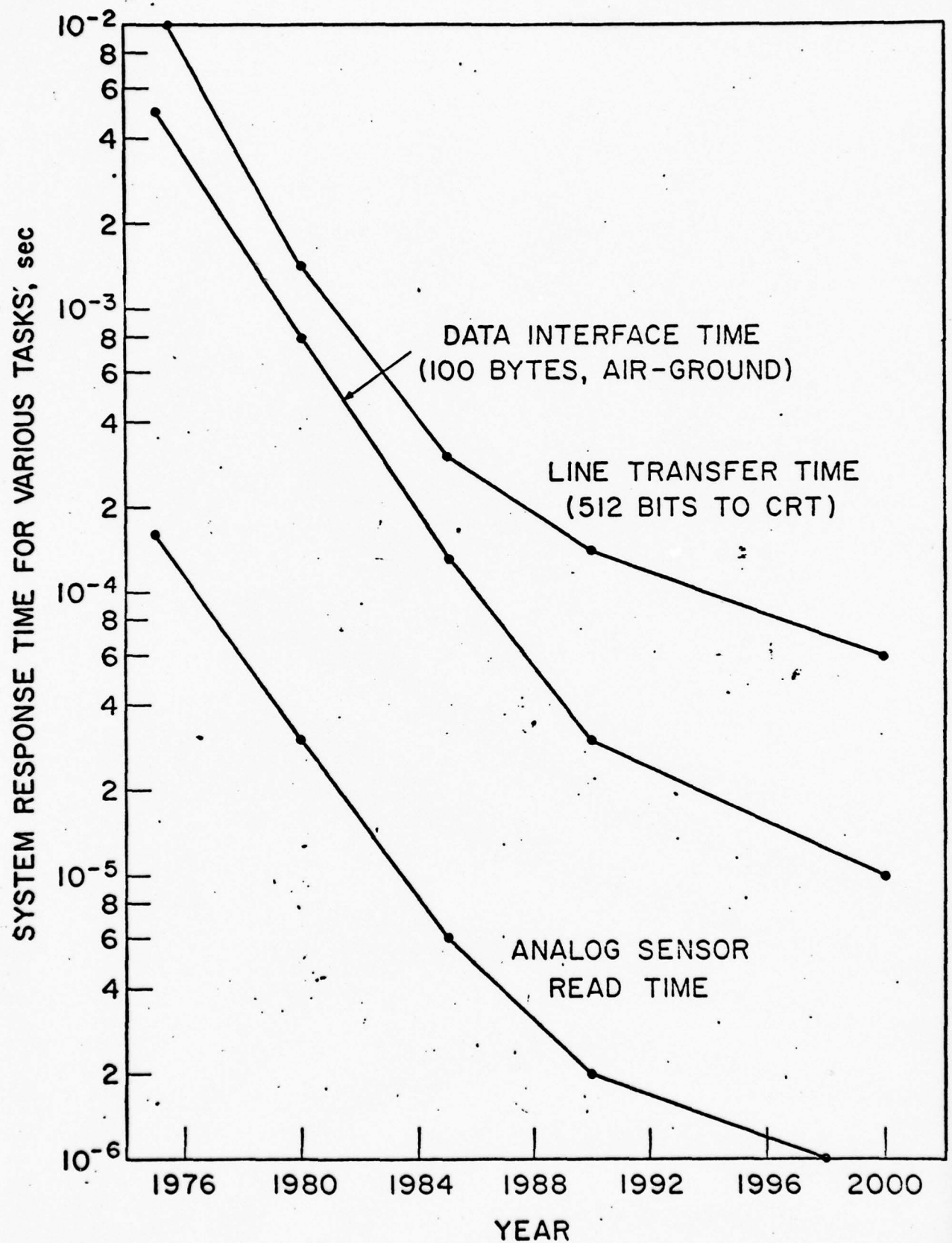


FIGURE 32: SYSTEM RESPONSE TIME

2. System Power

In estimating system power, each of the component parts must be considered. The sensors can be expected to dissipate relatively little power, and 10mw will be allocated for each of the designated sensors. The numeric displays represent 3mA per segment (50 mw per digit) in LED form and less in other display technologies. Assuming 20 continuously-illuminated digits, the total display power in 1975 LED technology is 1 watt. It is expected that three voltage levels will be sufficient to operate the entire system (e.g., +12, -5, and +5 volts) in addition to the CRT beam voltage. For a CRT display, a 10 to 12-inch tube has a power dissipation of approximately 80 watts, including its associated drive circuitry. The serial display memory composed of sixteen 16 kilobit CCD memory chips (1975 technology) would contribute about 10 watts of this power. After the early to mid-80's, the CRT may be replaced by a flat panel (gas plasma) display.

The RAM, ROM, and bulk memories associated with the microcomputer portions of the system each have different power levels per bit. The CPU power will depend on the number of gates involved. The assumption will be made that for the system described, a

processor having 5000 gates is adequate. This is equivalent to the larger second-generation processors in 1975 technology. Until 1985 it is assumed that CPU power is constant at about 0.5 watts while speed is enhanced by the smaller dimensions. Compared to the power consumed by displays, this level is negligible.

For a disk memory of 4 megabit capacity, a power of 50 watts or more will be dissipated in the drive. Its bubble replacement will dissipate about 20 watts in 1980 and less thereafter. A 4 K-bit RAM and 64 K-bit ROM in 1975 could be expected to dissipate approximately 0.5 watts and about 4 watts, respectively, in n-channel MOS technology and much less in CMOS. Thus the memory power for the system is dominated by the bulk storage medium but is still low compared with the display.

The power dissipation in the processor will depend on the technology chosen for its implementation and on its complexity. As pointed out above, 0.5 watts and 5000 gates are typical levels for n-channel MOS technology. In an airborne application such as that described, the enhanced functional capabilities achieved via higher speed are probably more desirable than saving power in the processor

and its memory. Hence, power is assumed to remain roughly constant as speed increases. Functional complexity (number of CPU gates and memory bits) is taken as constant (see Table 8).

System power is expected to decrease by about 60 percent over the next 25 years for this system. In 1975, the microcomputer, bulk memory, and displays account for about 3.6 percent, 36 percent, and 58 percent of the total, respectively. These numbers become 6.5 percent, 19.5 percent, and 72.7 percent, respectively in 1985. After 1985 some power reduction in the CPU is taken as opposed to strictly increasing speed, while continued slow progress shrinks the display power as well so that the percentages are approximately 4.2 percent, 18 percent, and 77 percent in the year 2000. Figure 33 summarizes power consumption in this system over the remainder of this century.

The message here is clear. Although the microcomputer makes this system feasible through its low cost and high functional complexity, it contributes a negligible amount to system power requirements. Bulk memory is much more significant; however, the replacement of the disk memory with its relatively high drive power by a bubble memory (or CCD) can be expected to decrease power as well as do away with moving parts. Bubble power could likely be reduced still further by operating in a standby mode when inactive, since

TABLE 8: AIRBORNE SYSTEM POWER (Watts)
FORECAST BY YEAR

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Bulk Memory	50	20	15	12	10
Serial CCD Display Memory	10	8	6	4	2
RAM (4K bits)	0.5	0.5	0.5	0.3	0.2
ROM (64K bits)	4	4	4	3	2
Microprocessor	0.5	0.5	0.5	0.3	0.1
Sensors	0.04	0.04	0.04	0.04	0.04
Numeric Displays	1.0	0.5	0.4	0.4	0.4
Panel/CRT Display	70	60	50	40	40
Misc. Interface Circuits	2.0	1	0.4	0.1	0.1
	<hr/>	<hr/>	<hr/>	<hr/>	<hr/>
	138	95	77	60	55

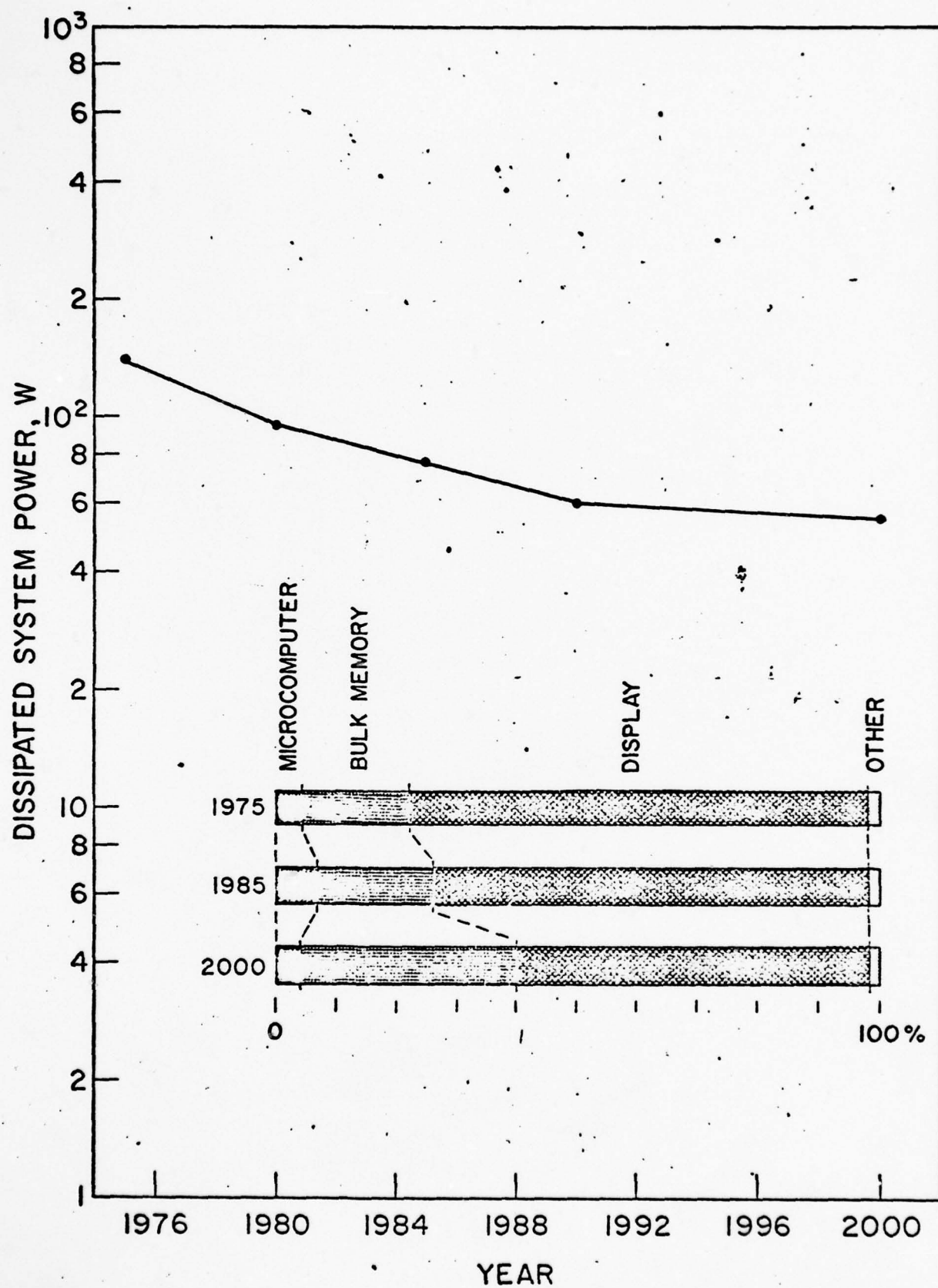


FIGURE 33: System Power Consumption

bubbles, unlike CCD's, need not be continuously recirculated. Power in this system is clearly dominated by displays, which is expected to decrease slowly as more efficient materials are developed. Cathode-ray tubes will possibly be replaced by some sort of flat panel display but more for size, weight, and reliability considerations than for lower power.

3. System Size

System size will be dependent on component complexity and on the packaging medium used. Power dissipation will limit the component density at the chip level. In 1975, the CPU, RAM, and ROM constitute a total of 20 circuit packages. In 1980, the RAM will be on the CPU along with some ROM, and the package count for the microcomputer will reduce to 10. Subsequently, the system changes as shown below.

The bulk memory in 1975 would typically consist of a dual drive disk; in the early 1980's it is replaced by a bubble memory unit composed of 128K-bit chips, followed by a unit based on 256K-bit chips by 1985. The ADC, UART, counter, and miscellaneous interface circuits constitute at least 60 SSI/MSI packages in 1975. By 1980, this drops to 20 and to 10 by 1985. The alphanumeric displays are assumed panel mounted on the front surface of the system beside the CRT/panel display. The CRT is assumed to occupy a 10 x 12-inch panel area.

Packaging is available for the circuitry in several forms. The most dense form is wirewrap, which allows up to 60 SSI/MSI packages in approximately 100 cubic inches. Interconnections are via 3-dimensional point-to-point wiring. Such boards are dense and reliable but also expensive (\$100 each with sockets and connectors, 1975). Alternatively, less dense and less expensive printed circuit cards can be used. It is assumed that this latter mode, will have a density of 30 MSI packages per 100 cubic inches or 15 LSI packages per 100 cubic inches (see Table 9).

Again, looking at the size consumed by the microcomputer, the bulk memory, and the display (including refresh memory), the percentages are; 3.2 percent, 20 percent and 35 percent in 1975, 5 percent, 17 percent, and 27 percent in 1985, and 3.4 percent, 6.8 percent, and 36 percent in the year 2000. These figures are shown graphically in Figure 34. With an estimated panel area of 14 x 16 inches (224 square inches), the depth of the console is 10 inches in 1975, decreasing to about 3 inches (one circuit board) in 1990 and beyond.

In actual implementation, the system size might be somewhat larger as dictated by convenience, human interface and packaging considerations, but the implication that the system will nonetheless be very

TABLE 9: AIRBORNE SYSTEM SIZE FORECAST

<u>System Part</u>	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
1. Microcomputer	[2]+(18) 80	[2]+(8) 40	[2]+(8) 40	[2]+(4) 30	[2]+(2) 20
2. Bulk Memory	500	300	[16]+(8) 140	[8]+(4) 70	[4]+(4) 40
3. Serial Display Memory	(24) 80	(12) 40	2 15	2 15	1 10
4. Miscellaneous circuits	[10]+(50) 250	[10]+(10) 100	[5]+(5) 50	[5]+(5) 50	[5]+(5) 50
5. Display (incl drive)	800	800	200	200	200
6. Power (Watts)	300	250	200	175	150
<hr/>					
Total component vol. (IN ³)	2010	1530	645	540	470
+25% for packaging	400	380	160	135	120
Total System Size:	2510	1910	805	675	590

[] = #LSI packages
() = #SSI packages

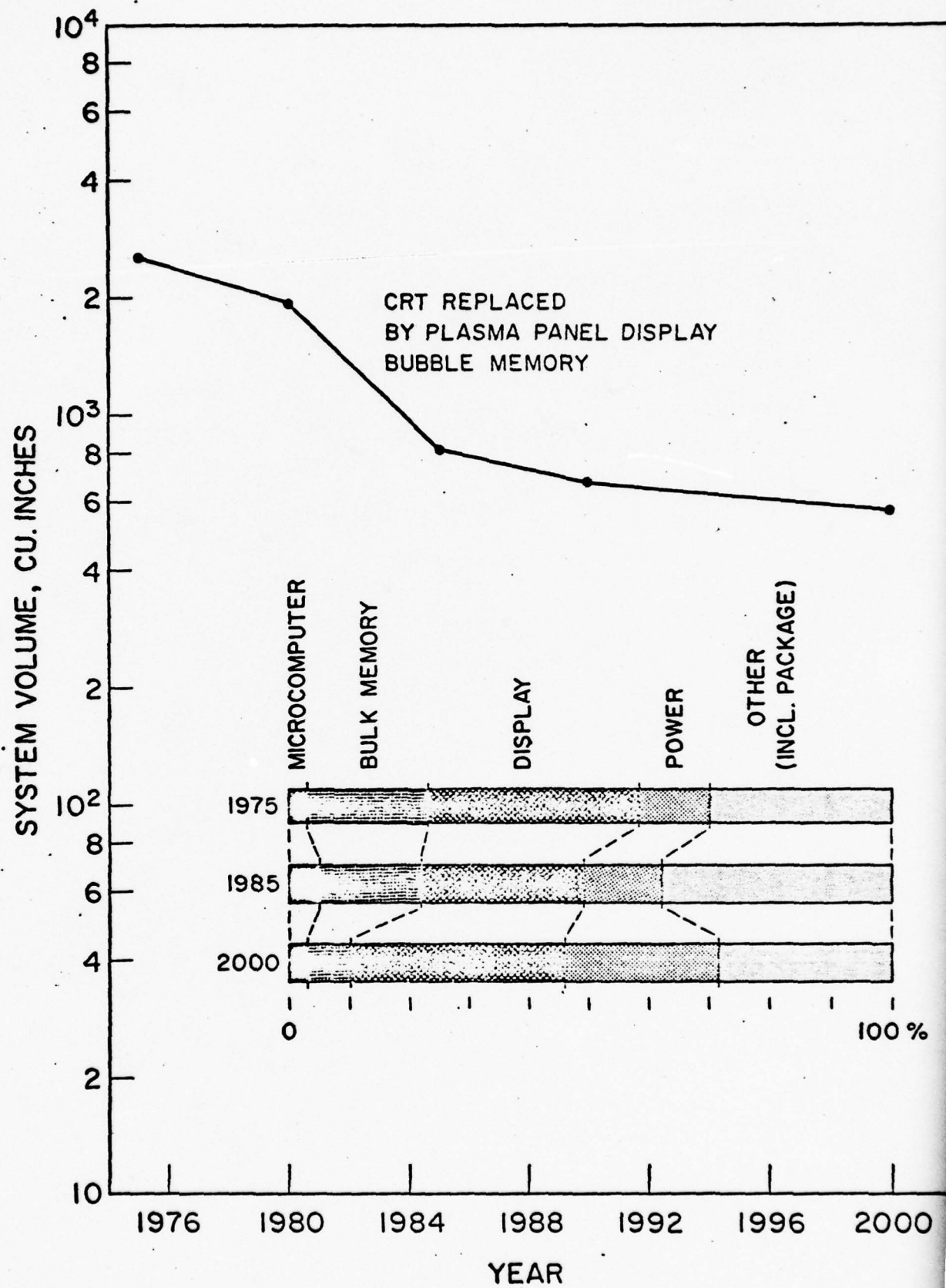


FIGURE 35: SYSTEM VOLUME

small is clear. The largest factor in system size is the display itself, and the possible reduction in depth from a 10-inch-deep CRT to a 2.5-inch-deep flat panel display about 1985 has a significant effect on the system. Again, the entire microcomputer represents only a few percent of the system volume.

4. System Weight

System weight can be estimated from the size information given above and from the measured and published weights of the component parts. Future systems are scaled in accordance with the size projections. The results of these considerations are given below and are summarized in Figure 35.

For components, a 100 cubic inch circuit board volume containing 30 MSI packages is estimated to weigh about 0.5 lbs. A chassis enclosing a volume of 2000 cubic inches will weigh about 10 lbs., and as volume decreases, weight will decrease as the $2/3$ power due to the different dependencies on dimension. The chassis and power weights given in Table 10 decrease with time reflecting the reduced size and power requirements of the system. The power assumes DC-DC converters having an efficiency of 50 percent. In this sense, the previous power levels ignore the inefficiency with which the three voltages (± 5 and

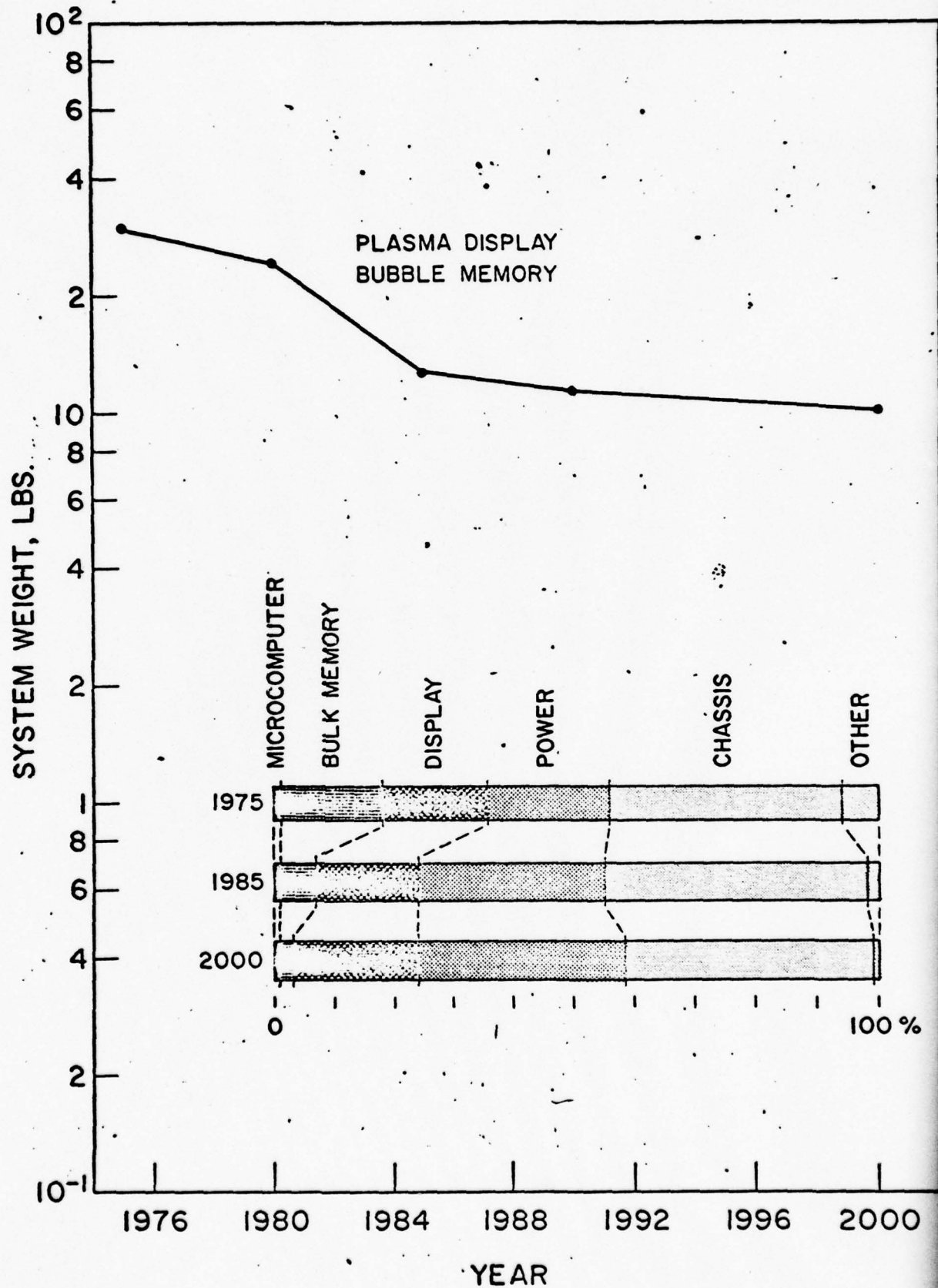


FIGURE 35: SYSTEM WEIGHT

TABLE 10: AIRBORNE SYSTEM WEIGHT (lbs) FORECASTS VS TIME

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Microcomputer	0.4	0.2	0.2	0.15	0.1
Bulk Memory	5	4	0.7	0.4	0.25
Display Memory	0.4	0.2	0.1	0.1	0.1
Display	5	5	2	2	2
Interface Circuits	1.25	0.5	0.25	0.25	0.25
Power Sources	6	5	4	3.5	3
Chassis	11.5	9.5	5.5	4.75	4.5
	<hr/>	<hr/>	<hr/>	<hr/>	<hr/>
Total	29.95	24.4	12.75	11.15	10.2

+12) are generated. System power requirements to the aircraft could approximately double from those previously given.

5. System Cost

In earlier sections of this report, the cost of LSI components (microprocessors and memory) have been forecast. As in that case, this section treats cost in constant 1975 dollars; however, the cost is treated at the system level. This necessitates considering the costs of a wide variety of other components, assembly, wiring, and testing costs (A, W, and T), and design costs. As in the other sections of this chapter, the emphasis here will be on identifying dominant cost elements. No attempt is made to perform an extensive or exhaustive cost analysis in all areas. It is also assumed that of primary interest is the cost of manufacturing the system (not the selling price), and that the system uses state-of-the-art production components purchased in moderately high volumes. The cost of the major circuit components are inflated a factor of 2 from the estimates of previous chapters to reflect probable lower-than-defect-limited yields. In all cases, the use of standard commercial components is essential.

a) Component Costs

The component costs for this system are

summarized in Table 11. These costs are based on present costs for similar components in volume production and on projected component developments.

These cost projections assign \$20 to the CPU in 1975, \$10 in 1980, and \$5 thereafter. The serial refresh (display) memory is estimated at 0.15 cents/bit in 1975 when the CCD serial memories were relatively new, dropping to 0.04 cents/bit in 1980, 0.008 cents/bit in 1985 and 0.004 cents/bit thereafter. Bulk memory cost is estimated at a probably-conservative \$500 in 1975. Values after 1980 are for assumed bubble memories. Display costs reflect the numeric readouts as well as the cost of the CRT itself. Interface electronics assume \$2 for an MSI circuit and \$5 for an LSI circuit, with ADC costs dropping from \$40 (1975) to \$10 (1980) and \$5 in 1985 and thereafter. Printed circuit board cost is assumed to be \$15 for a double sided board of about 50 square inches. Only the pressure and temperature sensors are included in these cost estimates and their cost reductions are partly the result of anticipated needs in the automotive area.

As shown above, the system costs for electronics,

TABLE 11: AIRBORNE SYSTEM COMPONENT
COST FORECAST VS TIME

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Microcomputer	\$ 150	\$ 51	\$ 36	\$ 28	\$ 21
Interface Electronics	190	75	35	30	25
Bulk Memory	500	400	200	150	120
Display Memory	393	104	40	20	10
Display	110	85	75	65	50
Sensors	60	40	20	15	15
PC Boards	60	45	35	30	20
Power Supply	325	280	150	120	100
Chassis	<u>75</u>	<u>60</u>	<u>40</u>	<u>35</u>	<u>35</u>
Total components	\$1,863	\$1,140	\$631	\$493	\$396

bulk memory, display, and power go from 41 percent, 28 percent, 6 percent, and 18 percent in 1975, respectively, to 18 percent, 33 percent, 12 percent, and 25 percent in 1985 and drop to 15 percent, 31 percent, 13 percent, and 26 percent by the year 2000. Clearly, the most dramatic drop is in the electronics. The display and chassis costs are expected to decline relatively little, and the declines noted in chassis costs are due largely to the size reductions possible as electronics and display technologies advance. Although these component costs are approximate at best, the hardware costs can be expected to shrink from about \$400 by the year 2000 - a cost reduction of a factor of 5.

b) Assembly, Wiring, and Testing Costs (AW&T)

AW&T charges for system assembly in 1975 are presented by component below and in Table 12 and 13.

\$ 7.00 per board
 .25 per MSI package
 .35 per LSI package
10.00 per module

The AW&T charges are listed in Table 13.

Hence the AW&T charges on the system are nearly constant with time at about \$100 in spite of reduced system component count. This reflects anticipated increased charges for assembly operations - particularly those involving manual operations.

TABLE 12: ASSEMBLY, WIRING AND TESTING
COSTS FORECASTS FOR AIRBORNE
SYSTEM COMPONENTS

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
PWB	\$ 7.00	\$ 10.00	\$ 15.00	\$ 18.00	\$ 20.00
MSI package	.25	.30	.35	.40	.40
LSI package	.35	.40	.45	.45	.40
Module	\$ 10.00	\$ 12.00	\$ 14.00	\$ 18.00	\$ 20.00

TABLE 13: ASSEMBLY, WIRING AND
TESTING COST FORECAST

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Microcomputer	\$ 5.20	\$ 3.20	\$ 3.70	\$ 2.50	\$1.60
Display Memory	6.00	3.60	.90	.90	.40
Bulk Memory	10.00	12.00	10.00	5.20	3.20
Display	10.00	12.00	14.00	18.00	20.00
Interface Elec.	16.00	7.00	4.00	4.25	4.00
Chassis	10.00	12.00	14.00	18.00	20.00
PC Boards	28.00	30.00	45.00	36.00	20.00
Power Supply	20.00	24.00	28.00	18.00	20.00
	<u>\$105.20</u>	<u>\$103.80</u>	<u>\$119.60</u>	<u>\$102.85</u>	<u>\$89.20</u>

c) Design Costs

Design costs will tend to increase due to anticipated increases in labor rates for such individuals; however, as the level of system integration increases and as improved design aids are developed, the design time is expected to decrease resulting in a system design cost which declines slowly over time. In 1975, it is estimated that the system described could be developed in about 4 man-years ($2\frac{1}{2}$ hardware, $1\frac{1}{2}$ software) at about \$50,000 per man-year. The total design cost would thus be about \$200,000. These design costs could be reflected in the final system cost in a variety of ways. It is assumed that complete recovery of design costs is achieved in the first 1000 systems. Using this assumption, the hardware, AW&T, and design costs are listed in Table 14. Total system cost is presented graphically in Figure 36, where the major cost components are again identified.

III. Microcomputer Applications in Data Processing

A. Specifications for a Ground-Based System

Many applications for microprocessors in ground-based systems will be oriented toward data processing. Among the possible system applications are the following:

- 1) Air traffic control
- 2) Airport administration

TABLE 14: TOTAL AIRBORNE SYSTEM
COST FORECAST

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Hardware	\$ 1863	\$ 1140	\$ 631	\$ 493	\$ 396
AW&T	105	104	120	103	89
Design	<u>200</u>	<u>200</u>	<u>150</u>	<u>150</u>	<u>100</u>
	\$2168	\$1444	\$ 901	\$ 746	\$ 585

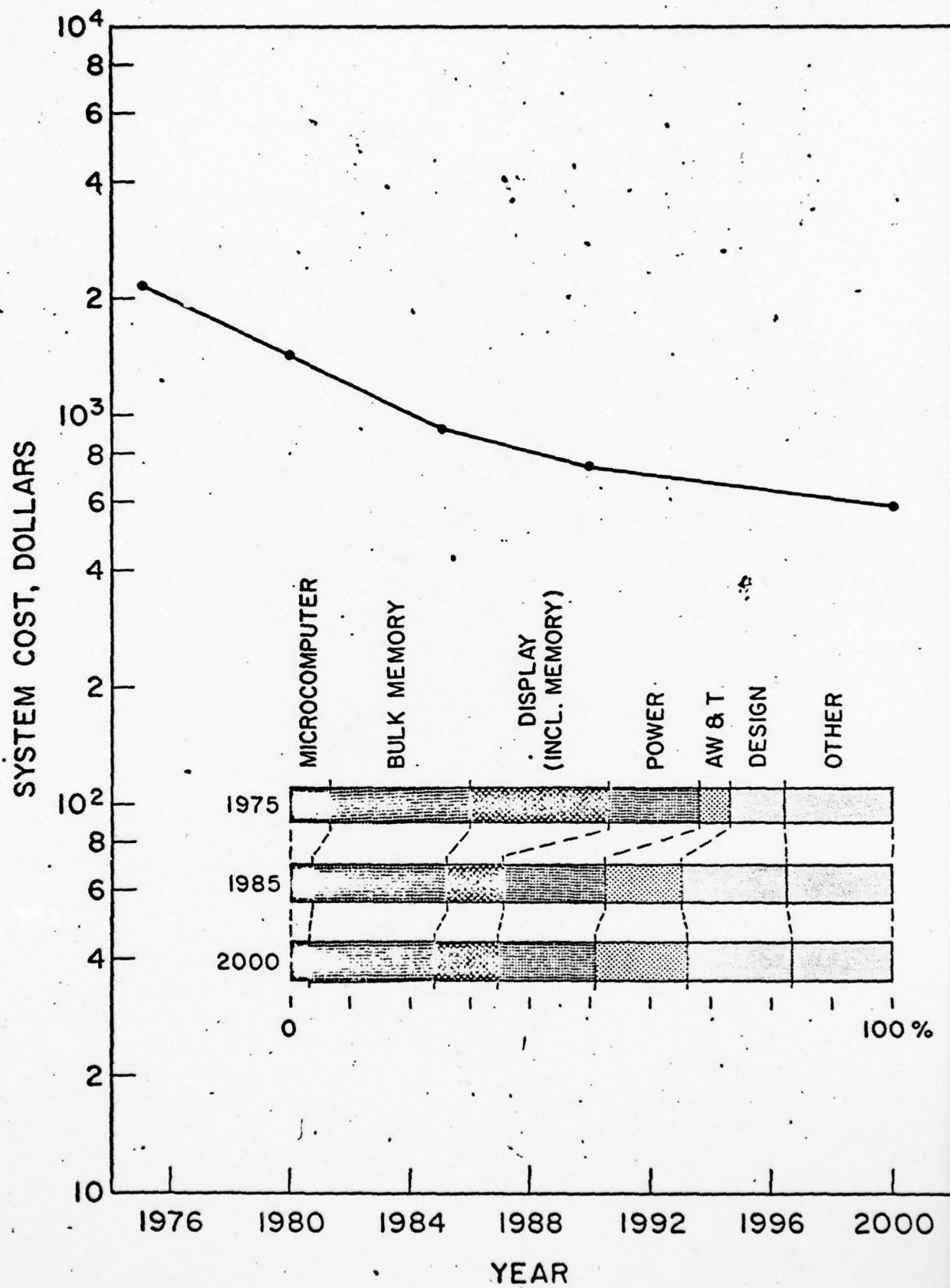


FIGURE 36: SYSTEM COST

- 3) Flight plan preparation (including sector maps)
- 4) Airport and Aircraft maintenance

All of these functions are heavily oriented toward data processing or record keeping and less toward input/output functions. It is expected that 'satellite' microcomputers will exist in all printers and terminals which interface with the ground-based central processor and that the CPU may well consist of a number of microcomputers, each dedicated to one of the above functions. System through-put and cost will be a function of microcomputer performance and for this system, unlike the airborne system, concentration will be on the speed, power, size, weight, and cost of the microcomputer itself. The cost of computer terminals will diminish over the coming 25 years, perhaps by a factor of 3 or 4, but developments in microcomputers and memory will motivate these reductions and they themselves will enjoy more dramatic reductions in cost.

Although these functions are not handled at present by microcomputers, it is important to assess the impact of LSI technology on this area since in the future microcomputers will be capable of handling many or all such functions. As with the airborne system, the approach here will be to first define the system and then forecast its size, weight, speed, power, and cost over the remainder of this century. Since this system

is primarily devoted to data processing, primary focus will be on the computer and not on its peripherals, which are equally important but beyond the scope of this work. Therefore, very large machines (by present standards), similar to the IBM 370/168 or 370/195 will be deliberately considered. These are clearly capable of handling the above functions but are hardly microcomputers at the present time.

System Features: CPU Complexity: 200,000 gates

Memory (RAM): 4 megabytes
(32 megabits)

The speed of the system will be partly dependent on the mix between serial and parallel processing and also on the gate delay itself. This mix will determine the number of gate delays per instruction cycle. For hardware oriented designs (slower gates but more of them, some parallel processing), this number will be about 30, while for smaller speed-oriented designs (faster gates, fewer of them, but more serial processing), it will be closer to 100.

B. Unconstrained Forecast of System Characteristics

1. Speed

The Rein Turn algorithm will be used (Ch. 3 [49]) to relate instruction cycle time to gate delay.

This approach defines a typical machine-language program to be made up of 70 percent add-type instructions (100 gate delays) and 30 percent multiply-type instructions (300 gate delays). At the gate and

the system levels, gate delay and hence instruction cycle time will depend on the power per gate and the system can be optimized either for speed or for size, weight, power, and cost since power will determine the allowed component densities. For this system a constant power level of 10^{-4} watts per gate will be assumed, consistent with Figure 12, and allow speed to develop accordingly. Since the CPU contributes relatively little of the system power, this does not fix system power, size, or weight which are determined more by the memory requirements. It is assumed here, as in Chapter Three, that the memory is transparent to the processor, i.e., that memory access time is significantly faster than CPU instruction cycle time so the processor does not have to wait for the memory. This will likely be true for serial processors (uniprocessors) and should be assured as pipeline architectures are applied.

A power level of 10^{-4} watts/gate is 200 times lower than the power levels of existing large machines, which use less dense (and in terms of power-delay product, less efficient) logic technologies, running with subnanosecond gate delays and machine instruction cycles of about 50 nanoseconds. These existing machines will be contrasted with the LSI system over

time. The CPU and memory sizes are similar.

In evaluating system speed, the gate delay at the assumed power level is estimated from Figure 12. The effective instruction cycle time is then calculated from the above-stated assumptions and the speed is expressed in terms of millions of instructions executed per second (MIPS). If t_D is the gate delay and t_C is the effective instruction cycle time, then

$$\begin{aligned} t_C &= 0.7(100t_D) + 0.3(300t_D) \\ &= 160t_D \end{aligned}$$

$$\text{MIPS} = \frac{1}{t_C} \quad (t_C \text{ in microseconds, } \mu\text{sec}).$$

The calculated speed of this system is shown in Table 15.

At the present time, the Amdahl 470 V6 system runs at a gate delay of 0.6 nsec and achieves, by the above algorithm, a speed of 10.4 MIPS. This is equivalent to the IBM 370 systems but at reduced size and power. However, this present system runs at a level of about 2×10^{-2} watts per gate (Amdahl 470).

Figure 37 summarizes the forecast speed for the present system.

TABLE 15: GROUND BASED SYSTEM
SPEED FORECAST VS TIME

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Gate Delay (nsec)	10	2	0.8	0.4	0.15
Effective cycle time (μ sec)	1.6	0.32	0.13	0.064	0.024
MIPS	0.63	3.13	7.81	15.63	41.67

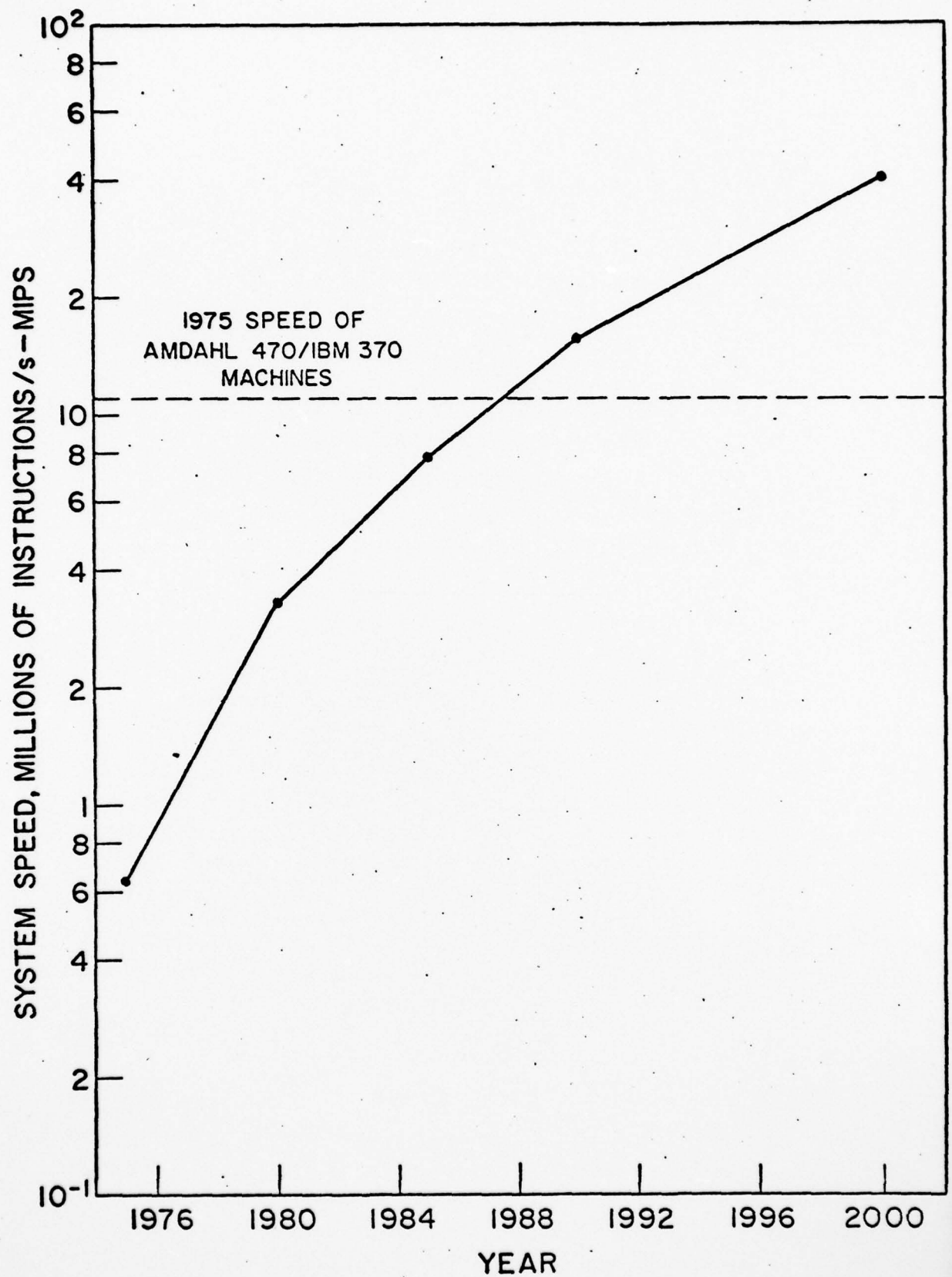


FIGURE 37: SYSTEM SPEED

2. System Power

Since the system is being optimized for speed, the power dissipation limits of the package will limit the gate density in the CPU and hence its size, weight, and to some degree its cost. In the memory, power gating is assumed so that only 25 percent of the memory is active at any one time while the rest is in standby. Dynamic circuitry in standby need only be refreshed periodically so that its active/standby duty cycle is only about 2 percent. Thus a 25 percent active/standby ratio is conservative and should support the fast access required. As stated in Chapter Three, it is anticipated that power can be held within package limits as memory speed and capacity increases. In Table 16, the technologically possible gate densities are given in parentheses, while the actual assumed densities (gates/chip) as limited by power dissipation are also shown. Chip size, which could increase, actually declines rapidly. The CPU power here is constant at 20 watts, while the memory power declines as shown in Table 16.

Gate area in this forecast is taken from Figure 9, and it is noted that were it not for power restrictions, the entire CPU would fit on a single chip. Hence if the speed requirements could be relaxed, this would be a real possibility by 1985. The

TABLE 16: GROUND BASED SYSTEM POWER
FORECAST VS TIME

<u>CPU</u>	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
Gate area (sq.mils)	10	2	0.35	0.08	0.02
Chip area (sq.mils)	20K	20K/(35K)	5.3K/(70K)	1.6K/(90K)	1.6K (120K)
Gates/chip	2K	10K/(17.5K)	15K/(200K)	20K/(1125K)	25K (6000K)
Power/chip	0.2	1	1.5	2	2.5
Packages/CPU	100	20	14	10	8
<u>Memory</u>					
Bits/chip	4K	16K	64K	128K	256K
Power/chip	0.5	1	1.5	2	2
# Chips	8K	2K	500	250	125
CPU Power	20	20	20	20	20
Memory Power	1K	500	375	250	125
Total Power (watts)	1,020	520	395	270	145

number of memory bits per chip is taken from Figure 21, but is somewhat more pessimistic, reflecting the needed speed improvements beyond the data presented there. Figure 38 shows the system power over time. It is to be noted that an IBM 370/168 CPU dissipates about 67 K watts and that the Amdahl 470 V6 with a 2 megabyte memory requires a similar amount.

3. System Size

System size is shown in Figure 39 over time. System size is dominated by the memory, where relatively dense packaging of 30 circuit packages per 100 cubic inches is assumed. The power dissipation density is well within the limits for air cooling listed by Turn (Ch. 3 [49]) and ventilation fans might not be needed. System volume declines from about 16 cubic feet in 1975 to one cubic foot by 1985. The procedures in arriving at system size are based on the assumptions stated for the airborne system and are similar to those used in the book by Turn. The CPU alone in the Amdahl system occupies about 60 cubic feet compared to 200 cubic feet for the IBM 370. The CPU for the present system in 1975 technology occupies 0.4 cubic feet.

4. System Weight

System weight is forecast in Figure 40, based on

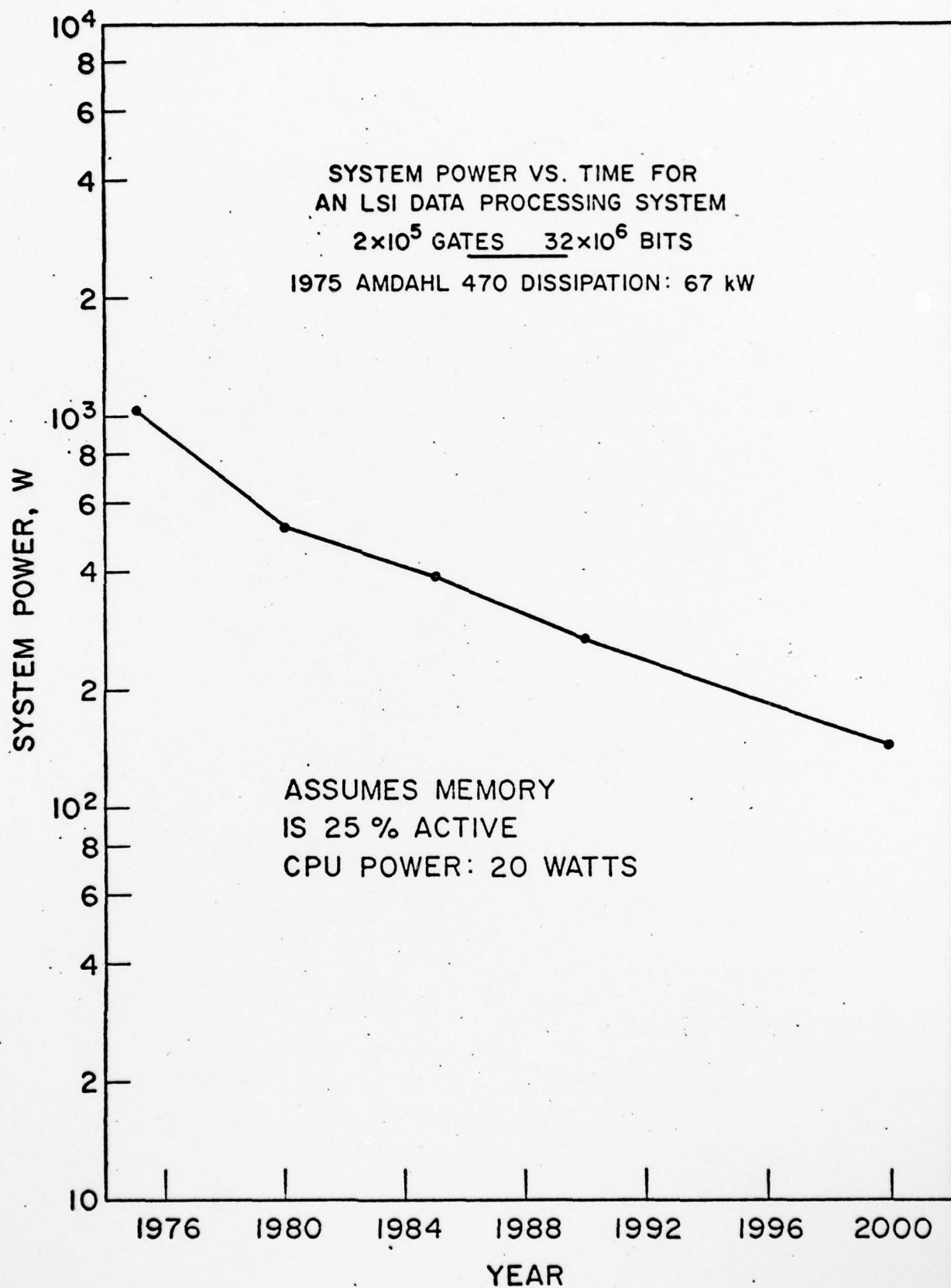


FIGURE 38: SYSTEM POWER

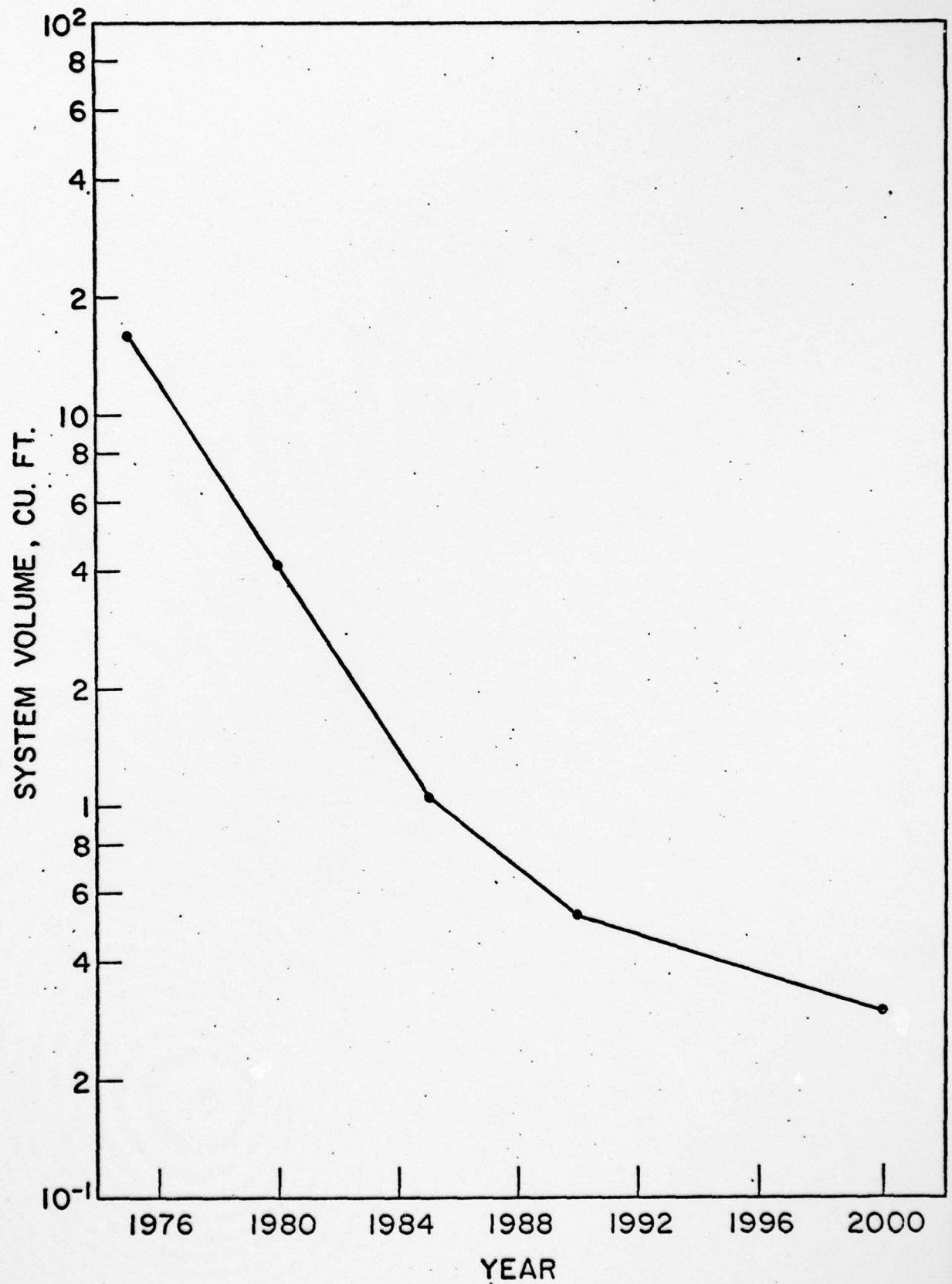


FIGURE 39: SYSTEM SIZE

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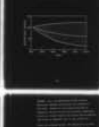
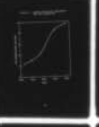
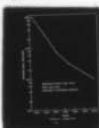
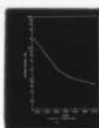
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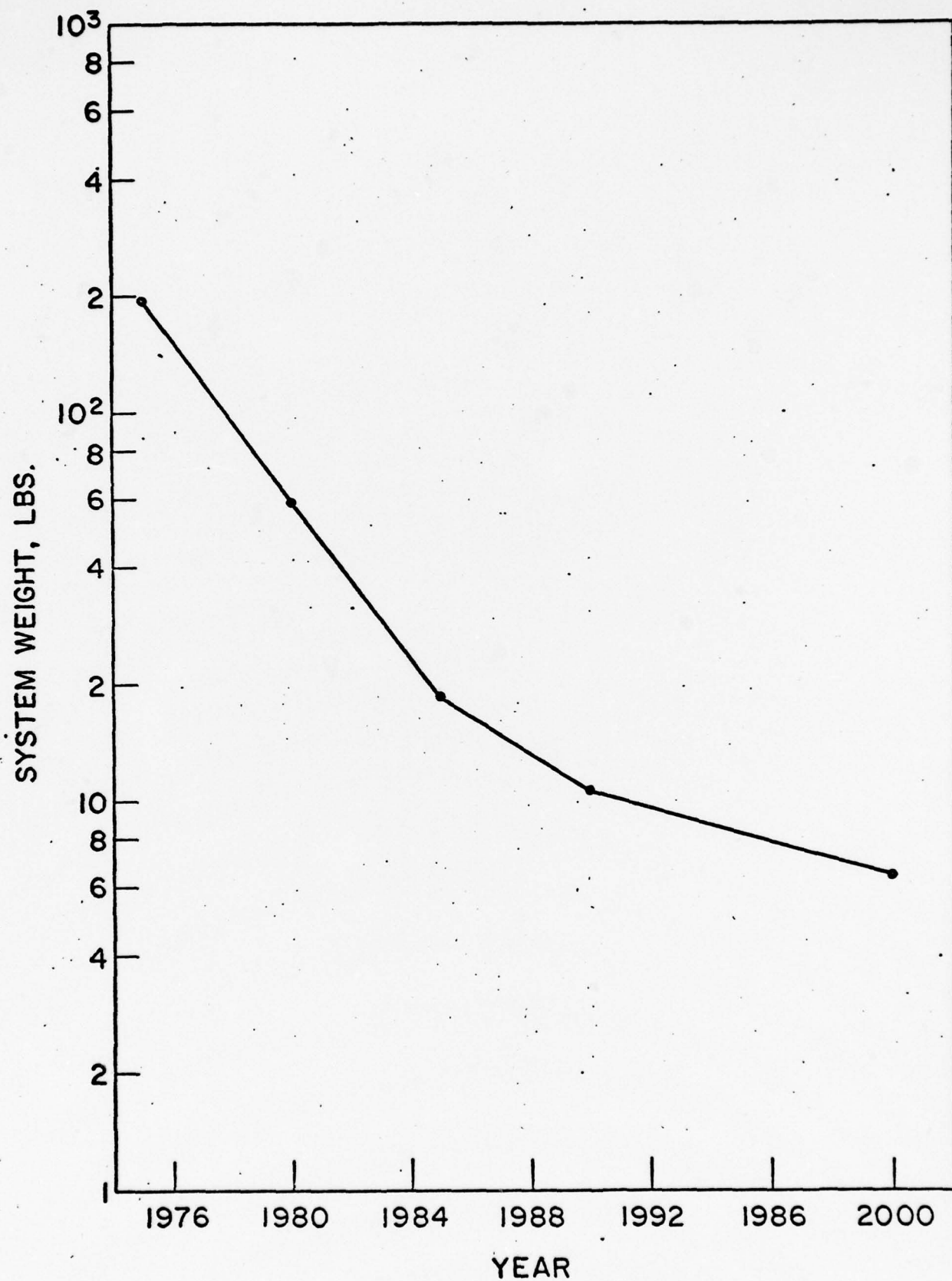


FIGURE 40: SYSTEM WEIGHT

the previously stated assumptions for the airborne system and on the size forecast just developed. It is clear that weight will be no problem in ground-based LSI computer systems.

5. System Cost

The final system parameter is cost. For the CPU, the chips are all LSI and highly custom (It is noted that a market for this system probably does not exist prior to 1985). A cost of \$20 per chip is estimated in 1975, dropping to \$10 per chip in 1980, and to \$5 in 1985 and beyond. The development of a market to permit these prices is by no means certain, but the CPU cost is small compared with the cost of memory. Memory cost per bit is taken from Figure 22 but reflects an additional penalty consistent with the bit densities to reflect the speed required. Other costs include the costing factors used for the airborne system. The results are summarized in Table 17 and Figure 41.

Cost in this system drops significantly, reflecting primarily the anticipated reductions in the cost of memory. The total system is in excess of \$100,000 in 1975 but should drop to \$1000 or less in 2000. Computing power will be widespread and inexpensive, tending to decentralize control and distribute it throughout the system. No attempt here is made to

TABLE 17: GROUND BASED SYSTEM
COST FORECAST VS TIME

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
CPU cost/chip	\$20	\$10	\$5	\$5	\$5
CPU component cost	\$2000	\$200	\$70	\$50	\$40
Memory Cost/Bit (cents)	0.3	0.08	0.02	0.008	0.002
Memory Cost	\$96K	\$25.6K	\$6.4K	\$2,560	\$640
# PC Boards	7+267	2+67	1+17	1+9	1+5
# IC packages	100+8K	20+2K	14+500	10+250	8+125
Cost of PC boards (incl. AW&T)	\$6028	\$1725	\$540	\$330	\$210
AW&T of IC packages	\$2025	\$606	\$180	\$104	\$54
Chassis cost	\$570	\$234	\$93	\$53	\$30
Total Cost	<u>\$106,623</u>	<u>\$28,365</u>	<u>\$7,283</u>	<u>\$3,097</u>	<u>\$974</u>

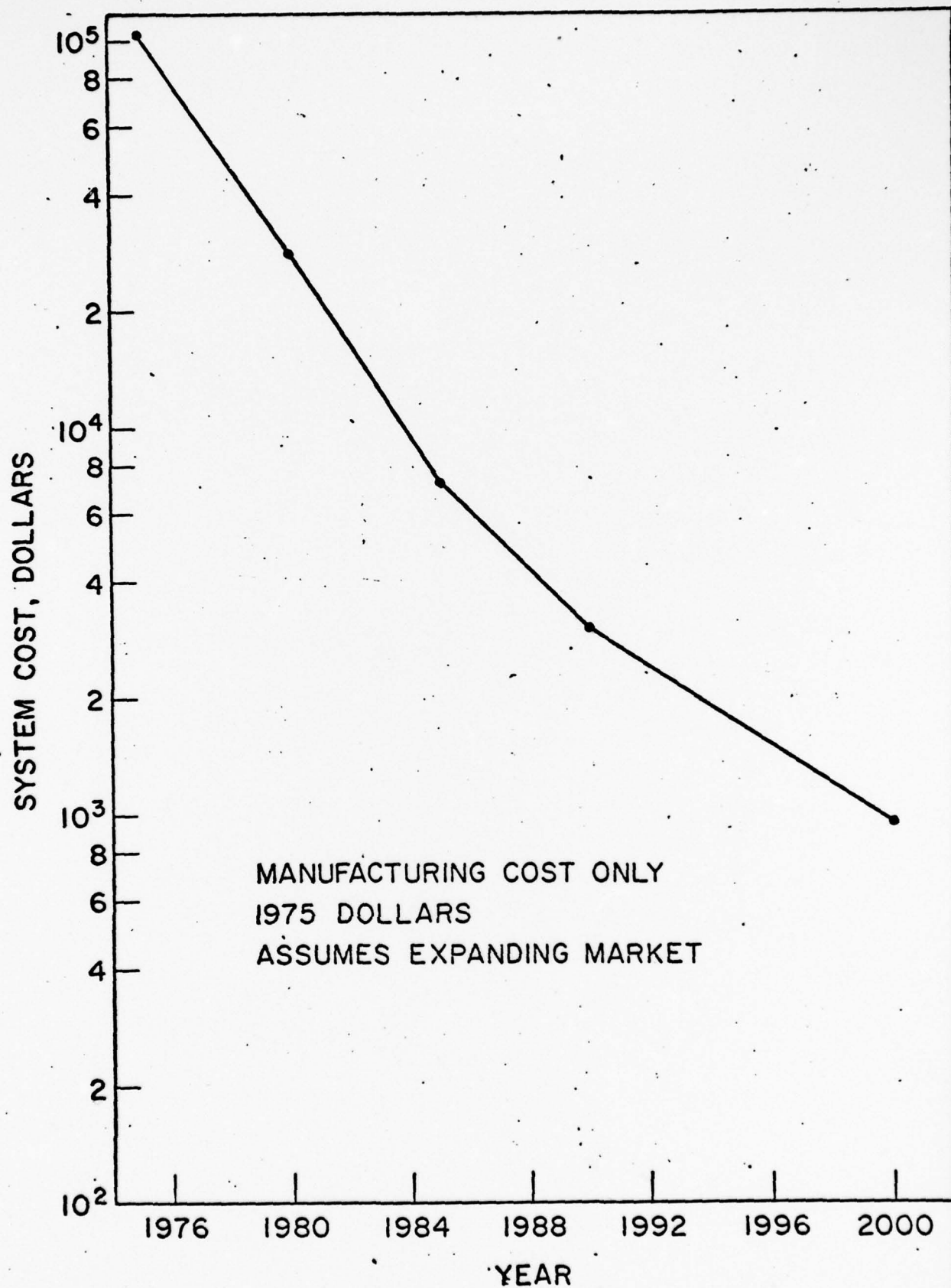


FIGURE 41: SYSTEM COST

TABLE 18: GROUND BASED/AIRBORNE
SYSTEM FORECAST SUMMARY

	<u>1975</u>	<u>1980</u>	<u>1985</u>	<u>1990</u>	<u>2000</u>
<u>Airborne System</u>					
.Speed (millisec.)					
.Line Transfer	12	1.4	0.3	0.14	0.16
.Data Interface	5	0.8	0.13	0.003	0.01
.Sensor Read	0.16	0.03	0.006	0.002	0.0009
.Power(watts)	138	95	77	60	55
.Size (cubic in.)	2510	1910	805	675	590
.Weight (lbs.)	29.5	24.4	12.8	11.2	10.2
.Cost (\$)	2168	1444	901	746	585
<u>Ground-Based System</u>					
.Speed (MIPS)	0.63	3.13	7.8	15.6	41.7
.Power (watts)	1020	520	395	270	145
.Size (cubic ft.)	16	4.13	1.04	0.53	0.3
.Weight(lbs.)	195	59	18.3	10.6	6.4
CPU & Memory only)					
.Cost (\$)	106,623	28,365	7,283	3,097	974
(excl.design)					

estimate the design/development costs of this system, which would be substantial, especially in near term. Since such systems take several years in development, a lag between technology and the resulting system is to be expected. Systems based on 1980 technology should, however, begin to appear prior to 1985, when the present system will not appear as large as it does today.

IV. Conclusions

Table 18 summarizes the results of this chapter for the two systems studied.

From these studies, a number of observations can be made:

A. Airborne Systems

1. A wide number of important microcomputer-based applications will be feasible within 10 years, both for commercial aviation and for the general aviation community. Such systems can be small, light, sophisticated, and relatively inexpensive.
2. Although the microcomputer is expected to make such systems feasible and contain most of the complexity, it will not contribute significantly to the power, size, weight, or cost of such systems.
3. Speed in such systems will be largely limited by peripherals and not by the instruction cycle of the microcomputer. Hence, functions requiring only more

computational complexity can be implemented almost at no cost.

4. The characteristics of such systems are relatively strong functions of developments in peripheral equipment, e.g., displays, bulk memory, and power sources. These areas should be monitored closely.

B. Ground-Based Systems

1. Ground-based computers are expected to proliferate as the results of LSI technology. Many functions which are now centralized will be implemented in distributed, dedicated LSI computers in the future.
2. During the next quarter century, the LSI data-processing computer will see its speed improve by a factor of 50, while power, size, weight, and cost will improve by a factor of 10 or more.
3. Compared with the most advanced large machines of 1975, LSI technology of 1985 should produce an equivalent machine, operating at approximately the same speed, dissipating 150 times less power, consuming 150 times less size and weight, and costing between one and two orders of magnitude less.
4. In dedicated applications where speed requirements can be reduced, further reductions in power, size, weight, and cost will be possible.
5. System characteristics are most strongly dependent on developments in memory technology, which should be monitored closely. The importance of design, assembly,

and testing in system cost will increase relative to hardware. Design costs will significantly reflect the expansion of the market for large machines.

In both airborne and ground-based systems, the microcomputer will have a significant impact on aviation. In ground-based applications, technological progress will support increased computer automation and a proliferation of dedicated computer control and data processing. In instrumentation and control systems, both airborne and ground-based, the impact of the microcomputer will be limited only by our ingenuity in using it for new applications.

CHAPTER SIX

UNCONSTRAINED TECHNOLOGICAL FORECAST OF MICROCOMPUTER ARCHITECTURE AND SOFTWARE

I. Introduction

This chapter carries the forecast for microcomputers into the area of software. Any attempt to project trends in software through the next 20 years cannot be separated from developments in hardware, many of which will significantly impact the computer architecture, simplifying the implementation of software systems, reducing development costs, and increasing reliability. That is, highly significant factors in determining the cost of software development derive from dramatic improvements in hardware costs and capabilities. During the last 25 years, improvements in hardware capability far exceeded long term projections. And some software development costs have been reduced or eliminated as a result. The forecast given in this chapter is a conservative one in the sense that it does not include unanticipated breakthroughs in technology. Such breakthroughs can be expected as methodologies are developed in fault-tolerant processing and self-repairing code as well as other areas of software engineering.

The purpose of this chapter goes beyond software costs and capabilities to explore the implications which new software has for availability of computing, adaptability for new

tasks, and flexibility for individual users of computing. This extended view is important since the impact of microcomputers on computation, process control, information handling and communication in aviation will far exceed the scope of computer use today. Especially since it is difficult to make a reliable projection beyond the mid-1980's, general guidelines are needed for planning new systems, anticipating alterations that can take advantage of new opportunities, and working within the constraints that must be placed on operational systems (e.g., reliability and redundancy).

The two sections immediately following describe the evolution of mainframe software and microcomputer software. Section IV discusses briefly some important measures applied to software, and the implications of these measures for forecasting costs and capabilities of microcomputer systems. Data on mainframe and microcomputer software are summarized in the next two sections. Particular attention is given to contrasts between the two areas of mainframe and microcomputer technology because differing characteristics--for example, size and power requirements--have considerable impact on software costs and capability.

The last two sections of this chapter list assumptions and major forecasts. In summary, changes in hardware and corresponding changes in the design of systems will lead to

new opportunities in software development. Costs of development and maintenance of software comparable to today's systems will decrease. Reliability of software will improve. Computer systems will be expected to do more for users, and perform more reliably, and the overall costs of software development will increase as a result of these additional requirements for systems with improved access and reliability.

II. Evolution of Mainframe Software

The history of software for mainframe computers reflects increasing attention to the requirements of the tasks which machines are expected to perform and the characteristics of the humans who use the machines. The cost of equipment has steadily decreased while the cost of labor continues to increase. Concern for efficiency from a machine point of view is being replaced by careful attention to efficiency and effectiveness of people using the machines. That programmers do their jobs well and in a reasonable time is, for some systems, much more important than the number of cycles the machine must execute to accomplish reliably the tasks assigned to it. The performance of the ground controller or pilot when interacting with a computer system is much more important than the efficiency of the machine executing a support function. The theme of human efficiency as well as machine efficiency is evident in mainframe software, and will become dominant in microcomputer software.

A. Machine Language, Assembly Language, and Compilers

The evolution of computer programming languages is well known. Software capability has moved from the binary language of machine logic through the mnemonics of assembly languages to the convenience of compilers. Each new development made another step away from machine oriented coding programs and data toward human representations of procedures and information. Languages became more suited to describing procedures and structuring solutions. Tools for arranging and manipulating data became more suited to the inherent structure of each problem and information file. More checking was accomplished at the time of compilation of the program, rather than leaving all testing of the completeness and correctness of a solution to execution time. Some new software has caused the user to give up access to certain aspects of the machine's capabilities. For example, with compilers it is increasingly difficult to know exactly where in the machine's memory a particular instruction will reside, or even the exact machine instructions which will be used to implement each higher-level instruction entered by the programmer. This isolation has made obsolete the old methods of program debugging which were dependent on knowing just such information.

B. Toward Independence of Specific Machines

Software in general has moved away from dependence on particular machines. Programs prepared to be transportable can be compiled readily on machines constructed by different vendors. The cost of transfer of software is small in comparison with the cost of system design. High level languages tend to be free of dependence on particular hardware.

C. Orientation to Tasks and Problems (Applications)

Languages are increasingly oriented toward classes of applications and even specific tasks. For some time, software designers had tended toward general purpose solutions as an ideal when attempting to meet the need for higher level languages. Now that task specific solutions have become practical, users benefit from languages engineered to the specific needs of each application.

Special purpose languages have been designed to satisfy single objectives, as in machine tool control or logical design. Languages oriented to applications incorporate facilities and notations which suit the functions to be served by the computer program. Some languages have been developed especially for the description of select classes of problems, for example, for programming procedures for pattern recognition, or for writing instructions to analyze non-formal languages.

D. Firmware Considerations

The evolution of software includes instances of building around hardware limitations to improve system utility. Eventually those extensions whose software implementations have proved useful are incorporated in the firmware or hardware system. Thus increases in the utility of the system can be obtained without corresponding increases in the cost of maintaining software. In this sense, the software system provides a good testing ground for potential hardware extensions. The usual progression is for the utility first to be provided in some "more complex" software package, after which it becomes a standard software system utility. Once it has been accepted within the software community and has reached a state of relative stability in its specification, for smaller systems it may be "burned into" programmable read-only memory (PROM) and become available as firmware. In larger systems typically very little firmware is used, but whenever hardware is being redesigned, the utility will eventually find its way into the hardware as one of the system's primitive operations. Novel data structures accommodated by some software bear little relation to the physical structure of the memory. New designs show increasing orientation to human considerations. The overall effect is for software to improve in capability, and for standard functions of

that software to move into firmware and hardware before the increased complexity would become a problem for maintenance and reliability of the system.

E. Structured Programming

A growing concern for problem analysis and modular design of systems has recently been identified by the level "structured programming." This approach to software is part of programming's evolution from a machine orientation toward a consideration of task and human factors.[10, 8] It is an approach to software specifications, documentation and coding which yields more detailed specifications, more usable documentation and more effective coding with minimal side effects.

III. Evolution of Microcomputer Software

Software for microcomputers has a much shorter history than that for mainframe machines, but it follows a similar evolution. The same trends can be observed, for example, an increasing orientation to tasks, and improved accessibility for human programmers and users. However, significant reductions in the size, portability and cost of typical microcomputer systems introduce new opportunities: networks, distributed processing, parallel processing, and personalized functions. Intelligent systems design now places computing where it is needed, for example, in sensing and control components, and literally in the hands of the user.

A. Direct Access to Hardware Through Low-Level Languages

The first generation microprocessors returned to the programmer full access to the hardware. Indeed, the machine level coding made complex programming a tedious operation on these machines. However, higher level language capabilities soon were written, first on larger machines as cross assemblers, and later on the microcomputers themselves. Initially the implementation of compilers within machines having limited storage space and instruction sets was accomplished only through careful programming and compromises in the capabilities of the compiler. However, rapid increases in the speed, power and storage of microprocessors have facilitated the introduction of very capable software: resident, relocatable macroassemblers; a full implementation of FORTRAN; PL/M, a reasonable subset of PL/1; and even Pascal, a high-level, structured language.

B. Introduction of Structured Languages

The introduction of structured programming languages, for example, Pascal, marked an important step for microprocessor software. Pascal is considered by many to be the best structured programming language currently available; it contains a rich set of structured primitives and does not try to be all things to all people. Pascal is not convenient for all purposes; for example, it lacks the powerful string handling of the SNOBOL

language which is useful in analysis of text. But because the designer of the Pascal language set reasonable limitations, the processor is able to make extensive checks of the programming code at compilation time, thus reducing the need for extensive error checking of the compiled program in execution. Pascal is already available on the Zilog Z-80 microprocessor, indicating that even the current small machines can handle the demands of task-oriented, structured languages. The limiting factor on software will be the ability of the design team to provide task-specific, application-oriented languages, rather than the power of the microprocessors to execute them. The richness of the instruction sets of the machinery will be more than adequate to the functions that are executed.

C. Networks and Distributed Processing

Although the early computer was a uniprocessor machine, that is, it had only one processor (the CPU), today a large machine typically has secondary processors that assist the central CPU by carrying out specialized tasks under its direction. Presently these secondary processors take care of I/O or other specific functions. A number of systems have been built which include processors working in parallel in various configurations. The loosest such network of processors is a network of mainframe computers which optionally communicate with

one another, such as in the Advanced Research Projects (ARPA) Network. In this loose connection of independent computer systems, each is able to send messages to any other processor in the network requesting unique data or specialized programs to operate on data already available.

D. Parallel Processing

At the other extreme, parallel processors have been used in very tight coordination in applications such as matrix operations. Two or more equivalent CPUs execute the same instructions at the same time on parallel data. Through parallel processing, a system can handle much more data within a given time, especially for specialized applications where the data exhibit considerable symmetry. Even more specialized architectures such as the associative parallel processors of the STARAN IV have shown that very high speeds can be obtained when there is sufficient symmetry in the data to be manipulated. [2, 3] Furthermore, one processor can interrupt the others if some condition met by its data eliminates the need for searching the other subsets of data.

Future computer systems will indeed communicate with other computer systems over transmission lines dedicated to the purpose, i.e., will be members of loosely connected networks. They will have architectures represented

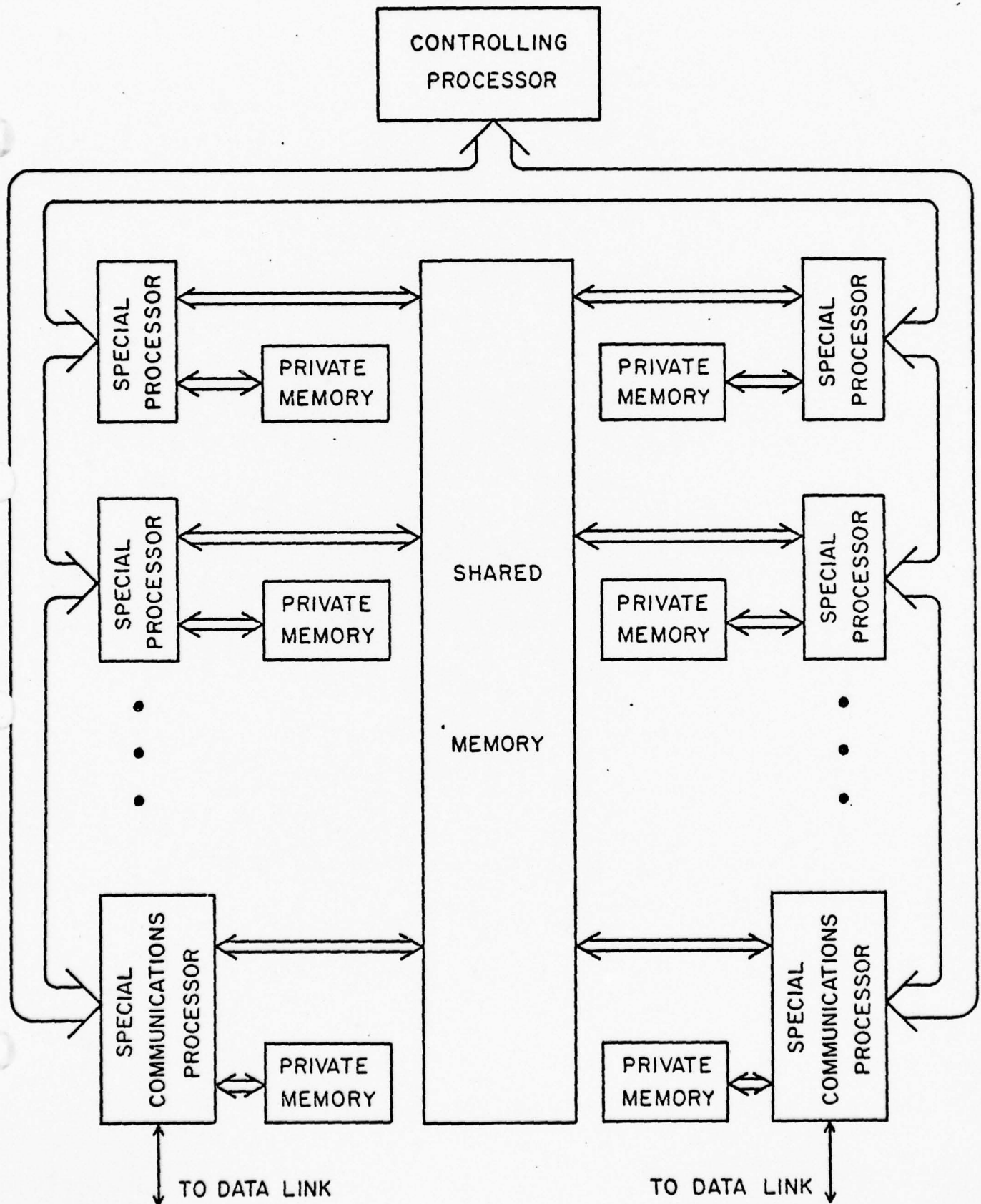
by Figure 42, with a central controller communicating with and overseeing communication among a number of specialized processors. Some of these will be executing in parallel while others will be doing specialized tasks as assigned by the controller. A few of these specialized tasks will concern maintenance of communications with other computer systems over dedicated lines. Each processor will have some private memory and will have access to the central memory, possibly in some restricted way to prevent its accessing or altering privilege information.

However, it is more important that most computer systems will be comprised of multiprocessor machines. They will have a number of processors executing programs independently, sharing memory. Such systems have three principal advantages: extended computing capacity, increased flexibility, and considerable redundancy which increases reliability and availability for critical tasks. Such a system can use some processors as redundant backup for others performing critical tasks.

E. Primitives for Systems Control, Applications and User Interface

Increasingly the primitives used in systems control programming become part of the hardware. Sections of programming which do not change can be determined and placed

FIGURE 42: CONTROLLING PROCESSOR SUPERVISING SPECIALIZED PROCESSORS



on a chip, i.e., "wired in." For example, missile control functions which required lengthy programs have been replaced by a primitive control function (for which the logic is wired into the hardware) and a list of parameters requiring one tenth of the storage of the assembly language program. The primitives are selected to be generally applicable, and can be applied in many situations (e.g., radar scanning, engine sensing, and weather analysis).

Eventually subsets of primitives for specific classes of applications will be determined and similarly implemented. A trivial example already having considerable economic impact involves the chips on which many video games for home entertainment are based. Considerable programming effort went into the first versions of "spacewar" on a Digital Equipment Corporation (DEC) PDP-1 during 1960-64. The interactive use of graphics involving two persons in a competitive situation intrigued designers of computing systems for learning and teaching. Coded in assembly language, it was difficult to revise, and it did not transfer readily to new machines. In the next generation of educational computing equipment, equivalent programs were distributed by DEC from the educational applications library. However, most machines and display devices were oriented to alphanumerics; graphic display was lost by most educational users of

of computers for a time. Today similar games, including versions of spacewar, are available on a chip for incorporation in home video products. These games are programmed in the assembly language of the microprocessor (a return to the constraints of lower level programming), but since they are provided as firmware rather than software they do not have to be loaded into the microcomputer's memory every time they are to be used. Since the cost of the chip is very small compared with programming costs, the addition of such chips to a system, providing a sophisticated set of primitives which save programmer time, reduces overall costs.

Primitives which deal with the interface between machine and user will facilitate programming individualized software for small groups of users. Already "personality modules" are offered with personal computers, adapting the basic machine through firmware for different kinds of functions: calculation, text editing, process control, and the like. In the future, intelligent terminals used with a central information and control system, or stand-alone pocket calculators, will be readily adapted through selected application of such primitives for the different needs and work styles of pilots, controllers, and maintenance personnel. One of a collection of chips will be selected and installed, or an erasable read-only memory (EPROM) will be erased and reprogrammed, to

implement inexpensively the conventions and notations for a particular group of users. Further, the personal style and preferences of each user can similarly be accommodated by sets of instructions placed within the pocket device or user terminal.[15]

F. An Evolutionary Process

In moving more and more of the necessary functions from the user's software into the set of system primitives, even the low level languages become much more powerful tools for solving the necessary tasks because of the application-specific primitives. Such primitives, combined with the structuring, testing, and convenience facilities of higher-level languages, are even more effective. This in turn reduces the costs of software development, testing and maintenance while improving productivity and reliability of the final systems. Current trends indicate that many of the needed functions will be added to the set of system primitives via the incorporation of intelligent subsystems within each larger system. These intelligent subsystems will of course be the direction of future development of the microprocessors and may therefore be referred to as microstructures of the larger systems in which they are found. It is the existence of these microstructures which provide the speed, reliability, and relatively low cost of future computing systems.

IV. Measures Applied to Software

In Chapter Five, a number of computer application areas expected in the future of avionics were listed with brief descriptions. The sheer numbers of programs to be written is impressive, but in determining the costs and reliability of future software, a number of measures must be considered. These include the complexity of the software, the ratio of software to total project costs, the impact of modularization on total system costs, including the integration of the software into the total system design, increasing requirements set for software, and program and project efficiency. These measures will be discussed in this section and their future trends will be indicated.

A. Complexity of Software

A rough indication of project complexity is provided by program size. This may be measured in various ways, including the number of lines of code produced by the programming team, the number of modules or routines included in the package along with the average size of such modules, or the memory size needed to store the program.[13] It is this last measure which has been used in previous studies to indicate program complexity. Memory requirements for program storage is an indicator of the number of machine language instructions in the project. This measure of program size and (to some extent) complexity has been useful in previous studies,

such as the CCIP-85 study cited in Chapter One because it is common to all operating programs and is independent of the language used for programming. But for this reason, raw size is misleading as a measure to indicate programming costs. Projected costs must be derived from measures of time and effort needed to produce a usable, debugged, easily maintained block of code; this is indeed very much dependent on the language used in the implementation. The average number of lines of usable code written by a programmer per day is not much influenced by the language of implementation. And yet code written in a high level language suitable to the application will generally accomplish the same functions as a machine language routine of many more lines. Therefore, if one merely compares the equivalent size in machine language, the considerable saving obtained by using a higher level language for program development is overlooked.

B. Ratio of Software Costs to Total Project Costs

The percentage of total system costs which goes to software has been a source of concern for those planning major new projects. As has been stated in Chapter One, by 1980 the software cost of a new project is expected to increase to 90 percent of the total cost of a project. However, this figure is misleading, since as noted in

Chapter Five, the cost of hardware is decreasing rapidly. The large ratio is primarily a result of the decrease in hardware costs and not an increase in software costs.

If in 1980 the software cost is 90 percent of the total system cost (for some systems), hardware solutions to problems will be relatively inexpensive. For example, doubling the memory and number of processors will add only 10 percent to the total system cost. Indeed, software costs on many kinds of systems are expected to go down as well. With the dramatic drop in hardware cost, the substitution of hardware for software will almost always reduce overall system cost. For example, a typical small system in 1975 may have cost \$100,000 for hardware and \$200,000 (67 percent) for software. A similar system in the time frame of 1985-95 might cost \$2,000 for twice as much hardware, and \$100,000 (98 percent) for software. And in many situations further reductions in software costs will be achieved through hardware solutions; doubling again the capacity (and cost) of the hardware adds only 2 percent to system cost.

C. Cost and Modularity

A more sensitive measure of complexity for the purpose of anticipating development costs is the number of

lines of code as written by programmers rather than the number of instructions stored in the machine ready for execution. This indication of complexity is more appropriately measured by the number and average size of modules (or subunits of programs), and the number of variables passed among them, rather than the total number of machine language instructions. These measures cannot be given a strict mathematical representation at this time, but the implications for software projects will be clear in subsequent discussion.

The software and hardware experts on a team work together throughout the design process, exchanging ideas and requirements at a much earlier stage than has been typical in software developments in the past. The team analyzes and subdivides down to a reasonable component level before dividing tasks between hardware and software. Such divisions then depend on the specific design performance requirements of each module. Decisions about specific implementation are postponed as long as possible in order that choice of chips, languages and specific programming best fit the task of the module and the current technology. And if the modularization has been accomplished well, modifications in the hardware-software system made later can use the current technology.

The CCIP-85 study cited data from a number of IBM projects producing large software packages. However, the study did not include the effects of integration between hardware and software, or the modularity of programs. The curve given in Figure 43 suggests the total number of instructions written for these large computer systems to be increasing exponentially during the period 1960 through 1973. The size of individual systems is not expected to continue to expand at this rate; the curve is based on only a small fraction of systems implemented, favoring the largest systems as constructed for the largest machines. Size as a measure of complexity is misleading since newer systems are written in higher level languages which generate more instructions at the machine level for each statement written or special routine called by a programmer. Modularity of programs and total project software will therefore decrease programming costs, but would appear to increase project complexity using measures such as those in CCIP-85.

D. Increasing Requirements Set for Software Projects

Although complexity of the project is indeed an indicator of programming costs, it has only indirect impact on software costs. The complexity of the programs needed by the project as analyzed into subtasks is the actual determinant of personnel requirements. Complexity

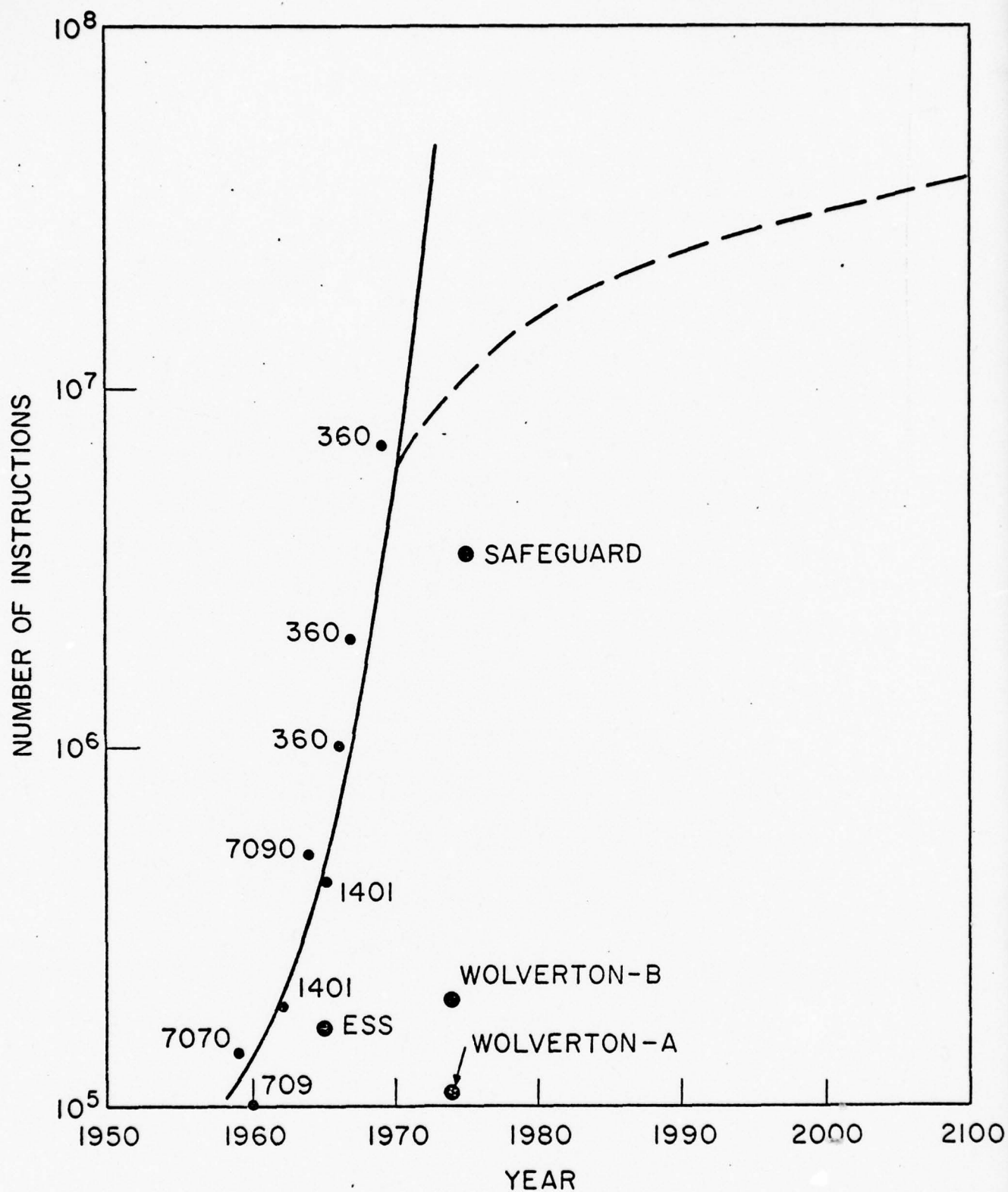


FIGURE 43: GROWTH IN SOFTWARE - NUMBER OF MACHINE INSTRUCTIONS

of large projects will continue to increase with the capability of computing systems to solve more complex problems. The costs will depend in large measure on suitable selection of machines, programming methodologies, and programming teams. Proper choice of machines with appropriate primitives (particularly with the logic distributed throughout the system where it is needed), use of structured programming methods, and use of design teams that can make the difficult choices between hardware and software alternatives for implementation, all these factors will reduce the programming costs of any large project.

E. Program or Project Efficiency

Another measure of software which influences development costs is desired program efficiency.[1, 7, 11, 9] Any requirement to write more efficient programs (i.e., to execute in fewer cycles of machine time and/or fit in fewer memory locations) requires careful attention to interaction between the hardware and the software. As a result of the considerable effort not otherwise necessary, software development costs rise quickly. However, as methods are applied which increase project efficiency, e.g., the overall effectiveness of the programming team, the costs decrease. The costs of future software projects will indeed hinge on the relative

importance of program efficiency and the discovery of techniques to increase the efficiency of the programming team. As hardware costs decline, the importance of code which is efficient from a machine point of view (i.e., which conserves memory or decreases processing time) will diminish, since one can alter the hardware more cheaply than one can modify the software. Concerns about program efficiency which were important in the early days of computing are rapidly losing their significance, while techniques to increase the efficiency of the programming team are being developed. The combination of these effects will result in software which will be less expensive both to produce and to maintain.

V. Data on Mainframe Software

Data on the costs of programming projects for large mainframes provide some insight into the future cost of software development for systems dependent on microcomputers. However, care must be taken not to extend inappropriately the statistics to the new region since some of the basic assumptions are very different for microcomputers. Most of the past data on mainframe software is based on hardware configurations which are basically uniprocessor configurations, i.e., configurations with just one CPU. Only in the last generation of hardware has "intelligence" moved into other parts of the systems such as the I/O channels of the IBM 360. In some

machines such as the CDC 6000 series machines there have been a number of peripheral processors, but generally these have been used to support multi-user timesharing systems, with the individual users' tasks being unrelated and with a somewhat heterogeneous mixture of user software. In the past and present, systems hardware was a major cost of the system; as has been seen in previous chapters, the price of hardware is decreasing quite rapidly. In future computer systems the cost of hardware will indeed be negligible when compared to the cost of software; this will lead to a philosophy in which program efficiency will take a much less important role than ease of programming and ease of software maintenance.[1]

A. Complexity of Software

Figure 43 shows the number of machine instructions for a selected set of large programming projects during a span of 15 years. The size of such programs, as indicated by this measure, is increasing at an alarming rate. Whereas a large software project in 1960 might be one which involved about 100,000 instructions, the large projects of only a decade later involved 100 times as many instructions. Using this criterion for judging complexity of software, it appears that software complexity is increasing at an exponential rate. Because of limiting saturation factors, this exponential growth

cannot continue; thus the dotted line shows an expected leveling of the growth curve.

B. Decreasing Comprehensibility

The increase in complexity is understandably accompanied by a decrease in comprehensibility of the resulting code.[12] Therefore, even simple modifications in large (unstructured) programs become extremely expensive.

This cost increase is especially characteristic in projects using assembler languages with the many possible interactions between routines in the software package. Any routine can access the variables of any other routine and indeed can even alter the code of other routines inadvertently as often as by intent. This makes debugging such software a tedious task and makes revisions extremely difficult and expensive, often beyond what is practical.

C. Tools to Aid in Design of Software Systems

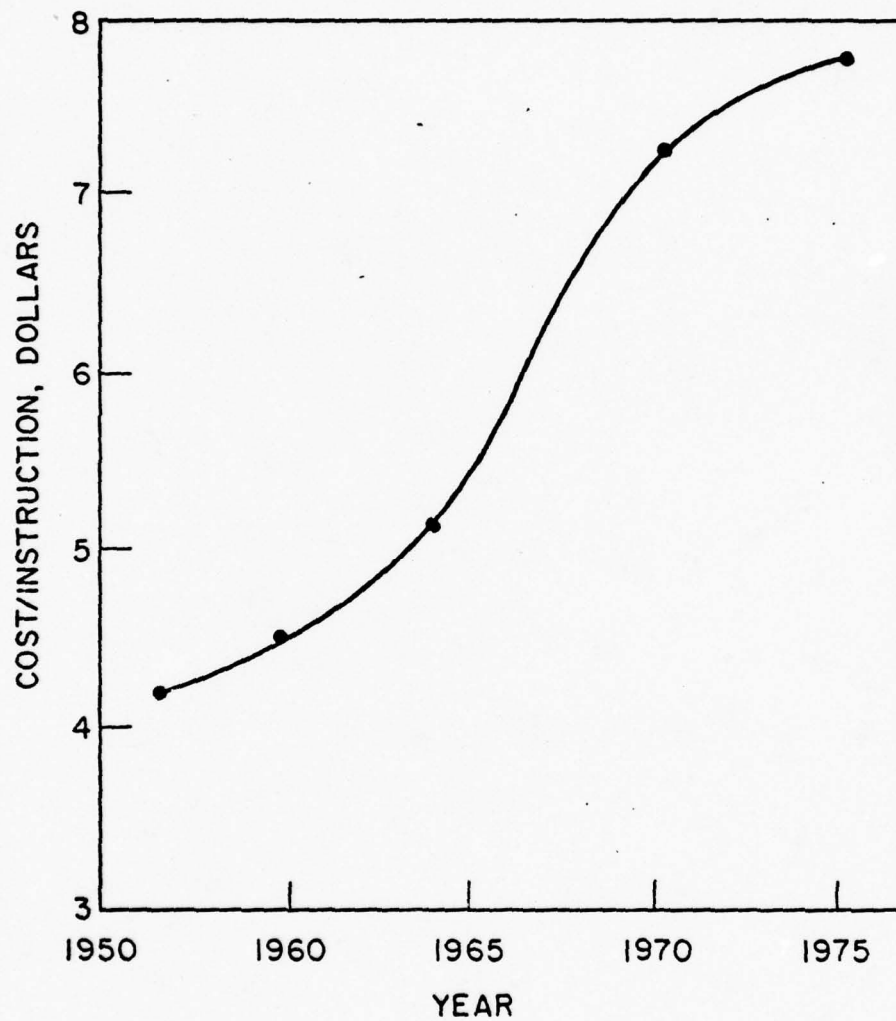
As higher level, structured languages come into use, especially languages specifically designed for the intended application, these cross effects between routines become much better defined and predictable.[1] Transfers of data or control between routines should occur only when the programmer specifically requests them and only as called for in the specification of the routines. Generally such interactions will only

occur when the variables involved are explicitly passed as parameters to the called routines, or when the called routines are nested blocks within the calling routines. In either case the interaction is much more clearly included in the code, making debugging and alterations easier and less costly. This description of programming structure is given in some detail in order to establish clearly the possibility of constant or lower software costs through the introduction of structured programming techniques. Estimated data on average cost per instruction is given in Figure 44.

D. Segmentation of Complex Software Systems

To the extent that the project can be segmented in a structured manner into tasks and subtasks, the programming process can be carried on much more efficiently. Programmers can work together as a team without one accidentally destroying the code or variable work space of another. The individual subtasks to be programmed are specified in detail with each possible output stated as a function of each possible input, and with the subtasks arranged in a hierarchical order. For a large system, such subdivision of the tasks will result in a great many subtasks and resultant subroutines. Proper use of these structured methods, called "top-down," to obtain such a subdivision can aid in understanding the

FIGURE 44: AVERAGE DESIGN AND PROGRAMMING
COST PER INSTRUCTION



interrelationship of the individual routines and will increase the comprehensibility of such large systems. The resulting code is much more readable and therefore much more easily debugged and altered to take into account future developments of the target system. It is this increase in readability and therefore comprehensibility that tends to make such systems easier (and cheaper) to program and maintain.

Progress is being made and will continue to be made on the development of new systems to increase the reliability of software.[4, 5] One of the most important steps in this direction is of course the development of reliable user-oriented, task-oriented, structured programming languages. Progress is also being made in programming technology, for example, redundant coding to provide alternate parallel means to solve a given algorithm so that one piece of code can be checked for validity by the results of another written independently. As such techniques are further developed, the total cost of software will decrease while the reliability increases.

E. Upward Compatibility in Hardware

Another feature relevant to the development of software for mainframes is the trend over the last decade to maintain upward compatibility in hardware development.

With upward compatibility, programs that have been written for one machine can be run on the new hardware with no changes. Such upward compatibility decreases software reinvestment every time the hardware is upgraded. One of the prime examples of this was the transition from the IBM 360 to the 370, where programs written for the 360 could immediately be run on the 370 with only the smallest of changes. When the programs were run on the upgraded processors, they did not make use of all of the new features, but they could run with essentially no alterations. The Amdahl 470 V6 was designed to use the same instruction set as the IBM 370/168, and indeed entire software systems, including operating system, languages, and user applications, can be moved from any IBM 370/168 to an Amdahl 470 V6 in little more than the time it takes to output copy to a mass storage medium and then reinput the software from the mass storage device into the new hardware system.

In summary, tools will continue to be developed to deal with the increase in complexity of future software systems. Furthermore, with proper choice of software and hardware configurations, an update in the hardware (to achieve reduced cost, greater speed, and improved reliability and throughput) need no longer require major software changes.

VI. Characteristics of Microcomputer Software

Microcomputers originated in the search for a simple design solution for a well-defined task. Datapoint, Incorporated, had a conventional TTL processor functioning in a well-defined system but wanted to replace it with a functional equivalent module using large scale integrations (LSI) circuitry. In designing the LSI equivalent, the first microprocessor (the Intel 8008) was born. Although the original cost of the 8008 was high, these chips and the more sophisticated 8080 are now available free as bonuses with the purchase of small quantities of memory chips from a number of computer hobby houses. Through mass production, the cost of such chips is already approaching its minimum; that is, the price is determined mostly by handling costs. The single price on microprocessor chips such as the 8080, F-8, and M6800 are currently (March 1977) between \$10 and \$25. Furthermore, the capabilities of each succeeding generation of chips are increasing significantly without correspondingly large increases in costs.

A. Upward Compatibility

Fortunately for computer costs, the state of affairs in microprocessors has reached a point that took 20 years to achieve with mainframe equipment. Current mainframe computers are being offered as parts of series of upwardly compatible systems so that users can move to larger systems as needs dictate without major software

revision. Such upward compatibility has saved users the large software revision costs associated with hardware changes. These design and marketing decisions by the mainframe manufacturers have been among the major forces which have helped the computer to be adopted in almost every aspect of modern life.

Although the microcomputer still is quite new, the impact of upward compatibility is very apparent. The original microprocessor, the Intel 8008, was too slow and had too few instructions for easy use in many potential applications. However, Intel's successor to the 8008 was designed to include a very similar instruction set so previous software could be used without major revisions. The newer 8080 chip of Intel is not truly upwardly compatible with the 8008, since some differences exist in the binary code to accommodate new features, for example, more input and output (I/O) ports and more "stack" area, needed for subroutine calls. However, by all appearances to programmers, the newer component runs the old software. By changing mnemonics for I/O statements in an 8008 program, a programmer can assemble and run that program on the 8080.

Furthermore, various vendors intentionally make chips compatible, at the same time adding features to make the newer chip more desirable. Zilog, a competitor of

Intel, designed the Z-80 to be upwardly compatible with the 8080, adding speed, more registers and some powerful instructions that resemble those of larger minicomputers. In this case, programs written for the Intel 8080 can immediately be run on the Z-80, since the only incompatibility is the redefinition of one flag which will not affect well-structured programs. Similar relationships exist within other microprocessor series on the market, for example, the Mostek 6800 and the MOS Technology 6500 series, which have remarkably similar instruction sets. IMSAI has even announced a distributed network of the Intel chips, called the Hybercube, reportedly with the power of existing IBM mainframes.

B. Facilitation of Modular Systems

The very low cost of microprocessor chips encourages designers of systems to adopt effective practices for modular systems. As has been apparent in the evolution of mainframe software, modern design criteria recommend a structured and modular approach in the design of computer systems. The low price of the hardware components forces very serious consideration of trading off hardware for software costs. Much of the work previously done with software can now be done more efficiently with hardware. Processors dedicated to various tasks (such as I/O) work in parallel, freeing the main processor of much of the burden it previously carried.

Not only does the mainframe more efficiently carry out the computational tasks for which it is well suited, but the structure of the overall system is more systematic. This structure simplifies the basic software, and in most cases reduces the cost of software development and maintenance.

The design of microcomputer systems builds on experience with large mainframes and minicomputers. Although the original machines had to be programmed in machine language, almost immediately assemblers appeared on the scene. Soon powerful relocatable macroassemblers, both resident in the microcomputer and cross assemblers operating separately on large computers, were used to generate code for these systems. Very soon thereafter BASIC became available for most of the chips. Now FORTRAN, PL/M, and Pascal are available for several microprocessors and are being programmed for other chips.

Sophisticated diskette systems are currently being marketed for use in microcomputer systems; this development indicates the speed with which microcomputer software is progressing. The spread of microprocessors and microcomputers into both the computer market and the consumer market, both extremely competitive, proves that they can be economically viable.

VII. Assumptions

Any forecasts about the nature and the costs of software development for microprocessors and microcomputers in aviation must be made in the context of possible hardware configurations in which microprocessor chips will be found, and with attention to the architecture of the systems envisioned. Current trends indicate three roles for microprocessors in aviation: as controllers, e.g., in aircraft and environment systems; as components of the data processing system, e.g., ground-based radar control systems; and as a personal aid, e.g., for sensing the environment, calculating distances and retrieving information, as in a wrist calculator-watch-thermometer.

A. Microprocessors as Controllers

Microprocessors will be used as controllers to sense and control various functional components of the aircraft, environment, radar and communication systems, both in the air and on the ground. Microprocessors in small systems dedicated to specific functions will communicate with other functional systems via I/O ports, as external devices. In the aircraft, for instance, they will form a network which, because of the digital nature of the communication, will be able to pass multiple signals along common interconnections, thereby saving costs of wiring and increasing reliability. Examples of this type of application appear already in

microwave ovens, microcomputer video games, and computer interfaces. The cost effectiveness of such applications is already well known in the hardware design community.

Within large mainframes such controllers will interface with various hardware components, whether mass storage devices, graphic CRT's, or radar antennae, either airborne or on the ground. (Early versions of some of these chips are already on the market.)

B. Microprocessors as Components of Mainframe

More important for overall cost considerations, microprocessors will take a significant place in what is today considered the main task of the mainframe. Just as dedicated hardware assumed the role of software in the form of multiply/divide circuits and then as floating point hardware, hardware will assume portions of the software role in other traditional mainframe tasks. One microprocessor component may, for example, be used to interrogate aircraft for altitude and other data, another to calculate the possible cone of travel, and these will be interacting with other such processors via shared memory. The mainframe would no longer carry the entire burden of calculations but would control the distributed network of microcomputers and assume those scheduling and comparator tasks for which it is well

suited. The modular design of both hardware and software in such a system, a structured design approach, leads to lower overall design and implementation costs and increased reliability.

C. Microprocessor as Personal Calculational Aid

The third application area for microprocessors is in a personal computer for the various personnel in aviation. A microcomputer can serve as a highly sophisticated calculator and personal information system requiring minimal interaction with the other aircraft systems. In this application the architecture would resemble that of today's minicomputers in that some removable mass storage medium would be available for storing commonly used user software and data. Input would be via a keyboard and perhaps analog devices such as thumb wheels or joy sticks. The display device would use LED, LCD, CRT or gas plasma panel technology. This system could be interfaced to the instrument panel, making available to the computer such parameters as airspeed, ground speed, and direction. The system software and the language processor for the high level, user-oriented language would be stored in read-only memory. Such a language might resemble the language of today's programmable calculators or it might resemble an interactive user-oriented language possibly derived from BASIC.

D. Well-Defined Subtasks

The microprocessor is very well suited to such well-defined subtasks as following the progress of an individual aircraft. Its speed is easily sufficient to predict the future positions of aircraft. This microstructure only needs to inform the mainframe if the specified aircraft deviates from a specified trajectory, or if it receives an indication of a possible collision course from its interaction with the other dedicated microprocessor. As a hardware controller, e.g., controlling a CRT displaying radar information or controlling the internal environment of the aircraft, its task would be equally well defined. One could readily specify the needed output for each possible input. In the case of the CRT controller the task is to display the ever-changing information on the screen as instructed by the mainframe; for the air handling apparatus on the aircraft, it would be maintaining some range of temperature and pressure as a function of the current altitude. Indeed, even as a calculation aid its task could be well defined in terms of an implementation of a specific user-oriented software system. The formal definition of such a language, together with the I/O of the hardware system, would clearly delineate its specifications.

With such a design the costs incurred will be amortized over the production of a large number of identical modules, thus reducing the cost per individual unit produced. The design effort is assumed to be an integrated one involving both hardware and software in a unified treatment. Because of the need for a higher level of decision, that is, to determine which of the tasks should be handled by either hardware or software, hardware and software design must be considered together as total system design. This total system design will be accomplished in terms of the tasks that must be implemented and their subdivision into manageable subtasks. Each subtask will then be implemented as a unified hardware/software module independent of all other modules except as clearly defined in the formal interactions with other subtasks.

E. Hardware Replaces Software

In such a unified design, hardware will replace some traditional software functions, as was accomplished earlier with chips for floating point multiplication and division. Also software will replace hardware as in the use of microprocessors to handle control tasks previously carried out by hardware logic. Each module will be treated as a functional unit and will be implemented in the appropriate hardware/software mix to make

its design, implementation, and use both economical and reliable.

F. System Simplifications Due to Modularity

Due to the highly modular nature of the systems, whether control systems or mainframe applications, replacement of components will be straightforward when the system needs updating or when a failure occurs. Each module is defined in terms of its inputs and outputs. For each input condition the module's task will be clearly stated and the expected outputs will be a necessary part of the documentation needed in the original design. When it becomes necessary or desirable to replace a module, all that is needed to insure system integrity will be to determine that the new module is functionally equivalent, i.e., that it generates the identical output for the identical input. As new hardware technology becomes available this will be easily implemented by merely changing the modules involved. If the system needs to be expanded, this can be accomplished in a modular manner. If errors are found in a module, their effects will not create any major redesign difficulties, as the errors will only affect one module and possibly its communication with neighboring modules. Approaching the design of a system in a proper, structured fashion achieves a degree of modularity which will decrease

design and implementation costs and increase reliability and modifiableness.

G. Task-Oriented, Structured Programming Languages

Because of the new architectures, older languages such as FORTRAN will lose their dominance and a new set of structured, task-oriented languages will emerge. FORTRAN is based on the uniprocessor system, a system with just one CPU, and on a set of control structures patterned after those available in the assembly language of early computers. Although it is not well adapted to real-time applications, it has been used in these areas. However, it lacks many important features of a well-structured language, for example, control structures, nested blocks with locally-defined variables, and the ability to do extensive compilation time checking of the programs. The general purpose languages, such as PL/1, are now recognized as less appropriate for many modern computing tasks than special purpose, task-oriented languages. Programming control for the CRT display of a ground controller is more efficient in a language designed for displaying the dynamic information on the graphics screen than in a general purpose language within which each screen command must be individually programmed. Similarly, it will be easier to program a microprocessor to handle the sensing and control functions of the

on-board aircraft control system in a language that interfaces easily with analog to digital converters and which is designed to handle hardware interrupts, than to do the same task in language such as FORTRAN which was designed to handle solutions to algebraic equations. Such specific purpose languages are constantly being developed in response to needs and will be part of the standard set of software tools available to programmers of the distributed systems described earlier in this chapter.

H. Design Tools to be Developed

Design tools in computing as in other fields tend to be developed in response to perceived needs. Those tools needed by the system designers of distributed systems described in this report are currently being developed and will continue to be developed as new needs arise. These tools include techniques of structured system design, methodologies to increase the reliability of software, and special purpose languages designed for tasks at hand.

VIII. Forecast of Microprocessor Software

A. Personnel will Apply Skills and Abilities to Software Design, Reducing the Time Required for Development

In the future, persons working on what today are software problems will have new skills and abilities to

apply to their solutions.[1, 9, 11, 6] In part, an improvement in skills will be due to new tools available to software designers. In part, people with additional abilities will be attracted to the field.

First, the old distinctions between hardware and software will fade. Experts will apply a mix of tools and resources to the design of systems, and be comfortable about crossing over the old boundaries between software and hardware. Teams working on problem solutions will include persons expert in the technology to which computers are being applied, for example, radar. Experts in the application will be no less important in the design of the software system than in the implementation of specific applications.

Second, personnel will understand and be able to implement well structured, modular systems. Persons now being trained in computer systems are learning significantly different approaches to software design. In high technology fields such as aviation, such persons will be readily available as project managers by 1985.

Third, personnel involved in design of systems will effectively assign to hardware and software what is best done by each. Such decisions are already becoming important and will assume a major role in the design of computer systems by 1985. This integration of hardware

and software will result in systems with different architectures, but the systems will be simpler, less costly to design, and easier to maintain.

The design team will be composed of at least four types of individuals, all trained to interact effectively, combining their skills to design the target computer system. The four experts will include: the hardware designer; the software designer; the person knowledgeable about the specific equipment to be controlled, sensed or otherwise used; and the designer working on the problems of human factors and methods of more reliable and easier communication with the end users. For example, within the team working on a new graphics display for the ground controller, a variety of questions must be answered during the design process: What should be done by hardware and what by software; what is the nature of the communication between the display device and the remainder of the computer system; what is the most effective method to display the needed information so that the human ground controller can obtain the information he or she needs in the minimal time with minimal error? Answers to these and other questions can best be obtained by the members of the design team working together, each drawing from his or her unique background to obtain the best design possible.

Such a design team will approach the problem by considering the tasks that need to be implemented and specifying them carefully and completely. Individually and together, members will consider the hardware, software, and human tradeoffs involved with alternate designs, covering a broader range than currently possible. A team effort results in a cost-effective and reliable design that is cheaper to implement and modify and more reliable than current designs.

B. Costs for Software Development and Maintenance Will Decrease, With Savings Related to Modularity and Distributed Processing

Initial costs in the design of new large systems will be slightly less than at present for comparable complexity and reliability.[1] Costs will hold steady or decrease slightly (not allowing for inflation) because of the effective use of modular design concepts and new design tools. To some extent, programming tasks will be replaced by hardware solutions. However, increased demands for reliability and perhaps for new services will tend to increase the overall cost of large systems. New components can receive very thorough testing without the high costs associated with testing modifications in systems today. In sensing and control applications, costs can be expected to be reduced by 30 percent by 1985, while in data processing applications costs can

be expected to increase by 25-35 percent until 1985. By that time distributed processing will be a generally accepted design solution, after which costs may be expected to decline by a like amount by 2000. These estimates are represented graphically in Figures 45 and 46.

Projection of software costs into the future involves considerable uncertainty. Generalizable measures are very difficult to extract from specific cost figures in any present software project because of great variability in requirements and constraints from one project to another, and indefiniteness in measures of program size and complexity. A hypothetical average of software costs for 1975 has been taken as a baseline (100 percent) around which percentage projections are made.

The most pessimistic among reasonable estimates indicates a slight increase in cost over the next 15 years after which it levels off. The optimistic estimates, taking into account improvements in software engineering, show a sudden drop in costs. The best estimate that can be made at this time for sensing and control systems software is shown by the center line in Figure 45 with the outer lines indicating a very approximate 90 percent range of confidence.

FIGURE 45: RELATIVE COST OF SENSING AND
CONTROL COMPUTER SYSTEMS SOFTWARE

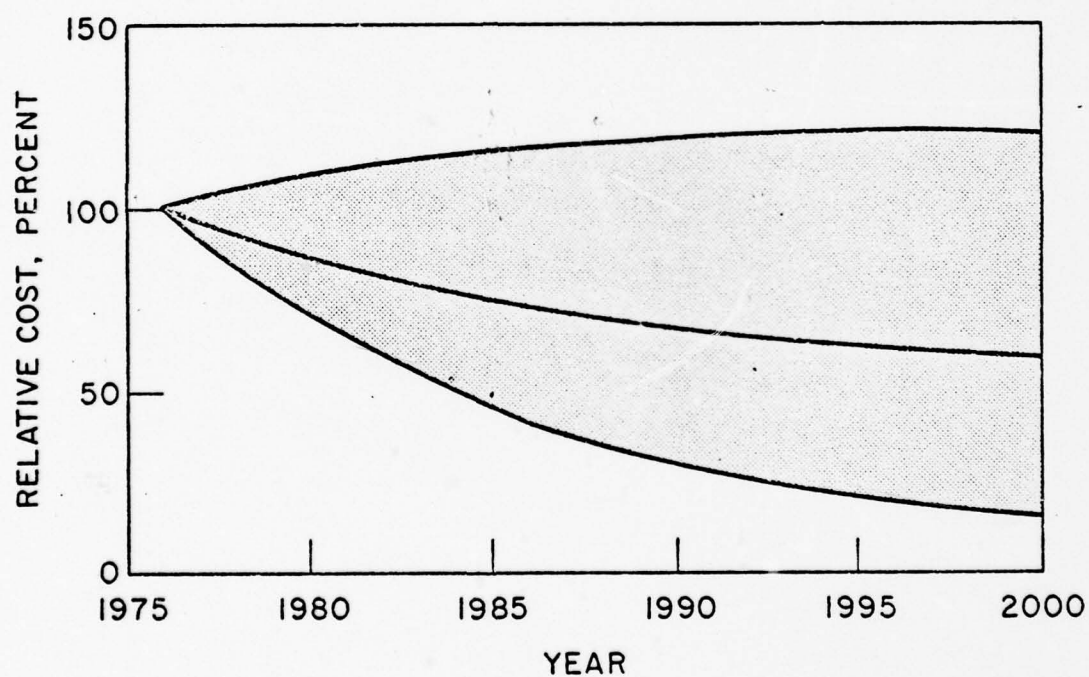
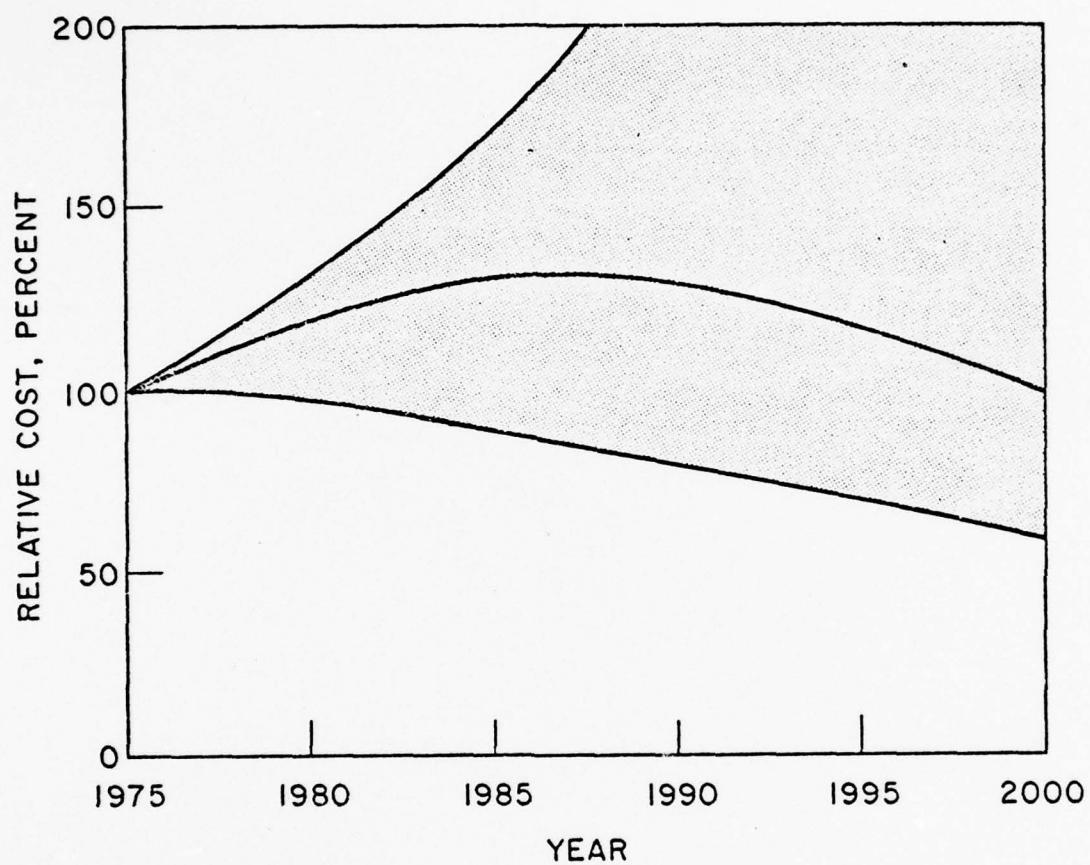


FIGURE 46: RELATIVE COST OF DATA PROCESSING
SYSTEMS SOFTWARE



The cost of software for data processing software has even more variance in predictions. The best estimate shows an increase and then a return to the same level of expenditures, indicated by the center line in Figure 46. However, if the new programming techniques are not used effectively, costs could resume the rapid increase evident in historical data for complex systems. On the other hand, effective replacement of software by hardware in data processing systems could bring costs down considerably. The outer curves indicate an approximate 90 percent confidence band.

Costs for updating a system will be considerably lower than at present. Savings will be accomplished through modularity in design, and increased willingness to replace components piecemeal. Many potential modifications will affect only one or a few modules in a system, and no others need be changed if the inputs and outputs of those few continue to match the requirements of other modules. New components will carry the software changes on chips which can be thoroughly tested with automatic means before installation. Then they are simply plugged in throughout the system.

A similar system of a different size, for example, a ground control system for a different airfield, will be obtained at a very small additional cost. Since size or capacity will tend to relate to the number of dupli-

cate modules (e.g., for the number of aircraft to be monitored), it can be increased through the addition of microprocessors rather than by increasing the size and speed of one central computer system. The central system may have to be enlarged to handle the added demand of the greater number of microstructures. In the case of a ground controller system with dedicated microstructures following the courses of individual aircraft, when expansion is needed to handle more aircraft, there will be an increase in the number of such microstructures needed which will be proportional to the increased number of aircraft to be monitored. This will necessitate a change in the controlling processor to handle the increased work load of managing the system. This increase in system size and the costs associated with it will be considerably less than similar costs incurred with today's systems.

Any increases in software costs will be due to new requirements set for the system. The additional capabilities provided system designers, to some extent shifting costs from labor to hardware, and involving fewer higher level staff, will result in savings of a few percent per year. Expectations for additional service from the centralized computer systems will increase software costs in proportion to the added complexity of the requirements. However, the structuring

of systems, including distributing some of the processing into components of a central system, will accommodate increased demands without corresponding increases in complexity. Indeed, some things which might now be expected to be part of a central system will be handled by personal calculators (pocket minicomputers) which make little or no demands on the central computer.

C. Reliability of Software Will Increase

The modular design of systems which integrate hardware and software will increase the reliability of performance of those systems. The design process will greatly reduce the likelihood of error in the initial product. The hierarchical and modular structure that will be used in future systems will facilitate reliability (preventive maintenance) and use of backup facilities at the microstructure level. A spare stock of modules can be maintained and modules can be replaced in the event of equipment failures.

Because the cost of duplicate microstructures is of little consequence relative to overall costs, different algorithms for serving a highly critical function such as tracking an aircraft can be put on different processors and compared by a monitor which determines discrepancies. On recording a discrepancy out of tolerance, the central processor will be alerted, thus notifying a human controller.

Present day systems are not truly expandable. Since most of the calculational burden is supported by a single large and fast processor the best that can be done is to obtain a scaled up version of that processor which is capable of higher speed and has more memory. Then the programmers must reprogram the entire system, taking into account the increased calculational load. The design of most of the current software systems makes this revision a major task. With a modular, structured design approach such expandability will be much more obtainable, thus allowing the systems to grow with need without much concern for modification costs.

Software reliability will also be increased through the use of techniques for proof of program correctness, and through use of good programming techniques to insure the robustness of the software--the ability of the software to tolerate errors. Research into such techniques is currently progressing and will continue to progress due to the current urgency of the need for such methodologies. By 1985 new techniques to improve program reliability will be sufficiently advanced to be very useful to the design team and can be expected to be a part of any such computer design.

In summary, personnel needed to design future systems will bring a new set of talents and tools to the design

process of future computer systems. They will be organized in design teams which will deal with the computer hardware and software in a unified manner using structured design techniques. Software costs will decline after about 1985 while reliability will increase.

CHAPTER SEVEN

AVIATION APPLICATION OF MICROCOMPUTER TECHNOLOGY

I. Introduction

A. Background

In the previous chapters, a number of technologies related to the microprocessor and microcomputer industry were described. Measures of performance, such as speed, size, power requirements, reliability, weight and costs, were forecasted for specific time periods to the year 2000. This was done at the component level as well as the system level.

In addition to these hardware related parameters, the software environment and its evolutionary development over the same time frame was presented.

The purpose of this chapter is to present both near-term and long-term feasible applications of microcomputers and microprocessors within the National Aviation System (NAS). It will be shown that a number of present day programs within the Federal Aviation Administration (FAA) are already reacting to the existing microcomputer technology. In addition, the industry as a whole, such as airframe manufacturers, avionics manufacturers and powerplant manufacturers, are taking advantage of the microcomputer technology.

Applications will be categorized into "landside" (ground-based) and "airside" (airborne). Portions of the discussion will delineate present day planned applications, many of which are in the laboratory testing stage, others are undergoing tests under actual conditions and still others have already appeared in the marketplace.

In Chapter Five two important application areas were cited, control/instrumentation and data processing. As Figure 31 of the control/instrumentation system shows, a number of peripheral devices are required in such an application. The applications discussed in this chapter will also require numerous peripheral devices. Such peripherals as analog-to-digital converters (ADC), multiplexers (MUX), control actuators, sensors, keyboard inputs, magnetic tape or magnetic disks, electrostatic printers and electronic displays, such as the cathode ray tube (CRT) and flat gas panel devices (GPD) will be included. The charts and figures presented in Chapter Four indicate that the peripherals can have a major affect on system costs, weight, size and power requirements. For example, the CRT display in the control/instrumentation system, required more than 60 percent of the total system power requirement. Because of this influence on system requirements, their future development will play an important role in determining the impact of microcomputers within NAS.

Another reason for the importance of peripherals is that they serve as the input/output (I/O) units. Their

adaptability and versatility will determine the success of the man/machine interface within a number of the applications. Therefore, attention will be given to available, as well as, forecasted I/O technologies in the applications discussed.

B. Assumptions

The long term future applications discussed in this chapter will assume that parameters such as size, cycle times, weight, etc., are at their early 1980's levels as forecasted in Chapter Five. One reason for this assumption is that normally about ten years is required to obtain a fully operational subsystem for field implementation, from the time that a requirement for such a subsystem is recognized within the FAA. Since studies to determine feasibility and effectiveness of new concepts, as well as acquiring funding for extensive experiments and building of a "breadboard" system can take 3-5 years, it is expected that early 1980 technology is current. The ten year figure, of course, assumes a non-trivial system change.

The two computer systems described in Chapter Five were presented for the purpose of recognizing the impact of technological development on the system parameters. Since both airside and groundside applications will be presented, some of which will involve a dedicated

microcomputer, while others may border on a general purpose microcomputer, an additional hypothetical microcomputer will be described. Its total computing capacity will fall between the capacities of the systems described in Chapter Five.

Since a significantly large programmable memory (using software) will be specified and no particular peripheral devices are included, it is reasonable to interpret this microcomputer as a general purpose computer (see Table 19). This hypothesized system will only serve as a benchmark, since acceptable levels of size, weight, power requirements and cost are dependent on the application of the microcomputer. For example, a system designed for a general aviation (GA) light twin turbo-powered aircraft will have requirements which are quite different from those which would apply to a system used in commercial jets.

In order to put the processing capability of the above microcomputer into proper perspective, the description of the capabilities of the minicomputer used in the automated radar terminal system, known as ARTS-3 is given in Table 20.

The functions of the ARTS-3 computer are:

1. Receives and decodes identity and altitude of aircraft using encoded beacon information;
2. Tracks up to 150 beacon equipped aircraft; and

TABLE 19: GENERAL PURPOSE MICROCOMPUTER

Word Size:	8 to 16 bits
Cycle Times:	500 nanoseconds (5×10^{-7} seconds)
Memory RAM:	1 mega bit (LSI Technology)
Memory ROM:	512 K bits (LSI Technology)
Number of Gates:	10,000
Power Requirements:	24 watts (approximately)
Size:	100 cubic inches
Weight:	3 lbs. (not including power supply)
Cost:	\$500.00 (approximately)

TABLE 20: ARTS-3 MINICOMPUTER

Word Size:	32 bits + 4 bits for parity
Cycle Times:	1 μ S (microsecond)
Memory:	1.5 mega bits
Power Requirements:	1800 watts
Size:	65,000 cubic inches
Weight:	800 lbs.

3. Presents track data using alphanumeric output to identify each aircraft on a plan position display.

Therefore, the microcomputer described has twice the speed of the ARTS-3 minicomputer and its size, weight and cost would permit it to be included in a large portion of general aviation (GA) fleet. The \$500 cost of this computer, when compared with an expected cost of \$750 for a transponder in the Discrete Address Beacon System (DABS), indicates that such a microcomputer would affect the total avionics costs to only a small degree.

II. Near Term Applications of the Microcomputer Technology on Aviation (1977 to 1980)

A. Landside

At the present time, there are several systems being studied and tested for possible implementation within the UG3RD System which incorporate microcomputers, specific examples are:

1. Modernized Flight Service Systems

The planned modernization of the Flight Service Stations (FSS) in the Upgraded Third Generation (UG3RD) ATC System includes a number of new applications of microcomputers.

The present plan calls for centralizing the 292 flight service stations into 20 major hubs. The use of large mainframe computers for the retention of weather data, ATC system status, Notices to Airmen

(NOTAMS), etc., and specialized Flight Service Specialist consoles and displays are included in this plan. Because of this centralized mode of operation, the use of pilot self briefing capability, as well as, direct contact with Flight Service Specialists plays an important role in this system [4].

Within the proposed system, the specialist will have access to the large data base, maintained in the central computer, by the use of terminals incorporating graphic displays and having keyboard entry capability. Specific applications of microcomputers, in the segment of the system, are in the area of "intelligent terminals." Such terminals would contain a processor and associated memory. This would permit processing of data received from the main computer within the processor itself. The degree to which a terminal attains the status of being described as "intelligent" depends on the processing capability of its internal computer.

Several enhancements of the modernized FSS system are planned. Among these is the widespread use of "self briefing terminals" for users. Such terminals will permit direct access to the data by the user. A number of studies are in progress which are investigating different design concepts of such terminals. These include the use of touch phone terminals with voice response, keyboard entry and hardcopy typewriter

or printer terminals, as well as, terminals with graphics display capability.

The voice response method requires a computer for transforming and processing digitized data into voice output. One such system under development at the Transportation System Center uses 11 Intel 8080 microcomputers for this function.

Graphics involve transmission of large amounts of data from the central computer to the terminals via telephone lines. With the use of microcomputers at the terminals, it will be possible to transmit data in compressed form and perform the processing at the terminal, in order to drive the display. With time sharing of input lines through multiplexing, more users can be served with a fixed set of data lines. In addition, it is expected that many different types of terminals will be in use, each having its own special data formats. By internal processing, using a microcomputer, the required transformation of formats from one type to another is performed at the terminal. Thus, the central computer can communicate with these remote terminals without performing any preprocessing of the data.

2. Landing Systems/Takeoff Systems

Wake Vortex and Wind Shear Detection

One of the high priority goals of the Federal Aviation Administration (FAA) and the major objective of

the wake vortex program is to allow an increase in capacity at high density air terminals. The Vortex Advisory System (VAS) is one specific attempt at realizing this goal. Based on analysis of large amounts of data, on the behavior of vortices under varying meteorological conditions, criteria for wind patterns have been developed. At present, a feasibility study is underway at Chicago O'Hare. The system contains meteorological sensors mounted on towers. Output of the sensors is digitized and transmitted to microprocessors (Intell 8080 A) where the data undergoes preprocessing. Each of these microprocessors contains 8K of Read-Only-Memory (ROM) and 8K of Random-Access-Memory (RAM). Each microprocessor (one for each tower) is packaged on a single plug-in board. A separate microprocessor, centrally located, is used to calculate allowable aircraft landing separations as a function of the vortex conditions under the existing meteorological conditions. Output is transmitted to a display console at the controllers position.

Wind shear detection studies also include the use of lasers. Data will be processed to predict the time of occurrence of a hazardous shear condition in the flight path of an aircraft. In order to minimize false alarms and maximize detection probabilities,

various algorithms are used to process the sampled data. At present, this system is in an early state of development [7], [8].

Some on-board detection methods are also under study. One of these methods considers predicted abrupt changes in ground speed by processing data from the Distance Measuring Equipment (DME) and comparing computed wind velocities along the final approach path and reported surface conditions. When the present ground speed of the aircraft differs from the predicted ground speed by a large amount, this information indicates the existence of a wind shear condition at a point along the flight path. This information would be relayed to the pilot through a display on the instrument panel.

3. Terminal Applications

Surface Control

Short term plans in Airport Surface Traffic Control (ASTC) call for the updating of the Airport Surface Detection Equipment (ASDE) using NU-BRITE displays. In addition, an updated version of the ASDE-2 radar, the ASDE-3, will be programmed for development

- a. At airports that need ASDE but do not presently have any equipment and
- b. As an eventual replacement for the aging ASDE-2's now installed.

The new ASDE-3 is based on solid-state technology and achieves improved performance over the older ASDE-2 equipment. It also is more reliable and less costly to maintain. The ASDE-3 will be able to "see through" heavier rainfall and will have an improved controller display. The improved display utilizes digitized enhancement of the radar return by using a processor to suppress undesirable returns from the radar and strengthen the returns from taxiways and runways by enhancing boundary definition. This digitized enhancement function is within the capabilities of present day microcomputers.

B. Airside

1. On-board Avionics

a. Area Navigation (RNAV)

Concept Description

There are a number of different RNAV systems which are distinguished by their capabilities in defining flight paths limited to either two, three or four dimensions. The fourth dimension being time.

RNAV permits electronic relocation of the geographic location of high frequency omnidirectional navigation sites (VOR) and distance measuring equipment (DME). Each relocated or actual VOR is referred to as a way point and the specification of two way points defines a route segment.

The complexity of the route structure, in terms of number of way points, altitudes at each way point,

times at specific points along the route, which can be specified, depends on the processing capability of a microcomputer. Thus a system permitting 20 way points and having a four-dimensional capability, requires a microcomputer with more computing power than required by a system which only permits two way points and has a two-dimensional capability.

The control/instrumentation application presented in Chapter Five is suitable for describing the RNAV microcomputer. A block diagram of such a system is given in Figure 47.

The ROM memory would contain the program which would control the input of information from the peripherals, as well as, process way points, altitude and time parameters, for generating the flight segments. Complete program control of the output displays would also be contained in the ROM. The programmable RAM memory permits storage of a variable number of way points, frequencies of VOR(s) altitudes and time constraints. The alphanumeric display would present the identity of the way point (VOR frequency) indication of time discrepancy along the flight path and increase and decrease in airspeed required to correct time errors.

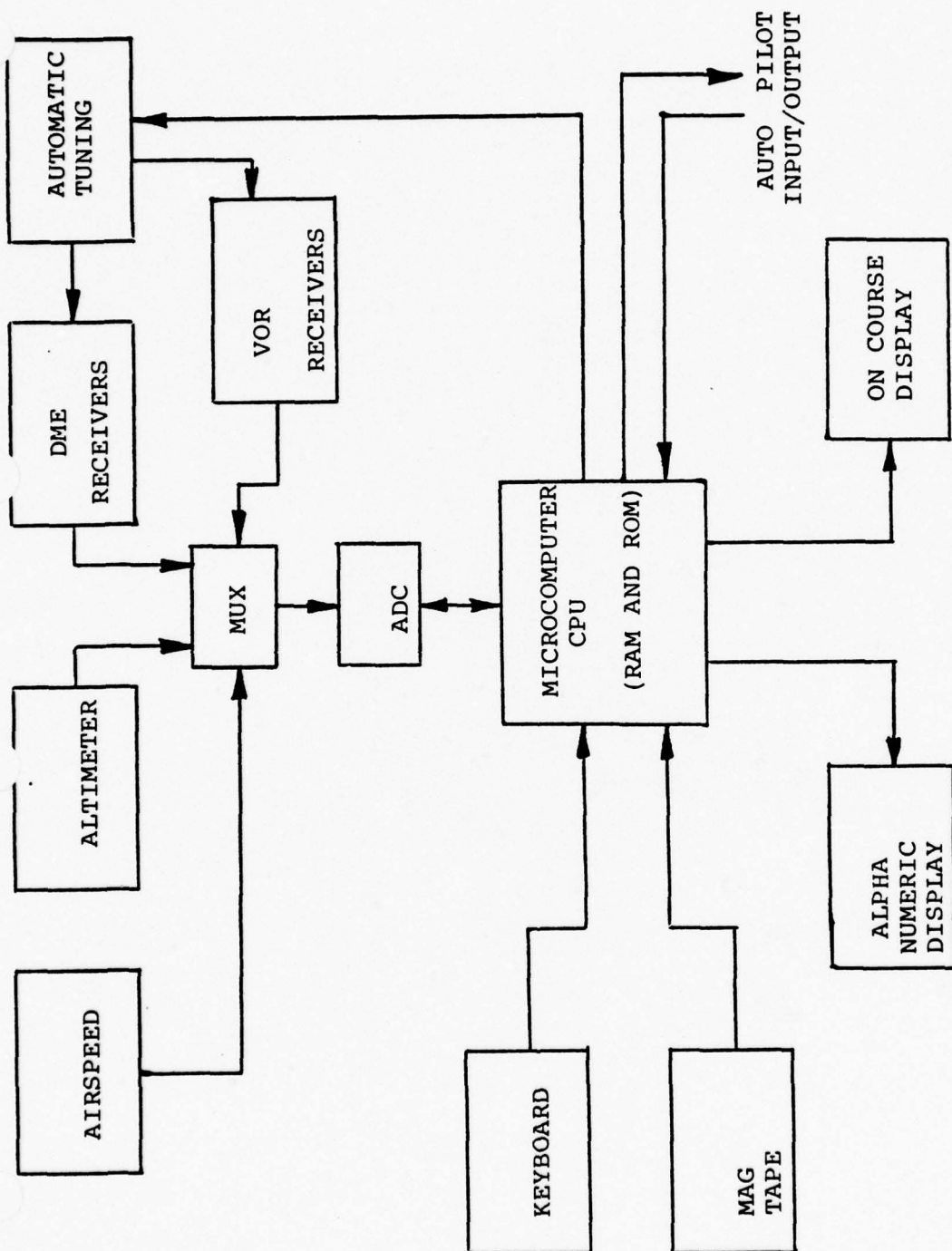


FIGURE 47: RNAV COMPUTER

b. Affect of RNAV Capability on the Terminal System

The use of two- and three-dimensional RNAV, in terminal areas, has been considered [12], [16]. These studies featured the use of special arrival and departure corridors, defined by way points. Such paths permitted maximum use of continuous climb-outs and descents along conflict free routes. Parallel offset routes for passing and segregation of traffic by destination airport in metroplexes (terminal areas with multiple high density airports) were also included. The conflict free routes are achieved by defining standard routes with prescribed non-intersecting altitude range at two-dimensional intersections. Results to date indicate that the use of two-dimensional area navigation in metroplex areas would have significant affect on relieving airspace congestion, reducing aircraft block time and reducing controller workload, particularly in time spent analyzing traffic situations for possible conflicts and reducing the amount of vectoring required to get the aircraft on the final approach path. Near term requirements for such an area navigation system include:

- (1) Six way point storage capability
- (2) Parallel offset capability in one mile increments up to 8 miles

- (3) Navigation accuracy comparable to a VOR/DME system with slant range correction

A number of evolutionary phases have been predicated on the number of user aircraft suitably equipped. These are:

- (1) Phase 1 - Few equipped user aircraft
- (2) Phase 2 - Significant number of equipped user aircraft (less than a majority)
- (3) Phase 3 - Majority of equipped user aircraft

These transition phases would be designed to provide operational incentives to encourage users to acquire the equipment. Initial steps in the Phase I system would include:

- (1) Complete arrival/departure route design
- (2) Addition of parallel offset routes
- (3) Separation of traffic by airport in multiple high density airport areas
- (4) Incorporation of metering and spacing

The existing concepts of metering and spacing involve path stretching techniques by issuance of radar vectors to pilots by controllers. An RNAV capability enables the system to also utilize speed control to a greater degree. The flight path itself would remain fixed, except for a small base leg vectoring area to reduce residual errors, just prior to final approach. The benefits of such a system are: aircraft navigate to within a few

miles of the outer marker without any vectoring by the controller and that airspace requirements for arriving aircraft are reduced, since the need for vectoring airspace is reduced.

The existing capability of on-board navigation computers would relieve pilot workload during arrival and departures. In addition, vertical navigation could be used as a backup to the instrument landing system (ILS) or microwave landing system (MLS) glide slope by controlling descent angle. This could result in the reduction of instrument flight rule (IFR) landing minimums at non-ILS runways. A general aviation two-dimensional RNAV system is described in the following section.

c. Existing RNAV Capability for General Aviation

For many years, avionics for general aviation typically were "stripped down" versions of equipment developed for commercial airline use. This often resulted in a reduction of performance, in order to achieve lower costs. However, at the present time, there have been developments in general aviation avionics systems which are making full use of the microprocessor and display technologies. Features in these systems surpass those found in even the latest commercial airline hardware.

One such system includes Dual Comm/Dual Nav/ILS. The system also includes an on-board computer which goes beyond the normal requirements of providing an RNAV capability. It serves as a master control center that permits the pilot to perform avionics channel changing from a keyboard device, as well as, inserting impromptu way points for area navigation. Through the use of a magnetic card programmable hand calculator, the pilot can insert up to 10 different way points. By connecting this hand calculator to the on-board computer, automatic loading of this information takes place. The on-board computer utilizes large-array microcircuits and two microprocessors. The system is designed in a modular form, so that by adding plug-in cards, a basic system can be extended to an ILS glide slope and marker beacon capability.

Not only is this system a complete solid state system, but also all moving parts such as synchros, motors, relays and resolvers have been eliminated. Plasma discharge displays are used, for the course deviation indicators and ILS glide slope indicators. Digital format plasma discharge displays also show the VOR radials, distance information or ground speed.

The microprocessors within the system permit the use of "intelligent filtering" to sort out spurious

replies from ground interrogators to provide more consistent distance data.

2. On-board Displays

a. General Aviation

In the previous section, plasma discharge displays which have appeared in the general aviation avionics market were discussed. Because of the absence of moving parts, such displays are expected to exhibit improved Mean Times Between Failures (MTBF). This in turn will have an impact on reducing maintenance costs and thus have a major affect on life cycle cost to the user. For the near term, some additional improvements in this area can be expected, viz: present day electro-mechanical displays will be replaced by solid state electronic displays.

b. Air Carrier

For the commerical carriers, somewhat more sophisticated devices are being tested for possible implementation. The "Heads Up Display" (HUD), is one such device. For some time, the military has been investigating the suitability of these devices for improving tracking, targeting and landing capabilities. However, there are HUD systems being tested in the air carrier environment also.

The flight testing of a HUD system, which is aimed at meeting the requirements for an all-weather

landing monitor and on-board visual approach slope indicator for commercial airline aircraft will begin early in 1977. The system at present offers the following advantages to pilots:

- (1) Independent monitoring of automatic landing systems during IFR approaches
- (2) Elimination of transition problems from IFR to VFR during the approach, since all the guidance required is in the HUD.
- (3) On-board vertical guidance for runways, where external aids such as ILS or visual approach systems (VASI) are unavailable.
- (4) Detection of wind shear conditions and guidance
- (5) Pilot workload reductions through reduced instrument scan requirements

The present system uses a cathode ray tube (CRT) and projects information onto a semi-transparent collimating lens mounted on the glass shield in front of the pilot. These data include:

- (1) Angle of attack
- (2) Velocity vector
- (3) Selected flight path marker
- (4) Potential flight path marker
- (5) Horizon bar
- (6) Aircraft symbol
- (7) Limit angle of attack
- (8) Synthetic sunway
- (9) True track indicator

Data is obtained by sampling the outputs of vertical gyros or inertial platform, vertical and longitudinal accelerometers. These are processed by a digital computer which drives the display. An image of the runway is generated by the computer by using the present position and altitude of the aircraft along the flight path and the geometric dimensions of the runway. The system also permits energy management by the digital processor.

The display system has proven to be quite effective in giving a pilot early visual cues as to the existence of wind shear. An abrupt change in headwind component results in immediate change in sink rate which is visible on the head-up display, because the velocity vector changes relative to the selected flight path and the angle of attack index.

An earlier version of this HUD system, which utilizes an electro-mechanical display, has been in use for over two and a half years for monitoring an autoland system in Europe. This system provides display of attitude, angle of attack and trajectory information, instrument landing system (ILS) deviation warning, decision height signal and "decrab" malfunction signal. The combination of the autoland system and the HUD has been used for Category III A conditions. This permits

decision heights of 50 feet and runway visual range (RVR) down to 450 feet. Over 2000 automatic approaches have been logged using this system with over 95.7 percent of these terminating in a completed automated landing and the remainder ended with either a manual landing or go-around.

The above system is by necessity very complex. The number of different data sources and the critical visual presentation, for the pilot, involves complex data processing. Microcomputers, because of their predicted low costs, size and processing capability, can be expected to contribute to the development of the HUD devices in the near future.

III. Future Applications of Microcomputer Technology in Aviation (1980-2000)

In Section II, a number of near term applications in the National Aviation System (NAS) were discussed. The number of specific applications of microcomputers which are at present being analyzed and tested indicate a high degree of awareness of the potential of microcomputers. The forecasted evolutionary development presented in Chapter Five of microcomputers indicate that they will possess characteristics which should cause serious consideration of a large number of additional applications within NAS. The forecasted decreases in physical size, power requirements and costs are particularly important. The adaptability of the microcomputer will be increased by the

existence of a large completely programmable random access memory (RAM). Certain functions would be "hard wired" by being coded into the read-only-memory (ROM). However, additional functions, when desired, could be programmed and these programs could be input through a peripheral device such as a tape disk. In addition, the actual size, in terms of bits, of the RAM and ROM can be increased by the use of plug-in modules. This will be particularly beneficial to users in general aviation (GA) who could start with a basic system and then add on to it as their need dictate.

In this section several applications, which are feasible in the 1980 to 2000 time period, will be presented. These applications are based on normal evolutionary trends in the microcomputer field rather than being predicated on revolutionary "breakthroughs."

A. Landside

1. Flight Service Stations (FSS)

The internal computing capability which a remote computer terminal contains determines the level of "intelligence." Because of the expected low cost of future microcomputers and the total number of bits contained in the RAM and ROM memory, very sophisticated terminals will be developed. The success of the centralized FSS concept is highly dependent on the ability of the users to obtain direct access to large amounts of data to be able to select only that data which is of interest to their specific mission. The "intelligent

terminal" offers such a capability. By reducing the requirements for a user to possess a high skill level in operating a terminal, the use and versatility of the automated portion of the system will significantly increase. This, will in turn, reduce the frequency of direct contacts between flight service specialists and pilots. Since the one-on-one basis of operation (specialist-pilot) increases manpower requirements, such reductions will reduce operating costs. Terminals will possess the ability to take an "active" role as an agent for the users, in interfacing them with the data-base. They will provide "instant operating instructions," and identify data-blocks which can be selected through a "fingertouch" method. Upon user command, "hardcopy" of such specifies as weather data, flight plan filed, clearances, etc., would be available. Through software control such terminals could present continuous information of the latest weather data for the area in which the terminal is located. Time sharing of data links between the terminal and central computer complex multiplexing of communication lines will greatly reduce the number of such lines required by the system.

The FSS must also serve the airborne user providing current weather along the flight route, accepting VFR or IFR flight plans, etc. To increase capacity and keep manpower requirements at an acceptable level, direct access to the data base by the pilot is essential.

Through the use of a data link and a microcomputer such direct access is feasible. By tuning the data link to the frequency allocated for the particular area, the pilot could request specific information such as weather, pilot reports (PIREPS) or indicate he wishes to file a flight plan. The microprocessor could obtain the information from the data base and format the information for transmission through the up-link. In the case of flight plan filing, the microcomputer could interrogate the pilot, using the up-link, for the required information. Long messages, from ground to air, could be transmitted using digitized voice which would be done under the control of the microprocessor. Digitized voice capability on the up-link reduces the complexity of the airborne data link capabilities. This would be essential in order that a large number of general aviation users would be able to acquire the equipment.

2. Remote Monitoring of Ground Based System

The presence, within NAS, of widely distributed ground based systems such as, VOR/DME, DABS/Synchros-DABS, Mini-DABS, requires large expenditures for operation and maintenance (OM) of these facilities. The new generation of solid state electronic hardware, in the ground based systems, together with the capabilities of microprocessors and microcomputers, permits the use of remote monitoring techniques. For example, a VOR/DME site contains the necessary transmitters, as

well as, environmental systems and emergency power sources for driving generators. By connecting a microcomputer, using a multiplexer and analog-to-digital converters, essential system parameters can be sampled. If operating levels of system parameters indicate degradation of operation, the microprocessor could control switching on stand-by transmitters or power sources. By using automatic "call-up" of central maintenance control, the system status could be presented to maintenance personnel at display stations or terminals. Through the terminals, the maintenance personnel could interrogate the microcomputer for additional data in order to pinpoint the cause of the problem. At this point, corrective measures would be taken.

In order for this concept to be cost effective, the total maintenance system must be designed to take advantage of such remoting capability. Location of spare parts and maintenance personnel, for servicing inoperative equipment are extremely important for obtaining a cost-effective system.

Several studies, [1], [2], [3], have analyzed the feasibility of the remote monitoring concept of the updated VOR/DME system and the associated environmental system. Different design concepts of the maintenance system have been investigated. Such levels of centralization as:

- a. Conventional Maintenance - Assumes the present maintenance structure.
- b. Area Maintenance - Assumes all VORTAC facilities in a sector are maintained from a single location, with technicians dedicated only to VORTAC maintenance.
- c. Highly Centralized Maintenance - Assumes all VORTACS in a region are maintained from a single location.

Together with these different maintenance concepts, several levels of remote monitoring were included.

These are:

- a. Remote certification of VORTACS.
- b. Remote monitoring and control of standby power systems and environmental systems.
- c. Remote fault diagnostics to subassembly level or printed circuit board level.

Results of these studies show that this technique can have significant impact on technician workload reduction. This in turn gives rise to an increase in productivity.

3. MLS - Monitoring

The monitoring and control of the time reference scanning beam MLS system would also be centered in a microprocessor or microcomputer. All data logging and diagnostics would be transmitted to central control.

Through the use of software and a high speed polling loop, all important system parameters would be monitored. The microprocessor, in the case of system

degradation due to parameters exceeding their specified limits, would generate alarms and take (pre-programmed) corrective actions or accept on-line commands from central control. Upon operator command, the identities of failed units would be provided in order of most critical first. This combination of automatic and manual modes of operation for performing diagnostic and fault isolation to subassembly levels, would provide a useful man-machine interface.

4. Automated Terminal Operations - Metering and Spacing (MS)

Planned enhancements for the ARTS-3 system include the concept of automated metering and spacing. These plans call for development of computer algorithms which would assign a landing sequence number of a given aircraft and computer headings and speeds which must be maintained in order that separation minimums are not violated and that the aircraft arrives at the runway threshold at a particular time.

In order to implement metering and spacing and other functions such as conflict prediction and minimum safe altitude warning (MSAW), a second minicomputer will be added to the present ARTS-3 system.

Initially, metering and spacing and conflict prediction will only make use of beacon derived positions and altitudes received from the MODE-C transponders. When MLS is installed, at terminal areas which have an ARTS-3 system, the metering and spacing algorithms can take advantage of the curved or multileg segmented

approaches, which users equipped with MLS can make. If RNAV capabilities are added, as well as some form of data-link, (either purely digital or a combination of digital and synthesized voice), the system can take advantage of this user capability. This simply means that way points, specific offset routes, segmented approaches as well as heading and speed information, could be generated by the computer and transmitted to the aircraft via the data-link.

The controller would have to be interfaced into the system by suitable displays and "intelligent terminals" to take over by manual control in special situations. This system, would by necessity, be quite complex. The computer would perform parallel processing and could be implemented by using a number of microcomputers which perform specific functions all under the control of a central control unit. The forecasts in Chapters Five and Six indicated that memory size and speed of computers, using LSI technology and structured programming techniques, would make them capable of performing tasks which now require relatively large minicomputers or medium size mainframe computers.

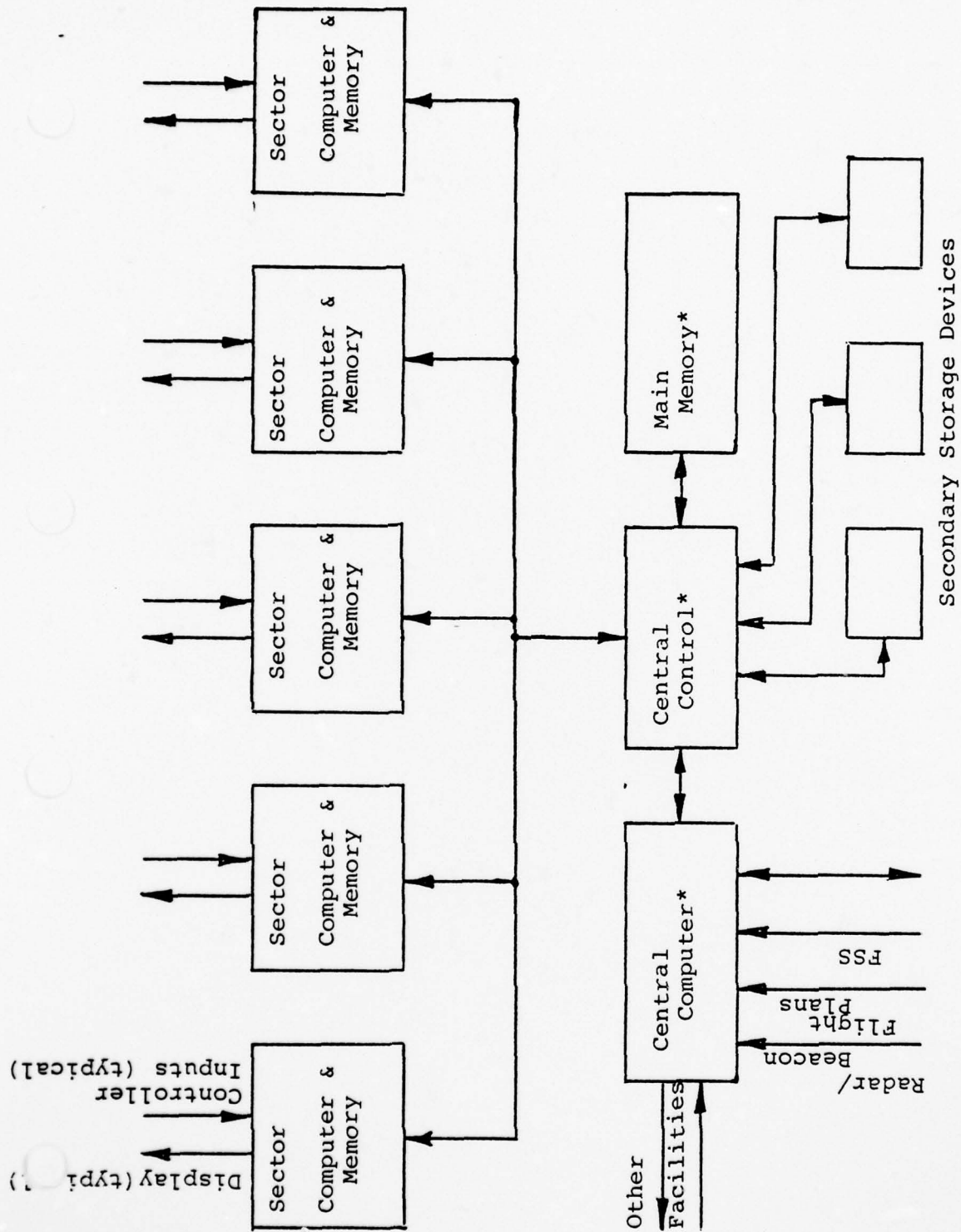
The operation of the parallel processors would be under the control of the central control unit, which itself may be a large microprocessor. Large here simply means that it would have a significantly larger memory capability than the other processors. Several different modes of operation would be possible. The memory

of the central control computer could retain all data and algorithms required by the other processors. The data and pertinent algorithms would be transferred to a specific processor as the need arises. All timing of the processing would be controlled by the central unit, as well as control of data transfers between other processors, if required. Built in redundancy is possible by supplying "spares" or selecting the size and speed of the processors suitably, to permit a single processor to perform more than one task if necessary. The forecasted cost figures indicate that using stand-by processors may prove to be sufficiently economical.

5. Modular Computer Networks

The modular design of computer systems can be extended to the en route system as well as the terminal system (See Figure 48). This could have an effect on program complexity (software) for operating the system. In particular it may simplify the maintenance of system software.

The logistics of maintaining software for the large main frame computers, as in the Central Computer (CC), is accomplished at cost levels which are at best undesirable. The software is strongly dependent on local-geometries, (i.e. location of VOR's defining the route structure) which vary from site to site or center to center. These geometrics require the development of specialized algorithms for conflict



*Duplicate Central, Computer, and Control unit also assumed.

FIGURE 48: MODULAR EN ROUTE SYSTEM

prediction, sequencing, etc. Each CC, therefore, has its own unique set of subroutines reflecting these differences in geometries.

By isolating these geometries within external microcomputers, which are interfaced to the CC, a modular, time-shared system is presented. Thus, it is intrinsically coupled to the external microcomputer. Now the microcomputer can, on a time-shared basis with others, interrogate the CC for 3-dimensional dynamic information, position, altitude and velocities; then generate control commands and decisions. This approach can result in a more or less semi-static or "standardized" software package for the CC and shift the dynamics of software changes to isolated units. This approach also permits operating on the basic data and "driving" the display totally independent of the CC algorithms. Thus specialized geometries and algorithms for handling these geometries as well as methods of display are isolated from the CC functions.

6. Terminal Operations

Present plans call for the use of trilateration methods for determining aircraft positions while on the ground. The positions and identities of the aircraft would be displayed to the ground controller on a planned view display. The system is the Tower Automated Ground Surveillance System (TAGS) and functionally it is similar to the ARTS-3 concept. Since the aircraft all are on the surface and usually move

along well defined taxiways and runways, the control problem is significantly less complicated than the one in ARTS-3.

The computer would derive position and identity, generate tracks and update the displays for the controller. The controller through the use of digitized voice messages could issue taxi clearances to the aircraft. By using a "finger-touch" type display the controller could select the aircraft which is to receive a message through the data-link. By restricting controller-pilot man to man voice transmissions, to handle non-standard or low priority procedures, a significant decrease in controller work load would be expected.

The TAGS computer could also handle issuance of clearances. When the flight crew signals it is ready to copy, the computer could transmit the clearance, which it has received from the center, over the data-link. The aircraft would receive the message in hard copy by the use of a printer or on a magnetic cassette or disk for play back.

An additional function of the TAGS computer would be the control of signals at intersections of taxiways and runways. These signals would be visible to the flight crews and give them updated taxi clearances. The automatic intersection control system (AIC) is another planned enhancement of the ASTC system.

B. Airside

In order to present applications of on-board microcomputers, particularly in the areas affecting the interaction of the aircraft with the total system, it is necessary to present a "scenario" of the system and its users in the time frame 1980 to 2000.

The user classes for this time period have been defined in a report by the Federal Aviation Administration (FAA). [13] The FAA report specifies the characteristics of the users by different classes; including fleet mixes, operational characteristics and avionics capabilities. There are 6 basic user classes. These classes represent levels of capability of the avionics that the future fleet may be expected to install and use. It is expected that different users would carry avionics of different quality, redundancy, and degree of sophistication, based on cost and level of service they choose and the airspace category in which they fly. The FAA defined classes and their avionics capabilities are presented in Table 21.

In addition the FAA report specifies four airspace categories which are assumed to be representative of the classification of airspace in which users would fly:

1) High Density Positive Controlled Airspace

This requires sophisticated 4D-RNAV navigation, surveillance and communication equipment including microwave landing system equipment.

TABLE 21: TYPICAL AVIONICS COMPLEMENTS BY USER CLASS

Class	Avionics
A	Dual High Quality DABS Transponders Dual High Quality Encoding Altimeters Dual High Quality IPC/ATC Data Link Logic and Displays Dual 4D-RNAV Navigation Equipment Dual High Quality Microwave Landing System Equipment Dual AEROSAT Avionics (Optional) Dual Voice Communications Equipment
B	Dual High Quality DABS Transponders Dual High Quality Encoding Altimeters Dual IPC/ATC Logic and Displays Dual Voice Communication Dual 3D-RNAV Navigation Equipment Dual Microwave Landing System Equipment Dual AEROSAT Avionics (Optional)
C	DABS Transponder Encoding Altimeter IPC/ATC Logic and Displays 2D-RNAV Navigation Equipment Microwave Landing System Equipment Dual VOR Navigation Equipment Dual Voice Communications Equipment
D	DABS Transponder Encoding Altimeter IPC Logic and Displays Dual VOR Navigation Receivers Dual Voice Communications Equipment
E	DABS Transponder Encoding Altimeter IPC Logic and Display Voice Communications Equipment VOR Navigation Receiver
F	Voice Communications Equipment VOR Navigation Receiver

2) Positive Controlled Airspace

Requires a similar set of equipment with only a 3D-RNAV Navigation System.

3) Mixed Airspace

Requires transponder, communications and simpler (2D-RNAV) navigation equipment, as well as, some form of intermittent positive control equipment.

4) Uncontrolled Airspace

Requires no specific equipment.

With these "scenarios" as background the description of expected on-board instrumentation, microprocessor and microcomputers will be given. When appropriate, the user class to which the described on-board system will apply will be indicated.

1. On-Board Avionics Displays

The microprocessor and microcomputer within a total avionics/display package will be utilized in two different functional modes. The first of these is as a dedicated device, while the second, is as a general purpose device. An example of dedicated computers are the navigation computers. These will permit some flexibility in input; however, for the most part, they will be designed to accept data from specific on-board navigation devices as well as key-boards. The software will be contained in a read-only-memory (ROM) and very little actual programming will be possible. The general purpose computer will,

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THE IMPACT OF MICROCOMPUTERS ON AVIATION: A TECHNOLOGY FORECAST--ETC(U)

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however, permit programming in the will be accomplished by inputting magnetic cassettes or disk packs. will give a microcomputer a wide 1 applications.

7

Examples of such functional integr computers within the aircraft environ Table 22.

A wide variety of avionics subsystems are available, permitting modular assemblies at a wide cost latitude as well as a wide variety of microprocessors of considerable breadth of power and various display subsystems at a significant level of computing power at costs which would be acceptable for Classes C & D. For example the computer which is shown in Section IB which was costed at \$100,000. A specific application, which would be of interest to users in Classes A through D is the TSD display (TSD) concept. Such a system requires the existence of a data-link. The display which exists within the cockpit is not a new concept. As early as 1946, investigations of TSD display methods were carried out [1]. The FAA conducted simulations using a cockpit simulator. These investigations declared that the information could be obtained by using the information from the displays. However, because of

TABLE 22: FUNCTIONAL INTEGRATION OF MICROCOMPUTER

- I. Flight Monitor Computer
 - Altitude Alert
 - Engine Warnings
 - ILS Deviation
 - Over Rotation
 - Landing Gear
 - Max/Min Speed
 - Windshear Warning
 - Ground Proximity
 - Failure Warning
 - Maintenance Fault Isolation
- II. Flight Control Computer
 - Attitude Hold
 - Auto-land/Rollout
 - Go Around
 - Control Wheel Steering
 - Take-Off
 - Auto-Throttle
 - Flight Director
 - Failure Warning
 - Maintenance Fault Isolation
- III. Flight Management Computer
 - Auto-Tune Nav aids
 - Flight Plan
 - Map Data

TABLE 22: (CONTINUED)

Navigation

- . Mode & Select Sensor
- . Lateral & Vertical
- . 4-Dimensional

Performance

- . Fuel Management
- . Speed Control
- . Vehicle Configuration Control (Actual Control)
- . Optimum Profile

Failure Warning

Maintenance Fault Isolation

Note:

Because of the implied sophistication of the above examples they would normally be limited to users in Classes A and B.

the displays, the attention span required of flight crews was too high. These initial efforts lacked the ability to provide the essential information about the traffic in an easily interpreted format. However, microcomputer driven displays, such as a CRT or a GPD can overcome this previous drawback. The digital computer will permit symbolic presentation of relevant traffic information in a self centered "heading-up" display.

The total TSD package would require a data-link (up-link is a minimum requirement), CRT or GPD display and a microcomputer. For example, in an ARTS-3 environment when an aircraft is assigned a particular sequence number, digitized data via the data-link would specify the relative positions of other aircraft in the vicinity. The aircraft which is scheduled to land just prior to the subject aircraft would be indicated on the display. The microcomputer would utilize this information as well as input from directional gyros and present a pictorial presentation of present separation. A number of experiments to determine the type of information required to increase capacity and safety would be necessary. For example, one possibility is to only display the aircraft which is sequenced immediately prior to the subject aircraft using the TSD Approaches to closely-spaced parallel runways could be

monitored and recognition of a "blunder" would be significantly improved. The application of this concept, could lead to reduced controller workload since fewer, if any, radar vectors would have to be given. In addition, the crew of the subject aircraft could predict that a violation of minimum separation standards is imminent and take corrective measures. This monitoring capability by the crew could lead to acceptance of a reduction of separation standards in high density areas for suitably equipped aircraft. This would clearly lead to closer spacing at the runway threshold and increase runway capacities. Another important effect of the TSD would be increased assurance to the pilot that a safe and logical sequence of events is occurring. This increase in assurance would enhance acceptance of automated control concepts.

2. Standardization

Some degree of standardization for pin connectors, resolvers and signal levels will be practiced by vendors. This standardization will also apply to other avionics packages. For example, the output of a navigational receiver or DME will be digital rather than analog and be available through a standard pin connector. These signals will be sampled by input to a microcomputer, where processing takes place and output to displays is generated.

Airframe manufacturers will incorporate wire bundles

and data busses with standard connectors. Just as today, certain optional packages will be available to a buyer and installed by the airframe manufacturer. The motivation for this will be provided by the market conditions.

Instrument panels will undergo a significant change reacting to the digital processing versatility and capability. At first, present day electro-mechanical (dial or needle movement output) will have additional digitized output capabilities. This will permit sampling these outputs under control of a microcomputer. These digitized outputs will be implemented through the use of solid state converters and built in microprocessors in the instruments. Normal evolution will lead to elimination of the moving dial and needle indicators and only electronic display methods will be used. Instruments whose output is required infrequently, will no longer physically appear. Transducer outputs will be sampled in a controlled loop by a microcomputer, which will provide outputs to electronic displays on a time-shared basis. Through software, the display information will be controlled by flight crews on demand. This will permit analysis of the various aircraft systems such as power plants, fuel flow and electrical systems and actuating visual alarms in the form of enunciator panels.

This is the environment which can be expected in the

aviation industry of about 1990 to 1995. This forecasted environment is far from being "highly speculative." As pointed out, a period of 18 years (1977-1995) represents one-fourth of the entire history of powered flight, this same period of 18 years represents about one-half of the history of commercial aviation. Considering the "state of the art" in avionics between 1935 and the present 1977, one can linearly extrapolate and arrive at the above described environment. In fact, the appearance of the micro-computer represents a significant "breakthrough." As such, it introduces an inflection point in the trend curves and linear extrapolation may prove to be somewhat conservative.

3. Active Control Technology (ACT)

Recent experiments using active control techniques (ACT) of aircraft geometry and control systems, have indicated that a number of functions can be identified which could improve aircraft performance and increase safety, by decreasing structural stresses on the airframe.

Some of these functions are;

- a) augmented stability control
- b) gust load alleviation
- c) maneuver load control
- d) ride control
- e) flutter mode control.

New aircraft designs, especially energy conservative configurations, which would normally have high aspect ratios, will experience great benefits from ACT. This is because the "slender wings" experience critical flexing and hence could experience structurally excessive loads due to gusts and overcontrol.

The trend, at present, is in the direction of using digitized techniques to control airfoils and other control surface movement and appears to indicate that this will tend to advance the "state-of-the-art." The forecasted microcomputer memory capacities and cycle speeds will be more than adequate in accomodating the present changing requirements in ACT. It is expected that the application of microcomputers and microprocessors will reduce costs below those using analog circuitry.

4. Engine Control Units

The use of engine control units, utilizing digital methods are beginning to undergo increased development. Flight tests on the Concorde have resulted in successful control of fuel flow and jet efflux nozzles. These units were designed to handle all parameters essential to power plant management such as; variable intake geometry, afterburning and noise abatement. Another important capability of these digital control systems is the presence of a memory module to record engine performance. Upon landing, the unit can be

interrogated to provide data for future service requirements.

IV. Implications

A. Landside

One of the most significant results of the forecast is the expected large reduction in costs for computing systems using large scale integration (LSI) technology. This indicates that increased cost benefits can be realized by replacing manpower needs by additional automation with the use of digital computers.

It will be possible to obtain levels of reliability, which of necessity must be high, by the use of redundant hardware components. For example, rather than relying on a single large main frame computer to perform the en route functions a modularized system could be considered. A single control unit (with a standby) would be connected to a set of microcomputers. These microcomputers would each have sufficient memory capacity to perform their designated functions, as well as upon command by the central control unit, be capable of taking over for another module which is malfunctioning. The system would also contain a large central memory, which could be accessed by the individual modules through the central control unit. This central memory would contain copies of all programs used by individual modules as well as a global data base. When a malfunctioning module is sensed, the control unit would select another module and initiate a transfer of required programs from

the central memory to the module for execution.

Such a system would have a simple "add-on" growth capability. As traffic densities increase or airspace geometry is changed by redefining sector boundaries for example, new modules could be added with the requisite software.

In order to fully realize the benefits of automation, to the fullest degree and at the earliest possible time, a number of studies and experiments will be required. This form of testing of hypotheses should even take place before "off-the-shelf" hardware is available. This is true because of a built in delay which normally can cover a span of 8 to 10 years before implementation.

B. Airside

Similar reductions in costs, power requirements weight and size apply also to airborne systems. Therefore a large amount of computing power should be available to a significant portion of the general aviation Classes C and D.

One of the specific applications discussed in Section III was the use of traffic situation displays (TSD). It was pointed out that with a sufficient amount of computing power and a suitable display the surrounding relevant traffic situation can be presented to the crew. This may pave the way for some decentralization of the control concept. For example, the pilot could predict future conflicts and select the best course of action to maintain

safe separation as well as make good a specific scheduled time at the runway threshold. This could prove to be beneficial in terminal areas as well as in the en route area. Suitably equipped aircraft would not require a large amount of speed and directional control information transmitted from the ground but would be able to "lock on" the aircraft sequenced to land first and the following aircraft would maintain a safe distance without additional commands.

Whether or not users will acquire large amounts of hardware is, of course, dependent on the benefits that such hardware acquisitions will imply. Therefore the "total system" must provide certain benefits such as reduced delays, fuel conservation and an increase in safety to equipped aircraft.

V. Conclusions

- A. The large cost reductions expected will generate additional cost benefits for automating control functions.
- B. System reliability through hardware redundancy should prove cost beneficial.
- C. Expected advance in "smart terminals" will benefit the modernized flight service station by permitting direct access to the data base.
- D. The development of modular systems versus large central main frame systems will be feasible.
- E. Increased on-board computing capability at acceptable costs to users will permit decentralized control of aircraft.

- F. Remote monitoring of ground-based equipment will result in a centralized maintenance system.
- G. Concept testing should be carried out through studies well prior to the availability of specific hardware packages.

GLOSSARY OF TECHNICAL TERMS

Anisotropic etching - the use of chemical etchants whose etch rate is a pronounced function of crystallographic orientation of the substrate material to produce specialized geometrical structures. In silicon, potassium hydroxide removes material 100 times faster in the $\langle 100 \rangle$ direction than in the $\langle 111 \rangle$ direction.

Avalanche-induced tunneling - In a p-n junction under high reverse voltages, carriers traversing the depletion layer receive enough energy to create additional carriers, e.g., electrons, via collisions with the crystal lattice. This carrier multiplication can lead to high reverse currents (avalanche breakdown). Carriers can also gain sufficient energy to tunnel through a thin surface oxide, a phenomenon used to some read-mostly memory structures as a means for inducing charge on a floating silicon gate electrode to write information into the memory.

Base Transit Time - In a bipolar transistor, the time required for electrons to traverse the base region, from emitter to collector.

Bipolar transistor - a structure in which both negatively-charged electrons and positively-charged holes (absence of a valence electron) are important in the conduction process and in which typically a relatively small amount of current injected into the base controls the flow of a larger current between the emitter and collector terminals. Such transistor structures function either as amplifying or as switching elements, depending on the applied current level.

Birefringence - doubl. bending of light by crystalline materials (double refraction)

Bootstrapping - using some already running part of a language processor as a tool to get the rest of it running more easily (or using such a processor to get itself running on another machine without rewriting it). These shortcuts are possible when the translator can be written using only a small but well-defined subset of the language it translates; when it has this property, only so much of it as is necessary to translate that subset need be hand coded, after which the description of the whole translator can be processed by the handwritten fragment. The output of this procedure is the whole translator in object form, "bootstrapped" into existence by the handwritten fragment of itself. "Bootstrapping" is used to describe the process whereby a programmed loader, whose job it is to load other pieces of software into a machine, gets itself in.

Cache memory - a small high-speed memory for the temporary storage of information, usually used between a slower large memory and a fast central processing unit.

Charge transport - movement of electrical charge from one point to another, either via an applied electric field or via diffusion.

Correctness proofs - are accomplished by automated verification systems which allow the analyst to prove the correctness of small programs by means similar to those used in proving mathematical theorems. Axioms and theorems derived are used to establish the validity of program assertions and to provide a fundamental understanding of how the program operates.

Cross-assembler - is a computer program that accepts symbolic instruction mnemonics for a selected target computer and generates target-computer machine code while operating on another computer. It allows a code written for a micro-computer to be assembled on a larger computer with additional convenience features.

Data structure - is characterized by labeled-directed graphs that allow operators on data objects having the given structure to be naturally and simply defined by means of graph transformation rules. Some examples are arrays, lists, trees, stacks and queues. Data structures capture the notion of computational structure at a level that is sufficiently abstract to emphasize logical relations among components of a data object, independently of details of implementation but at the same time sufficiently concrete to preserve some relation between a structure and its computational realization.

Depletion layer - the region surrounding a p-n junction which is depleted of mobile charge as a consequence of equilibrium between drift and diffusion currents there. The depletion layer thickness, across which applied voltage is dropped, expands under reverse applied bias and decreases under forward bias.

Design language processor - aids in the development of an understandable representation of the software design as that design evolves. The processor helps in constructing and expanding software in a hierarchical fashion, with documentation of each decision contributing to the design. A top-down design methodology is encouraged.

Dielectric constant - the proportionality constant relating the coulombic force between charged particles in a material to their separation. The permittivity of the material.

Diffusion - a high temperature process by which impurity atoms which have been deposited on the surface of a material (e.g., a silicon wafer) have sufficient thermal energy to penetrate the material seeking to equalize their densities displacing the host atoms, and altering the electrical properties of

the material in desired ways. Normal diffusion temperatures are between 900°C and 1200°C for the most frequently-used impurities in silicon.

Dopants - impurities which are selectively introduced into the substrate material to modify its electrical properties in specific regions. Examples are boron and phosphorous in silicon.

Double dielectric structure - a structure employing two successive layers of materials having different dielectric properties. Charge induced at the interface between the materials can be stored nearly indefinitely, resulting in a non-volatile, read-only semiconductor memory.

Edge drop out - circuits fitting partially, but not completely, on the circular silicon wafer and thereby rendered defective.

Electromigration - Atomic migration induced by the presence of internal electric fields in the material.

Emulation - uses programming techniques and special machine features to permit a computing system to execute programs written for another system. Through emulation of existing systems on new microprocessor-based systems, the cost of rewriting software can be avoided, and the overall system cost greatly reduced. The microprocessor in the IBM 5100 emulates a medium-sized IBM 370 so that the APL and BASIC language processors did not have to be rewritten for the new machine.

Epitaxy - a process in which silicon atoms are deposited on a polished silicon wafer surface, increasing the wafer thickness. By introducing controlled amounts of specific impurities into the epitaxial film as it is grown, its properties can be electrically different from those of the starting substrate and can be adjusted to achieve best device performance. The epitaxial film, crystallographically, represents a natural extension of the substrate materials.

Extensible language processor - is a computer program that allows users to define new language features. Working with a base language and definition facilities, the user can create new notations, data structures, operations, and even new control structures.

Fault tolerance - is the capability of the system to perform its functions in accordance with design specifications, even in the presence of hardware or software failures. If, in the event of faults, the system functions can be performed, but do not meet the design specifications with respect to the time required to complete the job or the storage capacity required for the job, then the system is said to be partially

or quasi fault-tolerant. Fault tolerance is provided by the application of protective reliability. These resources may consist of more hardware, software, or time, or a combination of all three.

Firmware - is an aspect of a computer system that is neither fully hardware nor software. An example of firmware is a microprogram, which directly controls the sequencing of computer circuits at the detailed level of the single instruction. Firmware provides economy of circuitry if the machine must have complex instructions. Further, it is possible to emulate another machine through a set of microprograms.

Flip-flop - a bistable circuit consisting of two transistors which is frequently used as a memory element.

Gate area - the area consumed by the circuit elements making up a single logic gate. A typical 4-input gate would require at least 5 transistors.

General-purpose languages - do not exist in the sense of absolute applicability, to all programming situations nor does there exist a clear and separate category of languages called application-oriented. All languages are application-oriented, but some are for larger or smaller application areas than others. However, the term "general purpose" is sometimes used in a variety of areas e.g., report generation and list processing as well as computation.

Hard contact printing - contact printing in which the mask is pressed against the substrate with appreciable force.

Ion Implantation - a process for the controlled introduction of specific atoms (impurities) into the semiconductor (silicon) lattice in which the impurity atoms are ionized, accelerated to a high velocity, and allowed to impact the surface where their introduction is desired. Penetration distances (doping depths) are shallow and depend on the impurity type and accelerating potential. Implantation can be selectively masked by retaining a glass, metal, or polymer film over portions of the wafer by photoengraving.

Junction isolation - a process by which individual circuit elements in an integrated circuit are electrically isolated from each other, to be later interconnected in desired ways by printed metallization. Typically, circuit elements are realized in n-type semiconductor regions which are surrounded by p-type regions. The resulting p-n junction (a reverse-biased diode) electrically isolates the circuit elements from the substrate and from each other.

Junction reverse leakage - the leakage current in a p-n junction (diode) which is reverse biased. Such currents are typically due to the thermal generation of electrons and holes in the vicinity of the junction.

K-mil² - abbreviation for thousand square mils, i.e., K-mil² = ten thousand square mils (1 sq. mil = .001 sq. inch)

Luminance Noise - fluctuation in luminance intensity between elements in a display for a fixed input level.

Magnetic bubbles - circular magnetic domains having a magnetization opposite from that of the substrate and which can be shifted about in the substrate material under the inductive influence of surface control electrodes. Under suitable polarized light, the domains are observable as small circular areas or "bubbles".

Mask steps - the steps in which a mask is used to transfer a desired pattern onto the substrate surface via a photoengraving or lithographic operation. A contact print using an opaque-and-clear glass mask on an oxidized, photoresist-coated silicon wafer is an example.

Merged device structure - a device structure in which one material region functions electrically as part of more than one device, reducing the area required for implementation of the circuit function.

Metal migration - physical atomic displacement of metal as when under the influence of an electric field. See electromigration.

Microcomputer - a computer, consisting of a microprocessor and associated memory, which is fabricated as (typically) a single monolithic circuit using batch production techniques.

Microprocessor - an electric system, integrated as one or a few monolithic circuits, and containing the necessary circuitry to allow for the sequencing, recognition, and execution of a variety of externally addressable instructions.

Modular programming - produces relatively small, easily interchanged, computer routines which meet standardized interface requirements. Modularity is accomplished by breaking the program into limited segments which perform complete functions and are therefore completely understandable in themselves. This technique greatly facilitates development and verification of complex programs and systems.

Monolithic circuit - a circuit formed in a single piece of the substrate material as opposed to a hybrid circuit, in which individual (physically separate) circuit components are electrically interconnected to form the final circuit.

MOS Transistor - a metal-oxide-semiconductor structure in which the application of a potential across a thin dielectric layer (oxide) on the surface of a semiconductor (between a metal gate and the substrate) regulates the flow of current between source and drain regions in the substrate. A structure in which an applied electric field at the surface controls the flow of current along the surface, perpendicular to the applied field.

Noise immunity - the ability of a circuit to ignore noise in the form of extraneous voltage transients which are introduced from external elements.

Peripheral processors - are system components, each having their own memory, although they may share some arithmetic circuitry among themselves. The CDC 6600, which has been described as a "network computer" with a CPU and 10 peripheral processors, is programmed as an eleven-way multiprocessor. Since I/O and operating systems functions may be performed concurrently with user programs, very little of the central processor time is taken up with operating-system overhead.

Photoresist - a photosensitive polymer which changes its solubility in a developer when exposed to radiation of a given wavelength. Typical photoresists become insoluble in xylene-based developers when exposed to ultraviolet light. Photoresists are applied in thin layers less than one micron thick and allow submicron dimensional control.

Piezoelectric effect - change in the output voltage of a material when pressure is applied.

Piezoresistive effect - change in the resistance of a material when pressure is applied.

Piezojunction effect - change in the current-voltage characteristics of a material when pressure is applied.

Planar process - the basic process for monolithic integrated circuits, in which circuit components are formed and interconnected using photoengraving and thin film deposition on a flat, polished wafer, usually silicon. The minimal amount of disturbance to the flatness of the wafer surface and hence the formation of the entire circuit in the flat plane of the wafer, led to the term 'planar' to describe the process.

Problem-oriented languages - are generally considered to be those oriented to specific applications or other special purposes. Their uses range from numerical control programming to information retrieval systems.

Procedure-oriented languages - are ones in which the user specifies a set of executable operations that are to be performed in sequence and which specify a procedure. The key

element is that the operations are definitely executable, and the sequencing has to be specified by the user. Fortran, Cobol, and P/l are examples; RPG is not considered a procedure-oriented language.

RC time constant - a time constant (response time) given by the product of a resistance (R) and capacitance (C) and often determining the speed of a device or circuit.

Stacking faults - disruptions in the normal periodicity of a single-crystal lattice structure in which one atomic layer fails to align (stack) on the layer beneath, creating a local defect which may propagate through many successive layers.

Structured programming - is concerned with improving the programming process through better organization of programs and better programming notation to facilitate correct and clear descriptions of data and control structures. The physical structure of a well-organized program corresponds to the sequence of steps in the algorithm being implemented. Good languages for structured programming must have a carefully thought out assortment of control structures and data-structure definition facilities. Good practices lead to reduced cost of program modification and maintenance as well as original development.

Threshold voltage - in an MOS transistor, the gate-to-source voltage required to establish conduction between the source and drain terminals.

Voltage transients - voltage excursions, typically of short duration and possibly of high amplitude, which are generated by or induced in a circuit and which are not necessarily part of its normal operating characteristic.

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