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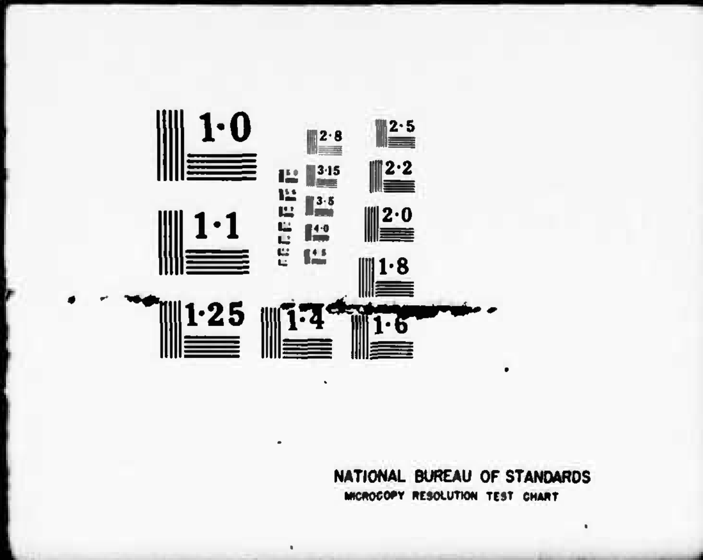

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SHORT CHANNEL MOS FOR CCD READOUT CIRCUIT

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3011 Malibu Canyon Road
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Wafer processing techniques have been developed to allow fabricating an n-MOS clamp-sample-and-hold (CSH) circuit suitable for detecting outputs from charge couple device shift registers operating at 25 MHz. The techniques developed include methods to define circa 1 μm (micrometers) device features using electron beam lithography as well as the methods of wafer processing to make functional MOSFET devices at these dimensions. In addition, the CSH circuit was designed and thoroughly simulated with computer models.

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The development work required determining techniques to etch fine structures in thin films of silicon nitride and polycrystalline silicon. Data were also obtained of the amount of underoxidation when a silicon wafer is oxidized using silicon nitride masking features. Methods were also developed to provide 400 Å gate oxides, shallow n^+p junctions, and reliable contacts to these junctions without metallization spiking.

Several diagnostic chips were designed and fabricated. Experience with these provided a list of design rules for the fabrication, in general, of circuits using the high resolution nitride masked oxidation process. It also provided a list of device performance parameters.

CONTENTS

SECTION		PAGE
1	OBJECTIVE AND PRINCIPAL RESULTS	1
2	OVERALL VIEW OF WAFER PROCESSING	5
3	LITHOGRAPHY DEVELOPMENTS	9
	A. Alignment Mark Studies	9
	B. Benchmark Protection	14
	C. One-Micrometer-Wide Patterns in Silicon Nitride	15
	D. Underoxidation of Silicon Nitride	18
	E. One-Micrometer-Wide Patterns in Polysilicon	23
	F. Design Rules for NIMOX Process	24
4	TEST CHIPS	27
5	WAFER PROCESSING	35
6	CIRCUIT DESIGN	43
7	CONCLUSIONS	55
	REFERENCES	59

Section
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ILLUSTRATIONS

FIGURE		PAGE
1	Registration with MOS compatible Ta benchmarks	10
2	Contrast enhancement from a Ta gap	11
3	The liftoff method	12
4	Percentage contrast improvement as a function of benchmark gap width	14
5	SEM photomicrograph of oxidized silicon wafer after removing nitride mask	16
6	Nitride feature etched with CF_4 plasma using aluminum contact mask	17
7	Edge view of oxidized silicon wafer after cleaving through nitride feature	19
8	Edge view of oxidized silicon wafer after cleaving through 0.9-μm-wide nitride feature	20
9	Underoxidation parameters versus pad oxide thickness	21
10	Polysilicon transistor gates etched with CF_4 plasma and using aluminum masks	24
11	Diagnostic chip N42	28
12	Diagnostic chip N41	29
13	Diagnostic chip N44	30
14	IV characteristics of n-channel MOSFET made with electron beam lithography	31
15	Results from testing implant continuity	32
16	IV characteristics of field oxide transistor	33
17	Calculated doping profiles for NIMOX process	36
18	Comparison of diode characteristics from O_2 versus N_2 implant anneal	37

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ILLUSTRATIONS (Continued)

FIGURE		PAGE
19	Reversed bias IV character with respect to substrate of spike test diode and source drain	39
20a	CV curve for NIMOX process wafer, n^+ polysilicon gate	40
20b	CV curve for gate oxidation run monitor, n^+ polysilicon gate	41
21	CSH circuit configuration	45
22	Transfer characteristics of a source-follower stage for two values of threshold voltage	47
23	Source-follower output and drain current versus bias FET voltage	48
24	Output voltage swing ΔV_{out} for 5 V input versus V_{TO}	50
25	Linearity of CSH circuit for V_{TO} = -1.75 V	51
26	Input-output linearity of CSH circuit for V_{TO} = 0.5 V	51
27	Time sequence of voltages required to operate CSH circuit	52
28	Input-output waveforms of CSH circuit showing response to full bucket and empty bucket	52

SECTION 1

OBJECTIVE AND PRINCIPAL RESULTS

The objective of this program is to develop an n-MOS clamp-sample-and-hold (CSH) circuit suitable for detecting outputs from charge-coupled device (CCD) shift registers. This report summarizes the work of the first year, during which the device processing techniques were developed. The techniques developed include methods to define *circa* 1 μm device features using electron beam lithography, as well as the methods of wafer processing to make functional MOSFET devices at these dimensions. In addition, the CSH circuit was designed and thoroughly simulated with computer models. The second year of the program will be used to fabricate and test the the fast output CSH circuitry.

Two high-resolution lithographies had to be developed for this program — patterning thin films of silicon nitride and of polycrystalline silicon. This need resulted from an early decision to fabricate the devices with planar processing involving nitride features masking the field oxidation.[1] We refer to this as the nitride masked oxidation (NIMOX) method. The CSH circuit will require other lithographies, such as contact vias (in SiO_2) and interconnection patterns (in aluminum). However, patterning techniques for those structures were available from work on other programs.

There were three high-resolution lithography tasks. First, etching techniques had to be developed for the nitride and polysilicon thin films. We chose CF_4 plasma etching with aluminum contact masks. These aluminum masks were made by first exposing the pattern in the electron resist polymethyl methacrylate, evaporating aluminum, and then dissolving the resist (liftoff) which removes excess metal. Another task was to obtain linewidth data. Using these data the pattern written by the electron beam was then widened (or narrowed) to account for the mean value of over- (or under-) etching. In the case of the nitride patterns another source of linewidth narrowing is underoxidation, because when the wafer

is oxidized the oxide grows laterally beneath the nitride edges as well as into the silicon wafer. We found that the necessary linewidth corrections were a significant fraction of 1 μm features. In addition, a third task studied electron beam registration marks consisting of a gap in a heavy metal such as tantalum. Such features have greater signal contrast detecting backscattered electrons than bar-type features made of the same material.[2] We determined the contrast enhancement for Ta gaps.

For the high-resolution MOSFETs the vertical structure must be changed from the conventional one to have desirable device parameters. For example, to maintain threshold voltage the gate oxide thickness should be 400 to 600 Å rather than 1,000 Å. Also, the source/drain junction depth should be 0.1 to 0.3 μm rather than 1 to 2 μm.[3] For the source-to-drain punchthrough voltage to be greater than the drain voltage, the substrate doping must be raised to 10^{16} cm^{-3} from the conventional value 10^{15} cm^{-3}. The field oxide thickness can be slightly thinner, ∿7,000 Å rather than 1 μm.

These changes in vertical structure required several developments in wafer processing. We developed methods to grow the thin gate oxides while maintaining breakdown voltages at fields greater than 5×10^6 V/cm. We developed a self-aligned As ion-implantation process to form the shallow-junction source drains, and we determined the appropriate anneal conditions to make them with low leakage. We also devised a technique to contact the shallow junctions without the aluminum interconnection shorting through to the substrate. Another problem is to dope the polysilicon gates with phosphorus for low sheet resistivity without transporting any of the dopant across the thin gate oxide into the channel region. These changes in wafer processing were made while maintaining adequate margins for such parameters as junction breakdown voltage and field inversion voltage.

Also, during this year the CSH circuit was designed. A modified version of a circuit simulation program called XSPICE was used to test

different versions of the design. This work resulted in a basic layout of transistors, their W/L ratios, and the necessary capacitances. The simulation showed that with the reset transistor working at 100 MHz the output signal reached its final value within 30 nsec.

These results are discussed in detail in the remaining sections of this report. We present first an overall short version of the sequence of steps that comprise the wafer processing. Section III describes the lithography results and presents a table of design rules. The test chips that were devised and fabricated for this program are described in Section IV. The impact of these structures is most evident from the changes made in wafer processing which are explained in Section V. Typical device results are shown. In section VI the results of circuit simulation are presented.

SECTION 2

OVERALL VIEW OF WAFER PROCESSING

Several major topics are discussed in the remaining sections of this report. The relationships of these topics are evident from an understanding of the wafer processing. Table 1 lists the major processing steps that are suitable for making high-resolution circuits with n-channel MOSFETs.

Table 1. n-Channel MOSFET Processing

1. Grow a thin oxide (≡ pad oxide) and deposit silicon nitride film.
2. Define tantalum benchmarks (photolithography).
3. Protect benchmarks (photolithography).
4. Define nitride pattern (e-beam lithography).
5. Grow field oxide, strip nitride, grow gate oxide, and deposit polysilicon film.
6. Dope polysilicon with phosphorus and define polysilicon patterns (e-beam lithography).
7. Arsenic-ion implant source and drain, then anneal.
8. Deposit SiO_2 and define contact holes (e-beam or photolithography).
9. Deposit polysilicon and dope with phosphorus.
10. Aluminum metallization, aluminum etch (photolithography or e-beam lithography) and polysilicon etch.

Each of these steps is discussed below.

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Step 1. Notice the nitride is deposited on a pad oxide and not bare silicon. Without the intervening oxide, degradation of the silicon substrate occurs. The pad oxide thickness and the nitride thickness are critical parameters affecting both the amcunt of underoxidation and the lithography.

Step 2. A method is required for defining Ta benchmarks used by the electron beam machine for alignment. With previous work we learned that such benchmarks are compatible with making MOS devices. For this program we investigated gaps in Ta rather than bars. Such gaps enhance the registration signal.

Step 3. The Ta benchmarks are used to register all the e-beam patterns and therefore must survive practically all the wafer processing. This includes several high-temperature oxidations, diffusions, and anneals. Protection must also be provided from chemical attack when etching device features.

Step 4. A method had to be developed to etch the nitride pattern. Also, we had to find how much typical overetching occurs. If this dimension is known, then it can be added to the feature size at the layout stage.

Step 5. Growing the field oxide narrows any channels defined by the nitride. The amount of underoxidation must be determined and it also will be added to the feature size at the layout stage.

Step 6. Another high resolution lithography had to be developed to write 1 μm polysilicon lines.

Step 7. Arsenic was chosen rather than the conventional phosphorus to form the ion-implanted source drains. The As atom has a smaller diffusion coefficient in Si, thus, subsequent high-temperature processing is possible while maintaining shallow junctions.

Step 8. Conventional processing methods were used to define contact holes.

Step 9. This step was introduced because aluminum interconnections present a problem contacting shallow n^+ junctions. Excess aluminum

sintering can cause the metallization to penetrate the doped region creating substrate-to-metal shorts. Depositing 0.3 μm polysilicon at this stage gives an effective depth of 0.5 μm at the aluminum contacts while maintaining 0.2 μm junction depths at the channel edges.

Step 10. The aluminum patterns were etched using conventional methods. In turn, the aluminum pattern is an effective mask for removing the excess polysilicon with CF_4 plasma etching.

SECTION 3

LITHOGRAPHY DEVELOPMENTS

A. ALIGNMENT MARK STUDIES

For the electron beam pattern to be aligned to previous patterns, alignment marks are necessary. Generally, these are referred to as benchmarks. The principle of registration is depicted in Figure 1. First, the electron beam is directed to scan in x and y directions at three nonlinear positions on the wafer. A benchmark creates a signal as the beam sweeps its edge because of the change in the number of backscattered electrons. The positions of these edges are determined, and these data are used to calculate the necessary translation, rotation, and magnification corrections.

The key to accurate registration is to have benchmarks with a relatively high ratio of backscattered electrons with respect to the substrate. Previous work at Hughes Research Laboratories (HRL) had shown that benchmarks consisting of Ta bars provided high signal contrast and, moreover, were compatible with MOS device processing. No degradation of MOS properties is observed when benchmark passivation and protection are provided. However, even greater signal strength can be expected if one uses benchmarks consisting of Ta gaps rather than bars.

Shadowing is the basic mechanism that predicts an enhanced signal strength for gap benchmarks as depicted schematically in Figure 2. When an electron beam scans the tantalum edge at (A), backscattered electrons from the silicon substrate are counted at the detector. However, the contribution of electrons that backscatter from below the point (S) are decreased as a result of shadowing from the other Ta edge (B). Complete shadowing occurs below T for single-event backscattering. Consequently, the signal from the substrate should decrease compared to that from a simple edge, while the signal with the

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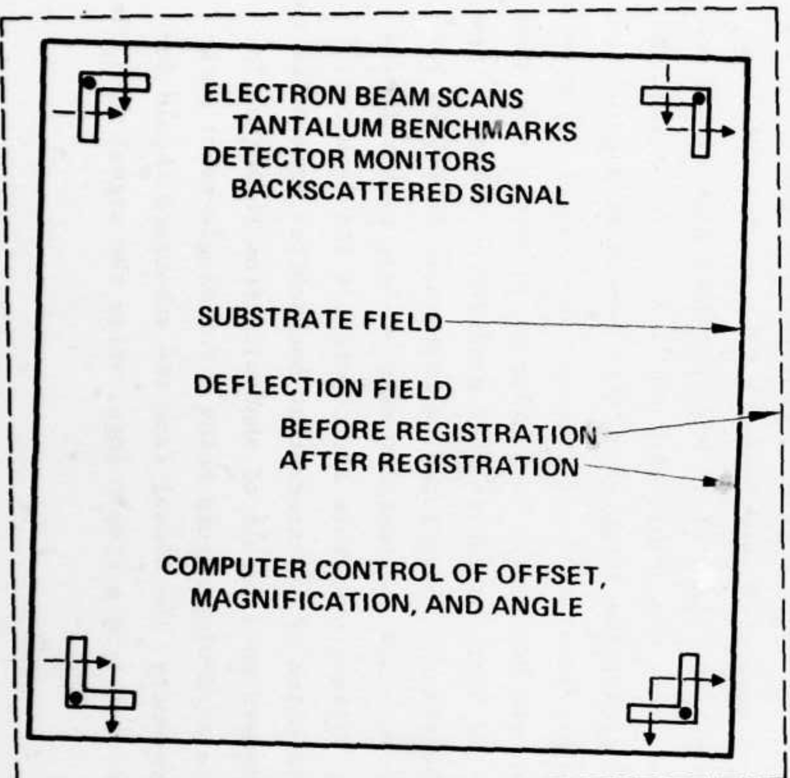

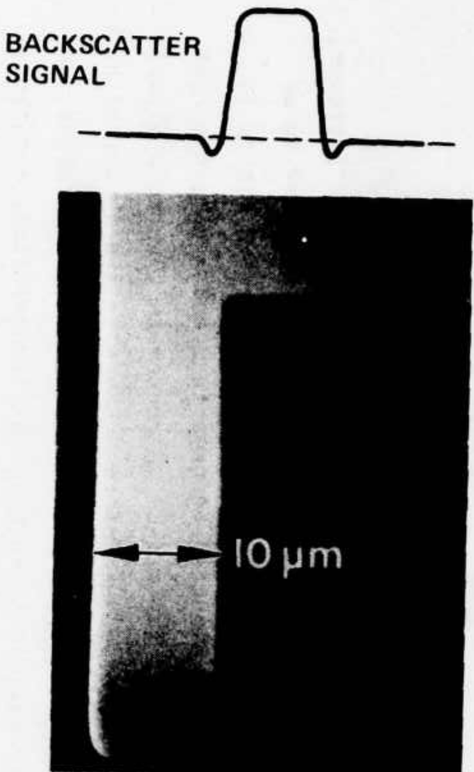

Ta BENCHMARK

EXCELLENT CONTRAST, S/N
EXCELLENT EDGE ACUITY
COMPATIBLE WITH MOS
±0.25 μm ACCURACY

Figure 1. Registration with MOS compatible Ta benchmarks.

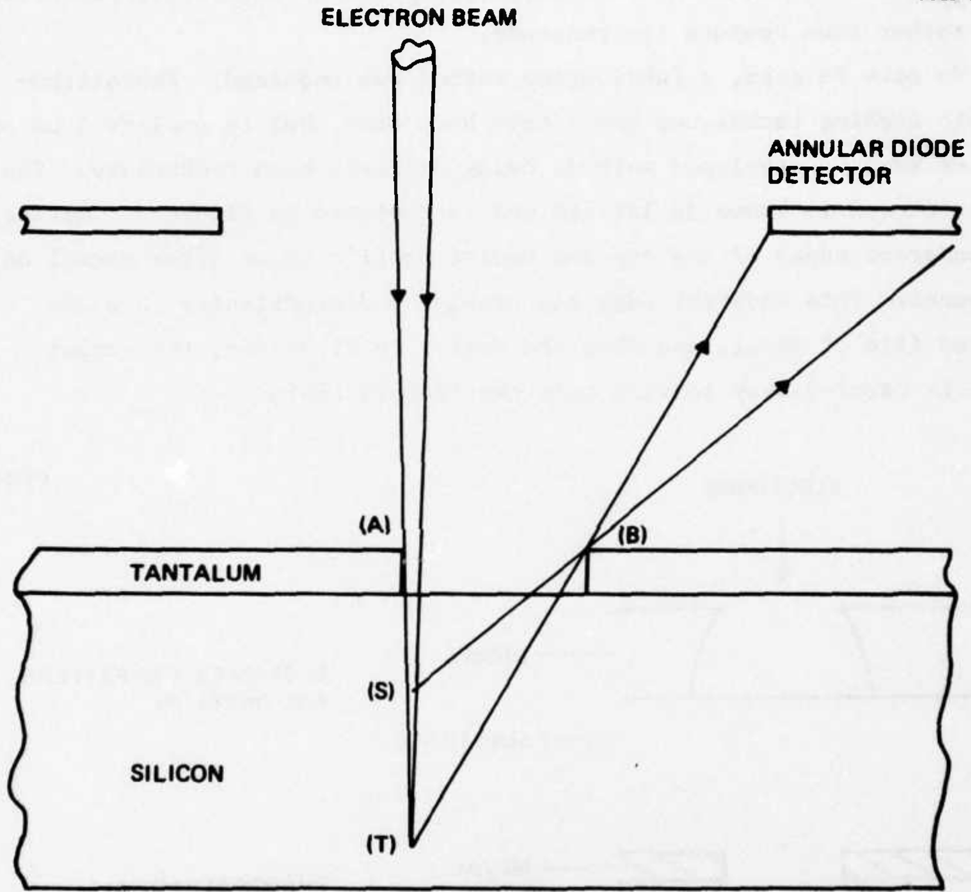

Figure 2. Contrast enhancement from a Ta gap.

beam just onto the Ta edge should remain unchanged. The corresponding increase in signal height should, in principle, allow faster and more accurate registration. Because of the complex and unknown distribution of backscattered electrons with depth, we chose to obtain experimental data rather than compute the response.

To make Ta gaps, a fabrication method was required. Photolithographic etching techniques could have been used, but to explore 1 μm or smaller gaps we developed methods using electron beam technology. The method chosen is known as liftoff and is depicted in Figure 3. Notice the undercut edges of the exposed resist profile shown after normal development. This undercut edge can provide a discontinuity in a deposited film of metal, and when the resist is dissolved, the excess metal is carried away leaving only the feature behind.

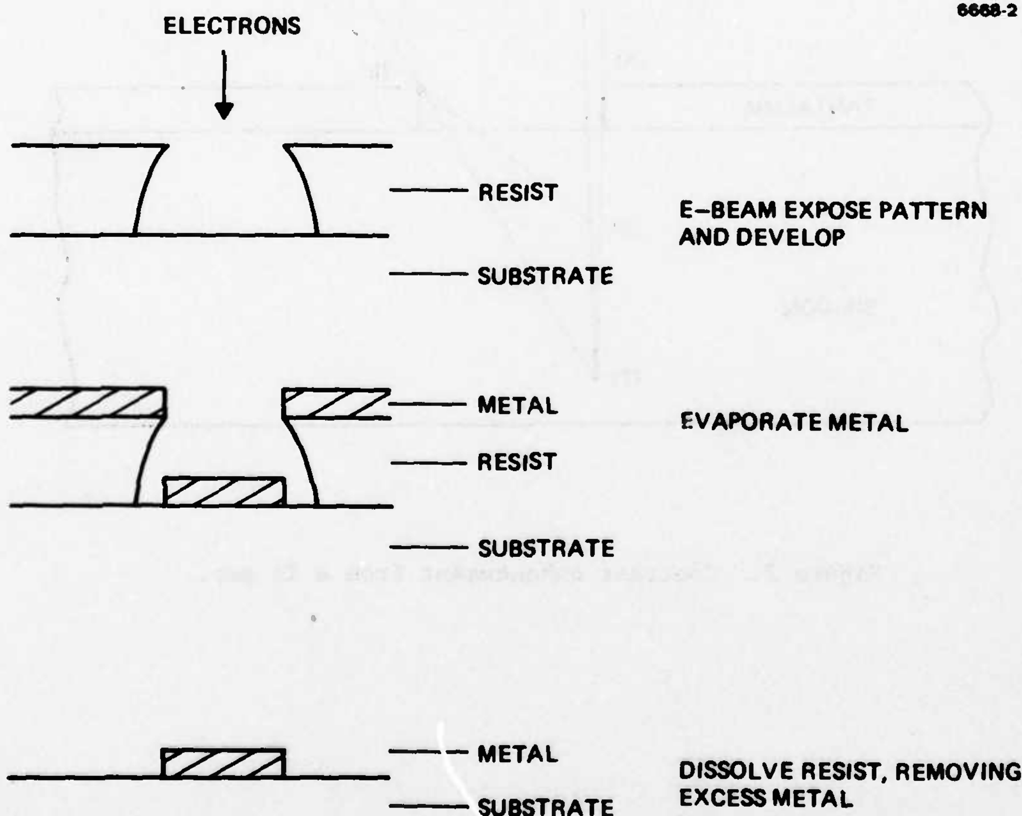

Figure 3. The liftoff method.

For control and ready availability we favor the use of rf sputtering for the Ta deposition. However, in a typical configuration the temperatures generated by this method are sufficient to soften the patterns in polymethyl methacrylate (PMMA). In fact, we did not get good liftoff from a polymer of PMMA that was partially cross-linked with anhydride groups, although separate studies had shown this cross-linked material was thermally robust up to 150°C. The best samples were made heat sinking the wafers to a water-cooled table. The Ta films are smooth and the metal lifts off directly with sharply defined edges. However, Ta bridging sometimes occurs, particularly for the very narrow gaps and the process was not judged reliable although it was sufficient to construct samples for obtaining the enhancement data.

The signal enhancement obtained with 30 keV electrons is shown in Figure 4 which plots the percent of contrast enhancement versus gap width. The insert figure depicts the actual signal found at the detector when scanning two slightly separated Ta bars. The signal heights relative to no detected electrons define edge and gap contrast. Therefore, the data plotted show how much better a gap is compared to a bar (which only has edge contrast).

Notice in the figure that beyond 3 μm there appears no effect. This number compares with the ∿4 μm backscatter distance or range of 30 keV electrons in silicon. As the gap dimension gets smaller, the corresponding value of I_g decreases. The smallest gap we measured (0.6 μm) gave the greatest enhancement. Here, the signal contrast was 46% greater than that detected from a single edge.

The signal enhancement from the 0.6 μm gap is good, but this improvement must be considered against the difficulty in processing submicron features. For the device fabrication portion of the program we used Ta bar features for benchmarks.

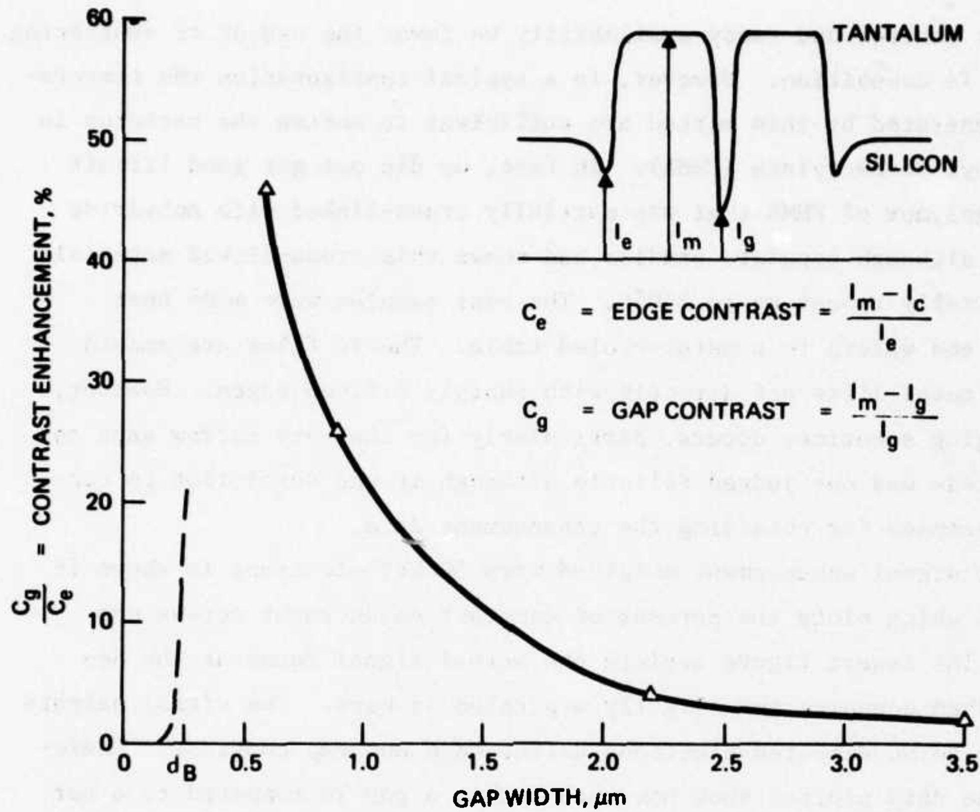

Figure 4. Percentage contrast improvement as a function of benchmark gap width.

B. BENCHMARK PROTECTION

Several processing steps could deteriorate or destroy Ta benchmarks. Volume changes caused by chemical reaction can form bubbles or blisters that destroy edges. Benchmarks can be accidentally removed as a result of etching or undercutting. Moreover, since we use a single set of marks to register all the electron beam levels, marks must survive practically all the wafer processing.

The four major processes that could destroy benchmarks are (1) silicon interdiffusion, (2) corrosion from oxidation growing in field oxide, (3) corrosion from phosphorus doping the polysilicon, and (4) etching during removal of polysilicon or nitride.

The scheme determined to provide protection from all of these was to form the benchmarks on the Si_3N_4 layer and then to cover them with 5,000 Å of deposited SiO_2. This method requires another mask step, which we term the benchguard. This benchguard pattern leaves a square of oxide covering the benchmark area with the Ta underneath and in the middle of the pattern.

With the NIMOX process, after patterning the nitride and oxidizing the wafer there is a thin film of oxide on the nitride (step 5, Table 1). This oxide must be removed with a light etch. However, this etch can also remove the oxide that is covering the benchmark. As a precaution we re-expose the benchguard pattern for this etch. Several wafer lots have shown the benchmark protection schemes to be reproducible.

C. ONE-MICROMETER-WIDE PATTERNS IN SILICON NITRIDE

We developed a technique for etching 1-μm-wide lines in silicon-nitride thin films using plasma etching with aluminum contact masks. In turn, the aluminum contact masks were formed using the liftoff technique described in the previous section. Here, we used either filament evaporation or e-gun evaporation with success. The best liftoff is obtained with the evaporation at normal incidence.

In our work the plasma etcher was a tubular type (LFE Corporation) and the gas was 96% CF_4 and 4% O_2. A perforated aluminum shield was used to separate energetic ions from the wafers. With this configuration the etch rate of Si_3N_4 is 500 Å/min.

Determining the etch endpoint of nitride etching is important since too great overetching will cause loss of linewidth control. The technique we favor is to examine the wafer for the color of the underlying SiO_2 film. This has the practical effect of limiting the minimum thickness of this oxide since films less than 500 Å are transparent.

Quite narrow gaps and lines are possible with this method using an aluminum contact mask and plasma etch. Figure 5 shows a photomicrograph of a wafer after patterning the nitride, 5,000 Å wafer oxidation, and removing the nitride. As evident from the liftoff figure (Figure 3), it is more difficult to leave fine gaps rather than lines in the aluminum mask. Yet the features in Figure 5 show submicron gaps were etched in the nitride film, i.e., the aluminum was left in the regions where there was no oxide growth.

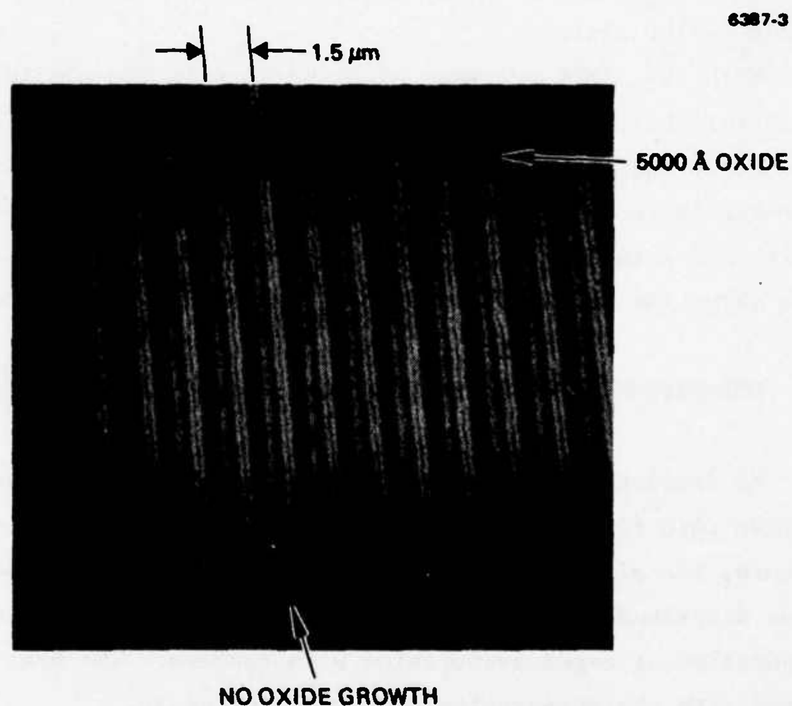

Figure 5. SEM photomicrograph of oxidized silicon wafer after removing nitride mask.

After etching the silicon nitride pattern, the aluminum contact mask must be removed. For many of the wafer lots we used an aluminum etchant Type B (Transcene Corporation, Rawly, Mass.). Later, we used

a simpler procedure. The standard wafer cleaning before furnace oxidation involves a hot NH_4OH and H_2O_2 solution. This cleaning step removes the aluminum completely. The aluminum etchant from Transcene Corporation must be heated and if the temperature gets out of range then some attack of the nitride takes place. Thus, the peroxide cleaning method is safer and simpler.

The characteristics of the plasma etch process at the mask edges were determined with scanning electron microscopy. Figure 6 shows a silicon nitride feature after just etching through to the silicon dioxide substrate and then removing the aluminum. The shelf indicates the etch rate in the immediate neighborhood of the aluminum mask is lower than compared with open areas. SEM measurements of linewidth clearly show that the shelf extends from the aluminum mask edge, i.e., the linewidth including the shelf is larger than the aluminum linewidth. Abe[4] has also observed this phenomenon.

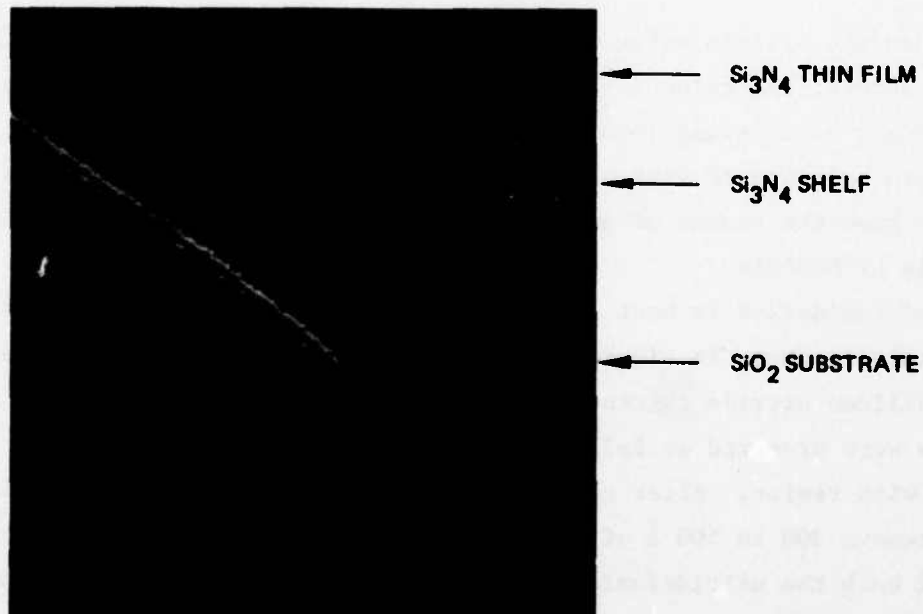

Figure 6. Nitride feature etched with CF_4 plasma using aluminum contact mask.

We studied linewidth with PMMA masking the CF_4 plasma etching. In this case the etching appeared isotropic; it undercuts at the same rate as it etches. It is interesting that with CF_4 plasma etching we have observed three cases:

(1) Etch rate at the mask edge is less than in the open area etching silicon nitride with aluminum mask.

(2) Etch rate at the mask edge equals that in the open area etching silicon nitride with PMMA mask, or etching polysilicon with aluminum mask.

(3) Etch rate at the mask edge is greater than in the open areas etching polysilicon thin films with PMMA mask.

Actually, the decreased Si_3N_4 etch rate at the Al mask edges is a desirable effect because controlled overetching removes the shelf in Figure 6. This means nitride features can be defined with zero undercut so that the mask and feature size are identical.

D. UNDEROXIDATION OF SILICON NITRIDE

When the silicon wafer with nitride patterns is oxidized, underoxidation occurs; the oxide layer grows laterally beneath the silicon nitride edges as it grows into the wafer. In the process the nitride edges are bent upward with respect to the wafer surface. There is a need to know the amount of underoxidation because it narrows the channels of MOSFETs.

Underoxidation is best observed with an SEM and cleaved samples. An example is shown in Figure 7. This sample had a pad oxide thickness and a silicon nitride thickness of 1,000 Å. To obtain the end view the samples were prepared as follows: Before cleaning the samples were coated with resist. After cleaning they were lightly etched in buffered HF to remove 300 to 500 Å of oxide thereby providing a better demarcation of both the nitride/oxide and the silicon/oxide interfaces. The resist can be removed and then the samples are ready for end-on viewing with the SEM. Note the feature labeled etch edge is an artifact of the oxide etching used to prepare the samples.

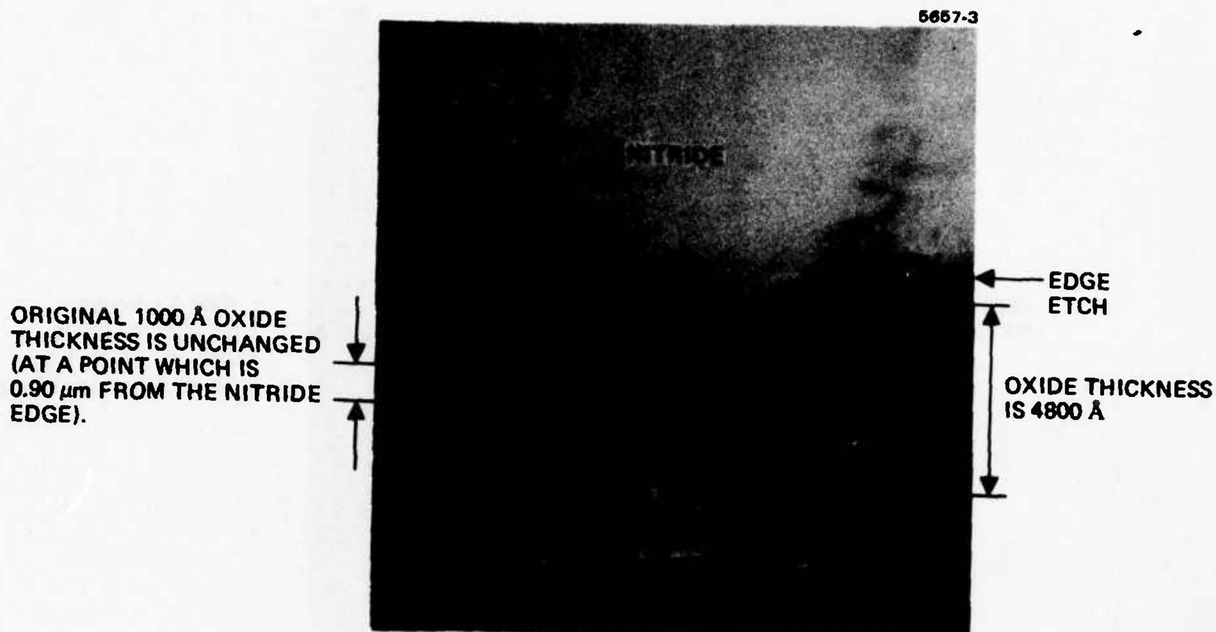

Figure 7. Edge view of oxidized silicon wafer after cleaving through nitride feature.

In the photomicrograph the nitride/oxide interface is shadowed, but the underoxidation is clearly seen at the silicon/oxide interface. The image indicates that zero undergrowth occurs at 0.7 to 0.8 μm from the edge. Such a large value for underoxidation limits the minimum usable size of nitride feature. For example, Figure 8 shows an end view from a different feature on the same wafer. Here the nitride was only 0.9 μm wide. Notice that the pad oxide thickness is 2,000 Å beneath the middle part of the nitride feature indicating 1,000 Å of growth occurred here.

The variables that most strongly control the amount of underoxidation are the pad oxide thickness, the field oxide thickness, and the nitride thickness. During the course of our work an article by Bassesus et al.[5] appeared showing it is desirable that the pad oxide thickness be minimal and the silicon nitride film thickness be large to get the lowest value of undergrowth. Our studies confirm these conclusions,

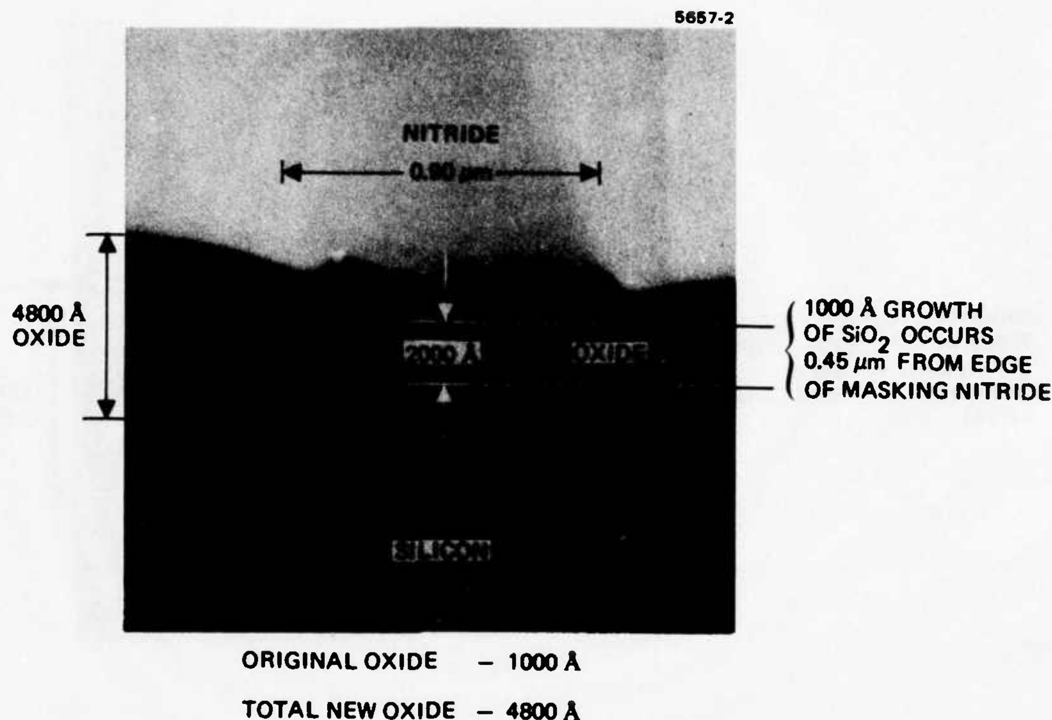

Figure 8. Edge view of oxidized silicon wafer after cleaving through 0.9-µm-wide nitride feature.

although numerical values of undergrowth differ. The results of both studies are summarized in Figure 9. Here, we plot two parameters, B_2 and H_3, versus the pad oxide thickness. As can be seen from the insert, B_2 and H_3 characterize the undergrowth. B_2 is the distance from zero undergrowth to the projection of the nitride edge above the original surface, whereas H_3 is the distance the nitride edge has been raised.

Notice that H_3 appears to be slightly dependent on pad oxide thickness and feature size. On some of the samples we measured with 1,000 Å oxide, H_3 is less for submicron features than for larger ones. The reason is that with submicron features on 1,000 Å pad oxides, B_2 is larger than the feature so there is oxide growing everywhere beneath the nitride surface. Figure 8 is an example of this. With undergrowth beneath all of the nitride structure, the amount of curvature logically should be less.

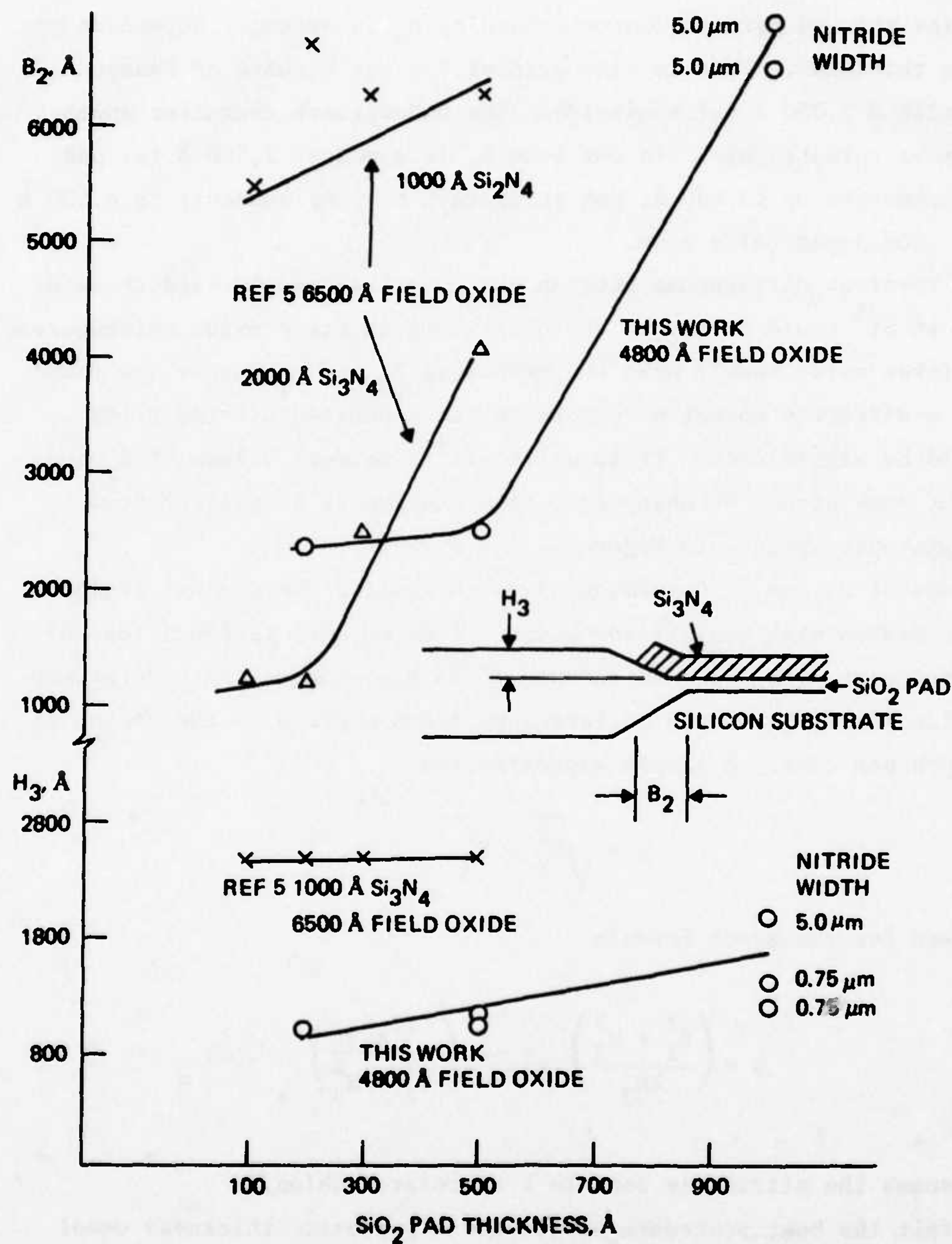

Figure 9. Underoxidation parameters versus pad oxide thickness.

Notice the undergrowth characterized by B_2 is strongly dependent on pad oxide thickness. This is also evident for the results of Basseous et al.[5] with a 2,000 Å thick nitride. The undergrowth character appears to be almost catastrophic. In our case B_2 is a modest 2,500 Å for pad oxide thicknesses up to 500 Å, but it appears to jump suddenly to 6,500 Å for the 1,000 Å pad oxide case.

The apparent differences between our numerical results and those of Basseous et al[5] could be due to the difference in field oxide thicknesses. Their thicker oxide should make the values of H_3 and B_2 larger, as found. However, a different amount of stress in the deposited nitride films also could be significant. It is difficult to measure values of B_2 and H_3 without some amount of observer interpretation as is evident from the SEM photomicrographs in Figures 7 and 8.

Values of B_2 and H_3 determine how much smaller the channel region will be compared with the nitride width. (The channel region is essentially that part with zero undergrowth.) To accommodate the undergrowth the nitride linewidth should be larger by 2 x S where S is the amount of undergrowth per edge. A simple approximation,

$$S \approx \sqrt{B_2^2 + H_3^2} \quad ,$$

can be used for the exact formula

$$S = \left(\frac{B_2^2 + H_2^2}{2H_3} \right) \sin^{-1} \left(\frac{2B_2H_3}{B_2^2 + H_3^2} \right) \quad ,$$

which assumes the nitride is bent in a circular fashion.

We felt the best procedure was to use a pad oxide thickness equal to 500 Å and nitride thickness 1,000 Å, giving an oversize value for S of 0.27 μm. We prefer not to use thinner pad oxides because these are transparent and do not provide a convenient etch endpoint detection.

Moreover, since extended etching is required to remove the nitride shelf, very thin oxides do not provide sufficient protection from etching the silicon substrate. We also chose not to use thicker nitride films because the change in S would be small at the risk of making the etching of submicron features a more difficult task.

E. ONE-MICROMETER-WIDE PATTERNS IN POLYSILICON

The problem here is the same as was the case with the nitride pattern — there is a need to remove large areas of material with only a positive resist available. Consequently, we explored the aluminum replacement technique with CF_4 plasma etching for the polysilicon layers.

The application of this method was straightforward. As with patterning the nitride, we removed the polysilicon with CF_4 plasma using the LFE reactor equipped with a perforated cylinder. Placing the wafers within the cylinder shields them from plasma-induced damage while still permitting diffusion of silicon etching reactants to the surface. This is important for the case of etching the polysilicon because CV measurements have shown that without the shield a high density of surface states occurs.[6]

Linewidth measurements showed only a modest amount of undercutting with the CF_4 plasma etch using the aluminum mask of polysilicon. We took pictures of the aluminum features at 10,000x using the scanning electron microscope. Then the same features were examined again after stripping the aluminum. Averaging 11 samples showed that a polysilicon feature was 0.3 μm ±0.1 μm smaller than the aluminum feature, i.e., ~0.15 μm was lost at each edge. This is the value to be expected for 10% overetching when the etching character is isotropic.[7]

Figure 10 shows some photomicrographs of polysilicon features after etching and stripping the aluminum mask. In this case, the gate features cross over oxide features formed from the nitride masked oxidation. Notice the 1.1 μm x 1 μm transistor. This used the oversizing information for both polysilicon and nitride.

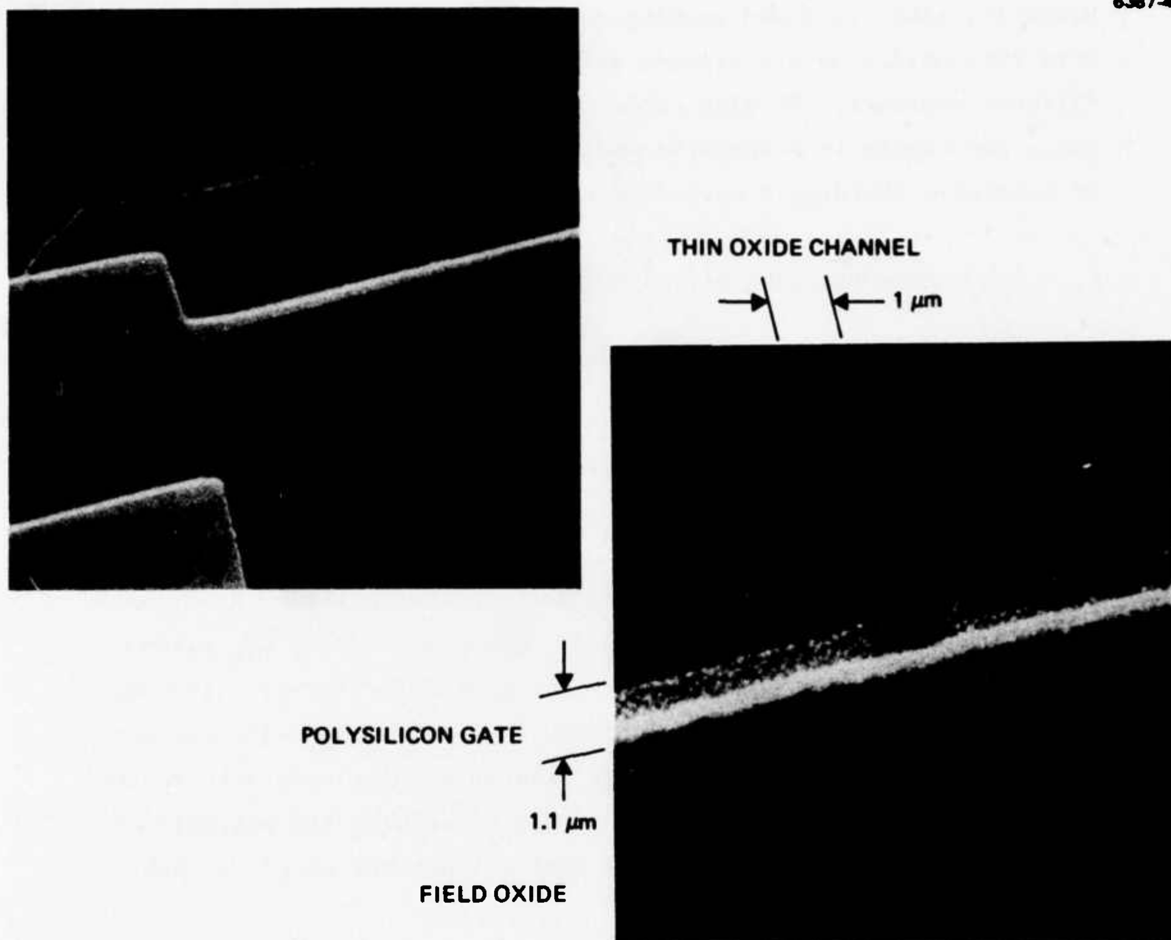

Figure 10. Polysilicon transistor gates etched with CF_4 plasma and using aluminum masks.

F. DESIGN RULES FOR NIMOX PROCESS

The design rules consist of three elements. First, there is the amount of over- or undersize necessary. This is the change by which the feature must be drawn so that the actual feature size equals the desired dimension. Second, there is the minimum gap and the minimum feature

permitted by the lithography. Finally, there is the alignment tolerance. If one separates or overlaps the drawn features that already have the linewidth bias, then the alignment tolerance is the electron beam machine tolerance. These rules are listed below for the nitride, polysilicon, contact hole, and aluminum lithogrphies. The contact hole and the aluminum rules are taken from other work at HRL and are included in Table 2 for completeness.

Table 2. Design Rules for NIMOX Process

Linewidth bias		
Nitride	Oversize by 0.55 μm	
Polysilicon	Oversize by 0.3 μm	
Contact via	Undersize by 0.2 μm	
Aluminum	No bias required	
Minimum feature separation and feature size		
	Separation	Size
Nitride	1.0 μm	0.8 μm
Polysilicon	1.0 μm	0.8 μm
Contact hole	1.5 μm	1.0 μm
Aluminum	1.0 μm	0.8 μm
Feature alignment ±0.4 μm		

SECTION 4

TEST CHIPS

A number of test chips were designed for this program. To avoid any delay due to mask making we used a test die from an existing mask set. The active structures were not those of interest to this work, but these posed no difficulty because they were defined with e-beam lithography. The e-beam layers only required digitizing a drawing and generating a data tape. It was only necessary to lay out the new electron beam defined structures to interface with the existing photolithographic masks for contact holes and aluminum.

Figure 11 shows the N42 chip. (In the figures of the test chips the light color is the polysilicon and the darker gray are the thin oxide areas delineated by the nitride masking. Each of these interface with a series of contact holes and aluminum leads about the edges of the chip.) The five implant-continuity testers in Figure 11 can be used to determine the implant resistivity or they can test the probability of an open versus feature size. The polysilicon continuity testers can be used for the same purposes. The polysilicon continuity runners pass over many steps in the field oxide as shown in the insert SEM photomicrograph. There is an N43 version of this test chip in which the runners pass over only a smooth field oxide. The MOS thin oxide capacitor is used to characterize substrate doping, gate oxide thickness, flat band voltage, surface state density, and Na contamination. The spiking test is merely a large area contact that examines the probability of a short from the aluminum metallization through to the substrate. The transistors consist of many different W/L combinations with minimum W and L values of 1 μm.

Figure 12 shows the N41 chip. The top structures allow determining the leakage between narrowly separated implant regions. The W/L test is an attempt to measure underoxidation electrically. All features are laid out with the same value of W/L; however, they have differing

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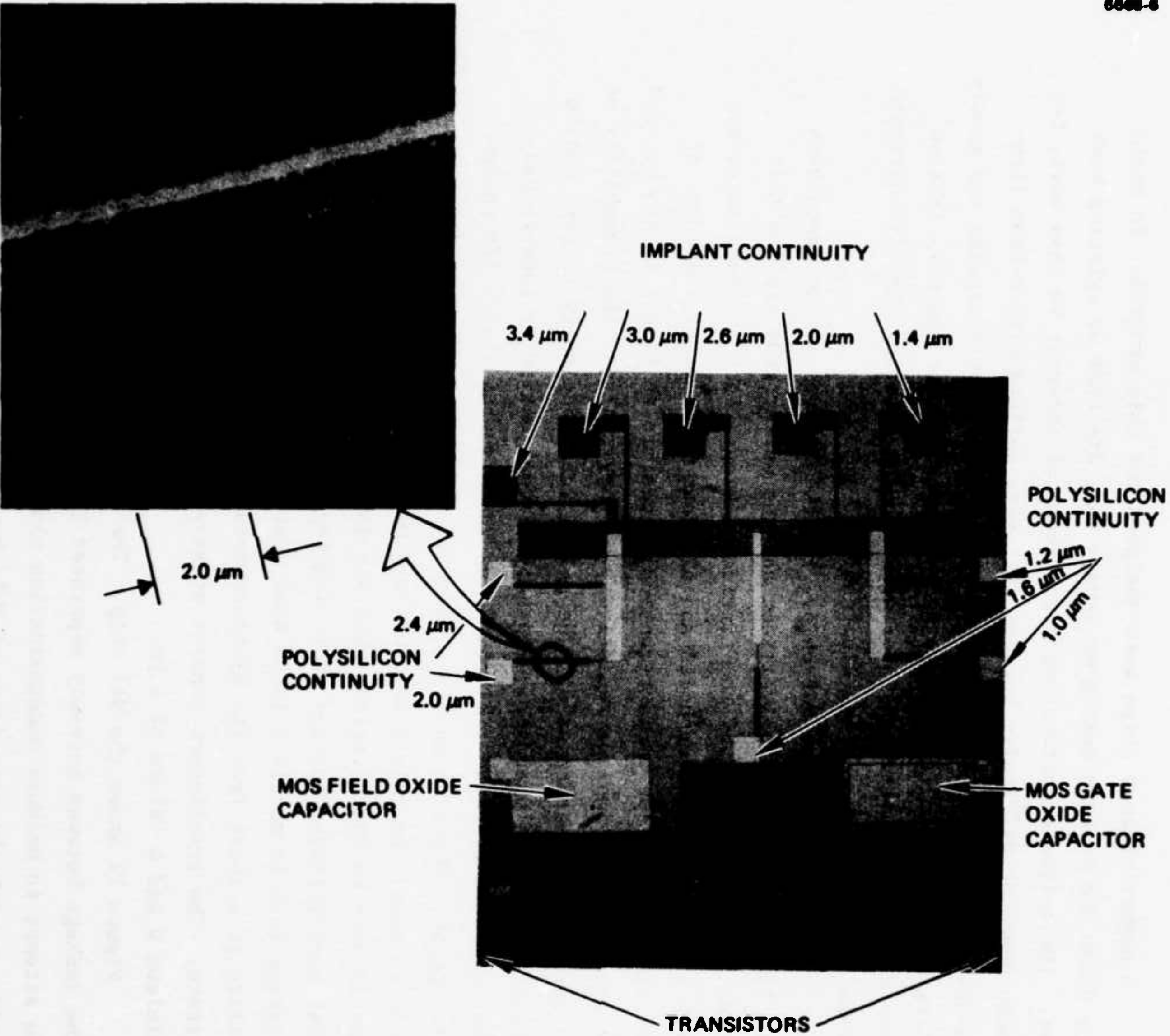

Figure 11. Diagnostic chip N42.

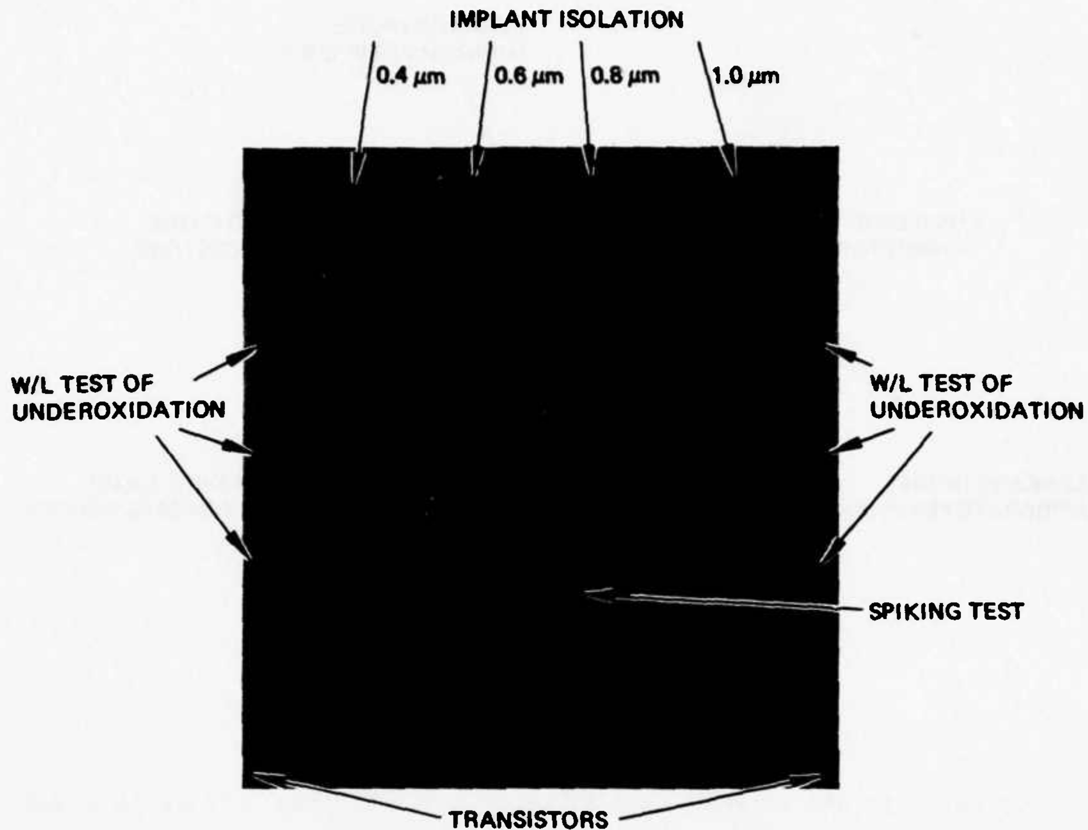

Figure 12. Diagnostic chip N41.

absolute values. Underoxidation will affect W and not L, so measuring the resistance and plotting the ratio should, in principle, permit determining the underoxidation. Chip N41 also includes a set of transistors.

Chip N44 is shown in Figure 13. The field oxide transistors are useful for determining the field threshold voltage. This chip is also used to test implant to substrate leakage. For this purpose we make three n^+p diodes with the same area but different periphery. Figure 5 is an SEM photomicrograph of the diode with the closest spaced fingers (also the largest periphery). The insert in Figure 13 shows the moderate periphery diode after oxidation and removal of the nitride.

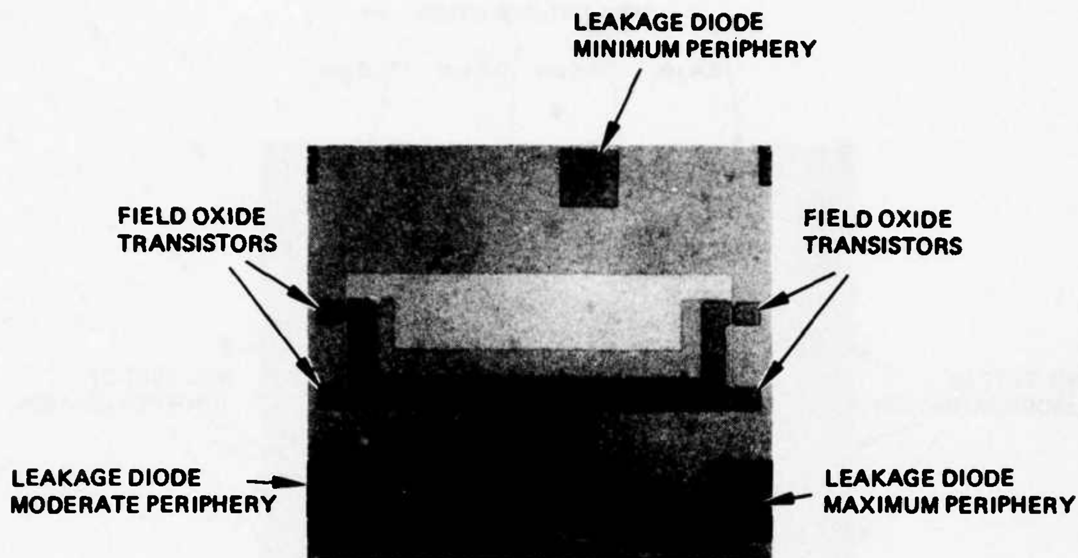

Figure 13. Diagnostic chip N44.

Figures 14 and 16 show some selected test results. Figure 14 shows some IV results testing 1-μm-long transistors as contrasted with a more conventional size transistor. As would be expected, the short channel transistor shows more channel length modulation. Figure 15 shows results testing the isoplanar continuity tester. From the results it can be deduced that the implant Ω/□ is 180. Figure 16 shows the IV characteristics of the field oxide transistor. On this particular wafer there was a leakage problem in the field region since the transistors will not shut off. Such results demonstrate a difficulty controlling the wafer doping in the field region which is discussed more fully in the next section.

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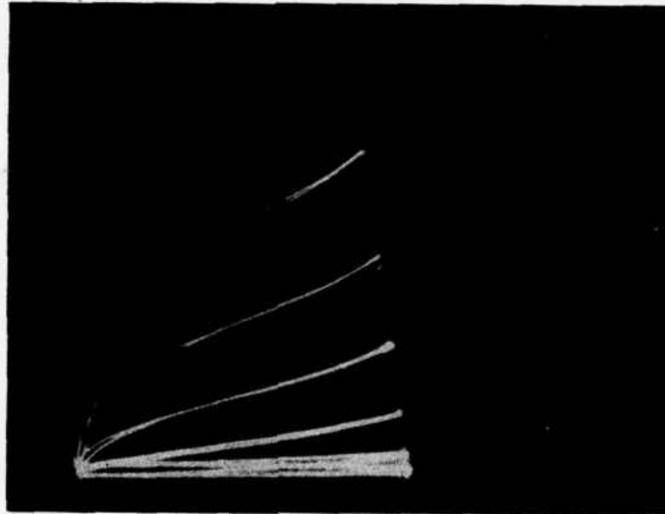
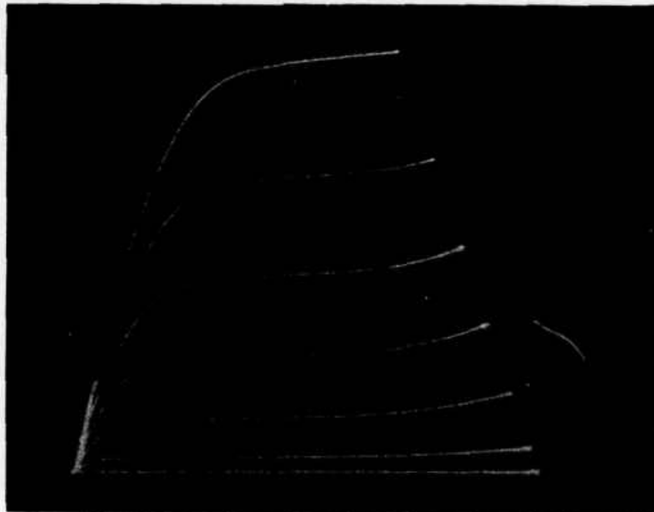


n–CHANNEL MOSFET
W = 1 μm
L = 1 μm



n–CHANNEL MOSFET
W = 30 μm
L = 5 μm

Figure 14. IV characteristics of n-channel MOSFET mode with electron beam lithography.

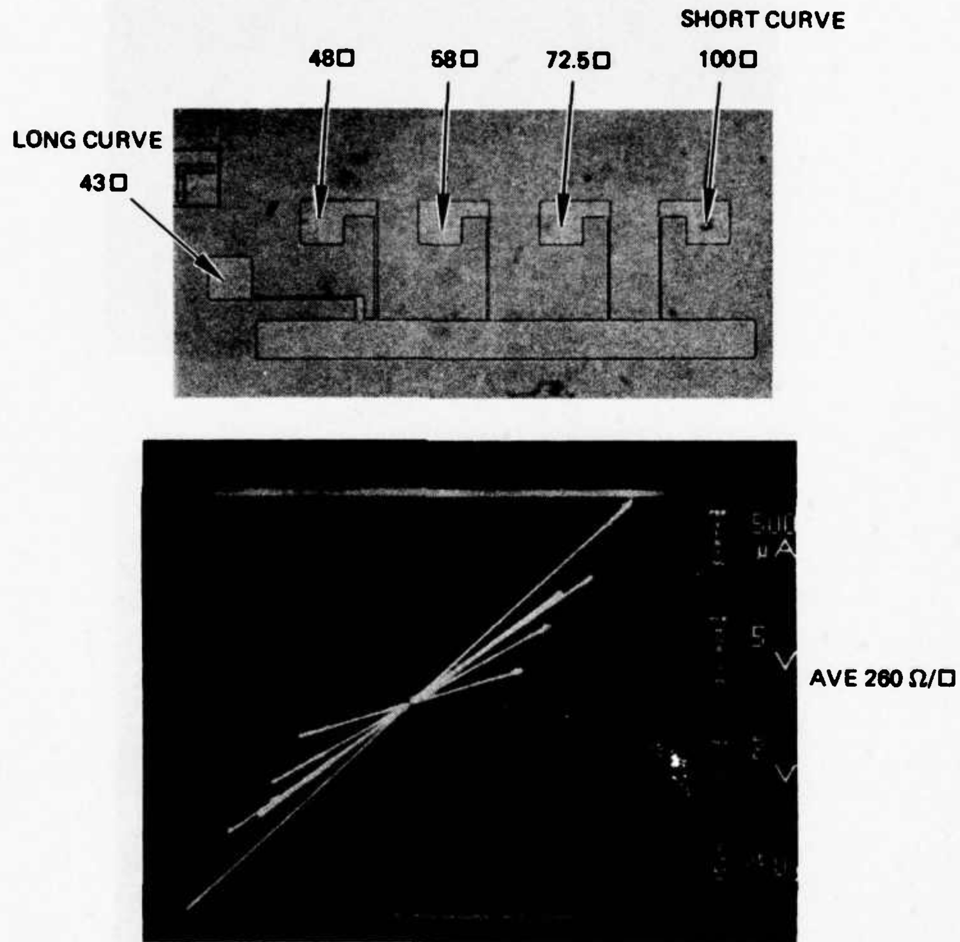


Figure 15. Results from testing implant continuity.

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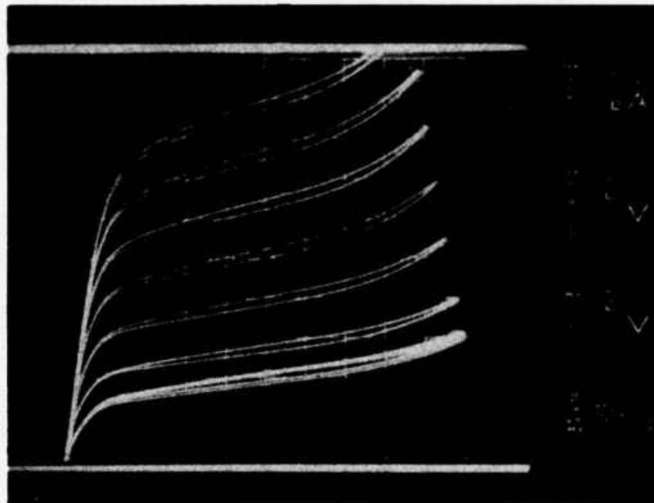

Figure 16. IV characteristic of field oxide transistor.

SECTION 5

WAFER PROCESSING

The wafer processing was summarized in Table 1. This processing was modeled with a simulation program. The doping was analyzed at four positions of a typical transistor — the field (A), the gate (B), the source or drain (C), and the contact region (D). Figure 17 plots the doping for each of these areas. First we note that the junction depth of the source drain is shallow (about 2,600 Å). This is caused by the limited penetration of the As^+ ion during implant as well as the low value of its diffusion coefficient. As mentioned earlier, such shallow junctions are desirable for short-channel transistors to maintain constant values of threshold voltage for different gate lengths. Shallow junctions, on the other hand, exacerbate the problem of metallization spiking through to the substrate. However, we have solved that problem by depositing 0.5 μm of polysilicon before the aluminum. This contact region is also plotted in Figure 17 although the simulation program cannot calculate the diffusion of phosphorus through the polysilicon. The values plotted in Figure 17 approximate this by assuming that phosphorus diffuses in polycrystalline films the same as in single-crystal material. Since the diffusion is much slower in single crystals, the data plotted in Figure 17 underestimate the phosphorus depth, but nonetheless, assure that the phosphorous doping procedure penetrates the polysilicon film into the contact region.

Notice that the boron doping in the field region is depleted by a factor of two with respect to the gate region. This depletion arises because the boron dopant is preferentially absorbed into the growing oxide phase. Higher field doping could be obtained if the wafer were implanted prior to field oxidation.

The initial process we chose had to be modified in several details. For example, we use 150 keV arsenic implants rather than 300 keV. The larger voltage was used initially to assure that all the arsenic penetrated the thin gate oxide that was left in place over the source/drain.

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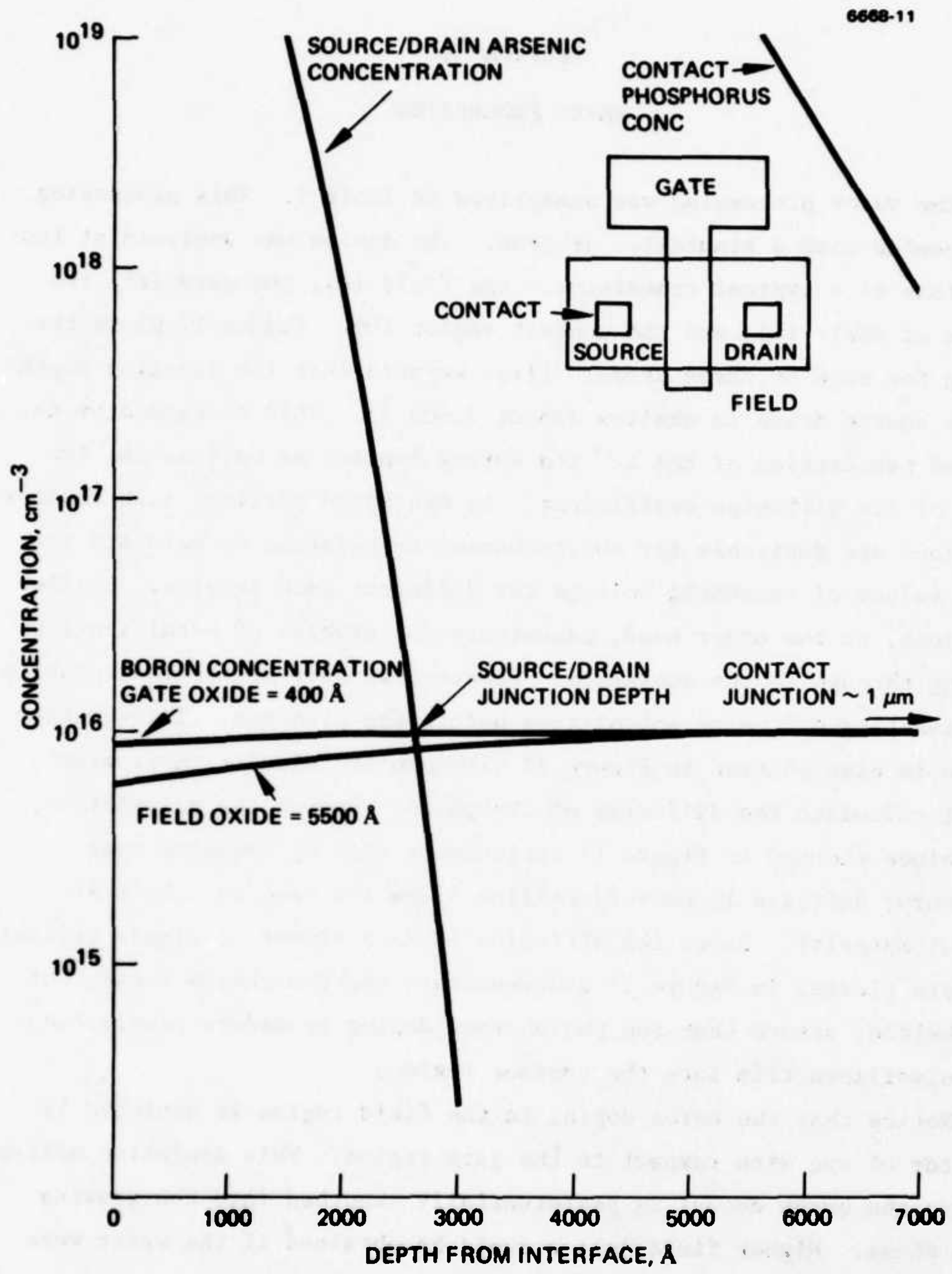

Figure 17. Calculated doping profiles for NIMOX process.

However, it turned out that a significant tail of 300 keV As ions penetrated the polysilicon gate to create n-type doping in the semiconductor. Switching to 150 keV eliminated the gate penetration without causing any difficulties doping the source/drain.

Another problem of early lots was diode leakage. This problem was traced to the type of gas ambient with the anneal step after arsenic implant. If we annealed with N_2, leakage was acceptable, but if we used O_2, leakage was excessive. This is illusttated from the data obtained from the periphery type diode shown in Figure 18.

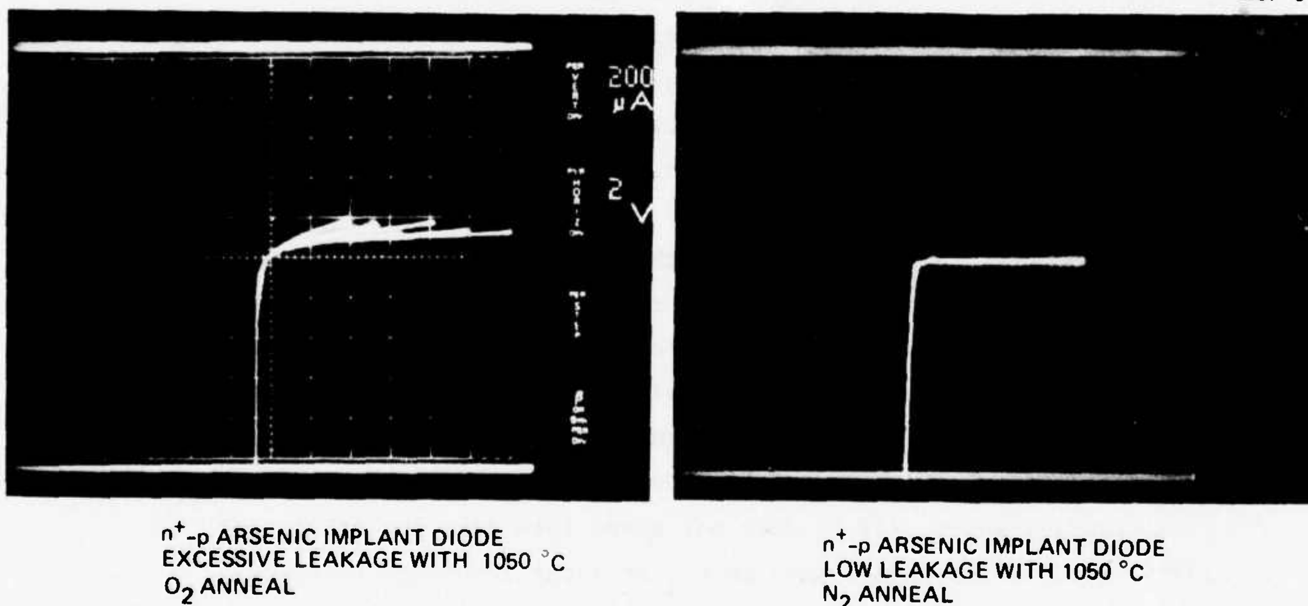

Figure 18. Comparison of diode characteristics from O_2 versus N_2 implant anneal.

The original reason for using O_2 for the implant anneal was to provide pinhole protection at polysilicon/aluminum crossovers by thermal oxidation of the polysilicon layer. Revising the process so that the oxidation step takes place after a N_2 implant anneal provides both the pinhole protection and low diode leakage.

Several schemes were tried for doping the contact regions. We tried originally a phosphorus diffusion into the contact hole and then a second photolithography procedure to remove the glass in the contact regions. However, even submicron misalignment prevented this technique from working. We also tried a simple wash etch after diffusion, obtaining the glass etch time from a monitor wafer. With skill and attention this method works, but it is vulnerable to overetching. The best method was to deposit another polysilicon film after etching the contact windows, and then diffuse phosphorus into this layer. When the aluminum is deposited and etched, it serves as a plasma etch mask to remove excess polysilicon. This method leaves a polysilicon/aluminum sandwich structure for the interconnection metallization and, in effect, creates a deep junction by the separation of the aluminum to the substrate through the addition of the polysilicon layer. To date, we have tested sufficient contacts to exceed 10^6 μm^2 total area without a substrate short or a contact open.

The major unresolved problem with the processing appears to be inordinately large values of Q_{ss} for the gate oxides combined with lack of control of the field threshold. For example, Figure 20 contrasts the CV traces from test capacitors made with the NIMOX process and one made from a simple oxidized wafer, i.e., the gate oxidation monitor. The differences between these are that the NIMOX wafer (1) has a more negative flatband shift, (2) it does not sweep into deep depletion, and (3) it returns its capacitance to C_{ox} at large inversion voltages. Obviously, the differences are due to additional processing since both wafers were oxidized at the same time. The reason for the NIMOX capacitor behavior at inversion is thought to be caused by lack of doping control in the silicon under the field oxide providing a ready supply of minority carriers adjacent to the depletion region. As shown in Figure 16, the field oxide transistor cannot be shut off indicating a layer of electrons beneath the field oxide.

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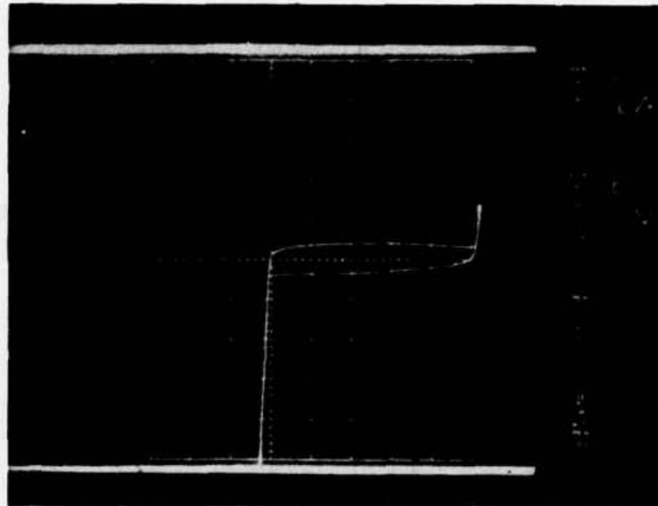
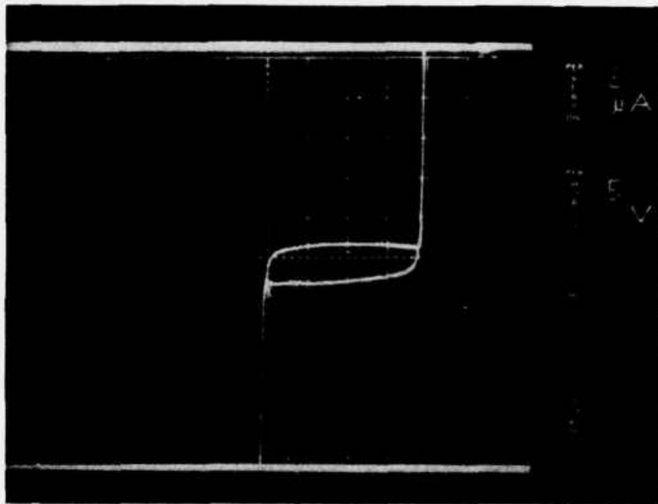


SPIKE TEST



SOURCE/DRAIN

Figure 19. Reversed bias IV character with respect to substrate of spike test diode and source drain.

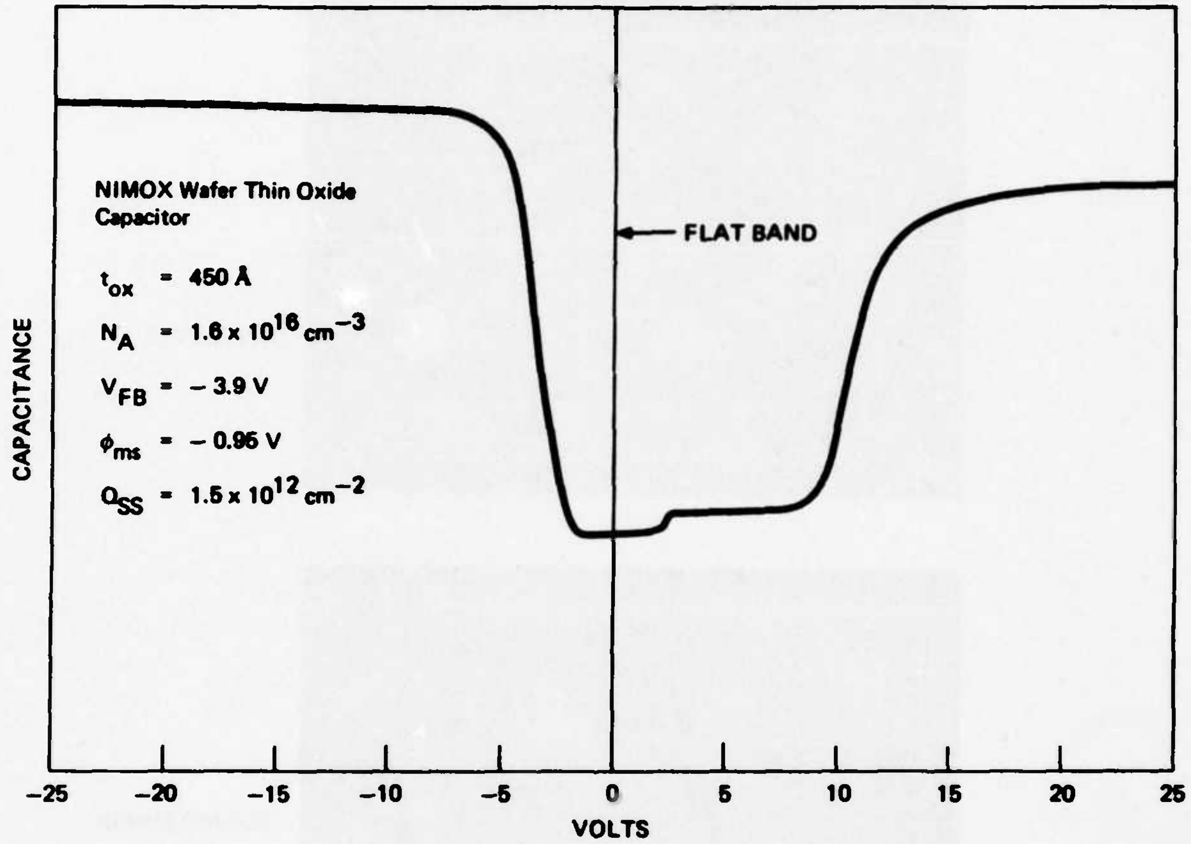


Figure 20(a). CV curve for NIMOX process wafer, n^+ polysilicon gate.

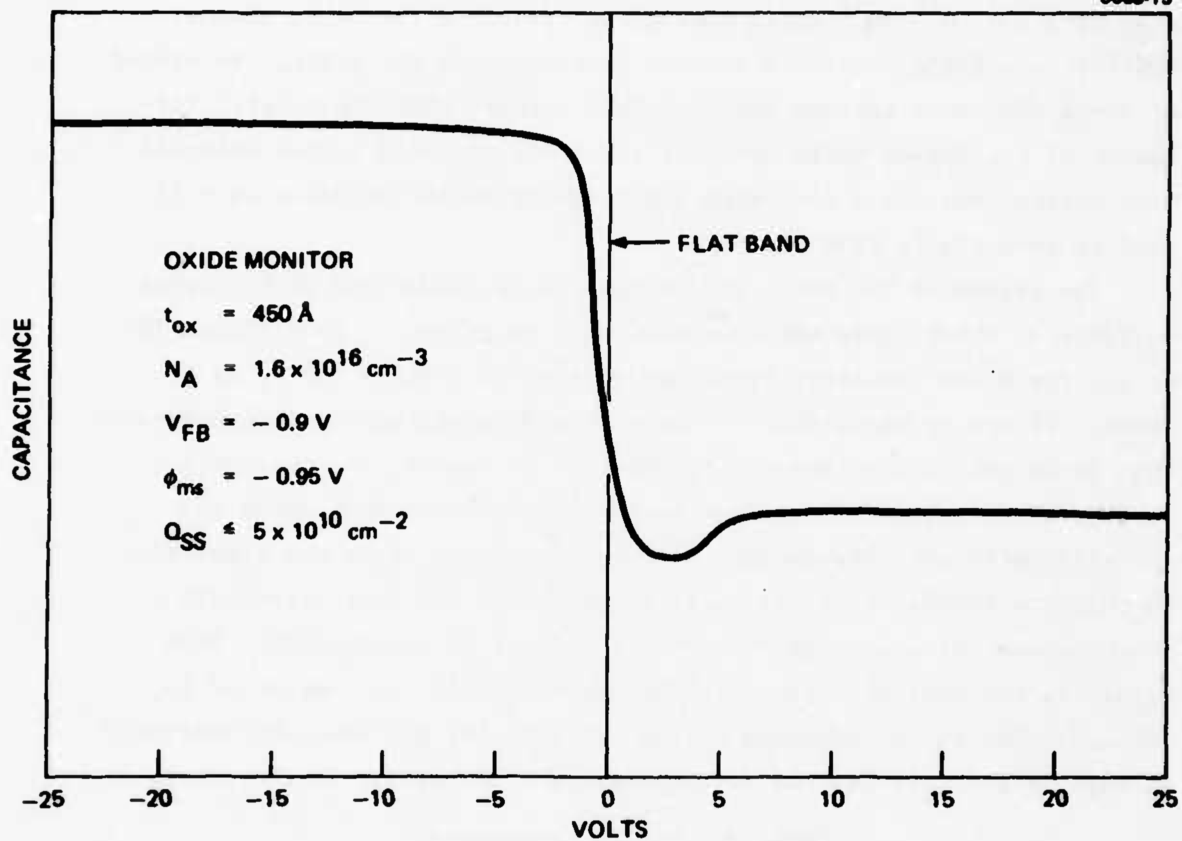


Figure 20(b). CV curve for gate oxidation run monitor, n^+ polysilicon gate.

We need to do further work to determine the reason for the unusually negative turn-on voltages. The field oxide threshold voltage problem can probably be solved with a boron implant prior to oxidation, as is done with NIMOX processing with conventional devices. We had anticipated that with the 10^{16} cm^{-3} doped substrates, required for short channel MOSFETs, the field threshold voltage problem would not arise. We wanted to avoid the boron implant approach from concern that the lateral diffusion of the dopant would possibly pinch off the very narrow channels. Nonetheless, the field inversion shown in Figure 16 indicates we will need to investigate this approach.

The status of the wafer processing can be summarized with respect to Table 3, which lists the desired device parameters. From Figure 19 we see the n^+-to-substrate breakdown voltage is clearly $\sim$15 V, as desired. Figure 20 shows that the gate breakdown voltage is indeed greater than 20 V, the gate oxides are the desired thickness, the substrate doping is the required level and that the phosphorus that dopes the polysilicon is not penetrating the channel region. From the transistor IV characteristics in Figure 14 it is seen that the source-to-drain punchthrough voltage is greater than 7 V for 1 μm transistors. From Figure 11 the implant resistivity is approximately that specified in Table 3. The field threshold voltage (Figure 16) and the gate threshold voltage (Figure 20) are the two parameters that require further work.

Table 3. Device Parameters

Parameter	Value
Breakdown voltage n^+ to substrate	15 V
Breakdown voltage, gate to substrate	20 V
Threshold voltage, gate oxide	0.5 V
Threshold voltage, field oxide	10 V
Punchthrough voltage, source to drain	7 V
Polysilicon sheet resistivity	25 Ω/□
Gate oxide thickness	400 to 600 Å
Field oxide thickness	6,000 to 7,000 Å
Substrate doping	1×10^{16} cm^{-3}
Implant sheet resistivity	200 Ω/□

SECTION 6

CIRCUIT DESIGN

The clamp-sample-and-hold (CSH) circuit was designed to detect analog output signals from an n-channel CCD operating at a clock frequency of 25 MHz. Our design philosophy has been to minimize circuit and processing complexities, while retaining all the essential elements of a CSH circuit.

To aid in circuit design we have used XSPICE, a Hughes modification of SPICE (originally written at Berkeley), which is a general-purpose simulation program for nonlinear transient analysis of any given circuit. The MOS circuit models in XSPICE are improved versions of the work done by D. Frohman-Bentchkowsky and A.S. Grove.[8] This model includes provisions for the effects of bulk charge on channel conduction, channel length modulation, channel carrier mobility reduction resulting from large normal electric fields, and the various voltage dependent gate, source, and drain capacitance.

The first consideration in the CSH circuit design was its basic configuration — common source amplifiers or source follower amplifiers. A common source configuration was rejected for several reasons. First, there are problems associated with building a dc-coupled multistage amplifier. Each stage would have to be correctly matched in gain and bias to the following stages in order that the output of each stage be a linear function of its input. Our preliminary work indicated this would be difficult to do. Conceivably, one could ac couple the stages, but this would require additional undesirable circuit elements. Also, a problem would result from the 5 V limitation on FET drain voltages to avoid punchthrough of 1 μm transistors. Thus the gain of each common source stage could not be made much greater than one, or the input voltage swing would have to be small (input capacitance large), and thus decrease the noise immunity of the circuit. The source-follower amplifier provides only current gain and therefore these problems do not exist

in a multistage amplifier. It was also felt that a source-follower stage would be more immune to FET nonlinearities than a common source stage.

The circuit calculations used device parameters given in Table 2 and the following:

Drain resistance = 100 Ω
Source resistance = 100 Ω
Gate overlap of source and drain = 1,000 Å
Zero bias source-substrate capacitance = 1.9×10^{-11} F/cm
Zero bias drain-substrate capacitance = 1.9×10^{-11} F/cm
Electron mobility = 500 cm^2/V-sec.

Conservative values of 5 V and 10 pF were taken for maximum drain voltage and output load capacitances, respectively. To determine as nearly as possible the parasitic capacitances, the charge detection node and the first stage of the CSH circuit were laid out. The parasitic capacitances on the charge detection node included 5×10^{-16} pF of capacitance that was due to polysilicon lines running from the CCD output diffusion to the input of FET gate and 5.8×10^{-16} pF capacitance of the output diffusion.

The CSH circuit shown in Figure 21 uses three amplification stages and has a clamping capacitance of 6×10^{-14} pF. The parasitic capacitances C_{p1} and C_{p2} were conservatively estimated from the layout as 1.9×10^{-15} pF and 7.6×10^{-16} pF. The W/L values of each FET are indicated in microns. The appropriate function of each part of the circuit is indicated by the dotted lines. Each amplification stage except the last consists of an input FET and a bias FET. The voltage applied to the bias FETs is given in terms of the turn-on or threshold voltage V_{to}. With a 3/1 input FET, a voltage swing on the input gate of 5 V would correspond to a maximum detectable signal of 86K electrons. Various design tradeoffs must occur in the choice of a CSH circuit. These are discussed below.

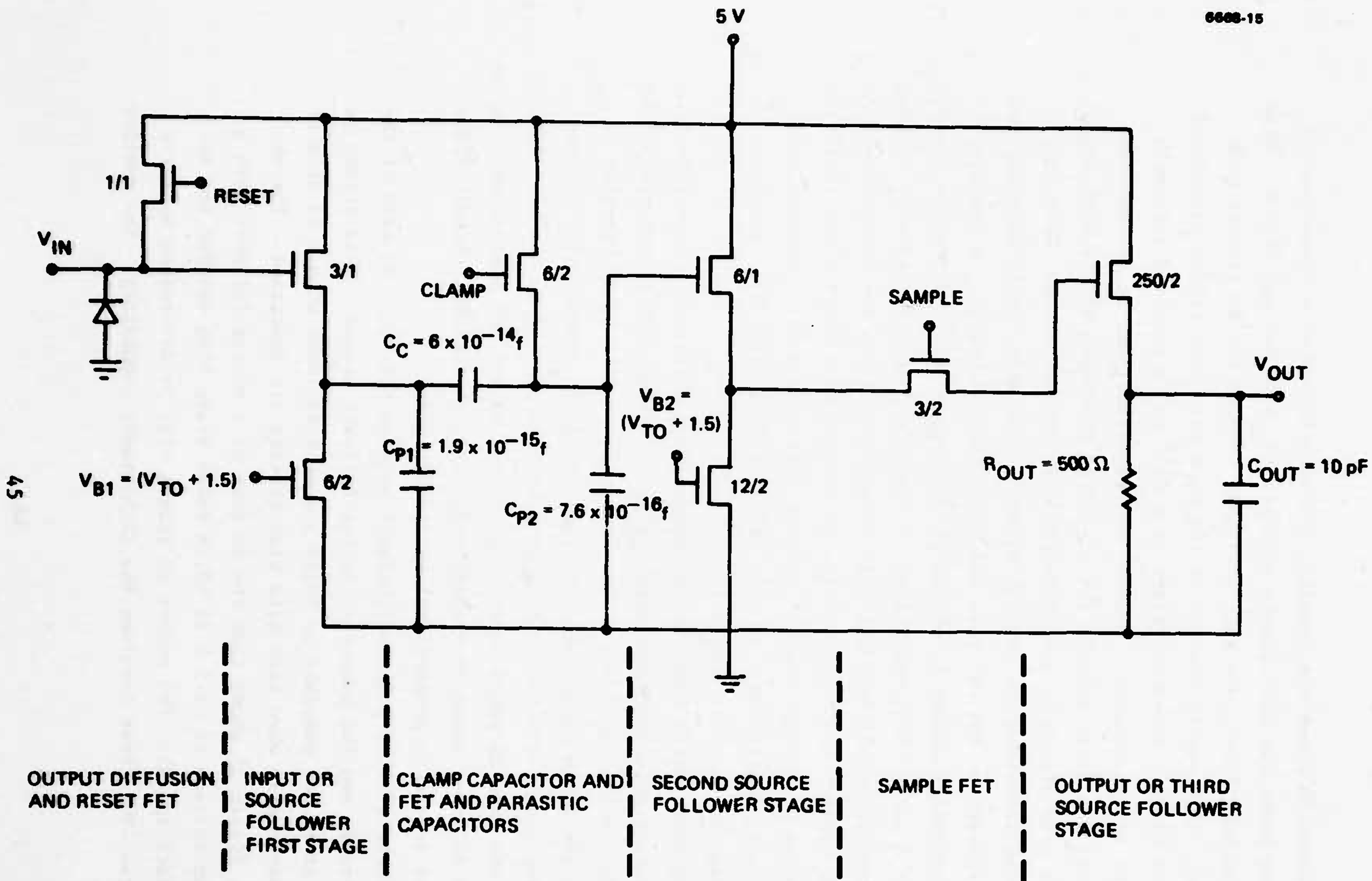


Figure 21. CSH circuit configuration. W/L values in microns are given for each FET.

Figure 22 shows the transfer characteristics of a single-source follower stage for FET turn-on voltages (V_{to}) of 0.5 and -1.5 V. Note that the negative V_{to} is more desirable because the dc gain is much greater. This occurs because of the back gate bias effect associated with the heavily doped substrate (1×10^{16} cm^{-3}) required for small geometry CCD structures. Because the substrate must be at the same potential (we chose ground) for all FETs, the input FET of each stage is back gate biased by the output voltage of that stage. This back gate bias increases the turn-on voltage, thus effectively reducing the input voltage to the FET gate and hence the stage gain. A negative turn-on voltage serves to offset the back gate bias and restore the dc gain of a source-follower stage. To produce a negative turn-on voltage an n-type threshold implant would be required since the turn-on voltage with no implant would be 0.56 V. It is true that many of the test structures have a negative turn-on voltage (see Figure 19). However, this is not well controlled. Thus, a tradeoff will exist here between circuit gain and process complexity.

Another design tradeoff is between gain and speed. A source-follower dc gain increases with the increased channel resistance of the bias FET, while the drain current decreases. This is illustrated in Figure 23, which shows output voltage and drain current of a source-follower stage as a function of gate voltage applied to the bias FET. Since the rate at which capacitors can be charged and discharged by a source follower stage is proportional to drain current, circuit speed will be inversely proportional to circuit gain.

There will be a second tradeoff between the total dc gain of the CSH circuit and the number of source-follower stages. This occurs because it is not possible to build a source follower with a dc gain of one, especially when back gate bias effects are important. For example, Figure 21 shows that the dc gain of a source follower with a turn-on voltage of -1.5 V is $\sim$0.74 (with stage bias set for the appropriate speed). The number of stages will be determined by three factors. The first involves the lithography capability. The smaller

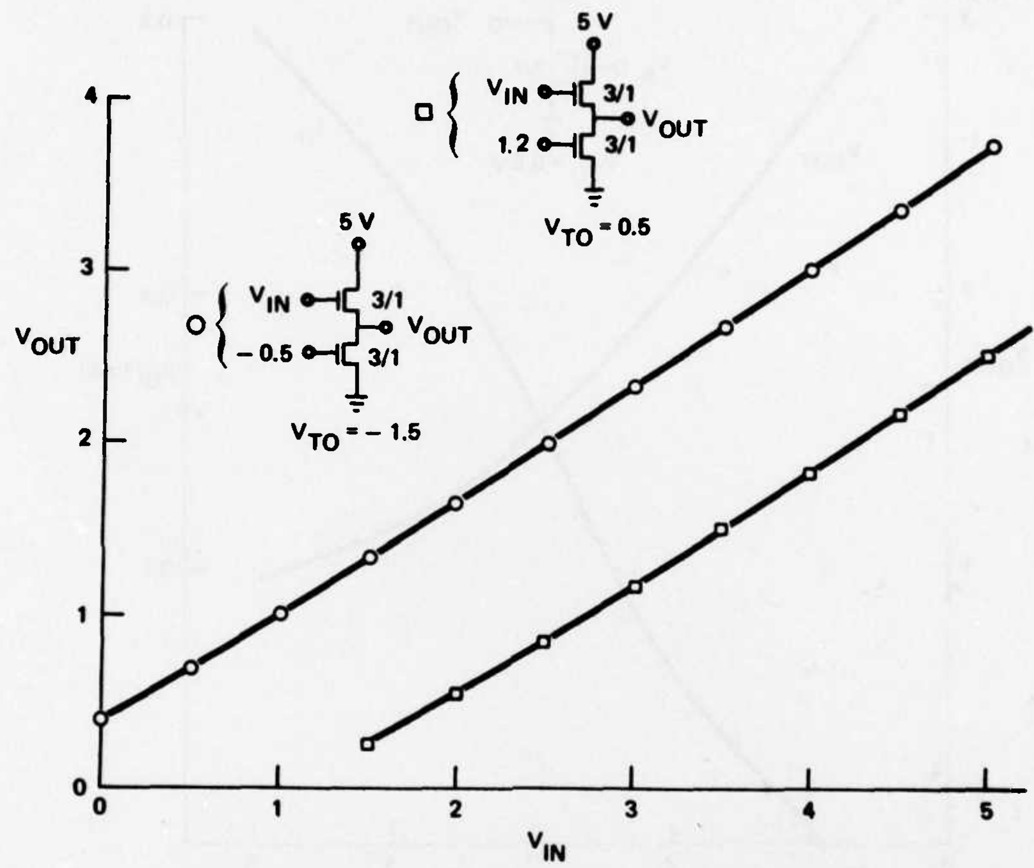


Figure 22. Transfer characteristics of a source-follower stage for two values of threshold voltage.

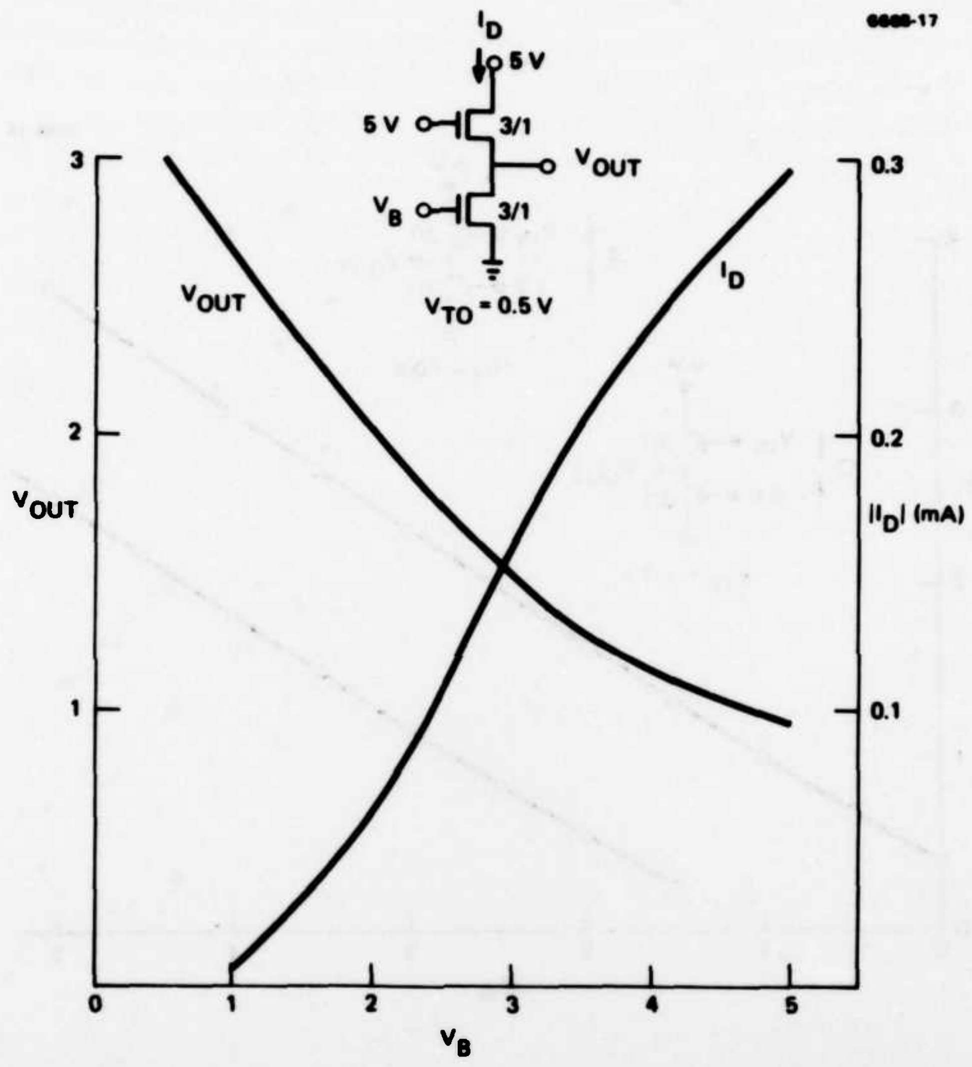


Figure 23. Source-follower output and drain current versus bias FET voltage.

the gate length, the smaller the gate capacitance for a given FET transconductance g_m. Therefore, fewer stages will be required to drive the FET gate capacitances. A second consideration is the input and output drive requirements of the CSH circuit. The input gate size or the input FET g_m will be determined by the CCD bucket size and the output FET g_m will be determined by the size of the output capacitance load. The smaller the value of the input FET g_m or the larger the output FET g_m, the more stages will be required for a given lithography capability. A final factor affecting the number of amplifier stages is the required size of the clamping capacitor C_c (Figure 21). This capacitor reduces the reset noise according to the ratio C_n/C_c, where C_n is the capacitance of the CCD output charge detection node. This capacitor has to be charged and discharged through the bias FET of the first source-follower stage. The very small current that flows in this stage then puts a limit on the maximum value for C_c. Even larger values of C_c would require inclusion of an additional stage here.

A final design tradeoff is associated with the large g_m required by the output FET which drives the 10 pF load. Since the output bias resistor (Figure 21) cannot be greater than about 1 kΩ to allow fast enough speed, the gain of the last stages will be determined entirely by the g_m or, in particular, the W/L ratio of this output FET. We have tentatively settled on a W/L of 250/2, since this value provides a reasonable gain ($\sim$0.45 for R_{out} = 1K, V_{to} = 0.5), yet still appears possible to build from a fabrication viewpoint.

Performance of the CSH circuit of Figure 11 is illustrated in Figures 24 through 28. Figure 24 shows the maximum output voltage swing versus V_{to} that results when a 5 V bucket of charge is dumped on the input. One sees that the maximum voltage swing is optimized for V_{to} = -1.75 V, or about three times that for V_{to} = 0.5 V. A second curve in this figure demonstrates the increase in gain which occurs when the voltage on the bias FETs is decreased and R_{out} is increased (with these changes the circuit will not operate at the required speed). Figures 25 and 26 illustrate the input-output linearity

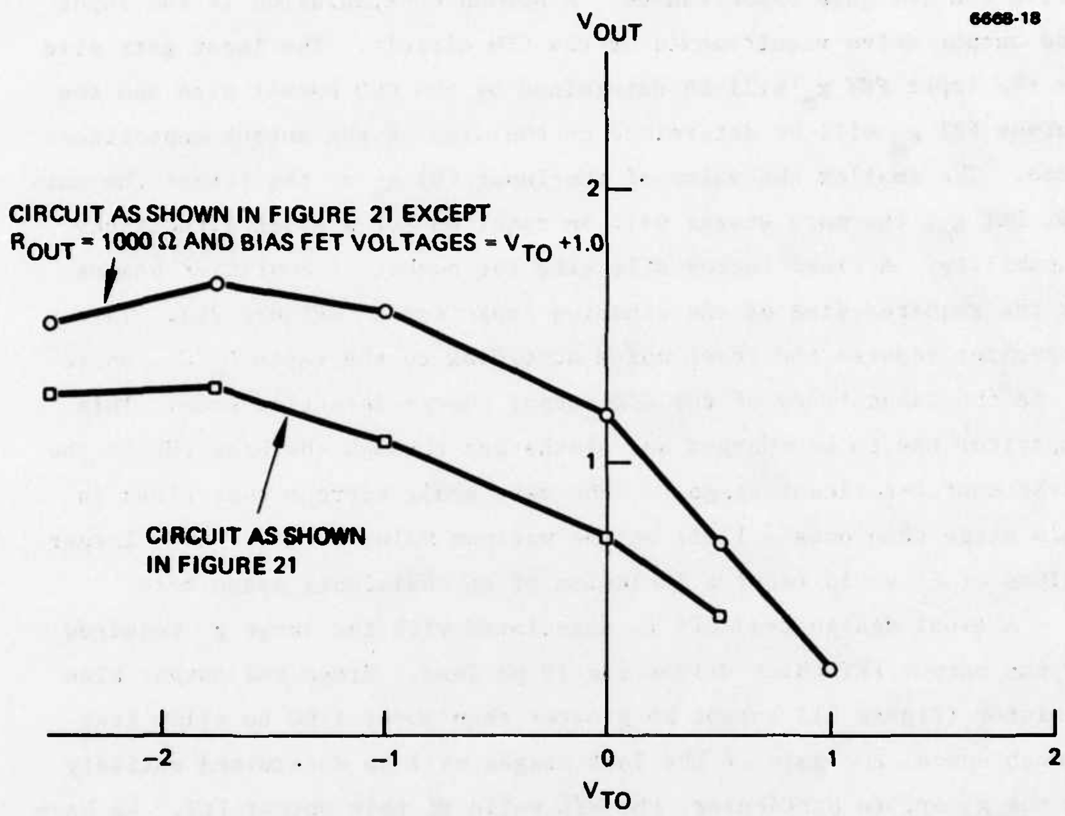


Figure 24. Output voltage swing ΔV_{out} for 5 V input versus V_{to}.

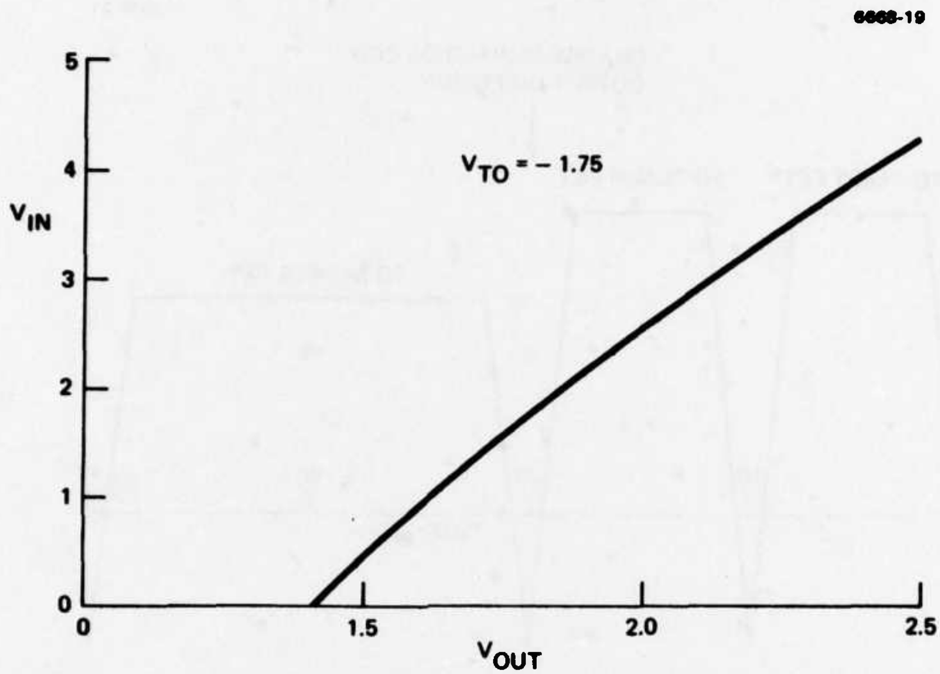


Figure 25. Linearity of CSH circuit for V_{to} = -1.75 V.

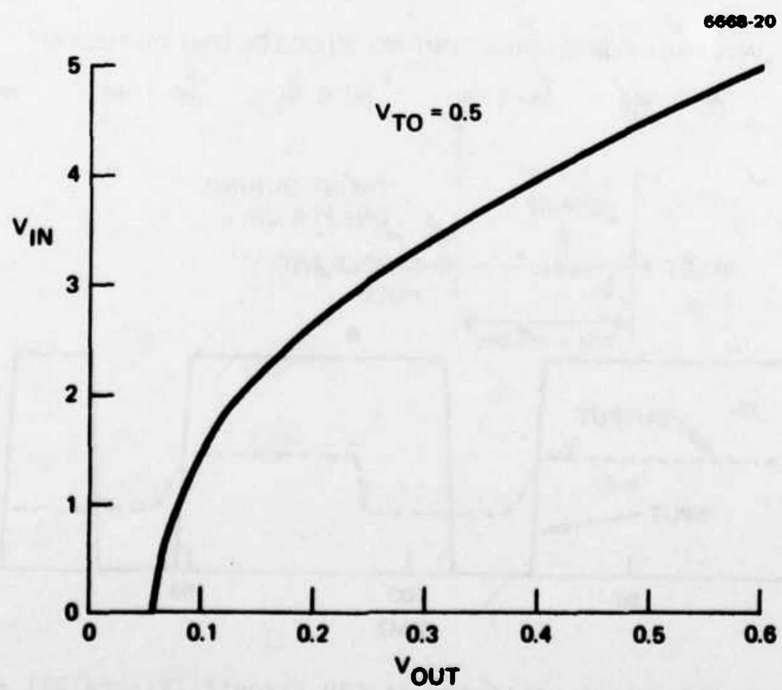


Figure 26. Input-output linearity of CSH circuit for V_{to} = 0.5 V.

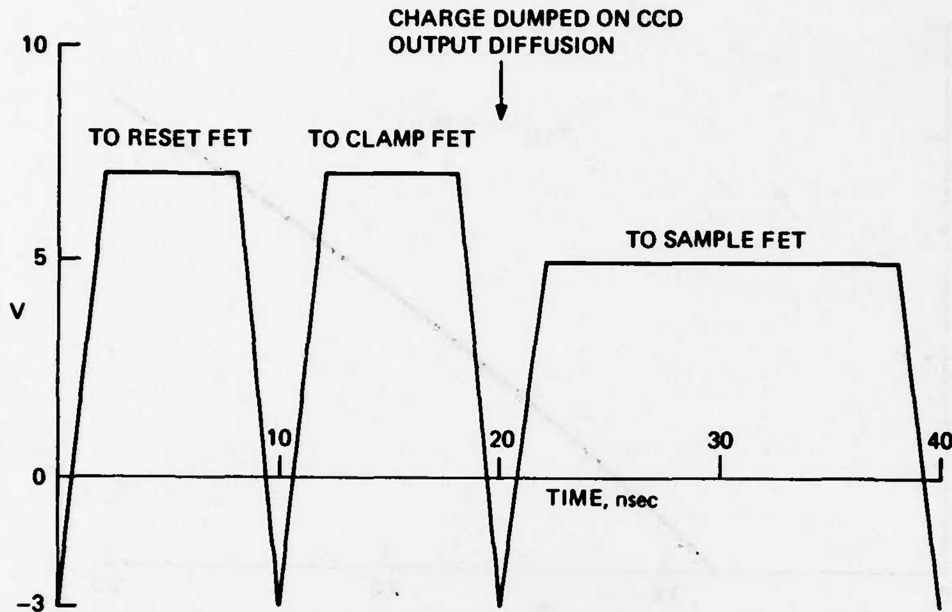


Figure 27. Time sequence of voltages required to operate CSH circuit. One CCD clock period is 40 nsec.

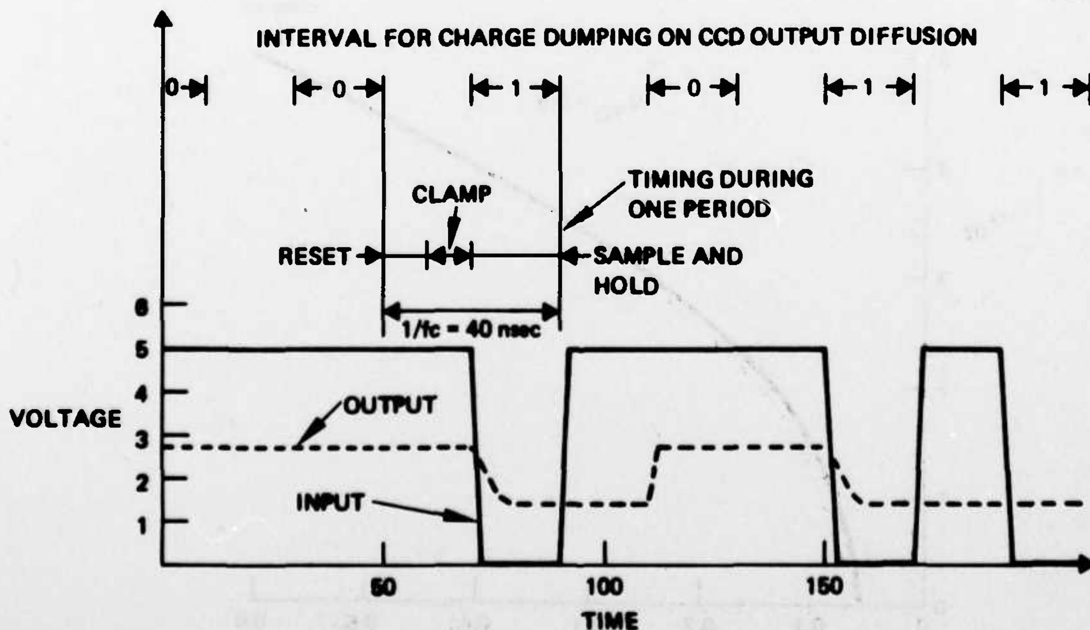


Figure 28. Input and output waveforms of CSH circuit (Figure 21) showing response to full buckets or "1's" (V_{in} = 0) and empty buckets or "0's" (V_{in} = 5). Sample gate is closed before reset occurs. Corresponding CCD clock frequency is 25 MHz.

of the circuit of Figure 21 for V_{to} = -1.75 and 0.5. Here again we see an advantage of a negative turn-on voltage. Figure 27 shows the timing waveforms and voltages required to operate the CSH circuit. Since the slowest stage in the circuit is the last, we felt it desirable to turn on the sample gate immediately after charge is dumped on the input FET. Figure 28 shows typical output transients for a complete clock cycle.

Thus, we have completed the initial phase of computerized circuit simulation in which we examined a number of different CSH circuit configurations and identified processing/design tradeoffs. This phase showed the circuit in Figure 21 will fulfull the detection objectives and that its performance can be improved with negative threshold voltages. These conclusions are regarded as firm because the simulation uses conservative values for the output capacitance load (10 pF), for the maximum drain voltage (5 V), and for the parasitic capacitances. Additional computer simulation efforts are planned that will include velocity-field channel saturation effects on MOSFETs and compare these computerized results with actual MOSFET IV characteristics. We will also determine the variations of gate capacitances (from wafer-to-wafer vibration in polysilicon overetch, gate oxide thickness, etc.) and the effect these variations have on CSH circuit output. It is expected this work will only modify and not change the essential conclusions of the initial phase of computer simulation.

SECTION 7

CONCLUSIONS

As originally outlined for the first phase of this program, several unknowns were to be investigated:

(1) The effect of Ta gaps on electron beam registration

(2) The compatibility of Ta benchmarks with the NIMOX type wafer processing

(3) Methods for high resolution pattern generation in polysilicon and silicon nitride thin films

(4) The amount of underoxidation with nitride masked features

(5) The method of contact metallization for shallow junctions

(6) The design of 100 MHz CSH circuit.

This first phase has clarified or answered each of these technical issues.

For example, with 0.5 μm wide Ta gaps, we found a contrast improvement of 46% was obtainable from the electron beam backscattered signal. We also showed that Ta benchmarks deposited on the nitride and then covered with a CVD layer of SiO_2 will not be affected by the rigors of oxidation, diffusion, etc.

We also developed the aluminum replacement technique for CF_4 plasma etching nitride and polysilicon films. SEM studies showed the nitride etch rate at the aluminum/nitride edge is somewhat slower than fully exposed nitride. This means a nitride shelf is left at the feature outlines unless the wafer is intentionally overetched, in which case the nitride feature dimension and the aluminum mask dimension are equal. Polysilicon, however, undercuts as the etch proceeds, so that the final feature is $\sim$0.3 μm smaller than the mask feature.

Despite no etch undercutting nitride mask features must also be larger than the desired dimension because of underoxidation. By

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studying cleaved samples we determined this amount of underoxidation as a function of pad oxide thickness. For the optimum case nitride features should be 0.55 μm oversize.

To solve the problem of spiking when contacting a shallow junction we chose a sandwich of a polysilicon and aluminum layers to form the metallization. In the contact areas this gives an effective junction depth greater than 0.5 μm, which is sufficient to prevent the aluminum spiking through to the substrate. We have tested over 10^6 μm^2 of contact area without finding a substrate short or contact open.

We have also finished the design of a three-stage CSH circuit and analyzed it with computer simulation programs. This work has showed that tailoring the threshold voltages is a desirable ability to maximize the output, but that a nominal threshold voltage is good enough that the designed circuit will meet the speed objectives for the CSH circuit.

The first phase of the work has thus completed (1) a list of design rules for fabrication, in general, of circuits using the high-resolution NIMOX process, (2) the design of a series of test or diagnostic chips including transistors, capacitors, isolation and continuity testers, leakage monitors, etc., and (3) a list of device performance parameters.

We have also completed several lot runs using the diagnostic chips, and these runs identified several important factors for successful device fabrication. For example, we determined the procedures needed to make 400 Å gate oxides and to form phosphorous-doped polysilicon gates without penetration of the phosphorus into the silicon substrate. We also found that too high an As ion accelerating voltage can give dopant tails in the silicon adversely doping the MOSFET channel region. It was also learned that the appropriate ambient for annealing is important to control junction leakage. These lessons when incorporated into the wafer processing allowed us to successfully manufacture transistors as small as 1 μm long by 1 μm wide and to obtain their IV characteristics.

The one major unresolved problem was control of the field region inversion, apparently due to an inordinately large amount of interface states. These states are being introduced as a result of wafer processing subsequent to the field oxidation, and development work remains to determine and eliminate the source.

In summary, the CSH design appears to be well understood and we are confident it will meet the desired circuit goals, the lithography development required to fabricate the circuit appears in hand, and the practically all the device parameters are being achieved by the wafer processing. This progress is sufficient to start development of the CSH circuit.

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7