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HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS.(U)
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SIXTH QUARTERLY DEVELOPMENT REPORT. no. 6

3 May – 3 Aug 77.

FOR

(6) # HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS.

3 MAY 1977 TO 3 AUGUST 1977

(11) 3 Aug 77

(12) 25 p.

Prepared By
RCA Solid State Divison
Route 202, Somerville, N.J. 08876

For

DEPARTMENT OF THE NAVY
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.

(16) F54586

(15) Contract No. N00039-76-C-0248
Project No. 62762N
Subproject No. XF54586
Task No. 002

(17) XF545864002

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SECTION I

ABSTRACT

Wafer fabrication is proceeding as scheduled. The technology development for platimum sputter etching using gold as the etch mask has progressed sufficiently to allow conversion of the COS/MOS circuits to sputter etching. Reliability data to date obtained on CA741 devices shows a 0.0044% per 1000 hours failure rate at 120°C at the 60-percent confidence level. Copper migration in epoxy packages at 125°C has not been observed as a failure mode. Salt atmosphere resistance tests to date have produced excellent results. All required life-test sockets for Phase II and some of the sockets for Phase III of the program have been ordered.

SECTION II
PURPOSE

The objective of this program is to investigate alternate approaches to MIL-M-38510 for achieving high reliability integrated circuits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve semiconductor reliability which will meet military requirements without a severe cost penalty.

The approach to achievement of the goals of this program will be the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. The program will be carried out in three phases.

Phase I - Completed

(a) Process Feasibility - The required photomasks were generated using existing masks to the maximum extent possible. Then, small quantities of each device type were fabricated to assure that the masks and processes were available for the production runs of Phase II. Also, each device type was fabricated using a matrix of carefully varied process parameters to assess their impact on yields and reliability.

(b) Process Development - The processes required to fabricate the eight integrated-circuit types to be produced in Phase II were defined and documented. Silicon nitride passivation and the titanium-platinum-gold metallization system were used to achieve chip hermeticity and a corrosion-free metallization system. In addition, a silicon nitride overcoat layer was applied for protection of the metallization. A series of experiments was completed at each critical processing step to

assure repeatability. Real-time indicators and accelerated life tests were used to assess the effects of process changes on reliability and to measure progress in achieving the required failure rate.

(c) Automated Assembly - The technology to be used in Phase II was defined and documented. The effect of assembly process parameters on cost and yield was assessed. Bonding tapes and lead-frames compatible with each of the device types were designed and fabricated. A number of devices of each type were assembled using the automated assembly system. Reliability was monitored continually by means of accelerated life tests.

The photomasks, wafer process, and assembly process required to fabricate the eight integrated-circuit types in the low-cost high-reliability device-fabrication phase have been defined and documented and sample devices of each type were fabricated. Additionally, preliminary reliability data have been generated to demonstrate the soundness of the chosen approach.

At this time, the production runs of Phase II have begun.

Phase II - Fabrication

The low-cost high-reliability device fabrication phase of the program will involve significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits will be constructed in both plastic and ceramic packages. This will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes will be defined and documented. The utilization of existing equipment and mask sets will be demonstrated, and the cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions

at wafer probe and final test will be used to monitor the production run and to assure process reproducibility. All devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and asembled.

Phase III - Reliability

The reliability of the devices produced in Phase II will be demonstrated. The conventional aluminum-metallized integrated circuits, packaged and tested to military high-reliability requirements, will be used as the baseline from which to appraise the new process developed under the program. In addition, the level of testing required over and above commercial screening to assure a reliable product for military end use will be determined, and the cost impact of this testing will be analyzed and verified.

SECTION III
PHASE II PROGRAM

Phase II, the low-cost high-reliability device-fabrication phase of the program, will involve significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits will be constructed in both plastic and ceramic packages. This plan will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes will be defined and documented. The utilization of existing equipment and mask[illegible] will be demonstrated, and the cost impact of converting to this t[illegible] processing will be estimated. In-process quality controls, real-[illegible] indicators, and parameter distributions at wafer probe and final test will be used to monitor the production run and to assure process reproducibility. Devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and assembled. The milestone chart for Phase II is shown in Fig. III-1.

As shown in Fig. III-2, the minimum quantity of units required for delivery to the Navy and for the Phase III test plan is 5165 devices per type. Reliability testing during Phase II will require additional units, and other needs will surface during the course of the contract. It is anticipated, therefore, that approximately 10,000 units of each type will be fabricated during Phase II.

In addition to initiating the long-term 125°C life tests during Phase II, a program of accelerated life testing is planned for two circuits,

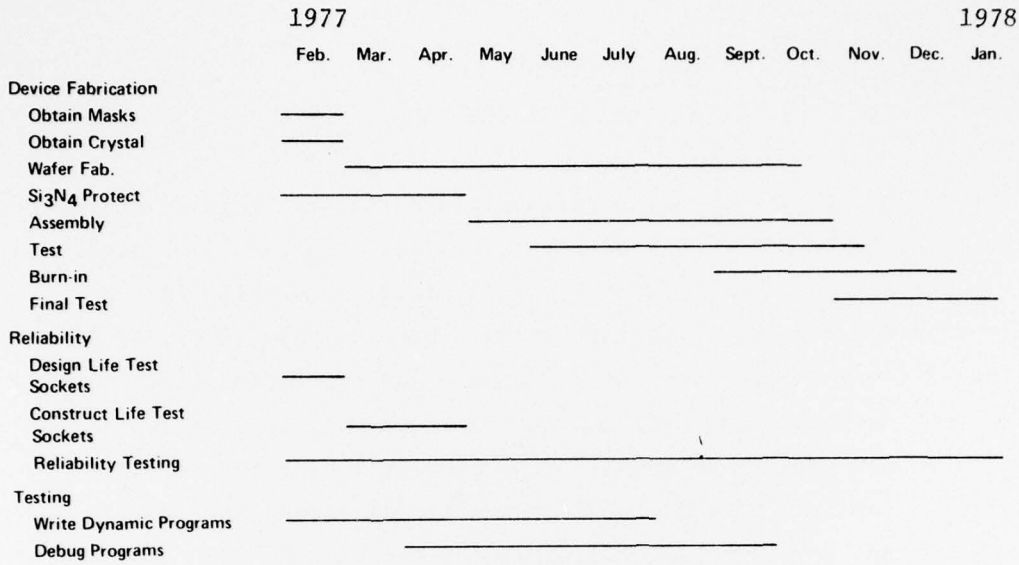

Fig. III-1 - Phase II Milestone Chart

Type	CD4012B	CD4014A	CD4027B	CA741	5420	54S20	5470	5472
Technology	COS/MOS	COS/MOS	COS/MOS	Bipolar Linear	Au-T^2L	Schottky	Au-T^2L	Au-T^2L
Wafer Lot Size	25	25	25	25	25	25	25	25
Net Units Required								
Internal								
Al DIP	115	→						
Al DIC	145	→						
Trimetal DIC	155	→						
Trimetal DIC (Unencapsul.)	25	→						
Trimetal DIP	725	→						
To Be Delivered	4000	→						
Total	5165	→						

Fig. III-2 - Phase II Device Fabrication Plan.

the CA741 and the CD4012B. This program will verify that the reliability goals being met, compare encapsulation techniques, compare the results achieved with devices in dual-in-line ceramic packages, and establish the activation energy to be used for extrapolating the results of accelerated tests. The planned test matrices are shown in Fig. III-3.

Life Tests	Encapsulation Technique				
	Silicone	Epoxy Novolac	Epoxy Novolac With Junction Coat	DIC	Non-Hermetic DIC
Bias					
150°C	20	20	20	15	15
175°C	20	20	20	15	15
200°C	20	20	20	15	15
225°C	20	20	20	15	15
250°C	20	20	20	15	15
Storage					
150°C	15	15	15	10	10
175°C	15	15	15	10	10
200°C	15	15	15	10	10
225°C	15	15	15	10	10
250°C	15	15	15	10	10
Step Stress					
150°C	20	20	20	15	15

Types: CD4012B, CA741

Fig. III-3 - Phase II Test Plan.

SECTION IV

DETAILED FACTUAL DATA

TECHNICAL DISCUSSION

Product Generation

Wafers of all eight integrated-circuit types are currently being processed according to schedule. A by-type status of wafers in the line is shown in Fig. IV-1.

Sputter-Etch Process Development

The sputter-etch process using gold as an etch mask for platinum definition results in the elimination of one metallization photoresist step and in the ability to define closely spaced lines that are typical of large-scale integrated circuits.

The process of sputter etching results in the heating of the silicon wafers. If the temperature rise is not controlled, permanent degradation of the metallization system can occur. A prototype sputter etch system that utilizes a water cooled plate to which the wafers are clamped during etching has been fabricated. COS/MOS circuits have been reproducibly processed using this system, and wafers fabricated under the contract are being processed by use of this technique.

COS/MOS circuits are fabricated by means of processing techniques that yield tapered oxide cuts that are readily adaptable to sputter etching. Bipolar circuits, on the other hand, have relatively steep oxide cuts conducive to the formation of platinum filaments during the sputter-etch process and require increased etch times under slightly different conditions. While bipolar circuits have been successfully fabricated using sputter etching, sufficient data has not been generated to justify the processing of wafers under the contract in this manner.

	TA NO.	DESCRIPTION	ALUMINUM	TRIMETAL
1.	TA10151	5420 DUAL 4-INPUT NAND GATES	AT CKT PROBE	READY FOR METAL
2.	TA10152	54S20 SCHOTTKY DUAL 4-INPUT NAND GATE	AT EMITTER	1/3 AT EMITTER 2/3 AT ISO
3.	TA10153	5470 EDGE-TRIGGERED J-K FLIP-FLOP	READY FOR ASSEMBLY	2/3 AT METAL 1/3 AT B&R
4.	TA10154	5472 MASTER SLAVE J-K FLIP-FLOP	AT CKT PROBE	READY FOR METAL
5.	TA10155	CD4012B COS/MOS DUAL 4-INPUT NAND GATE	READY FOR ALUMINUM	AT GOLD PHOTO
6.	TA10156	CD4027B COS/MOS DUAL J-K FLIP-FLOP	READY FOR ALUMINUM	AT GOLD PHOTO
7.	TA10219	CD4014A COS/MOS 8-STAGE SHIFT REGISTER	READY FOR ALUMINUM	AT GOLD PHOTO
8.	TA10158	CA741 OPERATIONAL AMPLIFIER	READY FOR EMITTER	AT THE METAL STEPS

Fig. IV-1 - Wafer fabrication status.

Hence, bipolar devices will continue to be fabricated by means of the wet etching technique.

A photograph of the work holder of a production sputter-etch system manufactured by Materials Research Corporation is shown in Fig. IV-2. This system is capable of processing twenty-four three-inch-diameter wafers at one time, and is designed so that as one load of wafers is being processed the previous load is being demounted and the succeeding load placed in position.

Reliability Testing

CA741 gold-metallized integrated circuits using plasma silicon nitride protect, automated assembly technology, and silicone molding compound have been subjected to a series of reliability tests.

CA741G 250°C Bias Life

After 1500 hours of 250°C bias-life testing, five failures out of 45 units were observed. Using a 1.1 electron-volt activation energy and a 60-percent confidence level, the failure rate at 125°C is 0.0044% per 1000 hours. A Weibull probability plot for this test indicates that no wear-out mechanism is being exhibited by these devices and that the mean time to failure at 250°C is 40,000 hours. This plot is shown in Fig. IV-3.

CA741G Sequence Testing

A group of tests designed to determine the resistance of the CA741G to salt atmosphere was run.

Devices with plasma deposited silicon nitride overcoat and assembled using beam-tape bonding were compared to devices using CVD PSG overcoat and wire bonding. The tests consisted of exposing the devices to 48 to 96

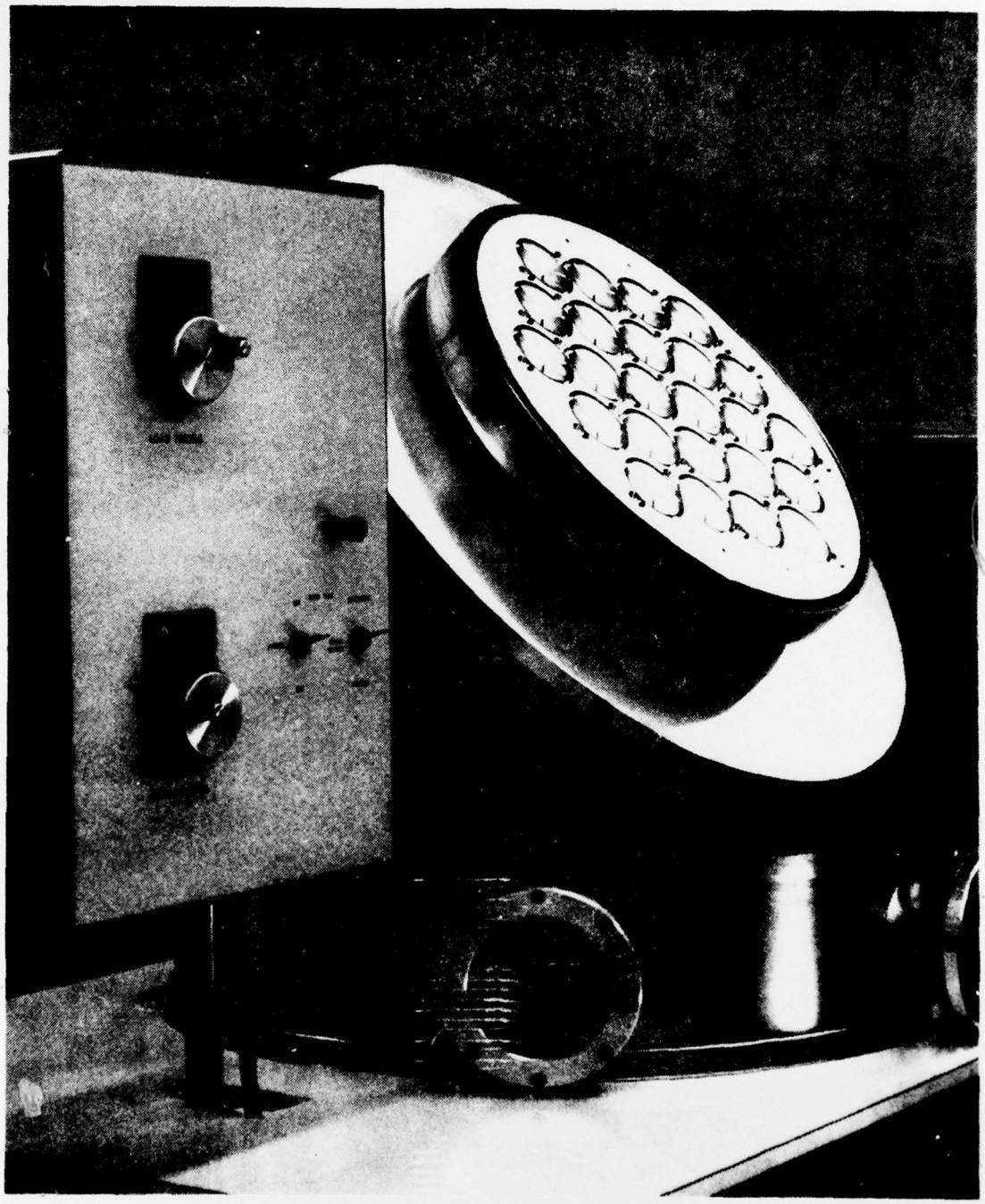

Fig. IV-2 - Sputter-etch process work holder.

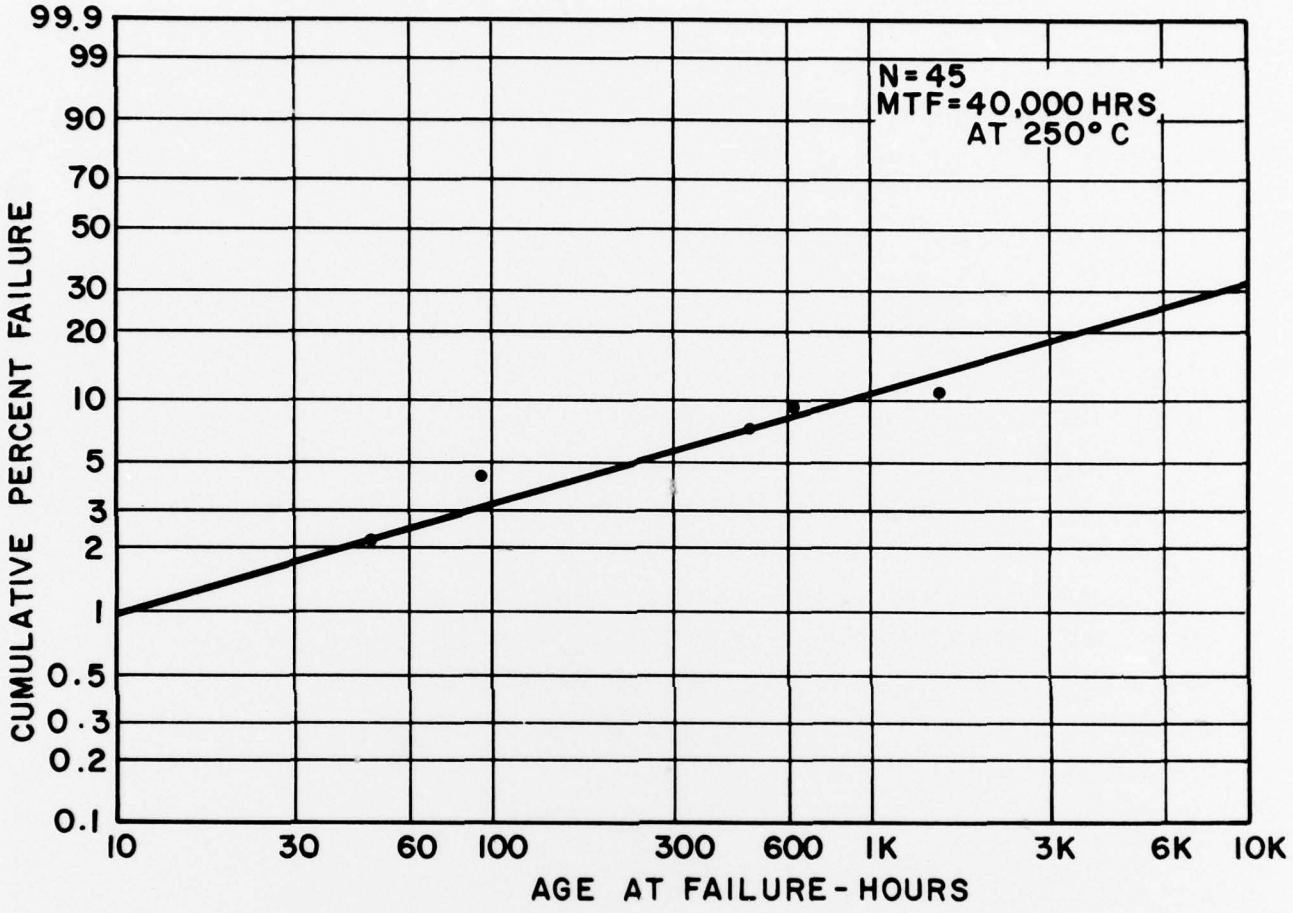

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Fig. IV-3 - Weibull probability chart, CA741G 250°C bias life test.

hours of salt atmosphere (MIL 883, Method 1009.1) followed by either 85°C/85% RH bias or pressure cooker testing (30 PSIA, 121°C) and 85°C/85% RH bias testing. The excellent salt resistance of the silicon nitride protected beam-tape bonded devices demonstrated by these tests is shown in Fig. IV-4.

Investigation of Copper Migration Failure Mechanism

Copper dissolution and redeposition has been reported earlier as a failure mechanism at temperatures exceeding 200°C in the presence of epoxy molding compounds. This phenomenon is believed to be caused by chemical changes that occur in the molding compound at elevated temperatures. In order to confirm that this is not a failure mechanism at normal operating temperatures, extended operating life tests using the CA3046G transistor array are being conducted at T_A = 125°C (T_j = 155°C). After 3500 hours (196,000 device hours) zero failures related to copper migration have been observed. If a 1.1-eV activation energy for this phenomenon is assumed, failure at 960 hours would be predicted. This test is continuing.

Step Stress Testing CA741 & CD4012B

The required CD4012B and CA741 units have been assembled for step stress testing. Data will be obtained during the next reporting period.

Status of Life-Test Sockets

Orders have been placed for all of the necessary life-test sockets for Phase II of the program. An updated summary of life-test socket status is shown in Fig. IV-5. In order to fulfill the obligations of Phase III of the contract, it will be necessary to order additional sockets. The additional requirements for Phase III are summarized in Fig. IV-6.

SEQUENCE TEST SUMMARY

TYPE	PROTECTIVE LAYER	ASSEMBLY	MOLDING COMPOUND	TEST	RESULTS
CA741G	PSG	WIRE BOND	SILICONE	96HOURS SALT ATMOSPHERE (METHOD 1009.1)	0/10
				+	
				336HOURS 85°C/85% RH BIAS LIFE	3/10
CA741G	PLASMA Si_3N_4	AUTO DIP	SILICONE	96HOURS SALT ATMOSPHERE	0/25
				+	
				48HOURS PRESSURE COOKER (30 PSIA, 121°C)	0/24
				+	
				168HOURS 85°C/85%RH BIAS LIFE	1/24 (1)
CA741G	PLASMA Si_3N_4	AUTO DIP	SILICONE	48HOURS SALT ATMOSPHERE (Method 1009.1)	0/12
				+	
				1000HOURS 85°C/85%RH BIAS LIFE	0/12
CA741G	PLASMA Si_3N_4	AUTO DIP	SILICONE	96HOURS SALT ATMOSPHERE (Method 1009.1)	0/43
				+	
				GP 1: 85°C/85%RH BIAS LIFE GP 2: 250°C BIAS LIFE GP 3: PRESSURE COOKER + 85°C/85%RH BIAS LIFE (2)	

1. 1 UNIT LOST DUE TO LEAD CORROSION AFTER PRESSURE COOKER. 1 UNIT CRACKED AFTER 85°C/85% RH BIAS LIFE TEST
2. TESTS IN PROGRESS.

Fig. IV-4 - Sequence test summary.

TYPE	LIFE TEST	ORDERED	RECEIVED	SCHEDULED DELIVERY
CA741	125°C OPERATING	189	108	8/26
	125°C BIAS	216	234	COMPLETE
	85°C/85% RH BIAS	48	48	COMPLETE
	175°C BIAS	96	96	COMPLETE
	150°C BIAS	81	90	COMPLETE
	200°C BIAS	48	48	COMPLETE
	250°C BIAS	240	0	9/16
CD4012B	125°C OPERATING	132	54	8/19
	125°C BIAS	184	54	8/19
	85°C/85% RH BIAS	48	48	COMPLETE
	175PC BIAS	104	96	COMPLETE
	200°C BIAS	48	48	COMPLETE
	250°C BIAS	240	0	9/1
	150°C BIAS	104	104	COMPLETE
5420	125°C OPERATING	126	130	COMPLETE
	125°C BIAS	170	168	COMPLETE
	250°C BIAS	48	48	COMPLETE
CD4027B	125°C OPERATING	182		9/2
	125°C BIAS	182		9/2
CD4014A	125°C OPERATING	182		9/2
	125°C BIAS	182		9/2
54S20	125°C OPERATING	182		9/9/
	125°C BIAS	182		9/9
5470	125°C OPERATING	182		9/16
	125°C BIAS	182		9/16
5472	125°C OPERATING	182		9/23
	125°C BIAS	182		9/23

Fig. IV-5 - Status of life-test sockets for Phase II.

Type	Life Test	Additional Sockets Required
CA741	50°C/85% RH Bias	35
	250°C Bias	56
CD4012B	50°C/85% RH Bias	35
	200°C Bias	26
	125°C Operating	68
5420	85°C/85% RH Bias	55
	50°C/85% RH Bias	35
	200°C Bias	70
	250°C Bias	56
	125°C Operating Life	70
	175°C Bias	100
CD4027B,CD4014A		
54S20,5470	85°C/85% RH Bias	55
5472	50°C/85% RH Bias	35
	85°C Bias	43
	175°C Bias	100
	200°C Bias	70
	250°C Bias	80

Fig. IV-6 - Additional Life-Test Sockets Required for Phase III.

Flow Charts For The Phase II Program

A wafer process flowchart comparing the high-reliability low-cost technology for COS/MOS and bipolar circuits with standard aluminum technology is shown in Fig. IV-7.

A detailed flowchart for assembly of Phase II product is shown in Fig. IV-8.

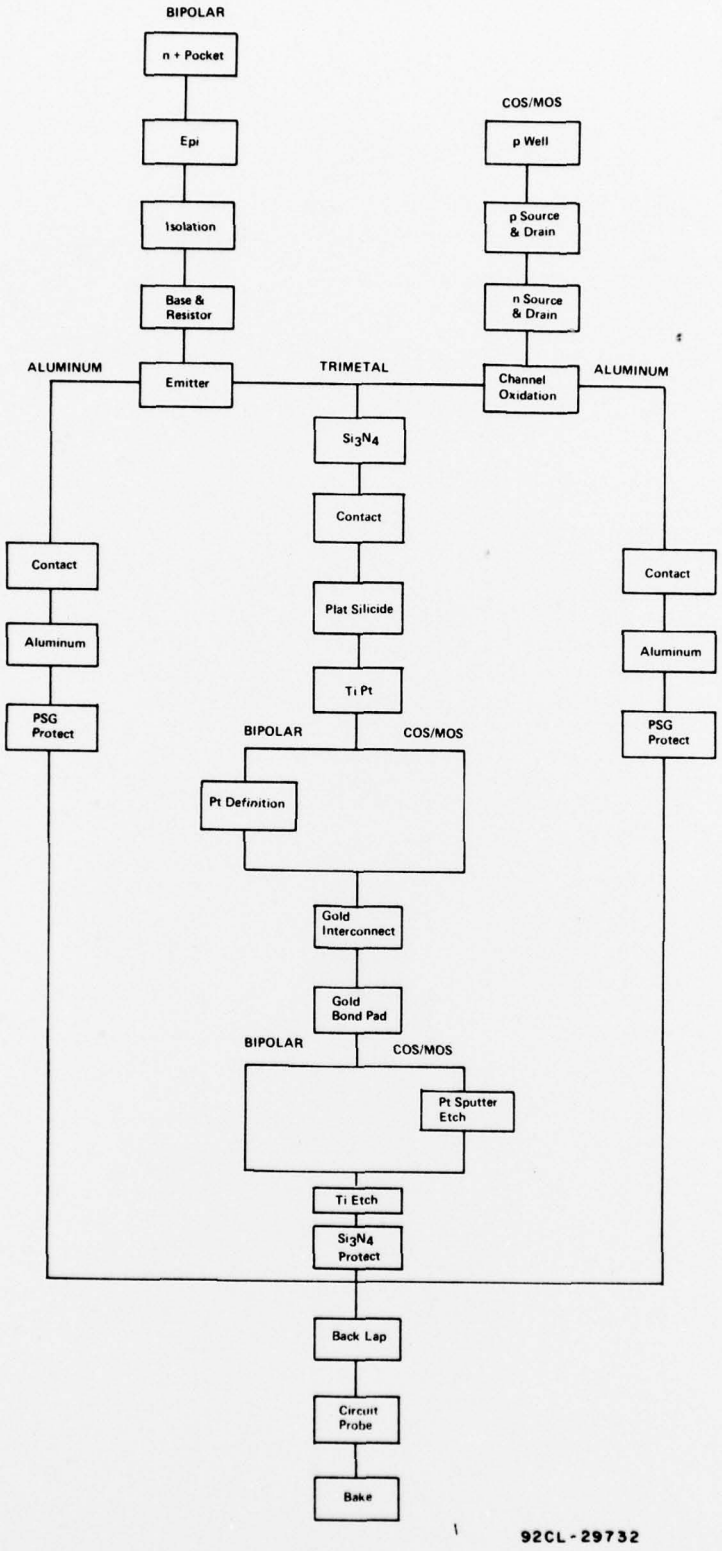

Fig. IV-7 - Wafer-process flowchart for basic bipolar and COS/MOS types.

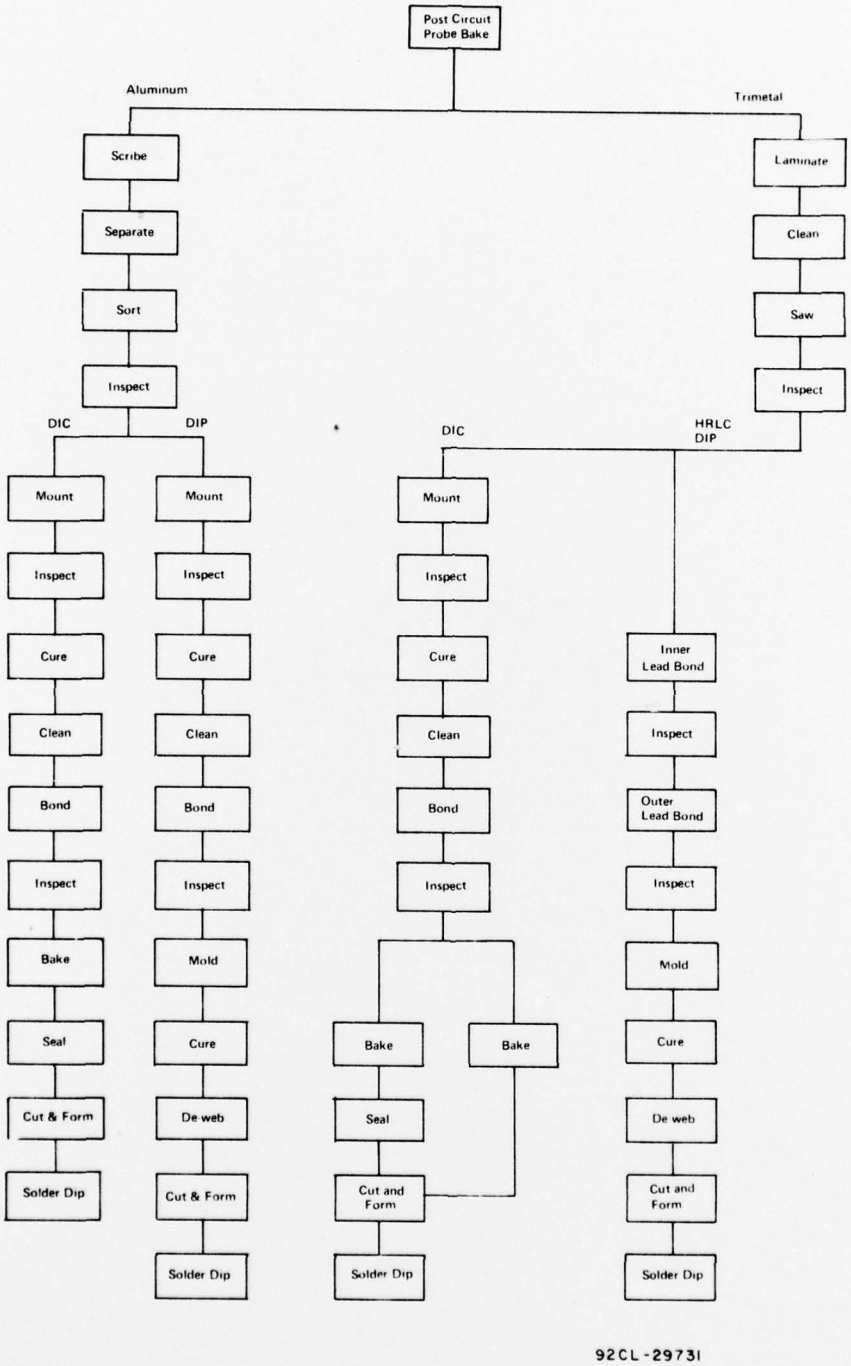

Fig. IV-8 - Detailed assembly technology flowchart for Phase II program.

SECTION V

TECHNICAL PRESENTATIONS RELATED TO CONTRACT TECHNOLOGY

Structural Aspects of Beam Tape Bonding By A.S. Rose, F.E. Scheline, and T.V. Sikina.

Presentation was made at NEPCON EAST, May 17, 1977, Philadelphia, Pa.

Metallurgical Considerations for Beam Tape Assembly By A.S. Rose, F.E. Scheline, and T.V. Sikina.

Presentation was made at the 27th Electronic Components Conference, May 16, 1977, Arlington, Va.

On June 23-24, 1977 presentations were made to four major military groups to review the first year technical performance of the contract. The presentations were in Washington, DC by H. Khajezadeh and A.S. Rose to:

1. NAVELEX
2. Strategic Systems Program Office (Trident - SPO)
3. Navy Material Command
4. Pentagon - DDRTE

On July 8, 1977, a presentation relating to chips on tape technology was made by A.S. Rose to Jet Propulsion Laboratory, Pasadena, California.

A similar presentation was made by A.S. Rose on July 18, 1977 to Lockheed Missile and Space Corporation, Sunnyvale, California.

SECTION VI

CONCLUSIONS

1. The required Phase II wafer-fabrication program is on schedule.
2. Technology development has resulted in the conversion of COS/MOS types to platinum sputter etching.
3. Preliminary reliability data generated by using the CA741 shows what the required 0.005%/1000 hours failure rate at 125°C can be met.
4. Reliability data on salt-atmosphere testing is excellent.
5. Copper migration in epoxy at 125°C has not shown up as a failure mode after 3500 hours of test.

SECTION VII

PLANS FOR THE NEXT INTERVAL

1. Continue wafer fabrication.
2. Continue reliability testing of CA741 and CA3046.
3. Initiate the step-stress testing program for the CA741 and CD4012B devices.
4. Establish baseline costs for comparison of HRLC product to commercial high-reliability plastic product.

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