Thin Film Hybrid Microcircuitry

Part II. Modulator Circuit for an Experimental Fuze

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HDL-TM-77-24—*Thin Film Hybrid Microcircuitry Part II. Modulator Circuit for an Experimental Fuze.*
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This work consisted of the development of a thin film hybrid version of a specialized modulator circuit that had some very stringent requirements. The scheme that was followed used tracings of the outlines of resistors and conductors; also, templates were used to represent add-on devices to permit easy trial of a number of alternative layouts. Computerized thermal analyses were used to determine steady-state component temperatures before

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adopting the final circuit design. Standard thin-film processing methods were used to fabricate and package the circuits. A number of materials were tried in attempts to encapsulate the circuits for protection during temperature cycling. An encapsulating procedure using flexibilized epoxies was developed that eliminated circuit failures that appeared to be caused by encapsulation stresses. Further work needs to be done on circuit failures at elevated temperatures that are thought to be caused by corrosion or degradation of the aluminum metallization on silicon chip devices.

CONTENTS

FIGURES

1. INTRODUCTION

A three-stage segment of an experimental fuze circuit was selected as the subject for development of a thin film hybrid circuit. Included in this segment was a highly specialized modulator circuit (fig. 1) that provided modulation for the transmitter output (to forestall countermeasures). Due in part to this specialization, the following very stringent requirements were imposed upon the circuit:

(a) Maximum circuit size to be 2.54 × 5.08 × 0.254 cm

(b) A ±1-percent tolerance on certain resistors

(c) A ±2-percent tolerance on certain capacitors

(d) Total circuit power dissipation of some 5.5 W excluding element Q5, which must be mounted separately with a heat sink

(e) Temperature stability of circuit sufficient to meet electrical specifications over the temperature range from -31.7 to 57.2°C

(f) Circuit input and output must be at opposite ends of substrate to facilitate connection to adjacent circuitry

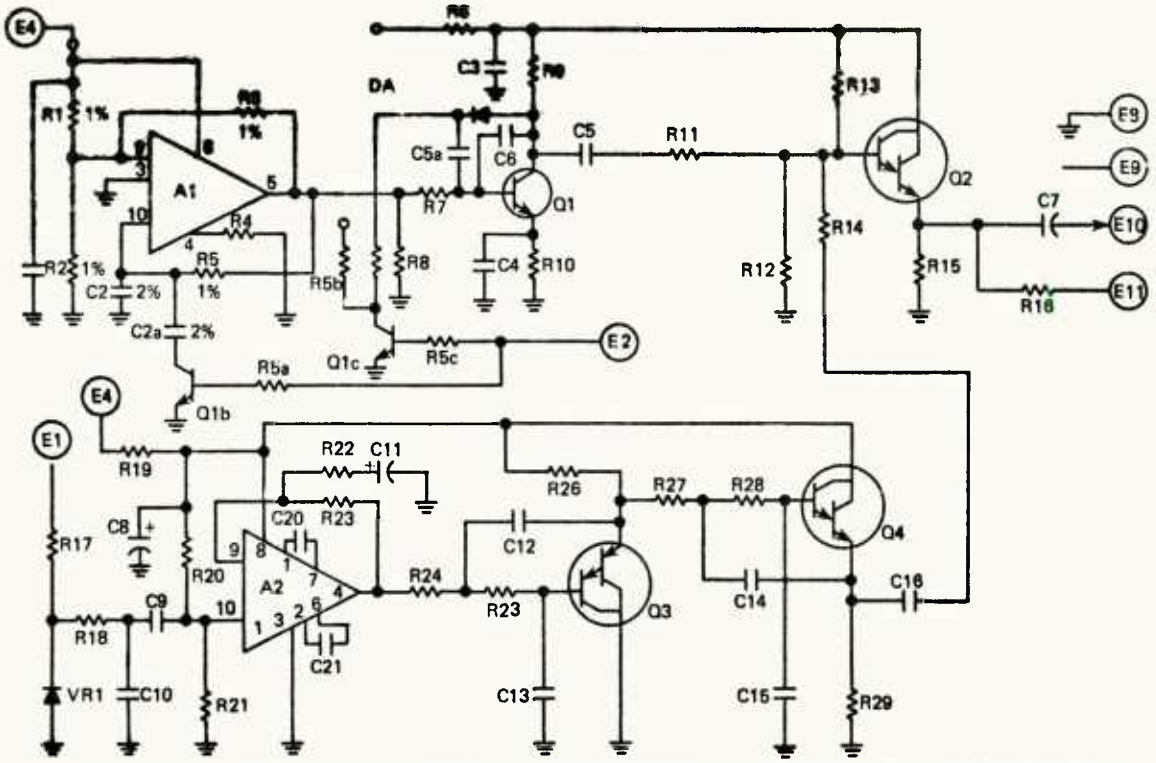

Figure 1. Schematic diagram of modulator circuit to be fabricated by methods of thin film hybrid technology.

These requirements provided a stern test for the methods of thin film hybrid technology.

2. PROCEDURE

2.1 Circuit Layout

Templates of all add-on components were made up at a 20:1 scale so that a number of alternative layouts could readily be tried. The preliminary layouts were made on clear plastic film backed with a piece of coordinate paper so that various thin film conductor and resistor configurations could be tried simply by drawing the outlines with a grease pencil (fig. 2). Resistor area determinations were based upon design rules[1] relating the minimum line widths to allowable power densities. Typically, for a resistor metallization with a sheet resistance of 100 ohms per square on a glazed ceramic substrate, the maximum allowable power density is 6.2 W/cm^2. If these data are used to calculate the minimum line width permissible for a resistor that dissipates 0.004 W and has a 15-kohm total resistance value,

$$R_T = 15\ K\Omega,\ P - 0.004\ W\ .$$

Minimum resistor area

$$A = \frac{0.004\ W}{6.2\ W/cm^2} = 6.45 \times 10^{-4}\ cm^2$$

Total number of squares,

$$n = \frac{\ell}{w}\ .$$

Since $A = \ell \times w$,

$$n = \frac{\ell}{w} = \frac{\ell \times w}{w^2} = \frac{A}{w^2}\ .$$

[1] *M. R. Zyetz, Fundamentals of Thin Film Microcircuit Design and Manufacture, Industrial and Scientific Conference Management, Inc., Chicago, IL, 7.4.3A (1970).*

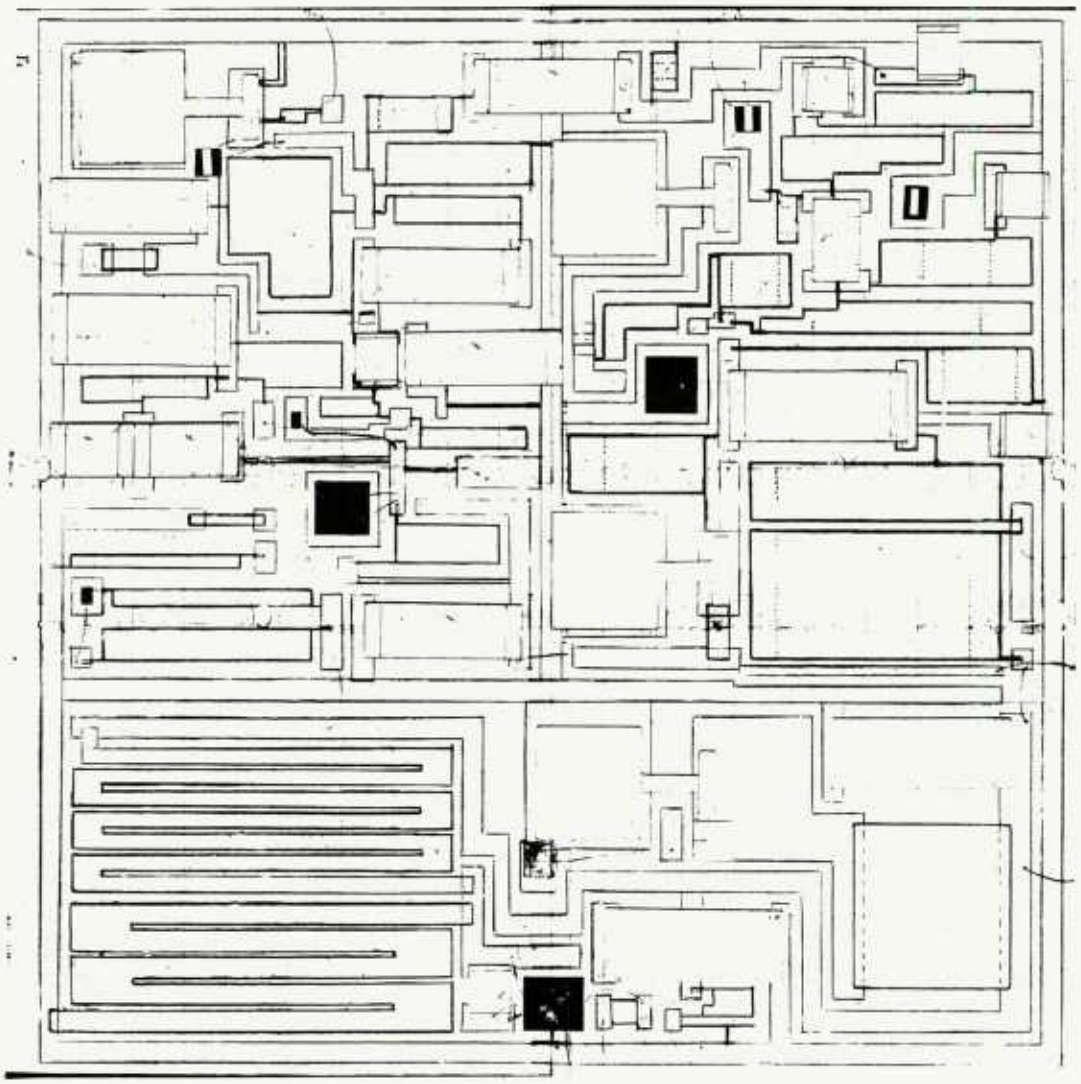

Figure 2. Preliminary layout of modulator circuit with resistors and conductors outlined on plastic film and templates of add-on components attached.

The total number of squares is also given by

$$\frac{R_T}{R_{sh}} = \frac{15000}{100} = 150$$

Equating the two expressions for the total number of squares,

$$\frac{A}{w^2} = \frac{6.45 \times 10^{-4}\ cm^2}{w^2} = 150 ,$$

$$w^2 = \frac{6.45 \times 10^{-4}\ cm^2}{150} = 4.3 \times 10^{-6}\ cm^2 ,$$

$$w = 2.07 \times 10^{-3}\ cm^2 ,$$

$$w \simeq 0.02\ mm .$$

Minimum resistor line width, w = 0.02 mm

where

R_T = total resistance

R_{sh} = sheet resistance

ℓ = length of resistor line

w = width of resistor line

Similar calculations were performed for all the circuit resistors and a compromise value of 0.064 mm, which is somewhat larger than any calculated, was selected for the general resistor line width to conform with the recommended circuit design practice of a common line width for all resistors.[1] To compensate for line width reduction during etching, an allowance was made in the resistor lengths based upon previous observations[2] of an average 0.013-mm reduction of a 0.064-mm line. The actual lengths of the resistors were computed as follows:

$$\frac{\ell_{actual}}{w_{actual}} = \frac{\ell_{calc}}{w_{design}}$$

$$\ell_{actual} = \frac{w_{actual}}{w_{design}} \times \ell_{calc} = \frac{0.064 - 0.013}{0.064} = 0.80\ \ell_{calc} .$$

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[1] *M. R. Zyetz, Fundamentals of Thin Film Microcircuit Design and Manufacture, Industrial and Scientific Conference Management, Inc., Chicago, IL, 7.4.3A (1970).*

[2] *A. J. Edwards, Thin Film Hybrid Microcircuitry, Part I; Boxcar Circuit for a Current HDL Fuze System, HDL-TM-73-10 (1973).*

Thus, all resistor lengths were laid out to be only 80 percent of the calculated lengths. By using all these design considerations, we tried several alternative layouts before tentatively adopting a particular configuration that included the entire circuit on a 2.54 × 2.54 cm substrate.

2.2 Thermal Analysis

Due to the extremely high power dissipation of the circuit, it was deemed necessary to determine if the circuit elements would overheat before a final design was adopted. A computer program[3] was obtained for determining the steady-state temperature distribution on substrates and integrated circuit chips. This program, "Thermal Analysis of Substrates and Integrated Circuits," was adapted for use on the Harry Diamond Laboratories (HDL) IBM 7094 computer. The program uses a Green's function approach to the solution of Poisson's equation:

$$\frac{\delta^2\theta}{\delta x^2} + \frac{\delta^2\theta}{\delta y^2} + \frac{\delta^2\theta}{\delta z^2} = - \frac{Q(x,y,z)}{K} ,$$

where

$\theta = T(x,y,z) - T_{ambient}$

Q = source strength

K = thermal conductivity

The inputs to the program are

A = x-length of substrate

B = y-length of substrate

C = z-length of substrate

TC = thermal conductivity of substrate

H1 = film coefficient of circuit side of substrate

[3] *V. L. Heinz and V. Lenzi, eds., Thermal Analysis of Substrates and Integrated Circuits, Proceedings, 1969 Electronic Components Conference (1969), 166-177.*

H2 = film coefficient of back side of substrate

NS = number of sources

NB = number of leads

TO = lead sink temperature

TAMB = ambient temperature

XS(I) = x-coordinate of i^{th} source

YS(I) = y-coordinate of i^{th} source

DX(I) = x-length of i^{th} source

DY(I) = y-length of i^{th} source

Q(I) = power generated by i^{th} source

The inputs for the layout that was tentatively adopted were entered into the computer program (assuming a 50°C ambient temperature) and the resulting computed, steady-state temperature ranged from 130 to 270°C (fig. 3, p. 11). These temperatures were clearly unacceptable in that they could cause active devices to exhibit intrinsic conductivity. Consultations were held with the HDL circuit designers and it was suggested that components R34, VR2, and C20 be disconnected on the substrate and external discrete components be substituted. These changes removed the two highest power dissipating components and yet allowed retention of the initial layout. A computer thermal analysis of this revised layout (again assuming a 50°C ambient temperature) resulted in computed temperatures of 86 to 137°C (fig. 4, p. 12). This temperature range, while a bit high, is considered acceptable. Nonetheless, the circuit designers thought it best to revise the circuit again by removing the entire voltage regulator from the substrate and reducing the substrate size to 2.54 × 1.27 cm. The thermal analysis of this revised circuit resulted in computed temperatures ranging from 90 to 120°C (fig. 5, p. 13). These temperatures correspond to those frequently required by joint Army-Navy specifications and are thought to be completely acceptable.

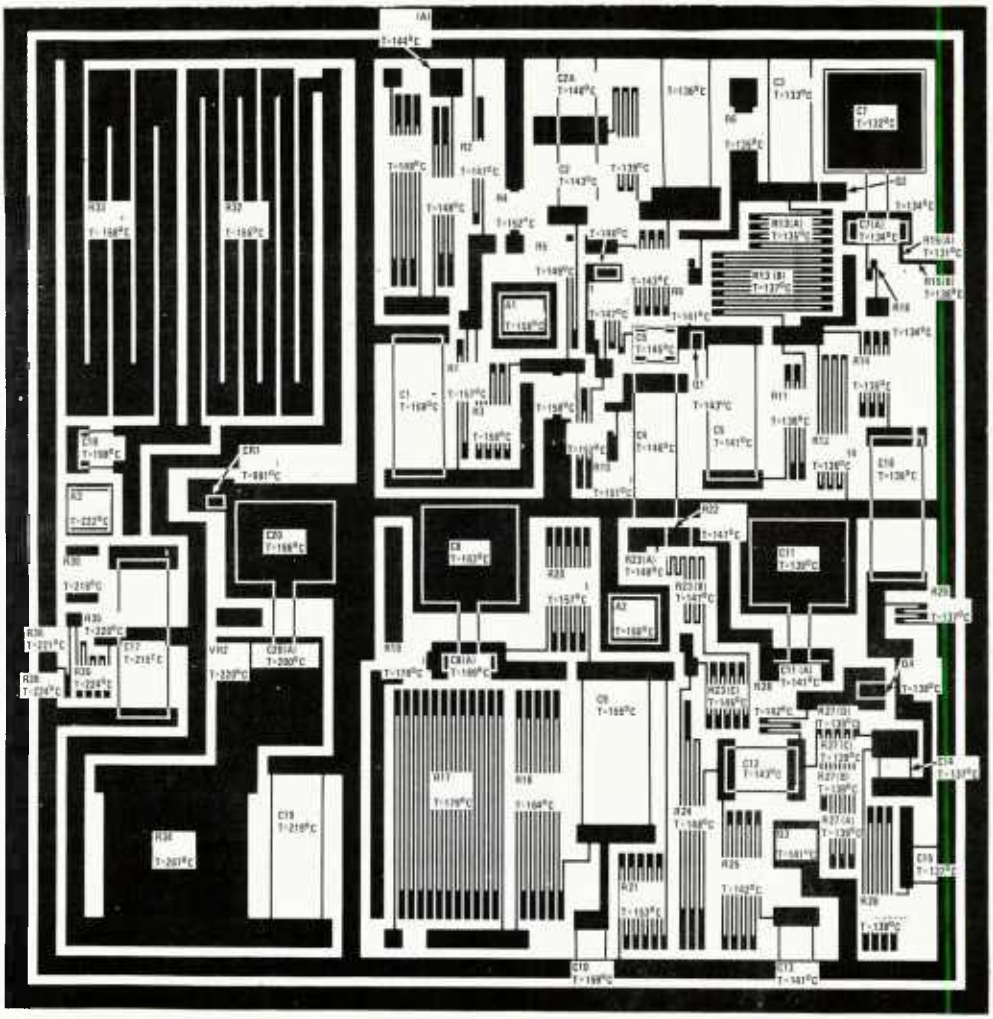

Figure 3. Detailed layout of thin film hybrid version of modulator circuit with steady-state temperatures, as determined by computerized thermal analysis, superimposed on components.

2.3 Artwork Generation

The layouts were used as models for detailed drawings of the final design of the circuit. To aid the draftsman, the coordinates of the start and end points of the conductor and resistor patterns were listed. The detailed drawings were then used as guides to produce the primary artwork on rubylith film by tracing on a coordinatograph. Finally, two-step photoreduction was used to produce the working negatives.

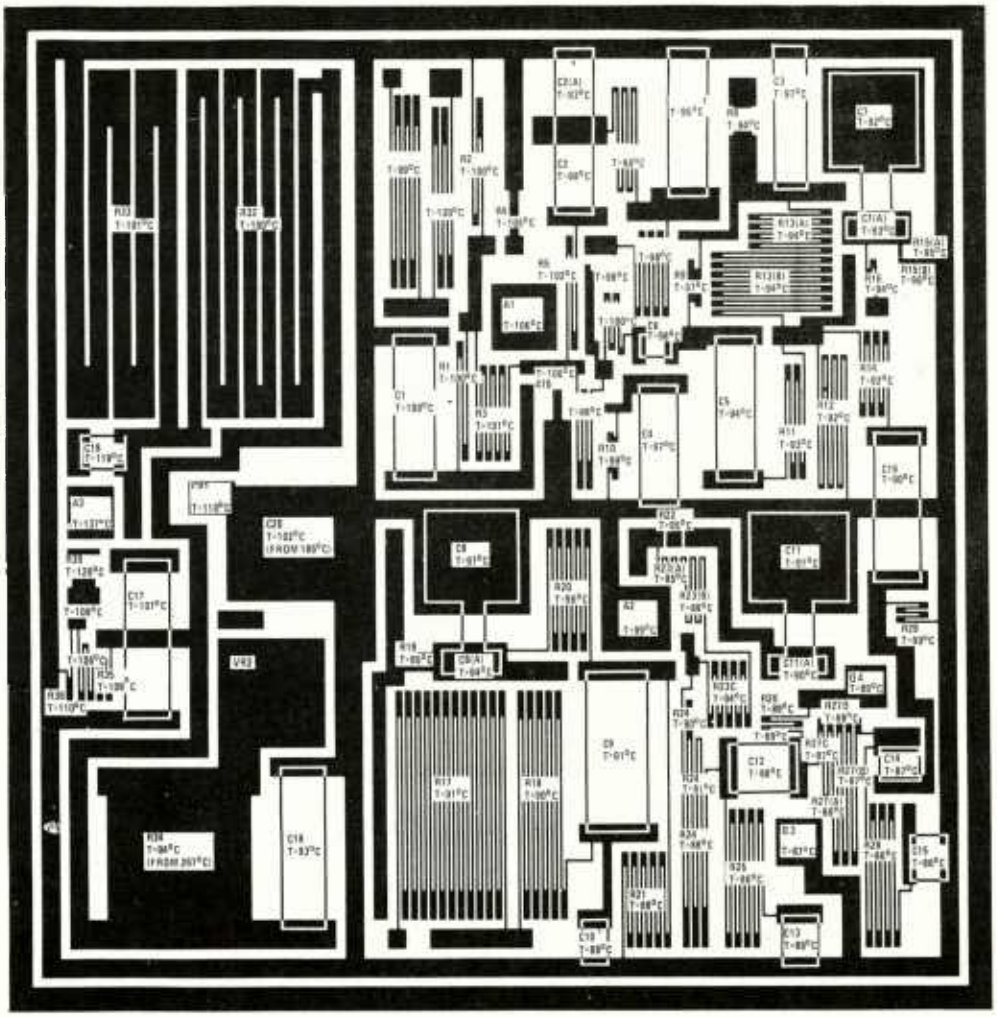

Figure 4. Results of computer thermal analysis of revised modulator circuit with component temperatures indicated.

2.4 Production of Metallization

In order to achieve the required temperature stability, nichrome was used as the thin film resistor material. The original and first revised layouts were for 100 ohms per square resistor metallization (thickness ≈20 nm), while the second revised layout was for 200 ohms per square resistor metallization (thickness ≈15 nm). Metallizations of each value were both produced in-house and purchased from commercial sources to assure a ready and adequate supply. The resistor metallization produced in-house was deposited onto ceramic substrates held at 250°C. Both glazed ceramic substrates (surface

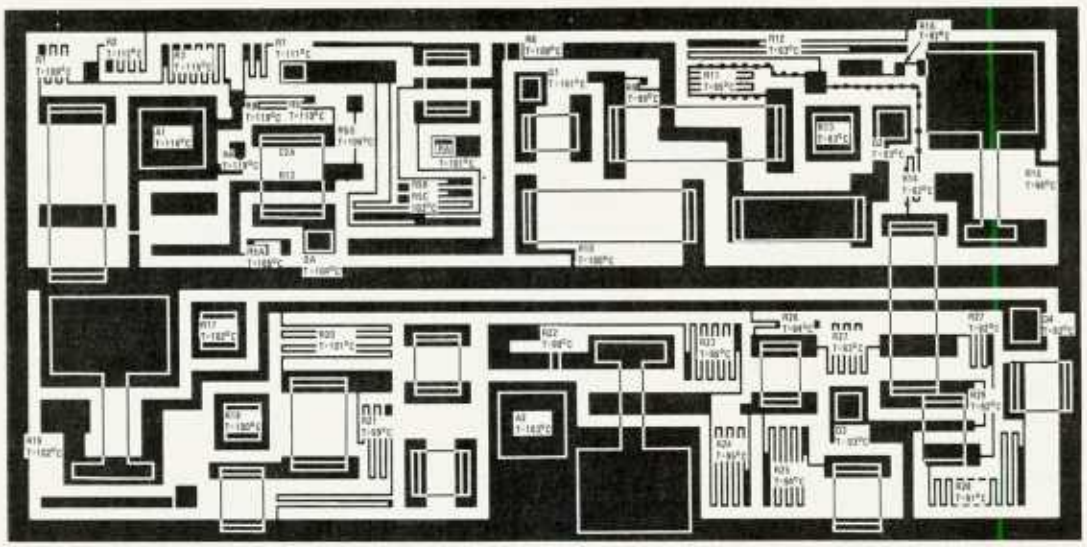

Figure 5. Results of computer thermal analysis of second revision of modulator circuit, with component temperatures indicated.

finish <25 nm center line average--CLA) and as-fired ceramic substrates (surface finish ±75 nm CLA) were used. We deposited the metallization to a sheet resistance 80 percent of the design value, as is customary, intending to adjust the resistor values in a later stabilization operation. The gold conductor layer was then deposited to a thickness of 2000 nm while the 250°C substrate temperature was maintained. This composite was then annealled by holding it at 250°C for an additional hour. The purchased resistor metallization also had a sheet resistance that was 80 percent of design value. The gold conductor layer, however, was produced by electroplating up a sputter-deposited film to a total thickness of 6250 nm. Both the in-house and the commercially produced metallizations were subsequently processed, with equal facility, to produce the desired circuit patterns.

2.5 Photolithography

The recommended procedure[4] was followed: etching through both the conductor and resistor layers initially and then applying a second photoresist pattern for the etching of the conductor layer from the resistor elements. The gold conductor layer was etched with a sodium

[4] *R. W. Berry et al, Thin Film Technology, D. Van Nostrand Co., Inc., Princeton, NJ (1968), 653-655.*

cyanide solution and the nichrome resistor layer was etched with a solution containing ceric hydrogen sulfate. Some of the purchased metallization was processed by Scope Electronics, Inc., where a negative photoresist was used. Both purchased and in-house-produced metallizations were processed at HDL where Shipley AZ 1350 positive photoresist was used. Initially, some difficulties were experienced due to the degradation of the positive photoresist in the caustic sodium cyanide solution. The difficulties were overcome by warming the cyanide solution, thereby increasing the etching rate and decreasing the time that the photoresist was in contact with the solution. Measurements of resistor line widths on circuit patterns etched both in-house and at Scope Electronics, Inc. indicated diminutions in width averaging 0.013 mm.

2.6 Resistor Adjustment and Stabilization

Since the sheet resistance of the resistor metallization was 20 percent below design value and the lengths of all resistors were 20 percent shorter than the calculated values, the measured values of all resistors were generally well below design value. Standard practice is to adjust these values upward by heating the circuits in air to oxidize the surfaces, thereby decreasing the thicknesses of the resistive film. The rate of oxidation has an exponential dependence on both temperature and time, with the temperature dependence being much stronger. Ideally, the temperature used is the highest feasible that will cause the resistance to increase controllably without overshooting. This practice stabilizes the films against further oxidation at lower temperatures, even for prolonged periods of time. A temperature of 375°C was used for these circuit patterns, and, by monitoring one of the 1-percent tolerance resistors, it was found that the resistors on the unglazed ceramic substrates were adjusted to value within 10 to 15 min. The resistors of the circuit patterns on glazed ceramic substrates could not be adjusted because of a reaction between the resistor metallization and the glaze. The reaction is thought to be an attack on the metal by the caustic contained in the glaze, resulting in discontinuous (open) resistor films. Allowances had to be made for the difference between the resistance at the elevated temperature and at room temperatre in the adjustment of the resistor values. The practice followed was to assume a temperature coefficient of +100 ppm/°C (10^{-4}) for the resistor metallization of the first circuit pattern adjusted from each run. The target resistance by which the adjusting process is monitored is thus calculated:

$$R_T = R_o \left[1 + 10^{-4} \ (375 - 25)\right]$$

$$R_T = 1.04 \ R_o \ .$$

The true temperature coefficient of resistance is then calculated from the results of the first circuit pattern from each run and is used, or adjusted if need be, for calculating the target resistance values for subsequent circuit patterns from the same run.

After the adjusting process, all the resistors on the substrate were measured and tabulated. If the precision resistors were below tolerances, further adjustment by air oxidation was performed. If the precision resistors were within tolerances, any necessary adjustment to the other resistors was made by laser trimming to increase the resistance value, or by short circuiting a segment by wire bonding to decrease the resistance value.

2.7 Assembly

The chip devices (integrated circuits, transistors, capacitors, and resistors) were attached to the substrate metallization with silver-bearing conductive epoxy (E-Solder #3012). The substrates were then attached to platform case headers with nonconductive epoxy (Epon 815), and both epoxies were cured by being held at 125°C for 6 hr. The last step in the fabrication was wire bonding to the appropriate device and metallization pads and to the platform header lead-out pins. The circuits assembled in-house were thermocompression wire bonded with 0.025-mm-diam gold wire, while those assembled by Scope Electronics, Inc. were ultrasonically wire bonded with 0.025-mm-diam aluminum wire. Upon completion of the wire bonding, the circuits (fig. 6) were finished and ready for testing.

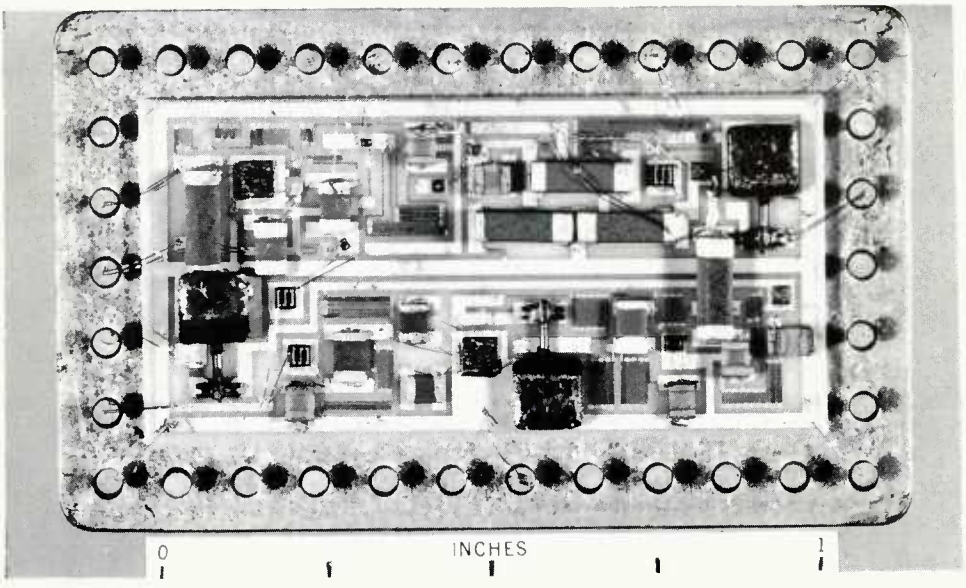

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Figure 6. Completed thin film hybrid modulator circuit mounted on platform case header.

2.8 Testing, Trouble-Shooting, and Adjusting

We tested the circuits by applying the appropriate supply voltages to them and observing the outputs on an oscilloscope. When malfunctions occurred, the circuits were probe tested and the signals traced to the location of the problem. After a minimum of trouble-shooting and rework, most circuits were made to function properly. The outputs of the triangle generator and the noise generator were then adjusted to the desired amplitudes and amplitude ratio. The output resistors of both the triangle-generator and the noise-generator stages had to be adjustable to permit adjustment of the absolute amplitude of each output and the ratio of these amplitudes. Initially, minimum values of each output resistor had been determined and the remainders of the resistor lengths, beyond that necessary to give these minimum values, had been short circuited by "stitch" wire bonding. The values of each output resistor could then be incrementally increased to obtain the desired amplitude and ratio by removing the required number of stitches. The procedure followed was to short circuit the noise diode, thus removing the noise-generator output and to set the triangle-wave amplitude slightly above the desired value by adjusting resistor R11 as previously described. The triangle generator output was then removed and the noise amplitude was set slightly above the desired value by adjusting resistor R14. By alternately adjusting resistors R11 and R14, the desired amplitudes and amplitude ratios were obtained.

The circuits were then submitted to the HDL circuit designers for precise measurements of the electrical parameters. These parameters depended largely upon the absolute values of the precision resistors and their ratios. According to HDL personnel who tested the circuits, all specified electrical parameters were met by these thin film hybrid modulators when they were tested at room temperature.

2.9 Encapsulation

We investigated the possibility of providing protection during temperature cycling and environmental testing by encapsulation, as an alternative to solder-sealing or welding. The first effort involved the encapsulation of four circuits in a polyurethane resin designated "Scotchcast #221." Upon subsequent electrical tests, one circuit functioned properly, one circuit exhibited an intermittent behavior, one circuit produced an output from only one stage, and one circuit produced no output. It was suggested that the failures were due to the lifting of wire bonds due to encapsulation stresses and that a flexible encapsulant might place less stress on wire bonds. A formulation of

Epon #815 (70 pbw), LP-3 (30 pbw), and DETA (7 pbw) was used to encapsulate two additional circuits. Both circuits remained operative after encapsulation and were submitted along with the one operative circuit encapsulated in Scotchcast #221 to circuit testing personnel for temperature cycling and environmental tests. All three circuits functioned properly over the required temperature range of -31.7 to 57.2°C. To get an idea of the margin of safety in the operation of these circuits, temperature cycling was extended to the range -40 to +74°C. The circuit encapsulated in Scotchcast #221 and one of those encapsulated in the Epon formulation failed at +74°C. Before failure, however, the circuits continued to meet the stringent specifications over the temperature range explored, as did the circuit that did not fail. Two other encapsulants, Stycast #2850 and RTV #643, were tried next, but all circuits so encapsulated produced no output after curing.

At this juncture a series of consultations on this problem was held with personnel at other hybrid microcircuit facilities, both in government and in private industry. Most personnel contacted had experienced similar problems and the opinion most often expressed was that expansion of the encapsulant caused lifting of wire bonds. It was suggested that one of the junction-coating resins, which are used in the semiconductor industry to cover wire bonds in silicon chips, might alleviate this problem. Two semiconductor junction-coating resins, Emmerson & Cummings' Eccocoat SJB and Dow Corning's XR-62-047, were obtained for use in the encapsulating procedure. The wire bonds of one circuit were coated with Eccocoat SJB and those of a second circuit were coated with XR-62-047. Both junction-coating resins were cured according to the manufacturer's instructions before encapsulation in a slightly more flexible epoxy formulation, which consisted of Epon #815 (50 pbw), LP-3 (50 pbw), and DETA (5 pbw). Both circuits functioned properly immediately after encapsulation and continued to function properly through prolonged operation at room temperature, during which time the circuit temperatures surely rose to their steady-state values. The circuit on which the Dow Corning XR-62-047 junction-coating resin was used functioned properly when heated to the high temperature end of the required temperature range of -31.7 to 57.2°C. However, the circuit malfunctioned as the +74°C temperature was approached in an attempt, as before, to determine the margin of safety. The fact that those circuits encapsulated in flexibilized epoxies failed only after heating above some 65.5°C suggests that the problem here is not one of the lifting of wire bonds by stresses imposed by the encapsulant since such stress would have been operative during the prolonged operation at room temperature.

Further consultations with personnel from other microcircuit facilities brought forth the suggestion that corrosion or degradation of the aluminum conductors on silicon chip devices, which would be more temperature sensitive, might be the cause of the failures. Such degradation is known to be accelerated by chloride or fluoride ions and, of course, by heat. Conventional epoxy formulations, such as those used in this work, often contain residual chloride ions. Other possible sources of the deleterious chloride and fluoride ions are the etching reagents and the cleaning solvents used in semiconductor processing. Further work is needed to definitely determine the cause of the failures at elevated temperatures, but such work is beyond the scope of this effort.

3. CONCLUSIONS

(a) Space limitations of the magnitude encountered in this fuze design are easily met by thin-film hybrid technology.

(b) The use of templates during the initial stages of layout permits trial of multiple alternatives without the laborious drawing and redrawing usually required.

(c) The use of computerized thermal analyses gives indications of the steady-state temperatures of circuit components and, thus, is a valuable tool in microcircuit layout and design.

(d) The inherent stability of metal thin film resistors easily met the precision requirements of this circuit.

(e) The low temperature coefficient of resistance (TCR) of metal thin film resistors was adequate to maintain the electrical parameters within specifications over the required temperature range.

(f) Stresses introduced during encapsulation can cause open or intermittent circuit connections, probably by the separation of wire bonds from silicon chip-device metallization. The use of flexibilized encapsulants appears to eliminate this problem.

(g) Malfunctions occur in these circuits at temperatures above some 65.5°C. Since these malfunctions do not occur at lower temperatures, even after extended operations, the cause is thought to be a thermally activated process, such as corrosion. The corrosion of aluminum metallization by residual chloride and/or fluoride ions--often reported by other workers--might well be the culprit here.

(h) Commercially available junction-coating resins appear to help alleviate the problems of open or intermittent circuits occurring during encapsulation.

4. DISCUSSION AND RECOMMENDATIONS

Thin film hybrid technology was demonstrated to be an attractive and workable method of fabricating reliable circuits that have extreme requirements, such as small size, high power dissipation, tight electrical parameter tolerances, and temperature stability. The use of templates and computer thermal analyses allows for optimization of the circuit layout while assuring the workability of that layout. A completely satisfactory method of encapsulating circuits has yet to be established. The cause of the malfunctions at elevated temperatures remains to be determined and probably requires depotting and scanning electron microscopy techniques which were not available at HDL during the course of this work.

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