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THE EVALUATION OF A DIGITAL HARDWARE VOTER/MONITOR IN AN AIRCRA--ETC(U)
MAY 77 H W SCHREADLEY F33615-75-C-3068
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AFFDL-TR-77-30

THE EVALUATION OF A DIGITAL HARDWARE VOTER / MONITOR IN AN AIRCRAFT CONTROL SYSTEM

DYNAMIC CONTROLS, INC.
DAYTON, OHIO 45404

MAY 1977

TECHNICAL REPORT AFFDL-TR-77-30
Final Report for Period – January 1975 – January 1977

AIR FORCE FLIGHT DYNAMICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
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This report describes an evaluation and presents the test results of a Digital Hardware Voter/Monitor used as an input signal selector and fault detector when used in conjunction with an electro-hydraulic control system.

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The DHVM operated as intended by design although asynchronous operation caused the failure detection to be frequency dependent. A digital filter could be incorporated to reduce the frequency dependency of the failure detection circuitry.

FOREWORD

The effort described in this document was performed by the Dynamic Controls, Inc., of Dayton, Ohio under Air Force Contract F33615-75-C-3068. The contract was performed under Project Number 1987 and 2049 entitled "Flight Control Actuation Systems Development". Work under the contract was carried out in the Air Force Flight Dynamics Laboratory (AFFDL), Flight Control Division at Wright-Patterson Air Force Base utilizing United States Air Force facilities. The work was administered by Bruce H. Earley, (AFFDL/FGL), Project Engineer.

This report covers work performed between January 1975 and 31 January 1977. The technical report was submitted by the author in February 1977.

The author wishes to express his appreciation to the Dynamic Controls, Inc. personnel Gavin D. Jenney, Carl N. Allbright, Heinrich J. Wieg and William G. Talley for their contributions in the areas of analysis, fabrication and testing associated with the DAIS effort. The author wishes to express his acknowledgement and thanks to DAIS personnel Captain George Lacy, Rafael Umana, Edward Collins and Captain Robert Hendrix for their cooperation and assistance during this effort.

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LIST OF ABBREVIATIONS AND SYMBOLS

ABBREVIATIONS

A/C	Aircraft
A/D	Analog-to-digital converter
A/R	Amplitude ratio, db
Asynch., asynch.	Asynchronous
CH, ch	Channel
cis	Cubic inches per second
DAIS	Digital Avionics Information System
db	Decible
DHVM	Digital Hardware Voter Monitor
DHVMT	Digital Hardware Voter Monitor Tester
div	Division
Freq., freq.	Frequency
F.S.	Full Scale
HFCS	Hybrid Flight Control Simulator
Hi, hi	High level digital signal
Hz	Hertz
in.	Inch

ABBREVIATIONS

Lo	Low level digital signal
LVDT	Linear variable differential transformer
ma	Milliamps
max	Maximum
msec., ms	Millisecond
No.	Number
Op.	Operation
P-P	Peak to peak
psi	Pounds per square inch
PWM	Pulse width modulated
rad.	Radian
sec.	Second
TTL	Transistor-Transistor-Logic
V,v	Volts

SYMBOLS

A	Ripple amplitude % of PWM signal amplitude
C	Capacitor
E	Voltage
E_{in}	Input voltage
f	Frequency in Hz
f_n	Natural frequency
K	Proportional gain constant
N_z	Normal acceleration
p	Pulse
ΔP	Differential pressure
p_t	Theoretical number of pulses
R	Resistor
$\overline{\text{Select}}$	Not selected
t	Time, sec.
TC	Time constant in second
X_a	Actuator position
uf	Micro-farads
#	Number

SYMBOLS

%	Percent
O	Pitch rate
ϕ	Phase angle
δe	Elevator Position
ω_n	Natural frequency in radian/second
ω	Frequency in radian/second
ζ	Damping ratio

SECTION I

INTRODUCTION

This report describes a digital voter monitor evaluation conducted by Dynamic Controls, Inc. for the Air Force Flight Dynamics Laboratory from September 1975 to December 1976 under Air Force Contract F33615-75-C-3068. The work was conducted at Wright-Patterson Air Force Base using government furnished facilities.

The objective of the effort was to evaluate the use of a Digital Hardware Voter Monitor (DHVM) as an input signal selector and signal fault detector when used with a hydraulic actuation system. The specific application of the DHVM is intended to be an integral part of the AFFDL/DAIS Flight Engineering Facility. The DHVM was designed and realized into a hardware under Contract F33615-74-C-3068 and is described in Reference 1, AFFDL-TR-74-94.

The units submitted to Dynamic Controls, Inc. for evaluation were a redesign fabricated by the AFFDL/FGL DAIS Group.

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1. Mrazek, Jerry G., Ph.D., "Digital Hardware Voter/Monitor Breadboard Development and Evaluation", Final Report, AFFDL-TR-74-94, July 1974

SECTION II

EVALUATION OF THE DHVM CONCEPT

1.0 TECHNICAL APPROACH

Dynamic Controls, Inc. with the co-ordination of the AFFDL/FGL DAIS Group, developed a test plan, Test Plan No. TB-600-300, for use as a guide in evaluating the DHVM when applied to actual electro-hydraulic servo systems and an aircraft aerodynamic simulation. The objectives of the evaluation were the following:

a. Verify the basic performance characteristics of the DHVM

b. Establish guide lines to assist in the application of the DHVM to control systems

c. Identify DHVM operational problem areas

2.0 DHVM DESCRIPTION

2.1 General Description

The DHVM, FIGURE 1, is shown in FIGURE 2 as a functional element in a digital flight control system. The DHVM accepts 4 digital inputs from 4 flight computers that are operating asynchronously. The DHVM

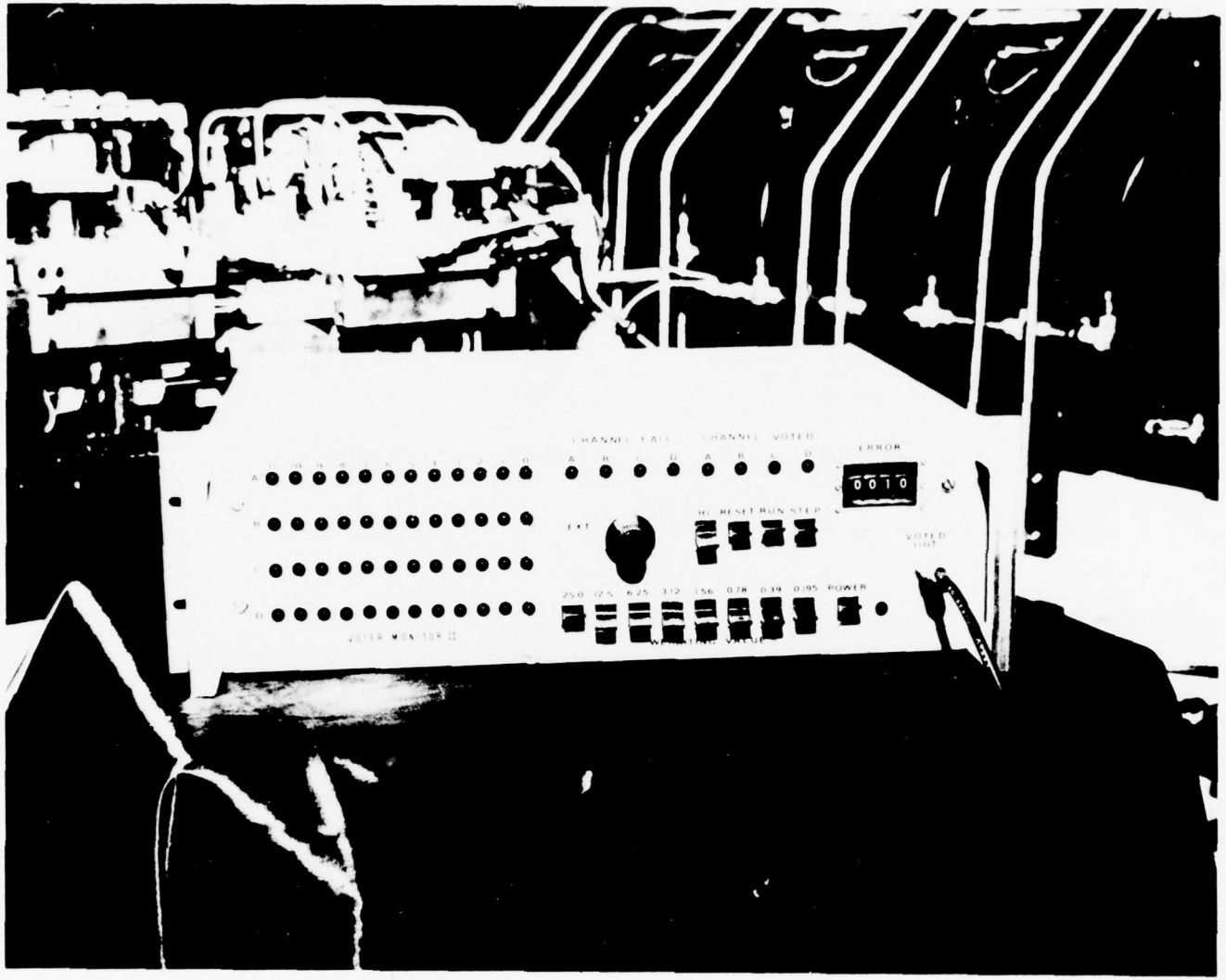


FIGURE 1 DIGITAL HARDWARE VOTER MONITOR

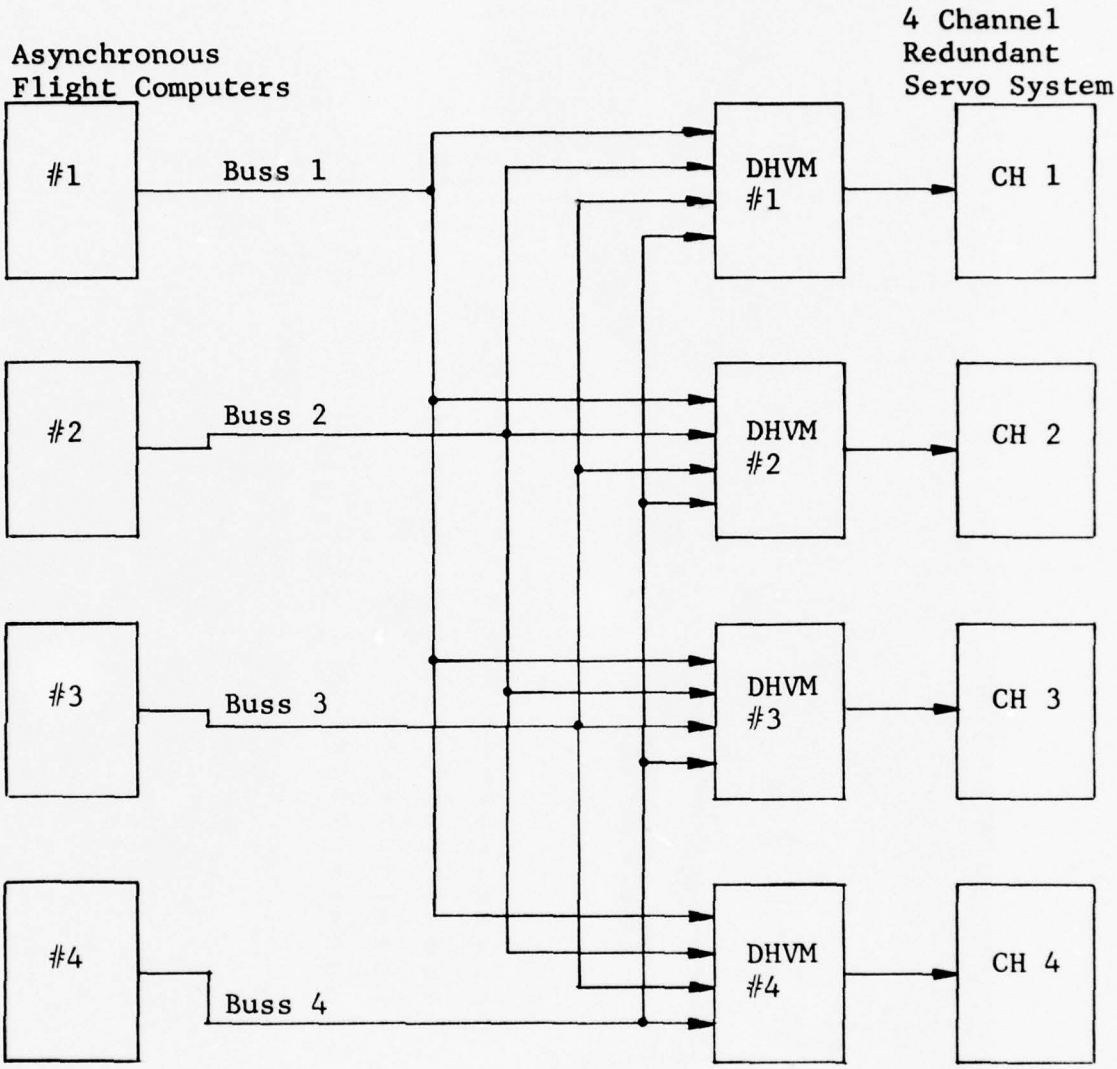


FIGURE 2 The DHVM as an element in a Digital Flight Control System

provides the following primary functions:

a. Selection of the next to lowest absolute value of the input words for an output.

b. Determination of out-of-tolerance signals and exclude failed channels. (The DHVM is designed to determine if the remaining three non-selected signals are within a selected tolerance. The tolerance is a plus or minus percentage of the full scale signal.)

c. Conversion of the input digital word to a pulse width modulated (PWM) output signal.

2.2 DHVM Detail Description

The Digital Hardware Voter Monitor (DHVM) accepts four 12 bit words, from which a pulse width signal (modulated proportional to the magnitude of input word) is generated. Since 12 bits are used for an input word, the modulation of the pulse width signal has a theoretical resolution capability of 2^{-12} of the full scale input value. A 100% duty cycle creates a maximum positive output.

To provide input signal failure detection, the DHVM receives four separate input words over separate input lines. These words are stored and used to set up each of the four synchronous binary counters. The time for each synchronous binary counter to count to the magnitude of its input word is measured (using the carry out pulse from the last counter segment of the counters to indicate counting completion). The time counting pulses are transferred to failure logic which determines out-of-tolerance signals and selects the low median signal to be used for the output of the DHVM. The low

median signal is selected using the criteria that it is the signal with the next to the lowest absolute magnitude.

To establish time counting tolerances for failure detection, the DHVM incorporates tolerance counters capable of counting from 2^0 to 2^{10}. The DHVM uses both a low and hi-limit tolerance counter. The low-limit counter is started when the counting of the lowest value signal has been completed. The low-limit counter is stopped when the 2nd smallest signal completes counting, and the hi-limit counter is started. A failure has occurred if the low-limit counter completes its counting before the 2nd smallest signal counter stops or if the hi-limit counter completes before either of the remaining signal counters complete counting. The failure counter limits are user settable on the front panel and are capable of being varied from errors of $\pm$ .195% to $\pm$ 50% of full input magnitude.

The DHVM incorporates failure event counters which act as time delays to prevent nuisance disconnects. Each time a channel is determined to be out-of-tolerance, that channel's failure counter is incremented. Each time a channel is determined to be within the voting tolerance, the counter is decremented with the lower limit on the decremented value being zero. When a channel counter reaches a full count, the channel is locked out until manually reset. When three channels have failed, the DHVM generates a 50% duty cycle pulse width modulation, corresponding to an output of zero when integrated. A full count on the failure counter is programmed by thumb wheel switches on the front panel.

2.2.1 Pulse Width Modulated Output Signal

The DHVM output signal is a pulse width modulated signal proportional to the 12 bit input words received by the DHVM. This produces a theoretical output signal

resolution of 2^{-12} times the full scale analog signal. For the $\pm$ 10.0 volt test system, the resolution is 2^{-12} x 20 = 4.88×10^{-3} volts/bit (or in the case of the pulse width modulated word 4.88×10^{-3} volts/count).

The pulse width modulated signal is a fixed repetition rate square wave carrier controlled by 2^{12} clock pulses that have been programmed by the digital input word to a synchronous counter. When the counters are counting, the output is hi. The output returns to the low output when the counters stop.

FIGURE 3 indicates the PWM output signal. T is the repetition rate in seconds (or update frequency^{-1}) and t is the weight of the input word. During the time T, 2^{12} clock pulses occur. During time t, 2^{X} (programmed) pulses occur with each pulse having an amplitude E relative to the low output value.

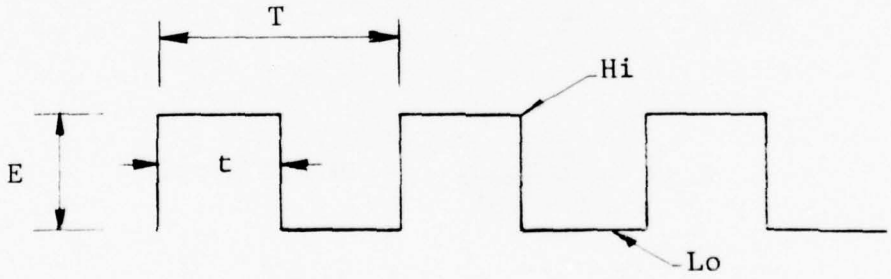


FIGURE 3 PWM Signal

Demodulation of a pulse width signal requires only a low pass RC filter. This provides an average output proportional to the pulse width. The output will contain some ripple at the repetition rate (update frequency) at which pulse width amplitude is controlled. The following example calculation indicates the peak to peak ripple amplitude as a percentage of the full scale amplitude of the pulse width modulated signal when using a simple RC filter for demodulation:

$$A = \frac{100}{\sqrt{1 + \left(\frac{f}{f_n}\right)^2}}$$

Reference 2

A = Ripple amplitude % of PWM signal amplitude

f = Update frequency, Hz

$f_n = \frac{1}{2 \sim RC}$

For $\frac{f}{f_n} = 10$:

$$A = \frac{100}{\sqrt{1 + 10^2}} = 9.95\% \text{ Ripple}$$

Therefore, with a $\pm$ 10 volt PWM signal and $\frac{f}{f_n}$ ratio of 10, the output ripple will be $\pm$ .995 volts.

---

2. Millman, Jacob, Ph.D. and Taub, Herbert, Ph.D. "Pulse and Digital Circuits", Mc-Graw Hill Book Company, Inc., New York 1956

3.0 TEST DESCRIPTION

3.1 General

Evaluation of the Digital Hardware Voter Monitor (DHVM) was carried out in the following four phases:

PHASE I - DHVM Testing

PHASE II - DHVM and Servo System Testing

PHASE III - DHVM, Servo System and Aircraft Dynamics Testing

PHASE IV - Two DHVM's and Servo System Testing

3.1.1 Phase I

In this phase, the Digital Hardware Voter Monitor was tested as a separate unit using the Digital Hardware Voter Monitor Tester (DHVMT), FIGURE 4 , as a test instrument. The DHVMT is an instrument (developed by the Flight Dynamics Laboratory) that converts four analog channels ($\pm$ 10 volt) into binary words compatible with the DHVM input requirements. The DHVMT has the following channel control parameters:

Analog Input

1. D.C. Offset $\pm$ 5 volts
2. Channel Gain .0 to 1 volts/volt

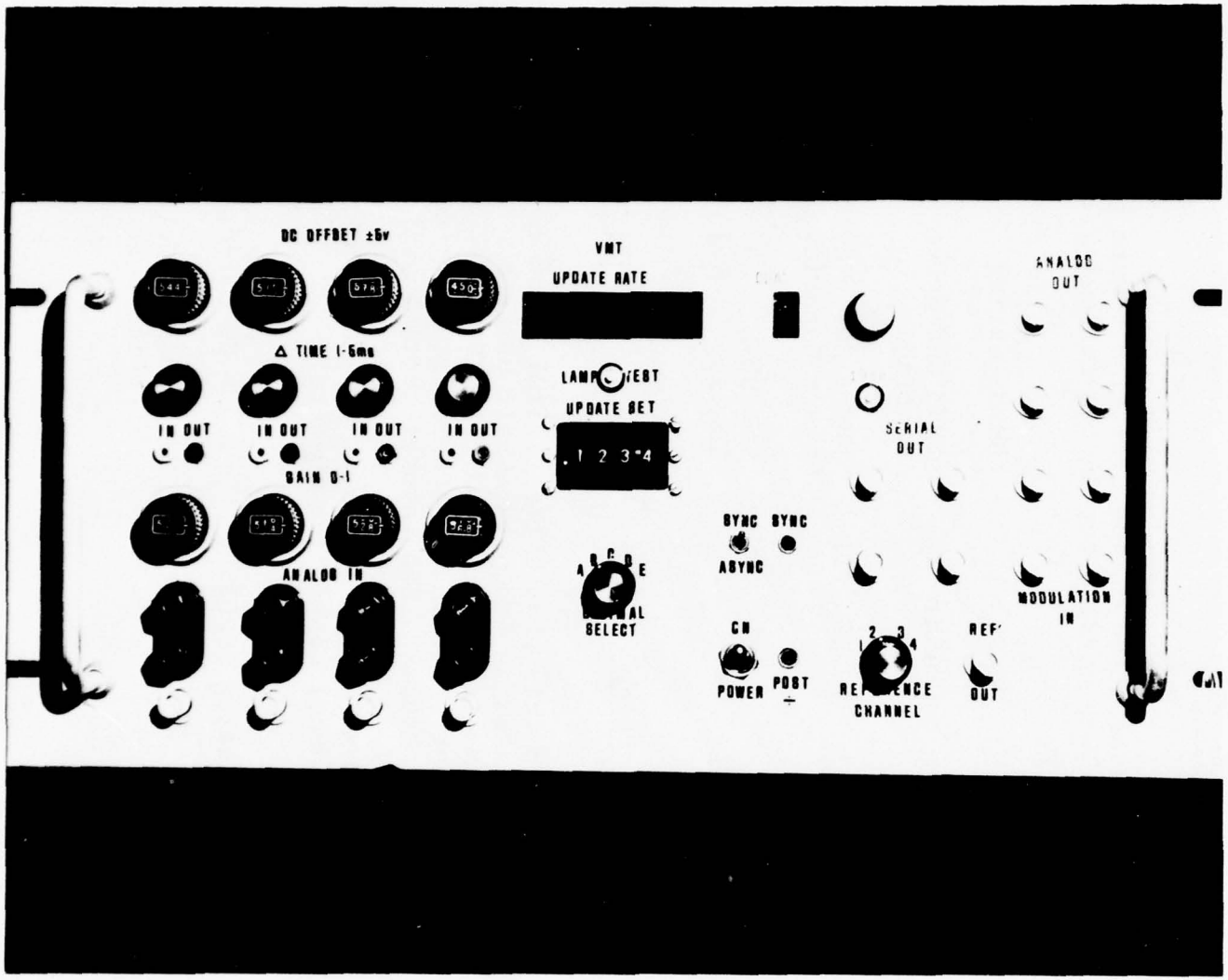


FIGURE 4 DIGITAL HARDWARE VOTER MONITOR TESTER

Digital Output

1. Time Delay .5 to 4.5 milliseconds
2. Asynchronous sampling period of .005 to 1000 milliseconds
3. Synchronous sampling period of .0013 to 1000 milliseconds

In testing the DHVM, the ability of the unit to perform the following functions was measured:

1. Conversion of an input word to a proportional pulse width modulated signal output.
2. Selection of the low median input (statically and dynamically).
3. Determination of out-of-tolerance inputs.
4. Operation and voting after out-of tolerance channels have been voted out.

FIGURE 5 , shows the test circuit for the Phase I testing.

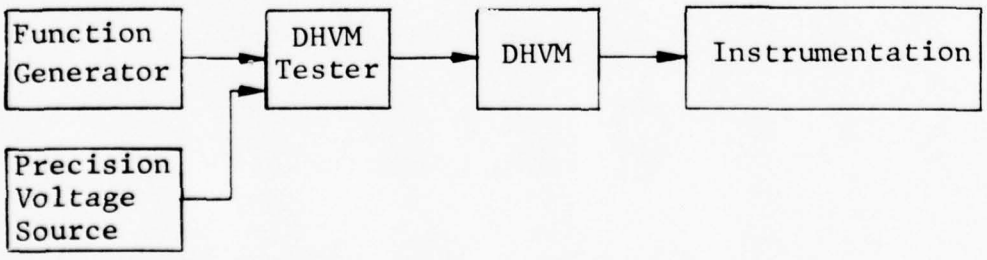


FIGURE 5 Phase I Test Set-Up

3.1.2 Phase II

For the Phase II tests, the DHVM's output was connected to an electro-hydraulic servo system. The AFFDL/FGL Hybrid Flight Control Simulator (HFCS), as shown in FIGURE 6 was used as an electro-hydraulic servo system. The HFCS was programmed to simulate the F-4 680J secondary Fly-By-Wire system which has a dynamic response out to 30 Hz.

For the Phase II evaluation, measurement of the input-output characteristics of the HFCS with the DHVM (connected in series with the command input to the HFCS) was made. These measured results were then compared to the input-output characteristics of the HFCS without the DHVM. In measuring the input-output characteristics, the effect of input channel failures on the combined performance of the DHVM and HFCS was measured.

The following performance characteristics were recorded:

1. Linearity
2. Resolution
3. Hysteresis
4. Dynamic Response
5. Signal Distortion
6. Failure Mode Operation

The effect of sample rate and asynchronous clock operation on the control system was also evaluated during this phase testing.

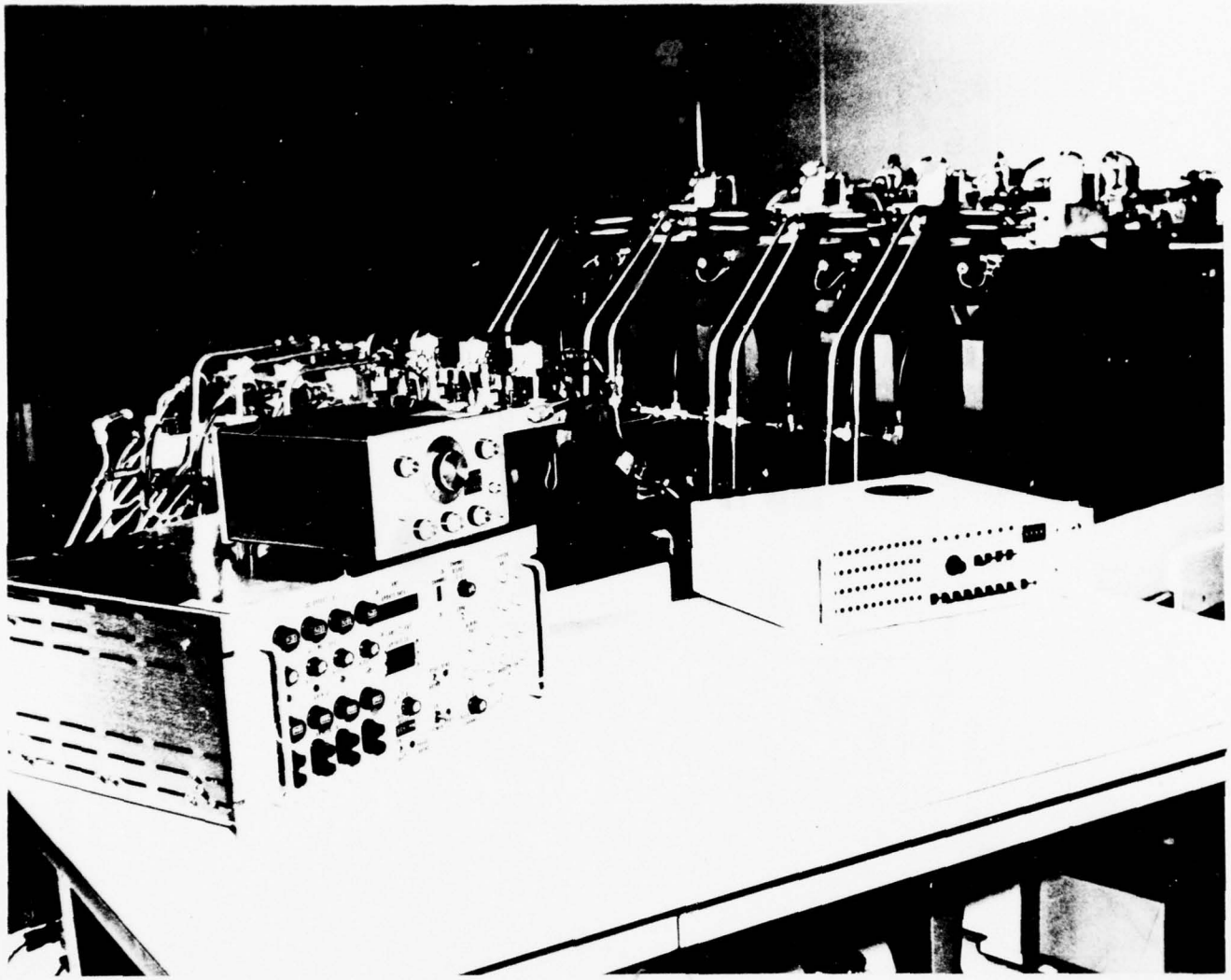


FIGURE 6 HFCS, DHVMT, DHVM and Function Generator

FIGURE 7, shows the test circuit for the Phase II testing.

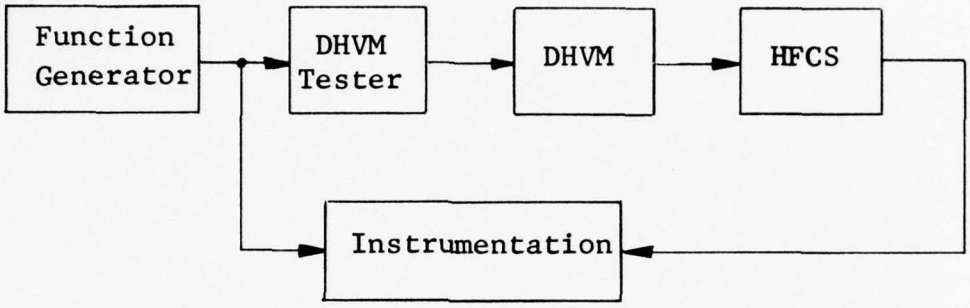


FIGURE 7 Phase II Test Set-Up

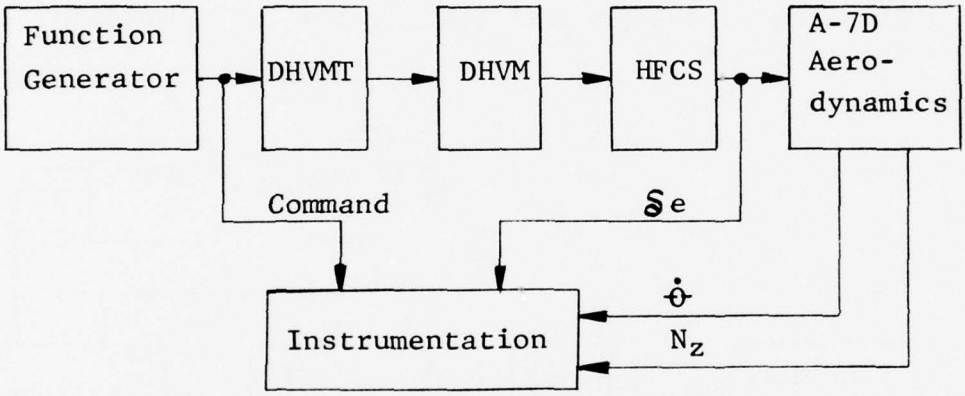
3.1.3 Phase III

In order to evaluate the effect of using the DHVM in the control loop on aircraft performance, simulated A-7D aerodynamics (longitudinal axis) were added to the Phase II test set-up. A 680J secondary system was connected to A-7D primary actuator dynamics on the HFCS.

The combination of the A-7D airframe dynamics and power actuator response in conjunction with the 680J

secondary actuator dynamics, was representative of state-of-the-art in terms of both the airframe and the fly-by-wire flight control system.

The following schematic illustrates the test set-up used for Phase III and is identical to FIGURE 87, appearing later in the report.



Phase III DAIS Test Set-Up

The performance measurements recorded were the pitch rate and normal acceleration of the aircraft with and without the DHVM in the control channel.

Both sinusoidal and step inputs were used to drive the simulation.

3.1.4 Phase IV

The Phase IV testing was an evaluation of multiple DHVM's operating asynchronously in a redundant electro-hydraulic control system. The performance measurements concentrated on the output error magnitude of asynchronous operation and effect on the electro-hydraulic redundancy monitoring scheme for the HFCS. FIGURE 8 , illustrates the general test system configuration.

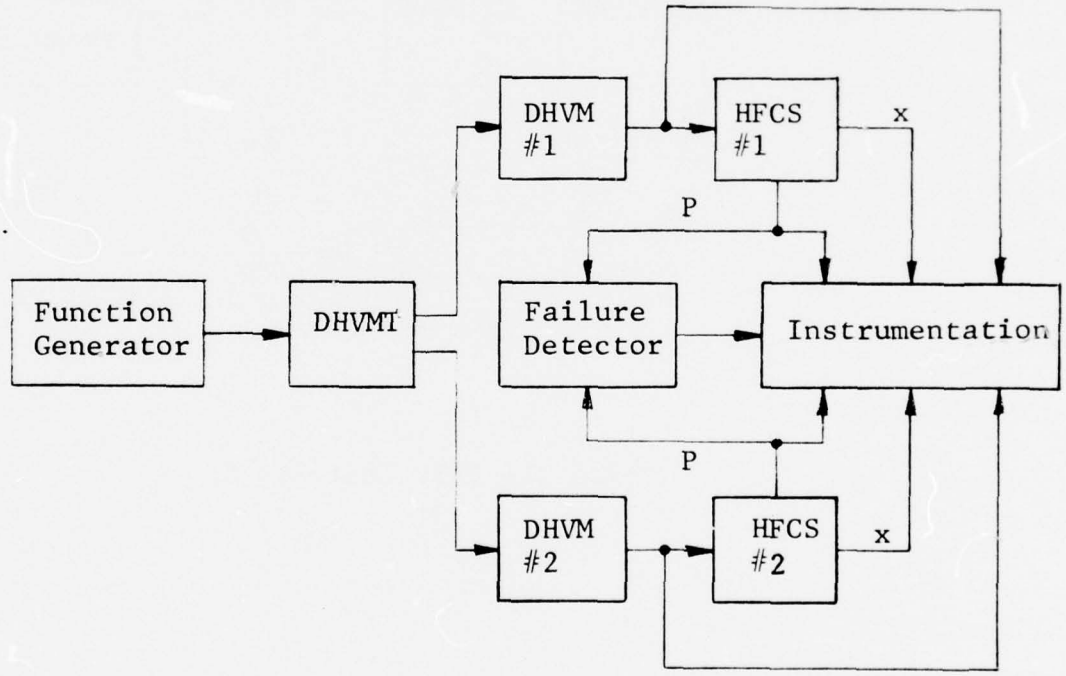


FIGURE 8 Phase IV Test Set-Up

4.0 TEST RESULTS

4.0.1 DHVM Equipment Familiarization

Several items requiring consideration were found during the preliminary investigation and equipment familiarization phase of this test program. These are discussed in the following sub-section.

4.0.1.1 PWM Signal Off-Set

The output of the DHVM as provided for evaluation was TTL Logic. This gave measured values of the PWM signal 3.9 volts Hi level and .100 volts Lo level. This output was not compatible to the HFCS' ± 10 volt input requirements. Therefore, several methods were investigated that would provide the bias and gain required to convert the TTL logic output to a ± 10 volt signal. Two conversion methods were investigated, an optical coupler as shown in FIGURE 9, and an analog converter and bias circuit as shown in FIGURE 10.

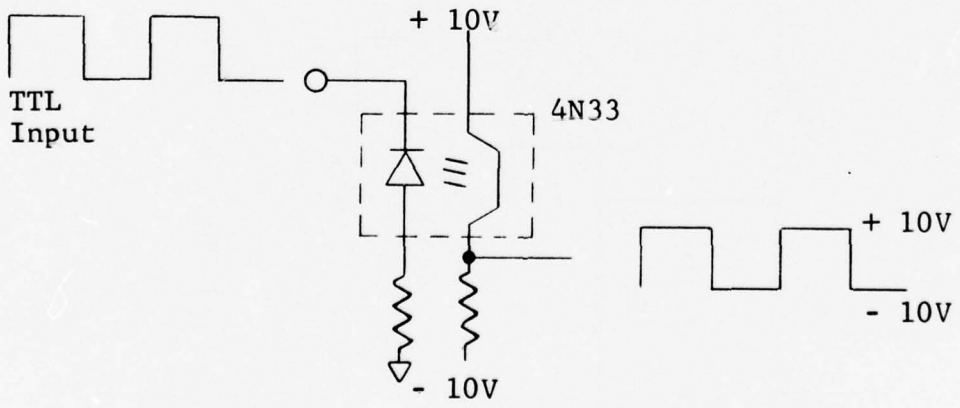


FIGURE 9 Optical Coupler

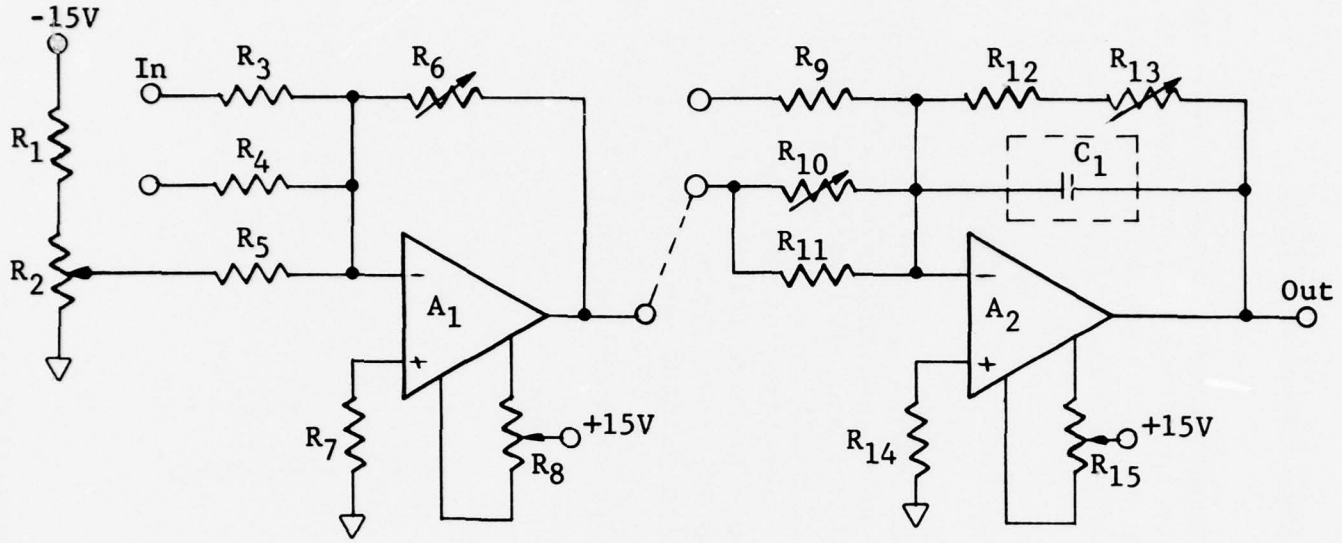


FIGURE 10 DHVM Analog Converter and Bias

The optical coupler FIGURE 9, was initially chosen for conversion because of the ability to remove the inherent clock noise from the Hi and Lo TTL signal levels. A problem encountered with the optical coupler was that the time constant of switching from Hi to Lo and Lo to Hi were quite different. The non-symetrical signal transitions created a null off-set in the output signal.

The interface circuit inserted between the DHVM and the HFCS is shown in FIGURE 10, potentiometer R_2 provides the bias. Potentiometer R_6 adjusts the gain of A_1 while R_{10} adjusts the gain of A_2 (R_{11} being in parallel desensitizes R_{10} for easier trimming). Potentiometer R_{13} adjusts the static and dynamic gain of A_2. C_1 was added for Phase II testing to cause A_2 to act as a PWM demodulator.

4.1 Phase I Tests

4.1.1 PWM Signal Linearity and Resolution

The DHVM output signal linearity and resolution were measured using two methods, an indirect and a direct method.

4.1.1.1 Indirect Method Description

The indirect method utilized a time/frequency counter to measure the time that the PWM output signal was at the Hi level. The DHVM up-date frequency used for the test was also measured. This data was then used to convert the pulse width to clock pulses (the clock pulses occurring during the measured time are directly proportional to the input voltage amplitude). The clock pulses "p" were calculated as follows:

$p = tf$ Where:

p = pulses that have occurred during Hi level output

t = pulse width, sec.

f = clock frequency Hz

This calculated value from the measured time was compared to the theoretical number of pulses representing the input voltage. The theoretical number of pulses were calculated as follows:

$$p_t = \frac{10 + E}{20} \times 2^{12}$$

Where:

p_t = theoretical number of pulses

E = input voltage

Each channel was individually measured for resolution and linearity by applying off-sets in the other channels in order to position the channel of interest to the low median position. The inputs were driven simultaneously in a synchronous mode, so that the channel of interest remained in the low median position.

In evaluating the test results, it should be realized through all sections of this test program that the DHVMT and DHVM were treated as one unit. The resolution measurements were basically affected by the DHVMT, since it had 2 least significant bits of noise out of its

analog-to-digital converters. This was readily apparent by viewing the input word data lights on the front panel of the DHVM. The 2 least significant bits of noise convert to an observed .010 volt signal resolution uncertainty (for a $\pm$ 10 volt full scale input). The values are considered to be representative of those encountered in a typical digital system.

The DHVM, by design, should not have any inherent errors generated internally. Once the synchronous counters are programmed by the input digital word from the DHVMT (or computer) the DHVM will count to the instructed value unless there is a basic malfunction of one of the counters.

4.1.1.2 PWM Linearity Measurements - Indirect Method

The linearity data was obtained by measuring the width of the Hi level pulse. Data was taken for -9.00 volt, -5.00 volt, 0.00 volt, +5.00 volt and +9.00 volt inputs from a precision voltage source. For each input voltage, DHVM up-date rates of 91.5/sec., 122/sec., 183/sec., 244/sec., 366/sec., 488/sec., 732/sec., 977/sec., and 1465/sec. where used. The measured data showed no variation with up-date rates. Therefore, the data for each input level was averaged and minimized as shown in the following tables:

TABLE 1 indicates the average pulses for each input level.

TABLE 2 is the averaged percent error of the reading.

TABLE 3 is the averaged percent of full scale error.

TABLE 1

PWM AVERAGE CLOCK PULSE COUNT
DURING HIGH LEVEL OUTPUT

INPUT VOLTAGE	-9.00V	-5.00V	0.00V	+5.00V	+9.00V
Calculated Theoretical Pulse Count	204.8	1024.0	2048.0	3072.0	3891.2
Channel A	198.8	1022.3	2048.0	3071.5	3857.0
Channel B	205.1	1025.2	2048.2	3073.0	3887.0
Channel C	207.3	1026.5	2048.8	3070.0	3886.0
Channel D	206.7	1025.5	2046.6	3072.7	3892.0

TABLE 2

PERCENT DEVIATION FROM THEORETICAL PULSE COUNT

INPUT VOLTAGE	-9.00V	-5.00V	0.00V	+5.00V	+9.00V
Channel A	-3.02%	- .17%	0.00%	- .02%	- .89%
Channel B	+ .15%	+ .12%	+.04%	+ .03%	- .11%
Channel C	+1.21%	+ .24%	+.04%	- .07%	- .13%
Channel D	+ .92%	+ .15%	-.07%	- .02%	+ .02%

TABLE 3

PERCENT DEVIATION FROM A FULL SCALE PULSE COUNT

INPUT VOLTAGE	-9.00V	-5.00V	0.00V	+5.00V	+9.00V
Channel A	.15%	.04%	.00%	.02%	.85%
Channel B	.01%	.03%	.02%	.02%	.10%
Channel C	.06%	.06%	.02%	.05%	.12%
Channel D	.05%	.04%	.04%	.02%	.02%

From these tables, the average resolution is .37% and the average linearity is .08%. The tabulated data shows that Channels A and C have the largest errors. This corresponds to the visually observed bit noise on these channels (Channels A and B had 2-3 bits of noise and Channels C and D had 1-2 bits of noise.

4.1.1.3 Direct Method Description

For the direct method of measurement, the DHVM pulse width modulated signal was fed into an RC filter with a time constant of .004 seconds. The output of the RC filter was connected to an X-Y recorder. The time constant of the RC filter was selected to leave the minimum amount of PWM noise in the signal connected to the X-Y plotter.

Resolution and linearity were recorded on X-Y plots using the test set-up in FIGURE 11.

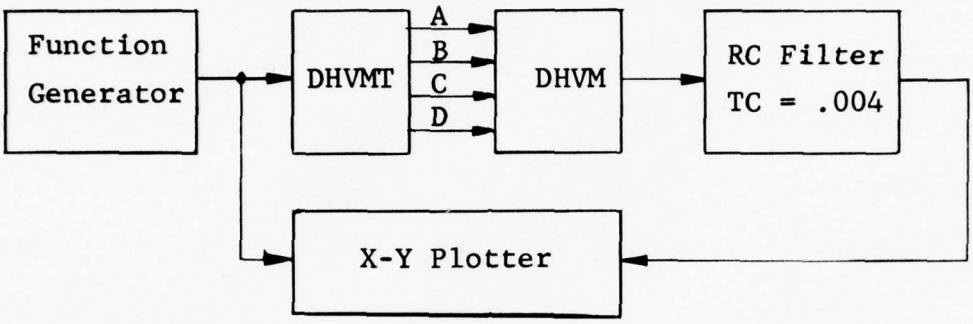


FIGURE 11 Resolution and Linearity Test Set-Up

The data was recorded with the DHVMT updating at 200 samples/sec. and the DHVM set at 1465 updates/sec. The plots were generated with a triangle wave at a frequency of .01 Hz and amplitudes of $\pm$ 2.5 volts, $\pm$ .25 volts and $\pm$ .025 volts. (A $\pm$ .5 volt input was used for clarity in some cases.)

The triangle wave input signal frequency of .01 Hz was selected to allow the theoretical resolution of 2^{-12} times 20 volts or .0049 volts/bit to be recorded with the input of $\pm$ .025 volts. (The input voltage change

per sample was .001 volt/sec. times the .005 sec./updates, resulting in an input voltage change of 5×10^{-6} volts/update.) The input amplitudes were recorded about zero volts input bias to the DHVMT.

4.1.1.4 PWM Linearity Measurements - Direct Method

The data from Channels B and C was selected as representative of the X-Y linearity and resolution data. Channel B with 2-3 bits of noise and Channel C with 1 to 2 bits of noise represent the channels with the highest and lowest signal to noise ratios.

FIGURES 12 through 15 are the Channel B X-Y plots. The resolution can be seen on FIGURES 14 and 15. The predicted resolution with 2 uncertain bits would be the binary value of the uncertain bits divided by the full scale binary word value times the full scale voltage as follows:

Example:

$$\frac{2^2 \text{ bit uncertainty}}{2^{12} \text{ bit full scale}} \times 20 \text{ volts full scale} = .0195 \text{ volts}$$

FIGURE 12 indicates an output with a .039 volt wide step at every .312 volts of input. The expanded scale on FIGURES 13 and 14 indicates intermediate steps every .156 volts for a .020 volt width. This type of respective stepping is generally caused by differential nonlinearity in the analog-to-digital converters.

FIGURE 15 represents the basic resolution of .0195 volts (2^2 bit) and the step which relates to the un-

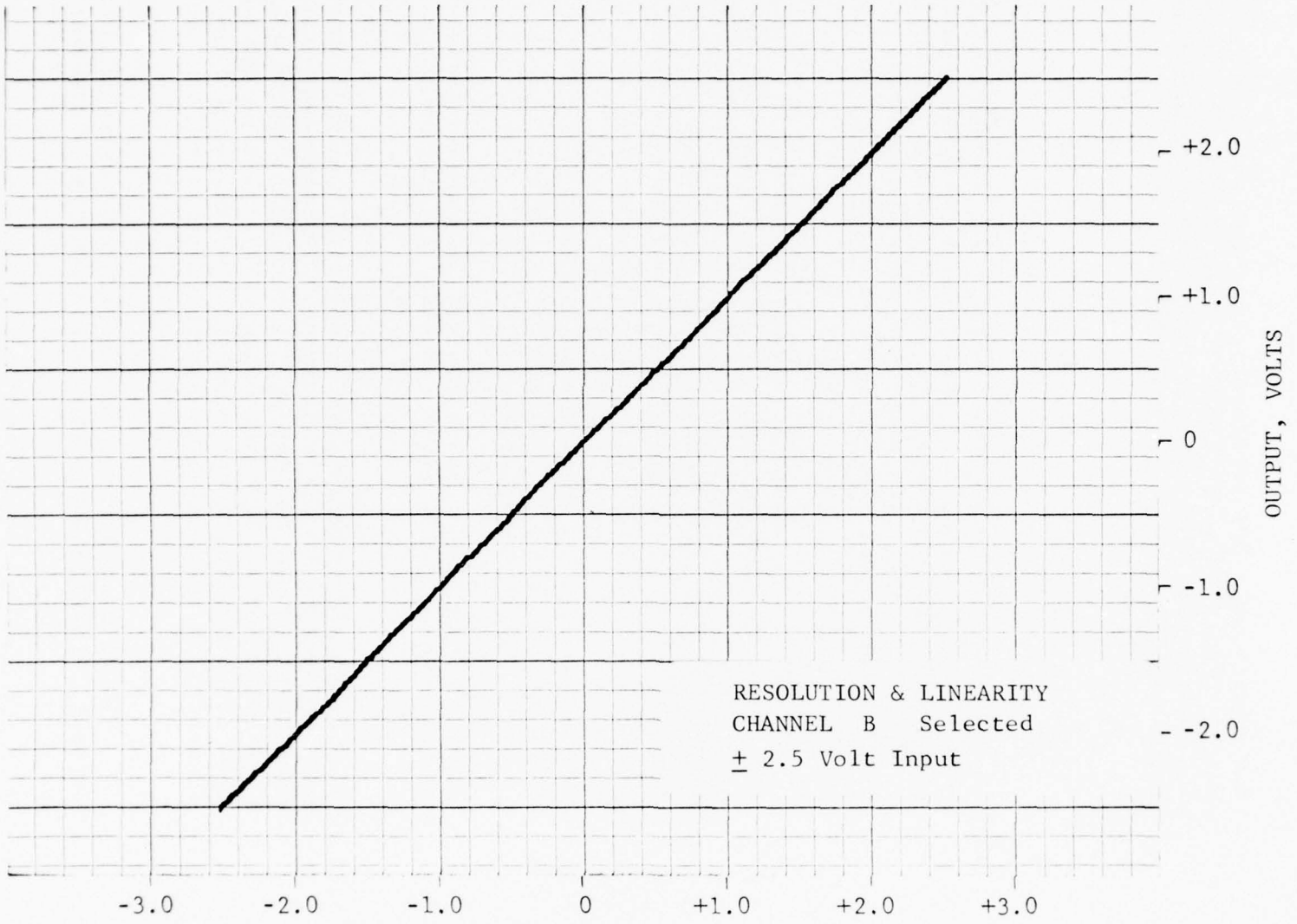

+2.0
+1.0
0
-1.0
-2.0
OUTPUT, VOLTS
RESOLUTION & LINEARITY
CHANNEL B Selected
± 2.5 Volt Input
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
INPUT, VOLTS

FIGURE 12

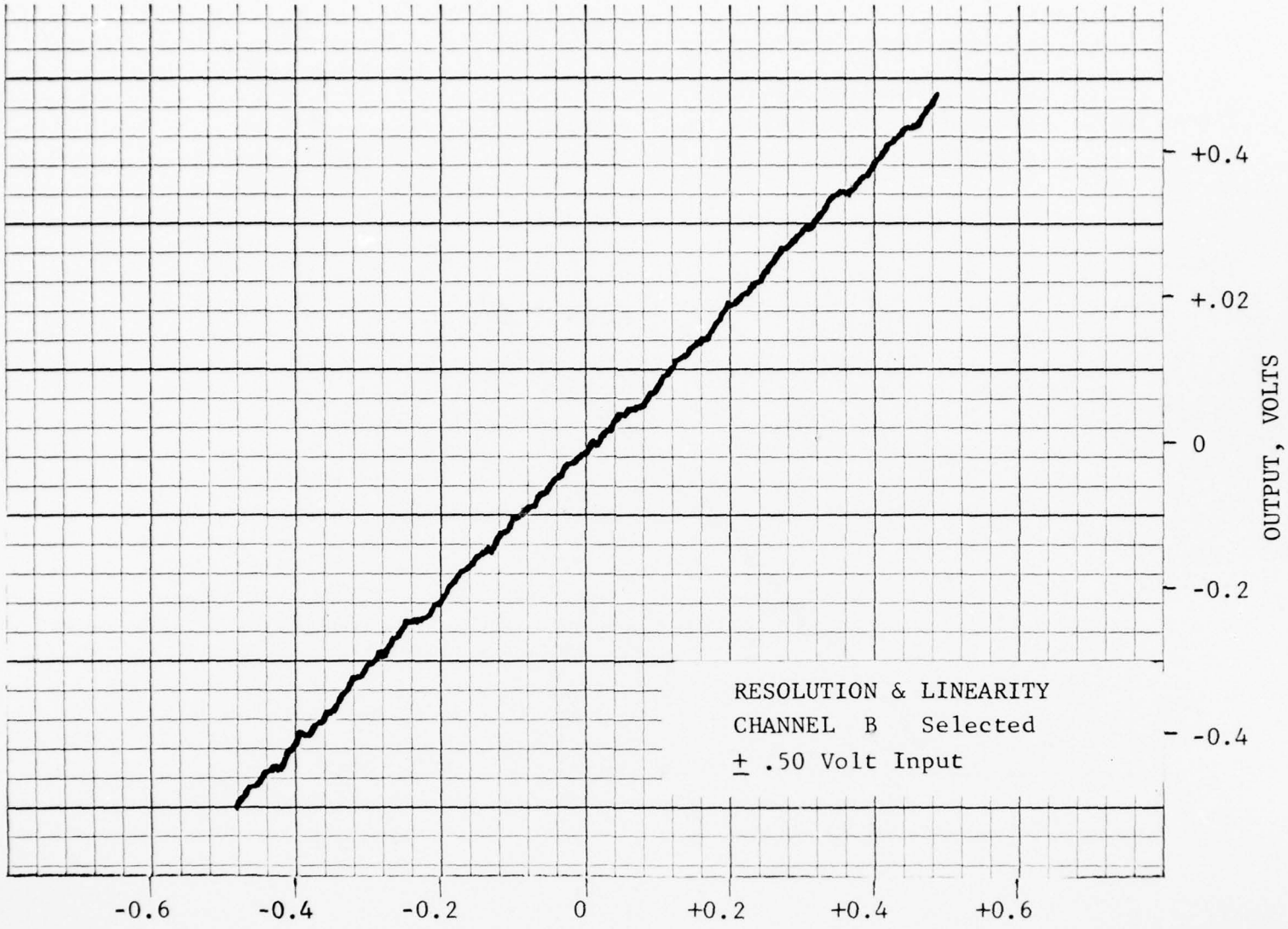

+0.4
+.02
0
-0.2
-0.4
OUTPUT, VOLTS
RESOLUTION & LINEARITY
CHANNEL B Selected
± .50 Volt Input
-0.6
-0.4
-0.2
0
+0.2
+0.4
+0.6
INPUT, VOLTS

FIGURE 13

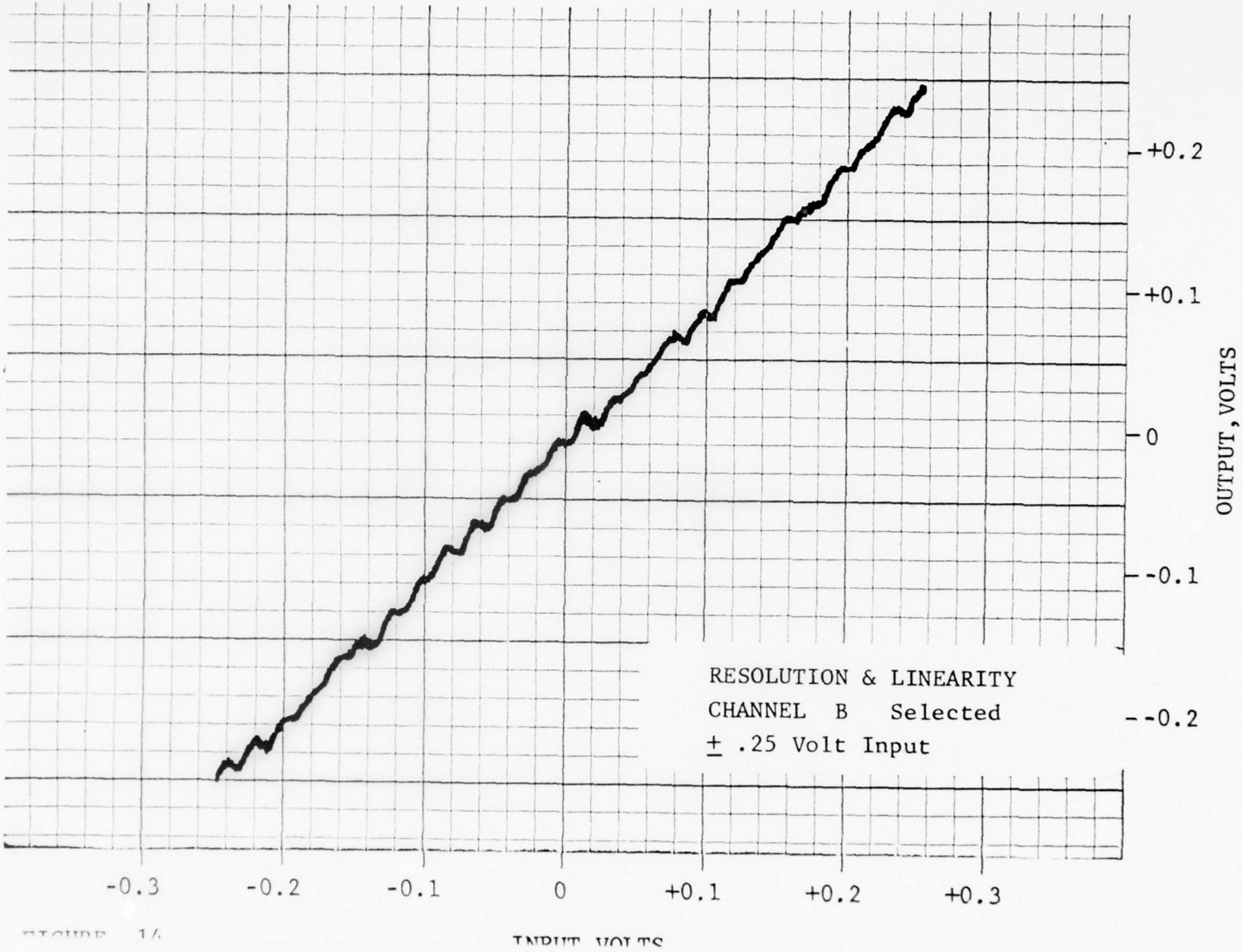

RESOLUTION & LINEARITY
CHANNEL B Selected
± .25 Volt Input
+0.2
+0.1
0
-0.1
--0.2
OUTPUT, VOLTS
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
INPUT VOLTS

FIGURE 14

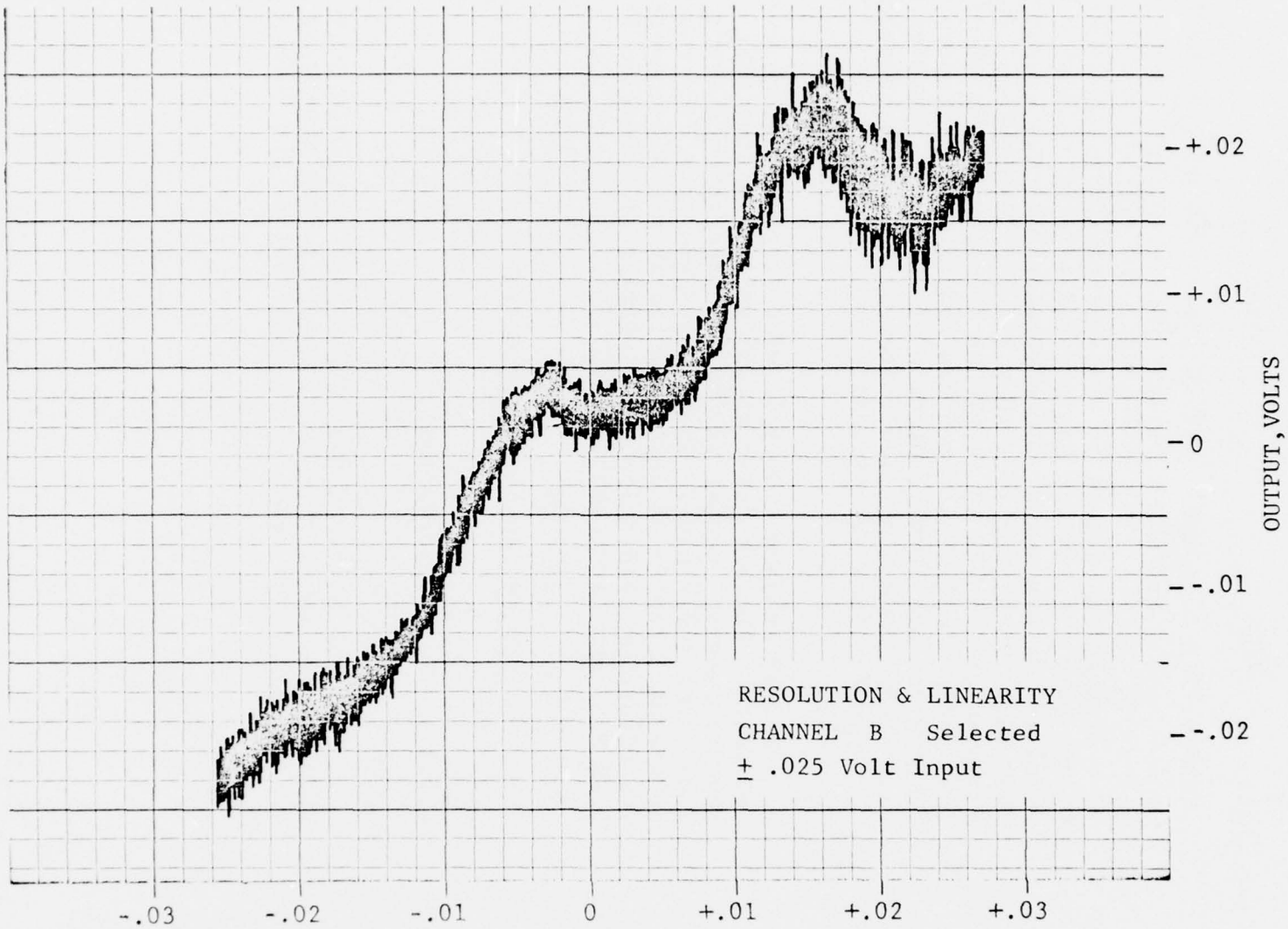

+.02
+.01
0
-.01
-.02
OUTPUT, VOLTS
RESOLUTION & LINEARITY
CHANNEL B Selected
± .025 Volt Input
-.03
-.02
-.01
0
+.01
+.02
+.03
INPUT, VOLTS

FIGURE 15

certain bits of noise noted at the output of the DHVMT.

FIGURES 16 through 19 are the Channel C X-Y plots. FIGURE 18 indicates the basic resolution of Channel C where the output has a .010 volt wide step for every .039 volts resulting in a 10 millivolt resolution. The expansion of FIGURE 18 is FIGURE 19 on which the 10 millivolt and a 5 millivolt step has been recorded, representing the absolute resolution of the analog-to-digital converter. This 5 millivolt step is the expected resolution under ideal conditions.

FIGURE 16 shows .02 volt wide steps repeating every .62 volts. There is also a .039 volt wide step that appears near the center of the plot and repeats every 5.00 volts (2^{10} bit). These steps are generally caused by the differential non-linearities in the A/D converter. The resulting resolution and linearity of Channel C is 0.2% F.S. and .1% respectively.

4.1.2 Low Median Signal Selection

4.1.2.1 Test Description

The test set-up shown in FIGURE 20 was used to determine that the low-median (next to lowest algebraic value) signal was selected as an output of the DHVM.

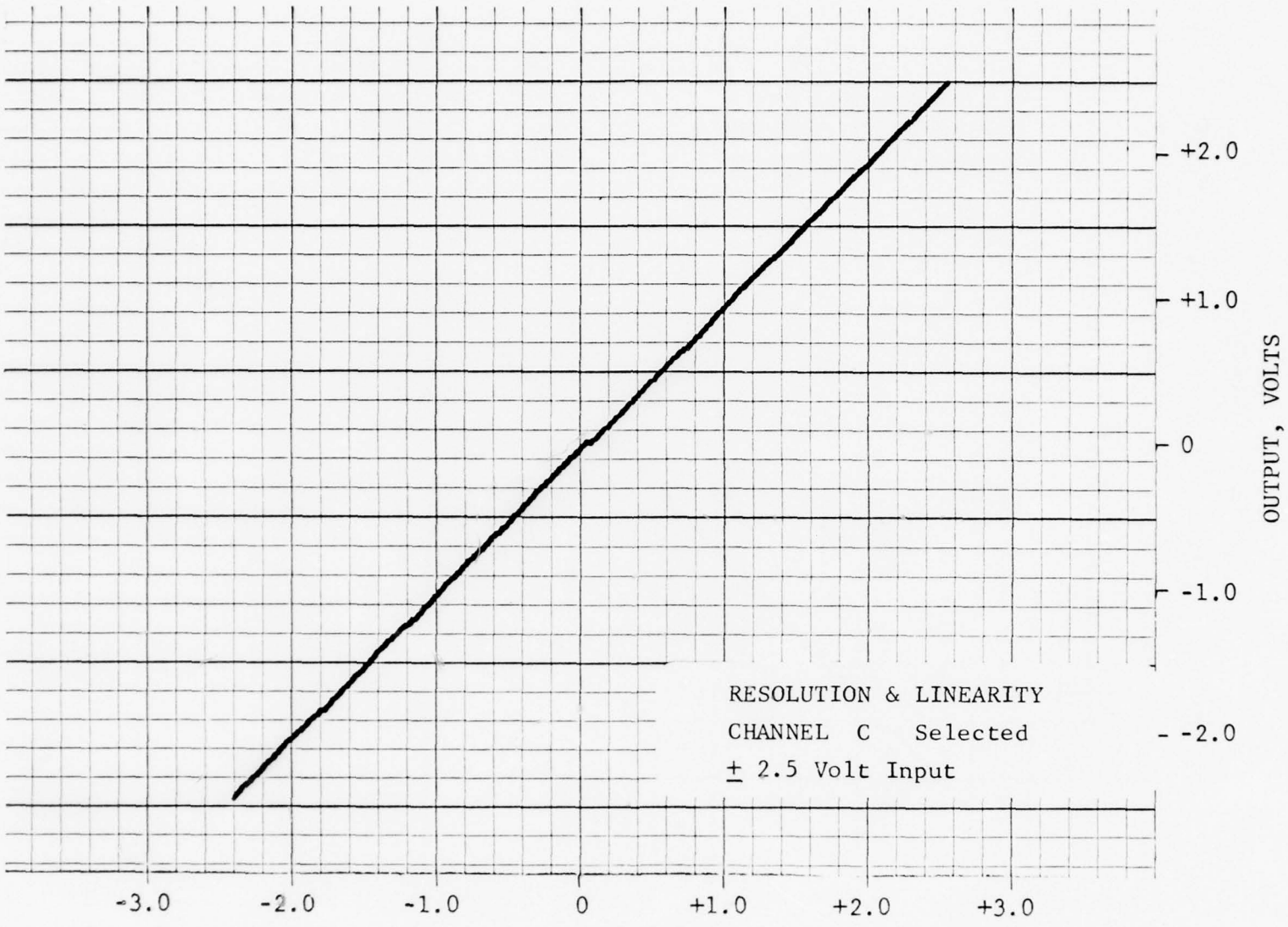

+2.0
+1.0
0
-1.0
-2.0
OUTPUT, VOLTS
RESOLUTION & LINEARITY
CHANNEL C Selected
± 2.5 Volt Input
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
INPUT, VOLTS

FIGURE 16

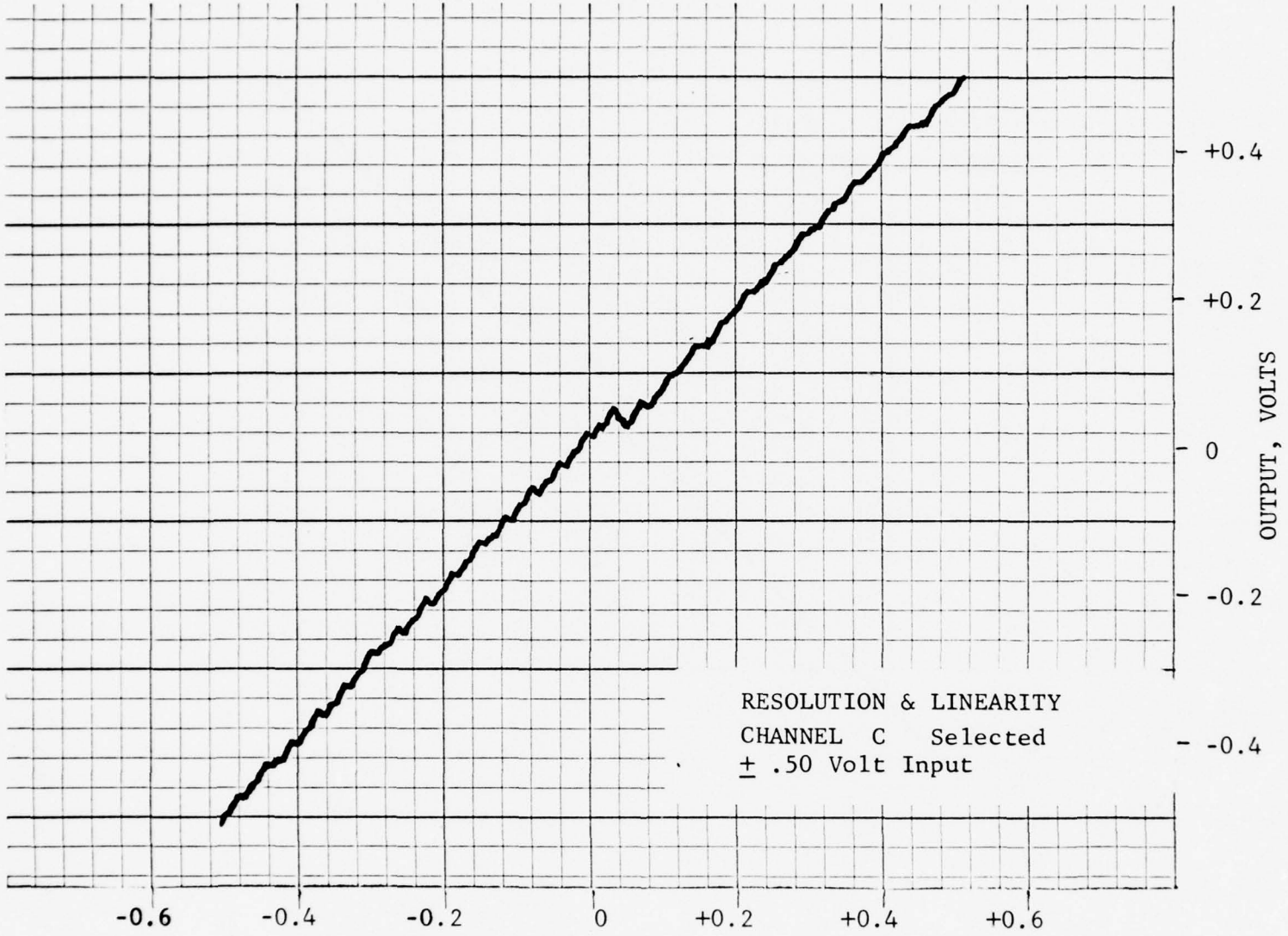

+0.4
+0.2
0
-0.2
-0.4
OUTPUT, VOLTS
RESOLUTION & LINEARITY
CHANNEL C Selected
± .50 Volt Input
-0.6
-0.4
-0.2
0
+0.2
+0.4
+0.6
INPUT, VOLTS

FIGURE 17

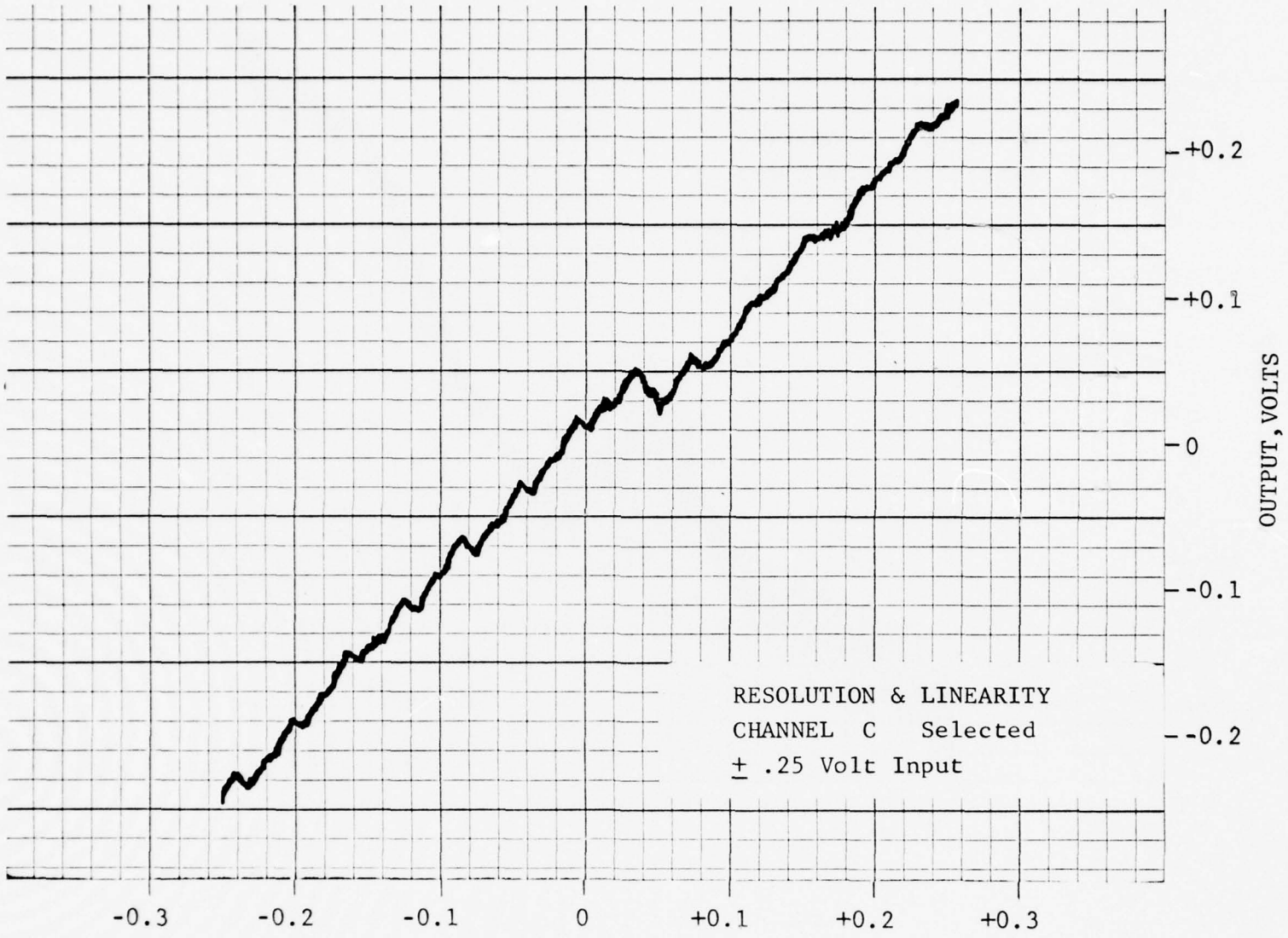

+0.2
+0.1
0
-0.1
-0.2
OUTPUT, VOLTS
RESOLUTION & LINEARITY
CHANNEL C Selected
± .25 Volt Input
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
INPUT, VOLTS

FIGURE 18

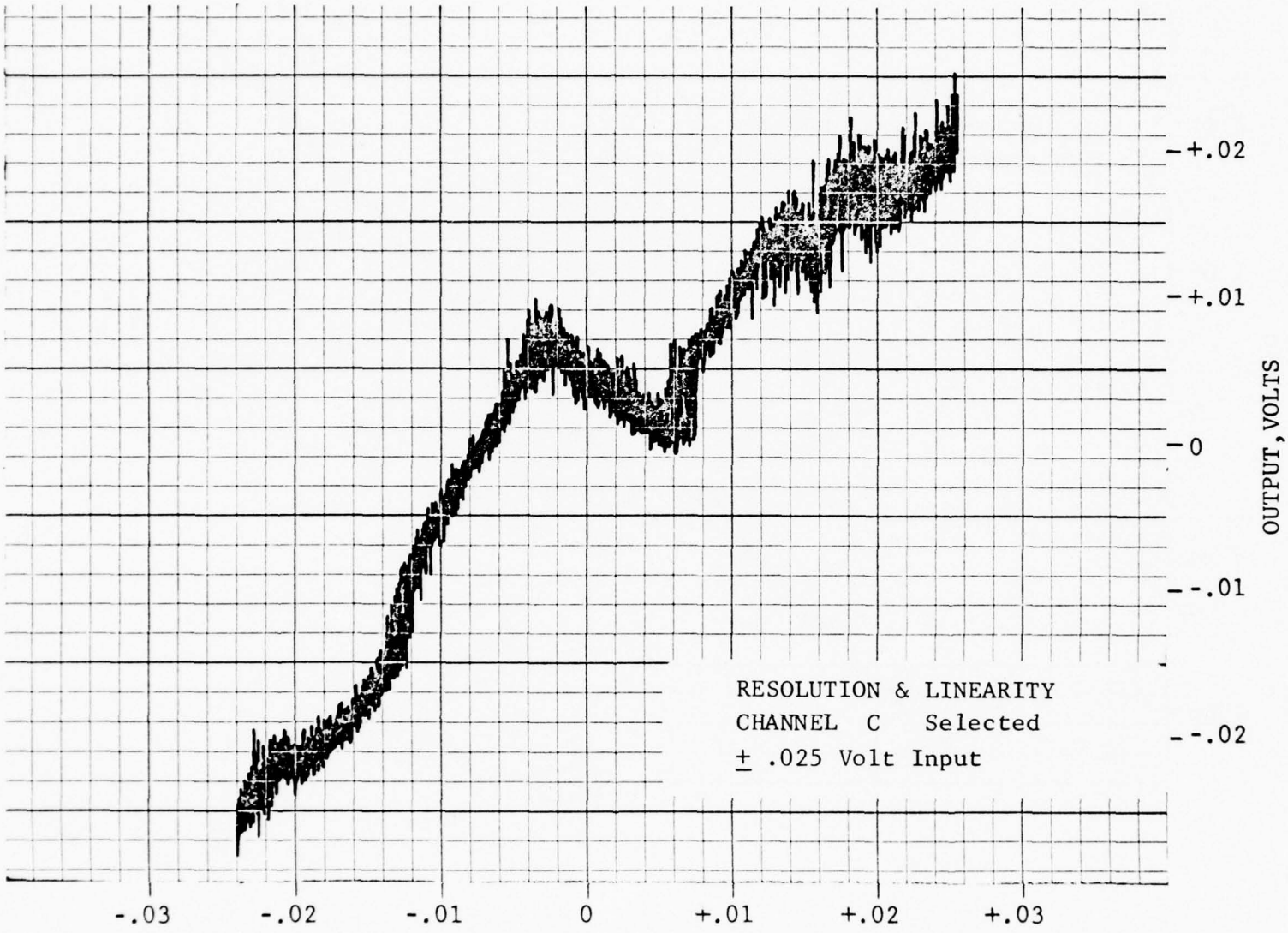

RESOLUTION & LINEARITY
CHANNEL C Selected
± .025 Volt Input
-+.02
-+.01
-0
--.01
--.02
OUTPUT, VOLTS
-.03
-.02
-.01
0
+.01
+.02
+.03
INPUT, VOLTS

FIGURE 19

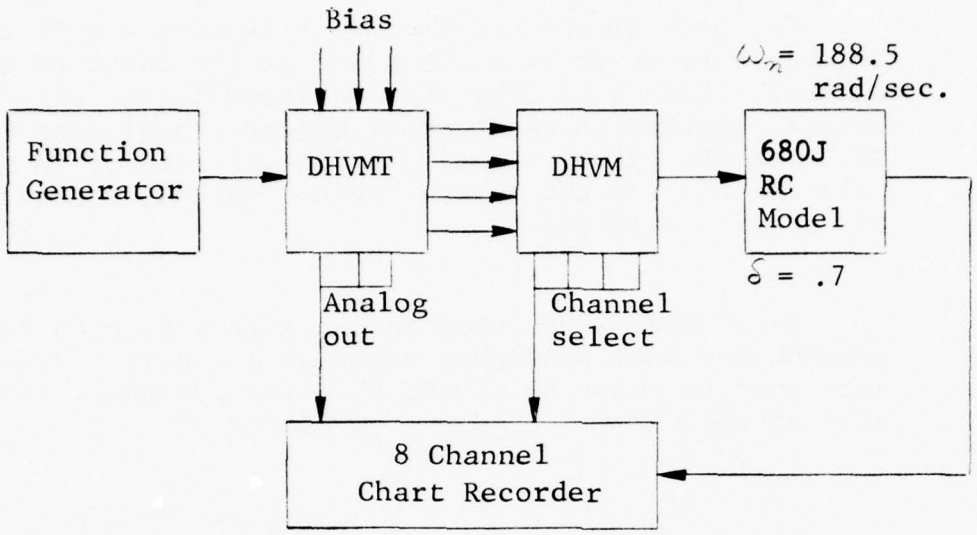


FIGURE 20 Signal Selection Test Set-Up

To measure the signal selections, a bias was set into each channel of the DHVMT as shown in TABLE 4:

TABLE 4

SIGNAL SELECTION CHANNEL BIAS

	Condition 1	Condition 2	Condition 3
Channel A	+1.50V	-1.50V	+.045V
Channel B	+1.00V	-1.00V	+.030V
Channel C	+ .50V	- .50V	+.015V
Channel D	.00V	.00V	.000V

For each of the conditions in TABLE 4 a $\pm$ 2V triangular wave at .5 Hz was applied to the input of each channel. Both D.C. bias and modulated inputs were recorded, along with the channel select signal from the DHVM and the output signal from the RC filter. A zero volt output from the channel select circuit indicated the channel selected.

An RC Model was used in the test set-up to represent the 680J secondary actuator bandpass. The circuit used is shown in FIGURE 21. The frequency response plot of the circuit is shown in FIGURE 22.

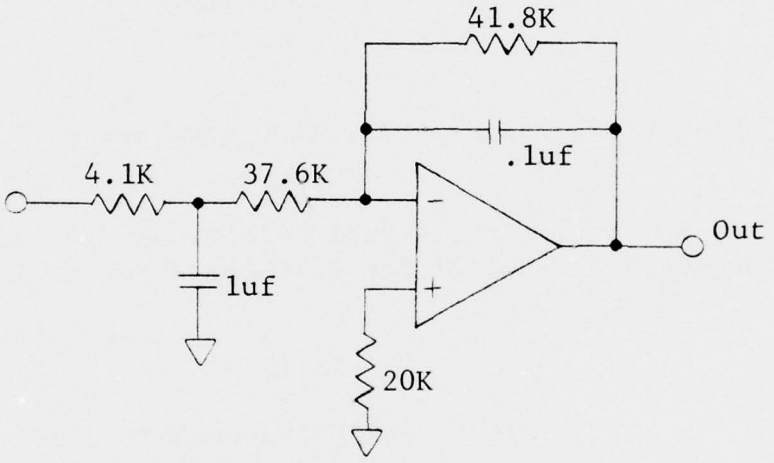


FIGURE 21 680J RC Model

The basic tests were conducted with the DHVMT operating at 200 updates/sec. and the DHVM at 1465 updates/sec.

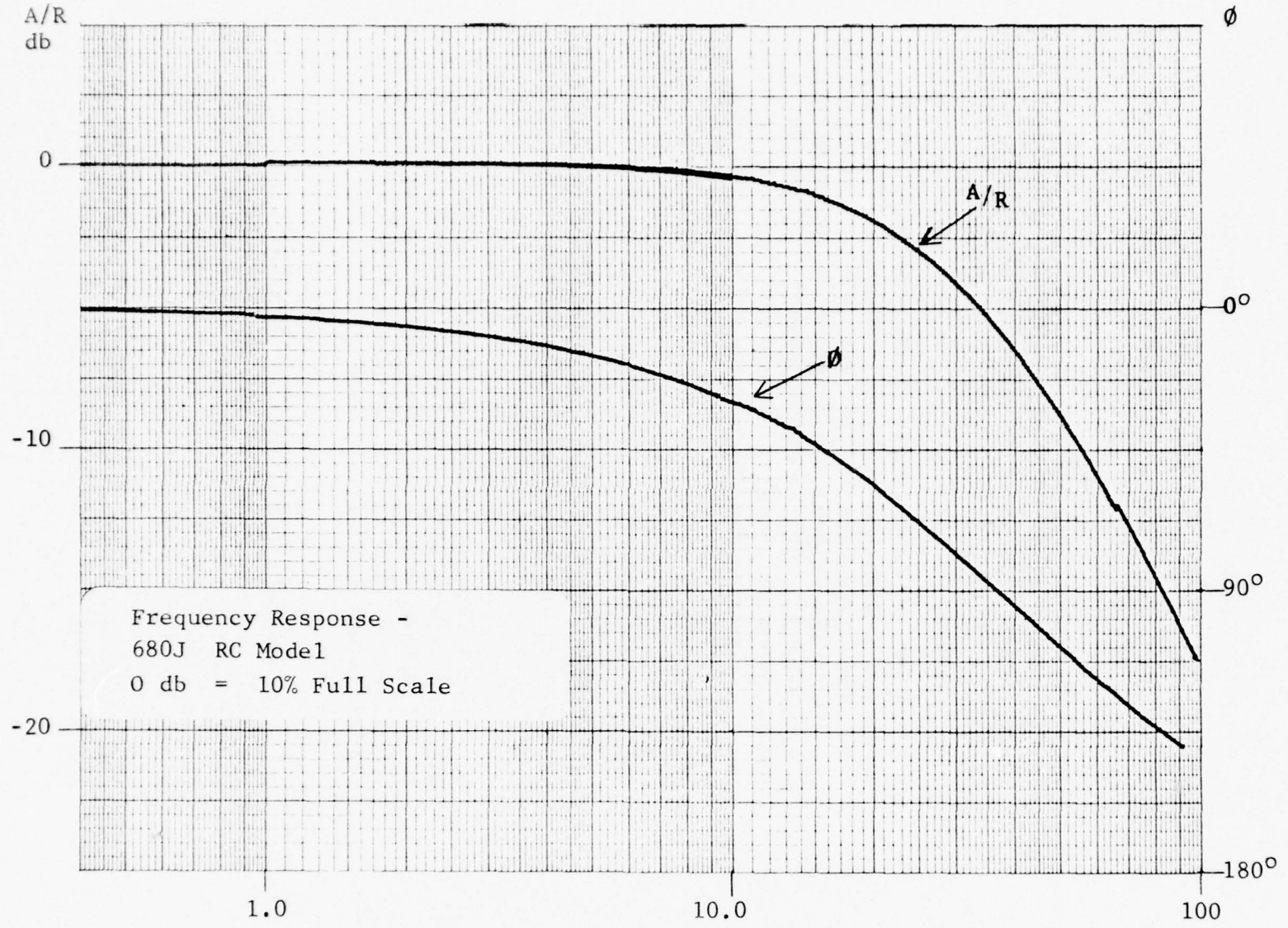

A/R
db
0
-10
-20
Ø
0°
90°
180°
A/R
Ø
Frequency Response -
680J RC Model
0 db = 10% Full Scale
1.0
10.0
100
FREQUENCY Hz

FIGURE 22

4.1.2.2 Test Results - Signal Selection

FIGURE 23 represents a reduction of measured data with the biases set as in Condition 1 and the .5 Hz input to Channel A. The heavier line indicates the DHVM output and that the low median signal had been selected at the proper time. The measured data indicated that the channels were selected at the proper time and within the 15 millivolt (digital value) noise amplitude.

FIGURE 24 is a sample of recorded data under Condition 2 with the input to Channel B. The conclusion from this basic data is that for all test conditions, the low median signal was properly selected within the noise tolerance of the DHVMT output. FIGURE 24 also demonstrates an occurrence that was observed several times while reducing the measured data. The data indicates that Channels B and C were selected simultaneously for a period of .005 sec. This time coincides with one sample period of the DHVMT. A study of the DHVM circuit design revealed that up to four channels could be indicated as selected simultaneously, if identical digital word values programmed the synchronous counters during the same sample period.

The indicated selection of two or more channels does not appear to be a problem, since the indication is reflecting the actual case where the two or more lowest value signals are identical and a low median signal is not actually present.

To evaluate the effect of a reduced update rate, the DHVMT update rate was set at 20 updates/sec. The results are shown in FIGURE 25. The results indicate that a .200 volt deviation exists between the theoretical level the channel should have been selected and the actual voltage level that the channel was selected. The explanation for the apparent deviation is that the input triangular wave of $\pm$ 2.00 volt at .50 Hz is

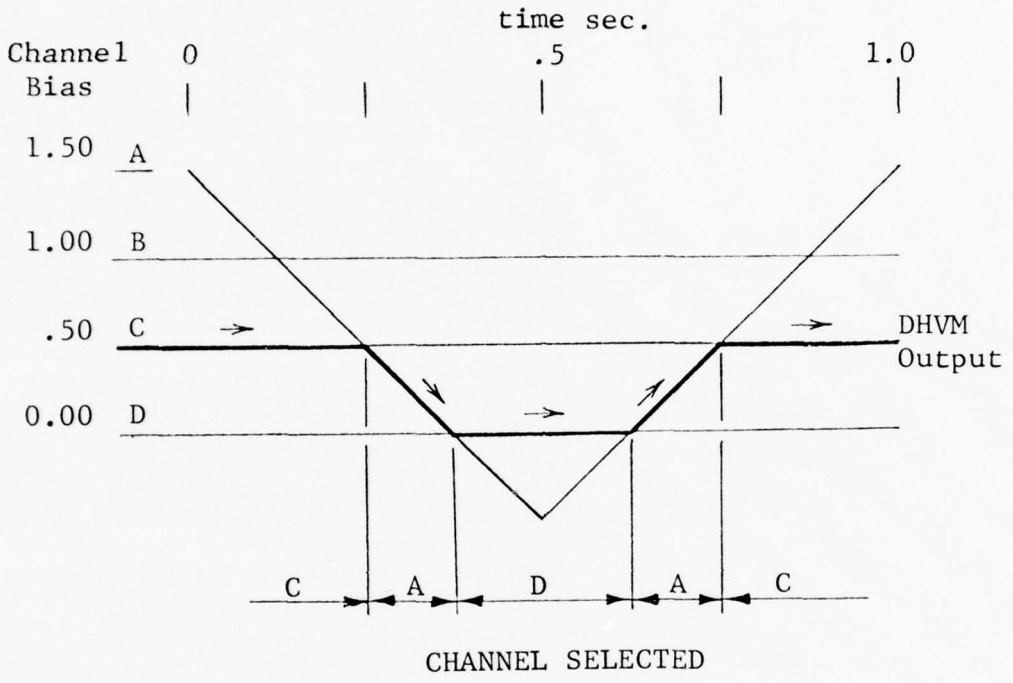


FIGURE 23 Low Median Signal Selection

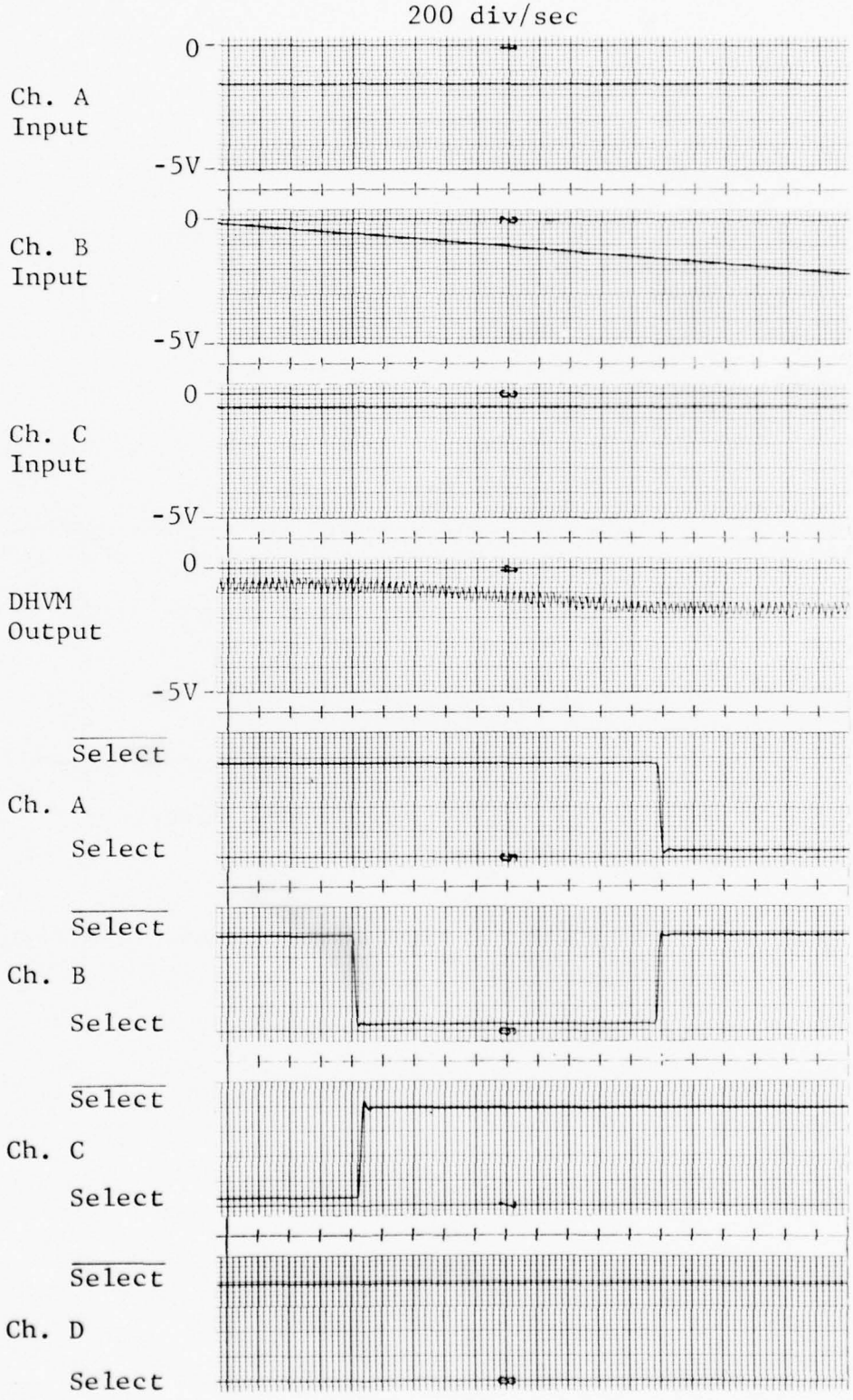


FIGURE 24 Channel Select Overlap

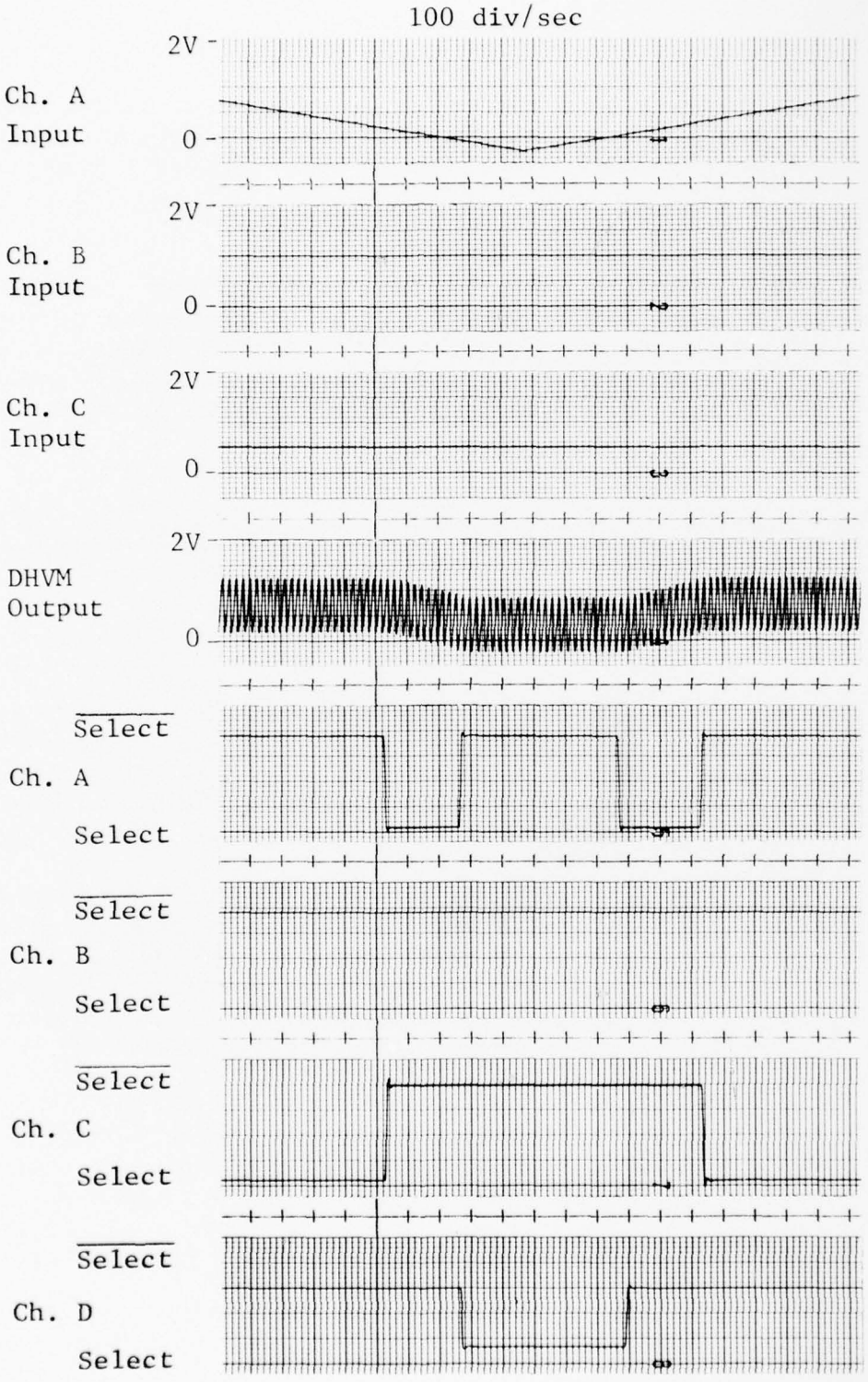


FIGURE 25 Channel Select Delay

changing at a rate of 4.00 volts/sec. at the input of the DHVMT and the DHVMT updates the output every 1/20 sec./update. Therefore, 4.00 volt/sec. times 1/20 sec./update is .200 volts/update.

Analysis of the data verifies that the DHVM will select the low median signal as presented to the input of the DHVM. As a system, a slower update can produce apparent errors in the selection of the low median signal when dynamic signals are used as an input to the system.

4.1.3 Out-Of-Tolerance Channel Determination

4.1.3.1 Test Description

The general set-up used to test the out-of-tolerance channel determination characteristics of the DHVM was the same as shown in FIGURE 20. The following three tests were conducted to evaluate the characteristics:

1. A precision voltage standard was used in place of the function generator as a test input to each channel. The positive and negative voltages required for a failure indication were recorded as a function of the error tolerance switch settings.

2. The function generator shown in FIGURE 20 was used to apply an input to all channels with DHVMT output operating synchronously. The minimum tolerance setting of the DHVM for no failure indication with a 10 Hz input was recorded.

3. The function generator shown in FIGURE 20 was used to apply an input to all channels with the DHVMT set to provide asynchronous inputs to the DHVM. The effect of the asynchronous settings on the failure reduction as a function of frequency and input amplitude was recorded. The bias pots were set for zero.

In addition to the preceding three tests, the effect on the out-of-tolerance determination characteristics with variations of the update rates and error counter settings was made qualitatively. The error settings and the update rate were varied and the effect was observed.

4.1.3.2 Test Results

TABLE 5 are the test results when the error tolerance switches were set at .195%, 10%, 15% and 50% of full scale with the DHVM error counters preset to 0010 and an update rate set at 488/sec.

TABLE 5

DHVM STATIC FAILURE LEVEL

Preset Failure Tolerance Level		Input Voltage Required to Fail Each Channel			
		A	B	C	D
.195%	+	.020	.018	.021	.019
	-	.018*	.019	.017*	.021
10%	+	1.036	1.037	1.035	1.042
	-	1.023	1.024*	1.030*	1.025

Present Failure Tolerance Level		Input Voltage Required to Fail Each Channel			
		A	B	C	D
15%	+	1.585	1.583	1.588	1.592
	-	1 573*	1.572	1.579*	1.572*
50%	+	4.994	4.994	5.017	5.003
	-	4.987*	4.995	5.015	5.007*

*All Four Channels Indicated a Failure

This data shows a random failure of all four channels when a single channel is driven negative toward the preset tolerance level. This characteristic was verified as follows:

The individual channels were adjusted to the same static output of $\pm$ .001 volt. When a negative bias was applied to a single channel and slowly increased, all channels would fail when the preset tolerance level was equal to the input bias.

The result of this testing indicates a problem with the basic circuit design. The circuit design described in Reference 1, AFFDL-TR-74-94, was reviewed to isolate the cause of the problem. The cause appears to be in the area of the input synchronous counters and the error counter "carry out" pulse.

The low limit counter starts when the first of the four input synchronous counters stops. The low limit counter stops when it "counts out" or when the second of

the four input synchronous counter stops. When the low limit counter "counts out", the "carry out" pulse from the 54163 module is 1 clock pulse wide. The time delay of associated gates and inverters amounts to approximately another clock time when operating at 1465 updates/sec. This "carry out" pulse opens the error counter NAND gates. Any input synchronous counter that is Hi during the error counter's "carry out" pulse duration will be determined to be in error. Since the preset negative error tolerance was approached by one channel very slowly, the three channels that remained at null made a Hi to Lo transition during the time that the "carry out" pulse from low limit counter was present at the NAND gates. This incremented their respective error counters to the failure limit. The input signals only have to be matched within one to two clock pulses equivalent to between .005 to .010 volts) for this problem to occur.

When the dynamic input of $\pm$ 10 volts at 10 Hz was applied to all inputs with the DHVMT operating synchronously, the minimum tolerance settings without any channel failures was .39% (Channels A and B would fail). This minimum tolerance level at 10 Hz refelects a dynamic mismatch in the DHVMT and not a problem with the DHVM detection.

In testing the out-of-tolerance channel determination while operating with asynchronous inputs to the DHVM, the method used to off-set the sampled data was to operate the DHVMT in the pseudo-asynchronous mode. The time delays on the rear panel of the DHVMT were adjusted to the desired delay setting. Operation in this mode provided the method of simulating the amount of time that the sample times would be off-set. Actual hardware would have a continuously varying sample off-set time because the clocks are not synchronized to the same rates.

Static operation in this mode indicated that there is no difference in detection characteristics than the operation in a synchronous mode. However, dynamic operation indicated that the out-of-tolerance detection is amplitude and frequency sensitive. FIGURE 26

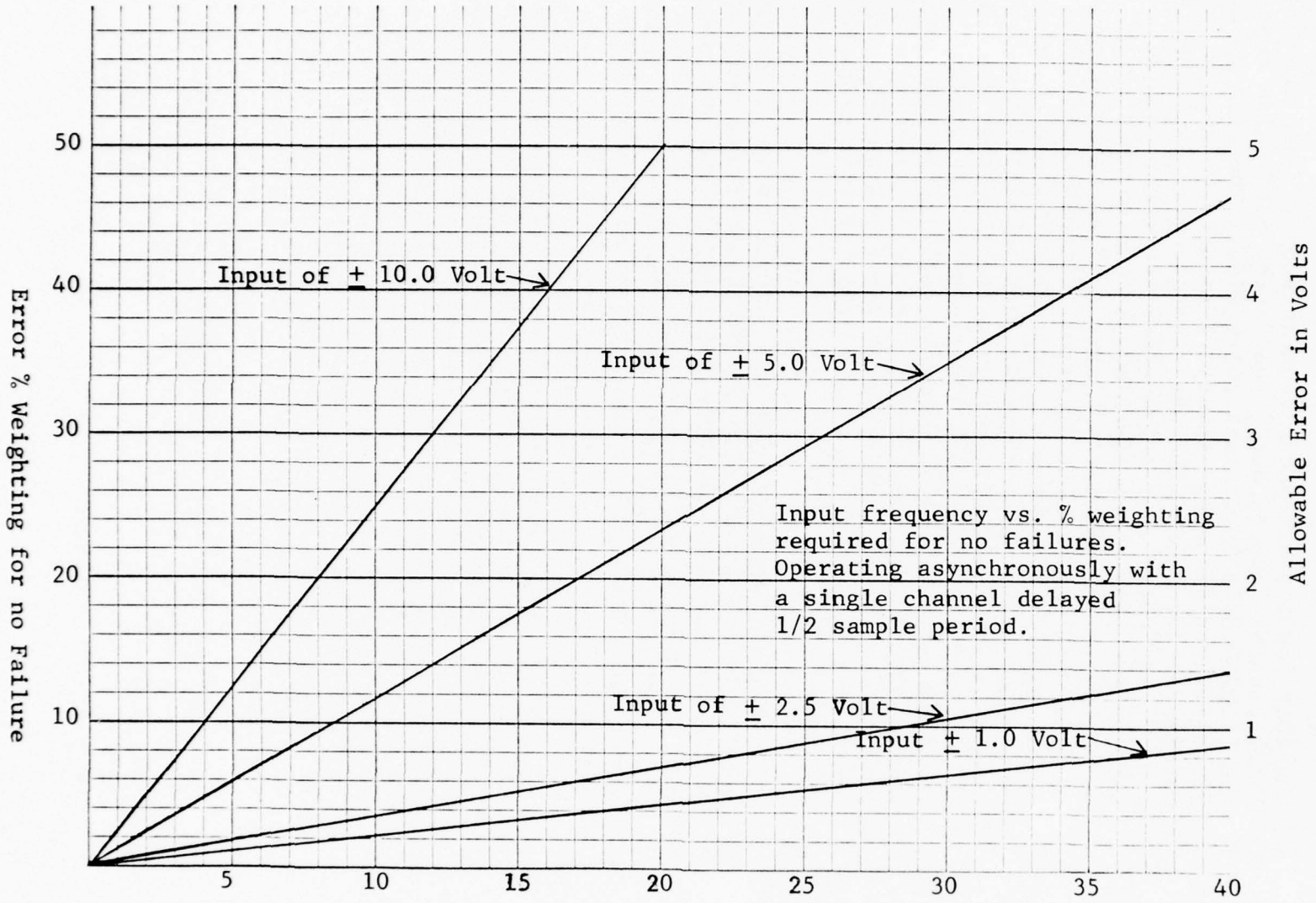

Error % Weighting for no Failure
50
40
30
20
10
Input of ± 10.0 Volt
Input of ± 5.0 Volt
Input frequency vs. % weighting required for no failures. Operating asynchronously with a single channel delayed 1/2 sample period.
Input of ± 2.5 Volt
Input ± 1.0 Volt
5
10
15
20
25
30
35
40
Input Frequency as a % of the Sample Frequency
Allowable Error in Volts
5
4
3
2
1

FIGURE 26

and 27 show the detection characteristic of input levels of ± 1.0 volt, ± 2.5 volt, ± 5.0 volt and ± 10 volt for sine wave inputs. The "X" axis is represented as the input frequency (for example, 100 samples/sec. with an input frequency of 15 Hz would be 15% on the "X" axis). The "Y" axis is the setting on the error tolerance switches to operate with no failures, expressed as a percent of full scale (± 10 volts). The data in FIGURE 26 was measured with the Channel A sample time off-set by 50% of a sample period. FIGURE 27 data was measured with the Channel A sample time off-set by 25% of a sample period.

An example of how data may be applied is to assume a system has a full scale input of ± 10 volts, an asynchronous sample rate of 80 samples/sec. and a maximum error between channels of 5% F.S. The maximum input frequency for no failure operation is 2% of 80 Hz or 1.6 Hz. This is based on the assumption that the asynchronous clocks will reach a maximum skew of 50% of a sample period (which is the worst case). This indicates that a system being updated at 80 times per second should have an input and output bandwidth limited to 1.6 Hz or less. Variation in the update rates in the DHVM does not change this characteristic. The only effect of the DHVM update rate is to change the time to detect the error (because the error would be recognized more or less often).

Variations in the error counter did not directly affect the DHVM's ability to detect an out-of tolerance channel. The effect of the error counter is that it provides a method to delay the DHVM from taking action to remove an out-of-tolerance channel for a period of time that would prevent transients from failing any one channel. The time delay is proportional to the reciprocal of the update rate in Hz times the number of allowable errors counted. Since the error counters are incremented up and down,

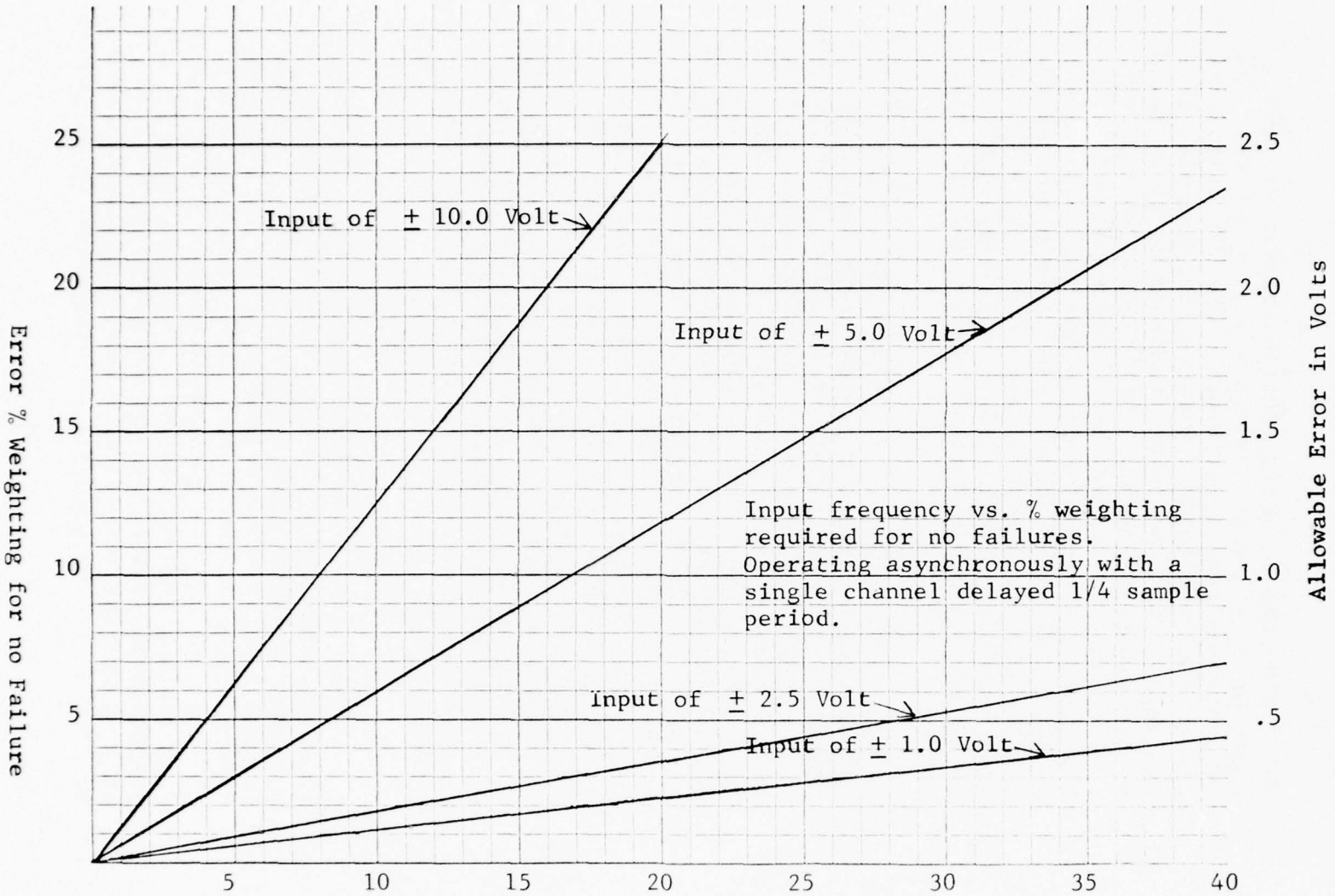

25
20
15
10
5
2.5
2.0
1.5
1.0
.5
Input of ± 10.0 Volt
Input of ± 5.0 Volt
Input frequency vs. % weighting required for no failures. Operating asynchronously with a single channel delayed 1/4 sample period.
Input of ± 2.5 Volt
Input of ± 1.0 Volt
5
10
15
20
25
30
35
40
Error % Weighting for no Failure
Allowable Error in Volts
Input Frequency as a % of the Sample Frequency

FIGURE 27

continuous transients could eventually cause failure of a channel if the transients are long enough in duration and occur repeatedly.

4.1.4 Operation and Voting Ability after Channel Failures

4.1.4.1 Test Description

The test set-up in FIGURE 28 was used to verify the ability of the DHVM to operate and vote after channel failures. The affect of simultaneous failures was also evaluated using this test set-up.

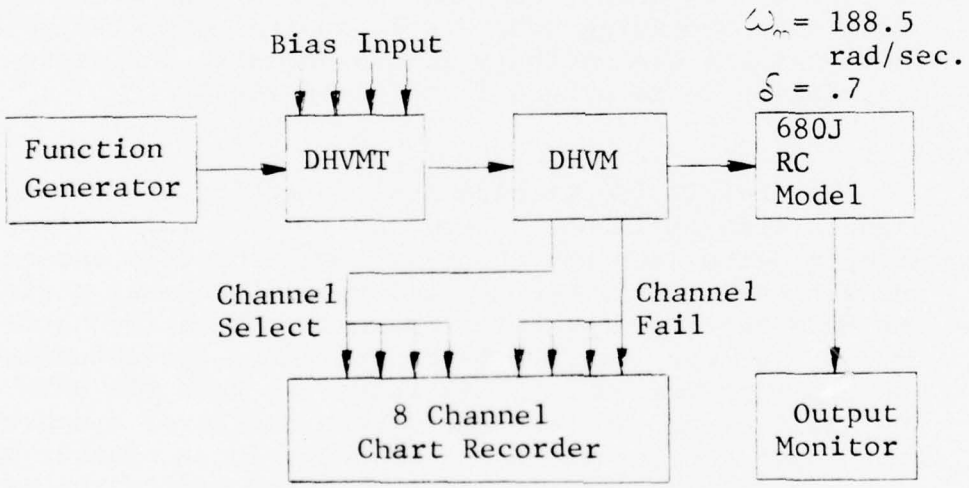


FIGURE 28 Voting Ability Test Set-Up

The function generator was used as a parallel input to all four channels. The channel select and channel fail signals were recorded on the chart recorder while the output of the RC Model was monitored on an oscilloscope. Hardover inputs were injected at the DHVM bias inputs. Null failures were created by removing the function generator input from the channel or channels under test.

4.1.4.2 Test Results

The test results indicate a single channel failure by being out-of-tolerance, the DHVM had no problem in selecting a new low median signal. When two failures were injected simultaneously, the DHVM would select the highest of the two remaining values. When the third failure was injected, the DHVM switched into a 50% duty cycle mode providing a 0.00 volt analog output signal. These results are entirely consistent with the design description in Reference 1, AFFDL-TR-74-94.

The result for simultaneous injection of failure signals were different. Hardover ($\pm$ 5.0 volt) signals were injected into two channels simultaneously and output was recorded. When the injected signal was positive, the DHVM rejected those two channels. When the hardovers were negative, the DHVM kept those two channels. The apparent reason for this result is that the DHVM low-limit error counter starts when the first synchronous input counter stops. The second input counter that stops, resets the low-limit counter and starts the hi-limit counter. This causes the last two counters to stop in an error condition if the hi-limit is exceeded. Therefore, the two highest algebraic values will always be considered in error even though negative hardovers are applied to the two channels that remain active.

Failure transients on the output due to the DHVM selecting a new median low signal with injected failures were not observable. The reason for this is that

the DHVM switches to a new median low signal every update period. Therefore, a single hardover or grounded input cannot be present at the output.

4.1.5 Summary of Phase I Test Results

4.1.5.1 PWM Signal Linearity and Resolution

The average resolution measured is .37% of full scale input. The average linearity is .08%. Both resolution and linearity are dependent on the accuracy of the analog-to-digital converters used to input the DHVM and the number of bits that are used for the data portion of a digital word.

4.1.5.2 Low Median Signal Selection

The DHVM correctly selects the low median signal from its four input signals.

The DHVM does indicate two or more channels selected if the input values are identical. No operational problems were observed with the channel selection.

4.1.5.3 Out-Of-Tolerance Channel Determination

The DHVM will fail all four channels if one channel is equal to the negative tolerance level and the other three channels are matched within .010 volts. This is a design problem that needs to be solved.

The out-of-tolerance detection is amplitude and frequency sensitive during asynchronous operation. This is a characteristic that limits the usefulness of

the DHVM for general application and needs to be changed.

4.1.5.4 Operation and Voting Ability after Channel Failure

Failure transients in the output were not observed for the first two injected failures. The third failure initiates a 50% duty cycle output.

The DHVM rejects the two highest algebraic channels when two hardover failures are injected simultaneously, a characteristic which in application should not be a problem.

4.2 Phase II

This phase of testing was conducted to establish the effect of driving an electro-hydraulic control system with the output of the DHVMT and DHVM simulating a DAIS configuration. The Hybrid Flight Control Simulator (HFCS) was used as the electro-hydraulic control system and was programmed to simulate 680J pitch axis hardware.

To evaluate the general effect of using a pulse width modulated signal as a direct input into an electro-hydraulic actuator, the DHVM was set up to provide the input to the HFCS during the Phase II preliminary testing. The result of this preliminary evaluation was that although the electro-hydraulic actuator will act as a pulse width demodulator, the servo valves respond too well to the pulse width modulation frequency. This response causes the servo valves to operate in a "bang-bang" mode (switching back and forth from hardover to hardover) with the potential of damaging the first stage of the servo valves. In addition, the response of the 680J HFCS simulation to the direct pulse width command

signals allowed a considerable amount of the pulse width modulation frequency to appear on the motion output of the secondary actuator. Although a small amount of high frequency dither is not undesirable for the operation of a servo system, the large amount of the pulse width modulation dither when used as a direct input to a servo system was undesirable from a distortion and wear aspect.

During this preliminary evaluation, the pulse width modulation update frequency was varied from 91.5 updates/sec. to 1465 updates/sec. As expected, the amount of motion at the modulation frequency reduced with increasing update rate. As a result of the preliminary testing, the update frequency was set to 1465 updates-sec. (the maximum rate available for the DHVM) for all subsequent tests. In addition, a low pass filter having a break frequency at 150 Hz was inserted between the DHVM and HFCS as a PWM demodulator. The combination of the high pulse width modulation frequency and low pass filter reduced the modulation dither to an acceptable level for the subsequent testing.

4.2.1 Base Line HFCS Testing

4.2.1.1 Base Line Test Description

A model of the 680J secondary actuator was programmed on the HFCS using References 3 and 4 as a guide. Test data was recorded as a baseline to compare to data taken with the DHVMT and DHVM interfaced in the system.

---

3. Hooker, David S., et.al., "Survivable Flight Control System", Final Report, AFFDL-TR-73-105, December 1975
4. Amies, Gerald E., et.al., "Survivable Flight Control System", Interim Report No. 1, Studies, Analyses and Approach, AFFDL-TR-71-20, Supplement 3, May 1971

The base line data test set-up is shown in FIGURE 29.

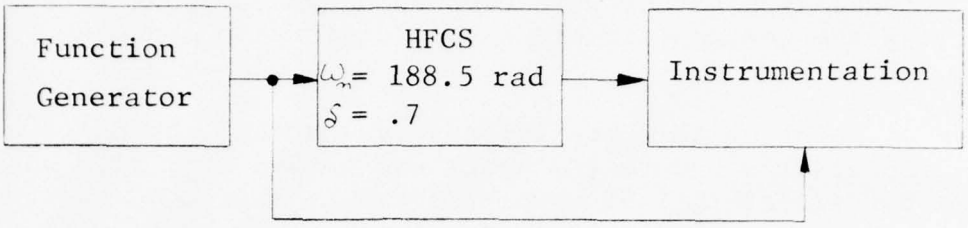


FIGURE 29 Block Diagram HFCS Base Line

The HFCS was set-up as shown in FIGURE 30 to model the response of the 680J secondary actuator.

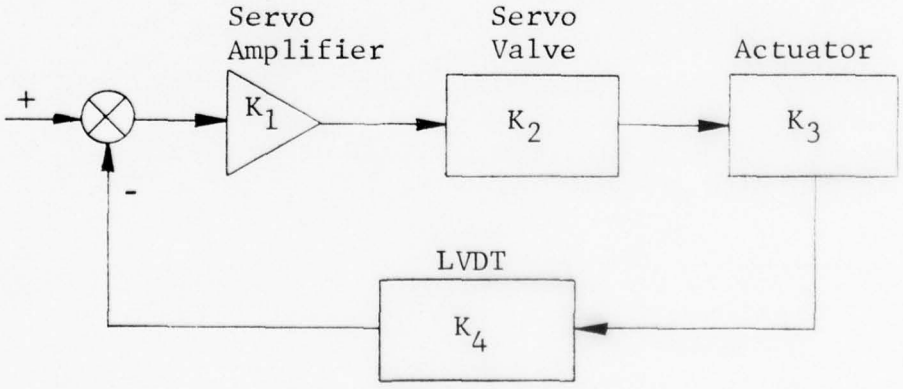


FIGURE 30 HFCS - 680J Secondary Model

Where:

K_1 = 1.71 ma/v

K_2 = 1.04 cis/ma

K_3 = .188 in^2

K_4 = 20 v/in.

4.2.1.2 Test Results

FIGURES 31 through 34 are baseline performance measurements of the HFCS with the 680J response set-up.

FIGURE 31 shows the response of the simulation bracketed with the gain and phase limits of the 680J secondary actuator response taken from Reference 4, Page 130.

FIGURES 32, 33 and 34 are X-Y plots with input amplitudes of $\pm$ 2.5 volt, $\pm$ .25 volt and $\pm$ .025 volt. This data indicates that the system linearity is better than 0.5%, the resolution is better than 0.15% and hysterisis is less than 0.2%. The stair stepping shown in the expanded linearity plot of FIGURE 33 is typical for a small drive area actuator because the seal friction requires a high percentage of the available output force.

The output signal distortion was measured and charted in TABLE 6. The input signal distortion was less than .15% for all frequencies and amplitudes. The data indicates that the higher amplitude output signals have less distortion. Actuator friction

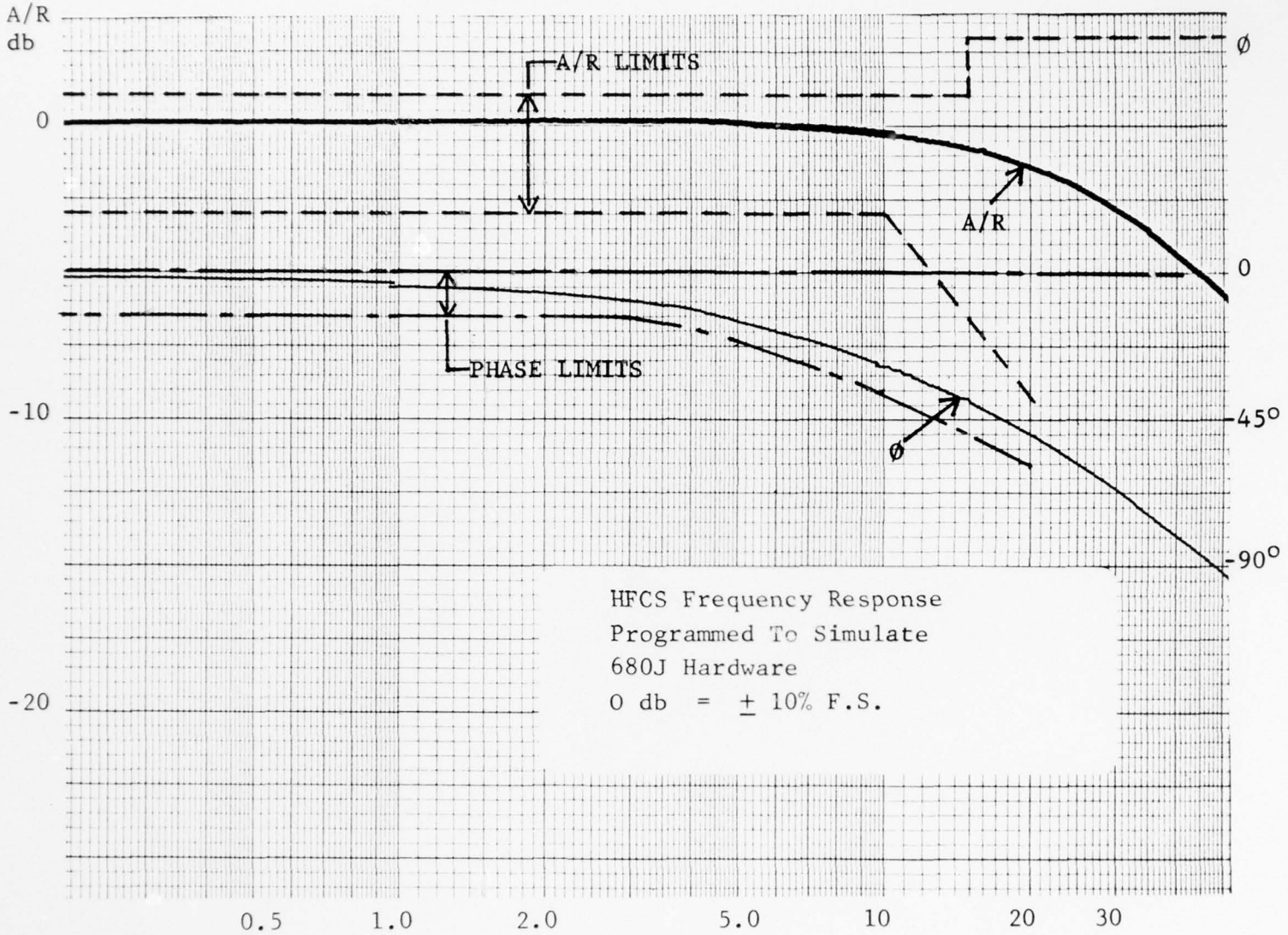

A/R
db
A/R LIMITS
0
A/R
Ø
0
PHASE LIMITS
-10
-45°
Ø
-90°
HFCS Frequency Response
Programmed To Simulate
680J Hardware
0 db = ± 10% F.S.
-20
0.5
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 31

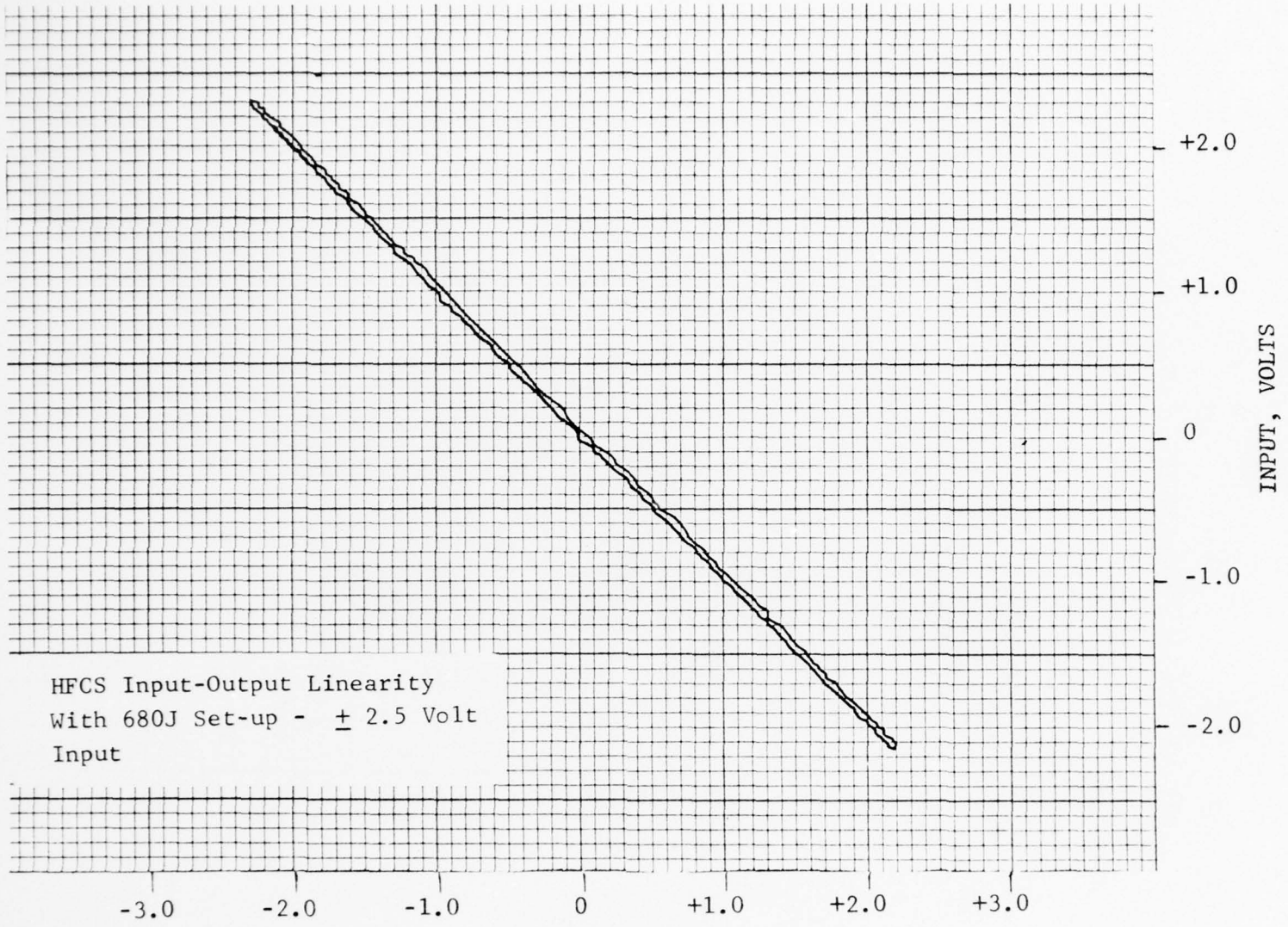

+2.0
+1.0
0
-1.0
-2.0
INPUT, VOLTS
HFCS Input-Output Linearity
With 680J Set-up - ± 2.5 Volt
Input
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
OUTPUT, VOLTS

FIGURE 32

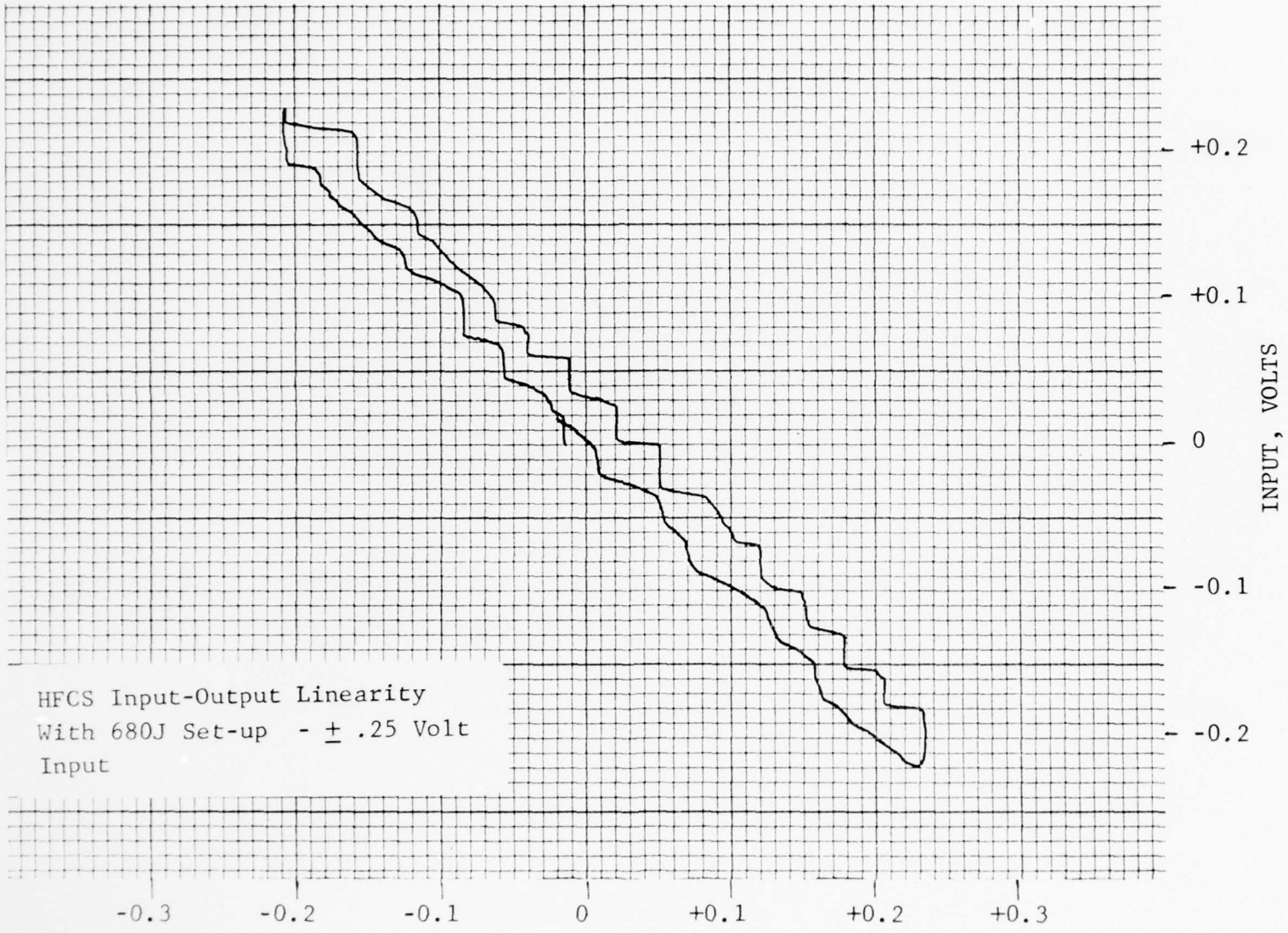

+0.2
+0.1
0
-0.1
-0.2
INPUT, VOLTS
HFCS Input-Output Linearity
With 680J Set-up - ± .25 Volt
Input
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
OUTPUT, VOLTS

FIGURE 33

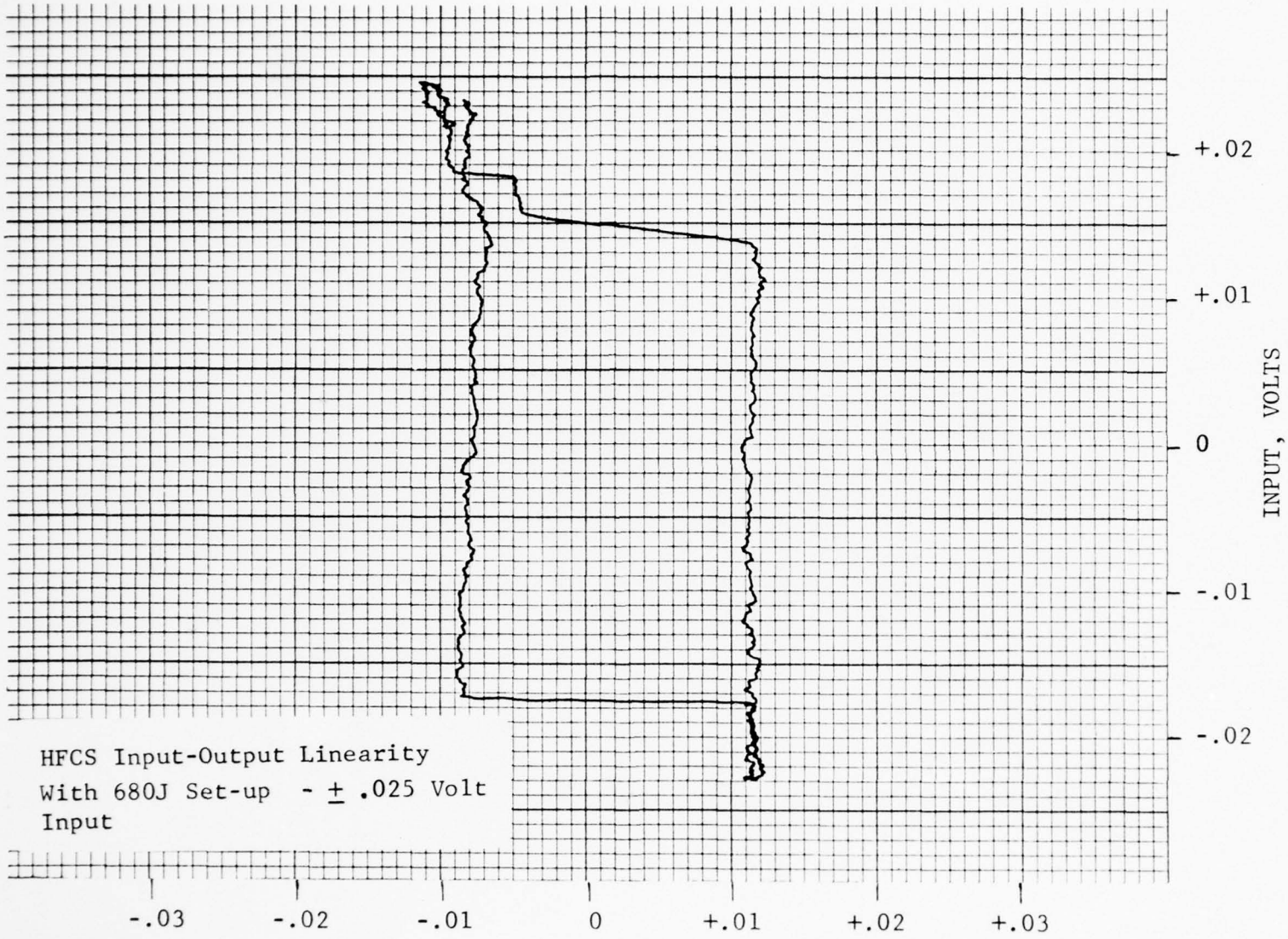

+.02
+.01
0
-.01
-.02
INPUT, VOLTS
HFCS Input-Output Linearity
With 680J Set-up - ± .025 Volt
Input
-.03
-.02
-.01
0
+.01
+.02
+.03
OUTPUT, VOLTS

FIGURE 34

affects the output signal distortion in this manner since with a constant friction level the percent distortion associated with the friction decreases with increasing output amplitude.

TABLE 6

OUTPUT SIGNAL DISTORTION WITHOUT DHVMT & DHVM

Input Freq. Hz	P-P Output Amplitude ± 1.0 Volt	± 2.0 Volt	± 5.0 Volt
5	7.0%	2.8%	2.0%
10	8.8%	4.0%	1.85%
20	9.5%	2.8%	1.80%
40	13.0%	3.0%	2.8%

In order to observe uniform distortion, a frequency sweep from 1.0 to 50 Hz at an amplitude of ± 5.0 volts was applied to the HFCS as an input. The input and output were recorded for reference comparison.

FIGURES 35 and 36 are the input-output relationship at frequencies of 10 and 40 Hz.

4.2.2 The Effect of Sample Rate Variation On The 680J Simulator

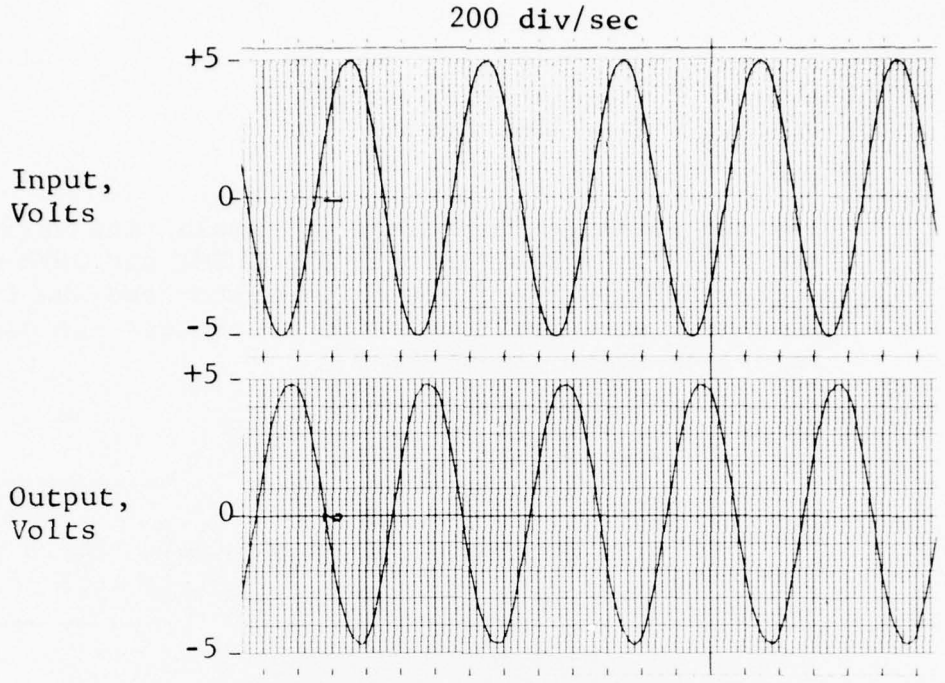


FIGURE 35 10 Hz Input-Output, Base Line

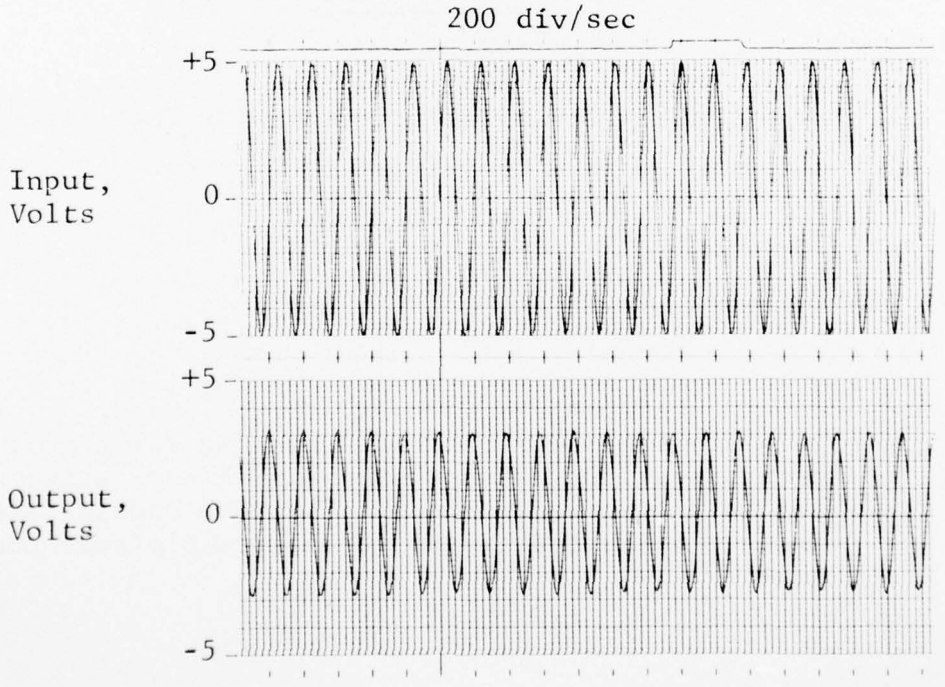


FIGURE 36 40 Hz Input-Output, Base Line

4.2.2.1 Test Description

To evaluate the effect of sample rate variation on the 680J Simulation output, the DHVMT and DHVM were inserted between the function generator and the 680J secondary actuator simulation to process the command input, as shown in FIGURE 37.

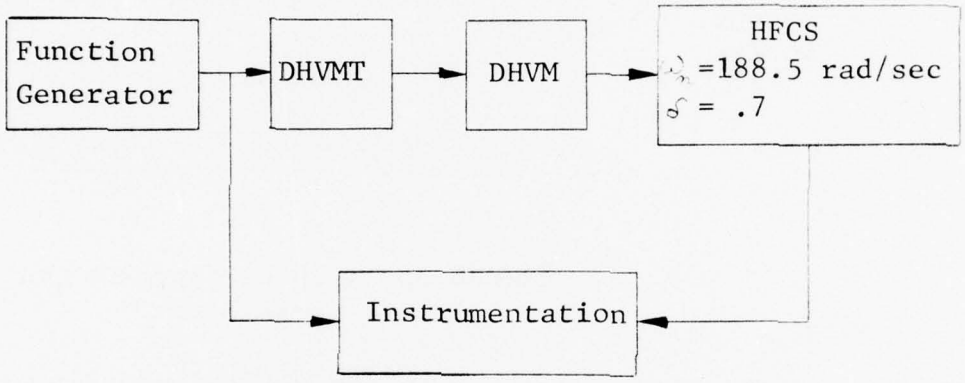


FIGURE 37 Sample Rate Variation Test Set-Up

The base line data was repeated for sample rate settings of 80, 125 and 400 samples/sec. while operating in a synchronous mode. The DHVM update rate was set at 1465 updates/sec. for all sample rate conditions.

4.2.2.2 Test Results

FIGURES 38, 39 and 40 represent the frequency response data with the DHVMT set at 80, 125 and 400 samples/sec. Comparing these plots to the base line indicates that the phase angle is affected more than the amplitude ratio. This is an expected result because there is a time delay of one update period each for the DHVMT and DHVM when the information is processed. TABLE 7 is a listing of expected, measured and base line phase shift at input frequencies of 1, 10 and 20 Hz. The values for the 400 samples/sec. are comparable to the base line, but the 80 samples/sec. are not comparable. This is because the output signals for the slower sample rates are quite distorted and the test instrumentation cannot properly evaluate the signal. When signal distortion is more than 10%, the frequency response analyzer plots

TABLE 7

PHASE LAG COMPARISON

Input Freq. Hz	Sample rate samples/sec.	Phase Lag in Degrees Base Line	Expected	Measured
1	80	4.5	11.9	9.0
1	125	4.5	7.6	8.0
1	400	4.5	5.7	6.5
10	80	29.5	76.9	58.0
10	125	29.5	60.8	54.0
10	400	29.5	41.0	43.0
20	80	49.5	144.4	112.0
20	125	49.5	112.4	103.0
20	400	49.5	72.8	81.0

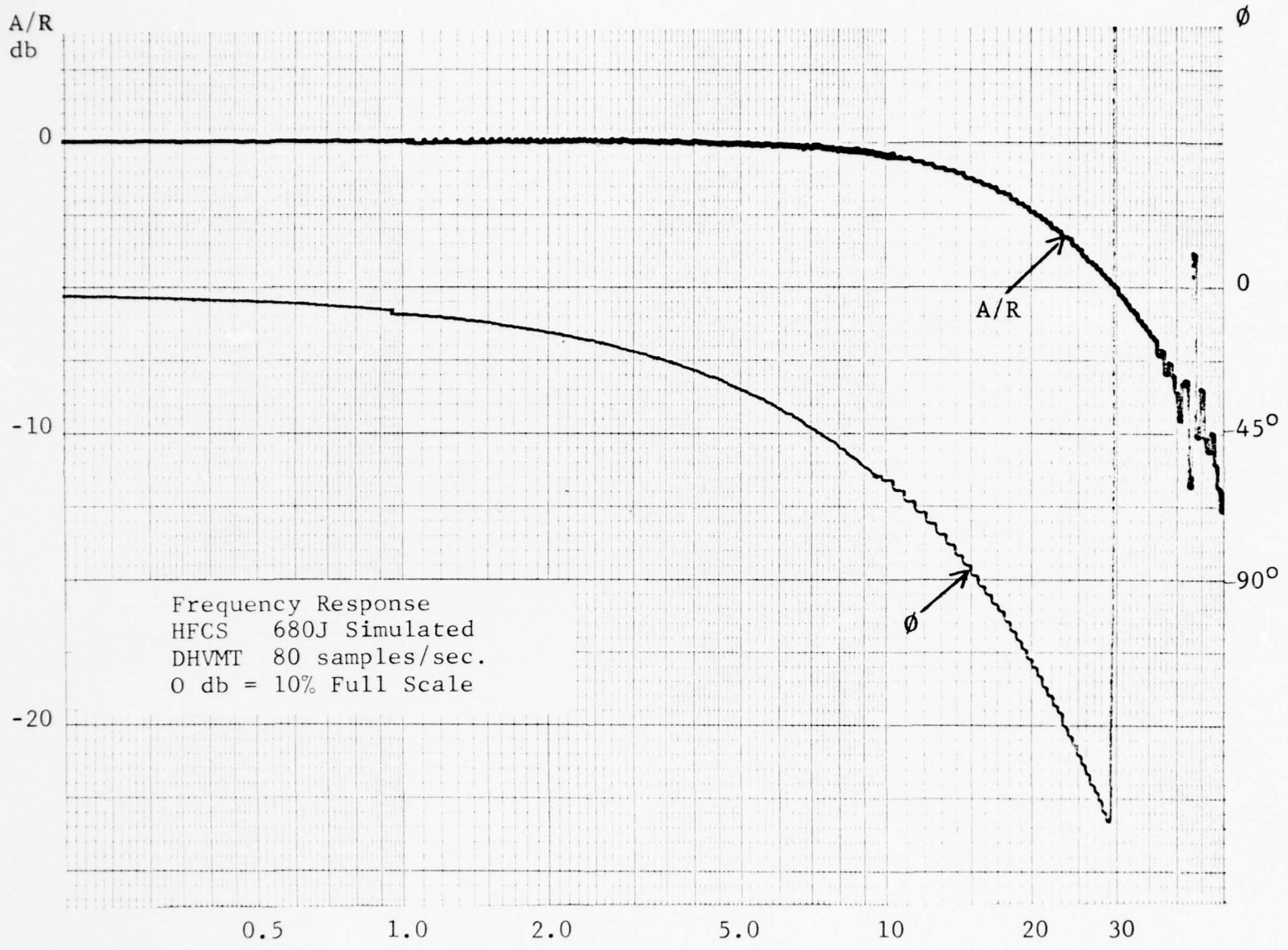

A/R
db
0
-10
-20
Ø
0
45°
90°
A/R
Ø
Frequency Response
HFCS 680J Simulated
DHVMT 80 samples/sec.
0 db = 10% Full Scale
0.5
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 38

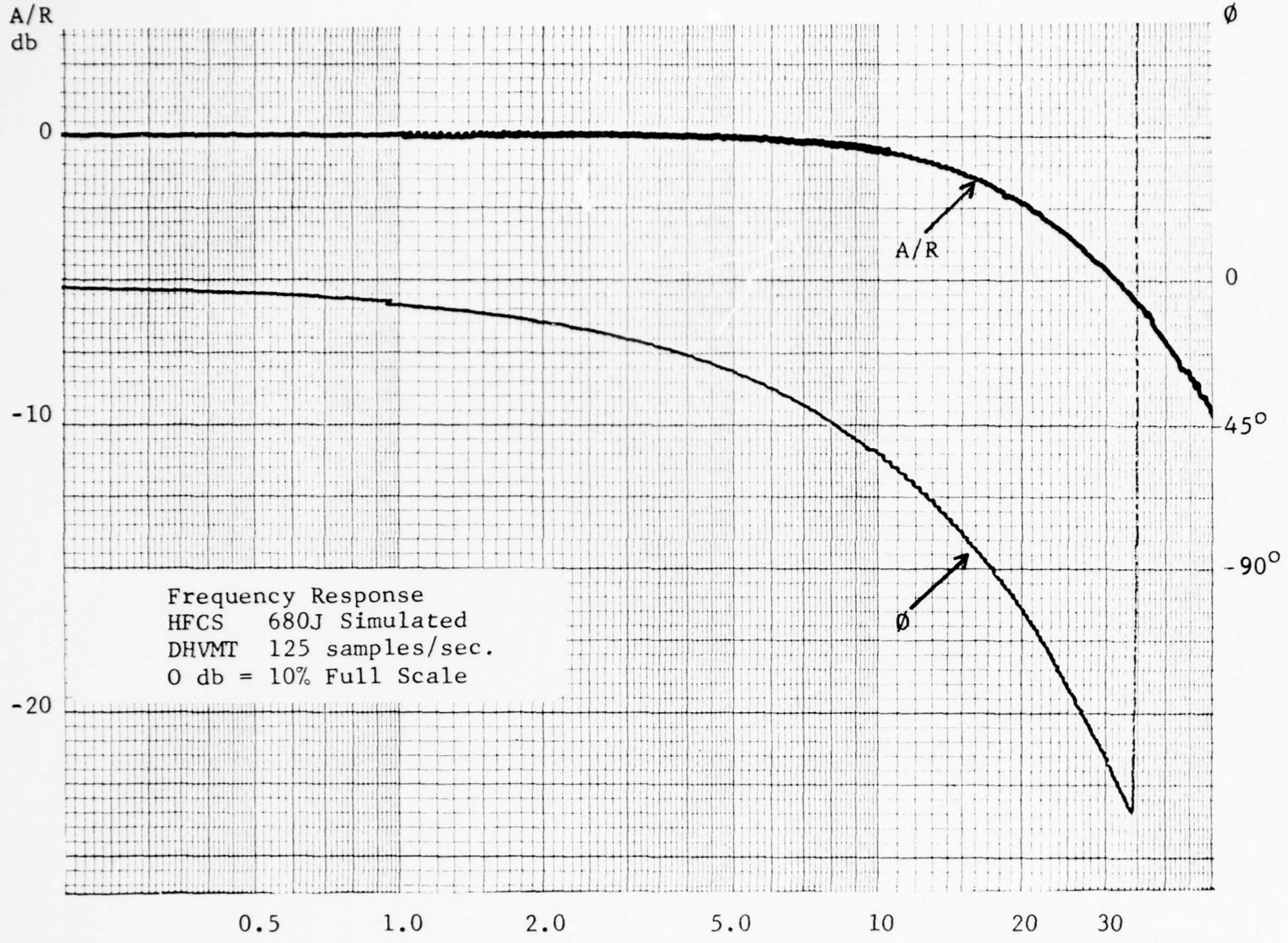

A/R
db
0
-10
-20
Ø
0
-45°
-90°
A/R
Ø
Frequency Response
HFCS 680J Simulated
DHVMT 125 samples/sec.
0 db = 10% Full Scale
0.5
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 39

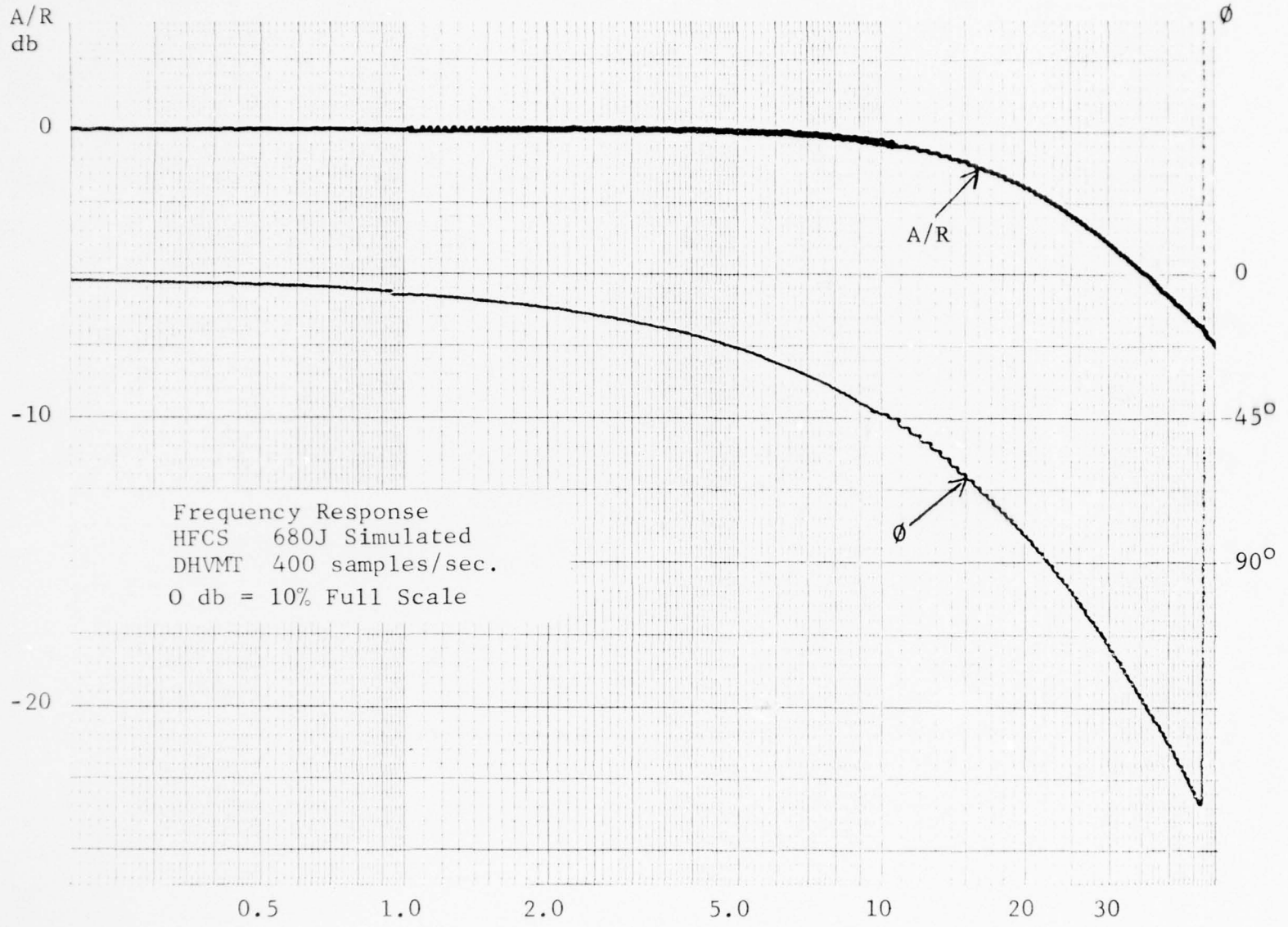

A/R
db
0
-10
-20
Ø
0
-45°
-90°
A/R
Ø
Frequency Response
HFCS 680J Simulated
DHVMT 400 samples/sec.
0 db = 10% Full Scale
0.5
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 40

are not valid (since Bode plots are based on a pure sine wave analysis). The expected phase angles listed in TABLE 7 are calculated values arrived at by adding phase angle associated with the time delay period to the base line phase angles.

The Bode plot on FIGURE 38 shows amplitude ratio degradation relative to the base line response (FIGURE 22). This is caused by input signal distortion at the lower sample rates affecting the measured sinusoidal response.

The amplitude burst on the amplitude ratio trace of FIGURE 38 reflects a modulation mode of the system input when the input frequency into the DHVMT approaches one-half of the sample frequency.

FIGURES 41 through 49 are the X-Y plots for inputs of $\pm$ 2.5 volt, $\pm$ .25 volt and $\pm$ .025 volt at sample rates of 80/sec., 125/sec. and 400/sec. The linearity remained unchanged compared to the base line. However, the resolution increased from .15% to .10% and the hysterisis was reduced from .20% to .15% compared to the base line test results. This is because the DHVM output allowed enough dither to the HFCS to reduce the actuator's inherent static friction effects on the actuator motion.

TABLE 8 is comparative signal distortion data for the three update rates. Referring to TABLE 7 of the base line data, the 400 samples/sec. rate closely compares to the base line data. The 80 samples/sec. is quite distorted by comparison.

FIGURES 50 through 55 are input-output traces of the frequency sweep at $\pm$ 5.0 volts at 10 Hz and 40 Hz frequency ranges at sample rates of 80, 125 and 400 samples/sec.

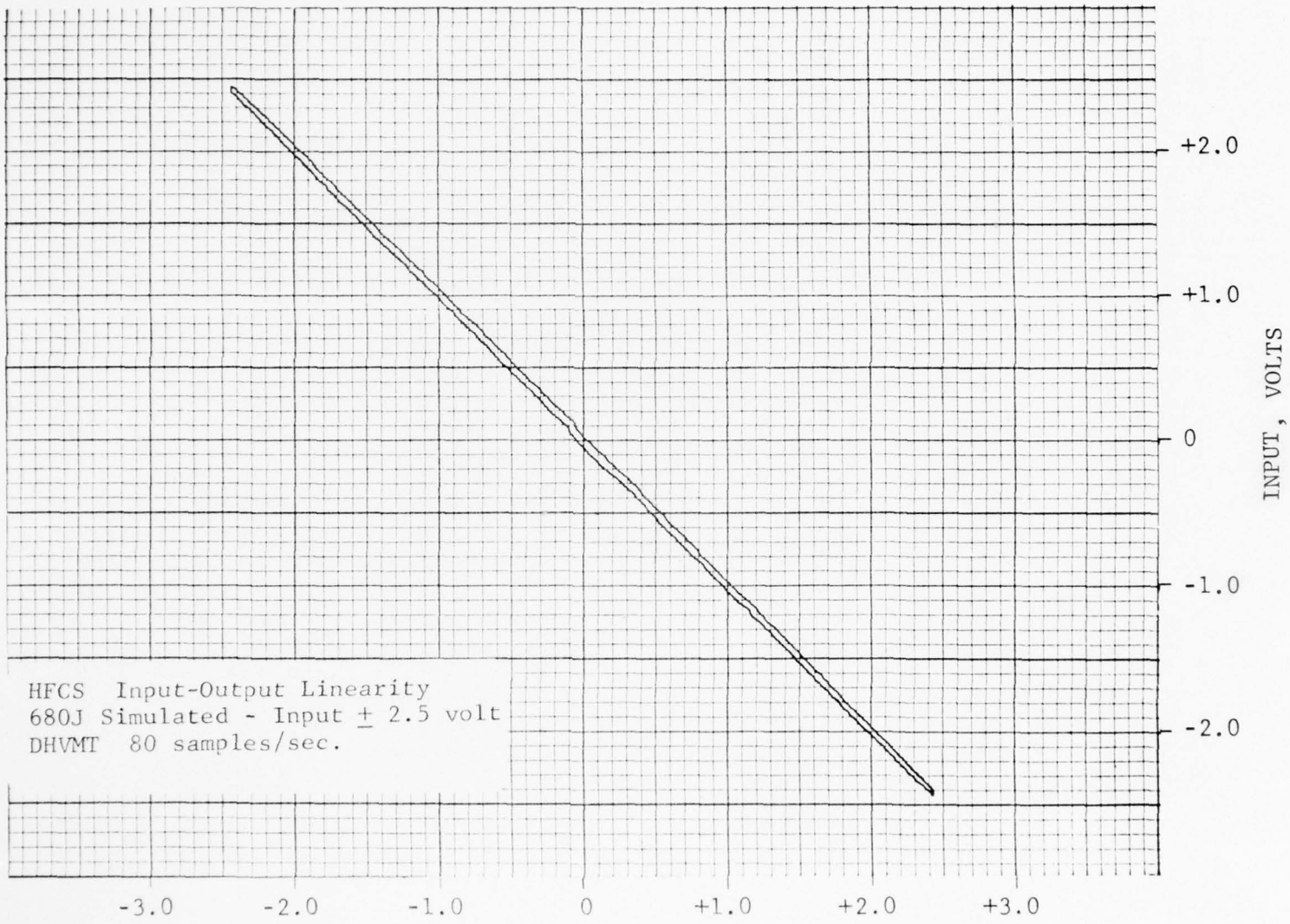

HFCS Input-Output Linearity
680J Simulated - Input ± 2.5 volt
DHVMT 80 samples/sec.
+2.0
+1.0
0
-1.0
-2.0
INPUT, VOLTS
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
OUTPUT, VOLTS

FIGURE 41

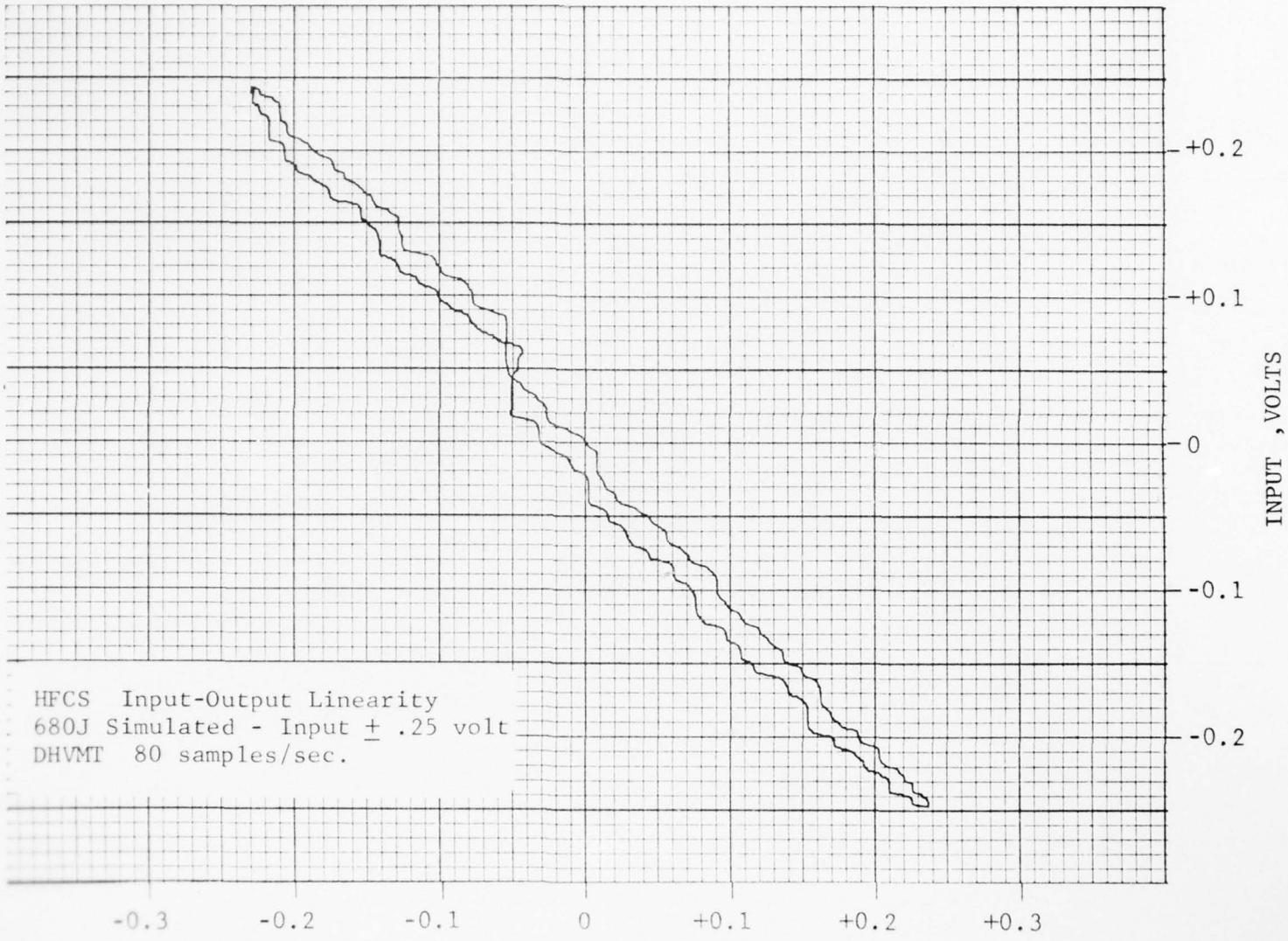
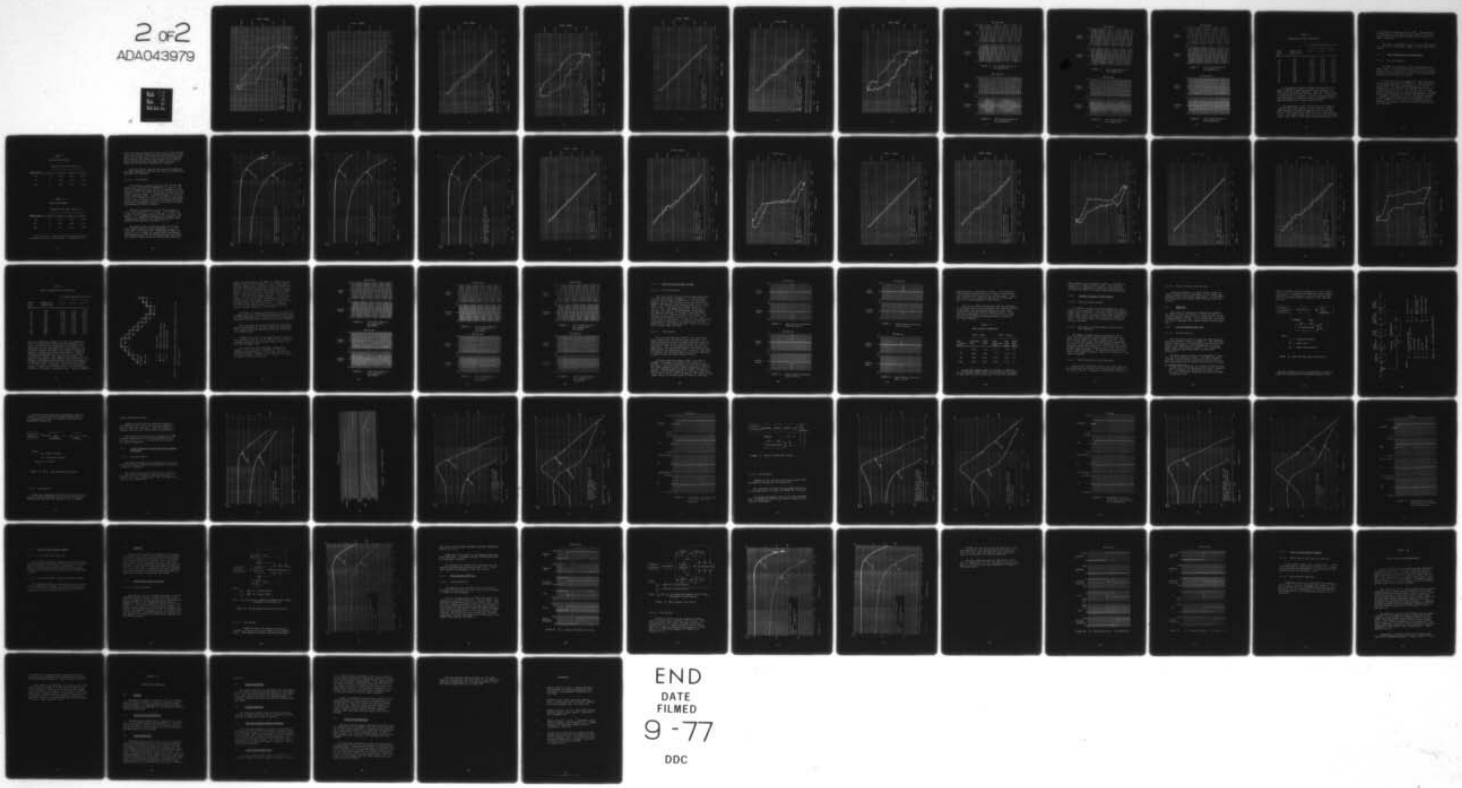

HFCS Input-Output Linearity
680J Simulated - Input ± .25 volt
DHVMT 80 samples/sec.
+0.2
+0.1
0
-0.1
-0.2
INPUT , VOLTS
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
OUTPUT , VOLTS

FIGURE 42

AD-A043 979 DYNAMIC DEVICES INC DAYTON OHIO F/G 1/4
THE EVALUATION OF A DIGITAL HARDWARE VOTER/MONITOR IN AN AIRCRA--ETC(U)
MAY 77 H W SCHREADLEY F33615-75-C-3068
UNCLASSIFIED AFFDL-TR-77-30 NL

2 OF 2
ADA043979



END
DATE FILMED
9-77
DDC

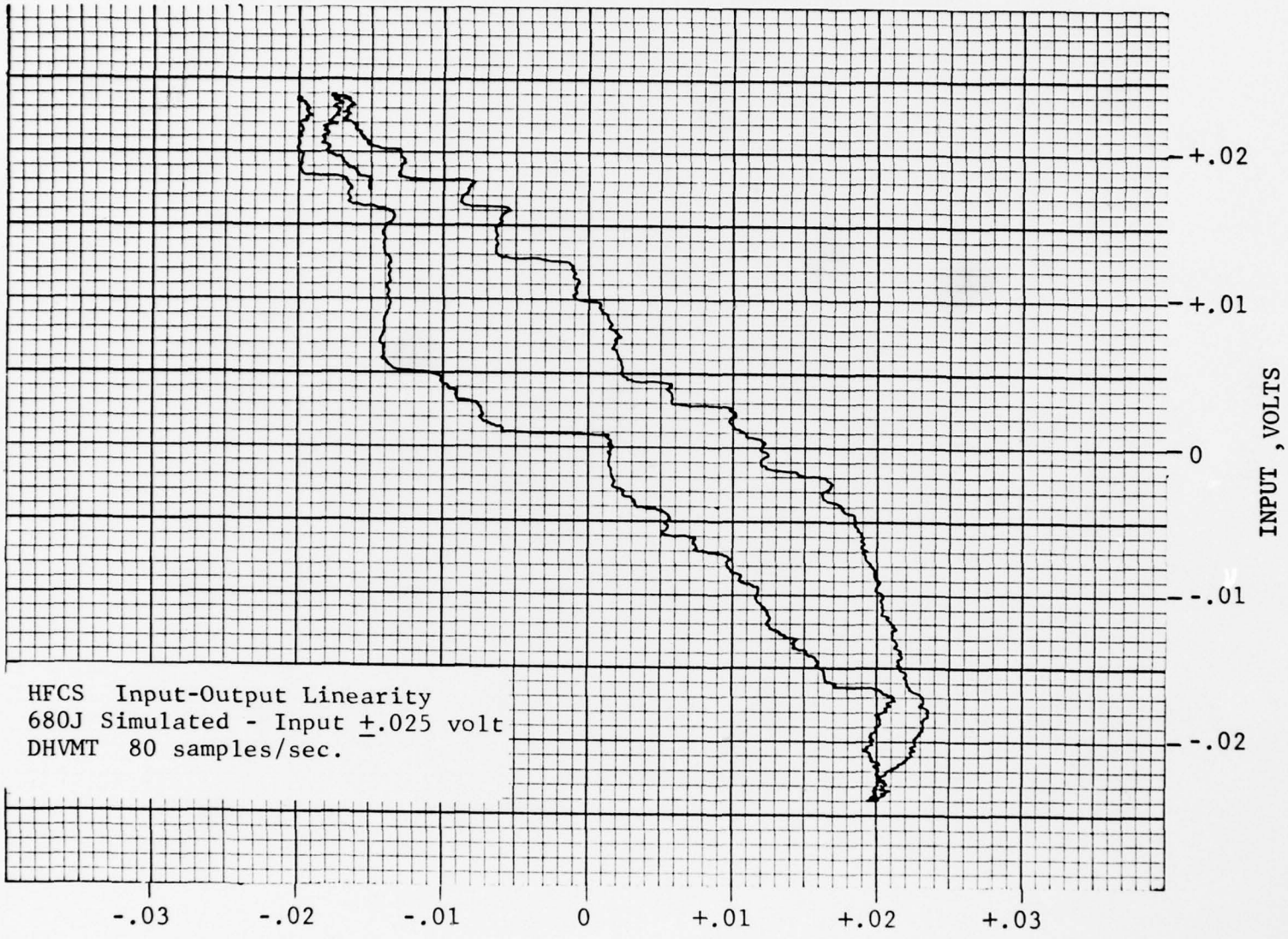

HFCS Input-Output Linearity
680J Simulated - Input ±.025 volt
DHVMT 80 samples/sec.
+.02
+.01
0
-.01
-.02
INPUT , VOLTS
-.03
-.02
-.01
0
+.01
+.02
+.03
OUTPUT , VOLTS

FIGURE 43

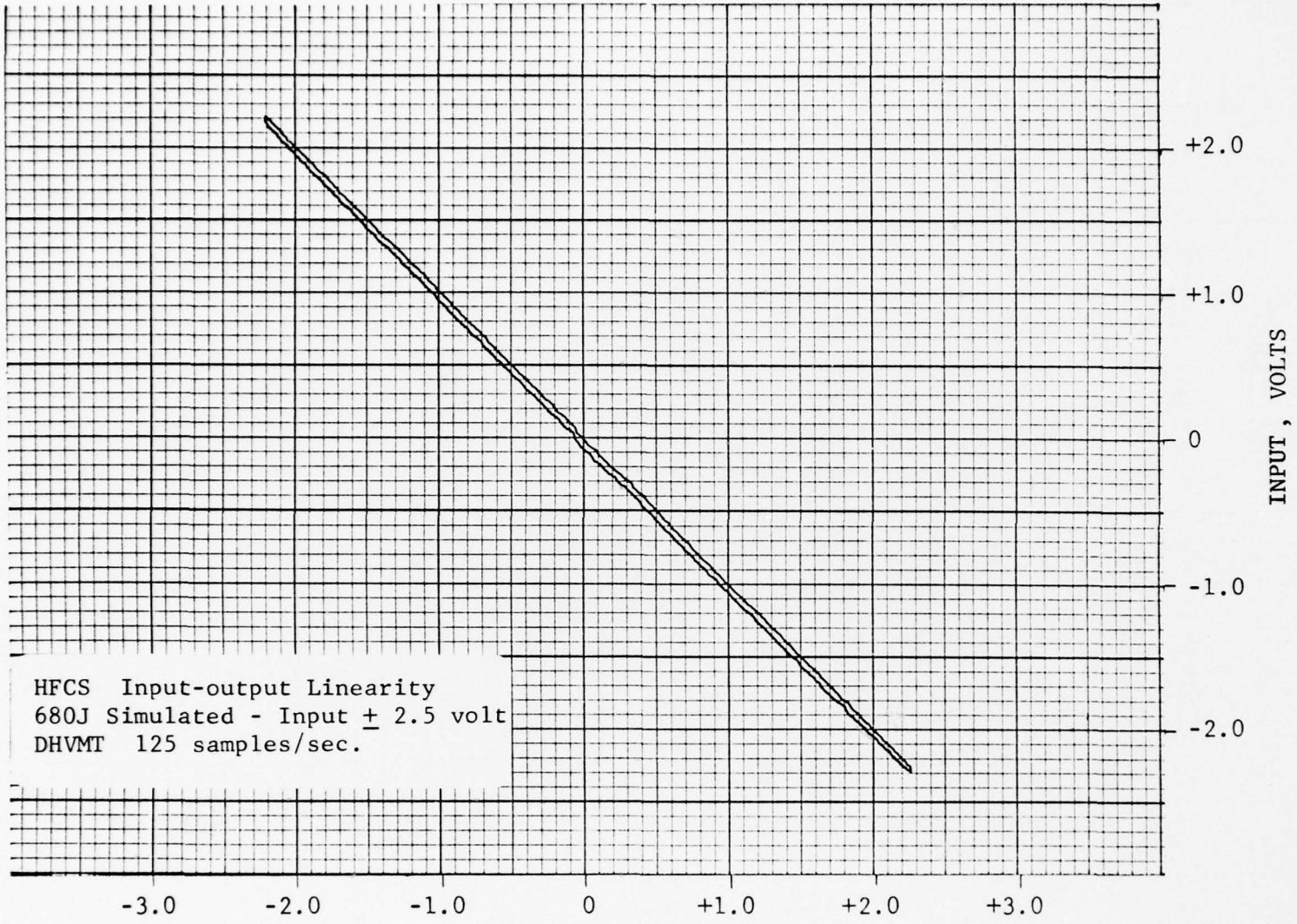

HFCS Input-output Linearity
680J Simulated - Input ± 2.5 volt
DHVMT 125 samples/sec.
+2.0
+1.0
0
-1.0
-2.0
INPUT , VOLTS
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
OUTPUT , VOLTS

FIGURE 44

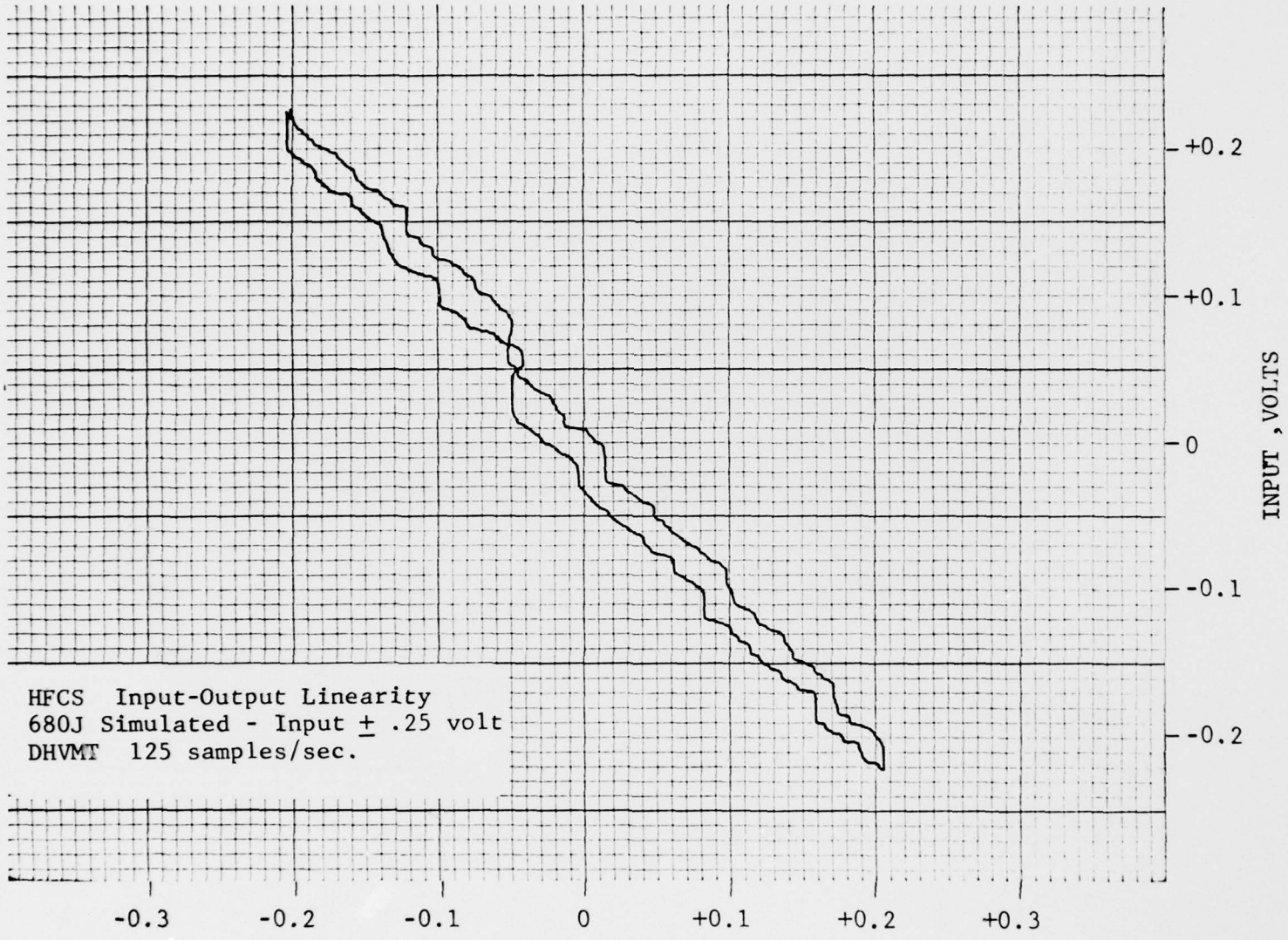

+0.2
+0.1
0
-0.1
-0.2
INPUT , VOLTS
HFCS Input-Output Linearity
680J Simulated - Input ± .25 volt
DHVMT 125 samples/sec.
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
OUTPUT, VOLTS

FIGURE 45

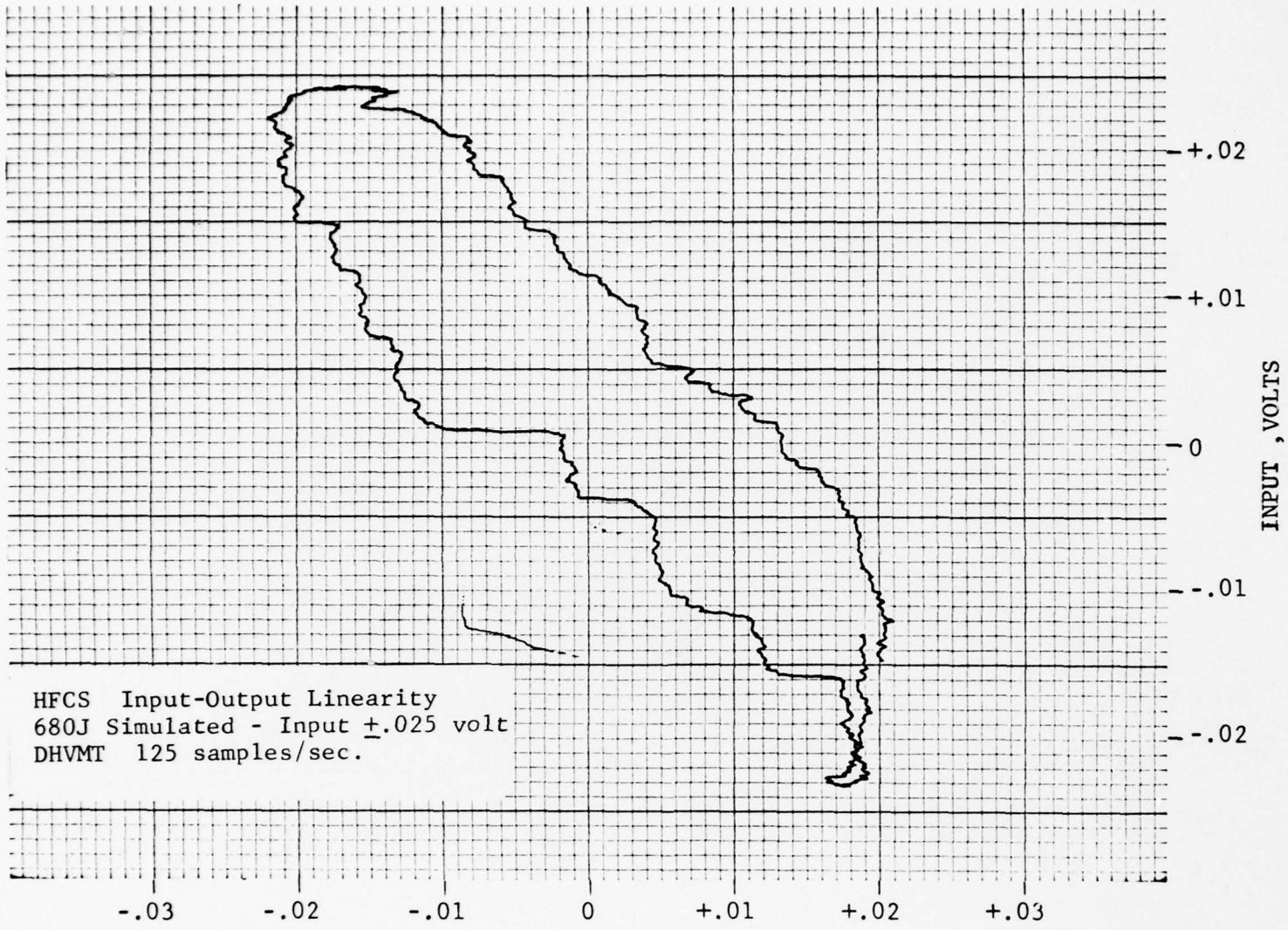

HFCS Input-Output Linearity
680J Simulated - Input ±.025 volt
DHVMT 125 samples/sec.
+.02
+.01
0
-.01
-.02
INPUT , VOLTS
-.03
-.02
-.01
0
+.01
+.02
+.03
OUTPUT , VOLTS

FIGURE 46

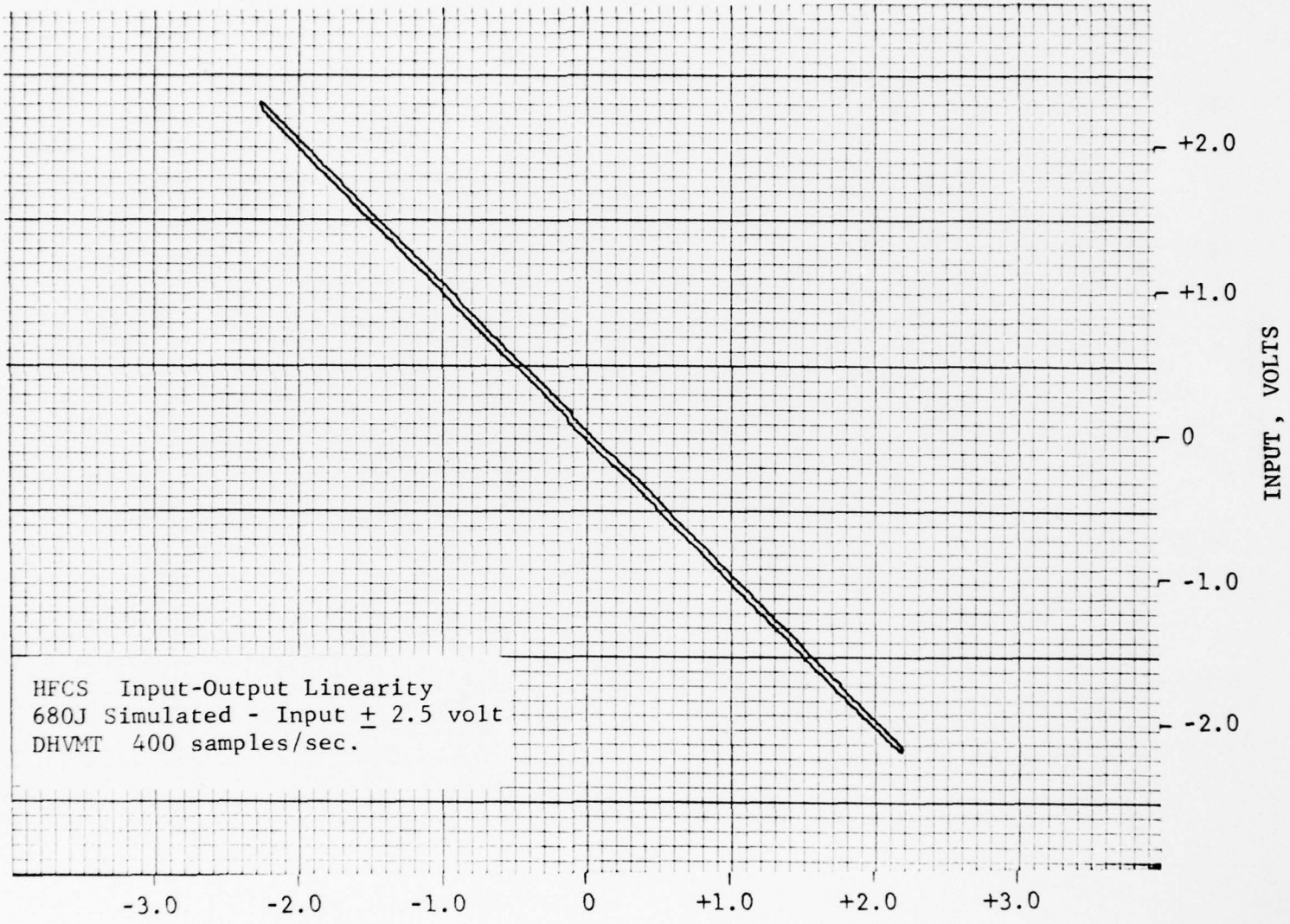

HFCS Input-Output Linearity
680J Simulated - Input ± 2.5 volt
DHVMT 400 samples/sec.
+2.0
+1.0
0
-1.0
-2.0
INPUT , VOLTS
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
OUTPUT , VOLTS

FIGURE 47

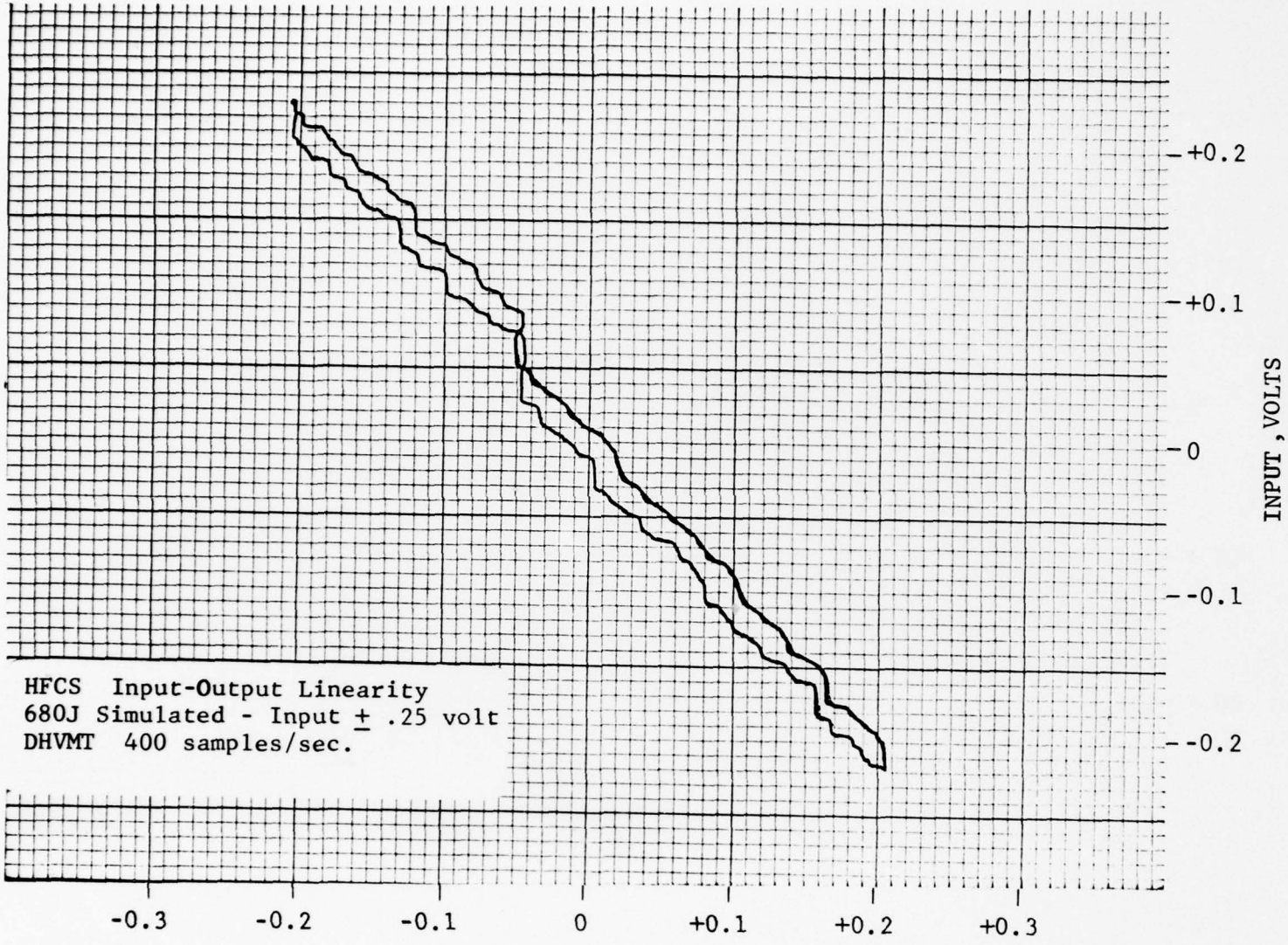

HFCS Input-Output Linearity
680J Simulated - Input ± .25 volt
DHVMT 400 samples/sec.
+0.2
+0.1
0
-0.1
-0.2
INPUT, VOLTS
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
OUTPUT, VOLTS

FIGURE 48

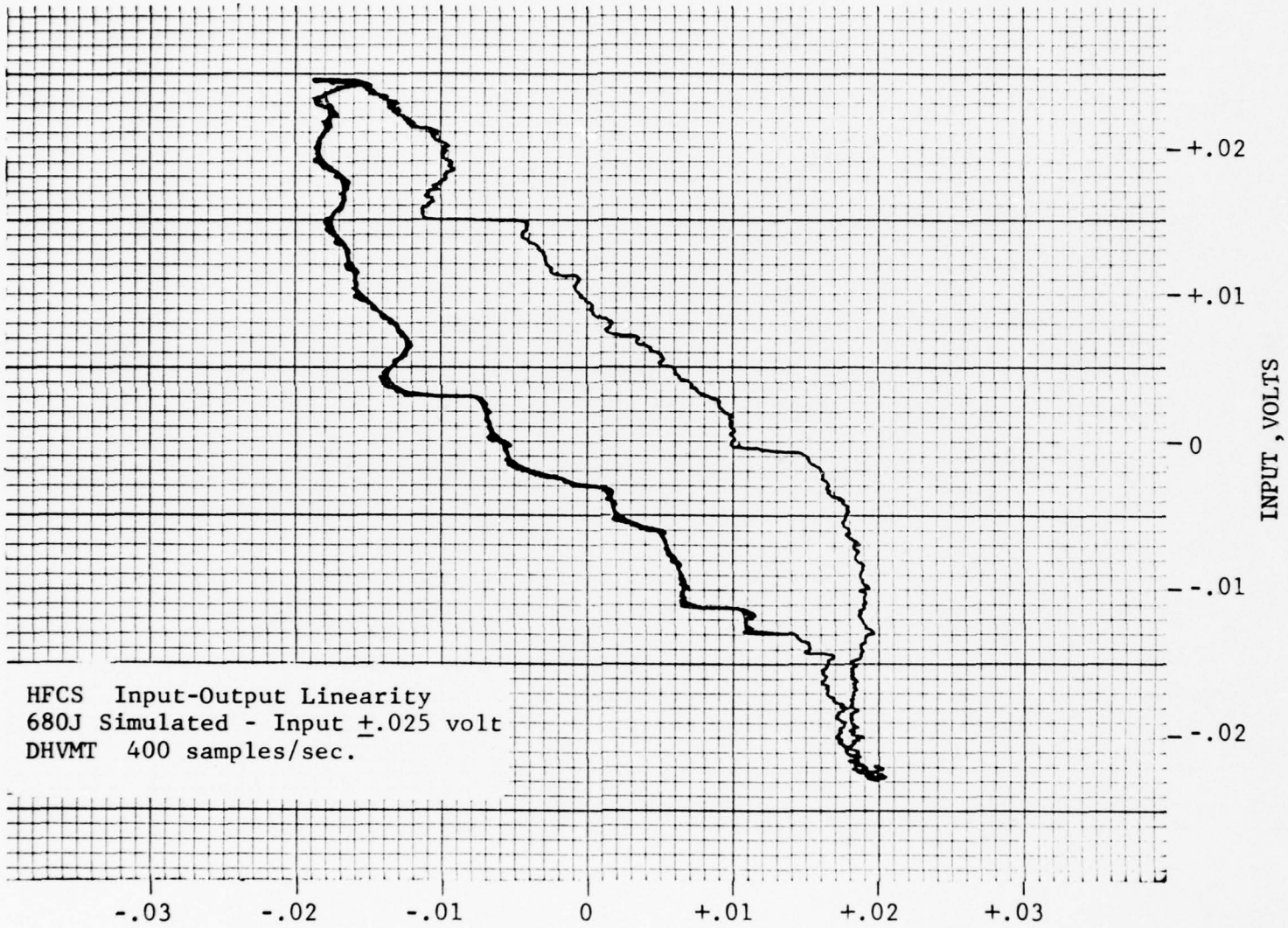

HFCS Input-Output Linearity
680J Simulated - Input ±.025 volt
DHVMT 400 samples/sec.
+.02
+.01
0
-.01
-.02
INPUT, VOLTS
-.03
-.02
-.01
0
+.01
+.02
+.03
OUTPUT, VOLTS

FIGURE 49

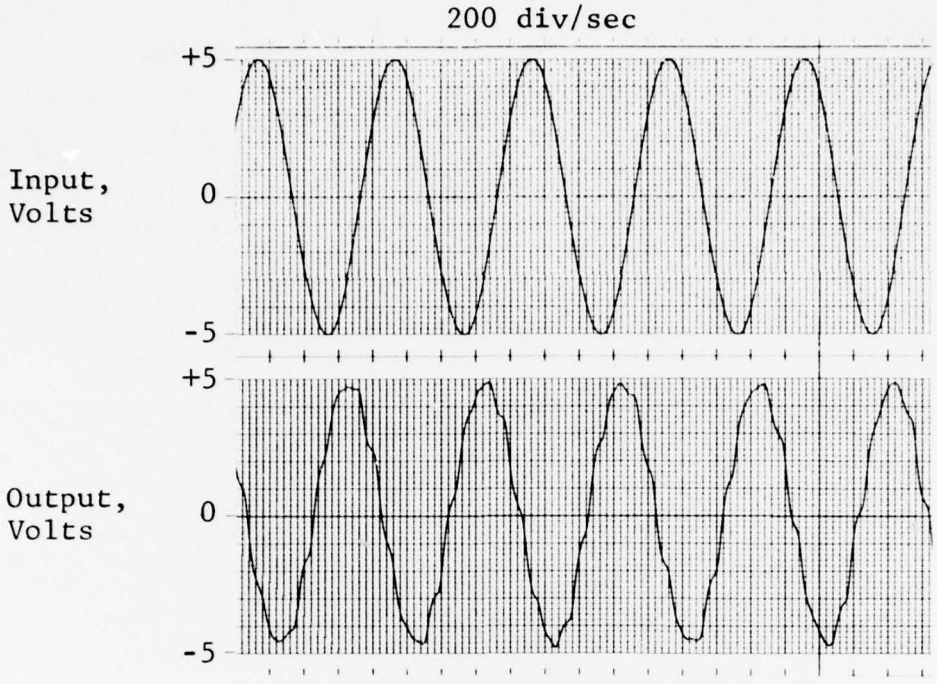


FIGURE 50 10 Hz Input-Output at 80 samples/sec.

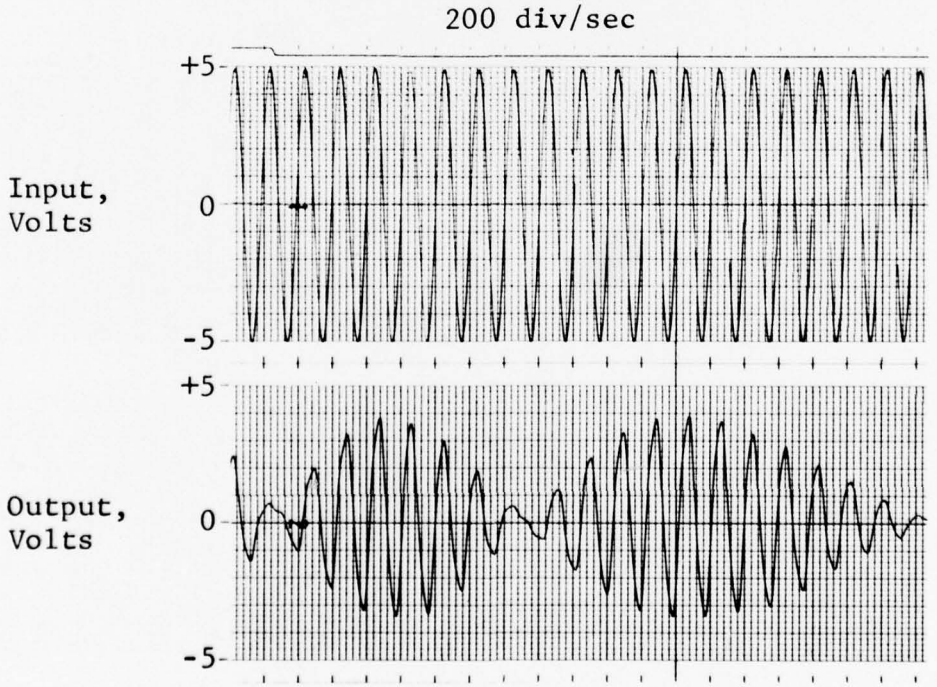


FIGURE 51 40 Hz Input-Output at 80 samples/sec.

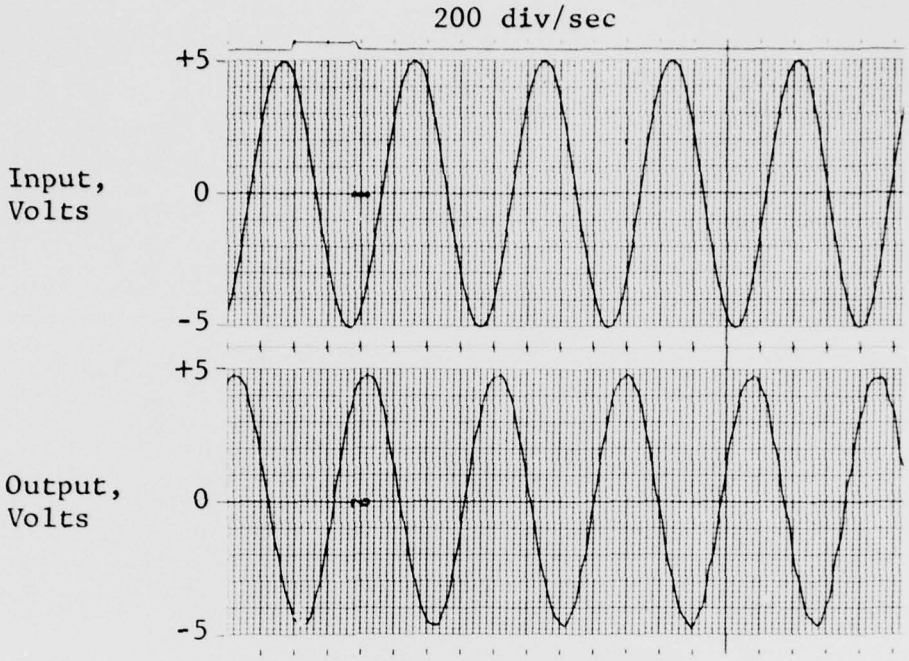


FIGURE 52 10 Hz Input-Output at 125 samples/sec.

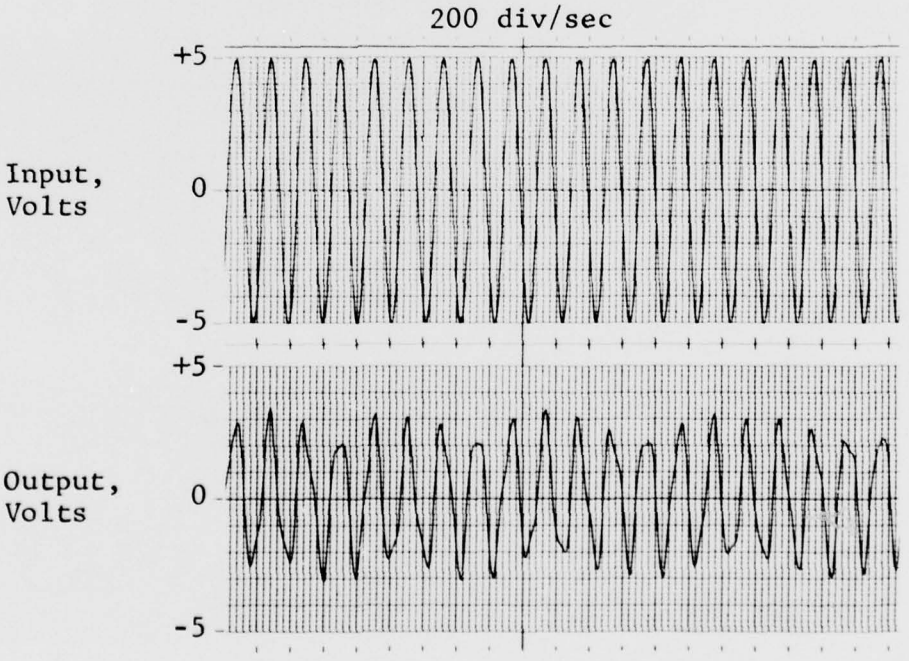


FIGURE 53 40 Hz Input-Output at 125 samples/sec.

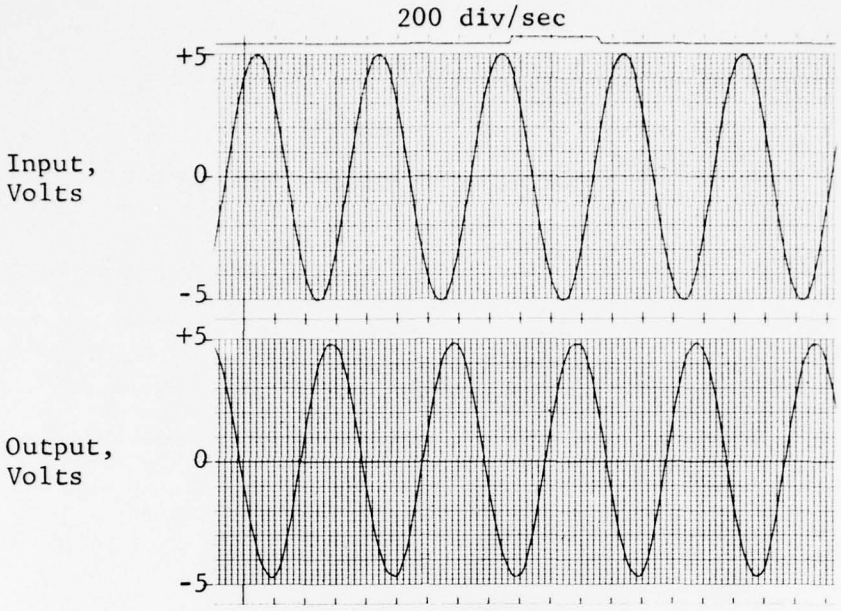


FIGURE 54 10 Hz Input-Output at 400 samples/sec.

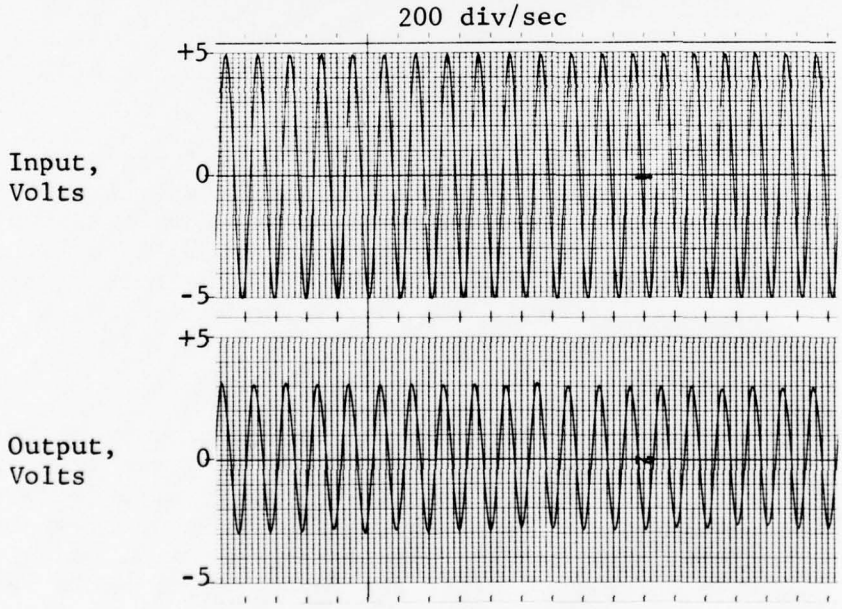


FIGURE 55 40 Hz Input-Output at 400 samples/sec.

TABLE 8

COMPARATIVE SIGNAL DISTORTION

Input Freq. Hz	Sample rate samples/sec.	P-P Input Amplitude in Volts ± 1.0	± 2.0	± 5.0
5	80	7.4%	4.0%	2.8%
10	80	8.5%	6.1%	5.6%
20	80	15.8%	15.0%	13.5%
40	80	64.0%	42.0%	50.0%
5	125	7.0%	3.6%	1.8%
10	125	7.4%	4.2%	2.9%
20	125	9.6%	6.8%	6.0%
40	125	27.5%	25.0%	23.3%
5	400	7.0%	3.5%	1.5%
10	400	7.2%	3.6%	1.8%
20	400	8.4%	4.2%	2.1%
40	400	12.5%	6.5%	3.8%

A considerable amount of signal distortion can be seen in FIGURE 50 where the sample rate frequency is eight times the input frequency. When the sample rate to input frequency ratio is less than 4 to 1, some amplitude modulation is apparent. As the ratio approaches 2, the modulation is severe (as shown in FIGURES 51 and 53 where the ratios are 3 and 2 respectively).

The modulation is the result of when the sampler "samples" the input signal. In the case of a sample rate frequency to signal frequency ratio of approximately 2, the samples are taken twice per input signal cycle. The sample voltage can vary from near full amplitude to zero volts as the phase relationship between the

two frequencies changes from 0 to 90°. The frequency of modulation of the input carrier depends on the frequency difference between the input and a harmonic of sample frequency.

The traces in FIGURES 54 and 55 are the 400 samples/sec. which show good output signals at this sample frequency.

4.2.3 680J Asynchronous Clock Operation

4.2.3.1 Test Description

The DHVMT was operated in the pseudo-asynchronous mode. This is the mode where the clock offset for the sampled data is controlled. Control of the clock offset enables the evaluation of the affect that asynchronous operation will have on the system.

The test set-up for asynchronous clock evaluation was as shown previously in FIGURE 37. The sample rates of the DHVMT used for testing were 80, 125 and 400 samples/sec. According to the intended test plan, the offsets were to be at 0%, 25%, 50% and 75% of sample period for Channels A, B, C and D respectively. However, because the time delay provided in the DHVMT is limited to a range of 1.00 ms to 4.70 ms, the desired percent of sample period offsets were not attainable for all cases. TABLE 9 is a listing of the desired offsets and TABLE 10 indicates the actual setting used for this test sequence.

INPUT, VOLTS

TABLE 9

DESIRED TIME DELAYS

Sample Rate	Channel clock time delay, ms			
	A	B	C	D
80	0	3.13	6.25	9.38
125	0	2.00	4.00	6.00
400	0	0.63	1.25	1.88

TABLE 10

ACTUAL TIME DELAYS

Sample Rate	Channel clock time delay, ms			
	A	B	C	D
80	0	3.1	4.75	3.10
125	0	2.0	4.00	4.75
400	0	1.9	1.25	1.90

Note that all of the time delays desired were not achieved for a given sample rate. In performing the

tests, the time delays were set as close to the desired value as possible (within the circuit adjustment range). Where the settings were limited by the delay range for the channels, one channel was adjusted to the maximum delay setting and the remaining channel adjusted to match one of the other correctly set channels.

With the nearest time delays set on the DHVMT and the DHVM updating at 1465/sec. the data for asynchronous operation was recorded.

4.2.3.2 Test Results

The frequency response plots for 80, 125 and 400 samples/sec. are shown in FIGURES 56, 57 and 58. The phase and amplitude curves are quite comparable to the response curves in FIGURES 38, 39 and 40 where only the sample rate was varied. A difference that is noticable is the amplitude burst at 40 Hz in FIGURE 56 is not as severe as in FIGURE 38. This is because the low median select logic in conjunction with the sample time delay minimizes the modulation effect of the signal frequency approaching the sample frequency.

FIGURES 59 through 67 are the input-output X-Y plots with inputs of $\pm$ 2.5 volts, $\pm$ .25 volts and $\pm$ .025 volts at sample rates of 80/sec., 125/sec. and 400/sec. No significant changes were noticed in comparing these results to the synchronous sample rate variation test results of Section 4.2.2.2.

Distortion data is listed in TABLE 11 for the three sample rates at output amplitudes of $\pm$ 1.0, $\pm$ 2.0 and $\pm$ 5.0 volts P-P. Referring to TABLE 7 in Section 4.2.2.2, there is comparatively less distortion indicated for the 40 Hz input at both the 80/sec. and 125/sec. sample rates for asynchronous operation.

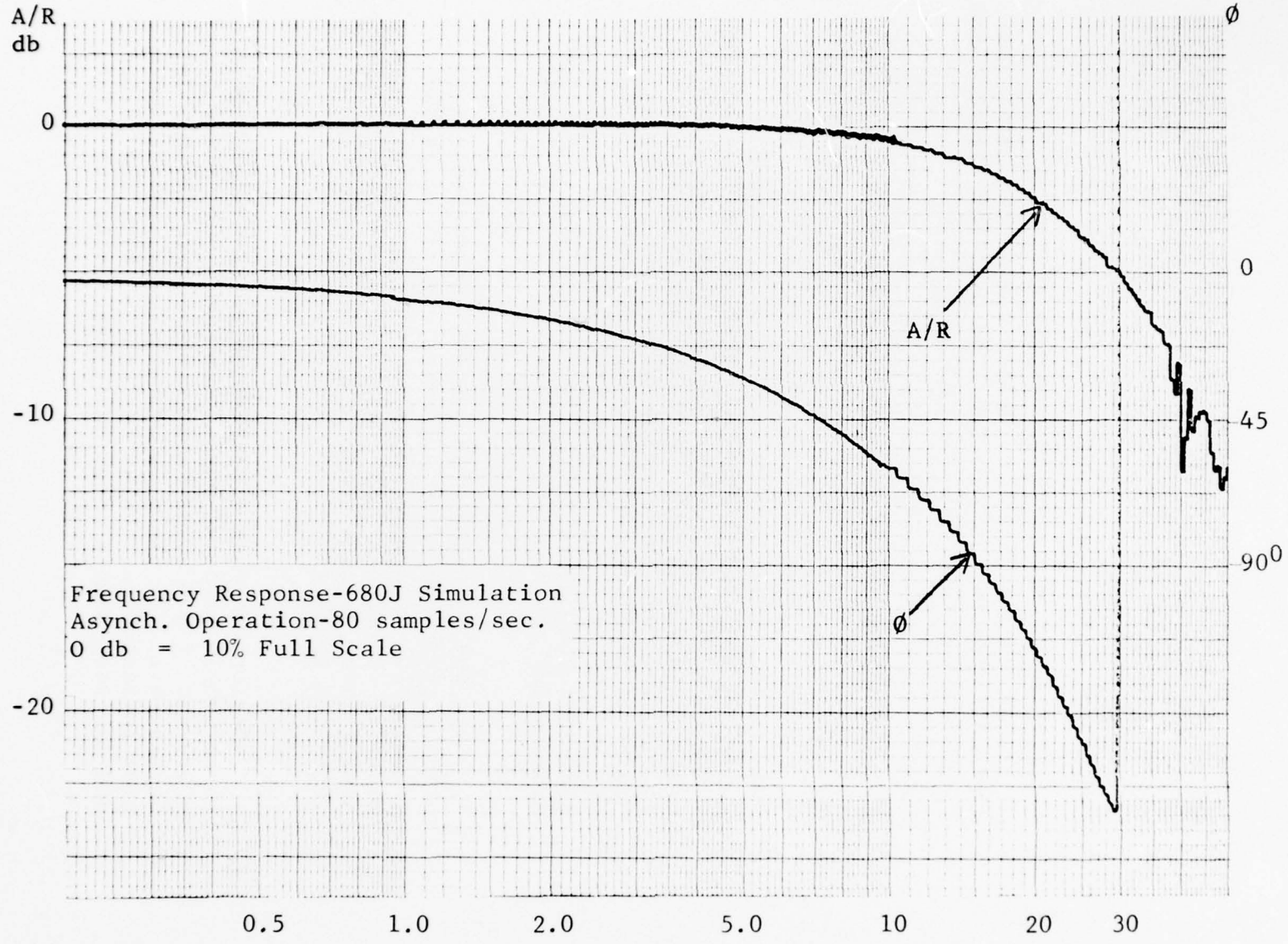

A/R
db
0
-10
-20
Ø
0
45
90⁰
A/R
Ø
Frequency Response-680J Simulation
Asynch. Operation-80 samples/sec.
0 db = 10% Full Scale
0.5
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 56

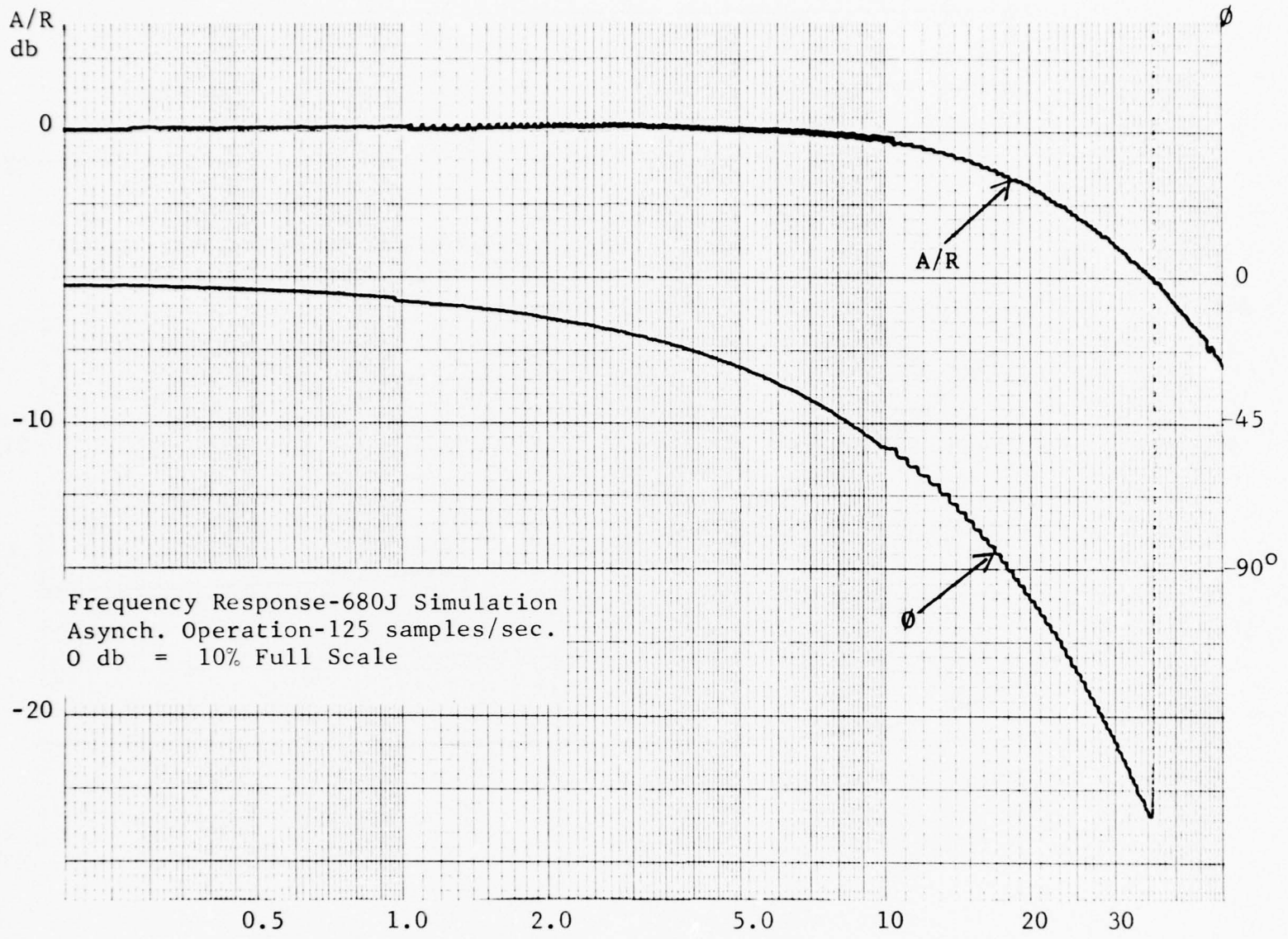

A/R
db
0
-10
-20
Ø
0
45
90°
A/R
Ø
Frequency Response-680J Simulation
Asynch. Operation-125 samples/sec.
0 db = 10% Full Scale
0.5
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 57

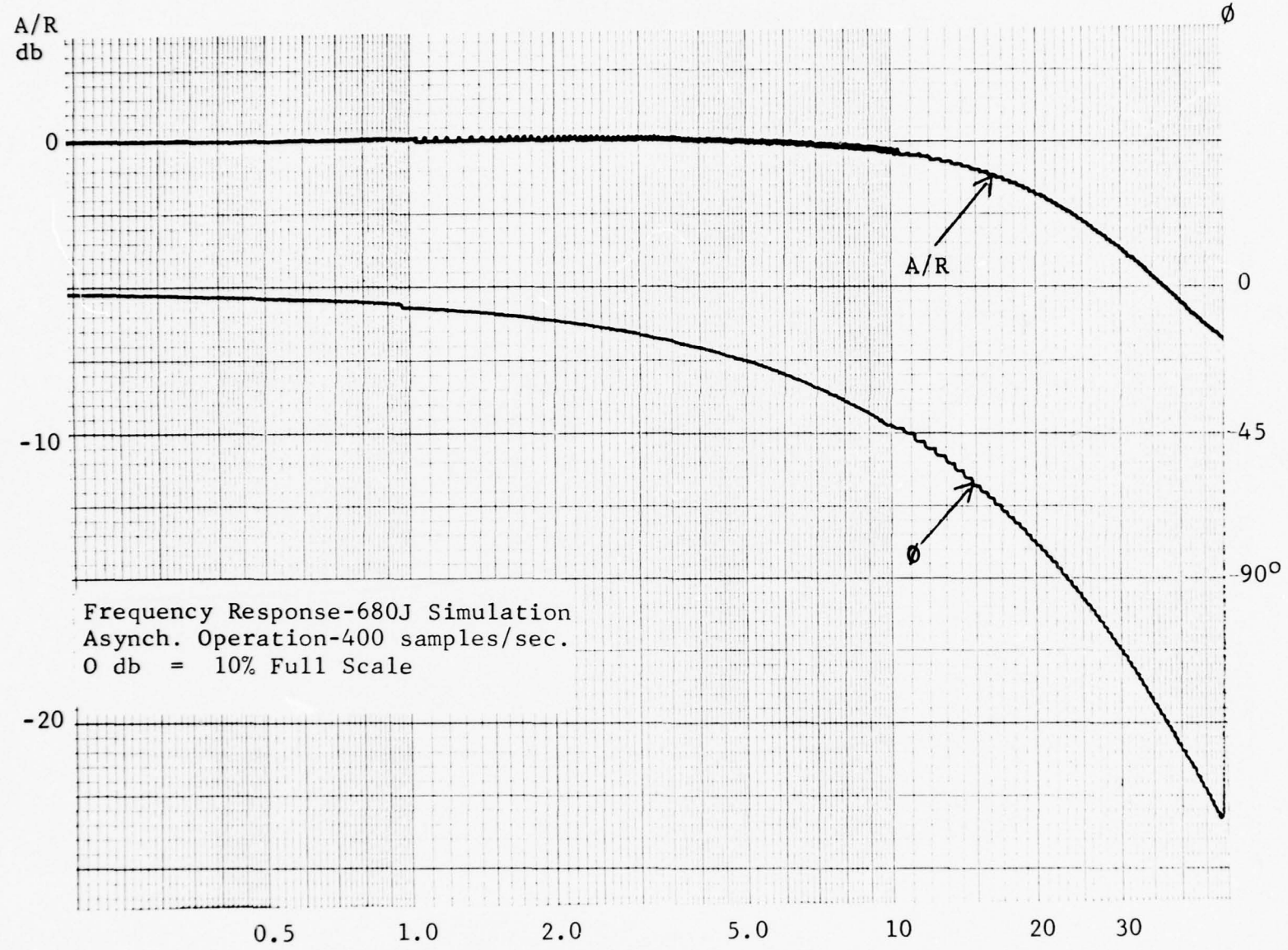

A/R
db
Ø
0
-10
-20
A/R
Ø
0
-45
-90°
Frequency Response-680J Simulation
Asynch. Operation-400 samples/sec.
0 db = 10% Full Scale
0.5
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 58

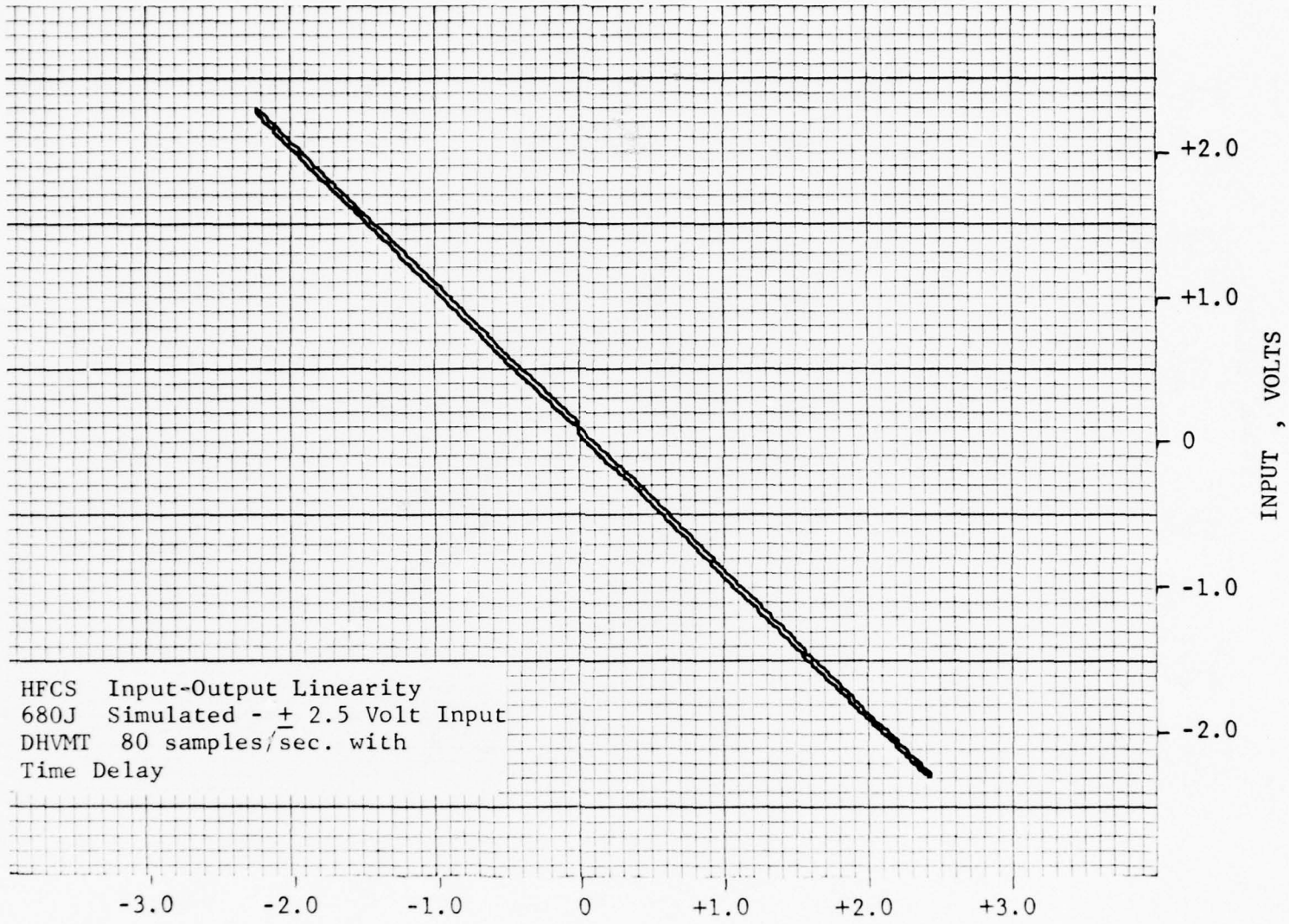

HFCS Input-Output Linearity
680J Simulated - ± 2.5 Volt Input
DHVMT 80 samples/sec. with
Time Delay
+2.0
+1.0
0
-1.0
-2.0
INPUT , VOLTS
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
OUTPUT, VOLTS

FIGURE 59

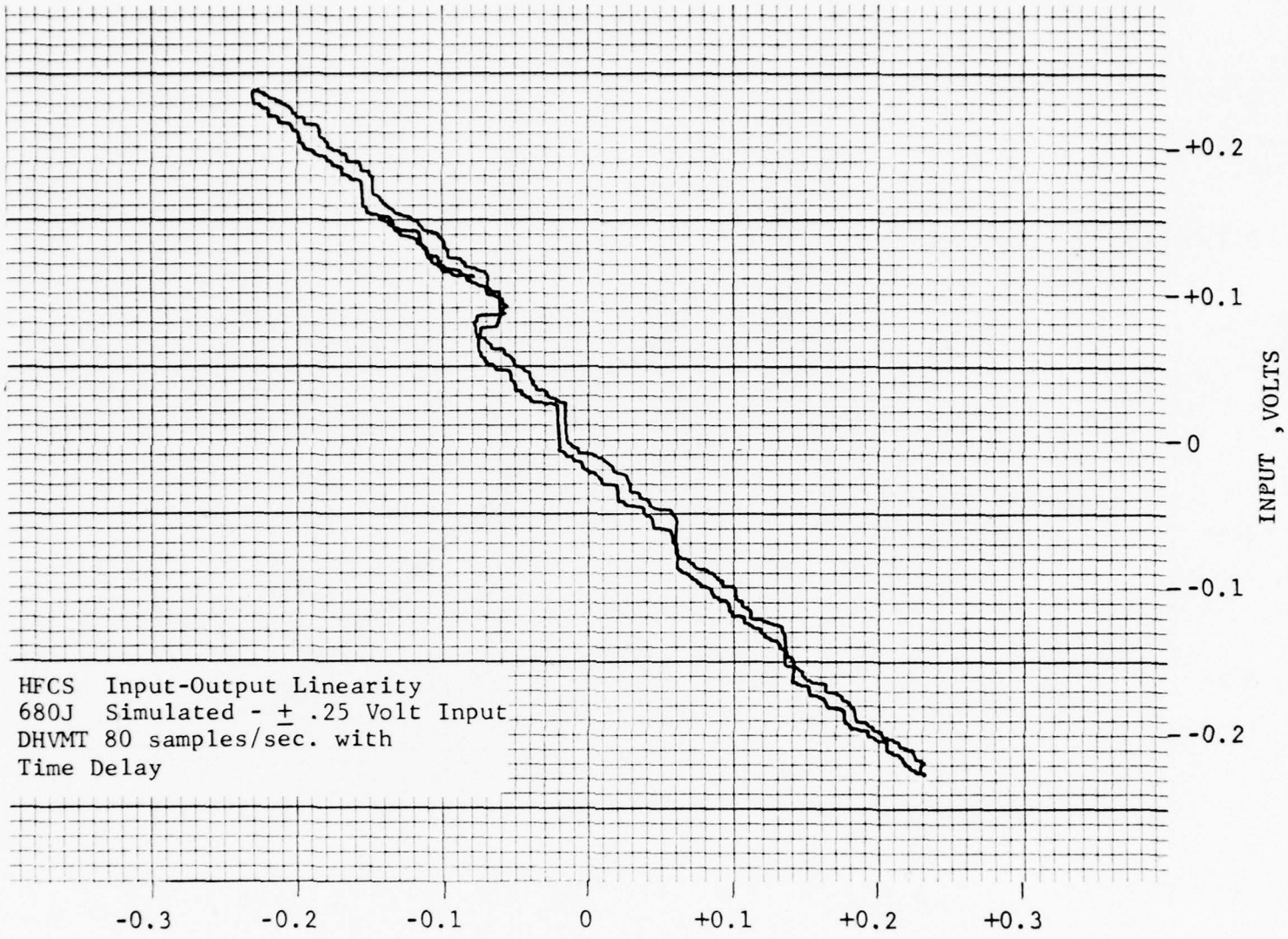

HFCS Input-Output Linearity
680J Simulated - ± .25 Volt Input
DHVMT 80 samples/sec. with
Time Delay
+0.2
+0.1
0
-0.1
-0.2
INPUT , VOLTS
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
OUTPUT , VOLTS

FIGURE 60

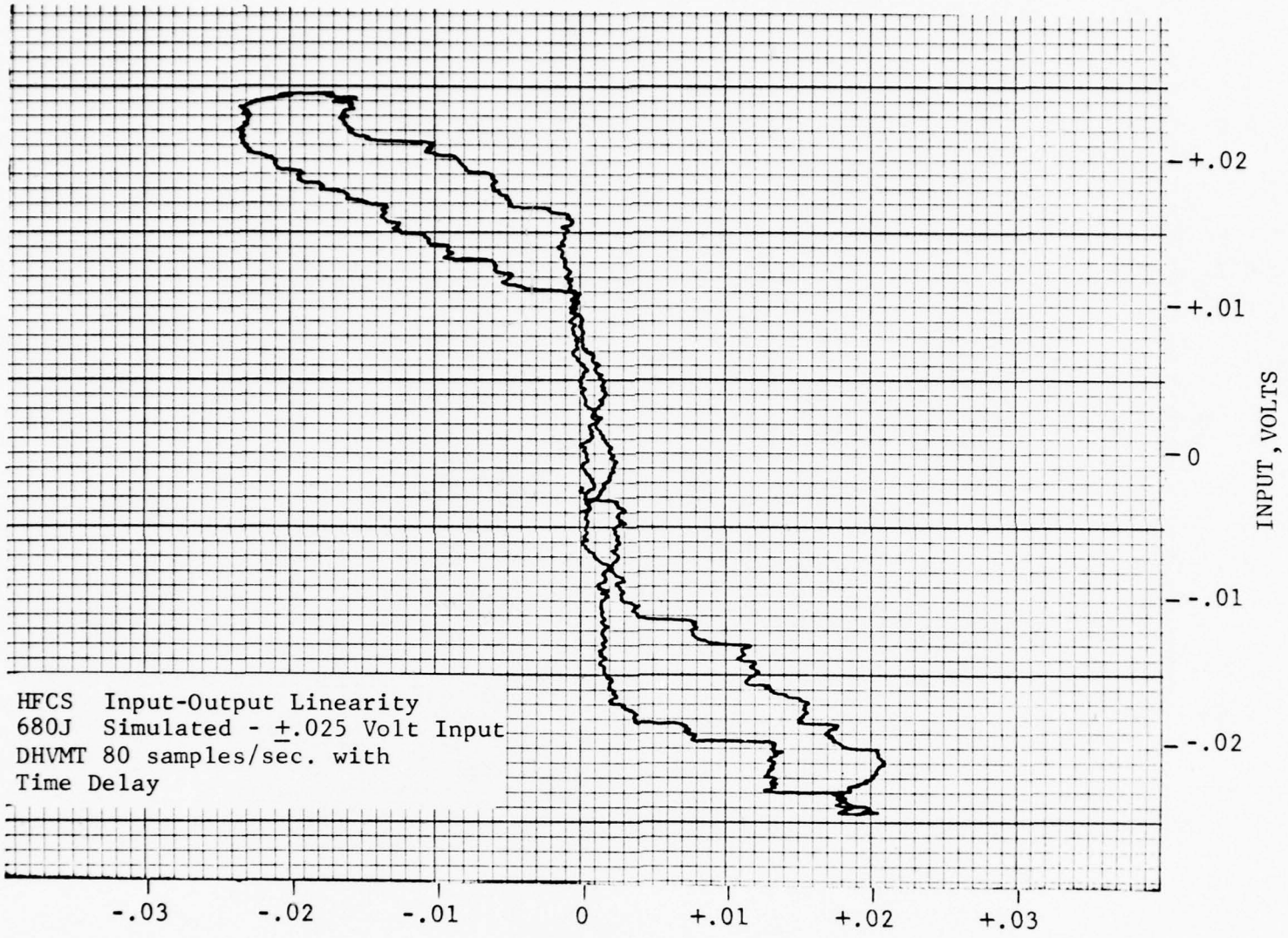

HFCS Input-Output Linearity
680J Simulated - ±.025 Volt Input
DHVMT 80 samples/sec. with
Time Delay
+.02
+.01
0
-.01
-.02
INPUT, VOLTS
-.03
-.02
-.01
0
+.01
+.02
+.03
OUTPUT, VOLTS

FIGURE 61

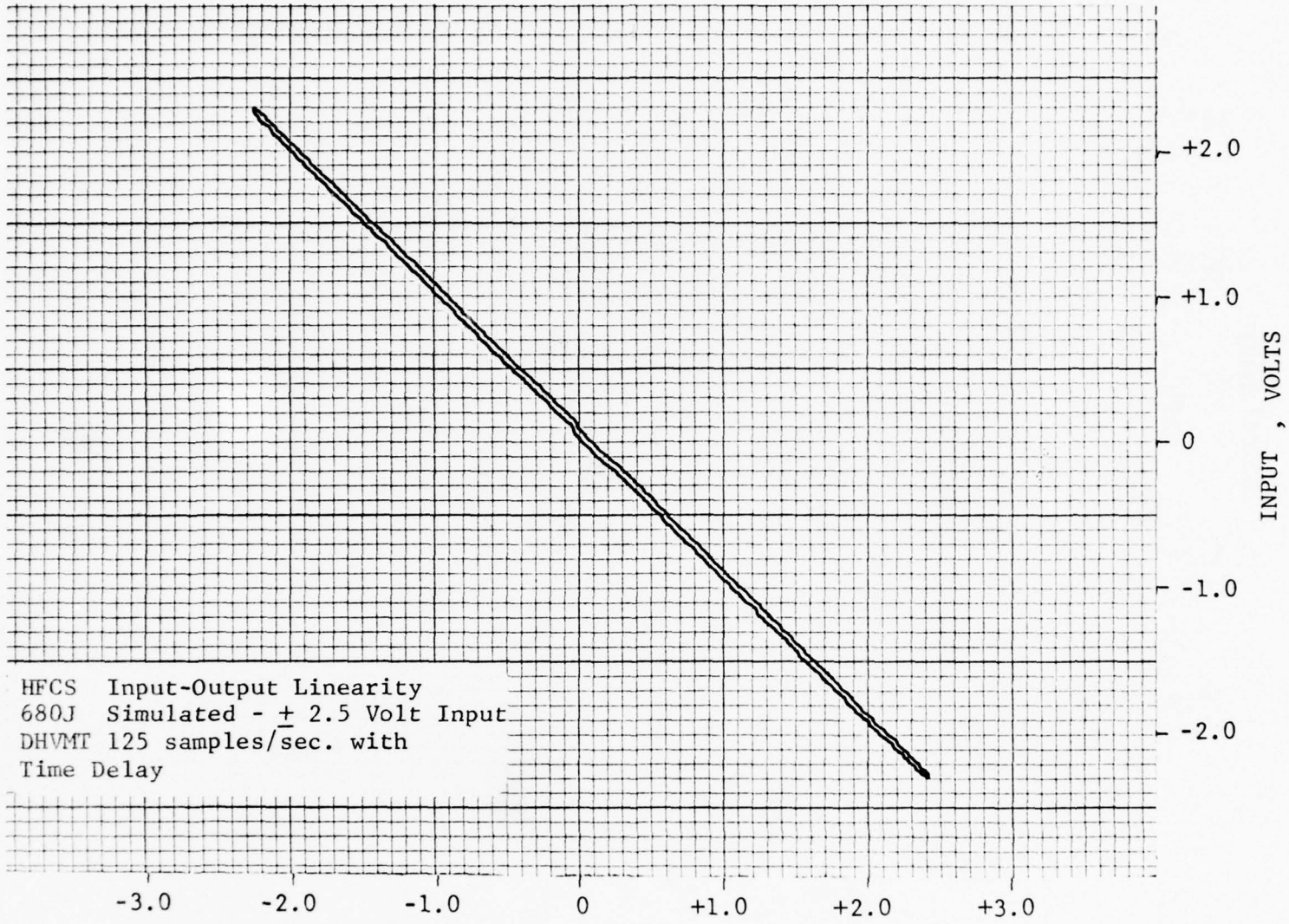

HFCS Input-Output Linearity
680J Simulated - ± 2.5 Volt Input
DHVMT 125 samples/sec. with
Time Delay
+2.0
+1.0
0
-1.0
-2.0
INPUT , VOLTS
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
OUTPUT, VOLTS

FIGURE 62

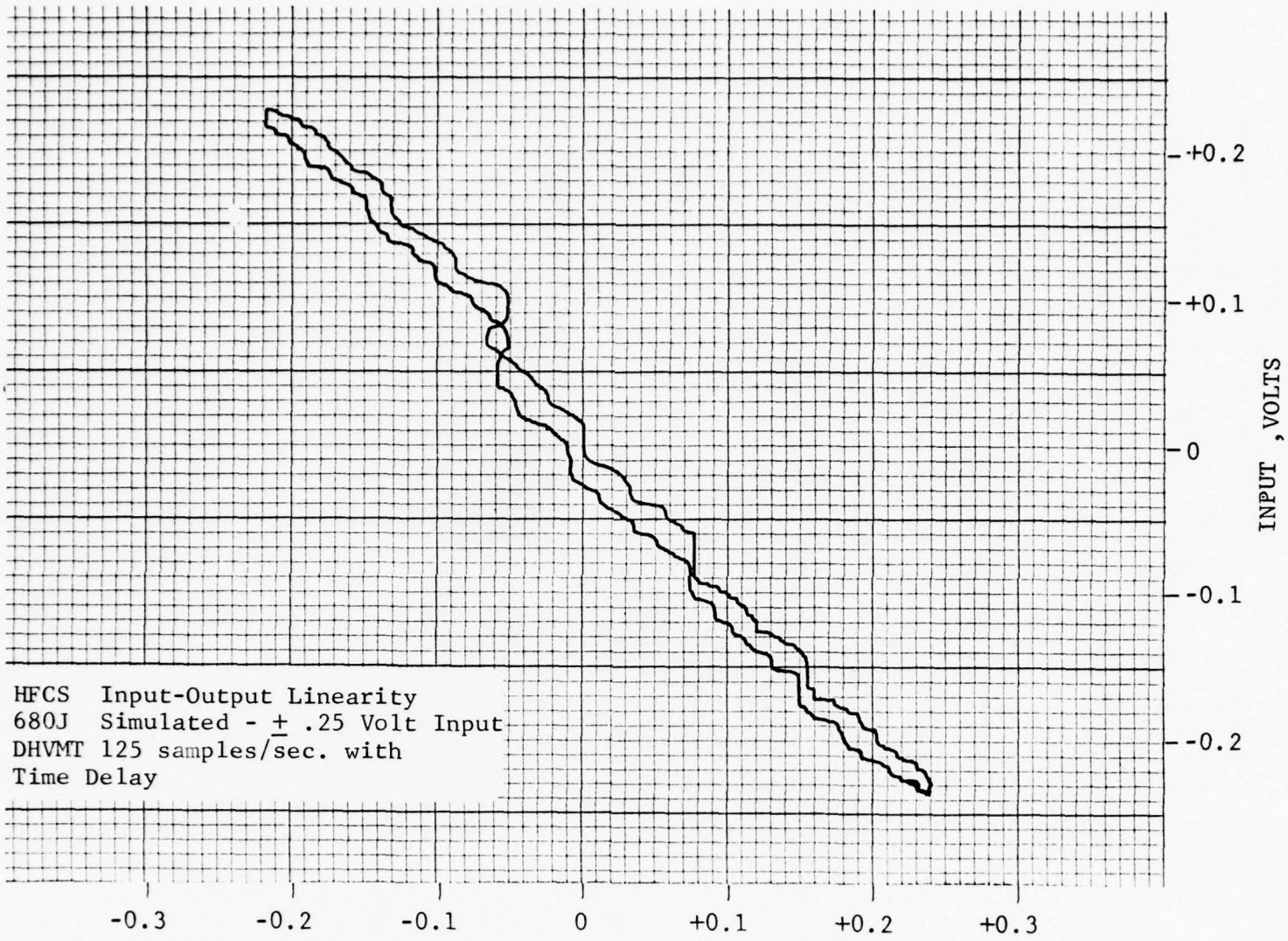

HFCS Input-Output Linearity
680J Simulated - ± .25 Volt Input
DHVMT 125 samples/sec. with
Time Delay
+0.2
+0.1
0
-0.1
-0.2
INPUT, VOLTS
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
OUTPUT, VOLTS

FIGURE 63

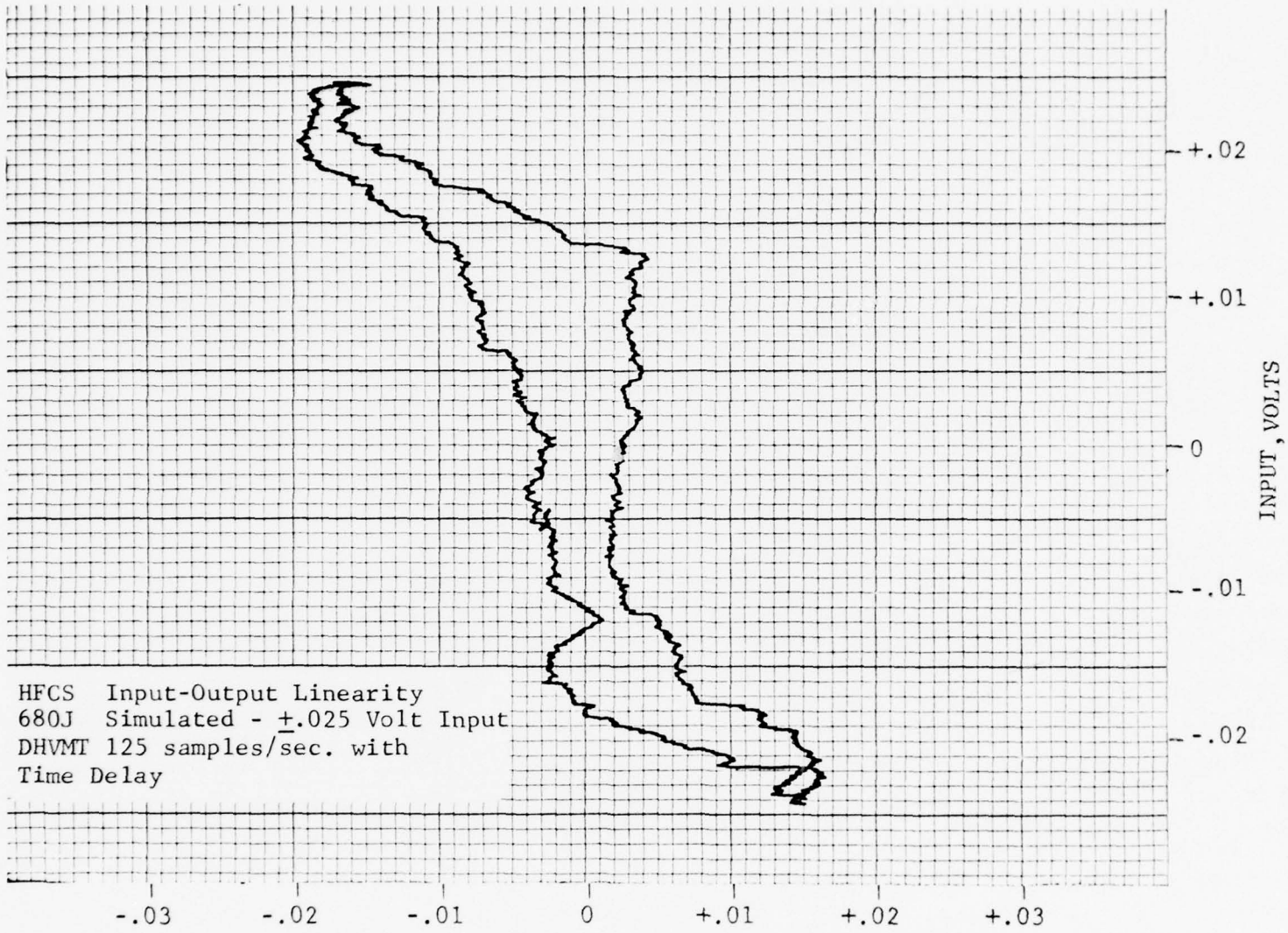

HFCS Input-Output Linearity
680J Simulated - ±.025 Volt Input
DHVMT 125 samples/sec. with
Time Delay
+.02
+.01
0
-.01
-.02
INPUT, VOLTS
-.03
-.02
-.01
0
+.01
+.02
+.03
OUTPUT, VOLTS

FIGURE 64

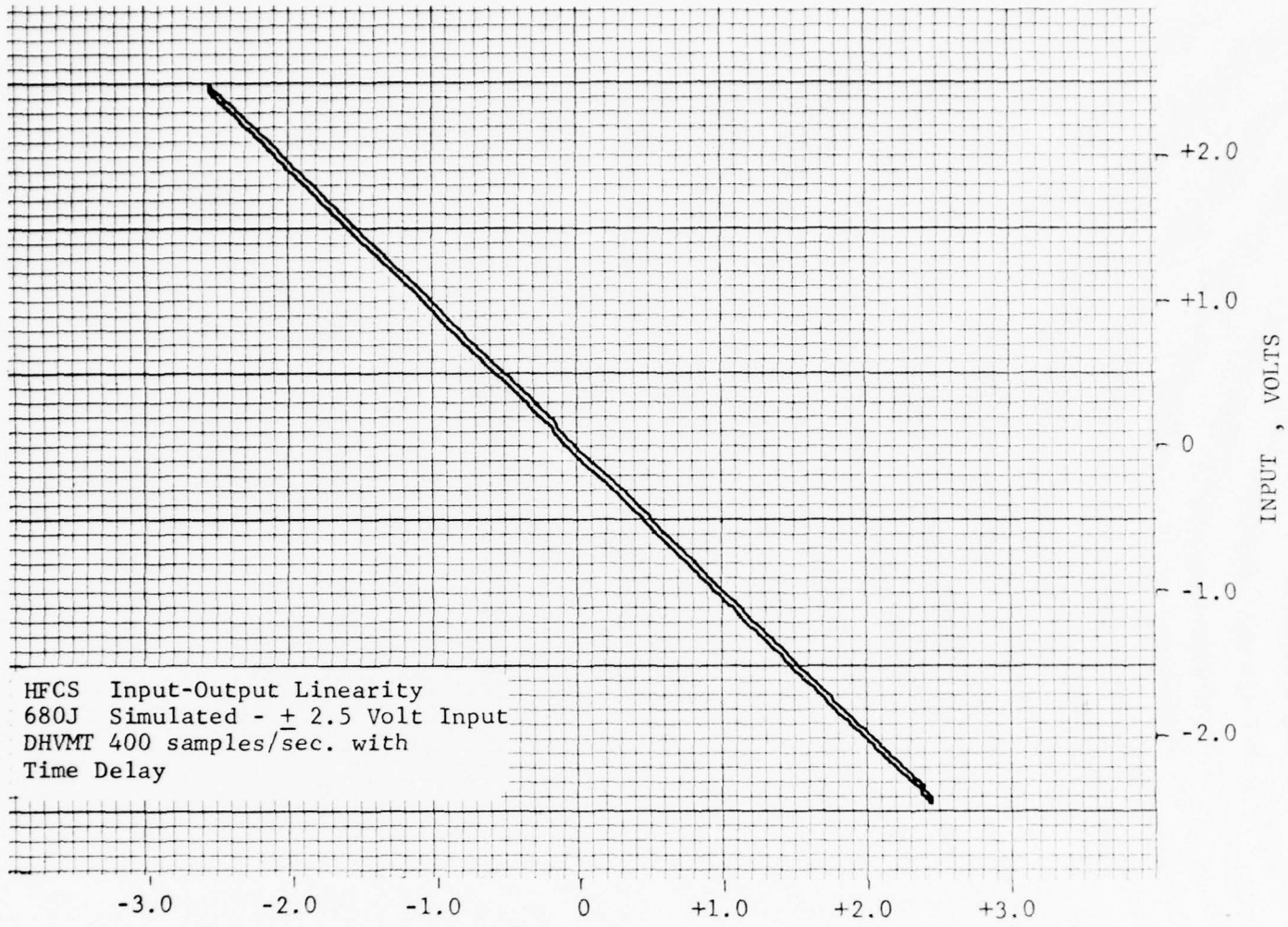

HFCS Input-Output Linearity
680J Simulated - ± 2.5 Volt Input
DHVMT 400 samples/sec. with
Time Delay
+2.0
+1.0
0
-1.0
-2.0
INPUT , VOLTS
-3.0
-2.0
-1.0
0
+1.0
+2.0
+3.0
OUTPUT, VOLTS

FIGURE 65

INPUT, VOLTS
+0.2
+0.1
0
-0.1
-0.2
-0.3
-0.2
-0.1
0
+0.1
+0.2
+0.3
OUTPUT, VOLTS
HFCS Input-Output Linearity
680J Simulated - ± .25 Volt Input
DHVMT 400 samples/sec. with
Time Delay

FIGURE 66

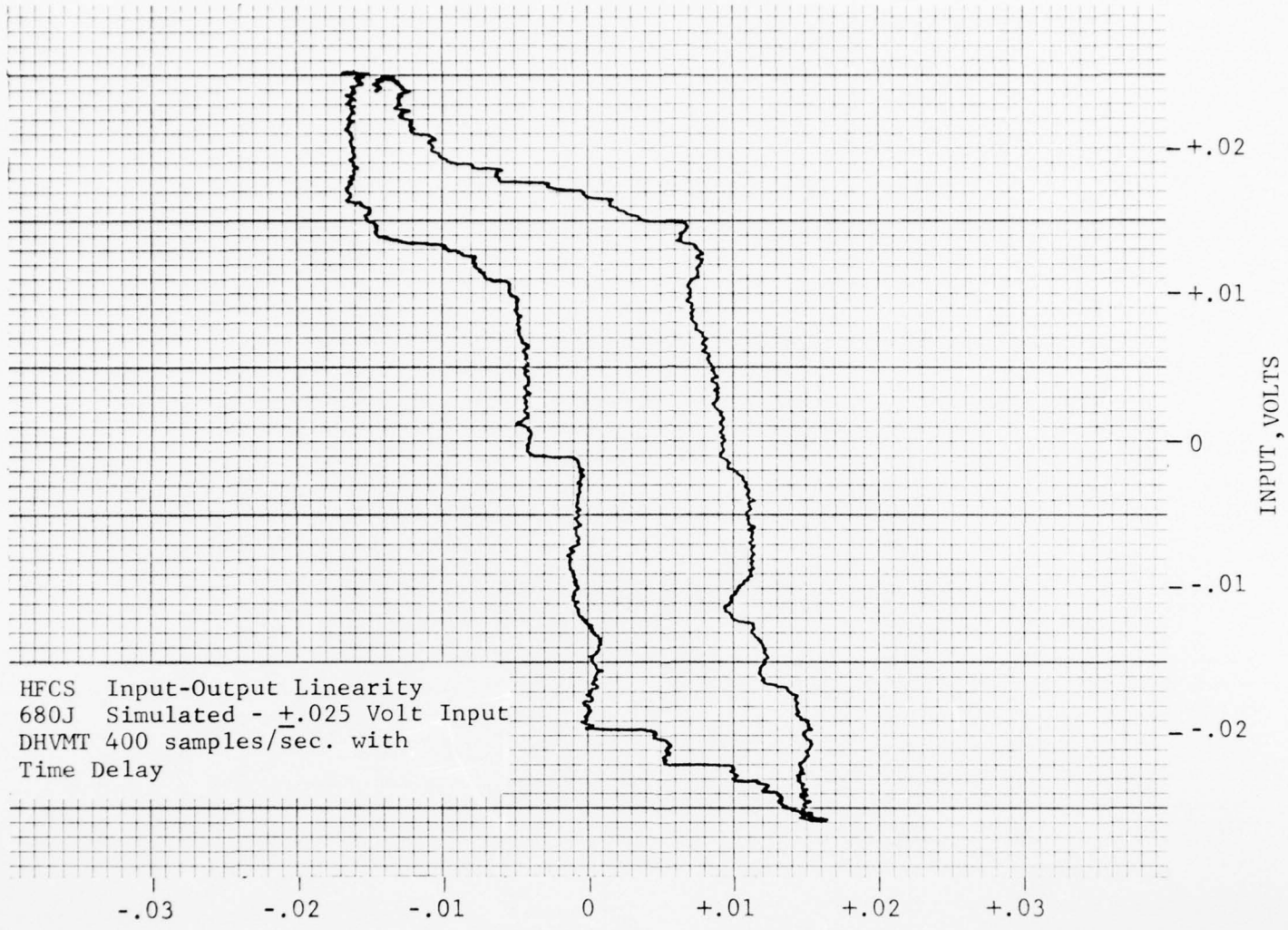

HFCS Input-Output Linearity
680J Simulated - ±.025 Volt Input
DHVMT 400 samples/sec. with
Time Delay
+.02
+.01
0
-.01
-.02
INPUT, VOLTS
-.03
-.02
-.01
0
+.01
+.02
+.03
OUTPUT, VOLTS

FIGURE 67

TABLE 11

SIGNAL DISTORTION WITH TIME DELAY

Input Freq. Hz	Sample rate samples/sec.	P-P Input Amplitude in Volts ± 1.0	± 2.0	± 5.0
5	80	7.5%	4.2%	2.9%
10	80	9.2%	6.7%	5.8%
20	80	17.0%	16.3%	14.0%
40	80	42.0%	39.0%	29.0%
5	125	7.3%	3.5%	2.0%
10	125	7.7%	4.0%	2.9%
20	125	9.1%	5.3%	4.1%
40	125	16.0%	11.8%	9.7%
5	400	7.1%	3.4%	1.5%
10	400	7.4%	3.6%	1.7%
20	400	8.4%	4.0%	1.9%
40	400	12.5%	6.0%	3.4%

The most significant change is at the 125 samples/sec. rate. The distortion values have been reduced by a factor of one-half with asynchronous operation. The distortion for the 80 samples/sec. rate would have indicated a similar reduction if the DHVMT had been designed to provide the desired time delays. FIGURE 68 graphically demonstrates the reason for the decrease in signal distortion. The figure illustrates a triangular input signal being sampled by two channels, with Channel B sampling one-half period later than Channel A. An important point to realize is that the input signal is in "real time". Therefore, when the time delayed sample is taken from a dynamic input, the second sample will have a different amplitude value. When two sampled

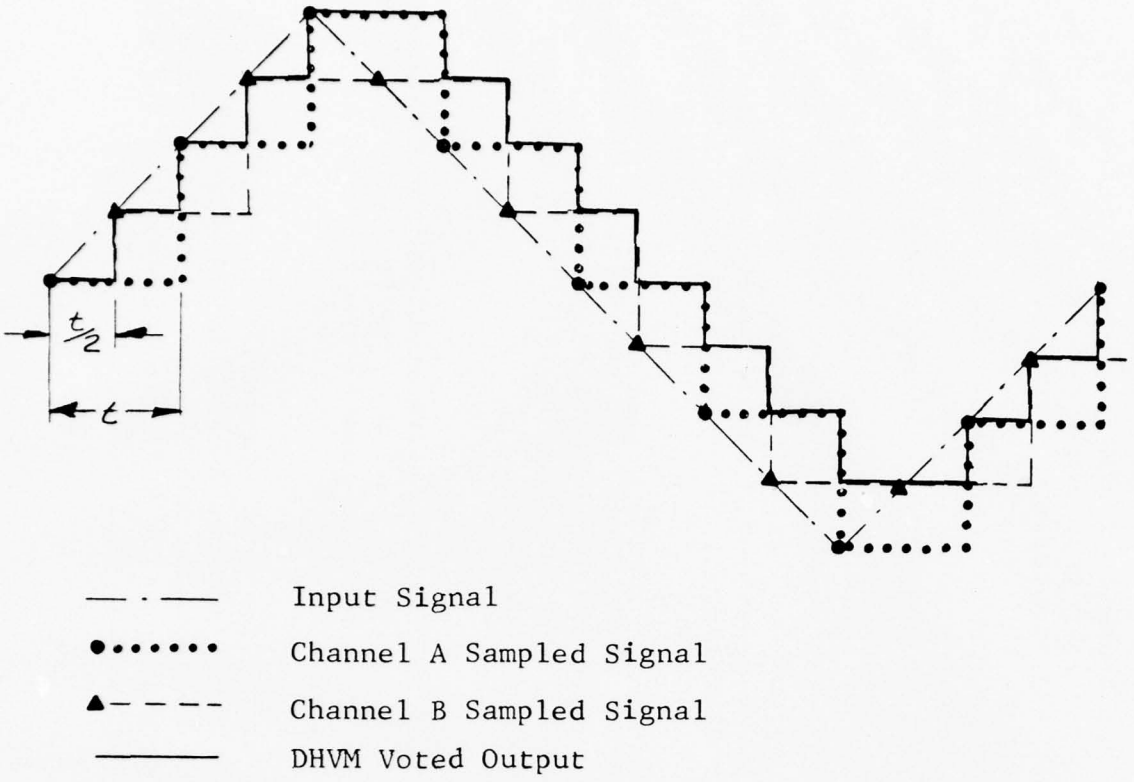


FIGURE 68 Asynchronous Sampling, with Channel B delayed by 1/2 of the Sample Period, t.

inputs are processed by the DHVM, it selects the low median signal at a rate that is 4 to 15 times faster than the sample rate. Because of this, the DHVM output has effectively doubled the resolution when compared to an output derived from synchronously sampled inputs. This is only true for dynamic signals that have a slope changing faster than basic bit resolution (.005 volts) per sample period. A system that samples at 125 samples/sec. asynchronous operations could increase the dynamic resolution if the input is changing faster than 1.60 volts/sec. (Example: A $\pm$ 1.00 volt P-P sine wave at .25 Hz has a maximum rate of voltage change of 1.60 volts/sec.

The effect of inherent time delay of one fourth of a sample period on a filtered increasing monotonic signal and three-fourth of a sample period on a decreasing monotonic filtered signal can also be seen in FIGURE 68.

From the above discussion the dynamic resolution could be quadrupled if an input signal was sampled by four samplers with the sampling off-set by one fourth of a sample period.

FIGURES 69 through 74 are input-output traces of the frequency sweep at $\pm$ 5.0 volts at 10 Hz and 40 Hz frequency ranges at time delayed sample rates of 80, 125 and 400 samples/sec.

The modulation that originally appeared in FIGURE 51 is not present in FIGURE 70. The only difference between the two sets of data is the time delayed sampling. FIGURE 71 also indicates a decreased amount of output distortion.

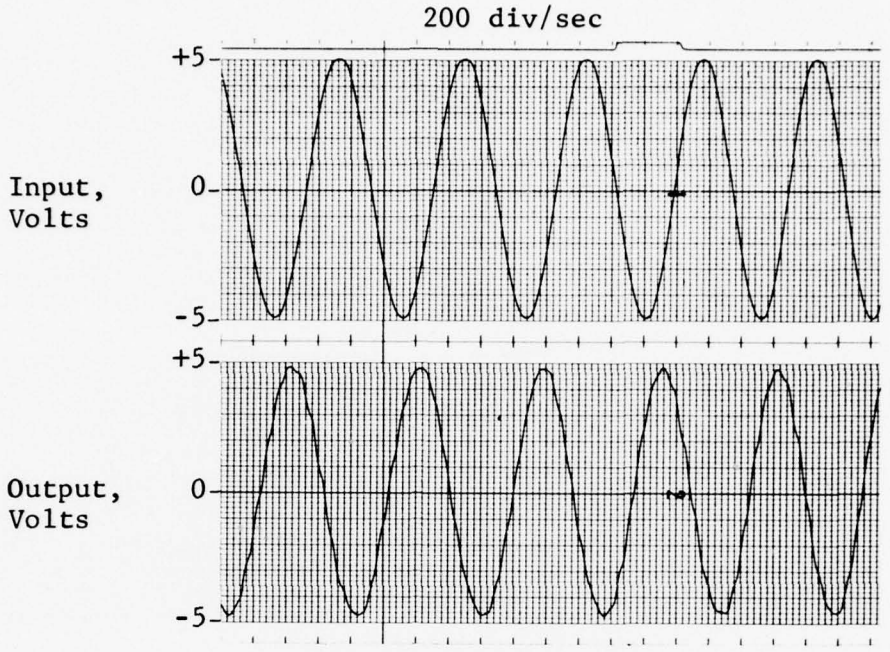


FIGURE 69 10 Hz Input-Output at 80 samples/sec., Time Delay

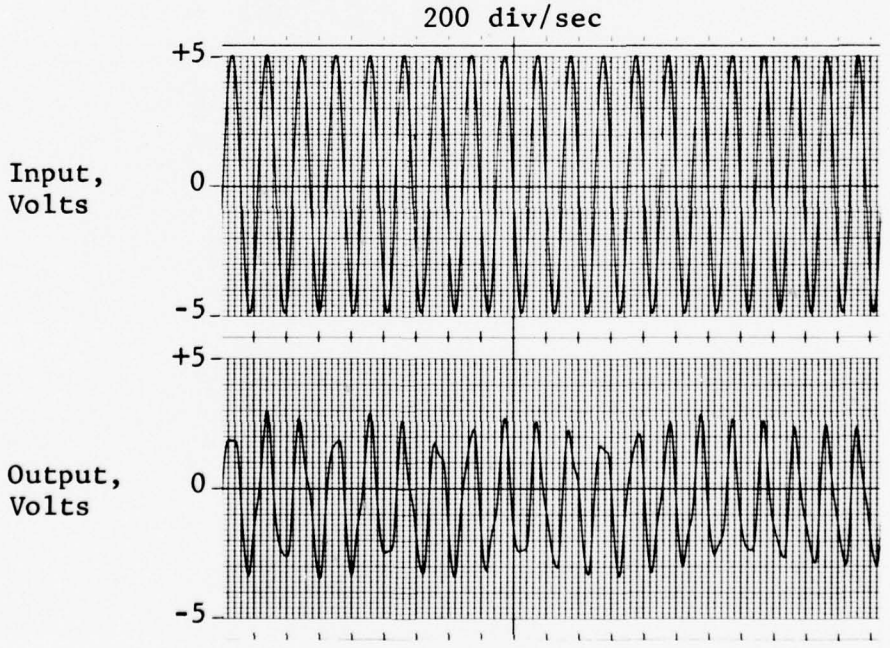


FIGURE 70 40 Hz Input-Output at 80 samples/sec., Time Delay

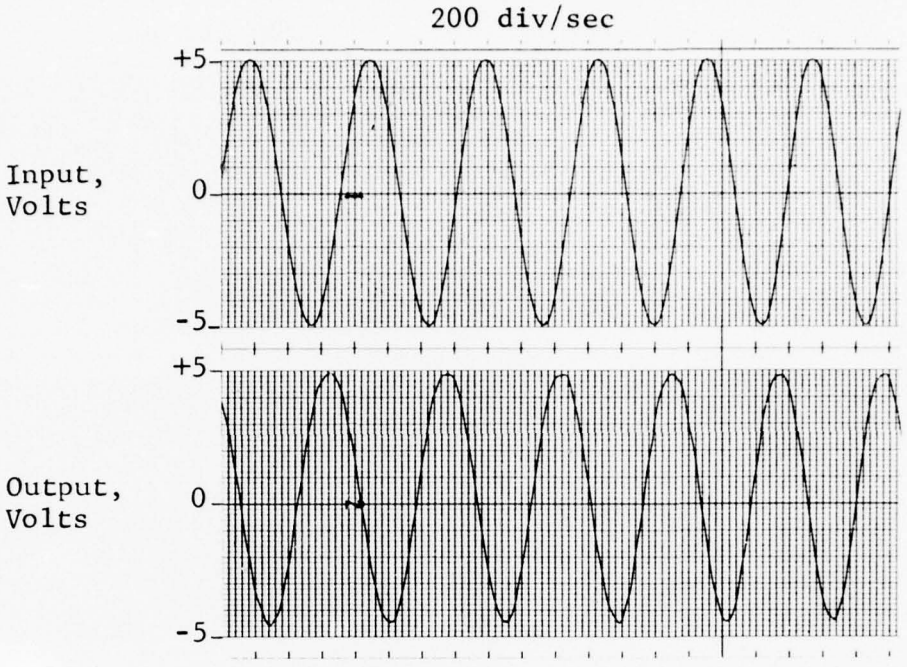


FIGURE 71 10 Hz Input-Output at 125 samples/sec., Time Delay

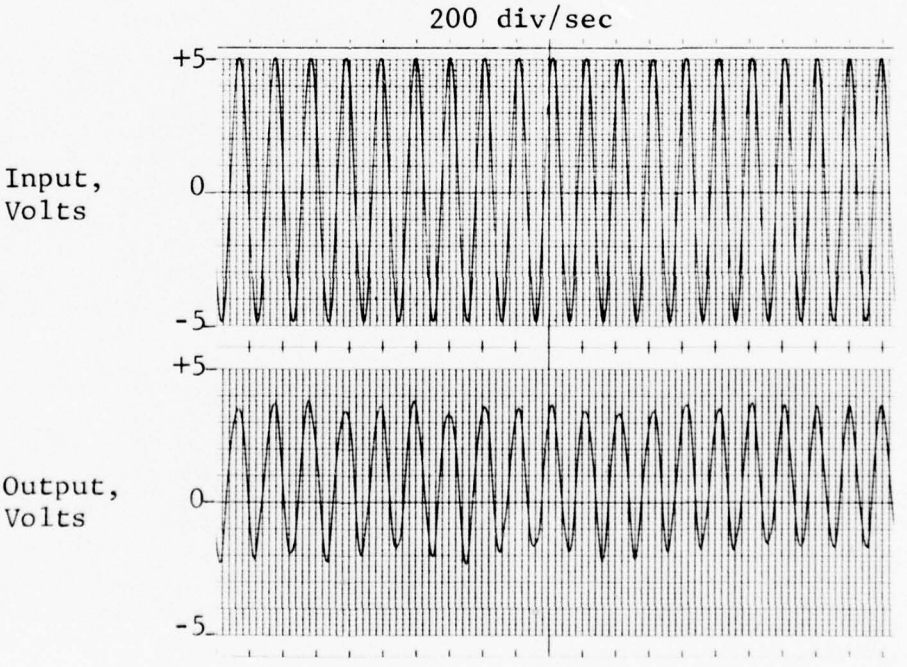


FIGURE 72 40 Hz Input-Output at 125 samples/sec., Time Delay

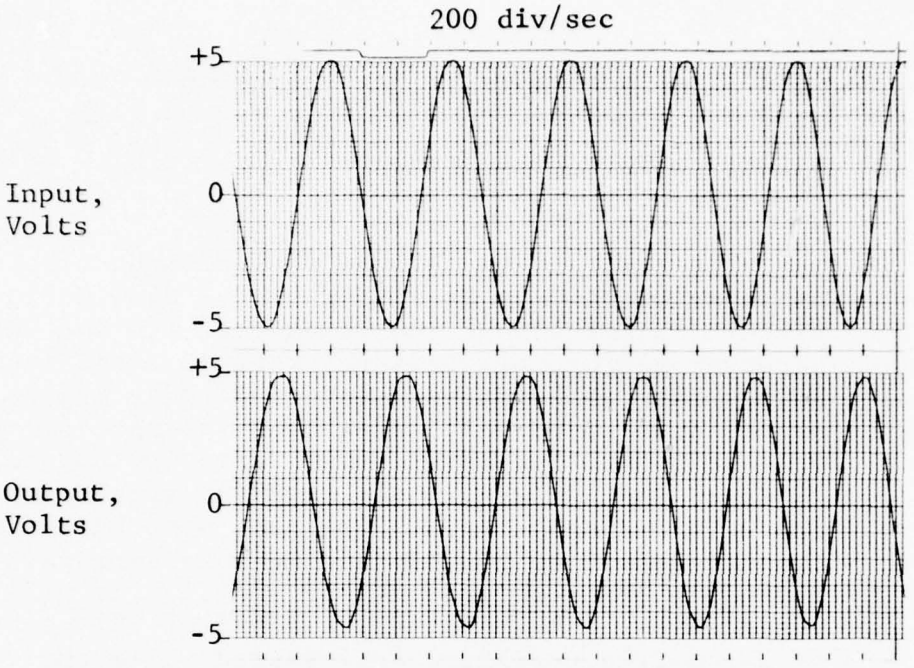


FIGURE 73 10 Hz Input-Output at 400 samples/sec., Time Delay

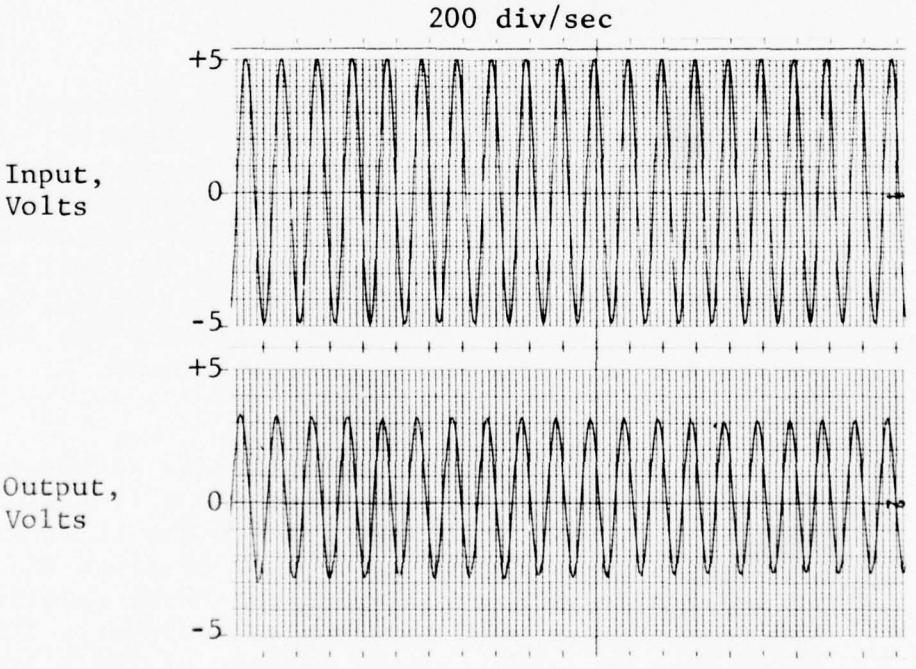


FIGURE 74 40 Hz Input-Output at 400 samples/sec., Time Delay

4.2.4 Phase II Failure Mode Testing

4.2.4.1 Test Description

The test set-up for the failure mode testing was as shown previously in FIGURE 37. A combination of sixteen failure modes including one, two and three hardover and/or null failures were injected into the DHVMT. The failures were injected under static null, static bias -1.00 volt and a dynamic input of $\pm$ 2.5 volt at 5 Hz. The DHVMT sample rate was 80/sec., 125/sec. and 400/sec. while sampling synchronously. The DHVM was updating at 1465/sec. with the error counter set at 5, 10, 50 and 100 total errors. The allowable error weight was set at 3.12% of a full scale value $\pm$ 10.0 volts. A total of 161 combinations of parametric variation were tested while the four DHVMT inputs, HFCS input, and HFCS output were recorded on a strip chart recorder.

4.2.4.2 Test Results

The test data did not indicate any output transients when up to two failures were injected. The third failure did create an output transient when the injected failure was more positive than the actual input signal. This is an expected result because the DHVM selects the low median signal. The failure input amplitude is the DHVM output for a period of time that is dependent on the DHVM update rate and the allowable errors set into the error counter circuit.

The HFCS input and output signals as shown on FIGURES 75 through 78 illustrate the effect of injecting a $\pm$ 4.00 volt hardover for the third failure. The traces represent error counter settings of 100, 50, 10 and 5 allowable errors with the DHVMT sampling at 400/sec. and the DHVM updating at 1465/sec. This data shows that an error counter setting of 100 allows a much larger step as a system output in terms of time and

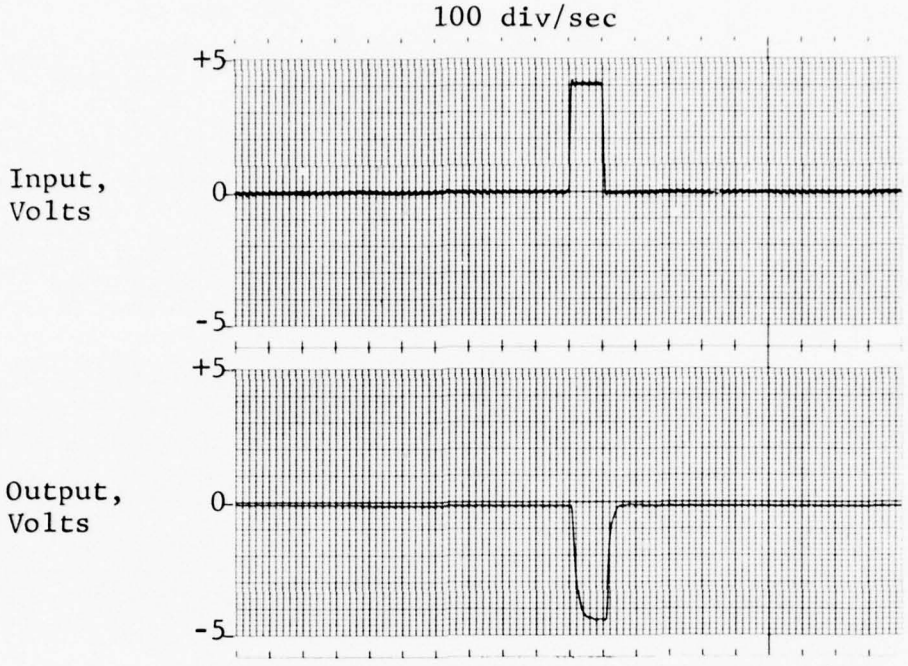


FIGURE 75 Third Failure Transients with 100 Errors

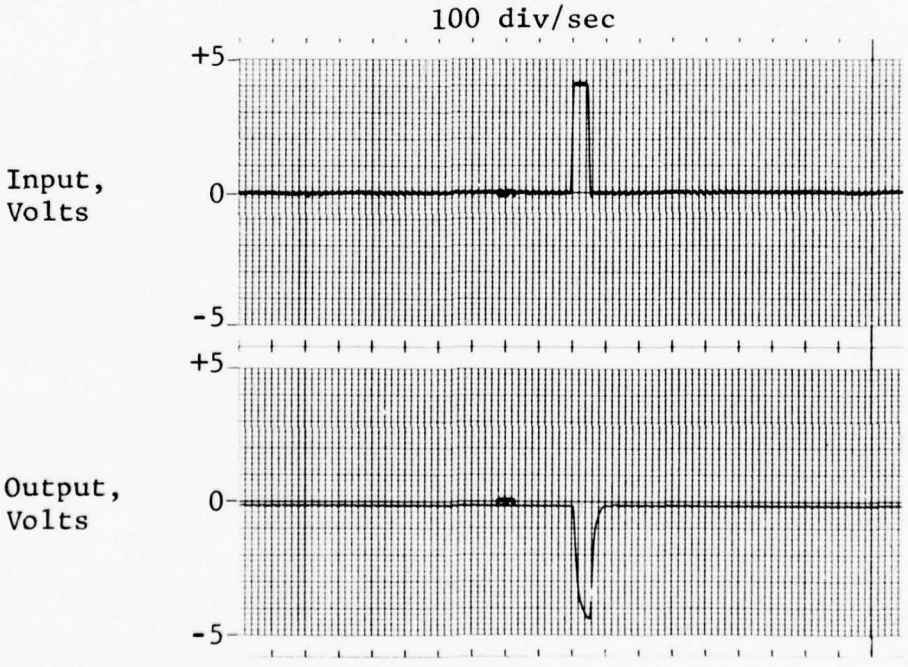


FIGURE 76 Third Failure Transients with 50 Errors

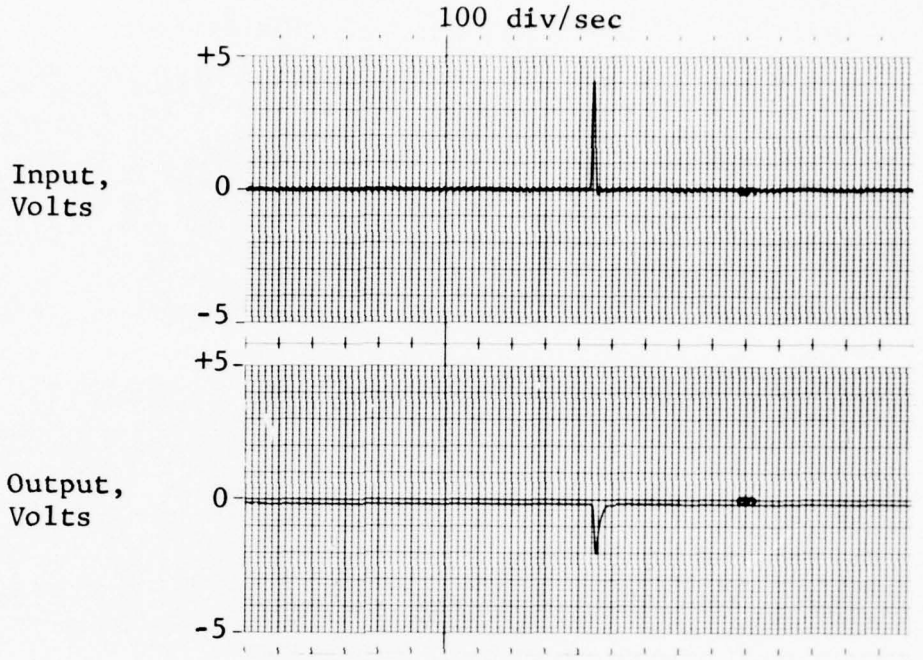


FIGURE 77 Third Failure Transients with 10 Errors

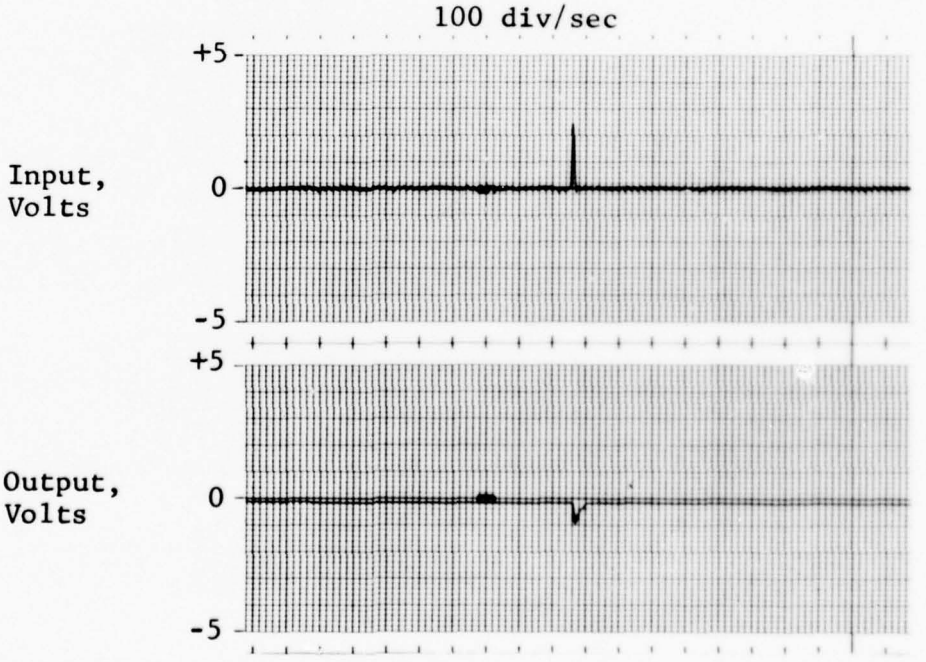


FIGURE 78 Third Failure Transients with 5 Errors

amplitude than a setting of 5 errors. The instrumentation chart recorder used had a limited response and only indicated the trend not the actual values. Therefore, TABLE 12 was prepared from actual oscilloscope data for a third hardover of +10.0 volts.

The data in TABLE 12 indicates that the selection of an error counter setting requires the system designer to determine the time and amplitude ofa pulse that system will tolerate without negative effect. Items that would determine this in an aircraft system would be the surface position deviation and the resulting air frame response.

TABLE 12

ERROR COUNTER COMPARISON

	HFCS Input		HFCS Output		
DHVM Allowable, Errors	Amplitude Volts	Width msec.	Peak Amplitude Volts	Rise Time msec.	Decay Time msec.
5	10.0	3.4	4.7	3.4	25
10	10.0	6.8	7.3	6.8	25
50	10.0	34.0	10.0	25.0	25
100	10.0	68.0	10.0	25.0	25

During this failure mode test series, a negative 10 volt hardover DHVM output was observed for the period of time that the reset switch was in the reset position.

This would not be a desirable feature of the DHVM if adapted to a flight control system. This could be corrected by triggering a single shot multivibrator to limit the reset to a single update period function.

4.2.5 Summary of Phase II Test Results

4.2.5.1 Base Line HFCS Testing

In order to protect the electro-hydraulic servo valves it was necessary to set the DHVM to its maximum update rate of 1465/sec. The servo valves responded to slower update rates, causing a "bang-bang" operation of their first stages which could potentially damage the valves. This is an area to be considered in applications of the DHVM.

4.2.5.2 The Effect of Sample Rate Variation On The 680J Simulator

The DHVMT and DHVM caused an additional 30^{o} of phase lag and noticeable signal distortion when the ratio of the sample to input frequency was 8:1. This is 7.5^{o} more phase shift than theoretically predicted for a zero order sampler at this frequency ratio. Low frequency amplitude modulation of the system output was present when the input frequency was at 1/2, 1/3 and 1/4 of the sample frequency. The amplitude modulation was 100% at the sample frequency, less at 1/3 and 1/4 of the sample frequency.

4.2.5.3 680J Asynchronous Clock Operation

Asynchronous operation (fixed clock skew) improved the phase lag, distortion and resolution measurements of the system output as compared to synchronous operation.

4.2.5.4 Phase II Failure Mode Testing

Positive hardovers as a third failure create an output transient that is dependent on the update rate, allowable error and control system gain. No transients were observed on the system output for the first two failures.

4.3 Phase III

This phase of testing was conducted to evaluate the effect on aircraft motion of using the DHVM in an electro-hydraulic flight control system used to control a fighter-bomber aircraft. An A-7D aircraft simulation was used to represent the fighter-bomber aircraft dynamics.

4.3.1 A-7D Aerodynamic Base Line

4.3.1.1 Test Description

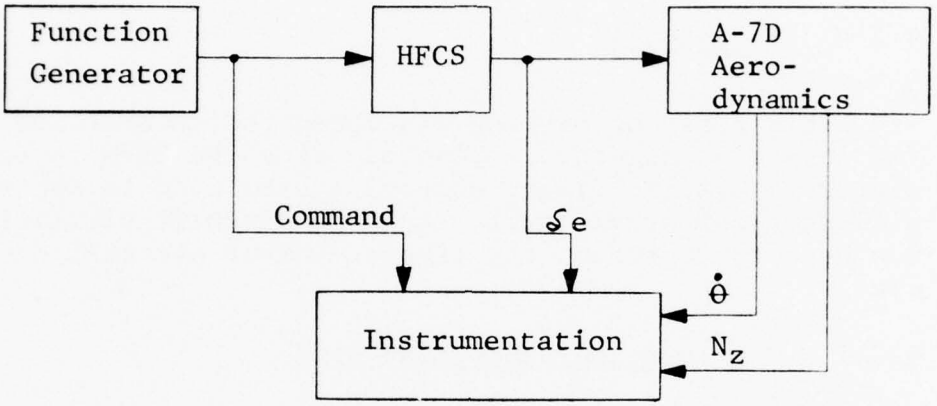
The test set-up used to obtain the baseline data without the DHVM is shown in FIGURE 79. The AFFDL/DAIS group provided the A-7D longitudinal aerodynamic simulation. The simulation was programmed on a Systron Donner Model SD-80 analog computer. The aerodynamic model stability derivatives were obtained from Reference 5.

The HFCS primary actuator was programmed to simulate the A-7D elevator actuator. The 680J secondary actuation system dynamics previously used in Phase II were substituted for the normal A-7D secondary actuator.

---

5. "Flight Test Evaluation of a Digital Flight Control System for the A-7D Simulation Test Plan"; Honeywell Inc., Government and Aeronautical Products Div.; Contract Item A-005 of Contract AF-33615-73-C-3098, 15 February 1974

The A-7D primary actuator parameters for the longitudinal axis as obtained from Reference 5 are: Frequency Response - 20 radians at -3db, No Load Slew Rate - 25°/sec., Maximum elevator position 6.25° down and 26.5° up.



Where:

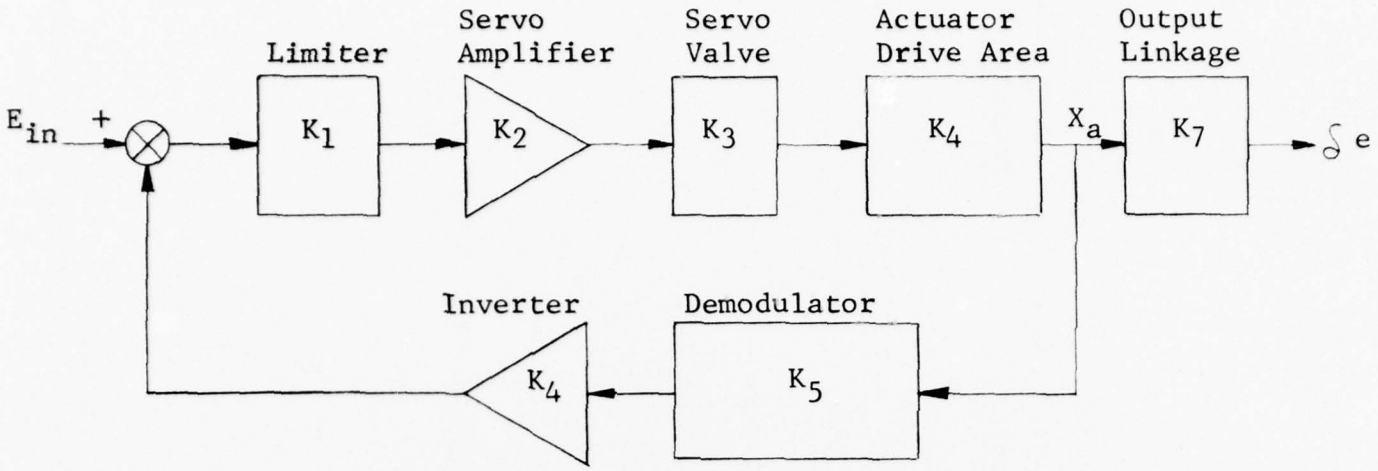
e = elevator position

$\dot{\theta}$ = pitch rate

N_Z = normal acceleration

FIGURE 79 Phase III Base Line Test Set-Up

The HFCS primary section was programmed as shown in FIGURE 80 to provide an A-7D primary actuator model.



Where:

K_1 = 1.0 volt/volt with limits of $\pm$ 1.26 volt

K_2 = 3.16 ma/volt

K_3 = 1.55 cis/ma

K_4 = .98 in^2

K_5 = 4.00 volts/in.

K_6 = 1.00 volt/volt

K_7 = 4°/in.

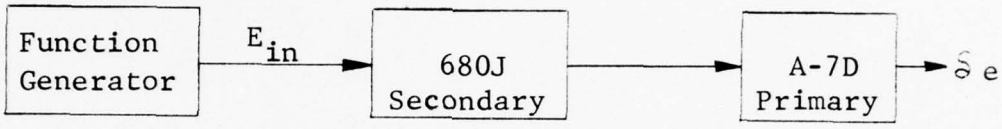
E_{in} = Input voltage from HFCS secondary

δe = Elevator position

X_a = Actuator motion

FIGURE 80 A-7D Primary Actuator Model

The HFCS total system was programmed as shown in FIGURE 81 to provide an input-output relationship of 1.0 degree/volt in order to interface with the A-7D aerodynamic simulation.



Where:

E_{in} = Input Voltage

δe = Elevator Position

$E_{in}/\delta e = 1^{o}$/volt

FIGURE 81 HFCS - Aero Simulation Interface

4.3.1.2 Test Results

Since the aerodynamic simulation was valid only for small amplitude perturbations, all testing for dynamic response and step data was limited to $\pm$ 2.0 degree

surface deflection inputs.

FIGURE 82 shows baseline frequency response of the simulated A-7D surface position and FIGURE 83 shows the measured slew rate. Both the frequency response and slew rate agreed with A-7D parameters.

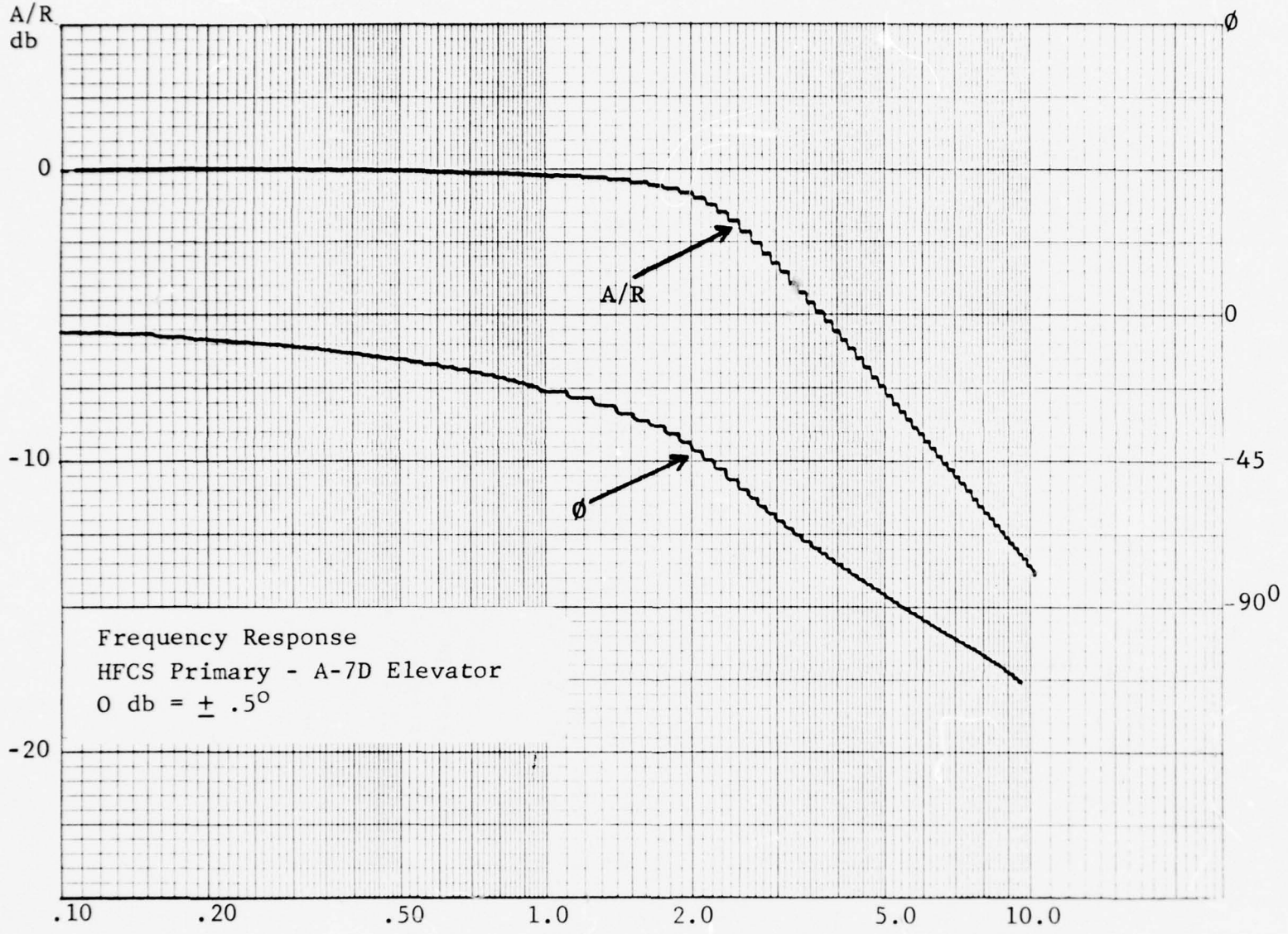
The normal acceleration (N_z) and pitch rate ($\dot{\theta}$) frequency responses are as shown in FIGURES 84 and 85 respectively. The δ_e, N_z and $\dot{\theta}$ step responses are shown in FIGURE 86.

4.3.2. A-7D Aerodynamic Testing with DAIS Hardware Interfaced

4.3.2.1 Test Description

The DHVMT and DHVM were interfaced with the A-7D longitudinal axis hardware and aerodynamic simulation as shown in FIGURE 87.

The baseline tests were repeated for comparison. For these tests the DHVMT was again operated at 80 samples/sec. and 125 samples/sec. with the DHVM operating at 1465 updates/sec.


A/R
db
0
-10
-20
Ø
0
-45
-90°
A/R
Ø
Frequency Response
HFCS Primary - A-7D Elevator
0 db = ± .5°
.10
.20
.50
1.0
2.0
5.0
10.0

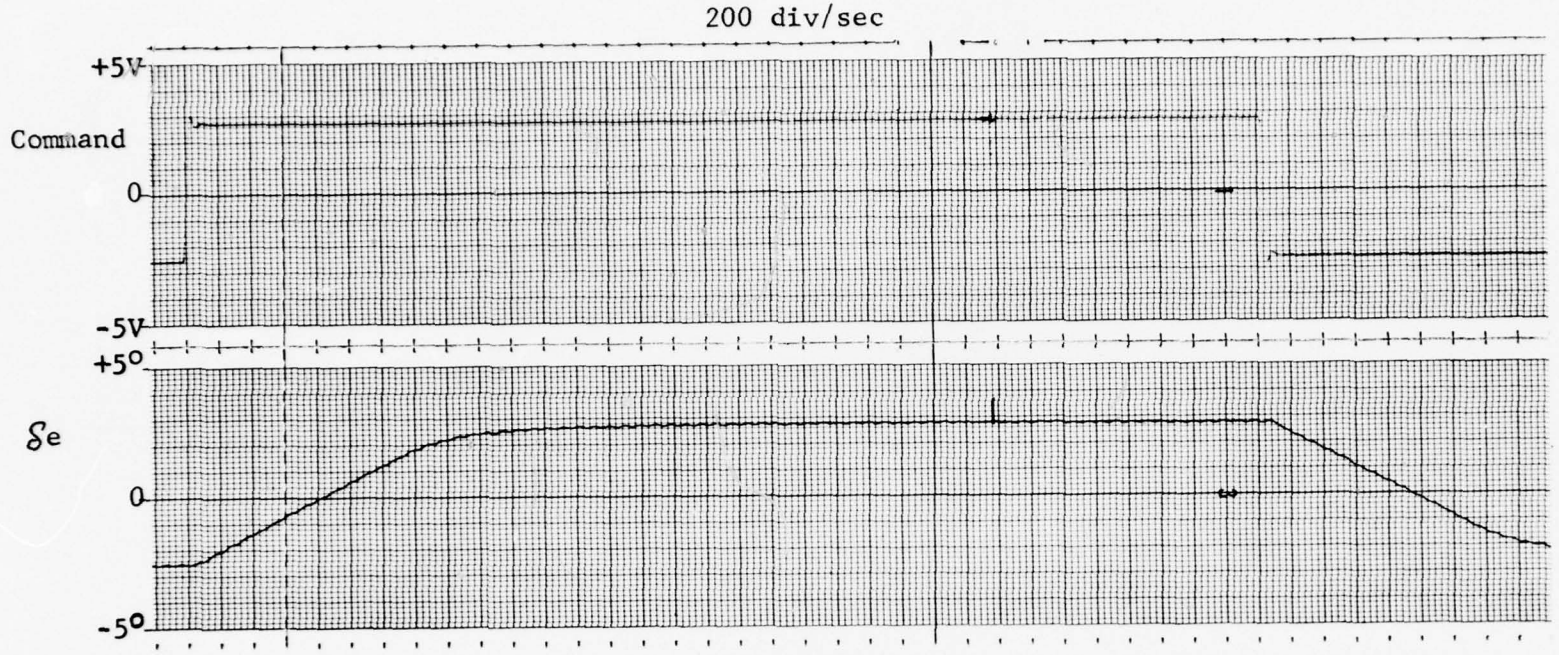


FIGURE 83 A-7D Actuator Slew Rate

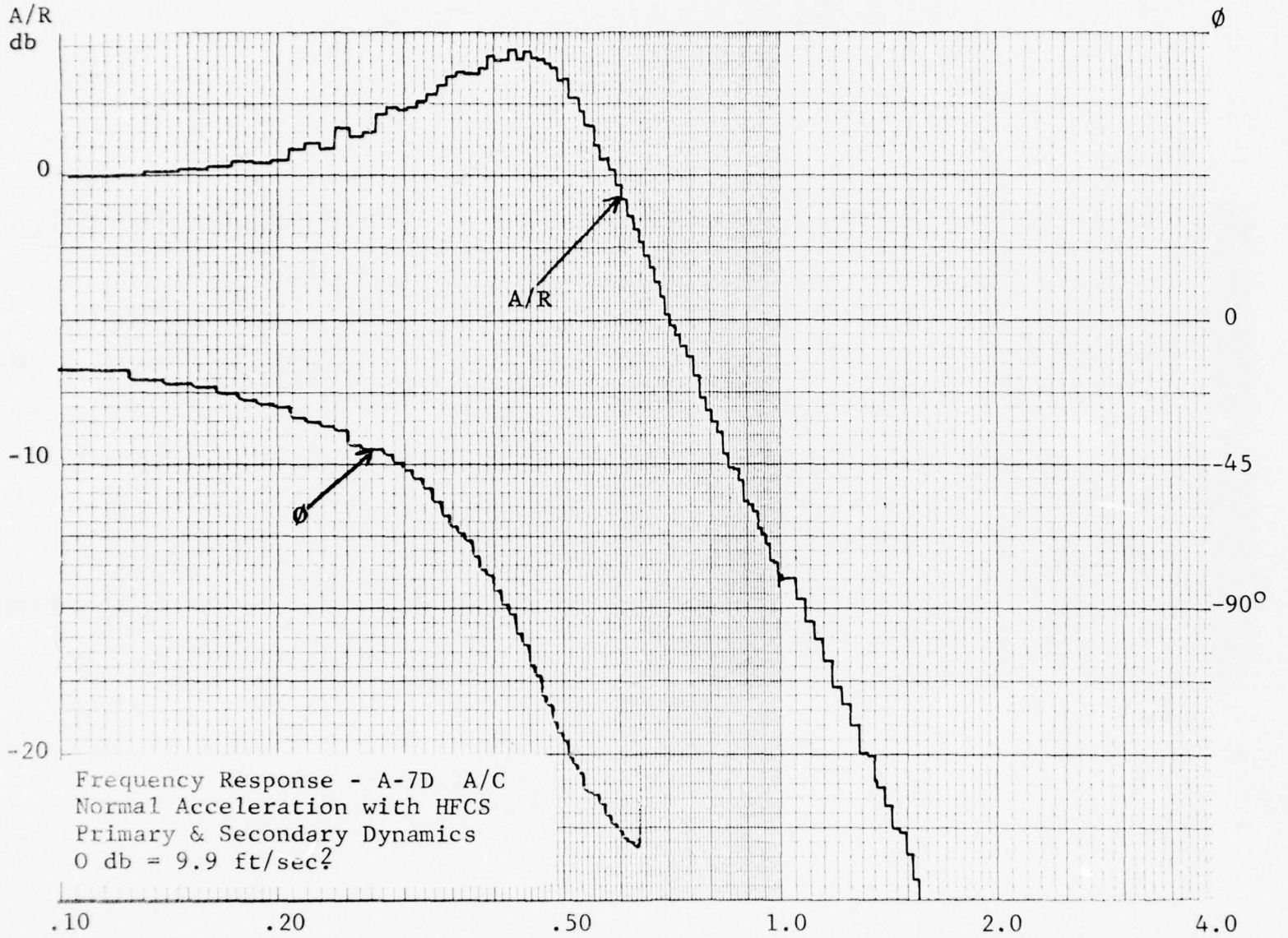

A/R
db
Ø
0
-10
-20
0
-45
-90°
A/R
Ø
Frequency Response - A-7D A/C
Normal Acceleration with HFCS
Primary & Secondary Dynamics
0 db = 9.9 ft/sec²
.10
.20
.50
1.0
2.0
4.0
FREQUENCY Hz

FIGURE 84

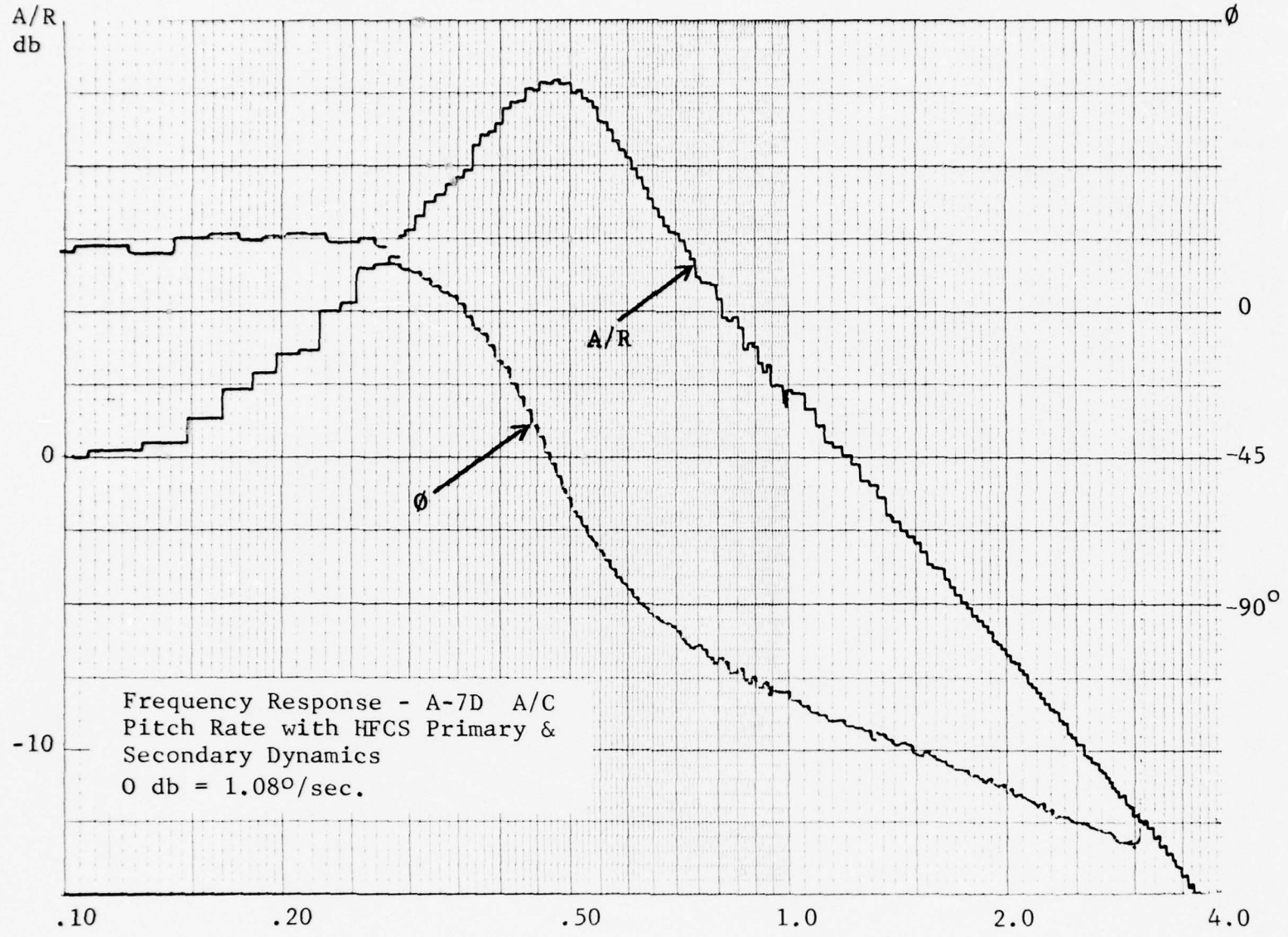

A/R
db
Ø
0
-45
-90°
-10
A/R
Ø
Frequency Response - A-7D A/C
Pitch Rate with HFCS Primary &
Secondary Dynamics
0 db = 1.08°/sec.
.10
.20
.50
1.0
2.0
4.0
FREQUENCY Hz

FIGURE 85

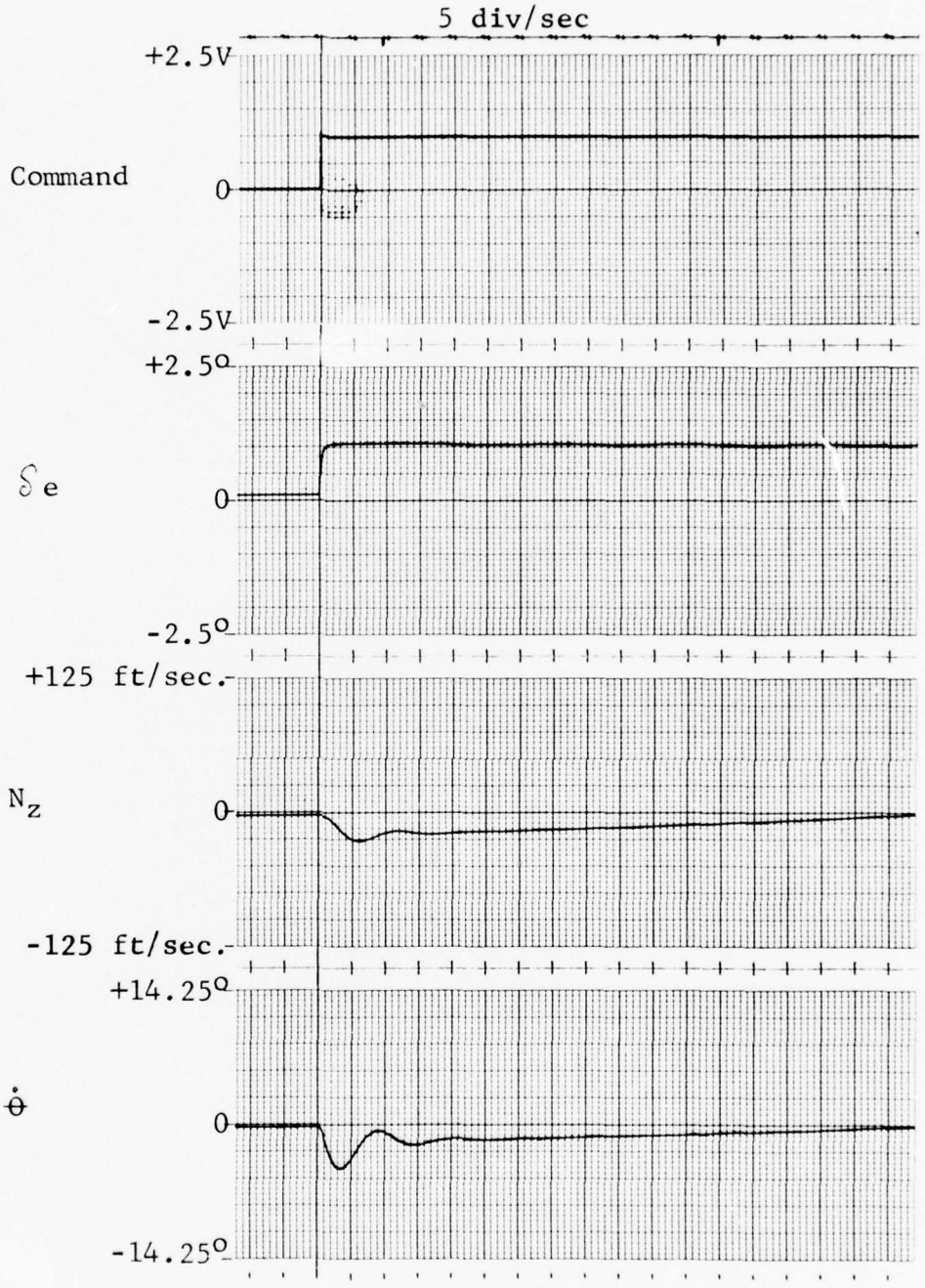


FIGURE 86 Aerodynamic Baseline Data A-7D Pitch Axis Step Response

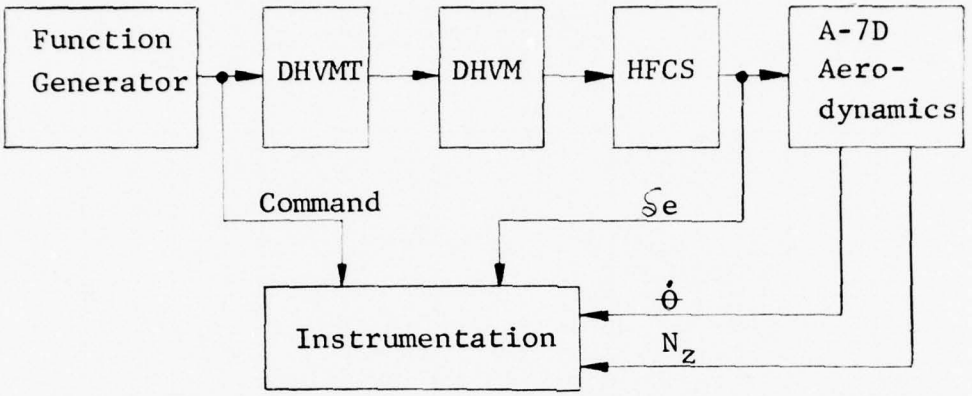


FIGURE 87 Phase III DAIS Test Set-Up

4.3.2.2 Test Results

FIGURES 88, 89, and 90 are the test results when the DHVMT was operated at 80 samples/sec.

The test data recorded with the DHVMT operating at 125 samples/sec. is shown in FIGURES 91, 92 and 93.

Comparing the baseline data to the data recorded with the DHVMT and DHVM in the control system did not show any difference.

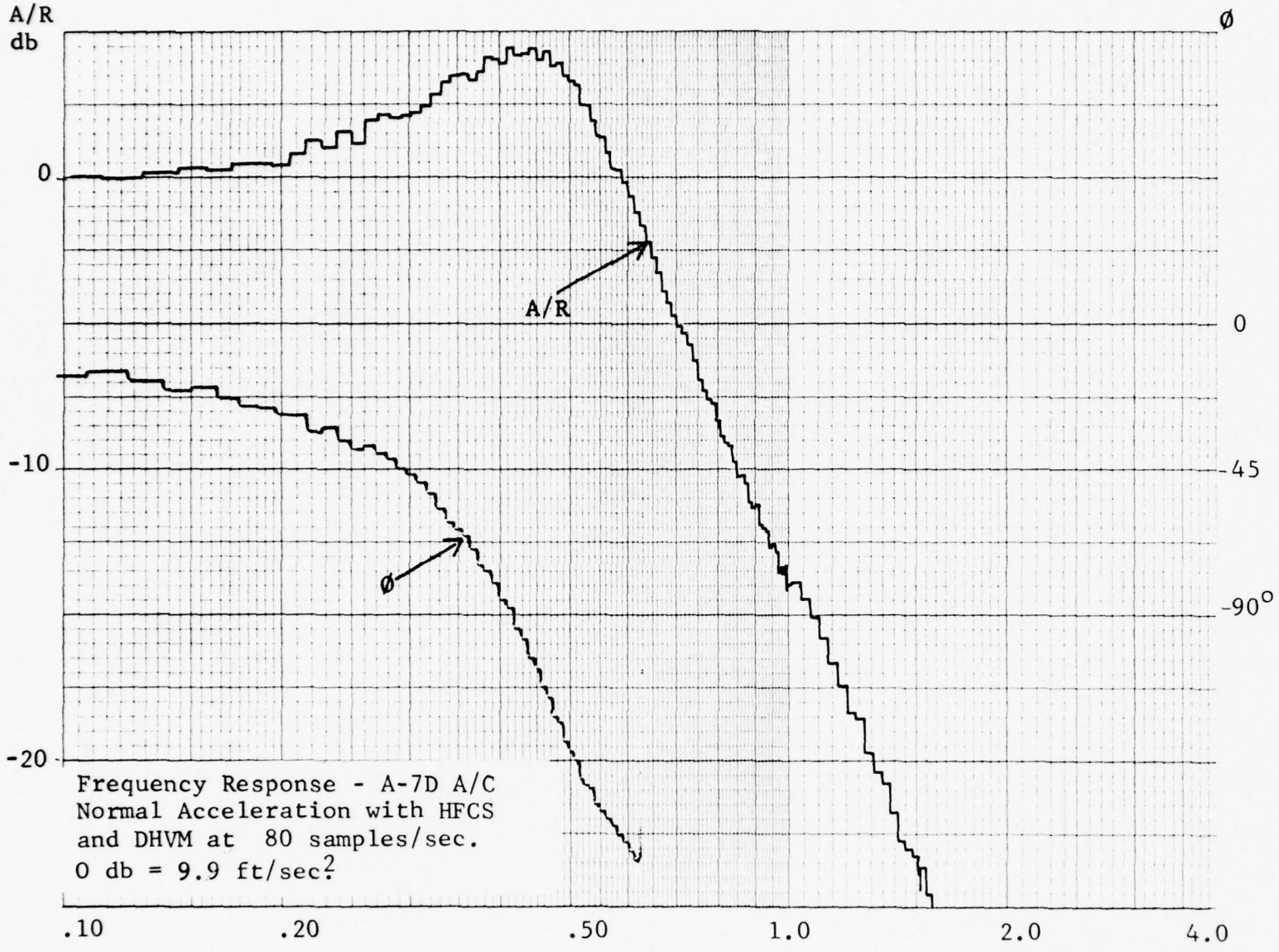


FIGURE 88 FREQUENCY, Hz

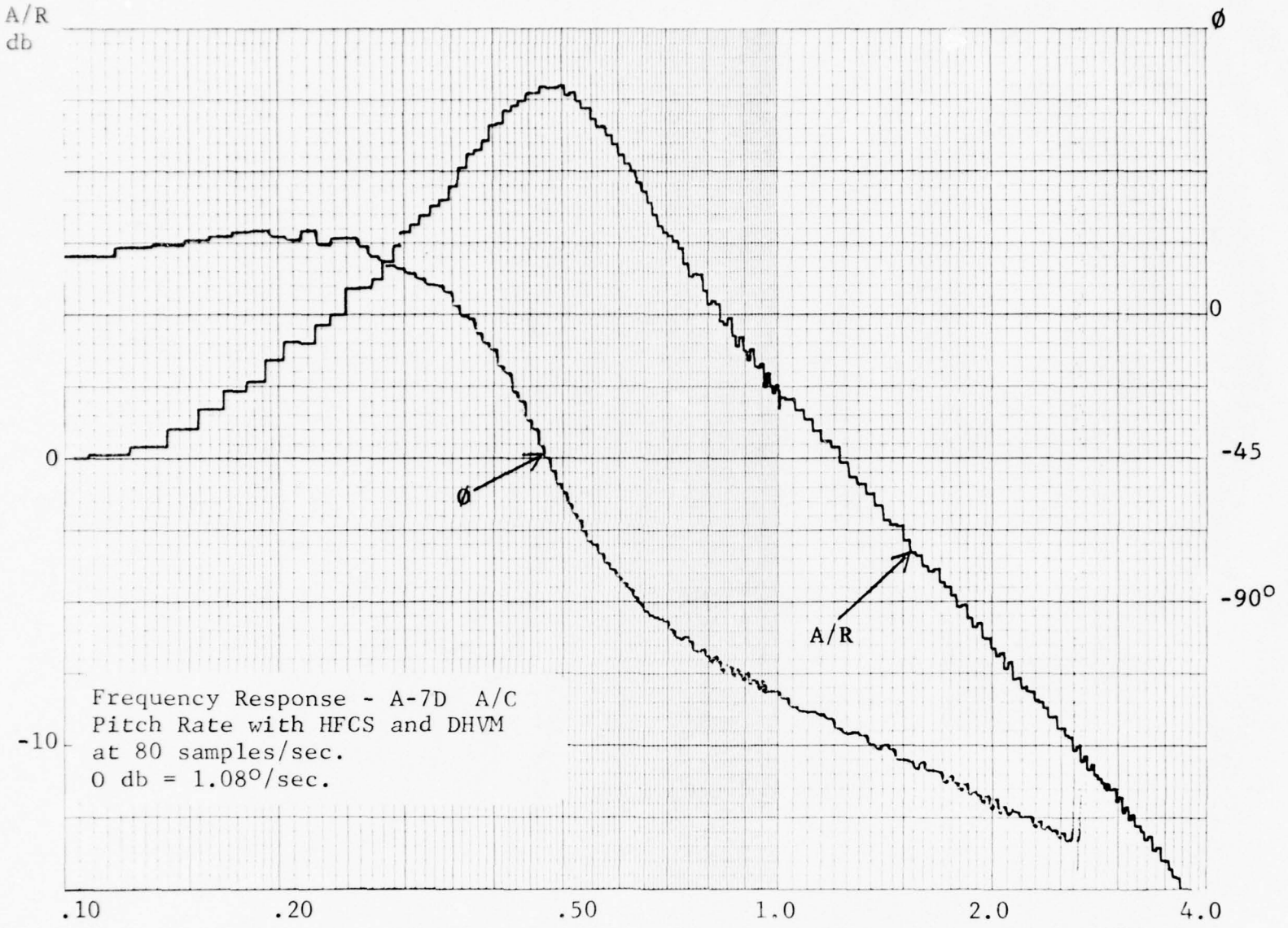

A/R
db
Ø
0
-45
-90°
0
-10
Ø
A/R
Frequency Response - A-7D A/C
Pitch Rate with HFCS and DHVM
at 80 samples/sec.
0 db = 1.08°/sec.
.10
.20
.50
1.0
2.0
4.0
FREQUENCY Hz

FIGURE 89

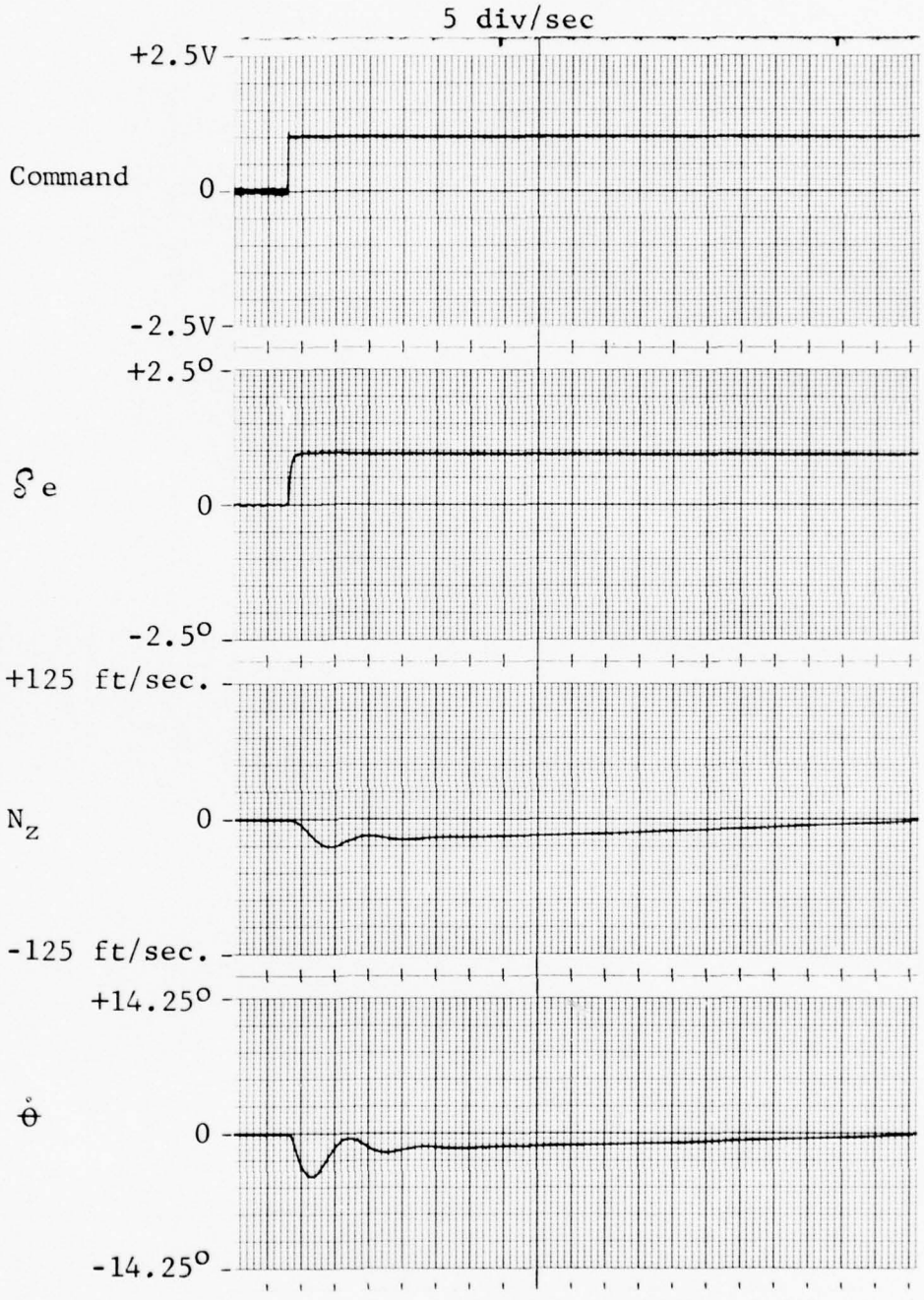


FIGURE 90 Aerodynamic Data A-7D Pitch Axis Step Response, at 80 samples/sec.

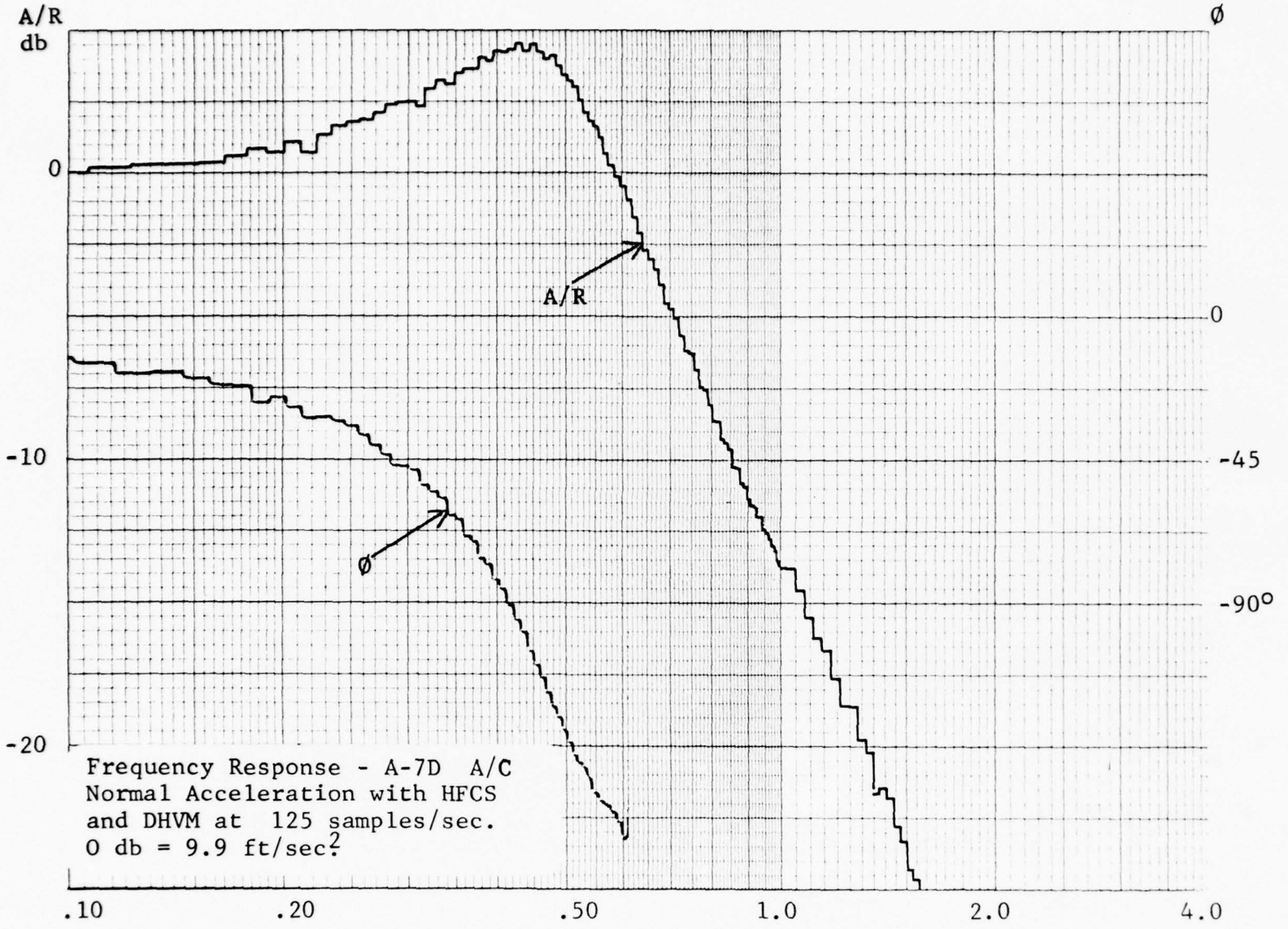

A/R
db
Ø
0
-10
-20
0
-45
-90°
A/R
Ø
Frequency Response - A-7D A/C
Normal Acceleration with HFCS
and DHVM at 125 samples/sec.
0 db = 9.9 ft/sec²
.10
.20
.50
1.0
2.0
4.0
FREQUENCY Hz

FIGURE 91

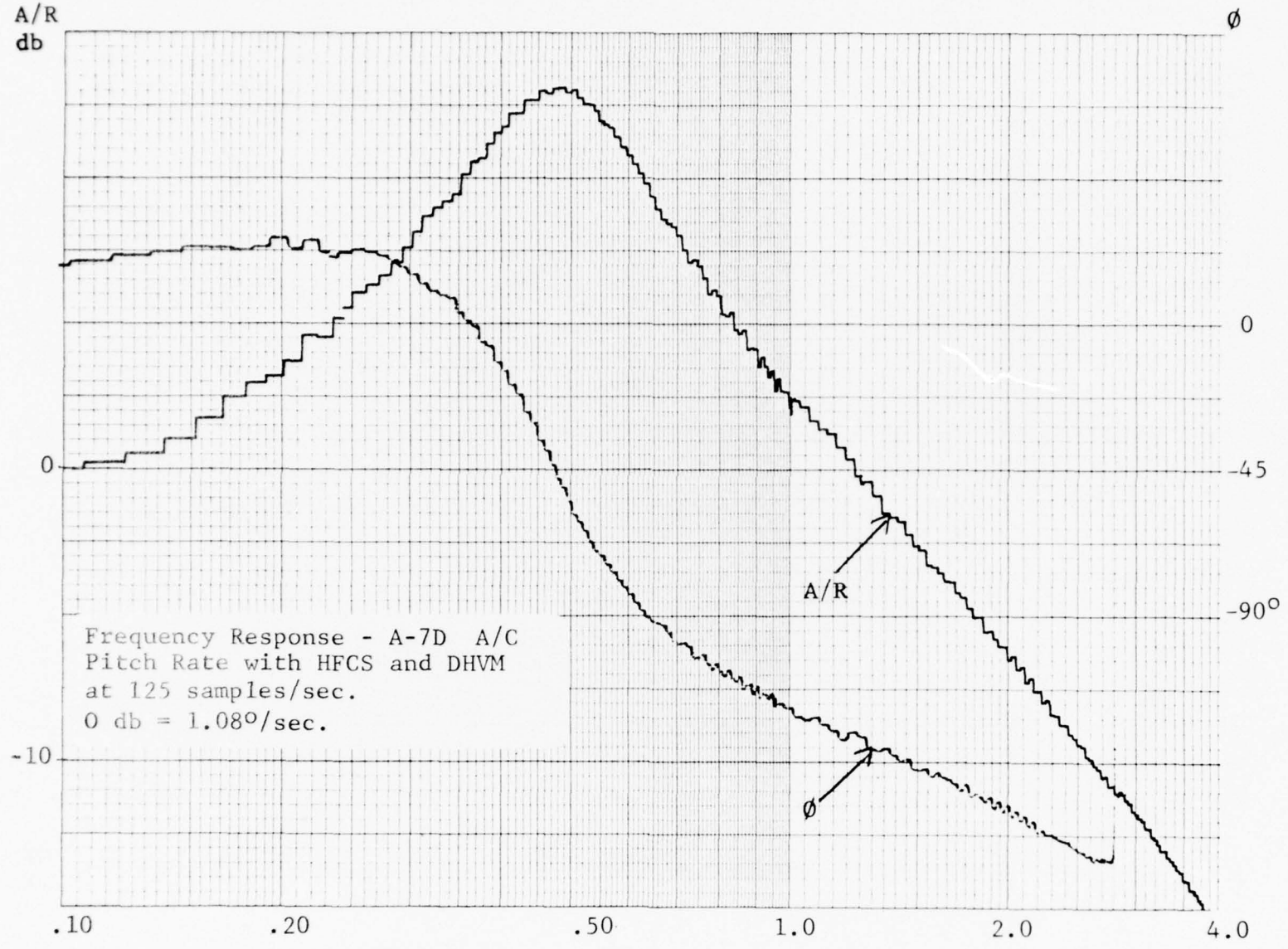

A/R
db
Ø
0
-45
-90°
0
-10
A/R
Ø
Frequency Response - A-7D A/C
Pitch Rate with HFCS and DHVM
at 125 samples/sec.
0 db = 1.08°/sec.
.10
.20
.50
1.0
2.0
4.0
FREQUENCY Hz

FIGURE 92

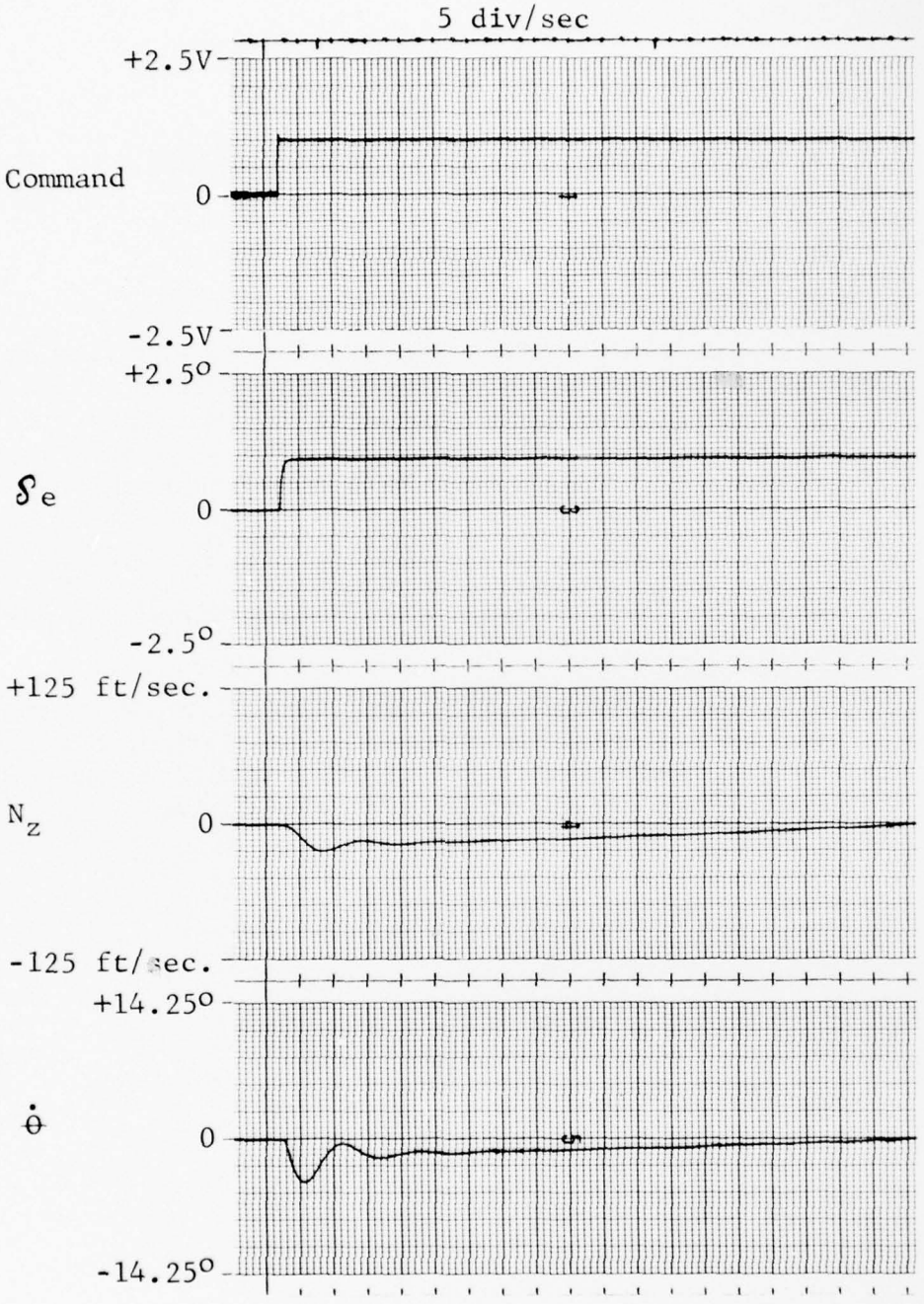


FIGURE 93 Aerodynamic Data A-7D Pitch Axis Step Response, at 125 samples/sec.

4.3.3 Phase III Test Result Summary

4.3.3.1 A-7D Aerodynamic Base Line

The baseline frequency response and slew rate data recorded from the simulated A-7D surface position shows good correlation with the data in Reference 5. The normal acceleration and pitch rate step and frequency responses verified that A-7D aerodynamic simulation was accurate.

4.3.3.2 A-7D Aerodynamic Testing with DAIS Hardware

The DHVMT and DHVM were interfaced in series with the A-7D simulation command. The monitored parameters δe, N_Z and $\dot{\theta}$ were not effected with the command input sampled at a rate of 80/sec. and 125/sec.

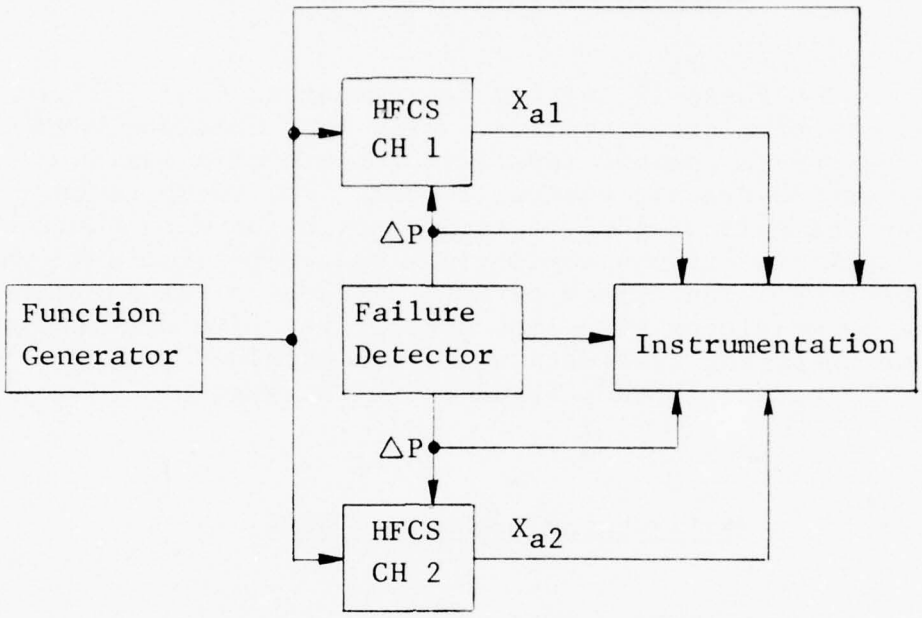
4.4 Phase IV

The Phase IV testing was conducted to establish any problem areas that may exist when multiple DHVM's are used to command separate channels of a redundant electro-hydraulic control system. For these tests two channels of 680J secondary actuation with their associated failure monitoring logic were simulated on the HFCS. The effect of multiple DHVM's was evaluated by obtaining base line data on the 680J simulation and comparing that data with data obtained with the DHVMT and two DHVM's inserted in the system.

4.4.1 Multi-Channel Base Line Data

4.4.1.1 Test Description

The HFCS was set up as a 680J secondary actuation redundant control system. References 1 and 2 were used as a guide in setting up the force sharing differential pressure ($\triangle$ P) monitoring system shown in FIGURE 94. The failure detection system was set up to detect a $\triangle$ P level of 936 psi for each actuator. To verify correct operations of the 680J two channel simulation, the frequency response of the two channel output was measured. A hardover signal was injected into one channel of the HFCS to verify correct operation of the failure detector.



Where:

X_{a1} = HFCS CH 1 Output Motion

X_{a2} = HFCS CH 2 Output Motion

Note: X_{a1} and X_{a2} are connected together with a rigid mechanical connecting bar

FIGURE 94 Multi-Channel Base Line Test Set-Up

4.4.1.2 Test Results

FIGURE 95 shows the frequency response of the HFCS as set-up for the two channel force sharing tests. This response is within the phase and ampli-

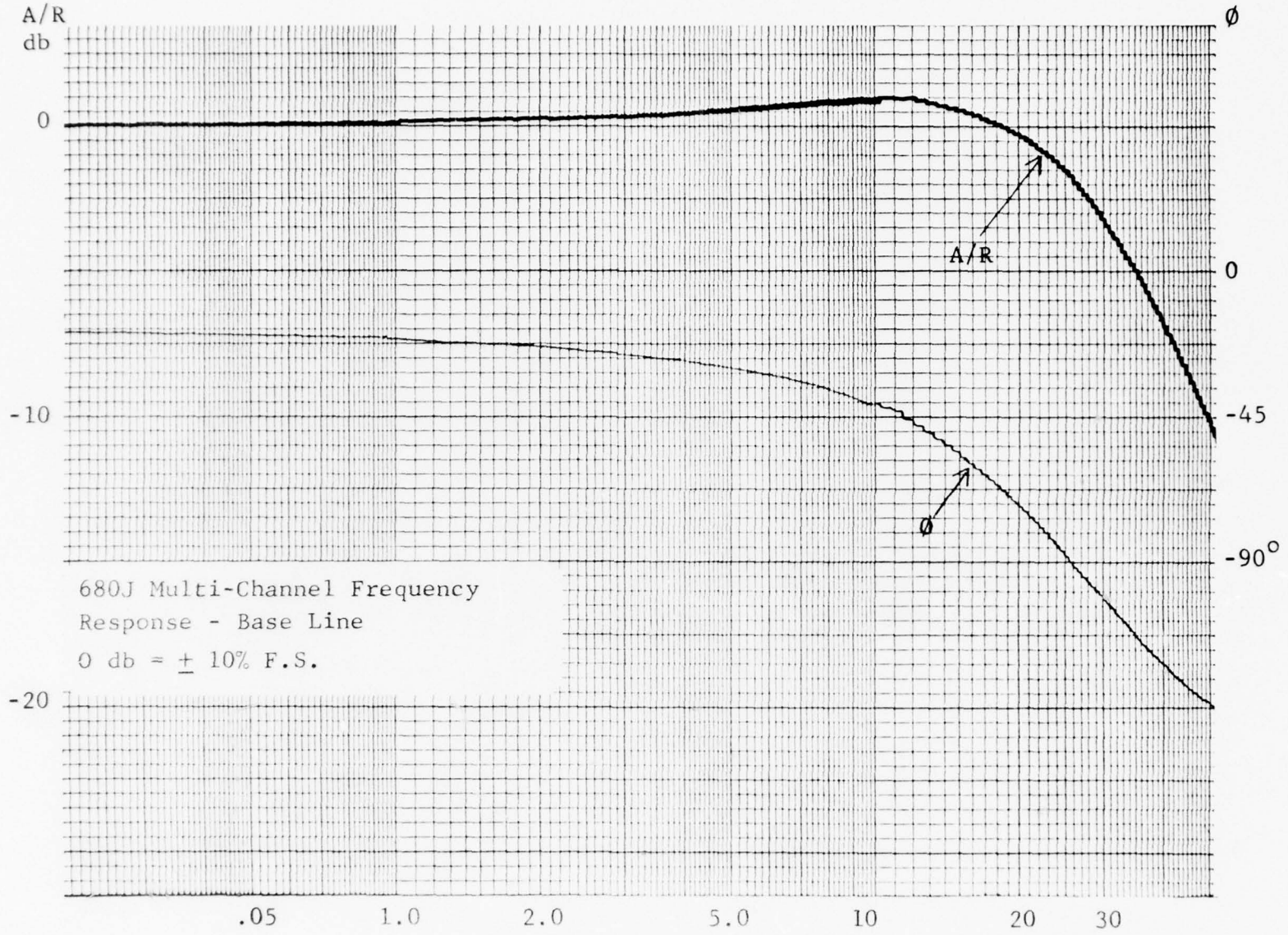

A/R
db
0
-10
-20
Ø
0
-45
-90°
A/R
Ø
680J Multi-Channel Frequency
Response - Base Line
0 db = ± 10% F.S.
.05
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 95

tude limits for the 680J secondary actuator (Reference Section 4.2.1.1).

FIGURE 96 is the result of the hardover input and shows that when ΔP reaches 936 psi, the failure monitor indicates a failure.

The baseline two channel 680J simulation did not indicate any failures when driven with a $\pm$ 5.0 volt input through the bandpass of the test set-up.

4.4.2 Multi-Channel DHVM Data

4.4.2.1 Test Description

The DHVMT and the two DHVM's were inserted into the multi-channel base line test set-up as illustrated in FIGURE 97 block diagram.

Data was recorded with the DHVMT operating at 80 samples/sec. and 125 samples/sec. The two DHVM's were operated asynchronously at the 1465 update rate. With the test equipment provided, there was no provision for controlling the amount of input update time differential between the two DHVM's Since the DHVM's updating times are approximately 1/8 of the test system's time constant, the system will not be expected to exhibit significant response deviations due to the skew of the update times between the DHVM's.

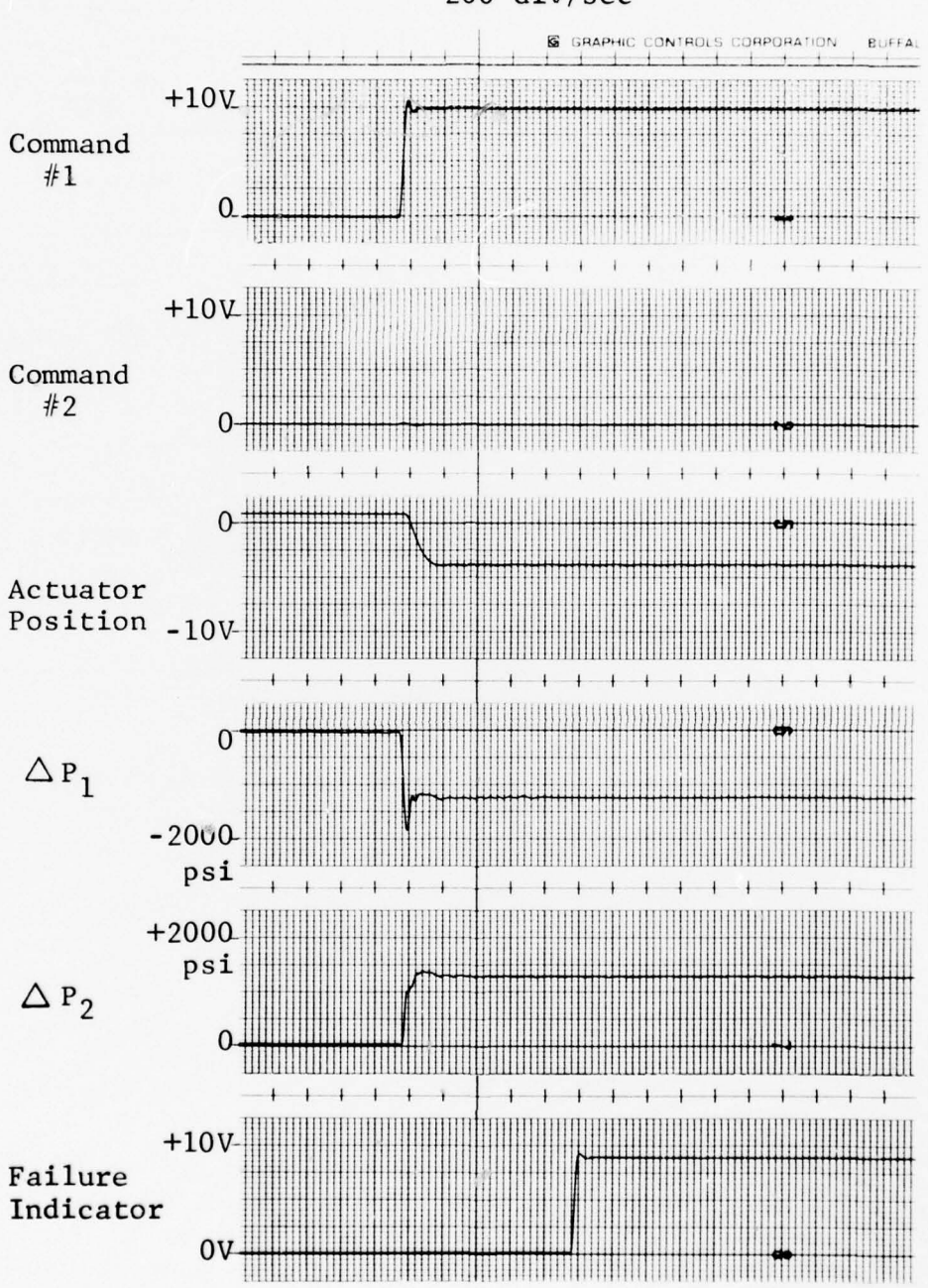
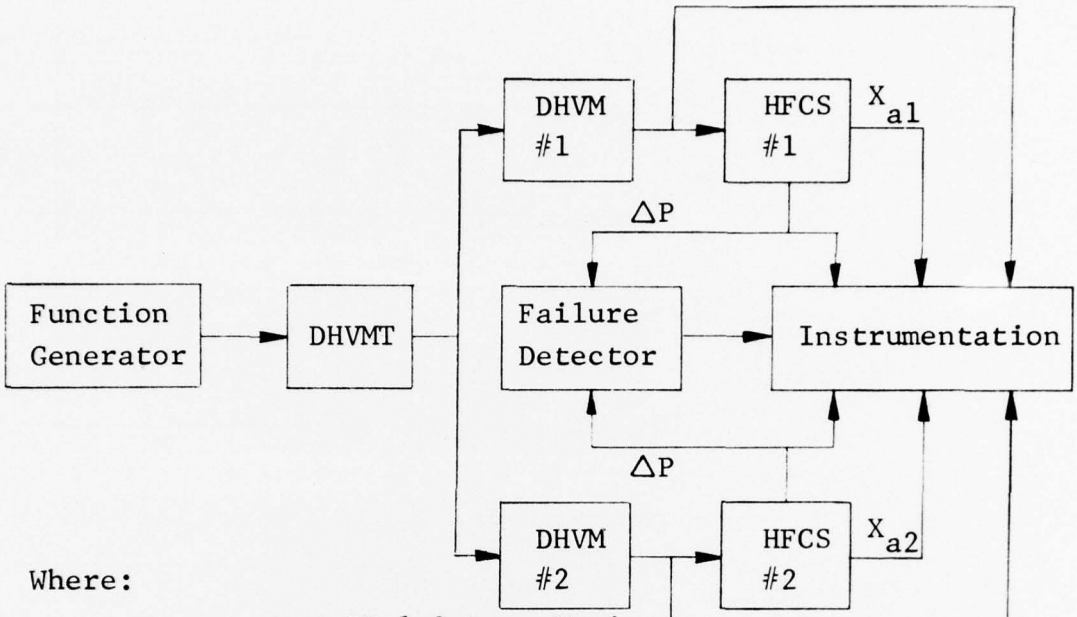


FIGURE 96 Δ P Failure Detection, Base Line



Where:

X_{a1} = HFCS CH 1 Output Motion

X_{a2} = HFCS CH 2 Output Motion

Note: X_{a1} and X_{a2} are connected together with a rigid mechanical connecting bar

FIGURE 97 Multi-Channel Test Set-Up

4.4.2.2 Test Results

FIGURES 98 and 99 are the frequency response plots at sample rates of 80/sec. and 125/sec. With the exception of the normal amplitude modulation peaking (at the 1/2 sample frequency for 80 samples/sec.) the frequency response plots appear to be the same as the base line response of FIGURE 95 in Section 4.2.2.2.

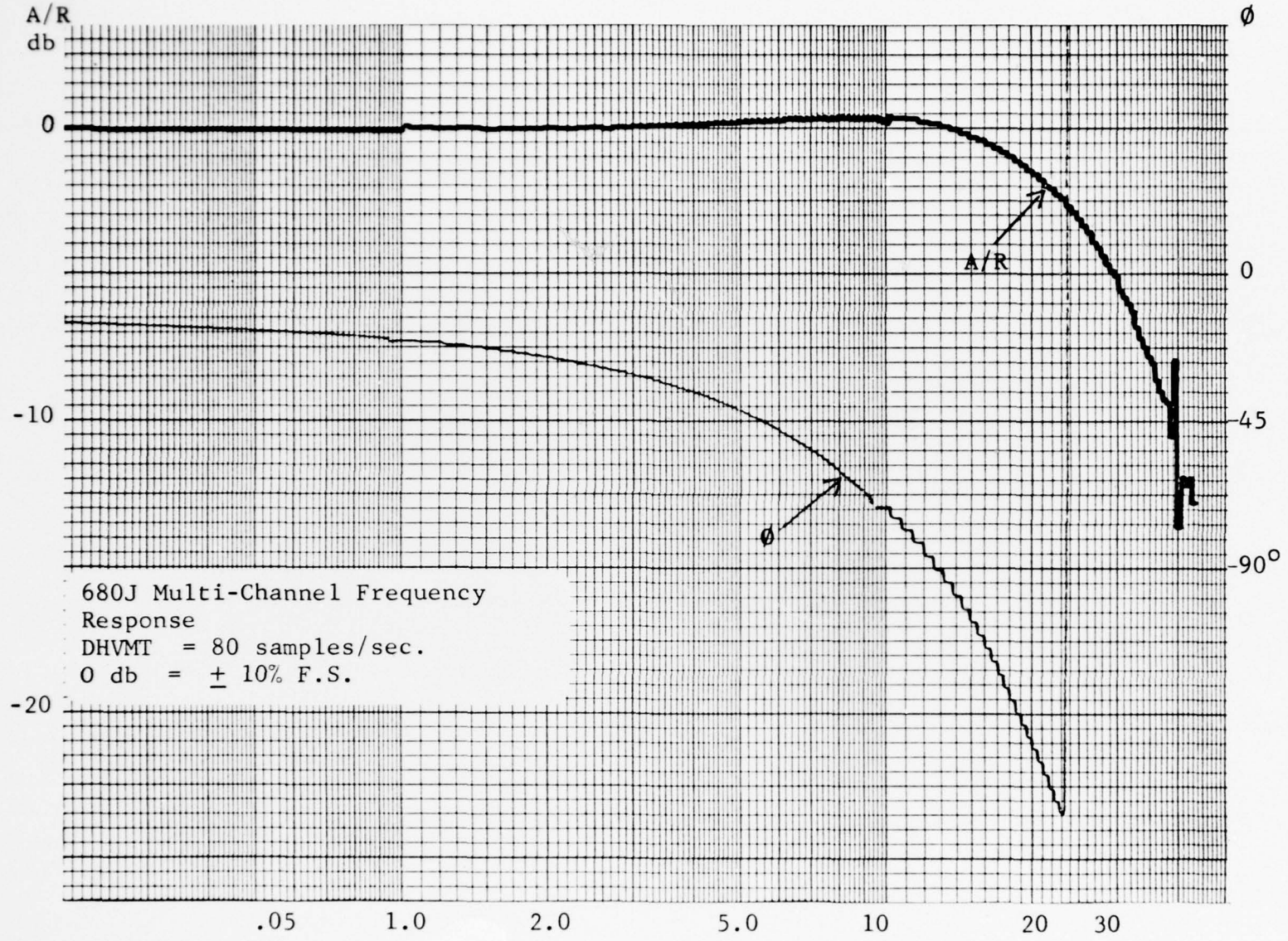

A/R
db
0
-10
-20
Ø
0
-45
-90°
A/R
Ø
680J Multi-Channel Frequency Response
DHVMT = 80 samples/sec.
O db = ± 10% F.S.
.05
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 98

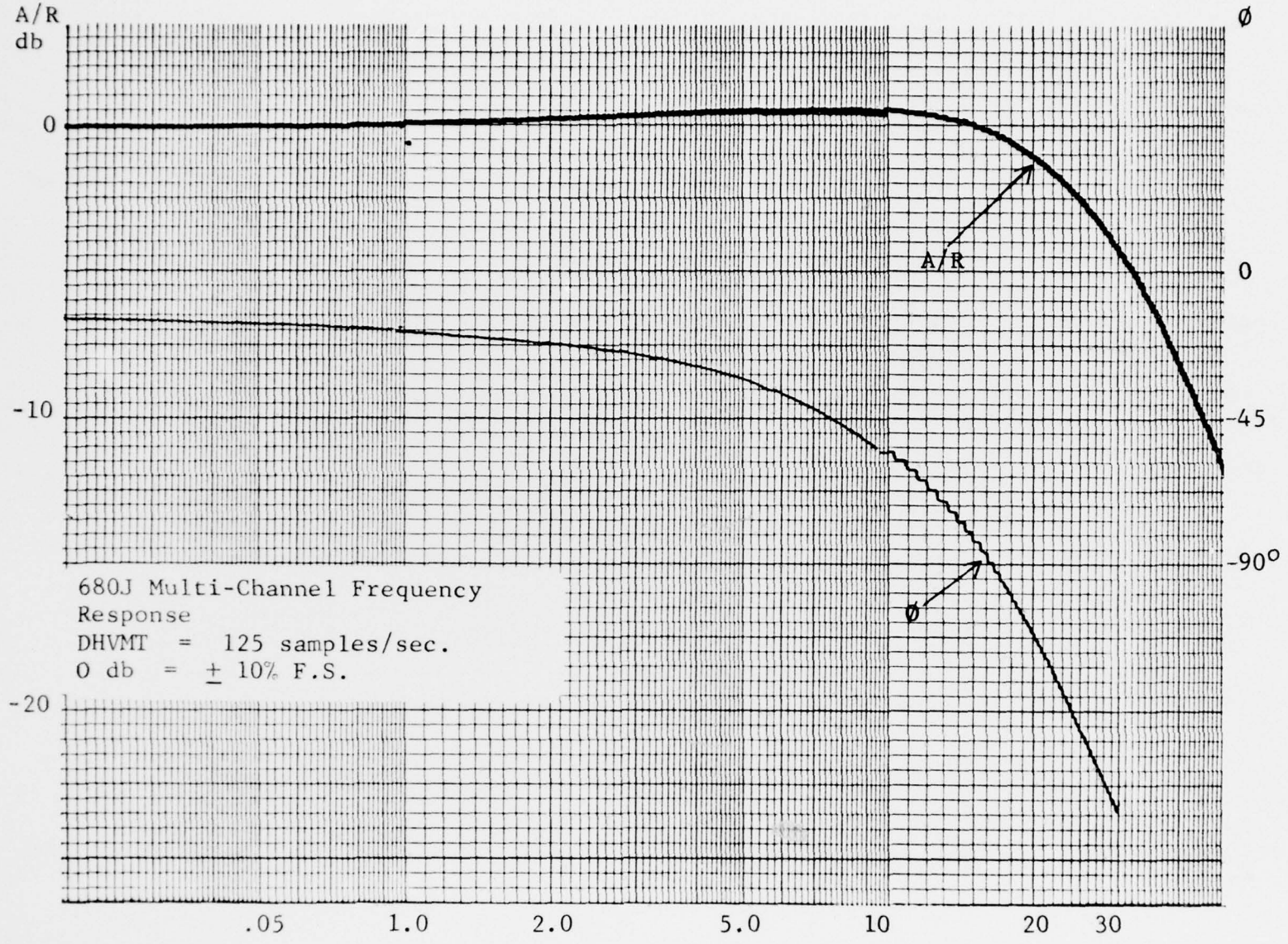

A/R
db
0
-10
-20
Ø
0
-45
-90°
A/R
Ø
680J Multi-Channel Frequency
Response
DHVMT = 125 samples/sec.
O db = ± 10% F.S.
.05
1.0
2.0
5.0
10
20
30
FREQUENCY Hz

FIGURE 99

FIGURES 100 and 101 are the 80 samples/sec. and 125 samples/sec. for hardover failure in Channel 1. This data shows that the failures are detected the same as in the base line data in FIGURE 96.

The 680J simulation did not indicate any failures or increase in $\triangle P_1$ or $\triangle P_2$ when a sine wave input at $\pm$ 5.0 volts was swept through the bandpass of the test set-up.

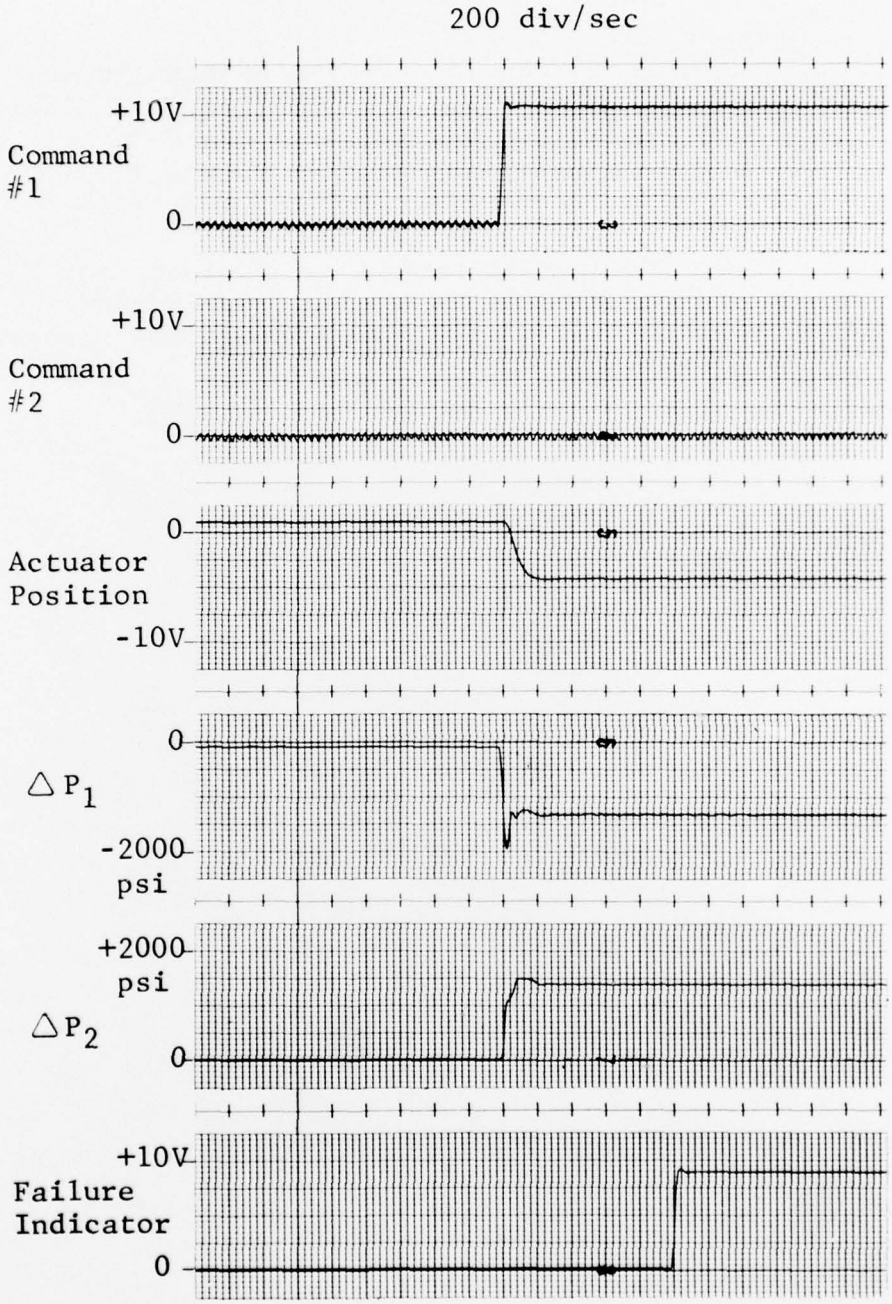


FIGURE 100 △P Failure Detection, 80 samples/sec.

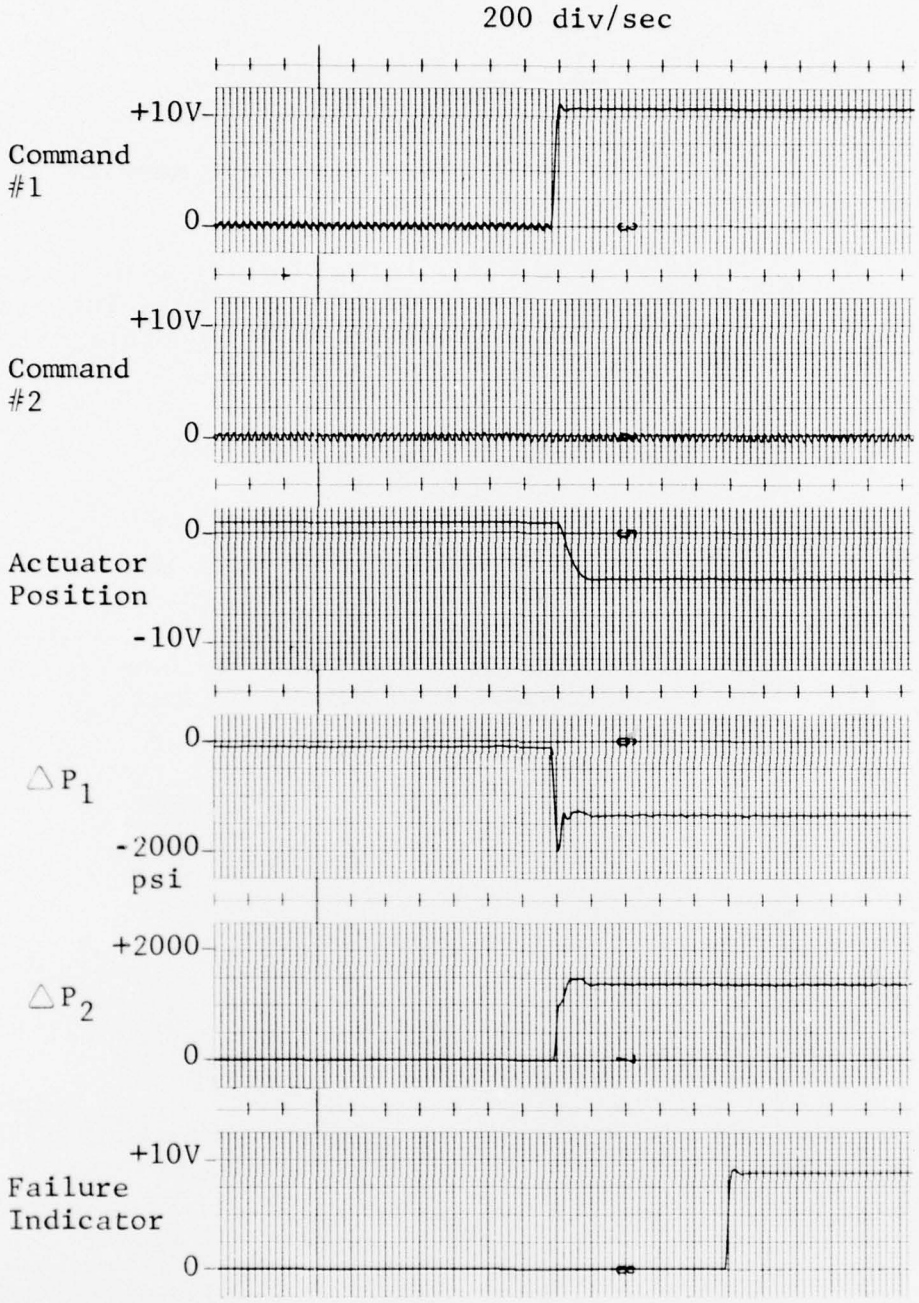


FIGURE 101 △P Failure Detection, 125 samples/sec.

4.4.3 Phase IV Test Results Summary

4.4.3.1 Multi-Channel Base Line Test Results

A two channel, 680J, force sharing with P failure monitoring was simulated on the HFCS. The simulation was tested and determined to be accurate by comparing the data to Reference 1 and 2.

4.4.3.2 Multi-Channel DHVM Data

A DHVM was inserted in series with the command input of each of the two simulated 680J channels. The data recorded with the two DHVM's operating asynchronously was an exact comparison with the baseline data. The DHVMs did not cause inadvertent failures in the simulation.

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

It is concluded that the DHVM operated essentially as intended by design. The 680J configured electro-hydraulic control system exhibited some frequency response degradation when the system was driven with the DHVM. This degradation was caused by the rate at which the analog input was being sampled. Performance degradation of the A-7D aircraft response was not noticeable at the sample rates used for testing.

From the tests, it is concluded that analog electro-hydraulic servo systems should be driven with a pulse width modulation frequency high enough to prevent large amplitude response of the servo valve's first stage. A pulse width signal demodulator may be used to roll off the amplitude of the modulation frequency with some potential of degrading the system response. A desirable maximum amplitude for the modulation frequency driving the servo valves would be 5% of full scale. (Ref. Section 4.2)

The DHVM will fail all four channels when a single channel is at the negative failure tolerance and the remaining three channels are matched within 5.0 millivolts. The problem is located in the circuit design. One solution to the problem would be prevention of the input synchronous counter's output transition from being presented to the failure logic simultaneously. (Ref. Section 4.1.3.2)

Asynchronous operation causes the failure detection to be frequency dependent. Using a digital filter

to reduce the failure detection sensitivity with increasing input frequency would eliminate this problem with asynchronous operation. (Ref. Section 4.1.3.2)

The output of the DHVM goes to negative full scale value when the momentary re-set switch is held in the re-set position. This occurs because the PWM signal stops and the TTL Lo value is at the output. One solution to this problem would be to use the re-set switch to trigger a single shot multivibrator, allowing a hardover output for a single clock cycle when the DHVM is re-set. (Ref. Section 4.2.4.2)

SECTION IV

APPLICATION GUIDE LINE

1.0 General

The DHVM is designed to monitor up to four digital inputs and select one for an input to flight control system hardware. In applying this device to a flight control system, the guidelines in the following sections should be considered.

1.1 Signal Level and Polarity

The PWM output signal must be compatible to the input of the control system being considered. Since output of the DHVM is TTL and the input for most control systems requires a bipolar signal, an off-set and scaling interface will be required.

1.2 DHVM Update Rate

The DHVM update rate should be set at the highest rate at which the available ditital hardware operates reliably. The control system to be interfaced should be reviewed to insure that the PWM frequency will not have undesirable effects on the electro-hydraulic hardware. One area to consider is the servo valve. To prevent damage to the first stage, the valve's amplitude response should be at least -26db relative to full scale input at the modulation frequency. The modulation frequency should not be at a mechanical resonance frequency (or one of its harmonics) of the electro-hydraulic

hardware.

1.3 Signal Resolution

The signal resolution is dependent upon the number of bits that is used for the data portion of the digital word. The word length should be selected on the basis of availble digital hardware and required system resolution, allowing for one to two bits of inherent digital noise.

1.4 Failure Tolerance

The failure tolerance level selection is based upon the allowable deviation that is acceptable to the aircraft to which the system is applied.

1.5 Time Delay Before Channel Exclusion

The time delay should be selected on the basis of the time that the aircraft can accept a hardover input to the control channel of the control axis of interest. This transient will normally effect the control channel on the third failure, since positive hardovers are selected as the output signal. The first two channel discrepancies are detected before a transient could be output from the DHVM.

1.6 Input Signal Sample Rate

The input analog signal should be sampled at a minimum of eight times the highest frequency of inter-

est. When the input frequency is at 1/2, 1/3 and 1/4 of the sample frequency a significant amplitude modulation of the control system output will be present (when the input sampling is synchronous). The amplitude modulation that occurs with input frequencies at 1/2 of the sample frequency is 100% and at a much lower frequency than the input. The modulation frequency is dependent upon the rate that the input frequency moves in and out of phase with the sample frequency.

Another consideration that should be given to the sample frequency is the time delay incurred when the information is processed through the digital portion of the system. This time delay converts directly to a specific phase shift at each specific input frequency. This can induce control system stability problems when used with aircraft motion closed loop systems.

1.7 Special Considerations

Two areas require special consideration unless they are designed out of the DHVM. One area is the sensitivity of the failure detection to frequency when operating with asynchronous inputs. The other area is that if three channels are closely matched and the fourth is at the negative error tolerance, all channels will be excluded.

The frequency sensitivity problem can be helped by increasing the allowable errors before a channel failure is acknowledged. This will compromise the original time delay considerations although the flight computer could set the time delay and/or error counter to a different value as channel exclusions are annunciated. This technique will not prevent the unit from failing with continuous sine wave inputs.

The four channel failure problem can be accomodated by insuring that the four inputs to the DHVM were separated in magnitude by a voltage equivalent to the last three digital bits of an input word.

REFERENCES

1. Mrazek, Jerry G., Ph.D., "Digital Hardware Voter/Monitor Breadboard Development and Evaluation", Final Report, AFFDL-TR-74-94, July 1974

2. Millman, Jacob, Ph.D. and Taub, Herbert, Ph.D., "Pulse and Digital Circuits", McGraw Hill Book Company, Inc., New York 1956

3. Hooker, David S., et.al., "Survivable Flight Control System", Final Report, AFFDL-TR-73-105, December 1973

4. Amies, Gerald E., et.al., "Survivable Flight Control System", Interim Report No.1, Studies, Analyses and Approach, AFFDL-TR-71-20, Supplement 3, May 1971

5. "Flight Test Evaluation of a Digital Flight Control System for the A-7D Simulation Test Plan", Honeywell, Inc., Government and Aeronautical Products Div., Contract Item A-005 of Contract AF-33615-73-C-3068, 15 February 1974

☆U.S.Government Printing Office: 1977 — 757-001/24