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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR TFT ADDRES--ETC(U)
MAY 77 D H DAVIES, W L ROGERS, H Y WEY DAAB07-76-C-0027
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Third Quarterly Report on Manufacturing Methods and Technology Engineering for TFT Addressed Display

for period

November 7, 1976 to February 7, 1977

D. H. Davies, W. L. Rogers, H. Y. Wey
and M. Green

placed by

Procurement and Production Directorate
US Army Electronic Command
Fort Monmouth, NJ 07703

with

Westinghouse Industrial & Government Tube Division
Westinghouse Circle
Horseheads, New York 14845

May 10, 1977

ACKNOWLEDGEMENT STATEMENT

This project has been accomplished as part of the US Army's Manufacturing and Technology Evaluation for Thin Film Transistor Display Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

Westinghouse R&D Center
1310 Beulah Road
Pittsburgh, Pennsylvania 15235

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The automatic pilot manufacturing unit is operating at overall satisfactory levels and producing displays to the required formats etc. The quality level of these displays is as yet not sufficient to pass the required legibility specifications but good progress has been made at identifying the key problem

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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR TFT ADDRESSED DISPLAY

THIRD QUARTERLY REPORT

November 7, 1976 to February 7, 1977

CONTRACT DAAB07-76-C-0027

Prepared by D. H. Davies, W. L. Rogers,
H. Y. Wey and M. Green

May 10, 1977

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ABSTRACT

This is the Third Quarterly Report on Contract DAAB07-76-C-0027; manufacturing methods and technology evaluation for the fabrication of thin film transistor based solid state display.

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1. PURPOSE

The overall objective of this program is to develop mass production methods and techniques for thin film transistor display technology. This novel technology is most amenable to computer control and the methods in development are based on an existing,Westinghouse developed, computer controlled thin film pilot line. Versions of the display in development have been made, with considerable success, in laboratory style equipment and this work continues under direct corporate support. The program includes the development of methods, procedures and optimal recipes followed by the rigorous examination of the displays for performance and life.

2. GLOSSARY

Dedicated Masks - A set of metal aperature masks (usually 12) each with a segment of the overall thin film pattern. One mask is equivalent to one evaporation step.

X'Y Masks - A pair of contacting masks that are moved over each other to generate a complete set of thin film patterns. The one mask pair is used for all of the evaporation steps.

Packaging Process - This term is used to summarize all the steps that are needed to take the complete thin film transistor circuit through to a complete display. It includes laminar photoresist (RISTON(R)), phosphor spray and seal of the top plate.

RISTON(R) - This is a Dupont trade-name for their laminar (sheet) photoresist. We use the term to cover the process of applying the material through a laminator, exposing and developing the pattern of phosphor aperatures.

APPLICON(R) - This is a trade-name (Applicon Co.) that is used to summarize the computer aided design (CAD) system. This interactive design tool is used for pattern layout and to generate magnetic tape to control the MANN photorepeater.

MANN(R) Photorepeater - A commercial unit that generates exposed, patterned, photographic plates of ultra high

quality. These plates are used to generate the metal masks.

Anneal - A long, high temperature bake, given to the thin film circuits as part of their fabrication process.

3. RESULTS AND DISCUSSION

3.1 Introduction

The bulk of the effort in this period has been concerned with Task V, recipe development for the TF circuit; the achieving of a fixed recipe that then allows us to test yield and throughput assumptions. This is the major goal of the program. As will be evident from the discussion below, a major constraint on progress was found to be the lack of throughput needed for adequate process and recipe development. After a revised critical path and process analysis it was decided to maximize effort on the pilot line and hence to discontinue direct effort at display fabrication on the laboratory 6-station dedicated mask unit. Hence fabrication of engineering samples (Task II) is now added to the obligations of the pilot operation. It should be noted however that, under Westinghouse corporate and divisional support, we continue to fabricate displays that meet the dimensions, formats and performance attributes required in this program. These displays, made with an X-Y laboratory technique, could serve as engineering samples, if so requested by the Army.

The effort having been centered on Task V this report is mostly concerned with progress on that Task. Other tasks reported on include Task VI recipe development for the packaging process and Task VII final test method development.

3.2. Task V - Recipe Development - TF Circuit

This section details the specific problems met with, and in most instances solved during the reporting period.

3.2.1. Limited Throughput and Turn Around Time

It became clear that we had to improve upon "turn around" time in the process. This is the time taken for the vacuum deposition system to be recharged, cleaned and closed again between runs. Given a

2 (operating 8 hr) days for actual circuit fabrication [4 complete half display circuits] as a fixed time for the near term present it was decided that a sequence cycle as follows was desirable:

Run - 2 days [four complete half circuits]

Down for recharge - 1 day

Run - 2 days

Down for recharge - 2 days (includes non-routine changes if needed)

Run - 2 days

etc. etc.

At the start of this period a typical cycle was Run-2 days, down-3 days, etc. etc. To achieve this improvement the entire down time process was evaluated.

Chart I shows the individual tasks involved in the "down time" with the observed typical times to perform those tasks. Tasks marked with an asterisk were identified as on the critical path (CP). It was discovered that many tasks not on the critical path were being performed while CP tasks were not yet done. This, of course, resulted from the lack of sufficient help.

Additional help was provided (from discontinuing the lab dedicated mask unit and through additional Westinghouse financial sources) and the program restructured as shown in Fig (1), the task numbers relate to Chart I. In this new operation the critical path is now fully attended with optimal assistance at all times. All the non-CP tasks are done by other personnel "off-line". The sequence is such that by the time the vacuum chamber is completely cleaned and its evaporation sources recharged then a new set of masks, cleaned glass substrates and cleaned shields and baffles are ready.

The overall task assignments in broad outline are shown in Chart II.

The new process sequence was implemented and, after a few "teething" problems has now slipped into operational gear. Fig (2) shows the improvement in throughput since the change. The average downtime for clean and recharge is now only ~6-7 hrs.

Chart I

Task Summary - Circuit Fabrication

Six categories of task

I Line operation-circuit fabrication

II Line support tasks

III Circuit checking

IV Mask preparation

V Glass substrate preparation

Task No.	Description	Elapsed Time Hrs
I-	*Circuit fabrication-line operations*	(best estimate)
-1*	Open chamber	0.2
-2*	Remove wheels	0.3
-3	Remove masks and substrates	0.4
-4*	Remove shields	0.4
-5*	Scrape wells	1.0
-6*	Clean hearths	0.2
-7	Clean chamber	0.2
-8*	Replenish sources	0.8
-9*	Replace shields	1.0
-10	Replace crystals	0.4
-11*	Reinstall wheels	0.3
-12*	Reinstall masks and substrates	1.5
-13	Data log for upcoming run	1.0
-14	Test for go	0.6
-15*	Rough out system	0.2
-16*	Pump down and pre-melt	4.0
-17*	Operation of line-fabrication	16.0

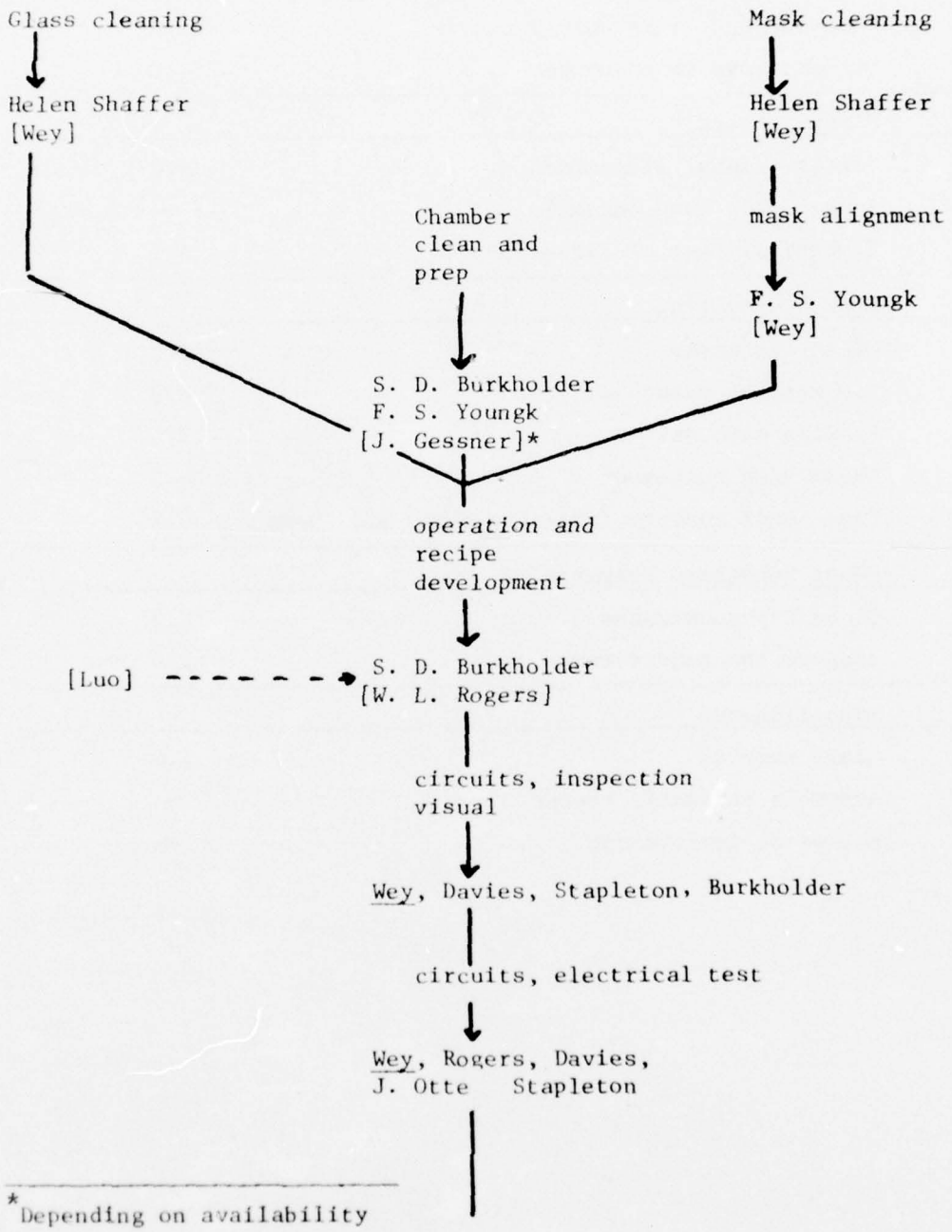
* indicates on critical path. Total critical path time 25.9 hrs

Chart I - (Continued)

II-	Line Support Activities	
-18	Material and line supply chores	2.6
-19	Preventative maintenance	4.0
III-	Circuit Check	
-20	Initial visual inspection	3.0
-21	Anneal prep (and anneal)	0.3 + (10.0)
-22	Electrical test of circuits	5-15
IV-	Mask Preparation	
-23	Clean the masks	5.0
-24	Inspect the masks	8.0
-25	Realign mask set	3.5
-26	Check mask alignment	0.5
-27	Final mask quality (cleaning check and clamp)	0.25
V-	Glass Substrate Preparation	
-28	Clean the substrates	5.0
-29	Inspect the substrates	2.0
VI-	Miscellaneous	
-30	Clean shields	4.0
-31	Assemble automatic tester	--
-32	Equipment improvement	--

Chart II

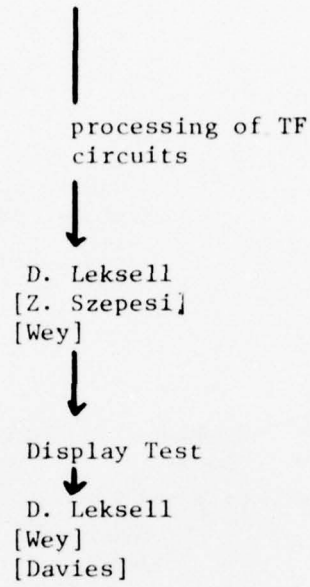
Overall assignments and tasks



*Depending on availability

OVER

Chart II - (Continued)



[John Doe]
This indicates
engineering
responsibility

In case of conflict the underlined name is
the key responsible person.

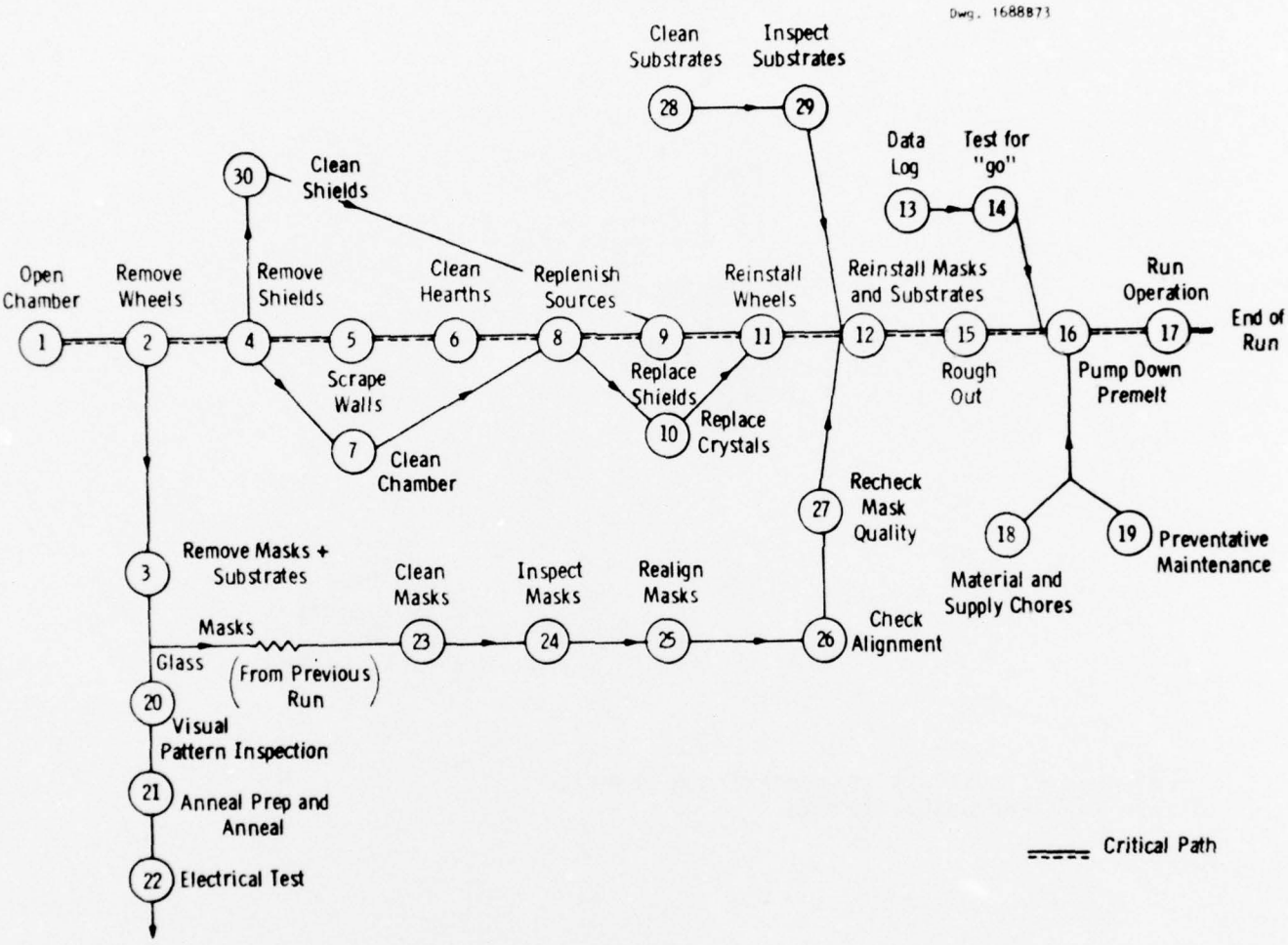


Fig (1) Circuit Fabrication and Test -
Critical Path Analysis

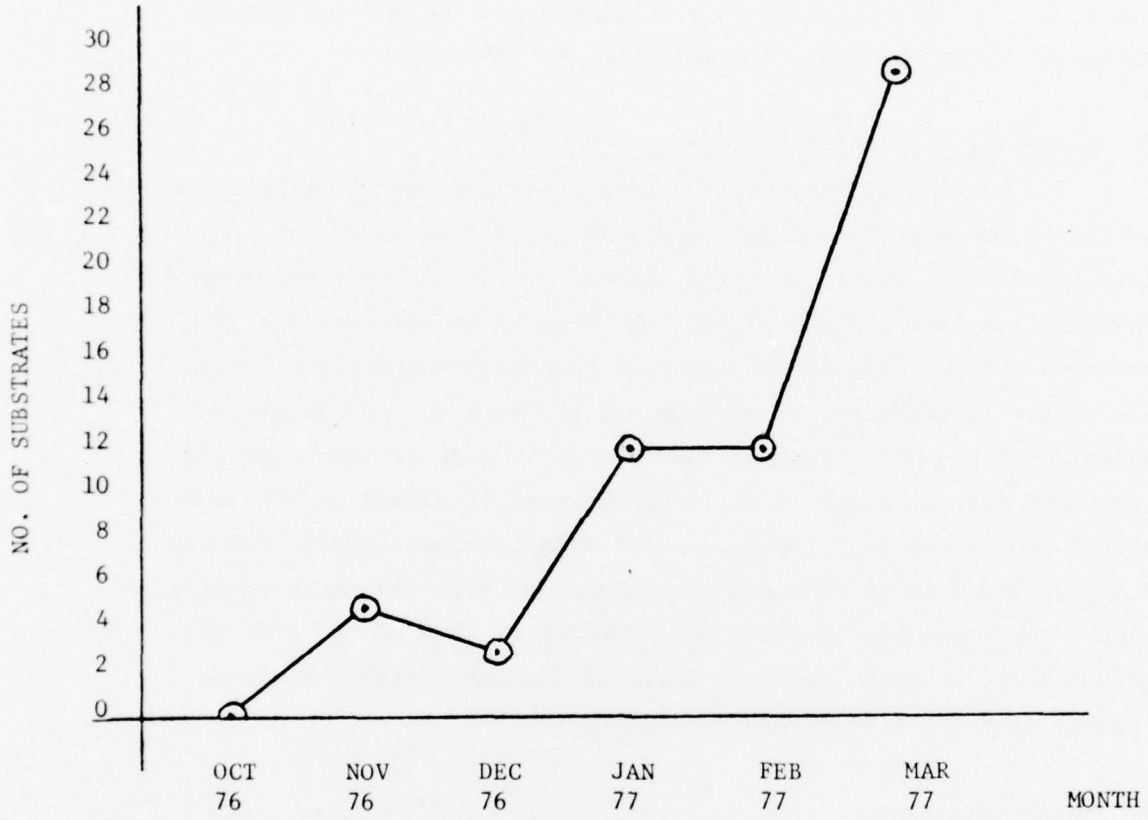


Fig (2) Improved Throughput Resulting from Altered Process

It should be emphasized that the achievement of improved throughput is not of itself of any value if what is being produced is not of good quality. The important point is that we have to go through a development cycle and unless we can have fairly quick turn-around to test ideas we will never have enough completed runs to make consistent conclusions. We now believe this condition is achieved.

3.2.2. Capacitor Misalignment

Examination of thin film patterns revealed that a marginal alignment condition prevailed in the double layer cell capacitor. As shown in Fig (3) in certain specific regions of the circuits the plates were overlapping (very slightly) over the edge of the dielectric. Two factors were thought responsible, lack of mask:mask pattern integrity in this particular mask set or movement of the mask during deposition or operation of the jig. Examination of mask to mask pattern registration revealed that although it could be improved it should be more than sufficient for non-shorted capacitors. A wide tolerance guard band was of course designed in to this pattern. Tests on jigs and masks revealed that the prime cause was inconsistent clamping tension of the mask to the mask holder. A more rigorous procedure was instituted and, as of this report date the problem has not reoccurred.

3.2.3. Metal Corrosion

One run of four substrates was annealed under the usual conditions and was found to have developed a metallic corrosion problem. After checking anneal oven temperature, location in the oven etc. the problem was clearly pinned down to the tank N_2 supply. A new supplier of nitrogen had been recently introduced (on a site basis) and an analysis of the nitrogen quality was performed. Table (1) shows the result of that analysis compared to the line (house) nitrogen that is usually used in lab operation. The house N_2 is not available to the pilot line; it was decided to anneal the substrate in the lab anneal systems from now on. This itself caused some minor problem since the

Table (1)

Analysis of N_2 Used in Anneal Process

Cylinder #1 - bad runs	0.13% O_2
Cylinder #2 - good runs	0.0077% O_2
House N_2 - used for most lab circuit anneal	0.0041% O_2

Analysis by GPC, O_2 is major impurity

Analysis #77-274.

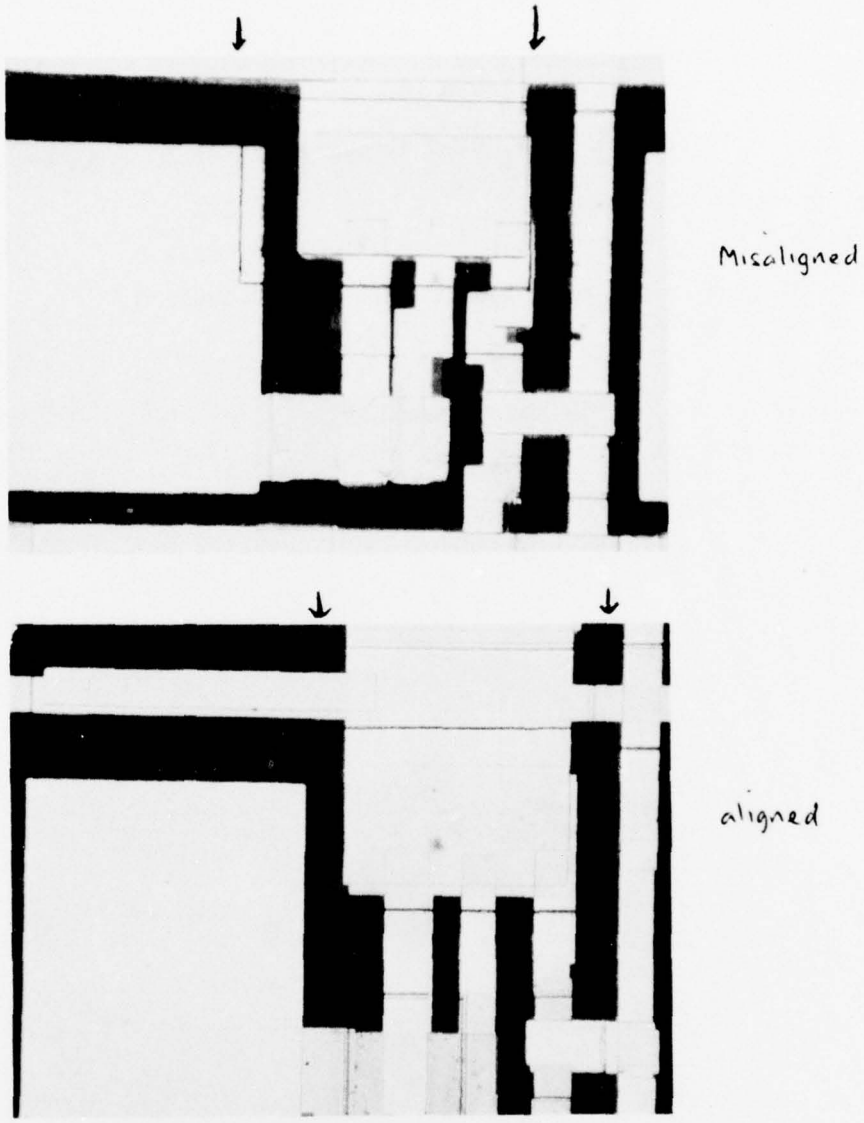


Fig (3) Marginal Alignment in
Elemental Capacitor

use of the four substrate stacking jig raised the substrates out of the good control zone of the oven. This caused some intermetallic corrosion. With better oven positioning this has now been solved.

Fig (4) shows typical "oxidation" corrosion and Fig (5) shows a typical example of intermetallic corrosion.

3.2.4. Aluminum Metal Spits

It is well established that many of the observed circuit shorts are caused by aluminum particles which "spit" onto the substrate during electron beam evaporation. Efforts to correlate this "spitting" with power surges originating in the deposition controller indicate that while these surges may cause part of the problem, they are not the major cause. Other facilities at the Research and Development Center where electron beam evaporation of aluminum is performed do not appear to have this problem. Examination of evaporation procedures used in these other facilities shows one primary difference: the use of a vitreous carbon hearth liner. Hearth liners had been abandoned in the pilot facility due to difficulties experienced with indium evaporation from a hearth liner. The experience of these other individuals, however, indicated that these problems do not occur with aluminum. As a result, a vitreous carbon hearth liner has been installed in the aluminum hearth in the Pilot Facility. An initial dry run showed no color changes during aluminum evaporation, indicating that perhaps the process is more stable.

This procedure appears to work quite well, except that the hearth liner cracks during the run. Brittle cracking is a fairly dirty process, that is, many small pieces of loose carbon will occur in the area of the crack. It was postulated that aluminum carbide (Al_4C_3) could be formed during the cracking process, and that sputtering would then occur during evaporation. Inspection of aluminum films using a dark-field microscope indicates that small inclusions are present. One way to prevent cracking is to reduce the number of thermal cycles the crucible is subjected to. The operating software treats every deposition as a free-standing system, as if nothing had occurred before, or nothing

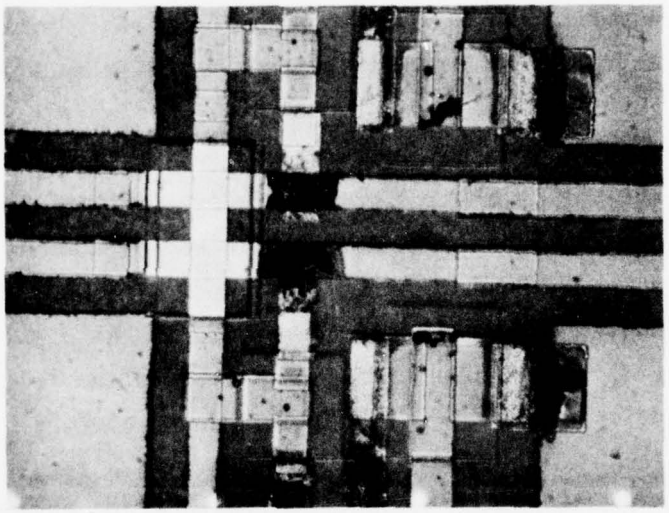


Fig (4) Oxidation Corrosion

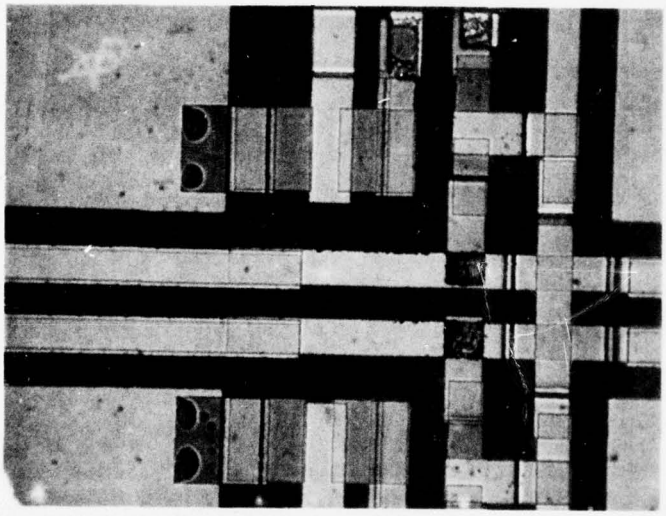


Fig (5) Intermetallic Corrosion

will occur after. Since most aluminum depositions occur in sets of three, if the hearth could be kept hot between depositions (as the wheels are moving), the number of thermal cycles could be significantly reduced. This change was implemented. (It should be noted that this problem would not apply to a larger production system with dedicated sources. The pilot facility system uses one, four-hearth gun for all metal evaporations. This means that the hearths have to be rotated to change metals, and only one hearth is addressed by the electron beam at one time).

To investigate the other potential source of spits, the erratic Sloan controller, a field engineer from Sloan Technology visited the Pilot Facility to witness the behavior of the deposition controller. Another unit that he had brought with him was connected to the system and exhibited similar problems. He was convinced the unit has a design problem, and, as proof, he sent recordings and notes to his engineering department for evaluation and possible solution. Sloan will also send us duplicate boards, a board extender and full schematics and we will examine the problem ourselves.

3.2.5. Aluminum Oxide Spits

Another well established cause of short circuits is spits in the aluminum oxide. Much progress has been made in this area but further improvement is needed. Fig (6) illustrates a dielectric badly contaminated with spits.

Early this period, the primary remaining cause of Al_2O_3 "spitting" was tentatively identified: flakes of Al_2O_3 peel off surfaces above the electron-beam gun during evaporation, fall into the hot crucible, and re-evaporate explosively. This observation was reinforced when thermal shields within the electron-beam gun well were relocated so that all surfaces were clear of the area above the crucible. The only major remaining source of peeling was the mask wheel. Past efforts to prevent peeling by roughing the stainless steel surface by wire brushing or sanding only made the problem worse, indicating that this work was creating a smoother, rather than a rougher, surface. Sandblasting the

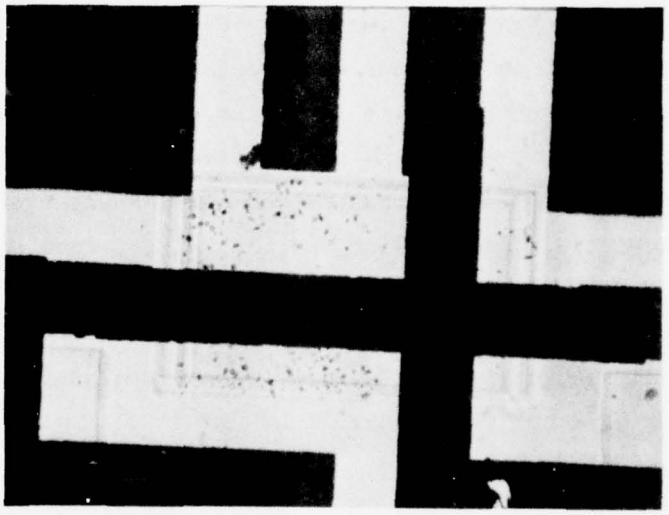


Fig (6) Typical Example of Bad Al_2O_3 Spitting

wheel was out of the question because of its size, delicate cam adjustments, and cracks and crevices which could not easily be cleaned. The solution was another molybdenum baffle, removable for sandblasting, located approximately 1/8" below the wheel, and covering all surface areas except the mask itself. Since the addition of this baffle, two runs (7 substrates) have been processed and inspected, and virtually all Al_2O_3 films have been found to have much reduced spec counts. Clearly, cleanliness of the gun wells is critical.

Another modification to improve gun well cleanliness was initiated. The original design specification for the vacuum system required that both electron-beam guns be movable, vertically. As a result, the water lines to the guns were long and flexible - corrugated stainless water lines, covered with stainless wire braid, snaked around the wells above the guns, acting as dirt collectors, impeding cleaning efforts, and preventing installation of the planned water-cooled baffle. These water lines were replaced with shorter, direct runs of smooth, rigid tubing. Unfortunately, moving the lines weakened a braised joint which caused a leak. By the time the leak was repaired (several times), and subsequent damage repaired (EB gun filament, ion gauge tube filament), eight production days had been lost.

3.2.6. Overall Clean Conditions

As has been evident for quite some time clean glass,chamber, and masks are a key problem. We believe that with the new operational procedure and the institution of new clean, multiple filtered, water we have achieved a high degree of consistent quality here. Examination of the substrates with high intensity light is now done as a routine test. The area requiring further input is in the overall handling of clean substrates, and masks, e.g. in moving from the clean assembly bench to the vacuum system or while sitting in the chamber prior to closing. A method to carry clean masks and glass was devised. It used a rack holder inside a vacuum container. Despite our high degree of confidence regarding this aspect we must be carefully not to lower standards as time goes on.

3.2.7. Device Electronic Characteristics

A major source of satisfaction in this reporting period is that good TFT consistency has been achieved. The leakage in the logic device (T_2) was almost always in the low na level ($-20V_G$) while the ON current is more than adequate. The power device (T_1) is typically able to stand-off $>250V_{SD}$ and also had more than adequate ON current. The specific data listed in Table (2) were achieved in the vast majority of substrates.

The only ambiguity lies in the d.c. gate stability of the devices. This problem is not so severe as to prevent operational devices but might have some potential instability effects on the power device. The symptom is that if a constant positive bias is applied to the gate, source-drain current which is initially very high, decreases with time. The opposite occurs with negative bias. A test procedure was devised which yields repeatable readings of stability, and a number of experiments attempted. The output of the test procedure is a figure of merit (F_M) which is a ratio of initial source-drain current to source-drain current after 10 seconds, with constant, positive gate bias. A negative bias is applied to the device before the test. This amplifies the symptom, making it easier to measure and therefore more repeatable. With this type of measurement, a "perfect" figure of merit would be 1 (no drift).

The first experiment involved re-annealing, since it is generally thought that higher annealing temperatures yield more stable transistors. While this experiment has not yet been completed, initial indications are that re-annealing at higher temperatures has little effect on this type of stability, and what effect it has is negative. Two substrates with initial figures of merit of 14.8 and 14.4 now have figures of 15.5 and 21.6 respectively, having been re-annealed three times at higher temperatures.

The second experiment involved the gate insulator to semiconductor interface. Theory predicts that better film quality at this interface results in fewer "traps" and, hence, better stability. Two substrates were produced (in the same run as the two above) using a

Table (2)

Device Properties - Typical

T_2	logic TFT	I_{dsatt} V_{GS} = +20V	250μa
		I_{off} V_{GS} = -20V V_{SD} = +25V	1-3na
T_1	power TFT	I_{dsatt} V_{GS} = +20V	300μa
		I_{off} V_{GS} = -20V V_{SD} = +200V	~0.5μa
		V_B (V_{GS} = +6V)	$>250V_{SD}$

procedure where the last 200 Å of gate insulator below the semiconductor and the first 200 Å above it were deposited at 1 Å/sec. (vs. the standard 5 Å/sec). These substrates had figures of merit of 44 and 62 - clearly worse.

The third experiment showed considerably more promise. A small amount of metal dopant (3 Å) was introduced directly into the semiconductor. The "standard" procedure is to apply dopant under the source-drain, and the excess then diffuses into the semiconductor during annealing. Four substrates produced in that run had figures of merit of 14.2, 7.6, 24.5 and 23.7. The substrate at 7.6 was the experimental substrate. The next sequence of runs will include two "standard" substrates, for control, and two with 5 Å of dopant in the (semiconductor) gap, to determine if, indeed, direct doping does improve stability, and if the process is repeatable. For comparison, the substrate which was half-legible had a figure of merit of 42, but it was only legible at fast refresh rate (250 frames/sec).

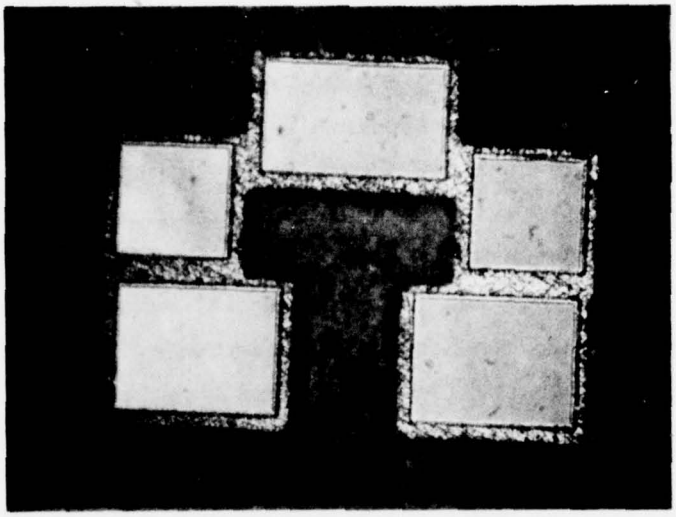
3.2.8. Mask Integrity

A troublesome but minor problem has been "lifting" off the nickel underside "bridge" in one of the dielectric masks. Fig (7) illustrates a good and bad "bridge." The lifting was found to be a problem associated with mask cleaning and was only significant with the thinner (3.7 mil) masks. The usual (5.5 mil) masks were not troublesome in this respect. We have now standardized on the thicker mask.

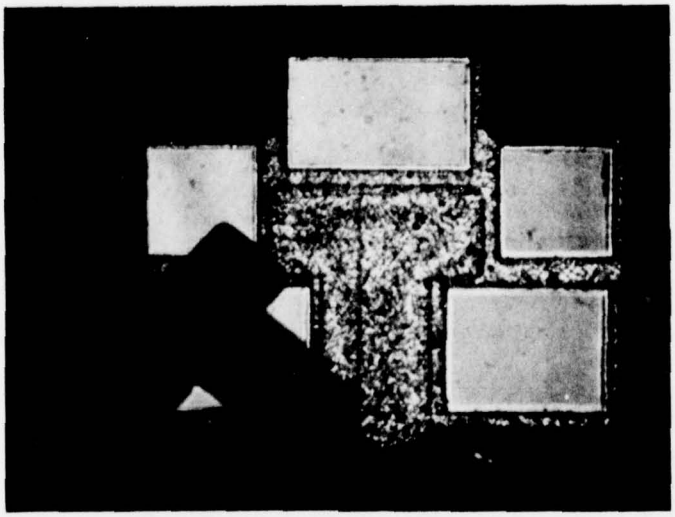
3.2.9. Summary of Results - TF Circuit Recipe Development

Over the last period the following problems appear to be consistently "solved", at least to the point where they will not inhibit the success of the program;

(a) Pattern definition
(b) Overall alignment
(c) Heat related mask buckling
(d) Throughput, although further improvements will be needed to meet the actual pilot run rates



GOOD



BAD

Fig (7) Mask Bridge Peeling

(e) Device operational characteristics, although some improved d.c. stability is desirable

(f) Glass cleaning

Several displays made in this period were processed and the best had ~75% of its characters legible. However the short stability was not good and on the initial "burn-in" more defects appeared. Detailed analysis of the shorts was done and they arise from small particulates not large enough to cause initial, as first tested, breakdowns but enough to induce breakdown in the first few hours of operation. This is not the case in the good X-Y displays which survive many hundreds of hours without further breakdown when stabilized.

We concluded that despite the first order improvement we still have a particulate/short problem. Microscopic examination of films, especially under "dark field" illumination conditions revealed the micro-particles in some quantities. Two approaches are being used to reduce this problem, one, the better control of the deposition through correction of the inherent fluctuations in the Sloan unit, and secondly modification of the dielectric gun surround to reduce "drop-in" of material collected on the hearth lip. Both approaches should lead to improved results in the next quarter. We believe this is the last obstacle to successful production of high quality, stable, displays in the computer controlled pilot line.

3.3. Results of X-Y Fabrication of Displays

As is well known to the Army we continue to fabricate displays in the exact format, cell layout, device recipe and overall dimensions required by this program using the laboratory X-Y method. This work while not formally part of the MM and TE program nevertheless is thought to be important as it bears heavily on the program. The effort is of course supported by Westinghouse with corporate funds but it is possible that the displays could be regarded as engineering samples in the above program.

Work continues with significant success in this area and displays with improved quality have resulted. See Fig (8). In addition we have fabricated the same display with a 2-level electrode, i.e. where the lit area is much increased over the elemental pad size. This improved legibility performance significantly, see Fig (9), although at some cost in power as detailed below.

3.4. Task VII - Final Test Procedures

We have begun, using displays made on the lab unit, the pilot line and the X-Y fabrication machines to examine the environmental performance tests. The shock test did reveal an unexpected problem; although the package remains intact the top gold sometimes breaks at the module crack location. Luckily the top gold is contacted separately on both modules so that provided we take care to use both module contacts there is no performance degradation.

Tests of phosphor brightness versus temperature have been conducted preparatory to the full display tests. The results, shown in Table (3) indicate that in the relevant parameters (brightness vs voltage, power efficiency) no significant temperature associated degradation occurs and that a few extra drive volts more than compensate for the slight change.

Further tests are continuing with full display testing to begin in during the next reporting period.

Temperature Test Procedure

The test panel was produced by our standard phosphor screening and packaging techniques. The panel was first measured at room temperature (1) then placed in a chamber containing solid carbon dioxide for approximately one and one-half hours. To prevent rapid temperature changes the panel was situated on a solid square plate of half-inch thick aluminum. Both the panel and plate were removed from the chamber to make the test measurements (2). A period of three hours passed before the second room temperature measurement (3) was performed to insure an equal temperature existed throughout the thickness of the

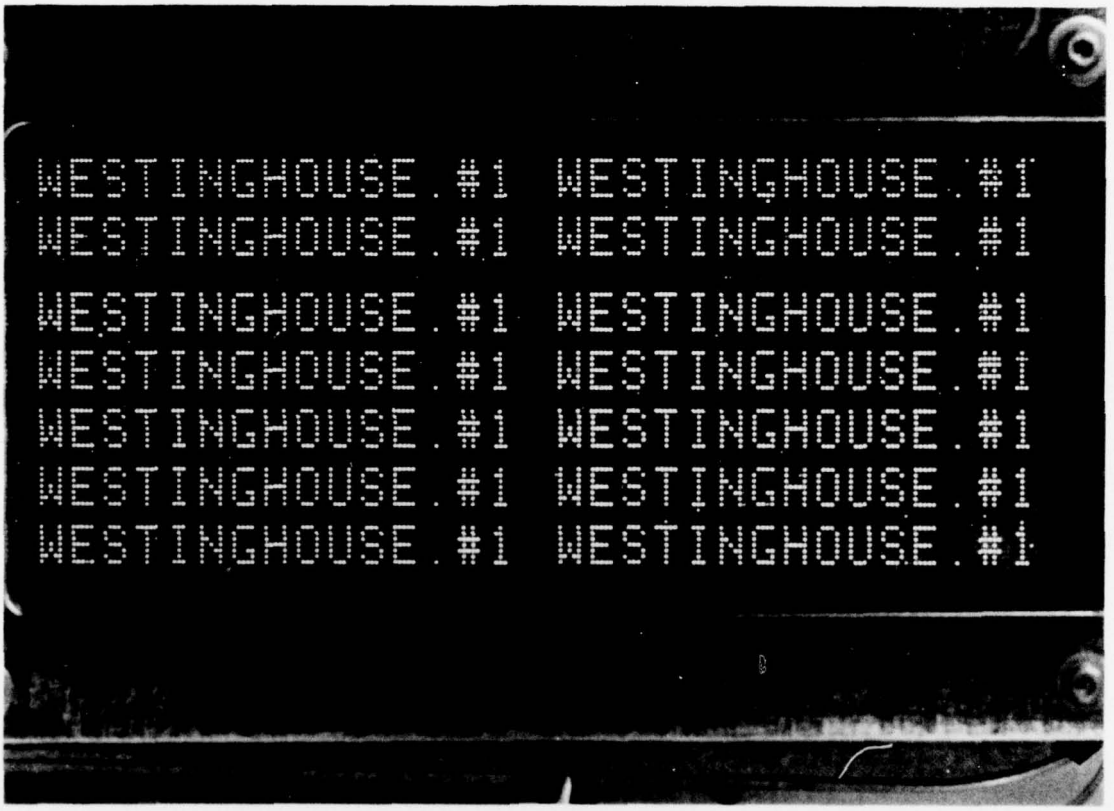


Fig (8) X-Y Fabricated DMD Display - Single Level

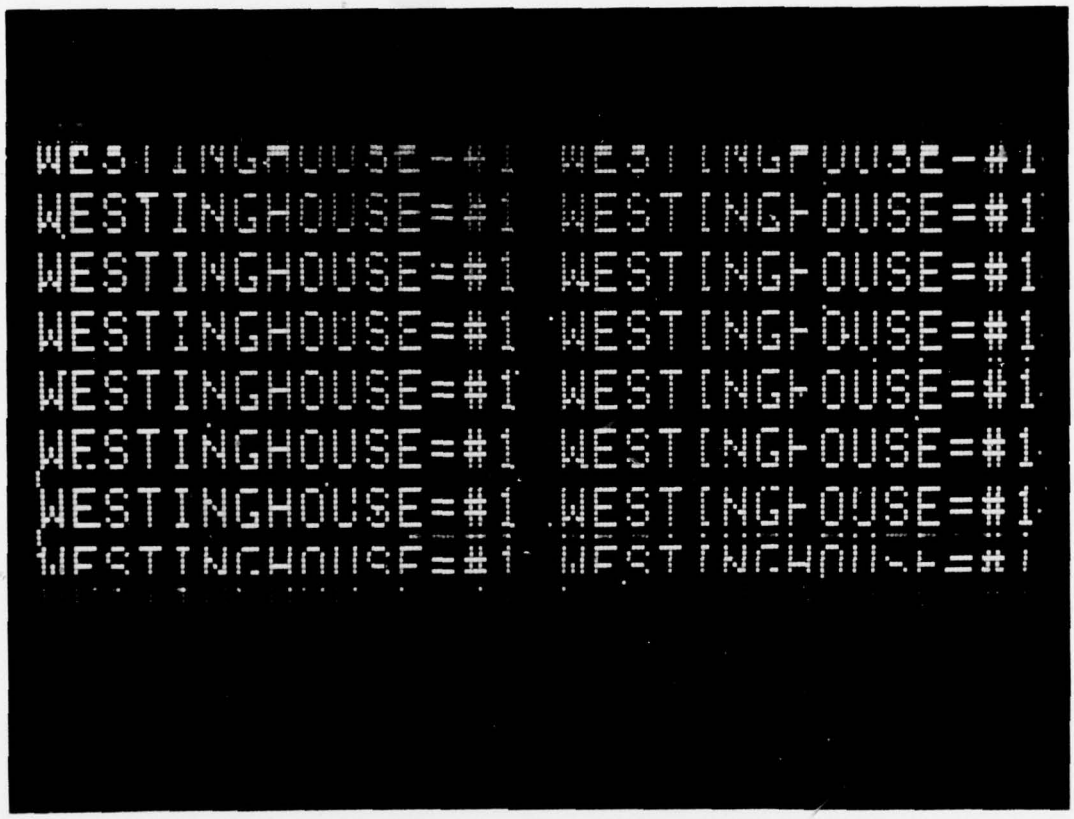


Fig (9) X-Y Fabricated 2-Level DMD Display

panel. The plate and panel were then placed into a furnace at 72° for two hours. Again both the panel and plate were removed to perform the measurements (4). After a two hour cooling period the final measurement (5) was made. The aluminum plate stabilized the temperature for a much longer time than was necessary to make the measurements. The temperature was measured by attaching an iron constantin thermocouple to the surface of the top cover plate at the panel and all measurements for a specific temperature were made simultaneously.

Equipment: Spectra Spotmeter Model B-1°
Fluke 8000A Digital Multimeter
Precision Thelco Model 16 Furnace
Electronic wattmeter described in a paper presented at Electrochemical Society Meeting in Las Vegas, October 21, 1976.

Table (3)

Panel No. 233.2	Temp*	Voltage 5 kHz RMS	Current mA	Brightness fl	Diss mW	Diss mW/cm^2	Eff lm/w
(1)	25°C	80	91.3	44	2221.1	65.7	.72
(2)	-52°C	100	65.0	44	2151.8	63.7	.74
(3)	25°C	80	87.5	45	2107.6	62.4	.78
(4)	72°C	77	114.3	45	2919.1	86.4	.56
(5)	25°C	80	93.0	43	2234.5	66.1	.70

Since several displays have been fabricated to the necessary format using the X-Y method we also decided to examine the validity relative to the power and legibility specifications. A single and double level display were utilized, the former has ∿30% lit area per cell and the latter ∿75% lit area per cell.

It was apparent from the observer tests conducted at normal room ambient that every character point in the panel (slightly less than 256 in the test due to edge losses) was correctly discernable. All the printable ASCII characters were correctly identified. At 2000 fc it was

*Actual, measured simultaneously to the measurement of other listed parameters.

found that a degree of enhancement was needed to obtain the same results. The best filter was a green louver(R) filter from the 3M Company. Utilizing this filter we repeated the tests above with similar acceptable results. The "double level" panel was better but both were legible. Note that the louver filter does restrict viewing angle somewhat although this is not so onerous as would be expected since it only restricts the angle in one plane. This plane can be chosen to be the least inconvenient to the observer.

The power dissipation in the panels was measured under conditions where the display was legible at 2000 fc (with filter). The results obtained were as follows:

Single level panel		Double level panel	
No. of characters*	Milliwatts total whole panel	No. of characters*	Milliwatts total whole panel
0	50	0	135
56	145	56	390
128	235	128	520
256	425	256	980

*8 character on the display.

Both single and double level panel are within the SCS 501 specifications.

3.5. Task VI Recipe Development - Packaging Process

One significant problem was encountered: this problem did cause the loss of some potential displays. A tendency was observed for the top gold/PbO electrode to electrically open at the joint where it attaches to the fingers. This is a troublesome problem since if it occurs after panel seal it is virtually unreclaimable. Since this particular problem was rarely encountered before a significant search was made to discover the cause. Analysis of the control "chips" that always proceed with the panel through each stage revealed that the PbO (the top

gold adhesion layer) was significantly thinner than specified.

The reason for this change was pinned down to a replacement of an evaporation boat in the resistance heated deposition of the PbO. A molybdenum boat had been replaced with Al_2O_3 coated tungsten. This was corrected and to date this problem has not reoccurred.

Since the "packaging process" actually consisting of laminar resist, phosphor spray, top electrode evaporation, only applies to TF circuits that pass the tests there have been no problems of throughput at this stage.

4.0 Conclusions

At this stage we can, with a high degree of reliability, state the following:

(a) We have proven we can fabricate the required TFT-patterns with good sharpness.

(b) We have solved the heat related mask buckling problems.

(c) We have achieved pattern registration and alignment sufficient to the needs of the display.

(d) Significant improvements in glass, mask and chamber cleanliness have been achieved.

(e) The rate of "throughput", i.e. the number of completed display circuits, has risen dramatically.

(f) Definite improvements in film quality have resulted from improved shielding in the deposition well.

(g) That we have achieved a good, reproducible, TFT device recipe.

(h) That the prime residual problem is microparticulate induced shorts primarily in the dielectric films.

(i) We have successfully made several displays in the required dimensions and formats using the X-Y method and that those displays meet all of the required performance specifications of SCS 501 that have been measured to date.

5.0 Program for Next Quarter

(1) Continue to improve dielectric film quality, and hence display quality. Through changes in the e-beam gun well and hearth arrangements.

(2) Continue to improve metal film quality through optimization of hearth liners, deposition parameters, anneal control, etc.

(3) Modify Sloan controller to stabilize output.

(4) As a result of above improvements fabricate good quality displays.

(5) Complete the set up of the gamut of environmental and performance tests and perform the tests on both X-Y and pilot displays.

(6) Complete the construction of the automated testing station.

(7) Deliver engineering samples to Army.

6.0 Publications and Reports

None

7.0 Identification of Personnel

Overall supervision - Dr. M. Green and Dr. D. H. Davies

Pilot operation - W. L. Rogers, R. E. Stapleton, R. G. Abraham, S. Burkholder, J. Gessner, Dr. H. Y. Wey, S. Youngk, H. Shaffer

Laboratory ES fabrication (X-Y) - Dr. F. C. Luo and D. W. Yanda

Packaging and performance test - Dr. Z. Szepesi and D. Leksell

New mask design and fabrication - L. Sienkiewicz and M. Cresswell

Circuit test - P. R. Malmberg and others listed above.

Consultant - Dr. T. P. Brody

During the three months reported here the following personnel were charged to the contract or worked directly on the project. The following hours were charged:

	hours - approximate
M. Green	120
*D. H. Davies	40
W. L. Rogers	360
*R. E. Stapleton	20
R. G. Abraham	20
S. D. Burkholder	340
J. Gessner	350
H. Y. Wey	360
*F. S. Youngk	280
*Z. P. Szepesi	40
T. Csakvary	90
H. Shaffer	40

	hours - approximate
*D. Leksell	24
*L. J. Sienkiewicz	--
*M. W. Cresswell	--
*P. R. Malmberg	--
*T. P. Brody	--
Shop/Services	115

Note F. C. Luo and D. Yanda (X-Y fabrication of displays) are not directly part of the MMT and E program.

As is well know to the Army, a large part of the effort on this program is funded directly by Westinghouse. Those persons marked (*) are largely charged to Westinghouse programs.

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