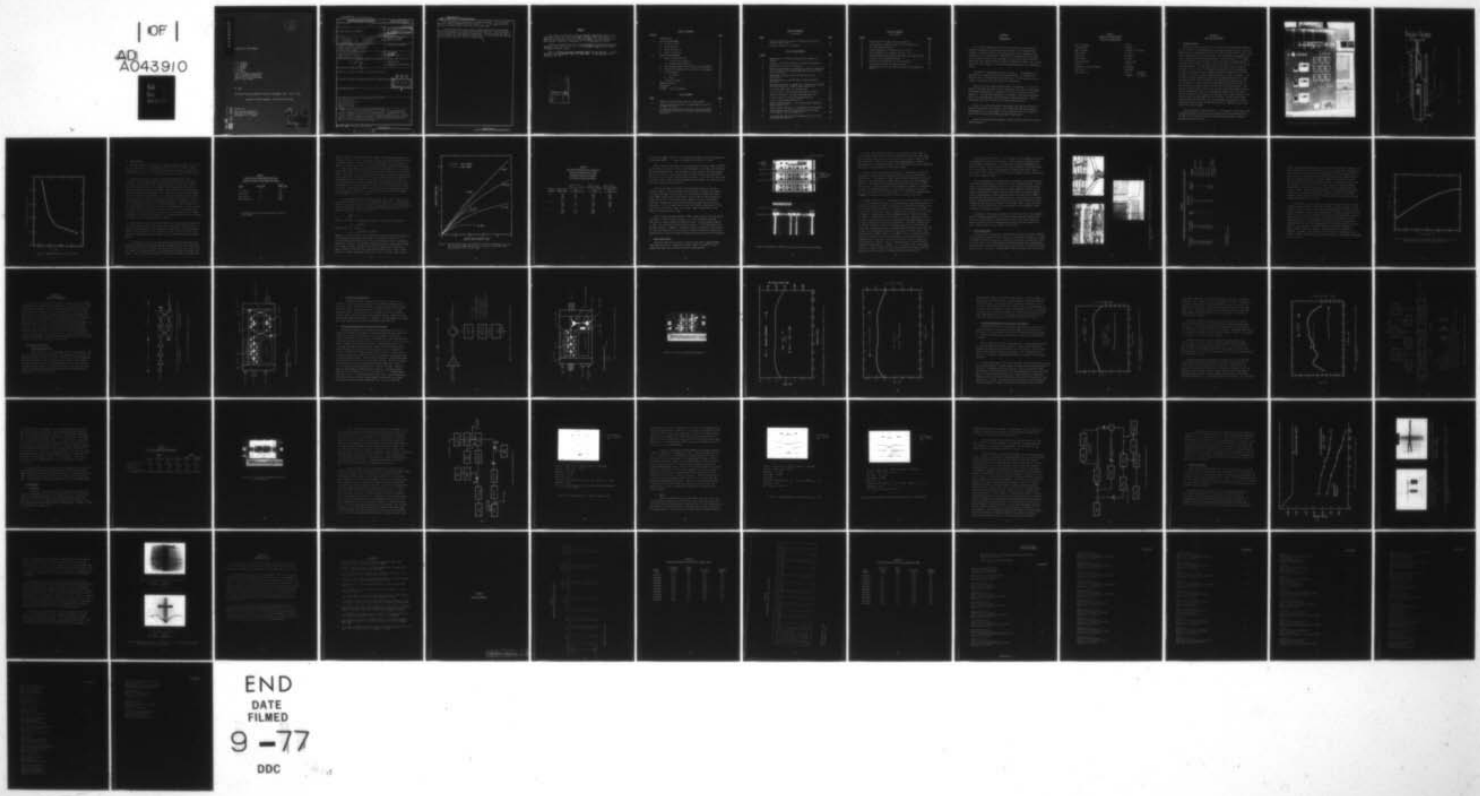
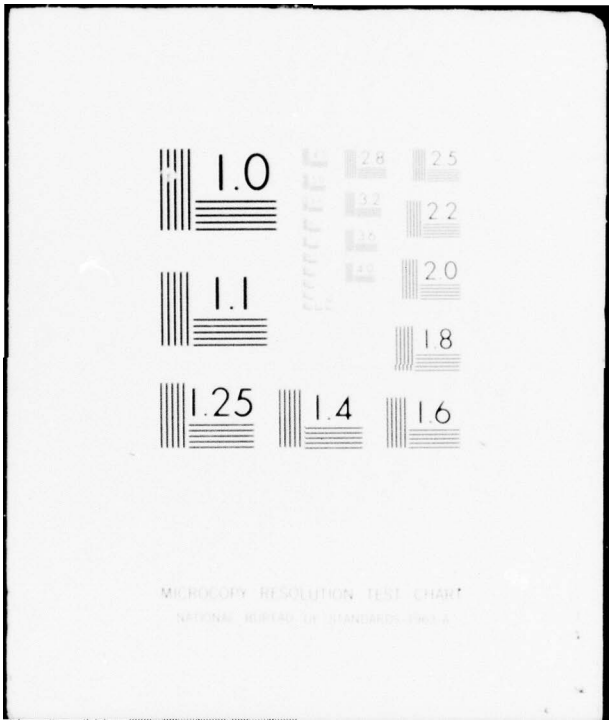
AD-A043 910 TEXAS INSTRUMENTS INC DALLAS CENTRAL RESEARCH LABS F/G 9/5
X-BAND SOLID STATE MODULE.(U)
MAY 77 W R WISSEMAN, F H DOERBECK N00173-76-C-0384
UNCLASSIFIED TI-08-77-22 NL



END
DATE FILMED
9-77
DDC


1.0
1.1
1.25
1.4
1.6
2.8
2.5
3.2
2.2
3.6
2.0
4.5
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

12
B S.

X-BAND SOLID STATE MODULE

W. R. Wisseman
F. H. Doerbeck
R. E. Lehmann
H. M. Macksey
V. Sokolov
H. Q. Tserng
Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75222

May 1977

Semiannual Technical Report for Period 30 September 1976 - 31 March 1977

Approved for Public Release - Distribution Unlimited

Prepared for

Naval Research Laboratory
4555 Overlook Avenue, S. W.
Washington, D. C. 20375

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

no. 1

4. TITLE (and Subtitle)

X-BAND SOLID STATE MODULE

5. TYPE OF REPORT & PERIOD COVERED

Semiannual Technical rept.
30 Sept 1976-31 March 1977

6. PERFORMING ORG. REPORT NUMBER

TI-08-77-22

7. AUTHOR(s)

W. R. Wisseman, H. M. Macksey
F. H. Doerbeck, V. Sokolov
R. E. Lehmann, H. Q. Tserng

8. CONTRACT OR GRANT NUMBER(s)

N00173-76-C-0384

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75222

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

11. CONTROLLING OFFICE NAME AND ADDRESS

Naval Research Laboratory
4555 Overlook Avenue, S. W.
Washington, D. C. 20375

12. REPORT DATE

May 1977

13. NUMBER OF PAGES

56

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

64p.

15. SECURITY CLASS. (of this report)

UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release - Distribution Unlimited

DDC
RECEIVED
SEP 8 1977
B

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Gallium Arsenide
Field Effect Transistor
GaAs FET Amplifier
Phased Array Radar

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This interim report covers the first six months of an eighteen-month program to develop an X-band solid state amplifier. The amplifier is the critical component of an all solid state transceiver module for use in active element, airborne, phased array radars. The performance goals are an output power of 5 W with 25 dB gain over the 9 to 10 GHz frequency band with an efficiency ≥ 20% under pulsed conditions.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

403833

LB

Two approaches are being pursued to meet these goals: an all GaAs FET amplifier and an FET/Read diode hybrid amplifier. At the completion of the program, two amplifiers of each type will be delivered.

The effort during this period was concentrated on GaAs FET development and the development of a three-stage FET driver amplifier. The driver amplifier will be used in both amplifier approaches. A three-stage driver amplifier breadboard has been completed that delivers 1.3 W with 19 dB gain and 20% efficiency over the 9 to 10 GHz frequency range.

PREFACE

This report was prepared by Texas Instruments Incorporated, Dallas, Texas under Navy Contract No. N00173-76-C-0384. The work under this contract is administered and funded by Naval Air Systems Command. Mr. Eliot Cohen of the Naval Research Laboratory, Washington, D. C., is the Scientific Officer.

At Texas Instruments the work is being performed in the Advanced Components Laboratory under the direction of Dr. W. R. Wisseman, Manager of the Advanced Microwave Components branch.

This is the first Semiannual Technical Report for the contract. It covers work done from 30 September 1976 to 31 March 1977. It was submitted by the authors in May 1977.

TABLE OF CONTENTS

SECTION		PAGE
I	INTRODUCTION.	1
II	GaAs FET DEVELOPMENT.	3
	A. Epitaxial Growth	3
	B. Device Design.	7
	C. Device Fabrication	12
	D. Device Performance	15
III	AMPLIFIER DEVELOPMENT	20
	A. Amplifier Configurations	20
	1. All-FET Power Amplifier	20
	2. FET/Read Hybrid Amplifier	23
	B. Four-Stage Breadboard Driver Amplifier Development . .	23
	C. Three-Stage Breadboard Driver Amplifier Development. .	29
	D. Rf Measurements.	34
	1. Pulse Data.	34
	2. Noise	40
	E. 3 dB Hybrid Coupler.	45
IV	SUMMARY AND PLANS	50
	REFERENCES.	51
	APPENDIX DEVICE DELIVERIES	53

LIST OF TABLES

TABLE		PAGE
1	X-Band Solid-State Module Amplifier Requirements.	2
2	Power and Gain Requirements for Each Stage of the Driver and Power Amplifiers.	8
3	Microwave Performance as a Function of Gate Finger Width for GaAs Power FETs Having 1 μm Gates and 1200 μm Total Gate Width.	11

TABLE OF CONTENTS

(continued)

TABLE		PAGE
4	10 GHz Microwave Performance of GaAs FETs with Several Different Gate Widths	17
5	FET Driver Amplifier Performance	35

LIST OF ILLUSTRATIONS

FIGURE		PAGE
1	Photograph of an Automatic GaAs Epitaxial Deposition System	4
2	Schematic of Epitaxial Reactor with Two $AsCl_3$ Bubblers	5
3	Doping Profile of an FET Structure	6
4	Maximum Output Power with 4 dB Gain at Several Frequencies for 1 μm and 2 μm Gate Length GaAs FETs as a Function of Total Gate Width	10
5	Photographs of 6400 μm Gate Width Devices During Fabrication	13
6	SEM Photographs of a Bonded 6400 μm Gate Width GaAs FET Chip	16
7	Maximum Output Power at 10 GHz with 4 dB Gain as a Function of Drain Voltage for a 3200 μm Gate Width Device	19
8	An All-FET Power Amplifier Configuration	21
9	Circuit Layout of the All-FET Power Amplifier Module	22
10	Schematic Diagram of the Hybrid FET/Read Amplifier	24
11	Circuit Layout of the Hybrid FET/Read Amplifier	25
12	A 0.5 W, Three-Stage FET Amplifier	26
13	Gain-Frequency Response of the Three-Stage FET Amplifier Shown in Figure 12	27
14	Gain-Frequency Response of a Breadboard Driver Amplifier	28
15	Gain-Frequency and Efficiency Characteristics of the First Stage of the Driver Amplifier	30
16	Gain-Frequency and Efficiency Characteristics of a Two-Stage GaAs FET Amplifier	32

TABLE OF CONTENTS

(continued)

FIGURE		PAGE
17	Block Diagram of a Power FET Driver Amplifier	33
18	A Three-Stage, Breadboard Power FET Driver Amplifier. . . .	36
19	FET Pulse Measuring Setup	38
20	Pulsed Response for a Two-Cell FET, V_D = 8 V.	39
21	Pulsed Response for a Two-Cell FET, V_D = 10 V	41
22	Pulsed Response Showing Amplitude Droop for a Two-Cell FET.	42
23	AM Additive Noise Measuring Setup	44
24	AM Additive Noise Results for Driver Amplifier.	46
25	3 dB Coupler, Design and Coupling Results	47
26	Measured Directivity and Return Loss for 3 dB Interdigital Coupler	49

SECTION I

INTRODUCTION

This interim report covers the first six months of an eighteen-month program to develop an X-band solid state amplifier. This eighteen-month program is the first phase of a four-phase program that is expected to be completed in a five-year period. The amplifier developed during this phase of the program is the critical component of an all solid state transceiver module for use in active element, airborne, phased array radars. The ultimate goal of the full program is a test bed systems demonstration of a 100-element array.

The amplifier requirements are given in Table 1. Two approaches are being pursued to meet the amplifier performance goals: an all GaAs FET amplifier and an FET/Read diode hybrid amplifier. At the completion of the program, two amplifiers of each type will be delivered.

Section II of this report describes GaAs FET development. To date, 20 GaAs FETs have been delivered to NRL in accord with the contract requirements. The microwave performance of these devices is given in Tables A1 and A3 of Appendix A. No Read diode development is required to meet the program goals, since this technology was already available at Texas Instruments. Twenty Read diodes have been delivered to NRL (see Tables A2 and A4).

Section III covers the amplifier development that has been carried out during this portion of the program. Most of the effort has been devoted to the development of a three-stage FET driver amplifier that will be used in both the all FET and the FET/Read diode hybrid amplifiers.

Section IV summarizes the progress to date and details plans for the next reporting period.

Table 1

X-Band Solid-State Module

Amplifier Requirements

Center Frequency	9.5 GHz
1 dB Bandwidth	± 500 MHz
Peak rf Output	5 W Goal, 4 W Minimum
Pulse Width	2 - 20 μs
Duty Cycle	Up to 50%
Overall Gain	≥ 25 dB
Final Stage Gain	5 dB Minimum
Risetime	< 50 ns
Harmonic and Spurious Output	50 dB Down
Efficiency	Maximized
Spectral Purity	at 10 Hz -48 dB/Hz
	> 1000 Hz -105 dB/Hz

SECTION II
GaAs FET DEVELOPMENT

A. Epitaxial Growth

GaAs FETs at Texas Instruments are fabricated using vapor phase grown epitaxial structures. Semiautomated reactor systems are used routinely to provide GaAs material for GaAs FETs, as well as for other microwave devices, such as Gunn diodes, Read diodes, and varactor diodes. The systems employ the Ga-$AsCl_3$-H_2 system, which has been discussed extensively in the literature.[1,2,3] Figure 1 is a photograph of such a system. All FET structures at present contain a high resistivity buffer layer between the active layer ($N \sim 10^{17}$ cm^{-3}) and the Cr-doped substrate. The low doping level of the buffer layers, which are typically 3 to 5 μm thick, is achieved by growing in a HCl-rich atmosphere. An additional amount of $AsCl_3$ is added to the gas flow downstream from the Ga source. A schematic of this two-bubbler system is shown in Figure 2. The principle of such a two-bubbler system has been described previously in the literature,[4] along with the reasons for the observed low doping levels.[5,6] All FET material is grown thicker than required for device fabrication and then thinned by successive anodic oxidation and oxide etching cycles. This process is self-limiting in such a way that the oxide growth stops as soon as the surface depletion layer, with bias applied, reaches the buffer layer. Then the structure is not biased any more beyond the avalanche condition, and holes required for oxide growth are not available. Before submitting the material to device fabrication, the layer thickness is measured on cleaved and etched cross sections, and the doping profile is measured using C-V data taken with a mercury probe.

Figure 3 presents a typical profile. It is important to note that series resistance effects of FET structures introduce errors into doping profiles and that the real profile always lies below the measured data in regions approaching the buffer layer.

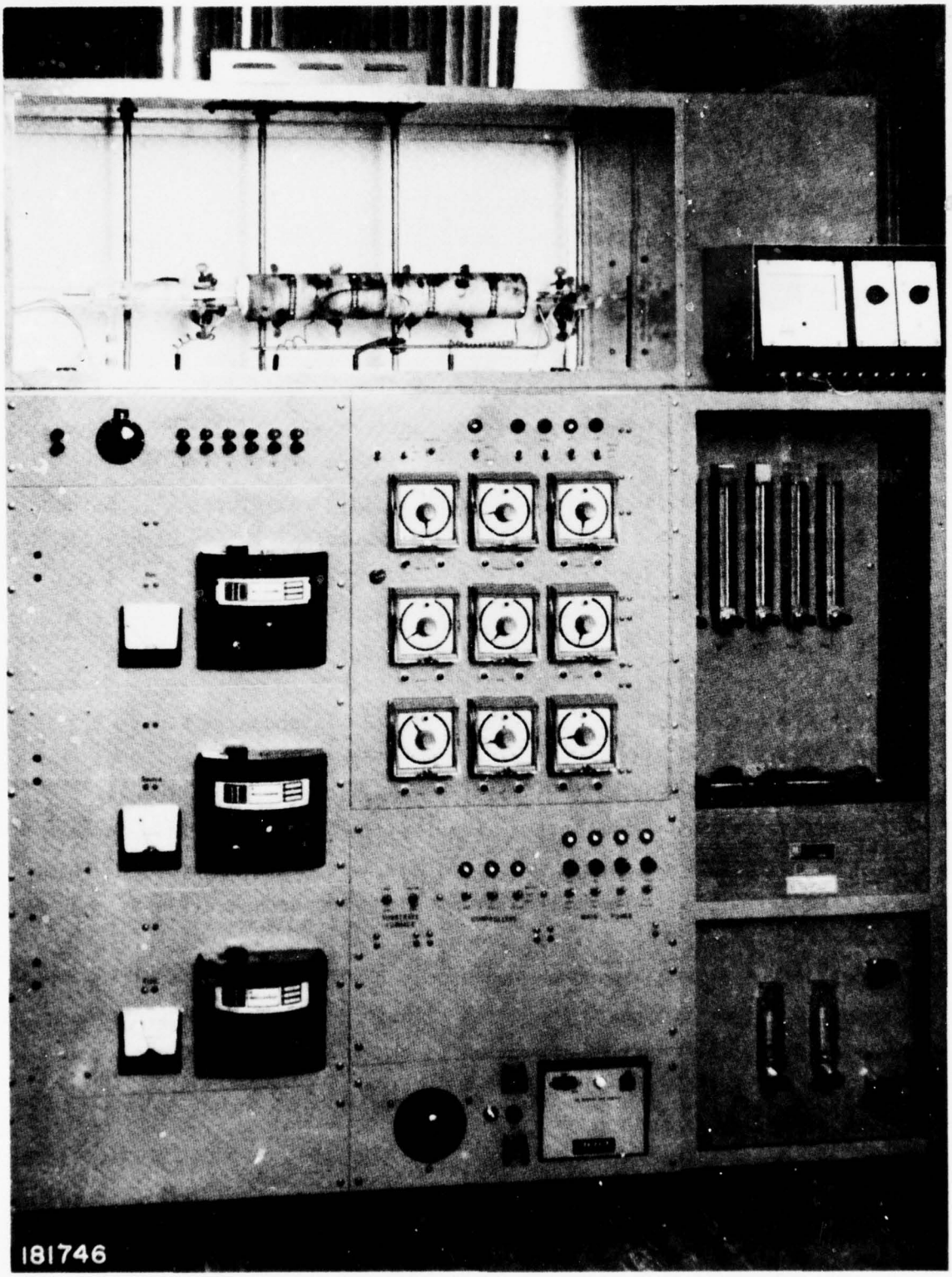


Figure 1 Photograph of an Automatic GaAs Epitaxial Deposition System

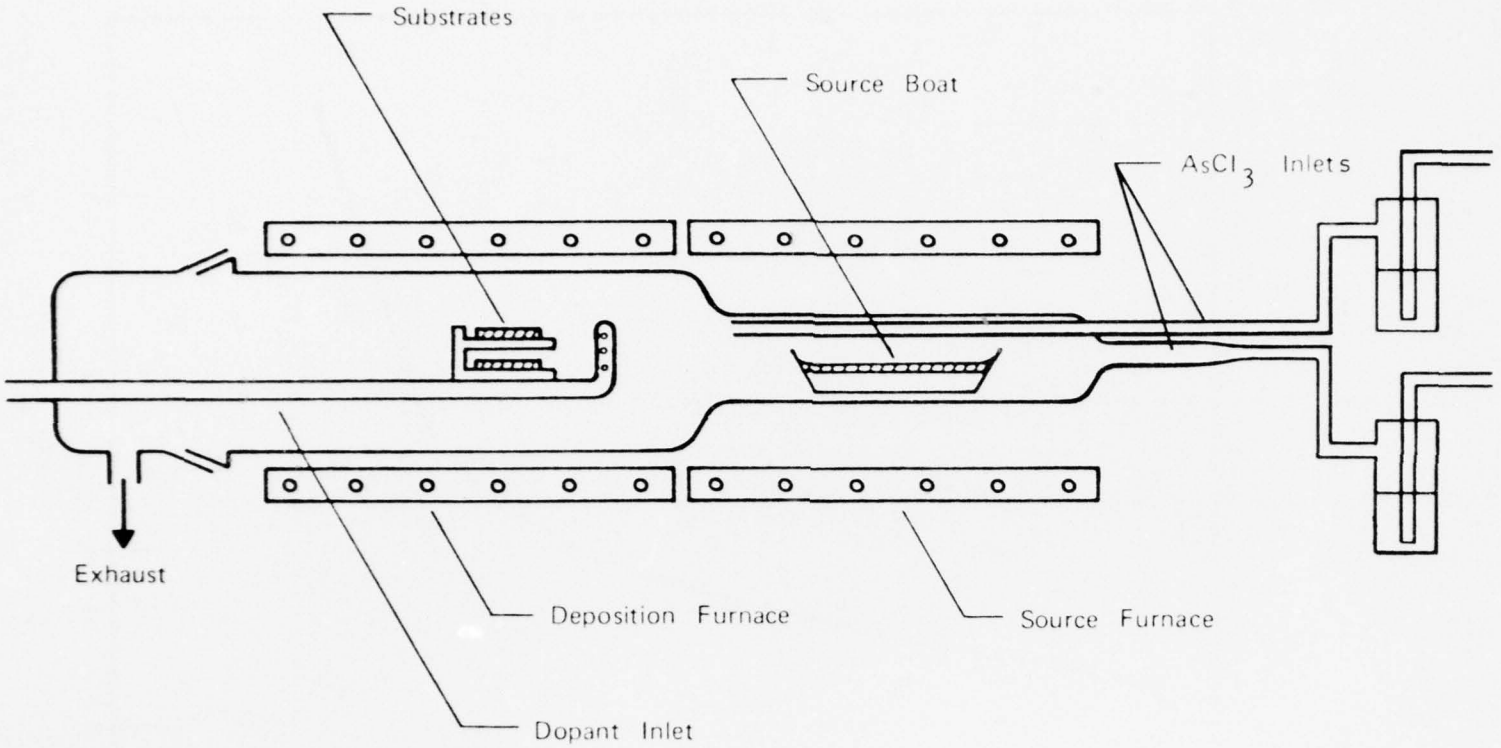


Figure 2 Schematic of Epitaxial Reactor with Two $AsCl_3$ Bubblers

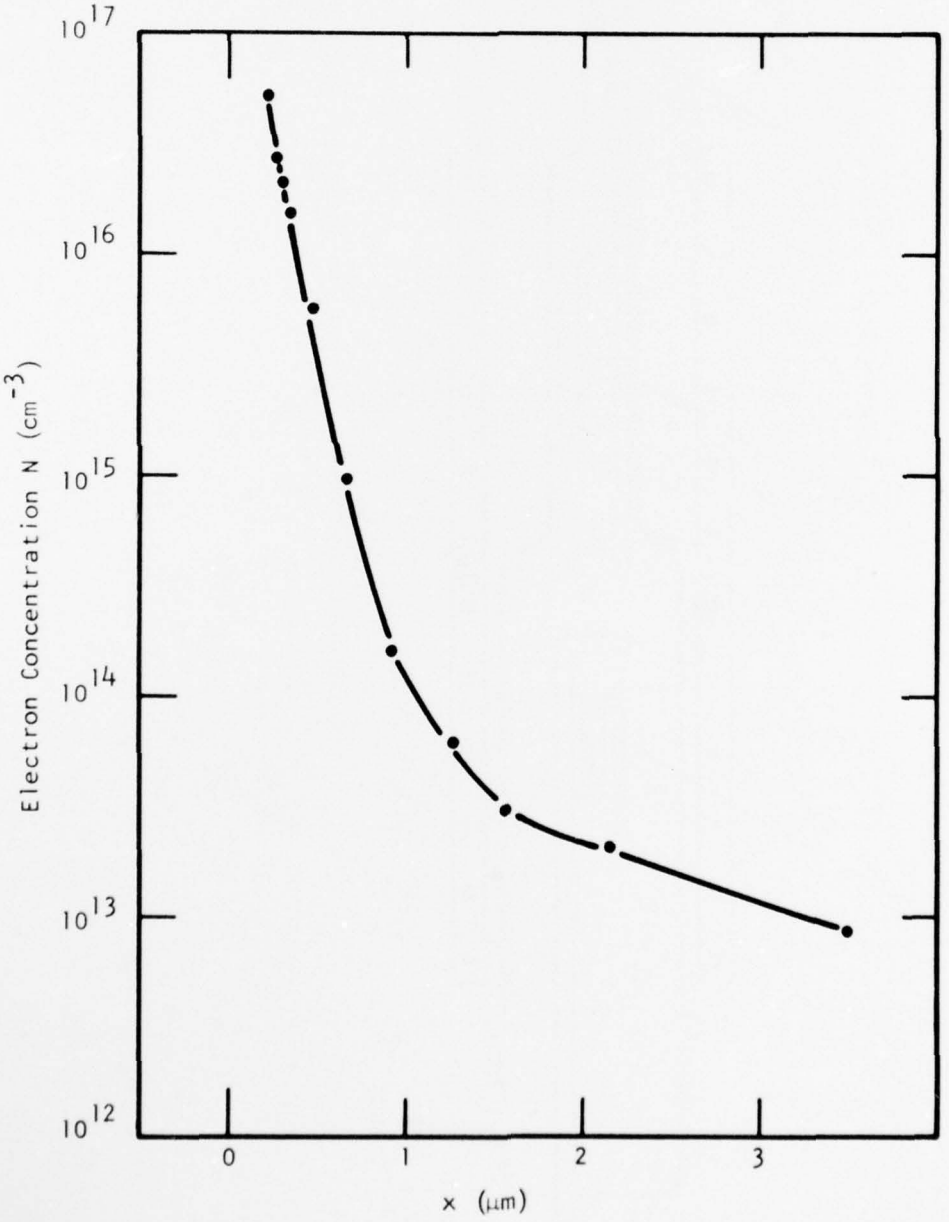


Figure 3 Doping Profile of an FET Structure

B. Device Design

The power and gain requirements for the power amplifier and for each stage of the driver amplifier are discussed in Section III of this report. These requirements are listed in Table 2, assuming no circuit loss. In practice, the devices must deliver 0.5 to 1 dB higher output power to overcome circuit losses.

GaAs FET output power increases with increasing gate widths, and it is necessary to make the gate width large enough so that the devices can readily achieve the required output power without employing such high drain voltages that device reliability becomes a problem. With present devices that have a thermal resistance of about 20°C/W (4800 μm gate width) and no n^+ layers under the ohmic contacts, drain voltages greater than about 10 V are probably unacceptable from a reliability standpoint. It is also necessary that the gate width not be so large that the device efficiency decreases. Our experience indicates that the maximum efficiency is obtained when the device is operated so that its gain is compressed 4 to 5 dB from the small signal gain. Device designs with gate widths that are slightly too large can be accommodated by reducing the pinch-off voltage with a larger gate recess (see Section II.C), but below some value (typically 3 to 4 V), the gain also decreases. The use of lower drain voltages is usually not satisfactory because the small signal gain drops with drain voltage, and ordinarily, all the gain available is needed.

The first driver stage requirements (Table 2) are met by presently available 300 μm gate width devices. Currently available 1200 μm gate width, single-cell devices have gate widths that are slightly too large (900 μm to 1000 μm would be better), but are adequate for the second driver stage. The third driver stage and power stages require multicell power devices to achieve the specified output powers.

At the outset of this program, FET performance results obtained under AFAL Contract No. F33615-76-C-1309 indicated that the 4800 μm gate width devices then available would not meet the power amplifier goal at safe drain bias levels (8 to 10 V) when it was considered that 3 W would probably be needed to overcome circuit losses. This is illustrated in Figure 4, where the influence of gate width and

Table 2

Power and Gain Requirements for Each Stage of the Driver and Power Amplifiers

Stage	Gain (dB)	Output Power (mW)
1st Driver	9	125
2nd Driver	6	500
3rd Driver	5	1585
Power Amplifier	5	2500*

* The outputs of two FETs are combined to give 5 W output power.

length on device microwave performance is shown. The maximum output power with 4 dB gain at 8 V drain bias is plotted as a function of total gate width (varied by bonding from one to four cells of the same device) at several frequencies. Data are included from an older 2 μm gate length, 2400 μm gate width device and a 1 μm gate length, 4800 μm gate width device. Even though the 2 μm device had higher output power at shorter gate widths and lower frequencies due to superior material parameters, the 1 μm devices were far superior at higher frequencies and larger gate widths. The reason is that the gain of both devices was degraded by interconnecting multiple cells, but the higher small signal gain of the 1 μm devices caused them to remain in saturation at the 4 dB gain level under conditions where the 2 μm devices could not. The results from the devices of Figure 4 and other similar devices demonstrated that the present program would require devices with gate lengths of 1 μm or less with a total gate width of somewhat more than 4800 μm for the final stage.

It is known theoretically that when the gate finger width is too great, the attenuation and phase shift of the rf signal will reduce gain. A rough idea of when this occurs can be obtained by treating a gate finger as an R-C transmission line with resistance r per unit length and capacitance c per unit length. The equation for voltage v along this line is

$$\frac{d^2v}{dZ^2} = j\omega rcv \quad ,$$

where $j = \sqrt{-1}$ and ω = the operating frequency. This equation is solved by

$$v(Z) = A\, e^{\pm\sqrt{j\omega rc}\, Z} \quad .$$

Requiring $v(Z \to \infty) = 0$ gives

$$v(Z) = A\, e^{-j\sqrt{\omega rc/2}\, Z}\, e^{-\sqrt{\omega rc/2}\, Z} \quad .$$

Changes in the first exponent shift the phase of the impressed signal, and as the second exponent becomes large, the signal is attenuated. Therefore, as Z is increased (as one moves down a gate finger) the impressed signal is attenuated and shifted in phase. The attenuation reduces the output voltage, and the phase shift causes the output voltage at one end of the gate to be slightly out of phase with that at the other end, producing some cancellation. Both of these effects will reduce the apparent device gain. For a 1 μm gate r may be about

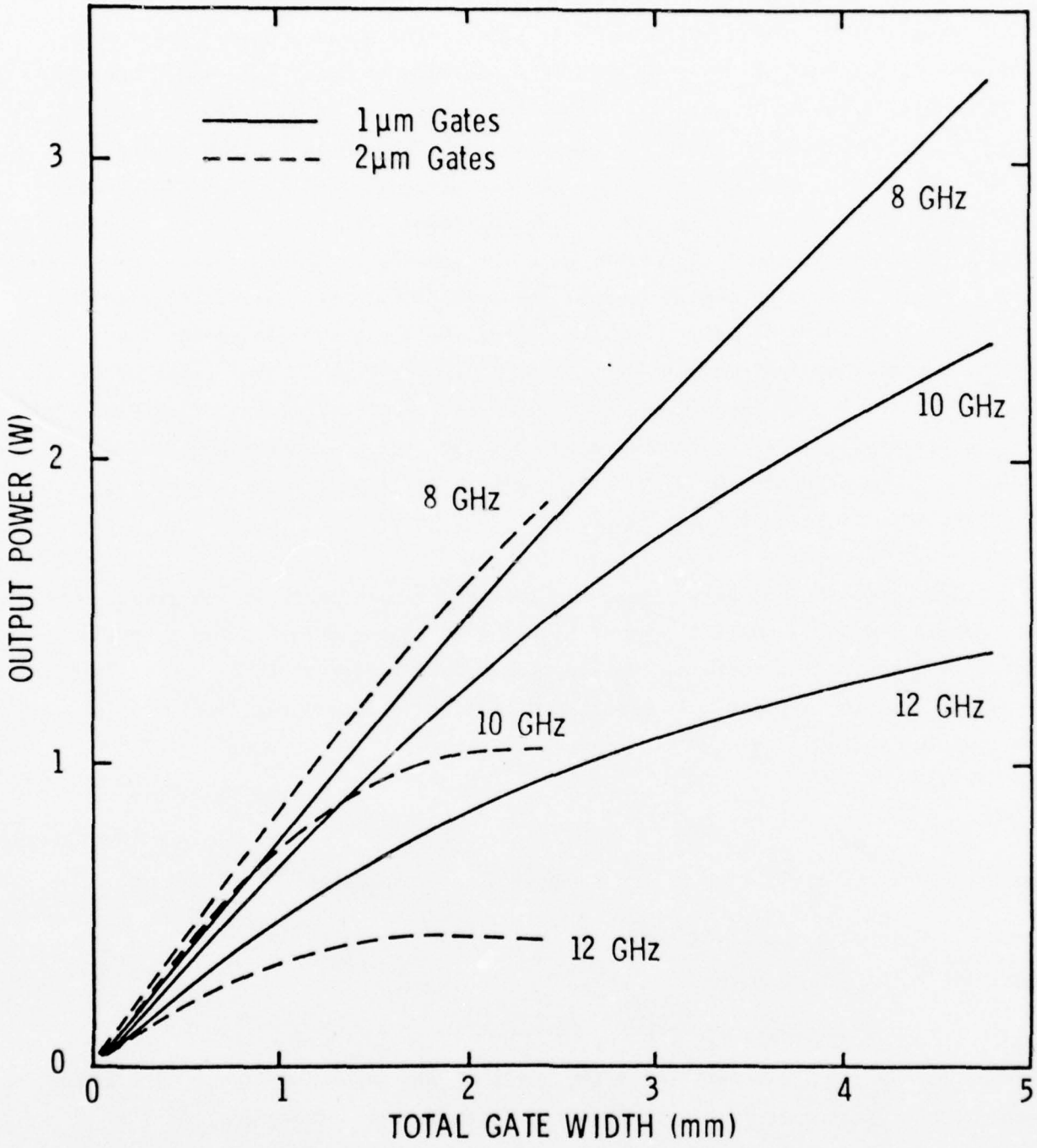


Figure 4 Maximum Output Power with 4 dB Gain at Several Frequencies for 1 μm and 2 μm Gate Length GaAs FETs as a Function of Total Gate Width. The drain bias is 8 V in all cases.

Table 3

Microwave Performance as a Function of Gate Finger Width for GaAs Power FETs Having 1 μm Gates and 1200 μm Total Gate Width

Frequency (GHz)	Gate Finger Width (μm)	Maximum Gain With P_{in} = 15 dBm, 5 V Drain Bias (dB)	Maximum P_{out} With 4 dB Gain, 8 V Drain Bias (mW)	Maximum P_{out} With 6 dB Gain, 8 V Drain Bias (mW)
8	150	8.2	890	810
	200	8.2	910	830
	300	7.4	910	660
10	150	7.0	850	520
	200	7.0	790	480
	300	5.9	600	300
12	150	6.2	660	-
	200	5.7	500	-
	300	5.0	340	-

750 Ω/cm and c about 10 pF/cm. The attenuation and phase shift would probably be serious when $\sqrt{\omega rc/2}\ Z = 1$, which corresponds to $Z \cong 200$ μm at 10 GHz.

Since r and c are not known very accurately and the precise value of $\sqrt{\omega rc/2}\ Z$ at which device gain begins to be seriously degraded is not known, the effect was determined experimentally. This was done by using a mask-set which had adjacent devices with different gate finger widths, but with the same total gate width. The results from a typical slice are shown in Table 3. At 10 GHz the finger width could be as large as 200 μm before performance was degraded. At 12 GHz this maximum finger width was less than 150 μm.

The data from Table 3, Figure 4, and similar devices led us to pick a four-cell, 6400 μm total gate width device with 200 μm fingers as the vehicle for meeting the power amplifier goal. It was originally thought that three cells (4800 μm gate width) of this device would be used for the third driver stage and one cell for the second stage. However, at that time the lower efficiency accompanying a wider than necessary gate width was not fully appreciated. It is now thought that only two cells (3200 μm gate width) will be best for the third driver stage, but one cell (1600 μm gate width) is too large for the second driver stage.

Figure 5 shows two photographs of a 6400 μm gate width device slice during fabrication. The gate length is about 1 μm. Other parameters have been kept about the same as those determined previously: the source-drain spacing is about 5 μm, the epitaxial doping level is about 1×10^{17} carriers/cm^3, and the basic design is unchanged. Included on the slice are several test patterns for measuring capacitance as a function of voltage (to determine the epitaxial doping profile), contact and sheet resistance, and gate metallization resistance.

C. Device Fabrication

The device fabrication process is basically the same as that developed under AFAL Contracts No. F33615-75-C-1123 and F33615-76-C-1309.[8-10] Minor changes have been made to improve the yield of good devices.

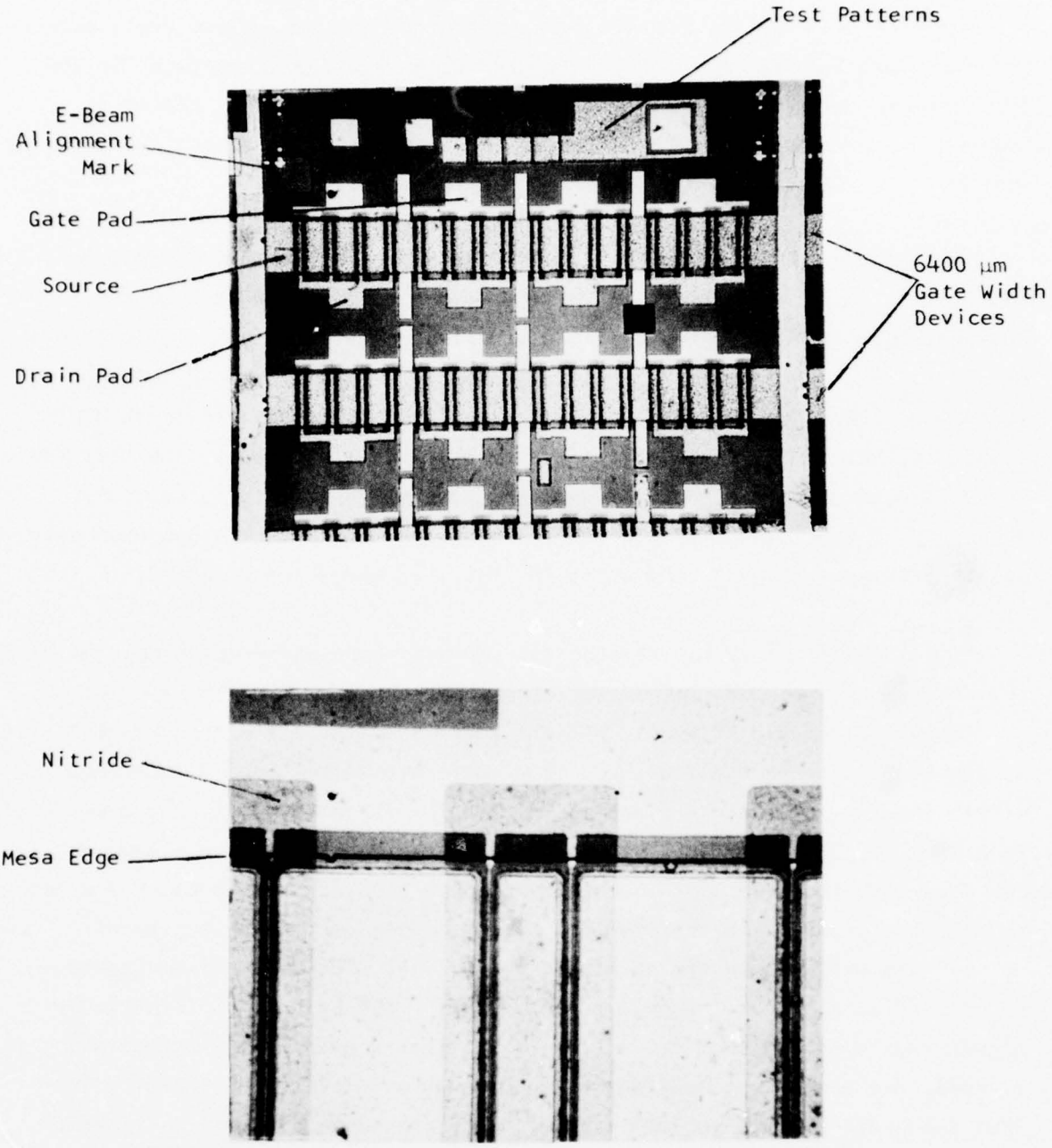


Figure 5 Photographs of 6400 μm Gate Width Devices During Fabrication

The first step following receipt of the anodically thinned slices is to etch mesas through the active layer to isolate the source and drain except for the channel under the gate and to provide an insulating surface for the gate bonding pad. The slices are etched with $H_2SO_4/H_2O_2/H_2O$: 1/8/40 at room temperature for about 30 seconds. This etch does not attach the photoresist and does not etch excessively near the resist edges.

The next step is source/drain metallization. The pattern is defined in photoresist, and the metal is evaporated over the slice and removed from regions where it is unwanted by dissolving the resist in acetone (the lift-off process). The metallization is 1500 Å eutectic composition AuGe followed by 500 Å Ni.[8] The contacts are made ohmic by alloying for one minute at 450°C in flowing He. This metallization system provides very smooth, low resistance contacts with sharp edge definition. The contact resistance is typically 0.3 Ω per mm gate width for slices having $n \sim 1 \times 10^{17}/cm^3$ and has been extrapolated to increase about 50% after 10^6 hours of operation at 165°C.

The gate metallization is also defined by a lift-off process, but the definition is by electron beam instead of ultraviolet light. The electron resist is polymethyl methacrylate (PMMA), and the gate is lifted off with acetone similar to the source/drain metallization. The gates are automatically realigned within the 5 μm source/drain gap to alignment marks in every 2 mm x 2 mm "field" to ± 2000 Å. These marks are the "L"-shaped patterns in Figure 5 and were put down with the source/drain metallization. The gate length can be varied by simply reprogramming the electron beam computer, and gate lengths of 0.5 μm or less are well within the machine's capability. The yield of devices with no shorted or open gate fingers following gate definition is substantially higher when electron beam definition rather than conventional contact printing is used, due to mask-slice abrasion and mask run-out with the latter. The PMMA thickness is 5000 to 7000 Å, and a 4000 Å Al film is readily lifted off. Aluminum is chosen as the gate metal because of the ease with which it is evaporated and its ability to produce good Schottky barriers to GaAs even after annealing at 400°C or more. An important step is to etch the slice slightly in $H_2SO_4/H_2O_2/H_2O$: 1/8/40 at 5° C immediately prior to gate metallization in order to recess the gate below the epitaxial surface. This has been found to improve device microwave performance significantly.[9]

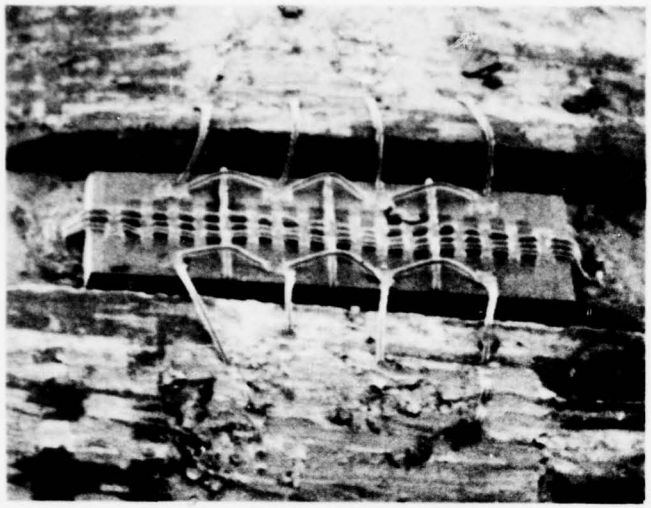
Following gate metallization, a 0.5 μm layer of Cr/Au (defined by lift-off) is evaporated onto the source and drain to improve current spreading to the contact edges and bondability. A nitride layer is then plasma-deposited on the active areas to protect them from scratches and shorts to the source wires. This is the stage at which the photographs of Figure 5 were taken. Next, a 10 μm layer of Au is plated to the sources and drain pads to aid in bonding, and the slice is lapped to 100 μm.

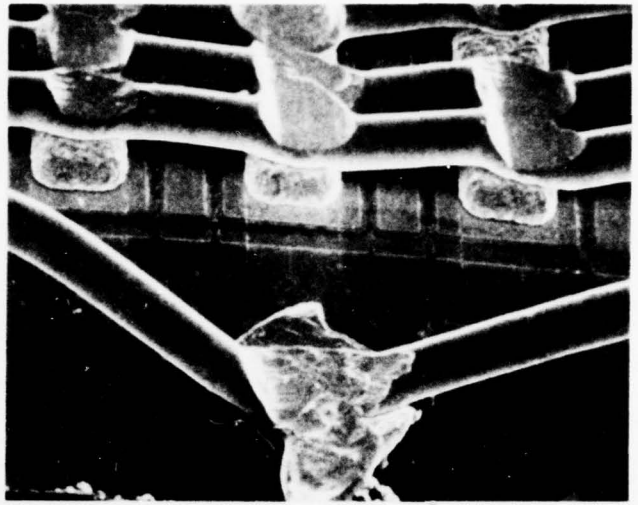
It is very important that device thermal resistance be as low as possible because gain decreases about 0.1 dB for every 10° C temperature rise. For this reason, devices are soldered directly to Cu blocks which are clamped between larger Cu blocks supporting the input and output impedance matching circuits. These larger blocks are screwed to a water-cooled heat sink during microwave testing. Measurements on well-mounted devices and calculations with 4800 μm gate width devices indicate a thermal resistance to the hottest point of about 20°C/W. Measurements with 200 μm wide gate fingers indicate about 25% higher temperature than with 150 μm fingers, so the present 6400 μm gate width chips probably also have about 20°C/W. SEM photographs of a mounted 6400 μm gate width device are shown in Figure 6.

The method of interconnecting cells of multicell devices is very important. With all schemes investigated so far there has been some gain reduction when cells are interconnected. It has been known for some time that a bond wire should interconnect each of the gate pads and each of the drain pads on the chip. Figure 6 shows a device bonded in this manner.

D. Device Performance

The best 10 GHz microwave performance observed to date from several different gate width devices operating at 8 V drain bias is summarized in Table 4. The module stage for which the device was intended is also listed. As mentioned in Section II.B, the first and second stage requirements have been met, although operating the 1200 μm device under conditions that will produce less power may reduce the gain and/or efficiency. The best 3200 μm device had lower gain than the best





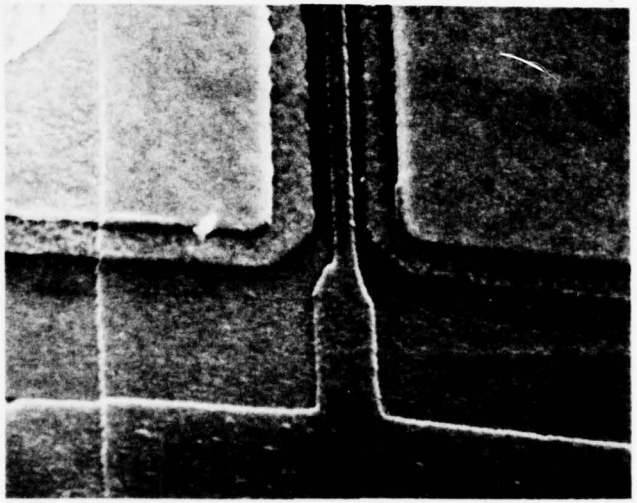


Figure 6 SEM Photographs of a Bonded 6400 μm Gate Width GaAs FET Chip. The gate length is about 1 μm.

Table 4

10 GHz Microwave Performance of GaAs FETs with Several Different Gate Widths

Gate Width (μm)	Output Power (mW)	Gain (dB)	Power-Added Efficiency (%)	Amplifier Stage	Comments
300	160	10	40	1	Meets requirements
600	450	7	37	2	Power low
1200	800	7	35	2	Meets requirements
2400	1450	6	31	3	Power low
3200	1740	5	32	3	Gain low
4800	2140	6	20	Power	Power low
6400*	3230	4	38	Power	Gain low, impedance difficult to match at 10 GHz

* Data taken at 8 GHz

2400 μm device, probably because many more of the latter have been tested, since their photomask sets have been available for a much longer time. Consequently, 2400 μm devices having more nearly ideal parameters for power generation have been fabricated. The 6400 μm gate width device had sufficient gate width to provide the necessary power for the power stage, but the gain was too low, and the impedance could not be matched at 10 GHz. The reason is probably that the increased finger size over 1200 μm gate width cells increases the gate capacitance by a proportionate amount, making the input impedance more difficult to match. The drain-source capacitance is increased by the same factor. In addition, the source-drain spacing is reduced about 20% from the older devices, further increasing the drain-source capacitance and making the output impedance more difficult to match.

It is possible to obtain higher output powers than those listed in Table 4 by operating the devices at higher drain voltages, as shown in Figure 7. This figure is a plot of maximum output power with 4 dB gain at 10 GHz as a function of drain voltage for a 3200 μm gate width device. The power saturated as a function of drain bias due to Joule heating of the device and breakdown of the gate Schottky barrier at higher voltages. The maximum output power of 3 W was very high (close to 1 W/mm gate width), but the difficulty in matching the impedance when more cells were added prohibited comparable three- and four-cell results. It is desirable to operate devices at lower drain voltages to achieve reliable operation, however. Many more device failures occur at high drain voltages; the temperature is higher; and after operation at the highest voltages, the gain has sometimes been observed to be permanently degraded by 0.1 to 0.3 dB.

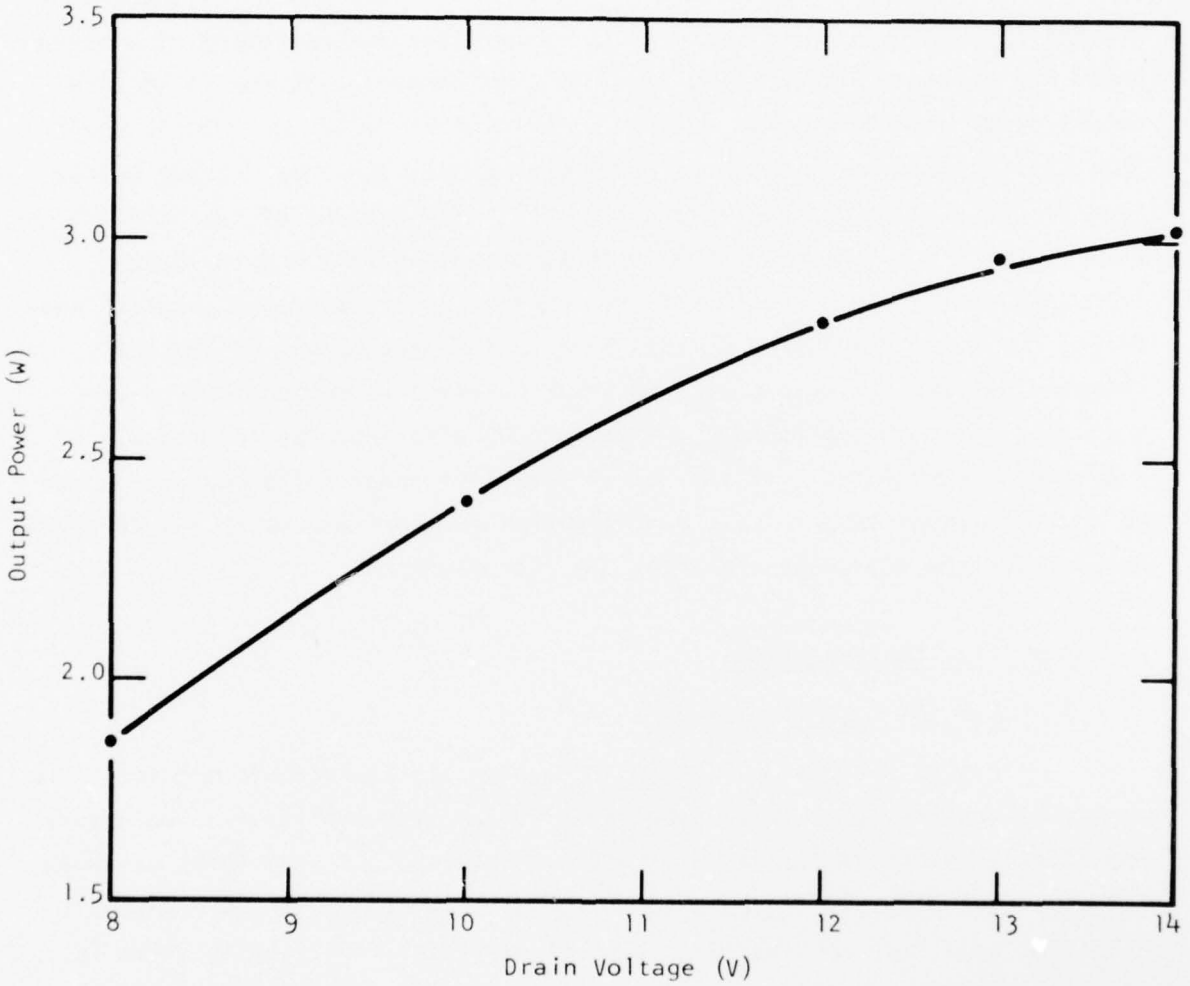


Figure 7 Maximum Output Power at 10 GHz with 4 dB Gain as a Function of Drain Voltage for a 3200 μm Gate Width Device

SECTION III
AMPLIFIER DEVELOPMENT

The circuit effort performed during the first six months of the X-band solid-state module program was directed toward the demonstration of a breadboard FET driver amplifier that is capable of producing 32 dBm (1.58 W) of output power with 20 dB gain over a 1 dB bandwidth of 1 GHz (9 to 10 GHz). This driver amplifier will be cascaded with an output stage (either FET or Read amplifier), to be developed during the later portion of the program, to achieve the 5 W output power goal with 25 dB gain over the 9 to 10 GHz frequency range. This section of the interim report describes progress made during the first six months of this program for development of the FET driver amplifier. Previous work at Texas Instruments on GaAs FET power amplifier has been published.[11] This section also includes the results of a preliminary evaluation of the driver amplifier under pulsed operation and AM additive noise data. Finally, the design and performance of a 3 dB hybrid coupler for the FET power amplifier are discussed.

A. Amplifier Configurations

1. All-FET Power Amplifier

Figure 8 shows an all-GaAs FET power amplifier configuration. The amplifier consists of a driver amplifier and a power amplifier. The driver amplifier provides 20 dB gain at 32 dBm (1.58 W) output with three cascaded FET amplifier stages. Figure 9 shows the circuit layout of the all-GaAs FET power amplifier module. The three-stage driver amplifier is shown in the upper left-hand section of the amplifier module. The first six months of the circuit effort have been concerned primarily with the design and optimization of the driver amplifier.

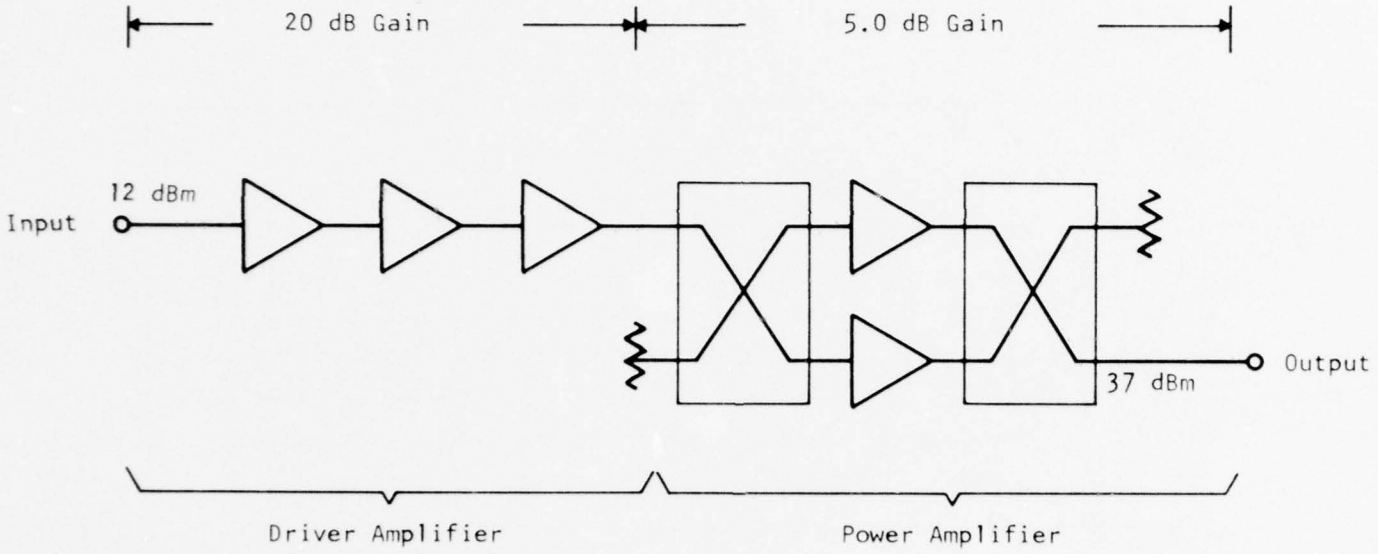


Figure 8 An All-FET Power Amplifier Configuration

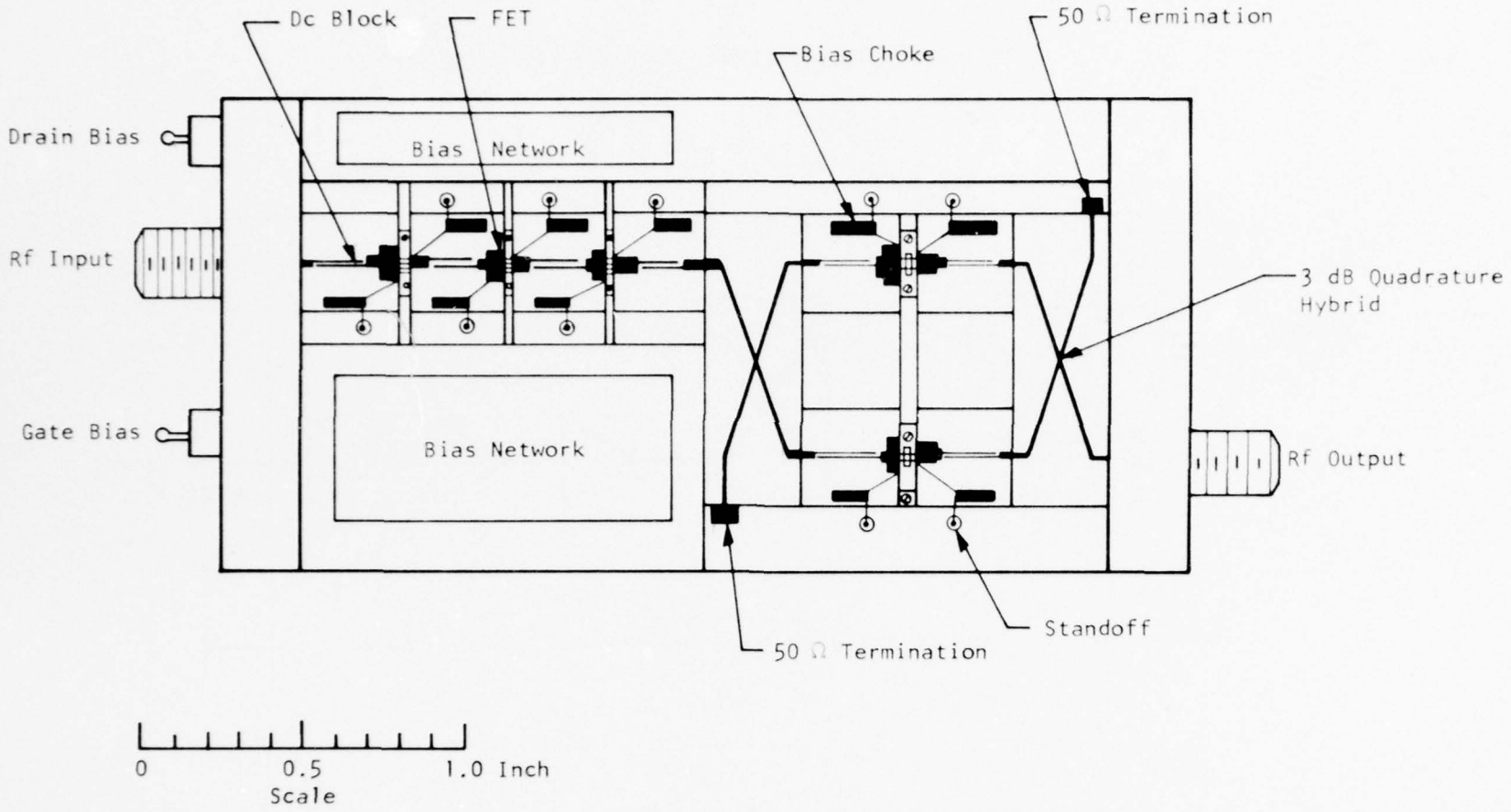


Figure 9 Circuit Layout of the All-FET Power Amplifier Module

2. FET/Read Hybrid Amplifier

The second amplifier configuration is shown in Figure 10. It consists of a GaAs FET driver amplifier and a GaAs Read diode amplifier as the output stage. The driver amplifier is the same as that shown in Figure 8, and is to have an output power level of 32 dBm (1.58 W) to drive the Read diode stage. The circuit layout of the hybrid amplifier is shown in Figure 11 and is similar to that of the amplifier shown in Figure 9 for the all-FET power amplifier configuration, except for the replacement of the power FET output stage by the circulator-coupled Read diode amplifier.

B. Four-Stage Breadboard Driver Amplifier Development

A prototype breadboard driver amplifier using GaAs power FETs with 1 μm e-beam defined gates was designed and fabricated during the early portion of the first six months of the program. For this purpose, a single-cell (1200 μm gate width) device was used in each stage of a three-stage amplifier module with dimensions of 4.8 cm x 3.3 cm x 1.8 cm (1.9 in. x 1.3 in. x 0.7 in.). Figure 12 shows this three-stage amplifier. A single-ended design with interstage impedance matching was used. Each of the input/output circuits and interstage matching networks was fabricated on a 15.2 mm (0.300 in.) by 15.2 mm (0.300 in.) alumina substrate (0.25 mm thick). A single section of edge-coupled line was used as part of the interstage matching networks and dc blocking between stages. The FET chip was mounted on a gold-plated copper carrier that fits into a slot on the amplifier housing. With an input power of 10 mW, this amplifier delivers 500 mW of output power with a gain of 17 ± 0.15 dB over the design bandwidth of 1 GHz (9 to 10 GHz). Figure 13 shows the gain-frequency response of this amplifier. The power supplies required for this module are + 9 V at 0.5 A and - 2.7 V. The power-added efficiency is 10%. To increase the output power level, a single-stage power FET amplifier with a three-cell device (3600 μm gate width) was cascaded with the 0.5 W amplifier module described above. Figure 14 shows the

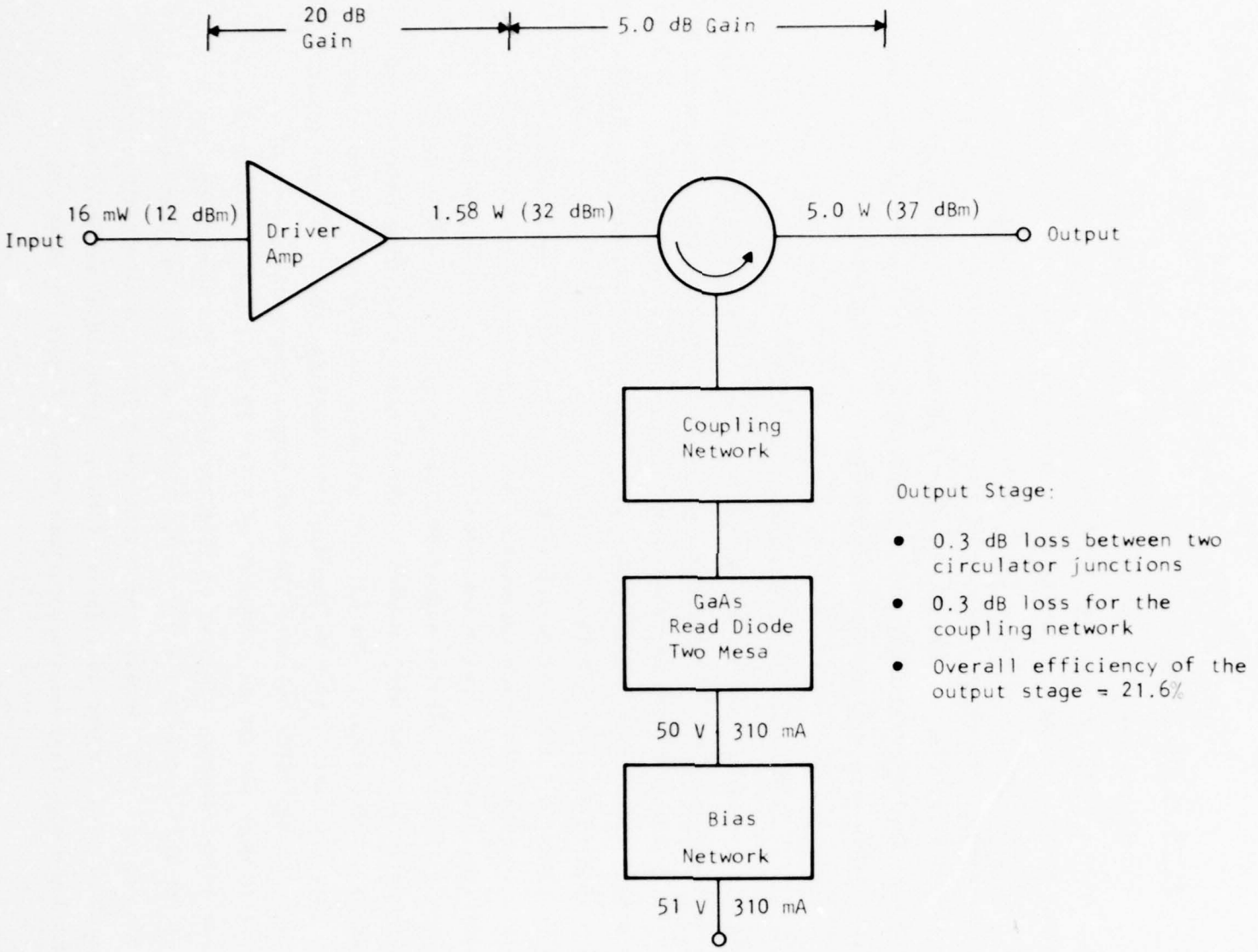


Figure 10 Schematic Diagram of the Hybrid FET/Read Amplifier

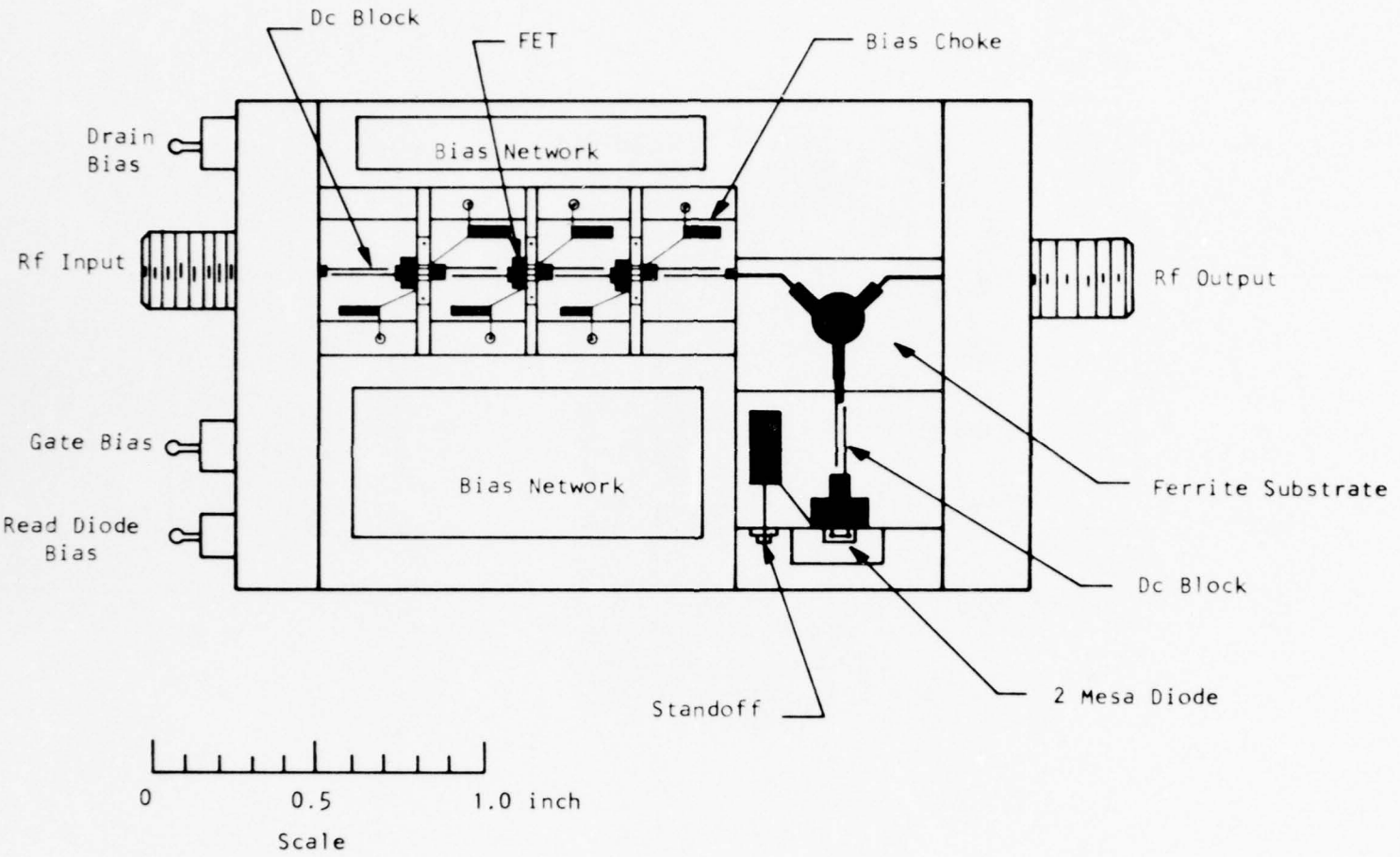


Figure 11 Circuit Layout of the Hybrid FET/Read Amplifier

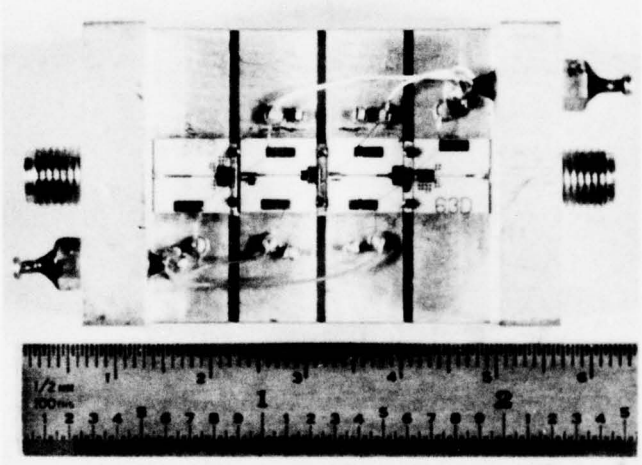


Figure 12 A 0.5 W, Three-Stage FET Amplifier

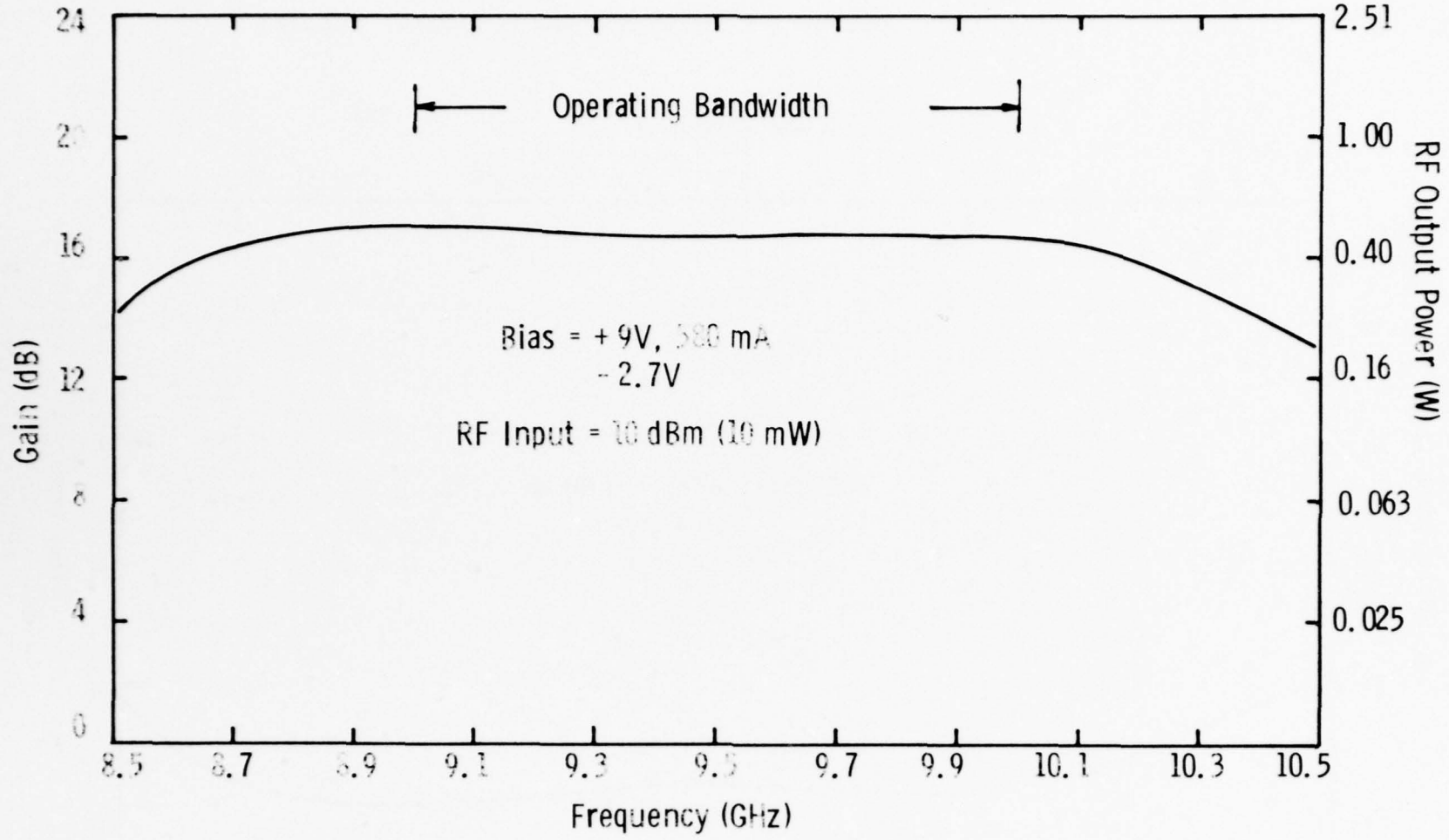


Figure 13 Gain-Frequency Response of the Three-Stage FET Amplifier Shown in Figure 12

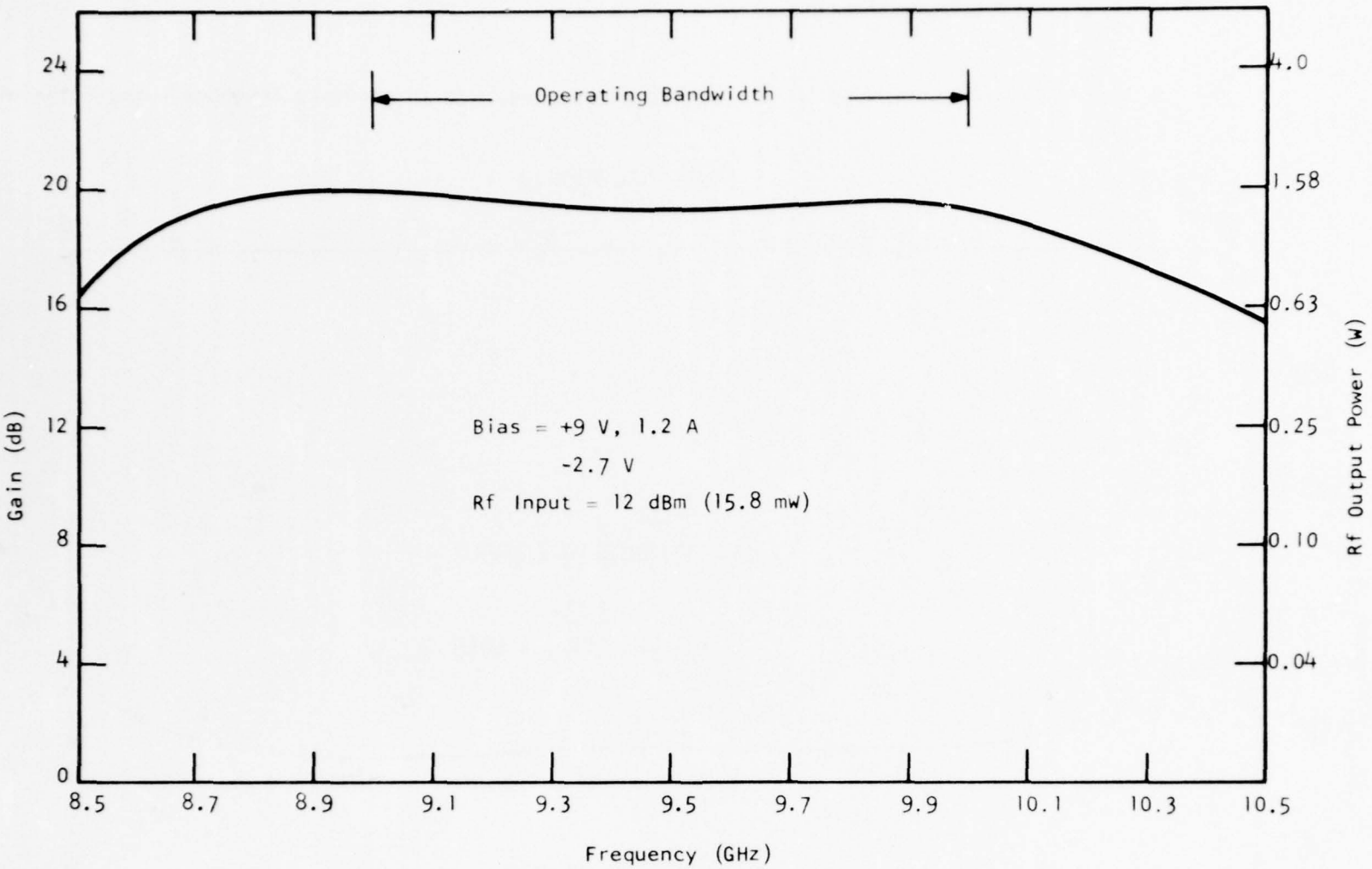


Figure 14 Gain-Frequency Response of a Breadboard Driver Amplifier

gain-frequency response of the four-stage amplifier. Over the design 1 dB bandwidth of 1 GHz (9 to 10 GHz), an output power of 1.58 W was achieved with a 20 dB gain. The overall dc-to-rf conversion efficiency is 14.5 %. It has thus been shown that the output power, gain, and bandwidth goals of the driver amplifier shown in Figure 8 are achievable. As will be discussed in Section III.C, further optimization of the device size (gate width) for each stage has resulted in a three-stage driver amplifier with about the same output power and gain and an overall efficiency of 20 to 25%.

C. Three-Stage Breadboard Driver Amplifier Development

The second three months of the program were devoted to the efficiency-gain optimization of the driver amplifier stages for obtaining maximum efficiency. For this purpose, devices with various gate widths were used in different microstrip circuits optimized for maximum gain and efficiency at X-band.

GaAs FET devices with 300 μm gate width and 1 μm gate length were used as the first stage of the driver amplifier. Figure 15 shows the gain-frequency and efficiency characteristics of this amplifier. The amplifier has an output power of 100 mW with 8 dB gain. The 1 dB bandwidth is 2.7 GHz (7.7 to 10.4 GHz). Power-added efficiencies in excess of 30% have been achieved.

For the second stage of the driver amplifier, the design goal was 6 to 7 dB gain at 500 mW output. Two 300 μm gate width GaAs FETs on the same chip were mounted in single-stage microstrip amplifier circuits for gain-efficiency optimization. With 6 V drain bias, 151 mW was obtained at 9.5 GHz with 9.8 dB gain. The gains of the amplifier were in excess of 8 dB for frequencies between 7 and 10.1 GHz with 12 dBm input. Within the 9 to 10 GHz band, the gain was 9.5 $\pm$ 0.3 dB. This amplifier could be used for the first stage of the driver amplifier instead of the amplifier described above utilizing a

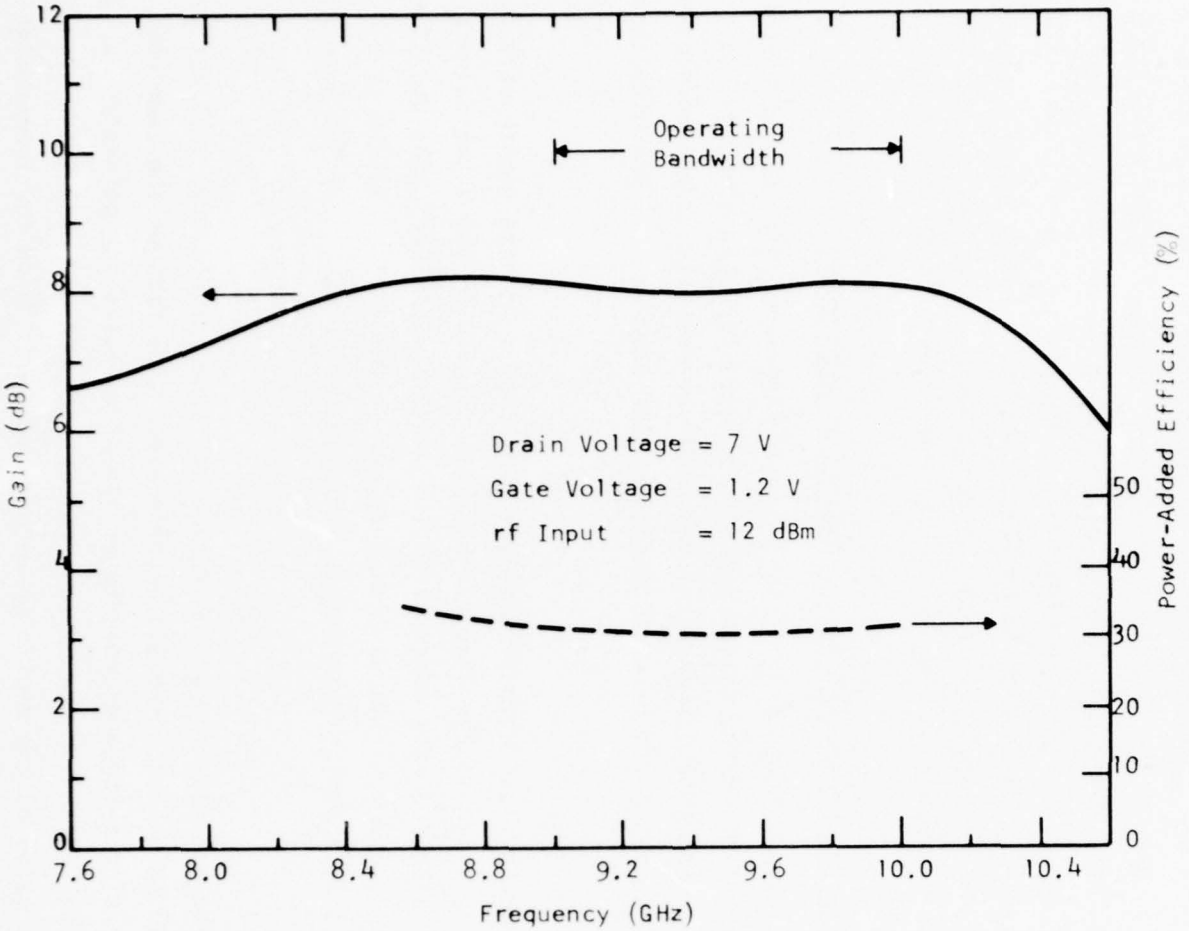


Figure 15 Gain-Frequency and Efficiency Characteristics of the First Stage of the Driver Amplifier

single 300 μm GaAs FET. The two-cell amplifier could offer a reliability advantage. With increase of the drain voltages to 7 and 8 V, the amplifier provides an output power of 400 mW and 447 mW at a gain of 6 and 6.5 dB, respectively, at 9.5 GHz. The power-added efficiencies were in the range of 35 to 40%. Under these conditions, the amplifier could be used as the second stage of the driver amplifier at an output power level of 400 to 500 mW and 6 to 7 dB gain.

Cascading the amplifier described above with the 100 mW, 8 dB gain amplifier using the 300 μm FET produces the gain-frequency response shown in Figure 16. The figure shows that this two-stage amplifier can provide an output power in excess of 400 mW with 14 dB gain. Power-added efficiencies as a function of frequency are also plotted in the same figure. Efficiencies on the order of 33 to 36% have been achieved.

For the third stage of the driver amplifier, experimental results indicate that an FET with a total gate width between 2400 μm and 3600 μm will be adequate to produce an output power of 1.5 to 1.6 W with ~ 5 dB gain and 20 to 25% power-added efficiency. With a 2400 μm gate width FET, an output power of 1.5 W with 4.8 dB gain and 24% efficiency has been achieved. The linear gain is 5 dB.

Attempts were made to cascade this 1.5 W amplifier with the two-stage amplifier having the performance shown in Figure 16 to achieve the performance goals of the three-stage driver amplifier. Unfortunately, the output FET was damaged during the circuit integration procedure, and it was necessary to use an output stage with lower efficiency and output power in the three-stage amplifier. Figure 17 shows a block diagram of the three-stage driver amplifier with the measured gains and dc currents, etc., indicated.

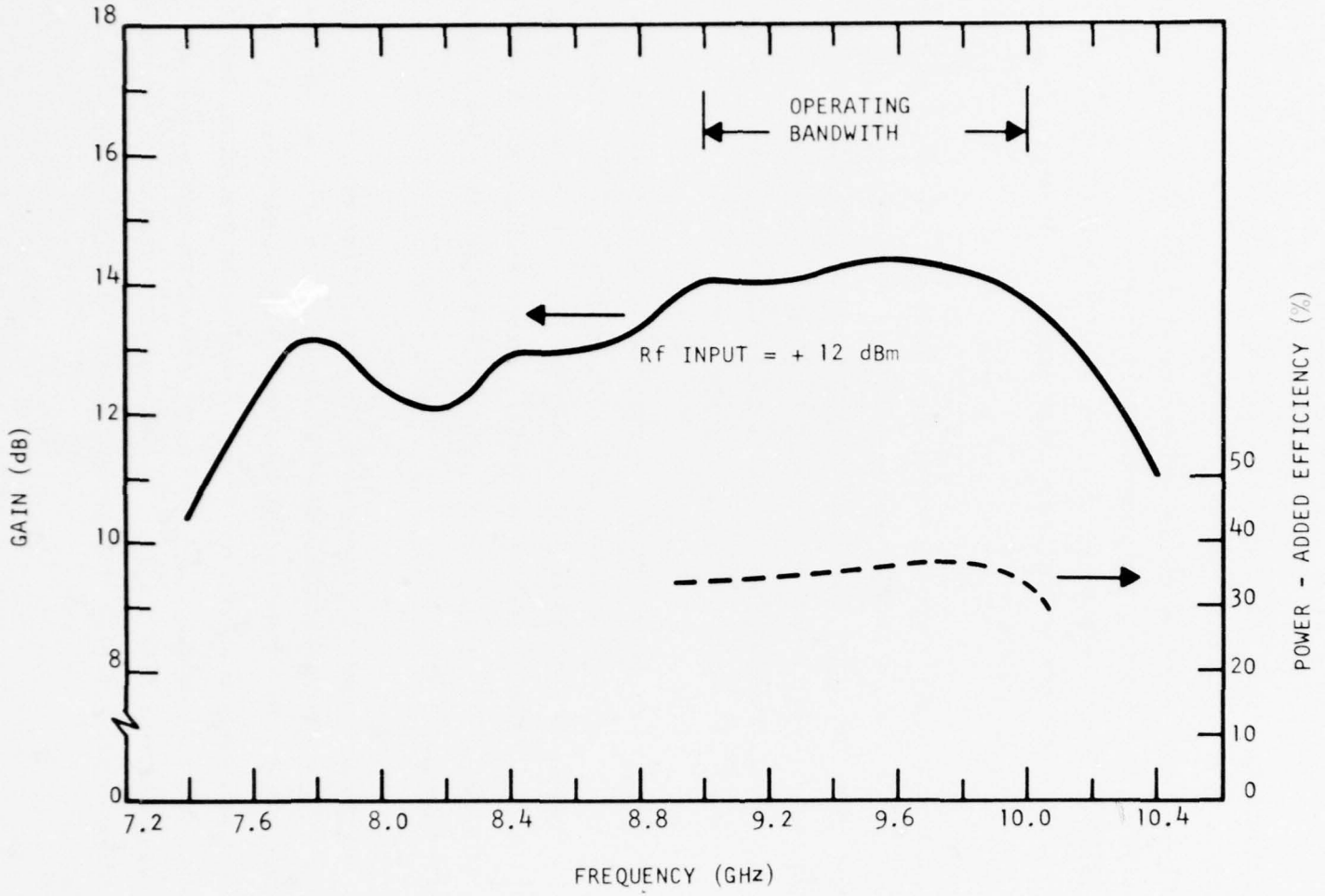
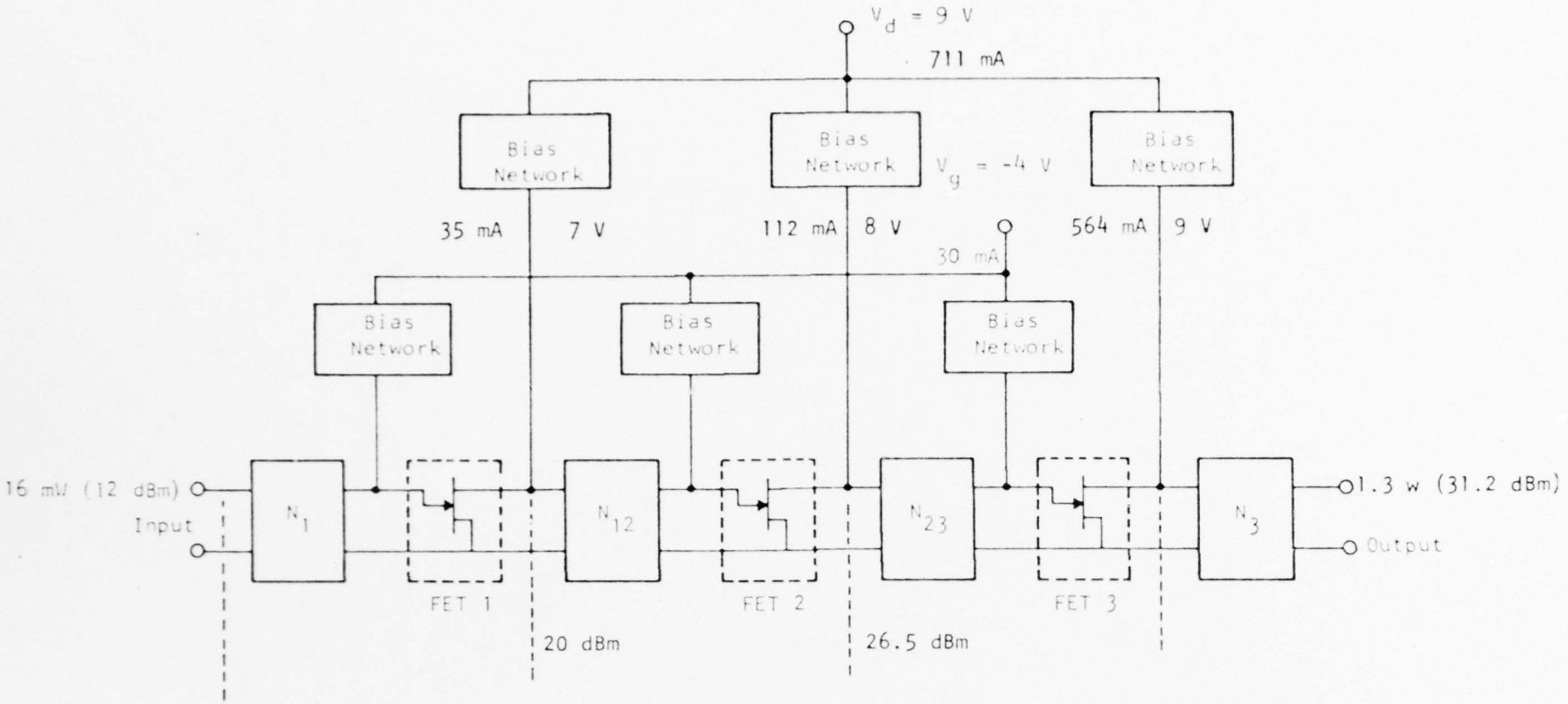


Figure 16 Gain-Frequency and Efficiency Characteristics of a Two-Stage GaAs FET Amplifier



Stage	I	II	III
Gain (dB)	8	6.5	4.7
Dc Input (watts)	0.245	0.9	5.08
Rf Output (watts)	0.100	0.447	1.3
Rf Power Added (watts)	0.084	0.347	0.95
Power-Added Efficiency (%)	34	37.7	18.7

- Total dc Power Input = 6.4 watts
- dc Power Loss in Bias Networks = 0.18 watts
- Amplifier Efficiency Excluding Bias Network Losses = 20.6%
- Overall Amplifier Efficiency = 20%

Figure 17 Block Diagram of a Power FET Driver Amplifier

It is shown that an output power of 1.3 W with 19 dB gain and 20% overall amplifier efficiency was achieved. Table 5 summarizes the performance of the individual stages and cascaded amplifiers. The projected three-stage amplifier performance is based on the use of the 24% efficient, 4.8 dB gain, and 1.5 W amplifier as the output stage. It is shown that an output power of 1.5 W with 19.1 dB gain and 25% efficiency could have been achieved if the more efficient output stage had been used. Figure 18 shows a photograph of the three-stage driver amplifier with the bias network, dc bias pins, and input/output rf connectors. As mentioned earlier, the individual stages were characterized in terms of gain, bandwidth, and output power prior to cascading in the three-stage housing. In the final design of the driver amplifier, a circuit design approach similar to that shown in Figure 12 will be used.

On the basis of the results obtained for the breadboard driver amplifier, the following conclusions have been reached concerning the optimum sizes (gate widths) to be used for maximizing the efficiency, with due consideration also for reliability. The first stage of the driver amplifier should have 300 μm total gate width, the second stage 900 μm, and the third stage 3200 μm.

D. RF Measurements

1. Pulse Data

Evaluation of the FET amplifier under pulsed conditions has been successfully performed on single- and multicell FETs using a pulse biasing scheme that pulses the gate from the pinch-off condition to the nominal gate bias. The input rf is applied as a cw signal, while the output of the FET amplifier pulses on and off according to the gate bias. The drain voltage is maintained at a constant value.

Table 5

FET Driver Amplifier Performance

	Stage				1+2+3	
	1	2	3	1+2	Actual	Projected
Output Power (mW)	100	447	1500	423	1300	1500
Gain (dB)	8	6.5	4.8	14.3	19.0	19.1
Efficiency (%)	34	37.7	24	36	20	25
1 dB Bandwidth (GHz)	8.0-10.4	8.8-10.3	9.0-10.0	8.4-10.2	9.0-10.0	9.0-10.0

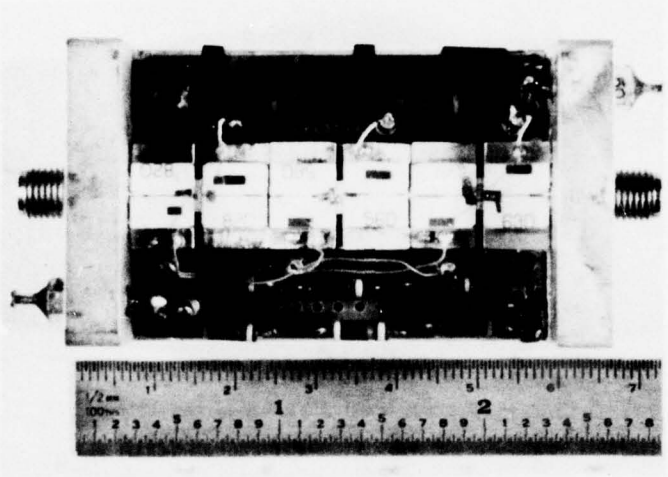


Figure 18 A Three-Stage, Breadboard Power FET Driver Amplifier

Figure 19 shows the system used for the pulse measurements. A cw source such as a sweeper/TWTA combination provides the input signal to the FET amplifier under test. The gate pulsing circuit generates the proper level and polarity for the gate signal. It is driven by an HP 214A pulse generator. The rest of the system consists of standard calibration and power-monitoring equipment for measuring gain under cw and pulsed conditions. A crystal detector (HP 8470B) is used to display the output power on the oscilloscope. The scope is also used to monitor the gate voltage. The detector output is calibrated under cw conditions using the precision attenuator and power meters without the amplifier under test. After the detector is calibrated, the test amplifier is inserted, and a cw power reference datum is established on the CRT screen. During pulsed operation, the relative power of the pulsed output can be compared with the cw datum.

Figure 20 shows a typical pulse response for a 200 ns pulse as detected by the crystal detector and displayed on the CRT screen (upper trace) of the oscilloscope. The device under test is a two-cell FET with an electron-beam defined gate; the total gate width is 2.4 mm, the nominal gate length is 1 μm, and the input rf power is 26 dBm. For the upper trace the cw reference is set at one division from the top graticule line and corresponds to a cw output power of 29.6 dBm. As seen from the photograph, the output power during the pulse is nearly identical to the cw output power, even after rf retuning for the pulsed mode of operation. During the off portion of the cycle, the gate voltage is nearly at pinch-off at -8.7 V, and during the on portion, it is adjusted for maximum output power. The risetime of the rf output pulse is determined by the risetime of the gate voltage waveform, and in the case of Figure 20, is seen to be about 30 ns. It must be noted that the calibration for the upper trace is highly nonlinear (due to the detector characteristic) and that the output power difference between the on and off portions of the pulse is actually about 11 dB. Since the output power during the pulse is nearly identical to the

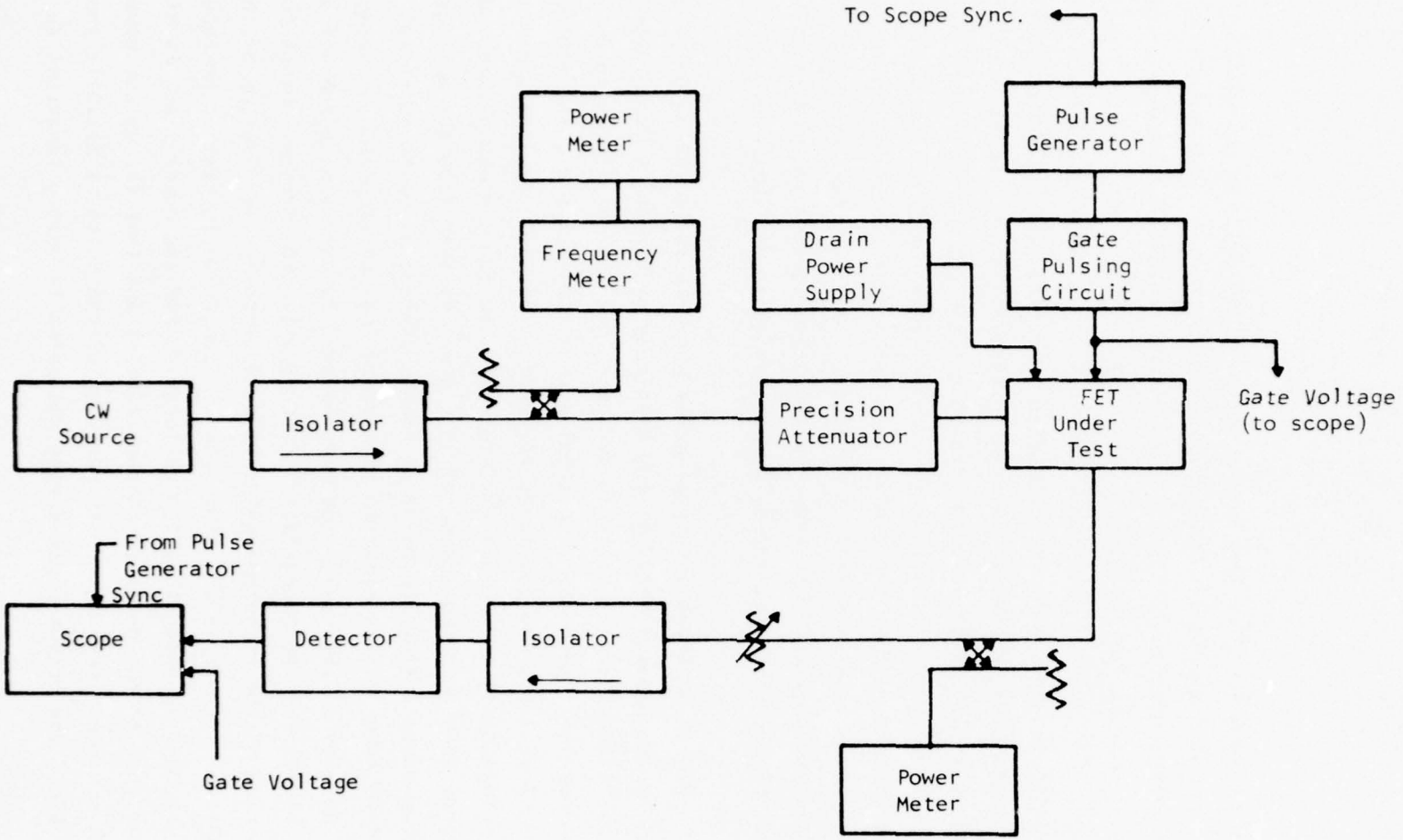
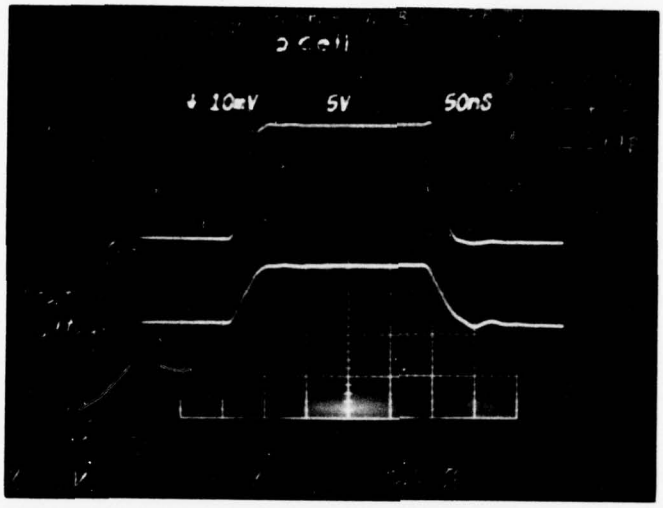


Figure 19 FET Pulse Measuring Setup



← Cw Reference
P_{out} = 29.6 dBm

Vertical - upper trace: 2 dB/div (between ± 1 dB marks)

Vertical - lower trace: 5 V/div

Horizontal: 50 ns/div

Input Power: 26 dBm

Duty Cycle: 0.2%

Transistor Bias Conditions: V_D = 8 V, I_D = 290 mA, V_g = -1.8 V

Frequency: 9 GHz

FET: 2 cell (2.4 mm gate width) with electron beam defined gate (~ 1 μm gate length)

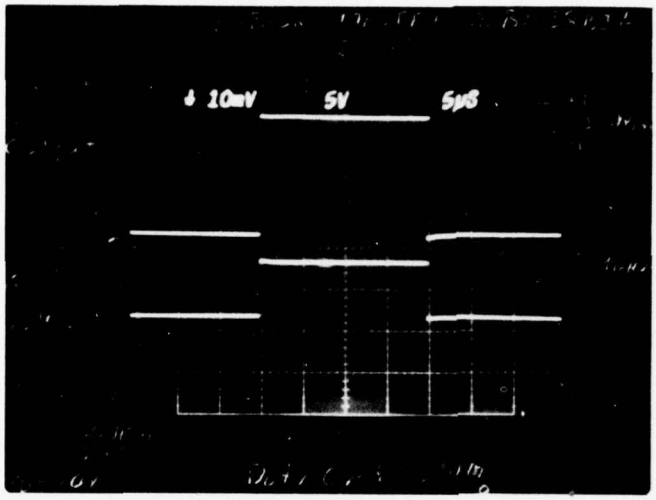
Figure 20 Pulsed Response for a Two-Cell FET, V_D = 8 V

cw power output for even the first 200 ns in Figure 20, the amplitude droop for varying pulse widths (> 200 ns) and duty cycles is negligible for this transistor under the given bias conditions. This is true in part because the total dc input power is at a relatively low level so that heating of the device during cw operation is not sufficient to cause significant power degradation, as compared to short pulse, low duty cycle operation when the device is at a cooler temperature.

Figures 21 and 22 show the pulse operation of the same transistor biased at a higher drain voltage of V_D = 10 V. The pulse lengths are 20 μs and 1 ms, respectively, and as before, the gate voltage and rf tuning are adjusted for maximum output power. The input power is 26 dBm, and the cw output power is 30 dBm. Again, the cw reference datum is set one division below the top graticule line. Because of the increased dc power input, a power advantage does occur in this case for the short pulse low duty cycle operation in comparison to the cw mode. However, the increase in power is only about 0.4 dB for pulse lengths between 200 ns and 1 μs and is even smaller for a 20 μs pulse, as shown in Figure 21. Figure 22 shows that for a very long pulse, for example greater than 0.5 ms, the output power has essentially approached the cw level. That is, for the two-cell FET shown in Figures 21 and 22 and for the bias conditions indicated, amplitude droop occurs up to 0.5 ms, although the magnitude of this droop is only about 0.8 dB/ms.

2. Noise

Preliminary AM additive noise measurements have been made on the four-stage driver amplifier at 9.4 GHz from 1 kHz to 200 kHz away from the carrier. Although the design goal is specified for the final 37 dBm amplifier, the AM additive noise for the 32 dBm driver amplifier is about 30 dB below this design goal at 1 kHz away from the carrier, and even further below for



← Cw Reference
P_{out} = 30 dBm

Vertical - upper trace: 2 dB/div (between ± 1 dB marks)

Vertical - lower trace: 5 V/div

Horizontal: 5 μs/div

Input Power: 26 dBm

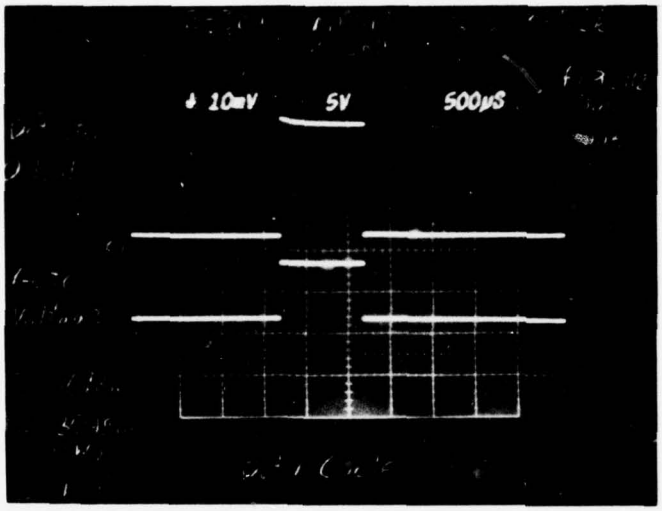
Duty Cycle: 4%

Transistor Bias Conditions: V_D = 10 V, I_D = 308 mA, V_g = -1.9

Frequency: 9 GHz

FET: Same as in Figure 20

Figure 21 Pulsed Response for a Two-Cell FET, V_D = 10 V



← Cw Reference
P_{out} = 30 dBm

Vertical - upper trace: 2 dB/div (between ± 1 dB marks)

Vertical - lower trace: 5 V/div

Horizontal: 500 μs/div

Input Power: 26 dBm

Duty Cycle: 3%

Transistor Bias Conditions: V_D = 10 V, I_D = 305 mA, V_g = -1.9

Frequency: 9 GHz

FET: Same as in Figures 20 and 21

Figure 22 Pulsed Response Showing Amplitude Droop for a Two-Cell FET

frequencies greater than 1 kHz away. In other words, there is roughly a 30 dB margin of additive noise allowed for the final power stage which will still meet the final amplifier noise requirement.

To characterize the noise due to the amplifier alone, i.e., the additive noise, it becomes necessary to exclude from the measurements the noise present in the driving or source signal. In this regard, a noise measuring system as described by Sann[12] can be used.

Figure 23 shows a simplified block diagram of the noise measurement system. The setup is realized in X-band waveguide. The basic system consists of the reference channel A, and the test channel B, which includes the amplifier under test. A single Gunn diode source provides the drive signal to the amplifier as well as the necessary signals to the other channels. A balanced mixer is used to down-convert the noisy signal in test channel B to baseband. Depending on the quality of the balanced mixer, the AM noise present in the reference signal is largely suppressed. The output of the mixer at the i.f. port contains the additive noise near the carrier, shifted down in frequency by the carrier frequency. This signal is amplified and applied to the input of the tunable wave analyzer. Channel C is used to suppress the carrier in the test channel (by proper leveling and phase shifting) so that the balanced mixer can be driven with a stronger signal without saturating the mixer diodes. Effectively, this raises the total system sensitivity. Finally, channel D, the calibration channel, is used to calibrate the system by injecting a known amount of modulation into the test channel and observing the corresponding meter reading on the wave analyzer. During calibration, the phase shifter in reference channel A is set for a maximum reading on the wave analyzer. For AM noise measurements the phase of the calibration channel D is set so as to produce AM sidebands in the test channel B. This is checked by switching the signal in the test channel to a crystal detector and spectrum analyzer, and adjusting the phase of the calibration signal for maximum output from the crystal detector.

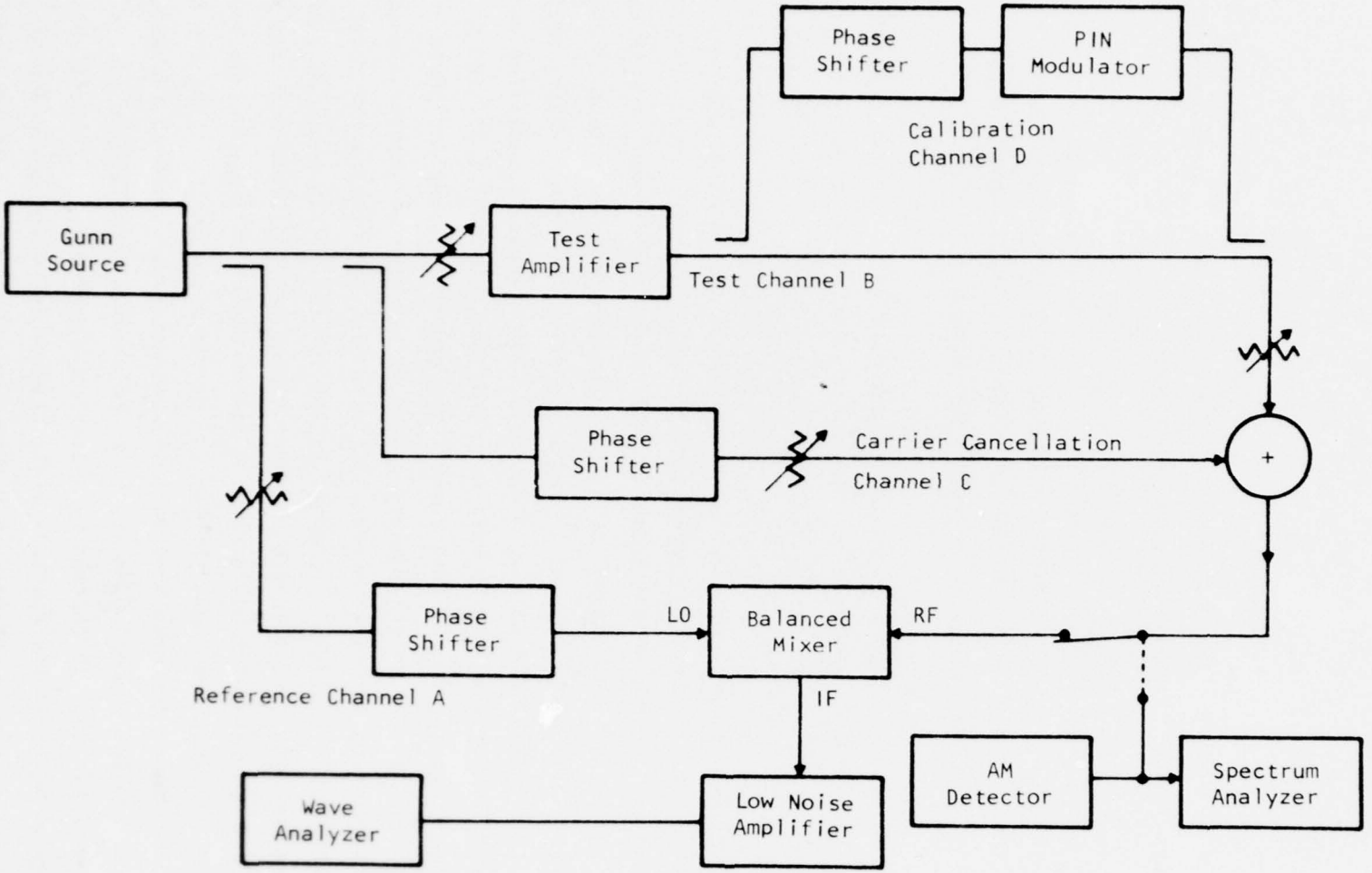


Figure 23 AM Additive Noise Measuring Setup

Figure 24 shows the results for the additive AM noise measurements for the driver amplifier at 9.4 GHz. The lower curve shows the measurement threshold, i.e., the system sensitivity. This curve was obtained without the test amplifier in channel B. The system sensitivity is basically limited by the noise contribution from the mixer diodes, the noise present in the Gunn source, and the noise figure of the i.f. amplifier. The middle curve shows the results with the driver amplifier inserted in the test channel B. As seen from the curve, the AM noise power (in a 1 Hz bandwidth) to carrier power ratio at 1 kHz away from the carrier is -136 dB. At 200 kHz away from the carrier it is down -149 dB. The top curve is the additive noise design goal for the 5 W amplifier.

E. 3 dB Hybrid Coupler

One of the essential components for a balanced amplifier is a low loss 3 dB hybrid, which is used for power combining as well as for providing a low return loss for the power amplifier stage. Two designs were investigated, the tandem 90° hybrid and the interdigital 90° hybrid, to determine which exhibited the best overall properties with regard to insertion loss, return loss, directivity, and amplitude and phase tracking of the direct and coupled ports over the frequency range of interest.

The tandem hybrid is composed of two 8.3 dB edge-coupled hybrids fabricated on a polished 0.25 mm alumina substrate (see Figure 25). A 3 dB hybrid with a single edge-coupled configuration is difficult to produce because of the extremely tight spacing tolerance between the coupled lines, so the tandem approach was undertaken. Using OSM coax to microstrip transitions on all four ports of the test fixture, the measured

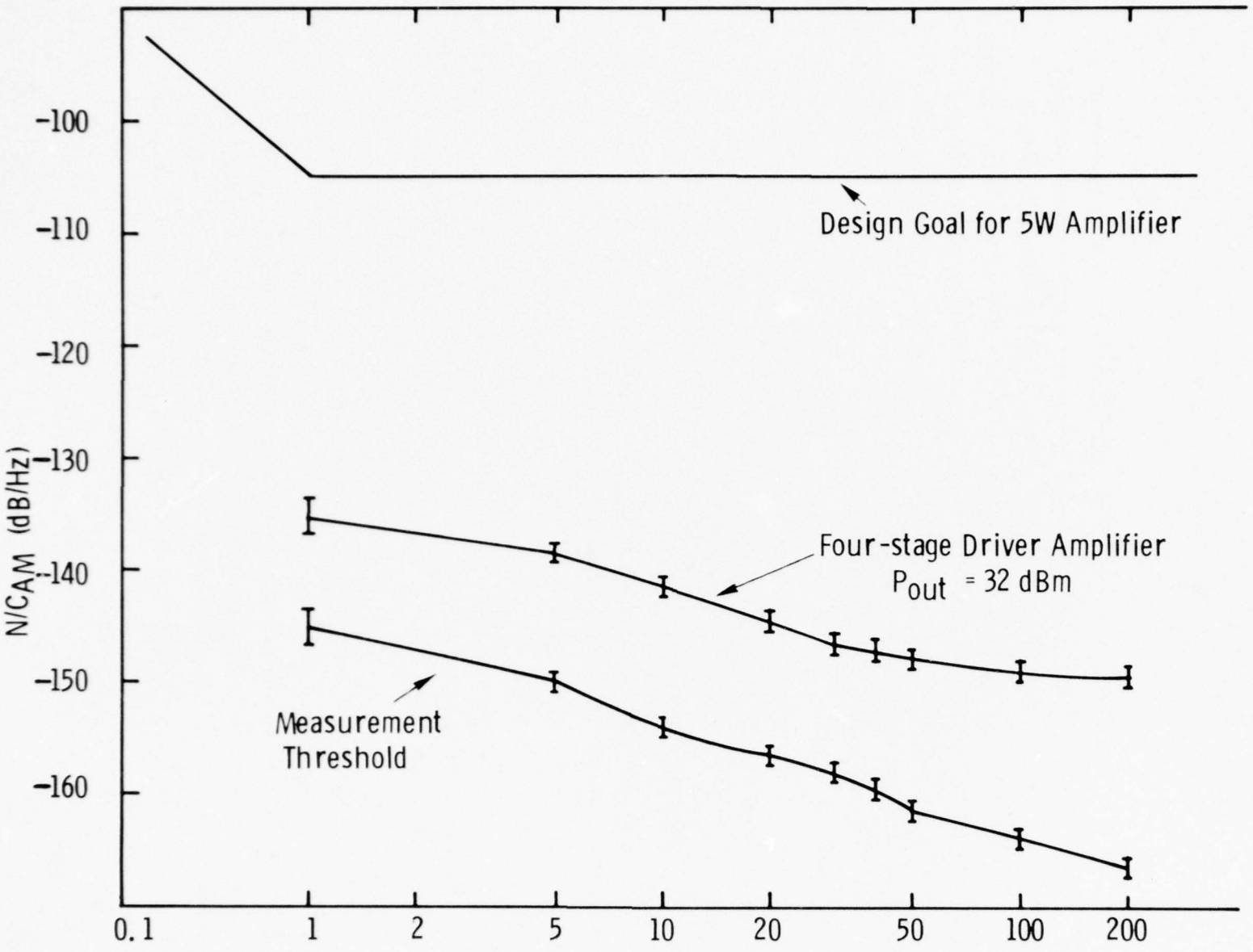
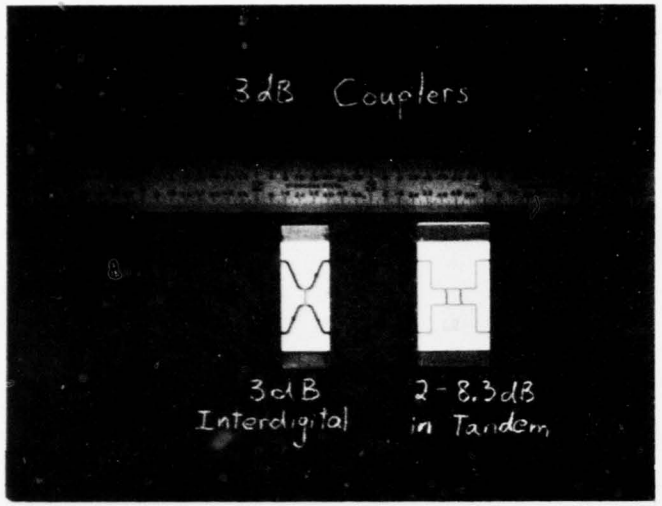
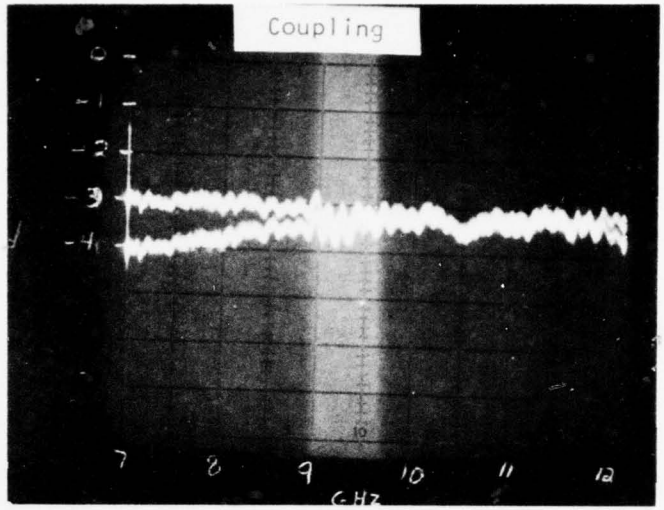


Figure 24 AM Additive Noise Results for Driver Amplifier



- Interdigital - on 25 mil Al_2O_3
- Tandem - on 10 mil Al_2O_3

(a)



Interdigital Coupled and Direct Port Response

Vertical: 1 dB/div
Horizontal: 500 MHz/div

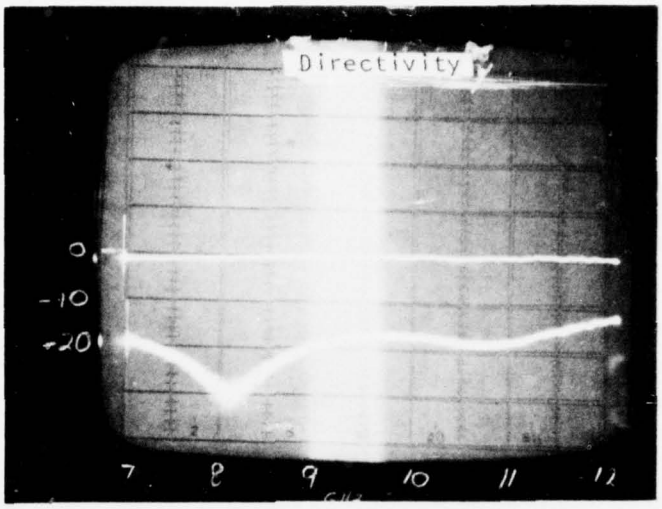
(b)

Figure 25 3 dB Coupler, Design and Coupling Results. (a) Comparison of tandem and interdigital design; (b) measured coupled and direct port response from 7 to 12 GHz for interdigital coupler.

output from the direct and coupled ports revealed nearly a 1 dB insertion loss (over and above the nominal 3 dB power split) in the 9 to 10 GHz frequency range. Although it is advantageous to have the hybrid fabricated on 0.25 mm alumina so it will be compatible with the substrate height of the FET matching circuits, the insertion loss observed with the tandem approach was larger than anticipated. An interdigital hybrid design was therefore undertaken.

The coupling region of the interdigital hybrid consists of several parallel microstrip lines with alternate lines tied together (See Figure 25). Due to tight tolerances on the spacings between lines, the interdigital hybrid was fabricated on polished 0.63 mm alumina instead of 0.25 mm alumina. As seen in Figure 25, the insertion loss observed at the coupled and direct ports was 0.4 dB in the frequency range of 9 to 12 GHz. Figure 26 illustrates the directivity (> 13 dB from 7 to 12 GHz) and the return loss (> 15 dB from 7 to 12 GHz) for the interdigital hybrid. On the basis of these results, the interdigital approach was chosen to be implemented in the balanced amplifier, due to its superior insertion loss characteristics.

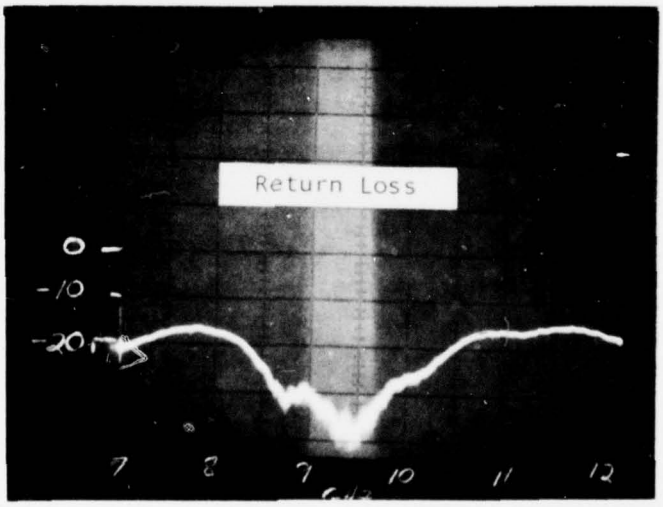
Future work on the 3 dB hybrid will involve adaptation to the final system. The isolated port could be altered to incorporate an internal termination on the alumina substrate. The insertion loss and overall dimensions can be reduced by shortening the input and output lines. Minor modifications will be performed as necessary for optimal performance.



Interdigital Coupled and Isolated Ports Response

Vertical: 10 dB/div
Horizontal: 500 MHz/div

(a)



Interdigital Return Loss

Vertical: 10 dB/div
Horizontal: 500 MHz/div

(b)

Figure 26 Measured Directivity and Return Loss for 3 dB Interdigital Coupler. (a) Directivity; (b) return loss

SECTION IV
SUMMARY AND PLANS

During the first six months of this program, GaAs FETs were fabricated that meet the performance requirements of the three-stage driver amplifier. Optimization of 6400 μm gate width devices for the power amplifier has begun.

Two breadboard driver amplifiers were developed. The first was a four-stage amplifier that delivered 1.58 W with 20 dB gain with 1 dB bandwidth of 1 GHz (9 to 10 GHz). The amplifier efficiency, including circuit losses, was 14.5%. A three-stage driver was built using more nearly optimum devices. This amplifier delivered 1.3 W with 19 dB gain and 20% efficiency over the required frequency band. The first two stages of this amplifier showed excellent performance, delivering 423 mW with 14.3 dB gain at 36% efficiency over the 8.4 to 10.2 GHz frequency band. Different devices will be used in the final driver amplifier stage in order to meet the 1.58 W power output, 20 dB gain performance goals.

The major effort planned during the next six-month period will be to develop the 5 W, 5 dB gain FET and Read diode power amplifiers. Work on the FET power amplifier will begin first because more effort is expected to be required to fulfill this task. This is to be a balanced amplifier combinirg two 3 W, 6 dB gain amplifiers with a hybrid coupler. Both the driver amplifier and the power amplifiers will be tested under pulsed conditions.

REFERENCES

1. W. F. Finch and E. W. Mehal, "Preparation of GaAsP by Vapor Phase Reaction," J. Electrochem. Soc. 111, 814 (1964).

2. D. Effer, "Epitaxial Growth of Doped and Undoped GaAs in an Open Flow System," J. Electrochem Soc. 112, 1020 (1965).

3. D. W. Shaw, "Kinetics of Transport and Epitaxial Growth of GaAs with a Ga-$AsCl_3$ System," J. Crystal Growth 8, 117 (1971).

4. I. Nozaki, et al., "Multilayer Epitaxial Technology for the GaAs Schottky Barrier FET," GaAs Symposium 1974, Deauville, France.

5. D. W. Shaw, et al., "GaAs Epitaxial Technology," GaAs Symposium 1966, Reading, U. K.

6. J. V. DiLorenzo, et al., "Vapor Growth of Epitaxial GaAs," J. Crystal Growth 17, 189 (1972).

7. J. D. Wiley and G. L. Miller, "Series Resistance Effects in Semiconductor Profiling," IEEE Trans. Electron Devices ED-22, 265 (1975).

8. H. M. Macksey, "Ohmic Contacts for GaAs Power FETs," Proceedings of 1976 North American Conference on GaAs and Related Compounds, to be published.

9. H. M. Macksey, R. L. Adams, D. N. McQuiddy, D. W. Shaw, and W. R. Wisseman, "Dependence of GaAs Power MESFET Microwave Performance on Device and Material Parameters," IEEE Trans. Electron Devices ED-24, 113 (1977).

10. H. M. Macksey, T. G. Blocker, and F. H. Doerbeck, "GaAs Power FETs with Electron Beam Defined Gates," Electron. Lett., to be published.

11. H. Q. Tserng, V. Sokolov, H. M. Macksey, and W. R. Wisseman, "Microwave Power GaAs FET Amplifiers," IEEE Trans. Microwave Theory Tech. MTT-24, 936 (1976).

12. K. S. Sann, "The Measurement of Near-Carrier Noise in Microwave Amplifiers," IEEE Trans. Microwave Theory Tech. MTT-10, 761 (1968).

APPENDIX

DEVICE DELIVERIES

Table A1

GaAs FETs Delivered to NRL, March 1977*

Device Number	Good Cells	I_{dss} (mA)	g_m (mmho)	V_P (V)	Gain (dB) P_{in}=15 dBm V_{ds}=5V, $V_{gs}\cong 0$	Maximum Output Power (W) 4 dB Gain V_{ds}=8V, V_{gs}=-2V	Maximum Output Power (W) 5 dB Gain V_{ds}=8V, $V_{gs}\cong$-2V	Power-Added Efficiency (%) (5 dB Gain)
76B1-18BIE #1	3	470	118	5.9	7.0	1.02	0.85	32.5
2	4	490	117	~7	7.2	1.07	0.91	31.1
3	1	460	124	5.4	7.1	0.98	0.87	34.6
4	4	460	120	6.0	7.3	1.12	1.05	35.1
5	2	460	122	5.5	7.4	1.00	0.89	31.3
6	2	480	120	~6	7.8	1.16	1.12	38.2
7	3	440	122	~5	7.0	1.05	0.93	37.3
8	2,3	960	240	6.2	7.1	1.55	1.12	21.0
9	1.2	860	220	~5.7	6.0	1.70	1.20	20.2
76B1-18BIE #10	3.4	940	240	~6	8.0	2.00	1.74	31.7

*GaAs FET Data at 10 GHz

Table A2

GaAs Read Diodes Delivered to NRL, January 1977

Diode Number	Operating Voltage (V)	Output Power (W)	Efficiency (%)	Frequency (GHz)
C27B-6001	51.0	3.0	25.0	9.2
C27B-6002	57.8	3.1	24.1	8.9
C27B-6003	59.0	3.2	22.3	9.1
C27B-6004	57.4	3.4	23.2	9.0
C27B-6005	56.4	3.2	24.4	9.0
C27B-6006	57.6	3.9	24.8	9.0
C27B-6007	56.9	3.4	25.3	9.0
C27B-6008	57.9	3.3	24.5	9.0
C27B-6009	57.6	3.2	24.1	9.0
C27B-6010	55.0	3.2	27.4	9.1

Table A3

GaAs FETs Delivered to NRL, January 1977*

Device Number	Good Cells	Gate Finger Width (μm)	Gain (dB) P_{out} = 15 dBm V_{ds} = 5V	Max. P_{out} with 6 dB Gain V_{ds} = 8V (mW)	Max. P_{out} with 4 dB Gain V_{ds} = 8V (mW)	Power Added Efficiency (4 dB Gain) (%)	Gate Voltage (V)
17623-116B1b#1	1	200	6.6	460	690	32.5	-3.5
17623-116B1b#2	1	200	6.6	500	720	36.3	-3.1
17623-116B1b#3	1	200	6.6	500	720	31.1	-3.2
17623-116B1b#V1	1	200	7.4	540	740	36.0	-3.3
17623-116B1b#1X	1	200	6.8	550	740	34.2	-3.1
A94B1Vb#1	1	200	6.8	630	690	34.7	-1.0
76B1-25A1b#1	1	200	6.8	400	690	32.5	-2.6
76B1-25A1b#2**	1,3	150	8.4	1,350	1,510	33.5	-2.0
76B1-38B1b#1	1,2	150	7.5	810	1,150	36.6	-1.9
76B1-38B1b#111	3,4	150	6.8	525	1,200	29.2	-3.1

*GaAs FET Data at 10 GHz

**Data taken at 8 GHz

Table A4

GaAs Read Diodes Delivered to NRL, March 1977

Diode Number	Operating Voltage (V)	Output Power (W)	Efficiency (%)	Frequency (GHz)
C27B-6011	51.0	3.2	22.5	8.7
C27B-6012	58.3	3.3	23.4	9.0
C27B-6013	59.1	3.4	21.8	9.1
C27B-6014	59.5	3.7	23.0	8.9
C27B-6018	55.5	3.2	26.5	9.3
C62B-6020	44.7	3.4	17.0	10.3
C87B-6021	53.5	4.0	19.6	8.9
C87B-6023	45.3	4.1	19.9	8.5
C51B-6031	51.9	4.1	16.3	9.5
C51B-6033	52.0	4.2	20.2	9.4
C51B-6034	55.9	3.8	16.3	9.4

N00173-76-C-0384
Item 0001AC (A002)

DISTRIBUTION LIST FOR SEMI-ANNUAL REPORT ON CONTRACT NO. N00173-76-C-0384 (TI)

X-BAND SOLID STATE MODULE PROGRAM

	# OF COPIES
Defense Documentation Center Building 5, Cameron Station Alexandria, Virginia 22314	12
Advisory Group on Electron Devices 201 Varick Street, 9th Floor New York, New York 10014	3
Commanding Officer Naval Research Laboratory Attn: Library, Code 2627 Washington, D.C. 20375	6
Commanding Officer Naval Research Laboratory Attn: Mr. Eliot D. Cohen, Code 5211 Washington, D.C. 20375	50
Commanding Officer Naval Research Laboratory Attn: Dr. John E. Davey, Code 5210 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. Albert Brodzinsky, Code 5200 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Dr. Kenneth J. Sleger, Code 5211S Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. Richard C. VanWagoner, Code 5258 Washington, D.C. 20375	10
Commanding Officer Naval Research Laboratory Attn: Mr. William A. Douglas, Code 5334 Washington, D.C. 20375	1

	# OF COPIES
Commanding Officer Naval Research Laboratory Attn: Mr. Ronald Chilluffo, Code 5733B Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. John M. Hardley, Code 5733 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. K. Reed Gleason, Code 5211G Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. A. C. Macpherson, Code 5210.2 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. B. C. Dodson, Jr., Code 7903 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. R. Neidert, Code 5258 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. H. Willing, Code 5258 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Dr. P. DeSantis, Code 5258 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Dr. B. Spielman, Code 5259 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. T. apRhys, Code 5366 Washington, D.C. 20375	1

	# OF COPIES
Commanding Officer Naval Research Laboratory Attn: Mr. J. T. McCullough, Code 5709 Washington, D.C. 20375	1
Commanding Officer Naval Research Laboratory Attn: Mr. David Townsend, Code 5435 Washington, D.C. 20375	1
Commander Naval Air Systems Command Attn: Mr. Robert C. Thyberg, AIR 360-C Washington, D.C. 20361	5
Commander Naval Air Systems Command Attn: Mr. Andrew Glista, Jr., AIR 52022 Washington, D.C. 20361	10
Commander Naval Air Systems Command Attn: Mr. Harry Bauer, AIR 533314 Washington, D.C. 20375	1
Office of Naval Research Attn: Dr. J. O. Dinmock, Code 427 800 N. Quincy Street Arlington, Virginia 22217	1
Office of Naval Research Attn: Mr. M. N. Yoder, Code 427 800 N. Quincy Street Arlington, Virginia 22217	1
Commander Naval Electronic Systems Command Attn: Mr. L. W. Sumney, Code 3042 Washington, D.C. 20360	1
Commander Naval Electronic Systems Command Attn: Mr. R. A. Wade, Code 3042-1 Washington, D.C. 20360	1
Director Naval Weapons Center Attn: Mr. Joseph A. Mosko, Code 35203 China Lake, California 93555	1

	# OF COPIES
Commander Naval Electronics Laboratory Center Attn: Library 297 Catalina Boulevard San Diego, California 92152	1
Commander Naval Ships Engineering Center Attn: Code 6157D Prince Georges Center Hyattsville, Maryland 20782	1
Commander Naval Electronic Systems Command Engineering Office U. S. Naval Station Attn: Mr. M. W. McLerran Norfolk, Virginia 23511	1
Commander U. S. Army Electronics Command Attn: DRSEL-TL-IC, Mr. V. G. Gelnovatch Fort Monmouth, New Jersey 07703	1
Commanding Officer Harry Diamond Laboratories Advanced Research Laboratory Attn: AMXDO-RAA, Mr. H. W. A. Gerlach Washington, D.C. 20438	1
Commander Air Force Avionics Laboratory Attn: Mr. R. L. Remski Wright Patterson Air Force Base, Ohio 45433	1
Commander Air Force Avionics Laboratory Attn: Mr. T. Kemerley Wright Patterson Air Force Base, Ohio 45433	1
Commander Air Force Avionics Laboratory Attn: Mr. C. Huang Wright Patterson Air Force Base, Ohio 45433	1
Commander Rome Air Development Center Attn: Mr. R. H. Chilton Griffiss Air Force Base, New York 13441	1

	# OF COPIES
Director of Defense Research and Engineering Attn: Tech Library Room 3E1039, The Pentagon Washington, D.C. 20301	1
Defense Advanced Research Projects Agency Attn: Dr. Richard Reynolds 1400 Wilson Boulevard Arlington, Virginia 22309	1
Director U. S. Army Ballistic Missile Defense Advanced Technology Center Attn: ATC-R, Mr. G. Jones P. O. Box 1500 Huntsville, Alabama 35807	1
Dr. N. Walter Cox Georgia Institute of Technology Engineering Experiment Station Atlanta, Georgia 30332	1
Dr. George I. Haddad University of Michigan Electrical Engineering Department Ann Arbor, Michigan 48104	1
Dr. Walter Ku Cornell University Electrical Engineering Department Phillips Hall Ithaca, New York 14850	1
Aertech Industries 825 Stewart Drive Sunnyvale, California 94086	1
Communication Transistor Corporation Attn: Dr. W. H. Weisenberger 301 Industrial Way San Carlos, California 95051	1
Hewlett-Packard Company, Inc. Attn: Dr. B. Berson HPA Division 640 Page Mill Road Palo Alto, California 94304	1
Hewlett-Packard Company, Inc. Attn: Dr. C. Liechti 1501 Page Mill Road Palo Alto, California 94304	1

	# OF COPIES
Hughes Aircraft Company Hughes Research Laboratories Attn: Dr. G. Ladd 301 Malibu Canyon Road Malibu, California 90265	1
Raytheon Company Research Division Attn: Dr. Robert Pucel 28 Seyon Street Waltham, Massachusetts 02154	1
Varian Associates Attn: Dr. B. Fank 611 Hansen Way Palo Alto, California 94304	1
Watkins-Johnson Company Attn: Mr. Martin G. Walker 3333 Hillview Avenue Palo Alto, California 94304	1
Westinghouse Research Laboratories Attn: Dr. H. C. Nathanson Beulah Road Pittsburgh, Pennsylvania 15235	1
Mr. H. Velsor Veda, Inc. 1911 Jefferson Davis Highway Arlington, Virginia 22202	1
Westinghouse Electric Corporation Defense and Electronic Systems Center Attn: Dr. Thomas M. Eppinger Box 746, M.S. 339 Baltimore, Maryland 21203	1
Alpha Industries, Inc. Attn: Mr. Martin Reid 20 Sylvan Road Woburn, Massachusetts 01801	1
Hughes Aircraft Company Attn: Dr. T. Midford Torrance Research Center 3100 West Lomita Blvd Torrance, California 90509	1

	# OF COPIES
Rockwell International Science Center Attn: Dr. Dan Ch'en 1049 Camino Dos Rios (P.O. Box 1085) Thousand Oaks, California 91360	1
RCA Laboratories David Sarnoff Research Center Attn: Dr. Y. Narayan Princeton, New Jersey 08540	1
Dr. Jeffrey Frey Cornell University Electrical Engineering Department Phillips Hall Ithaca, New York 14850	1
The Narda Microwave Corporation Attn: Dr. John Eisenberg 2900 Coronado Drive Santa Clara, California 95051	1