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InSb MIS DEVELOPMENT

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FINAL REPORT

Contract No. N00173-77-C-0022

Prepared by:
J.C. Kim and J.M. Swab

Sponsored by:
Naval Electronic Systems Command

Directed by:
Naval Research Laboratory

Program Project No. 62762N
XF54583004

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)

InSb MIS DEVELOPMENT,

5. TYPE OF REPORT & PERIOD COVERED

Final Report,
Dec 1976 - April 1977,

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)

Dr. J. C. Kim and J. M. Swab

8. CONTRACT OR GRANT NUMBER(s)

N00173-77-C-0022 new

9. PERFORMING ORGANIZATION NAME AND ADDRESS

General Electric Company
Optoelectronic Systems Operation
Electronics Park, Bldg. #3-201
Syracuse, New York 13201

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

62762N
XF 54583004
F54583

11. CONTROLLING OFFICE NAME AND ADDRESS

Naval Electronic Systems Command N00039
Code 3042, L. W. Sumney
Washington, D. C. 20360

12. REPORT DATE

August 1977

13. NUMBER OF PAGES

19

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

Naval Research Laboratory N00173
Code 5262, Dr. W. D. Baker
Washington, D. C. 20375

12 27p.

15. SECURITY CLASS. (of this report)

Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

A. Approved for public release, distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Indium Antimonide, Infrared Detectors, MIS Technology

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

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microsec.

microns

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General Electric Company
Optoelectronic Systems Operation
Electronic Systems Division
Syracuse, New York 13201

FOREWORD

This Final Technical Report was prepared by the Optoelectronic Systems Operation of Electronic Systems Division, General Electric Company, Syracuse, New York under Contract No. N00173-77-C-0022, entitled "InSb MIS Development".

This effort was sponsored by Naval Electronic Systems Command, and directed by Naval Research Laboratory with Dr. W. D. Baker as the Project Monitor. The work was performed for the period December 1976 through April 1977.

Mr. L. A. Branaman, Manager of Engineering, was the Program Administrator. Dr. J. C. Kim, the Principal Investigator, directed the overall program. Other contributors to the program were W. E. Davern, D. Colangelo, T. Shepelavy, V. F. Meikleham, E. M. Littebrant, and R. J. Schultz.

The report was submitted and distributed in August 1977.

ABSTRACT

Further improvement on both line and two-dimensional InSb CID arrays has been made. The sensitivity of line arrays has been improved by using thin-gate oxide and low-doping substrate materials, which reduce the input line capacitance. The co-planar two-dimensional array structure also has been further improved.

Effort on a low-noise amplifier has been carried out and performance of the JFET preamplifier was much better than that of the MOSFET. The NETD for a line array was found to be $0.11^{o}K$ using a JFET preamp and $0.5^{o}K$ using a MOSFET. The measurement was made with a narrow spectral filter of 3.6 to 4.0 μm, f/3.25 lens system, and a 500 μsec integration time.

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I. INTRODUCTION

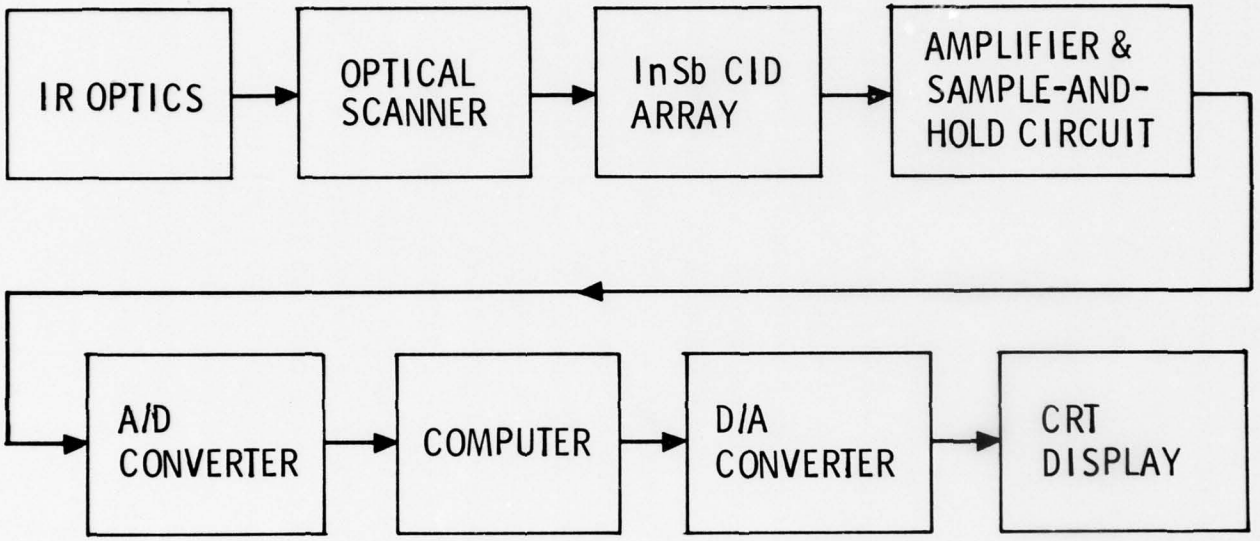
This final report covers the continuous development of InSb MIS and CID arrays. The improvement of line array performance is discussed in Section II and further progress of two-dimensional arrays is described in Section III. The work of p-diffused planar InSb P-N junction diodes is presented in Section IV. In Section V, an effort of low noise amplifier is described.

II. IMPROVEMENT OF LINE ARRAY PERFORMANCE

The sensitivity of the line array structure has been improved by reducing the input capacitance. This was accomplished by fabricating the arrays with thin-gate oxide and low-doping substrate materials. The evaluation of these improved arrays has been carried out by displaying two-dimensional image pictures with a scanning mirror, as discussed in the previous report[1].

Figure 1 shows the block diagram of the imaging setup with a line array. The sampled output video signal was further processed by a computer, which then simply removed background-generated non-uniformities (pattern noise). The first line of background video information from a constant background scene as a reference line was stored in the computer, and that reference line information was then subtracted from each of the subsequent lines of image video information. This removed, effectively, the background-generated dc level. However, no correction was made for responsivity variation between array elements. The computer-processed image of a man's face was displayed on a CRT and is shown in Figure 2. It is shown that the eyebrows, nose and cheeks appear darker, an indication of slightly lower temperature than that of the face. It is also interesting to note that the eyes appear slightly brighter than the surrounding face, indicating that their temperature is slightly warmer than the surrounding face, a fact which is attributed to the exposed veins in the eyes. From these results it is estimated that InSb CID line arrays presently are capable of resolving a few tenths of a degree (^{o}K) difference in temperature. However, it is shown later in the report that further improvement in sensitivity can be expected by the use of JFET rather than MOSFET preamplifiers so that a noise equivalent temperature difference (NETD) of less than one tenth of a degree can be achieved.

Fig. 1. BLOCK DIAGRAM OF InSb CID LINE ARRAY IMAGING SETUP



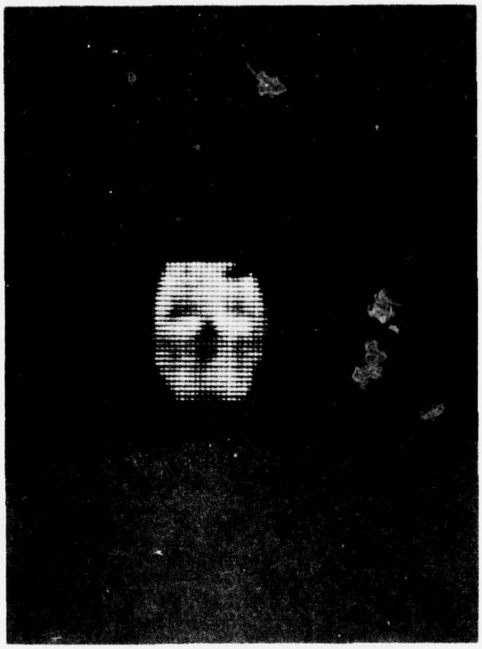


Figure 2. Image Display of a Man's Face Produced With an Improved 32-element InSb CID Line Array.

II. FURTHER PROGRESS OF TWO-DIMENSIONAL ARRAYS

It has been reported[1] that the co-planar two-dimensional array structure has been the best as far as the operation was concerned. In the parallel gate overlapping structure, the top gate oxide was twice as thick as the bottom gate oxide so that it was difficult to create the deep potential wells necessary for effective charge transfer. Reducing the thickness of the top gate oxide to overcome this problem often caused shorting between the two overlapped gates, or it increased the coupling capacitance which, in turn, contributed to pattern noise. The co-planar arrays, on the other hand, result in a more uniform output video signal, with much less pattern noise. The charge transfer capability is also much better, probably because deep potential wells are more readily created. Further improvement in this co-planar array structure has been made.

Figure 3 shows the co-planar overlapping array structure. The gold layer bridging the two gates was used to provide continuity over the steep step. However, it obscured some of the infrared collection area and thus reduced the optical sensitivity. Therefore, an effort was made to eliminate the opaque gold metal layer.

Instead of using opaque gold over the step, a semitransparent metal layer such as Cr was employed. This is the same metal layer used for the second gate; in fact, the metallization can be done at the same time, both on the gate and over the step. A typical photomicrograph of a complete array structure is shown in Figure 4. As one can see, the whitish lines are metallized gold bus line interconnections and there is no opaque gold layer over the step in the overlapped region of the resolution elements. Evaluation of this array geometry indicates that charge transfer does occur properly between the row and column gates in each resolution element. This means that the co-planar overlapping array structures can be fabricated without the use of a gold layer over the step of two gates, resulting in simpler array structure and fewer processing steps.

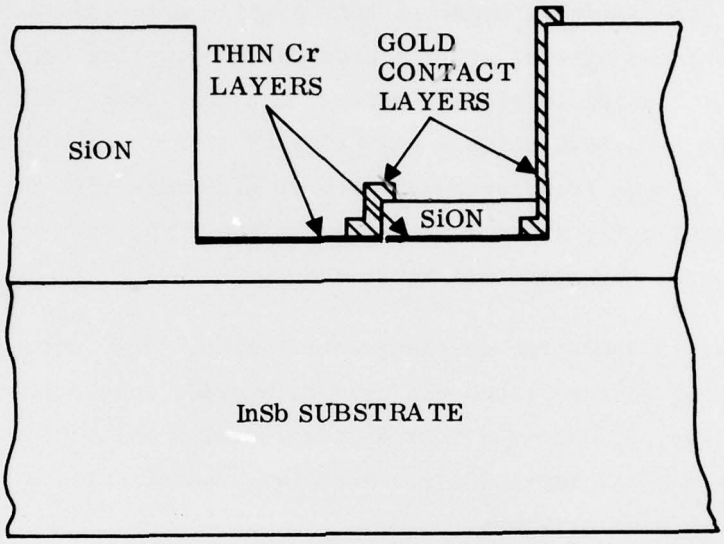


Figure 3. Co-Planar Two-Dimensional Array Structure

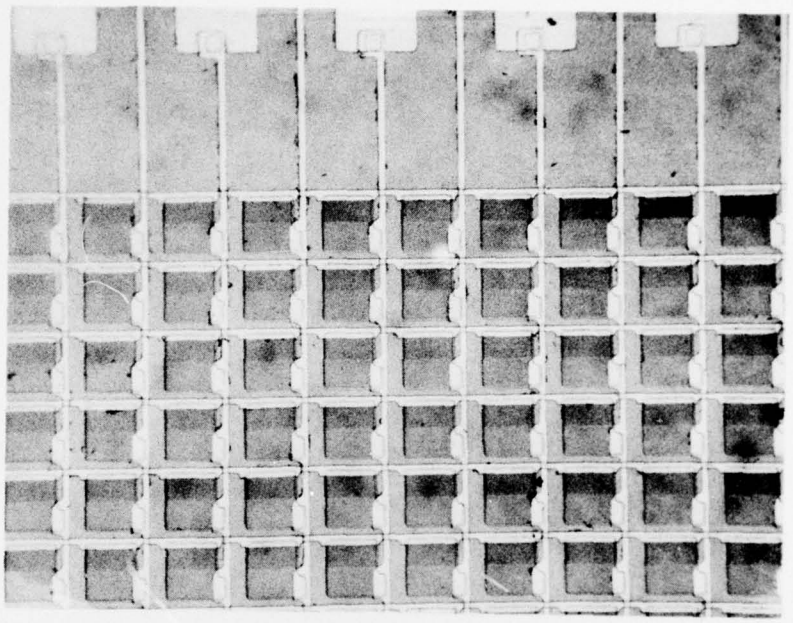


Figure 4. Photomicrograph of the Co-planar Array Fabricated Without Using Gold Layer Between the Row and Column Gates.

III. P-DIFFUSED PLANAR InSb P-N JUNCTION DIODES

Based on the results of the co-planar array structure effort, it is felt that an even better array structure can be built using a p-coupled island between the two gates in each resolution element. Since both gates can again be placed on the same thin gate oxide, the ability to create deep potential wells is to be expected. Also, in this array structure, because the row and column gates are physically separated, the capacitive coupling betwen them, and, therefore, pattern noise, should be minimized. The operation of this array should be simpler because the row and column gates have the same oxide thickness and so they can have the same operating bias voltage.

Because of these potential advantages, an effort has been made to develop a planar p-diffused p-n junction on InSb. Planar InSb p-n junction diodes have been fabricated successfully. First, p-type doping was diffused through selected areas and then the surface was cleaned after removing the mask oxide and a SiON dielectric layer was deposited just as it is done for MIS structures. Small contact windows were then opened on the diffused areas, and a metal layer for contact leads was deposited. The typical performance of such a planar p-n junction diode is shown in Figure 5, exhibiting an excellent I-V characterisitic. The reverse leakage current is very low, but the breakdown voltage is small.

An effort has been made to fabricate two-dimensional array structures with a p-coupled bridge between the row and column gates using the diffusion process referred to above. For this work, a 1x16, one column two-dimensional array structure was used. It has proven difficult to fabricate a p-coupled CID two-dimensional area array with the diffusion process. Diffusion was made through small windows, but the diffusion through these windows caused problems of selective diffusion; the diffusion occurred under the mask oxide in the periphery of the open windows. It appears that diffusion takes place underneath the open windows. Thus, it was difficult to fabricate the p-coupled CID two-dimensional area arrays with the diffusion process.

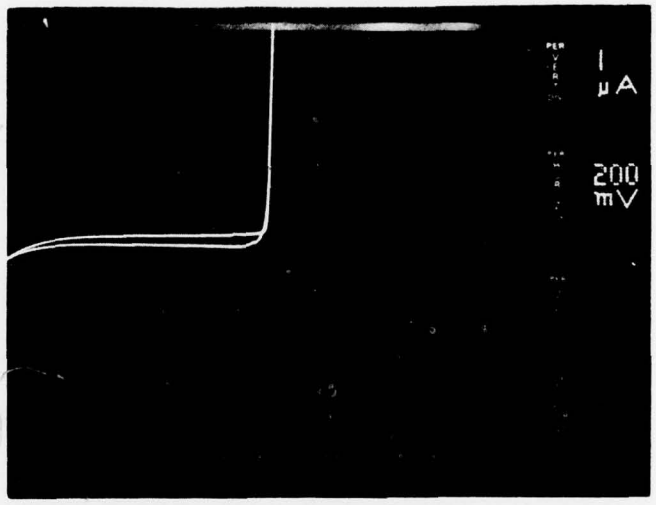


Figure 5. I-V Characteristic of an InSb Planar P-N Junction Diode.

However, an attractive technique for forming p-coupling islands is by means of ion implantation, which has been developed elsewhere. An effort, therefore, will be made to use this technique for the fabrication of p-coupled CID area arrays.

V. LOW NOISE AMPLIFIER

A low noise linear amplifier is required to amplify the video signal from the enable line to a suitable level so that it can be DC restored and sampled. This amplifier must have high input impedance so that when the stored charge is transferred to the amplifier input, a reasonable voltage will be generated and will not leak off before the output voltage is sampled. An input impedance of 10^7 ohms is sufficient to prevent appreciable leakage, but the input capacitance must be minimized so that it will not add appreciably to the total shunt capacitance of the enable line.

The amplifier also must have high dynamic range, since the noise level is expected to be equivalent to 10^2 charge carriers and the maximum stored charge can be 10^7 carriers. This 100 dB dynamic range extends from about 1 microvolt to 100 millivolts on the enable line. In addition to this, the amplifier must tolerate and rapidly recover from the injection pulse which is on the order of 2 volts.

Currently, a p-channel, enhancement mode MOSFET is used inside the dewar as an on-chip amplifier. An on-chip amplifier is desirable since it reduces the shunt capacitance and the FET works better at $77^{\circ}K$ than at room temperature. Unfortunately, even at $77^{\circ}K$ the MOSFET has poor noise performance. The 1/f noise corner frequency is about 100 KHz, which makes 1/f noise significant at high sampling frequencies and dominant at low sampling frequencies.

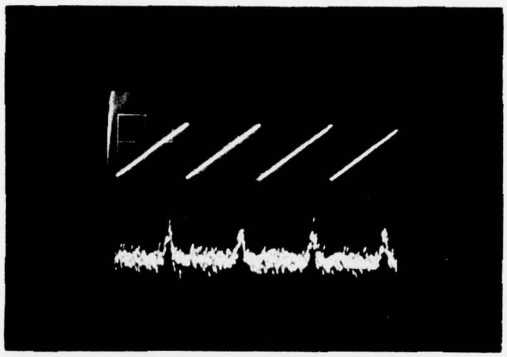
Several discrete semiconductor devices were considered to replace the on-chip MOSFET (on the scanner). The device was to be mounted off-chip but within the dewar, and operated at low temperature ($>77^{\circ}K$). Bipolar transistors were not considered because of the high input impedance required, and the low operating temperature. An rf type of FET would seem to be the appropriate device, combining low noise, low input capacitance and good low temperature performance. Unfortunately, common rf MOSFETs and JFETs are of the n-channel type and available p-channel devices have poor noise performance. A p-channel device would be preferred in a common source amplifier configuration for this application because the large positive-going

injection pulse would tend to cut the device off rather than drive it into saturation. However, the increased noise is too great a penalty to pay so a "garden variety" n-channel JFET was mounted in a dewar for testing.

The JFET preamplifier in the dewar can be used in a number of configurations including common source, source follower, or as the input part of a cascode stage. The normal common source configuration has two disadvantages; first, the large injection pulse tends to drive the JFET into saturation and secondly, the gain of the stage tends to amplify the feedback capacitance and increase the total input capacitance. The cascode configuration keeps the input capacitance down, but the injection pulse is still a problem unless a differential input is used, which in turn, adds more noise. The source follower has a gain of less than one, but the effective gate-to-source capacitance is reduced, thus reducing the input capacitance somewhat.

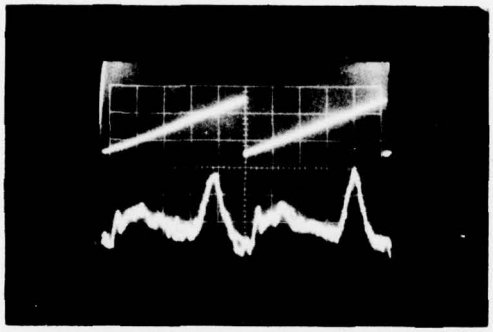
A comparison of the on-chip MOSFET and off-chip JFET preamplifier was made using both of them in source follower configurations with similar following amplifier stages. The lower trace of Figure 6 shows the MOSFET sample-and-hold video output from a single element of a line array, as the array is mechanically scanned across a test target with a $3^{o}K$ temperature difference. The test target was 3 two-watt resistors mounted on a large circuit board. Both the resistors and the circuit board had thermistors mounted on them for temperature measurement. The resistance of the thermistors was measured with a digital multimeter and then the temperature difference was determined by looking up the resistance valves in a table. The upper trace shows the scan mirror drive waveform.

Figure 7 shows similar video from the same array element using the JFET, except that in this case the test target temperature difference was $1.75^{o}K$. In both cases the integration time was 500 μsec, which requires a sampling rate of 68 KHz for the 33-element line array. The low sampling frequency is well into the 1/f noise region of the MOSFET; therefore, the JFET provides a much better signal-to-noise ratio.



A266 Element #24
MOSFET Preamplifier
$\Delta T = 3^{o}K$
10 m Sec/Div

Figure 6. Scan and video waveforms while scanning a test target with a $3^{o}K$ temperature difference and using the MOSFET preamplifier.



A266 Element #24
JFET Preamplifier
$\Delta T = 1.75^{o}K$
5 m Sec/Div

Figure 7. Scan and video waveforms while scanning a test target with a $1.75^{o}K$ temperature difference and using the JFET preamplifier.

The NETD for this array element was measured using the resistor test target. The signal voltage was measured from the oscilloscope trace shown in Figures 6 and 7, and the noise voltage was measured by turning off the mechanical scanner and measuring the voltage with an rms voltmeter. The NETD was found to be $0.11^{o}K$ using the JFET preamp and $0.5^{o}K$ using the MOSFET preamp. The $0.11^{o}K$ NETD is near BLIP for this f/3.25 lens system with a 3.6 to 4.0 μm filter and a 500 μsec integration time.

The test circuit used with the JFET preamplifier is shown in Figure 8. It can be considered a source follower driving a common gate amplifier or a differential amplifier with one JFET inside and one outside the dewar. This circuit handles the injection pulse gracefully, by simply letting it cut Q2 off, and the JFET sources present the cable with both a source and load impedance near its characteristic impedance. The penalty for these features is an increase in the noise voltage. The equivalent amplifier input noise voltage is

$$V_N = \sqrt{\frac{8K\,\Delta f}{3}\left(\frac{T_1}{g_{m1}} + \frac{T_2}{g_{m2}}\right)}$$

where g_{m1} and T_1 are the transconductance and temperature of Q1, while g_{m2} and T_2 refer to JFET Q2. It is convenient to determine the equivalent noise input resistance so that the amplifier noise can easily be compared with the selection switch thermal noise. The equivalent noise input resistance, R_n, for this amplifier is

$$R_n = \frac{2}{3T_r}\left(\frac{T_1}{g_{m1}} + \frac{T_2}{g_{m2}}\right)$$

where T_r is the temperature of R_n. When T_r, T_1 and T_2 are all equal to room temperature, the calculated equivalent noise input resistance is 400 ohms. A value of 550 ohms was measured, using a 50 KHz to 1 MHz bandpass.

In normal operation the dewar is cooled to $77^{o}K$, and T_1 is reduced to nearly $77^{o}K$ while T_2 stays at about $300^{o}K$. For comparison with the select switch noise, the equivalent noise input resistance temperature is

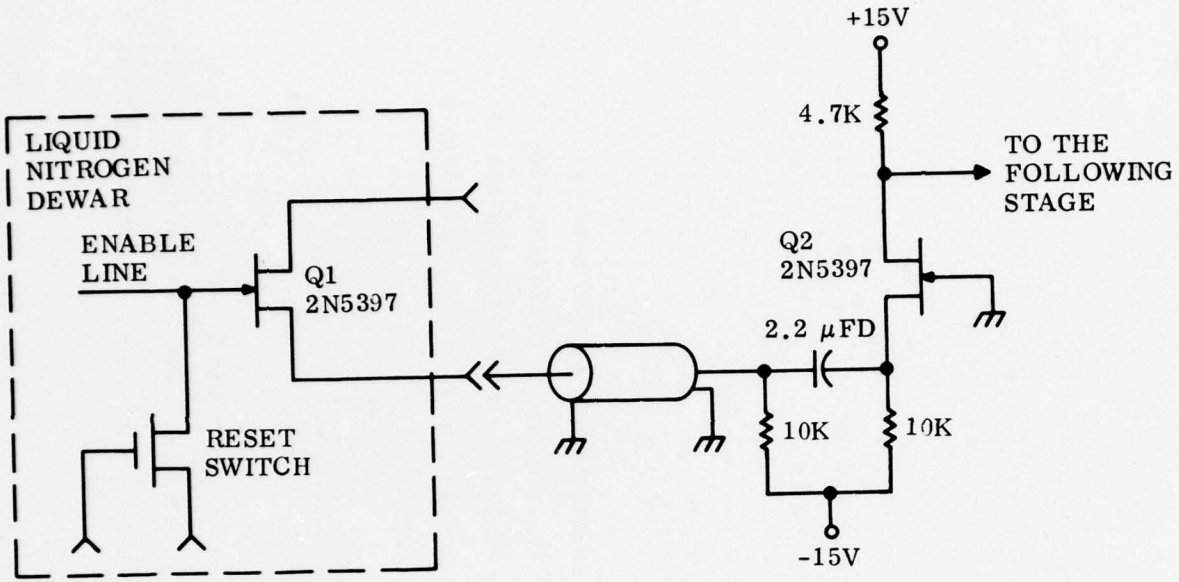


Figure 8. A Schematic of JFET Test Amplifier

$77^{o}K$. The transconductance of the cooled JFET, g_{m1}, was determined by measuring the output impedance of the source follower circuit. Using these values, R_n was calculated to be 890 ohms. The short circuit noise voltage could only be measured by shorting the amplifier input with the reset switch, so the measured equivalent noise resistance of 2400 ohms is the sum of the reset switch resistance and the amplifier equivalent noise input resistance. The reset switch is assumed to contribute about half of the measured noise resistance.

A complete video amplifier circuit, shown in Figure 9, was designed by adding a DC restorer, a sample and hold amplifier, and a cable driver to the linear amplifier. This circuitry was designed to preserve the noise and dynamic range performance of the linear amplifier. The preamp bias resistors and the low pass filters are mounted on plug-in assemblies so that they can be easily changed. The JFET preamp in the dewar dissipates about 12 milliwatts as it is presently biased.

The video amplifier was tested with the dewar mounted JFET preamp at room temperature. First, just the linear amplifier was tested with the digital clock and circuits disables and the output measured at the test point ahead of the DC restorer and sample and hold circuits. The measured equivalent noise input resistance and the dynamic range of the linear amplifier were 700 Ω and 91 dB respectively. Then, the complete amplifier was tested with the digital circuits operating normally and both the DC restorer and the sample and hold in operation. The equivalent noise input resistance was found to be 2300 Ω with a dynamic range of 89 dB.

The complete amplifier has been operated with a 33 element line array, but the performance of the amplifier has not been measured independently with the dewar mounted JFET cooled to $77^{o}K$. However, the noise voltage does go down when the dewar is cooled, indicating an improvement in both noise and dynamic range performance. Shot noise is clearly evident when amplifier is used with a 33 element line array.

Better JFETs have been ordered for evaluation. It is assumed that the equivalent noise input resistance can be reduced by about a factor of

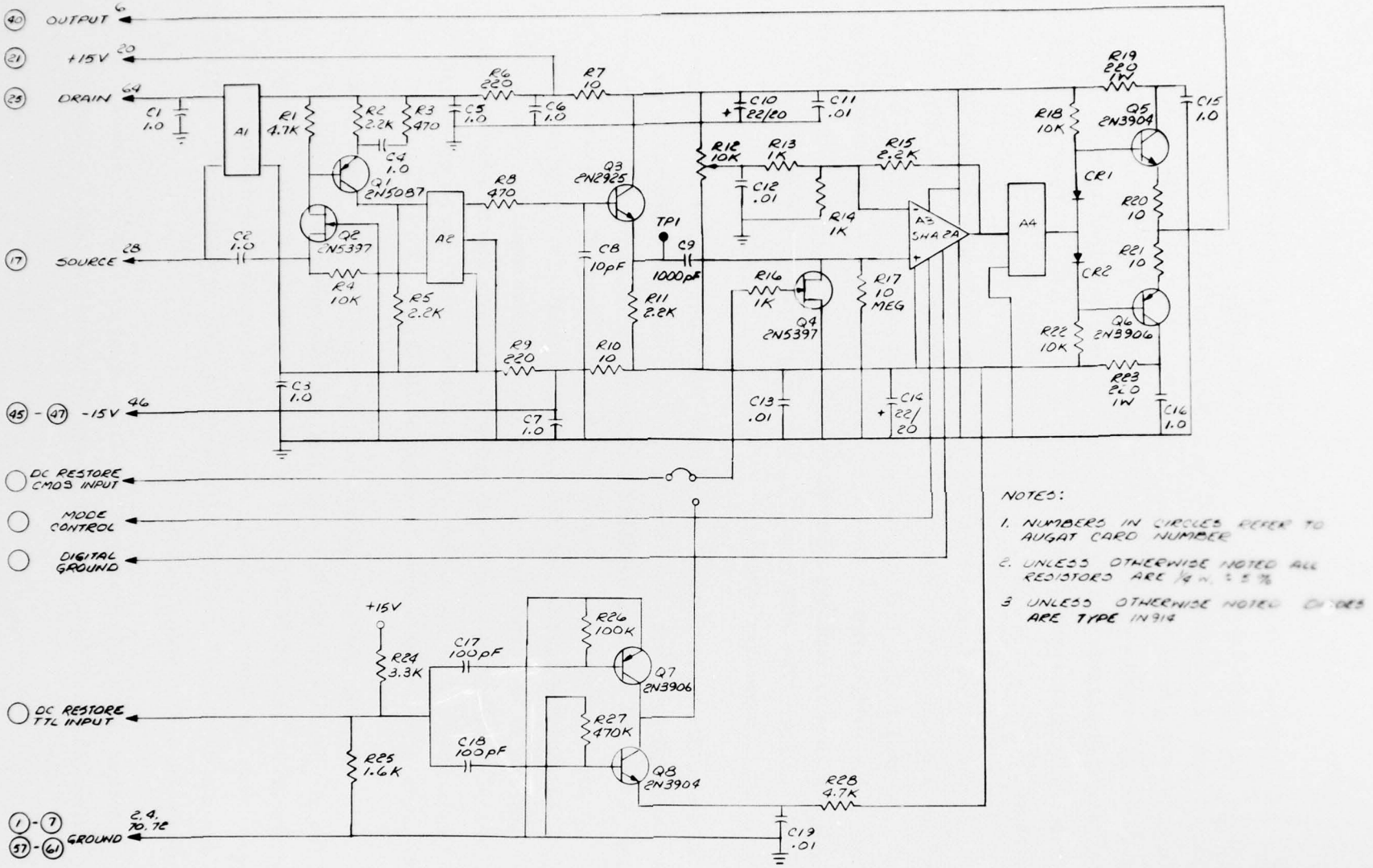


Figure 9. New Amplifier (Single-Ended) and Sample-and-Hold Circuits.

two, using these devices in the same amplifier configuration. Other configurations also will be tested in follow-on efforts, for improved performance.

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