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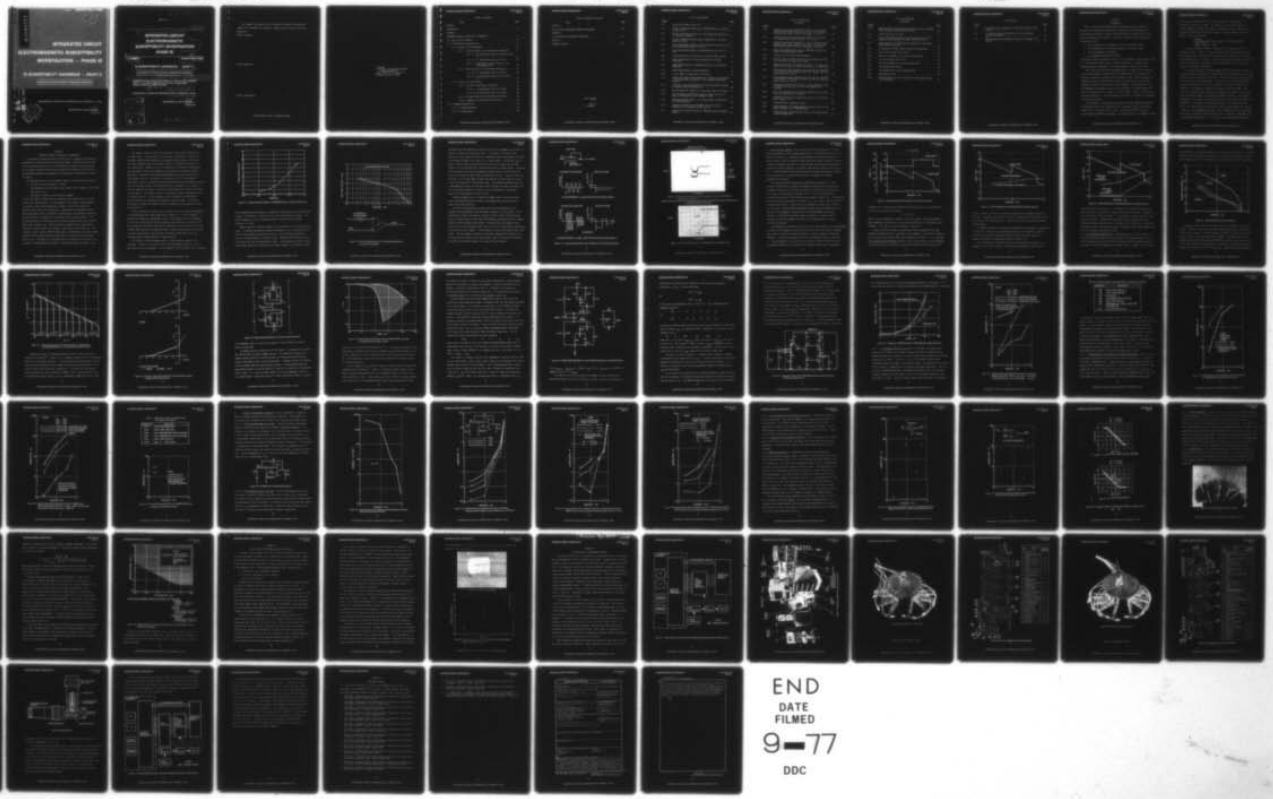

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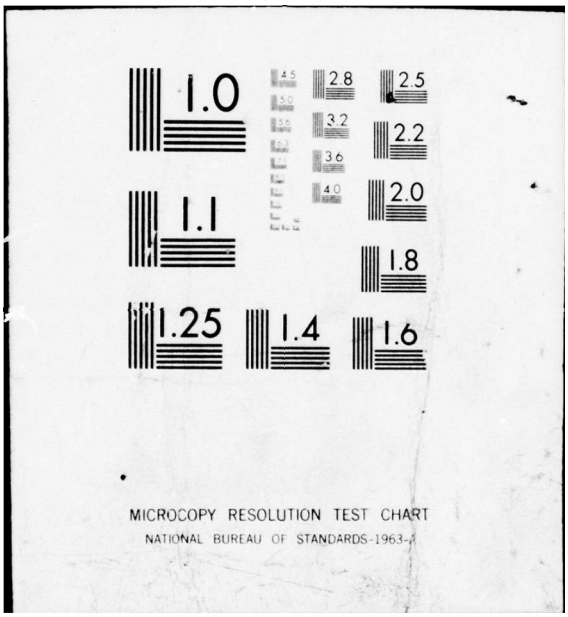
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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION — PHASE III

IC SUSCEPTIBILITY HANDBOOK — DRAFT 2

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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION. PHASE III.

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IC SUSCEPTIBILITY HANDBOOK — DRAFT 2

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SUBMITTED TO THE CONTRACTING OFFICER, U.S. NAVAL SURFACE WEAPONS CENTER — DAHLGREN LABORATORY, DAHLGREN, VIRGINIA, 22448
UNDER CONTRACT NO. N60921-76-C-A030

(15) ____ (18) NSWC/DL

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Commander
U. S. Naval Surface Weapons Center
Dahlgren Laboratory
Attn: DF-56 (V. G. Puglielli)
Dahlgren, Virginia 22448

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CHAPTER 1

INTRODUCTION

The U. S. Naval Surface Weapons Center - Dahlgren Laboratory (NSWC-DL) is developing the technology base required to enhance the cost-effectiveness of preventing Navy electronic systems from being vulnerable to the effects of high power electromagnetic environments. The overall program includes development of technology bases on:

a. the susceptibility of integrated circuits to microwave signals,

b. the susceptibility of discrete components to microwave signals,

c. the electromagnetic environment,

d. electromagnetic pickup and shielding.

The McDonnell Douglas Astronautics Company - East (MDAC-EAST), under contract to the U. S. Naval Surface Weapons Center - Dahlgren Laboratory, is developing the technology base on integrated circuit electromagnetic susceptibility (ICES).

Each of the technology bases developed under this program will be integrated into an electromagnetic vulnerability (EMV) handbook which may be used by the designers of electronic systems for the prevention of EMV. The EMV handbook will include all areas of the EMV problem, and the ICES program will issue an ICES Handbook for eventual inclusion into the EMV handbook. The EMV examples in the ICES Handbook are intended to show how to use the data in the ICES Handbook and are not a substitute for the methods in the EMV handbook. There is no pick-up or shielding information in the ICES Handbook except what is included in the examples to make them realistic.

This document is the second draft version of the ICES Handbook and contains the technology base on the susceptibility of integrated circuits to microwave signals which is available at this time. A previous draft[15] was issued on 4 June 1976 and was publicly reviewed. This revised version is intended to refine

the previously established format, and test information significance. New susceptibility data are included. Future versions of the ICES Handbook will include additional susceptibility data as it becomes available. Comments and suggestions regarding the format and contents of the ICES Handbook are invited. Comments should be directed to:

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An overall hardening approach is proposed for the prevention of EMV in electronic systems. Figure 1-1 shows the task flow that would occur during the EMV hardening design of electronic systems designated to operate in a high power electromagnetic (EM) environment. From the system design viewpoint, the definition of the EM environment is dictated by the operating envelope of the system and imposed by contractual requirements.

For a given environment, the EMV hardening designer must perform a worst case EM pickup analysis to determine the maximum amount of microwave power that will be picked up by the system cables and wiring. The EM pickup analysis requires the EM coupling section of the EMV handbook. The designer must then determine whether unacceptable effects are likely to be produced in the system's components by referring to the component susceptibility section of the EMC handbook. EMV analysis is accomplished by comparing the expected pickup levels to the minimum power required to produce the unacceptable component responses. The hardening requirement is the ratio of expected pickup power to the component susceptibility threshold. If the hardening requirement value (dB) is less than 0 dB, many dollars in system cost can be saved by not worrying further about EMV. However, if the worst case hardening requirement value is greater than 0 dB, the designer must select a candidate hardening approach which is dependent on the value (dB) of the hardening requirement. If the worst case hardening requirement value is

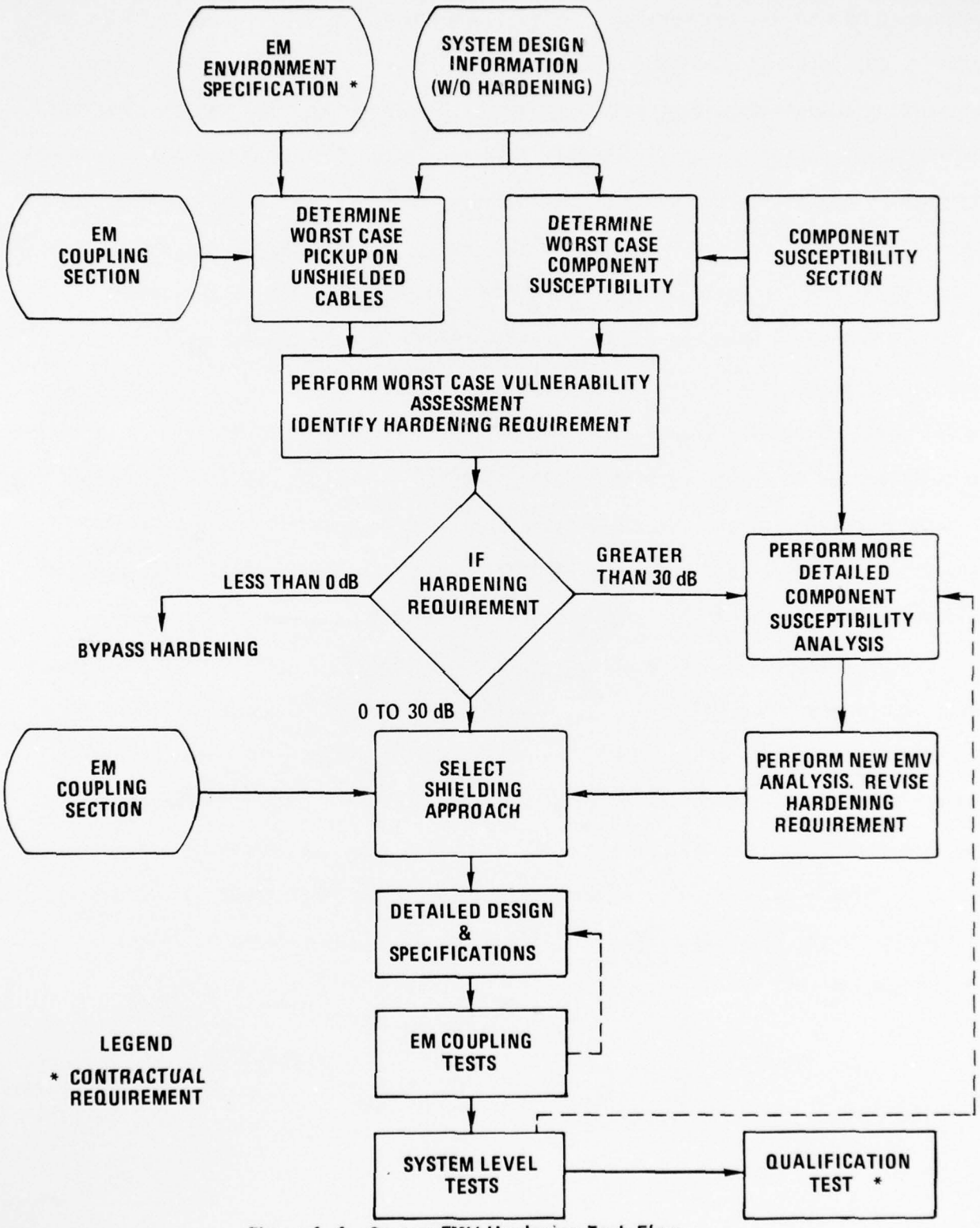


Figure 1–1. System EMV Hardening Task Flow

between 0 and 30 dB, the most cost-effective hardening approach appears to be to provide the required shielding, rather than delve into the more costly approach of performing component susceptibility analyses. There is nothing "magic" about the 30 dB value and further shielding effectiveness information on practical shielding techniques may revise the value in the future. However, past experience has shown that the 30 dB value is a realistic breakpoint in the hardening requirement in terms of economy and achievement. In the future, if the costs of performing detailed component analyses can be made low enough, a more precise vulnerability assessment may eliminate the need for such arbitrary divisions. If the worst case hardening requirement value is greater than 30 dB, at this time it is probably cost-effective to investigate the implications of the worst case assumptions by performing a component susceptibility analysis. The component susceptibility analysis is accomplished using the integrated circuit (IC) susceptibility and the discrete component susceptibility sections of the EMV handbook.

It is anticipated that most system hardening designers will employ an iterative approach by examining different techniques based upon refining the estimates of component susceptibility and pickup values until a satisfactory system hardening approach has been developed. It is also likely that hardening requirements will be developed for individual portions of systems to minimize hardening overdesign in less vulnerable portions. At this point, the designer proceeds to the detailed hardening design task which involves such items as gasket selection, filter specification, etc.

CHAPTER 2

INTEGRATED CIRCUIT SUSCEPTIBILITY INFORMATION

This chapter provides predictions of worst case IC susceptibility based upon measurements of device samples and theoretical models. Predictions are provided for many different classes of ICs, and susceptibility models are provided which may be used to estimate the worst case susceptibility thresholds for many others. The predicted susceptibility parameter is minimum power incident upon the leads of the device.

The susceptibility of ICs to microwave signals is divided into three factors:

a. The class of device (digital or linear),

b. The parameters of the microwave signal (power level, frequency, pulse width, pulse rate, etc.),

c. The degree of severity (interference or damage).

In the first factor, linear devices are generally more susceptible to microwave signals than digital devices. For the purpose of this chapter, digital devices are defined as those devices designed to operate in one or two states only (possibly three states for some devices). Linear devices are defined as those devices designed to have a continuous or smooth output. The operating conditions of the device also influence the IC susceptibility to microwave signals. The operating conditions for digital devices include the output states (low or high), power supply voltages, etc., while the operating conditions for linear devices include bias levels, offset null settings, circuit gain, input levels, etc. For instance, a typical device (7400 TTL NAND gate) is susceptible to microwave signals injected into the output when the output state is low, but not when the output state is high. The opposite is true when the RF is injected into the input (i.e., the gate is susceptible when the output is high, but not when the output is low).

The degree of severity implies the magnitude of the problem caused by the microwave signal. For the purpose of this chapter, interference is defined as a microwave-induced effect which does not produce permanent damage to the device. The effect disappears when the microwave stimulus is removed and the device is fully operational. Damage to the IC is divided into two categories, degradation and catastrophic failure, which depend on the severity of the damage suffered. Degradation is defined as limited permanent damage to the device resulting from the microwave stimulus. The device is operational only in a limited manner. Catastrophic failure is defined as extensive permanent damage to the device resulting from the microwave stimulus so that the device will not operate in any manner. As might be expected, more power is required to cause damage than simply to interfere with the device. For example, figure 2-1 illustrates a typical interference plot of a 7400 digital IC. As the microwave stimulus increases, the interference effect increases as evidenced by the increase in output voltage. If the power continued to increase, the 7400 would reach the damage level and some part of the chip would fail.

Actual susceptibility data as shown in figure 2-1 carry an implicit dependence on the measurement test fixture (described in Chapter 4). For this handbook it is desirable to remove such dependences so that a more universal result is produced. In most cases of empirically derived susceptibility predictions, a measure of the power absorbed by the device under test has been used as an estimate of the minimum incident power required to produce the effect. Where an absorbed power measurement had large uncertainties, other estimates of minimum incident power were used including actual incident power for a tuned condition.

The frequency of the microwave signal is a very important susceptibility parameter. Figure 2-2 is a typical plot of the interference effects in a 741 op amp (linear IC) versus frequency. As the frequency of the microwave signal increases,

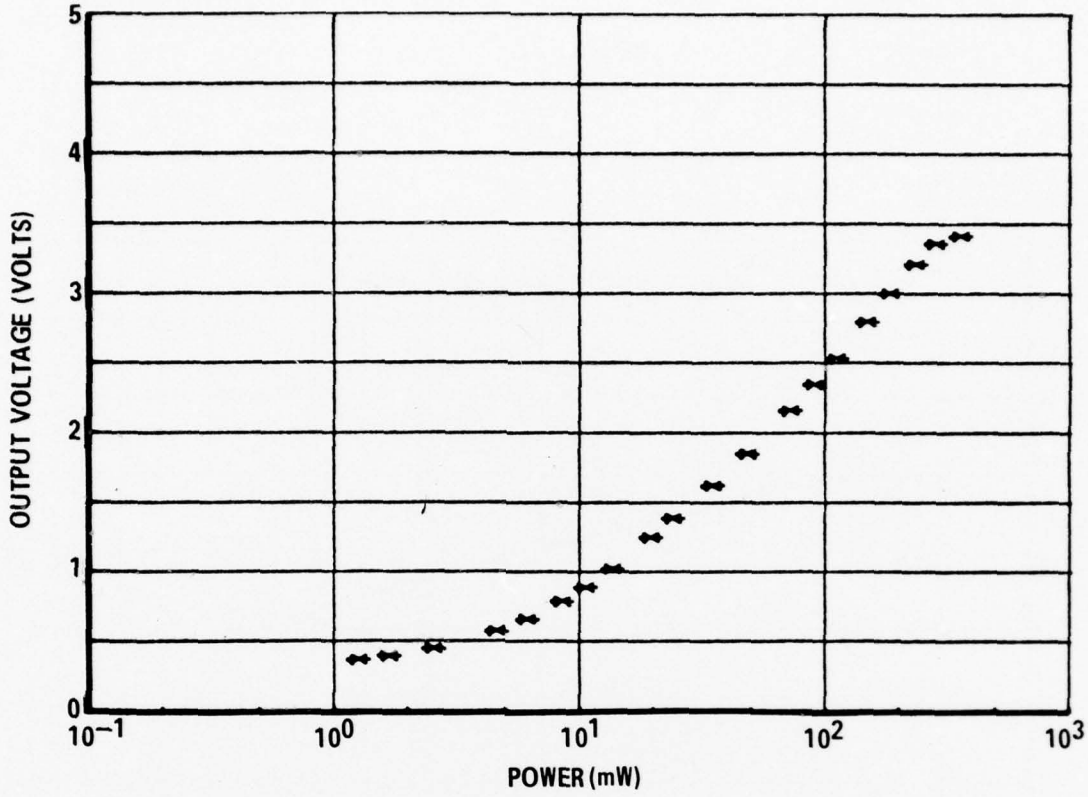


Figure 2–1. Typical Interference Effects on a 7400 NAND Gate As a Function of Power Level

the interference effect decreases as evidenced by the decrease in the input offset voltage. This behavior is typical for most linear and digital ICs tested. The lowest frequency at which ICs have been tested is 220 MHz and the highest frequency is 9.1 GHz.

Another important microwave parameter is the modulation of the interfering RF signal. In general the mechanism causing interference in ICs is rectification of the RF in the assorted pn junctions of the IC. This rectification mechanism results in envelope detection of the RF signal. Therefore the interfering signal is basically the same as the modulating signal. Pulse modulation of the RF causes pulsed video interfering signals while CW signals produce a dc interfering signal.

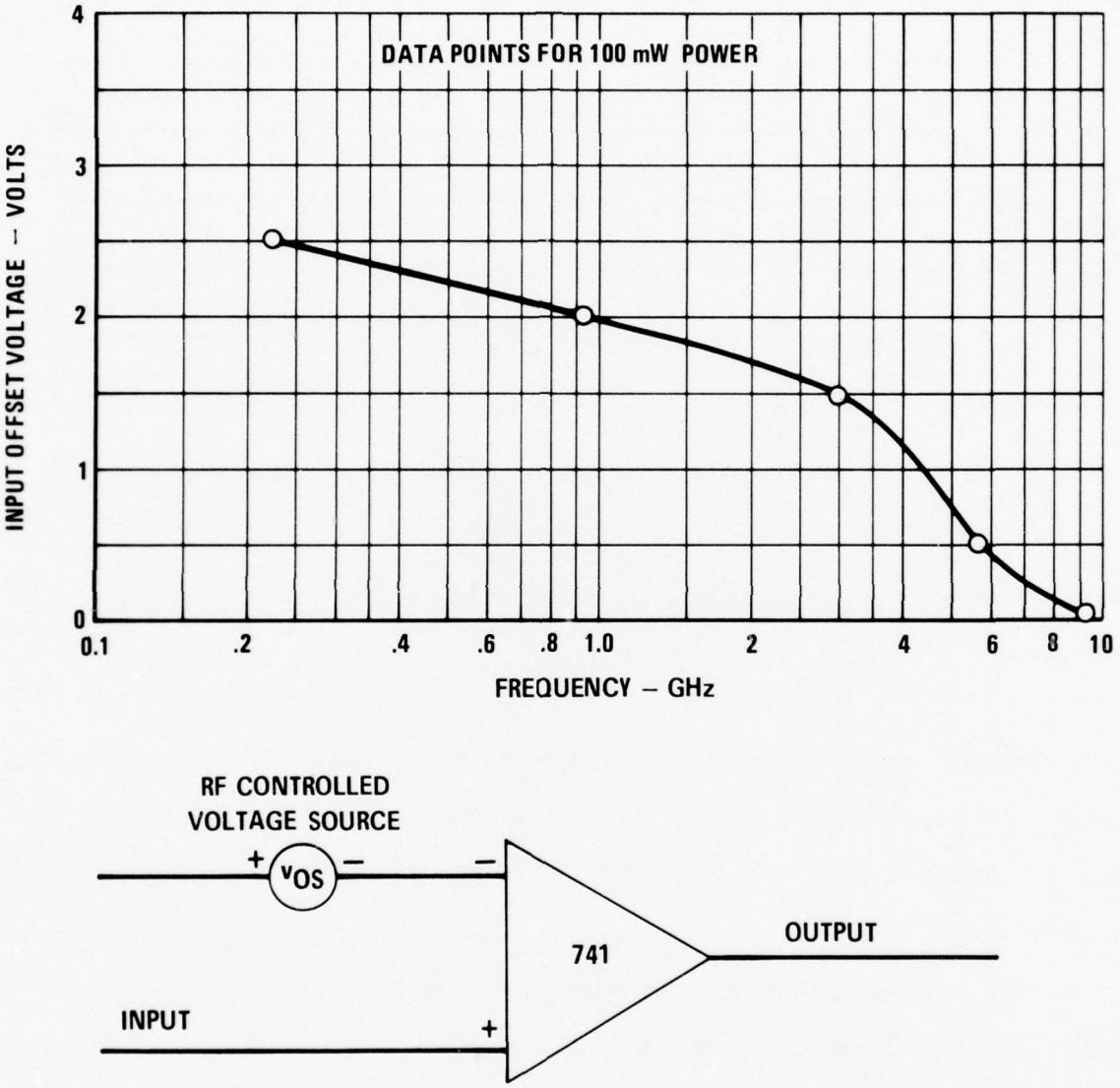
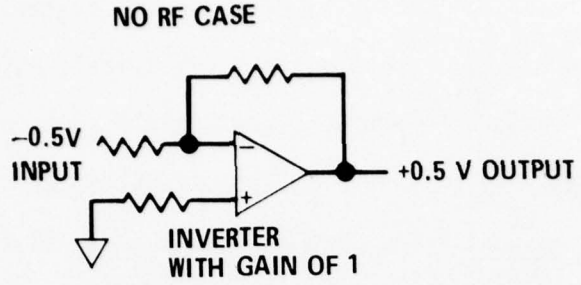


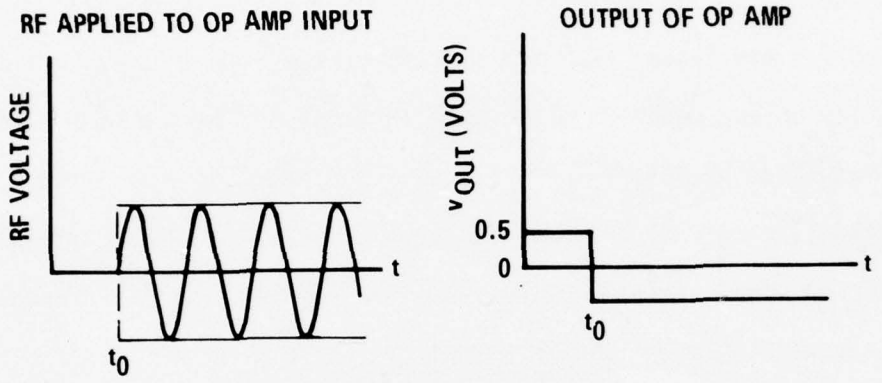
Figure 2–2 Typical Interference Effects on a 741 Operational Amplifier As a Function of Frequency

The effect that the interfering signal has on the circuit depends on the circuit's ability to process the interfering signal. For example, a CW signal, which rectifies in a pn junction to form a dc interfering signal, would cause a dc offset to the output voltage of the circuit, as in figure 2-3(a). A pulsed RF signal as shown in figure 2-3(b) would interfere with the op amp in such a way that the output of the op amp would have a pulsed offset from its nominal output. The output of the op amp can not follow the modulating pulses exactly if the rise and fall times of the pulses are faster than the specified slew rate. Figure 2-4 shows the the case of a 741 op amp under RF whose slew rate was not fast enough to respond to the pulse-modulated RF interference signal. The detected interference pulse on a 7400 NAND gate (figure 2-5) has much faster rise and fall times, consistent with the high switching speed of this device, and the 7400 exhibits interference exactly like the modulation of the RF signal.

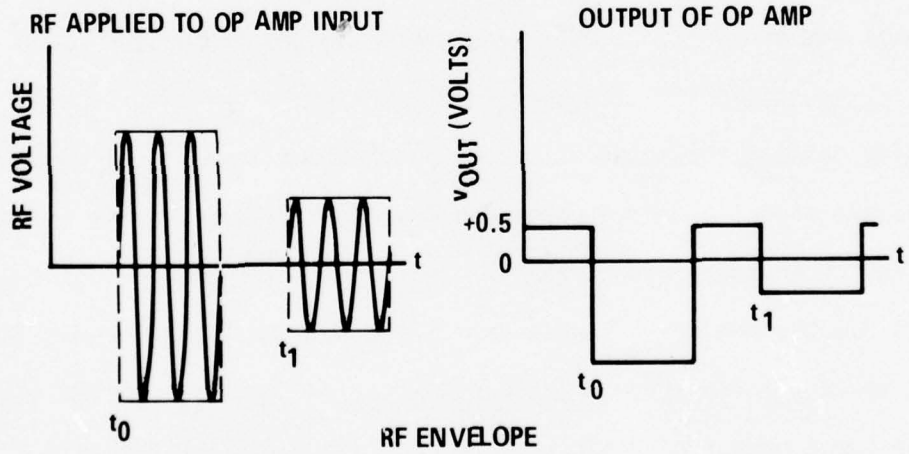
Another parameter which is important at damage levels is the pulse width. Since the damage mechanisms are thermal, they depend upon total pulse energy (power level times duration).

All tests and measurements were made utilizing the integrated circuit susceptibility measurement system described in Chapter 4 of this report. The IC susceptibility testing consisted of injection into one lead of the device under test a microwave signal of known power and frequency, and measuring the RF-induced changes in device voltages and currents. The tests cover the frequency range from 0.22 to 9.1 GHz and power levels from 10 μW to 4 kW (interference, degradation, and failure testing included). A large number of devices were tested at many power levels. The large number of devices is required to determine the spread in the device-to-device variation; while various power levels are required to determine the effects on the device under a wide range of EM environments.





a) CW RF BEGINNING AT t_0 AND ITS EFFECT ON THE OP AMP'S OUTPUT



b) PULSED RF PULSES AT t_0 AND t_1 AND ITS EFFECT ON THE OP AMP'S OUTPUT

Figure 2–3. Typical Interference Effects Due to Modulation of the Interfering RF Signal

INVERTER OPERATION
RF INTO INVERTING INPUT PORT

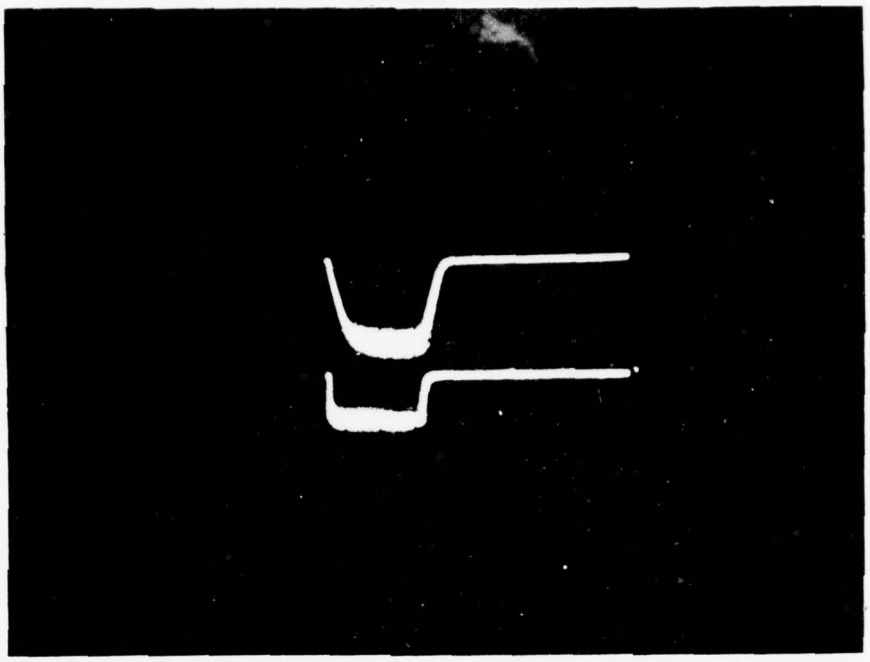


Figure 2–4. Pulse Interference Effects on 741 Op Amp Due to Fast Rise Time RF Pulse and Slower Rise Time of 741

RF INTO INPUT PORT, OUTPUT HIGH

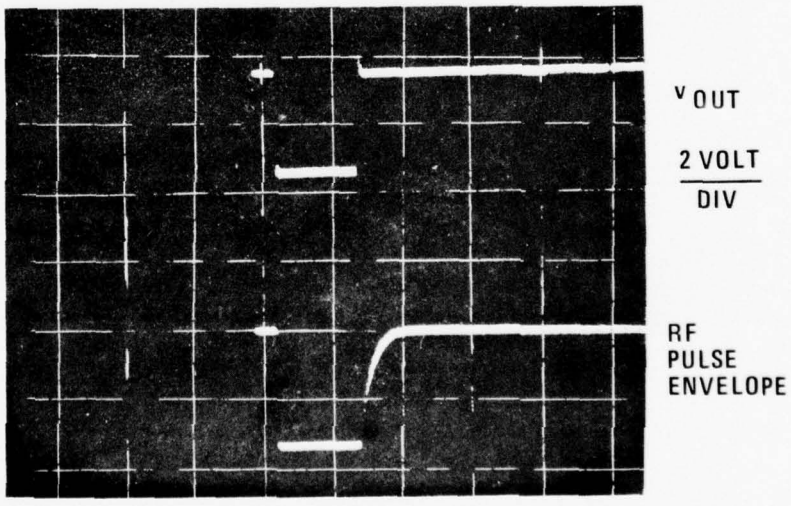


Figure 2–5. Pulse Interference Effects on 7400 NAND Gate with Fast Rise Time

2.1 How to Use This Chapter - This chapter has two main subdivisions: IC interference susceptibility and IC damage susceptibility. Each subdivision covers both digital and linear ICs. Predictions based on empirical results are presented in these sections as well as analytical models which can be used for devices for which no data are presently available. The available data have been sorted into general groups by the types of devices: TTL devices, CMOS devices, bipolar linear devices, etc. A composite graph has been made for each type showing the worst case susceptibility profile (i.e., minimum RF power level vs frequency for selected susceptibility criteria).

The user must define the applicable susceptibility criterion (i.e., the component response which is deemed unacceptable) based upon his own application. In general, the user will find that such factors as noise immunity, allowable bit error rates, normal component tolerances, etc., will set the susceptibility criterion while bearing in mind that the more stringent criteria (e.g., no detectable response) lead to low susceptibility values (i.e., low RF power level for the onset of excessive RF effects). Excessively low susceptibility values imply the need for excessively large shielding and protection values which can become quite costly. The use of this handbook in conjunction with the EMV handbook should assist designers in determining the proper amount of shielding. The example which follows shows how this handbook may be used in the determination of system shielding requirements.

Electromagnetic environment levels (in terms of power density, P_d) are determined according to the stockpile to end of service life cycle of the system of interest, and a table or graph of required test levels is usually included in contractual documents. A possible environment level for this example is shown in figure 2-6.

An unshielded wire or cable will pick up various amounts of power from this environment according to such variables as frequency, aspect angle, terminating

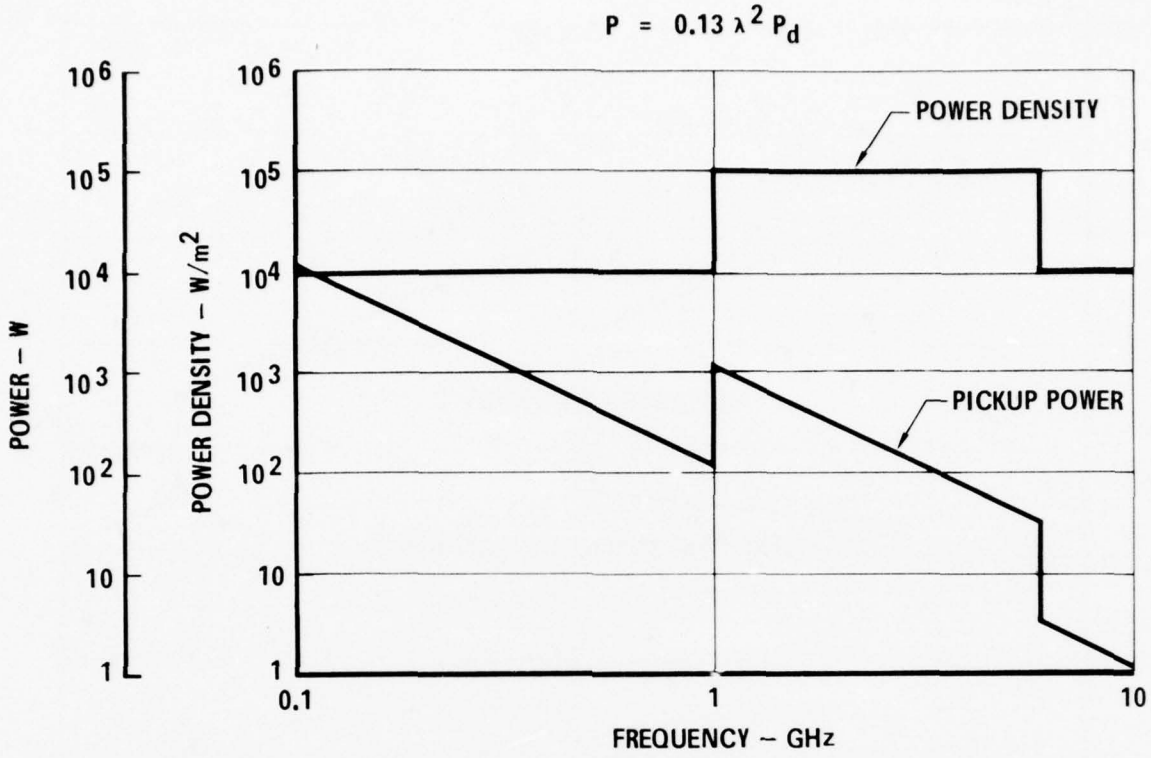


Figure 2–6. Sample Calculation of Pickup Power From Given Power Density

impedance, etc. One method for determining the maximum amount an unshielded wire will pick up is given by the formula:

$$P = 0.13 \lambda^2 P_d$$

where λ is the wavelength of interest. From this formula, the maximum amount of power expected on system wiring in the given environment can be calculated at each frequency. This result is also illustrated in figure 2-6.

Figures 2-7 and 2-8 repeat the maximum power levels expected but also add component information which is available in this handbook. In particular, figure 2-7 shows the worst case burnout levels ever observed for IC burnout. It is clear that, in the absence of any shielding, burnout is quite possible across a large frequency range, and some sort of protection in the form of shielding (either enclosure or

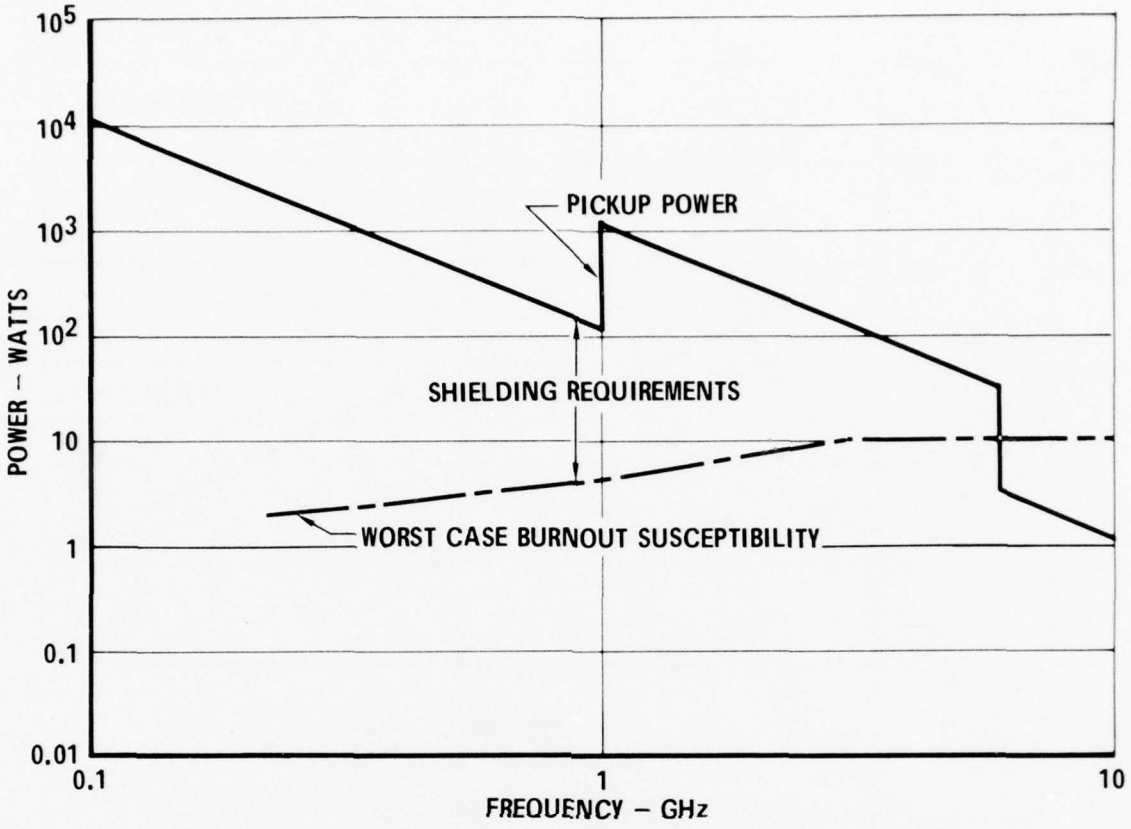


Figure 2–7. Sample Determination of Shielding Required for Burnout Protection

cable, or both) or filtering is required to guarantee that component burnout will not occur. The amount of protection required is indicated by the separation of the two curves on this logarithmic plot. Figure 2-8 shows similar results for interference effects.

The degree of overall system protection required for this example is summarized in figure 2-9. Many options are available to meet such requirements including: splitting the shielding requirements between enclosure and cable shielding, filtering, isolation of particularly sensitive circuits, etc.

This example shows one method for applying the predictions available in this handbook to a realistic situation. The predictions presented in the following

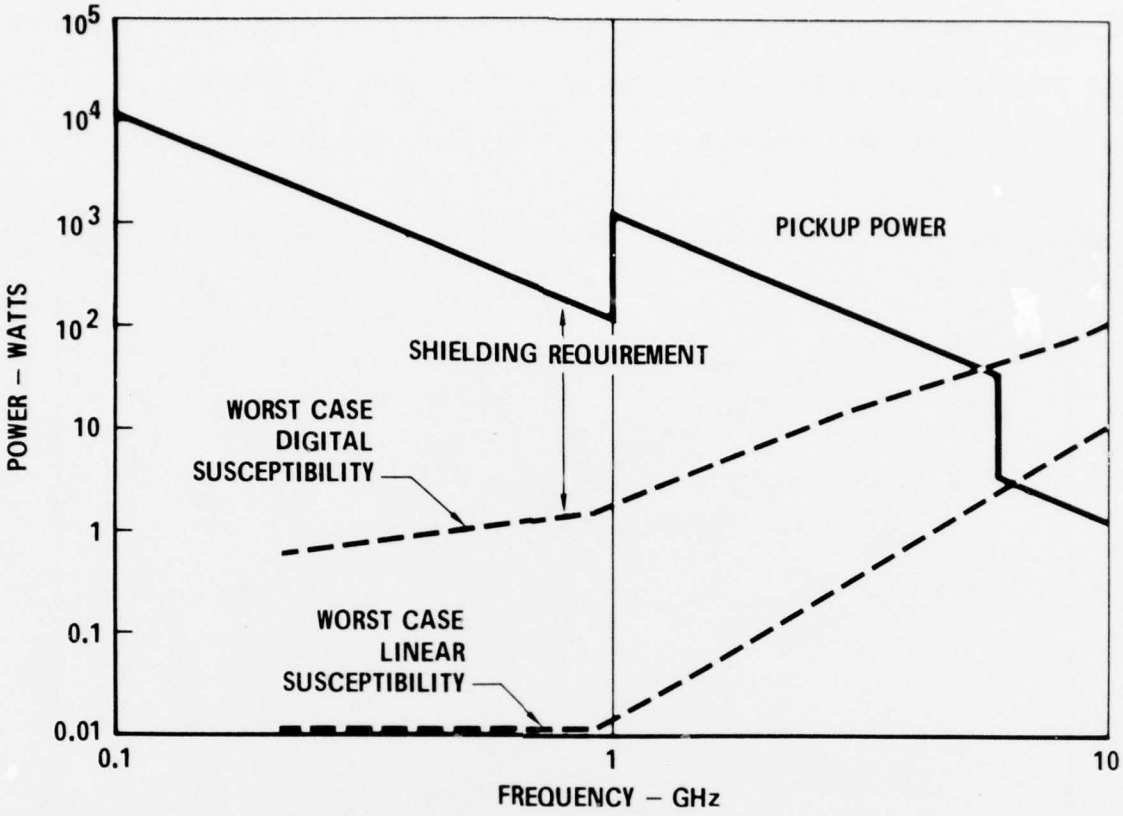


Figure 2–8. Sample Determination of Shielding Required for *Interference* Protection

sections are worst case values, i.e., thousands of ICs have been tested and the data from the most susceptible are used as the worst case estimates. Because of the vast quantity of data available, it is impossible to tabulate the data without publishing volumes. Therefore the susceptibility data have been subdivided according to device classifications, TTL, CMOS, bipolar linear, etc., and plotted. The power absorbed in the device provides an estimate of the minimum incident power and is also used for the modeling effort.

2.2 IC Interference Susceptibility - Interference occurs in ICs as a result of rectified microwave signals which cause changes in the expected output of the IC. If the microwave signal enters the IC at the output port, the observed effect on the output is directly related to the microwave signal. However, if the microwave

signal enters the IC through some other port, then the rectified signal is processed through the device circuitry and the change in the output is indirectly related to the microwave signal with the intermediate circuitry determining the relationship.

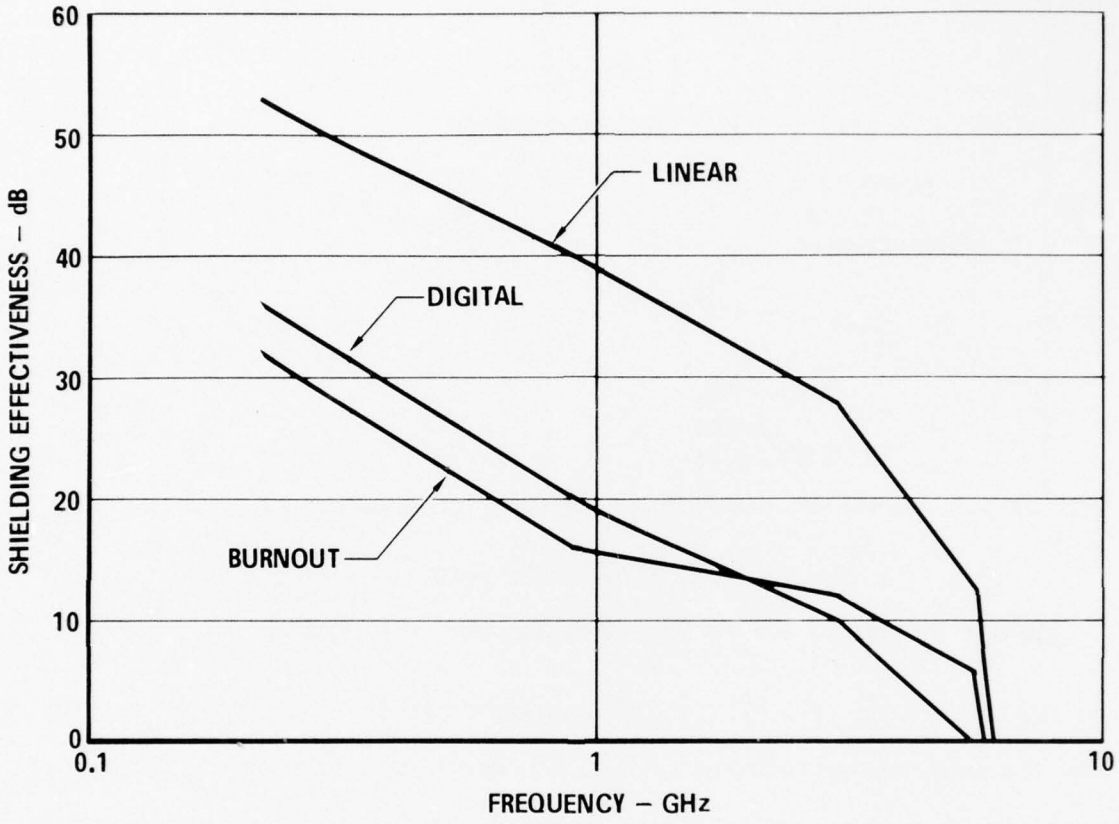


Figure 2–9. Sample Requirements for System Shielding

Two general classifications of ICs are used in this handbook: digital and linear. The digital class was subdivided by manufacturing process into bipolar, of which the TTL family is the more prevalent, and CMOS, of which the B-series is the first series to have an industry-wide standard. The linear class was subdivided by device type into operational amplifiers (op amps), which make up most of the linear category, voltage regulators, comparators, and miscellaneous linear devices to pick up the rest of the linear class. General models are presented to

analyze devices which are not represented in the test data. Some devices may be similar enough to tested devices so that their susceptibility levels may be approximated using the tested devices.

2.2.1 Digital IC RF Interference - The digital devices covered in this section include bipolar and CMOS. The TTL 54/74 family of digital devices is emphasized as it is the single largest digital family. CMOS is separated because of its different manufacturing process.

2.2.1.1 Bipolar Digital IC RF Interference Information - This section describes bipolar digital device interference. A general model is presented, and worst case interference predictions are shown. For digital circuits the main susceptibility parameters are the output voltage and the total device current.

2.2.1.1.1 RF Interference Model for Bipolar Digital ICs - Models of RF effects in integrated circuits are intended to extend the predictability of IC susceptibility to devices not represented in the measured data section. The models basically account for the effects of RF interference in pn junctions, and the ramifications of the location of affected junctions must be studied for individual circuit layouts. To aid this study, the models are compatible with large circuit analysis codes and an example of adapting the models for use with SPICE is presented. No attempt has been made to model the RF transmission characteristics of IC chips, but a worst case analysis based upon a parametric variation approach is recommended. Specific examples will make this concept clearer.

The simplest RF model needed to perform RF interference analysis is for the isolated pn junctions (i.e., not part of an active transistor junction). Examples of such junctions include diodes, isolation junctions, and parasitic junctions associated with diffused resistors. Figure 2-10 is a schematic diagram of a model which will produce a piecewise linear approximation to actual pn junction response under RF stimulus. D1 represents the normal, unperturbed junction characteristic

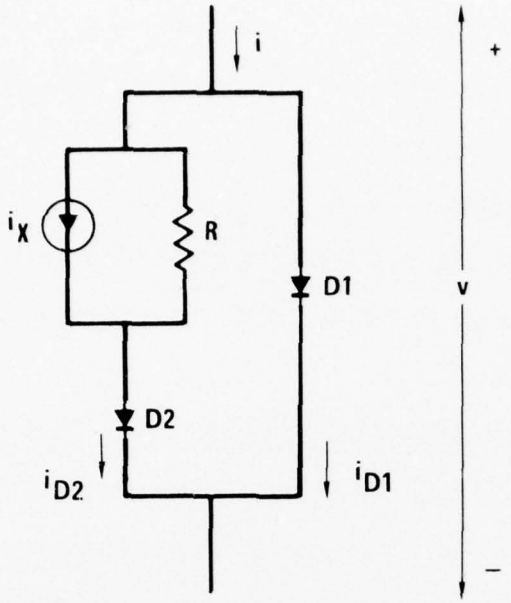


Figure 2–10. Circuit Model of Diode under RF Influence

which can be described by an equation of the form:

$$i = I_0(exp\ (qv/kT) - 1)$$

where i is the current through the junction, v is the voltage across the junction, I_0 is the leakage current, q is the charge on an electron, k is Boltzmann's constant, and T is the temperature in °K. (q/kT is approximately 40 V^{-1} at room temperature).

Diode D2, resistor R, and current source i_X comprise the RF-induced leg of the circuit, which models the difference in the diode IV characteristics resulting from rectification in the diode. D2 is identical to diode D1 in characteristics. R and i_X depend on the RF signal level, frequency, and tuning conditions. Figure 2-11 shows the range of i_X versus R for an ideal diode shunted by a capacitance C. This range is conservative for real diodes (i.e., i_X and R will be smaller than the values indicated). Figure 2-12 shows the type of diode characteristic predicted by the model along with an actual curve measured at 220 MHz.

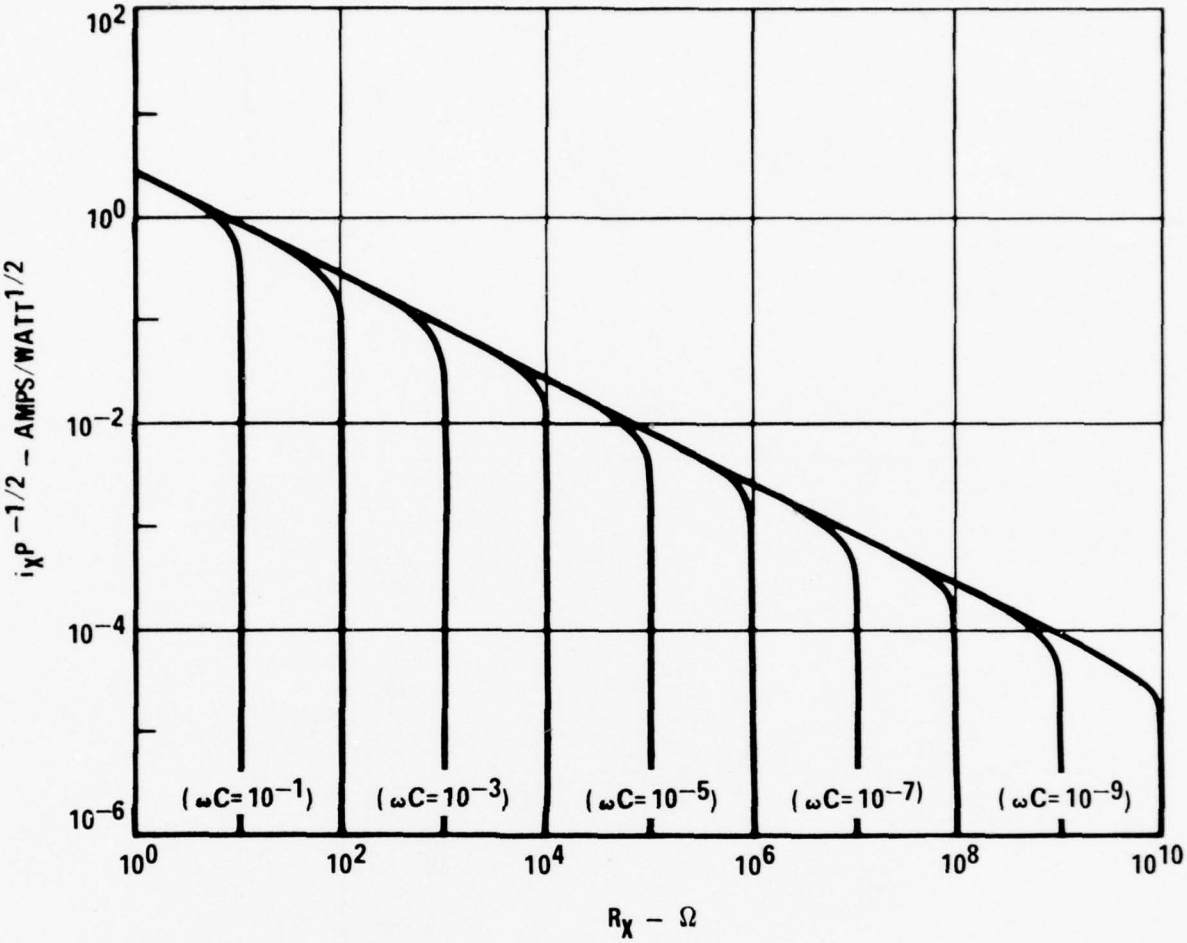
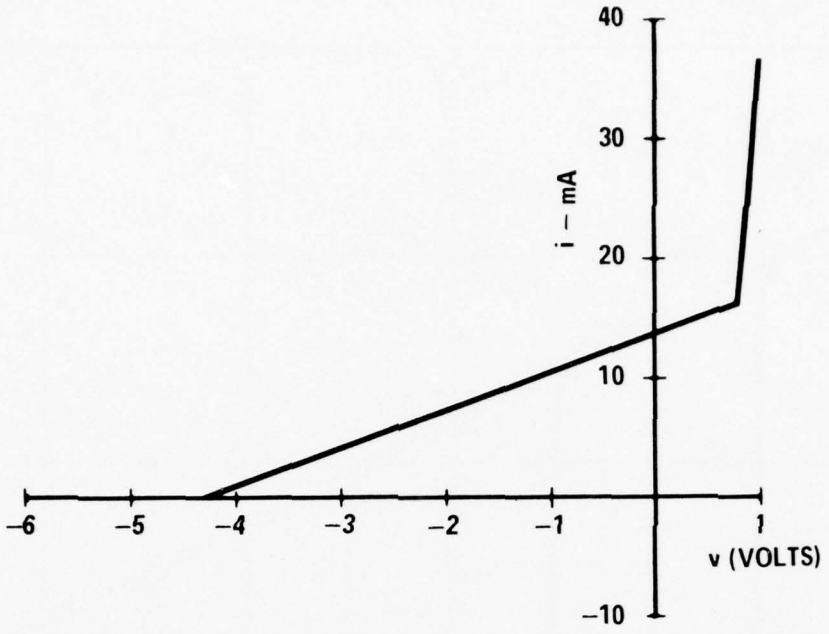
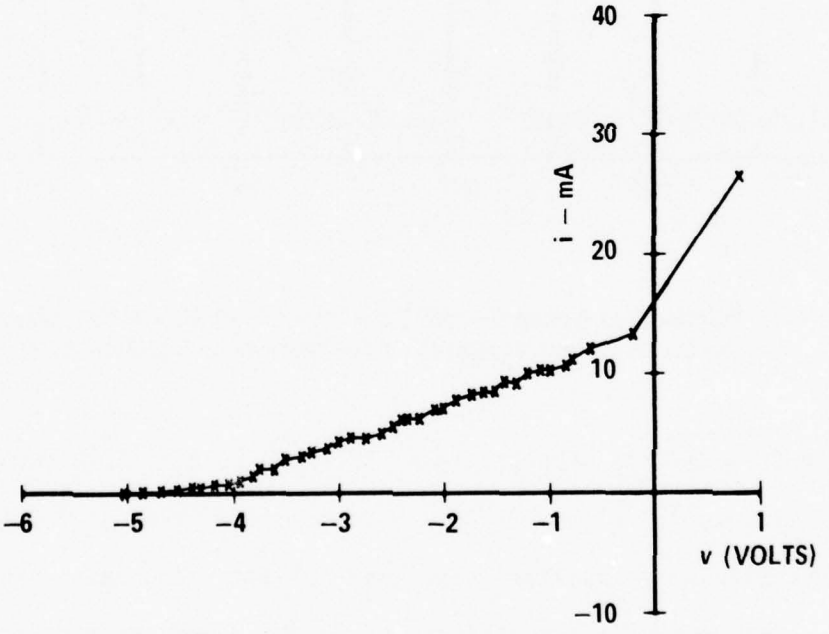


Figure 2–11. Relationship Among Current Generator, RF Power, and Resistance in the Diode Model (Parametric in the Frequency-Capacitance Product)

An Ebers-Moll model for bipolar transistors can be similarly modified to account for RF effects[16]. Figure 2-13 is a schematic diagram of the RF interference model for an npn bipolar transistor. The base-collector and base-emitter junctions are modified as described for the isolated pn junction and the subscripts C and E refer to the collector and emitter respectively. In addition to the modified diode characteristics (which account for changes in the saturation region), both the forward and reverse alphas (α_F and α_R respectively) depend upon the RF signal.



a) MODEL



b) ACTUAL 1N4154 DIODE
f = 220 MHz RF POWER = 90 mW

Figure 2–12. Piecewise Linear Approximation RF Interference Model Compared to Observed Diode Characteristics

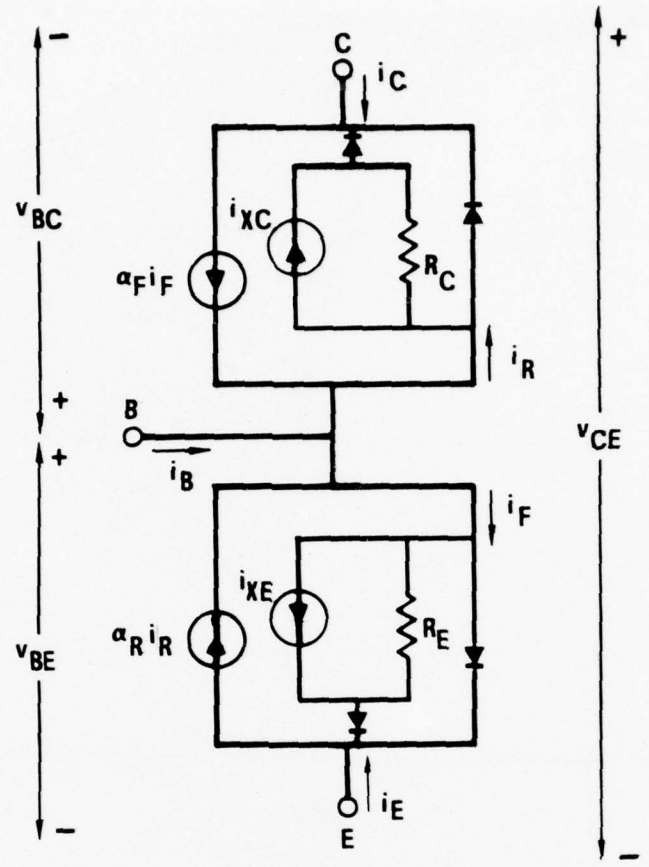


Figure 2–13. Modified Ebers-Moll Model for a Transistor Under RF Influence

This dependence, shown in figure 2-14, appears to be significant only when RF enters the base lead.

To perform a worst case analysis with this model it is necessary to recognize that the RF signal can affect either junction. Any combination of power split between the two junctions is possible subject to the constraint that the total power be less than or equal to the applied power. It appears that for RF injected on the collector lead, the base-collector junction is stimulated more than the base-emitter junction, while the opposite is true for RF injection on the base and emitter leads. It is also true that different RF driving impedances (which will be a random factor in real world cases) will affect the Norton elements (i_X and R)

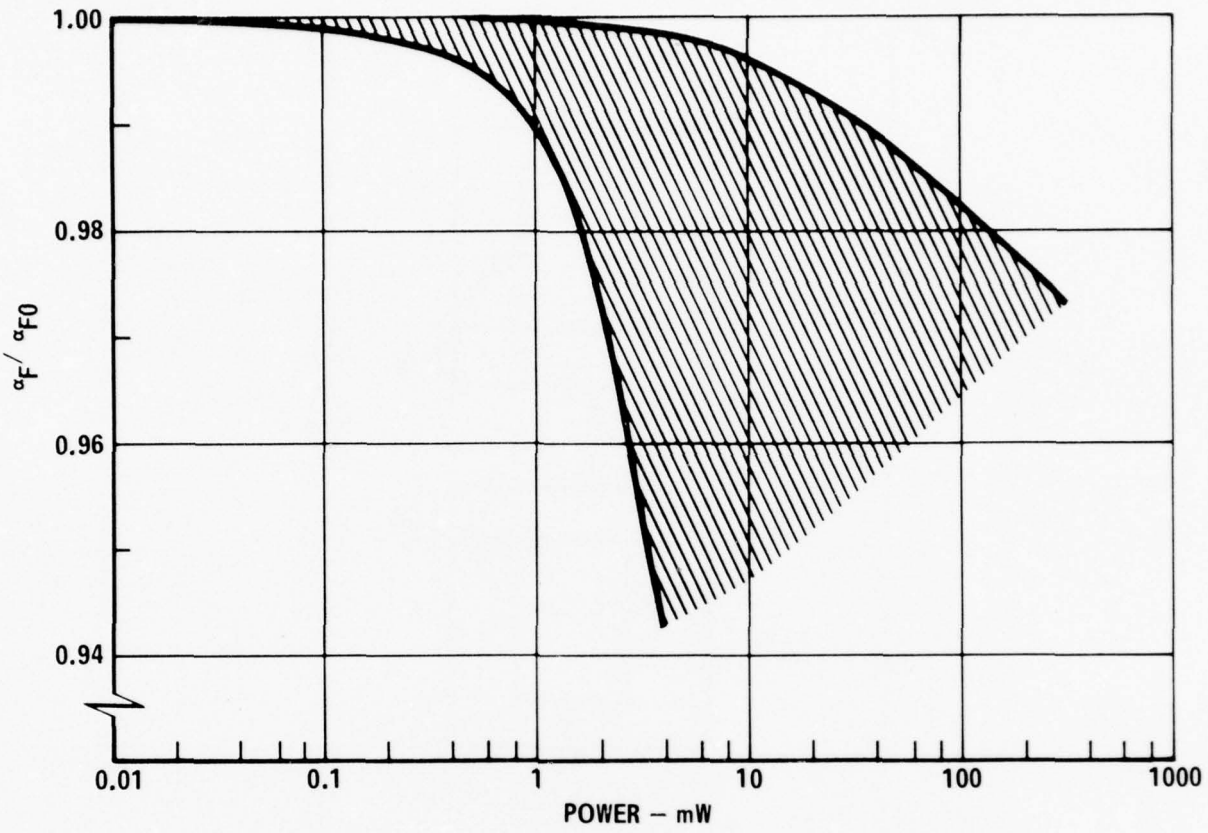


Figure 2–14. Observed Range of Normalized Transistor Alpha With RF Into the Base for Frequencies From 0.22 GHz to 3 GHz

subject to the constraints implied by figure 2-11. In any event, external circuit constraints will greatly affect the significance of any particular power split or i_X and R combination so that an iterative search for the worst case is necessary. It is anticipated that a large circuit analysis program will be used to perform this iterative analysis.

One such computer circuit analysis program is SPICE (Simulation Program with Integrated Circuit Emphasis)[17]. SPICE is a versatile, general purpose circuit analysis program which performs dc, ac, or transient analysis of linear or non-linear electronic circuits. Two versions are in use: SPICE 1 has been available since 1972; SPICE 2 is an improved version that has been available since 1975.

The program is written in Fortran IV, and contains approximately 13,000 statements. Versions are available for several large computers, notably the CDC 6400 and the IBM 360. SPICE can be obtained from Prof. D. O. Pedersen, c/o University of California at Berkeley, for handling charges only. A time-sharing version ISPICE, is available commercially from National CSS, Norwalk, Connecticut.

Circuit elements are specified by numbering the nodes in the circuit and specifying to which nodes each element is connected along with the element parameters. To use the RF models, it is necessary to decide which circuit elements (diodes or transistors) are most likely to be affected by the RF signal. As a guide, the elements closest to the RF injection port will usually account for the worst case effects. Since SPICE only recognizes voltage-controlled current sources, it is necessary to modify the previous models slightly by adding one ohm sensing resistors which convert currents to voltages. Figure 2-15 shows the bipolar transistor model modified for SPICE. The two resistors RCSENSE and RESENSE develop the voltages which control the current generators IARIC and IAFIE, respectively. (In this example IAFIE would be described by the data statement)

IAFIE V 8 12 12 13 .XXX

where IAFIE is the name of the circuit element connected between nodes 8 and 12 (node numbers are arbitrary in this example), the controlling voltage is between nodes 12 and 13 (across RESENSE in this example) and .XXX is the value of α_F (i.e., IAFIE = $.XXX(V_{12} - V_{13})$).

Also shown is a scheme to realize the RF dependence of ISCC and ISCE for fixed values of RGC and RGE. Both of these current sources are controlled by the voltage between nodes 16 and 20 (in this example). The voltage generator VGEN is used to step the values of ISCC and ISCE over the range of interest (as determined from figure 2-11). For given values of RGC and ω, figure 2-11 shows the relationship between i_{XC} and $\sqrt{P}$. Hence, for a maximum power there is a maximum value of i_{XC}.

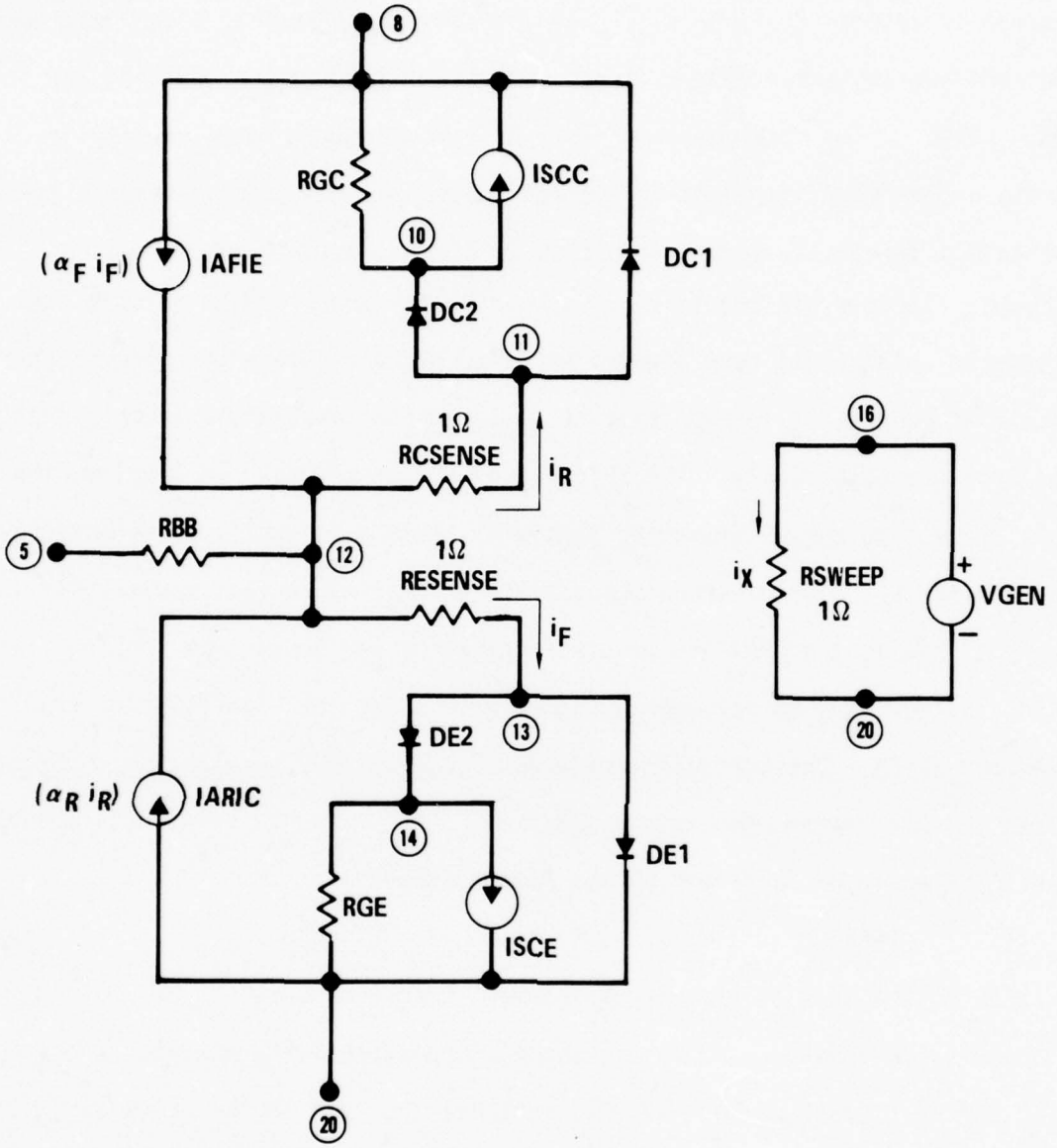


Figure 2–15. Modified Ebers-Moll Model in an External Model Configuration for SPICE Simulation

Since $i_{XC(max)} = v_{GEN(max)}/1\Omega$, stepping v_{GEN} from 0 to $v_{GEN(max)}$ is equivalent to stepping i_{XC} from 0 to $i_{XC(max)}$.

To account for the possible power split between the base-collector and base-emitter diodes, the factors K_C and K_E are used. K_C and K_E are constants of

proportionality relating the RF stimulation in the B-C and B-E junctions, respectively, to v_{GEN}. Thus one could have:

$$ISCC = K_C \, v_{GEN},$$

and

$$ISCE = K_E \, v_{GEN}$$

for the worst case dependence shown in figure 2-11. The corresponding SPICE statements would be:

ISCC V 10 8 16 20 K_C,

and

ISCE V 14 20 16 20 K_E .

K_C and K_E are varied parametrically while i_{XC} and i_{XE} are stepped over their total range by stepping v_{GEN}. The generator VGEN is stepped over a range with a control statement such as

.DC TC VGEN .AAA .BBB .CCC

where .AAA is the value of $v_{GEN(min)}$, .BBB is the value of $v_{GEN(max)}$, and .CCC is the step size. From figure 2-11 .BBB is given by $i_{X(max)}$ corresponding to the maximum RF power expected and the frequency of operation. .AAA and .CCC tell the program where to start the v_{GEN} sweep and the increment at each step.

The output of a SPICE simulation is selected circuit voltages or currents corresponding to the stepped values of v_{GEN}. To display the explicit relationship between the interfering RF signal and any particular circuit response, it is necessary to establish a one-to-one correspondence between the stepped values of v_{GEN} and the RF power.

As an example of the application of the modified Ebers-Moll model and SPICE, consider the problem of RF entering the output circuitry of a 54/74 family device when the output is low. The 5400/7400 NAND gate will serve as a specific example.

The circuit diagram of a 7400 NAND gate is shown in figure 2-16 together with external connections that were used during the experimental phases of the IC Susceptibility Program. For an RF signal entering the output, it is suspected that only transistor T4 (which is "on") will be affected by the interfering signal. Accordingly, a SPICE simulation of the circuit was performed with transistor T4 modeled by the circuit shown in figure 2-15. The relationship between v_{GEN} and the RF power, P, is assumed to be $v_{GEN} = 20\sqrt{P}$ where v_{GEN} is given in volts and P is given in watts. The voltage v_{GEN} was stepped over a range of .2 to 20 volts which corresponds to a range of RF power from .1 to 1000 mW. The power split constants were chosen to be $K_C = 3.79 \times 10^{-3}$ and $K_E = .667 \times 10^{-3}$. The calculated results are compared to typical measured results in figure 2-17. The SPICE simulation shows that the assumptions that T4 is responsible for the observed RF effects is reasonable

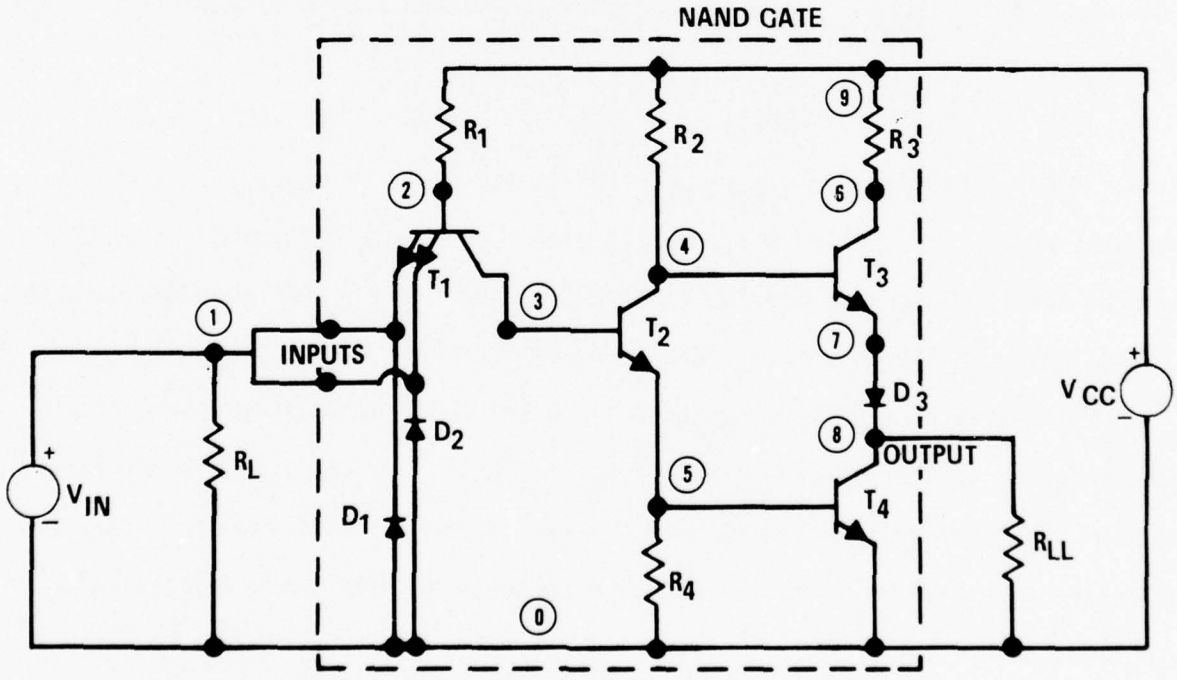


Figure 2–16. Schematic Diagram of One 7400 NAND Gate With External Connections for Producing Transfer Curves

up to perhaps 200 mW, at which point the measured data begins to turn down. It is easy to see that particular interference thresholds can be determined by this procedure.

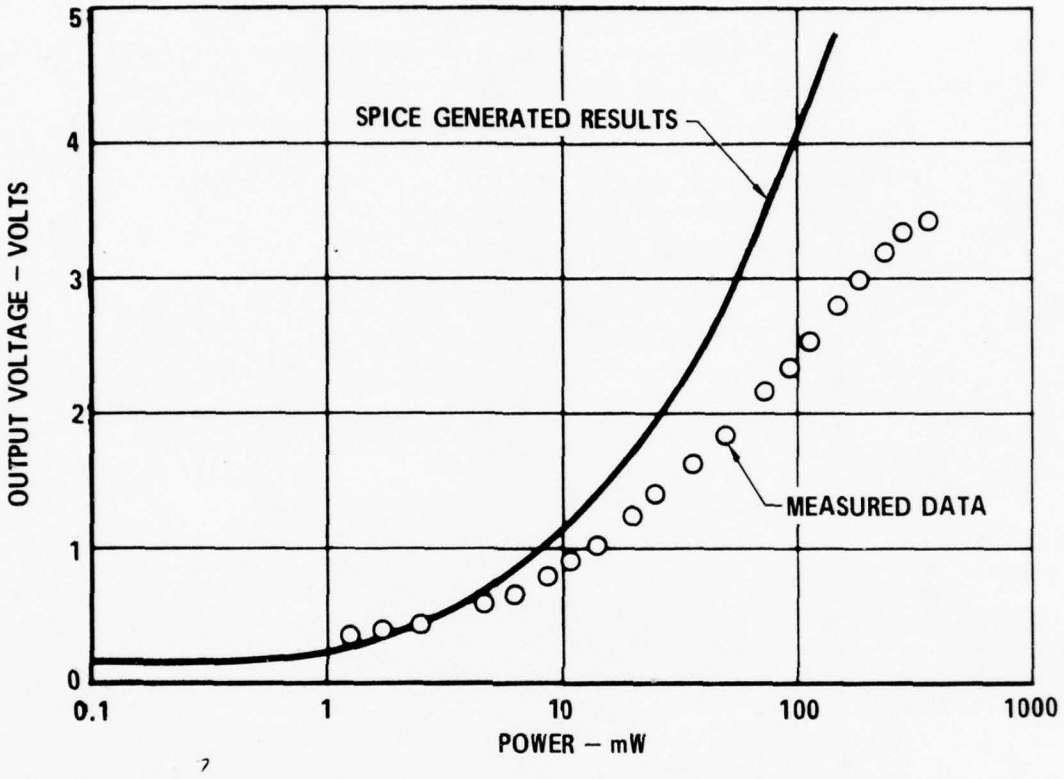


Figure 2–17. Comparison of SPICE Simulation of 7400 NAND Gate to Measured Results

2.2.1.1.2 RF Interference Data for TTL ICs - All available interference data acquired on TTL devices are included in figure 2-18 which is a composite graph showing the worst case susceptibility curves of power versus frequency for different susceptibility criteria. Table 2-1 is a list of the types of devices whose interference data are included in the composite graph. Each susceptibility criterion for this graph is a combination of a high and a low output state value. The first criterion, labeled manufacturer's guaranteed specification limit, is the maximum allowable voltage for the low state, 0.4 volt, or the minimum allowable for the high state, 2.4 volts. Since this graph is worst case, which state is susceptible

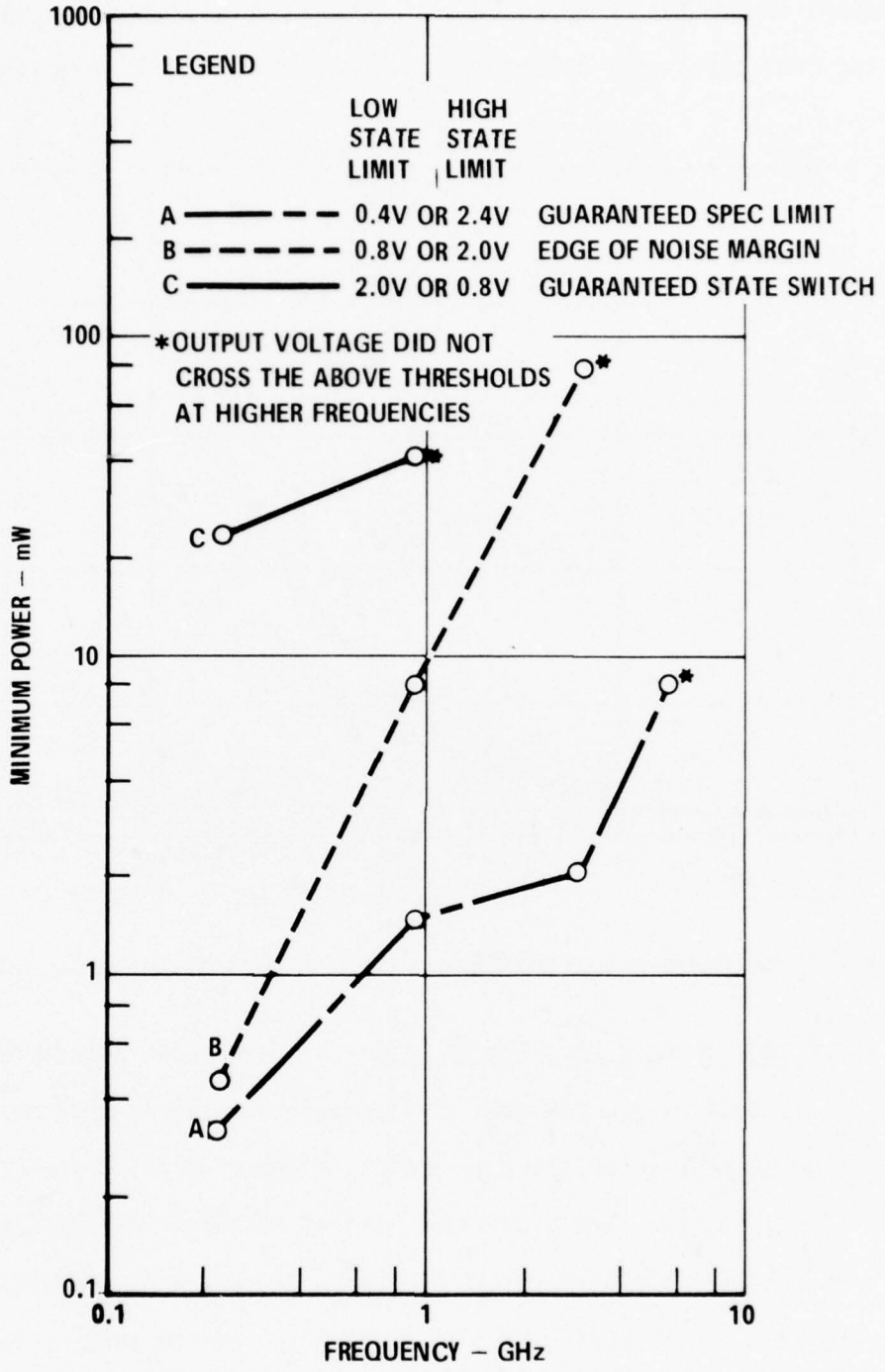


Figure 2–18. Composite Worst Case Susceptibility Values for TTL Devices (Maximum Specification Value for Low V_{OUT} = 0.4 Volt and Minimum Specification Value for High V_{OUT} = 2.4 Volts)

Table 2–1. TTL Devices Whose Susceptibility Data Are Included in This Section

DEVICE NO.	DEVICE TYPE
7400	QUAD 2 INPUT NAND GATE
7402	QUAD 2 INPUT NOR GATE
7404	HEX INVERTER
7405	HEX INVERTER (OPEN COLLECTOR)
7432	QUAD 2 INPUT OR GATE
7450	EXPANDABLE DUAL 2 WIDE, 2 INPUT AND–OR–INVERT GATE
3021	QUAD EXCLUSIVE OR GATE

is irrelevant in terms of the RF power level at which it breaks either limit. The second criterion is the edge of the 0.4 volt noise margin built into each state of the device, i.e., the minimum or maximum value that the input of the next stage will be guaranteed to recognize as the correct output state. These noise-margin-limit values are 0.8 volt for the low state and 2.0 volts for the high state. The third criterion on the graph is the guaranteed switch limit which means that a high output would be below 0.8 volts and recognized as a low state or a low output would be above 2.0 volts and recognized as a high state. Either of these conditions would cause bit errors and incorrect system outputs. Figure 2-19 is the composite graph showing the susceptibility levels for package supply current.

2.2.1.1.3 Miscellaneous Bipolar Digital IC RF Interference Data - At this time the only bipolar digital data available outside of the TTL family are on a line driver/line receiver (9614/9615) pair. These two devices have been tested at 220 MHz to determine their interference thresholds. Of special interest were the signal lines between the driver and receiver which may be very long and act as pick-up wires for interfering signals. Table 2-2 shows the measured susceptibility for each port. The RF power listed in the table caused a switch in the receiver output state.

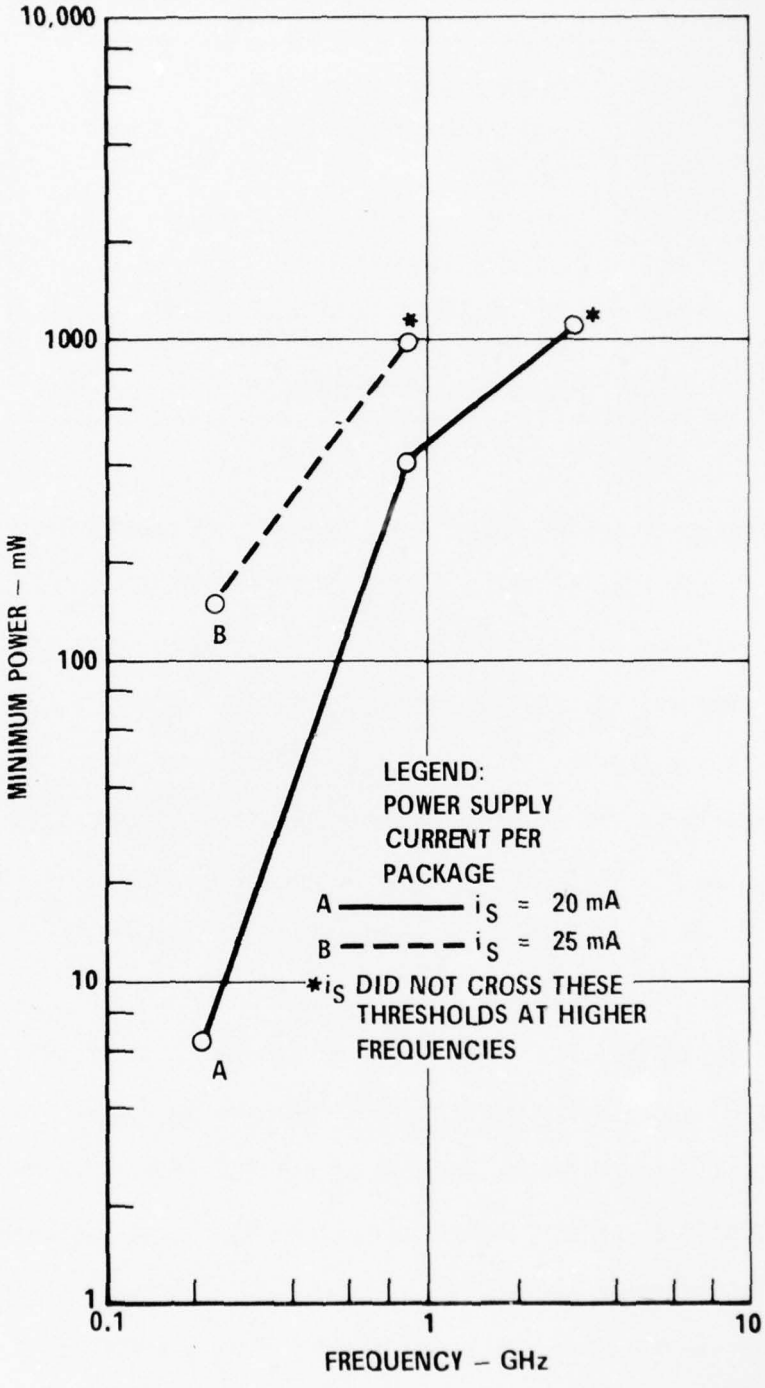


Figure 2–19. Composite Worst Case Susceptibility Levels of TTL Devices for Package Supply Current (Typical 10 to 15 mA)

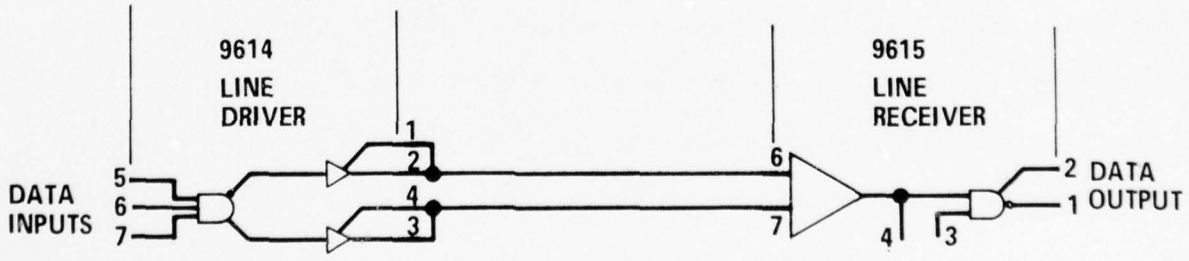
Table 2–2. RF Susceptibility Characteristics of Line Driver/Line Receiver at 220 MHz

9614 (LINE DRIVER)

RF INJECTION PORT	RF POWER REQUIRED TO PRODUCE STATE CHANGE IN RECEIVER OUTPUT
ACTIVE PULLUP (PIN 1)	> 566 mW
OUTPUT (PIN 2)	> 566 mW
OUTPUT (PIN 3)	464 mW
ACTIVE PULLUP (PIN 4)	175 mW
INPUT (PIN 5)	54 mW
INPUT (PIN 6)	41 mW
INPUT (PIN 7)	41 mW

9615 (LINE RECEIVER)

RF INJECTION PORT	RF POWER REQUIRED TO PRODUCE STATE CHANGE IN RECEIVER OUTPUT
OUTPUT (PIN 1)	68 mW
ACTIVE PULLUP (PIN 2)	216 mW
STROBE (PIN 3)	120 mW
RESPONSE CONTROL (PIN 4)	13 mW
INPUT (PIN 5)	> 566 mW
INPUT (PIN 6)	> 566 mW
INPUT (PIN 7)	> 566 mW



2.2.1.2 CMOS Digital IC RF Interference Information - This section describes CMOS digital device interference. Worst case interference data measured to date on typical family representative devices are given. The primary susceptibility parameters are output voltage and device current.

2.2.1.2.1 RF Interference Model for MOSFETs - The MOSFET model is not yet ready for inclusion in this handbook. It will be presented in the next edition.

2.2.1.2.2 RF Interference Data for CMOS Digital ICs - All available interference data on CMOS devices are included in figure 2-20 which is a composite graph showing the worst case susceptibility curves of power vs frequency for different susceptibility criteria for output voltage. Table 2-3 is a list of the types of devices whose interference data are included in the composite graph. As in the TTL case each susceptibility criterion for this graph is a combination of a high and a low output state value. The specification limits used are the industry wide acceptable limits for CMOS B-series devices or a given increment from these specifications.

The first criterion, labeled manufacturer's guaranteed specification level, is the maximum allowable voltage for the low state, 0.05 volt, or the minimum allowable voltage for the high state, 4.95 volts with V_{DD} equal to 5 volts. The second criterion is the edge of the 1-volt noise margin which is 1.05 volts for the low state and 3.95 volts for the high state. These values are the guaranteed limits which can be recognized by the input of a following CMOS device as being in the correct state. The third criterion is an arbitrary 2-volt limit, two volts above zero or two volts below 5 volts, which is 3 volts. This criterion would be in the gray area between logic states where no state can be guaranteed for a specific voltage. Figure 2-21 shows the composite graph for the package current.

2.2.2 Linear IC RF Interference - The linear category of ICs consists of op amps, comparators, voltage regulators, video amplifiers, etc. Op amp differential input circuitry is the most susceptible to RF of all ICs tested by a considerable margin.

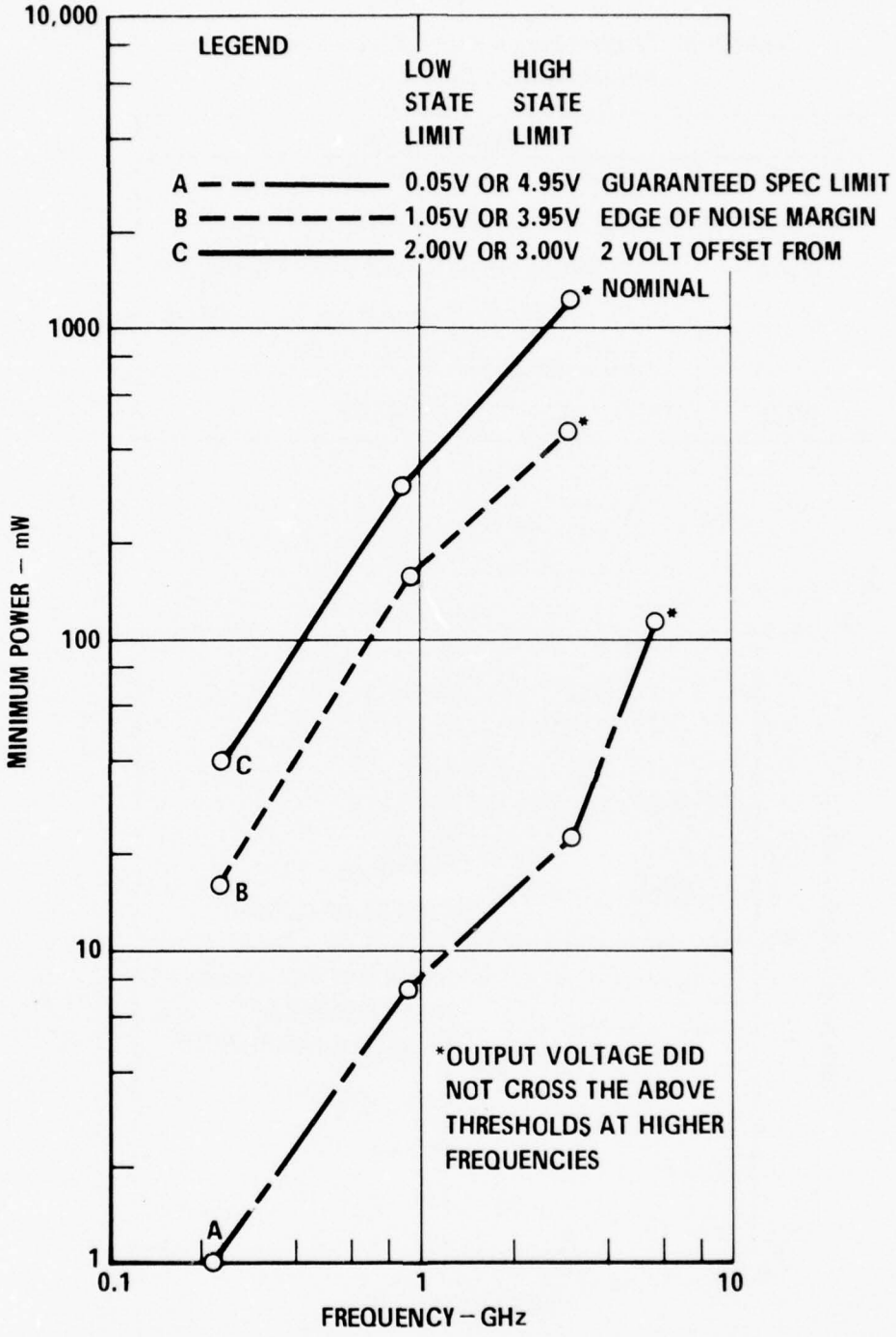


Figure 2–20. Composite Worst Case Susceptibility Values for CMOS Devices (Maximum Specification Value for Low V_{OUT} = 0.05 Volt and Minimum Specification Value for High V_{OUT} = 4.95 Volts)

Table 2–3. CMOS Devices Whose Susceptibility Data Are Included in This Section

DEVICE NO.	DEVICE TYPE
4011A	QUAD 2 INPUT NAND GATE
4011B	QUAD 2 INPUT NAND GATE
4007A	DUAL COMPLEMENTARY PAIR PLUS INVERTER
4007B	DUAL COMPLEMENTARY PAIR PLUS INVERTER
4001A	QUAD 2 INPUT NOR GATE
4013A	DUAL "D" – TYPE FLIP-FLOP

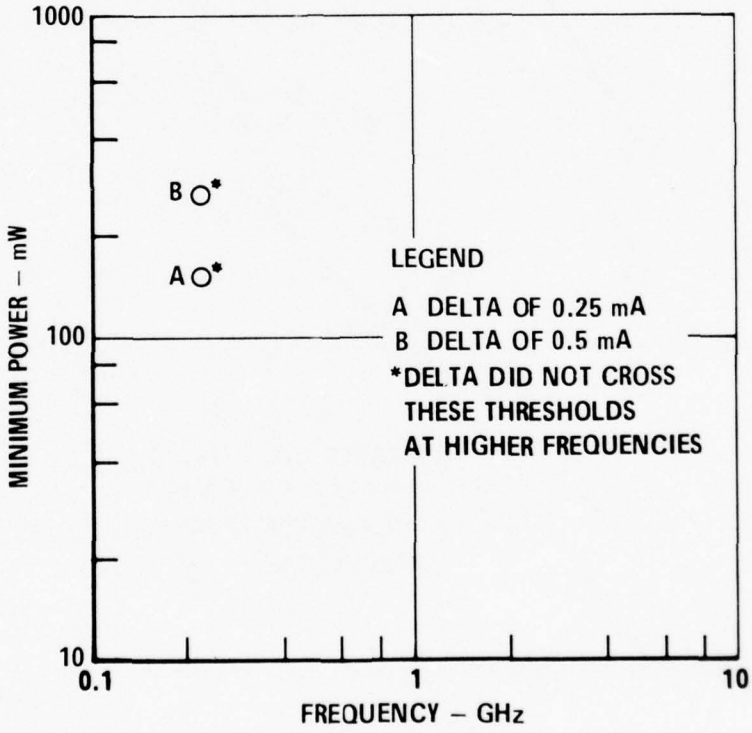


Figure 2–21. Worst Case Susceptibility Levels of CMOS 4011B Devices for Change in Package Supply Current

2.2.2.1 Op Amp RF Interference Information - Op amp interference is treated in terms of a general model and the data presently available. The susceptibility criteria are the RF-induced offset voltage on the input and the package current.

2.2.2.1.1 RF Interference Model for Op Amps - Figure 2-22 shows an operational amplifier circuit with the addition of an offset interference generator. The voltage v_{II} provided by this generator to the inverting input is a function of the RF drive signal and the injection port. Up to a voltage limit of one volt, v_{II} is approximately proportional to the incident power level with a decreasing proportionality constant with increasing frequency as shown in figure 2-23. This estimate is conservative at higher power levels. The polarity of v_{II} depends upon the RF injection port and a worst case analysis must consider that v_{II} could be of either sign. The time dependence of v_{II} is the same as the time dependence of the modulation on the RF interference signal.

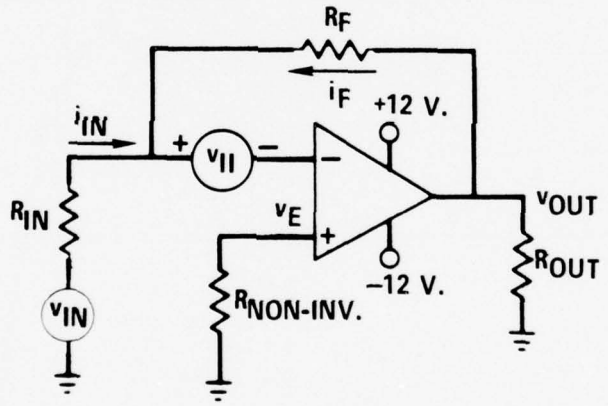


Figure 2–22. OP AMP Circuit Including Offset Generator

2.2.2.1.2 RF Interference Data for Op Amps - The RF interference data available for op amps is defined in terms of the input offset voltage v_{II} as is the model. This general term v_{II} can then be applied directly to other circuits without taking the measurement circuit into account. The composite worst case op amp interference data for v_{II} are presented in figure 2-24. Figures 2-25 and 2-26 show the worst case levels for negative and positive device current, respectively.

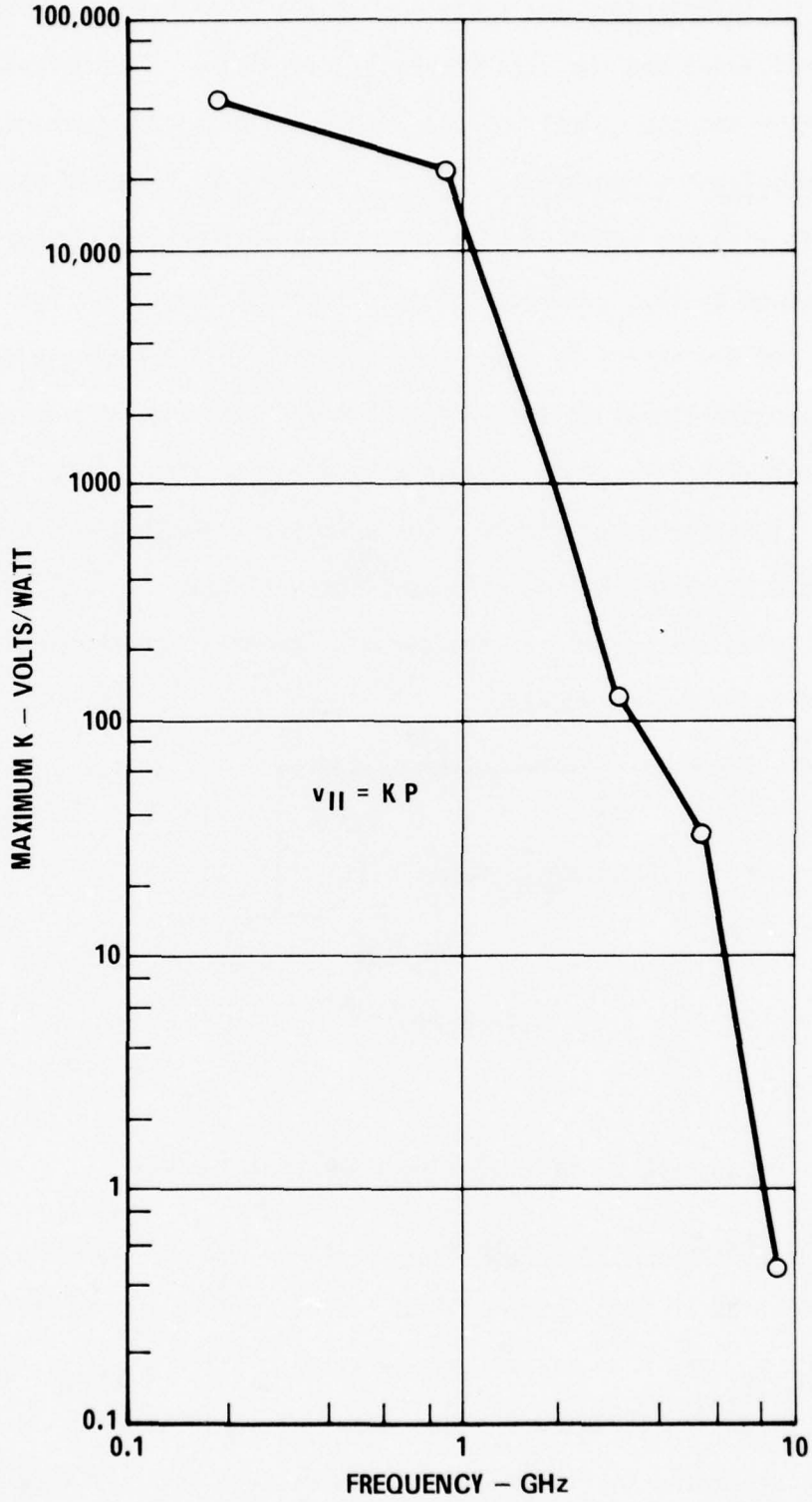


Figure 2–23. Maximum Values of Proportionality Constant Between Interference Input Offset Voltage and RF Power

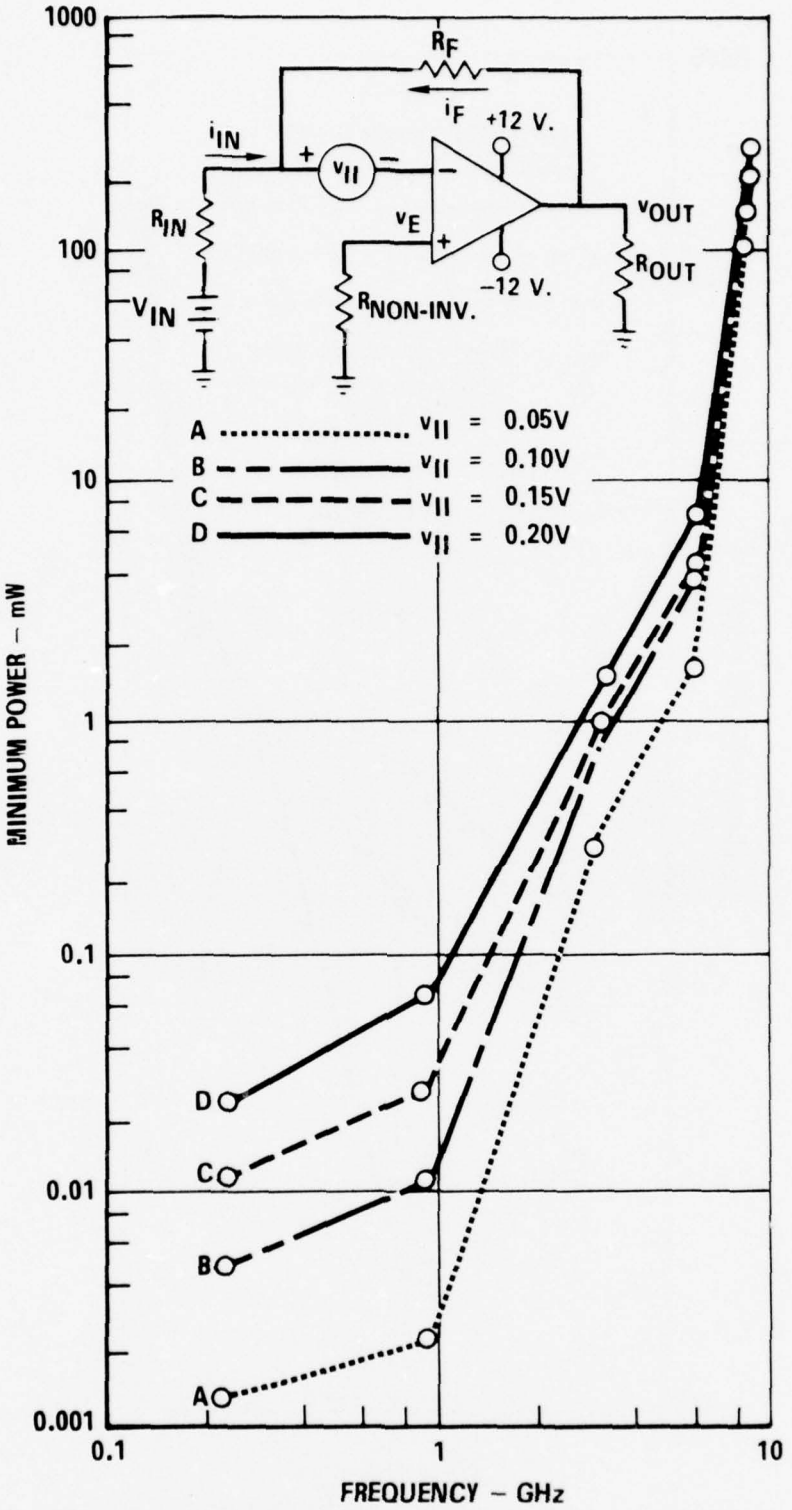


Figure 2–24. Composite Worst Case Susceptibility Values for OP AMPS Using Input Offset Voltage v_{II} (Typical Maximum v_{II} is 0.005 Volt)

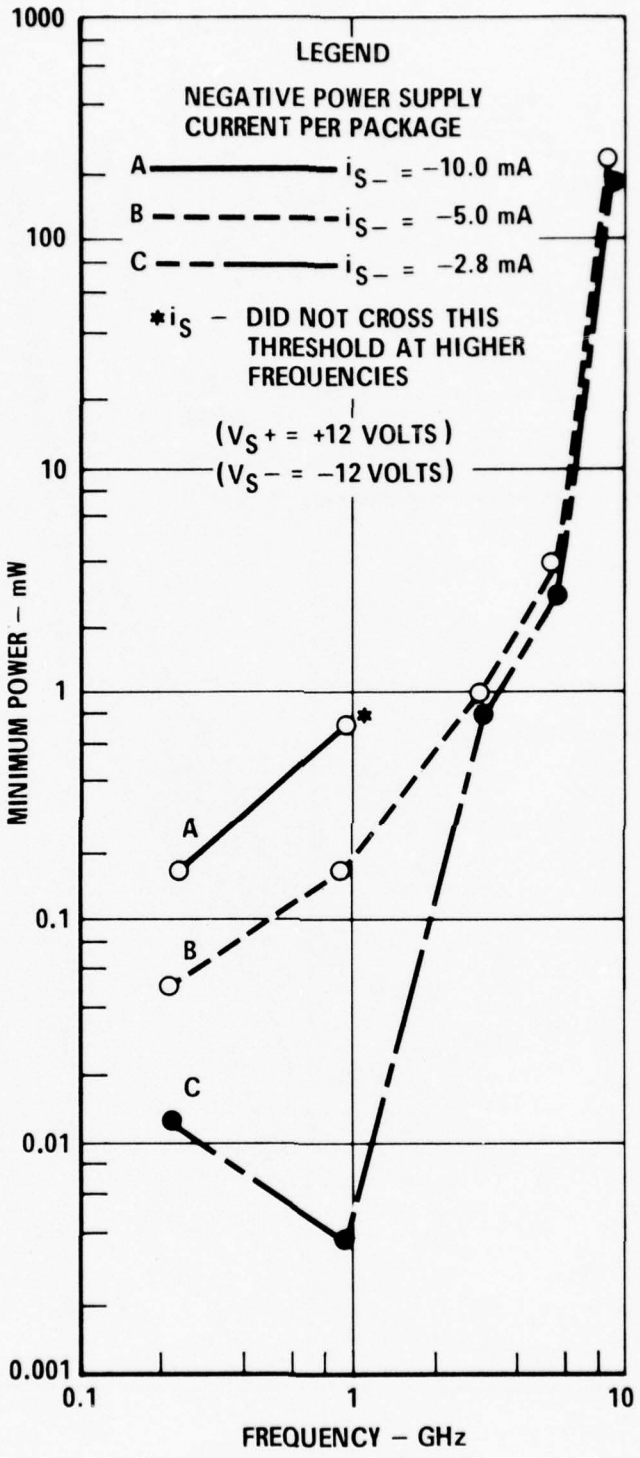


Figure 2–25. Composite Worst Case Susceptibility Values for 741 Operational Amplifier (Negative Device Current i_S) Maximum Specified Supply Current is −2.8 mA

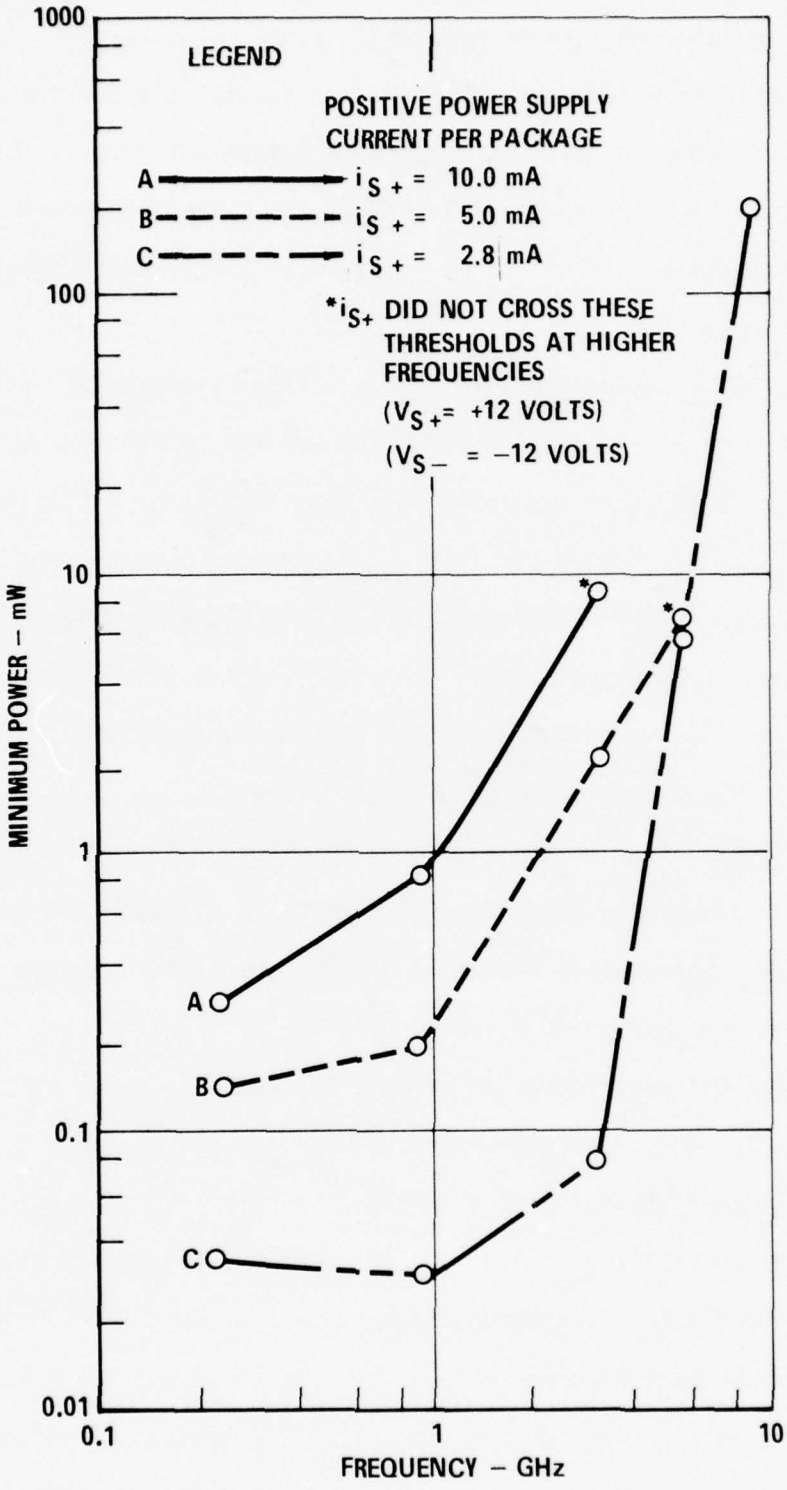


Figure 2–26. Composite Worst Case Susceptibility Values for 741 Operational Amplifier (Positive Device Current i_{S+}) Maximum Specified Supply Current is 2.8 mA

2.2.2.2 Voltage Regulator RF Interference Information - The results of tests on two voltage regulators show that one regulator was susceptible and the other was not susceptible. The LM 309H Positive Voltage Regulator was only slightly susceptible at 220 MHz and not susceptible at all to higher frequencies. The LM 320H-05 Negative Voltage Regulator was susceptible to the RF test signal. Figure 2-27 shows the susceptibility levels for the LM 320H-05.

2.2.2.3 Comparator RF Interference Information - Since a comparator uses a differential input similar to an op amp, the simple op amp input model may be used for comparators. Figure 2-28 shows the worst case data available at this time for a comparator.

2.3 IC Damage Susceptibility - Integrated circuits can suffer damage from sufficiently intense microwave signals. The energy in the RF signal can be sufficient to cause thermal failures in the silicon junctions, the metallization stripes, or the bond wires. The significance of damage suffered by the IC is determined by its ability to function after injection of the RF signal. If the device can still function in a limited capacity after the RF stimulus is removed, the device is considered degraded. For example figure 2-29 shows the transfer curve for an op amp installed in an inverter circuit with a gain of 10. After exposing the op amp input circuit to a high level pulsed RF signal, the transfer curve changes as shown in figure 2-29. This degradation occurs when one of the input transistors of the differential pair has suffered a junction failure. Catastrophic failure is defined as complete inability of the device to perform its intended function.

Thus the difference between degradation and catastrophic failure in ICs is in the criticality of the part damaged, not in the type of damage mechanism. For instance, while a metallization failure may only cause degradation if it occurs in the offset null circuit of an op amp, a similar metallization failure in the output circuit will cause catastrophic failure.

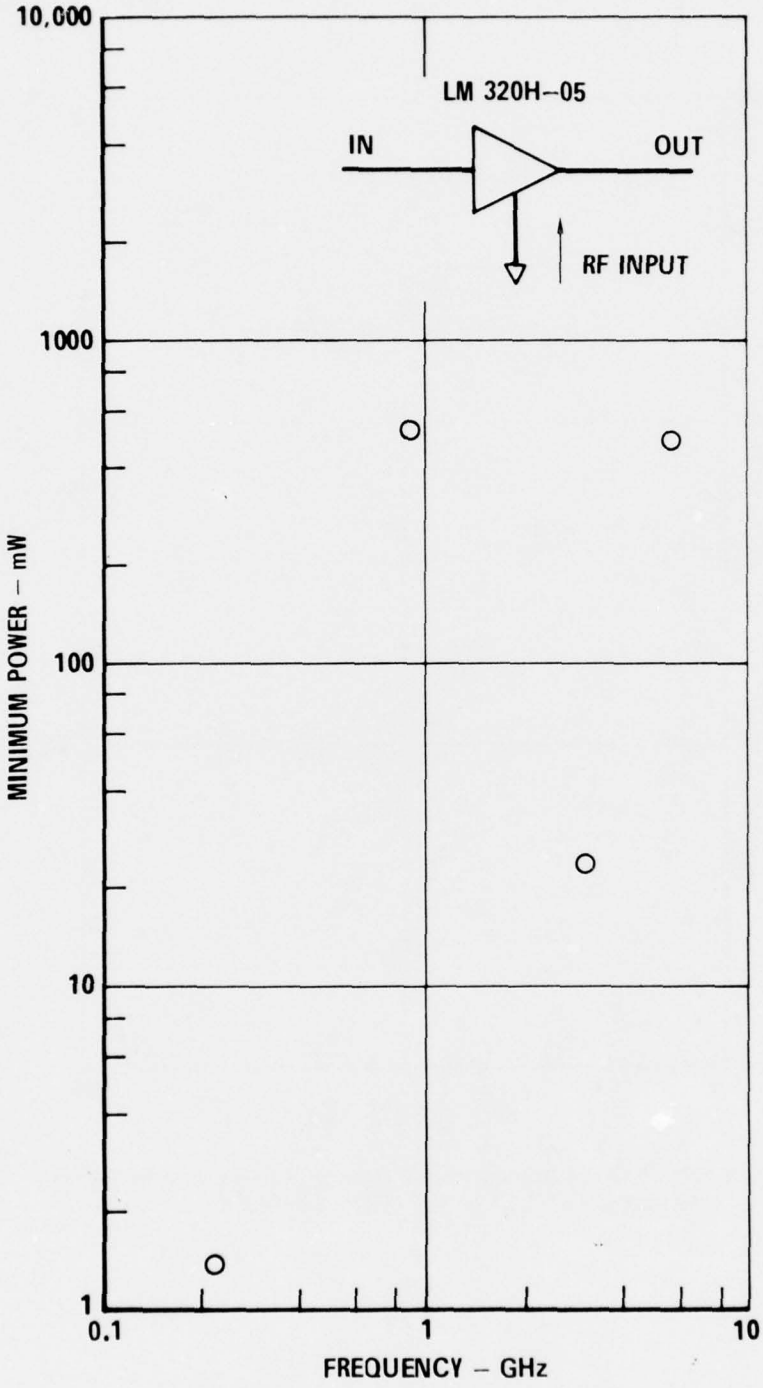


Figure 2–27. Worst Case Susceptibility Values for Voltage Regulator Using Change of 0.5 Volt out of 5 Volts as Susceptibility Criterion

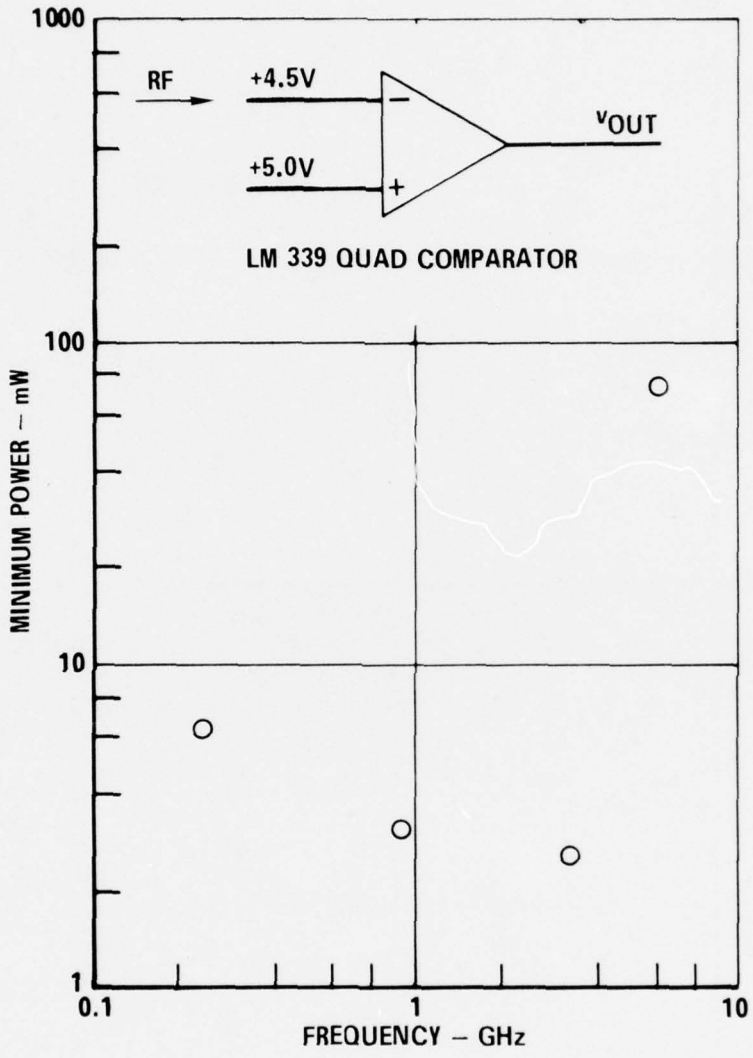
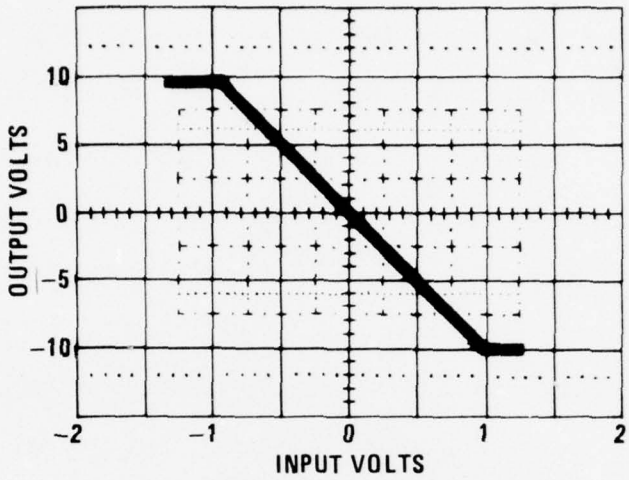


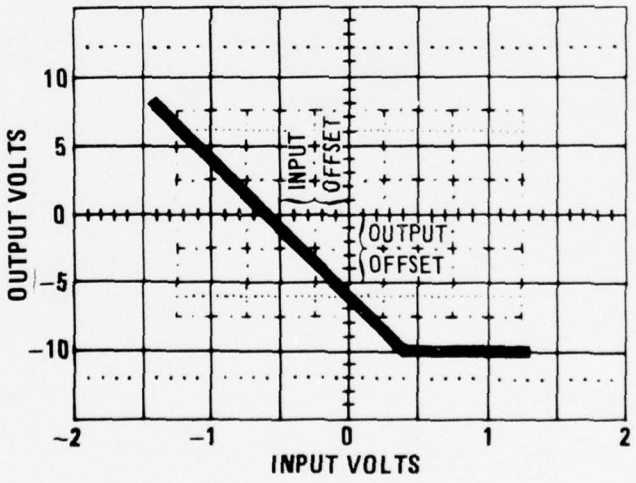
Figure 2–28. Worst Case Susceptibility Values for Comparator Using Output Switch as Susceptibility Criterion

(V_{S+} = +12 VOLTS)
(V_{S-} = −12 VOLTS)



a) V_{OUT} VS V_{IN} CURVE FOR 741 UNDER NORMAL CONDITIONS

(V_{S+} = +12 VOLTS)
(V_{S-} = −12 VOLTS)



b) V_{OUT} VS V_{IN} CURVE FOR DEGRADED 741

Figure 2–29. Degradation Effect on 741 Operational Amplifier in Amplifier Circuit (Gain = −10)

2.3.1 IC Damage Mechanisms - Under RF stress only three types of damage mechanisms have been discovered: bond wire failure, junction failure, and metallization failure. Figures 2-30, 2-31 and 2-32 are photomicrographs showing typical examples of a bond wire, a junction, and a metallization failure, respectively. These types have been observed both singly and in combination throughout high power RF testing. During this testing over 2500 devices have been exposed to microwave signals varying in frequency, pulse width, and power level. Throughout this testing all damage fell into one of these three damage mechanisms. The following efforts will be directed toward evaluating the minimum energy necessary to cause at least one of these mechanisms to occur regardless of whether degradation or catastrophic failure results.

2.3.2 IC Damage Models - Since the damage mechanisms are thermal in nature, the damage models are derived from basic heat flow analysis. For worst case analysis the heat is assumed to be produced by I^2R dissipation of the RF signal and there is no frequency dependence. RF power level and pulse duration are the important parameters.

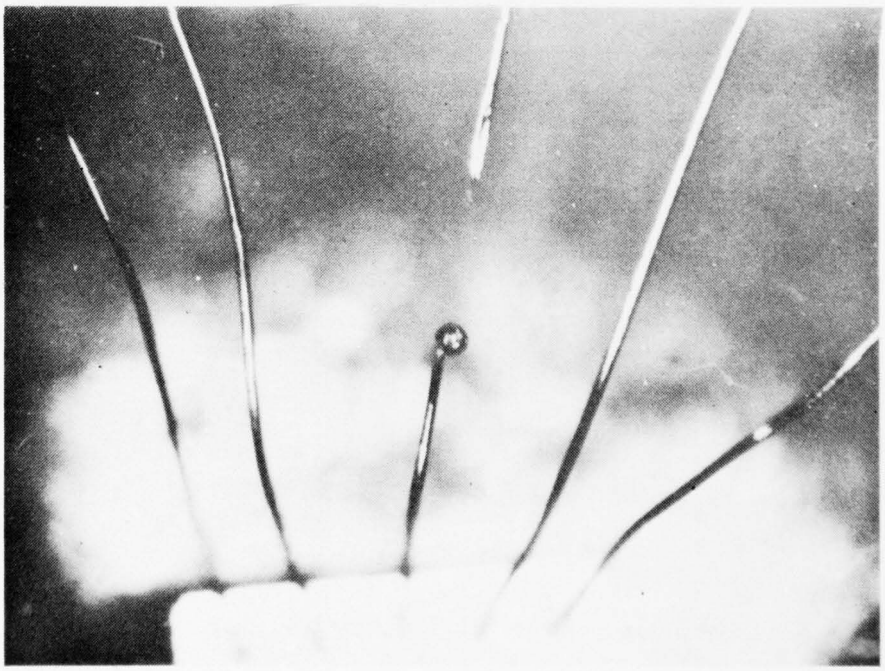


Figure 2–30. Photomicrograph of Bond Wire Failure

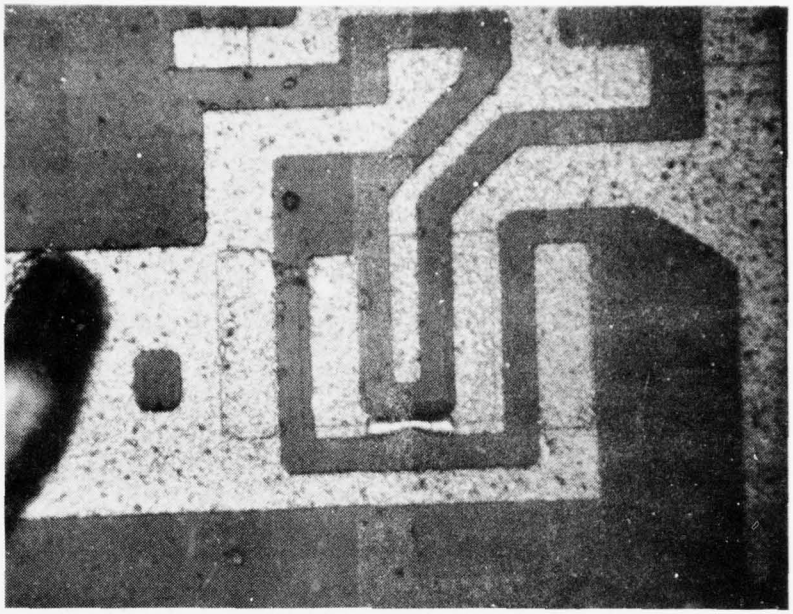


Figure 2–31. Photomicrograph of Collector-Emitter Junction Failure in the Output Transistor of a 7400 NAND Gate

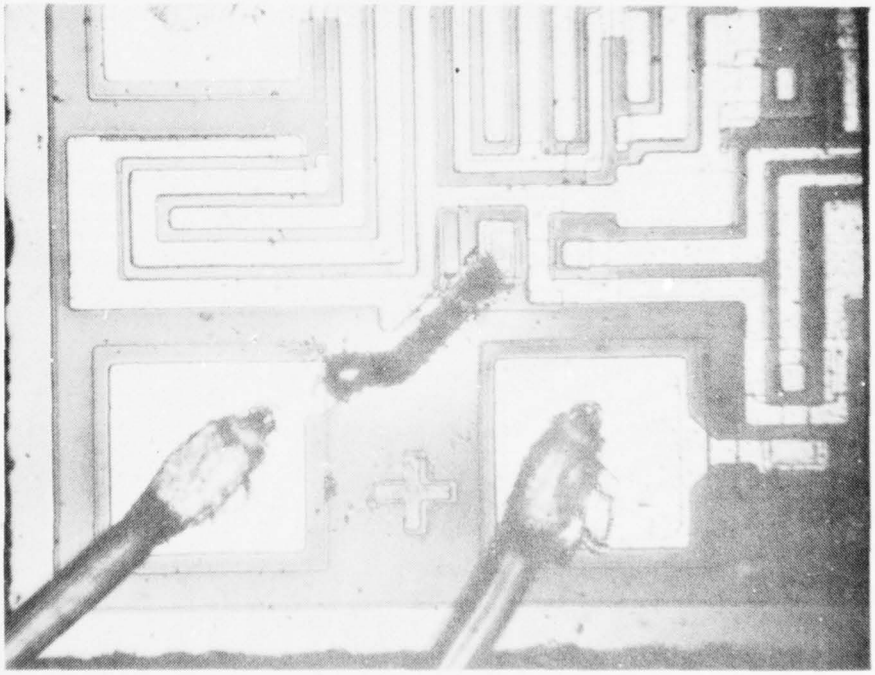


Figure 2–32. Photomicrograph of Metallization Failure in the Input Lead of a CMOS 4011 NAND Gate

The bond wire model assumes the wire is a rod with a perfect heat sink at each end and the RF power is dissipated uniformly through the wire volume. Since the temperature is highest in the center of the wire, the desired solution of the heat flow problem is a power versus time relationship to raise the temperature at the center of the wire to the melting point. The latent heat of fusion actually required to melt the wire is assumed negligible so that the solution gives a theoretical relationship:

$$P = \frac{8\,AK\,(T_f - T_o)}{L\left[1 - \frac{32}{\pi^3} \sum_{n=1,3,5\ldots}^{\infty} \left(\frac{1}{n^3}\right) \left(\exp^{\left(-\frac{n^2\pi^2 kt}{L^2}\right)}\right)\left(\sin\frac{n\pi}{2}\right)\right]}$$

where P is power in watts,

t is time in seconds,

k is thermal diffusivity of wire material in cm^2/sec,

K is thermal conductivity of wire material in watts/cm/°C,

A is wire cross-sectional area of wire in cm^2,

L is wire length in cm,

T_f is wire melting temperature in °C,

and T_o is ambient temperature in °C.

The failure models for the junction and metallization damage modes are essentially identical. In both cases, the source of heat can be described as a thin sheet (in either silicon or aluminum) where it is assumed that all the power is being dissipated. Since the sheet is very thin, it is assumed that a uniform temperature exists through the thickness of the sheet and both cases can be treated as uniform surface heating. Both models reduce to the same boundary value problem where heat is conducted away from one surface through the silicon chip. The junction and metallization failure models assume one dimensional heat flow through the silicon chip. The lower surface of the chip is assumed to be

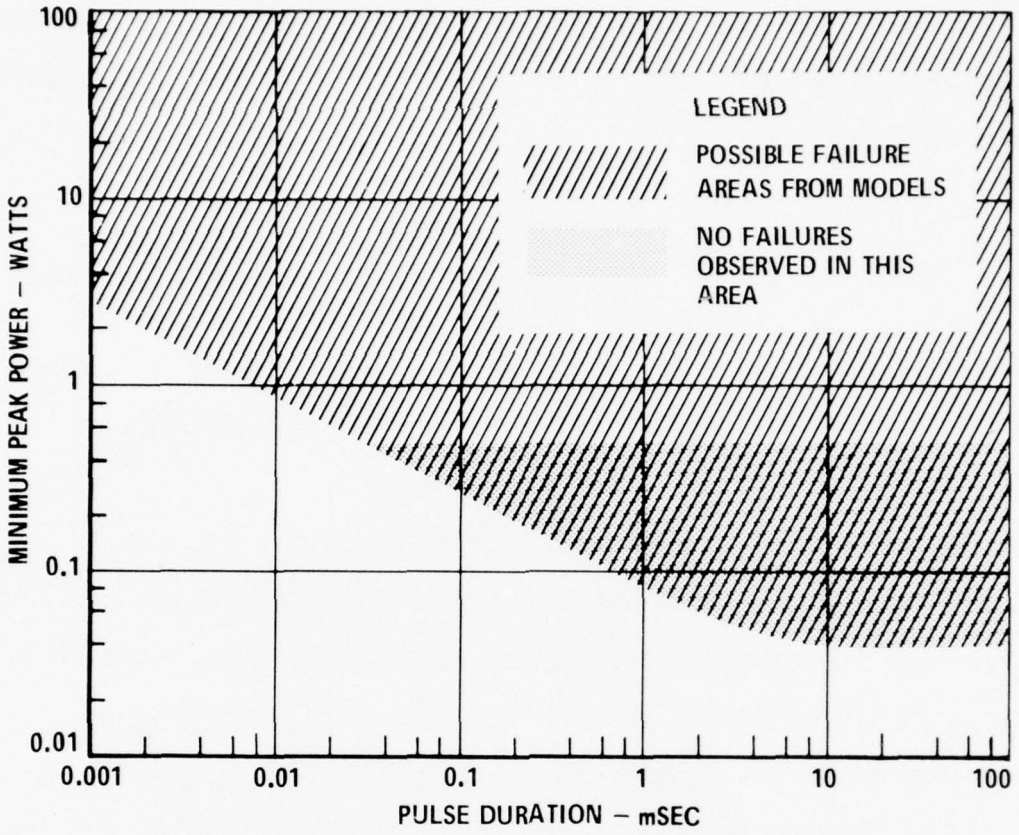
attached to a perfect heat sink which remains at ambient temperature. The silicon chip initially is at ambient temperature. The power to produce failure temperature T_f in time t is given by:

$$P = \frac{\left(\frac{T_f - T_o}{L}\right) KWD}{1 - \frac{8}{\pi^2} \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n^2} \left(\exp\left(- kn^2\pi^2 t/4L^2\right)\right)\left(\sin \frac{n\pi}{2}\right)}$$

where the area of the failure site (metallization stripe or junction) is given by the product W (width in cm) and D (length in cm) and L is the thickness of the silicon chip in cm.

The worst case assumption used for the failure models is that all the incident power is actually absorbed in the failure site. This assumption is conservative since it does not account for the power dissipated elsewhere in the chip. Also worst case values are used for the physical parameters in the predictions to calculate the minimum power to cause failure. For example the minimum bond wire diameter in current use is 0.001778 cm (0.7 mil) and a length of 0.5 cm is as long as can be reasonably expected. For junction or metallization failures, the area of the junction or stripe is the primary factor affecting a worst case prediction of failure. The worst case areas for junction and metallization failures are both assumed to be 6×10^{-6} cm^2 (a representative failure site area based on actual measurements). The worst case failure temperature for the junction model was taken to be 660°C (anything hotter would presumably melt the aluminum metallization first).

Figure 2-33 shows the pulse-power pulse-width plane separated into two regions. In the lower (unshaded) region, no failures of any kind are expected. A failure could probably occur anywhere in the shaded region; however in the darker area below 0.5 watt no failure has ever been observed even though many ICs have been tested (for interference) in this area.



SHADED AREAS DETERMINED FROM FAILURE MODELS FOR: BOND WIRE
ALUMINUM
DIAMETER $\geq$ .001778 cm
LENGTH $\leq$ 0.5 cm

JUNCTION
SILICON
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS $\leq$ .032 cm

METALLIZATION
ALUMINUM
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS $\leq$ .032 cm

Figure 2–33. Composite Predictions of Worst Case Failure Levels From Bond Wire, Junction, and Metallization Models

Actual failure thresholds measured in terms of incident power are some 10 to 15 dB higher than the worst case model line. Since different drive impedances could narrow this gap, the inherent safety factor of the conservative assumptions appears warranted.

CHAPTER 3

HIGH RF POWER INTERFERENCE PEDUCTION TECHNIQUES

At present, system designers must rely on cable and enclosure shielding and filtering techniques to prevent system vulnerability to microwave signals. There are often severe penalties in terms of size, weight, and cost which give impetus to the search for other techniques for reducing vulnerability to microwave signals at the component level. Three approaches currently under investigation are:

a. screening for less susceptible components,

b. use of less susceptible circuit designs,

c. use of lossy materials.

Screening for less susceptible components implies finding a reliable indicator of relative susceptibility so that a screening procedure can be derived. Two possibilities include an RF screening technique based upon the test methods described in Chapter 4, and identification of critical parameters which can be more easily measured and/or specified. For example, both measurement and modeling show that slow speed TTL logic circuits (54L/74L family) are slightly more susceptible than higher speed circuits (54H/74H family). The difference is not great enough to be significant but the modeling and parametric analysis techniques described in Chapter 2 are expected to shed more light on such possibilities.

The use of less susceptible circuit designs is another possibility for reducing overall system susceptibility. For instance, linear ICs are more susceptible than digital ICs so use of digital circuits could be several orders of magnitude less susceptible than a linear circuit if that choice is available. Likewise, both measurement and modeling have shown that higher fanout loads on TTL devices cause the devices to be more susceptible. Again, the differences are not great enough to be significant but more detailed parametric analysis may yield suitable circuit design techniques to reduce susceptibility.

Lossy materials consist of small iron or ferrite particles imbedded in a suitable matrix material such as epoxy or silicone rubber. Such materials are available commercially in a variety of forms including solid stock and castable liquids. To use the material, the wire carrying the signal to be attenuated should be encased in the material (as closely as possible since the absorption effectiveness falls off with distance from the wire), and the attenuation of the signal will depend upon the length of the absorbing section and the frequency of the signal (the absorption generally increases with both factors). The RF absorptive materials are for the most part nonconducting. Applying these concepts to the IC susceptibility reduction problem, one can envision using such lossy material in the fabrication of IC sockets and packages, PC boards, and/or a potting material for electronic assemblies.

One example of a lossy IC socket was made using a castable resin and molding it into a 16 pin DIP socket. The mold was machined and fitted with metal clips taken from a plastic IC socket. Figure 3-1 is a photograph of the complete ferrite socket. This socket was evaluated at four frequencies using the relative susceptibilities of three different types of devices. Figure 3-2 shows the protection provided by the socket at three frequencies. At 220 MHz there was no improvement. At the highest test frequency (5.6 GHz), the protection was the highest observed. In some cases at 5.6 GHz, the protection was so high that the change in the dc parameters under RF was negligible with the socket and could not be measured.

The concept of a lossy ferrite socket can be optimized to obtain improved performance over this sample socket. However, there is a limit to the improvement available because of the allowable size of the socket. Also use of lossy material is probably not practical at this time for two reasons. First lossy material is not qualified for use on military hardware as a method of susceptibility reduction. Second, the added weight and volume of the socket make it economically impractical

on flight hardware. This reduction technique may be of use in the future but presently it is not practical.

Figure 3–1. 16–Pin Lossy Ferrite Socket

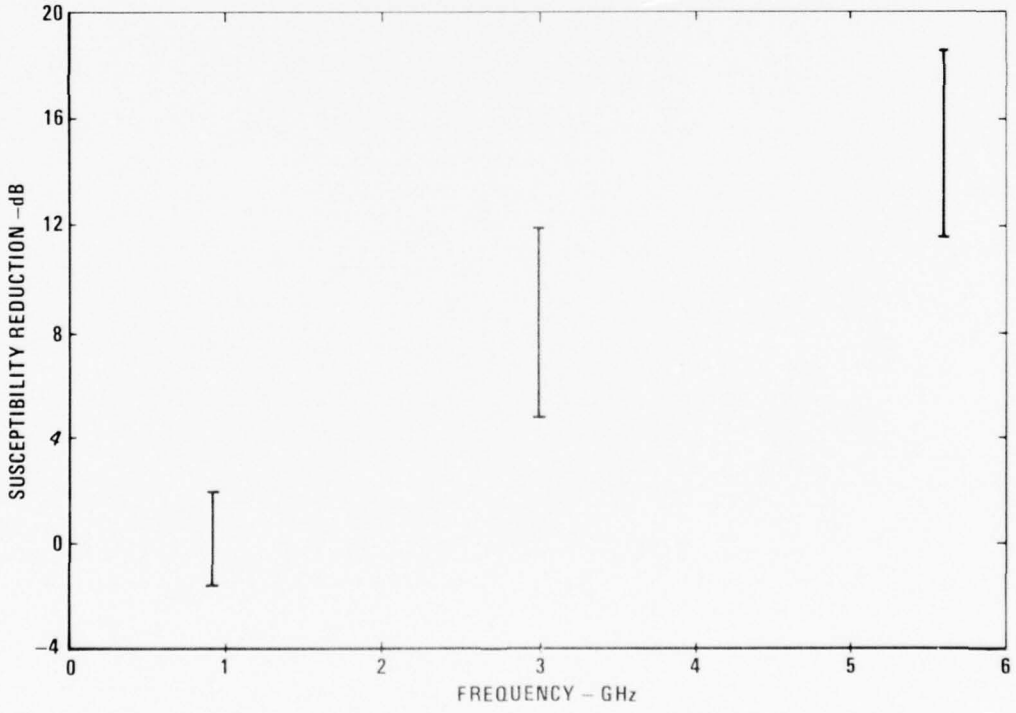


Figure 3–2. Plot of Protection from Lossy Ferrite Socket Showing Total Spread of Values Measured for 4007, 7400, and 747 ICs

CHAPTER 4

IC SUSCEPTIBILITY MEASUREMENT TECHNIQUES

The specifications for an IC susceptibility measurement system must be derived from a consideration of the IC susceptibility problem. In general ICs may receive microwave signals on any lead and in any operating condition (including unpowered). Thus it is necessary to control the microwave parameters (frequency, modulation, power level, impedance, and injection port), while providing the IC with operating voltages and currents, and monitoring device responses. Clearly a specialized test fixture is required to intermix microwave signals with the device operating signals, and a computer is needed to control experiments, acquire data, and produce understandable outputs. A block diagram of the system used to develop the IC data reported herein is shown in figure 4-1, and a photograph of the system is shown in figure 4-2. Reference 5 provides a detailed description of the system, and a brief description follows.

The IC susceptibility test fixtures (for 16 pin DIPs, 16 pin flatpacks, and 10 pin TO-5 packages) are described in figures 4-3 through 4-8. The microwave signals can be injected on any pin via bias units (described below) and a stripline RF network which interfaces with a conventional IC socket. Detailed drawings are available from the U. S. Naval Surface Weapons Center (see address in Chapter 1). The losses of both the bias units and stripline sections are calibrated at five frequencies (0.22, 0.91, 3.0, 5.6, and 9.1 GHz) so that it is possible to estimate the power absorbed in the test device when the incident, reflected, and transmitted powers are known. These powers are measured with calibrated crystal detectors which are attached at the ports other than the input port, and via directional couplers on the input port.

Device operating voltages and currents are provided via the video arm of the bias units as shown in figure 4-9. Video signals with rise times as fast as 80

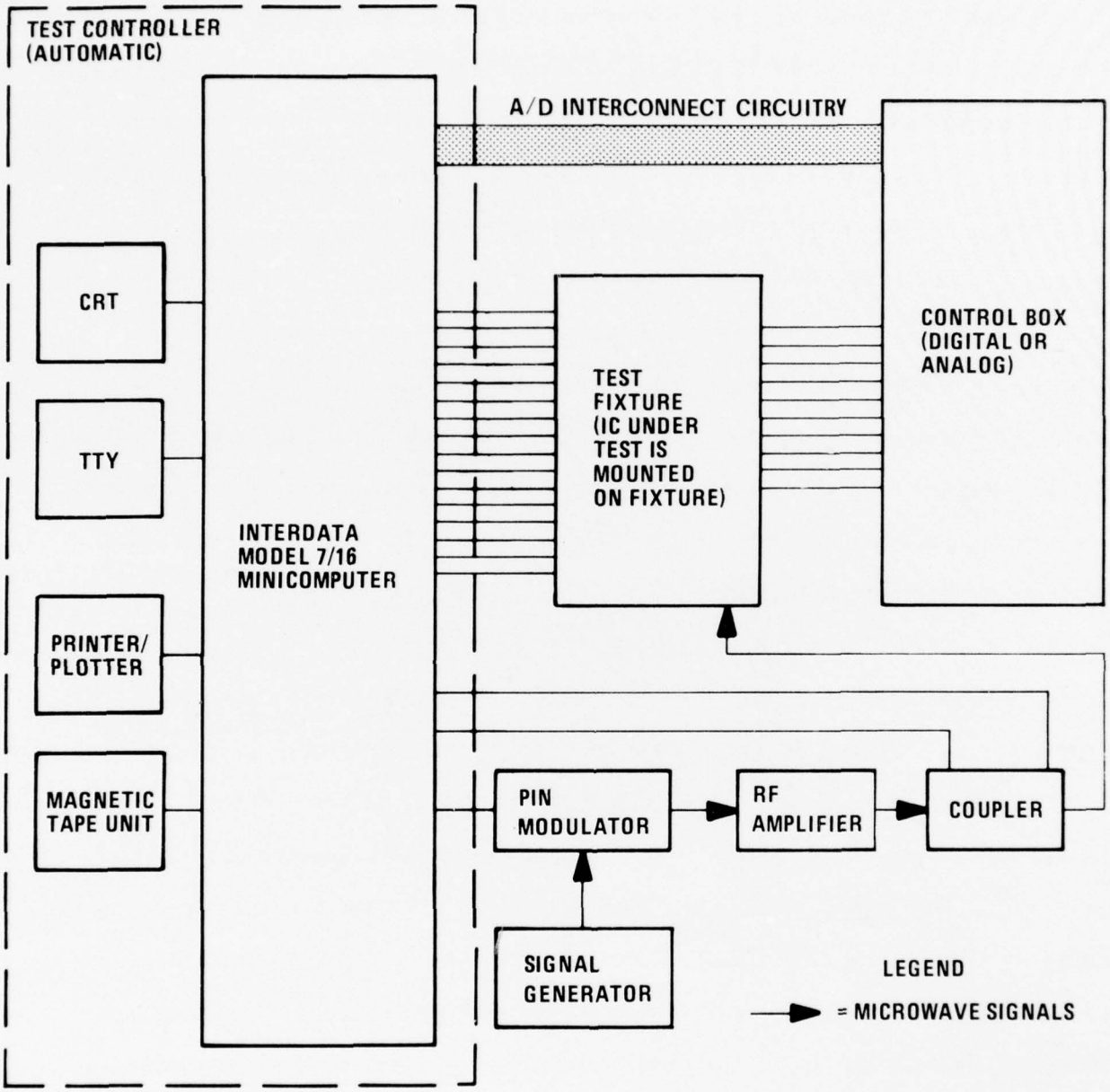


Figure 4–1. Block Diagram of IC Interference Susceptibility Measurement System with Minicomputer

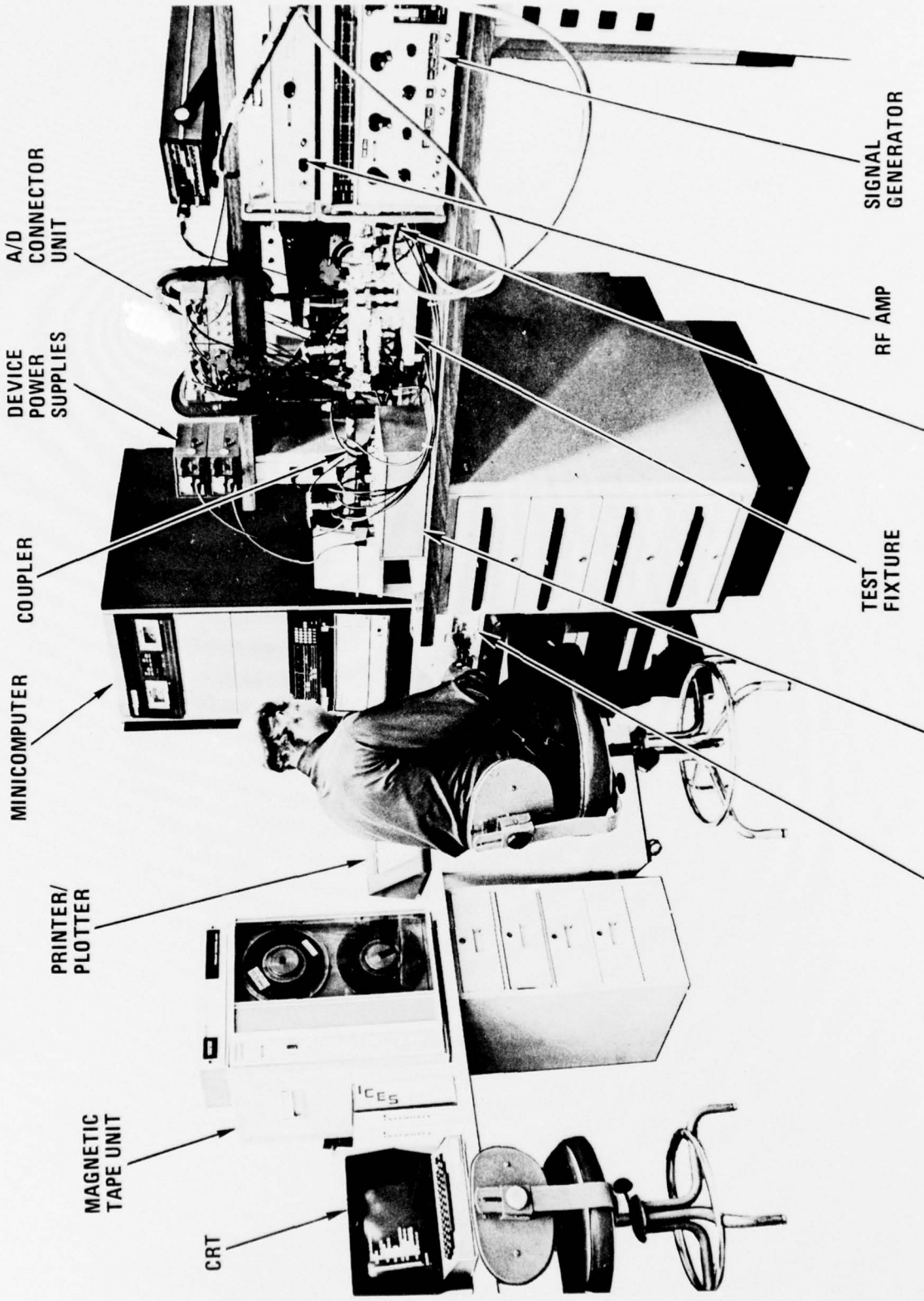
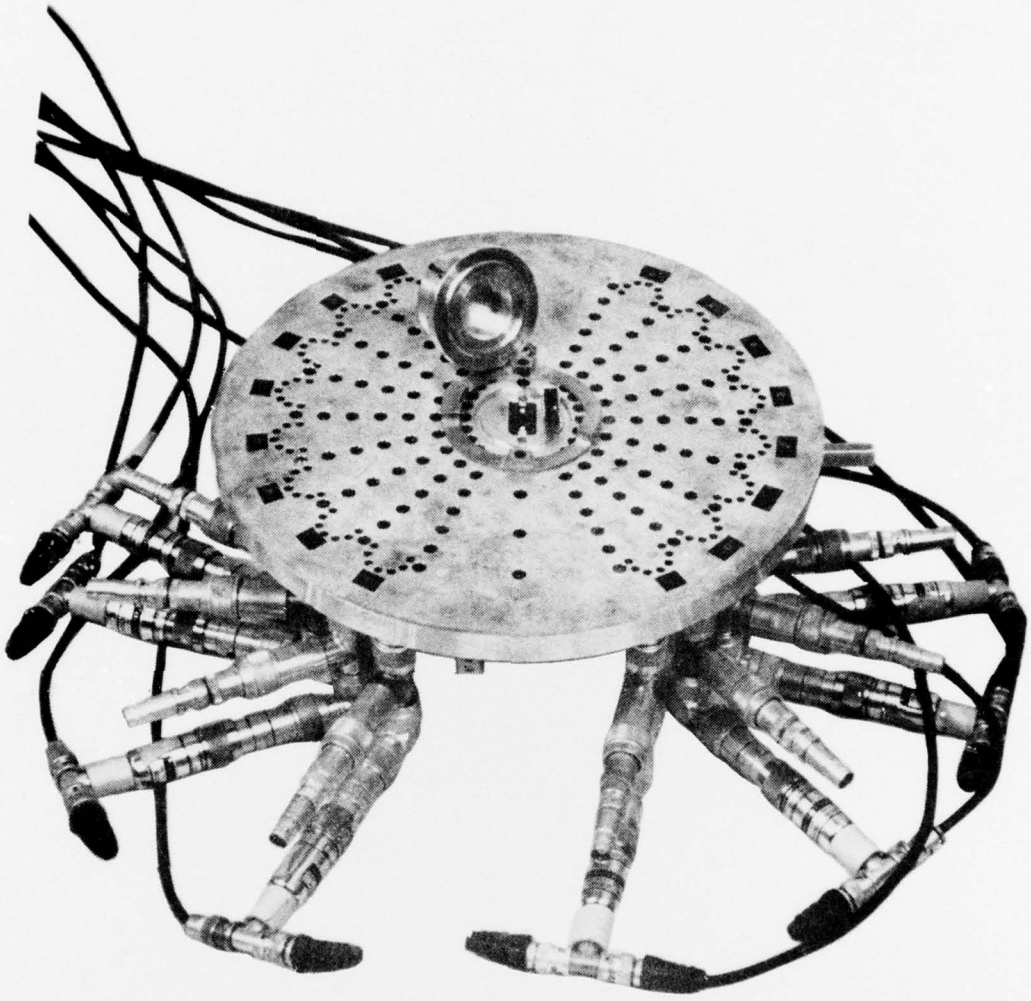
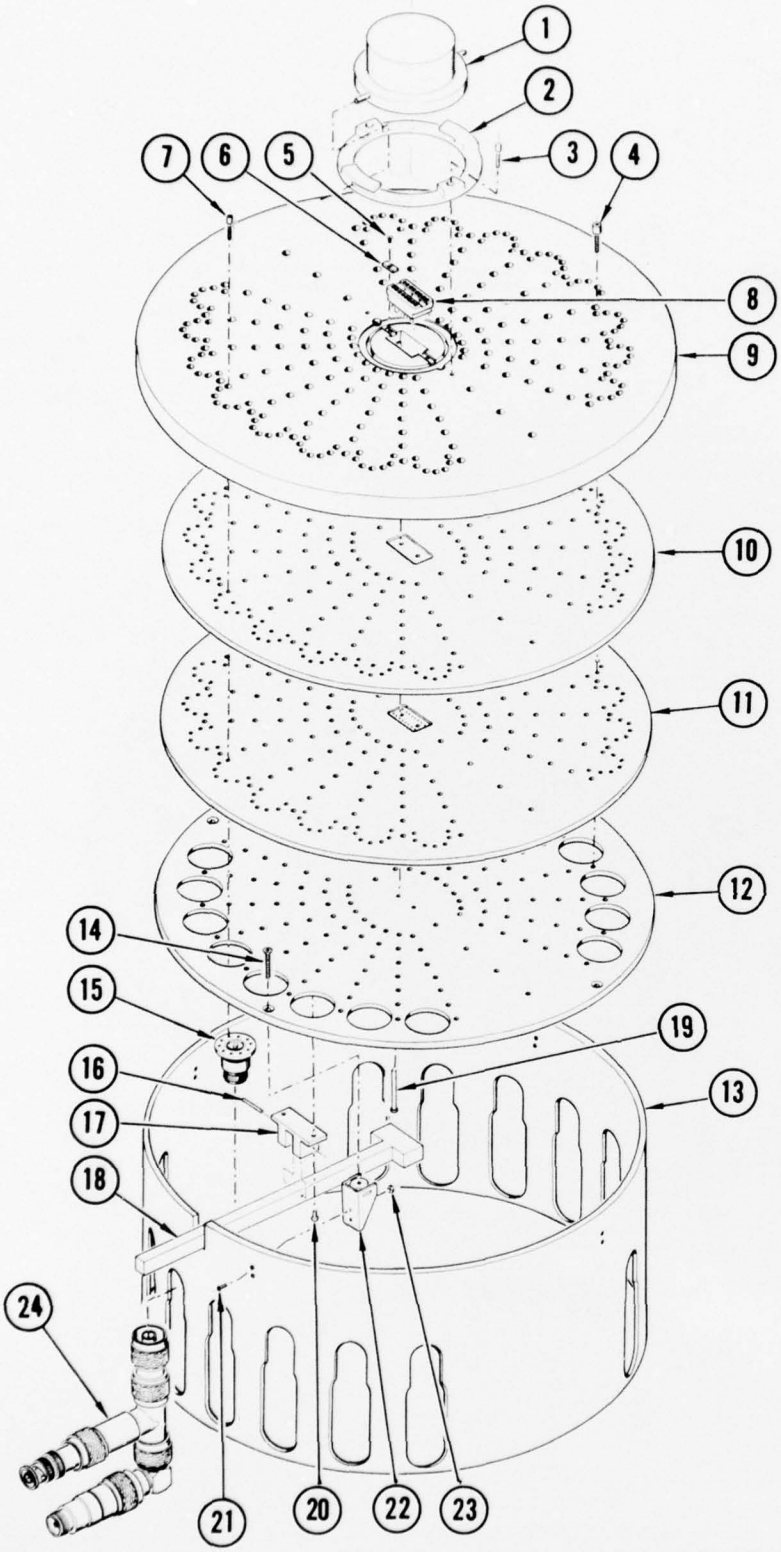


Figure 4–2. IC Susceptibility Measurement System with Minicomputer



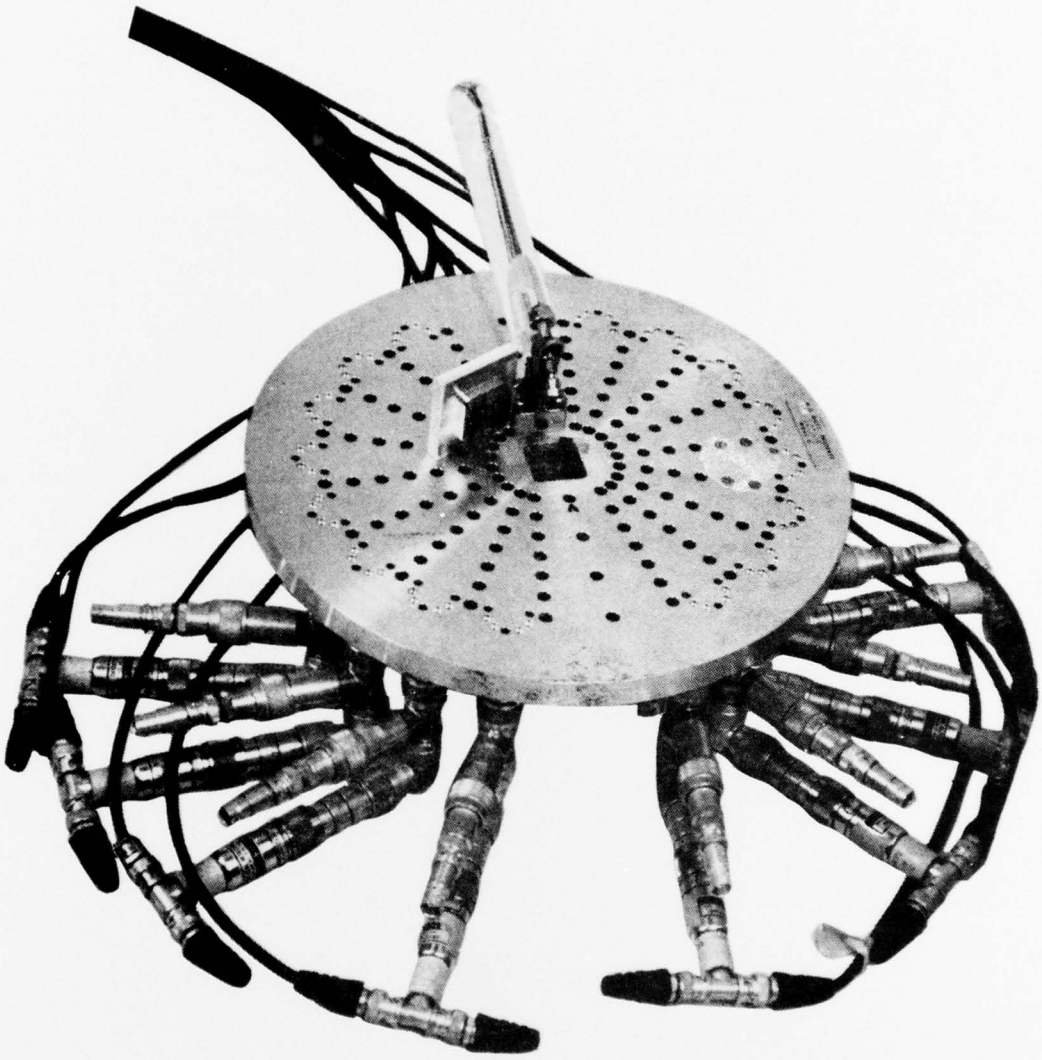
(TEST FIXTURE SKIRT OMITTED FOR CLARITY)

Figure 4–3. Dual In–Line Package Test Fixture



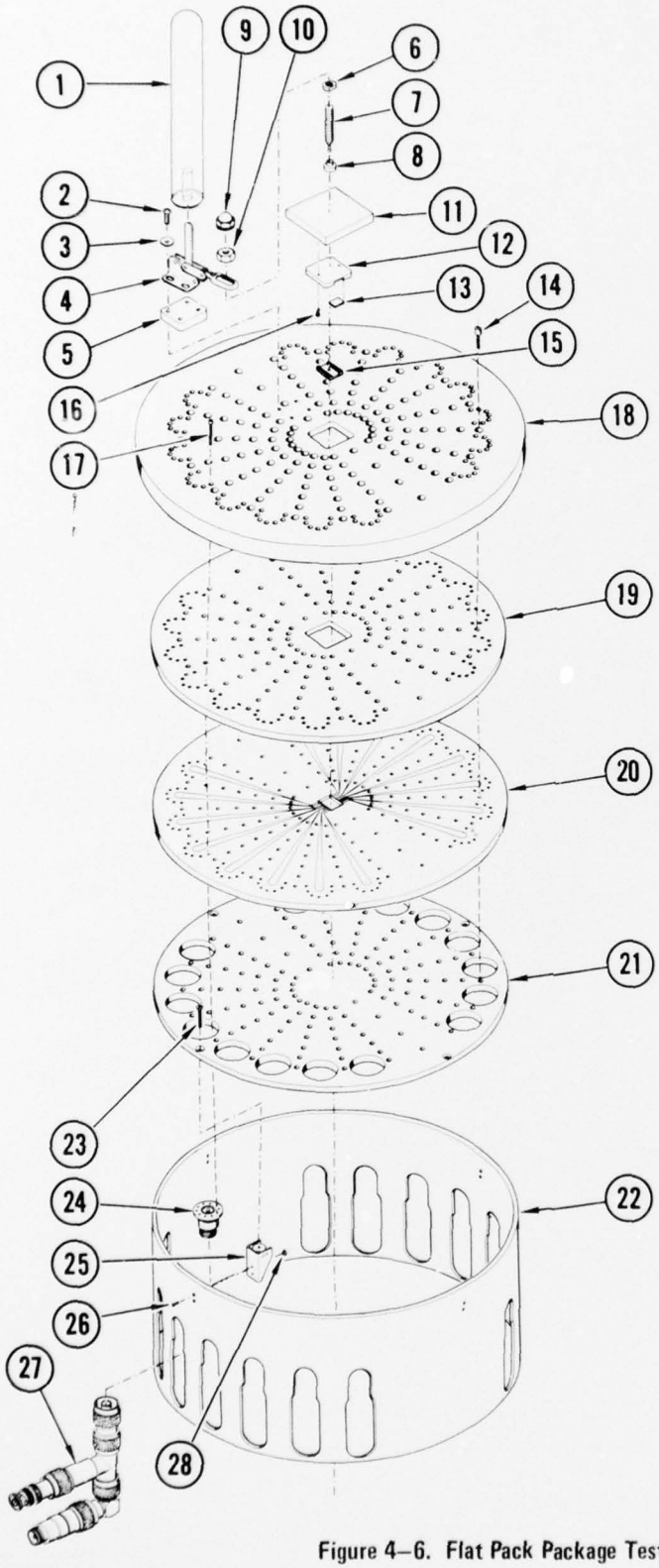
PARTS LIST		
ITEM NO.	NAME	NUMBER REQUIRED
1	COVER PLUG	1
2	SPRING LOADED HOLD DOWN	1
3	SCREW – 4–40 X 3/4	2
4	SCREW – 6–32 X 1/2	114
5	SCREW – 0–80 X 1/8	2
6	TAB	2
7	SCREW – 2–56 X 1/2	112
8	16 PIN DIP SOCKET	1
9	TOP COVER PLATE (DIP)	1
10	TOP STRIP LINE BOARD (DIP)	1
11	BOTTOM STRIP LINE BOARD (DIP)	1
12	BOTTOM COVER PLATE (DIP)	1
13	TEST FIXTURE SKIRT	1
14	SCREW 6–32 X 3/4	4
15	STRIPLINE LAUNCHER	16
16	EJECTOR PIVOT PIN	1
17	EJECTOR PIVOT	1
18	EJECTOR ARM	1
19	EJECTOR PIN	2
20	SCREW 4–40 X 1/8	2
21	SCREW 2–56 X 1/4	8
22	FASTENER	4
23	NUT 2–56	8
24	BIAS UNIT	16

Figure 4–4. Dual In–Line Package Test Fixture (Exploded View)



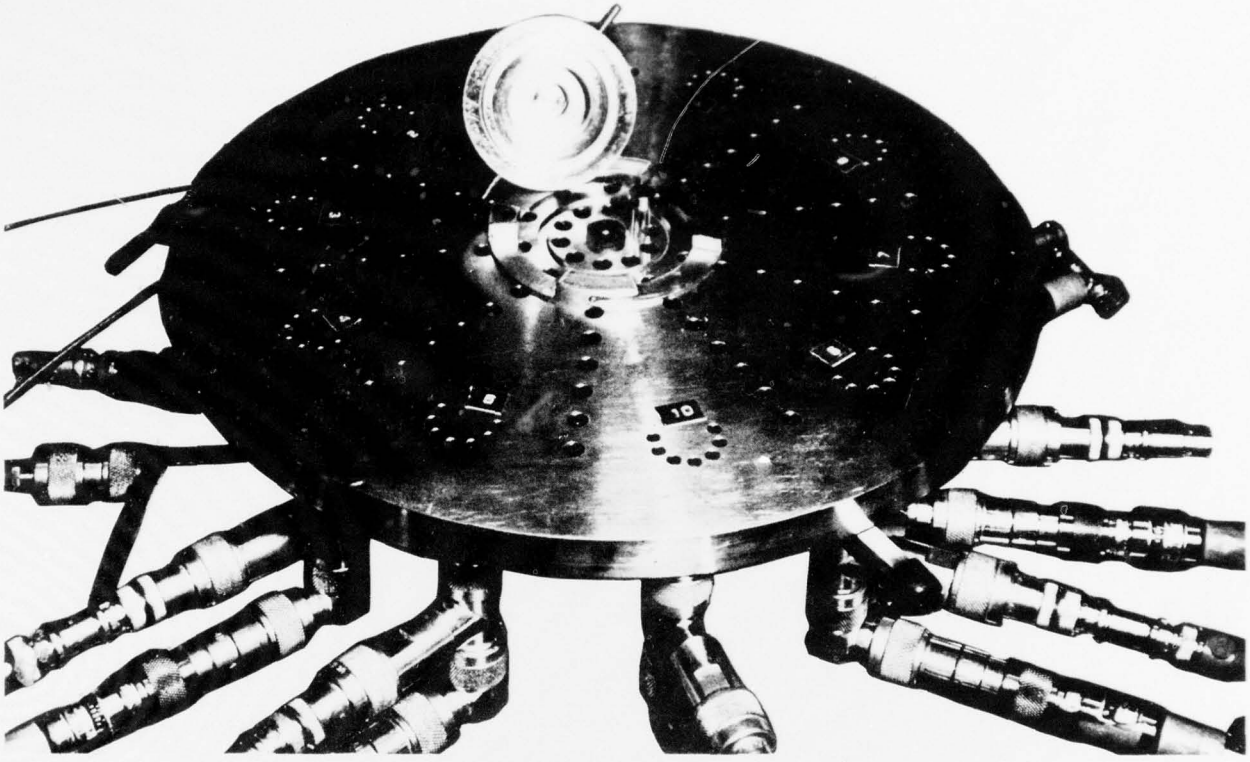
(TEST FIXTURE SKIRT OMITTED FOR CLARITY)

Figure 4–5. Flat Pack Package Test Fixture



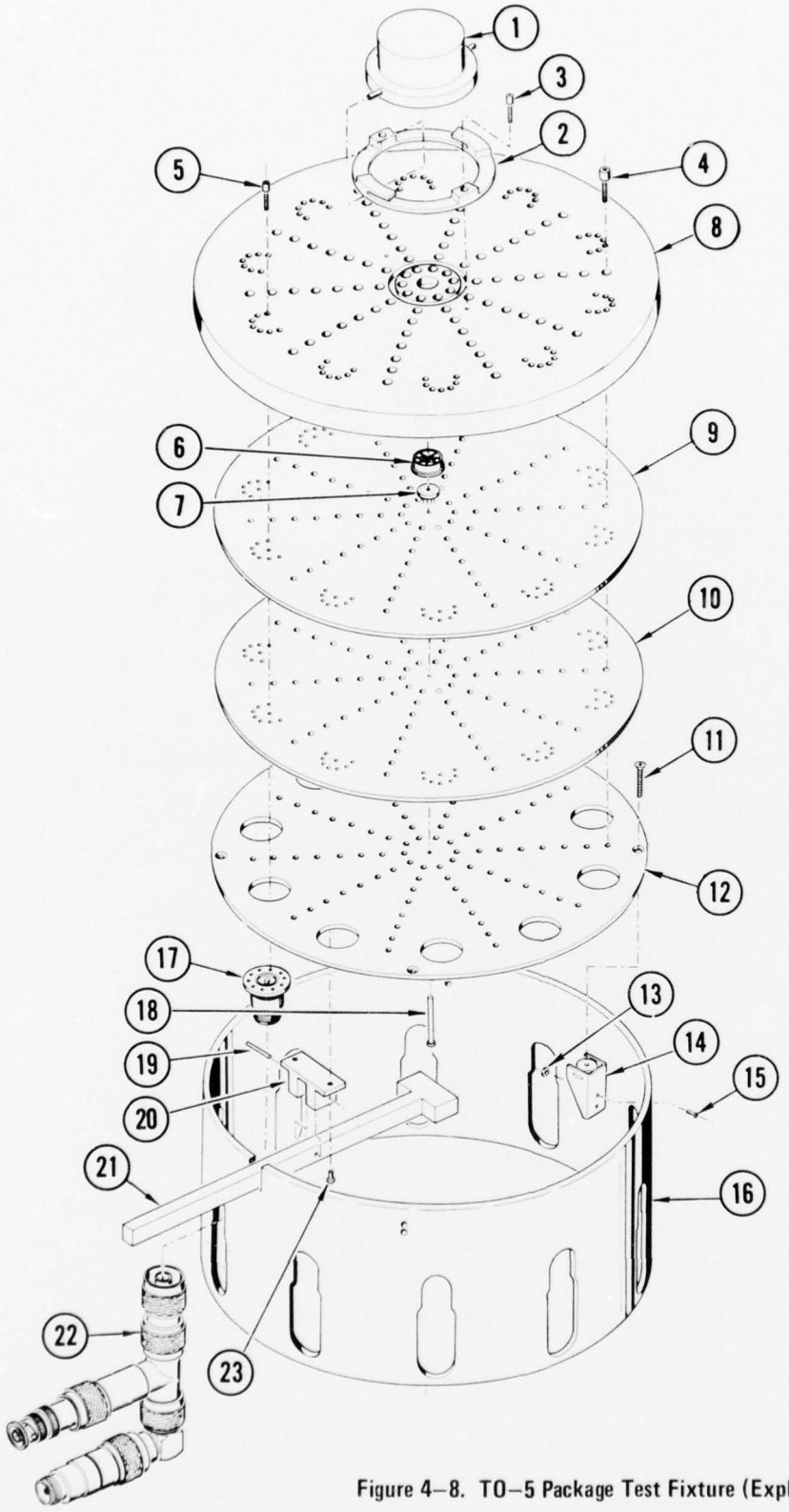
PARTS LIST		
ITEM NO.	NAME	NUMBER REQUIRED
1	PLASTIC HANDLE	1
2	SCREW 8-32 X 0.375 ROUND HEAD	4
3	WASHER FOR 8-32 SCREW	4
4	TOGGLE CLAMP	1
5	TOGGLE CLAMP BASE	1
6	NUT 10-24	1
7	COVER PLUG PRESSURE SCREW	1
8	COVER PLUG PRESSURE FOOT	1
9	CAP NUT	1
10	NUT	1
11	COVER PLUG TOP	1
12	COVER PLUG DIELECTRIC INSERT	1
13	NON CONDUCTIVE COMPRESSIVE RUBBER FOR IC LEAD CONNECTION	2
14	SCREW 6-32 X 1/2	114
15	IC LEAD LOCATOR PLUG	1
16	SCREW 8-80 X 1/4 FLAT HEAD	2
17	SCREW 2-56 X 1/2	112
18	TOP COVER PLATE (FLAT PACK)	1
19	TOP STRIP LINE BOARD (FLAT PACK)	1
20	BOTTOM STRIP LINE BOARD (FLAT PACK)	1
21	BOTTOM COVER PLATE (FLAT PACK)	1
22	TEST FIXTURE SKIRT	1
23	SCREW 6-32 X 1/2	4
24	STRIP LINE LAUNCHER	16
25	FASTENER	4
26	SCREW 2-54 X 1/4	16
27	BIAS UNIT	16
28	NUT 2/56	16

Figure 4-6. Flat Pack Package Test Fixture (Exploded View)



(TEST FIXTURE SKIRT OMITTED FOR CLARITY)

Figure 4–7. TO–5 Package Test Fixture



PARTS LIST		
ITEM NO.	NAME	NUMBER REQUIRED
1	COVER PLUG	1
2	SPRING LOADED HOLD DOWN	1
3	SCREW 4-40 X 3/4	2
4	SCREW 6-32 X 1/2	80
5	SCREW 2-56 X 1/2	70
6	TO-5 TEST SOCKET	1
7	TO-5 SOCKET	1
8	TOP COVER PLATE (TO-5)	1
9	TOP STRIPLINE BOARD (TO-5)	1
10	BOTTOM STRIPLINE BOARD (TO-5)	1
11	SCREW 6-32 X 1/2	4
12	BOTTOM COVER PLATE (TO-5)	1
13	NUT 2-56	8
14	FASTENER	4
15	SCREW 2-56 X 1/4	8
16	TEST FIXTURE SKIRT	1
17	STRIPLINE LAUNCHER	10
18	EJECTOR PIN	1
19	EJECTOR PIVOT PIN	1
20	EJECTOR PIVOT	1
21	EJECTOR ARM	1
22	BIAS UNIT	10
23	SCREW 4-40 X 1/8	2

Figure 4-8. TO-5 Package Test Fixture (Exploded View)

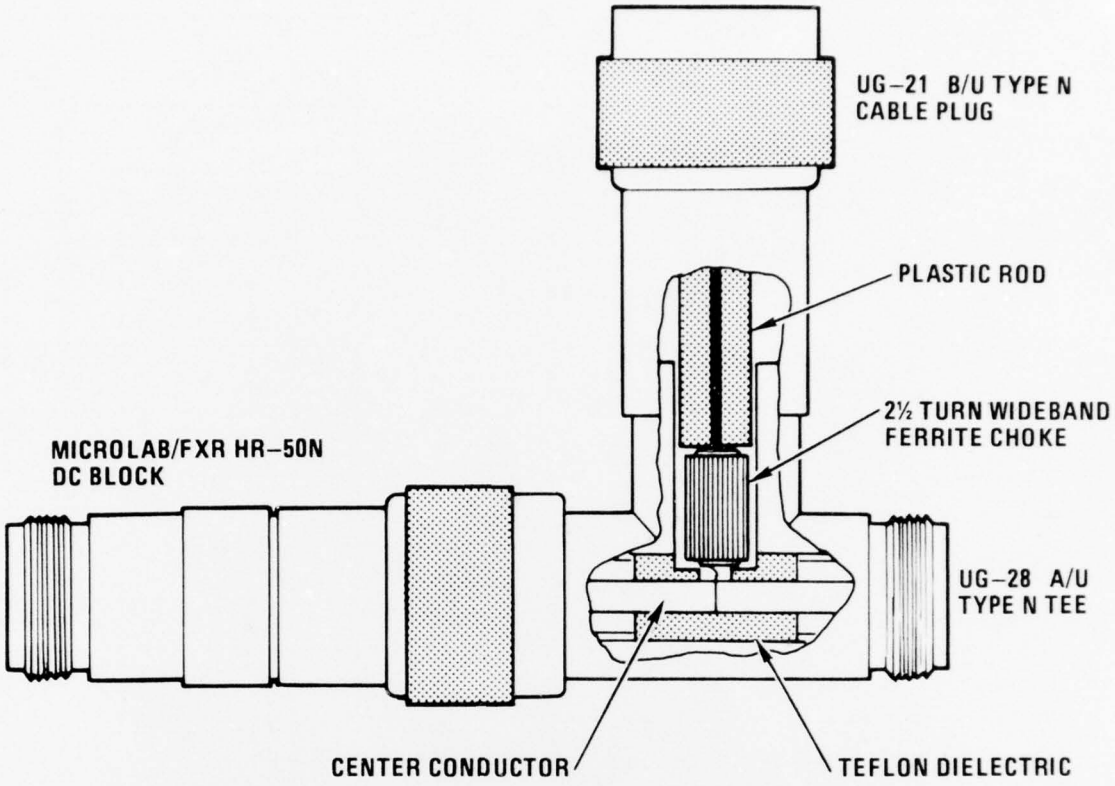


Figure 4-9. Microwave Bias Unit

nanoseconds can pass through this arm while RF frequencies below 100 MHz are effectively attenuated in the RF arm.

A minicomputer provides experiment control, data acquisition, and data analysis The computer peripherals include an A-D subsystem for reading device and crystal voltages, a D-A subsystem for controlling RF parameters and some device parameters, a printer and plotter for hard copy of data, and magnetic tape data storage. In usage, a stored program establishes test conditions, controls the RF signal level (usually 20 levels at 2 dB per step are used), reads the crystal and device voltages, applies calibration factors, analyzes the data for specific effects, and prints and stores a formatted output.

While the interference test setup described so far is a CW test, high power damage testing requires pulsed RF signals. To provide capability for single pulse testing, peak detectors were added to hold the crystal detector voltages (produced by the RF pulse) long enough for the computer to read them. Figure 4-10 shows a block diagram of the high power pulsed RF test setup.

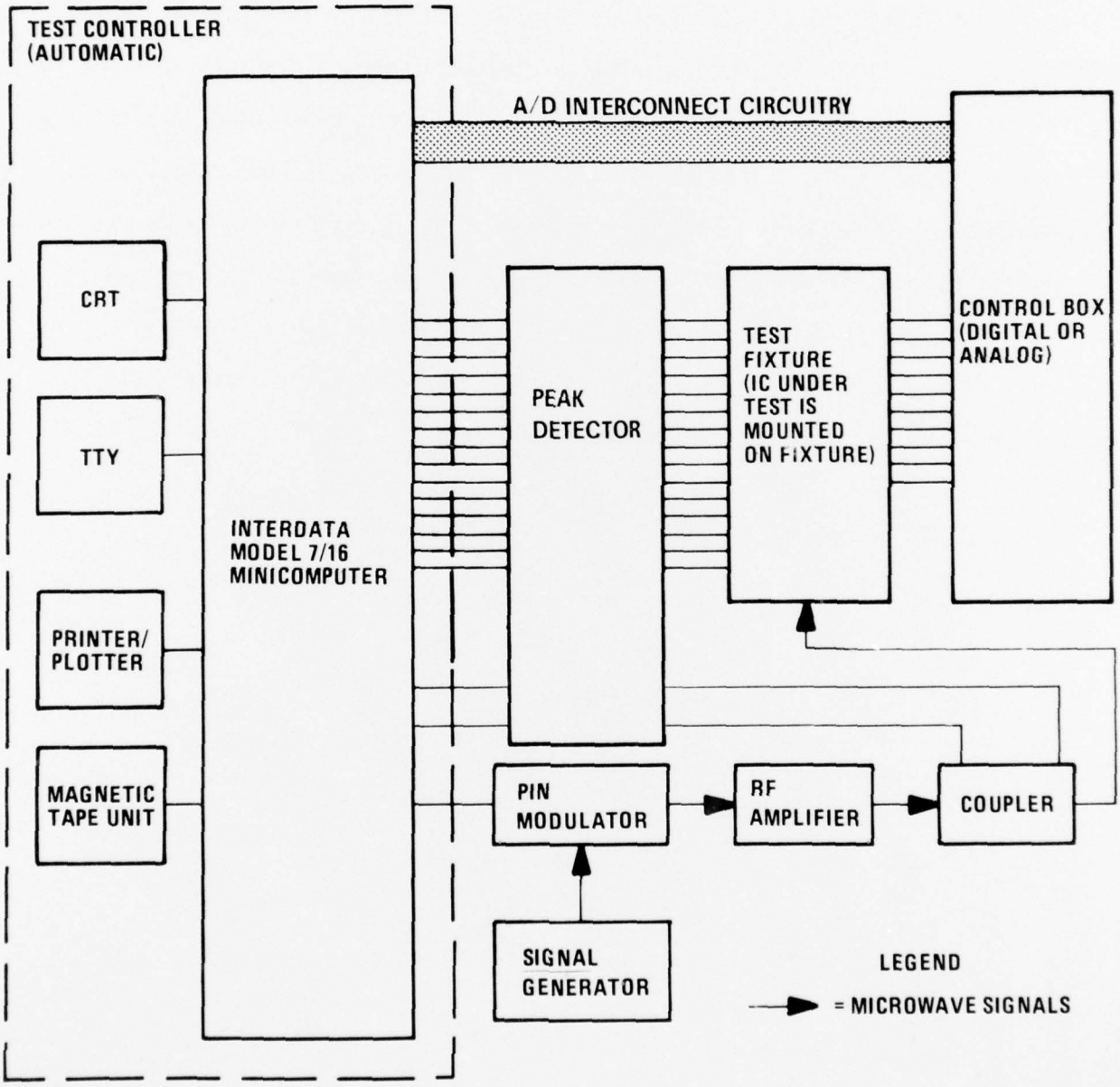


Figure 4–10. Block Diagram of IC Pulse Susceptibility Measurement System with Minicomputer

The instrumentation must be designed, built, and calibrated with great care as there are many pitfalls in the path to a reliable system. Calibration of losses, couplers, and crystals is dependent upon the frequency, and the non-linear nature of the ICs leads to generation of harmonic signals which are in turn dependent upon the power level. The signal seen by the peak detectors depends upon the impedance of the device under test, and the impedance often changes abruptly at the instant of a failure in the device. Large values of reflected and/or transmitted power in the system can lead to problems of comparing small numbers whose uncertainties are on the same order as the values themselves. The measurement system described is a research tool which permits all the variables of IC susceptibility to be studied (including statistical variables), hence, it may be too powerful for ordinary IC susceptibility jobs. A simpler and less costly measurement system could be developed as a viable solution to determining IC susceptibilities, especially for devices which do not yield to analytical treatment.

CHAPTER 5

REFERENCE MATERIAL

5.1 This chapter provides a list of all the documents used as sources of information in the preparation of this report. The MDC documents are reports published by McDonnell Douglas Astronautics Company - East. The sources are:

1. MDC E0595, "Integrated Circuit Electromagnetic Susceptibility Investigation - Study Phase Report", dated 5 May 1972.

2. MDC E0690, "Integrated Circuit Electromagnetic Susceptibility Investigation - Development Phase Report", dated 19 October 1972.

3. MDC E0883, "Integrated Circuit Electromagnetic Susceptibility Investigation - Interim Report No. 1", dated 24 August 1973.

4. MDC E0981, "Integrated Circuit Electromagnetic Susceptibility Investigation - Interim Report No. 2", dated 28 December 1973.

5. MDC E1099, "Integrated Circuit Electromagnetic Susceptibility Investigation - Test and Measurement Systems", dated 14 July 1974.

6. MDC E1101, "Integrated Circuit Electromagnetic Susceptibility Investigation - MOS NAND Gate Study", dated 26 July 1974.

7. MDC E1102, "Integrated Circuit Electromagnetic Susceptibility Investigation - Pulse Interference Study", dated 12 July 1974.

8. MDC E1103, "Integrated Circuit Electromagnetic Susceptibility Investigation - Package Effects Study", dated 12 July 1974.

9. MDC E1123, "Integrated Circuit Electromagnetic Susceptibility Investigation - Bipolar NAND Gate Study", dated 26 July 1974.

10. MDC E1124, "Integrated Circuit Electromagnetic Susceptibility Investigation - Bipolar Op Amp Study", dated 9 August 1974.

11. MDC E1125, "Integrated Circuit Electromagnetic Susceptibility Investigation - MOS/Hybrid Study", dated 9 August 1974.

12. MDC E1126, "Integrated Circuit Electromagnetic Susceptibility Investigation - Susceptibility Survey Study", dated 9 August 1974.

13. MDC E1261, "Integrated Circuit Electromagnetic Susceptibility Investigation - RF Injection Test of Government-Owned Circuits", dated 30 June 1975.

14. MDC E1513, "Integrated Circuit Electromagnetic Susceptibility Investigation - Technical Report No. 1", dated 4 June 1976.

15. MDC E1515, "Integrated Circuit Electromagnetic Susceptibility Investigation - IC Handbook - Draft 1", dated 4 June 1976.

16. MDC E1667, "Integrated Circuit Electromagnetic Susceptibility Investigation - Technical Report No. 2", dated 3 June 1977.

17. L. W. Nagel and D. O. Pederson, "SPICE (Simulation Program with Integrated Circuit Emphasis)", Memorandum No. ERL-M382, Electronics Research Laboratory, College of Engineering, University of California, Berkeley, 94720, 12 April 1973.

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NSWC/DL TR-3654	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Integrated Circuit Electromagnetic Susceptibility Investigation - Phase III IC Susceptibility Handbook - Draft 2		5. TYPE OF REPORT & PERIOD COVERED 6. PERFORMING ORG. REPORT NUMBER MDC E1669
7. AUTHOR(s) J. M. Roe, et. al.		8. CONTRACT OR GRANT NUMBER(s) N60921-76-C-A030
9. PERFORMING ORGANIZATION NAME AND ADDRESS McDonnell Douglas Astronautics Company - East P. O. Box 516 St. Louis, MO 63166		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62762N, XF54585 XF54585.B02, DF98(A)
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Electronic Systems Command Research and Technology Directorate Washington, DC 20360		12. REPORT DATE 3 June 1977 13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Naval Surface Weapons Center Dahlgren Laboratory (Code DF-56) Dahlgren, VA 22448		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A
16. DISTRIBUTION STATEMENT (of this Report) Approved for Public Release; Distribution Unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) EMV Integrated Circuit Microwave EMI Hardening RF Susceptibility		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The objective of this handbook is to provide system designers with integrated circuit (IC) susceptibility information in terms of microwave signals. This is the second draft of the IC Handbook for comments from eventual users. The comments on the first draft have been studied and incorporated where possible. The data in this handbook include both interference and damage susceptibility. Both types of susceptibility are evaluated through modeling and testing. Both digital and linear ICs are covered in the handbook. This version includes →		

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20.
all data available at the end of the second of three increments. The handbook explains the electromagnetic vulnerability (EMV) hardening approach for electronic systems. On the component level susceptibility reduction techniques such as lossy ferrite materials and screening for less susceptible devices are included. The handbook includes a description of the automated measurement system used to take and analyze the IC susceptibility data. This handbook will provide designers with actual test data when available and modeling techniques to determine susceptibility information where no test data are available.

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