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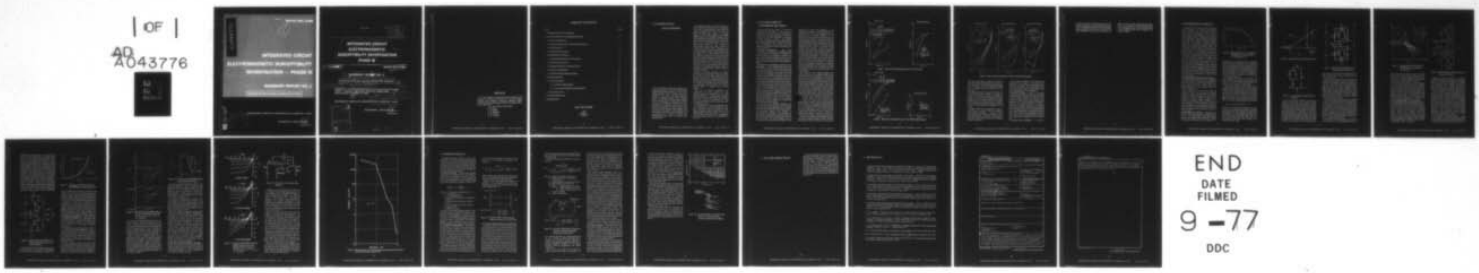

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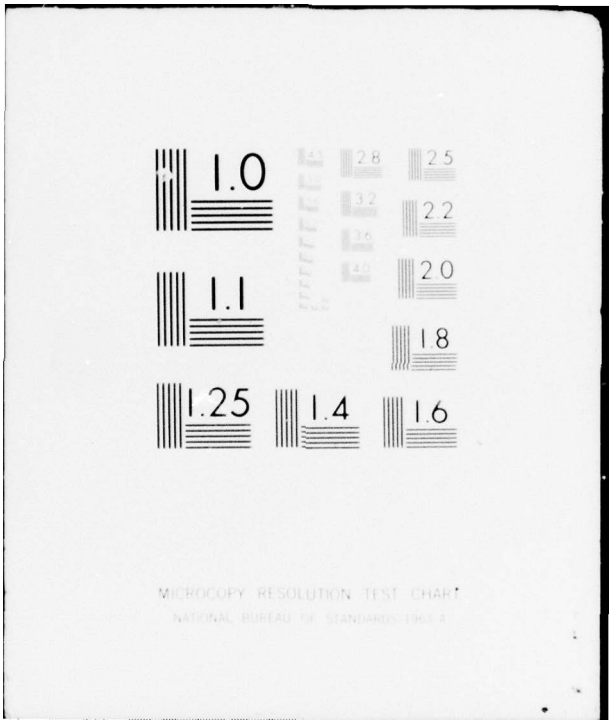
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REPORT MDC E1668

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION — PHASE III

SUMMARY REPORT NO. 2

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MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST

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C. R. /Chubb
C. N. /Kohlberg
C. E. /Larson

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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE III

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(9) SUMMARY REPORT NO. 2

APPROVED FOR PUBLIC RELEASE: DISTRIBUTION UNLIMITED

(12) 23p.

(16) XF54585 (17) XF54585B02

SUBMITTED TO THE CONTRACTING OFFICER, U.S. NAVAL SURFACE WEAPONS CENTER – DAHLGREN LABORATORY, DAHLGREN, VIRGINIA, 22448
UNDER CONTRACT NO. N60921-76-C-A030

(15) (19) (18) NSWC/DL TR-3653

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST
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PREFACE

The work reported in this document was performed under Contract No. N60921-76-C-A030 for the U.S. Naval Surface Weapons Center, Dahlgren Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

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C. N. Kohlberg
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1. INTRODUCTION AND SUMMARY

The work described herein was performed by McDonnell Douglas Astronautics Company-East (MDAC-EAST) under contract to the U.S. Naval Surface Weapons Center / Dahlgren Laboratory (NSWC/DL). It is part of an ongoing program seeking to understand high power microwave effects in a cost effective manner. This Integrated Circuit Electromagnetic Susceptibility (ICES) contract is concerned with microwave effects in semiconductor integrated circuits (ICs). This document summarizes the work performed in the second of three increments, which together, form the third and last phase of this program. The ICES effort is directed toward characterizing IC susceptibilities to microwave energy and identifying possible means of reducing these susceptibilities.

The primary output of the ICES effort is an ICES Handbook which provides IC susceptibility information to system designers. This information consists of susceptibility models and data. The ICES Handbook also contains a complete approach to the Electromagnetic Vulnerability (EMV) problem and a detailed example of using the IC information to determine the system shielding requirements. During the second increment, Draft 1 of the ICES Handbook[1], which was issued after increment 1, was reviewed by potential users. Part of this review occurred at a seminar held in October 1976. In response to the comments received, the ICES Handbook has been revised and Draft 2 is being issued in parallel with this report. This revision includes new models and updated test data from the work performed during the second increment. The review cycle for Draft 2 of the ICES Handbook[2] will include an expanded mailing list, and all those who have shown interest in the IC susceptibility problem will receive a copy. Approximately 500 names are included in the mailing list. Another seminar is planned for the fall of 1977 for further review and comment of Draft 2.

During the second increment the bipolar junction transistor RF effects model was refined. This model is an Ebers-Moll model modified to include the RF effects observed during a large amount of RF testing of diodes and transistors. This model has been used with SPICE (Simulation Program with Integrated Circuit Emphasis) as an example of how RF effects in ICs can be modeled using a standard circuit analysis program.

The study of damage susceptibility was completed in the second increment. A large testing program was performed to study each damage mechanism — junction failure, metallization failure, and bond wire failure. Also a general worst case model was generated for each mechanism based on heat flow as each mechanism is thermal in nature.

The feasibility of various susceptibility reduction techniques was reviewed during this increment. The value of device screening and circuit design techniques require further study as the modeling effort continues. However, the use of lossy material, such as ferrite, as a susceptibility reduction technique, appears to be impractical at this time.

2. IC SUSCEPTIBILITY HANDBOOK REVISION

During increment one, Draft 1 of the ICES Handbook was designed. It was issued to potential users for their comments, criticisms, and suggestions as to content and format. During increment two, the users responded in a generally favorable manner to Draft 1 with specific comments and suggestions. Their responses have been incorporated into Draft 2 wherever possible. Also the modeling and test data have been updated to include the work performed during the second increment.

2.1 **System Considerations** — From initial comments it was obvious that a detailed example for using the IC Susceptibility Handbook was needed. Therefore, an example to determine the total system shielding requirements with a given EM environment was created and presented at Seminar I, and is included in the ICES Handbook, Draft 2.

2.2 **Component Susceptibility Information Requirements** — In the susceptibility information section of the revised handbook there have been several major changes: (1) the individual graphs showing the data spread by frequency have been removed; (2) all graphs and models have been changed to show estimated minimum RF power; (3) the graphs of the susceptibility criteria for digital devices have been changed and (4) the composite graphs for digital devices with high and low output states have been combined into one graph.

The individual graphs which showed the data spread for each frequency have been removed in answer to several comments that they were confusing and unnecessary. Originally these graphs were provided to give designers some idea of the best case susceptibility for ICs but this does not appear to be of much use. Since the worst case susceptibility levels were shown on the composite graphs, the composite graphs were retained and the individual graphs deleted.

For the worst case approach adopted in the handbook, the quantity of interest is the minimum amount of RF power (defined as power available from the source) which will produce the unacceptable component response. The estimates of minimum power contained in the handbook are derived from measurements on statistical samples of ICs and on theoretical considerations based on physical models. The data measured with the measurement scheme described in Chapter 4 of the handbook must have the dependence on the measurement technique removed because it is recognized that the IC susceptibility level may depend upon the driving impedance of the microwave source (whether a laboratory source or a cable or wire exposed to a microwave field). One useful approach has been to determine the amount of power dissipated within the package since it can be postulated that reflection losses and external dissipation losses could be minimized under suitable tuning conditions. Likewise, the failure models are derived in terms of power dissipated in the failure site. The use of absorbed power as an estimate of minimum power is conservative since it is probably not possible to match the driving source to a nonlinear load such as a semiconductor junction; and it is likely that losses in diverse parts of the IC chip are inevitable. To minimize the very real danger of producing over-cautious estimates, the degree of conservatism in the handbook predictions has been estimated and these estimates are made clear to the reader and user of the handbook.

The format of the composite graphs also brought comments that for digital devices whichever output state is susceptible is irrelevant and only the worst case susceptibility is important. Therefore the composite graph for TTL devices and the composite graph for CMOS digital devices include both the high and low output states. Draft 1 had separate composite graphs for each output state, but Draft 2 has one graph which includes both states. The susceptibility criteria for these two-state composites have also been changed to reflect both states and to make the criteria more useful. Draft 2 has criteria whose values are tied to [illegible]fication limits wherever possible. For [illegible]le, the criteria for TTL devices used in [illegible] 1 were .4, .6, and .8 volt for the low output state and 2.4, 2.2 and 2.0 volts for the high output state. In Draft 2 the combined criteria values are .4 or 2.4 volts (the guaranteed specification limit for a low or high state), .8 or 2.0 volts (the edge of the .4 volt noise margin), and 2.0 volts or 0.8 volt (a guaranteed switch from the low or high state, respectively). Figures 1 through 3 show the revised composite graphs as they appear in Draft 2.

In Draft 2 several interference models have been presented, including a bipolar junction transistor model with RF effects, which can be used with a

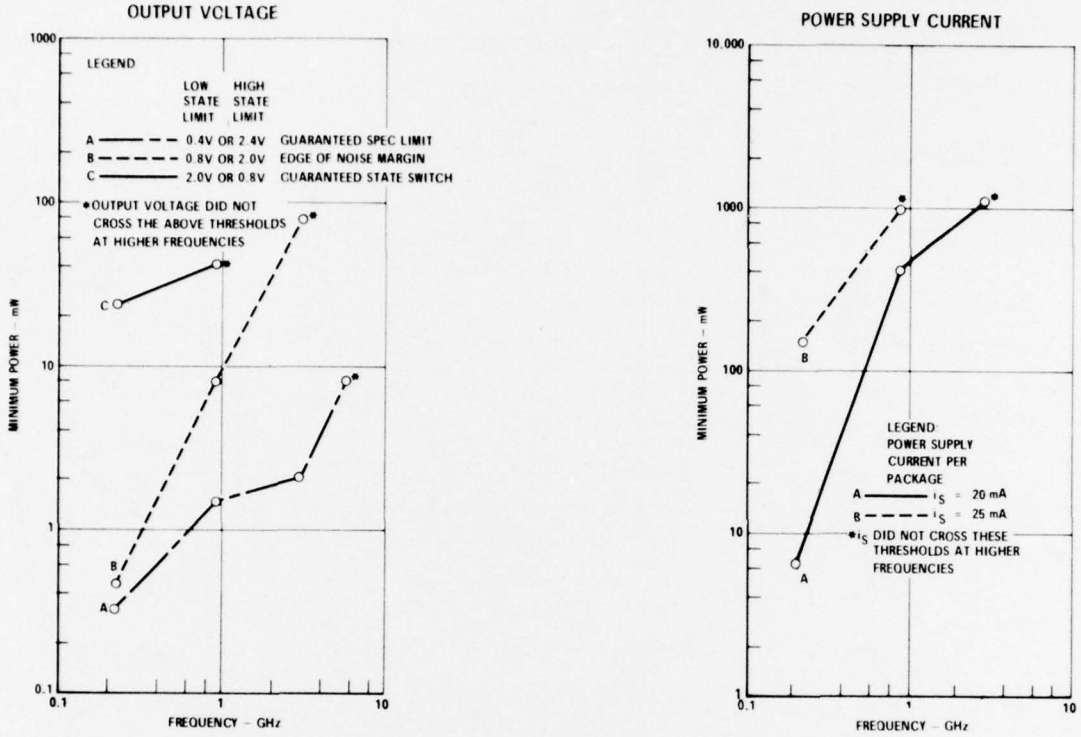


Figure 1. Worst Case Susceptibility Levels For TTL Devices

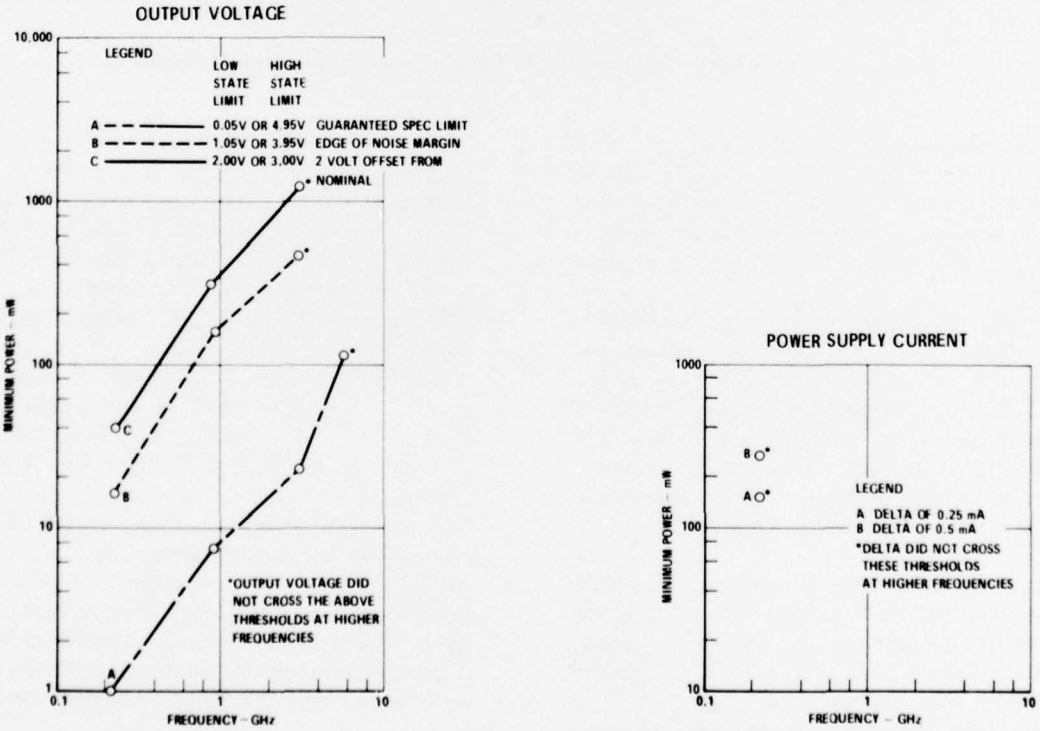


Figure 2. Worst Case Susceptibility Levels For CMOS Digital Devices

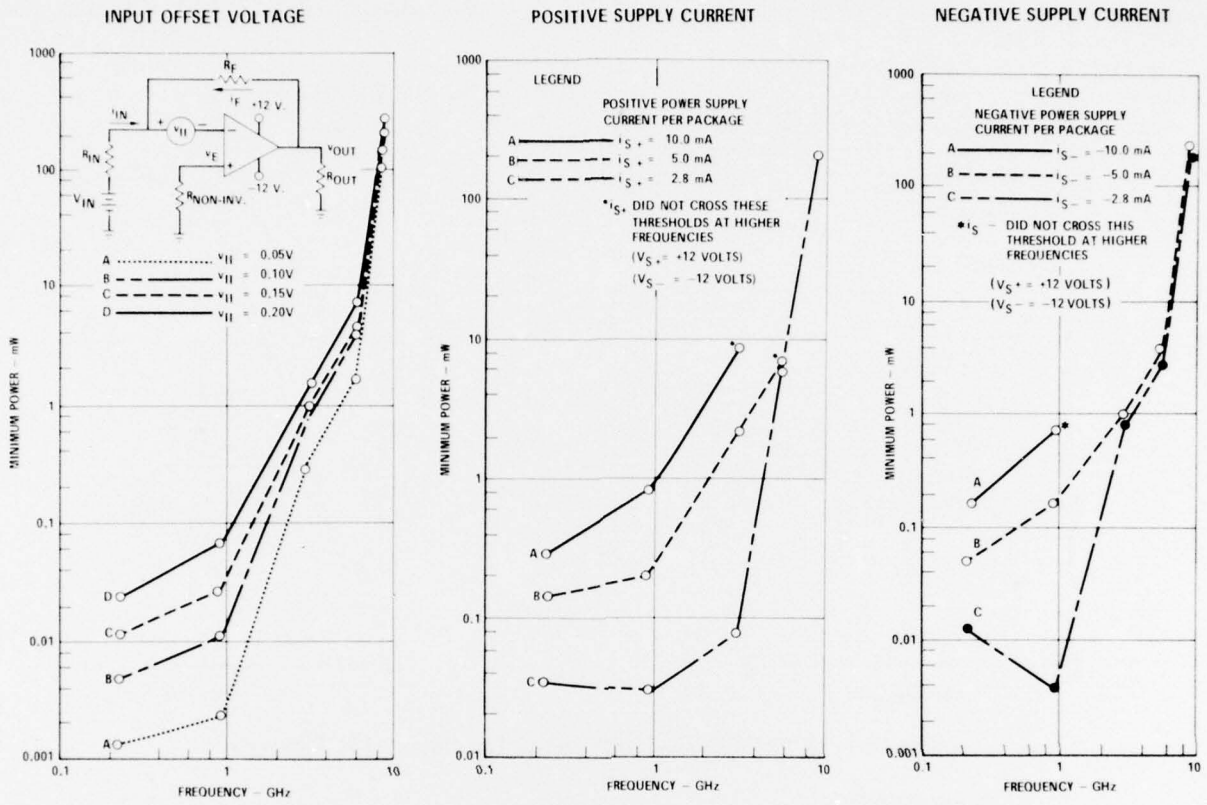


Figure 3. Worst Case Susceptibility Levels For Operational Amplifiers

circuit analysis program to model ICs, and an op amp input model. These models are intended to serve as analysis tools for the designers who want to go more deeply into the susceptibility problem than is possible using the worst case data presented.

The bipolar transistor model with RF effects is an Ebers-Moll model modified to include the effects of the RF. This model is described in Chapter 3. The op amp input model uses an offset generator in the inverting input lead to simulate the RF effects on the input circuitry. The translation from RF power to input voltage is empirical in Draft 2 and is presented in Chapter 3 of this report.

Damage models are also presented in Draft 2 which were not in Draft 1. There is a model for each damage mechanism — junction failure, metallization failure, and bond wire failure. Since these mechanisms are thermal, each model is derived from the heat flow equation with differing boundary conditions.

The preliminary MOSFET model presented in Chapter 3 of this report is not ready for the handbook at this time. More effort is required to study the RF effects on the MOSFETs, both testing and analysis, before a final model is ready to be incorporated into the handbook.

2.3 Outline Revisions — There is one major outline revision in Draft 2 which occurs in Chapter 2. The breakdown of Chapter 2 was by device class in Draft 1 (digital devices and linear devices). Each class of devices had its own interference and damage section. During the extensive testing performed in the second increment, all types of damage were grouped according to mechanism rather than by class of device and this regrouping led to the logical step to revise the outline according to type of susceptibility (interference and damage). This revision was accomplished with the class of devices as the subheading for the interference section and the damage section covering all ICs.

2.4 Further Review Planning — In order to

increase the number of reviewers for Draft 2, the external mailing list has been expanded. All those who have expressed an interest in the IC susceptibility problem will receive a copy of Draft 2 of the ICES Handbook for review and comment. In addition, another seminar is planned for the fall of 1977 to get comments of users firsthand along with any suggestions for the third and final draft of the handbook which will be issued in the summer of 1978.

3. INTERFERENCE EFFECTS

The goals of the interference effects investigation are twofold: 1) to catalog the interference effects in integrated circuits to provide useful information to system designers, and 2) to gain a more complete understanding of the origin of these interference effects. Regarding the first goal, the susceptibilities of the TTL family of digital devices and of the bipolar operational amplifier family have been studied in detail in previous reports [3-5]. In regard to the second goal, the understanding of observed interference effects has increased to the point where it is now possible to form models for the interference effects in integrated circuits. The interference mechanism, which has been documented previously[3], is the rectification of RF signals in the pn junctions of the integrated circuit. Models are initially shown for the rectification effects in diodes and transistors, the simplest semiconductor devices; then the models are extended to 4-layer (IC construction) devices and MOSFET devices. Through a computer program intended for circuit analysis, the transistor model is applied to model the case of RF entering the output of a TTL device, with the output in a low state. Op amps are modeled for the case of RF entering the input by using a small-signal approach.

3.1 Large Signal Rectification in PN Junctions — Small signal detection theory does not adequately account for many of the effects observed since the microwave signal may be of large amplitude. A large signal rectification theory has been developed based on a time-domain analysis of junction waveforms.

This rectification theory is valid across the frequency band as it accounts for junction capacitance. Due to this capacitance the rectified current in a junction decreases as the frequency increases as shown in figure 4. Plotted is the amount of rectified current produced by a 2N2369A base-collector diode at an RF power of 80 mW and $V_D = 0$. The rectification does not decrease significantly up to a frequency of approximately 40 MHz; above 40 MHz the rectification decreases rapidly, and is decreased by a factor of 100 at 2 GHz.

3.2 RF Effects in Transistors — Transistors respond to RF signals through rectification which occurs in the base-emitter and base-collector junctions. The effect of the rectification is to make the transistor characteristic curves change. It is

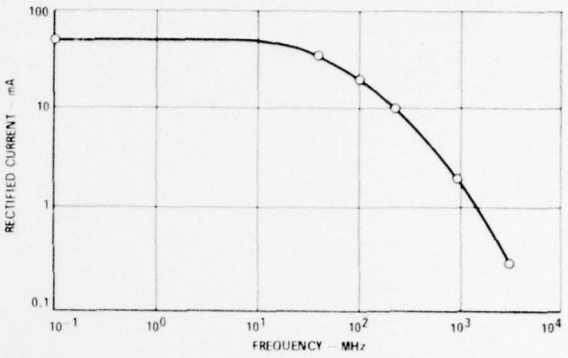


Figure 4. Rectified Current vs. Frequency For 2N2369A Base-Collector Diode ($P = 80$ mW, $V_D = 0$)

probable that a time-domain type of calculation would account for the effects, but this approach would be unwieldy and of little practical use. A transistor model has been developed which is both powerful and practical. It can be used with existing computer-aided circuit analysis programs to analyze interference in circuits. An extension of the method allows an analysis of RF effects in 4-layer pnpn structures.

In modeling RF effects in transistors, the approach taken was to start with an existing transistor model, the Ebers-Moll representation, and modify it to account for the RF effects.

Under RF, a diode I-V characteristic has a somewhat piecewise linear behavior which can be approximated by summing the two curves shown in figure 5. The solid line represents the dc diode characteristics, while the dashed line represents the effect of RF energy on the diode. A circuit which realizes the curves of figure 5 is shown in figure 6. Diode D1 is assumed to be the dc diode, having a current-voltage characteristic given by

$$i_{D1} = I_o (\exp (qv_{D1}/kT) - 1)$$

where Io is the diode reverse saturation current. D1 produces the solid line of Figure 5, while the left branch of the circuit produces the dashed line. Diode D2 acts as a switch, allowing current to flow through the Norton equivalent only when it is "on". The voltage at which the diode turns on is determined by the open circuit voltage of the Norton equivalent, $i_X R$.

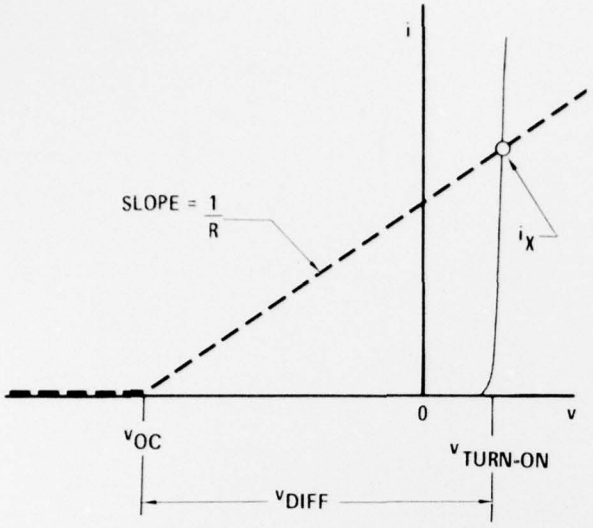


Figure 5. Approach Used to Model Diode Curves

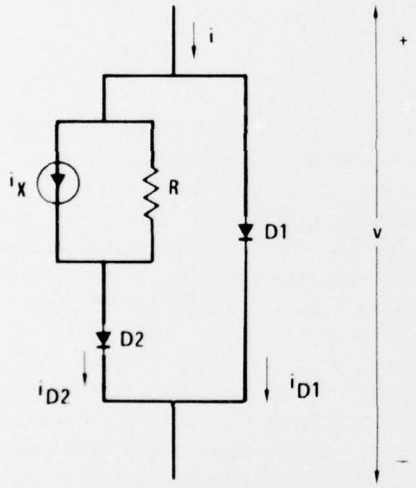


Figure 6. Circuit Model of Diode Under RF Influence

The Norton generator elements, i_X and R, are functions of RF power and frequency. Experimental results show that, in general, R is constant for different RF power levels at a given frequency, but that i_X varies with the microwave power level.

By inserting the diode model into the Ebers-Moll representation, a model for the transistor with RF stimulus is obtained. Figure 7 shows the modified Ebers-Moll transistor model. This model is valid as long as the RF stimulus does not affect the beta of the transistor (as in the case of RF injection into the collector). For RF injection into

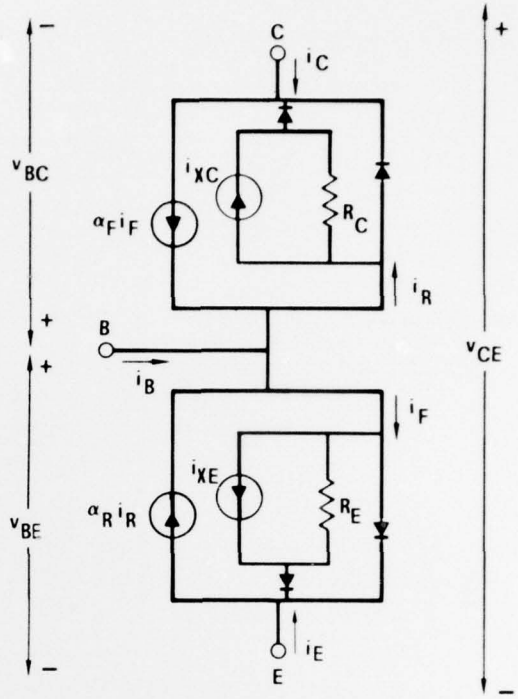


Figure 7. Modified Ebers-Moll Model For A Transistor Under RF Influence

the base of the transistor the beta will change. For some transistors the change is significant for low levels of RF power.

Figure 8 shows a plot of beta vs. RF power at 220 MHz on the base for several transistors. For the 2N930 and 2N930A, beta begins to decrease at less than .1 mW of RF power, and decreases quite rapidly, reaching one-tenth of its original value at approximately 3 mW. Other transistors do not show a significant beta decrease until about 1 mW of RF power is reached, and decrease less rapidly than the 2N930 and 2N930A. To date, no general quantitative relationship exists between changes in beta and RF power level.

The modified Ebers-Moll model can be applied to transistors with RF energy entering the base if α_F and α_R are allowed to vary as the RF power is increased. This means that the forward and reverse alphas (or equivalently, the betas) must be treated as functions of RF power. Once the betas or alphas ($\alpha = \beta/(\beta+1)$) are determined, the RF diode characteristic curves can be obtained. At present, a logarithmic polynomial curve fit may be the best way to characterize beta vs. RF power, since no general relation exists.

A proposed 4-layer pnpn structure model[6] is shown in figure 9. It is an expanded version of the

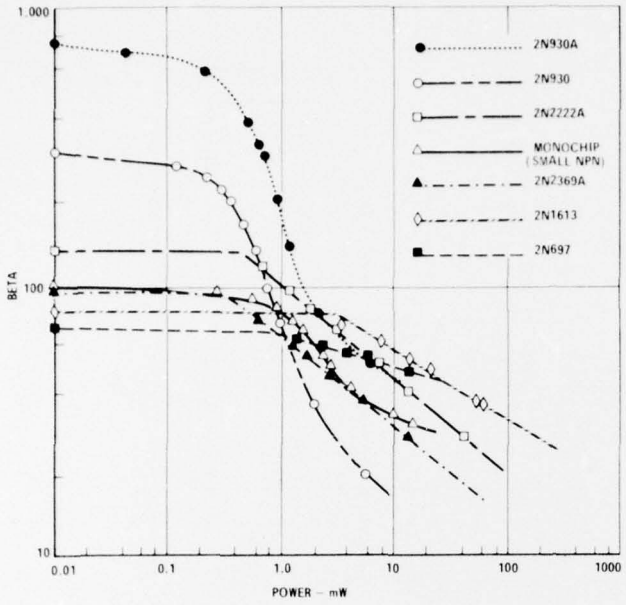


Figure 8. Transistor Beta As A Function of 220 MHz RF Power Conducted Into The Base

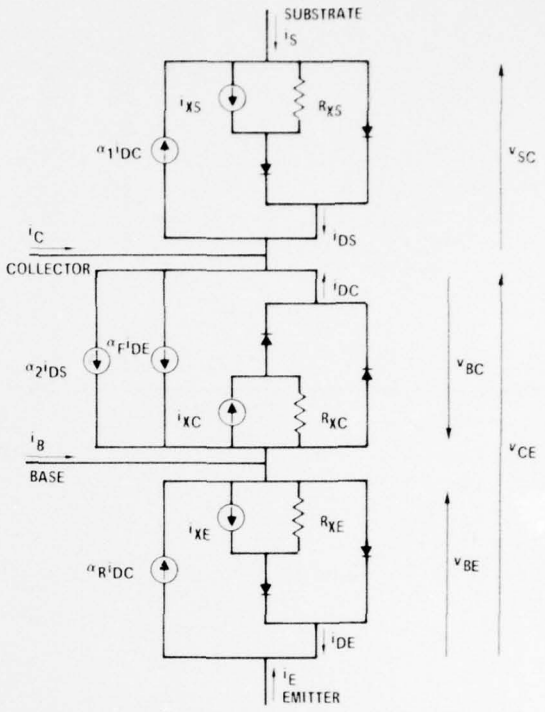


Figure 9. Proposed Model For RF Interference In Four Layer Structures

Ebers-Moll transistor model, with an extra diode to account for the substrate-to-collector junction, and two extra current-controlled current sources to account for coupling between the substrate-to-collector and base-to-collector junctions.

The diode RF characteristic curves obtained from a given transistor vary with the transistor bias. For example, if the base current is changed, the diode curves may also change. However, for small to moderate changes in transistor bias, the change in diode curves is slight. Therefore, when modeling circuits using the modified Ebers-Moll transistor model (figure 7), the transistor parameters should be obtained at or near the transistor's operating point for best accuracy.

3.3 Modeling RF Effects in Integrated Circuits — The semiconductor models described earlier can be used to model RF effects in more complex circuits. Of special interest in this report is integrated circuit modeling. Integrated circuits typically contain many devices, including transistors, diodes, resistors, and capacitors, and their analyses can become quite complicated. For this reason, use can be made of any of several available computer programs intended for circuit analysis. These include CIRCUS, CORNAP, ECAP 2, NET 2, SCEPTRE, SLIC, and SPICE.

Modeling interference effects in integrated circuits is illustrated using SPICE in this report. SPICE[7] (an acronym for Simulation Program with Integrated Circuit Emphasis) is a versatile, general purpose circuit analysis program. It performs dc analysis, ac analysis, and transient analysis of linear or non-linear electronic circuits.

The circuit example is the 7400 NAND gate, for the case when RF enters the output with the output low (its most susceptible configuration). The adaptation of the modified Ebers-Moll transistor model for SPICE is shown, while an RF effects model for the TTL output-low case is developed. When RF energy is conducted into the NAND gate output, with output low, it is postulated that most of the interference effect occurs in the output transistor. In this case, the RF energy enters the collector of the transistor. The RF effects produced can be accounted for in the 7400 by replacing the output transistor with the modified Ebers-Moll model shown in figure 7.

The modified Ebers-Moll transistor model shown in figure 7 is a general model which cannot be implemented directly in SPICE. SPICE does not accept current-controlled current sources, so

modifications must be made to accommodate the current sources labeled $\alpha_F i_F$ and $\alpha_R i_R$. SPICE does, however, accept voltage-controlled current sources, so the addition of resistors to sense currents i_F and i_R will allow the model to be accepted. Figure 10 shows the modified Ebers-Moll model adapted for SPICE by the addition of two one ohm current-sensing resistors, RCSENSE and RESENSE. The value of one ohm was chosen because it is small enough that circuit operation is not likely to be upset, and has the additional property that the voltage drop across the resistor is numerically equal to the current flow through it. The voltage VGEN can be swept by SPICE to simulate RF effects over a range of RF power levels. In figure 10, VGEN is an independent voltage source shown to the right of the transistor model. For example VGEN could be stepped from .2 volt to 20 volts in .2 volt steps. The corresponding range of P_{RF} would be .1 mW to 1000 mW.

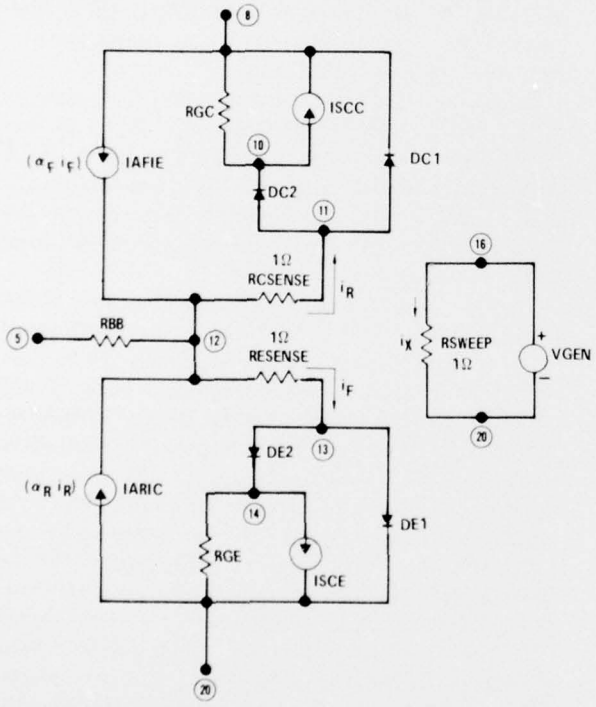


Figure 10. Modified Ebers-Moll Model In An External Model Configuration For SPICE Simulation

The results of the 7400 NAND gate simulation are shown in figure 11 compared to measured data for a 7400. The output voltage is plotted as a

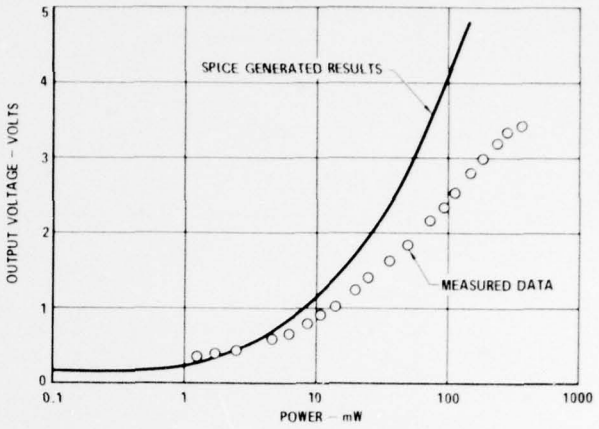


Figure 11. Comparison of SPICE Simulation of 7400 NAND Gate to Measured Results

function of RF power incident on the output. The shape of the curve is the same as that for the measured case, although the SPICE simulation predicts a higher output voltage at high levels of RF power than is actually measured. This may occur because all of the RF power was assumed to be incident on the output transistor. This assumption is conservative, however, since it is unlikely that all of the RF power incident on the output will reach the output transistor. RF impedance mismatches will result in some power being reflected, and of that being absorbed, some will be absorbed by other elements within the integrated circuit besides the output transistor.

3.4 RF Effects in MOSFETs — Like their bipolar counterparts, MOSFETs are also affected by RF. The pn junctions at the drain-to-substrate and source-to-substrate interfaces are rectification sites for RF just as the bipolar transistor junctions are.

When RF energy is conducted into the drain of an n-channel or p-channel MOSFET, the i_D vs v_{DS} characteristic curves change. This effect is similar to the RF effects seen in junction diodes and bipolar transistors. Rectification, which was the mechanism in the case of transistors and diodes, is also the mechanism of the interference in MOSFET devices.

The i_D vs v_{DS} curves for an MFE 3003 p-channel MOSFET are shown in figure 12 for the cases where no RF, 110 mW and 220 mW of RF power are incident on the drain. As the RF power increases, the drain current becomes less negative, especially at the high drain-to-source voltages. It

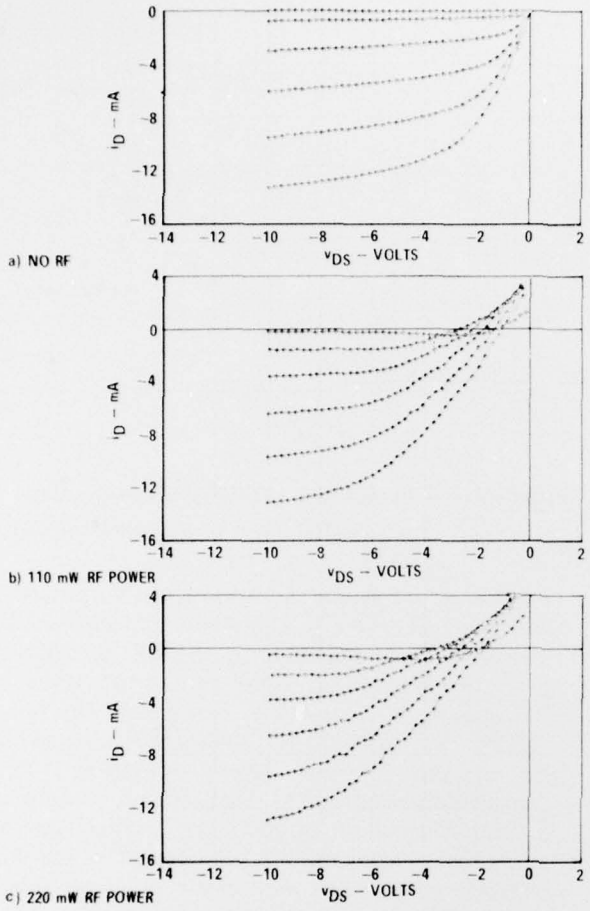


Figure 12. MFE 3003 P-Channel MOSFET Characteristics With 220 MHz Conducted Into Drain (v_{GS} = 0, –4, –5, –6, –7, –8 volts)

is necessary to model the rectification in the junctions in order to model the RF effects in the device. A simplification occurs for the case where the source and substrate are at the same potential and RF energy enters the drain, because the primary rectification effect occurs in the drain-to-substrate diode, so that it becomes necessary to model the rectification in that junction only.

Figure 13 shows a MOSFET model for RF entering the drain, where the drain-to-substrate diode has been modified to include rectification. Diode D1 is equivalent to the normal drain-to-substrate diode, and for simplicity, diode D2 is also assumed equivalent. Resistor R_X and current source i_X determine the interference characteristics of the device. Both are obtained from plots of rectification in the diode under RF stimulus, as was shown in figure 5.

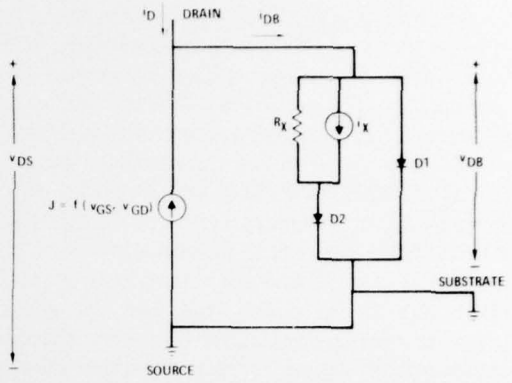


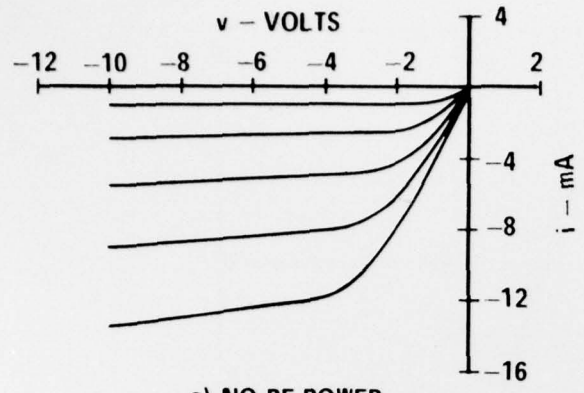
Figure 13. Proposed P-Channel MOSFET Model For RF Conducted Into Drain

In order to model the interference effects in the MFE 3003 MOSFET, first the no RF case was modeled to obtain an adequate model for normal operation, then the additional elements were added to account for rectification in the drain-to-substrate diode. A model similar to that used in SCEPTRE[8] was used to calculate the i_D vs v_{DS} curves shown in figure 14a.

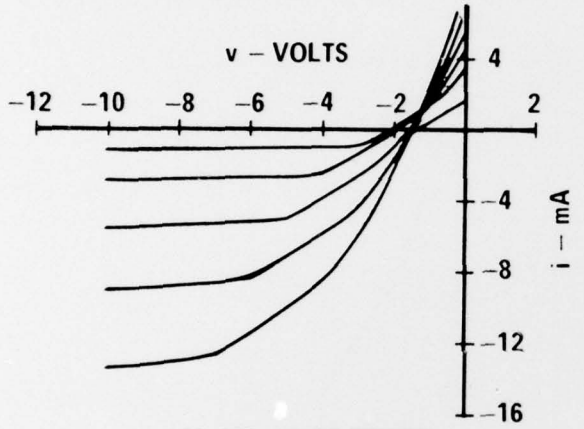
To account for rectification in the drain-to-substrate diode, the model shown in figure 13 was used. Figures 14b and 14c show the i_D vs. v_{DS} curves calculated from the MOSFET model at 110 mW and 220 mW of RF power incident on the drain. The agreement with the measured curves of figures 12b and 12c is good.

There are differences between regular MOSFETs and the FETs in a CMOS IC. One difference is the use of an n-type substrate in CMOS so that n-channel devices must be located in a p-well which forms a parasitic diode in the substrate. Another difference is the addition of a protective resistor and diode combination to the gate circuitry in CMOS to protect the gate oxide from static electricity. Since the RF rectifies in pn junctions, these additional junctions are paths for the RF and the RF-generated currents to flow. These additional paths have been observed under RF testing. The observed currents in these junctions cause the CMOS FETs to behave slightly differently from the simple MOSFETs. Further investigation of these effects will be carried out in the next increment.

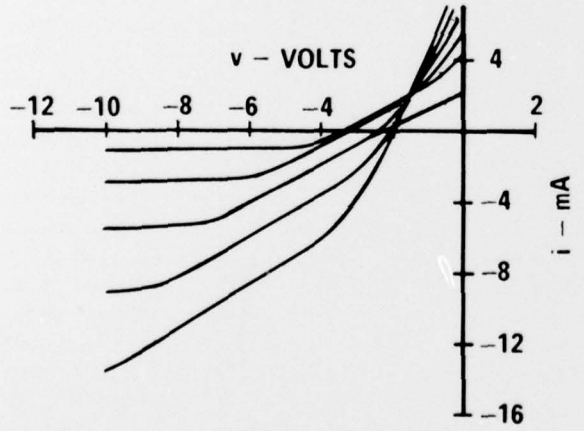
3.5 RF Effects Model for Bipolar Op Amps — During the second increment the available data on bipolar op amps have been studied in more detail. An input offset generator model for op amps was presented previously[5]. It will be repeated here with additional supporting data.



a) NO RF POWER



b) 110 mW RF POWER



c) 220 mW RF POWER

Figure 14. Simulation of MFE 3003 P-Channel MOSFET Characteristics With 220 MHz RF Power Conducted Into Drain (v_{GS} = 0, –4, –5, –6, –7, –8 volts)

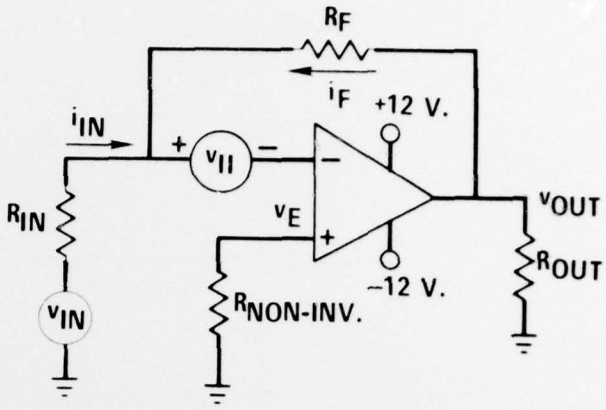


Figure 15. OP Amp Circuit Including Offset Generator

Available op amp interference data show that the voltage at the inverting input terminal, v_{II}, varies significantly with the applied RF signal. In normal operation, this voltage is very near zero volts (a "virtual ground") due to the negative feedback used in typical circuit applications. Modeling the nonideal performance of the amplifier under interference conditions as an ideal differential amplifier with a series offset generator in the inverting input leg achieves a very satisfactory explanation of all the observed interference effects in the 741.

Figure 15 shows an op amp circuit with the addition of the offset interference generator. The voltage v_{II} provided by this generator to the inverting input is a function of the RF drive signal as shown in the observed data. From figure 15, the voltage and current equations can be derived. These equations show v_{OUT} in terms of v_{IN} and v_{II}. The known input for the circuit is v_{IN}, and v_{II} is the RF generated voltage to account for RF effects. At this time v_{II} must be evaluated empirically. Up to a voltage limit of one volt, v_{II} is approximately proportional to the RF power level.

Figure 16 shows how the proportionality constant decreases as frequency increases. This is a coarse approximation which is conservative at high power levels. However, from the available data, it is a reasonable worst case model.

The value of this model is that it applies to RF entering one of the op amp input transistors and the input is the most susceptible port for the op amp. Therefore, this op amp model is a worst case model with RF entering other less susceptible ports not requiring consideration.

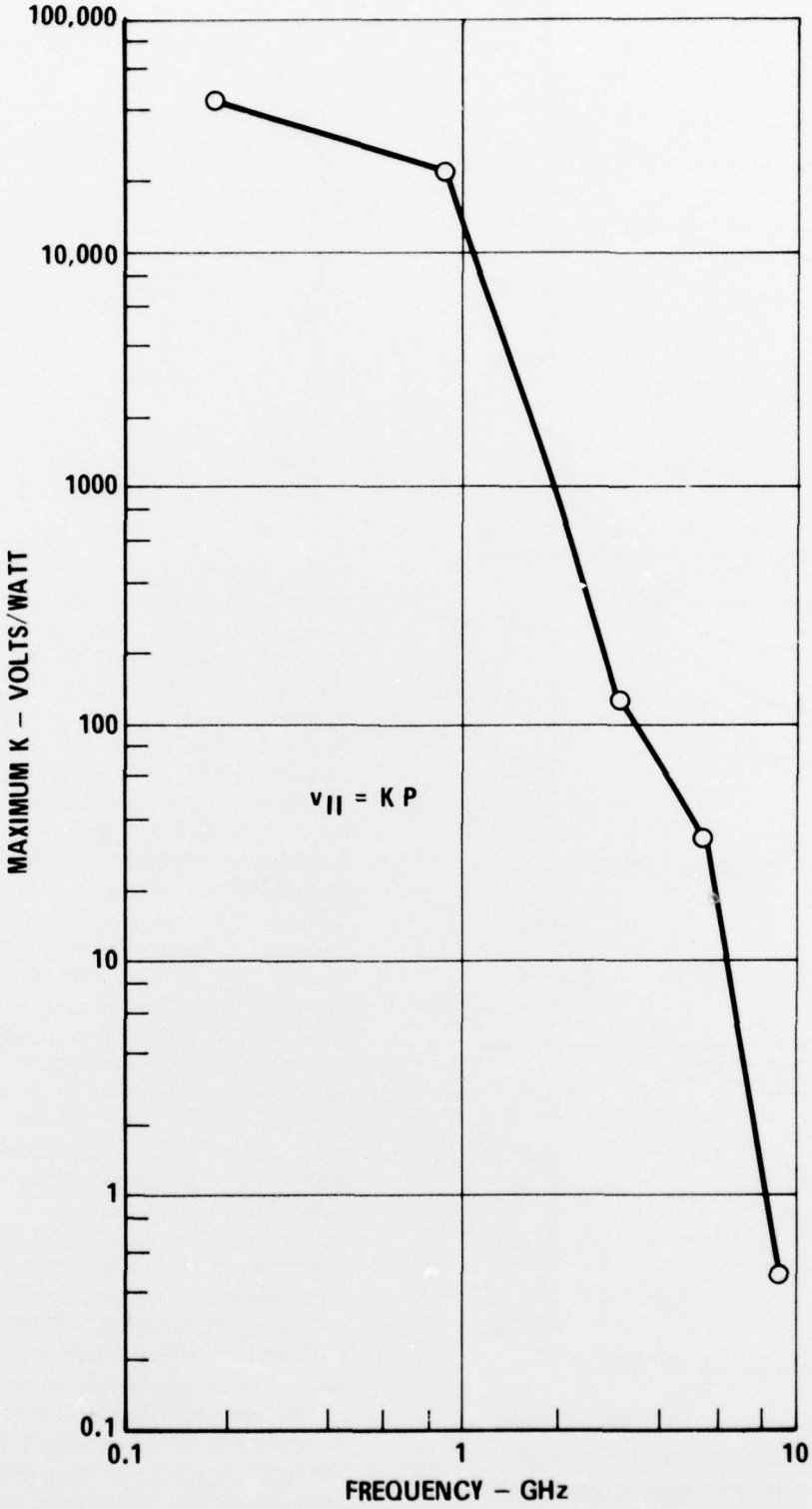


Figure 16. Maximum Values of Proportionality Constant Between Interference Input Offset Voltage and RF Power

4. DAMAGE EFFECTS

Preliminary studies in Phases I and II have shown that ICs could be damaged by high power RF pulses. The previous testing had been limited to pulse widths greater than or equal to 500 μsec and maximum power inputs of 20 dBW. This preliminary work uncovered only three different failure mechanisms: junction failures, metallization failures, and bond wire failures.

4.1 Theoretical Models — Since all three damage mechanisms are thermal in nature, the theoretical model for each mechanism is derived from the basic heat flow equation. The one dimensional form of the differential heat flow equation with heat produced uniformly through the volume [9,10] is:

$$\frac{\partial u(x,t)}{\partial t} = k \frac{\partial^2 u(x,t)}{\partial x^2} + C$$

where u = the change in temperature in °C,
t = the time in sec,
x = the distance in cm,
k = the thermal diffusivity of material in cm^2/sec,
K= the thermal conductivity in watts/cm/°C,
Q= the strength of the heat source in $watts/cm^3$, and
C= Qk/K in °C/sec.

The basis for all three damage models is that sufficient energy is required to increase the temperature to the failure point of the material. For bond wires and metallization, aluminum was the material in the ICs tested although some devices in current production utilize gold. The different models for each mechanism arise from the different boundary conditions for each mechanism.

4.1.1 Bond Wire Damage Model — The bond wire model consists of solving the heat flow equation with the boundary conditions as shown in figure 17. Both ends are assumed to be terminated in perfect heat sinks and no heat is radiated out of the rod. Heat is generated uniformly throughout the rod due to I^2R heating. The skin effect which occurs at high frequencies tends to crowd the RF current into an outer annulus but it is assumed that the dimensions are small enough to permit the core of the rod to be at the same temperature.

The highest temperature will occur in the center of the rod as this point is the greatest distance from the two heat sinks. The failure power, P, can be shown as a function of t, the pulse duration, in terms of T, the temperature at the center of the rod and T_o, the ambient temperature. The solution is

$$P = \frac{8AK(T - T_o)}{L\left[1 - \frac{32}{\pi^3} \sum_{n=1,3,5..}^{\infty} \left(\frac{1}{n^3}\right)\left(\exp\left(-\frac{n^2\pi^2 kt}{L^2}\right)\right)\left(\sin\frac{n\pi}{2}\right)\right]},$$

where A is the cross-sectional area of the rod in cm^2, L is the length of the rod in cm, and all other parameters have been defined previously.

This is a worst case model since all power is assumed to be dissipated in the bond wire although some power is dissipated in the bonding pads, package leads, etc.

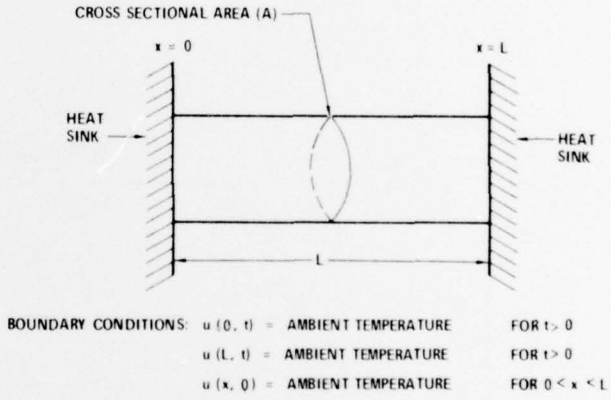


Figure 17. Bond Wire Model Diagram Showing Boundary Conditions and Dimensions

4.1.2 Junction and Metallization Damage Models — The failure models for the junction and metallization damage modes are essentially identical. In both cases the heat is generated in a thin sheet of material and the heat flow is down through the volume of the silicon chip. The thickness of both the metallization and the junction is sufficiently small to permit the assumption that the temperature is uniform throughout the thin sheets. The heat flow problem becomes one of a uniform material (the silicon chip) with constant heat flux across one surface ($watts/cm^2$) with the other surface connected to a heat sink. Figure 18 shows the heat flow diagram used for both the junction and metallization models. There is no heat radiated above the top surface of the chip. Both models

reduce to the same boundary value problem where heat is conducted away from one surface through the silicon chip.

The power to produce temperature T in time t is given by:

$$P = \frac{KWD\left(\frac{T - T_o}{L}\right)}{1 - \frac{8}{\pi^2} \sum_{n=1,3,5..}^{\infty} \frac{1}{n^2} \left(\exp\left(-\frac{kn^2\pi^2 t}{4L^2}\right)\right)\left(\sin\frac{n\pi}{2}\right)}$$

where L = thickness of silicon chip in cm,
K = thermal conductivity of silicon in watts/cm/°C,
k = thermal diffusivity of silicon in cm^2/sec,
Q = surface heat flux in watts/cm^2,
$Q = \frac{P}{WD}$ P = dissipated power in watts,
W = width of failure area in cm,
D = length of failure area in cm,
t = time in sec, and
T_o = ambient temperature.

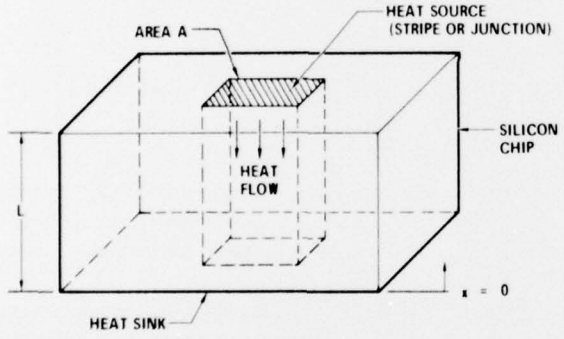


Figure 18. Junction or Metallization Stripe Heat Flow Diagram Showing Boundary Conditions and Dimensions

It is assumed that there is a critical temperature ($T = T_f$) at which the failure threshold will be reached. The amount of energy required to produce the actual failure (latent heat of fusion) is assumed negligible compared to the energy required to raise the temperature to the critical temperature.

For a worst case model, the thin sheet of material where all the power is assumed to be dissipated is taken as the area (WD) in the model even though some power is dissipated in the bond wires, the package leads, the bonding pad, etc. The silicon chip thermal characteristics are approximated by values at temperatures representative of the type of failure involved. The thermal constants for silicon vary with temperature significantly, while those for aluminum remain relatively constant over the temperature range of interest.

The junction failure probably occurs at a localized region of high temperature (a hot spot) caused by second breakdown. The hot spot is caused primarily by nonuniform current conduction in the semiconductor junction. After the hot spot, however small, occurs, the resistivity of the silicon in the hot spot increases with increasing temperature until the material becomes intrinsic. Beyond this critical point, the resistivity begins to decrease. The temperature at which any given silicon material reaches the intrinsic state depends on the inherent doping concentration and can range from 300°C to 1000°C for doping levels normally encountered in ICs[11]. If the temperature continues to increase after the material becomes intrinsic, the resistance of the hot spot decreases and additional current flows through the hot spot. This current increase, in turn, causes the hot spot to heat up even more with an additional decrease in the resistance until failure occurs. The temperature in this localized area exceeds the melting point of silicon (1412°C), but the temperature at which this process starts in motion is far less than the melting temperature. Therefore the critical temperature for a junction failure may be less than the melting point of silicon.

For metallization failures the critical temperature would be the melting temperature of the material in the stripe, usually aluminum (660°C).

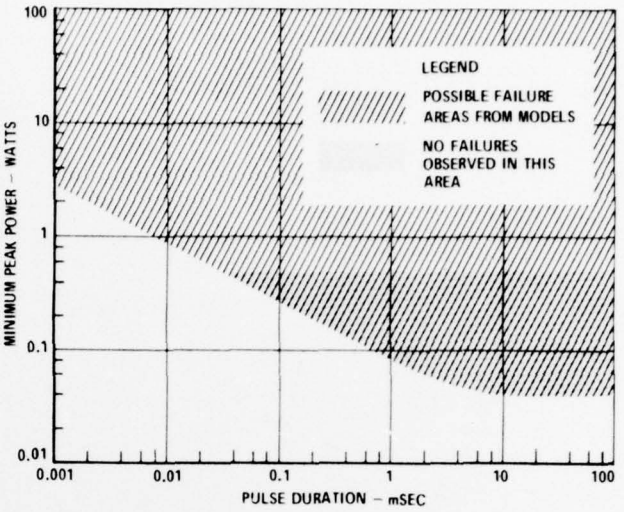
4.2 Damage Summary — The theoretical models based upon thermal analyses and worst case assumptions yield predictions which are conservative when compared to actual failure data. There is a typical factor of 10-12 dB between the measured and predicted values. It is recommended that this be utilized as a safety factor when using the failure results in an EMV hardening effort.

The relatively tight bunching of the failure data shown previously suggests that, for practical considerations, all failure mechanisms can be treated the same. The failure models also overlap closely for practical ranges of the model parameters. Figure 19 shows the overall worst case predictions on one composite graph. The physical parameters,

used for the model curve and listed in figure 19, are worst case values to obtain the minimum power to cause failure. For example the minimum bond wire diameter in current use is 0.001778 cm (0.7 mil) and a length of 0.5 cm is as long as can reasonably be expected. For junction or metallization failures, the area of the junction or stripe is the primary factor affecting a worst case prediction of failure. The worst case areas for junction and metallization failures are both assumed to be 6×10^{-6} cm^2 (a representative failure site area based on actual measurements). The worst case failure temperature for the junction model was taken to be 660°C (any higher temperature would presumably melt the aluminum metallization first).

There are three regions shown on the composite failure prediction graph in figure 19. The dividing line between shaded and unshaded areas is the composite worst case failure prediction for all three mechanisms with parameters listed. In the lower (unshaded) region, no failures of any kind are expected. From the worst case models, a failure could occur anywhere in the two shaded regions; however, in the darker area below 0.5 watt no failure has even been observed. Many ICs have been tested during interference testing, which is CW testing, in this area and no failure or degradation has been noted.

Actual failure data show that minimum RF power failure levels are 10 to 15 dB above the worst case model line. There is a possibility that different impedance combinations could decrease this difference. Therefore, the conservatism of this approach provides a needed safety factor for most devices.



SHADED AREAS
DETERMINED FROM
FAILURE MODELS FOR:

BOND WIRE
ALUMINUM
DIAMETER $\geq$ .001778 cm
LENGTH $\leq$ 0.5 cm

JUNCTION
SILICON
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS
$\leq$ .032 cm

METALLIZATION
ALUMINUM
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS
$\leq$ .032 cm

Figure 19. Composite Predictions of Worst Case Failure Levels From Bond Wire, Junction, and Metallization Models

5. FUTURE DIRECTIONS

In the next and final increment of the IC electromagnetic susceptibility contract, the effort will be concentrated on completion of the IC susceptibility handbook. To complete the handbook, the existing models require verification through extension to other devices and modifications where necessary. Through this verification testing the data base of the handbook will also be increased. The final form of the handbook will also be influenced by the comments from potential end-users, particularly at the seminar to be held in the fall of 1977.

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1. REPORT NUMBER NSWC/DL TR-3653	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Integrated Circuit Electromagnetic Susceptibility Investigation - Phase III Summary Report No. 2		5. TYPE OF REPORT & PERIOD COVERED 6. PERFORMING ORG. REPORT NUMBER MDC E1668
7. AUTHOR(s) J. M. Roe, et. al.		8. CONTRACT OR GRANT NUMBER(s) N60921-76-C-A030
9. PERFORMING ORGANIZATION NAME AND ADDRESS McDonnell Douglas Astronautics Company - East P. O. Box 516 St. Louis, MO 63166		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62762N, XF54585 XF54585.B02, DF98(A)
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Electronic Systems Command Research and Technology Directorate Washington, DC 20360		12. REPORT DATE 3 June 1977 13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Naval Surface Weapons Center Dahlgren Laboratory (Code DF-56) Dahlgren, VA 22448		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release; Distribution Unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

EMV
Integrated Circuit
Interference
Catastrophic Failure
RF Susceptibility
Hardening

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report summarizes in a general manner the progress made in investigations into the susceptibility of integrated circuits (ICs) to RF power. This is an interim report covering the work performed in the second of three increments. This increment includes expansion of the modeling effort to incorporate the transistor models into a standard circuit analysis program SPICE (Simulation Program with Integrated Circuit Emphasis) so that RF effects on ICs can be modeled. The testing necessary to support the modeling effort is also

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included. A complete study of the damage mechanisms suffered by ICs under RF stress is also included in this report as second increment work. This damage study includes both modeling and an extensive testing program. The changes to the first draft of the IC susceptibility handbook and the rationale behind the changes are also included in this report.