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MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT. (U)

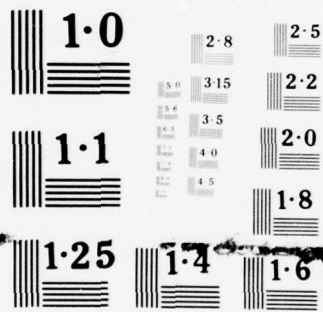
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MNOS BORAM  
MANUFACTURING METHODS  
AND TECHNOLOGY PROJECT

Third Quarterly Progress Report  
1 January 1977 to 31 March 1977

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Contract DAAB07-76-C-0048  
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TECHNICAL REPORT  
MNOS BORAM MANUFACTURING METHODS AND  
TECHNOLOGY PROJECT

Third Quarterly Progress Report  
1 January 1977 to 31 March 1977

Prepared by  
J.E. Brewer, T.G. O'Donnell, P.C. Smith, L.A. Epstein

PROJECT OBJECTIVE: Establish a production capability for metal nitride oxide semiconductor (MNOS) integrated circuits for block oriented random access memory (BORAM).

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WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER  
Systems Development Division  
Baltimore, Maryland 21203

## ABSTRACT

A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductors (MNOS) block oriented random access memory (BORAM) multichip hybrid circuits. During the past quarter the first set of engineering samples were delivered, and fabrication of the second set was initiated. Further experience was gained with a new low cost MNOS BORAM die. Hybrid circuit and memory card development progressed. In addition, transistor endurance testing concepts were explored.

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## PURPOSE

The purpose of manufacturing methods and technology (MM&T) project number 2769758 is to establish a production capability for metal nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random access memory (BORAM).

Military organizations are faced with a difficult hardware problem in the use of modern day computers. A suitable militarized secondary storage technology simply does not exist. Drums and discs cannot stand up under the stress of the ground mobile environment. Military real time programs are forced to be resident in main memory because electromechanical storage access delays cannot be tolerated.

MNOS BORAM holds considerable promise of meeting the military's secondary storage needs. An advanced development Army/Navy MNOS BORAM module has proven that significant volume, weight, power and use flexibility advantages can be achieved. When compared to fixed-head electromechanical storage MNOS BORAM offers MTBF's 10 times longer, and access times about 500 times faster.

This MM&T project will establish for the government a source of supply for MNOS BORAM secondary storage. A pilot production line with a demonstrated capacity of 1,875 hybrid circuit per month will be established. Each hybrid circuit will contain 16 MNOS BORAM integrated circuits. This production rate will provide sufficient hybrid circuits to allow fabrication of three 16.8 megabit BORAM modules per month. The hybrid circuits will conform to Electronics Command Technical Requirement SCS503, and the MM&T project will be conducted in accord with Electronics Command Industrial Preparedness Procurement Requirement Number 15.

## 1. NARRATIVE AND DATA

MM&T project results during the reporting period were particularly encouraging. Satisfactory results have been achieved using the 6000C chip as a development vehicle. Initial sample delivery requirements have been met. The elements associated with a cost reduced hybrid have also matured. Marked improvements in end product cost potential are expected to be confirmed.

### 1.1 ENGINEERING SAMPLES

During January, the first set of engineering samples were delivered to ECOM. This discussion reviews the purpose and requirements for the sample, and then explains and documents the elements which compose the sample.

#### 1.1.1 Sample Requirements and Description

The MNOS BORAM MM&T requires delivery of two sets of engineering samples to demonstrate technical progress. These devices are produced to gain information concerning product and process characteristics. Each set of samples consists of 17 hybrid circuits. Test data and an explanation of test methods are to be provided with the samples. The detailed device specification is SCS-503.

In January, the first set of samples were delivered to Fort Monmouth. Each of the 17 hybrid circuits contained 16 of the BORAM 6000C devices. The total chip delivery was 272 devices. All of the chips had been qualified as bin-0 die at wafer probe (The wafer probe test was described in the second quarterly report). After hybrid assembly, the die were rescreened on the same test equipment using a simplified version of the wafer probe program. Later, the hybrids were also mounted on a memory card, and were operated in the BORAM module advanced development model.

### 1.1.2 BORAM 6000C

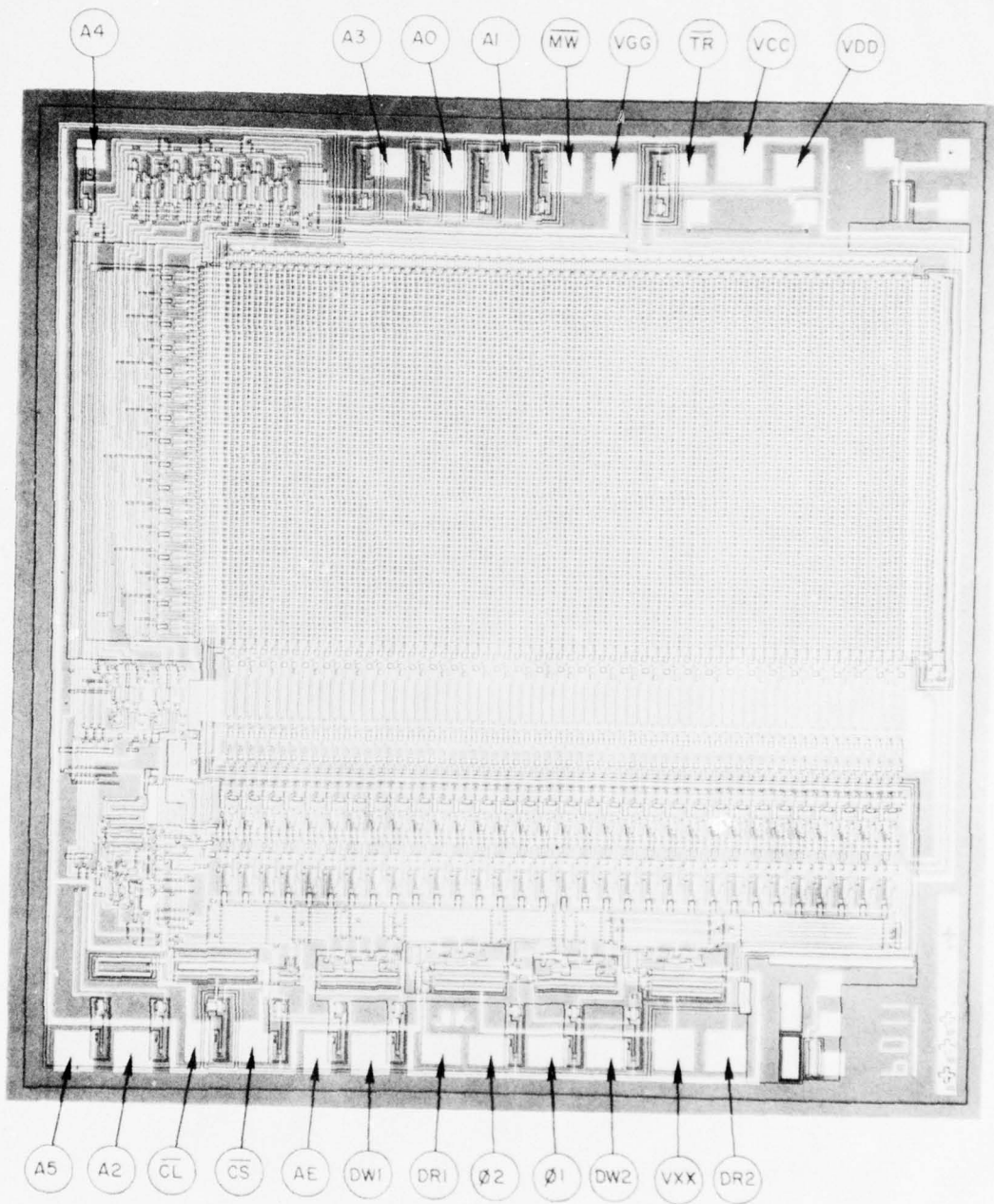
The 6000C chip provides 2048 bits of nonvolatile data storage. Figure 1-1 shows the die and identifies the bonding pads. Pads are greater than 5 mils<sup>2</sup>, and are located on opposite sides of the die. The chip measures 163 by 169 mils. A glass overcoat guards against scratches due to handling. Protective devices on all inputs avoid damage by static charge.

As shown in figure 1-2, the chip contains a fully decoded 64-word by 32-bit random access memory and two dynamic 2-phase 16-bit shift registers. All data I/O takes place serially through the shift registers. The RAM and the shift registers may operate independently. Data is transferred in parallel between the RAM and registers via a 32-bit latch. Data output drivers are three-state devices capable of sinking a low power Schottky load. The 6000C has been operated over the -55°C to +125°C temperature range. The circuit design tolerates changes due to temperature and is also insensitive to variations in power supply voltages.

### 1.1.3 Type 1000 BORAM Microcircuit

The type 1000 MNOS BORAM microcircuit is shown in figure 1-3. This early design was developed for use in the Army/Navy BORAM module advanced development model. The platform package is manufactured by Tekform. The multilayer alumina substrate contains four screened metal layers separated by dielectric. A complete hybrid weighs 37.4 grams.

Figure 1-4 identifies the pins, and labels individual chip mounting sites. Figures 1-5 and 1-6 provide the electrical circuit for the hybrid. The connection scheme was established to allow device experiments. Extra pads were provided for changing block select signals and for modifying VDD voltages. These features were useful with the older one-transistor cell chip designs, but are not used with the 6000C chip.



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Figure 1-1 The BORAM 6000C Die

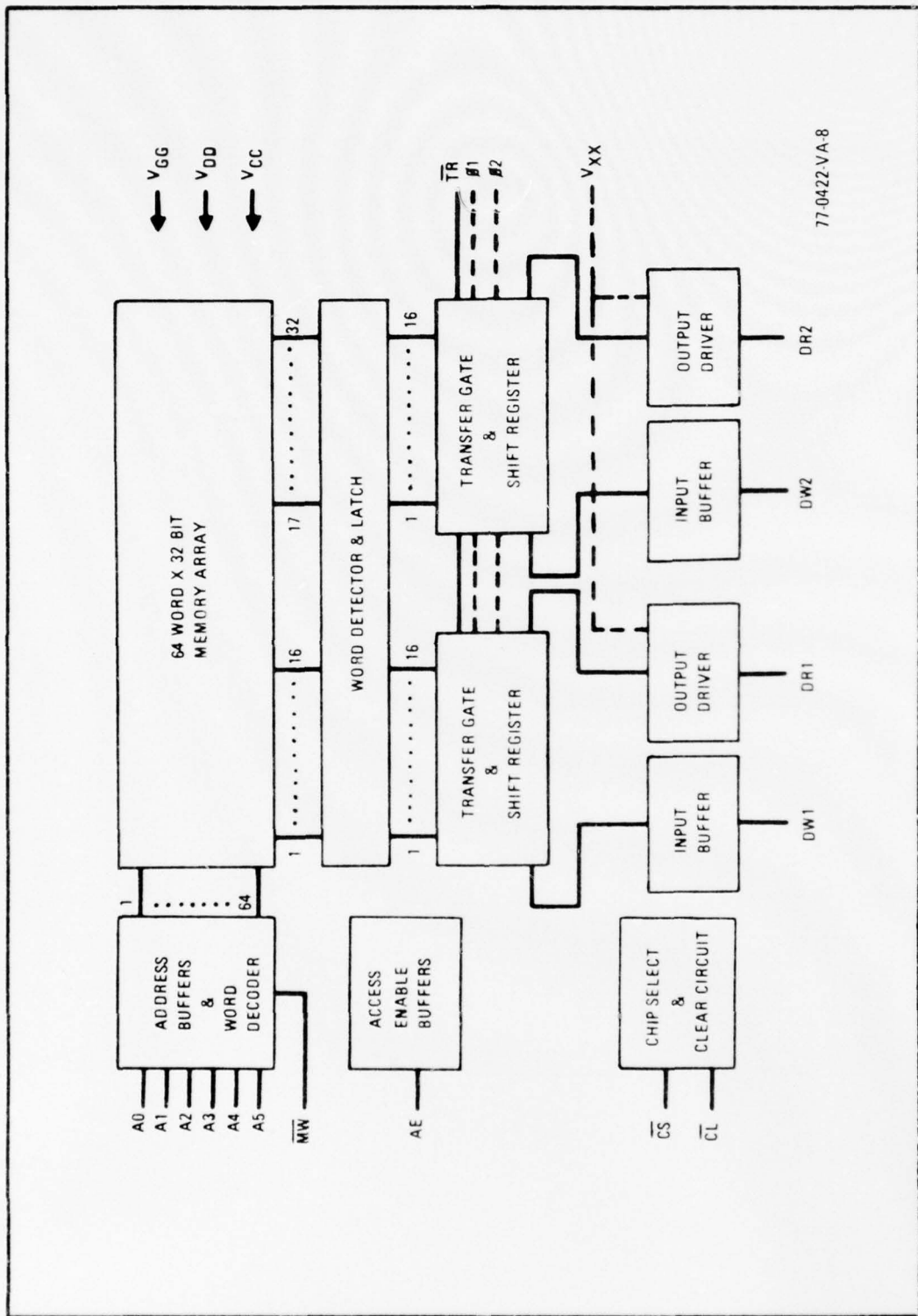


Figure 1-2 Structure Oriented Block Diagram of the BORAM 6000C Integrated Circuit

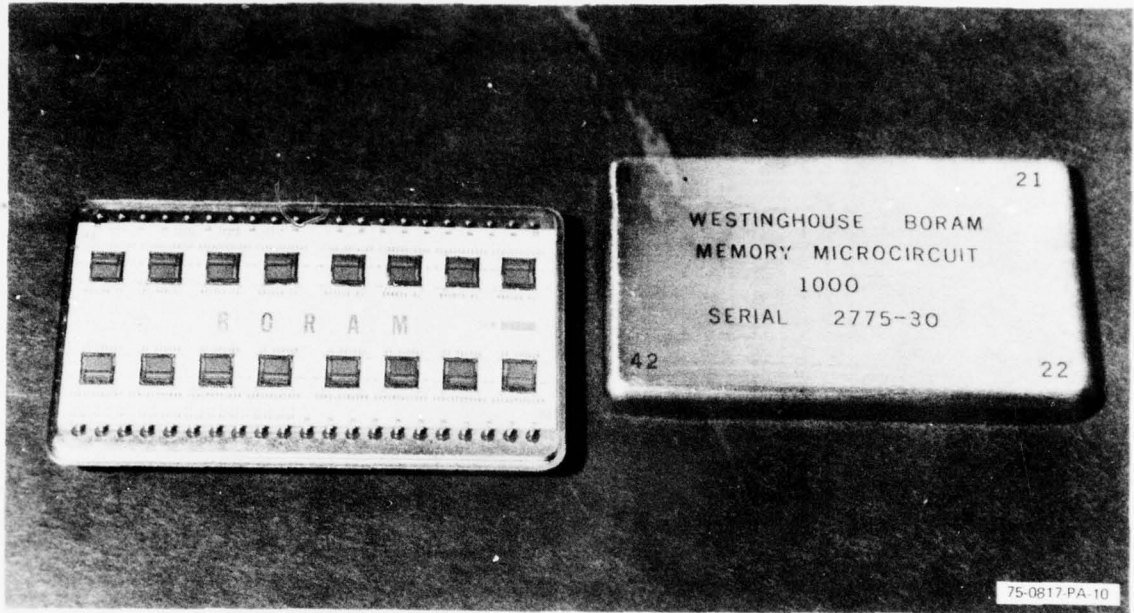


Figure 1-3 BORAM Memory Microcircuit Type 1000

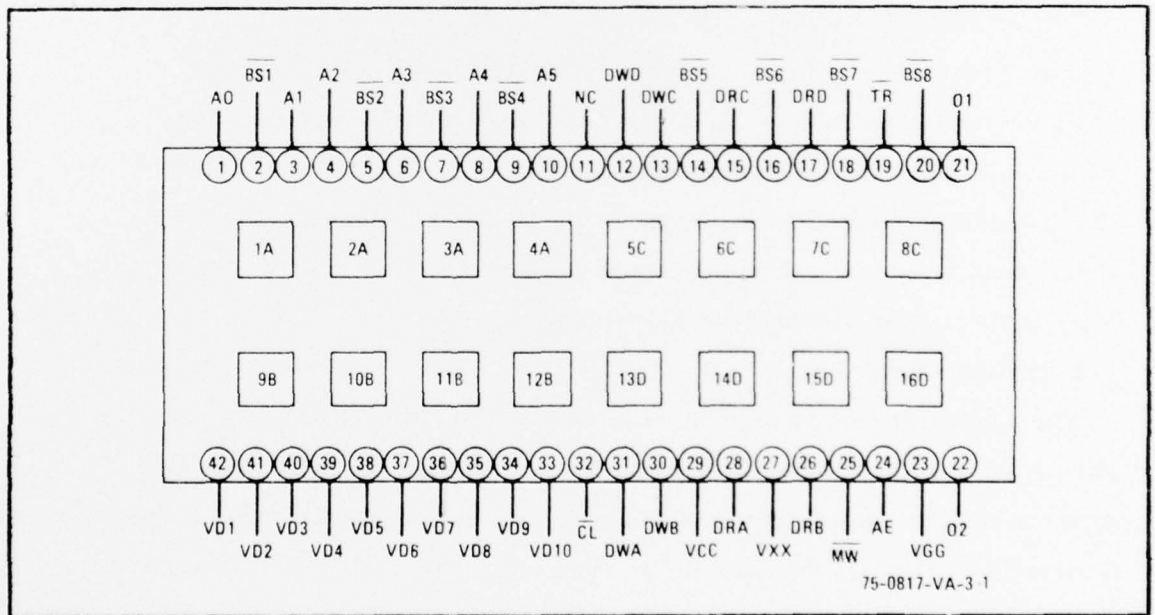


Figure 1-4 Pin Identification for Type 1000 BORAM Memory Microcircuit

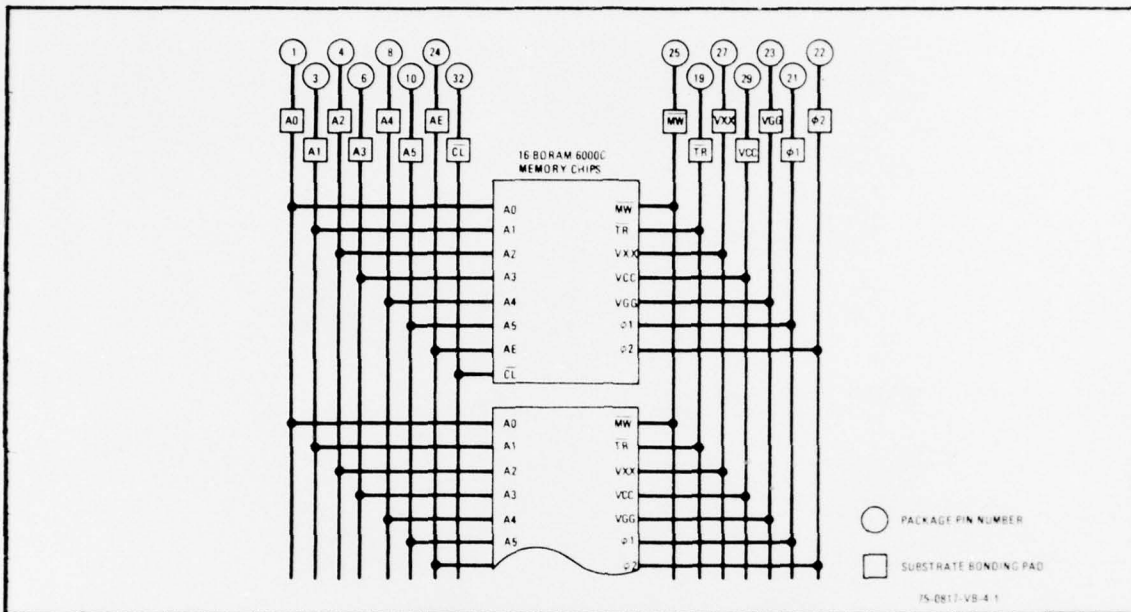


Figure 1-5 Bused Connections in Type 1000 BORAM Memory Microcircuit

#### 1.1.4 Type 1000 BORAM Memory Card

The Army/Navy BORAM module advanced development model was designed to accommodate 32 of the type 1000 memory cards shown in figure 1-7. A card provides a physical storage capacity of 622, 592 bits. The board measures 9.5 by 12 inches. Height is measured from the tip of the connector shroud to the top of the board. The board occupies 50.3 cubic inches and weighs 2.39 pounds.

#### 1.2 BORAM 6002 STATUS

The 6002 integrated circuit resulted from studies of how to simplify and shrink the older 6000C. The appendix A contains a soon to be published paper which describes the device. The second quarterly report summarized the results achieved with the first runs of the device. This report reviews the progress through the end of March.



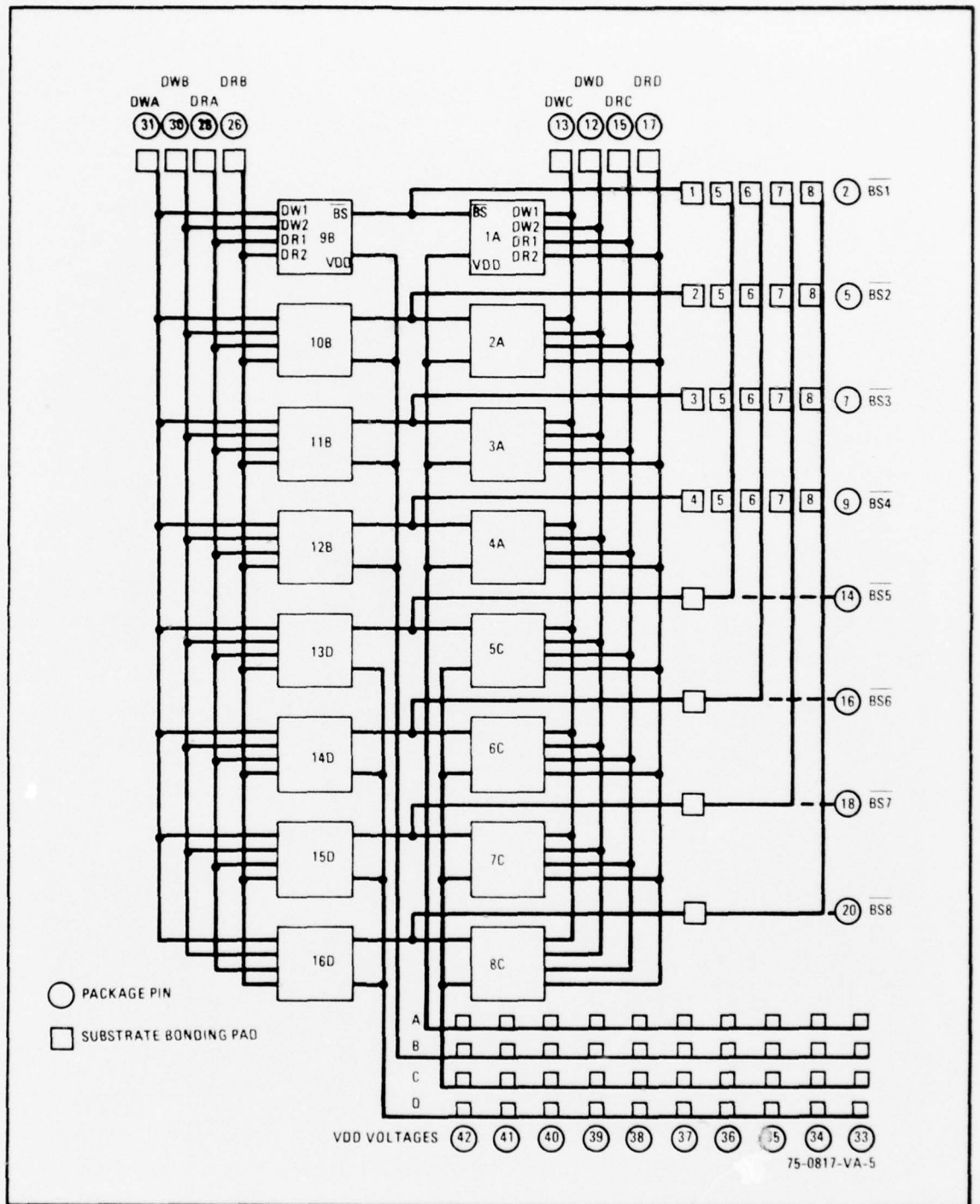


Figure 1-6 Unique Connections in Type 1000 BORAM Memory Microcircuit

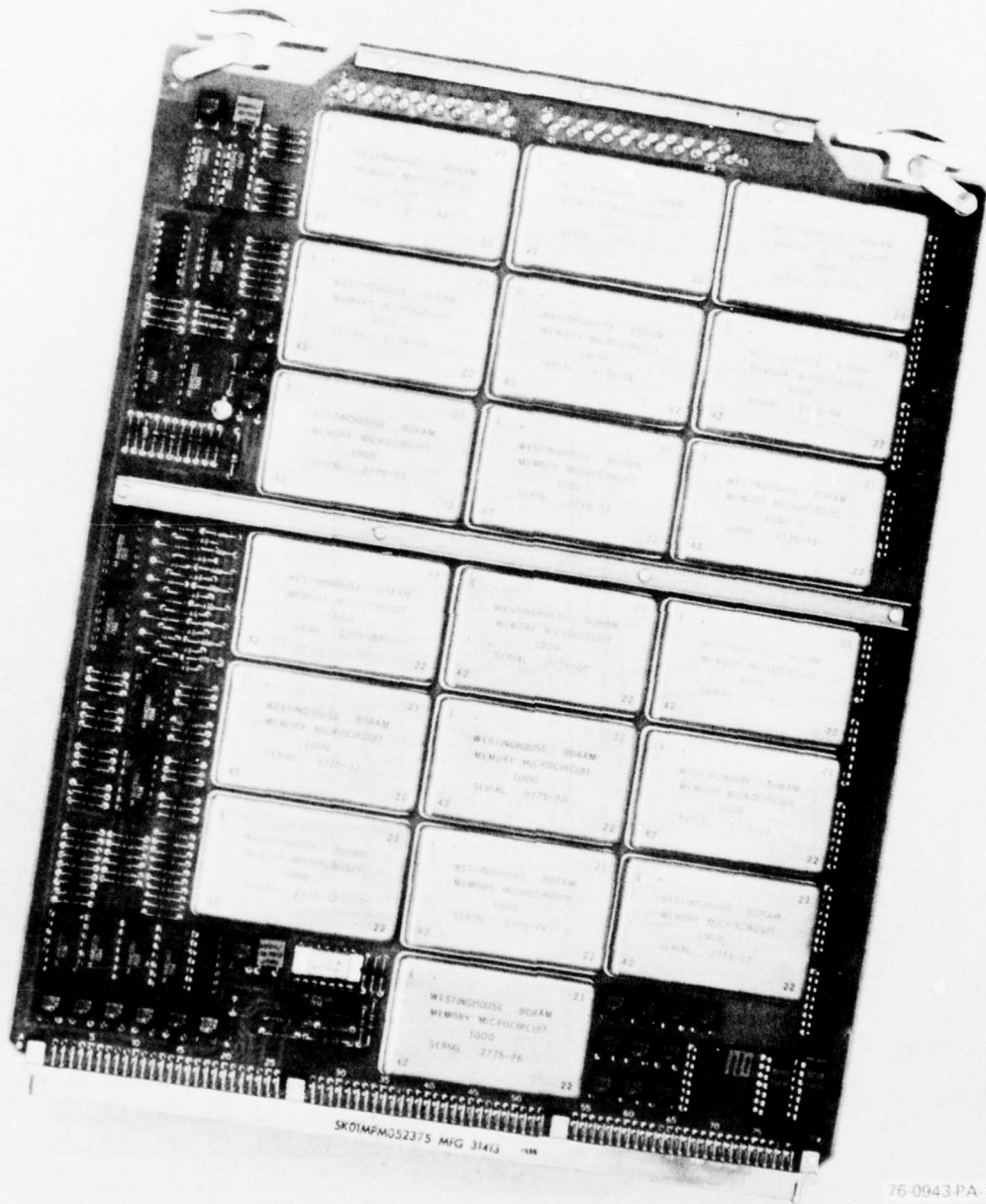


Figure 1-7. Type 1000 BORAM Memory Card

A wafer probe program for the Macrodata 154 test system has been written and debugged, and initial characterization of the 6002 is in progress. An error in the mask set has been corrected, and the correction has been verified. The field region ion implant has been adjusted to give a 40-volt inversion threshold.

### 1.2.1 Wafer Probe Test

Figure 1-8 is a simplified block diagram of the wafer probe test. The flow is intended to minimize test time by doing functional verification first. Die which pass these blocks are characterized and tested for DC operation.

Figure 1-9, the Test Program Listing, is a Macrodata computer printout of the program flow. The columns have the following meanings. SWN is the test number. FL or PR indicates a functional or parametric test. The next four columns are the file numbers of data used to setup the programmable clocks, power supplies and pattern generation hardware. LOG, BIN and BRN are actions to be taken after the test and may occur Always, Never, on Pass or on Fail.

As an example, test SWN 1 is a parametric test using power setup 1 and pattern 1. If the test fails, Log 20 is incremented, and the die is rejected to Bin 1. No branching will occur. After binning the tester returns to SWN 0 and stops. If SWN 1 passes, SWN 2 is immediately executed with similar decisions on the results. The commentary notes on the right indicate the nature of each test.

Substrate diode forward voltage is checked primarily to assure against misalignment of probes. This test usually fails about 5 percent of the die. These are devices around the edge of the wafer which were damaged in processing or are partial die.

The shift register is tested to collect process quality information. The register occupies small area of the die. It should have few photo defects and high yield if threshold, sheet rho etc., are within specifications.

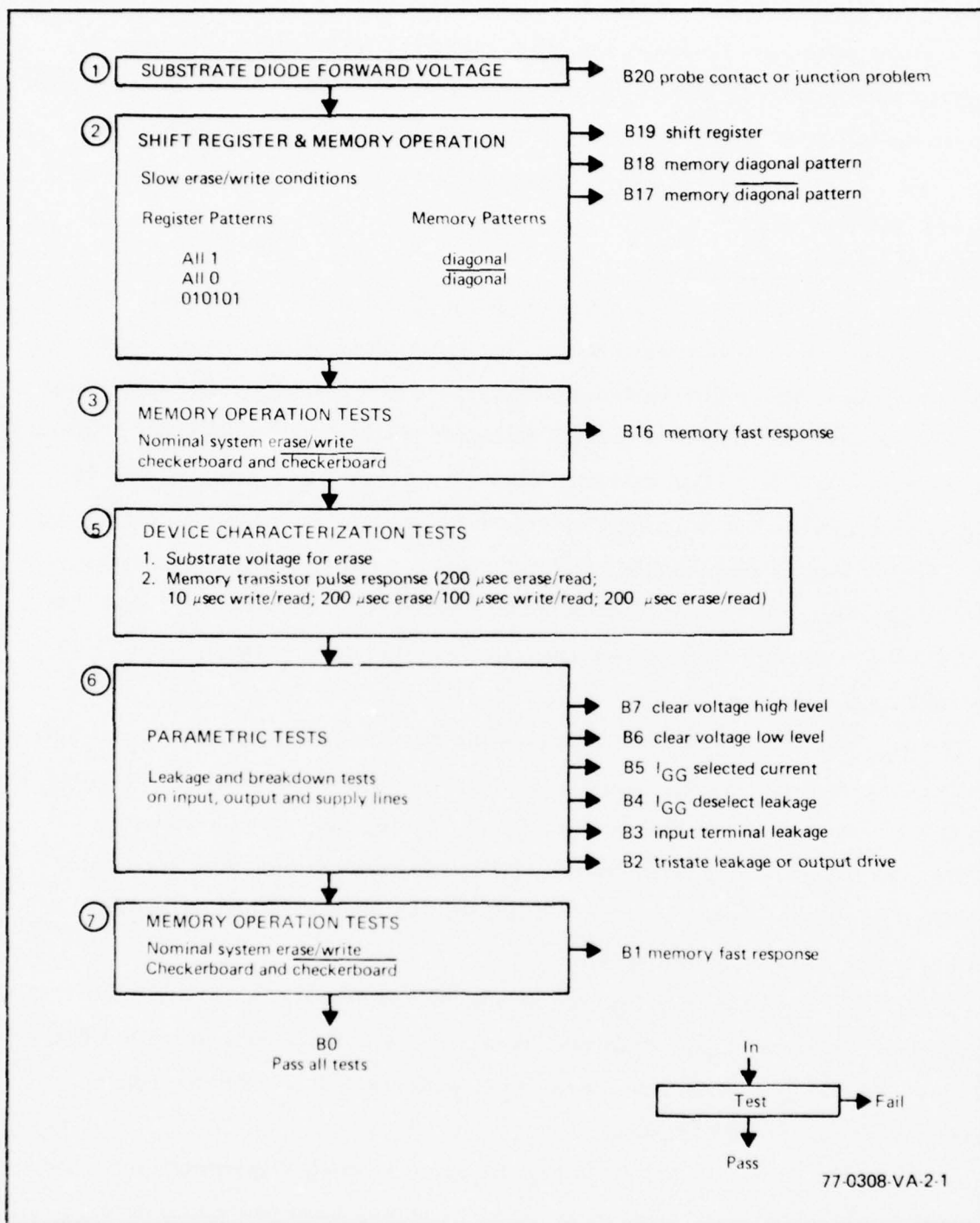


Figure 1-8 BORAM 6002 Wafer Probe Test Flow Diagram

TEST PROGRAM LISTING

STATEWORD TABLE

SWN		BUF	CTL	RPE		LOG	BIN	BRN	COMMENTS
		PWN	CKN	PTN	PRN				
0	FL	2	0	0		N 0	N 0	N 0	
1	PR	T	1		1	F20	F 1	N 0	CONTACT
2	FL	T	1	1		F19	F 1	N 0	SR
3	FL	T	1	3	2	N 0	N 0	N 0	CL - 2.5 msec
4	FL	T	1	1	3	N 0	N 0	N 0	WRITE DIA 1 msec
5	FL	T	1	2	4	F18	F 1	N 0	READ DIA
6	FL	T	1	3	2	N 0	N 0	N 0	CL - 2.5 msec
7	FL	T	1	1	5	N 0	N 0	N 0	WRITE DIA 1 msec
8	FL	T	1	2	6	F17	F 1	N 0	READ DIA
9	FL	2	0	1	0	N 0	N 0	N 0	
10	FL	T	1	3	7	N 0	N 0	N 0	CL - 200 μsec
11	FL	T	1	1	8	N 0	N 0	N 0	WRITE CKB 100 μsec
12	FL	T	1	2	9	F16	N 1	F 00	READ CKB
13	FL	T	1	3	7	N 0	N 0	N 0	CL - 200 μsec
14	FL	T	1	1	10	N 0	N 0	N 0	WRITE CKB 100 μsec
15	FL	T	1	2	11	F16	F 1	P 00	READ CKB
30	PR	T	1			11	F15	N 0	FIX VT
31	FL	T	7	4	13	N 0	N 0	N 0	200 μsec CL
32	PR	T	1			10	N 0	N 0	MEM VT
33	PR	T	7	5	15	N 0	N 0	N 0	100 μsec WRITE
34	PR	T	1			10	N 0	N 0	MEM VT
35	FL	T	7	4	13	N 0	N 0	N 0	200 μsec CL
36	FL	T	7	5	15	N 0	N 0	N 0	100 μsec WRITE
37	PR	T	1			10	N 0	N 0	MEM VT
38	FL	T	7	4	13	N 0	N 0	N 0	200 μsec CL
39	PR	T	1			10	N 0	N 0	MEM VT
41	PR	T	1			2	F 7	F 1	CL' AT VCC
42	PR	T	1			3	F 6	F 1	CL' AT -25
43	PR	T	2			8	F 5	N 1	I <sub>GG</sub> SELECTED
44	PR	T	2			9	F 4	F 1	I <sub>GG</sub> DESELECTED
45	PR	T	1			4	F 3	F 1	INPUT LEAK -20V
46	PR	T	1			5	F 2	F 1	CS LEAK -36V
47	PR	T	2			6	F 2	F 1	TRISTATE LEAK HI DRIVE
48	PR	T	2			7	F 2	F 1	TRISTATE LEAK LO DRIVE
49	FL	2	0	1	0	N 0	N 0	N 0	
50	FL	T	1	3	7	N 0	N 0	N 0	CL-200 μsec
51	FL	T	1	1	10	N 0	N 0	N 0	WRITE CKB 100 μsec
52	FL	T	1	2	11	P 0	P 0	N 0	READ
53	PR	N				P15	R 1	N 0	FAIL TO READ CKB

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Figure 1-9 State Word Listing for BORAM 6002 Probe Tests

SWN 3 thru 8 act to clear, write and read a diagonal and inverse diagonal pattern into the memory at relatively slow speed. Passing this test assures that each bit is being uniquely addressed, and that it will store either a one or zero. The yield of these fully functional photo defect free memories is a good indication of processing quality.

SWN 10 to 15 causes a clear, write and read of a checkerboard and inverse checkerboard at nominal speed. On pass at SWN 15 a branch to 30 occurs. Testing stops on fail. This gap has been left for additional functional characterization tests which will be added later.

SWN 30 to 39 use the on chip test patterns to collect data on memory transistor response. Because the test device is physically close to the memory array, the measurements should correlate to array properties. SWN 41 to 48 are DC measurements which assure that the die has sufficient clear voltage and is not leaky. Finally a retest of the nominal speed checkerboard inverse is performed, and the die is binned.

#### 1.2.2 Initial Characterization Results

Figure 1-10 shows the input signal timing for read mode operation of the device. Characterization tests are being performed to determine how wide an operating range exists for all important timing relationships. For example, the shift register has been operated from 1.6 MHz down to 5 Hz at room temperature. Figures 1-11 and 1-12 are schmo plots of read timing. The first schmo is VGC versus transfer pulsewidth. It indicates that the falling edge of transfer can be moved over a wide range without disturbing proper reading. The second plot holds TR width fixed at 900 nsec and moves the pulse toward the AE falling edge. This is a measure of the read access time. At VGG=-30V the latch is properly set about 600 nsec after the fall of AE. Operation of this particular part extends almost to VGG=-15 if the slower access time is acceptable.

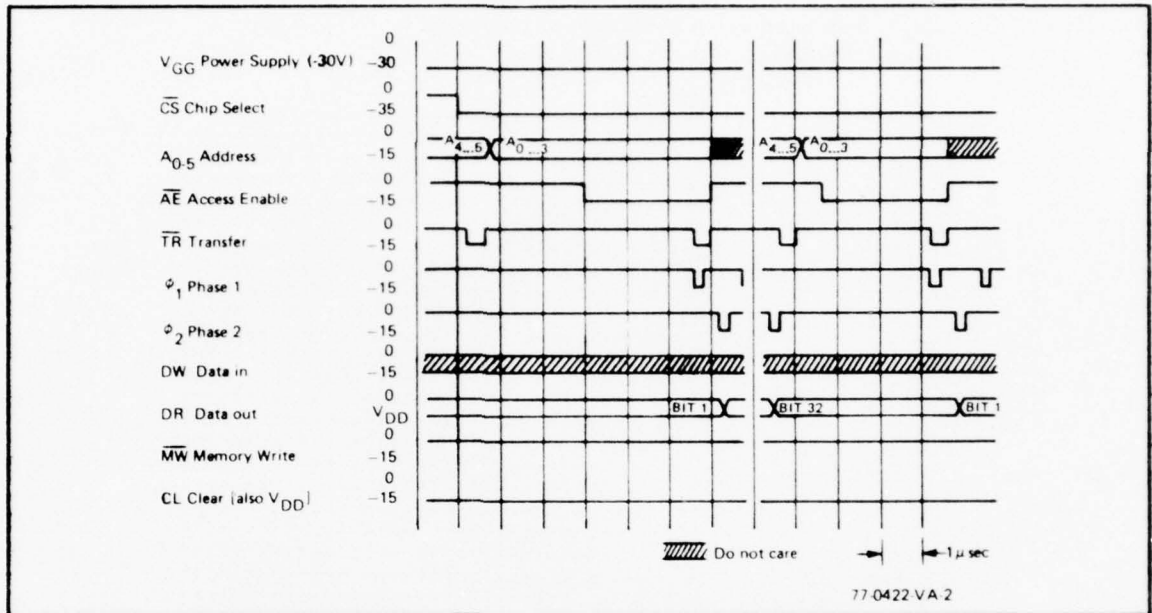


Figure 1-10 BORAM 6002 Read Mode Signal Timing

Numerous characterizations of this nature are being performed. A number of parts will be tested over the temperature range. When the failure edges are defined, test and system timing will be set to allow wide operating margins.

Figure 1-13 is a histogram of the clearing voltage reaching the array. A very tight grouping between -25 and -26 volts can be seen. This parameter is important since it ultimately determines the high conductance threshold the array will reset to. Uniformity will be necessary for endurance and retention assurance.

### 1. 2. 3 Correction of Initial Lot Problems

A layout mistake on the original mask set prevented clearing while TR was held at  $V_{CC}$ . This meant that four-row clear could operate only on rows with the same high and low order address since TR is used to set high order addresses. The problem was traced to a diffused cross under

POSITIVE EDGE OF TR HELD 3500NS FROM AE NEGATIVE EDGE  
 VGG IN VOLTS (300MV STEPS), VCC +15 VOLTS, DEVICE 0702-2-11A



TRPW IN NANSECONDS (40 NS STEPS) 77-0422-VA-3

Figure 1-11 V<sub>GG</sub> vs TR Pulsewidth Schmoo Plot



TR PULSEWIDTH 900 NS  
 VGG IN VOLTS (300MV STEPS), VCC +15 VOLTS, DEVICE 0702-2-5A



Figure 1-12  $V_{GG}$  vs TR Position Relative to AE Schmoor Plot

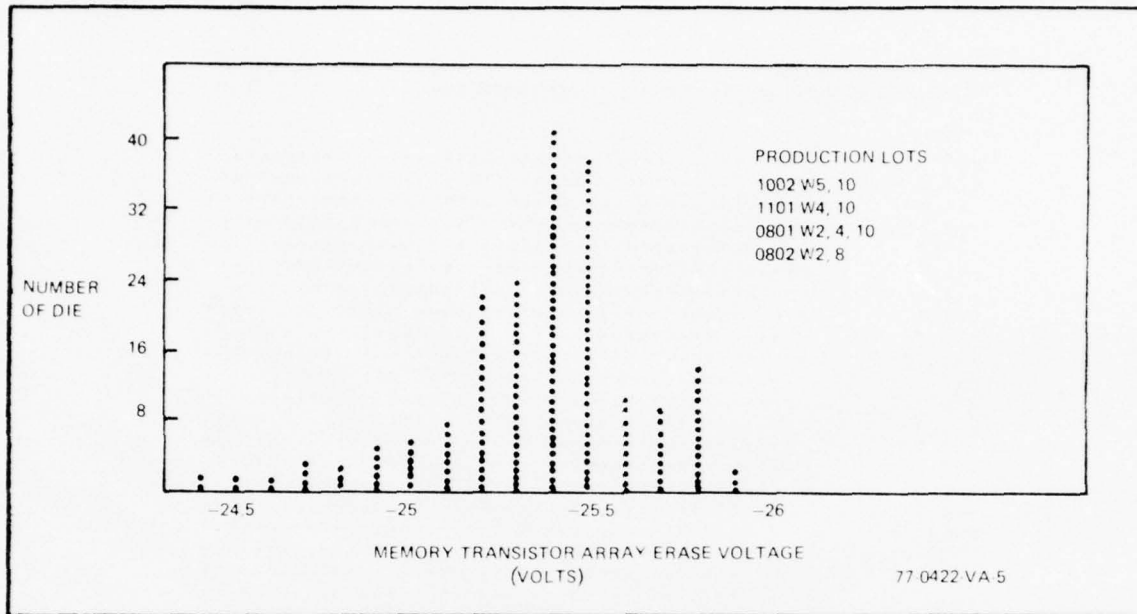


Figure 1-13 Array Erase Voltage Distribution

outside the isolation area and was fixed by closing a contact hole (level 8) and rerouting the metal line (level 9). The second lot had this correction and operated properly.

In addition to the mask error, the first lot also had a field inversion implant that yielded only 27v threshold. Since the supply and chip select voltages are 30 and 35 volts respectively, massive parasitic leakage was encountered. Lower voltages were used to test the first lot. The second lot received a corrected implant that produced field inversion thresholds in excess of 40 volts.

### 1.3 HYBRID CIRCUIT STATUS

The advent of the 6002 integrated circuit with its reduced pin count has allowed the development of a simplified cost reduced hybrid circuit. The primary features of the new hybrid were described in the second quarterly report. These comments describe the progress in preparation of the hybrid during the past quarter.

Figure 1-14 shows the new multichip hybrid microcircuit. Part number 647R527G01 has been assigned to this component. At the end of March all major elements had been defined, and fabrication and/or procurement had been initiated.

Figure 1-15 provides a more detailed view of the elements which compose the hybrid. The multilayer alumina substrate serves to interconnect the 16 BORAM 6002 integrated circuits.

A study of economic options established that in-house manufacture of the substrate was advantageous. The layers of metal and dielectric will be defined by screening. Finished substrates are scheduled to be available in May.

Automatic test equipment is being programed to allow individual testing of each substrate for shorts and/or opens. This equipment employs two probes which are moved from pad-to-pad at high speed under computer control. Probing paths are optimized by software during programming. The final control program is stored on a magnetic tape cartridge. Programming was nearly complete in March, and the system should be operational well before substrates are available in May.

The metal 1- by 2-inch package is being purchased from Tekform. Initial packages were delivered in March, and a second shipment is due in April. Experiments to insure process compatibility are being performed.

Overall, the hybrid package aspects of MM&T program are moving smoothly. It should be possible to use the new hybrid configuration for a portion of the engineering sample deliveries.

#### 1.4 MEMORY CARD STATUS

MNOS BORAM hybrids are intended for use in secondary storage systems. It is important that the suitability of the product for that application be confirmed under actual system operating conditions at an early date.

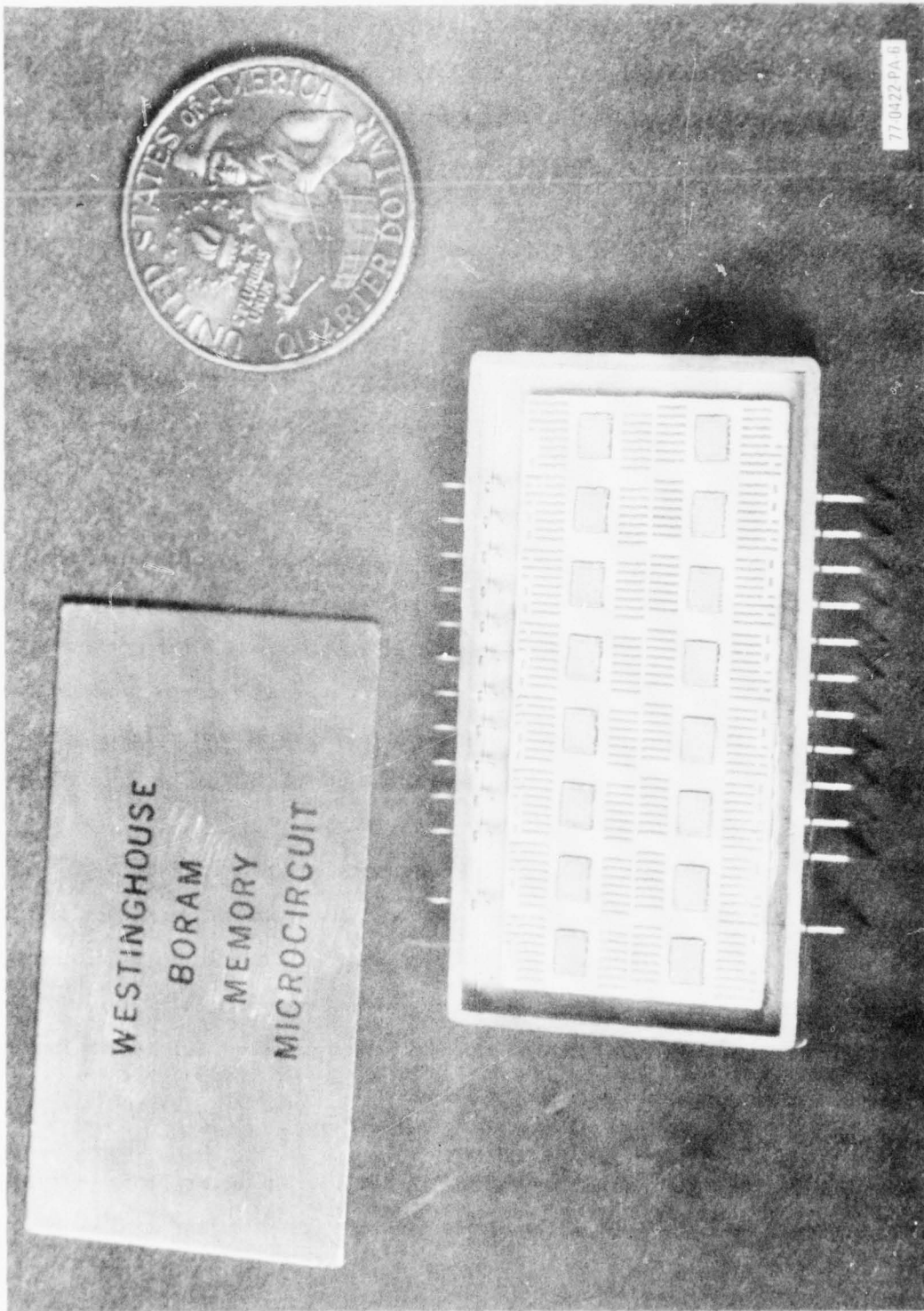


Figure 1-14 BORAM Memory Microcircuit Westinghouse Part 647R527G01

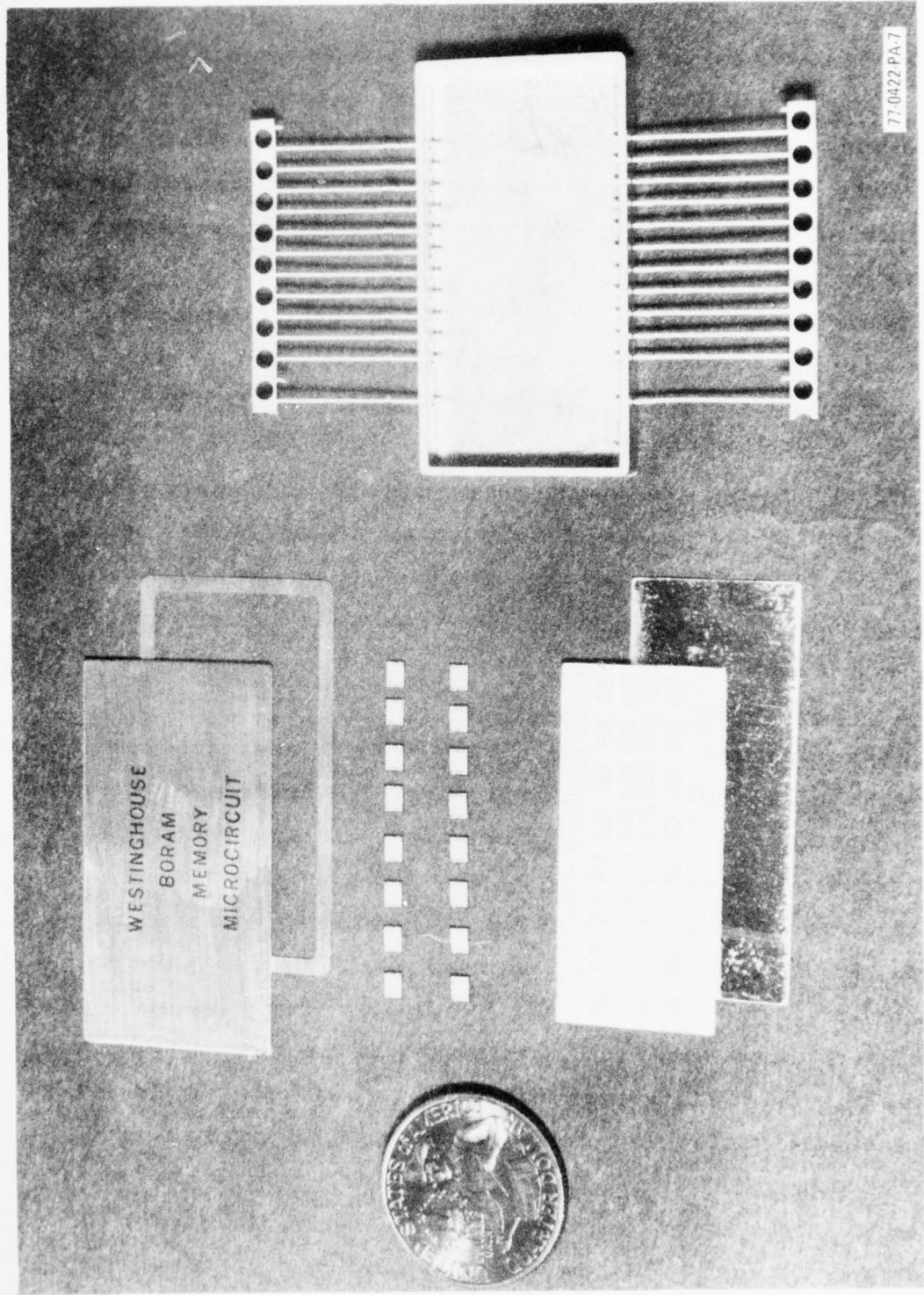


Figure 1-15 Component Parts of BORAM Memory Microcircuit  
Westinghouse Part 647R527G01

Toward this end, memory cards compatible with the Army/Navy BORAM module advanced development model are being prepared.

Each memory card will contain 19 of the 647R527G01 hybrids and appropriate driver and buffer circuitry. By the end of March all circuit design was complete. Driver and buffer circuits were breadboarded and tested.

The detailed board layout will be initiated in April. Final artwork is expected in May. At that time a make or buy decision will be made. Finished multilayer boards are expected to be available in July.

#### 1.5 ENDURANCE TESTING CONCEPTS

During the past quarter a series of exploratory efforts were undertaken to establish a means of routinely determining and monitoring the endurance characteristics of BORAM device production. At present the development effort is about 50 percent complete, and some of the concepts involved can be described.

##### 1.5.1 Device Endurance Considerations

The dynamic and static characteristics of MNOS transistors change as a function of accumulated erase-write cycling. The nature and magnitude of these changes must be known quantitatively, and must be tolerated by memory chip circuitry. In order to establish a viable MNOS BORAM production line, the MM&T project must provide a practical means of measuring and routinely monitoring endurance sensitive parameters.

From the standpoint of readily observable parameters the effects of erase-write cycling show up primarily in transistor pulse response and in threshold decay rate. Westinghouse has constructed a special unit called the "VT Tester" to automatically measure these characteristics on samples of one to eight transistors. The second quarterly report described in the VT Tester in some detail.

The stability of pulse response and threshold decay with endurance cycling depends on many factors. Electric field stresses should be well controlled. Transistor geometry and applied voltage waveforms must be defined with electric field stress limitations in mind.

Given that electric field stresses have been properly considered, differences in endurance can be related to differences in tunnel layer and nitride processing. Individual process combinations must be characterized for endurance under known electric field conditions. Selected processes must be monitored to insure repeatability of endurance properties.

#### 1.5.2 Cycle Accumulation Equation

The end use of the BORAM memory chip determines the number of erase-write cycles the MNOS transistor will see. Any given system application can be examined to establish how many cycles are likely to be accumulated in a fixed time period.

$$\text{Accumulated Cycles} = \frac{\text{Elapsed Time} \cdot \text{Module Duty} \cdot \text{Write Duty} \cdot \text{Block Duty}}{\text{Block Process Time}}$$

$$n = \frac{T_E \cdot D_M \cdot D_W \cdot D_B}{T_B} \quad \text{for } T_E \text{ and } T_B \text{ expressed in the same units}$$

$$n = 3.16 \times 10^{10} \cdot \frac{T_E \cdot D_M \cdot D_W \cdot D_B}{T_B} \quad \text{for } T_E \text{ in years and } T_B \text{ in milliseconds}$$

Accumulated cycles (n) refers to the number of erase-write cycles that a memory transistor within a BORAM chip will be subjected to. Elapsed time ( $T_E$ ) is calendar time, and is most conveniently expressed in years. Block process time ( $T_B$ ) is the time required by the BORAM module to store a data block. Generally, the block process time will be determined by the speed limitations of the computer interface protocol specified by the user.

As an example of a  $T_B$  time value, consider the NTDS (ANEW) interface and a block size of 2048 words. The fastest practical flow rate for this interface is about 167,000 words per second, or 6 microseconds per word. Therefore, the time to flow 2048 words is about 12 milliseconds. Because a BORAM storage system can accept data at this rate, the  $T_B$  value would be 12 milliseconds.

In any given operating environment, a BORAM system would actually be engaged in writing data for only a portion of the elapsed calendar time. The product of two duty cycle factors can be used to estimate the write time fraction. The module duty cycle ( $D_M$ ) is the ratio of the run time meter reading to elapsed time since the module was put into service. In other words, the module duty is the time fraction that the module is connected to an external power source - i. e. , run time.

The second duty factor identifies the portion of the run time that is devoted to writing data. This is a more complex factor in that all system operating states must be considered. Write duty cycle ( $D_W$ ) is the write time divided by the run time. For clarity, the run time should be broken down into its component parts.

$$D_W = \frac{\text{write time}}{\text{run time}}$$

$$D_W = \frac{\text{write time}}{\text{write time} + \text{read time} + \text{wait time} + \text{other time}}$$

"Read time" is the time devoted to reading data blocks. "Wait time" is the time when the module is waiting for the computer to provide a command. "Other time" is time devoted to execution of instructions other than write or read. An example of "other instructions" would include STATUS, TEST, and INTERRUPTS.



Another duty factor is required to relate module write time to the actual time spent writing one transistor within one chip in the module. A given chip is associated with one of 256 data blocks stored in the module. The frequency of writing one chip (i. e., one transistor) depends on how often a specific data block is written.

The lowest stress situation would occur if all areas of storage were written with equal frequency. Since there are 256 blocks, the lowest possible value for  $D_B$  would be  $1/256$  or 0.0039. In practice, a uniform distribution of writing over the module address space is improbable. Some blocks will experience a peak duty level while other are rarely written. A rough approximation of the peak might be to assume that only  $1/64$  of the module is written - i. e.,  $D_B$  is about 0.016.

### 1.5.3 Cycle Accumulation Expectations

It is helpful to make a few trial calculations to explore the magnitude of cycle accumulation that can be expected in a practical case.

$$D_M \approx 2/3 \text{ for a 2-shift operation}$$

$$D_W \approx 0.25 \text{ per comments in text}$$

$$D_B \approx 0.016 \text{ per comments in text}$$

$$T_B \approx 12 \text{ milliseconds for NTDS (ANEW)}$$

$$n = 3.16 \times 10^{10} \frac{T_E \cdot D_M \cdot D_W \cdot D_B}{T_B}$$

$$n = 3.16 \times 10^{10} \frac{T_E (2/3) (0.25) (0.016)}{12}$$

$$n = 7 \times 10^6 T_E$$

For these assumptions transistors in a module in use for a 20 year period would accumulate about  $1.4 \times 10^7$  cycles. For a 100-year period  $7 \times 10^8$  cycles would be accumulated. This is probably a reasonable upper bound for actual in service NTDS (ANEW) operation.

Consider the most adverse case allowed by the NTDS (ANEW) specification. Suppose that some means were provided to allow data transfer at 250,000 words per second. A block could then be processed in 8.192 milliseconds. Also arbitrarily assume high duty cycles.

$D_M$  1 for a 3-shift operation

$D_W$  0.5

$D_B$  0.032

$T_B$  8.192 milliseconds

$$N = 3.16 \times 10^{10} \frac{T_E \cdot D_M \cdot D_W \cdot D_B}{T_B}$$

$$n = 3.16 \times 10^{10} \frac{T_E (1) (0.5) (0.032)}{8.192}$$

$$n = 6.17 \times 10^7 T_E$$

For this extreme case, 20 years of operation would result in a transistor cycle accumulation of  $1.2 \times 10^9$  cycles. After 100 years the total cycle accumulation would be  $6.17 \times 10^9$  cycles.

From these exercises, one can conclude that a useful BORAM system can be built if the memory component can tolerate  $2 \times 10^7$  cycles. A comfortable operating margin would exist if more than  $10^8$  cycles can be achieved. If as many as  $10^9$  cycles could be achieved, practical systems would never be affected by transistor endurance during the system lifetime.

#### 1.5.4 Endurance Monitoring

Experiments with drain-source protected memory transistors have shown acceptable device stability out to  $10^{11}$  cycles. It is clear that the BORAM application does not require that level of endurance. For purposes of monitoring production during the MM&T project, it seems appropriate to investigate endurance effects up to  $10^{10}$  cycles.

The vehicle for observation of endurance will be test structures on the BORAM die. A test capacitor will be used to check nitride thickness. A memory transistor will be used to determine pulse response and threshold voltage decay characteristics as a function of cycle stress. The transistor is similar to the transistors in the BORAM array, and can be expected to accurately represent actual array behavior.

The primary tool for gathering data is the VT Tester. This system was described in detail in the second quarterly report. Information from the VT Tester is collected and stored in a computer file. Various data reduction programs have been prepared to process the data files and prepare summary reports.

Analysis of a sample requires several sequential steps. Initially, the device is characterized as to nitride thickness and processing history. Then it is examined thoroughly in an exploratory manner using the VT Tester. This test data is used to establish the proper operating conditions for cycle stress. The device is then cycled  $10^6$  times, and VT Tester readings are obtained again. This sequence is then repeated for every decade from  $10^7$  to  $10^{10}$  cycles. The resulting data is then prepared to show the stability of device characteristics as a function of accumulated cycles.

#### 1.5.5 Endurance Test Development Status

Considerable progress has been made toward establishment of an endurance monitoring capability. During the last quarter the major elements of the monitoring scheme were exercised on a trial basis. These learning experiences have led to an improved definition of hardware and software requirements, and further improvements in both areas are currently being introduced.

Initial experiences with the VT Tester have resulted in definition of some desired modifications. The voltage amplitude of the clear and write pulses were originally set internally by the system. It is now

desired that the operator be able to set those amplitudes to allow exploration of device characteristics for different electric fields. The labor of manually reading and recording data from the VT Tester memory is objectionable. A direct transfer from memory to some machine compatible format for computer data reduction is desired.

The cycle stress equipment is also being examined for possible improvements. At present, all devices being cycled must operate at the same voltage levels with the same timing sequence. Cycle accumulation is judged by recording start and stop time. It appears desirable to increase the flexibility of the cycle stress equipment. Improved control circuitry is being considered to allow individual adjustment of waveform amplitudes, rise and fall times, and pulsewidths for small groups of test samples. Cycle counters with automatic start and stop control are to be provided for each test group. The erase-write cycle time is also being studied for possible faster operation to reduce the elapsed time required to reach  $10^{10}$  cycles.

During February, portions of the software used in conjunction with endurance tests was demonstrated to ECOM personnel. In particular the automatic plotting of threshold decay data and pulse response data were displayed. A variety of programs have been prepared to treat results obtained from single devices, and to compile meaningful statistics from groups of homogenous devices. This work was exploratory, and several optional approaches were examined.

One promising line of approach deals with prediction and monitoring of retention characteristics. This matter will be discussed in further detail in future reports. The concept involved is to use regression analysis on decay slope data to obtain rough predictions of retention time for a device after each decade of accumulated cycle stress from  $10^6$  to  $10^{10}$ . Collection of such data for representative samples will allow computation of statistics for retention on product derived from specific process combinations.

## 1.6 PRODUCTION ACTIVITY

Significant progress was made during the third quarter of the MM&T project production effort. A three-inch wafer BORAM process line installation was completed, and a number of 6000C lots were started. Prototype runs of the 6002 die were evaluated. Adjustments to the 6002 mask set and process conditions were made, and additional runs were started. Additional chips were fabricated for use in the second set of engineering samples.

### 1.6.1 Engineering Sample Fabrication

Production flow as summarized in table 1-1 has improved considerably since the first quarter of MM&T effort. At that time, equipment problems forced an in-line hold of material before nitride deposition. At the end of September 1976, only 29 wafers had reached test against a plan of 78. By December of 1976 that 64 percent deficit of wafers tested was reduced to an 8 percent deficit. At the end of March 1977, the deficit was reduced to 6 percent.

As shown in table 1-1, the chips completed at the end of March were 610 against a goal of 1276. Those die were screened using a 200 microsecond clear and a 100 microsecond write. An additional 452 perfect chips were produced which have slower clear and write response. Therefore, the line yield of perfect devices was 1090 against the goal of 1276. The pulse response distribution was shifted to the slow side because of nitride thickness variation and tunnel layer processing experiments.

During the first 9 months of effort the primary experimental vehicle was the 6000C die produced on two-inch wafers. Two-inch wafer production has been terminated in favor of the new three-inch facility, and the last 6000C die cleared the line in February. Table 1-2 summarizes yield experience for the two-inch product.

TABLE 1-1  
ENGINEERING SAMPLE FABRICATION STATUS

Event	Status to 31 March 1977		
	Plan	Actual	Deviation
Wafer Starts	610	727	117
Wafer Completions	355	339	(16)
Wafers Tested	355	333	(22)
Chips Completed	1276	610	(666)

77-0422 TA 9

TABLE 1-2  
YIELD SUMMARY FOR 6000C EXPERIMENTAL LOTS

Yield Component	Yield Values				
	Target Yield	Actual 1st Quarter	Actual 2nd Quarter	Actual 3rd Quarter	Actual All Production
Process Yield $Y_W$	0.65	0.35	0.63	0.71	0.62
Probe Yield $Y_T$	0.06	No Activity	0.01	0.05	0.03
Sawing Yield $Y_S$	0.98	No Activity	1.00	0.98	0.99
Visual Yield $Y_V$	0.75	No Activity	0.92	0.96	0.95
Overall Yield $Y = Y_W \cdot Y_T \cdot Y_S \cdot Y_V$	0.029	Incomplete	0.006	0.033	0.015

77-0422 TA-10

Process yield is the ratio of wafers into probe test to wafer starts. Prior to production a target process yield of 0.65 was established. During the first quarter of effort a very poor yield of 0.35 was achieved because of improper starting material characteristics which caused low breakdown voltages. In-line screening was instituted to remove the worst material, but this problem also depressed probe yields during the second quarter. As material purchased to revised specifications filled the line during the second and third quarters, the yield rose sharply.

Sawing yield and visual yield exceeded expectations. In fact, the visual yields were so high as to raise some questions as to why. An investigation confirmed that no relaxation of requirements was involved. The product was screened per MIL-STD-883 Method 2010B. The high yield appears to be due to care in processing. For example, the incidence of scratches was very low compared to other products in the same facility. A second possibility is that visual defects for this product tend to cause electrical problems, and thereby, are being eliminated to a large extent at wafer probe.

The dominant yield component is that associated with electrical probe test. Mathematical yield models predict that a die of this size in stable and mature volume production should have an average probe yield of 15.7 percent or about 12 die per two-inch wafer. For engineering sample production, which involves experimental variations of small run quantities, an objective of 6 percent probe yield was established.

During the first quarter, equipment problems and test program development delays prevented testing any product. During the second quarter material began to flow, and a low 1 percent yield was experienced. At that time the low breakdown material and variability in nitride characteristics depressed the yield. By the third quarter a positive yield growth trend was established. The yield of perfect devices during this period was about 9

percent, but many of those chips had slow pulse response. Only 5 percent yield was experienced to the 200 microsecond clear and 100 microsecond write screen.

When examined in detail, the 6000C yield experience verified mathematical model predictions. High yield lots reached predicted levels. For this product as many as 30 die per wafer have been yielded to fast write criteria. It was not uncommon to see 10 to 20 die per wafer to fast criteria, and 15 to 25 die to slower criteria. Overall yield statistics were brought down by zero yield lots where a specific material or processing problem existed, or an experimental variation of process conditions was unsuccessful.

It should be commented that the production planning control functions for the past quarter have been complex because several versions of the BORAM product were running simultaneously. The 6000C chip was produced on both two- and three-inch wafers. The 6002 chip was produced on two-inch wafers. Three-inch production of the 6002 will be limited until yield levels for the 6000C are verified. Two-inch production of the 6000C has been terminated.

#### 1.6.2 Production Plan for Next Period

Production objectives for the next period include replacement of the 6000C by the 6002 as the primary production vehicle, and completing the conversion to the three-inch line. The 6000C will be used as the vehicle for initial tuning of the three-inch line. The line configuration for confirmatory sample production will be finalized, and the equipment and tooling identified to ECOM. BORAM 6002 chips from two-inch wafers will be provided for the second set of engineering samples.

#### 1.6.3 BORAM Three-Inch Wafer Processing Facility

Westinghouse has established a three-inch wafer processing facility for BORAM products. Conversion from two to three-inches diameter silicon wafers is expected to provide a 58 percent cost reduction for labor and materials per yielded die. The new line is being made available for use by the MM&T project.



The line development task was performed independently of the MM&T two-inch production activity. Equipment procurement, installation and process debugging was accomplished without major problems. The facility is in operation using 6000C chips to provide yield impact feedback data. The first 6002 lots will be processed during the coming period.

## 2. CONCLUSIONS

Work with the 6000C chip matured considerably during the past quarter. Consistent yields with a rising trend were demonstrated. The first set of engineering samples containing 272 of the 6000C devices were delivered. The first 3-inch wafer production of 6000C devices was initiated. Additional experience was gained with testing the devices in the hybrid circuit form.

At present, the project is oriented toward use of the 6002 integrated circuit manufactured on 3-inch wafers in an improved hybrid circuit configuration. The past quarter showed steady progress toward demonstration of each of those elements in time for confirmatory sample production.

The major problem areas for the project are test development and the time required for proper evaluation of process and product alternatives. It is expected that schedule delays will increase to about 8 weeks during the next quarter to resolve those issues.

### 3. PROGRAM FOR NEXT INTERVAL

Preparation of the second set of engineering samples is the major task for the next quarter. The samples will consist of 5 hybrids based on the 6002 chip, and 12 hybrids based on the 6002 chip. Test data and a description of test methods are required.

In addition to the above, three data items will be delivered with the second set of samples: (1) a revised version of SCS-503 per MIL-S-8349 for ECOM approval, (2) drawings and circuitry covering the mechanical and electrical requirements of the device, and (3) a layout of the pilot line indicating the processes and tooling that will be used for confirmatory sample fabrication.

Test development and evaluation of process and product alternatives will continue as high priority efforts. In particular, improvements will be made to the VT Tester and associated data reduction programs.

#### 4. PUBLICATIONS AND REPORTS

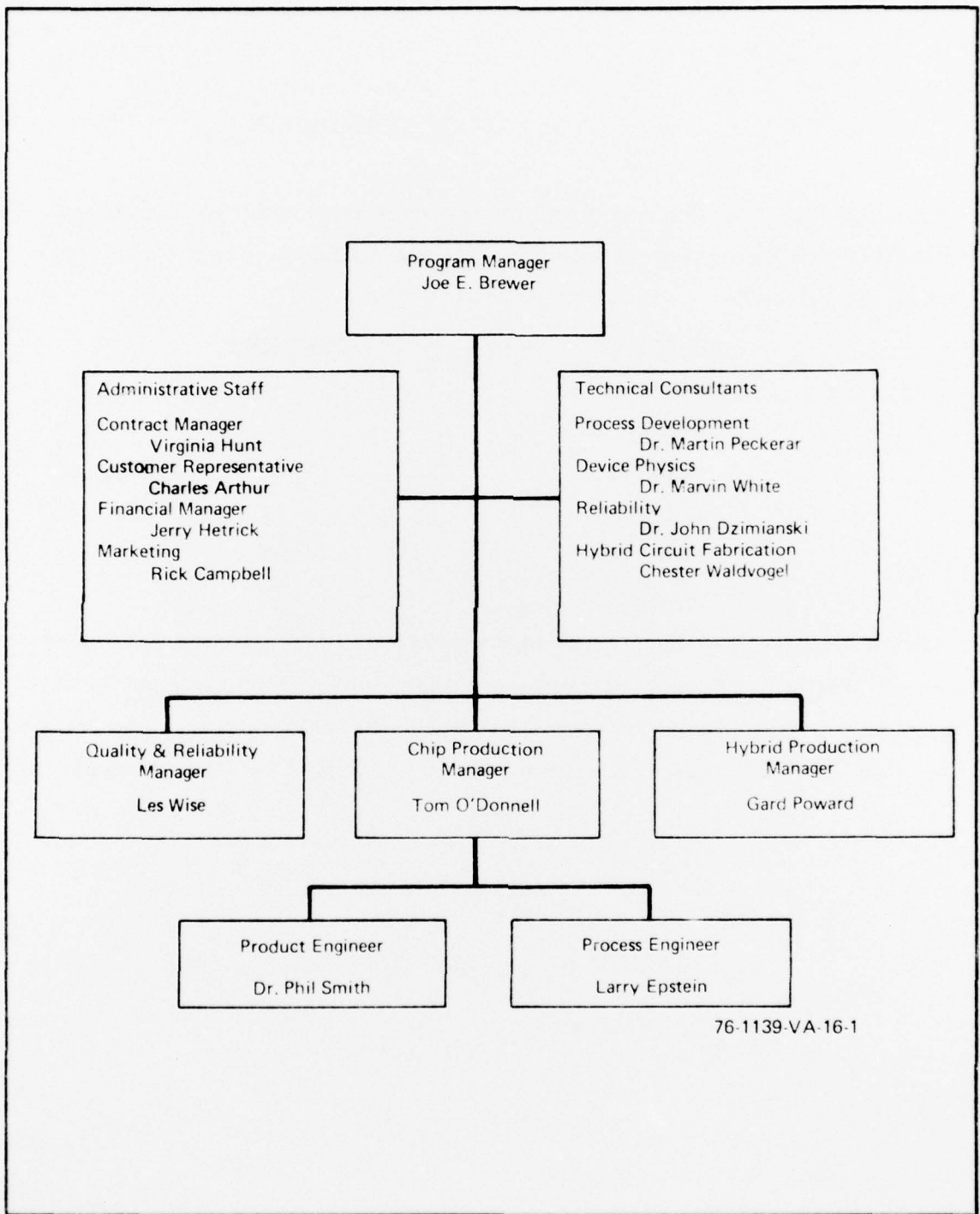
During the past quarter, a paper entitled "Low Cost MNOS BORAM" was accepted and approved for presentation in May at the 1977 National Aerospace and Electronics Conference in Dayton, Ohio. A copy of the text is appended.

## 5. IDENTIFICATION OF TECHNICIANS

The following key engineers and management personnel were employed on the BORAM manufacturing methods project during January, February, and March of 1977.

<u>Technician</u>	<u>Manhours</u>
J. Brewer	340
M. Peckerar	81
C. Walvogel	74
T. O'Donnell	62
P. Smith	258
L. Epstein	72

Some changes have been made in the program staff. Figure 5-1 shows the organization. Virginia Hunt has replaced Howard Weinstein as Contract Manager. Rick Campbell replaces Gerry Cooley in Marketing. Les Wise assumes the Q&R Managers tasks formerly performed by Roman Knysh.



76-1139-VA-16-1

Figure 5-1 Westinghouse MNOS BORAM Program Organization

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APPENDIX A

Low Cost MNOS BORAM

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National Aerospace and Electronics Conference  
Dayton Convention Center 17-19 May 1977

# Low Cost MNOS BORAM

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## ABSTRACT

The economic feasibility of MNOS block-oriented-random-access-memory (BORAM) as an alternative to fixed-head electromechanical storage depends on the producibility of the memory components. A new p-channel metal gate MNOS BORAM die is currently being used on a U.S. Army manufacturing methods project to demonstrate the practicability of low cost high-yield production. This paper describes the new chip in the context of previous MNOS technology, and points out the design features which contribute to cost reductions.

## INTRODUCTION

More than 10 years ago an engineer at the U.S. Army Electronics Command conceived the idea of a BORAM system as a non-mechanical storage which could access data blocks without rotational latency at electronic speeds. The objective of the BORAM concept was to provide the military with a reliable alternative to magnetic discs and drums.

MNOS BORAM development began in 1972 when ECOM let a contract to Westinghouse Electric Corporation for an advanced development model of a 16.8-megabit storage unit. Later, the U.S. Navy joined in the sponsorship of that program, and greatly influenced the design. Over the past five years both system concepts and integrated circuit design have been continuously refined and improved.

Reference 1 provides a detailed description of the BORAM advanced development model and of independent government evaluation results. The module is a self-contained general purpose secondary storage unit. No external controllers or power supplies are required for operation. It has very low (< 100 watts) power dissipation, and requires no special cooling arrangements. Data access delay time (< 30 microseconds) is more than 100 times better than the fastest drum. No rotational latency exists. Data flow rates match the maximums allowed by computer interface specifications. The module mechanical design demonstrates volume and weight advantages over comparable fixed-head magnetic systems. In addition, the highly modular nature of the design contributes to ease of interfacing and to economics in logistics.

Government evaluation results with respect to the advanced development model were positive. Observation of the module confirmed that MNOS BORAM systems can be a superior alternative to fixed-head electromechanical storage.

Other Government contracts have been established to address questions associated with the memory components. In July of 1976, Westinghouse Electric Corporation began work on a U.S. Army manufacturing methods project to establish a pilot production capability for MNOS BORAM multichip hybrid circuits. The initial vehicle for that development was the 2048-bit BORAM 6000C integrated circuit. This highly successful design has been used to establish and refine manufacturing processes suitable for volume production.

Throughout this manufacturing methods project cost reduction has been a dominate theme. The subject of this paper, the BORAM 6002 chip, is the result of efforts to shrink and simplify the older 6000C device. The 6002 device is currently being characterized, and will shortly go into pilot production.

## DEVICE DESCRIPTION

The BORAM 6002 integrated circuit is a nonvolatile block-oriented read/write memory device designed for use in computer secondary storage systems. Because of wide circuit design margins and a small die size, the 6002 provides a major cost improvement over previous BORAM devices. Figure 1 is a photograph of the 6002 die, and figure 2 shows its normal packaged configuration.

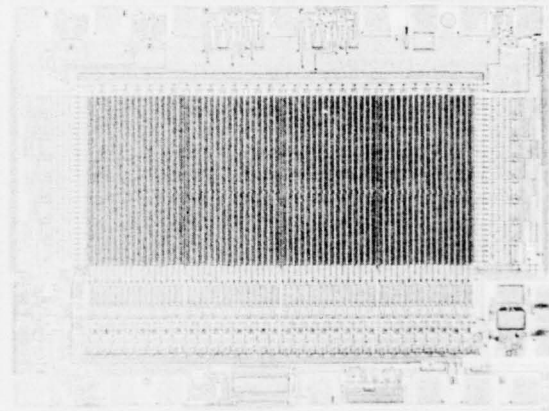


Figure 1. BORAM 6002 Die

Within the 6002, information is stored in metal-nitride-oxide-semiconductor (MNOS) memory transistors by trapping charge at the nitride-oxide interface in the dual dielectric gate insulator. Charge may be inserted or removed electrically. Power supply and signal voltages may be removed from the chip and the charge will remain intact for long periods of time. After being written with a 100-microsecond pulse, the 6002 is required to retain data for 4,000 hours independent of the presence or absence of power supply voltages.

Individual memory cells consist of two drain-source protected (DSP) memory transistors. Differential circuits are used in the 6002 to reduce sensitivity to manufacturing process variation, supply levels and temperature changes. The detection circuitry can reliably distinguish threshold voltage differences as small as 0.1 volts, and is immune to any disturbing factors which affect both transistors in a cell. No external read reference voltages are required. The operating temperature range is  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

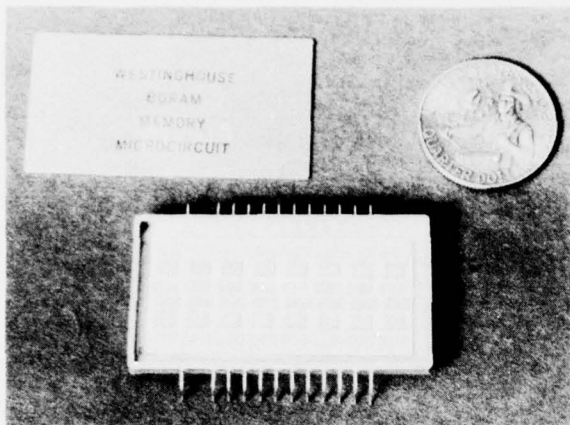


Figure 2. BORAM Memory Microcircuit

The 6002 is a read/write memory -- not an alterable ROM. As such, it is required to be usable after  $10^{10}$  erase-write cycles. In a typical BORAM system it would take almost 100 years to accumulate  $10^{10}$  cycles.

As shown in figure 3, the 6002 has 15 pins. All signals swing a nominal 0 to -15 volts except chip select ( $\overline{CS}$ ) which swings 0 to -35 volts. Signals are referenced to  $V_{CC}$  which is taken as 0 volts. The  $V_{EG}$  supply is nominally -30 volts. Power dissipation when operating is less than 200 mW. The address inputs are multiplexed and latched internally to save address pins. The data output line DR is tristate, and will enter the high impedance state if chip select ( $\overline{CS}$ ) is high.

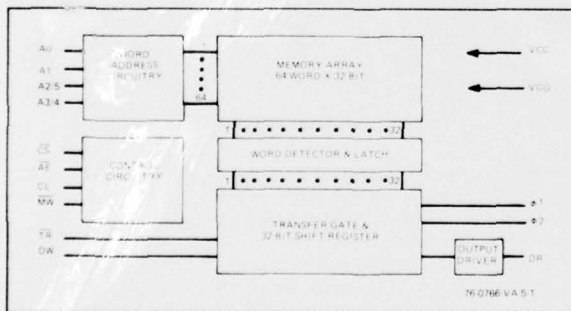


Figure 3. BORAM 6002 Functional Block Diagram

The chip incorporates many features to ensure reliability and to avoid problems during assembly. Bonding pads are greater than  $5 \text{ mils}^2$ , and are positioned on opposite sides of the die to allow efficient use of space in the hybrid circuit. The nitride layer in the gate dielectric serves as an ion migration barrier and eliminates reliability failures because of latent oxide defects. A glass overcoat guards against scratches due to handling. Protective devices on all inputs avoid damage by static charge.

## PHYSICAL FEATURES

The 6002 die measures  $2.5 \times 3.3 \text{ mm}^2$  ( $99 \times 128 \text{ mils}^2$ ), and features a  $1020\text{-}\mu\text{m}^2$  ( $1.58 \text{ mil}^2$ ) two-transistor cell. The ratio of array area to die area is 0.26. When judged in the context of contemporary MNOS die as shown in table 1, the 6002 layout is seen to be rather efficient. The two-transistor cell in the 6002 is almost one-half the size of the 6000C cell. In fact, it approaches the dimensions of some of the one-transistor cells. Only the Westinghouse 7006 chip which uses a polysilicon gate in the array region has a significantly higher density.

TABLE 1  
EXAMPLES OF CONTEMPORARY MNOS DIE

IDENTIFICATION	DESCRIPTION	DIE SIZE (mils x mils)	CELL SIZE (mil <sup>2</sup> )	ARRAY TO DIE AREA RATIO
6000C	2 x 2 FET cell	163 x 169	2.95	0.22
7006	16 x 1 FET cell	135 x 200	0.49	0.30
NCR 1105	1 x 2 FET cell	147 x 115	2.80	0.17
NCR 2401	4 x 1.1:16 FET cell	160 x 164	1.40	0.22
NCR 2800	8 x 1.1:16 FET cell	197 x 227	1.40	0.26
NCR 3400	4 x 1 FET cell	240 x 187	1.60	0.15
NCM 7040	256 bits, 2 FET cell	125 x 125	2.72	0.04
NCM 7050	1 x 2 FET cell	160 x 154	2.72	0.11
NCM 7051	1 x 2 FET cell	169 x 171	2.48	0.09

Figure 4 shows the details of the memory cell. It is conventional in form and conservative in dimensioning. Separate source and drain diffusions are provided for each memory transistor. A cell requires one metal line and four diffused lines. No contact windows to silicon exist. Four masks are used to form the cell, and alignment is not critical. All features are stripes compatible with present day 4-micron technology.

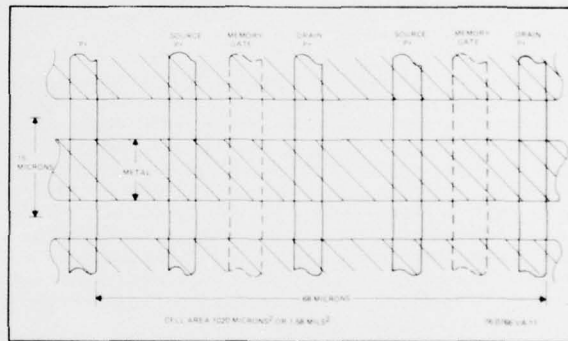


Figure 4. BORAM 6002 Two-Transistor Cell

In MNOS cell designs a limiting factor has been the dimensional pitch achievable by the circuitry on the periphery of the array. For example, the pitch of the word address circuitry (row decoder) in the 6000C device determined the vertical dimensions of the array. In the 6002 approximately the same decoder pitch was maintained, but two decoders were used. By bringing the row selection circuits into both sides of the array to interleaved rows, the cell density was almost doubled.

Examination of the die photo shows little wasted space in the peripheral circuit areas. The layout maintained a 0.26 array to die area ratio even with increased cell density. The 6002 die area is 46 percent of the 6000C area. The area reduction was achieved by approximately equal shrinkage of both array and peripheral circuitry.

## CIRCUIT OPERATION

As the functional block diagram of figure 3 shows, the 6002 contains a fully decoded 64-word by 32-bit RAM and a 32-bit dynamic two-phase shift register. All I/O takes place serially through the shift registers. Parallel bidirectional data transfer between the RAM and the shift register takes place via an internal 32-bit latch.

The RAM and shift register can operate independently. This allows the RAM to be writing data from the latch into the memory array while new data is being shifted into the register. High bit rates may be maintained at the I/O terminals while the RAM need operate at only 1/32 of the external rate. In a practical BORAM system working into standard military interfaces, maximum shift rates of a few hundred kilohertz will be required. Therefore, write times on the order of 100 microseconds can be allowed without delaying the data flow.

It is an interesting aspect of the BORAM chip organization and the system application that no critical dynamic performance requirement is imposed on the chip. The chip performance capability greatly exceeds actual use conditions. For example, the shift registers operate quite well at 5 MHz, but are only required to operate at a few hundred kilohertz.

To store data in a memory cell, two operations are performed. First, the cell is cleared or initialized using the clear signal (CL). This places both memory transistors in the high conduction threshold state. Second, the data present in the latch is written into the cell using the memory write (MW) signal. In response to writing, one transistor in the cell is forced into the low conduction state, while the second transistor remains in the high conduction state.

The 6002 allows clearing of the entire chip with one pulse, or optionally allows clearing of 128 bits as a function of the address inputs and the control signal sequence. Writing takes place in 32-bit words as a function of the address inputs and the control signal sequence.

## SUMMARY

The 6002 chip design has advanced the state-of-the-art of p-channel metal gate MNOS BORAM devices in terms of density and circuit simplification. The 1.58-mil<sup>2</sup> two-transistor cell and efficient peripheral circuit geometry are superior to designs described in the literature. The low voltage input signals, reduced number of supply voltages, and the reduced pin count imply economic gains at the system implementation level. Because of the reduction in die area, the 6002 chip is expected to cost less than 1/5 of its predecessor, the 6000C.

## ACKNOWLEDGEMENT

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