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SCAN CONVERTER FOR LIQUID WATER CONTENT ANALYZER

Raytheon Company
Boston Post Road
Wayland, Massachusetts 01778

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Final Report

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Cursor
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the work done to provide an interface between an Interdata 7/32 used as an analysis tool for the determination of liquid water content density along a rocket trajectory and a digital scan converter and contour refresh memory system developed as a tool for radar meteorological studies. A complete hardware description of the scan converter and contour refresh memory system as modified for operation with the Interdata 7/32 is provided.

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TABLE OF CONTENTS

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TABLE OF CONTENTS (CONTINUED)

LIST OF ILLUSTRATIONS

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SECTION 1. INTRODUCTION

This equipment converts the polar-coordinate outputs of a weather radar and signal processor to cartesian-coordinate form, contours the video, then stores the resulting data in four independent image-oriented memories, each of which refreshes one raster-scan color television monitor.

The most significant advantage of this system over conventional monochrome radar-image-storage devices lies in the ability of the operator to unambiguously recognize sixteen color-coded levels. Stored images of RHI or PPI radar scans can be retained indefinitely, updated, or erased independently of each other. When used with an appropriate radar scanning sequence, the system generates a constant altitude PPI (CAPPI) display for each of four selectable altitudes. Other front-panel controls determine distance scaling, origin location, range and altitude marker spacing and range cell width. Contour threshold colors - 0 (black) thru 15 (red) and levels (0 thru 99) having been set up on an array of thumbwheel switches can be entered into any or all of the displays in the form of a legend or color key.

Memory requirements have been limited to about 328,000 bits per display by performing operations such as coordinate conversion, scaling, translation, introduction of markers, and video contouring prior to storage of the image. Each of the four memories contains a 248 x 255 array with a four-bit code to represent the color and/or intensity of individual points. In addition, the contour threshold colors and levels as well as parameters such as antenna angle, marker spacing, and time are presented within a 248 x 70 ancillary data area along the right edge of each picture.

An interface with an external minicomputer permits manual or automatic transfer of image data between the refresh memories and the computer. A trackball-positioned cursor enhances operator interaction with both the scan converter and the computer.

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SECTION 2. GENERAL DESCRIPTION

The block diagram presented in Figure 2-1 should be referred to while reading the following description of the scan converter.

2.1 Scan Conversion Processor

All front panel controls (except for those on the monitors and power control panel) are located on the Scan Conversion Processor or on the LWCA (Liquid Water Content Analyzer) control panel and are connected to various cards within the processor as shown. The Scan Conversion Processor accepts synchro or binary inputs for antenna azimuth and elevation angles as well as video and timing signals from a radar signal processor. The input information is converted in real time from its polar form to a rectangular form suitable for entry into the image-oriented memories. The processor also generates all memory addresses, timing, and control signals needed by the four memory-inte[illegible] units, plus alphanumeric data and color patches.

[illegible]thin the Scan Conversion Processor is a Display Data Interface (DDI) [illegible] permits communication between the Scan Converter and a Universal Logic Interface (ULI) of an Interdata 7/32 minicomputer. The minicomputer treats the Scan Converter as a peripheral and can perform data transfers to and from its refresh memories. A cursor can be switched on in any display, its position adjusted, and the data in the refresh memory at that position transmitted to the computer by operator interaction through the LWCA control panel.

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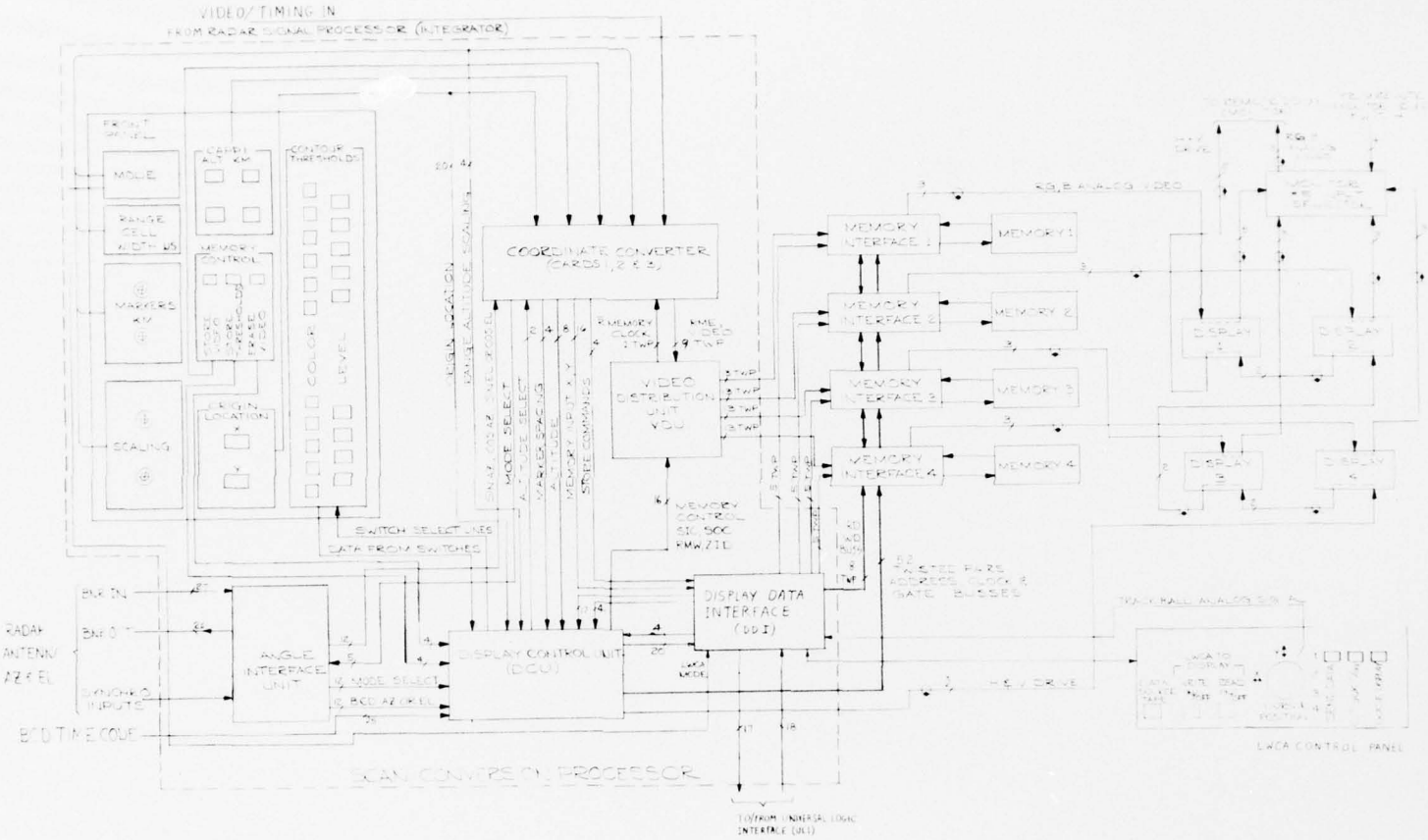

Figure 2-1. Scan Converter Block Diagram

2.2 Memory Interface Units

Each Memory Interface Unit (MIU) performs parallel to serial and digital to analog conversions on its memory output to generate red, green and blue video signals for the corresponding display. These units also execute code conversion and contouring on the incoming video as a function of color patches and contour levels stored in the associated memory. Intermediate storage and logic in each MIU enables it to alter data in its memory as commanded by the Scan Conversion Processor.

2.3 Memories

The image storage media are conventional AMPEX magnetic core memory systems having 8192 40-bit words for each display. They have split cycle times of 750 nanoseconds and self-contained power supplies which also power each associated MIU. Data sheets are included in the Appendix.

2.4 Displays

The displays are 19-inch CONRAC delta-gun color monitors of the type used in television studios. Each unit has red, green and blue video inputs driven by its MIU. All of the displays are synchronized by the same H and V drive pulses from the Scan Conversion Processor. A fifth monitor with remote selector can be switched to display the same image as any one of the four independent displays. Data sheets for the monitors have been included in the Appendix.

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SECTION 3. OPERATION

3.1 Display Adjustment

Each monitor should have its VIDEO switch in the 0 dB position for normal viewing. The MONO position may be helpful, in certain cases, for distinguishing colors. The OFF position might be useful as a standby mode in lieu of turning the power off.

The BRIGHTNESS control should be used to set the black background level (observe the area around the alphanumerics) to a point near the threshold of visibility. The CONTRAST control can then be used to obtain the desired intensity. The illuminated number at the top of each monitor is red when information is being stored in its memory.

3.2 Contour Threshold Entry

The contour threshold switches are arranged in the same pattern on the front panel of the Scan Conversion Processor (see Figure 3-1) as on the actual displays. Any of the 15 color-selectors can be set to any color between 0 (black) and 15 (red).* The 14 level-switches should be set up in ascending magnitude order from bottom to top. An area of the display will take on a color of a given patch if the corresponding signal processor output is equal to or greater than the level below the patch and less than the level above the patch. Should these levels be set to the same number, the color in the patch between them will never appear.

Having set up the contour threshold switches, the operator need only depress the STORE THRESHOLDS button for each display in which this set of contour thresholds is desired. The previous set of thresholds in that memory is then replaced by the new set without affecting the other display information which had been entered using the previous set of thresholds. (This situation, where the thresholds do not match the displayed information, can be avoided by pushing the appropriate ERASE VIDEO button before entering new contour thresholds.) All subsequent incoming video will be contoured according to the new set of thresholds.

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*Color 15, however, is reserved for range and altitude markers and has the property of not allowing itself to be written over. Patterns appearing in this color can only be removed by erasure.

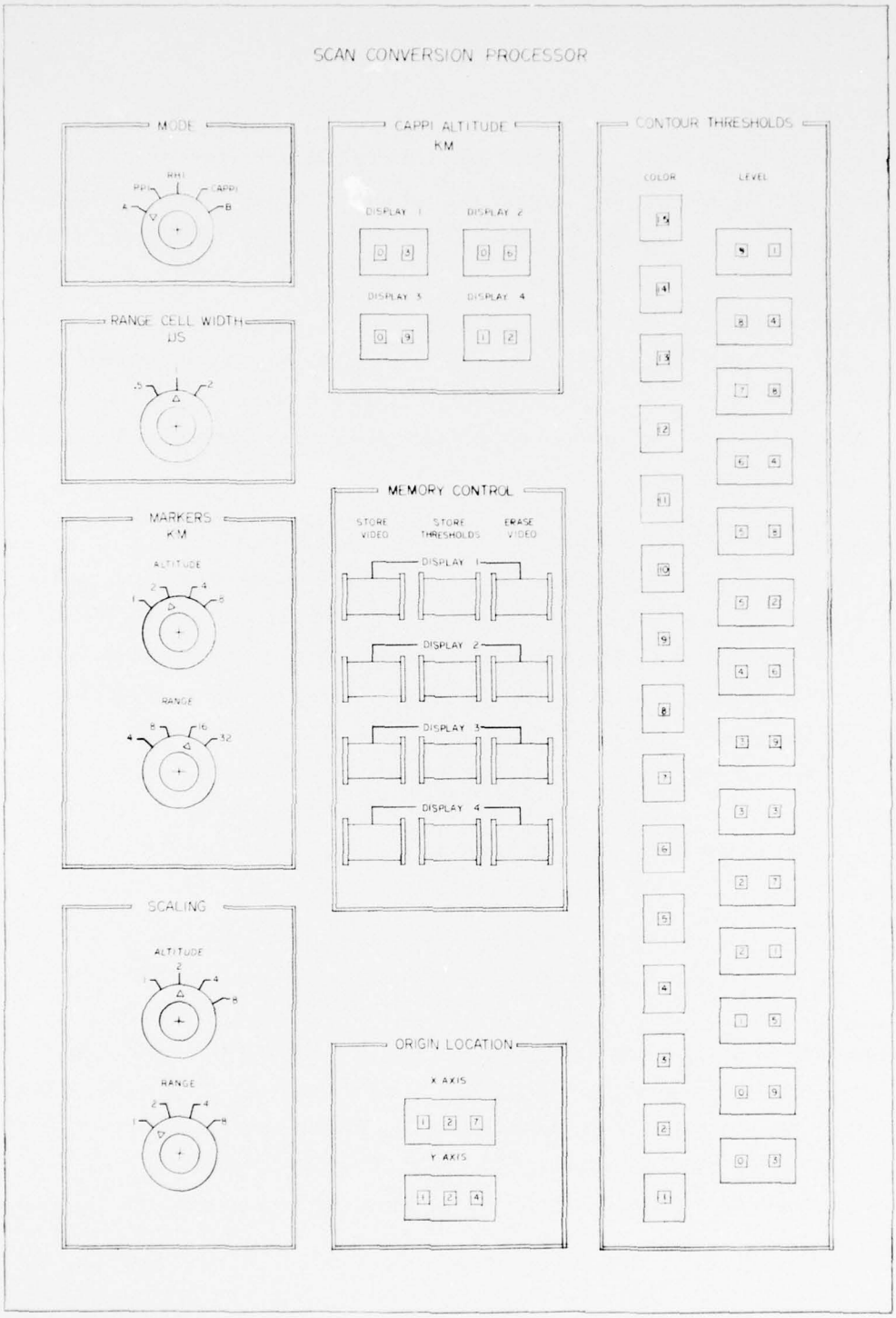


Figure 3-1. Scan Conversion Processor Front Panel

3.3 Mode and Range Cell Width Selection

These controls must be set to correspond with the radar scan sequence and the operating conditions of the radar signal processor. In the RHI (Range Height Indicator) mode, the display will present ground range along the X axis and height along Y. The antenna azimuth angle is shown after AZ, in the lower right corner, to the nearest degree.

The PPI (Plan Position Indicator) mode yields a plan-view display, with the Y-axis running North-South and the X-axis running East-West. The antenna elevation angle appears after EL to the nearest 0.1 degree.

Either RHI or PPI formats can be set up in any display or combination of displays by depressing the desired STORE VIDEO switches, which are active when lit. When a STORE VIDEO switch is on, the large number above the corresponding display is illuminated in red. The CAPPI (constant altitude PPI) mode, also permits use of any of the displays, with the CAPPI ALTITUDE switch settings appearing after AL at the lower right of each display. Each display represents a PPI at the altitude selected.

3.4 Scaling and Location of the Origin

The ORIGIN LOCATION switches provide a means of locating the point corresponding to the radar antenna at any position within the display area. The units employed correspond to display elements at (X, Y); (0, 0) is in the upper left corner, while (249, 247) is in the lower right. The center, normally used for PPI formats, is (127, 124).

ALTITUDE (RHI only) and RANGE SCALING switches can be used to vary the scaling as listed in Table 3-1.

Table 3-1. Full Scale Range and Altitude vs Scale Switch Positions (RHI Mode)

SWITCH POS:	1	2	4	8
ALTITUDE:	128 KM	64 KM	32 KM	16 KM
RANGE:	256 KM	128 KM	64 KM	32 KM

3.5 Marker Spacing Selection

MARKER switches are provided to select ALTITUDE (RHI only) or RANGE marker spacing. In PPI or CAPPI modes, the selected range marker spacing is indicated in kilometers after RM = at the lower right of the display. When the RHI mode is employed, the selected markers are indicated in the display in the following format: M (altitude marker spacing); (range marker spacing) in kilometers.

3.6 Time Code

The lower right corner of each display contains time information in the following format: T (day of the year); (hour of the day); (minute). The time readout of a particular display is updated only while information is being stored in the memory of that display.

3.7 Crosshatch

Mode switch position B is provided as a test position in which a crosshatch is developed for monitor alignment purposes. The crosshatch appears in the color corresponding to full-scale video (the top patch), while the background appears in the color corresponding to zero video (the bottom patch).

3.8 Liquid Water Content Analysis

Mode switch position A sets up conditions needed for LWCA operation, covered by AJJ-21 in the Appendix where LWCA control panel operation is also described.

SECTION 4. DETAILED CIRCUIT DESCRIPTION

The descriptions appearing in these sections generally refer to diagrams included among the text. In some cases; however, it might be helpful to refer to the actual schematics. A complete listing of drawings applicable to the LWCA scan converter can be found in AJJ-26 of Appendix D.

4.1 Angle Interface Unit

The Angle Interface Unit, located in the upper-rear position of the coordinate converter drawer, accepts synchro azimuth and elevation data in standard R_1, R_2 and S_1, S_2, S_3 format and converts these data to the following outputs:

Scaled BCD azimuth angle, 1^{o} resolution
Scaled BCD elevation angle 0.1^{o} resolution
Sine/cosine azimuth 13 bits
Sine/cosine elevation 13 bits
Elevation greater than 12.65^{o} flag

Azimuth and elevation synchro inputs are converted to 14-bit binary numbers (MSB=180^{o}) in Data Device Corporation synchro to digital converters model ESDC-6*. (These converters are inhibited during sampling by the S/D inhibit command input.) The 14-bit binary outputs are fed both to rear panel connector J3 through line drivers and to multiplexers A21 through A24 and A7 through A10.** These multiplexers select binary angle data from either a rear panel connector J4 or from the synchro to digital converters. They have been provided should the need arise to drive the system from a digitally generated angle source. If J4 is not connected, the multiplexer select line is pulled up so that the converter outputs are selected.

Binary angle data is next converted to sine and cosine in Interface Engineering sine/cosine controller model 109 and angle to sine converter model 108.* The controller adapts the angle to sine converter to full four quadrant sine and cosine operation. A logic zero on the controller input terminal 23 selects sine.

The sine/cosine converter channel is multiplexed once each PRF interval between azimuth and elevation inputs through multiplexers A16 through A18. This technique was employed to optimize the efficiency of the converters.

*See Appendix for Data Sheets

**Actually only 12 bits of Azimuth and Elevation are included in J3 and J4 at the rear panel; the two additional elevation bits, both input and output, are connected to J2 - See 897392.

An Interface Engineering binary angle to scaled BCD converter, model 107,* provides the drive for the CRT antenna angle display. This converter is switched between azimuth and elevation by multiplexers A11 through A14, controlled by the front panel mode switch. Azimuth is displayed in the RHI mode; while elevation is displayed in all other modes.

Multiplexers A3, A4 and A5 line shift the scaled BCD four lines down when displaying elevation to provide the increase in resolution from 1^{o} to 0.1^{o}.

The magnitude comparators, A20 and A25, generate a logic one when the antenna elevation angle exceeds 12.65^{o}. This output is used by the coordinate converter in the CAPPI mode to initiate the 2^{o} elevation step.

4.2 Coordinate Converter

The Coordinate Converter derives the cartesian memory address from the radar parameters of elevation angle, azimuth angle, radar trigger and the range gate clock. The azimuth angle and elevation angle are sampled once every radar period to form the basis of the coordinate transformation. The block diagram of the Coordinate Converter unit is shown in Figure 4-1.

4.2.1 Angle Parameters

In the angle interface unit, there are two synchro-to-digital converters; one dedicated to the azimuth angle, θ, and the other dedicated to the elevation angle, ϕ. The outputs of each S/D converter are multiplexed into a sin/cos converter such that by control of the multiplexer and function switch of the sin/cos converter, the following functions can be obtained and stored in a D type register:

$\sin \phi$
$\cos \phi$
$\sin \theta$
$\cos \theta$

4.2.2 Fixed Constant Multipliers

In the RHI display, the altitude is R $\sin \phi$, and the projection of the range is R $\cos \phi$ where R is the range expressed in kilometers. Card number 1 has two 12 x 12 fixed constant multipliers which multiply the single function input by a fixed constant such that the output is expressed in kilometers with the binary point 12 bits from the LSB. For a 2 μsec unit range cell, the conversion factor (radar distance) built into the multipliers is .2998046. All subsequent calculations following the fixed constant multipliers are done directly in kilometers which is a very useful simplification especially in determining the range markers.

*See Appendix for Data Sheets

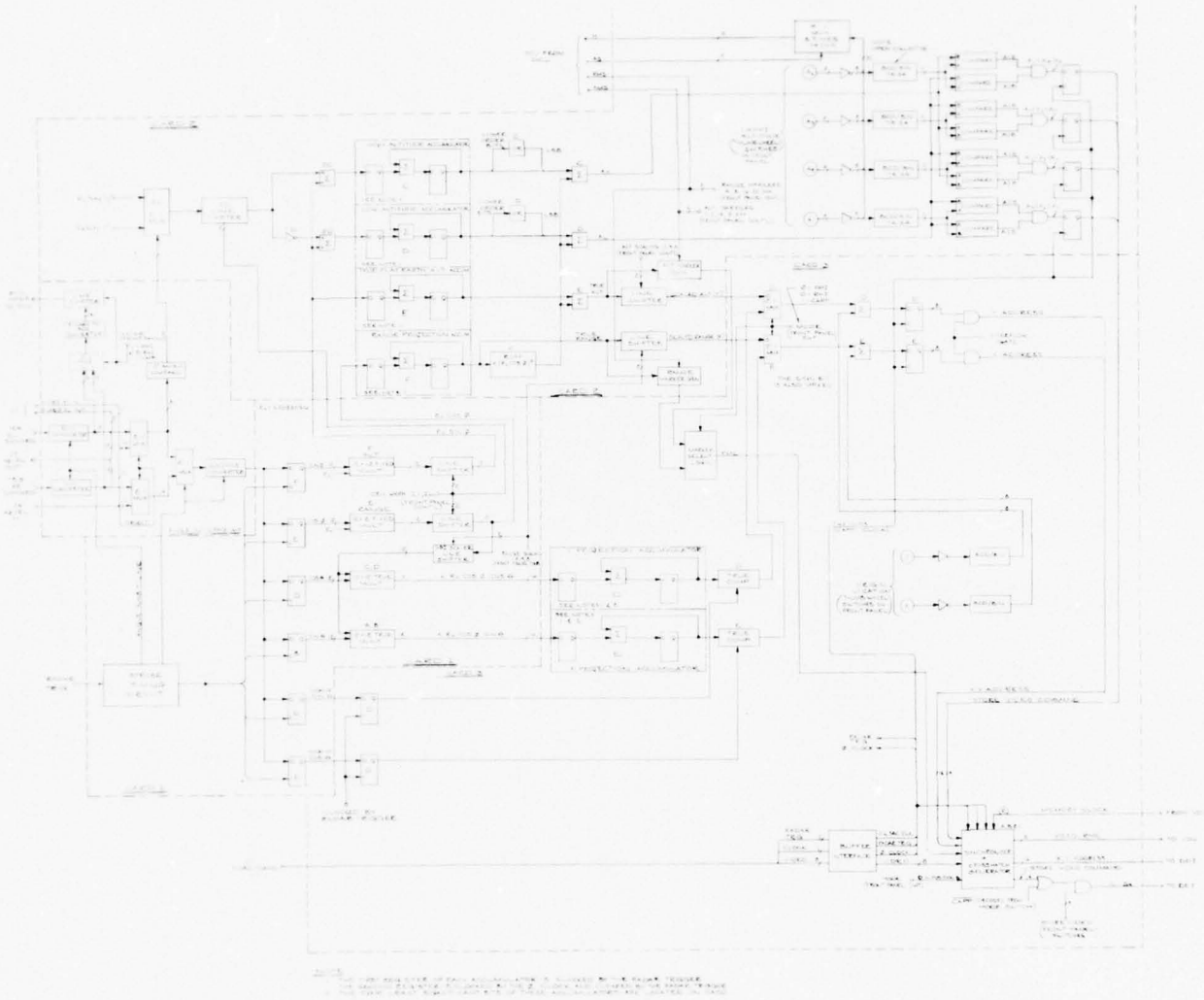


Figure 4-1. Coordinate Converter Block Diagram

The fixed constant multipliers are each composed of adders arranged in an array such that the input is multiplied by a constant. Groups of 4-bit adders are pyramided to form a subset of 4-bit numbers with all the carry-outs fed into the carry-inputs of the next higher order 4-bit array. The schematic diagram shows the array in detail and also in block diagram format. The line shifter following each multiplier array is controlled by the front panel switch that selects the range gate. The line shifter, *in effect, multiplies the output* by 1/4, 1/2 or 1 corresponding to the range gate widths of 1/2 μsec, 1 μsec or 2 μsec. A secondary line shifter operates on the unit range vector $R_o \cos \phi$ and is used for scaling in the PPI mode.

4.2.3 PPI Mode - True 12 x 12 Multipliers

In the PPI mode, the projected range, $R_o \cos \theta$, is broken up into its X (East-West) and Y (North-South) coordinates. The azimuth angle θ is measured from the North-South line such that

$$X_o = R_o \cos \phi \cos \theta$$

and

$$Y_o = R_o \cos \phi \sin \theta$$

Since $R_o \cos \phi$ had already been established in one of the fixed constant multipliers, two other multipliers are used to establish X_o and Y_o, the unit component vectors for the PPI display.

The 12 x 12 true multipliers consists of an array of partial product terms added in a pyramid structure very similar to the fixed constant multiplier. The partial product terms and summation pyramid are detailed in the schematic drawing of the 12 x 12 multipliers.

Card 2 of the coordinate converter thus develops the unit altitude $R_o \sin \theta$, the unit range $R_o \cos \phi$, and the component vectors of the unit range $R_o \cos \phi \cos \theta$ and $R_o \cos \phi \sin \theta$ all evaluated in kilometers.

4.2.4 Address Accumulators - Card 2 and Card 3

The unit coordinates have been derived for the first range cell. Coordinates for other range cells can be easily obtained by taking advantage of the fact that the range cell number increases linearly in a radar. Thus, the

coordinates for range cell j + 1 are the coordinates for range cell j added to the value of the respective coordinates of range cell 1. This accumulator type structure is shown in the block diagram and is repeated 6 times in the coordinate converter. The unit vectors are loaded into each accumulator at the beginning of each radar period and at the same time the old data is cleared out. The accumulator is clocked by the range gate clock of the integrator to form the cartesian coordinate addresses.

For the RHI mode of operation, the Y address corresponds to the scaled altitude and the X address is the scaled range. For the PPI or CAPPI mode of operation, the Y address corresponds to the North-South component of the range vector and the X address corresponds to the East-West component of the range vector. The mode switch controls the multiplexer to select the appropriate coordinates as shown in the block diagram. After the multiplexer, constants controlled by thumbwheel switches can be added independently to the X and Y coordinates to affect translation in both directions. A hard limiter circuit is used to prevent overflow and erroneous addresses.

4.2.5 Range and Altitude Markers

The outputs of both the range and altitude accumulators are in kilometers (see para. 4.2.2) i.e., the 13th bit is 1 KM, the 14th is 2 KM, etc. Detection of the clock cycle at which time the bit corresponding to a preselected range changes state is used as the marker pulse. The circuitry consists of comparing the selected bit with the same bit delayed one clock period in an exclusive or circuit to form the marker pulse. The marker pulse goes through the synchronizer to produce the range mark enable (RME) signal.

4.2.6 CAPPI Mode

In the CAPPI mode, the antenna sweeps 360°, or a segment thereof, at a single elevation angle and upon reaching its starting or terminal position (for less than 360° sweep) the elevation angle is incremented and the process is repeated. A typical CAPPI will use the following elevation angles, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 16, 18 and 20°. This volume scan permits

the operator to crudely establish a map of a prescribed altitude or many altitudes, since, in general, each radar beam will pass through all possible altitudes. By carefully selecting and storing the incoming data, it is possible to develop a constant altitude PPI map at any given altitude. Because the elevation angle of the antenna is incremented in small steps, a map at precisely the desired elevation would provide very few sample points; it is the established procedure to sample the elevation at or near the desired elevation.

Figure 4-2 shows a constant altitude intersecting three different angle vectors or rays. The solid lines represent the CAPPI elevation angles and the dotted lines represent elevation angles between the CAPPI rays. For elevation angle ϕj, information is recorded when the altitude reached by the altitude vector associated with the ray at $\phi\, j + 1/2$ is equal to the preselected altitude, similarly the data recording is stopped when the altitude reached by the altitude vector associated with the ray at $\phi\, j - 1/2$ equals the preselected altitude. From the diagram, it can be seen that there are no gaps in obtaining all the altitude information for a preselected altitude as the beam increments discretely in elevation angle.

In the coordinate converter, the altitude is developed in the altitude accumulator from the unit altitude vector $R_o \sin \phi$. A unit high altitude vector $R_o \sin (\phi + 1/2)$ and a unit low altitude vector $R_o \sin (\phi - 1/2)$ are also developed and introduced into their respective accumulators to form the high and low altitude addresses respectively, A_H and A_L.

For small angles, the approximations

$$\sin (\phi + 1^\circ) \approx \sin \phi + \sin 1^\circ$$

and

$$\sin (\phi - 1^\circ) \approx \sin \phi - \sin 1^\circ$$

were used.

The selection criteria for a preselected altitude A_j is the following:

$$A_L \leq A_j \leq A_H \quad ; \text{ store data in } j^{th} \text{ memory}$$

For each altitude, two comparators are used and are shown in the diagram of card 2.

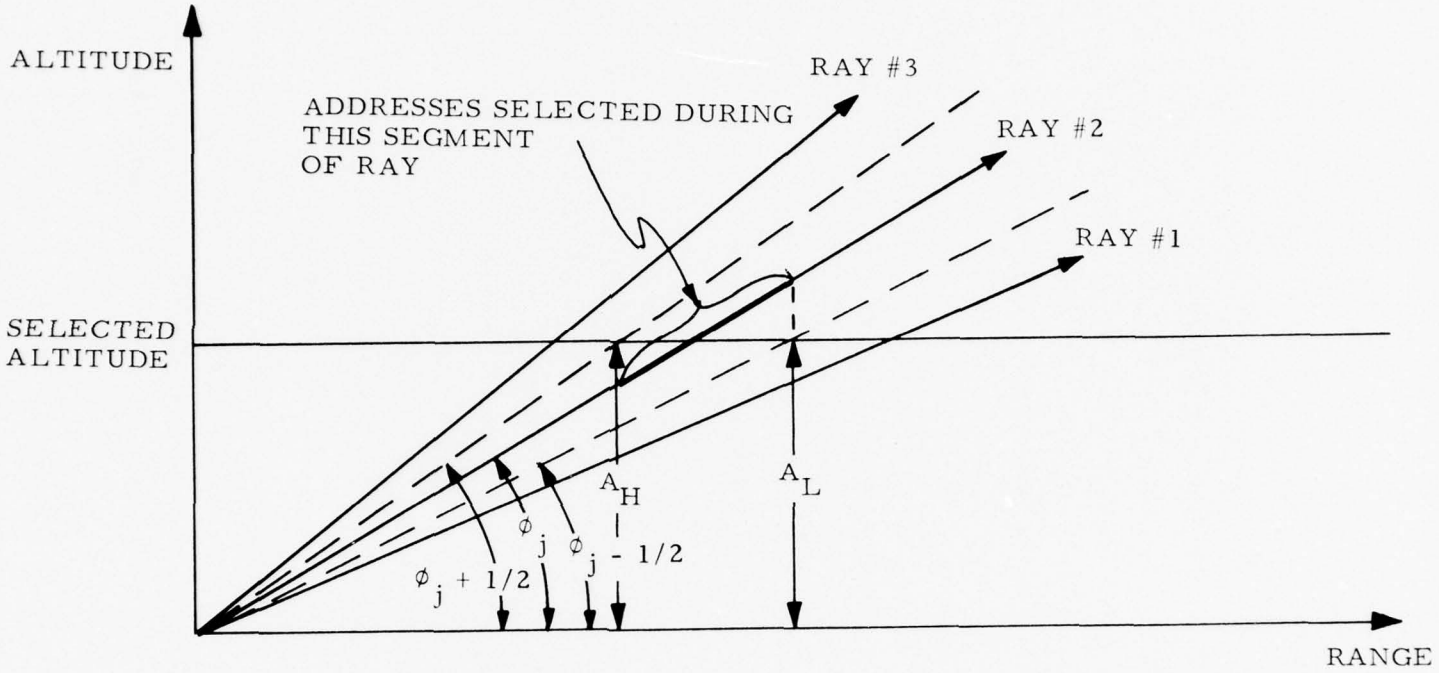


Figure 4-2. CAPPI Address Selection

4.2.7 Coordinate Converter/Integrator Interface

The Coordinate Converter is slaved to the integrator by using the radar trigger and range gate clock from the integrator. Synchronization between the Coordinate Converter and the integrator is the major reason for slaving the coordinate converter to the integrator. However, synchronization is not sufficient in order to format data rates greater than 0.6 MHz, the fastest data rate the memories can accept. For instance, it would be impossible to accept 1 μsec range gates directly from the integrator, but it is possible to receive alternate 1 μsec range gates from the integrator during one radar period and the previously non-selected 1 μsec range gates during the second radar period. This is possible because the integrator has holding loops already built into its output circuitry and, simply by selecting the starting range gate in a sequence, it is possible to store all of them.

A simple block diagram and timing waveform is shown in Figures 4-3 and 4-4. The radar trigger passes through a modulo 2 and modulo 4 counter. The output of the counter controls a multiplexer, the inputs of which are gate pulses that start on either the first, second, third or fourth pulses. These gate pulses are used to gate the range gate clock that ultimately drives the accumulators. The coordinate addresses are strobed by means of a 2 μsec clock into the synchronizer. The 2 μsec clock is also derived from the gated range-gate-clock and a modulo n counter where n depends on the range gate width.

4.2.8 Synchronizer

The Coordinate Converter and the memory unit run on independent clocking signals and the synchronizer is the means for interfacing these two asynchronous systems. The memory can accept data at a rate not to exceed 0.6 MHz, and the synchronizer will work at any input data rate provided the maximum 0.6 MHz rate is not exceeded.

The synchronizer input data consist of 8 bits each of X, Y and video information, RME, and 4-bits of memory select information(the store commands). Since these 29 bits come in parallel, operation of the synchronizer can be understood by considering a single bit. Figure 4-5 is a simplified block

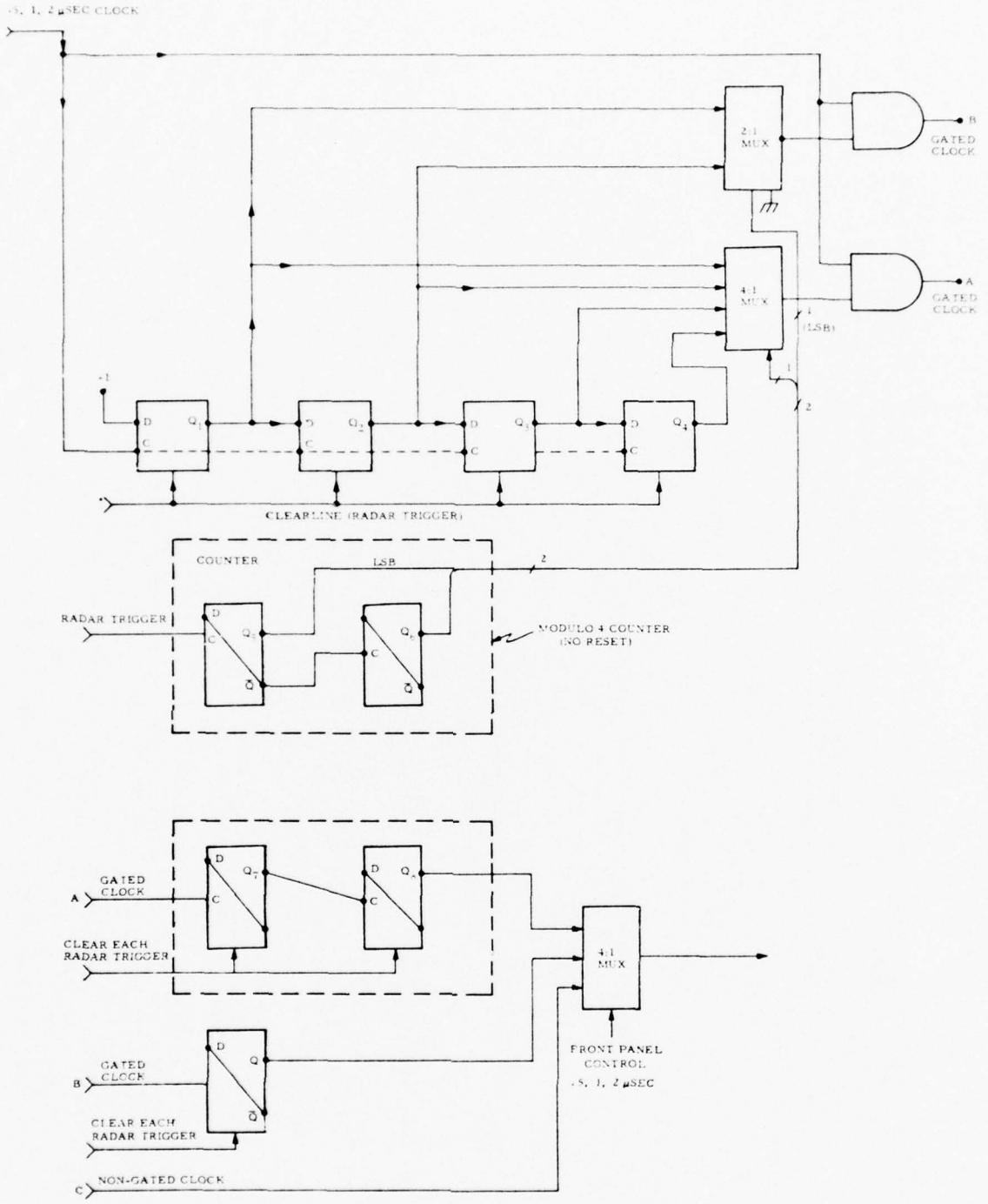


Figure 4-3. Timing Interface for Coordinate Converter and Integrator

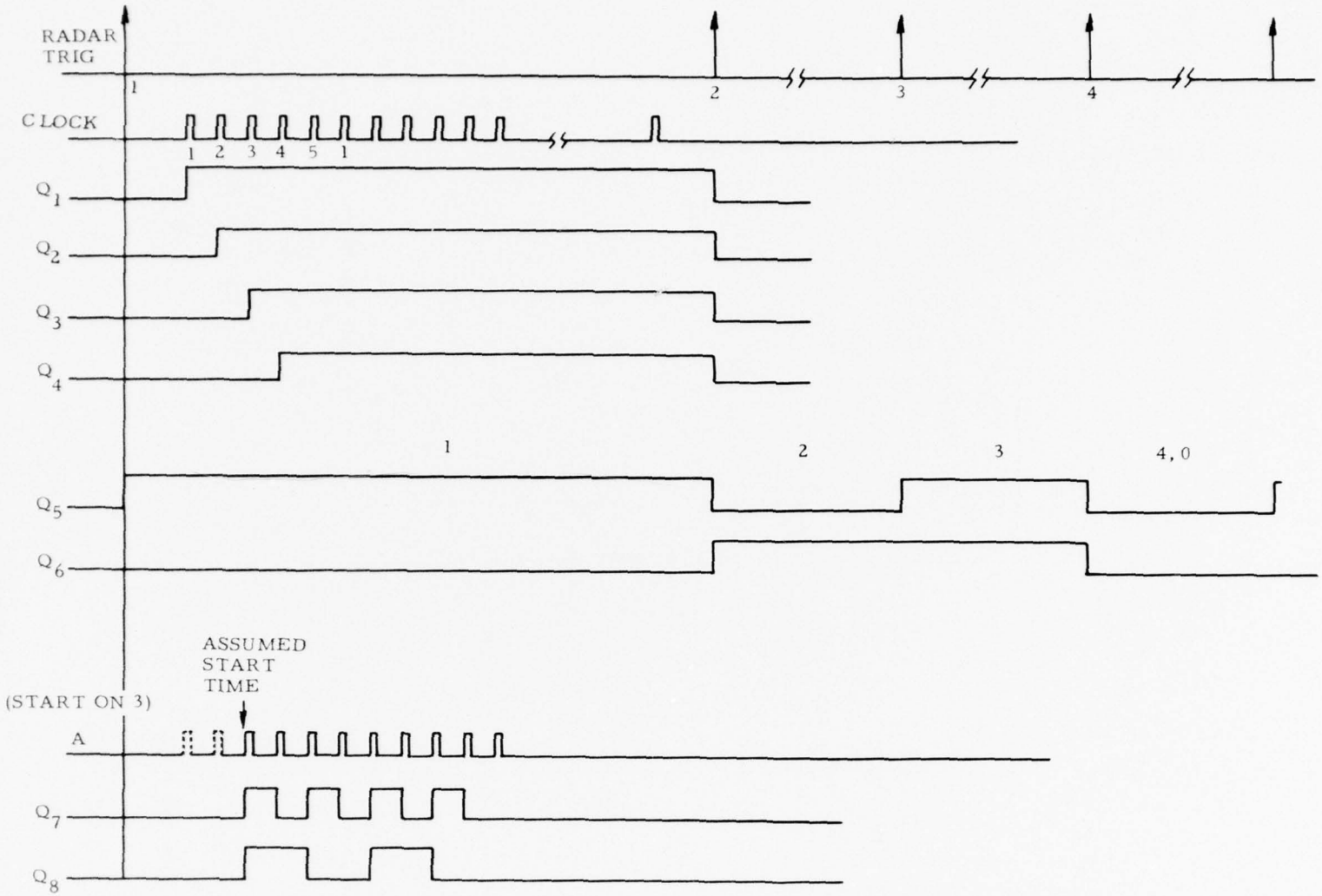


Figure 4-4. Integrator Coordinate Converter Timing Waveforms

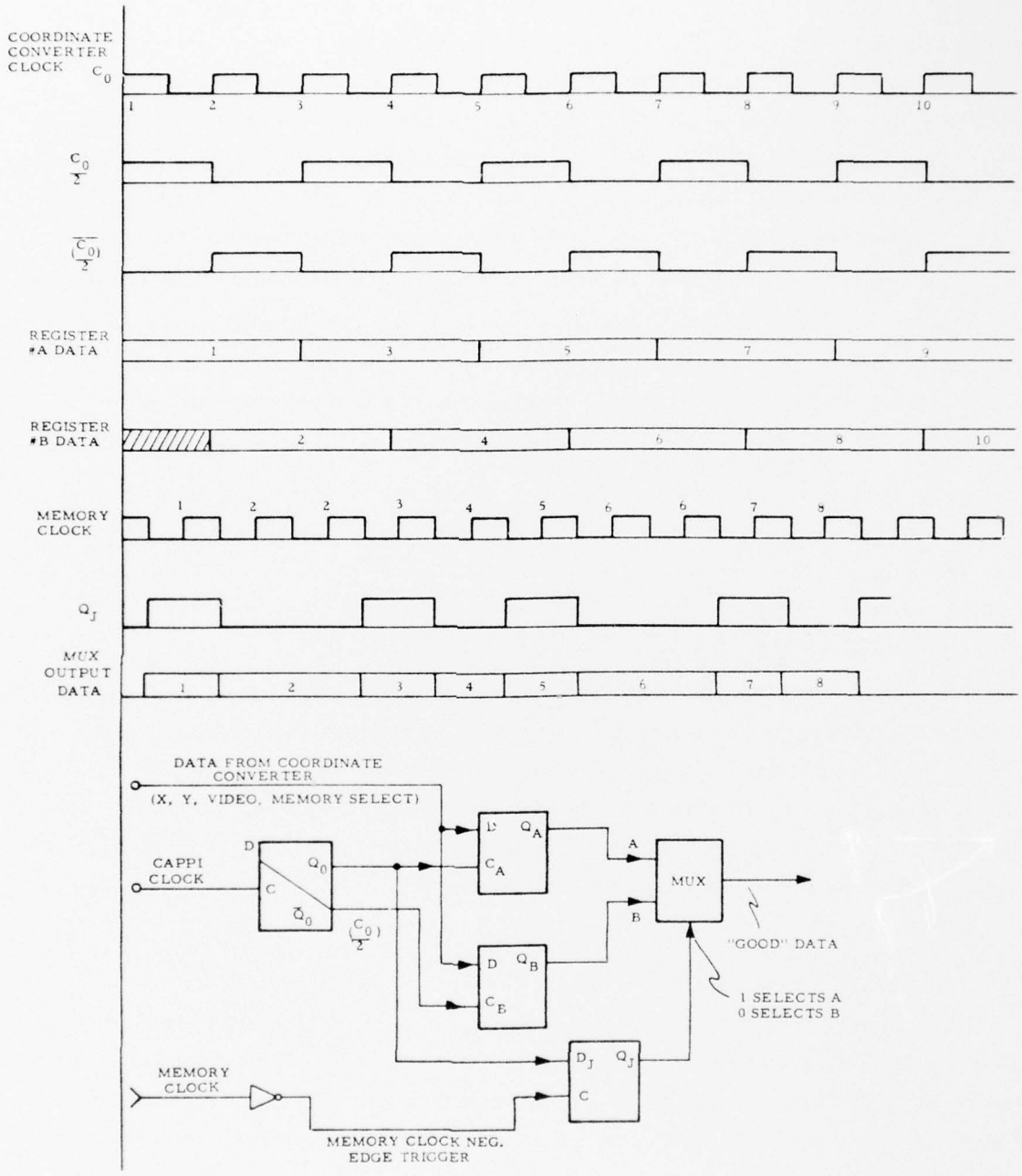


Figure 4-5. Coordinate Converter Memory Buffer Timing Waveforms

diagram of the synchronizer and the timing waveforms showing the operation of the system. Incoming data are stored in one of two D-type registers such that each DATA BIT is stored for 2 clocking cycles. The purpose of the synchronizer is to insure that the data are "good", i.e., there is no chance of a data edge or change during the time that the memory clock strobes out the data. It can be shown that at least one of the data inputs to the multiplexer will not change during the strobe time (pos. edge) of the memory clock. By strobing $(\frac{C_o}{2})$ into a D-EDGE register using the negative edge of the memory clock will provide an output signal Q_j that can control the multiplexer to select the signal that is guaranteed to be "good" by the time that the positive edge of the memory clock comes along. Notice that there can be an ambiguity in Q_j itself, i.e., assume $(\frac{C_o}{2})$ is changing at the time the negative edge of the memory clock arrives. This ambiguity, however, does not produce an ambiguity at the time the positive edge of the memory clock arrives, for regardless of which register was selected by the multiplexer, the data in either register cannot change for 2 μsec (the C_o clock period) and the data will be strobed out in .8 μsec, hence, the data will be good.

If on the other hand, we look at the situation in which the data are changing in one of the storage registers at the time of a positive going edge of the memory clock, we find that the multiplexer always selects the other register. Data can be clocked out twice as shown in the example (data #2 and #6), but will cause no problems in the system since it implies that the same data will be reentered at the same memory location, causing no change. The synchronizer is on card 3.

4.2.9 Angle Interface Timing

On card 1 is the angle interface timing which operates the control lines of the multiplexer and the control line of the sin/cos converter as well as providing an inhibit line for the S/D converters. At the start of each radar period, a gated delay line oscillator is turned on and drives a counter. The counter is decoded to derive the approximate control line code to obtain the desired function of either sin θ, cos θ, sin ϕ or cos ϕ. When this function is available, it is strobed into the appropriate D-register shown in the block diagram.

This is done only once every radar period. The input to the coordinate accumulators are those unit vectors that have been determined on the previous radar period.

4.2.10 Earth Curvature Correction

A correction term is added to the altitude address to correct for earth curvature. This correction term is a positive function that depends on the flat earth range. A ROM is used to obtain the correction factor from the range. A derivation of the correction term is shown in Figure 4-6.

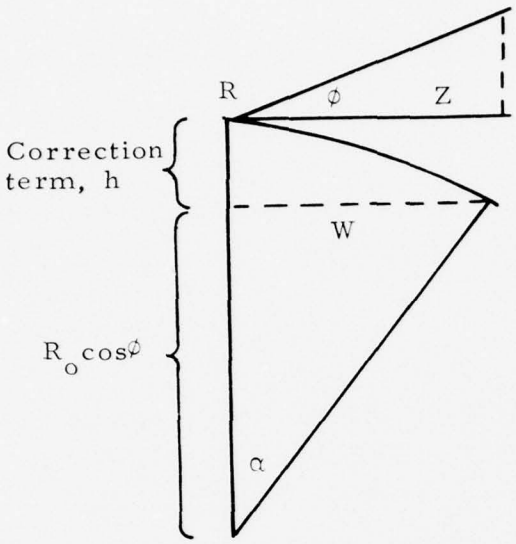
4.3 Display Control Unit

4.3.1 Timing and Control Logic

Figure 4-7 presents the DCU block diagram, where it can be seen that all timing waveforms are obtained by frequency division of the 11.958041 MHz crystal controlled clock. Discussion of the outputs of the clock generator, except for R, is postponed until the section on the MIU where these signals are used.

The square-wave R, with a period of 1.6725 microseconds, is illustrated along the X axis of Figure 4-8, which shows the display format along with waveforms. Along the X-axis, the display is organized into ten-point blocks designated DXBO through DXB31; each period of R corresponds to one block. Since each point requires four-bits for color/intensity coding, 40 bits are needed to specify each block. A memory with 40-bit words has been chosen so that one word in the memory represents each block, 32 words at consecutive addresses describe a line, and 8192 words contain the entire image.

In order to refresh the display, each memory is sequentially read while the CRT beam scans out a raster; this read cycle is always done while R is high, when the memory address multiplexer (see Figure 4-7) routes DXB and DY from the synchronous scan counters to the 13-bit memory address buss which drives all MIU's in parallel. During the remaining half cycle of R, if a store command is received from the DDI, data is written into the memory at an address IXB IYB. IYB is simply the input Y address from the DDI, IY, clocked into a register by PSL. In the code conversion ROM, IX is converted



$h = R_o - R_o \cos\alpha = R_o(1 - \cos\alpha)$
where R_o is radius of the earth.

But for small angles,

$$\cos\alpha = 1 - \frac{\alpha^2}{2} \ldots \text{ hence, } h = R_o\left(\frac{\alpha^2}{2}\right)$$

Also for small angles $\alpha \approx \frac{W}{R_o}$

$$h = R_o\left(\frac{W}{R_o}\right)^2 \quad \frac{1}{2} = \frac{W^2}{2R_o}$$

But $W = R \cos\phi$

$$h \approx \frac{(R\cos\phi)^2}{2R_o} = K(R\cos\phi)^2$$

Note: R_o = 3900 smi (6275.1 Km) used in ROM

Figure 4-6. Earth Curvature Correction Term

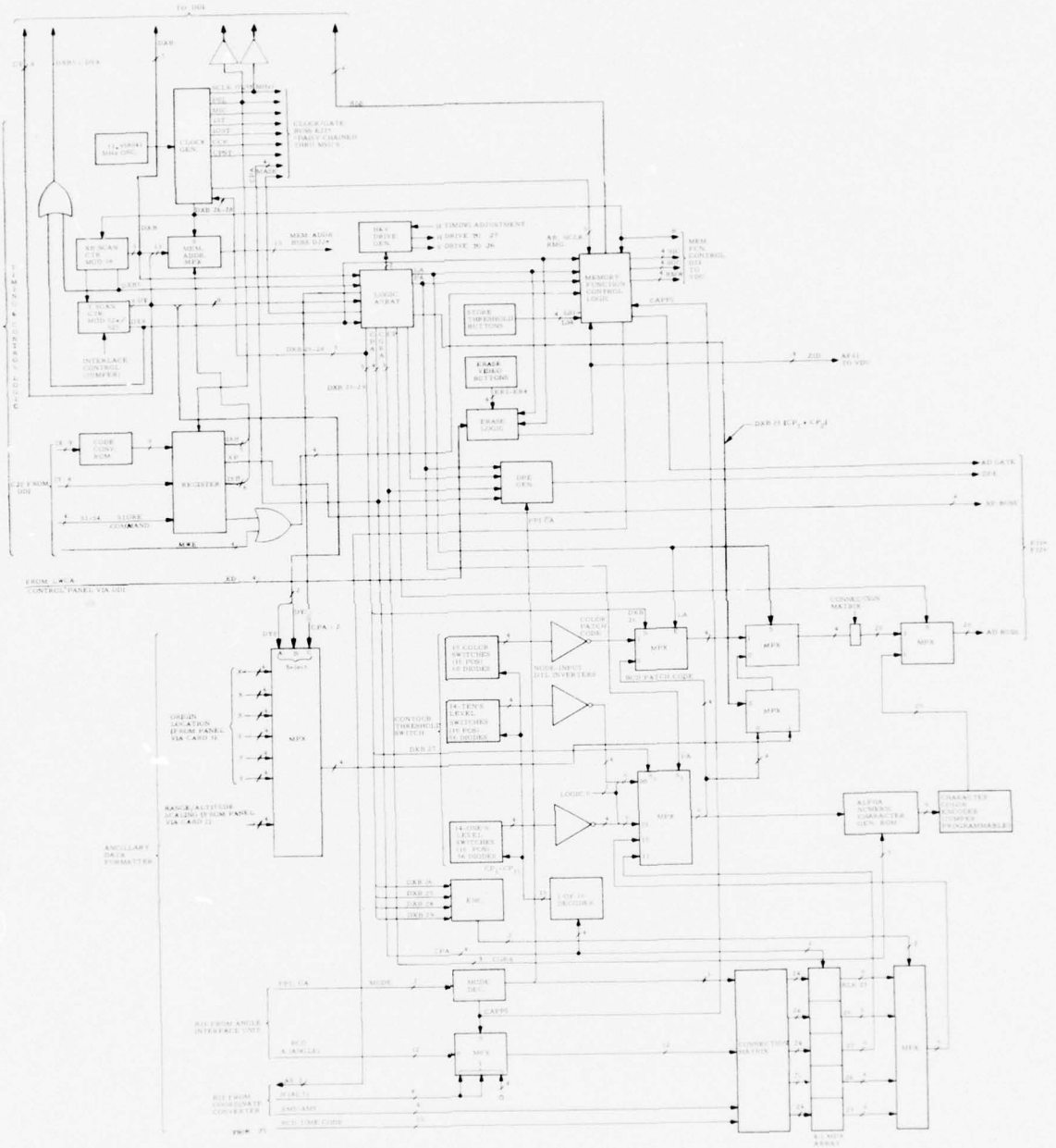


Figure 4-7. DCU Block Diagram

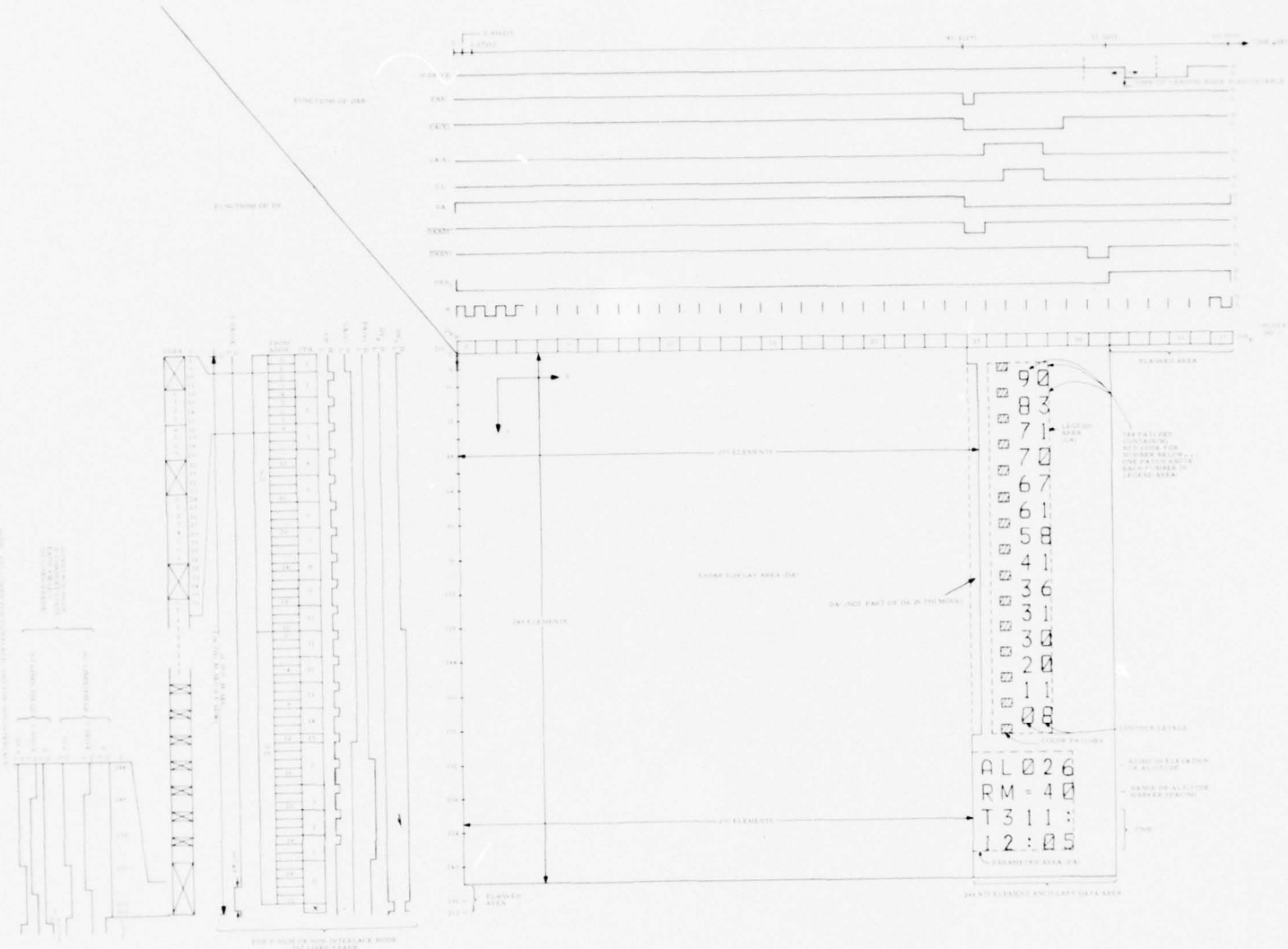


Figure 4-8. Display Format and Timing Diagram

into a code consisting of IXB (block select) and XP (point select). As is described in the MIU section, XP determines which one of the ten points within the block is to be changed.

The logic array generates waveforms, shown in Figure 4-8, which are functions of the scan counter outputs, DXB or DY. Waveforms which need to be functions of both DXB and DY are derived from them; for example: PA = PA(X) · PA(Y). The logic array is implemented with two 32 x 8 PROM (Programmable Read Only Memories) and a collection of decoders and gates. A truth table for these PROM, C16 and D20, is tabulated in the appendix, while the addressing and output waveforms are illustrated in Figure 4-8.

Interlaced scanning, possibly useful to fill interline gaps for photographic purposes, can be enabled by removing the jumper-carrier which grounds C27-9. The waveforms which result are shown in Figure 4-8. Timing of the H-drive pulse is adjustable over a range of ± 3 microseconds by means of the potentiometer in F28. This adjustment can be used to center the image in the raster of the display.

The memory function control logic generates SIC, SOC and RMW signals (to be discussed in the MIU section) which initiate various types of cycles in the memory. The AD GATE enables entry of ancillary data (contour thresholds, color patches and parameters) into the MIU. The memory function control logic also contains a four-state counter which advances once per field. The outputs of this counter, AS, select one of the four CAPPI ALTITUDES from the front panel switches for entry into the parameter area of the corresponding display.

The erase logic generates properly timed ZID signals which cause all zeroes (black) to be written into the memory at all addresses in response to an ED signal from the LWCA control panel, or at all but the legend-area addresses in response to an ER signal. The decimal point required in the elevation angle is located in point two, whereas all other ancillary data falls into points five through nine; hence, it requires a separate signal developed by the DPE generator. The RLS signals, needed by the DDI, are simply the outputs of the STORE THRESHOLDS buttons clocked by DY8 (once per field).

4.3.2 Ancillary Data Formatter

In order to minimize wiring complexity of the array of contour threshold switches, encoding diodes are mounted on the switches themselves as indicated

in Figure 4-7. One switch at a time is selected by CPI through CPI5 (CPA decoded, see Figure 4-8) as the display raster is scanned. The color switch outputs are applied to the AD BUSS (a 20-bit buss through which ancillary data can enter points five through nine of any block in memory) when the CRT scan is located in the color patch areas. Similarly stored above each number in the legend and parameter areas is a patch containing a BCD code for that number. The contour generator to be described in the MIU section makes use of these codes which are not visible on the display because a MASK waveform is applied to the MIU. The numbers themselves are generated in a row-select five-by-seven alphanumeric character generator ROM which outputs five bits in parallel to a character color encoder. This encoder generates a jumper-programmable four-bit code, now set up as green (0111) or black (0000) for each of the five points.

The ancillary data (angle, altitude, marker spacing and time) are entered into the character generator at the proper time by an array of multiplexers. The mode lines, from the front panel mode switch via the angle interface unit, drive a mode decoder which controls the multiplexers and applies the proper alphanumeric identifiers; AZ, EL, AL, M, RM, or T which are hard wired. Origin location and range/altitude scaling information is stored only in two unique color patches (See Appendix, AJJ-21, Figure 3) and not as alpha-numerics.

Signals appearing on the AD BUSS or on DPE are not displayed directly, even though they are synchronous with the raster scan format. Rather, the data are stored in the memory when appropriate store commands are issued. Only the memory contents themselves are displayed.

4.4 Video Distribution Unit

The VDU card consists simply of an array of line drivers which serves to distribute the eight-bit video signal from the coordinate converter to all of the MIU in parallel. The memory control lines SIC, SOC, RMW, RME, and ZID for each MIU are also routed through the VDU, while the memory clock, $\overline{R}$, passes through on its way to the coordinate converter (see Figure 2-1).

4.5 Memory Interface Units

The block diagram in Figure 2-1 contains four Memory Interface Units (MIU) which are identical rack-mounted drawers. Address, clock, and gate busses are supplied to the MIU in a daisy-chain configuration where each

unit taps off of a twisted-pair cable which is resistively terminated only at the last MIU (No. 1). A block diagram of one MIU is presented in Figure 4-9; the detailed descriptions of various components within it are contained in paragraphs following a discussion of memory cycles.

4.5.1 Memory Cycles

The timing diagram in Figure 4-10 shows all significant waveforms for examples of the four types of memory cycles. Each cycle occupies one-half period of the square wave R (shown in both timing diagrams, Figure 4-8 and 4-10), and is initiated by manual or automatic commands listed in Table 4-1. The state of R determines whether the raster-scan address DXB, DY or the code-converted input address IXB, IYB appears on the memory address buss.

As listed in the table, each of the four types of cycles happens in response to commands when the raster scan address DXB, DY is in certain areas of the display.

Table 4-1. Memory Cycles

	Commands					Type of Memory Cycle When DXB, DY is in each Area of Display (see Fig. 4-8):			
R	Video Store	Legend Store	Erase	Parameter Store	Memory Address Buss	DA	LA	PA	Retrace
1	X	O	X	X	DXB, DY	RR	RR	RR	∅
1	X	1	X	X	"	RR	RW	RR	∅
1	X	X	O	X	"	RR	RR	RR	∅
1	X	X	1	X	"	RW	RR	RW	∅
1	X	X	X	O	"	RR	RR	RR	∅
1	X	X	X	1	"	RR	RR	RW	∅
O	O	X	X	X	IXB, IYB	RR	RR	RR	RR
O	1	X	X	X	IXB, IYB	RMW	RMW	RMW	RMW

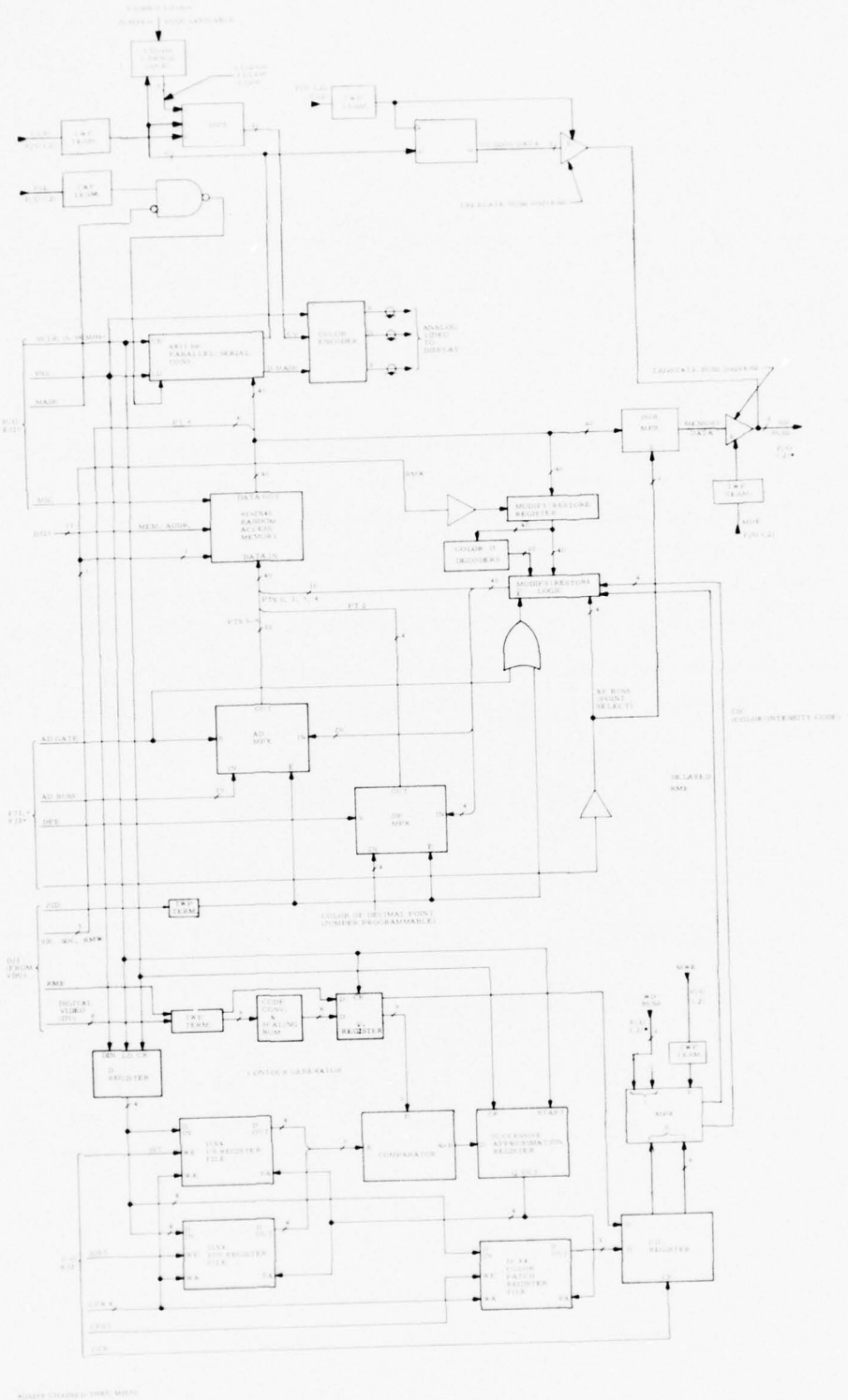
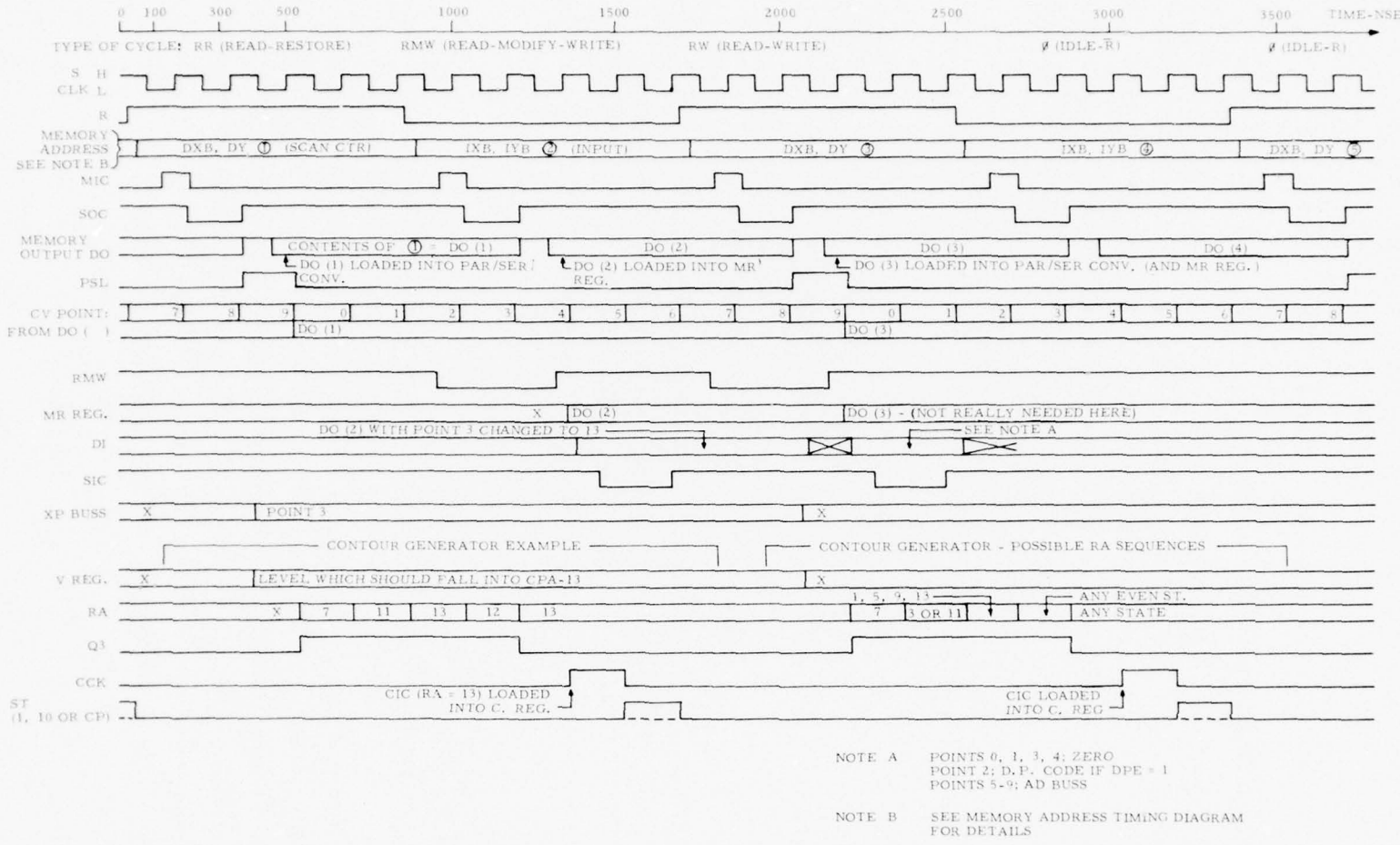


Figure 4-9. Memory Interface Block Diagram



NOTE A POINTS 0, 1, 3, 4: ZERO
POINT 2: D.P. CODE IF DPE = 1
POINTS 5-9: AD BUSS

NOTE B SEE MEMORY ADDRESS TIMING DIAGRAM FOR DETAILS

Figure 4-10. Memory Interface Timing Diagram

Table 4-1 (Cont)

Listing of Types of Memory Cycles

R	Cycle	Description
1	RR	READ-RESTORE. Data from memory address DXB, DY is transferred to the parallel/serial converter. Unchanged data is restored at the same address. This cycle is used for providing video information to refresh the raster-scan display.
1 or O	ϕ	IDLE. Do nothing.
1	RW	READ-WRITE. Data from memory address DXB, DY are transferred to the parallel/serial converter. New data, all zeroes for an erase operation or information from the AD (ancillary data) buss for legend or parameter storage, are written into the same address.
O	RMW	READ-MODIFY-WRITE. Data from memory address IXB, IYB is transferred to the modify/restore register and logic, then is partially changed and written back into the same address. This cycle is used to enter data into DA.

4.5.2 Parallel-To-Serial Converter

Parallel data from the memory are loaded into this converter at a positive edge of SCLK during PSL - see the timing diagram in Figure 4-10. The converter is wired as a four-bit-wide, ten-bit shift register having a four-bit output CV which changes at positive transitions of SCLK. The timing diagram describes which point from which memory output appears at each time interval. The D MASK output (see Figure 4-9) is simply MASK, a signal which blacks out the undesired areas of the display, delayed by three SCLK periods so that it changes only at boundaries between points zero and nine.

4.5.3 Color Encoder

The color encoder (see block diagram in Figure 4-11) accepts the four-bit output of the parallel-to-serial converter, and if DMASK is false, outputs three analog voltages to drive the red, green and blue video inputs on the color monitor. The three identical D/A converters only have three bits each, but nevertheless it is possible to generate 512 different color/intensity outputs. Voltages at each output take on eight different levels ranging from zero (black) to one volt (full intensity); the output loading must be 75 ohms through video coaxial cable.

The color encoder is programmable; that is, for each of the sixteen possible states of the input CV, an arbitrary set of analog output voltages can be programmed by means of switches. The switches are arranged in columns by colors, as shown in Figure 4-11, where an example of one possible program is shown. Within each column are three sub-columns which correspond to the bit weight 1, 2 or 4; finally, each switch in each sub-column in numbered from 0 to 15 to denote CPA (Color Patch Address-see Figure 4-8). In the example, the relative video values listed are obtained by simply adding the bit weights for each color at each CPA.

4.5.4 Modify/Restore Logic, Register and Multiplexers

The RMW memory cycle is fundamental in that it provides the means by which new data are entered into the display area. During the time when R is False and IXB, IYB is on the memory address buss, if a store video command occurs, the following sequence of events takes place (refer to Figure 4-9). The 40-bit memory output DO is loaded into the modify/restore register at the positive edge of RMW. In the modify/restore logic, one point (four-bits) as selected by the XP buss, is changed to whatever CIC (Color-Intensity Code) happens to be. The other nine points are unchanged.

If DELAYED RME is true, the selected point is written back as 1111, the code reserved for range markers. If a point is found to contain code 1111 by the COLOR 15 DECODERS, it is written back as 1111. Since these events happen when R is False, the AD and DP multiplexers are switched so that all 40 bits from the modify/restore logic go right back into the memory where they are written, still at the same address, when SIC comes along.

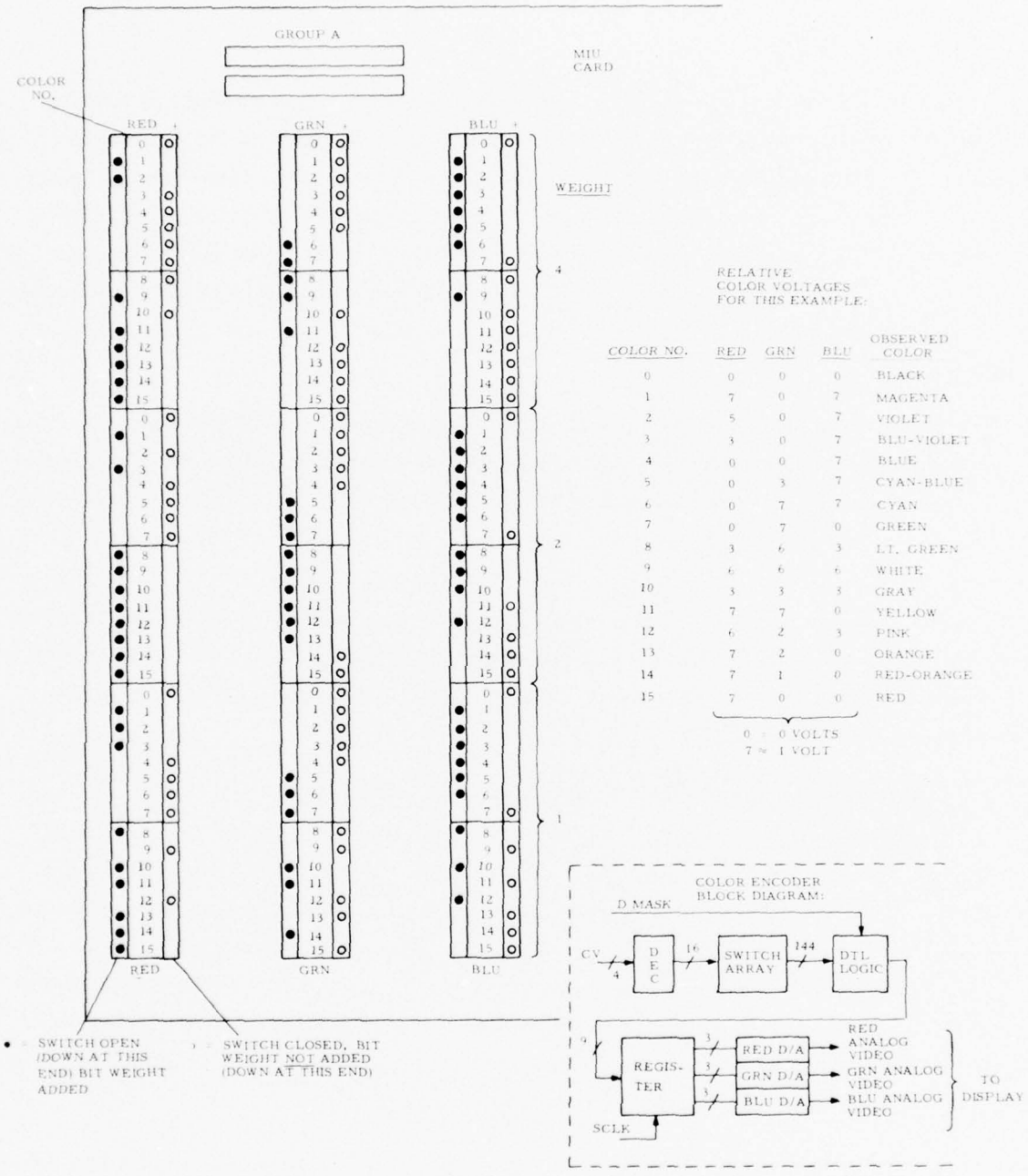


Figure 4-11. Color Encoder Switches and Block Diagram

As is evident from Table 4-1, the intervals when R is False have been reserved for RMW cycles, no matter where the raster scan counters happen to be. Thus, a new input data point can be accepted once every period of R (1.6725 μsec). During the same period, ten adjacent points are output to the color encoder. This ten-to-one difference in data rates results from the memory organization employed and the fact that the input addresses are in random order, while the output addresses are in sequential order.

When ancillary data or zeroes for erase are being written into the memory in RW cycles, points two and five through nine can be changed simultaneously by means of the DP and AD multiplexers. Ancillary data enters through the 20-bit AD multiplexer when AD GATE is true, while DPE causes a 4-bit jumper-programmable code for the color of the decimal point to be applied to point two. ZID zeroes all 40 bits during erase.

4.5.5 Contour Generator

The lower half of Figure 4-9 is the contour generator which accepts one 8-bit video word and RME every period of R and presents a corresponding four-bit CIC (color/intensity code) and delayed RME as its output. Contour thresholds, both colors and levels, are read from the memory when the raster scan is in the appropriate patch (see Figure 4-8) and are stored in register files -- small, fast memories capable of simultaneous reading and writing at different addresses. Data from the register files is used in a successive approximation algorithm to determine which CIC to assign to a given video input.

The incoming digital video is both scaled and converted to BCD in a ROM made up of two 256 x 4 PROM, D9 and D10 for which truth tables are included in the appendix. The ROM output is clocked by PSL into the V register where it remains available to drive the comparator during the remainder of the period of R. The example at the bottom of Figure 4-10 shows a digital video input which has a value such that it should be assigned the color which has been entered into CPA 13. The successive approximation register state RA always begins as seven whereupon the contents of the 1's and 10's register files at read address RA = 7 are compared with V. The decision made in the comparator determines that the next state for RA should be 11 (the other alternative is three), and the process continues to repeat in this manner until four decisions, corresponding to 16 bits, have been made. The final answer of RA = 13 then addresses

the Color Patch Register File which provides a four-bit code to be loaded into the CIC register by CCK. The second contour generator cycle at the lower right of Figure 4-10 shows all possible states of RA for each step.

The time interval after CCK is reserved for writing data into the three register files, as commanded by the three write strobe signals 1 ST, 10 ST and CPST. The write address applied to the register files is CPA, and the appropriate write strobe signal is gated-on when the raster scan is in the proper patch. Although each patch contains a five-by-four array of identically coded points, only one is needed to be written into the register files. Point eight has been arbitrarily chosen and is thus loaded into the D register (Figure 4-9) at PSL so that it can be entered into the proper register file when the corresponding write strobe signal occurs. Four write strobes appear during each field for every write address of the register files.

4.5.6 Write Data and Read Data Busses

The WD and RD four-bit busses, daisy-chained through the MIU as are the other busses (see Figure 2-1), permit direct access to any image point in the memory.

When the MWE control line is active, the multiplexer at the bottom of Figure 4-9 connects the WD buss directly to the CIC inputs of the Modify/Restore Logic. The Range Marker Enable signal is simultaneously rendered inoperative.

When the MDE control line is active, a tri-state driver shown in Figure 4-9 drives the RD buss with a four-bit code corresponding to one of the ten points currently available at the memory output. The DDR multiplexer selects this point as a function of the state of the XP Buss. The RD buss differs from all others in that signals flow away from the MIU; more than one MDE or CDE control line cannot be active simultaneously lest the buss drivers perish.

4.5.7 Cursor Interface

When the CUB (Cursor UnBlank) control signal is active, a cursor color code is applied to the CV inputs of the color encoder instead of the parallel/serial converter output. The color change logic ensures visibility of the cursor by defining its code as zero (black) except when the point being covered by the cursor (hence the background) is any of colors zero through three. In the latter case, the cursor appears as the jumper-programmed color, presently wired as color seven (light green).

The leading edge of the CDE (Cursor Data Enable) control signal enters the current four-bit word at the parallel/serial converter output into the cursor data register. As long as CDE remains active, this word appears on the RD buss. Individual MIUs are protected against simultaneous occurrence of MDE and CDE; CDE has priority.

4.5.8 Full-Screen Operation

When the FSE (Full-Screen Enable) control line is active, the MASK which normally blanks certain areas among the ancillary data is inhibited. This condition permits use of the full screen for display of data written through the WD buss.

4.6 Display Data Interface and LWCA Control Panel

The Display Data Interface (DDI) includes a multitude of interfaces necessary so that the LWCA control panel, the Scan Converter (DCU and MIU), and the computer's Universal Logic Interface (ULI) can collectively communicate. These interfaces include A/D conversion of the trackball outputs, code-conversion, generation of precisely-timed control signals, temporary storage of data, routing of data, synchronization, and sequential control of data transfer operations. Reference to the DDI Block Diagram in Figure 4-12, unless otherwise specified, is implied in the following sections.

4.6.1 Cursor Position

Digital binary-coded representation of cursor position (XC,YC) is derived from a mechanical trackball device* on the LWCA control panel.

*See Appendix for Data Sheet.

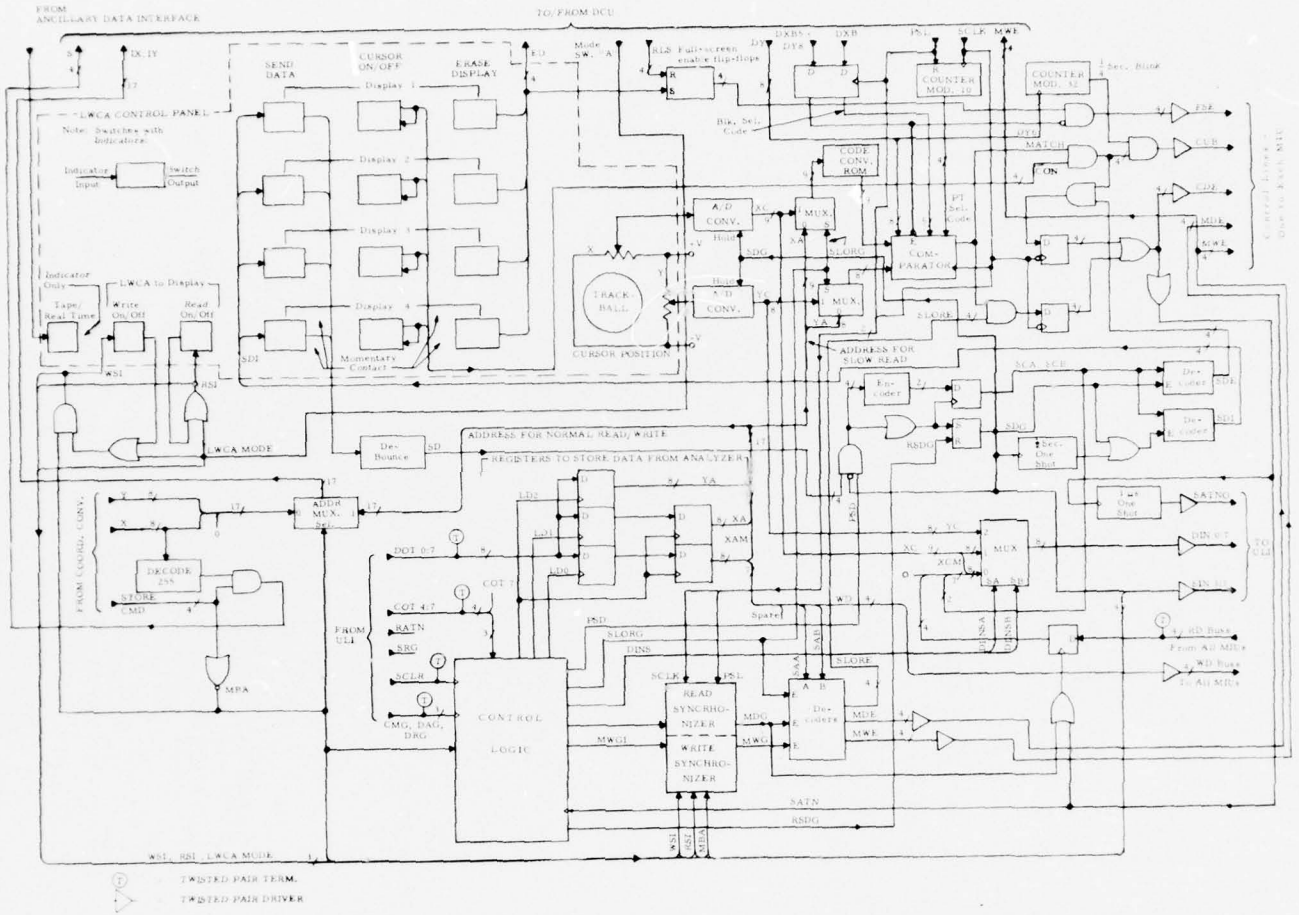


Figure 4-12. LWCA Control Panel and Display Data Interface (DDI) Block Diagram

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Bipolar voltages, obtained by zener regulation from the 15-volt supplies, are applied across the 10K trackball potentiometers. The resultant bipolar analog signals--one proportional to X-axis (left-right) displacement, the other to Y-axis displacement--are low-pass filtered and converted to binary-coded digital form in Datel ADC MA-10B modules*.

The converter modules are set up so that an input voltage of -10 volts gives an all zeroes output, while +9.9951 volts yields all ones. Outside of this range, the converters limit. The Y-channel analog voltage range is $\pm$12 volts (the last two volts at either end is not used) and the most significant eight bits of the converter output are clocked into a register to become YC.

The X-channel analog voltage range has been limited by a series resistor to -12 to +3.4 volts, while the most significant nine bits of its converter output are clocked into a register to become XC. Although the X analog voltage is limited, it is possible to exceed XC = 319, which is beyond the right edge of the screen. This condition is discussed from an operational standpoint in AJJ-21, see appendix.

In order to remain compatible with Interdata notation, YC and the least-significant eight bits of XC are numbered with the most significant bit having the least subscript--just opposite to all other scan-converter documentation. The MSB of X is handled separately as XCM; for an illustration of display addressing convention, see Figure 2 of AJJ-21 in the Appendix.

The self-clocked, successive-approximation A/D converters begin a conversion once per raster-scan field, at the trailing edge of DY7. Conversion is inhibited when SDG, the send-data gate to be discussed later, is true. This feature prevents (XC, YC) from changing during a data transaction.

*See Appendix for Data Sheet.

4.6.2 Cursor Generation

The cursor, a moveable single point on the screen, is made to appear by the generation of a narrow pulse properly timed with respect to the raster scan. This pulse is applied to the CUB input (described in section 4.5.7) of each MIU having its CURSOR ON/OFF switch in the on (illuminated) state.

Except for the Slow-Read case to be described later, XC and YC pass through the digital multiplexers shown. The code conversion ROM (the same as that in the DCU) develops the special code used in the DCU for generating X addresses, so that a digital comparison can be made directly. The raster scan location is defined to the nearest 10-point block by DY and DXB from the DCU. The state of the mod-10 counter driven by SCLK and reset by PSL defines the location of a point within that block. When the scan location equals the cursor location, the comparator MATCH output becomes true and the logic shown generates a CUB (cursor unblank) for those displays having their cursor switched on. The cursor is made to blink with a 0.5 second period in order to make it easy to find and to see what color it covers. The blinking can be disabled by closing switch 1 on C26 of the DDI. The comparator is disabled when the DXB5 + DY8 signal, corresponding to the vertical and horizontal blanking intervals, is true.

4.6.3 Full-Screen Enable

The flip-flops which are set by the ERASE DISPLAY buttons and reset by signals RLS (from the DCU and the STORE THRESHOLD buttons), simply generate the FSE (full-screen enable) signals. When FSE is true for a given display, the mask which normally surrounds the color patches and alphanumerics is disabled so that the full screen can be used. FSE is inhibited during retrace time intervals.

4.6.4 Address Multiplexer

The multiplexer at the center-left of the DDI block diagram selects whether the DCU inputs are to be driven from the coordinate converter outputs as they normally are, or from the analyzer. It selects the X and Y scan converter outputs for application to the DCU address inputs IX, IY

when any store command is active (MBA = LOGIC ZERO). In this case, the ninth (most significant) X bit is forced to zero and store commands are disabled for X = 255 since radar data must not appear in the ancillary data area which begins at X = 255 (see Figure 4-8). When all store commands are inactive, MBA is true and the DCU address inputs are driven by the outputs of temporary data storage registers YA, XA and XAM.

4.6.5 LWCA-DISPLAY Controls

The logic shown connected to the READ ON/OFF and WRITE ON/OFF switches and indicators is described functionally by Table 1 of AJJ-21 in the Appendix. The WSI and RSI logic signals which drive the indicators also control operation of the synchronizers and appear as status bits at the ULI inputs.

4.6.6 Computer Interface

The Interdata M48-013 Universal Logic Interface, described in their publication number 29-311, is a circuit card located within the computer itself. Line drivers and receivers for the signals indicated as "from ULI" and "to ULI" in the DDI block diagram have been built onto the ULI. The signals reach the DDI through a multiple twisted-pair cable having connectors at the computer's convenience panel.

The ULI is always operated in its Byte Mode. Data arriving at the DDI from the ULI on DOT 0:7 are loaded into one of three registers, according to load commands LD0, LD1 and LD2 from the control logic. Three of the user defineable command bits COT 4:6 and most of the control lines are used to drive the control logic, causing it to change state (as the computer executes I/O instructions with device number X'8B') according to the diagram in Figure 4 of AJJ-21 in the Appendix. The control logic is implemented as a four-bit sequential machine with two field-programmable 32 x 8 ROMs (see Appendix for data patterns) in its feed-back path. These ROMs have been programmed to cause the control logic to behave as characterized in the state diagram. A different section of one ROM can be selected to alter the behavior of the control logic for hardware tests covered in a later section.

The Read and Write synchronizers match the timing of certain control logic outputs to that of the scan converter. Control logic outputs are directed to the proper display channel by the decoders shown driven by the two-bit display select code SA received in one of the registers. Of these outputs, MDE (Memory Data Enable) and MWE (Memory Write Enable) drive the MIU circuitry directly, while the SLORE (Slow Read Enable) signals permit generation of corresponding CDE (Cursor Data Enable) control pulses following a subsequent MATCH occurrence. CDE pulses can also be generated similarly following a manually initiated send-data sequence. The incidence of any CDE results in the following actions: 1) A one-microsecond pulse is sent to the ULI on its SATNO (interrupt input) line, 2) the 4-bit word now on the RD Buss is stored in a register accessible to the ULI, and 3) the control logic state changes. Control logic, synchronizer, and CDE operation will be exemplified when specific types of data transfers are explained.

A multiplexer, driven by DINS (Data Input Select) from the control logic, selects data from various points in the DDI to be sent over DIN 0:7 to the ULI. Five of the eight status lines SIN 3:7 are used to tell the processor what it needs to know about the control logic state, the condition of the LWCA to DISPLAY indicators, whether or not the scan converter mode switch is in position A, and whether or not the memory buss is available. Examination of the status byte is entirely passive and does not affect DDI operation in any way (the SRG control line is not even connected).

4.6.7 Data Transfers

The explanations of the various types of data transfers, contained in the following sub-sections and supported by detailed timing diagrams, parallel those appearing in AJJ-21 of the appendix. Because the same examples have been used, correlation between the software-oriented information in AJJ-21 and the hardware-oriented discussions to follow should provide a thorough understanding of this interface.

4.6.7.1 Write Display Memory

The three different types of write operations are each represented in Examples 1, 2 and 3 of Figure 4-13. The leading edge of the first CMG pulse, occurring in response to execution of an OC instruction as indicated in the corresponding software example, coincides with the appearance of the code OOO on ULI outputs COT 4 through 6. The trailing edge of CMG compels the control logic to enter state RW1.

New data (not shown) appear on ULI outputs DOT 0 through 7 at the leading edge of each DAG pulse, while the control logic changes state at each trailing edge. The mutually-exclusive Load commands LD0, LD1 and LD2 occur during each DAG pulse in states RW1, RW2 and RW3, respectively. The trailing edge of each LD pulse loads the then-stable ULI data outputs into the appropriate register. The data do not all reach their final registers, however, until the last transition of LD2. The extra registers were added so that all 17 memory address bits change simultaneously; thus, avoiding possibility of anomolous behavior in certain situations.

As the control logic leaves state RW3, the Write synchronizer springs into action, driven by MWGI. If WSI is true (write indicator lit), the synchronizer generates an MWG (Memory Write Gate) pulse starting at the next positive edge of the PSL clock (from the DCU) at least 200 nanoseconds after the control logic state transition. At this time, all address bits are in their proper registers, the four-bit color/intensity code to be written is in a register driving the WD buss, and the display select code is at the decoder select inputs so it can direct the MWG pulse onto the proper MWE line. The write operation for one point is thus completed during the MWG pulse. Had WSI been false (write indicator not lit), no MWG would have been issued.

The three examples in Figure 4-13 differ only in the path taken through the control logic states, as determined by COT 4:6 (of the command byte). They each involve writing two points which could be accomplished as in example 3, but in examples 1 and 2, advantage has been taken of common information between the points or compact table organization to shorten the total execution time.

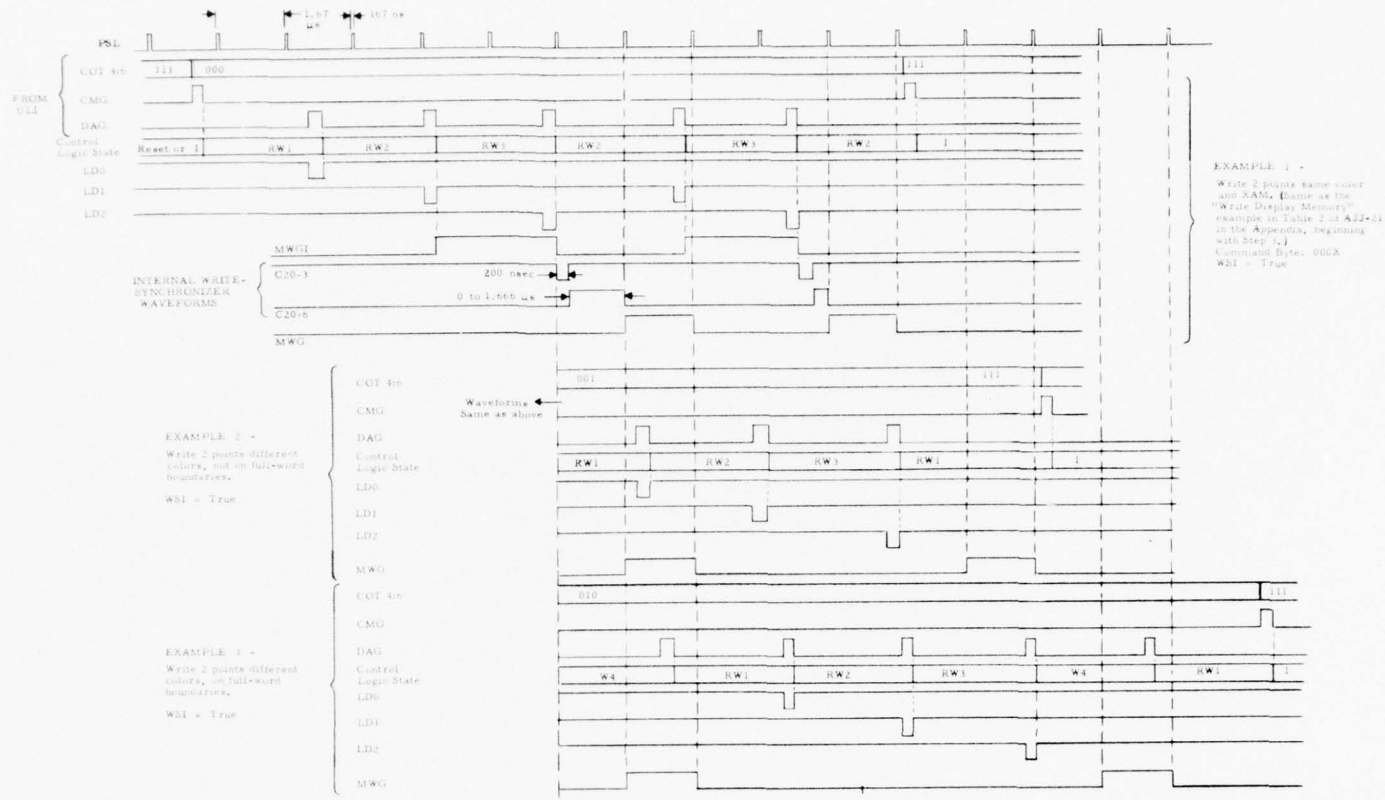


Figure 4-13. Write Timing

4.6.7.2 Read Display Memory

The write data transfer just described can be executed only if the scan converter memory buss is available. The normal read display memory operation, example 4 in Figure 4-14, also requires the memory buss. A slow read transfer, example 5 in the same figure, does not need the buss but requires an interrupt service routine in the software and may occupy a lengthy time interval.

Through state RW3, the normal read sequence is the same as a write sequence, except that a different command byte is issued. When the control logic goes from state RW3 to R4, the read synchronizer begins its work. Depending on the current phase relationship between the scan converter and the computer, the MDG pulse ends 1.34 to 3 microseconds after the state transition. At this time, the color-intensity code for the addressed point which had been on the RD buss during MDG, is clocked into a register on the DDI. Because DINS = 0, the outputs of this register reach ULI data inputs DIN 4:7. Note that on the DDI schematic, the inputs and outputs are oppositely numbered; this is another case where the Interdata bit-numbering convention conflicts with that established for the scan converter.

Because up to three microseconds can elapse before the data is ready, a delay should be programmed so that the DRG pulse from the MIU does not happen too early. This DRG pulse, the result of execution of a read instruction--see the corresponding software example--transfers the signals at the ULI data inputs to the computer and sends the control logic back to state RW1. Another point can now be read, or as in the example, a CMG pulse with command byte 010X111X issued to force the control logic into state I.

Should the memory buss not be available (MBA = false), the slow-read sequence (example 5 in Figure 4-14) must be employed to obtain data from the image memories. This sequence, through state RW3, is identical to that of a normal read. Command bit COT 6 can be left as a zero since the fact that MBA is false will force the control logic to follow the proper state sequence, or it can be set to a one in which case the slow read will be performed even if MBA is true.

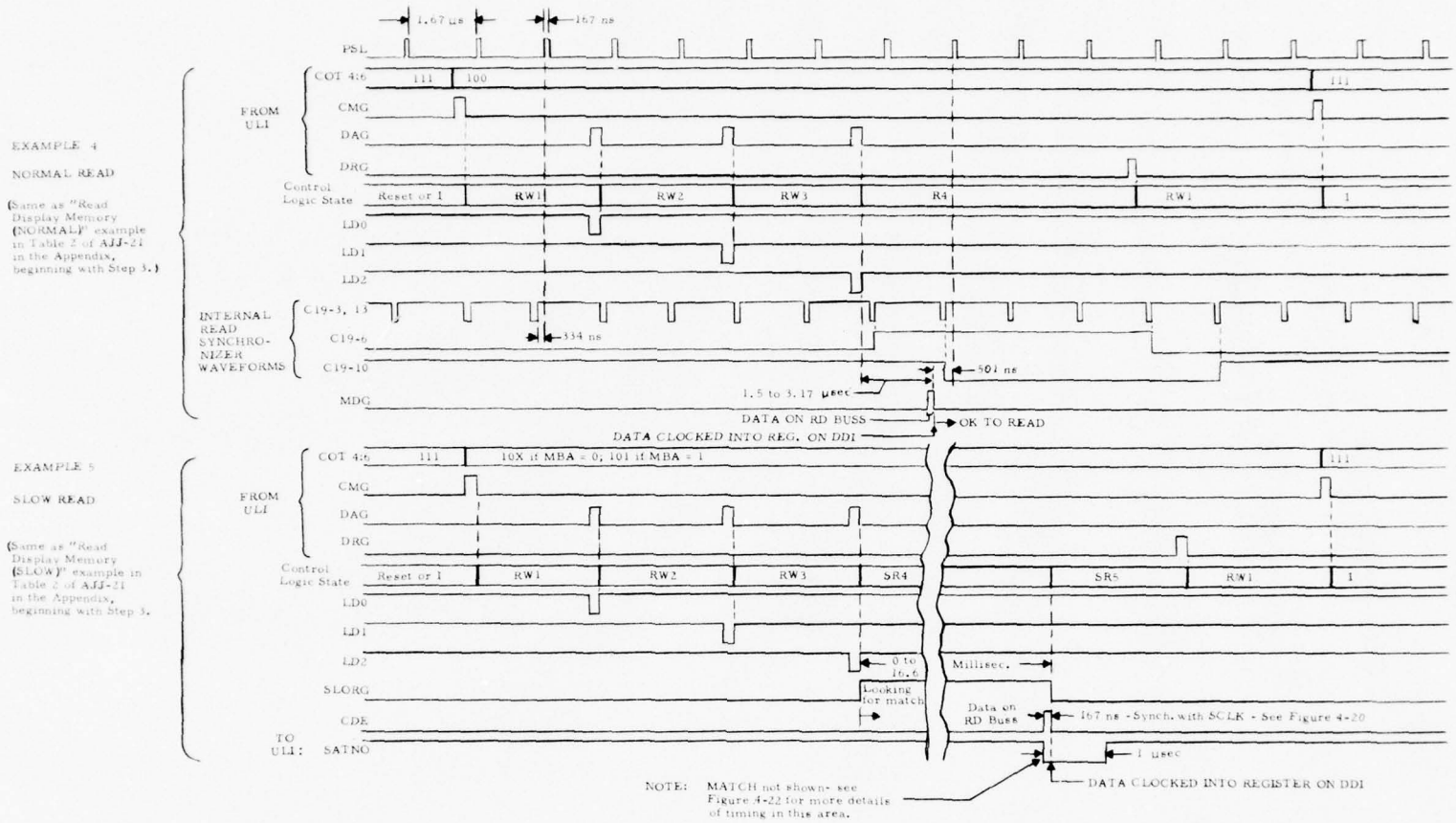


Figure 4-14. Read Timing

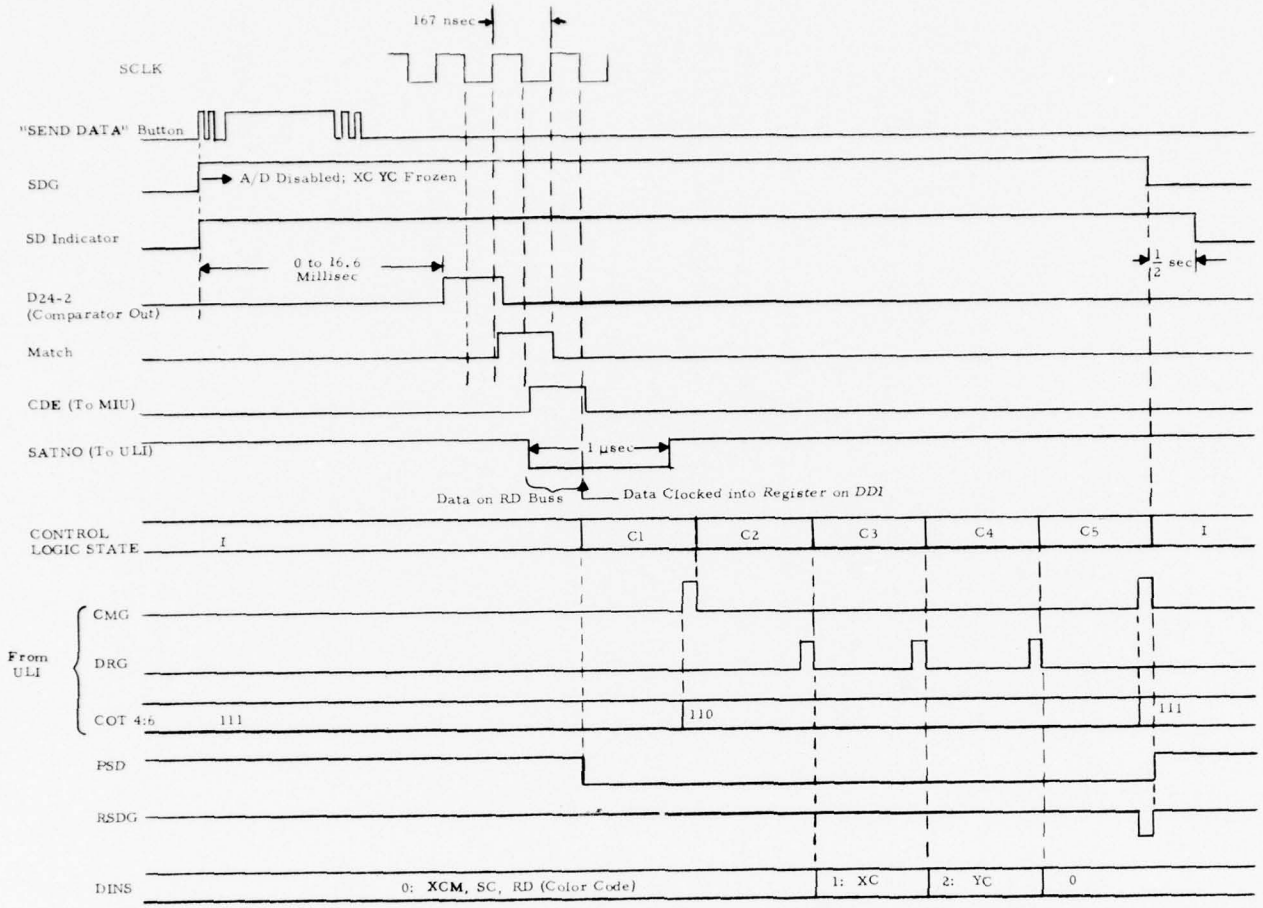
After the third DAG pulse, the control logic enters state SR4, and the SLORG (Slow Read Gate) signal goes true. While SLORG is true, the comparator inputs (XA, YA) supplant (XC, YC) from the trackball and one of the four D-flip flops, enabled by the SA-selected SLORE (Slow Read Enable) line, awaits a MATCH pulse. When this event finally happens, a CDE pulse is generated to snare the proper color/intensity code from the RD buss. Concurrently, the control logic goes to state SR5 and a one-microsecond pulse on the ULI/SATNO line awakens the computer, which shortly thereafter obtains the data by issuing a DRG pulse from the ULI as in example 4.

4.6.7.3 Cursor Data Entry

This operation is different from read and write in that it is manually initiated and all data flow toward the computer. While acquisition of the color/intensity code at the cursor position (XC, YC) employs the same lengthy wait-for-the-MATCH process as the slow read, the work is done by the DDI before the computer even becomes involved.

Figure 4-15 shows the cursor data entry example. When a SEND DATA button is pushed, SDG is set to a logic one condition, a two-bit code SC is stored in a register to describe which button was pushed, the corresponding SDE (Send Data Enable) signal is energized, and the corresponding SDI (Send Data Indicator) signal is activated to light the button. As did the SLORE in the slow-read case, the SDE enables a flip-flop to wait for a MATCH, which subsequently generates a CDE pulse to get data onto the RD buss and stuff it into the register on the DDI. At about the same time, the control logic is coerced into state C1 and a one-microsecond pulse on the ULI's SATNO input alerts the computer that the data is ready.

An interrupt service routine then executes instructions--see the software example--so that the ULI outputs shown in Figure 4-15 are generated. The control logic threads its way through states not reached in any other operation, while DINS changes to one and two for the first time in any example. The latter event gives the ULI data inputs access (through the multiplexer) to YC and the eight least significant bits of XC which are



EXAMPLE 6 - CURSOR DATA ENTRY (Same as Cursor Data Entry Example in Table 2 of AJJ-21 in the Appendix)

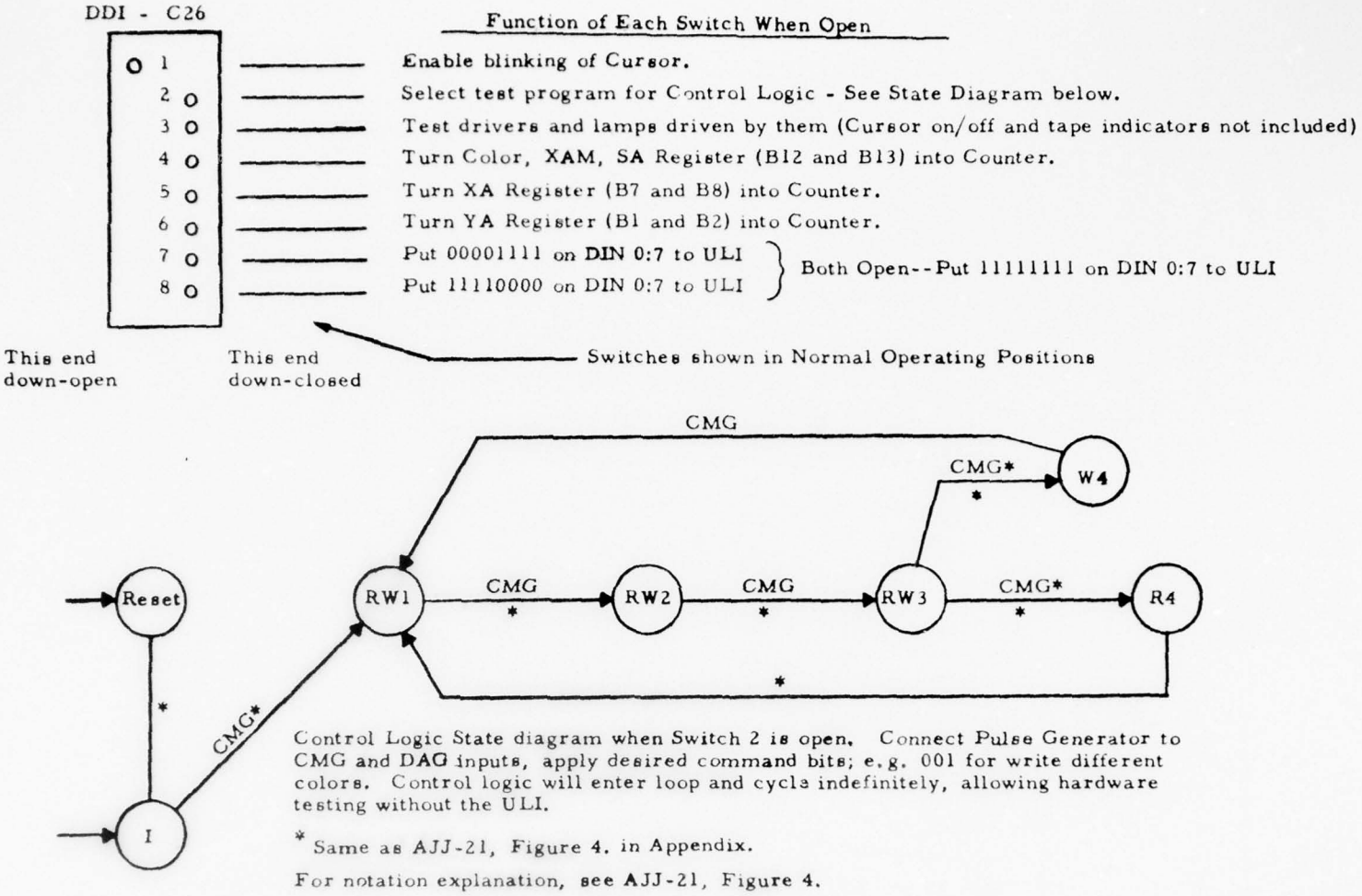
NOTE: Time scale varies along abscissa.

Figure 4-15. Cursor Data Entry Timing

not allowed to change at this time since SDG is still true. When all data have been obtained, the computer terminates the operation by producing a CMG pulse, together with a 010X111X command byte, to force the control logic back to state I while resetting SDG by means of the RSDG signal. The SD indicator persists in its state for an additional half-second so that it can be seen even when the wait for a MATCH is of short duration.

4.6.8 Hardware Test Switch

Located in C26 of the DDI card, this eight-circuit switch permits certain tests to be performed on the DDI without the ULI. The switch and its capabilities are illustrated in Figure 4-16.



Control Logic State diagram when Switch 2 is open. Connect Pulse Generator to CMG and DAG inputs, apply desired command bits; e.g. 001 for write different colors. Control logic will enter loop and cycle indefinitely, allowing hardware testing without the ULI.

* Same as AJJ-21, Figure 4. in Appendix.

For notation explanation, see AJJ-21, Figure 4.

Figure 4-16. Hardware Test Switch

APPENDIX A

Scan Converter Photographs

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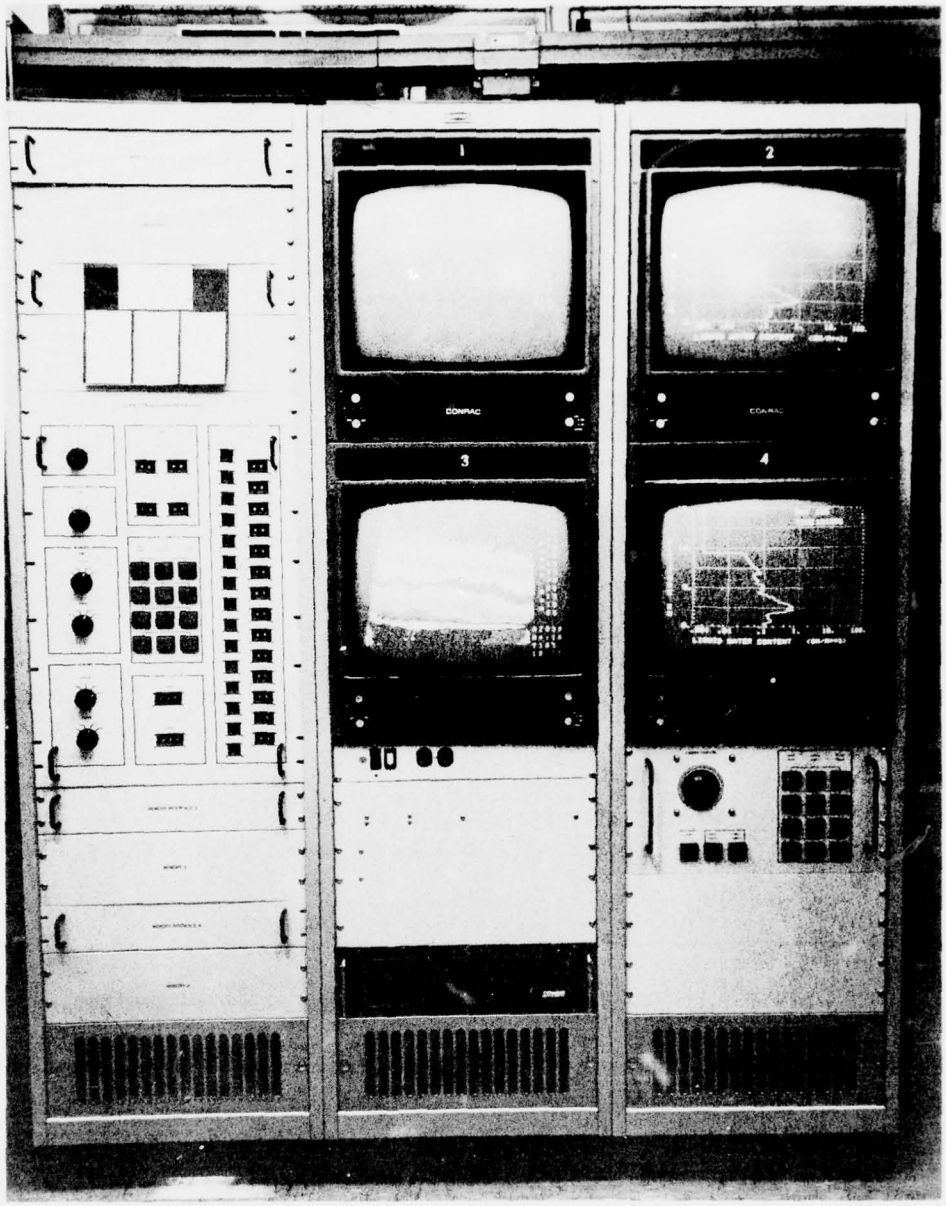

Figure A-1. Scan Converter - Front View

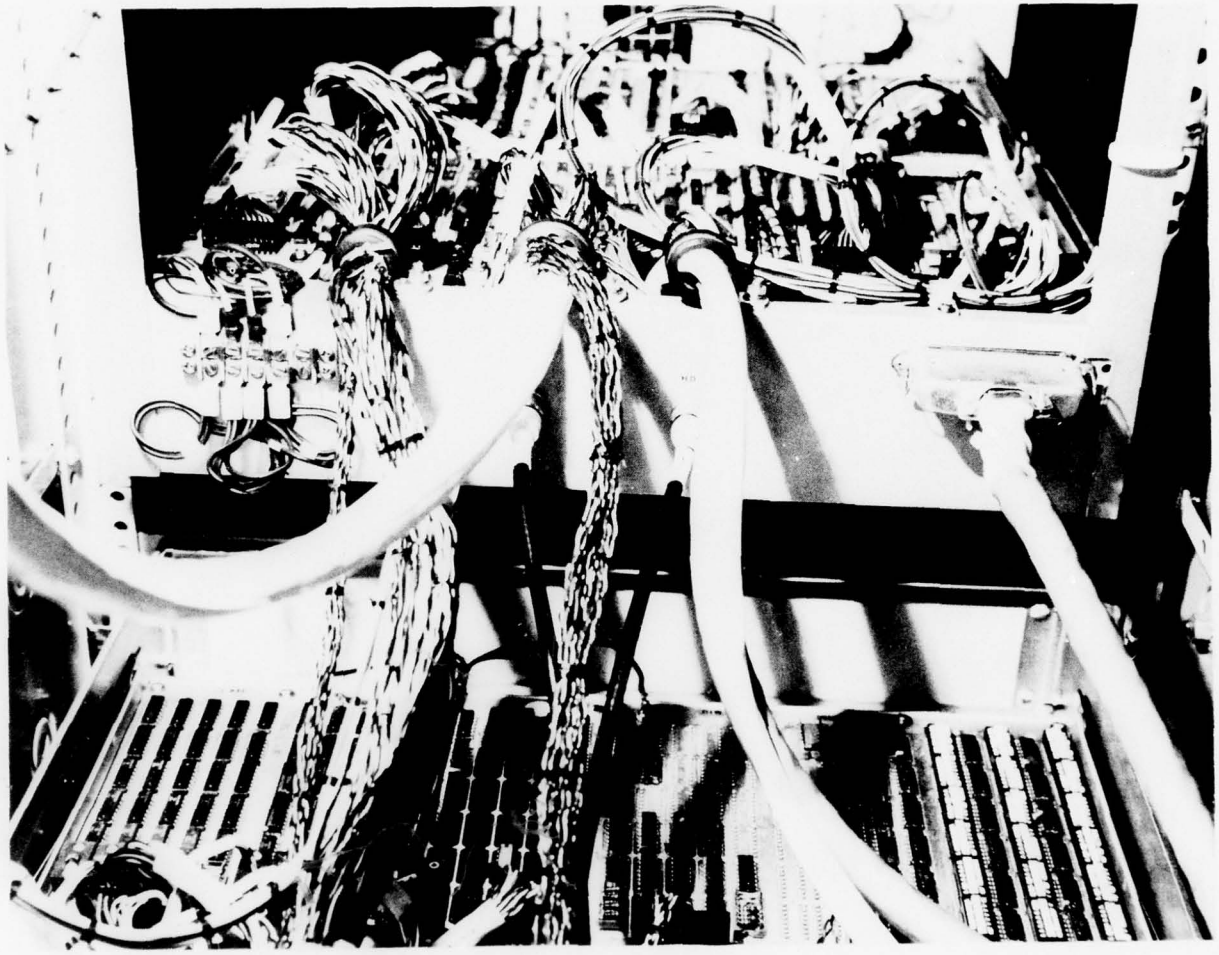

Figure A-2. Scan Conversion Processor - Rear View (Bottom)

Figure A-3. Scan Conversion Processor - Rear View (Top)

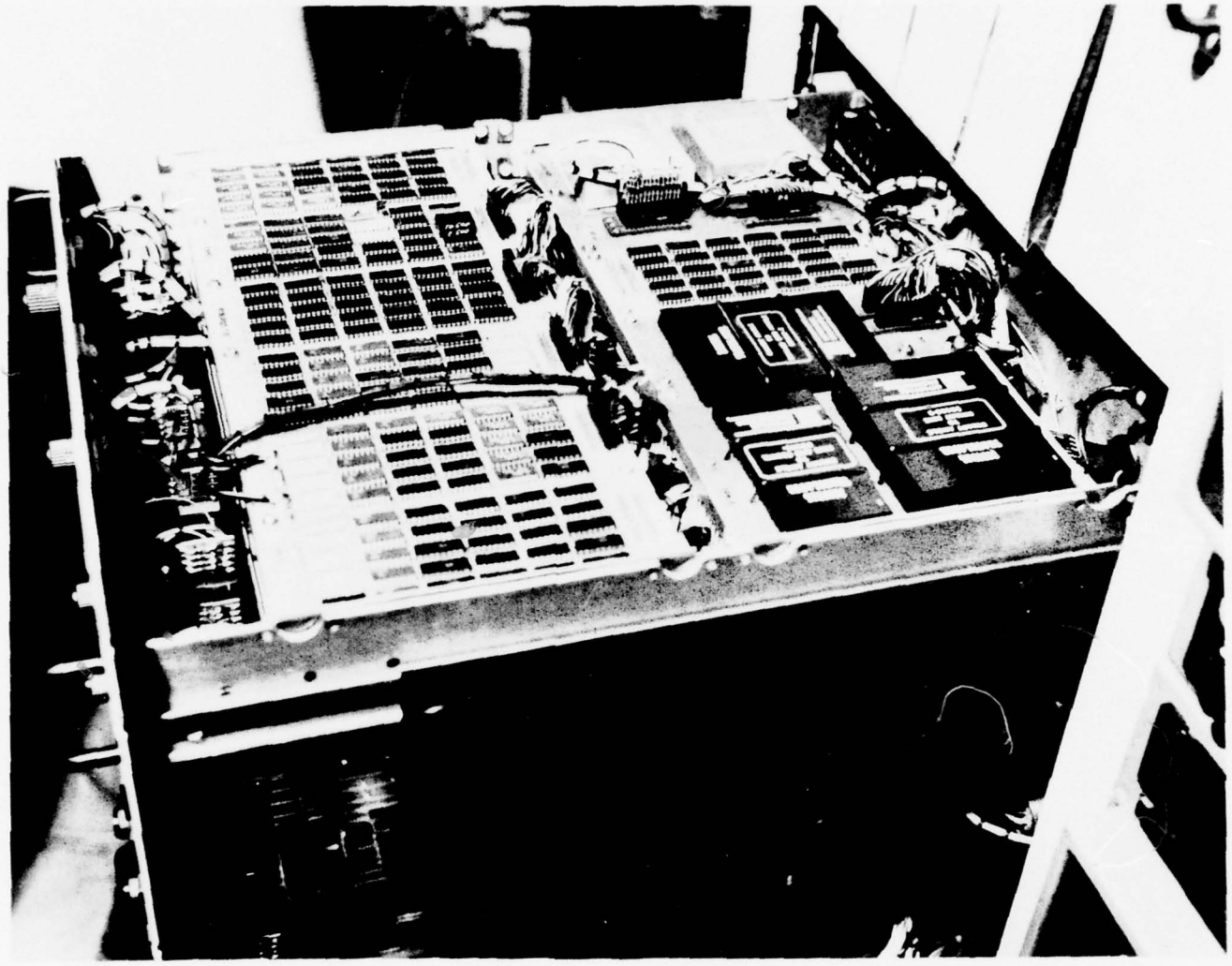

Figure A-4. Scan Conversion Processor - Top View Showing Angle Interface Unit and Card 1 of the Coordinate Converter

Figure A-5. Scan Conversion Processor - Bottom View of Top Drawer Frame Showing Coordinate Converter Cards 2 and 3

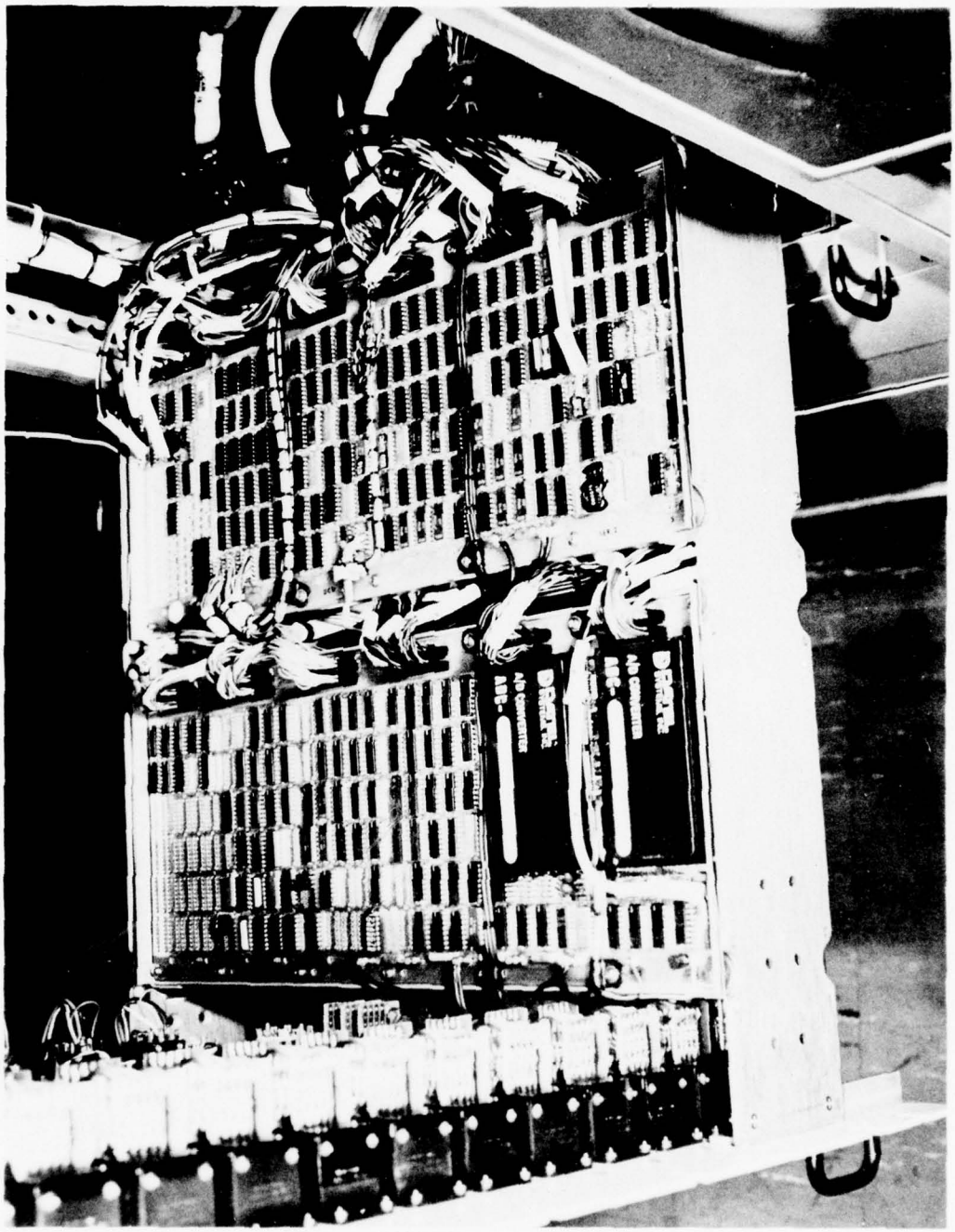

Figure A-6. Scan Conversion Processor - Top View of Bottom Drawer Frame Showing DCU and DDI

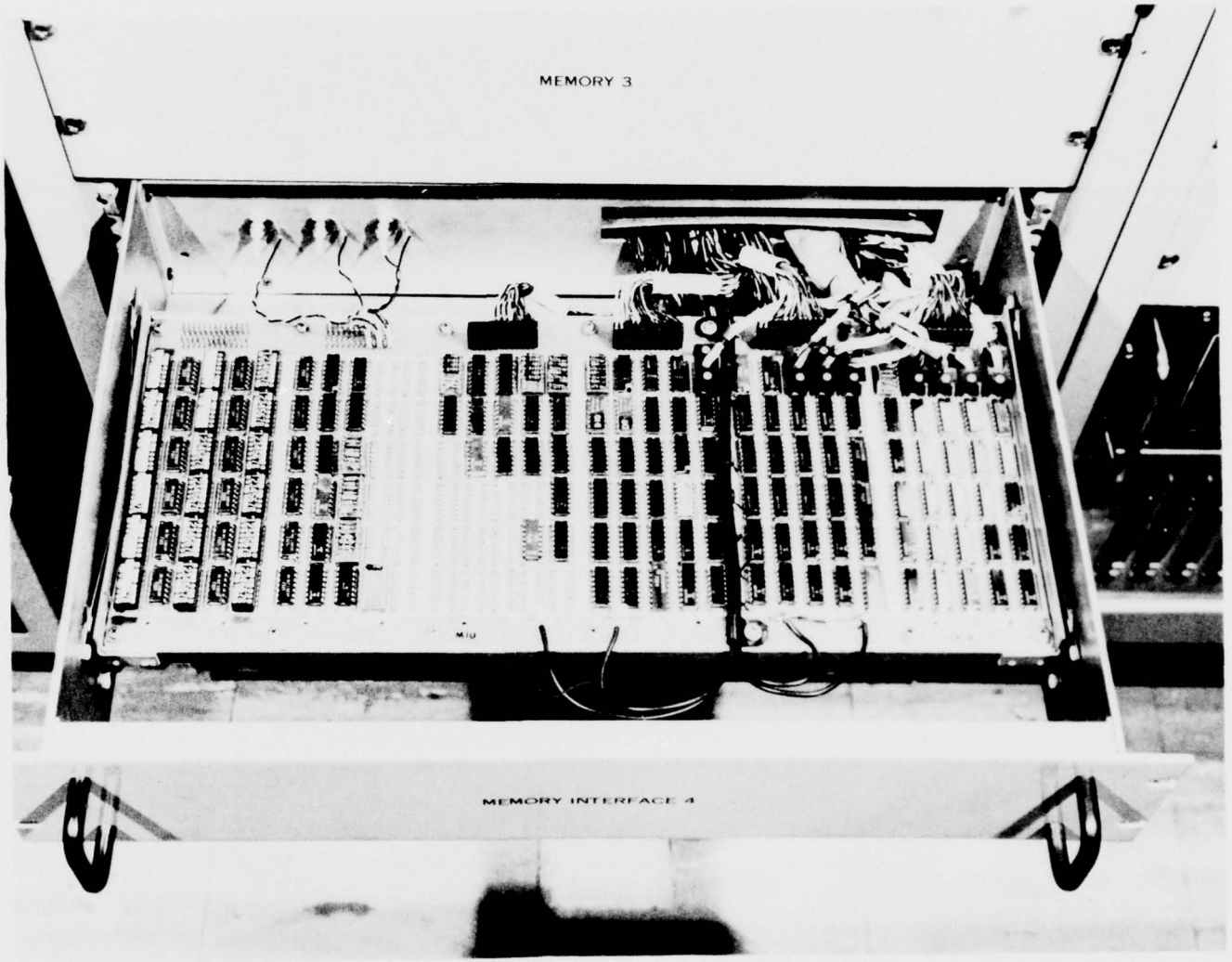

Figure A-7. Memory Interface Unit - Top View

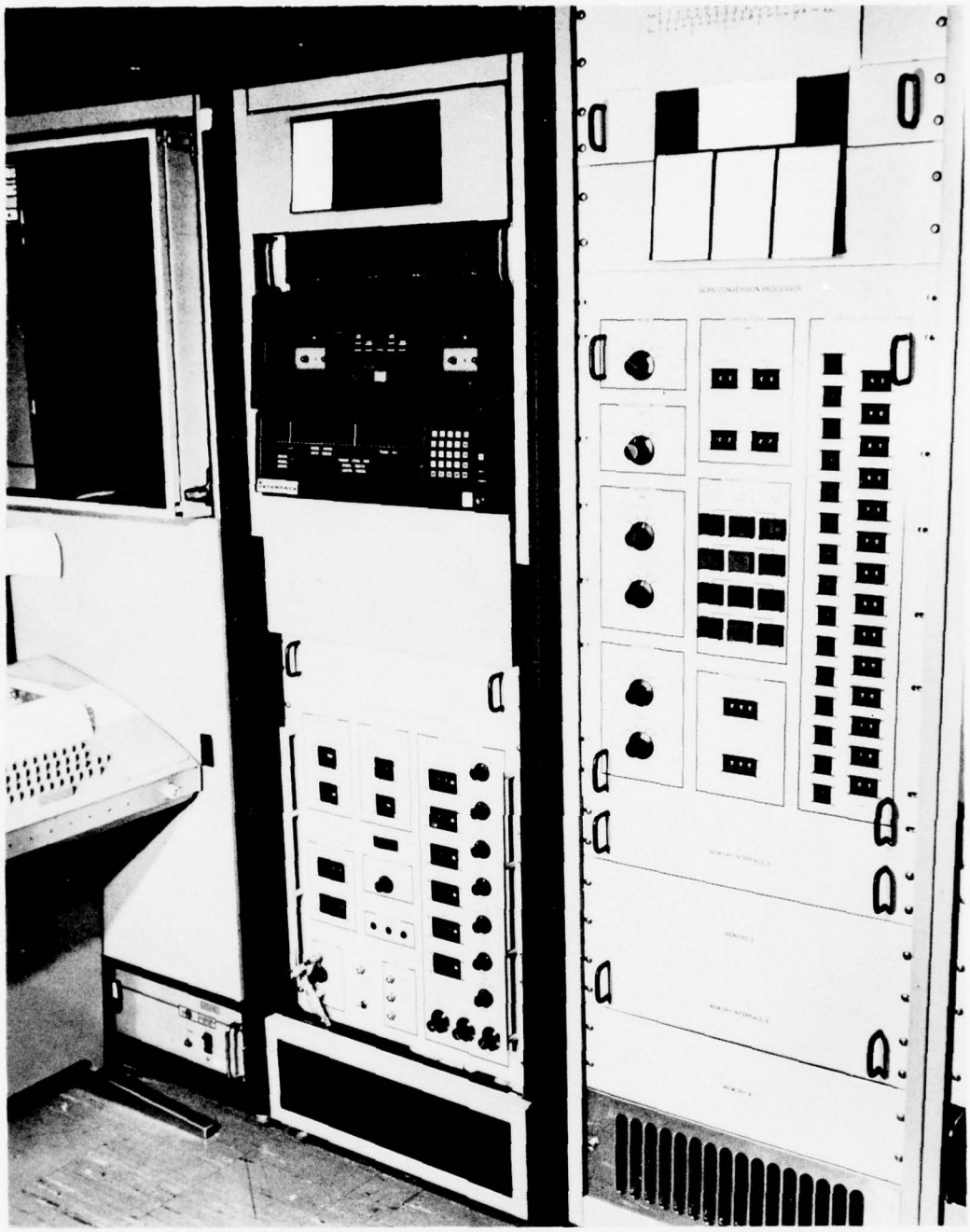

Figure A-8. Liquid Water Content Analyzer and Scan Conversion Processor

APPENDIX B

Product Information
on Sub-System Modules

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INTERFACE ENGINEERING

INCORPORATED

STOUGHTON, MASSACHUSETTS

DIGITAL TRANSLATOR

BINARY ANGLE TO SCALED BCD

MODEL DD107

DESCRIPTION

The DD107 Digital Translators accept the binary digital representation of angle (MSB = 180°) and develop the *angle scaled BCD equivalent*. The translation is performed by normalizing the input data with a scale factor and then converting the result into BCD.

The DD107-5 is a fast, high resolution, ripple-thru translator which accepts up to 15 bits of binary angle data and provides an 18 line BCD output with a resolution of .01°.

The DD107-4 accepts a 12 bit binary input and delivers a 14 line 4 digit *BCD output. This model contains an* input storage register and can be operated in either continuous, data freeze, or sampling modes of operation.

Input and output logic levels are DTL/TTL compatible. Accessory 4 and 5 decimal digit panel displays with decoder-drivers are available as optional accessories.

The translators are fully encapsulated in low profile cubes. Pins are arranged in groups of 7 on .100 centers permitting direct plug-in to wirewrap planes or PC boards.

FEATURES

- ☐ FAST – 500 Nanoseconds
- ☐ PRECISE – 0.01° Resolution
- ☐ CONVENIENT – Compact and logic compatible.

APPLICATIONS

- INTERCOMPUTER CODE CONVERSION
- NUMERICAL ANGLE DISPLAYS
- BINARY CONTROL OF BCD SHAFT POSITIONERS

SPECIFICATIONS

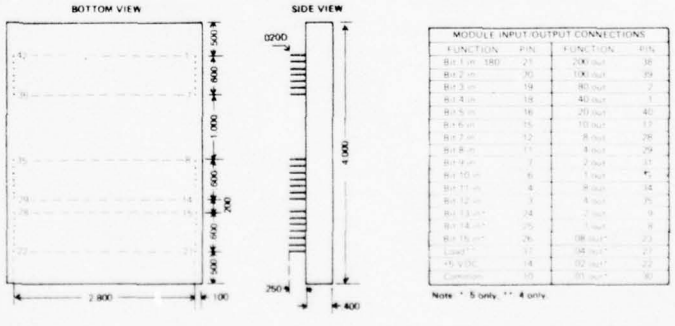
ELECTRICAL

	RESOLUTION				
MODEL	*IN*	*OUT*	*FULL SCALE*	*ACCURACY*	*STORAGE*
DD107-5	15 Bits	0.01°	359.99°	±.015°	External
DD107-4	12 Bits	0.1°	359.9°	±.055°	Internal

LOAD COMMAND (DD107-4)..... Positive True, 100 nanosec. min.
LOGIC LEVELS ..... Positive True DTL/TTL compatible
True = +2.0V to +5.5V
False = 0V to +0.8V
LOADING – Input ..... 4 Standard TTL loads max.
Output ..... 4 Standard TTL loads max.
POWER REQUIREMENTS ..... +5VDC±5% @ 750 MA

PHYSICAL

OPERATING TEMP. RANGE ..... 0° to +70°C
STORAGE TEMP RANGE ..... -54°C to +85°C
RELATIVE HUMIDITY ..... 100% non-condensing
SIZE ..... 3"W x 4"L x 0.4"H
PINS ..... .020" round, gold plated, 0.250" long min.
WEIGHT ..... 5 ounces



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INTERFACE ENGINEERING

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DIGITAL TRANSLATOR

BINARY ANGLE
TO
BINARY SINE

MODEL DD108

DESCRIPTION

The DD108 angle translators are purely digital devices which convert a binary input angle to the corresponding sine of the angle over an input angular range of 90° or, when operated with external quadrant and complementing logic, provide 4 quadrant operation with both sine and cosine digital outputs. (Refer to Bulletin 271007).

The translators employ parallel ripple-thru memories and interpolation logic providing a translation speed limited only by propagation delays. The translation speed, faster than equivalent computer operations, permits the translator to be time shared between using hardware providing the inherent precision of digital processing without tying up a general purpose computer on costly repetitive angle translation routines. Alternatively, the translators avoid the costs and accuracy degradation inherent in analog trig function generators. Both models provide a translation precision of 16 bits. The input resolution of the DD108-A is .088° and the input resolution of the DD108-B is .011°.

Input and output logic levels are DTL/TTL compatible. The translators are packaged in compact fully encapsulated low profile cubes. Pins are arranged as in-line groups of 7 on .100 centers permitting direct plug-in to wire-wrap planes or PC boards.

FEATURES

- ☐ FAST – 0.75 and 1.2 μsec.
- ☐ FINE – .088° and .011° steps
- ☐ PRECISE – 16 bit output
- ☐ ACCURATE – .005° arctan

APPLICATIONS

- SYNCHRO CONVERSION
- COORDINATE TRANSLATION
- SIGNAL PROCESSING
- RESOLVER COMPUTATION
- PATTERN GENERATORS

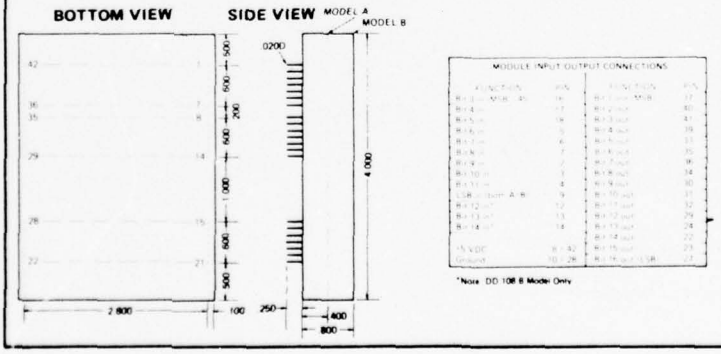
SPECIFICATIONS

ELECTRICAL

DD 108-A INPUT	10 bit binary angle, MSB = 45° LSB = 088°	
DD 108-B INPUT	13 bit binary angle, MSB = 45° LSB = 011°	
DIGITAL OUTPUT	16 bit binary magnitude Sine or Cosine	
ANGULAR RANGE	90° (Refer to bulletin 271007 for Sine and Cosine operation over 360° range)	
TRANSLATION ACCURACY	± .015% of full scale ± .005° arc (Sin/Cos)	
PROPAGATION DELAY	0.75 microseconds	DD 108-A
	1.20 microseconds	DD 108-B
LOGIC	Positive true, DTL/TTL compatible True = + 2.0V to + 5.5V False = 0V to 0.8V	
LOADING – Input	8 TTL loads max	
Output	2 TTL loads max.	
POWER – DD 108-A	+ 5 VDC ± 5% @ 600 ma	
DD 108-B	+ 5 VDC ± 5% @ 800 ma	

PHYSICAL

OPERATING TEMP. RANGE	0 to 70° C
STORAGE TEMP. RANGE	- 54 to + 125° C
SIZE AND WEIGHT – DD 108-A	3"W x 4"L x 0.4"H, 5 ounces
DD 108-B	3"W x 4"L x 0.8"H, 10 ounces
PINS	.020" round, gold plated, .250" L min.



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INTERFACE ENGINEERING

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STOUGHTON, MASSACHUSETTS

DIGITAL TRANSLATOR

BINARY ANGLE
TO
SIN/COS CONTROLLER

MODEL DD 109

DESCRIPTION

The DD109 Binary Angle to Sine and Cosine Controllers adapt the Model DD108 Binary Angle to Binary Sine translators to full four quadrant sine and cosine operation.

The controllers are purely digital devices which determine the quadrant in which the angle lies, determine the polarity of the sine and cosine outputs from the DD108, and route either the input angle or it's two's complement to the input of the DD108. Inhibit logic is provided for forbidden two's complement codes.

A single control line selects the sine or cosine output function. When the line is Low the combined output 17 bit code represents the sign and magnitude of the Sine of the input angle. When the line is High the output 17 bits represent sign and magnitude of the Cosine of the input angle.

The DD109 will accept up to 15 bits in binary angle and can be used with either the DD108A (.088° LSB) or DD108B (.011° LSB).

FEATURES

(With DD108 Angle to Sine Translator)

- ☐ FOUR QUADRANT OPERATION
- ☐ BOTH SINE AND COSINE OUTPUTS
- ☐ 12 OR 15 BIT ANGLE IN
- ☐ 17 BIT SIGN AND MAGNITUDE OUT
- ☐ ACCURACY ±0.005° ARCTAN

APPLICATIONS

- SYNCHRO CONVERSION
- SIGNAL PROCESSING
- COORDINATE TRANSLATION
- COORDINATE TRANSLATION
- PATTERN GENERATORS

SPECIFICATIONS

ELECTRICAL

Digital Input ..... 15 bit angle (MSB = 180°)

Function Select
- Sine ..... select line low (0)
- Cosine ..... select line high (1)

Digital Outputs

	Quadrant I	II	III	IV
Polarity (Direct Output)	0	0	1	1
Sine Polarity	0	1	1	0
Cosine Polarity	0	1	1	0

Angle to DD108 (MSB = 45°)

	Quadrant I	II	III	IV
Sine Select	θ	90° - θ	θ	90° - θ
Cosine Select	90° - θ	θ	90° - θ	θ

Translation Accuracy (With DD108)
- Magnitude ..... ±.015%
- Arc Sin/Cos Ratio ..... ±.005°

Propagation Delay ..... 0.95 usec with DD108A
1.50 usec with DD108B

Logic ..... Positive true, DTL/TTL compatible
True = +2.0V to +5.5V
False = 0 to 0.8V

Loading ..... Input ..... 3 TTL loads max.
Output ..... 10 TTL loads max.

Power ..... +5 VDC ±5% @450 ma

PHYSICAL

Operating Temp. Range ..... 0 to 70°C

Storage Temp. Range ..... -62 to + 125°C

Size and Weight ..... 2"W x 4"L x 0.4"H, 4 oz.

Pins ..... .020" round, gold plated
.250" L min.

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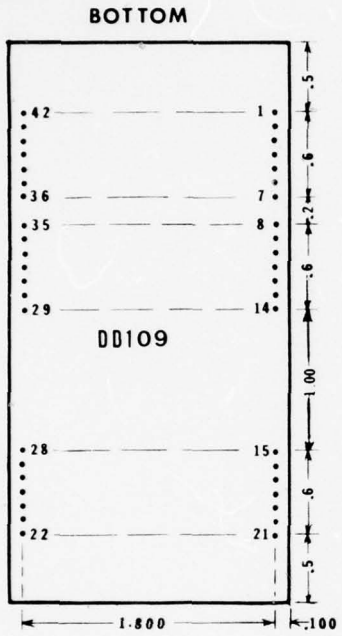
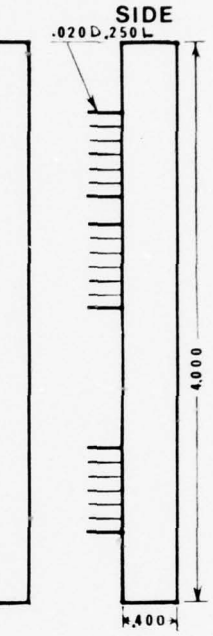
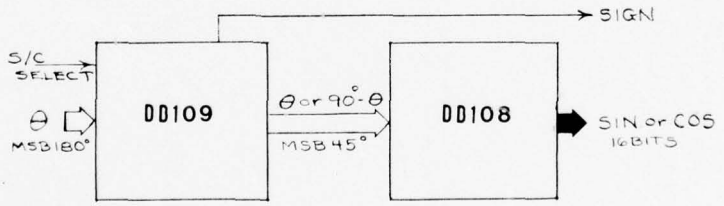


CONNECTIONS

FUNCTION	PIN	FUNCTION	PIN
Bit 1 In (180°)	25	Sign	26
Bit 2 In (90°)	24		
Bit 3 In (45°)	41	Bit 3 Out	3
Bit 4 In	39	Bit 4 Out	2
Bit 5 In	40	Bit 5 Out	1
Bit 6 In	38	Bit 6 Out	5
Bit 7 In	37	Bit 7 Out	8
Bit 8 In	36	Bit 8 Out	6
Bit 9 In	35	Bit 9 Out	7
Bit 10 In	34	Bit 10 Out	9
Bit 11 In	31	Bit 11 Out	15
Bit 12 In	30	Bit 12 Out	12
Bit 13 In	33	Bit 13 Out	13
Bit 14 In	32	Bit 14 Out	16
Bit 15 In (LSB)	18	Bit 15 Out	17
VCC + 5V	42		
Common	27	Sin/Cos Select	23





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Am2502/2503/2504

Eight-Bit/Twelve-Bit Successive Approximation Registers

Advanced Micro Devices

Complex Digital Integrated Circuits

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel counter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

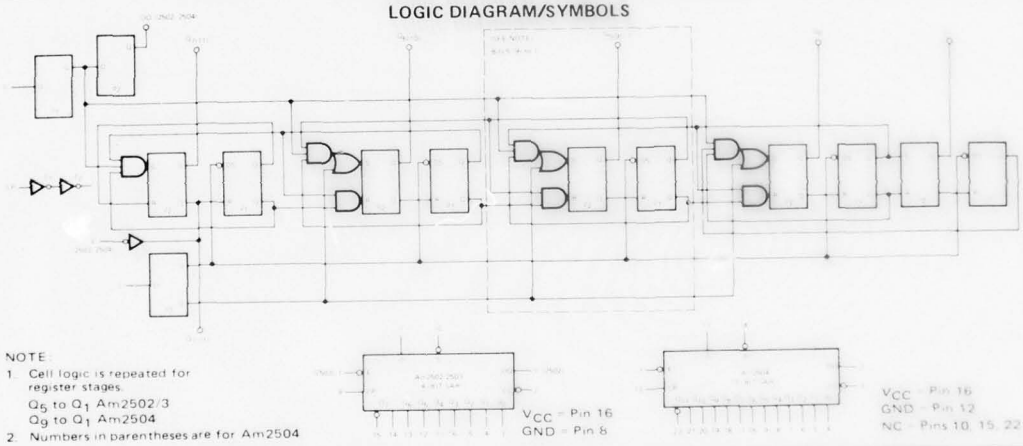
The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

LOGIC DIAGRAM/SYMBOLS



NOTE:
1. Cell logic is repeated for register stages.
   Q_5 to Q_1 Am2502/3
   Q_9 to Q_1 Am2504
2. Numbers in parentheses are for Am2504

V_{CC} = Pin 16
GND = Pin 8

V_{CC} = Pin 16
GND = Pin 12
NC = Pins 10, 15, 22

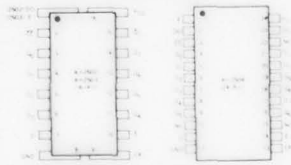
ORDERING INFORMATION

Package Type	Temperature Range	Am2502 Order Number	Am2503 Order Number	Am2504 Order Number
Molded DIP	0°C to +75°C	AM2502PC	AM2503PC	AM2504PC
Hermetic DIP	0°C to +75°C	AM2502DC	AM2503DC	AM2504DC
Hermetic DIP	−55°C to +125°C	AM2502DM	AM2503DM	AM2504DM
Hermetic Flat Pak	−55°C to +125°C	AM2502FM	AM2503FM	AM2504FM
Dice	Note	AM2502XX	AM2503XX	AM2504XX

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS

Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

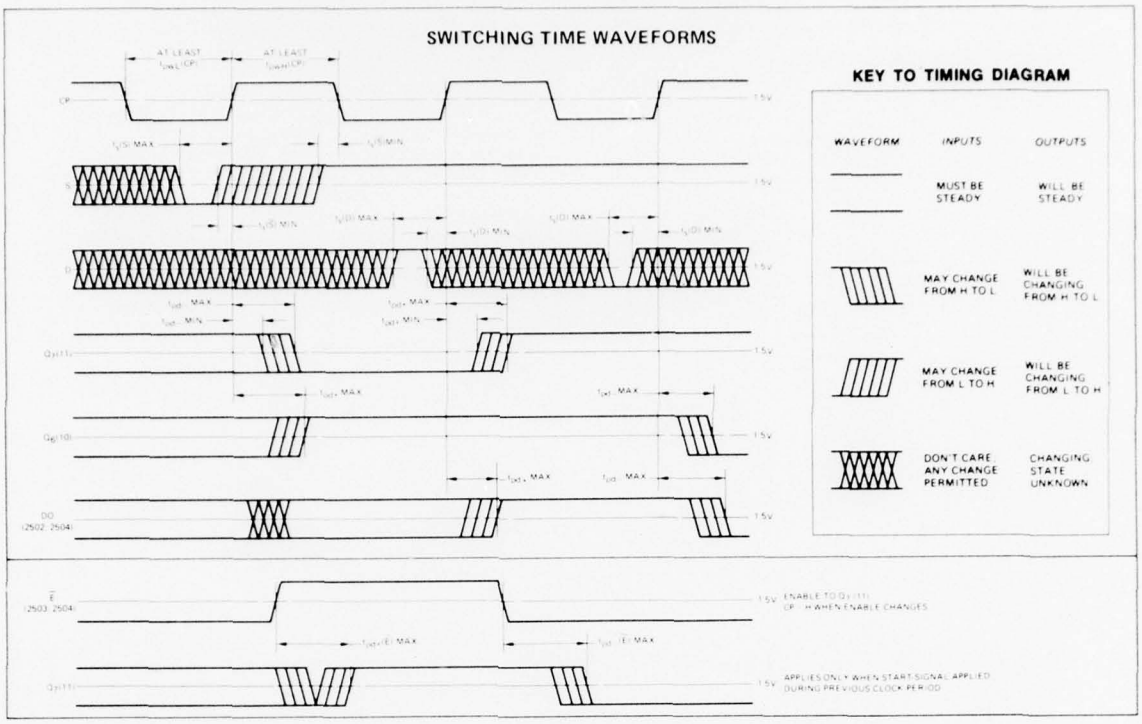
Am2502XC Am2503XC Am2504XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am2502XM Am2503XM Am2504XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				6.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			−10	−25	−45	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am2502	XM		65	85	mA
				XC		65	95	
			Am2503	XM		60	80	mA
				XC		60	90	
			Am2504	XM		90	110	mA
				XC		90	124	

Note 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF

Parameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	ns
t_s(D)	Set-up Time Data Input		−10	4	8	ns
t_s(S)	Set-up Time Start Input		0	9	16	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	(Am2503/4)		13	19	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW	C_P = H, $\bar{S}$ = L		16	24	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20	ns
f_{max}	Maximum Clock Frequency		15	25		MHz



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O *Output*

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2 L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the register.

E The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ The true output of the MSB of the register.

$\overline{Q_7(11)}$ The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\overline{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

t_{pd-}(E) The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

t_{pd+}(E) The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

t_s(D) Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max. and t_s min. before the clock.

t_s(S) Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

t_{pw}(CP) The minimum clock pulse width (LOW or HIGH) required for proper register operation.

Am2502/3 TRUTH TABLE

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

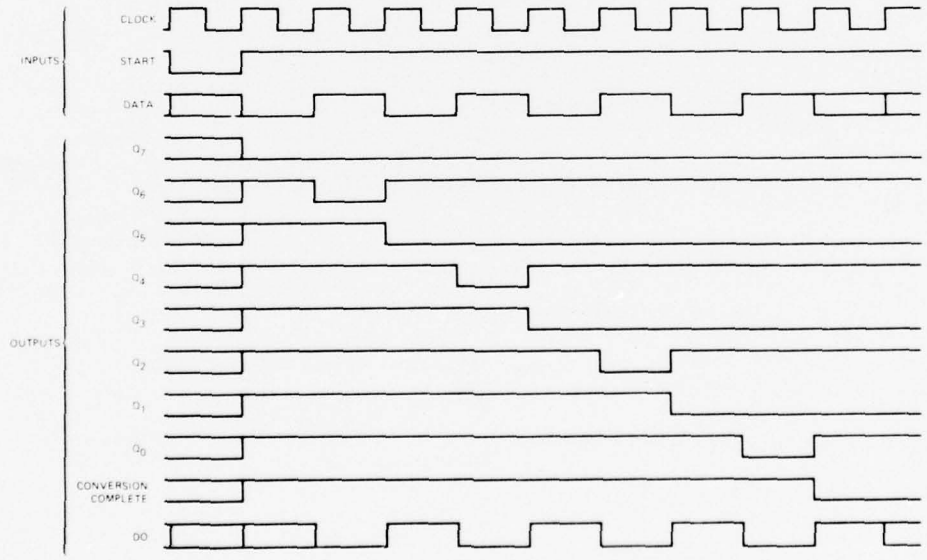
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for Am2504 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

Am2502/3 TIMING CHART



Am2502/3 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$ (2503)	1	2	2	–	–
DO (2502)	1	–	–	12	6
CC	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	2	2	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
S	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
$\overline{Q_7}$	14	–	–	12	6
Q_7	15	–	–	12	6
V_{CC}	16	–	–	–	–

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

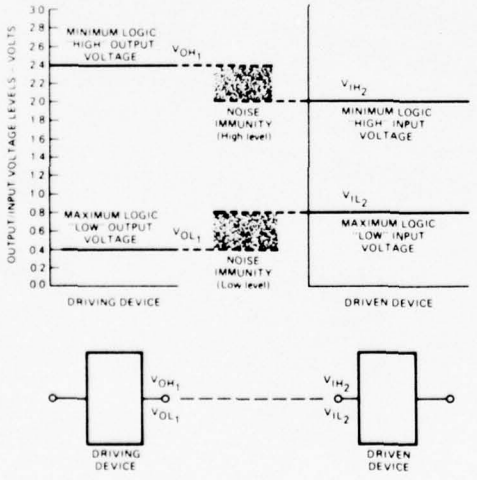
Am2504 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$	1	2	2	–	–
DO	2	–	–	12	6
CC	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–	–	12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	2	2	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
$\overline{S}$	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
Q_{11}	21	–	–	12	6
NC	22	–	–	–	–
$\overline{Q_{11}}$	23	–	–	12	6
V_{CC}	24	–	–	–	–

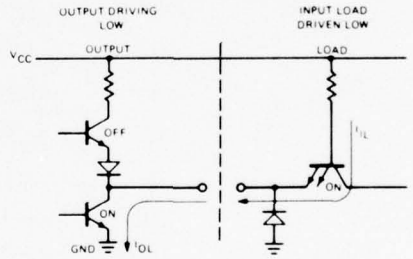
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

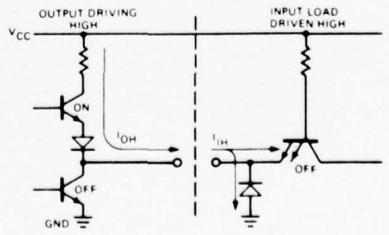
Voltage Interface Conditions – LOW & HIGH



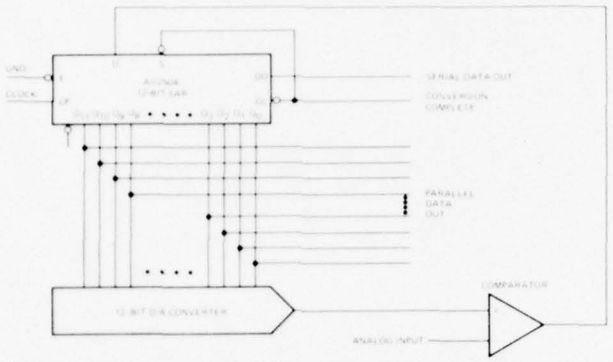
Current Interface Conditions – LOW



Current Interface Conditions – HIGH



Am2502/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter

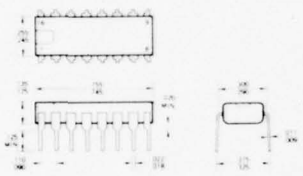


This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second. A 10-bit continuous conversion can be performed by connecting Q_1 to Q_3 and using Q_1 as the conversion complete signal. The comparator can be the Am111 precision comparator, Am106 high-speed comparator, or Am686 very high-speed comparator.

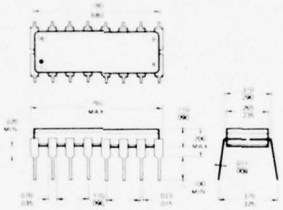
PHYSICAL DIMENSIONS

Am2502/3

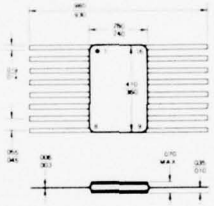
16-Pin Molded DIP



16-Pin Hermetic DIP

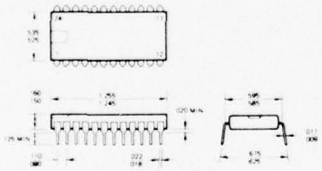


16-Pin Flat Pak

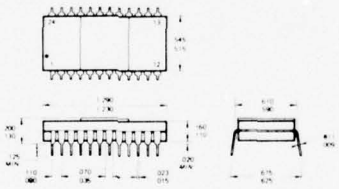


Am2504

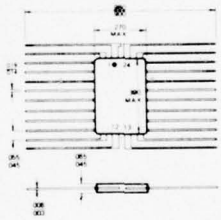
24-Pin Molded DIP



24-Pin Hermetic DIP

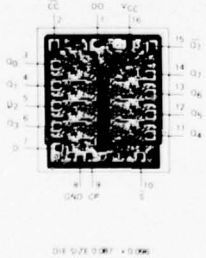


24-Pin Flat Pak

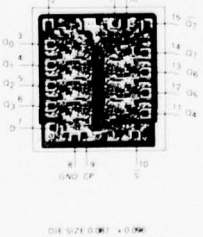


Metallization and Pad Layout

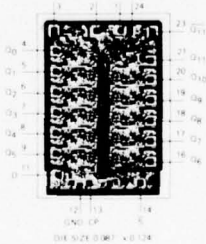
Am2502



Am2503



Am2504



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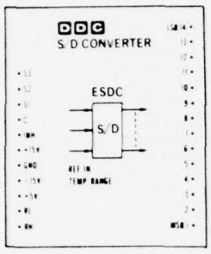
PIN DESIGNATIONS AND CONNECTIONS

Models ESDC or ERDC, H or L (400 Hz)

INPUT	CONVERTER CONNECTION	OUTPUT
Synchro input: 11.8V L-L, 400 Hz (ESDC-L), or 90V L-L, 400 Hz (ESDC-H)	S1, S3, S2	
Reference input: 26V, 400 Hz (ESDC-L), or 115V, 400 Hz (ESDC-H)	RH (high side), RL (low side)	
Power Supplies ±5%: +15V @ 55mA	+15V	
−15V @ 30mA	−15V	
+ 5V @ 280mA	+5V	
Common	GND	
Logic "0" forces data hold	INH	
	C	Converter busy when logic "1"
	MSB 1	180° True Logic
	2	90
	3	45
	4	22.5
	5	11.25
	6	5.625
	7	2.813
	8	1.406
	9	0.7031
	10	0.3516
	11	0.1758
	12	0.08799
	13	0.04395
	14	0.02197

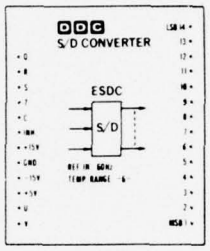


TOP VIEW OF MODULE

TOP VIEW OF TRANSFORMER MODULE

Model ESDC-6 (50-400 Hz)

INPUT	TRANSFORMER CONNECTION	CONVERTER CONNECTION	OUTPUT
Synchro input: 90V L-L, 50-400 Hz	S1, S3, S2		
Reference input: 115V, 50-400 Hz	RH (high side), RL (low side)		
	R	connect to R	
	Q, Q′	connect to Q	
	S	connect to S	
	W	*(no connection)*	
	T	connect to T	
	V	connect to V	
	U	connect to U	
Power supplies ±5%: +15V @ 75mA		+15V	
−15V @ 50mA		−15V	
+ 5V @ 400mA		+5V	
Common		GND	
Logic "0" forces data hold		INH	
		C	Converter busy when logic "1"
		MSB 1	180° True Logic
		2	90
		3	45
		4	22.5
		5	11.25
		6	5.625
		7	2.813
		8	1.406
		9	0.7031
		10	0.3516
		11	0.1758
		12	0.08799
		13	0.04395
		14	0.02197



TOP VIEW OF CONVERTER MODULE

SPECIFICATIONS

ELECTRICAL

PARAMETER	VALUE
ACCURACY(1)	±4 minutes ±0.9 LSB
RESOLUTION	14 Bits
CODING	natural binary 'angle'
DIGITAL OUTPUT	parallel, positive logic, DTL/TTL levels, 14 angle data, 1 inhibit and 1 converter busy line
SYNCHRO INPUT(2)(3)	11.8V rms L-L 400 Hz into 70KΩ min. L-L balanced (ESDC-L) 90V rms L-L 400 Hz into 600KΩ min. L-L balanced (ESDC-H) 90V rms L-L 50-400 Hz into 4MΩ min. L-L balanced (ESDC-6)
SYNCHRO INPUT RATES(5)	0 to 360°/sec., full accuracy; 180°/sec² = 1 LSB error (ESDC-H or L) 0 to 180°/sec., full accuracy; 6°/sec² = 1 LSB error (ESDC-6)
RESOLVER INPUT(2)(3)	11.8V rms L-L 400 Hz into 10KΩ min. L-L balanced (ERDC-L) 90V rms L-L 400 Hz into 600KΩ min. L-L balanced (ERDC-H)
RESOLVER INPUT RATES(5)	0 to 360°/sec., full accuracy 180°/sec.², 1 LSB error
REFERENCE INPUT(2)(3)	26V at 5mA rms 400 Hz (ESDC or ERDC-L) 115V at 0.6mA rms 400 Hz (ESDC or ERDC-H) 115V at 2.5mA rms 50-400 Hz (ESDC-6)
POWER SUPPLY REQUIREMENTS(4)	+15V at 75mA, −15V at 50mA, +5V at 400mA

(1) Accuracy applies over operating temperature range, ±5% variation of power supplies and ±10% amplitude and frequency variation.
(2) Other input voltages and frequencies available.
(3) Transformer isolated.
(4) *Available for use with ±12V supplies.*
(5) 4 R.P.S. available on 400 Hz converters by specifying suffix FT.

ENVIRONMENTAL

TEMPERATURE RANGES
- OPERATING: −55°C to +85°C (ESDC-H, L, or 6-1); 0°C to +70°C (ESDC-H, L, or 6-3)
- STORAGE: −55°C to +125°C

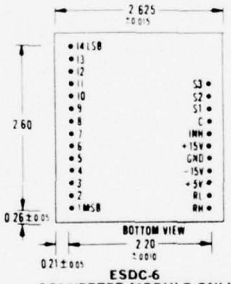
OTHER ENVIRONMENTAL
MEETS REQUIREMENTS OF *MIL-STD-202C, METHODS* 204A, 106B, 107B, 101B and 105.

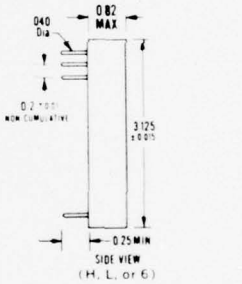
ORDERING INFORMATION

To order, specify model desired, followed by the designation of the operating temperature range required (e.g. ESDC-6-1).

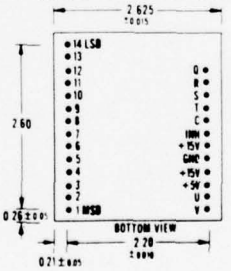
MECHANICAL

ESDC-H or L COMPLETE



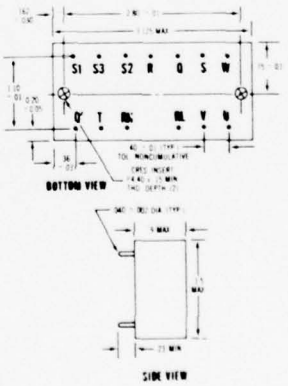


ESDC-6 CONVERTER MODULE ONLY



NOTE: In the 400 Hz versions (ESDC-H or L), the isolation transformers are packaged together with the converter in a single module. The 50-60 Hz version (ESDC-6) is supplied in two modules, one for the converter and one for the isolation transformers. Model 9010 mating sock accepts either module, but not the 50-60 Hz transformer module.

ESDC-6 TRANSFORMER MODULE



Timing

Figure 6 shows the timing waveforms of the converters. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a CONVERTER BUSY pulse. During the 3μs "busy" pulse, the output data is changing and should not be transferred into the computer output buffer. The converter will ignore an INHIBIT command applied during the "busy" interval until that interval is over. A simple method of interfacing to a computer is to: (a) apply the inhibit, (b) wait 5μs, (c) transfer the data, and (d) release the inhibit.

Although the computer usually will require that the data be synchronized and loaded as described above, it can be read-out asynchronously into a holding register using the trailing-edge of the "C" signal to effect the parallel transfer. This is shown in Fig. 7. In this configuration the data out of the register will change smoothly from θ to $\theta + 1$.

Testing

Because of the high accuracy of these converters, only laboratory-grade synchro or resolver substitution boxes or standards can be used. To avoid costly test equipment, we invite you to use DDC's facilities for "source inspection," at no extra cost.

To test the unit, arrange your test equipment as shown in Figure 8. A lamp-driver or suitable readout is necessary for each of the data outputs. We recommend the circuit shown in Fig. 5C. The Synchro Standard is set to the test angles. The angles corresponding to the lights which are on are added and compared with the standard angle. Maximum observed error shall be less than ±4 minutes ±0.9 LSB over the temperature range. A table of angles versus bits is given in Fig. 9. A typical room-temperature error curve is shown in Fig. 10. Each quadrant is identical, and error has been shown for the first quadrant. Error limits are also indicated for temperature extremes.

Figure 6: Timing

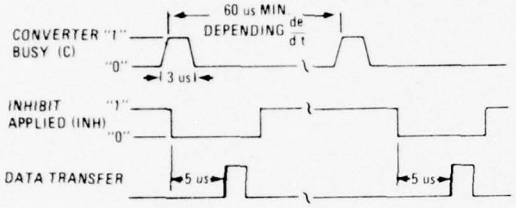


Figure 7: Asynchronous Parallel Transfer

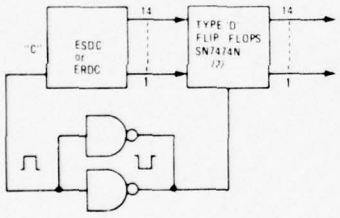


Figure 8: Test Configuration

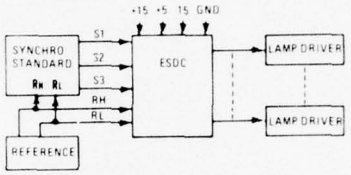
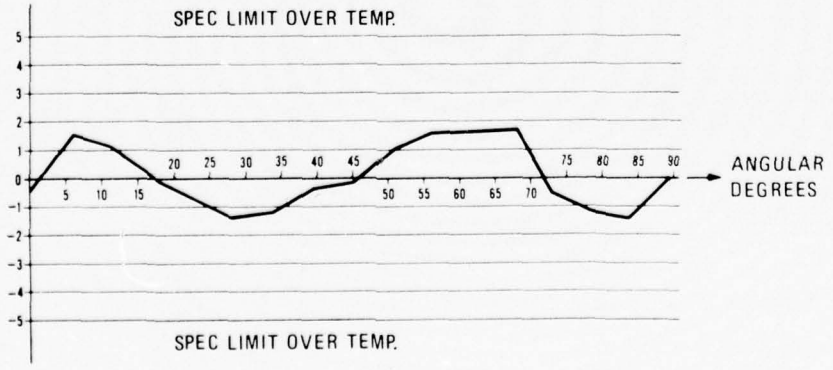


Figure 9: Angles vs. Bits

MSB 1	180
2	90
3	45
4	22.5
5	11.25
6	5.625
7	2.813
8	1.406
9	0.7031
10	0.3516
11	0.1758
12	0.08799
13	0.04395
LSB 14	0.02197

Figure 10: Typical Error, Minutes, Each Quadrant, 25°C for ESDC



2065

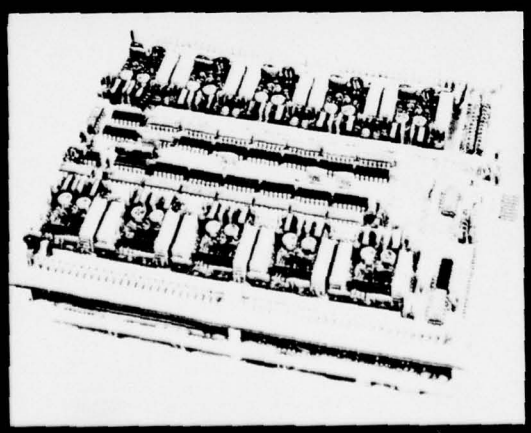
AMPEX

Ampex Computer Products Corporation
(3031 West Jefferson Boulevard
Marina del Rey, California 90291
A Subsidiary of Ampex Corporation

AMPEX CORE MEMORY MODULES, 250 NANOSECOND ACCESS AND 650 NANOSECOND CYCLE TIMES

Fast and compact
The Ampex 2065 core memory is faster and more compact than any other 20-bit word length memory available to the OEM. Access time is 250 ns, cycle time 650 ns. It measures only 8 inches high × 10 inches deep × 2 inches wide.

Unequaled packing density
You can store more than 160,000 bits in a single 2065 module which occupies only 170 cubic inches in your system. All circuitry is packaged on three removable printed circuit boards—data register, drive, and planar core stack. The compact dimensions of the 2065 provide inherent packaging flexibility which is superior to that of large single board systems. As a result, you have more space available for other important system functions.



Quality assured reliability
The 2065 has more built-in reliability than any comparable OEM memory. All critical areas of the memory receive extra attention, and design simplicity is followed throughout. Conservative derating practices, device qualification, and careful component specification further ensure overall reliability. Ruggedized construction used throughout the memory makes it particularly suited to industrial applications. Every stage of the manufacturing process is closely monitored by the Ampex Quality Assurance Department in accordance with MIL-Q-9858A.

Simple interface, easily expandable
Up to eight 8K × 20 modules can be combined in parallel for a capacity of 65,536 20-bit words. This flexibility permits the addition of memory capacity in increments to meet changing system requirements. Longer words can also be accommodated by combining modules. The use of module select decode and negative-TRUE open collector outputs makes interfacing extremely simple.

Faster switching, broader margins
The 2065 uses 18-mil temperature stable cores to provide fast switching and broad operating margins across the full 0°C to 55°C operating temperature range. Cooling requirements are also simplified. The planar stack consists of up to twenty 8,192-core mats with an integrated circuit diode decode matrix.

Maximum output, less noise
Coupled noise is reduced, and a maximum output signal is provided by high density core packaging which permits shorter sense, X and Y lines. Cores are aligned in a double-herringbone pattern with a center-to-center spacing (in the sense/digit winding direction) of less than one-half the core diameter. Precise core alignment is maintained by a proprietary silastic bonding which dissipates core switching heat and minimizes temperature gradients by providing a thermal path to the substrate.
Only two voltages are required +5 and −15.

Temperature compensated
There is no need for power supply temperature compensation, since drive current sources are temperature compensated in each module.
All the interconnections within the module between circuit boards are provided. No additional low level back panel wiring is required.

Modular interchangeability
Complete module-to-module uniformity is provided by optimization of memory timing, drive currents, and threshold levels in each module. Your field support and spares requirements are greatly simplified by the ability to interchange any module within a system or between different systems. Each module is a complete memory with self contained data register and timing and control functions.

AMPEX

Ampex Computer Products Corporation
(303) West Jefferson Boulevard
Marina del Rey, California 90291
A subsidiary of Ampex Corporation

2065

2065 specifications

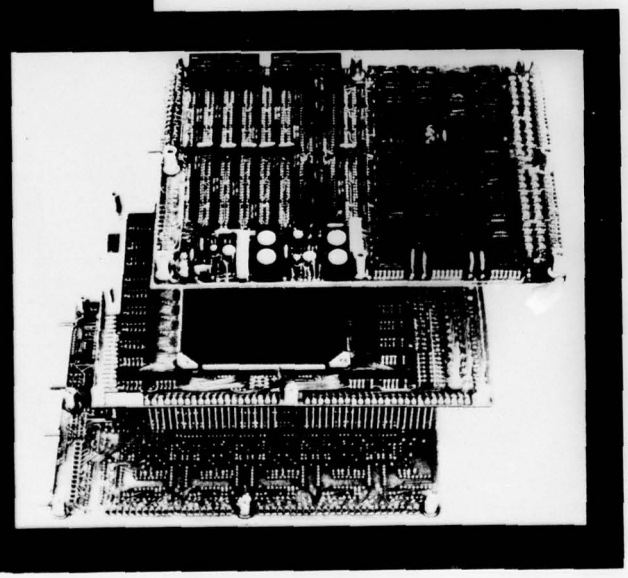
Access time	250 nanoseconds
Cycle time	650 nanoseconds
Capacity	2,048, 4,096, 8,192 words of 10, 16, 18 or 20 bits in a single module. Expandable in modules to a capacity of 65,536 words. Longer words can also be accommodated by combining modules.
Operational modes	Read-Restore Clear-Write Read-Modify-Write
Interface characteristics	TTL negative TRUE logic is used.
Standard input signal lines	Address input Data input Start input cycle (SIC) Start output cycle (SOC) Read-modify-write control Module select inputs (used to address separate modules in a multi-module system)
Standard output signals	Data output Unit available signal (memory busy) Data available signal End of cycle signal

DC power requirement

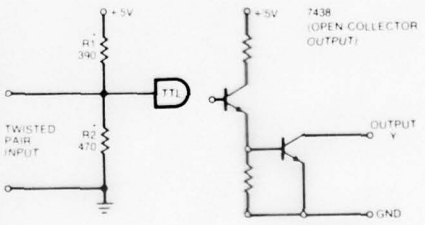
Voltage	Regulation	Current (Max)
−15 VDC	±3%	7.2 amps (20 bits)
+5 VDC	±5%	4.5 amperes source

No temperature compensation of either voltage is necessary.

Weight	4.0 lb.
Dimensions	8.0 inches (203.2 mm) high 10.0 inches (254.0 mm) deep 2.0 inches (51 mm) wide (2.125 inches with optional metal cover)
Operating Environment	0°C to 55°C ambient temperature Up to 90% relative humidity with no condensation
Non-operating environment	−55°C to +85°C ambient temperature Up to 95% relative humidity with no condensation
Available options	Byte control (2 bytes maximum) Zone control (2 zones maximum) External logic clear (Internal logic reset to ready) External memory register reset (Output lines at high logic state) External memory register transfer (For byte or zone control) Metal extractor handle Metal covers



Typical Input Receiver



Typical Output Driver

*R1 and R2 will be as shown unless otherwise specified.

Litho in U.S.A. C-341 11/72

1800 SERIES

AMPEX
CORE MEMORY
SYSTEMS USING
1800 SERIES
MODULES

AMPEX

Ampex Computer Products Corporation
13031 West Jefferson Boulevard
Marina del Rey, California 90291
A subsidiary of Ampex Corporation

Tailored to your needs

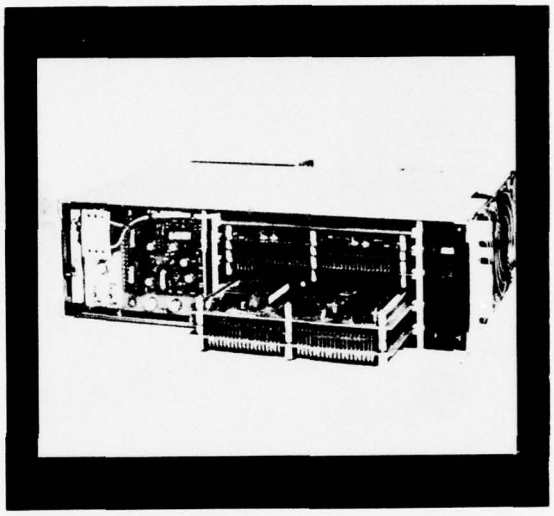
Complete Ampex 1800 Series core memory systems are designed to provide exactly the configurations and capacities you need for specialized OEM systems—at off-the-shelf prices. There are standard configurations which accommodate from two to eight memory modules. Any desired combination of standard or special interfaces, power supplies, testers, or blowers can be specified. System capacity extends all the way to 65,536 18-bit words. Word size is completely flexible—9, 12, 18 bits or longer if you choose. Access times are 230, 250, or 340 nanoseconds, and cycle times are 600, 650 or 850 nanoseconds, depending on the model you select. (Detailed performance and specification data on 1800 Series core memories is contained in individual Ampex product sheets on the following models: 1860, 1865, 1885, and the ruggedized 1800M Series.)

Lower design costs

You get a customized memory system — ready to plug in — for only a little more than module prices. You save even more money and time because your available design manpower can devote more effort to other portions of the system.

Higher packing density

Each of the basic 1800 Series memory configurations is carefully designed to provide maximum compactness and space-saving. You can build a complete Ampex memory system into your own system without sacrificing space required for other important system functions.



Standard or special interfaces

There are no interface problems when building the 1800 Series into your system. A standard interface is included, and space is provided in the memory card cage for any special interface you may require. If you wish, we also can supply special interface cards designed to your specification.

Fast, reliable, and expandable

The 1800 system is more than a fast, modular, building block memory customized to your specific requirements. It also has traditional Ampex reliability, full temperature range performance, and interchangeability. The MTBF is 10,000 hours, with an operating range from 0°C to 55°C. For applications requiring a ruggedized memory, the 1800M Series with an extended 0°C to 70°C temperature range and resistance to shock, vibration and dust can be specified. All Ampex 1800 Series memories are completely uniform from module-to-module and can be interchanged within a single system or between different systems.

Optional subsystems

You can select as many or as few subsystems as you need. These include 115V or 220V blower assemblies, one or two 115V or 220V power supplies, and an on-line tester which can completely check out total system operation. Standard connectors are supplied with all configurations.

1800

AMPEX

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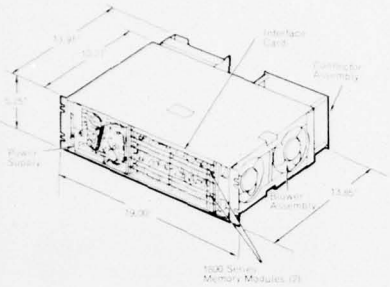
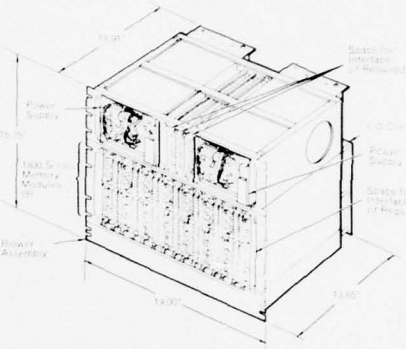
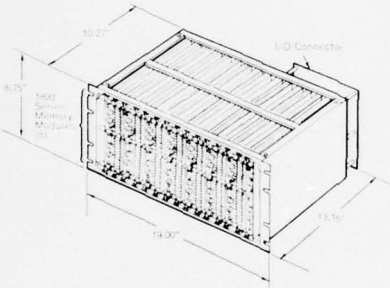
13031 West Jefferson Boulevard
Marina del Rey, California 90291
A subsidiary of Ampex Corporation



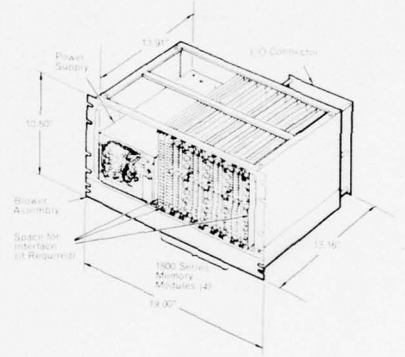
Two module configuration with interface card, power supply, connector assembly, and blower assembly.



Eight module configuration with two power supplies, blower assembly, I/O connector, and space for interface.

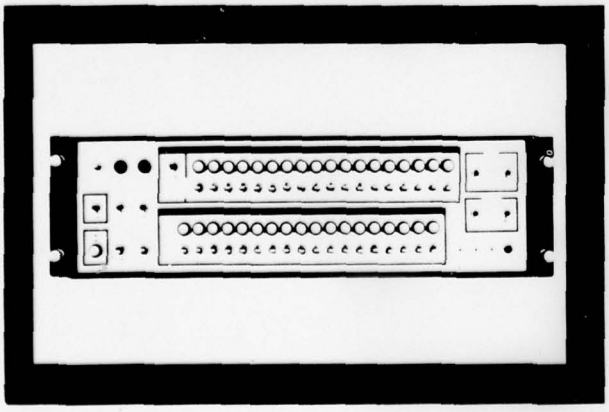


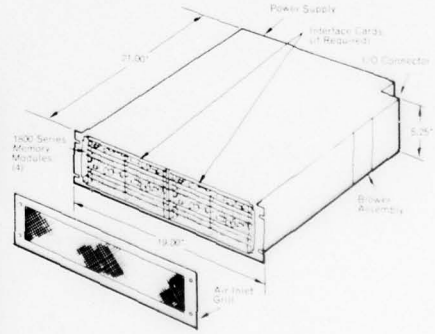
Eight module configuration with I/O connector, and space for interface.



Four module configuration with power supply, blower assembly, I/O connector, and space for interface.

An optional on-line tester capable of completely checking-out total system operation is available with most 1800 Series module configurations. Optional 115V or 220V power supplies also can be selected, as well as optional 115V or 220V blower assemblies. All configurations have standard connectors.





Four module configuration with power supply, blower assembly, I/O connector, air inlet grill, and space for interface.

Litho in U.S.A. C-330 11-72

RED, GREEN, BLUE TRANSISTORIZED COLOR VIDEO MONITOR

Model RHM19

Conrac's RHM19 is a compact, 100% solid-state, red-green-blue input color monitor designed to meet rigid performance requirements yet remaining simplified enough to permit operation by inexperienced personnel. It is available in a cabinet model for mounting on slides in 19" racks (taking up only 21" of vertical space) or for pedestal or ceiling mounting, permitting considerable flexibility in systems application. Its all-solid-state circuitry provides maximum stability, long life, low power drain (250 watts) and a minimum of heat. Its modular design and quick-disconnect circuit boards permit rapid replacement of circuits and ease of maintenance.

An independent, regulated second anode supply, plus regulation of the low voltage supply provides extremely stable pictures which will not change size or brightness as the AC line voltage varies between 105 and 130 volts or 210 and 260 volts. All power supplies incorporate current limiting and failure protection circuits.

The control of the contrast has been achieved by incorporating a unique automatic tracking system. The performance of this automatic system is greatly improved over the "three-gang potentiometer." This system is comprised of integrated circuit operational amplifiers and discrete components in a novel circuit to insure that the gain of all three video channels remain identical. A luminance ("Y") matrix is provided to permit viewing color pictures in monochrome and to facilitate testing. Brightness is controlled by the pulse addition technique to insure good gray-scale tracking and simplified setup procedures. Brightness pulses are generated in the monitor and synchronized to add to the video signal during horizontal retrace time. The amplitudes of the brightness pulses are adjusted from a single control on the front panel. This advantage makes the RHM19 monitor unique in the RGB field.

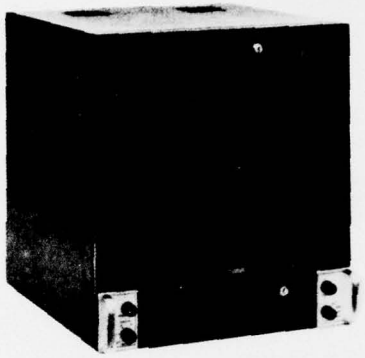
A vertical interval test switch on the front panel enables the operator to examine a test signal appearing in the vertical interval. An input video attenuator switch is provided with the following functions: OFF, Minus 6 dB, Zero dB, Monochrome.

All radial convergence controls, dynamic and static (DC), are located conveniently in the front panel. Dynamic correction is also applied to the blue lateral corrector. Dynamic pin-cushion correction is applied to both horizontal and vertical deflection systems. Complete control of individual guns allows the operator to turn on the beams in any combination in any desired sequence. This feature, coupled with an "Operate-Setup" switch and a color "On-Off" control switch, makes setup of the RHM19 easy and rapid.

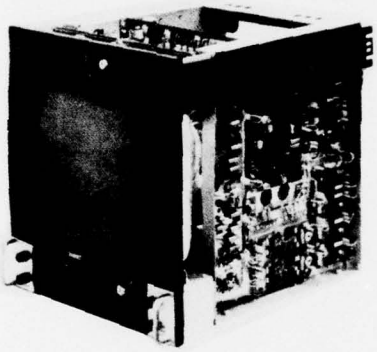
Input level compensation to permit balance of incoming signals is accomplished by keyed back porch clamps in each channel to accurately maintain black level.

The standard instrument is supplied with three sets of parallel coaxial connectors. It is optionally

(continued)



RHM19/C



RHM19/RS

CONRAC CORPORATION

available with dual A-B inputs with a front panel switch allowing either of two video signals to be viewed. With this option the unit is supplied with single input terminated connectors for red, green, and blue on both channels A and B.

In addition to the above features, the RHM19 also offers a built-in degausser, an underscan switch which permits inspection of the picture edges, electrical centering controls, a bonded safety shield on the kinescope for easiest possible tube cleaning, a coarse and a vernier tuning for the screen, locked trap doors for controlled operation and a conveniently located tally lamp which can be illuminated with either white or red.

This equipment complies with Department of Health, Education and Welfare rules — 42CFR — Part 78 — relating to X Radiation.

Specifications

TECHNICAL DATA

Input Power: 250 watts at 120/240 volts 60 Hz (525/60 N.T.S.C.), 50 Hz input power optional. All performance specifications will be met while the line voltage varies from 105 to 130 or from 210 to 260 volts AC. A three-wire line cord, six feet long, with twist-lock disconnect is furnished.

Video Signal: 0.35 volts p-p minimum. Sync negative at monitor input. 0.3 volts p-p minimum non-composite.

Video Input Impedance: High impedance bridging. Three sets of parallel coax input connectors. (Optional: The monitor may be ordered with two sets of inputs with a knob on the front panel to permit selection of Channel A or Channel B with remote switching between channel A and channel B. All inputs are 75 ohm single ended. It is possible to provide loop-through operation with both channel A and channel B by use of "T" connectors.)

Sync: Optional operation: Internal sync, external sync, or separate H and V drive. Parallel connectors for external 1-8 volts p-p for V drive. 1-8 volts p-p negative.

Video response: Flat to 7 MHz on each of three channels.

Linearity: Within 2% of picture height.

Kinescope: A 19301P22 tube, incorporating an etched laminated safety shield and controlled phosphors.

CONTROLS, CONNECTORS, ADJUSTMENTS

Primary Group, Front Panel:
Power (with optional A-B input selector)
Input attenuator monochrome switch
Preset and manual brightness
Contrast

Secondary Group, Front Panel:
Red, green, and blue fine screens
Red, green, and blue coarse screens
Red, green, and blue on-off switches
Brightness calibrate
Horizontal and vertical hold
Green and blue gain
Degaussing switch
Vertical linearity
Setup-operate
Height
Focus
Scan size
VIT-operate
Width

Adjustments, Top Front Panel:
20 convergence controls
Vertical and horizontal centering

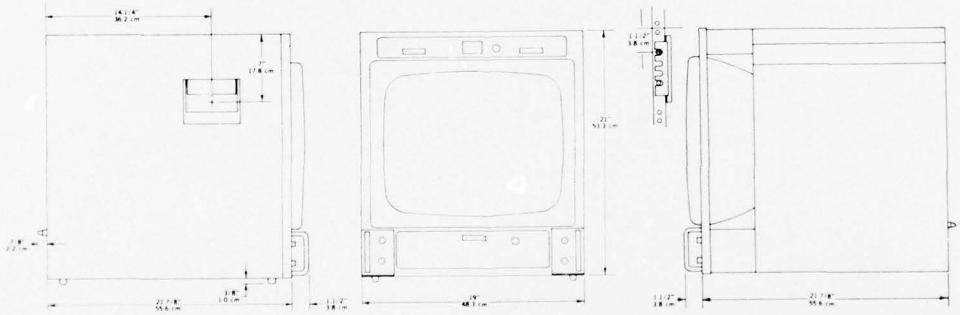
Rear Apron:
Internal-external/remote sync selector switch
Internal-external H and V drive switch
Red, green and blue parallel video input connectors
Channel "A" input red, green and blue (optional)
Channel "B" input red, green and blue (optional)
Horizontal drive parallel connectors
Vertical drive parallel connectors
Remote A-B connector (optional)
Twist-lock AC connector
AC outlet
Line fuse
Tally light connector

CONSTRUCTION

The RHM19 is constructed of heavy gauge aluminum while wave-soldered high-grade glass-epoxy boards are used for solid-state circuitry. Stranded Teflon insulated wires and high quality components are utilized. Panels and cabinets are finished in deep umber gray.

MECHANICAL

	Net Weight	Shipping Weight
RHM19/C Cabinet	101 lbs. 45.9 kilos	127 lbs. 57.6 kilos
RHM19/RS Rack Mount	102 lbs. 46.3 kilos	128 lbs. 58.1 kilos
RHM19/Y Bail Mount	102 lbs. 46.3 kilos	128 lbs. 58.1 kilos
M3 3-wheel dolly	22 lbs. 10.0 kilos	25 lbs. 11.3 kilos
M4 Pedestal mount	18 lbs. 8.2 kilos	20 lbs. 9.0 kilos
M5 Ceiling mount	8 lbs. 3.6 kilos	10 lbs. 4.5 kilos



RHM19/C

RHM19/RS

Conrac Division, 600 North Rimsdale Avenue, Covina, California 91722 / (213) 966-3511

CONRAC CORPORATION

Printed in U.S.A. November 1970

MS **MEASUREMENT SYSTEMS, INCORPORATED**

TRACKBALL MODEL 628

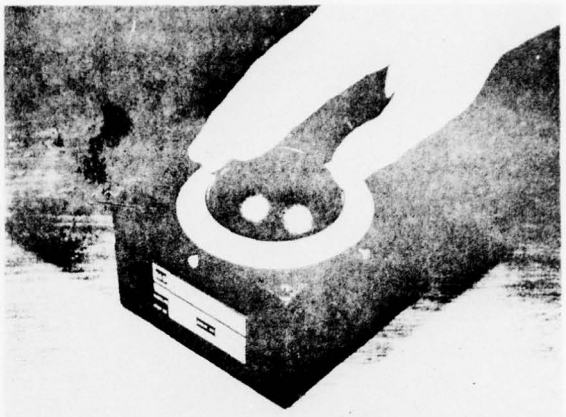
for

GRAPHIC DISPLAYS

AIR TRAFFIC CONTROL

RADAR CURSORS

MACHINE TOOL CONTROL



A small size trackball built to meet rugged environmental requirements is now available from stock in sample quantities.

EASY TO OPERATE

The Model 628 trackball is a fast and accurate 2 axis manual positioning device requiring a minimum amount of operator training and skill. Electrical signals proportional to magnitude and direction are resolved into X and Y components as the ball is rotated by the operator. Typically, bi-directional optical encoders are used that produce TTL pulses on an "up-count" or a "down-count" line.

DESIGN FEATURES

A 3 inch dia. ball in a 4.5 inch square package only 2.25 deep make this product a real space saver suitable for all but the most compact console designs. A drip-proof seal is standard on all models.

SMOOTH MOTION

Unique bearing and pick-off wheel designs provide this unit with the lowest operating force available. Tangential force required to move the ball in any direction is less than 2 ounces. Additional friction can be readily added to hold the ball from turning for turbulent environment applications.

MODEL 628 square waves

Uses long life optical shaft encoders that produce *square waves in quadrature* as the ball is rotated. The standard rate is 300 complete cycles per rotation of the ball. Output levels are TTL compatible, positive 5 volt. Other pulse rates available.

MODEL 628-1 potentiometer

Features multi-turn potentiometers that rotate full range for 3 turns of the ball. Resolution is .03% for standard 10k ohm potentiometers. Other resistance values are available.

MODEL 628-4 TTL pulses

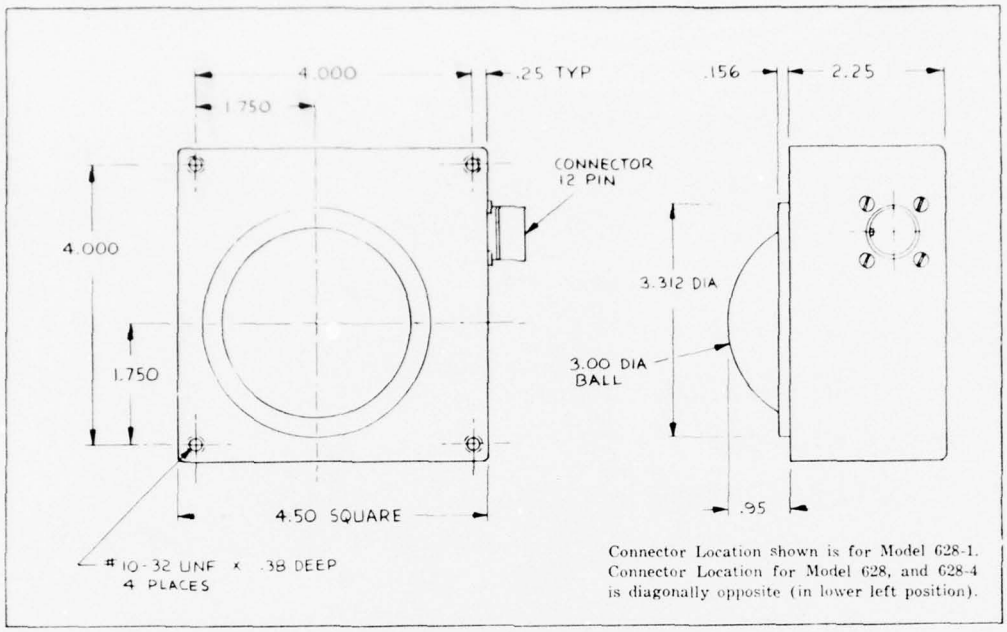
Identical to the 628 described above but with an additional logic circuit built into the package. Output becomes TTL pulses on an "up-count" line or a "down-count" line depending upon direction of rotation.

REPRESENTED B.
TEKDA

DEC. 73

MEASUREMENT SYSTEMS, INC. . . . 523 WEST AVENUE, NORWALK, CONN. . . . 203 838-5561.

MODEL 628 TRACKBALL



Connector Location shown is for Model 628-1. Connector Location for Model 628, and 628-4 is diagonally opposite (in lower left position).

SPECIFICATIONS

Weight	Less than 2 lbs
Tracking Force	Nom 1.5 oz, Max 2.0 oz
Housing	Aluminum Casting, Black
Environmental Seal	Drip Proof MIL-STD-108
MTBF	25,000 Hours
Power Requirements, Optical	+ 5vdc, 400ma
Connector	Amphenol 67-02E-14-12P
Counts per Revolution	300 Standard, other counts available

MODEL NO.	RESOLVER	OUTPUT, EACH AXIS
628	Optical Encoders	Square Waves in Quadrature +5V
628-1	Multi-turn Potentiometer	10k ohm, 1 watt, .03%, 3 turns full range
628-4	Optical Encoders	TTL Pulses on "Up" or "Down" line

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

MEASUREMENT SYSTEMS, INC. . . . 523 WEST AVENUE, NORWALK, CONN. . . . 203 838-5561.

DATEL SYSTEMS, INC.

GENERAL PURPOSE, ANALOG-TO-DIGITAL CONVERTERS

ADC-MA SERIES

FEATURES

- ▶ 10 & 12 Bit Resolution
- ▶ Selectable Input Ranges
- ▶ 20 & 40 μsec. Conversion Times
- ▶ Unipolar or Bipolar Operation
- ▶ Input Buffer Option
- ▶ Parallel & Serial Outputs

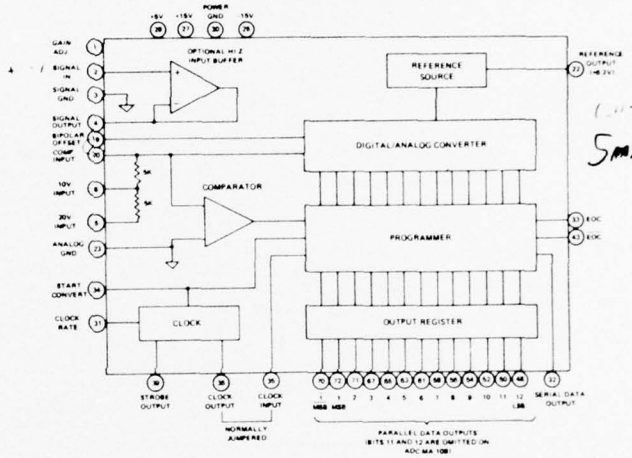
GENERAL DESCRIPTION

The ADC-MA series A/D converters consist of 10 and 12 bit resolution models with 20 or 40 microsecond conversion times. These units feature high performance and versatility at a low price.

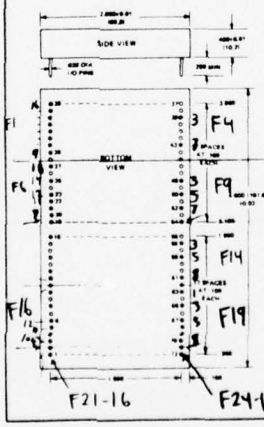
The exceptional versatility of the ADC-MA series is seen in the following features. Single-ended input voltage ranges of 0 to +5V, 0 to +10V, ±5V, and ±10V are pin selectable by the user. In addition, an internal high input impedance buffer amplifier is available as an option. This amplifier gives an input impedance of 1000 megohms on all voltage ranges. Without the amplifier the input impedances are 2.5K, 5K, and 10K ohms on 5V, 10V, and 20V full scale ranges respectively. Digital output data is available in either parallel form or serial NRZ format with synchronizing strobe pulses. Serial data is straight binary for unipolar operation and offset binary for bipolar operation. Parallel data is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. The ADC-MA units can operate either internally or externally clocked. In addition, the internal clock rate can be decreased by use of an external capacitor.

The ADC-MA series uses the successive approximation technique to achieve excellent linearity, speed, and stability. Temperature coefficient is held to ±30ppm/°C for gain and ±5ppm/°C for offset in unipolar operation. Tight temperature tracking of the weighted current sources results in monotonic operation with no missing codes over the 0°C to 70°C temperature operating range.

These converters are encapsulated in a 4 x 2 x 0.4 inch module with DIP compatible .100" pin spacing. Input power requirements are ±15VDC and +5VDC and are available from Datel's line of modular power supplies. All digital inputs and outputs are DTL/TTL compatible.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Open dots designate omitted pins. Pins 48 and 50 are omitted on 10 bit versions and pin 52 is the LSB. Pin position tolerance is ±0.005" from datum, non-accumulative.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Gain Adjust	35	Clock Input
2	Signal Input	36	Clock Output
3	Signal Gnd.	39	Strobe Output
4	Signal Output	43	E.O.C. (Status)
5	20 V. Input	48	Bit 12 Out (LSB)
6	10 V. Input	50	Bit 11 Out
19	Bipolar Offset	52	Bit 10 Out
20	Comparator In.	54	Bit 9 Out
22	Reference Out	56	Bit 8 Out
23	Analog Gnd	58	Bit 7 Out
25	-15V Pwr In	61	Bit 6 Out
27	+15V Pwr In	63	Bit 5 Out
29	+5V Pwr In	65	Bit 4 Out
30	Power Gnd	67	Bit 3 Out
31	Clock Rate	70	Bit 1 Out (LSB)
32	Serial Output	71	Bit 2 Out
33	E.O.C. (Status)	72	Bit 1 Out (MSB)
34	Start Convert		

SPECIFICATIONS (typical @ 25°C unless otherwise noted)

	ADC-MA10B	ADC-MA12B
INPUTS		
Analog Input Range	0 to +5V FS, 0 to +10V FS, ±5V FS, ±10V FS	
Input Overvoltage	±15V without damage to unit	
Input Impedance		
0 to +5V FS Range	2.5K ohms	2.5K ohms
±5V and 0 to +10V FS Range	5K ohms	5K ohms
±10V FS Range	10K ohms	10K ohms
With Optional Input Buffer	1000 Megohms	1000 Megohms
Start of Conversion	+2V min. to +5.5V max. positive pulse, DC coupled, with duration of 100 nsec. min. Rise and fall times 500 nsec. max. Three TTL loads. Logic "1" resets converter. Transition to logic "0" initiates conversion.	
Clock Input	Must be connected to Clock Output to use internal clock. Clock Input can also be used with an external clock.	
Clock Rate	Rate is internally set to give maximum conversion rate of 20 or 40 µsec. per conversion. This time may be increased with an external capacitor connected between pin 31 (Clock Rate) and pin 36 (Clock Out). See conversion time formulas.	
OUTPUTS		
Parallel Output Data	10 Lines of data	12 Lines of data
	Data is held until next conversion command. Each output is capable of driving 5 TTL loads. V out (Logic "0") ≤ +0.4V, V out (Logic "1") ≥ +2.4V	
Coding		
Unipolar Operation	Straight Binary, positive true.	
Bipolar Operation	Offset Binary or Two's Complement, positive true.	
Serial Output Data	NRZ (nonreturn to zero) successive decision pulse output generated during conversion with MSB first. Serial data is straight binary for unipolar operation and offset binary for bipolar operation. Output will drive 10 TTL loads. Two's complement is not available with serial output.	
Strobe Output	Available for serial data synchronization. Serial output is usable on strobe pulse leading edges. Will drive 9 TTL loads.	
EOC (End of Conversion)	Conversion status output. Logic "0" for conversion complete, Logic "1" during reset and conversion period. Will drive 10 TTL loads.	
$\overline{EOC}$	Complement of End of Conversion output. Logic "1" for conversion complete and Logic "0" during reset and conversion period. Will drive 7 TTL loads.	
Clock Output	Internal clock pulse train output gated on during conversion time.	
Signal Output	Output of optional internal buffer amplifier.	
PERFORMANCE		
Resolution	10 Bits (one part in 1024)	12 Bits (one part in 4096)
Accuracy	±.05% FS ±½LSB	±.012%FS ±½LSB
Linearity	±½LSB	±½LSB
Temp. Coefficient of Gain	±30 ppm/°C max. of Reading	±30 ppm/°C max. of Reading
Temp. Coefficient of Zero		
Unipolar	±5 ppm/°C max. of Range	±5 ppm/°C max. of Range
Bipolar	±10 ppm/°C max. of Range	±10 ppm/°C max. of Range
Conversion Time, max.	20 or 40 µsec. (depending on model)	20 or 40 µsec. (depending on model)
Power Supply Sensitivity (tracking ±15V supplies)		
Gain	±20 ppm/%	±20 ppm/%
Zero	±10 ppm/%	±10 ppm/%
POWER REQUIREMENT (with input buffer amplifier)	+15VDC ±0.5V @ 40mA, max. -15VDC ±0.5V @ 45mA, max. + 5VDC ±0.25V @ 200mA, max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to 70°C	
Storage Temperature Range	-55°C to +85°C	
Relative Humidity	Up to 100% non-condensing	
Case Size	4" x 2" x 0.4"	
Case Material	Black Diallyl Phthalate per MIL-M-14, epoxy encapsulated.	
Pins	.020" round, gold plated, .250" long min.	
Weight	8 oz. (227 grams)	
Mating Sockets (optional)	DILS-2, 4 required.	

TECHNICAL NOTES

The ADC-MA series contains an internal clock which is set to the maximum conversion rate. This rate may be decreased by connecting an external capacitor between pins 31 and 36. The approximate capacitor value to achieve the desired conversion time is shown in the table at the bottom of the next page. The longer conversion time obtained in this manner does not improve accuracy but it does permit compatibility or synchronization with interfacing equipment for many applications. To use the internal clock a jumper must be connected between pins 35 and 36. For *external clocking, which may be* desirable in some applications, the jumper is removed and the external clock applied to pin 35. Use a symmetrical 0 to +5V square wave with a minimum 3.0 µsec. period for the 40 µsec. converters and a minimum 1.6 µsec. period for the 20 µsec. converters. The Start Convert pulse should have a minimum 100 nsec. width and should not be made too long since clocking begins on the falling edge of this pulse and, therefore, its width is part of the total conversion time.

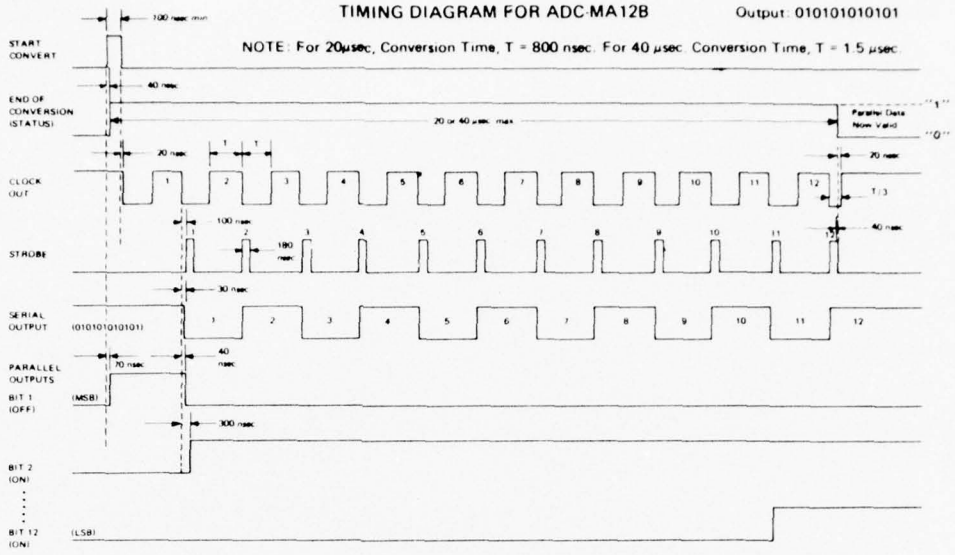
Analog inputs are connected to pin 6 for 10V ranges and pin 5 for the 20V range when the input buffer amplifier is not used. The input impedances in *these cases are 5K ohms and 10K ohms* respectively. For the 0 to 5V range, pin 5 is connected to pin 20, thus paralleling the two internal 5K resistors to give a 2.5K ohm input impedance at pin 6.

The end of conversion or status pulse is available at pin 33 and its complement $\overline{EOC}$ is available at pin 43. Normally the EOC output is used to control the mode of the input sample and hold. Serial output data is available at pin 32 in straight binary code for unipolar operation or offset binary for bipolar operation. Nonreturn to zero (NRZ) format is used and the data is valid at the leading edge of the strobe pulse. Parallel data output is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. Two's complement is obtained by using the complemented MSB output at pin 70.

TIMING DIAGRAM FOR ADC-MA12B

Output: 010101010101

NOTE: For 20μsec. Conversion Time, T = 800 nsec. For 40 μsec. Conversion Time, T = 1.5 μsec.



OUTPUT DIGITAL CODING, ADC-MA SERIES

ADC-MA12B (12 BITS)

UNIPOLAR INPUT RANGE		STRAIGHT BINARY	BIPOLAR INPUT RANGE		OFFSET BINARY	TWO'S COMPLEMENT
0 TO +10V FS	*0 TO +5V FS*	MSB LSB	±10V FS	±5V FS	MSB LSB	MSB LSB
+9.9976	+4.9988	111111111111	+9.9951	+4.9976	111111111111	011111111111
+8.7500	+4.3750	111000000000	+7.5000	+3.7500	111000000000	011000000000
+7.5000	+3.7500	110000000000	+5.0000	+2.5000	110000000000	010000000000
+5.0000	+2.5000	100000000000	0.0000	0.0000	100000000000	000000000000
+2.5000	+1.2500	010000000000	-5.0000	-2.5000	010000000000	110000000000
+1.2500	+0.6250	001000000000	-7.5000	-3.7500	001000000000	101000000000
+0.0024	+0.0012	000000000001	-9.9951	-4.9976	000000000001	100000000001
0.0000	0.0000	000000000000	-10.0000	-5.0000	000000000000	100000000000

ADC-MA10B (10 BITS)

+9.9902	+4.9951	1111111111	+9.9805	+4.9902	1111111111	0111111111
+8.7500	+4.3750	1110000000	+7.5000	+3.7500	1110000000	0110000000
+7.5000	+3.7500	1100000000	+5.0000	+2.5000	1100000000	0100000000
+5.0000	+2.5000	1000000000	0.0000	0.0000	1000000000	0000000000
+2.5000	+1.2500	0100000000	-5.0000	-2.5000	0100000000	1100000000
+1.2500	+0.6250	0001000000	-7.5000	-3.7500	0010000000	1010000000
+0.0098	+0.0049	0000000001	-9.9805	-4.9902	0000000001	1000000001
0.0000	0.0000	0000000000	-10.0000	-5.0000	0000000000	1000000000

EXTERNAL PIN CONNECTIONS

INPUT RANGE (FS)	BUFFER OPTION	INPUT TO PIN	JUMPER PIN 4 TO	JUMPER PIN 20 TO	JUMPER PIN 19 TO
0 TO +10V	WITHOUT	6	–	–	23
	WITH	2	6	–	23
±5V	WITHOUT	6	–	–	20
	WITH	2	6	–	20
±10V	WITHOUT	5	–	–	20
	WITH	2	5	–	20
0 TO +5V	WITHOUT	6	–	5	28
	WITH	2	6	5	23

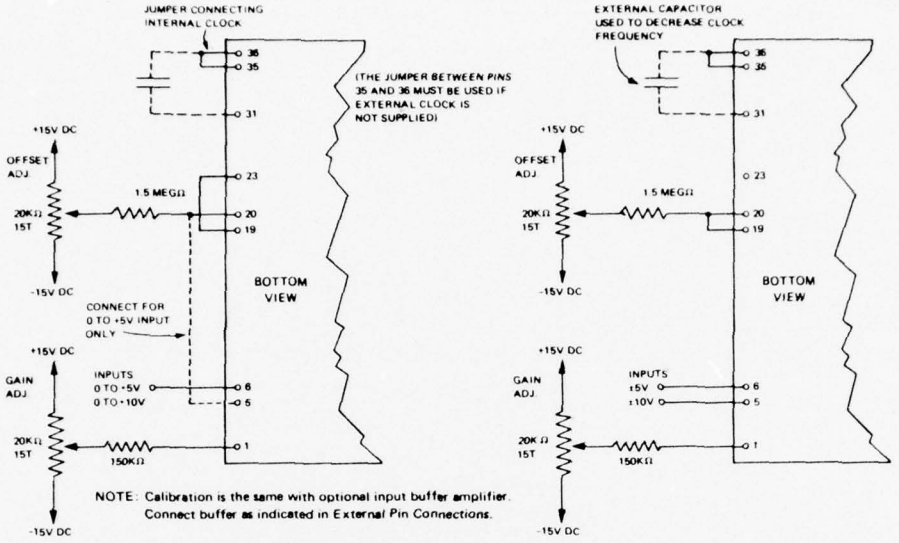
CONVERSION TIME USING EXTERNAL CAPACITOR

The external capacitor is connected between pins 31 and 36. Conversion time in the table is in microseconds and capacitor value is in picoferads.

Conversion Time Formula (approx.)		
*Conv. Time**	ADC-MA10B	ADC-MA12B
20 μsec.	C = 60(T-20μsec.)	C = 50 (T-20μsec.)
40 μsec.	C = 65(T-40μsec.)	C = 55(T-40μsec.)

*Maximum internal conversion rate when no external capacitor is used.

CALIBRATION CONNECTIONS



UNIPOLAR OPERATION (WITHOUT BUFFER)

BIPOLAR OPERATION (WITHOUT BUFFER)

CALIBRATION PROCEDURE

Gain and offset adjustments are accomplished as shown in the above diagram using the Calibration Table. The trimming potentiometers used should be 15 turn 100ppm/°C temperature coefficient cermet type units and are available from Datel Systems at $3.00 each. A pulse generator should be adjusted to give +5 volt pulses with 100 nsec. minimum duration and a spacing equal to or larger than the specified maximum conversion time (20 or 40 usec.). This generator should be connected to the "Start Convert" input. A precision voltage reference source should be connected to the selected analog input terminal.

Offset Adjustment: For unipolar operation set the output of the voltage reference source to zero plus 1/2 LSB. The value is shown in the Calibration Table. Adjust the offset trimming potentiometer until the LSB output flickers equally between logic "0" and logic "1". (Output between 000 . . . 000 and 000 . . . 001). For bipolar operation set the voltage reference source to minus full scale plus 1/2 LSB and make the same adjustment.

Gain Adjustment: Adjust the output of the voltage reference source to full scale minus 1 1/2 LSB. This value is also shown in the Calibration Table. Adjust gain trimming potentiometer until LSB output flickers equally between logic "0" and logic "1". (Output between 111 . . . 110 and 111 . . . 111).

CALIBRATION TABLE ADC-MA SERIES

	INPUT RANGE	ADJUSTMENT	INPUT VOLTAGE 10 BIT	INPUT VOLTAGE 12 BIT
UNIPOLAR	0 TO +5V	OFFSET	2.4 mV	0.61 mV
		GAIN	+4.9927V	+4.9982V
	0 TO +10V	OFFSET	4.9 mV	1.2 mV
		GAIN	+9.9854V	+9.9963V
BIPOLAR	±5V	OFFSET	-4.9951V	-4.9988V
		GAIN	+4.9854V	+4.9963V
	±10V	OFFSET	-9.9902V	-9.9976V
		GAIN	+9.9707V	+9.9927V

ORDERING INFORMATION

ADC-MA

NUMBER OF BITS AND CODING	WITH OR W/O HIGH Z BUFFER	CONVERSION TIME
10B = 10 BINARY BITS 12B = 12 BINARY BITS	1 = WITH 2 = WITHOUT	A = 40μSEC B = 20μSEC

ADC-MA10B1A 119

PRICES (1-9)

ADC-MA10B2A	$ 99.00	ADC-MA12B2A	$129.00
ADC-MA10B2B	$129.00	ADC-MA12B2B	$149.00

For optional internal high impedance buffer amplifier add $20.00 to price.

Mating Socket: DILS-2, 4 required @ $5.00 per pair
Trimming Potentiometers: TP20K $3.00 each (1-9)

DATEL SYSTEMS, INC. 1020 TURNPIKE STREET, CANTON, MASS 02021 TEL (617) 828-8000 TWX 710 348-0135 TELEX 924461

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

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8/74 BULLETIN AMA-L15408

APPENDIX C

READ-ONLY-MEMORY
TRUTH TABLES

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LWC DCU Card, D20 Harris H PROM 1-8256-5B (32 x 8)

Address		B7	PA(Y) B6	LA(Y) B5	CP B4	CPA3 B3	CPA2 B2	CPA1 B1	CPA0 B0	
0	(32			H	H	H		H	H	0
1				H		H		H	H	1
2				H		H		H	H	2
3				H	H	H	H			3
4	(36)			H		H	H			4
5				H		H	H			5
6				H	H	H	H		H	6
7				H		H	H		H	7
8	(40)			H		H	H		H	8
9				H	H	H	H	H		9
10				H		H	H	H		10
11				H		H	H	H		11
12	(44)			H	H	H	H	H	H	12
13		X								13
14		X								14
15			H		H					15
16	(48)		H							16
17			H							17
18			H		H				H	18
19			H						H	19
20	(52)		H						H	20
21			H		H			H		21
22			H					H		22
23			H					H		23
24	(56)		H		H			H	H	24
25			H					H	H	25
26			H					H	H	26
27		X								27
28	(60)	X								28
29		X								29
30		X								30
31	(63)	X								31

H ≡ High ≡ Logic One ≡ Programmed
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

DCU Card, C16 Harris H PROM 1-8256-5B (32 x 8)

Address		B7	PA(Y) B6	LA(Y) B5	CP B4	CPA3 B3	CPA2 B2	CPA1 B1	CPA0 B0	
0	X									0
1	X									1
2				H	H				H	2
3				H					H	3
4				H					H	4
5				H	H			H		5
6				H				H		6
7				H				H		7
8				H	H			H	H	8
9				H				H	H	9
10				H				H	H	10
11				H	H		H			11
12				H			H			12
13				H			H			13
14				H	H		H		H	14
15				H			H		H	15
16				H			H		H	16
17				H	H		H	H		17
18				H			H	H		18
19				H			H	H		19
20				H	H		H	H	H	20
21				H			H	H	H	21
22				H			H	H	H	22
23				H	H	H				23
24				H		H				24
25				H		H				25
26				H	H	H			H	26
27				H		H			H	27
28				H		H			H	28
29				H	H	H		H		29
30				H		H		H		30
31				H		H		H		31

H ≡ High ≡ Logic One ≡ Programmed
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

PROM Pattern for D9 and D10 on MIU Cards. H PROM 1-1024-5B

	HEX. DEC			
T.U	1248.1248			
	0.0000	16.0006	32.0012	48.0019
	0000.0000	0000.0110	1000.0100	1000.1001
	1.0000	17.0007	33.0013	49.0019
	0000.0000	0000.1110	1000.1100	1000.1001
	2.0001	18.0007	34.0013	50.0020
	0000.1000	0000.1110	1000.1100	0100.0000
	3.0001	19.0007	35.0014	51.0020
	0000.1000	0000.1110	1000.0010	0100.0000
	4.0002	20.0008	36.0014	52.0020
	0000.0100	0000.0001	1000.0010	0100.0000
	5.0002	21.0008	37.0014	53.0021
	0000.0100	0000.0001	1000.0010	0100.1000
	6.0002	22.0009	38.0015	54.0021
	0000.0100	0000.1001	1000.1010	0100.1000
	7.0003	23.0009	39.0015	55.0021
	0000.1100	0000.1001	1000.1010	0100.1000
	8.0003	24.0009	40.0016	56.0022
	0000.1100	0000.1001	1000.0110	0100.0100
	9.0004	25.0010	41.0016	57.0022
	0000.0010	1000.0000	1000.0110	0100.0100
	10.0004	26.0010	42.0016	58.0023
	0000.0010	1000.0000	1000.0110	0100.1100
	11.0004	27.0011	43.0017	59.0023
	0000.0010	1000.1000	1000.1110	0100.1100
	12.0005	28.0011	44.0017	60.0023
	0000.1010	1000.1000	1000.1110	0100.1100
	13.0005	29.0011	45.0018	61.0024
	0000.1010	1000.1000	1000.0001	0100.0010
	14.0005	30.0012	46.0018	62.0024
	0000.1010	1000.0100	1000.0001	0100.0010
	15.0006	31.0012	47.0018	63.0025
	0000.0110	1000.0100	1000.0001	0100.1010

Decimal Output

Decimal PROM Address

$O_3O_2O_1O_0$ Outputs of D10 PROM O=Low=Program

$O_3O_2O_1O_0$ Outputs of D9 PROM O=Low=Program

64.0025	80.0031	96.0037	112.0044
0100.1010	1100.1000	1100.1110	0010.0010
65.0025	81.0032	97.0038	113.0044
0100.1010	1100.0100	1100.0001	0010.0010
66.0026	82.0032	98.0038	114.0045
0100.0110	1100.0100	1100.0001	0010.1010
67.0026	83.0032	99.0039	115.0045
0100.0110	1100.0100	1100.1001	0010.1010
68.0027	84.0033	100.0039	116.0045
0100.1110	1100.1100	1100.1001	0010.1010
69.0027	85.0033	101.0039	117.0046
0100.1110	1100.1100	1100.1001	0010.0110
70.0027	86.0034	102.0040	118.0046
0100.1110	1100.0010	0010.0000	0010.0110
71.0028	87.0034	103.0040	119.0046
0100.0001	1100.0010	0010.0000	0010.0110
72.0028	88.0034	104.0041	120.0047
0100.0001	1100.0010	0010.1000	0010.1110
73.0029	89.0035	105.0041	121.0047
0100.1001	1100.1010	0010.1000	0010.1110
74.0029	90.0035	106.0041	122.0048
0100.1001	1100.1010	0010.1000	0010.0001
75.0029	91.0036	107.0042	123.0048
0100.1001	1100.0110	0010.0100	0010.0001
76.0030	92.0036	108.0042	124.0048
1100.0000	1100.0110	0010.0100	0010.0001
77.0030	93.0036	109.0043	125.0049
1100.0000	1100.0110	0010.1100	0010.1001
78.0030	94.0037	110.0043	126.0049
1100.0000	1100.1110	0010.1100	0010.1001
79.0031	95.0037	111.0043	127.0050
1100.1000	1100.1110	0010.1100	1010.0000

128.0050	144.0056	160.0062	176.0069
1010.0000	1010.0110	0110.0100	0110.1001
129.0050	145.0057	161.0063	177.0069
1010.0000	1010.1110	0110.1100	0110.1001
130.0051	146.0057	162.0063	178.0070
1010.1000	1010.1110	0110.1100	1110.0000
131.0051	147.0057	163.0064	179.0070
1010.1000	1010.1110	0110.0010	1110.0000
132.0052	148.0058	164.0064	180.0070
1010.0100	1010.0001	0110.0010	1110.0000
133.0052	149.0058	165.0064	181.0071
1010.0100	1010.0001	0110.0010	1110.1000
134.0052	150.0059	166.0065	182.0071
1010.0100	1010.1001	0110.1010	1110.1000
135.0053	151.0059	167.0065	183.0071
1010.1100	1010.1001	0110.1010	1110.1000
136.0053	152.0059	168.0066	184.0072
1010.1100	1010.1001	0110.0110	1110.0100
137.0054	153.0060	169.0066	185.0072
1010.0010	0110.0000	0110.0110	1110.0100
138.0054	154.0060	170.0066	186.0073
1010.0010	0110.0000	0110.0110	1110.1100
139.0054	155.0061	171.0067	187.0073
1010.0010	0110.1000	0110.1110	1110.1100
140.0055	156.0061	172.0067	188.0073
1010.1010	0110.1000	0110.1110	1110.1100
141.0055	157.0061	173.0068	189.0074
1010.1010	0110.1000	0110.0001	1110.0010
142.0055	158.0062	174.0068	190.0074
1010.1010	0110.0100	0110.0001	1110.0010
143.0056	159.0062	175.0068	191.0075
1010.0110	0110.0100	0110.0001	1110.1010

192.0075	208.0081	224.0087	240.0094
1110.1010	0001.1000	0001.1110	1001.0010
193.0075	209.0082	225.0088	241.0094
1110.1010	0001.0100	0001.0001	1001.0010
194.0076	210.0082	226.0088	242.0095
1110.0110	0001.0100	0001.0001	1001.1010
195.0076	211.0082	227.0089	243.0095
1110.0110	0001.0100	0001.1001	1001.1010
196.0077	212.0083	228.0089	244.0095
1110.1110	0001.1100	0001.1001	1001.1010
197.0077	213.0083	229.0089	245.0096
1110.1110	0001.1100	0001.1001	1001.0110
198.0077	214.0084	230.0090	246.0096
1110.1110	0001.0010	1001.0000	1001.0110
199.0078	215.0084	231.0090	247.0096
1110.0001	0001.0010	1001.0000	1001.0110
200.0078	216.0084	232.0091	248.0097
1110.0001	0001.0010	1001.1000	1001.1110
201.0079	217.0085	233.0091	249.0097
1110.1001	0001.1010	1001.1000	1001.1110
202.0079	218.0085	234.0091	250.0098
1110.1001	0001.1010	1001.1000	1001.0001
203.0079	219.0086	235.0092	251.0098
1110.1001	0001.0110	1001.0100	1001.0001
204.0080	220.0086	236.0092	252.0098
0001.0000	0001.0110	1001.0100	1001.0001
205.0080	221.0086	237.0093	253.0099
0001.0000	0001.0110	1001.1100	1001.1001
206.0080	222.0087	238.0093	254.0099
0001.0000	0001.1110	1001.1100	1001.1001
207.0081	223.0087	239.0093	255.0100
0001.1000	0001.1110	1001.1100	0101.0000

AD-A043 066 RAYTHEON CO WAYLAND MASS F/G 17/9
SCAN CONVERTER FOR LIQUID WATER CONTENT ANALYZER.(U)
JUL 75 A J JAGODNIK, L R NOVICK, J H TURNER DNA001-75-C-0050
UNCLASSIFIED ER75-4332 DNA-4130F NL

2 OF 2
AD
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END
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9-77
DDC

Coordinate Converter Altitude Error Correction (Card 2)

	F30				F26 LSB			
Input Address	D	C	B	A	Q	R	S	T
0-27	0	0	0	0	0	0	0	0
28-38	0	0	0	0	0	0	0	1
39-47	0	0	0	0	0	0	1	0
48-55	0	0	0	0	0	0	1	1
56-62	0	0	0	0	0	1	0	0
63-68	0	0	0	0	0	1	0	1
68-74	0	0	0	0	0	1	1	0
75-79	0	0	0	0	0	1	1	1
80	0	0	0	0	1	0	0	0
81	0	0	0	0	1	0	0	0
82	0	0	0	0	1	0	0	0
83	0	0	0	0	1	0	0	0
84	0	0	0	0	1	0	0	1
85	0	0	0	0	1	0	0	1
86	0	0	0	0	1	0	0	1
87	0	0	0	0	1	0	0	1
88	0	0	0	0	1	0	0	1
89	0	0	0	0	1	0	1	0
90	0	0	0	0	1	0	1	0
91	0	0	0	0	1	0	1	0
92	0	0	0	0	1	0	1	0
93	0	0	0	0	1	0	1	1
94	0	0	0	0	1	0	1	1
95	0	0	0	0	1	0	1	1
96	0	0	0	0	1	0	1	1
97	0	0	0	0	1	0	1	1
98	0	0	0	0	1	1	0	0
99	0	0	0	0	1	1	0	0
100	0	0	0	0	1	1	0	0
101	0	0	0	0	1	1	0	1
102	0	0	0	0	1	1	0	1

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

Input Address	F30 D	C	B	A	F26 LSB Q	R	S	T
103	0	0	0	0	1	1	0	1
104	0	0	0	0	1	1	0	1
105	0	0	0	0	1	1	1	0
106	0	0	0	0	1	1	1	0
107	0	0	0	0	1	1	1	0
108	0	0	0	0	1	1	1	1
109	0	0	0	0	1	1	1	1
110	0	0	0	0	1	1	1	1
111	0	0	0	0	1	1	1	1
112	0	0	0	1	0	0	0	0
113	0	0	0	1	0	0	0	0
114	0	0	0	1	0	0	0	0
115	0	0	0	1	0	0	0	0
116	0	0	0	1	0	0	0	1
117	0	0	0	1	0	0	0	1
118	0	0	0	1	0	0	0	1
119	0	0	0	1	0	0	1	0
120	0	0	0	1	0	0	1	0
121	0	0	0	1	0	0	1	0
122	0	0	0	1	0	0	1	1
123	0	0	0	1	0	0	1	1
124	0	0	0	1	0	0	1	1
125	0	0	0	1	0	1	0	0
126	0	0	0	1	0	1	0	0
127	0	0	0	1	0	1	0	0
128	0	0	0	1	0	1	0	1
129	0	0	0	1	0	1	0	1
130	0	0	0	1	0	1	0	1
131	0	0	0	1	0	1	0	1
132	0	0	0	1	0	1	1	0
133	0	0	0	1	0	1	1	0

Input Address	F30 D	C	B	A	F26 LSB Q	R	S	T
134	0	0	0	1	0	1	1	0
135	0	0	0	1	0	1	1	1
136	0	0	0	1	0	1	1	1
137	0	0	0	1	1	0	0	0
138	0	0	0	1	1	0	0	0
139	0	0	0	1	1	0	0	0
140	0	0	0	1	1	0	0	1
141	0	0	0	1	1	0	0	1
142	0	0	0	1	1	0	1	0
143	0	0	0	1	1	0	1	0
144	0	0	0	1	1	0	1	0
145	0	0	0	1	1	0	1	1
146	0	0	0	1	1	0	1	1
147	0	0	0	1	1	0	1	1
148	0	0	0	1	1	1	0	0
149	0	0	0	1	1	1	0	0
150	0	0	0	1	1	1	0	1
151	0	0	0	1	1	1	0	1
152	0	0	0	1	1	1	0	1
153	0	0	0	1	1	1	1	0
154	0	0	0	1	1	1	1	0
155	0	0	0	1	1	1	1	0
156	0	0	0	1	1	1	1	1
157	0	0	0	1	0	0	0	0
158	0	0	1	0	0	0	0	0
159	0	0	1	0	0	0	0	0
160	0	0	1	0	0	0	0	0
161	0	0	1	0	0	0	0	1
162	0	0	1	0	0	0	0	1
163	0	0	1	0	0	0	1	0

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

Input Address	F30 D	C	B	A	F26 LSB Q	$\overline{R}$	$\overline{S}$	T
164	0	0	1	0	0	0	1	0
165	0	0	1	0	0	0	1	0
166	0	0	1	0	0	0	1	1
167	0	0	1	0	0	0	1	1
168	0	0	1	0	0	1	0	0
169	0	0	1	0	0	1	0	0
170	0	0	1	0	0	1	0	1
171	0	0	1	0	0	1	0	1
172	0	0	1	0	0	1	0	1
173	0	0	1	0	0	1	1	0
174	0	0	1	0	0	1	1	0
175	0	0	1	0	0	1	1	1
176	0	0	1	0	0	1	1	1
177	0	0	1	0	1	0	0	0
178	0	0	1	0	1	0	0	0
179	0	0	1	0	1	0	0	1
180	0	0	1	0	1	0	0	1
181	0	0	1	0	1	0	1	0
182	0	0	1	0	1	0	1	0
183	0	0	1	0	1	0	1	0
184	0	0	1	0	1	0	1	1
185	0	0	1	0	1	0	1	1
186	0	0	1	0	1	1	0	0
187	0	0	1	0	1	1	0	0
188	0	0	1	0	1	1	0	1
189	0	0	1	0	1	1	0	1
190	0	0	1	0	1	1	1	0
191	0	0	1	0	1	1	1	0
192	0	0	1	0	1	1	1	1
193	0	0	1	0	1	1	1	1
194	0	0	1	1	0	0	0	0

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

	F30				F26 LSB			
Input Address	D	C	B	A	Q	R	S	T
195	0	0	1	1	0	0	0	0
196	0	0	1	1	0	0	0	1
197	0	0	1	1	0	0	0	1
198	0	0	1	1	0	0	1	0
199	0	0	1	1	0	0	1	0
200	0	0	1	1	0	0	1	1
201	0	0	1	1	0	0	1	1
202	0	0	1	1	0	1	0	0
203	0	0	1	1	0	1	0	0
204	0	0	1	1	0	1	0	1
205	0	0	1	1	0	1	0	1
206	0	0	1	1	0	1	1	0
207	0	0	1	1	0	1	1	0
208	0	0	1	1	0	1	1	1
209	0	0	1	1	0	1	1	1
210	0	0	1	1	1	0	0	0
211	0	0	1	1	1	0	0	0
212	0	0	1	1	1	0	0	1
213	0	0	1	1	1	0	1	0
214	0	0	1	1	1	0	1	0
215	0	0	1	1	1	0	1	1
216	0	0	1	1	1	0	1	1
217	0	0	1	1	1	1	0	0
218	0	0	1	1	1	1	0	0
219	0	0	1	1	1	1	0	1
220	0	0	1	1	1	1	0	1
221	0	0	1	1	1	1	1	0
222	0	0	1	1	1	1	1	1
223	0	0	1	1	1	1	1	1

Input Address	F30 D	C	B	A	F26 LSB Q	R	S	T
224	0	1	0	0	0	0	0	0
225	0	1	0	0	0	0	0	1
226	0	1	0	0	0	0	0	1
227	0	1	0	0	0	0	1	0
228	0	1	0	0	0	0	1	0
229	0	1	0	0	0	0	1	1
230	0	1	0	0	0	0	1	1
231	0	1	0	0	0	1	0	0
232	0	1	0	0	0	1	0	0
233	0	1	0	0	0	1	0	1
234	0	1	0	0	0	1	0	1
235	0	1	0	0	0	1	1	0
236	0	1	0	0	0	1	1	0
237	0	1	0	0	0	1	1	1
238	0	1	0	0	1	0	0	0
239	0	1	0	0	1	0	0	1
240	0	1	0	0	1	0	0	1
241	0	1	0	0	1	0	1	0
242	0	1	0	0	1	0	1	0
243	0	1	0	0	1	0	1	1
244	0	1	0	0	1	1	0	0
245	0	1	0	0	1	1	0	0
246	0	1	0	0	1	1	0	1
247	0	1	0	0	1	1	1	0
248	0	1	0	0	1	1	1	0
249	0	1	0	0	1	1	1	1
250	0	1	0	1	0	0	0	0
251	0	1	0	1	0	0	0	0

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

	F30				F26				LSB
Input Address	D	C	B	A	Q	R	S	T	
252	0	1	0	1	0	0	0	1	
253	0	1	0	1	0	0	1	0	
254	0	1	0	1	0	0	1	0	
255	0	1	0	1	0	0	1	1	

5 X 7 CHARACTER FONT*

MM6055

A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

ASCII INPUT ADDRESS	$B_1\ B_2\ B_3$ $A_3\ A_4\ A_5$ 000	$A_3\ A_4\ A_5$ 100	$A_3\ A_4\ A_5$ 010	$A_3\ A_4\ A_5$ 110	$A_3\ A_4\ A_5$ 001	$A_3\ A_4\ A_5$ 101	$A_3\ A_4\ A_5$ 011	$A_3\ A_4\ A_5$ 111
$B_4\ B_5\ B_6$* $A_6\ A_7\ A_8$ 000	@	A	B	C	D	E	F	G
$A_6\ A_7\ A_8$ 100	H	I	J	K	L	M	N	O
$A_6\ A_7\ A_8$ 010	P	Q	R	S	T	U	V	W
$A_6\ A_7\ A_8$ 110	X	Y	Z	[	\	]	^	_
$A_6\ A_7\ A_8$ 001	!	"	#	$	%	&	'	
$A_6\ A_7\ A_8$ 101	(	)	*	+	,	-	.	/
$A_6\ A_7\ A_8$ 011	0	1	2	3	4	5	6	7
$A_6\ A_7\ A_8$ 111	8	9	:	;	<	=	>	?

*FROM THE USASCII CODE $A_8\ B_7\ \overline{B_6}$

DDI Card, B23 Signetics 82S123 (32 x 8)

					Unconditional Next State				
	MEISB	MEISA	SATNE	CNSS	UNSD	UNSC	UNSB	$\overline{\text{UNSA}}$	
Address	B7	B6	B5	B4	B3	B2	B1	B0	
0		H		H					0
1		H	H	H				H	1
2	H						H		2
3	H					H		H	3
4	H			H			H		4
5	H	H					H	H	5
6	H						H	H	6
7			H		H			H	7
8	H	H					H	H	8
9	H	H			H	H	H		9
10	H	H			H				10
11		H			H		H	H	11
12									12
13									13
									14
	H	H			H	H			15
		H							16
17		H					H	H	17
18		H					H		18
19		H				H		H	19
20		H		H			H		20
21	H	H					H	H	21
22		H					H	H	22
23									23
24									24
25									25
26									26
27									27
28									28
29									29
30									30
31									31

H ≡ High ≡ Logic One ≡ Programmed
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

DDI Card, B29 Signetics 82S123 (32 x 8)

					Conditional Next State				
				MWGI	CNSD	CNSC	CNSB	$\overline{\text{CNSA}}$	
Address	B7	B6	B5	B4	B3	B2	B1	B0	
0							H	H	0
1							H	H	1
2							H	H	2
3									3
4							H	H	4
5							H	H	5
6									6
7									7
8							H	H	8
9							H	H	9
10							H	H	10
11							H	H	11
12									12
13							H	H	13
14					H		H		14
15									15
16				H			H		16
17				H			H	H	17
18				H		H	H	H	18
19									19
20						H			20
21						H	H		21
22									22
23									23
24									24
25									25
26									26
27									27
28									28
29									29
30									30
31									31

H ≡ High ≡ Logic One ≡ Programmed
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

APPENDIX D

MEMORANDA

"Display Data Port Programming", (A. J. Jagodnik memo #AJJ-21)

"Scan Converter Drawing List", (A. J. Jagodnik memo #AJJ-26)

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RAYTHEON

FORM 10-0557 (9-65) BOND

DIVISION Equipment
Operation ADL
Department ADL

		Classification	Unclassified
		Contract No.	DNA001-75-C-0050
		Distribution	As Listed
To	J. H. Turner	File No.	-
From	A. J. Jagodnik, Jr.	Memo No.	AJJ-21
Subject	Display Data Port Programming	Date	26 March 1975

Reference: 1. AJJ-17, "Design Plan for the Display Data Interface of the Liquid Water Content Analyzer System," dated 17 Dec. 1974

2. Scan Converter and Contour Refresh Memory Equipment Information Report, June 1974.

The Display Data Interface design plan contains sections entitled "Operation of the LWCA Control Panel" and "Hardware/Software Interaction". The purpose of this memo is to expand upon the contents of these sections, based upon the existing hardware which differs slightly from that originally planned. The programmer should find here information needed to write assembly language programs for the purpose of communicating between the scan converter color displays and the analyzer (Interdata 7/32 minicomputer).

The first section consists of operating instructions for the LWCA control panel and scan conversion processor, while subsequent sections discuss addressing conventions and each of the three basic types of data transfers: Write Display Memory, Read Display Memory, and Cursor Data Entry. Programming examples are also included.

Operation of the LWCA Scan Converter

Scan converter operation is covered in Reference 2; the information presented here is intended to serve as a supplement and covers operation with the LWCA Control Panel illustrated in Figure 1. Except for the ERASE DISPLAY buttons, all of the switches on the control panel also serve as indicators controlled by their state and/or the DDI (Display Data Interface) within the scan converter. An exception is the control labeled DATA SOURCE TAPE which functions only as an indicator to denote the fact that the Precision Digital Video Integrator has been set to accept data from Mag Tape for display on the scan converter.

The LWCA TO DISPLAY controls, when lit, indicate that write and/or read data transfers are enabled in the hardware. They are affected by several controls on the Scan Conversion Processor as indicated in Table 1. The state of these controls can be uniquely determined from the status byte of the Display Data Port which has been assigned device number X'8B'.

Table 1

Scan Conv. Controls		LWCA to Display Switches		LWCA to Display Indicators		Device X'8B' Status Byte
Mode	Memory Control Store Video	Write On/Off	Read On/Off	Write On/Off	Read On/Off	0 1 2 3 4 5 6 7
A	All OFF	X	X	Lit	Lit	x x x 1 x 1 1 1
A	One or More ON	X	X	Dark	Lit	x x x 1 x 0 1 0
Not A	All OFF	Off	Off	Dark	Dark	x x x 0 x 0 0 1
		Off	On	Dark	Lit	x x x 0 x 0 1 1
		On	Off	Lit	Dark	x x x 0 x 1 0 1
		On	On	Lit	Lit	x x x 0 x 1 1 1
Not A	One or More ON	X	Off	Dark	Dark	x x x 0 x 0 0 0
			On	Dark	Lit	x x x 0 x 0 1 0

X = don't care

The scan converter will operate normally in the following mode switch positions: PPI, RHI, CAPPI and B. If the appropriate LWCA TO DISPLAY indicator is lit, the analyzer can read or write into the display memories. In mode switch position A, the necessary conditions for LWCA operation are set up; these are:

(1) Scan converter in RHI mode,

(2) LWCA TO DISPLAY READ indicator forced ON

(3) LWCA TO DISPLAY WRITE indicator forced ON if the converter memory buss is available (all STORE VIDEO switches OFF).

The scan converter ERASE VIDEO buttons used in normal operation do not erase the entire screen; the contour threshold legend area is left unchanged. In addition, a mask obscures from view certain areas within the ancillary data portion of the screen. These areas contain coded information available to the analyzer and needed by the contouring hardware. The ERASE DISPLAY buttons on the LWCA CONTROL PANEL not only erase the entire display, but also inhibit the mask so that the entire screen is available to display information from the processor. The mask and the legend are restored when the operator actuates the corresponding STORE THRESHOLDS button on the scan conversion processor.

The cursor can be made to appear in any display by depressing the appropriate CURSOR ON/OFF switch; the on state is indicated by illumination of the switch. The cursor, a blinking single point on the display, can be located anywhere on the screen by means of the CURSOR POSITION trackball.[1] The cursor changes color as a function of its surroundings so as to remain visible. During normal scan converter operation, the mask will obscure the cursor. If the cursor cannot be found, the following property may be useful: along the Top and Left edges of the display, the cursor will stop even if the trackball is rotated too far. At the bottom edge, the cursor disappears. When moved beyond the right edge, it reappears at the left where it finally stops about an inch from that edge; however, if the SEND DATA button were pressed with the cursor in such a position, the address would be wrong.

The color/intensity code covered by the cursor, as well as its coordinates, can be entered into the analyzer by pushing the appropriate SEND DATA button. The corresponding cursor must be switched-on for this action to be recognized. The SEND DATA switch will light when depressed, if the DDI control logic is in the proper state, and will extinguish about one-half second after the resulting interrupt has been serviced by the analyzer.[1] Pressing the INI button on the analyzer console should always turn off any SEND DATA indicators which are lit for whatever reason.

Display Conventions

The four display channels, numbered one through four, contain independent memories. Each memory is organized so that its address corresponds with the (X, Y) coordinates within a 248 by 320 point matrix as indicated in Figure 2. Each point can take on one of sixteen color/intensity combinations as listed in that figure. (The observed colors are a function of the settings of an array of switches in each memory interface unit; those colors listed correspond to the settings indicated in Figure 4-11 of Ref. 2.) Note that color 15 has a non-over write property: once this code occupies a point, the only way the color code at that point can be changed is by erasure.

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1. If any SEND DATA indicator is lit, no cursor will respond to the trackball.

The ancillary data area has significance only in normal scan converter operation; its outline is indicated in Figure 2, while the details of its contents appear in Figure 3. Information necessary for interpretation of the radar video data portion of the display (scaling, origin location, time, contour thresholds, and antenna angle) is obtainable by reading the four-bit codes in the patches indicated. Each of these patches contains the same four-bit code at all addresses within it. Most of the code patches have dimensions of 5 x 4 points (the same as the color patches) except for the origin location and scaling codes which are only 5 x 1. In either case, it is only necessary to read one point per patch, unless some sort of error correcting scheme is implemented to make use of the redundancy.

Points written as color 15 by a normally operating scan converter (not through the display data port) within the ancillary data area do not have the non-overwrite property. Any address in the ancillary data area which is not occupied by a 4 x 5 patch or an 8 x 5 character can be used for storage of a 4-bit word (e.g., to "mark" a stored video image) except for the 8 x 5 area under each color patch. Only the characters and color patches are displayed; everything else in the ancillary data area is masked. Again, the entire display area is erased (changed to color zero) and the mask is inhibited when an ERASE DISPLAY button is pushed, the entire area is now available to accept data from the analyzer.

General Comments on the Display Data Port

The hardware which comprises the display data port controller consists of two parts: an Interdata Universal Logic Interface (ULI) and a Raytheon-designed Display Data Interface (DDI). The ULI responds to device address X'8B' and contains interrupt and byte/halfword logic controlled by bits 0, 1 and 2 of the command byte (see Figure 4, note 2). Bit 2 should always be zero since the display data port operates only in the byte mode. Bits 0 and 1 affect interrupts in the following way: 01-interrupts enabled; 10-interrupts disabled but queued; 11-interrupts disarmed (neither accepted nor queued); 00-previous interrupt state unchanged. The ULI does not affect any bits in the status byte.

The DDI contains control logic which is described by the state diagram in Figure 4. Much of the notation here will not be of concern to the programmer. It is sufficient to note that state transitions are typically caused by execution of the 7/32 I/O instruction listed before the comment under each transition, or by a hardware-generated interrupt. Operation of the DDI control logic depends on the state of bits 4, 5 and 6 of the command byte as tabulated at the lower right of Figure 4. Also located there is a definition of the status byte, of which bits 3 through 7 are used.

Write Display Memory

Three distinct types of write operations which might be useful in various situations are supported in the DDI control logic. Controlled by bits 4, 5 and 6 of the command byte (Figure 4), they include:

(1) 0 0 0 - Write single point or multiple points the same color. The first write instruction transfers S_A, X_{AM} and color code, while succeeding pairs of instructions transfer (X_A, Y_A). The notation used here is explained in Figure 2; and the relationship to the Interdata bit numbers can be determined from Table 2.[2] This type of transfer might be useful where many points of the same color are to be plotted and it is not convenient to re-write S_A, X_{AM} and the color code for each point. An example is listed in Table 2. After the initial write instruction, the following pairs correspond to halfwords so that a halfword table containing (X_A, Y_A) values could be easily accessed sequentially using a write block instruction.

(2) 0 0 1 - Write single point or multiple points different colors. This sequence operates as the one described above, except that after the Y_A transfer, the next instruction transfers another number for S_A, X_{AM} and color.

(3) 0 1 0 - Write multiple points, fullword boundaries. This sequence operates as the one described above, except that after the Y_A transfer, the next instruction transfers nothing (see Figure 4, state W4), while the one following it transfers another number for S_A, X_{AM}, and color. This type of operation is intended for sequentially writing from fullword tables where each fullword contains S_A, X_{AM}, COLOR, X_A and Y_A for one point.

The Scan Converter, although it has an independent memory for each display, shares a memory address buss among the four display channels. When one or more STORE VIDEO switches is on, this buss is not available to the display data port and the write display memory operation is disabled in the hardware. It is also disabled for certain other switch settings as indicated in Table 1. Whenever the write operation is disabled, status bit 5 is zero. Before a write operation, it is good practice to check status to determine that bit 5 is one, although nothing will happen if a write is attempted, because the operation is disabled in the hardware. Status bit 4 should be checked to make sure it is zero; this bit indicates that a cursor data transfer is in progress and that the display data port is not available.

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2. See page 13 for table.

Read Display Memory

There are two types of read operations, depending on whether or not the scan converter memory buss is available. If the buss is available (all STORE VIDEO switches off; status bit 7 = 1), then a normal read, which operates in much the same way as the write display memory transfer described in the preceding section, can be executed. Otherwise, the process must be a slow read, which involves an interrupt service routine. Both types of read operations are inhibited if the read indicator is not lit (status bit 6 = 0, see Table 1).

Read Display Memory -- Normal

An example of this type of data transfer appears in Table 2. First, the status is sensed to ensure that the memory buss is available, the read indicator is on, and that no cursor data entry is in progress. Next, the proper command byte is output to device X'8B' and S_A, X_{AM}, X_A and Y_A are transferred just as for the write operation. At this point, a delay of at least six μsec; (for example, four BTCR 0, 0 (0200) instructions) must be executed so that the hardware is sure to have the required data ready. Lesser delays might work but have not been tried. Next, a read instruction is executed; the 4-bit color code appears in the four least significant bits of the second operand. Finally, a command byte can be output to leave the control logic in state I.

Read Display Memory -- Slow

If, in the preceding section, status bit 7 had been found to be zero, then a slow-read operation must be used. An example is found in Table 2. Steps 0 through 6 are the same as for a normal read, except that interrupts are enabled. The control logic, after step 6, ends up in state SR4 (see Figure 4) where it waits for an interrupt. This wait could last as long as 16 milliseconds and ends when the DDI has obtained data. Other processing can be executed during this wait interval. When the interrupt occurs, a simple interrupt service routine consisting of steps 8 through 10 of the example in Table 2 completes the operation.[3]

---

3. Details on interrupt processing can be found in Interdata Documents:

Model 7/32 Reference Manual, Pub. No. 29 - 399R02, Section 2.4
32-Bit Series " " Pub. No. 29 - 365R01, Chapter 7.

Cursor Data Entry

As does the slow-read operation, the cursor data entry makes use of an interrupt service routine and a data acquisition method which does not require the scan converter memory buss. There is, however, no long delay because, following the pressing of a SEND DATA button, no interrupt is generated until after all required data has been obtained. The cursor data entry requires that the DDI control logic be in state I and that the ULI has interrupts enabled; hence, step 0 of the example in Table 2. The remainder of this example is an interrupt service routine which checks the status to see that the interrupt was caused by a cursor data entry, outputs a command byte to disarm further interrupts, then transfers S_C, X_{CM}, X_C and Y_C to the second operand locations of the three read instructions. Finally, the control logic is returned to state I, interrupts are again enabled, and the original program status word is restored.

Programming Examples

The SCPLT subroutine listed in Table 3 was used in the Liquid Water Content display subroutine to take care of getting the ninth bit of X in the right place and to execute the necessary IO instructions for writing one point. The inputs were left in registers and the subroutine was called using BAL F, SCPLT. Because no other data transfer modes were being used in this application, the command byte was programmed to always leave the ULI with interrupts disarmed. SCPLT is called many times during the main program; it always leaves the control logic in state I. But in order to ensure that the very first point is plotted, the following instructions should be executed before SCPLT is called for the first time:

```
LHI     B, X'8B'
OC      B, DDICMD2
```

Thus forcing the control logic to state I.

Another way to structure SCPLT would put what is now line 72 (Table 3) after line 58, thus SCPLT would not leave the control logic in state I, but would force it there first each time it is called. A third method would involve forcing the control logic to state I only once, then not using any OC instructions at all in SCPLT itself. This method is the simplest and fastest, but depends on nothing disturbing the control logic between calls of SCPLT, where it would be left in state RW1 (Figure 4).

Table 4 lists a program to copy one display to another. It was written directly in machine language as a diagnostic to test the hardware, which it does very well since it accesses all display memory locations and exercises the read circuitry in the source display and the write circuitry in the output display. A good test of the hardware would consist of the following:

1) Store a test pattern or radar data image which contains all 16 colors in display 1; erase displays 2, 3 and 4.

2) Put Q = 0 0 0 0 and P = 0 0 2 0 into the program and run. Displays 1 and 2 should now be identical.

3) Put Q = 0 0 2 0 and P = 0 0 4 0 into the program and run. Displays 1, 2 and 3 should now be identical.

4) Put Q = 0 0 4 0 and P = 0 0 6 0 into the program and run. All displays should be identical.

5) Erase display 1.

6) Put Q = 0 0 6 0 and P - 0 0 0 0 into the program and run. All displays should again be identical.

Table 4 is shown set up for a normal read; to exercise the slow read, follow the directions at the end of the table. Execution of the copy program takes about three seconds in the normal read mode, and five seconds in the slow read mode. If the full 16 milliseconds delay were incurred at every point in the slow read mode, the program would require over 21 minutes for execution. The reason it only takes 5 seconds lies in the format adopted for scanning in the copy program. Examination of Table 4 will reveal that the copy process is basically accomplished by reading one point from the source display, writing that data into the same address in the output display, incrementing by one to the next Y address, then repeating. When Y reaches 248, X is incremented by one and Y goes back to zero. The fact that Y changes more rapdily then X is the key to the reason for the unexpectedly fast performance in the slow read mode. The average delay is only about 67 microseconds because of the way in which the copy-program scan interacts with the display raster-scan.

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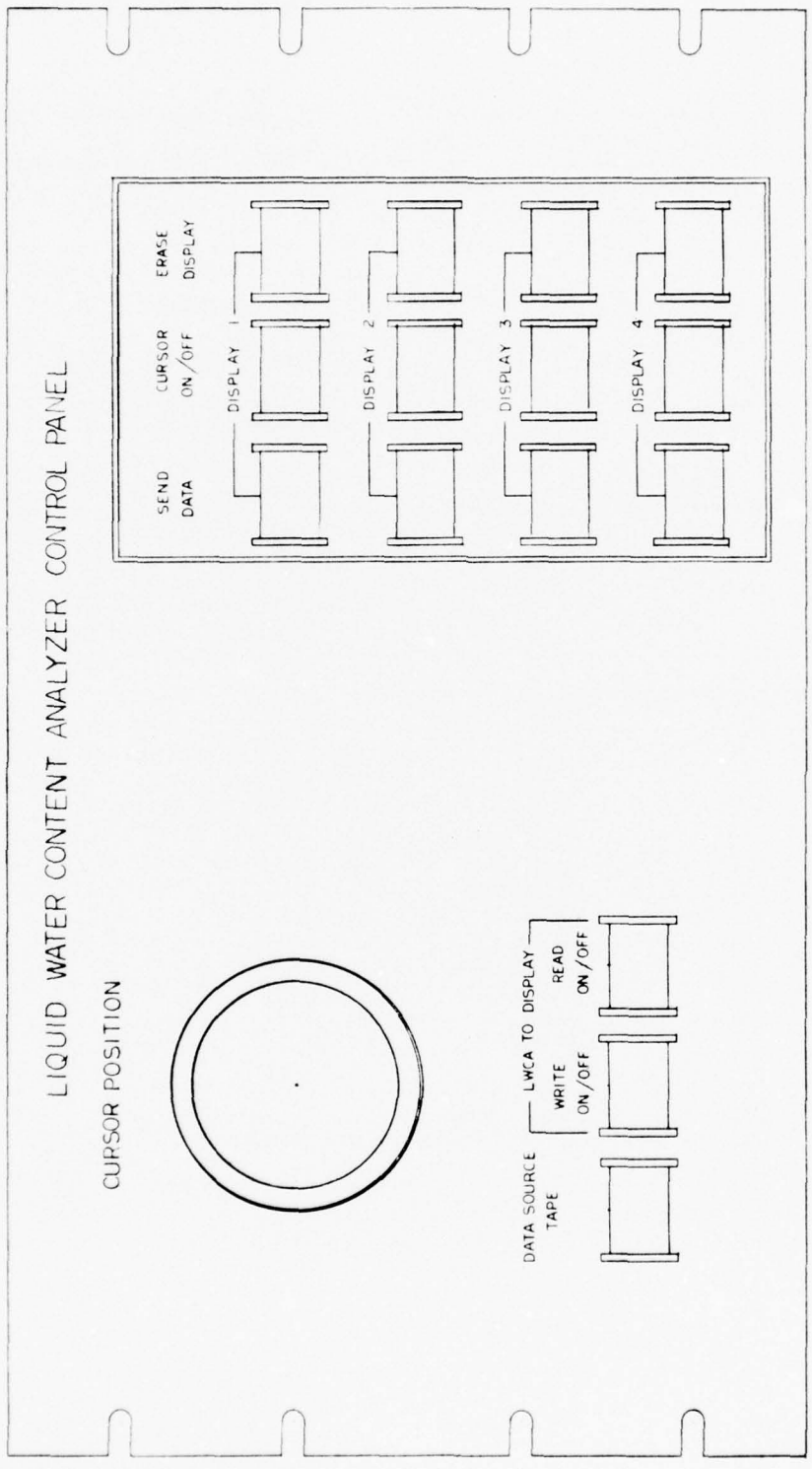
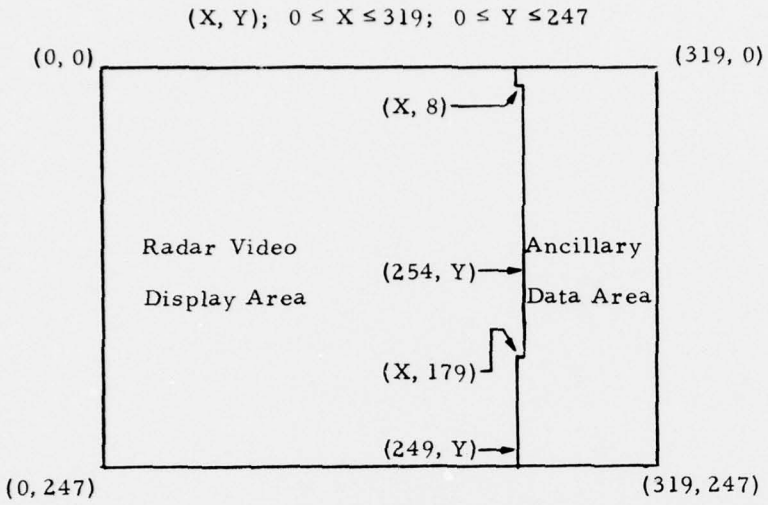


Figure 1. Control Panel



Represented by 8-bit codes:

Display coord. - X_A, Y_A

Cursor coord. - X_C, Y_C

Represented by 1-bit code:

Display coord. - X_{AM}

Cursor coord. - X_{CM}

(The most significant bit of X)

Represented by 2-bit codes:

Display select - S_A

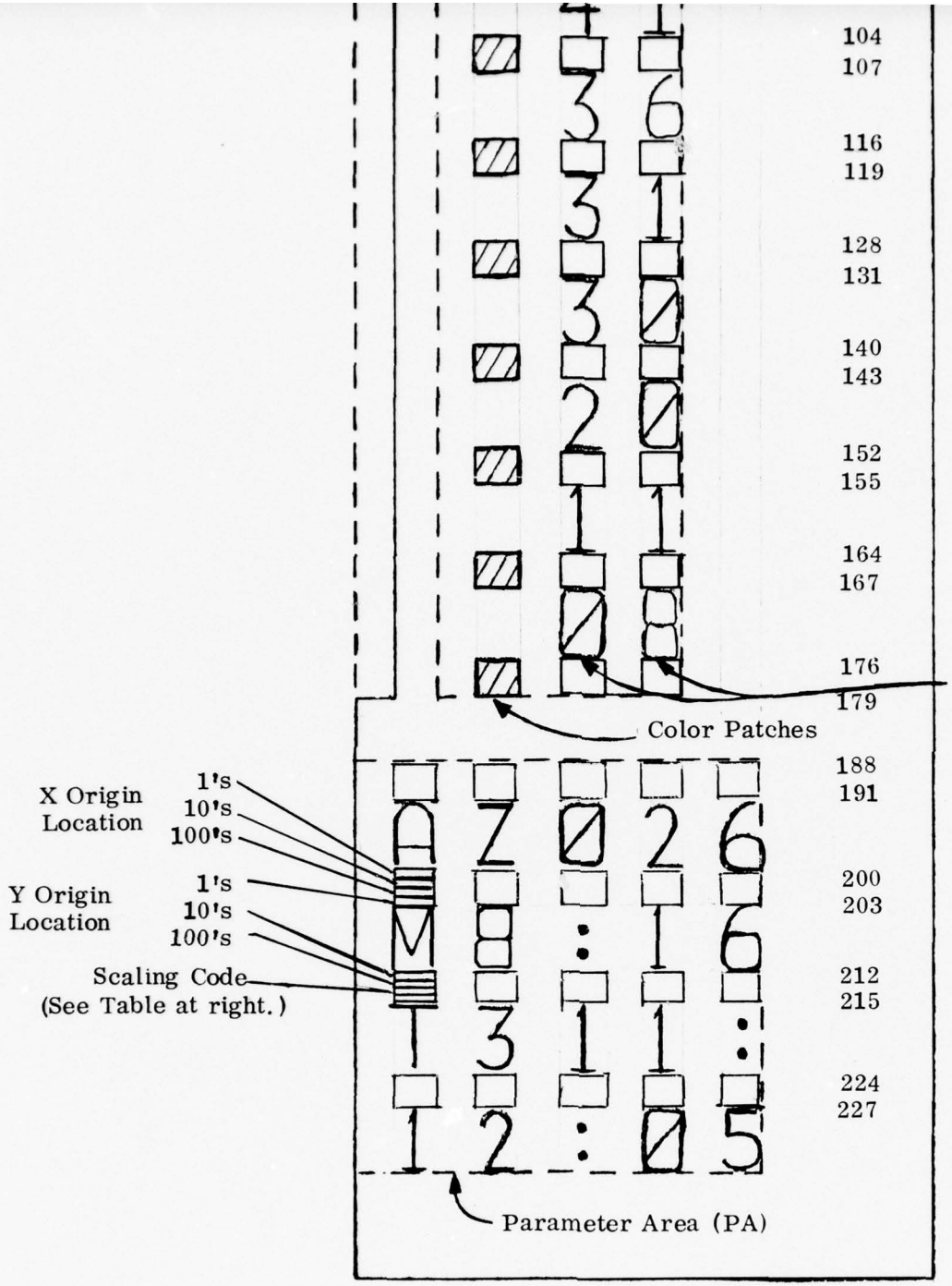
Cursor select - S_C

(Selects one of the four channels; 00 = display #1, 01 = display #2, etc.)

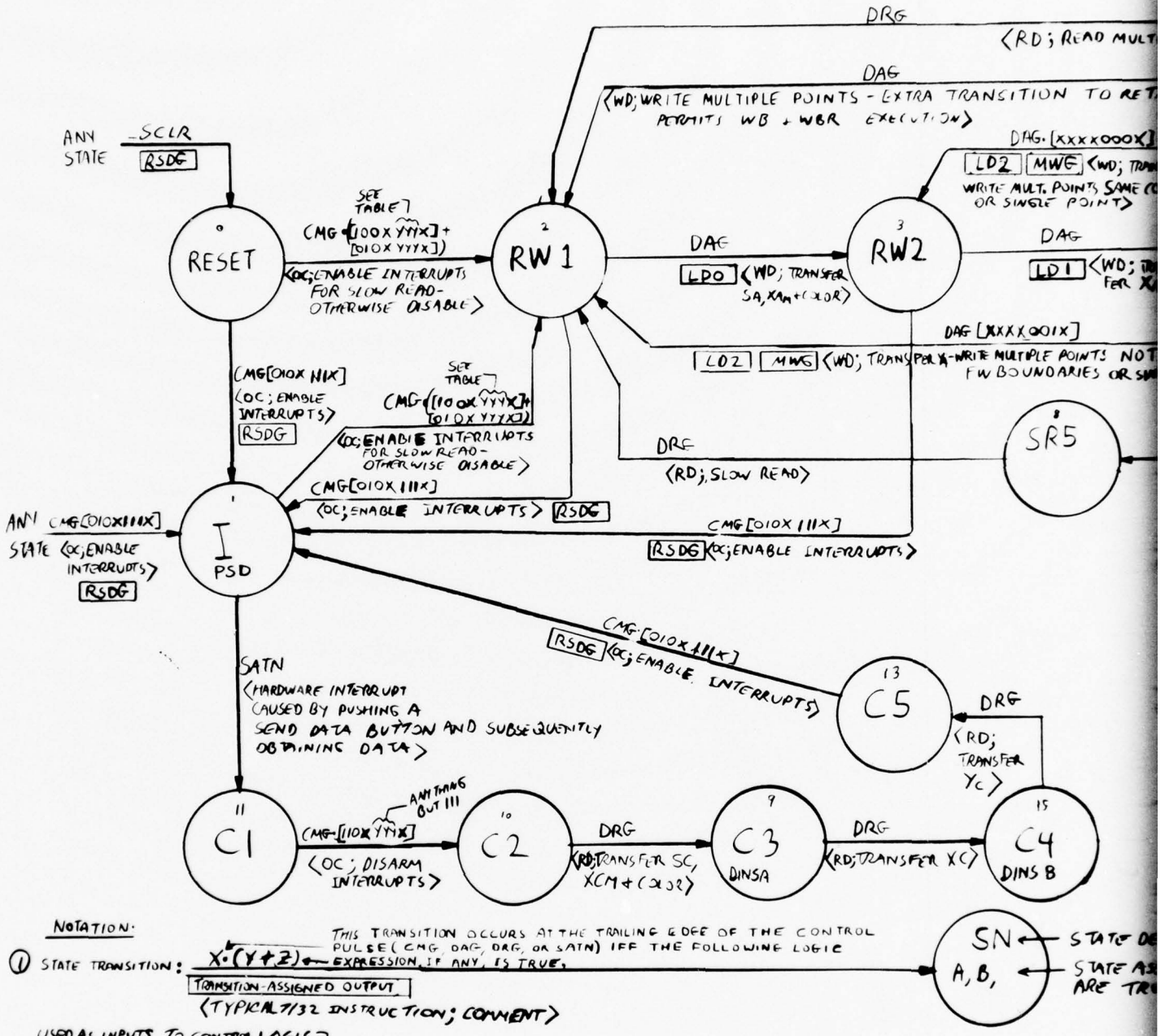
Color Code (4-Bits)	Relative Video Voltage Red	Green	Blue	Observed Color
0	0	0	0	Black
1	7	0	7	Magenta
2	5	0	7	Violet
3	3	0	7	Blue-Violet
4	0	0	7	Blue
5	0	3	7	Cyan-Blue
6	0	7	7	Cyan
7	0	7	0	Green
8	3	6	3	Lt. Green
9	6	6	6	White
10	3	3	3	Gray
11	7	7	0	Yellow
12	6	2	3	Pink
13	7	2	0	Orange
14	7	1	0	Red-Orange
15	7	0	0	Red (Can't be overwritten)

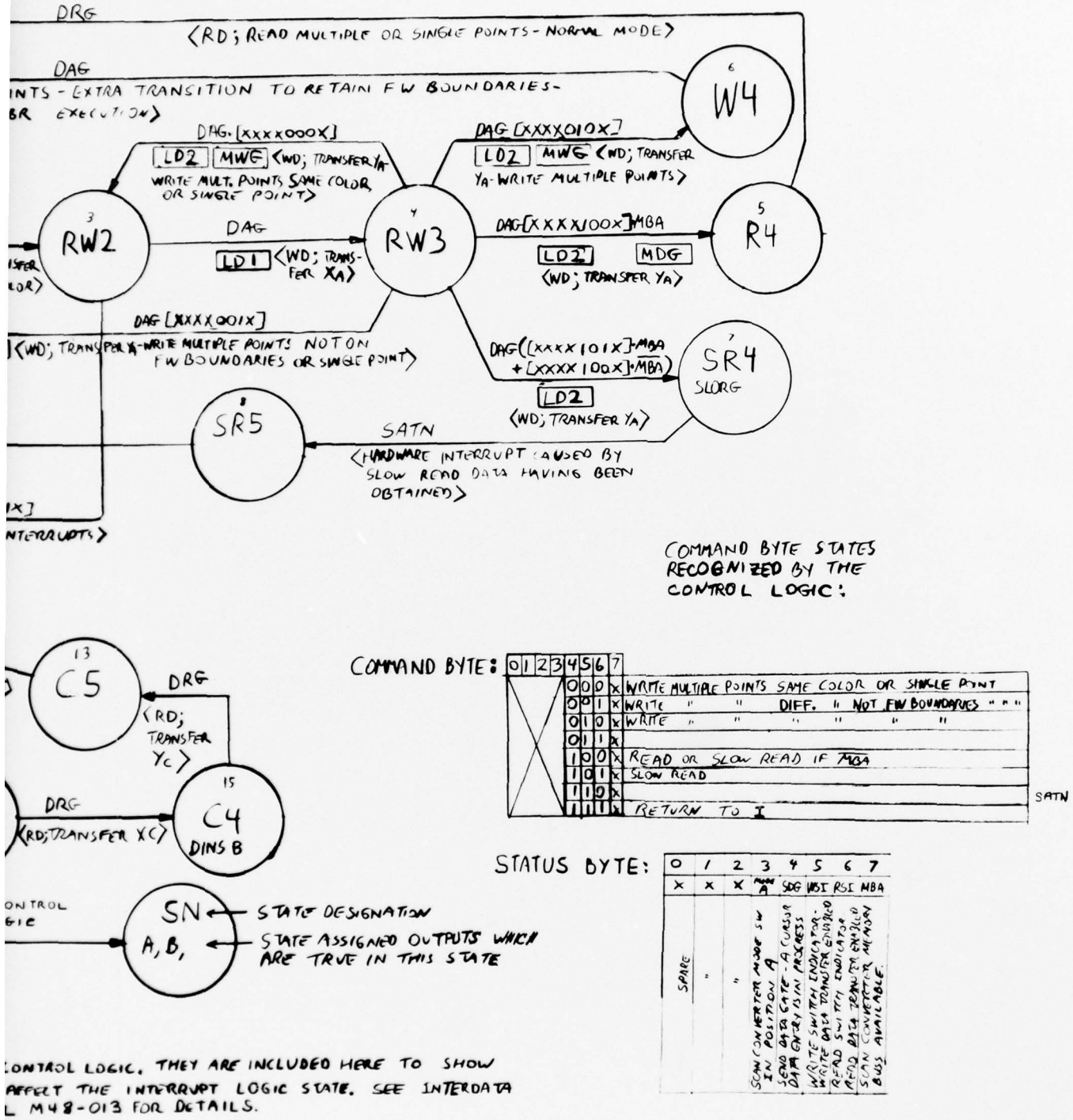
Figure 2. Display Addressing and Color Code Conventions for Each of the Four Channels

Figure 3. Address Locations of Ancillary Data



Alt. SCL = 1	X	X	O	O
2	X	X	O	1
4	X	X	1	O
8	X	X	1	1
Ring SCL = 1	O	O	X	X
2	O	1	X	X
4	1	O	X	X
8	1	1	X	X


ANY STATE
-SCLR
RSDG
0
RESET
SEE TABLE
CMG [100X YYYX] + [010X YYYX]
OC; ENABLE INTERRUPTS FOR SLOW READ- OTHERWISE DISABLE
2
RW 1
DRG
<RD; READ MULT
DAG
<WD; WRITE MULTIPLE POINTS - EXTRA TRANSITION TO RE
PERMITS WB + WBR EXECUTION>
DAG. [XXXX000X]
LD2 MWG <WD; TRA
WRITE MULT. POINTS SAME
OR SINGLE POINT>
DAG
LDO <WD; TRANSFER SA, XAM + (XOR>
3
RW2
DAG
LD1 <WD; TR
FER X
DAG [XXXX001X]
LD2 MWG <WD; TRANSFER - WRITE MULTIPLE POINTS NO
FW BOUNDARIES OR S
CMG [010X 111X]
<OC; ENABLE INTERRUPTS>
RSDG
SEE TABLE
CMG [100X YYYX] + [010X YYYX]
OC; ENABLE INTERRUPTS FOR SLOW READ- OTHERWISE DISABLE
CMG [010X 111X]
<OC; ENABLE INTERRUPTS> RSDG
DRG
<RD; SLOW READ>
4
SR5
ANY STATE
CMG [010X 111X]
<OC; ENABLE INTERRUPTS>
RSDG
1
I
PSD
CMG [010X 111X]
RSDG <OC; ENABLE INTERRUPTS>
SATN
<HARDWARE INTERRUPT CAUSED BY PUSHING A SEND DATA BUTTON AND SUBSEQUENTLY OBTAINING DATA>
CMG [010X 111X]
RSDG <OC; ENABLE INTERRUPTS>
13
C5
DRG
<RD; TRANSFER Yc>
11
C1
CMG [110X YYYX]
ANYTHING BUT 111
<OC; DISARM INTERRUPTS>
10
C2
DRG
<RD; TRANSFER SC, XCM + (XOR>
9
C3
DINSA
DRG
<RD; TRANSFER XC>
15
C4
DINS B
NOTATION:
① STATE TRANSITION:
THIS TRANSITION OCCURS AT THE TRAILING EDGE OF THE CONTROL PULSE (CMG, DAG, DRG, OR SATN) IFF THE FOLLOWING LOGIC EXPRESSION, IF ANY, IS TRUE.
X·(Y+Z)
TRANSITION-ASSIGNED OUTPUT
<TYPICAL 7/32 INSTRUCTION; COMMENT>
SN
A, B,
STATE DE
STATE AS
ARE TR
② COMMAND BYTE SENT TO ULI BY OC INSTR.:
USED AS INPUTS TO CONTROL LOGIC
[0 1 2 3 4 5 6 7]
DISABLE
ENABLE
HALFWORD
NOT USED
SPARE
THESE BITS CONTROL ULI INTERRUPT LOGIC, NOT THE CONTROL LOGIC. THEY ARE INCLUDED
HOW ANTICIPATED TYPICAL PROGRAMMING WOULD AFFECT THE INTERRUPT LOGIC STA
UNIVERSAL LOGIC INTERFACE INSTRUCTION MANUAL M48-013 FOR DETAILS.



COMMAND BYTE STATES RECOGNIZED BY THE CONTROL LOGIC:

COMMAND BYTE:

0	1	2	3	4	5	6	7	
0	0	0	x					WRITE MULTIPLE POINTS SAME COLOR OR SINGLE POINT
0	0	1	x					WRITE " " DIFF. " NOT FW BOUNDARIES " " "
0	1	0	x					WRITE " " " " " " "
0	1	1	x					
1	0	0	x					READ OR SLOW READ IF MBA
1	0	1	x					SLOW READ
1	1	0	x					
1	1	1	x					RETURN TO I

SATN

STATUS BYTE:

0	1	2	3	4	5	6	7
x	x	x	MODE A	SDG	WSI	RSI	MBA
SPARE	"	"	SCM CONVERTER MODE SW IN POSITION A	SEND DATA GATE - A CURSOR DATA ENTRY SIM. PROCESS	WRITE SWITCH INDICATOR - WRITE DATA TRANSFER ENABLED	READ SWITCH INDICATOR - READ DATA TRANSFER ENABLED	MBA - SCM CONVERTER MEMORY BUS AVAILABLE

CONTROL LOGIC. THEY ARE INCLUDED HERE TO SHOW
AFFECT THE INTERRUPT LOGIC STATE. SEE INTERDATA
L M48-013 FOR DETAILS.

Figure 4. Control Logic State Diagram—DDI

Table 2. Examples of Display Data Port—I/O Operations
(For Interrupt-Driven I/O: ISP Table Loc. X' E16' = X' D0' + 2 x (Dev. No.: X' 8B')
Must Contain the Address of the Int. Serv. Routine

OPERATION	TYPICAL STEPS	TYPICAL 7/32 INSTRUCTION	ULI INPUTS: DIN (DATA) 0...1...7 MSB ... LSB	ULI INPUTS: SIN (STATUS) 0...4,5,6,7				ULI INPUTS: 0... MSB
				0...4	SDG	MSI	RSI	MBA	MSB
WRITE DISPLAY MEMORY (TWO POINTS THE SAME COLOR)	0. SENSE STATUS	SS		x x x x	0	1	x	x	
	1. CHECK STATUS FOR 01XX	NI, ETC							
	2. OUTPUT CMD BYTE OR INI	OC							
	3. OUTPUT CMD BYTE	OC							
	4. TRANSFER SA, XAM, AND COLOR DATA	WD							② x SAB SAM
	5. TRANSFER FIRST X_A	WD							— X_A
	6. TRANSFER FIRST Y_A	WD							— Y_A
	7. TRANSFER SECOND X_A	WD							— X_A
	8. TRANSFER SECOND Y_A	WD							— Y_A
	9. OUTPUT CMD BYTE, ENABLE INTERRUPT	OC							
READ DISPLAY MEMORY (NORMAL MODE ALLOWED IFF SIN7 IS TRUE. OTHERWISE, THE SLOW READ MUST BE USED - SEE NEXT PAGE)	0. SENSE STATUS			x x x x	0	x	1	1	
	1. CHECK STATUS FOR 0X11	NI, ETC							
	2. OUTPUT CMD BYTE OR INI	OC							
	3. OUTPUT CMD BYTE	OC							
	4. TRANSFER SA, XAM	WD							② x SAB SAM
	5. TRANSFER X_A	WD							— X_A
	6. TRANSFER Y_A	WD							— Y_A
	7. DELAY - 6 μSec	4-BTCR							
	8. TRANSFER COLOR DATA	RD	x x x x — (COLOR (RD))						
	9. OUTPUT CMD BYTE, ENABLE INTERRUPT	OC							
CURSOR DATA ENTRY (INTERRUPT SERVICE ROUTINE)	0 OUTPUT CMD BYTE								
	1. OBSERVE PULSE ON SATN LINE (HARDWARE INTERRUPT)			x x x x	1	x	x	x	
	2. CHECK STATUS, IN REG 3, SET Θ, FOR BIT 4 TRUE	NI, ETC							
	3. OUTPUT CMD BYTE, DISARM INTERRUPT	OC							
	4. TRANSFER SC, X_{CM}, AND COLOR DATA	RD	② x S_C S_{CA} X_{CM} — (COLOR (RD))						
	5. TRANSFER X_C	RD	— X_C —						
	6. TRANSFER Y_C	RD	— Y_C —						
	7. OUTPUT CMD BYTE, ENABLE INTERRUPT	OC							
	8. RESTORE PROG. STATUS WORD	LPSWR							

① NOT AVAILABLE AT ULI OUTPUTS
② SEE NEXT PAGE

ULI INPUTS			ULI OUTPUTS			ULI CNTRL LINE ACTIVE	TYP. EXEC TIME -MS	CONTROL LOGIC STATE ENTERED
DIN (DATA)		SIN (STATUS)	DOT (DATA)		① COT (COMMAND)			
. . . 1 . . . 7 LSB		0. . . 4,5,6,7 MODE A SDG MSI RSI MBA	0. . . . . 7 MSB LSB		0,1,2,3 DISABLE ENABLE HWM NOT USED	4,5,6,7 SPARE			
		x x x x 0 1 X X					SRG	1+	-
								1.+	-
					1 0 0 X	1 1 1 X	CMG	4	RESET OR I
			②		1 0 0 X	0 0 0 X	CMG	4.	RW1
			$x S_{AB} S_{AA} Y_{AA}$	COLOR (WD)			DAG	3.75	RW2
			— X_A	—			DAG	3.75	RW3
			— Y_A	—			DAG	3.75	RW2
			— X_A	—			DAG	3.75	RW3
			— Y_A	—			DAG	3.75	RW2
					0 1 0 X	1 1 1 X	CMG	4	I
		x x x x 0 x 1 1					SRG	1+	
					1 0 0 X	1 1 1 X	CMG	4.	RESET OR I
			②		1 0 0 X	1 0 0 X	CMG	4.	RW1
			$x S_{AB} S_{AA} Y_{AA}$	x x x x			DAG	3.75	RW2
			— X_A	—			DAG	3.75	RW3
			— Y_A	—			DAG	3.75	R4
							-	6+	
x x x	— COLOR (RD)						DRG	3.75	RW1
					0 1 0 X	1 1 1 X	CMG	4.	I
					0 1 0 X	1 1 1 X	CMG	4	I
		x x x x 1 x x x							C1
②					1 1 0 X	1 1 0 X	CMG	4.	C2
$S_{CA} X_{CA}$	— COLOR (RD)						DR	3.75	C3
— X_C	—						DR	3.75	C4
— Y_C	—						DR	3.75	C5
					0 1 0 X	1 1 1 X	CMG	4.	I

NOT AVAILABLE AT ULI OUTPUTS
SEE NEXT PAGE

Table 2. (Continued)

OPERATION	TYPICAL STEPS	TYPICAL 7/32 INSTRUCTION(S)	ULI INPUTS: DIN(DATA) 0...1...7 (MSB ... LSB)	ULI INPUTS: SIN(STATUS) 0...4,5,6,7 (MODEA, SDG, NSI, RSI, MBA)
READ DISPLAY MEMORY (SLOW)	0. SENSE STATUS	SS		x x x x 0 x 1 0
	1. CHECK STATUS FOR 0X10			
	2. OUTPUT CMD BYTE OR INI	OC		
	3. OUTPUT CMD BYTE, ENABLE INTERRUPT	OC		
	4. TRANSFER SA, XAM	WD		
	5. " XA	WD		
	6. " YA	WD		
	7. INTERRUPT WHEN DATA IS READY (DELAY WILL VARY BETWEEN 0 AND 16 MILLISECONDS)	—		
INTERRUPT SERVICE ROUTINE	8. TRANSFER COLOR DATA RD	RD	x x x x — RO —	
	9. OUTPUT CMD BYTE	OC		
	10. RESTORE PROG STATUS WORD	LPSWR		

② DISPLAY + CURSOR SELECT CODES

S_{AB} S_{CB}	S_{AA} S_{CA}	DISPLAY #
0	0	1
0	1	2
1	0	3
1	1	4

Table 2. (Continued)

ULI INPUTS									ULI OUTPUTS												ULI CNTRL LAW ACTIV	TYP EXEC TIME MS	CONTROL LOGIC STATE ENTERED
DIN(DATA)								SIN(STATUS)				DOT(DATA)								COT(COMMAND)											
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7			
LSB				MODE A	SDG	WSI	RSI	MBA	MSB						LSB	DISABLE	ENABLE	NWM	NOT USED	R/W	SQB	SQA	SPARE			
				x	x	x	x	0	x	1	0													SRG	1T	
																1	0	0	x	1	1	1	x	CMG	4	RESET OR I
																0	1	0	x	1	0	x	x	CMG	4	RW1
												②												DAG	3.75	RW2
												x	S	x	x	x	x	x	x					DAG	3.75	RW3
													XA											DAG	3.75	SR4
													YA											SATN		SR5
x	x	x	-RO-																					ORG	3.75	RW1
																0	1	0	x	1	1	1	x	CMG	4	I

Table 3. SCPLT Subroutine

INPUTS: Reg. X, x-coord. $0 \leq X \leq 319$
Reg. Y, y-coord. $0 \leq Y \leq 247$
Reg. C, S_A in bits 25&26, color in bits 28-31, all other bits zero.
Reg. F, return address.

```
000082I  C8B0 008B           58  SCPLT     LHI   B,X'8B'     Device code in reg. B.
000086I  DEB0 4000 00BEI     59             OC    B,DDICMD1   Output Cmd-disarm int, DDI to st. RW1.
00008CI  C9D0 0100           60             CHI   X,X'100'    Compare X to 256.
000090I  4210 4000 00B0I     61             BM    SCPLTA      If X<256, go to SCPLTA.
000096I  CBD0 0100           62             SHI   X,X'100'    Decrease X by 256.
00009AI  CAC0 0010           63             AHI   C,X'10'     Make bit 27 of C a 1.
00009EI  9ABC                64             WDR   B,C         Write cont of reg C (S_A,X_AM,Color).
0000A0I  9ABD                65             WDR   B,X           "    "  "  "  X (input X-256).
0000A2I  CAD0 0100           66             AHI   X,X'100'    Restore X to what it was.
0000A6I  CBC0 0010           67             SHI   C,X'10'       "    C "  "  "  "
0000AAI  4300 4000 00B4I     68             B     SCPLTB      Go to SCPLTB.
0000B0I  9ABC                69  SCPLTA    WDR   B,C         Write cont of reg C
0000B2I  9ABD                70             WDR   B,X           "    "  "  "  X
0000B4I  9ABE                71  SCPLTB    WDR   B,Y           "    "  "  "  Y
0000B6I  DEB0 4000 00C0I     72             OC    B,DDICMD2   Output Cmd-disarm int,DDI to st. I.
0000BCI  030F                73             BR    F           Return to the address in reg. F.
0000BEI                      74             ALIGN 2
0000BEI  C200                75  DDICMD1   DC    X'C200'
0000C0I  CE00                76  DDICMD2   DC    X'CE00'
```

Table 4. Program to Copy One Display to Another

```
6000  C8A0      LHI   A,Q     source display:  1    2    3    4
   2                                      Q : 0000 0020 0040 0060
   4  C8B0      LHI   B,P     output display:  1    2    3    4
   6                                      P : 0000 0020 0040 0060
   8  C880      LHI   8,8B      device code in reg. 8.
   A  008B
   C  C890      LHI   9,C8      cmd byte for read in reg. 9.
   E  00C8
6010  C850      LHI   5,C2      cmd byte for write in reg. 5.
   2  00C2
   4  24D0      LIS   D,0       zero reg. D.
   6  24E0      LIS   E,0        "" "    E.
   8  9E89      OCR   8,9       output cmd byte for read.
   A  9A8A      WDR   8,A       write S_A,X_AM
   C  9A8D      WDR   8,D         "        X_A
   E  9A8E      WDR   8,E         "   Y_A
6020  0200      BTCR  0,0       delay (No-OP)
   2  0200      BTCR  0,0        "
   4  0200      BTCR  0,0        "
   6  0200      BTCR  0,0        "
   8  9B8C      RDR   8,C       read data into reg. C.
   A  C4C0      NHI   C,F       mask all but the 4 lsb of reg. C.
   C  000F
   E  9E85      OCR   8,5       output cmd byte for write.
6030  0ACB      AR    C,B       get the output display code in reg. C.
   2  9A8C      WDR   8,C       write S_A,X_AM,Color
   4  9A8D      WDR   8,D         "        X_A
   6  9A8E      WDR   8,E         "   Y_A
   8  26E1      AIS   E,1       increment Y_A by 1.
   A  C9E0      CHI   E,F8      compare Y_A with 248
   C  00F8
   E  4320      BNP   6018      if  Y_A ≤ 248, go to 6018.
6040  4000
   2  6018
   4  26D1      AIS   D,1       increment X_A by 1.
   6  24E0      LIS   E,0       zero Y_A.
   8  C9D0      CHI   D,100     compare X_A with 256.
   A  0100
   C  4210      BM    6018      if  X_A < 256, go to 6018.
   E  4000
6050  6018
   2  4330      BNE   6064      if  X_A ≠ 256, go to 6064.
   4  4000
   6  6064
   8  C9D0      CHI   D,13F     compare X_A with 319.
   A  013F
   C  4320      BNP   6018      if  X_A ≤ 319, go to 6018.
   E  4000
6060  6018
```

Table 4. (Continued)

```
6062   2200      BFBS   0,C       branch unc. to self.
   4   CAA0      AHI    A,10      add 16 to reg. A (make X_AM=1).
   6   0010
   8   CAB0      AHI    B,10       "  "  "   "   B   "    "
   A   0010
   C   4300      B      6018      go to 6018.
   E   4000
6070   6018
```

To do the same task using the slow read mode, change:

```
600E   004A                      cmd byte for slow read, interrupts enabled.

6020   2200      BFBS   0,0       branch unc. to self.
```

and include the following interrupt service routine:

```
6100   2612      AIS    1,2       increment reg. 1, the loc part of the PSW,
                                   by one halfword to bypass the 2200 at 6020.
6102   1800      LPSWR  0,0       restore the PSW
```

Run with immediate interrupts enabled, in reg. set 0. (PSW=4000)
In the interrupt service pointer table, at D0+2x8B, put the starting address of the interrupt service routine:

```
0E16   6100
```

Note: This program was written diectly in machine language; it was never assembled by CAL. The assembler notation included here is incorrect for CAL in that all numbers listed are in hex. In CAL, such numbers must be represented as X'NNNN' or Y'NNNNNNNN', except for 0-9.

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RAYTHEON

AM 10-0557 (2-65) BOND

		Classification	Unclassified
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Operation	EDL - Wayland		
Department	Advanced Development Laboratory	Distribution	Listed
To	J. H. Turner, Jr.	File No.	
From	A. J. Jagodnik, Jr.	Memo No.	AJJ-26
Subject	Scan Converter Drawing List	Date	4 June 1975

The fact that two slightly different scan converter refresh memory systems have been built and that both have been extensively modified in different ways has led to some confusion in the area of the applicability of drawings. The Table contained herein is intended to resolve the confusion. It contains all drawings related to the scan converters, ordered by Raytheon drawing number, and indicates the equipment to which each is applicable. Also included is information describing the size, type and form of each drawing and whether or not it references other drawings.

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Advanced Electronic Techniques
Wayland, Box M9, Ext. 2736

/bp

cc: G. Dennis
K. M. Glover (3)
D. L. Keefe
J. C. Murray
L. R. Novick
J. C. Westphal

SCRM DRAWINGS

Type: S - Schematic, I - Interconnection Diagram, M - Mechanical, B - Block Diag.
Form: V - Velium, M - Mylar, S - Sepia

Dwg No.	Size	Type	Form	Abbrev. Title (Notes)	Other Dwg Ref:	Application: S/N 2 Before LWCA	S/N 1 Before KMR	LWCA(2)	KMR: Master	KMR: Remote
895180	B	M	V	Mtg. Brkt. Interface (MIU Shelf)		X	X	X	X	X
895181	D	S	V	C.C. X Hatch Gen 3C		X	X	X	X	
895182	D	S	V	Test Card						
895183	D	S	V	C.C. Origin Trans. BCD/BW 3F		X	X	X	X	
895184	D	S	V	C.C. X Proj. Accum 3E		X	X	X	X	
895185	D	S	S	C.C. Hi Alt Acc 2C		X	X	X	X	
895186	D	S	S	C.C. Lo Alt Acc 2D		X	X	X	X	
SD895187	D	S	S	AIU		X	X	X	X	
895188	D	S	V	C.C. Y Proj. Accum 3D		X	X	X	X	
895189	D	M	V	Hole Layout, Rear Pnl Interface #1 (Lower SCP)		X	X	X	3 BNC's Added	
895190	D	M	V	" " " " " #2 (Upper SCP)		X	no J3 & J4 holes	X	no J3 & J4 holes	
895191	D	M	V	" " " " " #3 (MIU)		X	X	X	X	X
895192	D	S	S	C.C. T. F. Earth Alt. Acc. 2E		X	X	X	X	
895193	D	S	S	C.C. R. Proj. Accum 2F		X	X	X	X	
SD895194	D	S	V	VDU		X	X	X	X	
895195	D	S	S	C.C. Alt 12 x 12 Mult. 1F		X	X	X	X	
895196	D	S	V	C.C. Range 12 x 12 Mult. 1E		X	X	X	X	
895197	E	B	V	C.C. Block Diag.		X	X	X	X	
895198	E	S	V	C.C. X 12 x 12 Mult. 1A & B		X	X	X	X	
895199	E	S	S	C.C. Y 12 x 12 Mult. 1C & D		X	X	X	X	
SD895200	E	S	S	MIU (2 sht)		X	X			(1)
SD895201	E	S	1-V 2-M	DCU (2 sht)		X	X			
895202	E	S	V	C.C. Alt Compar. 2A & B		X	X	X	X	
895203	E	S	V	C.C. Interface 3A, B&C		X	X	X	X	
895204	E	M	S	S.C. Front Panel, Hole Layout		X	X	X	X	
895205	E	M	V	S.C. Silk Screen Layout		X	X	X	X	
895718	J	I	S	Int. Diag-KMR CC	X				X	
895720	E	S	S	KMR Master SCRM F & R Panels	X				X	
895726	C	I	S	KMR Master SCRM Power Supplies					X	
897392	E	I	V	C.C. Interconnect	X	X	X	X		
897393	C	I	1-V 2-S	Scan Conv. Interconnect	X	sht 2	sht 1			
897896	B	I	V	MEM to MIU		X	X	X	X	X
897897	C	I	V	DCU & VDU to MIU (Cables)		X	X	X	X	X
897898	E	S	V	S.C. Proc. F & R Panels	X	X	X	X		
897899	E	I	V	DCU to VDU	X	X	X	X		
897900	C	I	V	S. C. Proc. DC Power Supplies		X	X	X		

SCRM DRAWINGS (Continued)

Dwg No.	Size	Type	Form	Abbrev. Title (Notes)	Other Dwg Ref:	Application: S/N 2 Before LWCA	S/N 1 Before KMR	LWCA (2)	KMR: Master	KMR: Remote
897918	B	S	V	Term for Twp Lines		X	X	X	X	X
910161	D	M	V	Hole Layout F Panel				X		
910162	D	M	S	Silk Screen F Panel				X		
910163	C	M	V	Bracket for Conn.				X		
910166	D	S	V	LWCA Control Panel				X		
910167	C	S	V	Cable Wiring LWCA Cont. Panel to DDI				X		
910168	E	S	S	DCU (2 sht)				X		
910169	J	S	S	MIU (Sections C-F; Geo. has mylar from which this was made)	X			X		(1)
910170	C	S	V	Mon. No. 5 input sel.		X		X		
910171	E	S	V	Color Encoder (MIU Same as SD895200 sht 2)				X	X	(1)
910172	C	I	V	Cable - DCU to Card 2				X		
910173	D	I	S	Cable - DDI to ULI				X		
910174	D	I	V	Cable - DDI to DCU				X		
910175	E	S	M	DDI				X		
910176	D	I	V	LWCA Scan Conv.	X			X		
911046	C	S	V	Data Trans Control Panel & Cable					X	
911047	D	S	M	SDF					X	
911048	E	S	M	DRU						X
911049	D	I	M	Remote Refresh Memory	X					X
911050	D	I	V	Cables - KMR Master	X				X	
911101	C	I	S	KMR Master SCRM	X				X	
911102	E	S	S	KMR DCU (Sht 2 same as SD895201 sht 2)					X	
911103	E	I	S	KMR DCU to VDU	X				X	
911104	J	S	S	Master KMR MIU (C-F; Geo. has mylar from which this was made)	X				X	(1)
911155	B	I	V	Remote MIU Video Jumper						X
911156	D	I	V	RRM F & R Panels						X
911157	D	M	V	Silk Screen - F. Panel Data Trans Cntrl					X	
911158	D	M	V	Silk Screen RRMR						X
911159	D	M	S	Hole Ly F Panel RRMR						X
911160	D	M	S	Hole Ly F Panel Data Trans Cntrl					X	

(1) See 911049

(2) All LWCA drawings are not listed here; only those related to the SCRM.

Unclassified
AJJ-26
4 June 1975
Page 3 of 4

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