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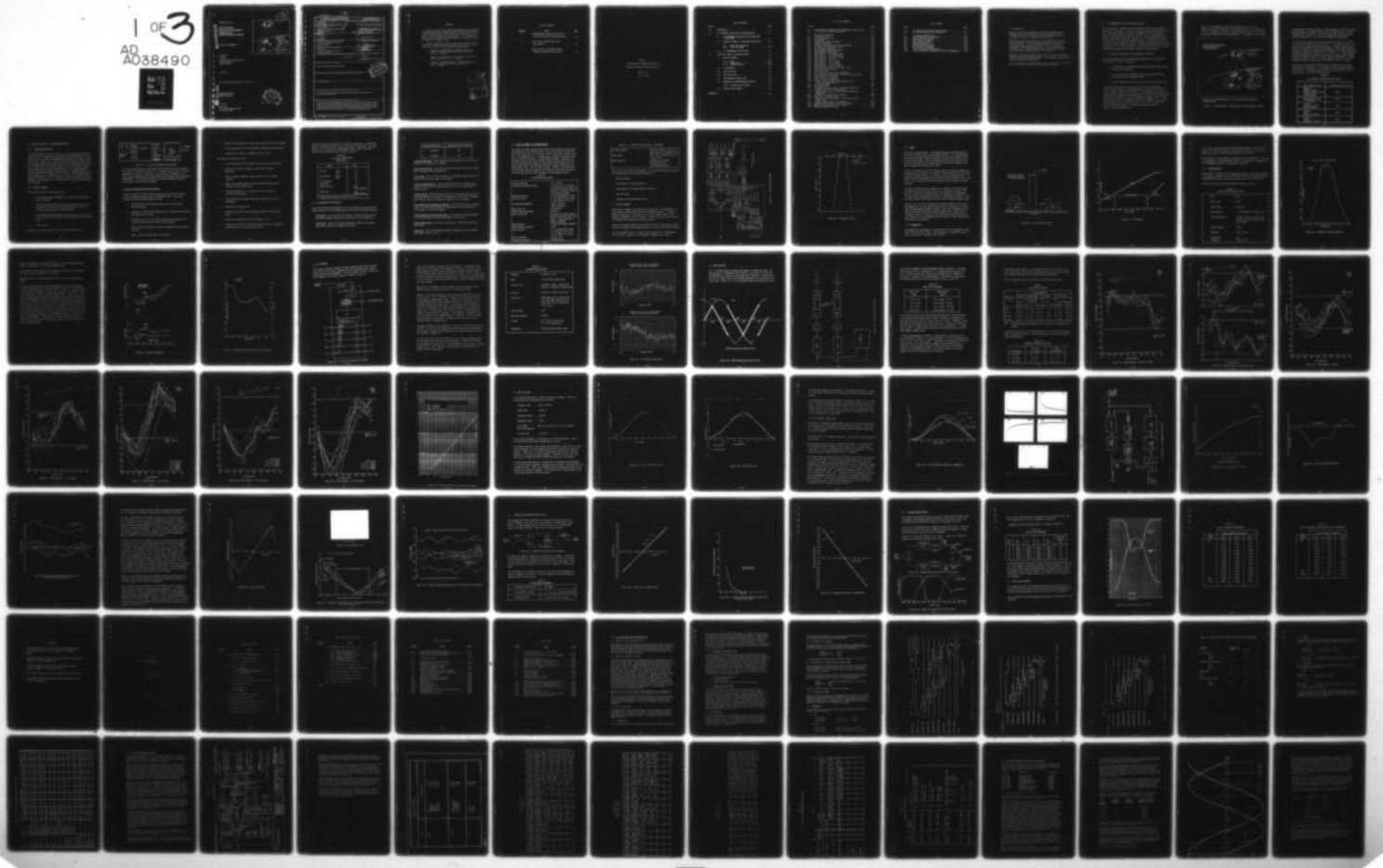

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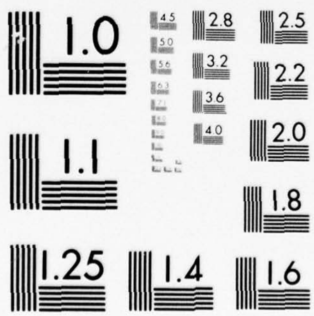

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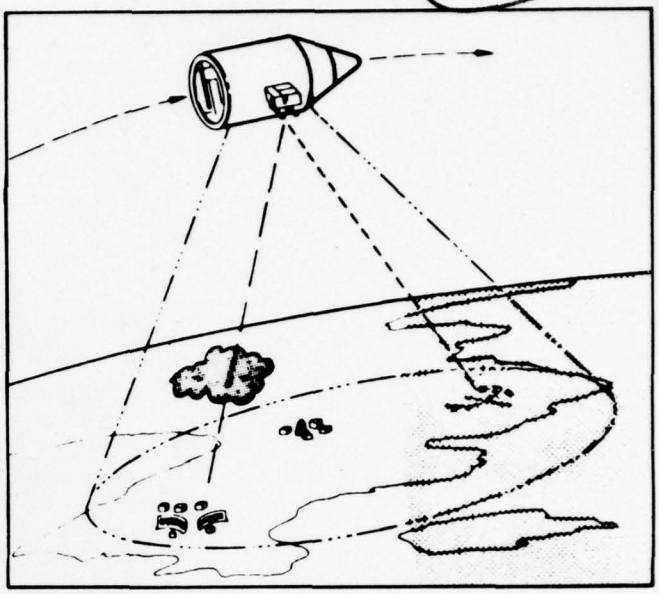

Volume III – Appendices

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Circuits to add a passive ranging capability to the Interferometric Landmark Tracker (ILT) to form a Passive Ranging Interferometric Sensor (PRAIS) were built and tested in the laboratory. The laboratory test data were used in a Monte Carlo simulation to demonstrate the performance of the PRAIS Navigation System in a highly elliptic orbit and a synchronous orbit (1° inclination). Navigation accuracies better than 1000 feet and attitude determination accuracy better than 15 arc seconds were indicated by the analyses.

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FOREWORD

This is volume III of a three-volume final report of the Self-Contained High Altitude Navigation System (SCHANS) study published by the IBM Corporation, Federal Systems Division under Air Force Contract F04701-76-C-0106. The final report satisfies the requirements of CDRL Item A003 under that contract. It is submitted to the USAF Space and Missile Systems Organization (SAMSO) for review by Captain R. A. Lawhern, USAF.

Volume I consists of a system summary, and Volume II presents the results of the seven technical tasks of the contract. This Volume III consists of the following three appendices:

- Appendix A, Interferometric Landmark Tracker (ILT) Receiver Electrical Design Description, prepared by Mr. L. O. Smith.
- Appendix B, SCHANS Pulse Conversion Unit (PCU) Final Report, prepared by Mr. R. E. Dreska.
- Appendix C, SCHANS Operational Software Computer Program Development Specification, prepared by Mr. G. A. Kooch.

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Appendix A

INTERFEROMETRIC LANDMARK TRACKER (ILT)

RECEIVER ELECTRICAL DESIGN DESCRIPTION

Prepared by

Lynn O. Smith

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1.0 INTRODUCTION

Sections 2 and 3 of this appendix are reprints from the Autonomous Navigation Technology Phase IB Final Report, SAMSO TR75-298, 1 November 1975. It is provided as background technical material in support of Section 3 of Volume II of this report.

The receiver described herein does not include the time of arrival (TOA) measurement circuits that were introduced to provide passive ranging capability. (See High Altitude Navigation System Study Final Report, SAMSO TR75-72, March 1975.) Those circuits were implemented in breadboard form and tested in the laboratory during the SCHANS study. The performance of those circuits, and results of the tests are described in Section 3 of Volume II.

References to the Signal Processing Unit (SPU) in Section 2.0 should be read as Pulse Conversion Unit (PCU) for consistency in designations presently assigned to SCHANS equipment. SPU in SCHANS terminology refers to the on-board dedicated computer.

In case of conflict or inconsistency between this appendix and any other portion of this final report, the latter takes precedence.

2.0 ILT AUTONOMOUS NAVIGATION SYSTEM DESCRIPTION

The Interferometric Landmark Tracker Autonomous Navigation System Concept is described in this section. Section 2.1 provides an operational description of the ILT Autonomous Navigation System with emphasis on the ILT operations. Section 2.2 summarizes the flight test model ILT design developed under this contract and delineates the major changes in the ILT receiver design concepts developed during this program phase and provides a functional description of the signal processor/computer interface. Section 2.3 summarizes the performance requirements for the flight test model ILT from which the ILT Flight Test Model Receiver design specifications given in Section 3.0 were developed.

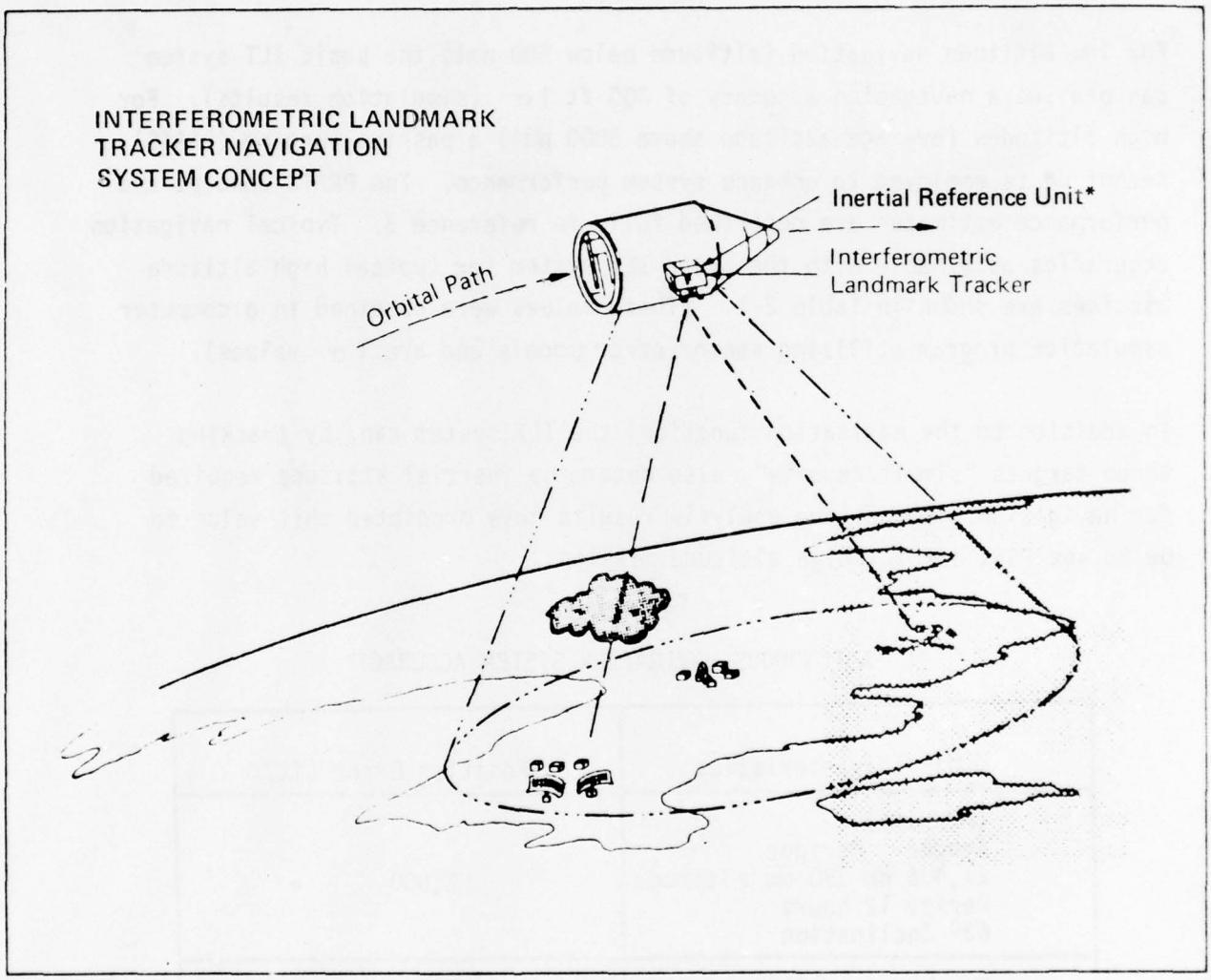
2.1 ILT AUTONOMOUS NAVIGATION SYSTEM OPERATIONAL DESCRIPTION

The ILT Autonomous Navigation System Concept (Reference 1) for space navigation shown in Figure 2-1 consists of:

- The strapped down ILT Sensor which provides precise angle tracking of known radar landmarks.
- A three-gyro inertial reference unit to provide attitude memory during "Coast" periods between landmarks.
- A digital computer to process the sensor data with a Kalman filter.

In operation, angle data is received by the ILT from such landmarks as air traffic control, defense early warning and coastal search radars operating in the frequency range of 2.5 to 2.9 GHz. This angle data is processed with a Kalman filter to determine spacecraft position, velocity and attitude vectors. The latitude, longitude, altitude and frequency of selected radars of known position are stored in the computer to be used as landmarks. Any of these stored landmarks within the field-of-view of the ILT can be acquired by tuning to the radar frequency. Day/Night, all-weather operation is inherent in this frequency band.

The ILT is a strapped down sensor which requires only four 2.1 inch diameter antennas to be mounted on an earth pointing face of the spacecraft. The small, lightweight, low power associated electronics unit may be mounted at convenient locations within the spacecraft. All components of this sensor



*This function can be provided by the ILT in orbits where at least two landmarks are continuously visible.

Figure 2-1. Interferometric Landmark Tracker Navigation System Concept

are operational in avionics systems. During ANT Phase 1 laboratory, measurements were made on a breadboard model of the ILT (Reference 2). A similar interferometer is operational in the ATS-6 synchronous satellite and has proved the feasibility of such precision spaceborne interferometers.

For low altitude navigation (altitude below 500 nmi) the basic ILT system can provide a navigation accuracy of 300 ft 1σ (simulation results). For high altitudes (average altitude above 5000 nmi) a passive ranging (PRAIS) technique is employed to enhance system performance. The PRAIS concept and performance estimates are described fully in reference 3. Typical navigation accuracies obtainable with the basic ILT system for typical high altitude missions are shown in Table 2-1. (These values were obtained in a computer simulation program utilizing sensor error models and are 1σ values).

In addition to the navigation function, the ILT system can, by tracking three targets "simultaneously", also determine inertial attitude required for navigation. Covariance analysis results have predicted this value to be 25 sec RSS, 1σ for high altitude missions.

Table 2-1

ILT AUTONOMOUS NAVIGATION SYSTEM ACCURACY

Orbit Characteristics	Position Error (ft/σ)
(MOLNIYA) Apogee Perigee 21,406 nm 390 nm altitude Period 12 hours 63° Inclination	2,500
Synchronous altitude 1° Inclination	2,300
Circular 10,000 nm altitude 63° Inclination	900
Circular Polar 68,000 nm altitude	8,000
Circular Polar 150,000 nm altitude	14,500

2.2 FLIGHT TEST MODEL ILT FUNCTIONAL DESCRIPTION

2.2.1 Flight Test Objectives

The orbital flight test of the ILT has as its primary objective the verification of the ILT's capability to discriminate selected uncooperative radar signals from a cluttered radar background and determine the angular orientation of the ILT-radar line of sight with sufficient accuracy to make the ILT an acceptable landmark tracking device for self-contained satellite navigation. A major part of the primary objective will be to determine whether the navigation sensor can make accurate time of arrival measurements to enhance navigation performance at high altitudes. Secondary objectives are verification of the ILT's sensitivity, its utility as an attitude reference device, detectability of radars suitable to function as uncooperative known landmarks, and to determine if a fifth antenna is required for phase ambiguity resolution.

2.2.2 Flight Test Model

The flight test model ILT design consists of:

- o A five antenna array to determine if a self-resolving interferometer is required.
- o A signal processor unit which converts the analog signals from the receiver to a digital format, provides logic for receiver control and interface with an onboard computer
- o A three channel superheterodyne receiver which provides the sensitivity and selectivity to select and track signals from radar landmarks.
- o A power supply.

Figure 2-2 is a block diagram of the ILT flight test model design.

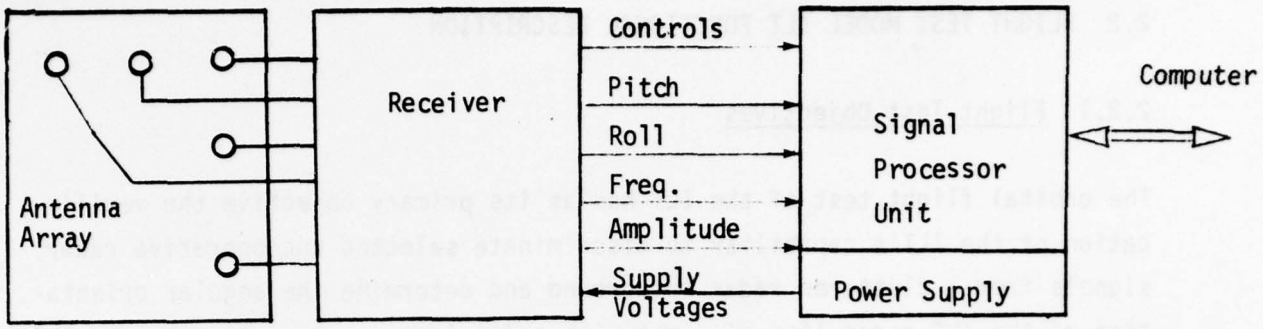


Figure 2-2. ILT Flight Test Model Block Diagram

During this contract phase, a detailed design of the receiver was carried out - this design is discussed in Section 3.0. The antenna array, since it is highly dependent upon spacecraft installation constraints was not studied in this phase and the antennas tested in the previous program phase provide satisfactory performances. A functional description of the signal processor operations are provided in the following paragraphs.

ILT Signal Processing Functional Description

A Signal Processor Unit (SPU) preliminary design was carried out to permit sizing for mechanical design of the ILT electronics unit. This design assumed the following were provided by the SPU:

- o A/D conversion of the frequency, phase, and log video signals from the receiver
- o Generation of the precision 60-MHz signal for the receiver calibration and time-of-arrival counter
- o D/A conversion of the local and RF calibration oscillators and RF calibrator amplitude control words from the computer
- o Control logic for receiver IF calibration commands and other control functions
- o Inputs a "qualified data" gate to the computer

- Buffers the received signal 128-bit data word for input to the computer
- The logic necessary for a 16-bit parallel interface with the computer
- Time-of-arrival counters to implement passive ranging.

The computer in supporting the SPU:

- Selects the next available landmark from the stored landmark table
- Searches for alternate landmarks if the primary landmark is unavailable
- Sends a frequency command to tune the receiver to the landmark frequency
- Centers the landmark signal in the IF pass band and resets the frequency in the landmark table
- Initiates the receiver IF calibration cycle and accepts the 128-bit calibration word
- Accepts 200 pulse measurement data words (128 bits) for each ILT measurements
- Processes RF calibration data
- Calibrates the signal data and averages the 200 calibrated signal pulses
- Inputs the calibrated data to the navigation filter
- Processes the ILT data in the Kalman navigation filter to determine spacecraft position, velocity, and attitude.

Table 2-2 lists the bit content of the 128-bit ILT data word. An additional 128-bit IF calibration word is sent for each group of 200 pulses. This word consists of 8 IF calibrations corresponding to ±45°, +135°, and +225° of phase for both the pitch and roll channels of the ILT.

Table 2-2
ILT SIGNAL PROCESSOR DATA
WORD CONTENT

Signal		Bits
RF Pulse	Pitch	16
	Roll	16
RF Calibrate	Pitch	16
	Roll	16
Fine Frequency		8
Log Video		8
*Time-of-Arrival		32
		112 Bits/Pulse
Spare Bits		16
		128 Bits/Pulse
*Required to add passive ranging to the ILT.		

2.3 ILT PERFORMANCE SPECIFICATION

To satisfy ANT mission requirements the ILT must measure two phase angles to radars operating in the RF frequency band within the following specifications.

DF Accuracy. The ILT shall have an overall direction finding accuracy goal after software calibration of one minute of arc one sigma (1σ).

Sensitivity. The ILT shall detect and process signals with incident power density meeting or exceeding those below.

INCIDENT POWER DENSITY	ANGULAR FIELD-OF-VIEW (FOV)
A. $-59\ dBm/m^2$	28^o
B. $-45\ dBm/m^2$	90^o

Frequency Measurement: Radar frequency shall be measured to an accuracy of 300 kHz (3) for the band of interest).

Angular Field-of-View. The angular field-of-view shall be conical in shape and in accordance with the above table.

Tuning Range. The ILT shall be tunable to a designated frequency within the range of 2.5 to 2.9 GHz within 1 millisecond.

Spurious Signal Rejection. Image frequency and spurious frequency signal suppression shall be at least 60 dB outside the 2.5 to 2.9 GHz range on a monopulse basis.

Emitter Sorting. The system accuracy shall not be degraded when up to five extraneous emitters all of which are separated by at least 45° of ambiguous phase from the signal of interest are present in the environment.

Pulse Width and Pulse Repetition Interval. The ILT shall detect and process signals with pulse widths between 500 nanoseconds and 5 microseconds and PRIs between 0.5 and 10 milliseconds.

Emitter Detection and Signal Processing. The confidence level for detection of any emitter meeting the above requirements shall be .983.

Signal Dynamic Range. The ILT shall operate over a 50-dB input signal dynamic range.

Temperature. The ILT shall meet performance requirements over the temperature range of +30°F to +160°F.

3.0 FLIGHT TEST MODEL ILT RECEIVER DESIGN

The flight test model receiver design differs from previous ILT operational configurations in the following areas. Since a five antenna array will be used in the flight test ILT, a five-port, 0° RF calibrator is required (four port in the operational ILT). A three-channel receiver configuration with switching at RF was selected to reduced weight and power. Calibration of the phase detectors was found to be more accurate and effective at IF frequency, hence the 90° RF calibration previously used was replaced with IF calibration at ±45°, +135° and +225° of phase. Finally, a YIG tuned oscillator provided sufficient stability and linearity to eliminate the need to count down the local oscillator frequency for VTO frequency control.

Table 3-1
ILT RECEIVER SPECIFICATION

Frequency Coverage	-	2.5 - 2.9 GHz
Frequency Measurement Accuracy	-	0.4 MHz max Error (Including LO uncertainty) when smoothing 100 pulses (software storage of LO end points allowed)
Frequency Variation (Pulse to Pulse)	-	At -76.5 dBm 600 kHz p-p max At -66.5 dBm 180 kHz p-p max At -56.5 dBm 60 kHz p-p max
Instantaneous Bandwidth	-	2 MHz-1 dB points 3 MHz-3 dB points
Sensitivity (m)	-	-96.5 dBm min
Dynamic Range (operating)	-	50 dB min
Spurious Rejection	-	60 dB min for signals 2 MHz or more away from the desired frequency. Image rejection by dither acceptable.
Phase Accuracy	-	1^{o} max error between channels
Phase Detector Linearity	-	$\pm.25^{o}$
Phase Variation	-	At -76.5 dBm 34.0^{o} p-p max At -66.5 dBm 11.4^{o} p-p max At -56.5 dBm 3.4^{o} p-p max
Input Pulsewidth	-	0.5 μs to 5 μs
RF Phase Calibration	-	Continuous Wave

Table 3-1. ILT Receiver Specification (Continued)

Max Video Risetime	-	300 ns (to within 1 dB of final amplitude for a rectangular pulse.
Tuning Speed	-	200 μs max to step full band to within 0.4 MHz.
Outputs Required	-	Frequency Discriminator Phase Detectors (2) Log Video Accept Pulse.

Figure 3-1 is the receiver block diagram. For discussion purposes the receiver can be broken down into the following subsections:

Receiver Channels

RF Calibrator & Calibration Control

Phase Detectors and Phase Detector Calibration

Local Oscillator

Frequency Discriminator/Qualification

3.1 RECEIVER CHANNELS

Three receiver channels are incorporated in the design. DF measurements are made between the center channel and the two adjacent channels. A receiver channel is comprised of (see Figure 3-1) an input bandpass filter, mixer, preamplifier/bandpass filter and limiter. The basic receiver channel function is provide RF to IF conversion, filtering and gain.

Three of five antenna outputs are selected by two SP2T switches on the output of the RF calibrator (to be discussed later) and fed to three receiver channels.

The input bandpass filter is an eight section device with a 1 dB bandpass of 2.5 to 2.9 GHz. Figure 3-2 is the measured response of this filter.

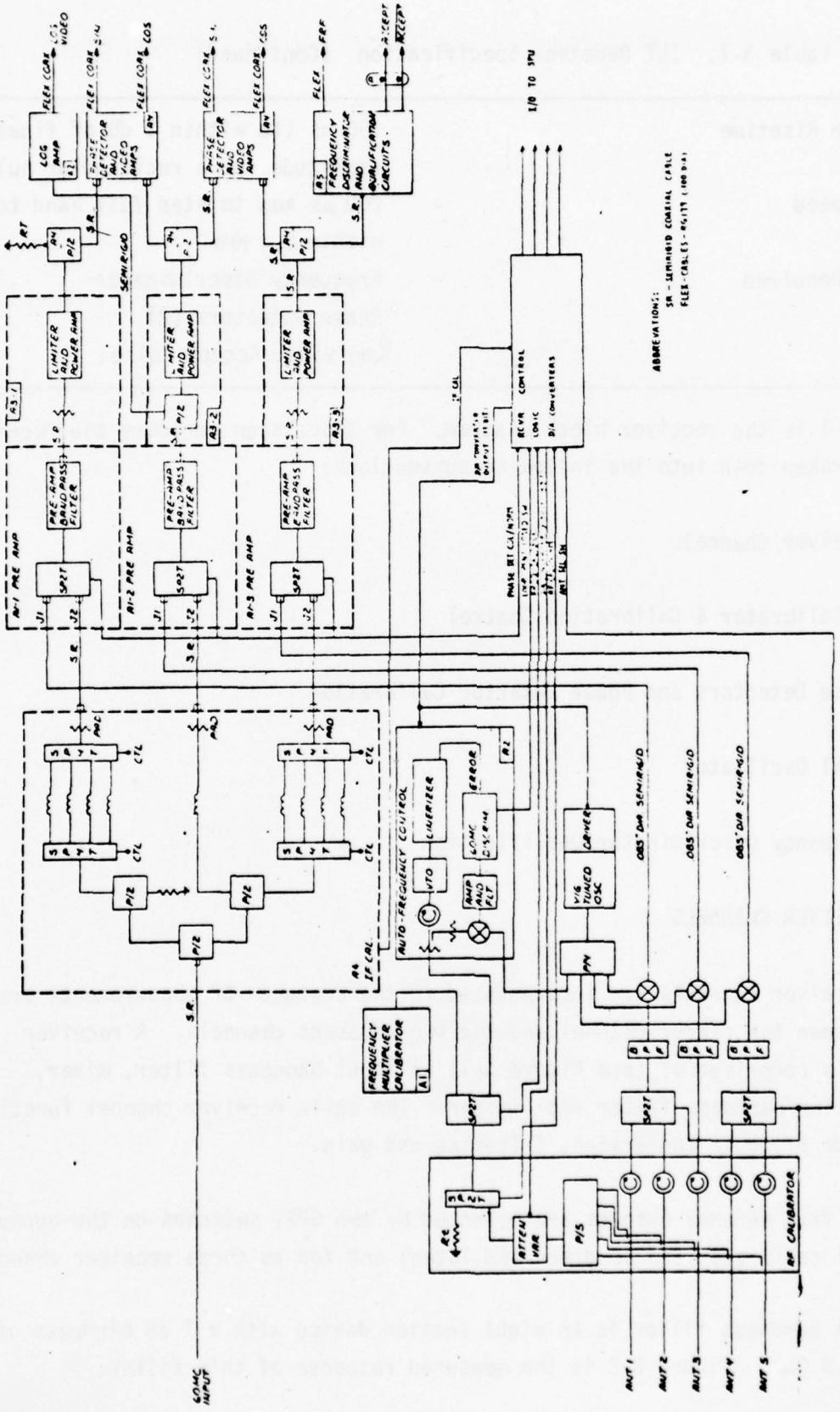


Figure 3-1. Receiver Block Diagram

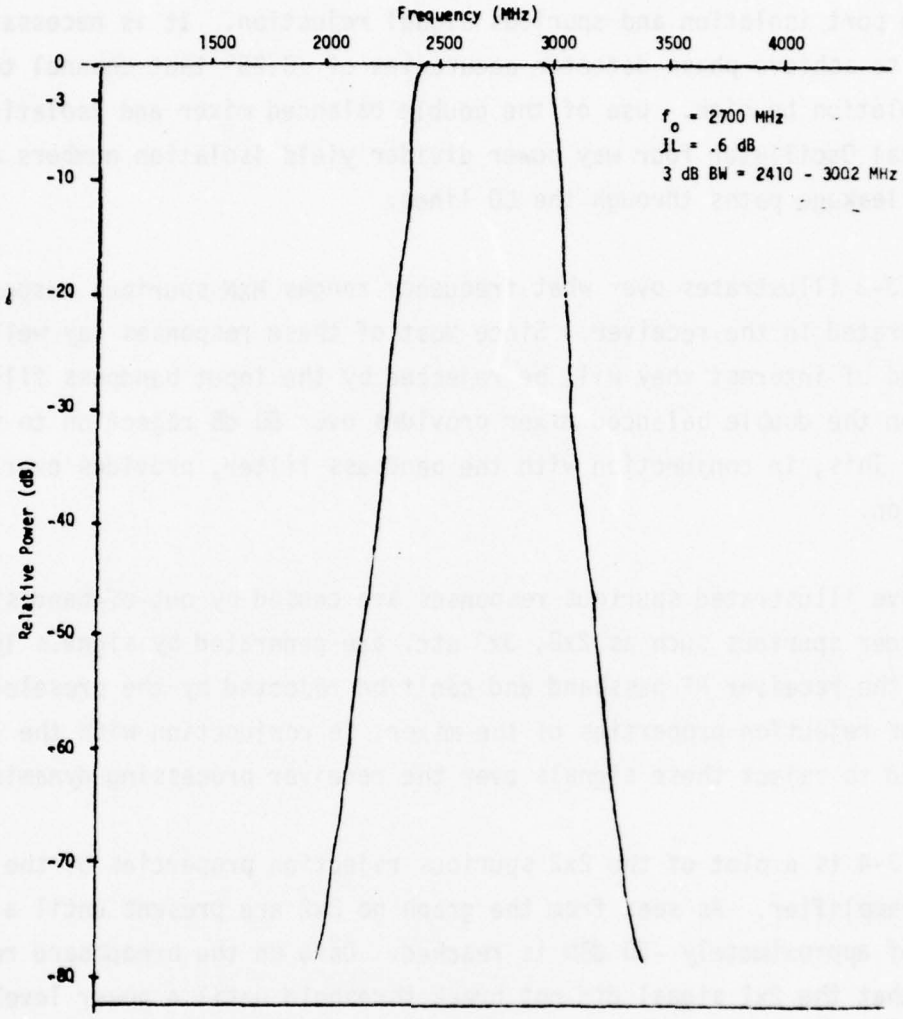


Figure 3-2. RF Bandpass Filter

3.1.1 Mixer

The mixer is double balanced. The double balanced mixer provides superior port to port isolation and spurious signal rejection. It is necessary when trying to achieve phase detector accuracies of ±0.25° that channel to channel isolation be high. Use of the double balanced mixer and isolation of the Local Oscillator four way power divider yield isolation numbers of >50 dB for leakage paths through the LO lines.

Figure 3-3 illustrates over what frequency ranges MxN spurious responses can be generated in the receiver. Since most of these responses lay well outside the band of interest they will be rejected by the input bandpass filter. In addition the double balanced mixer provides over 50 dB rejection to the listed spurs. This, in conjunction with the bandpass filter, provides over 80 dB rejection.

The above illustrated spurious responses are caused by out-of-band signals. Even order spurious such as 2x2, 3x3 etc. are generated by signals lying within the receiver RF passband and can't be rejected by the preselector. The spur rejection properties of the mixer, in conjunction with the IF filter, are used to reject these signals over the receiver processing dynamic range.

Figure 3-4 is a plot of the 2x2 spurious rejection properties of the mixer and preamplifier. As seen from the graph no 2x2 are present until a power level of approximately -30 dBm is reached. Data on the breadboard receiver shows that the 2x2 signal did not break threshold until a power level of -19 dBm was reached. Since this falls outside the specified operating dynamic range no circuitry dedicated to 2x2 or 3x3, etc., signal rejection was incorporated in the receiver.

3.1.2 Preamplifier

The preamplifier (A3-Assembly), in conjunction with the RF components, determine the receiver noise figure. The preamplifier is designed for a noise figure of less than 2.0 dB and a gain of 26 dB.

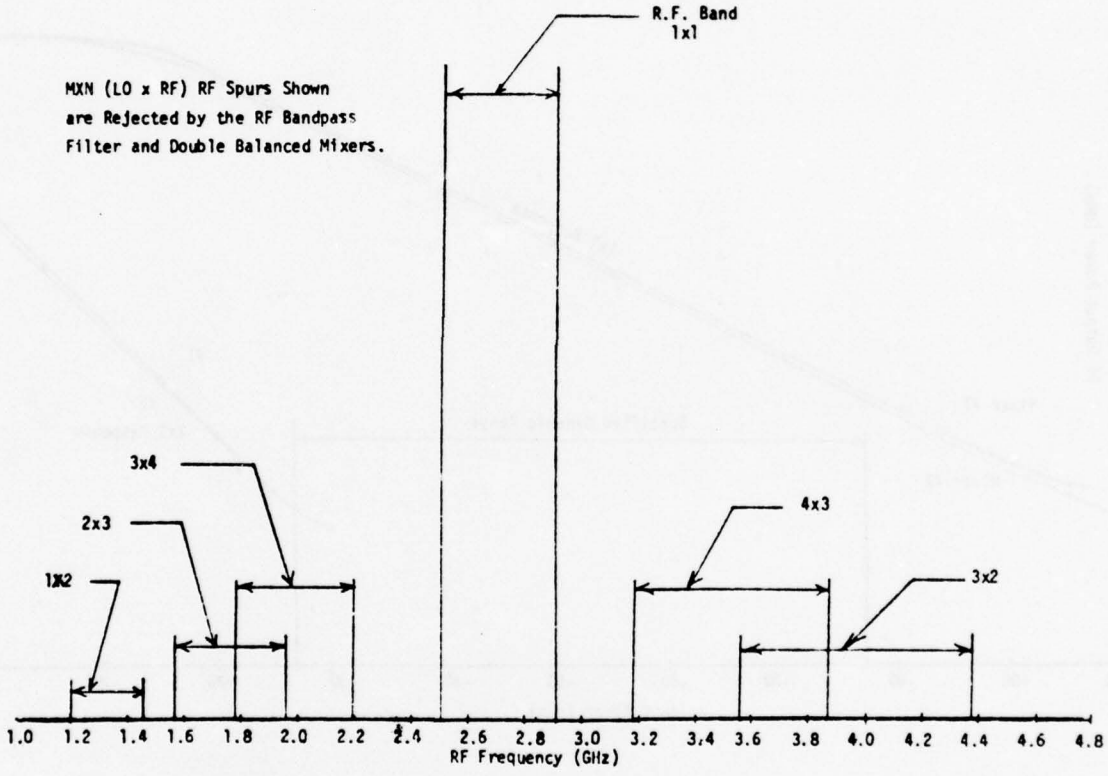


Figure 3-3. Spurious Response Chart

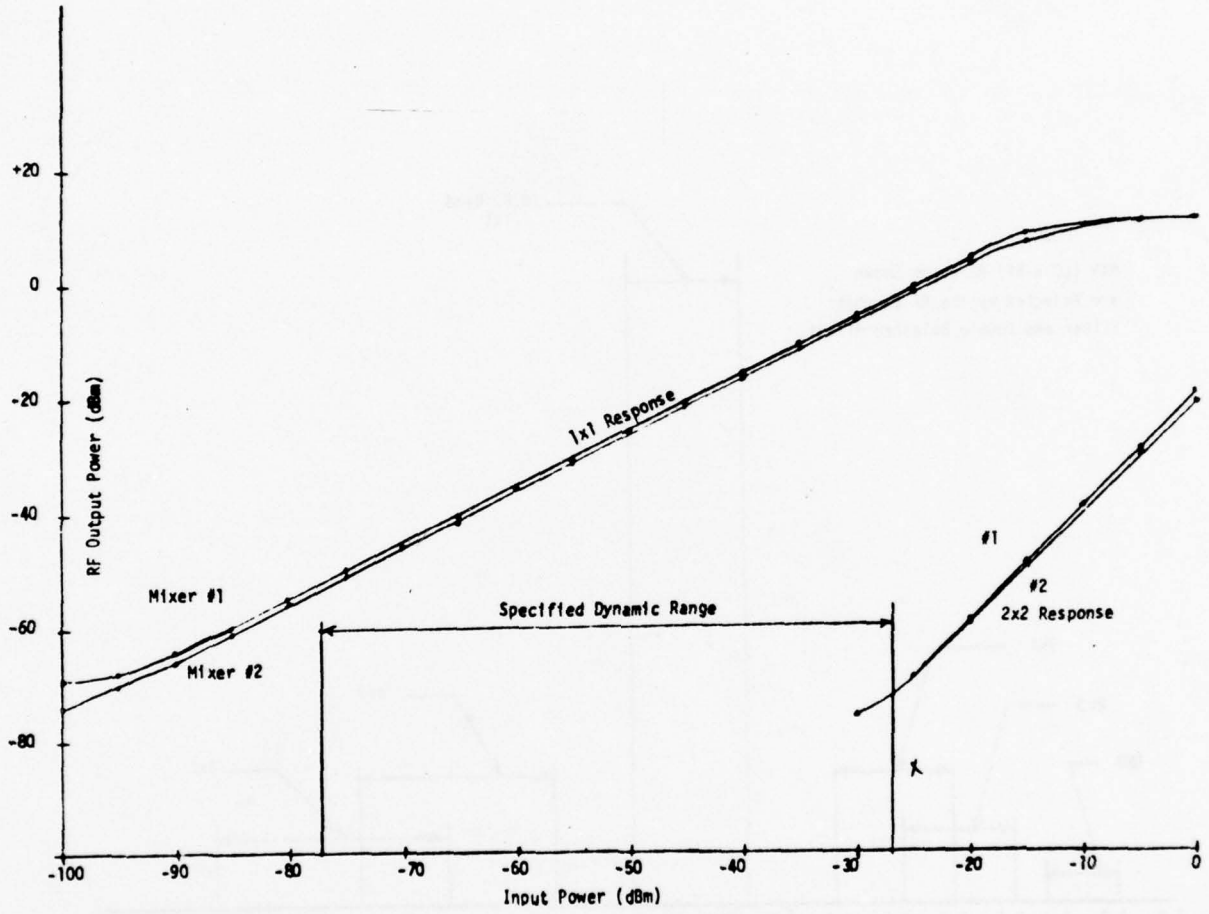


Figure 3-4. 2x2 Response

The IF filter is incorporated into the preamplifier design. This was done to place the IF filtering as close to the front end as possible to enhance spur rejection; but yet not significantly degrade the noise figure.

The IF filter is a three section device providing a 1-dB bandwidth of ±1 MHz and a 3-dB bandwidth of 3 MHz centered at 60 MHz. The normalized IF response curve for the breadboard amplifier is provided by Figure 3-5.

3.1.3 Limiter Amplifier

Phase Detector linearity and scale factor are sensitive to amplitude variations. It is therefore necessary that a limiting amplifier precede the Phase Detector. Additionally the limiter contributes a major portion of the receiver gain.

A brief list of the limiter specifications are given in Table 3-2.

Table 3-2
LIMITER AMPLIFIER SPECIFICATION

Gain	-	≥80 dB
Noise Figure	-	<10 dB
Output Power	-	≤+17 dBm min.
Phase Tracking	-	$\pm 1.5^{o}$ measured on breadboard units
Limiting Threshold	-	-70 dBm. Less than 0.2 dB output power variation over dynamic range from -60 dBm.
Center Frequency	-	60 MHz
Bandwidth	-	2 MHz 1 dB Min.
Input/Output Impedance	-	50Ω VSWR Max 2.0:1

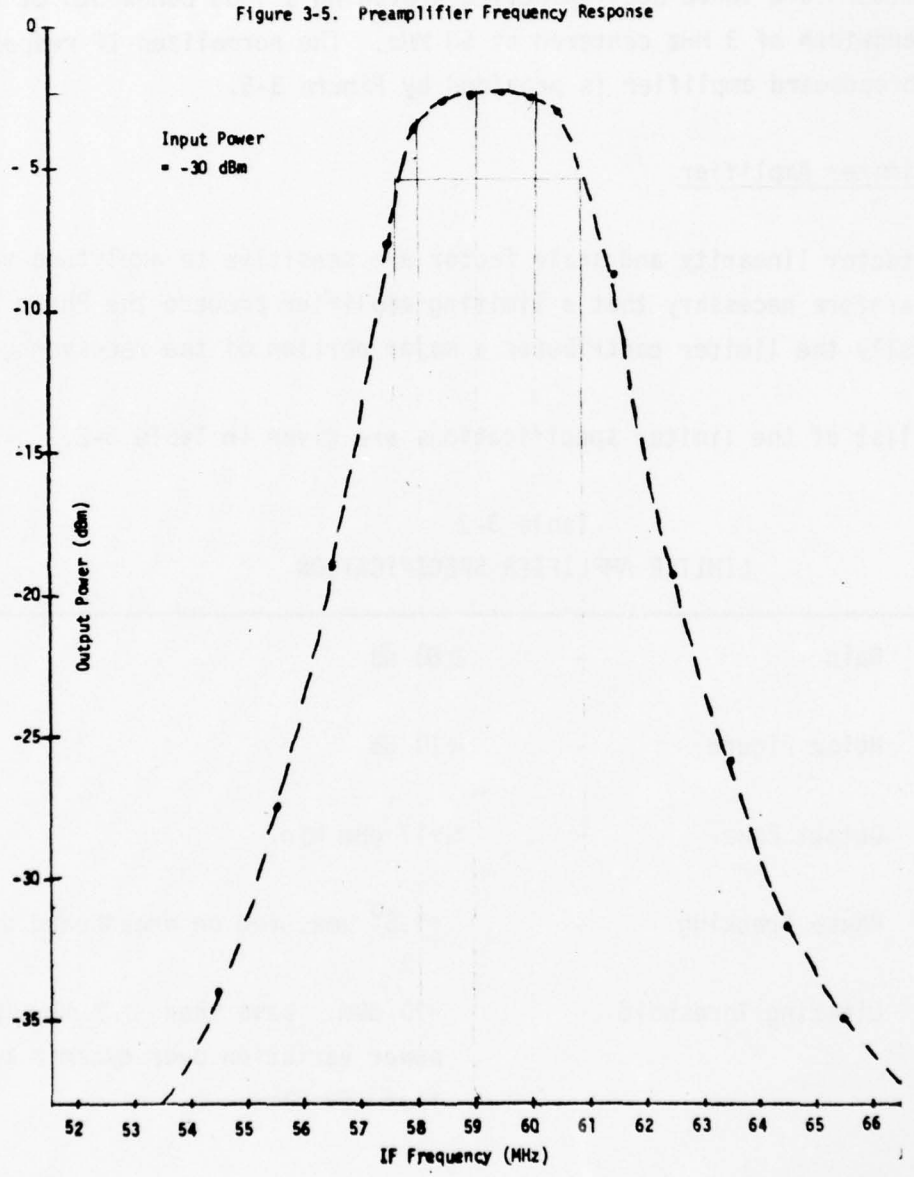


Figure 3-5. Preamplifier Frequency Response

Limiter performance is illustrated by Figure 3-6, (phase tracking and output power, vs input power), for the two breadboard units.

The breadboard limiter amplifiers were constructed using discrete components. The final circuit will be a thin - film hybrid.

Bandpass filters are used on the output of each limiter to remove harmonic power.

In addition to the gain and filtering requirements of the receiver channels the phase performance of the receiver channels is important. Phase tracking of all the passive components is specified to within ±1°. The active circuits do not achieve this accuracy over their dynamic range. Figure 3-7 is a plot of the phase tracking of the receiver channels over the input signal dynamic range. It demonstrates the need for pulse-to-pulse calibration of the receiver. To do this a calibration signal of 0° phase is injected via the RF calibration circuit (described in the next section). The calibration signal amplitude is set by computer control via the SPU to the same amplitude as the signal pulse. Specifically, the SPU A/D converts the log video signal output of the receiver to a digital word and enters it into the computer as part of the 128-bit data word. The computer then outputs the D/A command word to set the RF signal calibration attenuators. Since the phase of the calibration signal is 0°, the receiver can be calibrated on a pulse-to-pulse basis for phase fluctuations due to signal amplitude.

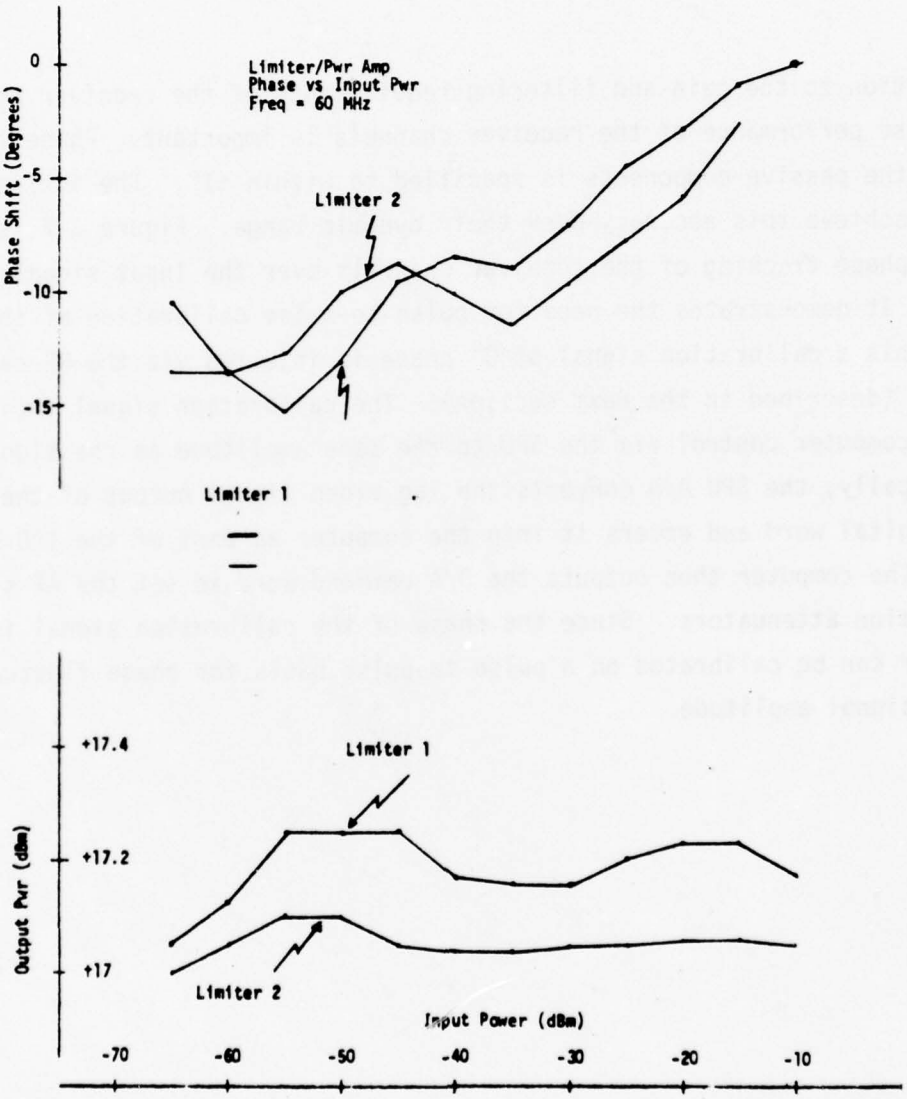


Figure 3-6. Limiter Performance

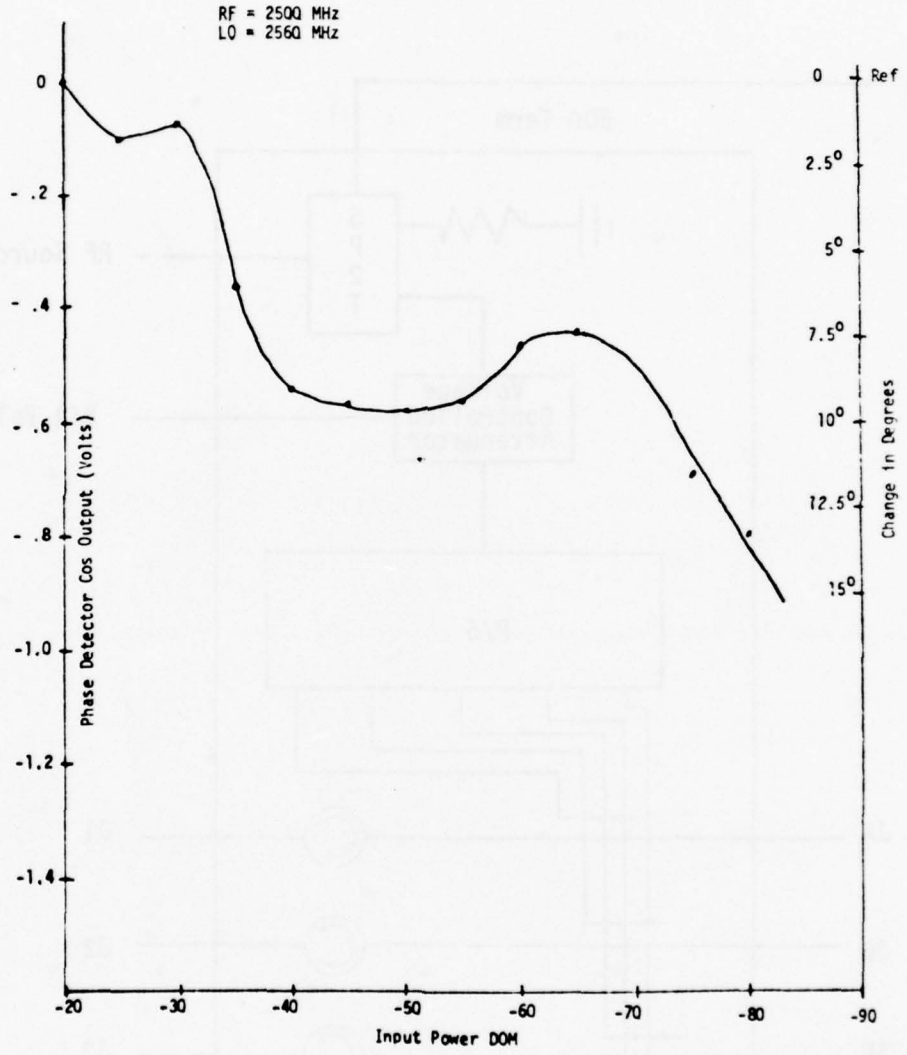


Figure 3-7. Receiver Phase Tracking Error vs Input Power

3.2 RF CALIBRATOR

The RF signal calibrator provides the means whereby receiver phase tracking errors that vary with time, frequency, and signal amplitude can be removed from the phase angle measurements. The block diagram is shown in Figure 3-8. Its orientation to the overall receiver is shown in Figure 3-1.

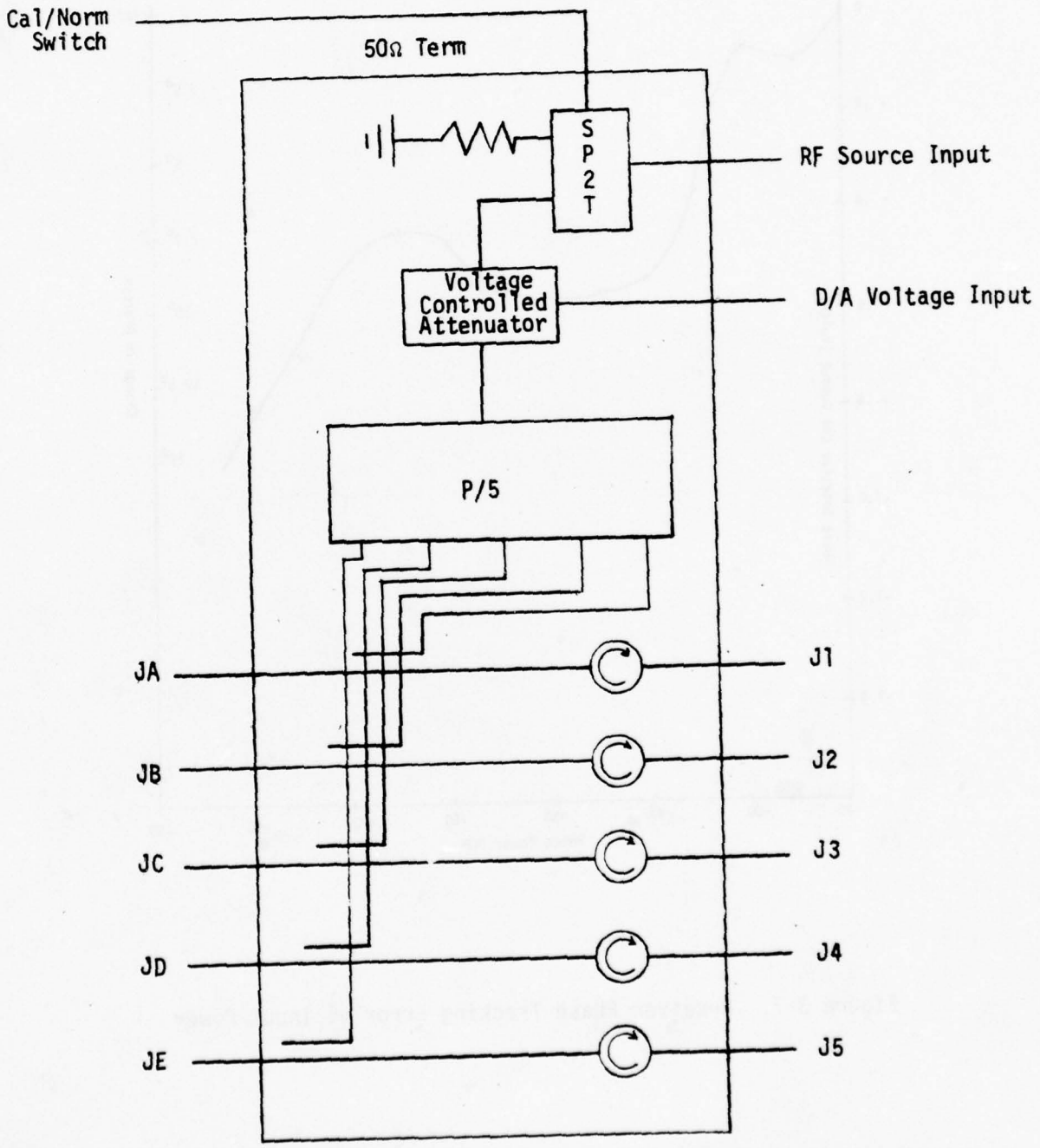


Figure 3-8. RF Signal Calibrator Block Diagram

There are three modes of operation for the calibrator. A termination mode where the RF input signal to the calibrator is fed into a 50Ω load, and the antenna signals directly into the receiver with no other signals coupled in. A 0^{o} calibration mode in which the calibrator RF signal is fed to a 5-way power splitter to produce four signals of equal phase. A frequency calibration mode in which signals are applied to the RF calibrator from the frequency multiplier/ calibrator assembly.

Mode control is provided by a switch internal to the RF calibrator and an external switch to select the RF source or frequency multiplier.

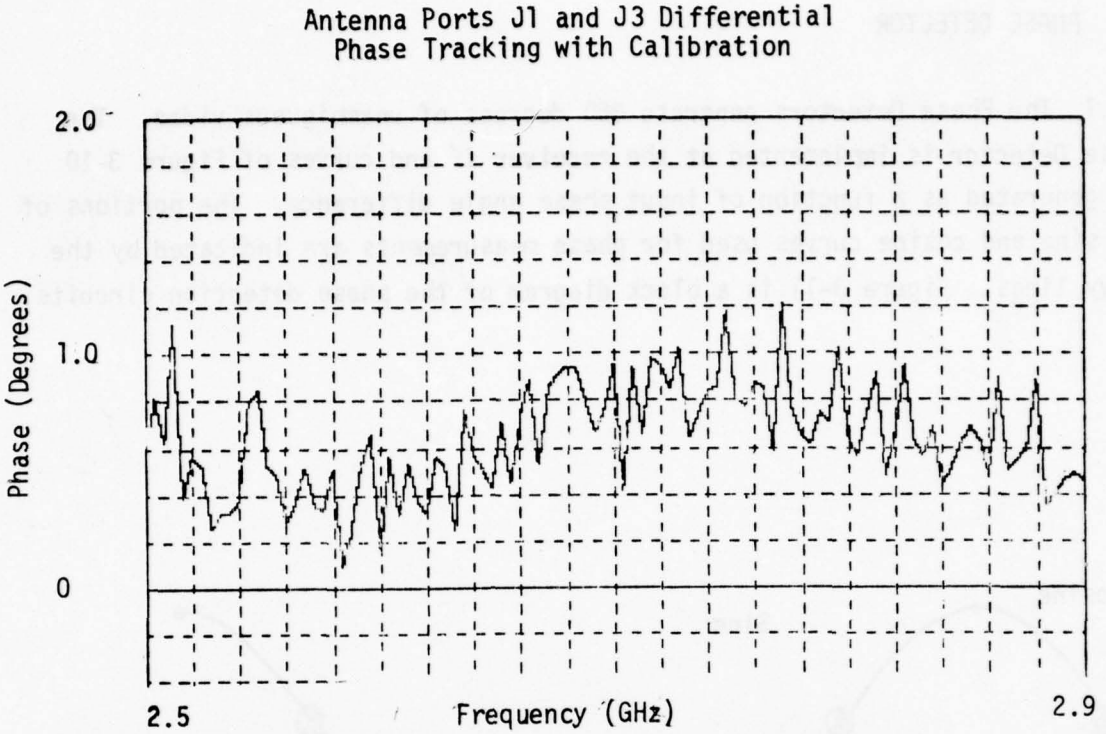
Ideally, it is desired to have the output of the phase detectors be 0^{o} for a 0^{o} input signal. This is difficult or impossible to do over the input frequency range and signal dynamic range. Therefore the calibration is used to remove phase tracking errors through the receiver. The calibration is inserted following each signal pulse. In normal operation the calibration signal will be adjusted to the amplitude and frequency of the incoming preceding pulse. The amplitude of the calibration signal is controlled by an internal voltage controlled attenuator. The attenuator is controlled by an 8-bit D/A converter with a nominal control of 6 dB/volt. The LSB is 1/4 dB. Frequency control is provided by a frequency locked loop and will be discussed in detail in Subsection 3.5.

The phase performance of the calibrator is critical to the performance of the receiver. Any error in the 0 degree input adds directly to the system phase error budget. The major specifications to which Anaren designed the calibrator are given in Table 3-3.

The calibrator was initially evaluated on an H.P. Automatic Network Analyzer prior to installation into the receiver breadboard. Figure 3-9 illustrates the performance of a typical pair of phase channels with calibration. The peak to peak error is 0.8^{o}. The bias or constant offsets of the curves are removed by receiver calibration.

Table 3-3
CALIBRATOR SPECIFICATIONS

Frequency	-	2.5 GHz to 2.9 GHz
VSWR	-	1.4:1 max input-output ports
Insertion Loss	-	1.0 dB max - input - output ports 37-40 dB - calibrator to output ports
Isolation	-	50 dB min - input to input ports
Directivity	-	Output phase not to vary more than $\pm 1.2^{o}$ with VSWR's applied to any input port or all 15 varied from 1.0:1 to 2.0:1
Phase Tracking	-	$\pm 1.0^{o}$
Amplitude Tracking	-	±0.2 dB
0^{o} Mode	-	0° ± 0.4 dB at output ports. $0^{o} \pm 1.0^{o}$ at output ports
Attenuation	-	60 dB continuous dynamic range.



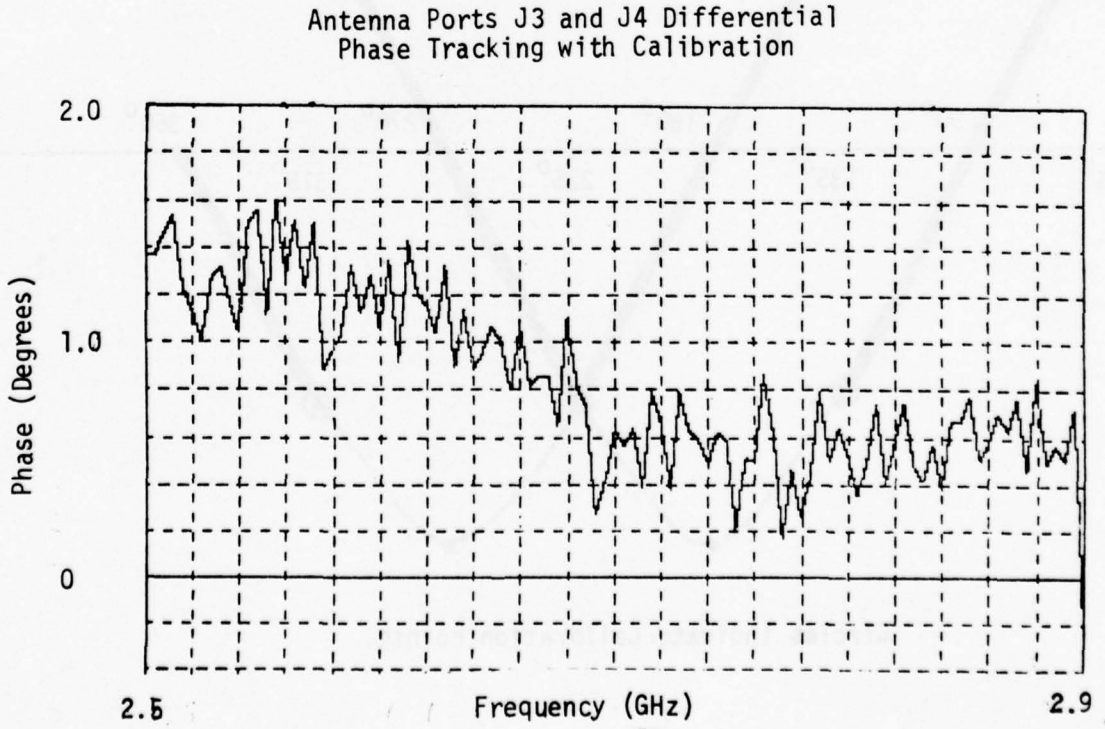
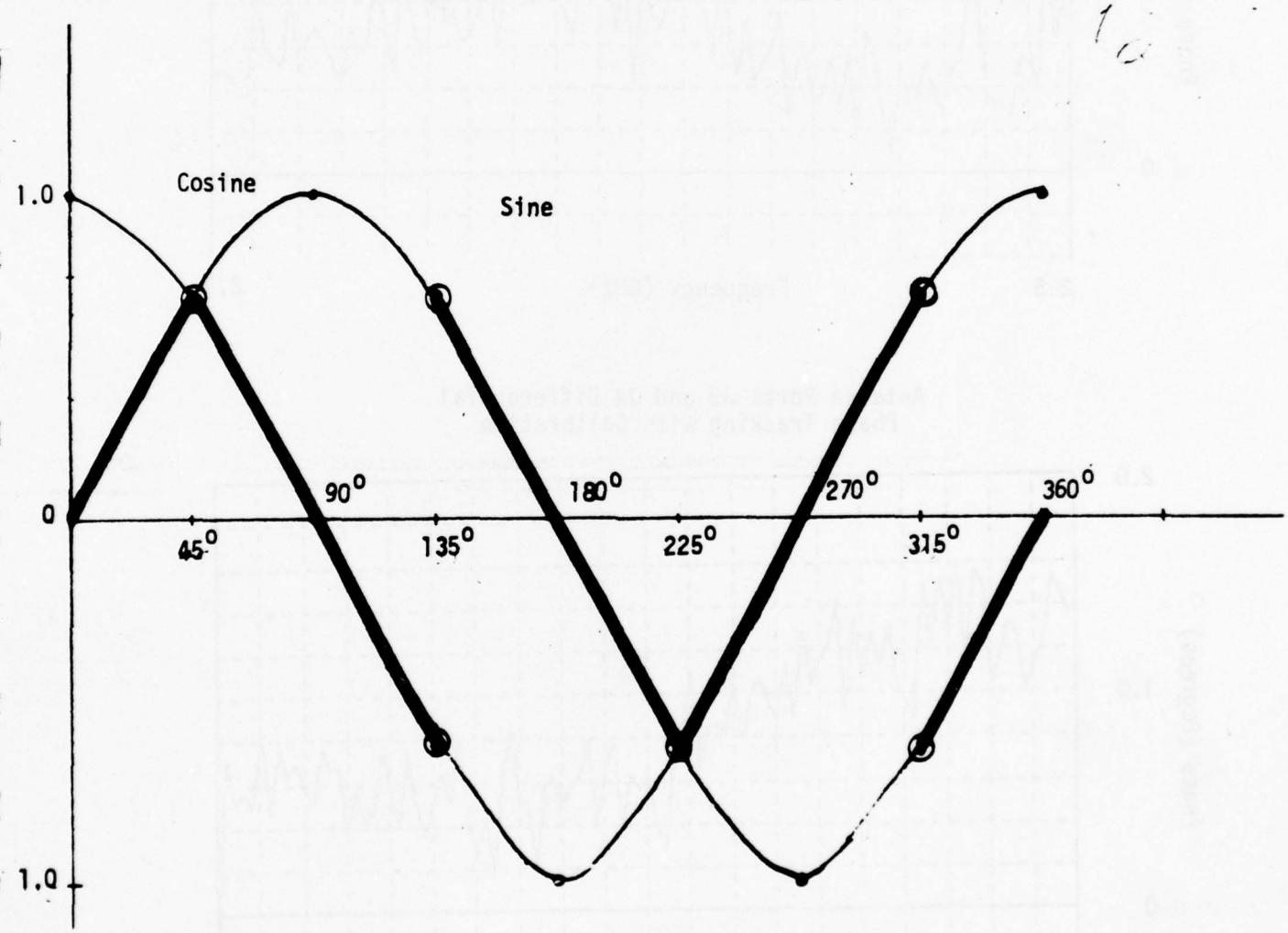


Figure 3-9. RF Calibrator Performance

3.3 PHASE DETECTOR

3.2.1 The Phase Detectors generate 360 degrees of unambiguous video. The Phase Detector is implemented at the receiver IF and curves of Figure 3-10 are generated as a function of input phase angle difference. The portions of the sine and cosine curves used for phase measurements are indicated by the heavy lines. Figure 3-11 is a block diagram of the phase detection circuits.



Circles indicate Calibration Points.

Figure 3-10. Phase Detector Sine-Cosine Curves

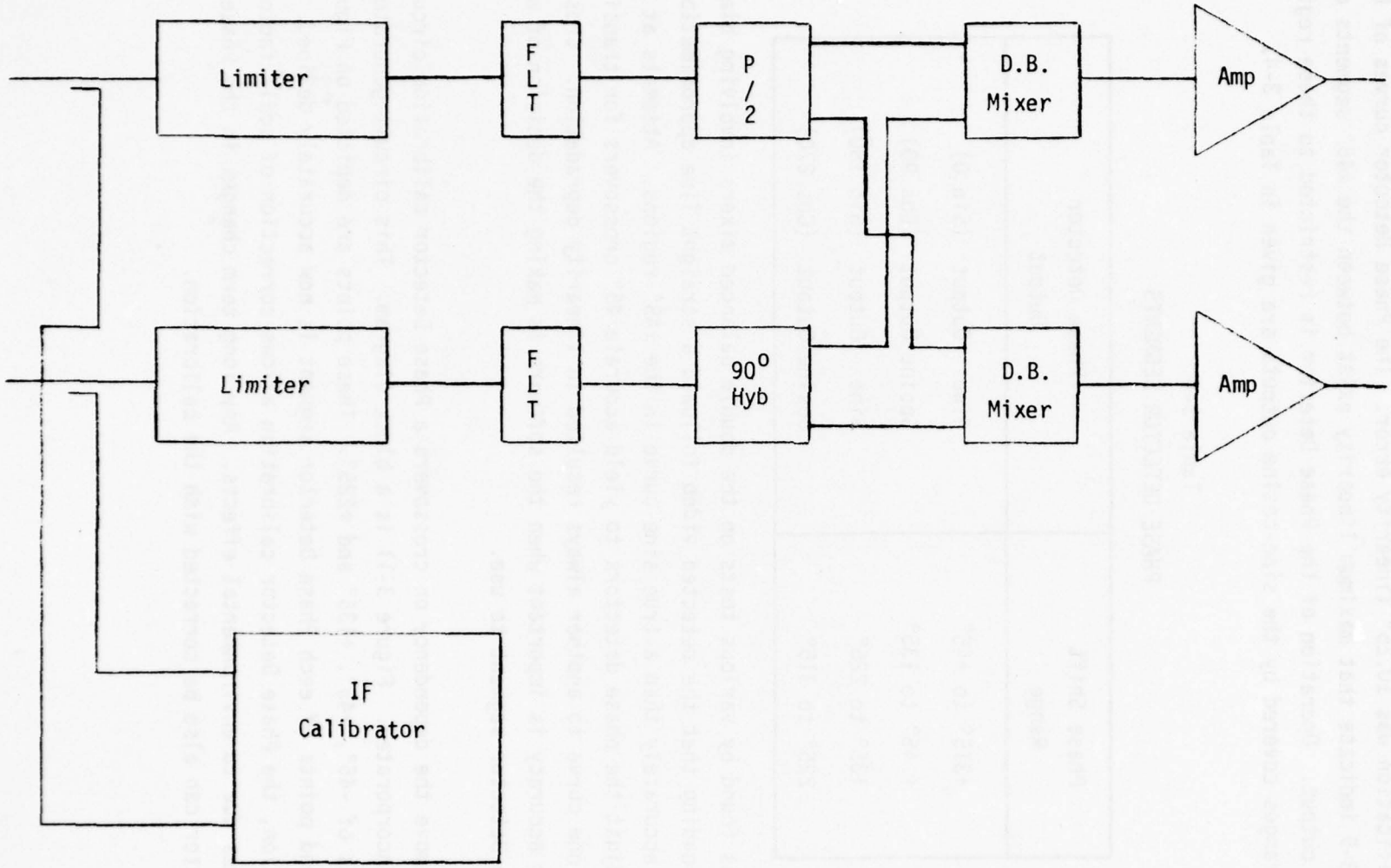


Figure 3-11. Phase Channel Block Diagram

The critical parameter in the Phase Detector design is linearity. The design specification was ±0.25° linearity error. The Phase Detector curves of Figure 3-9 indicate that maximum linearity exist between the ±45° segments of each output. Operation of the Phase Detector is restricted to these regions. The ranges covered by the sine-cosine outputs are given in Table 3-4.

Table 3-4
PHASE DETECTOR SEGMENTS

Phase Shift Range	Phase Detector Output
+315° to +45°	Sine Output (Sin 0)
+ 45° to 135°	Cosine Output (Cos 90)
135° to 225°	Sine Output (Sin 180)
225° to 315°	Cosine Output (Cos 270)

It was found by various tests on the double balanced mixers involving biasing and loading that the detected video followed a straight line approximation more accurately than a true sine curve in the ±45° regions. Attempts at trying to adjust the phase detectors to yield accurate 45° crossovers for transition from one curve to another always resulted in linearity degradation. Crossover point accuracy is important when the software is making the decision of which Phase Detector segment to use.

To remove the dependency on crossovers a Phase Detector calibration circuit was incorporated. Figure 3-11 is a block diagram. This circuit generates phase shifts of -45°, +45°, +135° and +225°. These points are depicted on Figure 3-10. The end points of each Phase Detector segment is now accurately defined. In addition, the Phase Detector calibration allows correction of scale factor changes due to environmental effects. Any long term changes in the Phase Detector can also be corrected with the calibration.

The Phase Detector linearity is illustrated by Figures 3-12 and 3-19. This data includes input signal power and temperature variations. These data show that software calibration can significantly improve performance.

Table 3-5 summarizes the worse case errors as read from these curves.

Table 3-5
PHASE DETECTOR ERRORS

Phase Detector Curve	Errors (Degrees)			
	Typical	Worse Case	Typical	Worse Case
	At 0° & 25°C	Over Temp Range of 0° 25°C	At 60° 85°C	Over Temp Range +60°C +85°C
Sin 0	±0.2°	-0.36° + 0.4°	±0.4°	-0.8° +0.6°
Cos 90	±0.1°	-.027° + 0.33°	±0.1°	-0.38° +0.25°
Sin 180	-0.5°	-0.8° + 0.1°	±0.6°	-0.9° +0.25°
Cos 270	±0.1°	-0.3° + 0.35°	±0.15°	-0.38° +0.15°

NOTE: The data contains an estimated ±0.2° error due to test equipment and operator.

The monopulse noise error of the Phase Detector as a function of input signal power is given by Figure 3-20. Table 3-6 summarizes this data and compares it to the specification.

Table 3-6
MONOPULSE PHASE DETECTOR ERROR

Input Power	P-P Phase Noise (Spec)	P-P Phase Noise Measured
-75.5 dBm	34° P-P	28° P-P
-66.5 dBm	11.4° P-P	9.3° P-P
-56.5 dBm	3.4° P-P	2.8° P-P

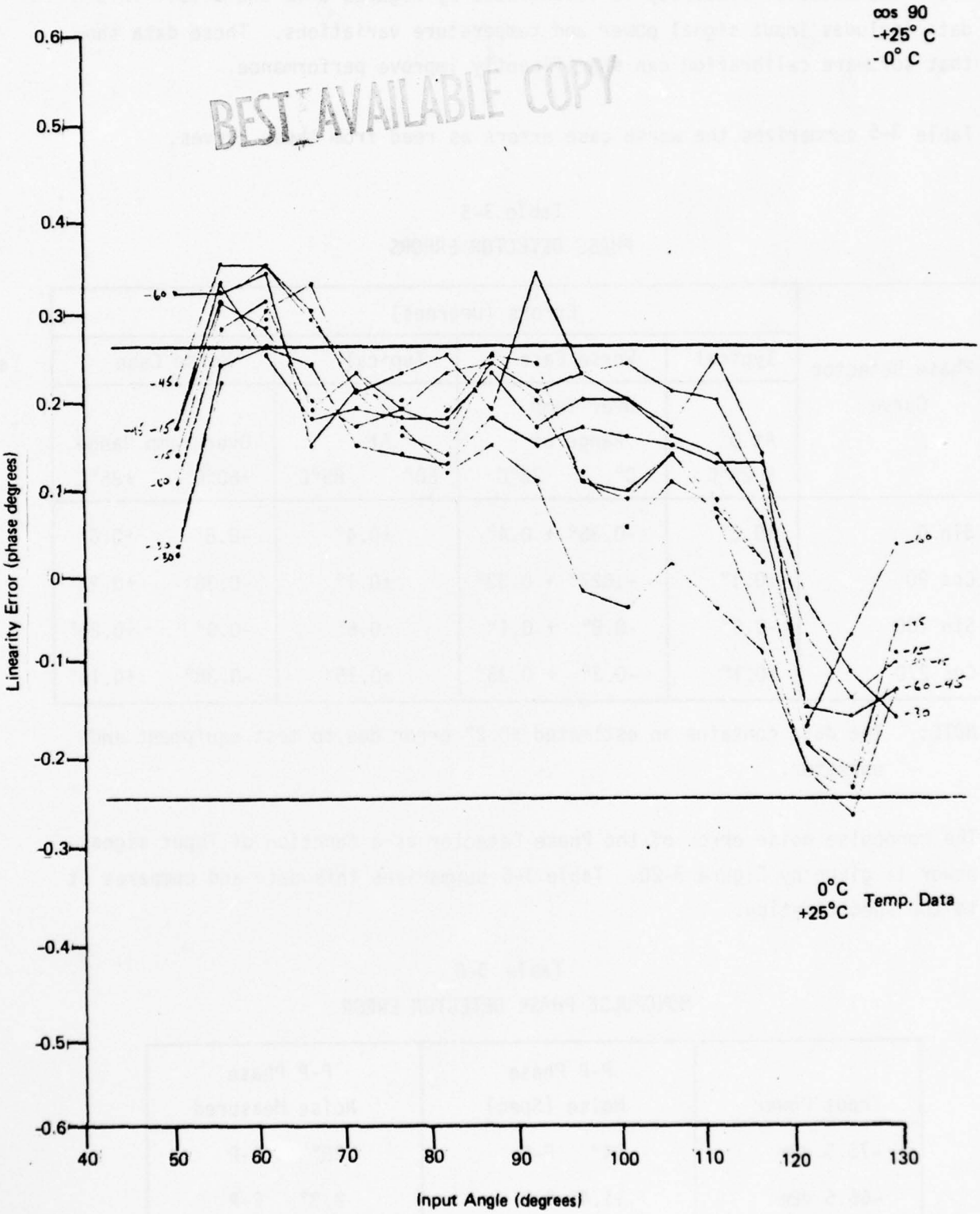


Figure 3-12. Phase Detector - Cosine 90° Output

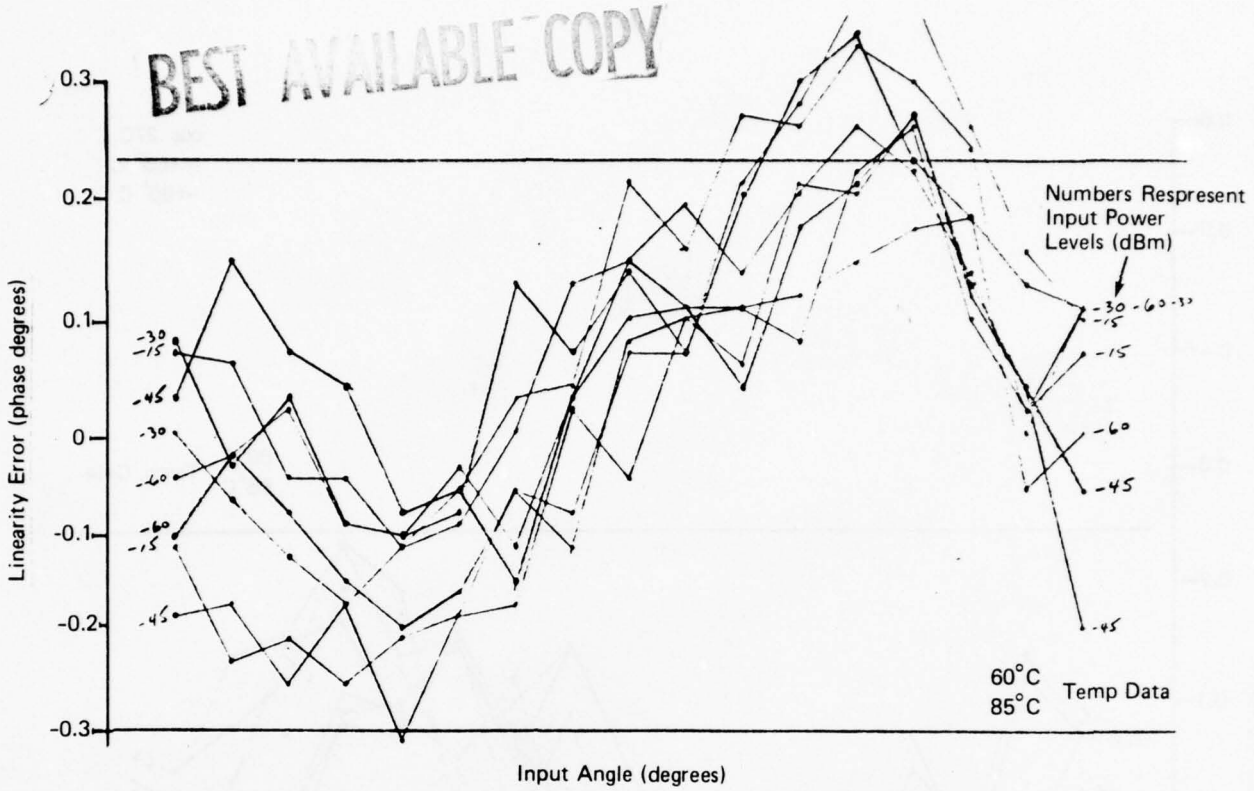


Figure 3-13. Phase Detector - Cosine 90° Output

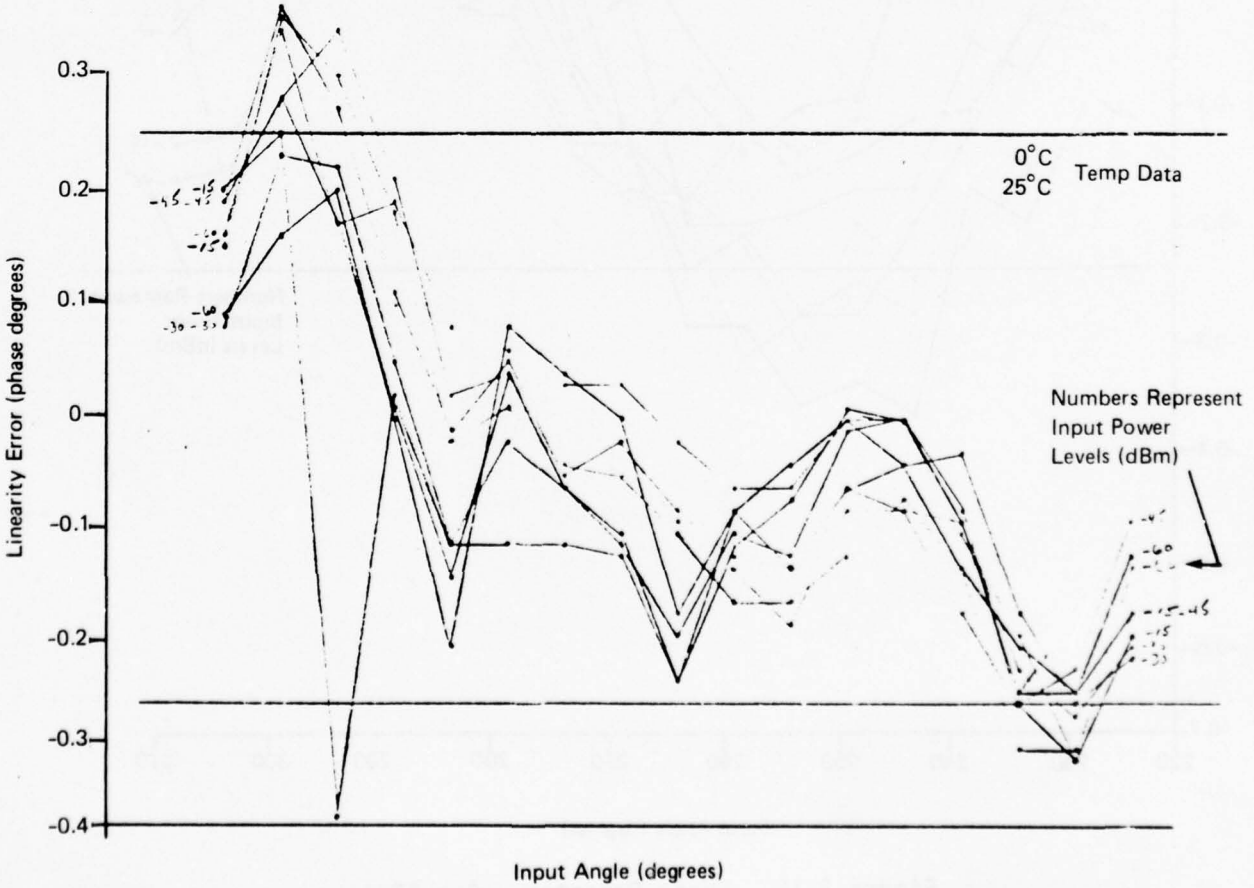


Figure 3-14. Phase Detector - Cosine 270° Output

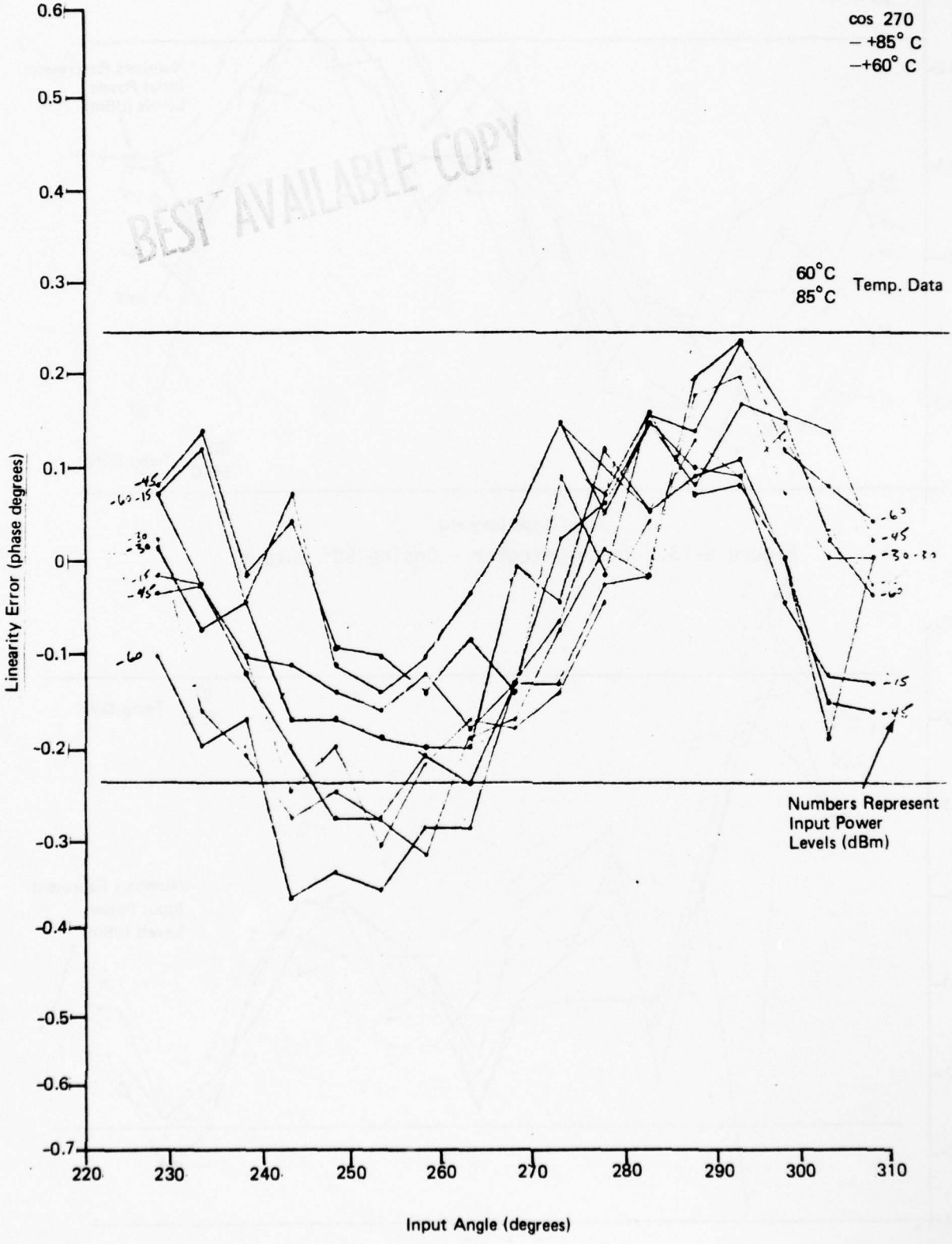


Figure 3-15. Phase Detector - Cos 270°

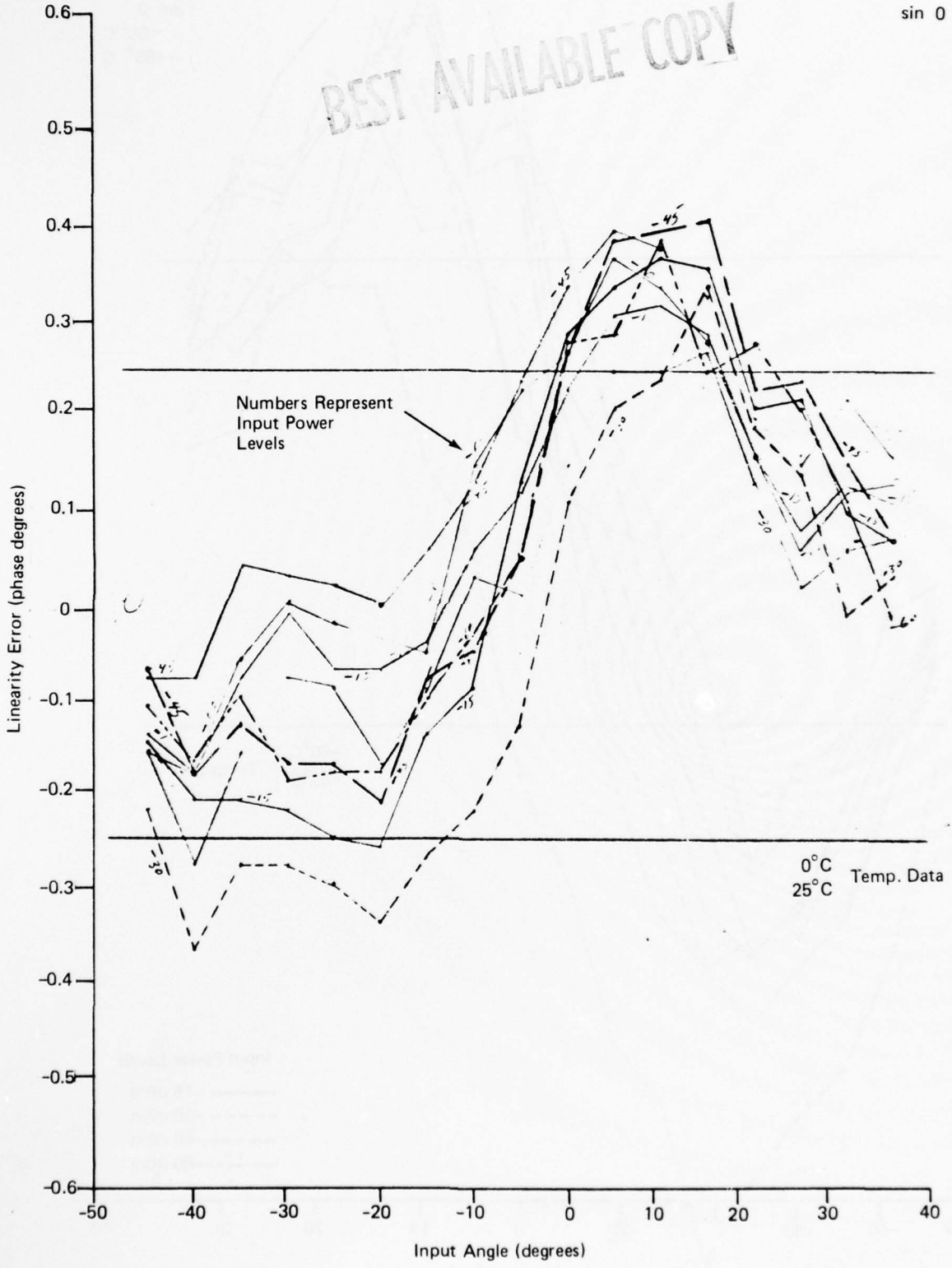


Figure 3-16. Phase Detector - Sin 0° Output

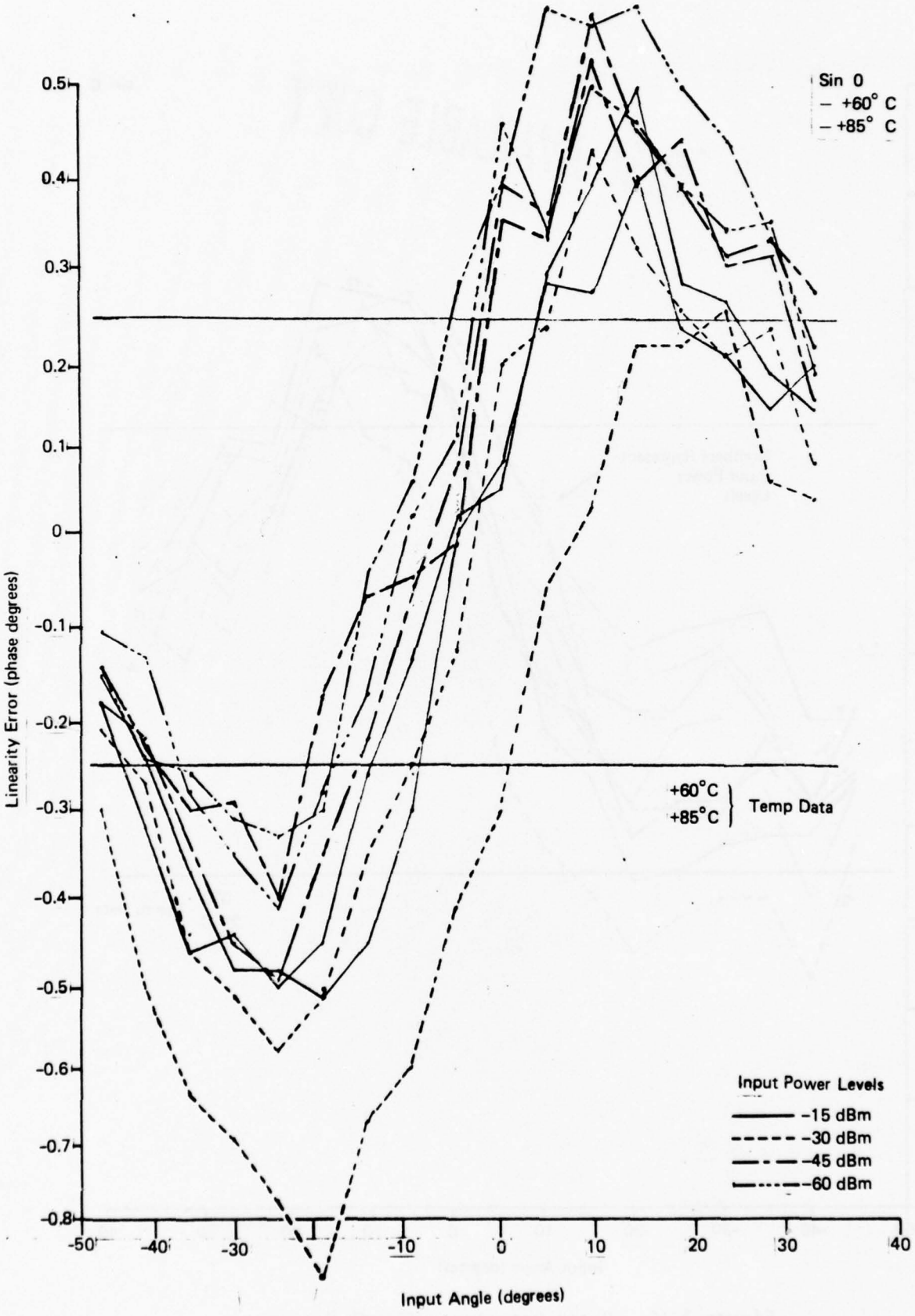


Figure 3-17. Phase Detector - Sin 0° Output

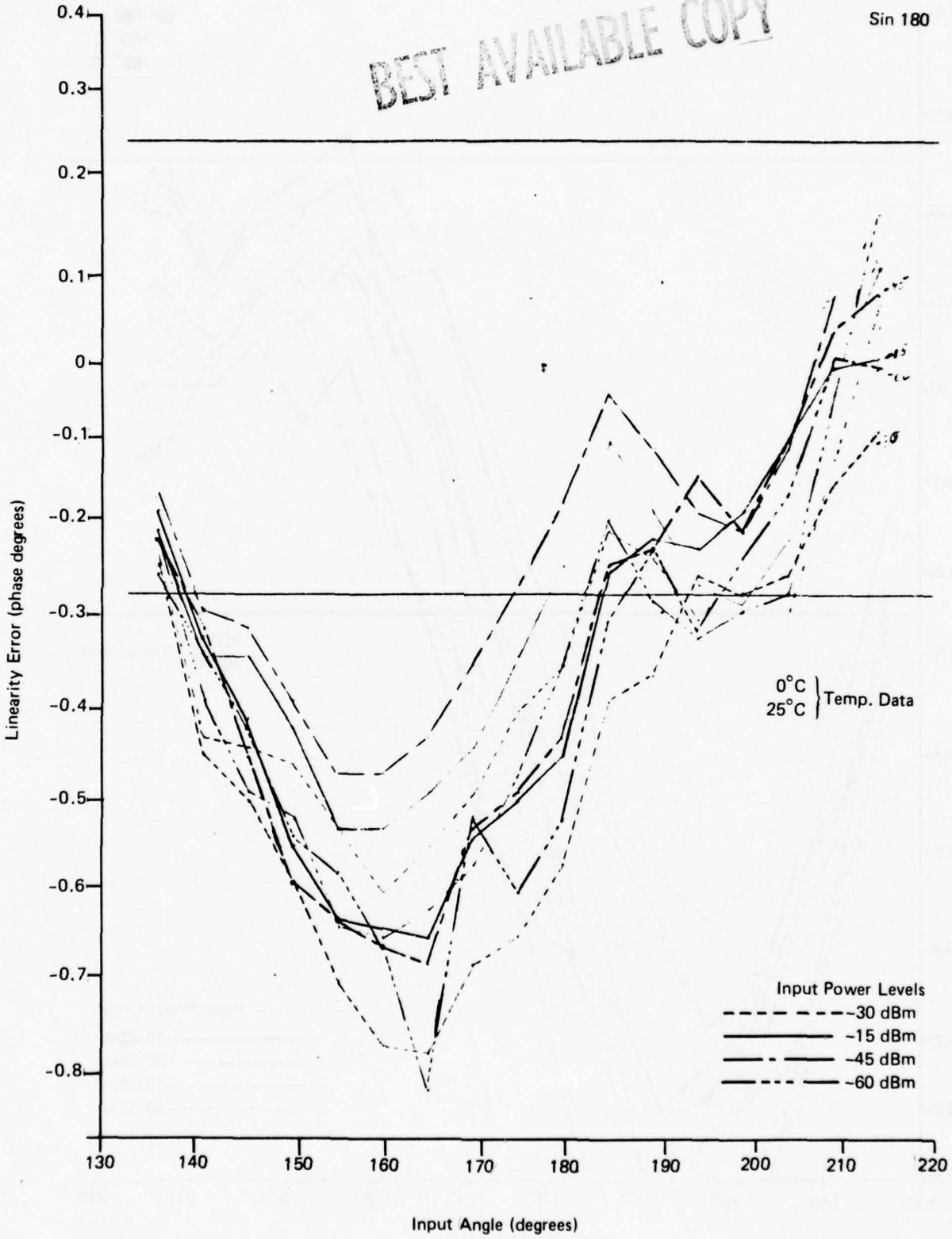


Figure 3-18. Phase Detector - Sin 180° Output

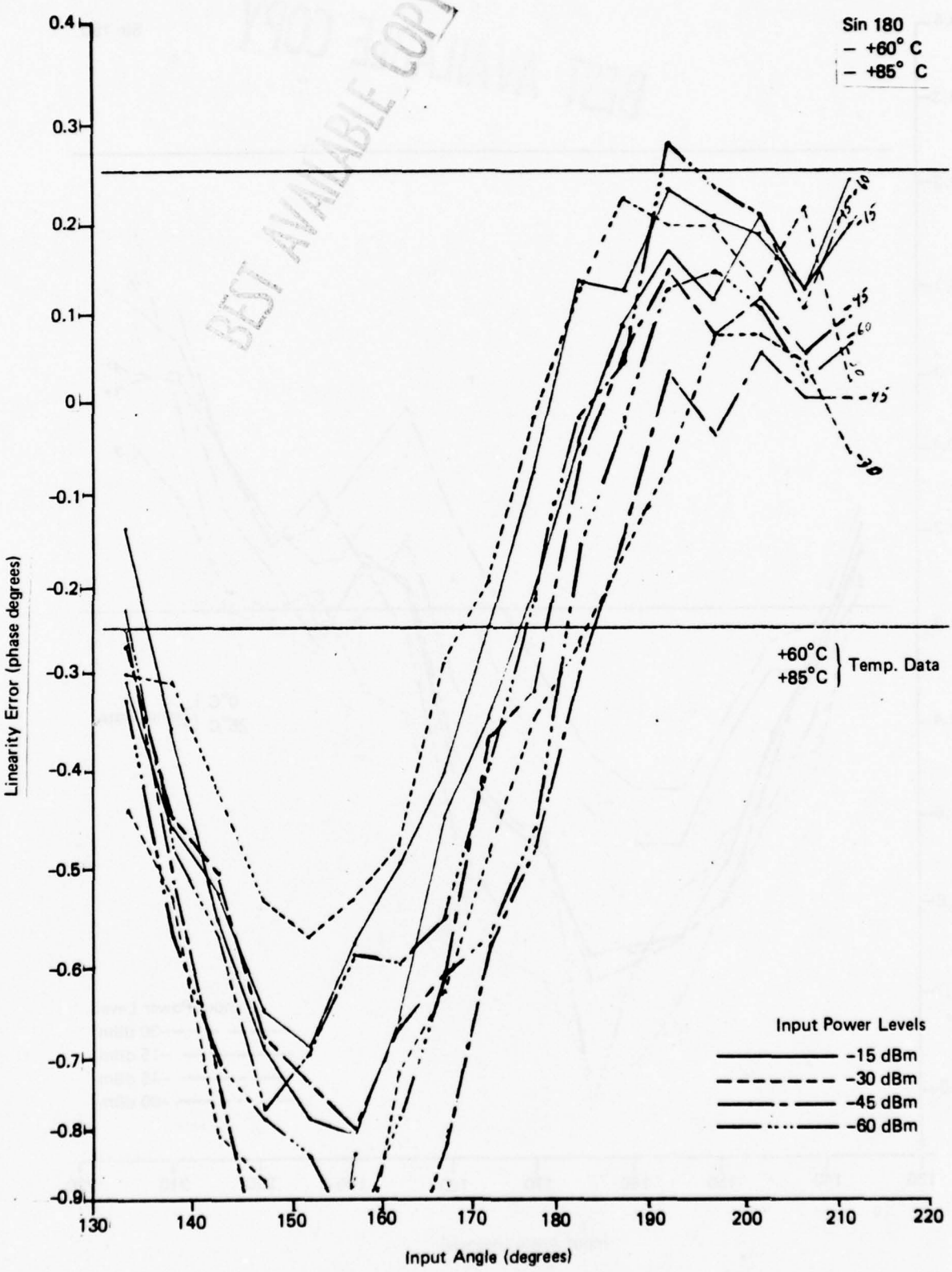


Figure 3-19. Phase Detector - Sin 180° Output

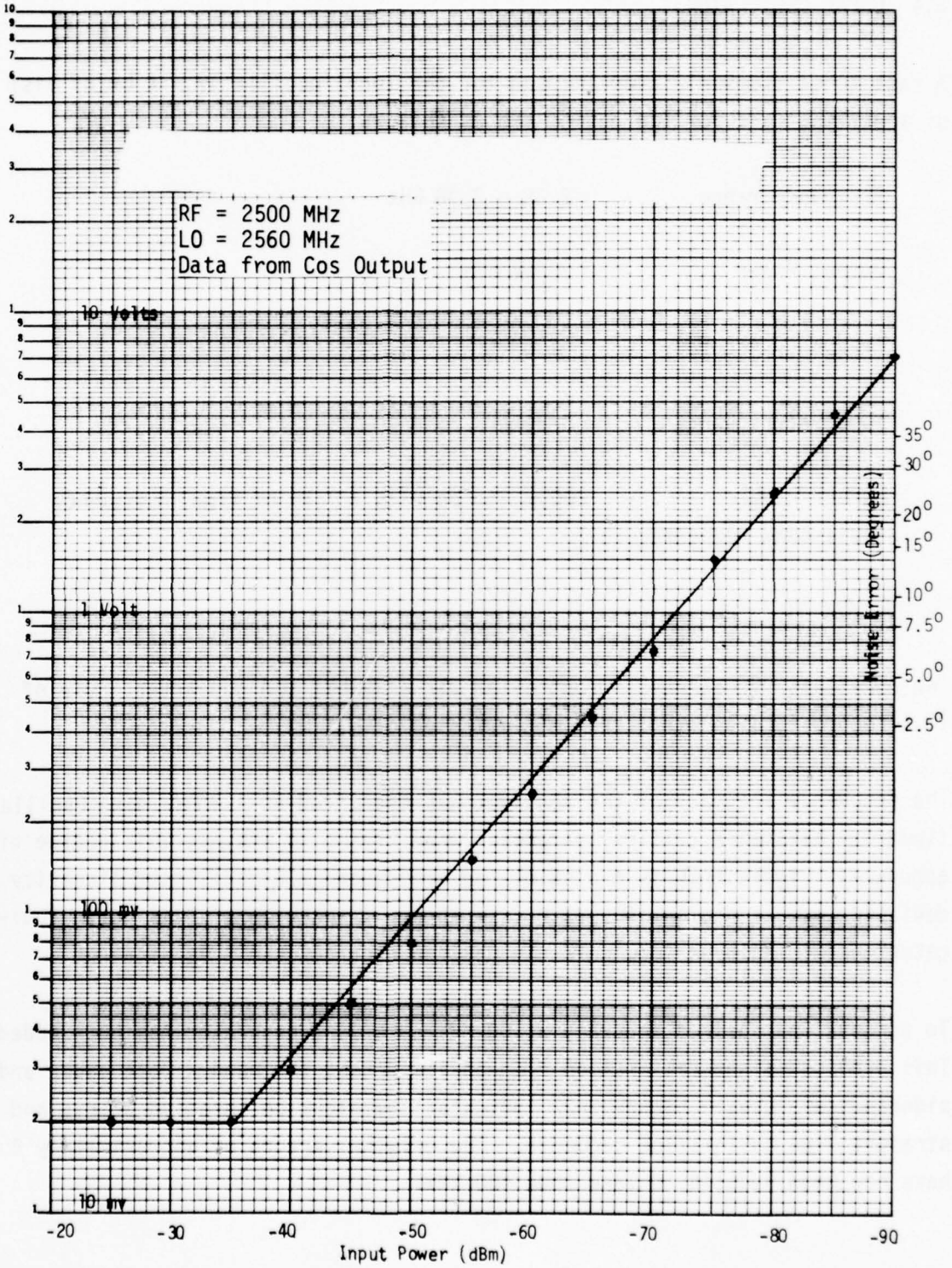


Figure 3-20. Monopulse Phase Noise vs Input Signal Power

3.4 LOCAL OSCILLATOR

A fast tuned YIG Oscillator is used for the local oscillator. A brief list of specifications for the device are as follows:

Frequency range	-	2.38 - 2.78 GHz
Output Power	-	30 mW min
Frequency Accuracy	-	$\pm$2.5 MHz
Temperature Range	-	0-71^{o}C
Tuning Speed (Full Band Response)	-	200 μs to be within 0.1% of final frequency
Tuning Voltage	-	0-10.2375 V

The oscillator frequency is controlled via a 12-bit D/A converter. Use of 12 bits provides an oscillator minimum step of 0.1 MHz.

The frequency accuracy of the receiver was specified as 1.8 MHz max. Oscillator linearity becomes a critical parameter when trying to achieve this degree of accuracy. Figure 3-21 is a plot of the breadboard YIG oscillator linearity deviation as a function of output frequency. Inspection of this curve indicates that in an open loop case the desired accuracy can't be attained.

To achieve the desired accuracy a 100-MHz comb line generator has been added. This provides eight calibration frequencies across the band. Both upper and lower sidebands are used. Figure 3-22 indicates the eight calibration points and the straight line calibration segments. The original errors of approximately 4 MHz have now been reduced to less than 400 kHz.

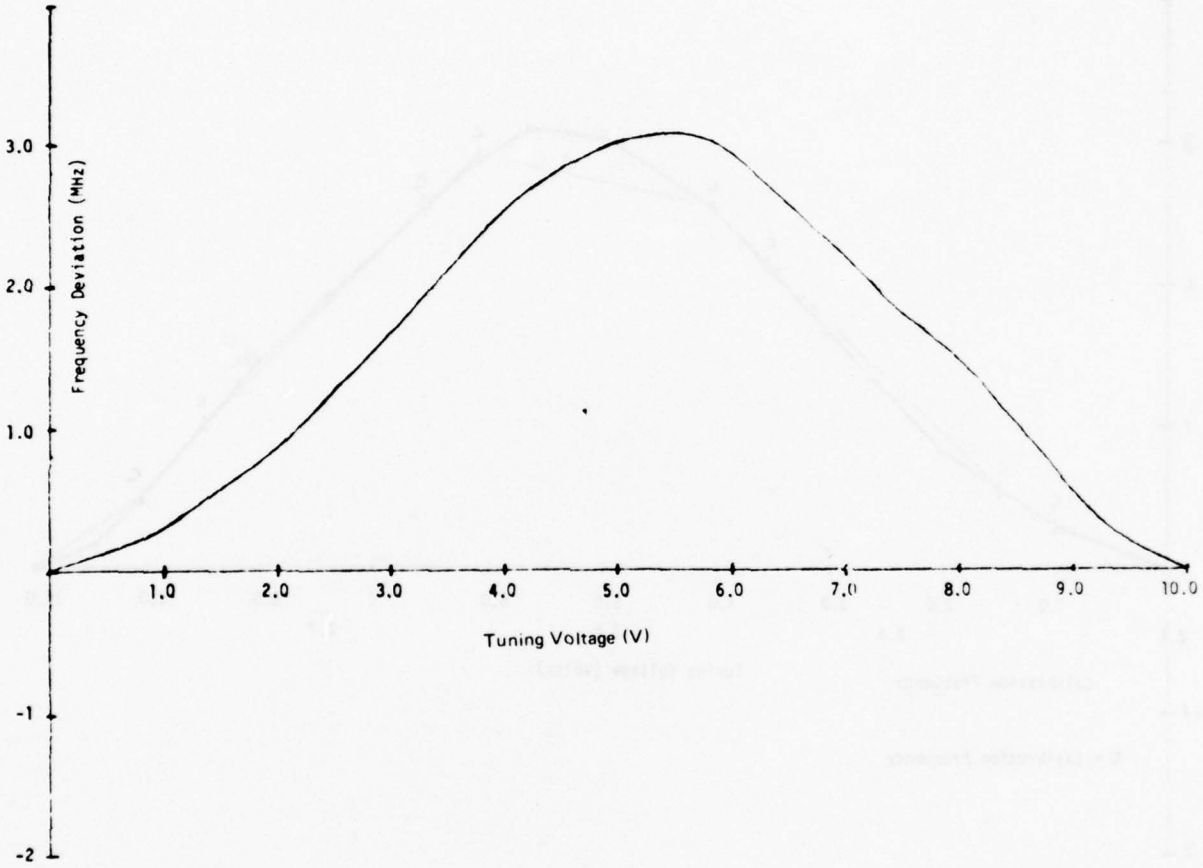


Figure 3-21. Local Oscillator Linearity

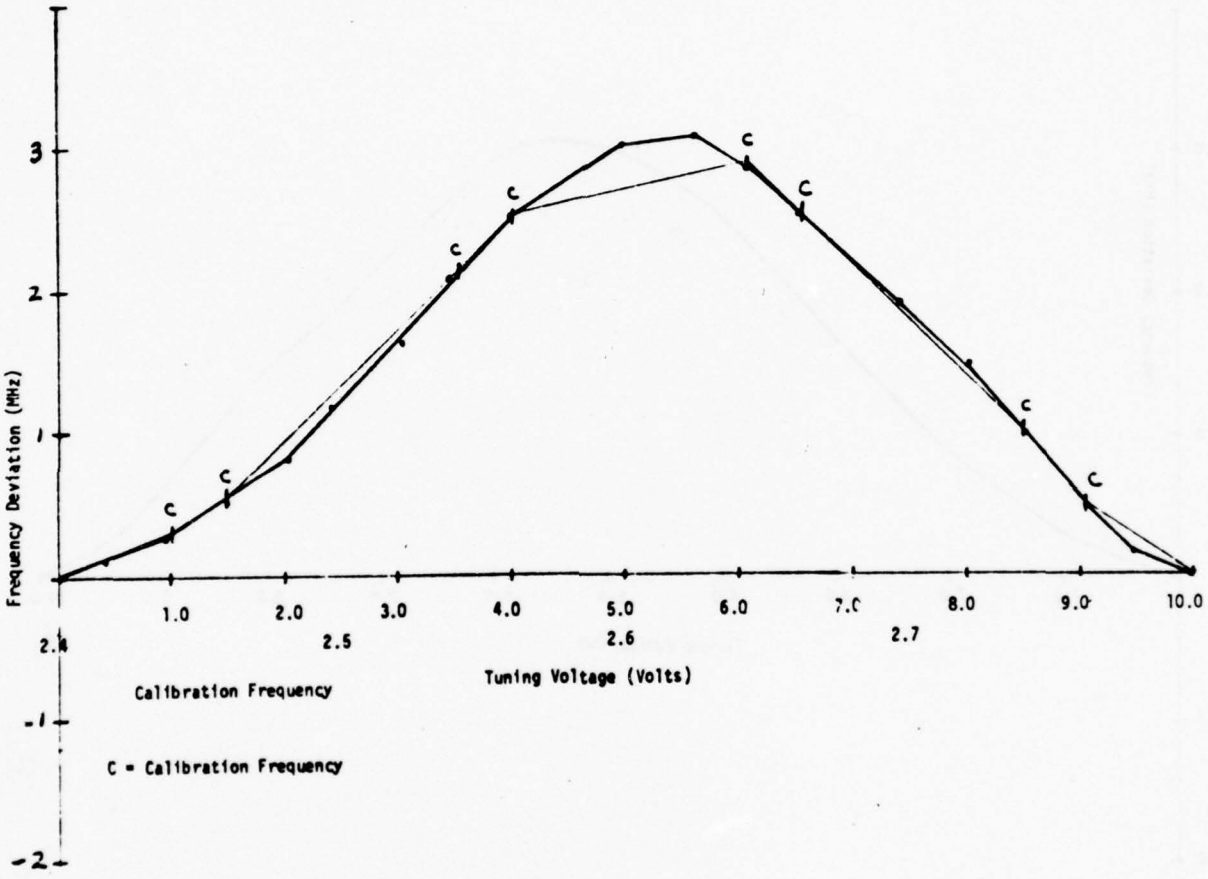


Figure 3-22. Calibration Curve

The oscillator temperature performance is illustrated by Figure 3-23. Again it is seen that the calibration is required to provide the desired frequency accuracy.

The tuning speed of the YIG Oscillator is presented in Figure 3-24. This figure is a series of photographs showing the oscillator response for full band steps. Curves A and B are steps from 2.8 GHz to 2.4 GHz. Curve B is an expanded version of A around zero time. Curves C and D illustrate steps from 2.4 to 2.8 GHz. Curve C is an expanded version of D around zero time. Curve E is the response for a 100 MHz step.

3.5 AUTO-FREQUENCY CONTROL LOOP

The function of the Auto Frequency Control Loop is to lock the voltage tuned oscillator exactly 60 MHz above the local oscillator frequency. This oscillator is tuned in conjunction with the LO and is used to provide the RF signal for the RF calibrator.

The control loop is a frequency locked loop. Figure 3-25 is a block diagram of this circuit.

Due to phase tracking errors as a function of frequency it is important that the calibration signal be present at the frequency of the incoming signal. Figure 3-26 is a plot of differential phase shift vs IF frequency. It illustrates the change in absolute phase shift vs IF frequency.

The Varactor Tuned Oscillator (VTO) used as the RF source for the RF calibrator is an Avantek-VTO 8240. This oscillator was used because of its small size and weight, low power drain and fast tuning speed. The oscillator requires linearization to track the YTO local oscillator to within ± 10 MHz with a 60 MHz offset. Linearity data is given in Figure 3-27. This indicates a worse case error of approximately 6 MHz. In addition a temperature drift error occurs. This is presented in Figure 3-28. To reduce drift with temperature the linearizer was compensated and an oven is installed that becomes activated below approximately 25^{o}C. The total drift between the environmental effects and tuning linearity result in worse case frequency errors of 12 MHz. This is the number which the loop must reduce to, ideally 0.

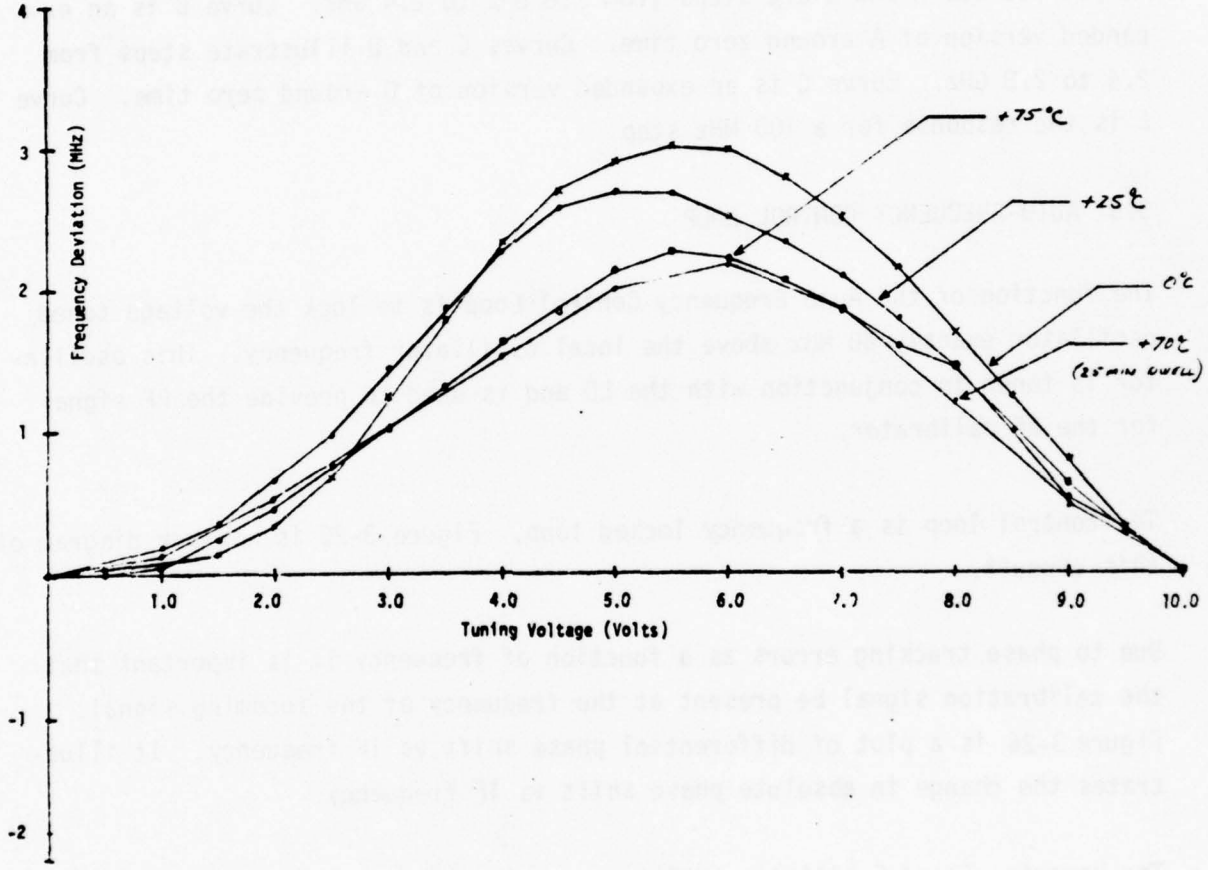
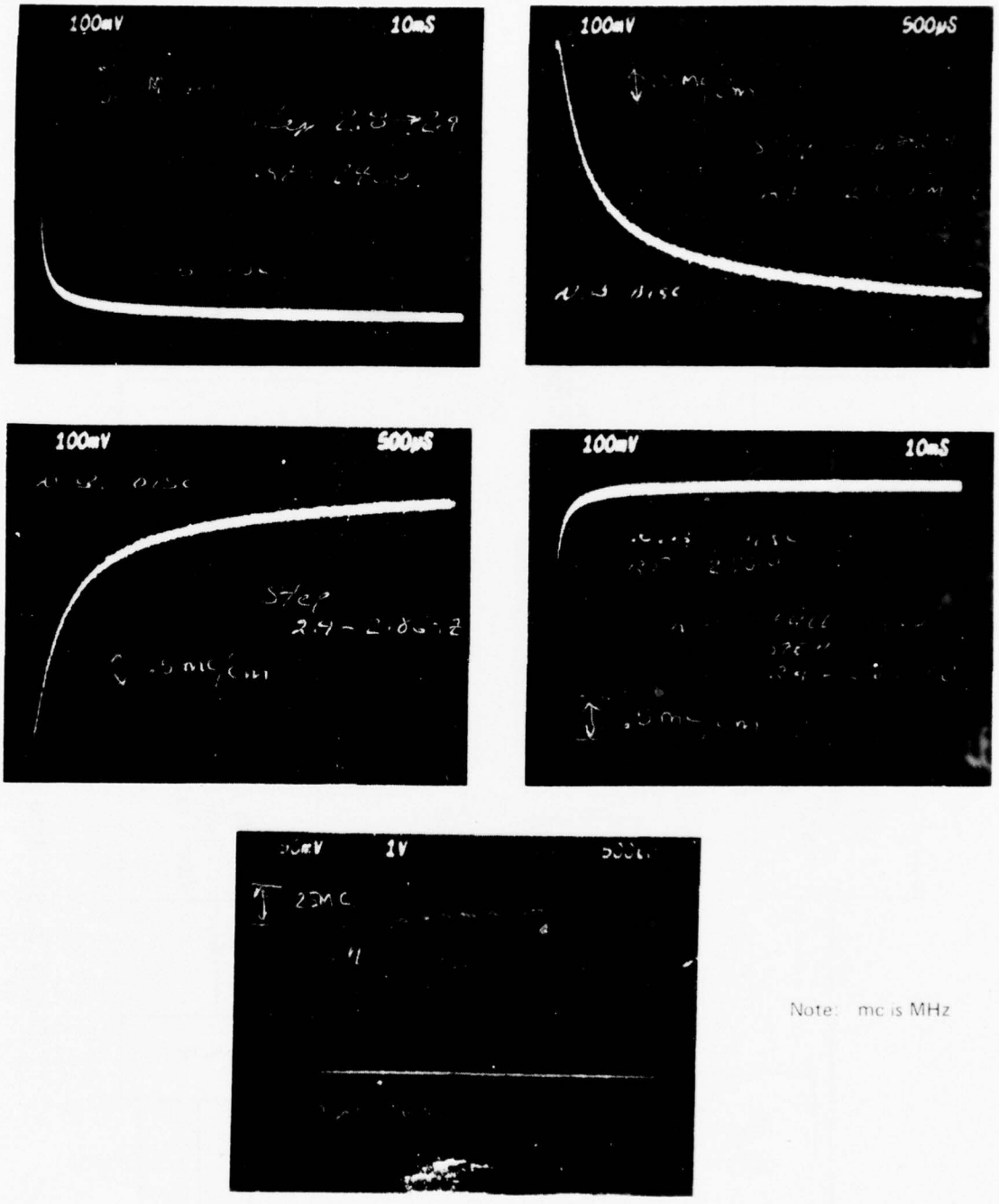


Figure 3-23. Local Oscillator Linearity vs Temperature



Note: mc is MHz

Figure 3-24. Local Oscillator Tuning Speed vs Input Voltage Step Size

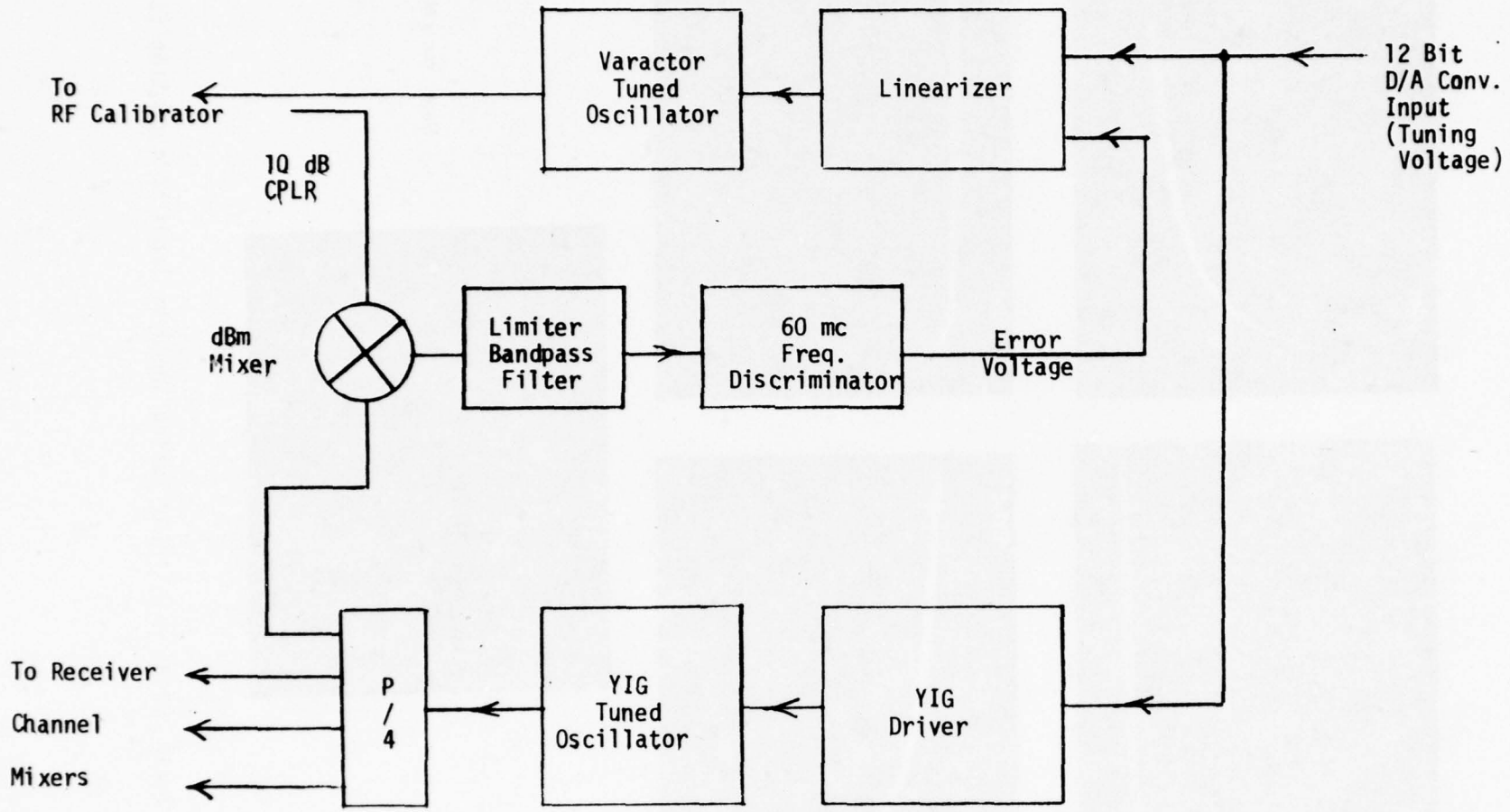


Figure 3-25. Auto Frequency Control Loop

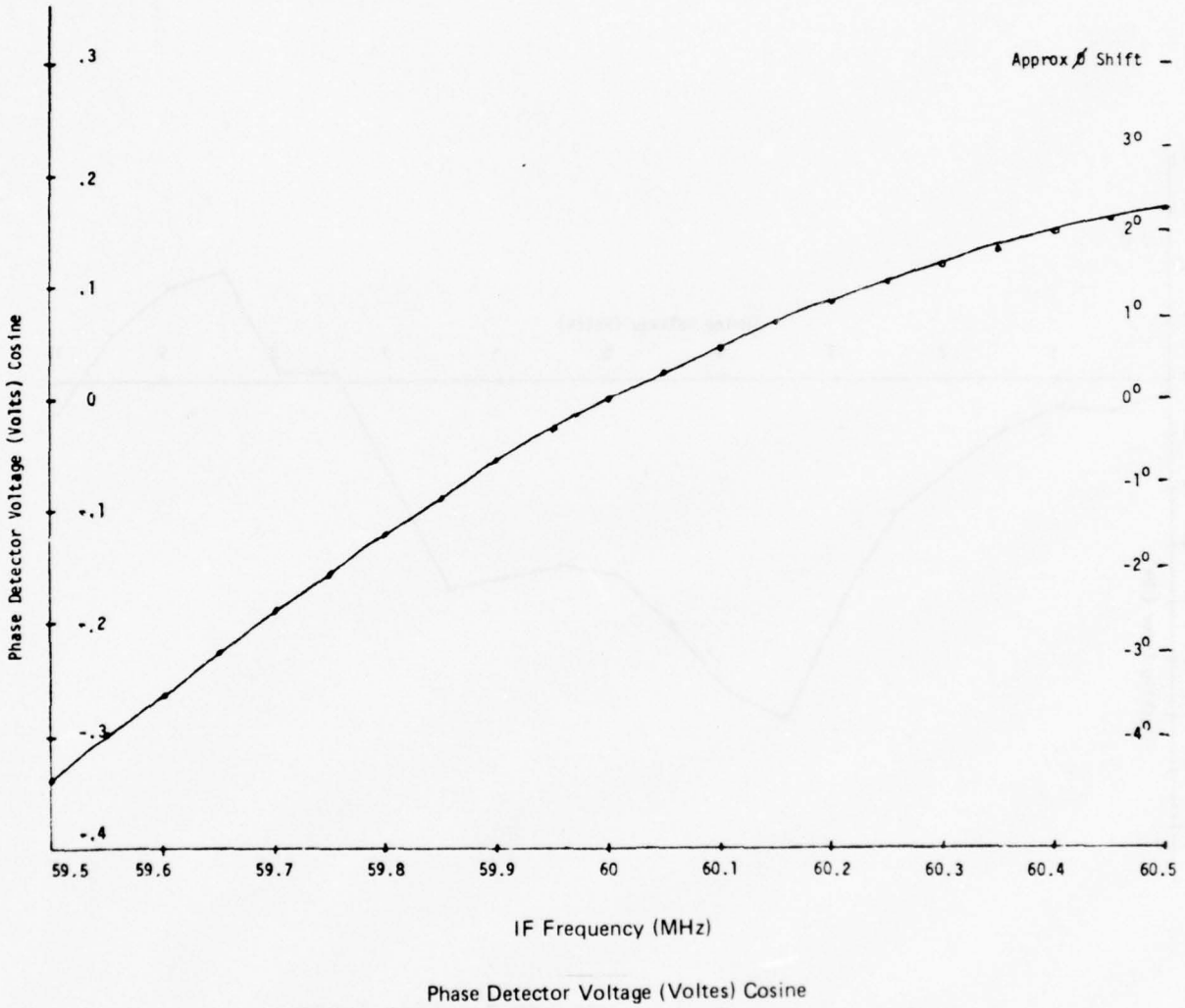


Figure 3-26. Phase Shift vs IF Frequency

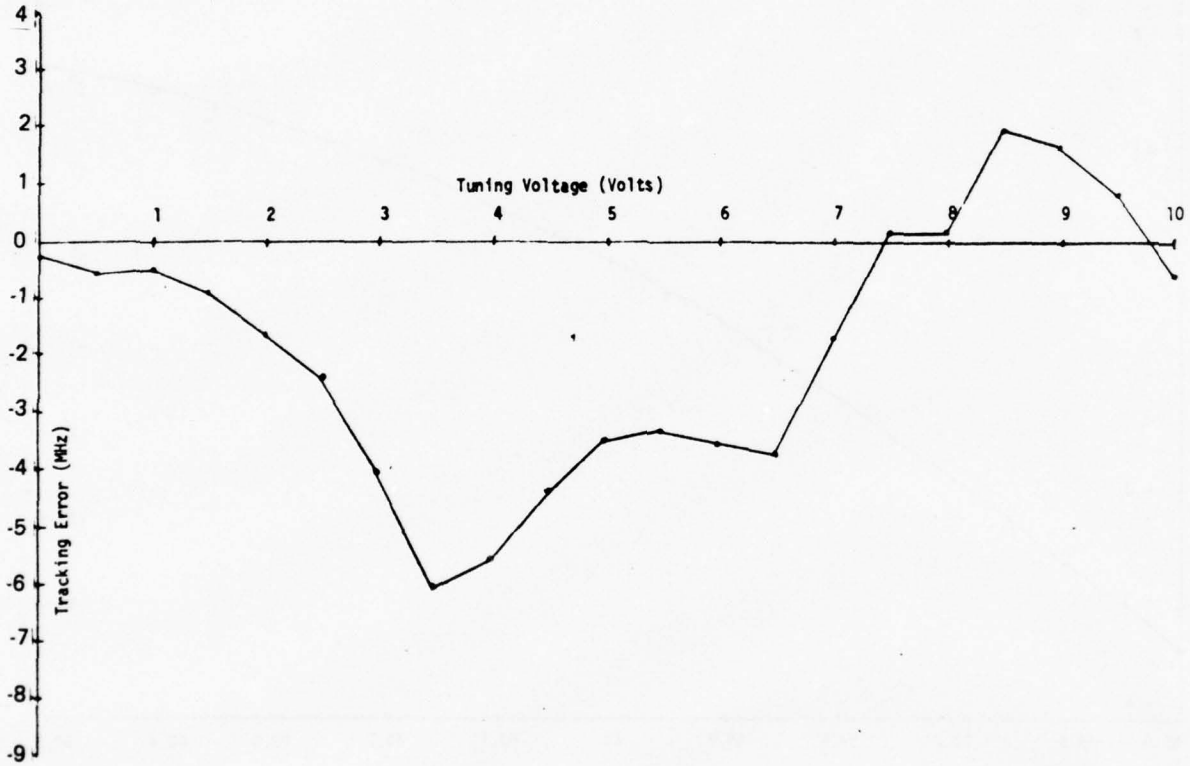


Figure 3-27. Typical VTO/YTO Tracking Error

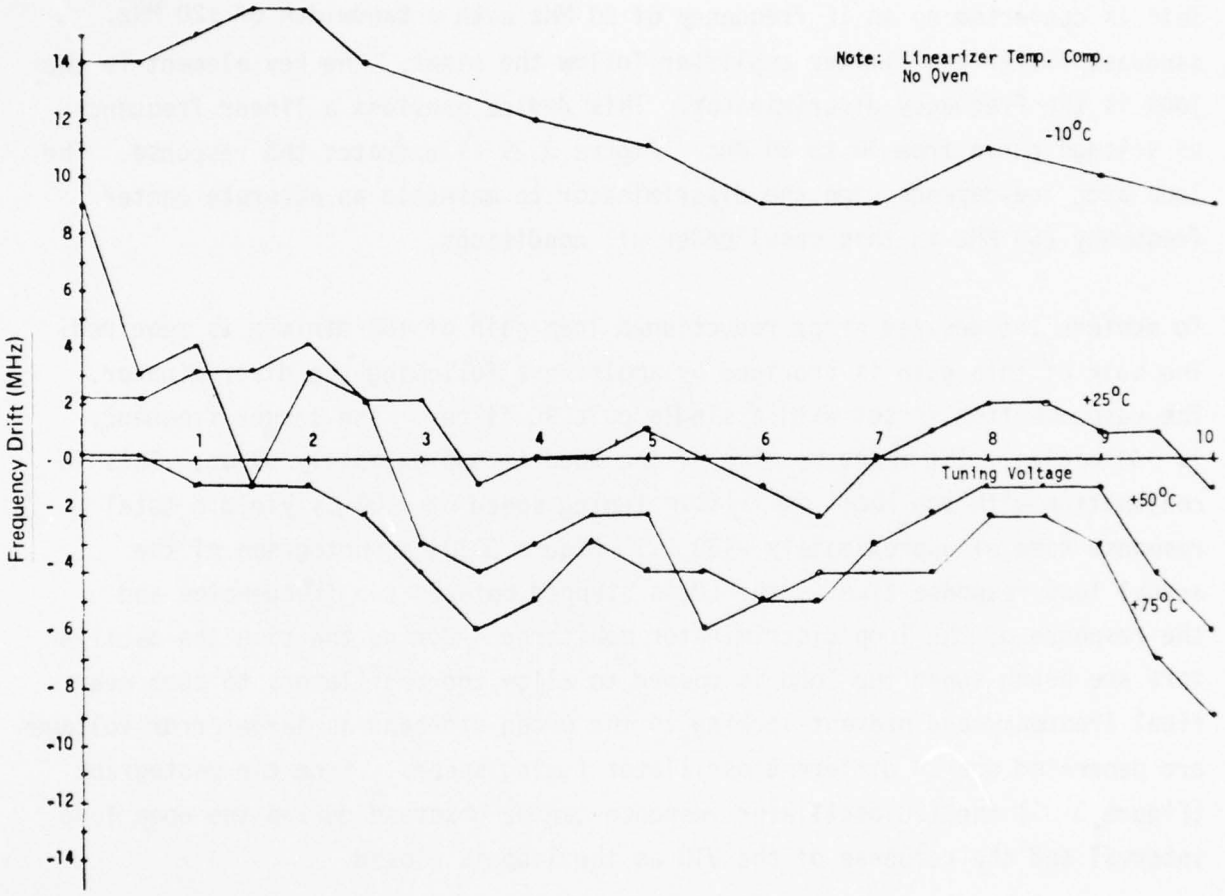


Figure 3-28. Varactor Tuned Oscillator and Linearizer Tuning Linearity Temperature Drift

The frequency locked loop was designed to reduce the oscillator tracking error to $\leq \pm$ 0.1 MHz over the frequency range and all environmental conditions.

The loop is implemented as illustrated in Figure 3-25. The output from the local oscillator is applied to the mixer in conjunction with the RF source. This is converted to an IF frequency of 60 MHz with a bandwidth of ±20 MHz. A bandpass filter and limiter amplifier follow the mixer. The key element in the loop is the frequency discriminator. This device provides a linear frequency vs voltage curve from 40 to 80 MHz. Figure 3-29 illustrates the response. The loop accuracy depends upon the discriminator to maintain an accurate center frequency (60 MHz in this case) under all conditions.

To achieve the desired error reduction, a loop gain of 150 minimum is required. The bulk of this gain is provided by amplifiers following the discriminator. The response time is set with a single pole RC filter. The corner frequency is .31 cycles. The response time of the loop is approximately 30 μs. This in conjunction with the local oscillator tuning speed of <100 μs yield a total response time of approximately ~130 μs. Figure 3-30, a photograph of the actual loop response time as the LO is stepped between two frequencies and the response of the loop discriminator monitored. During the time the oscillators are being tuned the loop is opened to allow the oscillators to tune near final frequency and prevent locking to the wrong sideband as large error voltages are generated due to different oscillator tuning speeds. From the photograph (Figure 3-30) the YIG oscillator response can be observed during the open loop interval and the response of the VTO as the loop is closed.

Figure 3-31 illustrates errors in the frequency locked loop for frequency differences in the YIG local oscillator and VTO over and beyond the normal error correction range at four discrete LO frequencies.

Figure 3-32 provides performance data on the breadboard receiver frequency locked loop as a function of tuning voltage and temperature. Discriminator offset errors as a function of temperature are evident. No offset compensation was included in the breadboard circuit. Inclusion of this temperature compensation should significantly reduce this error. Ignoring the offset error the loop error is within ±70 kHz. Alternately software can be used to correct offset errors using the narrowband frequency discriminator and adding or subtracting a correction factor.

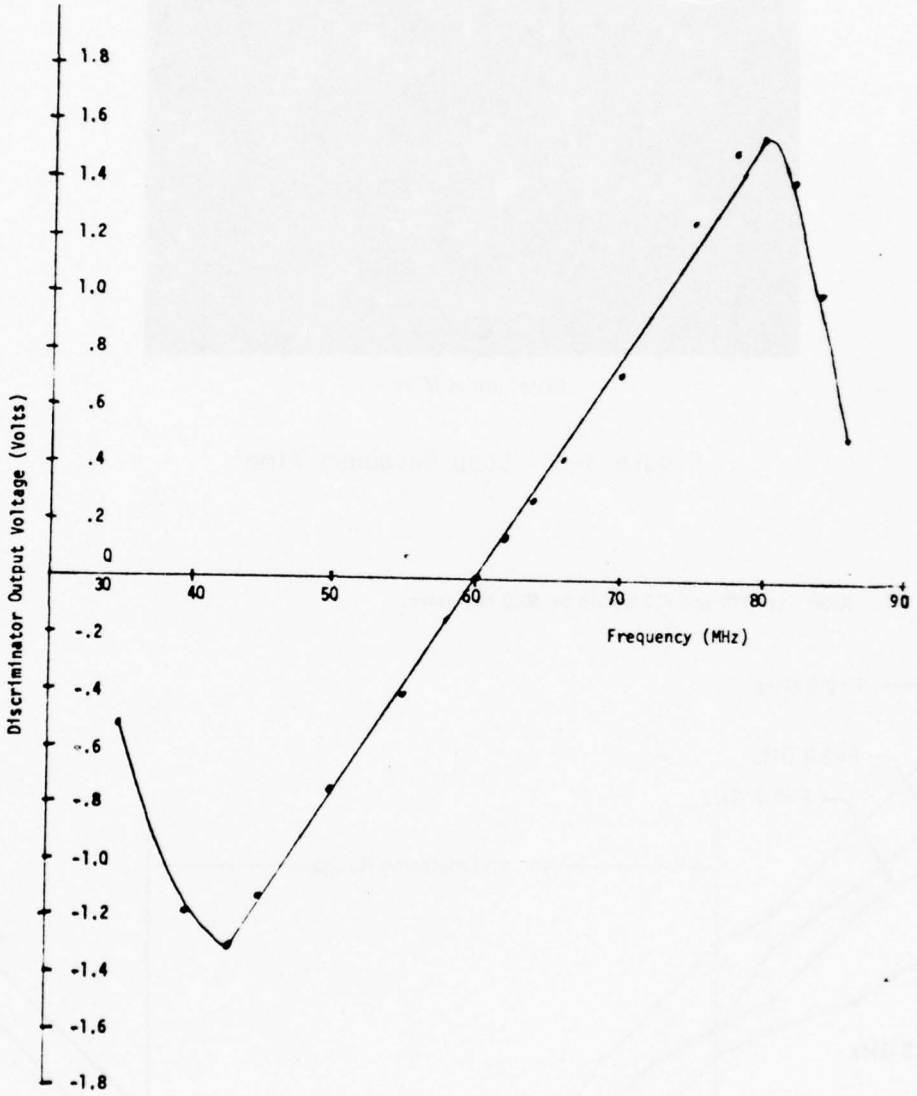
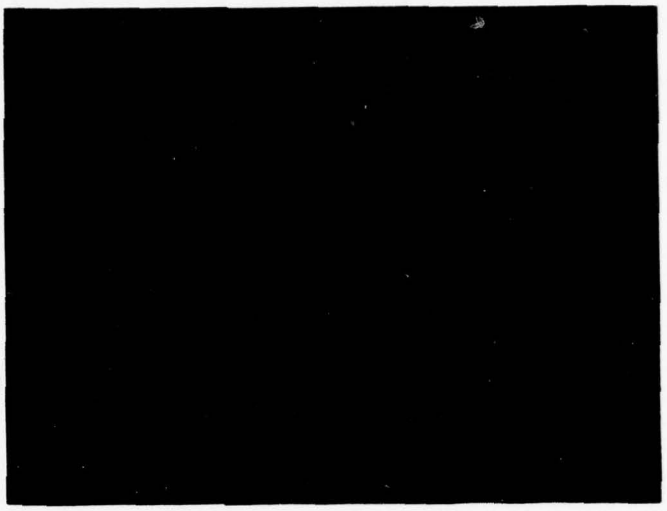


Figure 3-29. Loop Discriminator



Note: mc is MHz

Figure 3-30 Loop Response Time

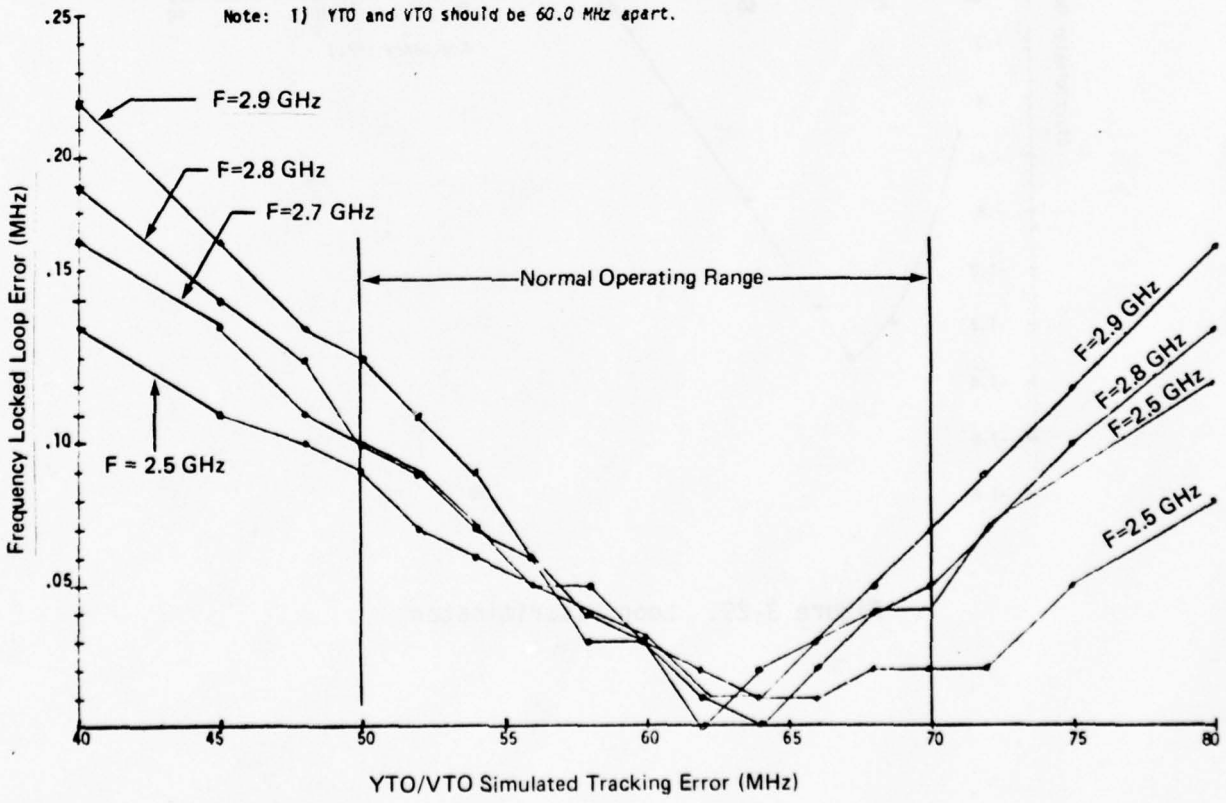


Figure 3-31. Frequency Locked Loop Error vs Simulated YTO and VTO Tracking Error at 4 YTO Frequencies

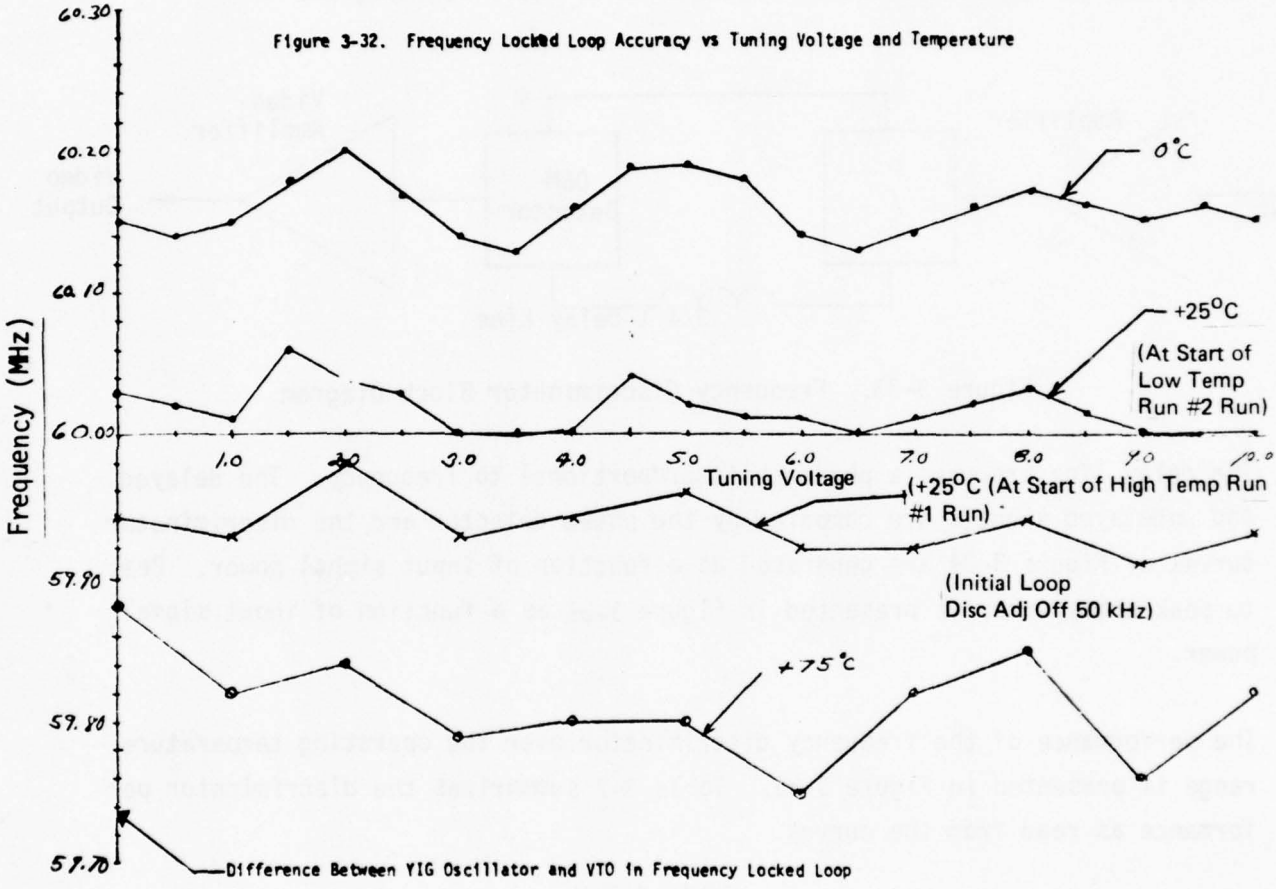


Figure 3-32. Frequency Locked Loop Accuracy vs Tuning Voltage and Temperature

3.6 FREQUENCY DISCRIMINATOR/QUALIFICATION

The frequency discriminator generates an analog voltage proportional to the input IF frequency. The input to the discriminator is tapped off one limiter channel. The discriminator design is based on the use of a 3/4 wavelength delay line and phase detector. Figure 3-33 is the block diagram.

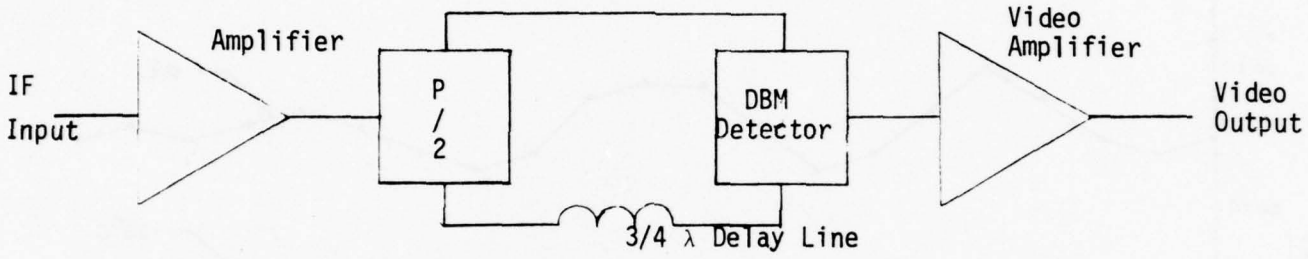


Figure 3-33. Frequency Discriminator Block Diagram

The delay line produces a phase shift proportional to frequency. The delayed and undelayed signals are compared by the phase detector and the discriminator curves of Figure 3-34 are generated as a function of input signal power. Peak to peak noise error is presented in Figure 3-35 as a function of input signal power.

The performance of the frequency discriminator over the operating temperature range is presented in Figure 3-36. Table 3-7 summarizes the discriminator performance as read from the curves.

Table 3-7
DISCRIMINATOR PERFORMANCE

Disciminator Scale Factor	200 mV/MHz
Discriminator Linearity	±0.1 MHz over 1 dB BW and S/N 20 dB
Temperature Error	±0.1 MHz from -10°C to +75°C.

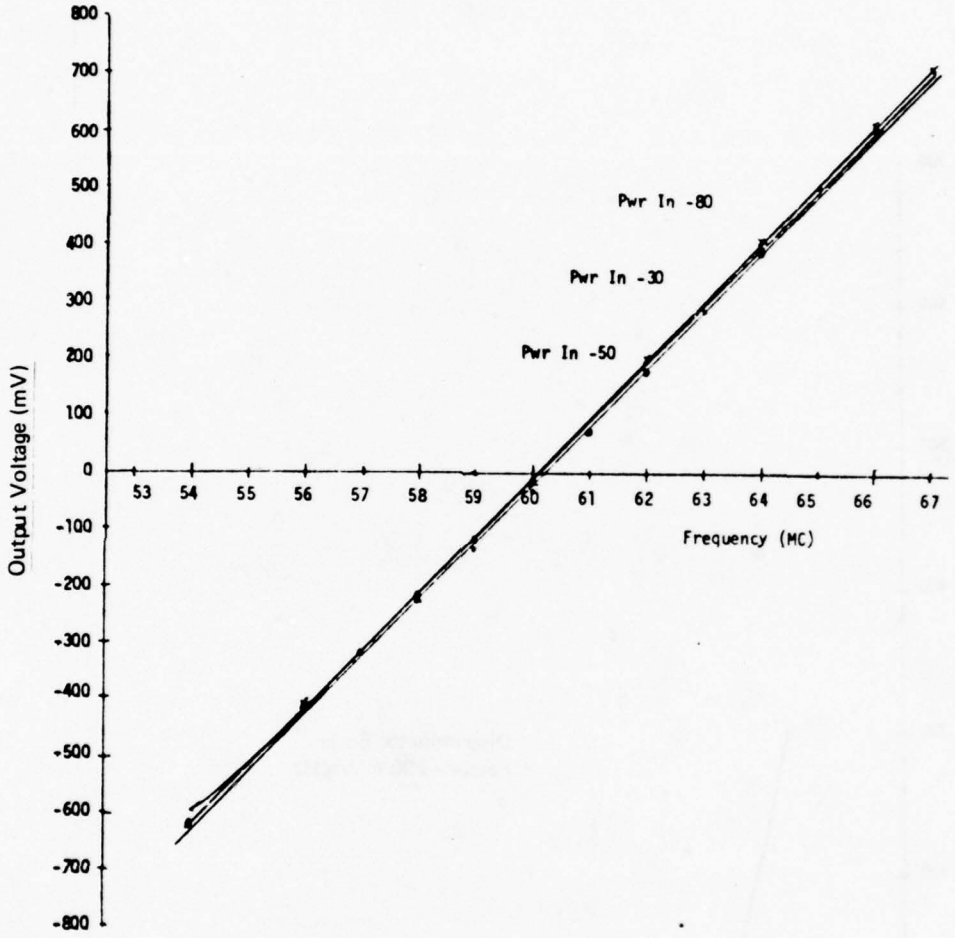


Figure 3-34. Freq. Disc. vs Dynamic Range

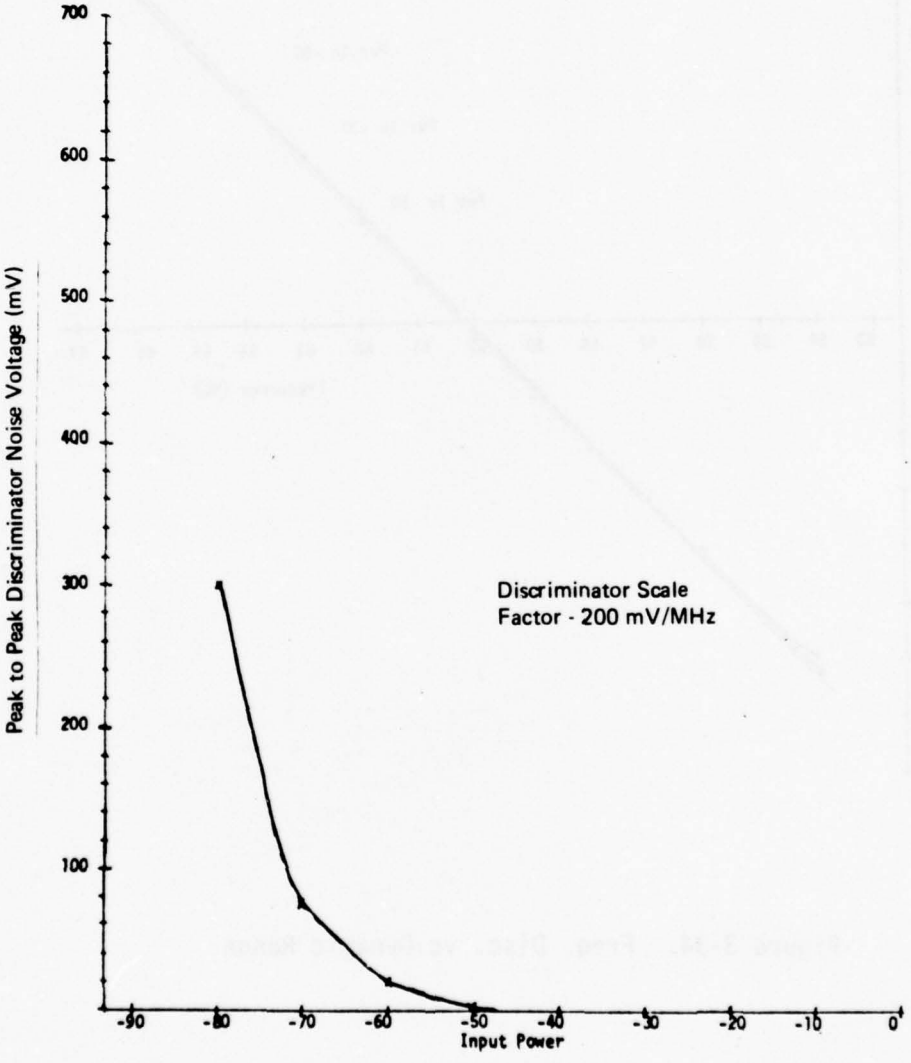


Figure 3-35. Frequency Discriminator Peak to Peak Noise vs Input Signal Power

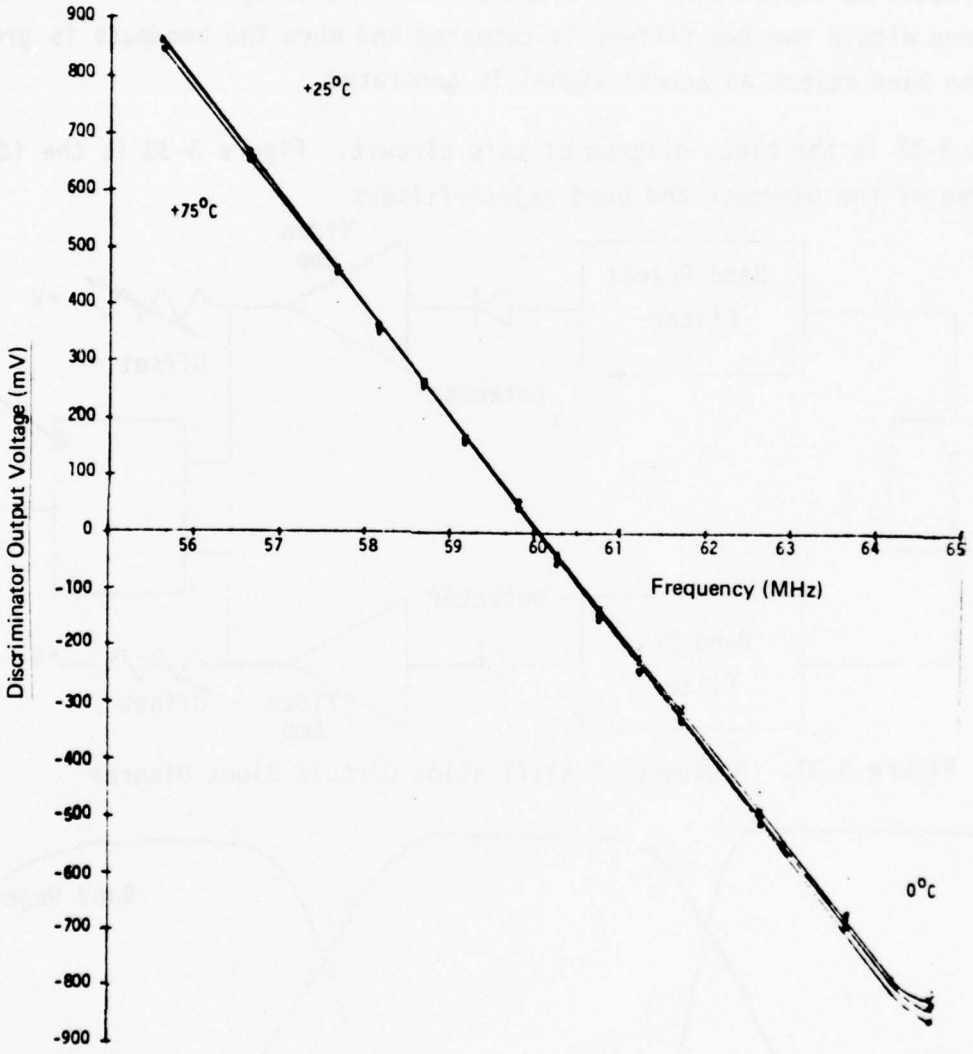


Figure 3-36. Frequency Discriminator vs Temperature

3.6.1 Frequency Qualification

The frequency qualification circuits are used to reject spurious signals caused by frequency discriminator ambiguity and fast rise time signals close to the IF passband producing transient response in the narrowband IF filters.

This circuit is implemented with a bandpass and band reject filter. The energy contained within the two filters is compared and when the bandpass is greater than the band reject an accept signal is generated.

Figure 3-37 is the block diagram of this circuit. Figure 3-38 is the ideal response of the bandpass and band reject filters.

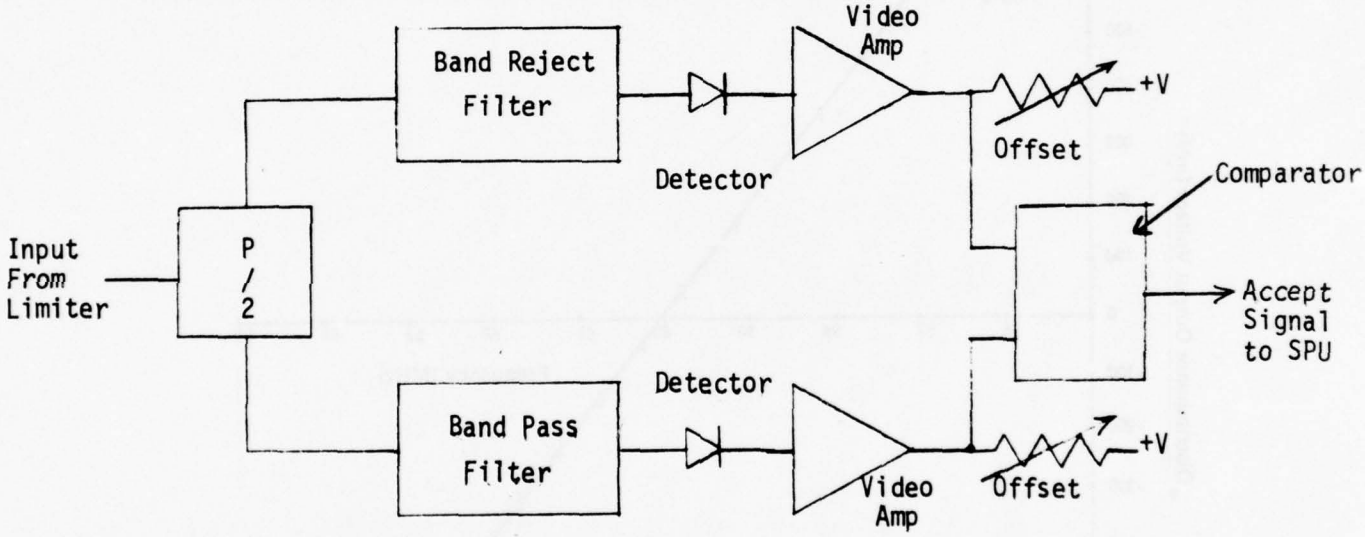


Figure 3-37. Frequency Qualification Circuit Block Diagram

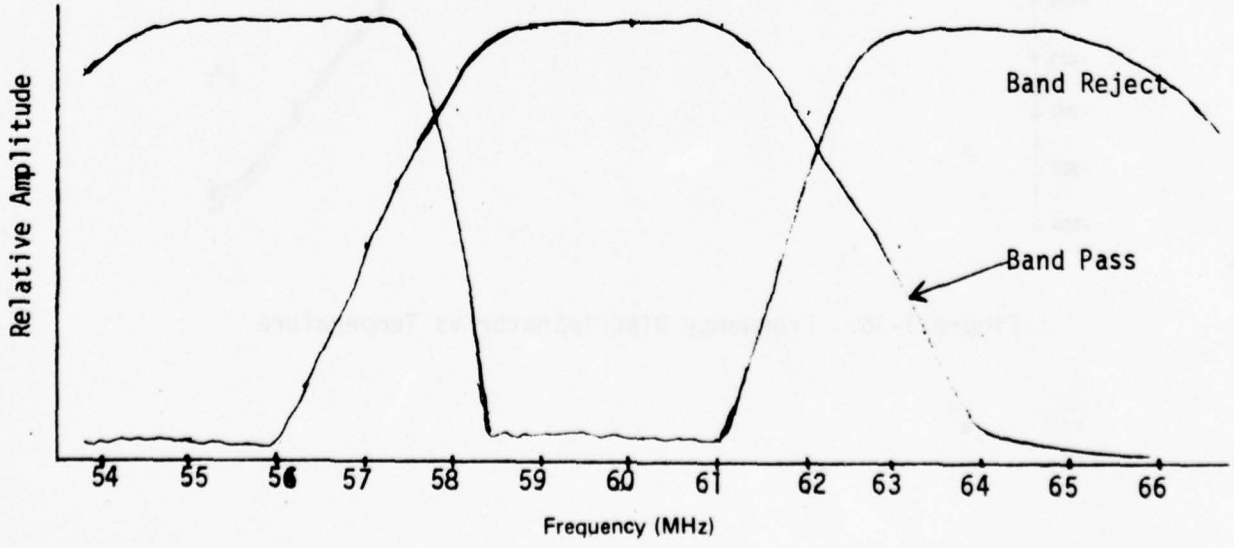


Figure 3-38. Bandpass and Band Reject Filter Response

The fall off of the band reject is caused by the preceding IF filter. Measured response of the filters is presented in Figure 3-39.

Performance of the qualification circuit is presented in Table 3-8.

Table 3-8
QUALIFICATION PERFORMANCE

Input Power	f_{LL} Out	f_{LH} In	f_{HL} In	f_{HH} Out	Effective Bandwidth MHz
-30	2497.3	2497.5	2502.2	2502.9	4.7
-50	2497.3	2497.5	2502.1	2502.4	4.6
-70	2497.3	2497.6	2502.1	2502.3	4.5
-75	2497.3	2497.6	2502.0	2502.3	4.4
-80	2497.2	2497.8	2501.9	2502.4	4.1

As seen from the data there exists a small indecision range in the Qualification circuit where it is possible to accept a signal or reject it. All signals with $\pm$ 2 MHz of center are processed and all signals outside $\pm$ 3 MHz are rejected. One effect of the Qual. is the apparent use of an infinite rejection IF filter as signals greater than $\pm$ 3 MHz of center frequency are not processed.

3.7 CONTROL LOGIC ASSEMBLY

This assembly provides the interface between the SPU and receiver, the D/A converter circuits for control of the Local Oscillator and RF attenuator, and the switch drivers providing current to the RF and IF switching networks.

Tables 3-9 and 3-10 provide performance data on the 12 bit D/A and 8 bit D/A converters.

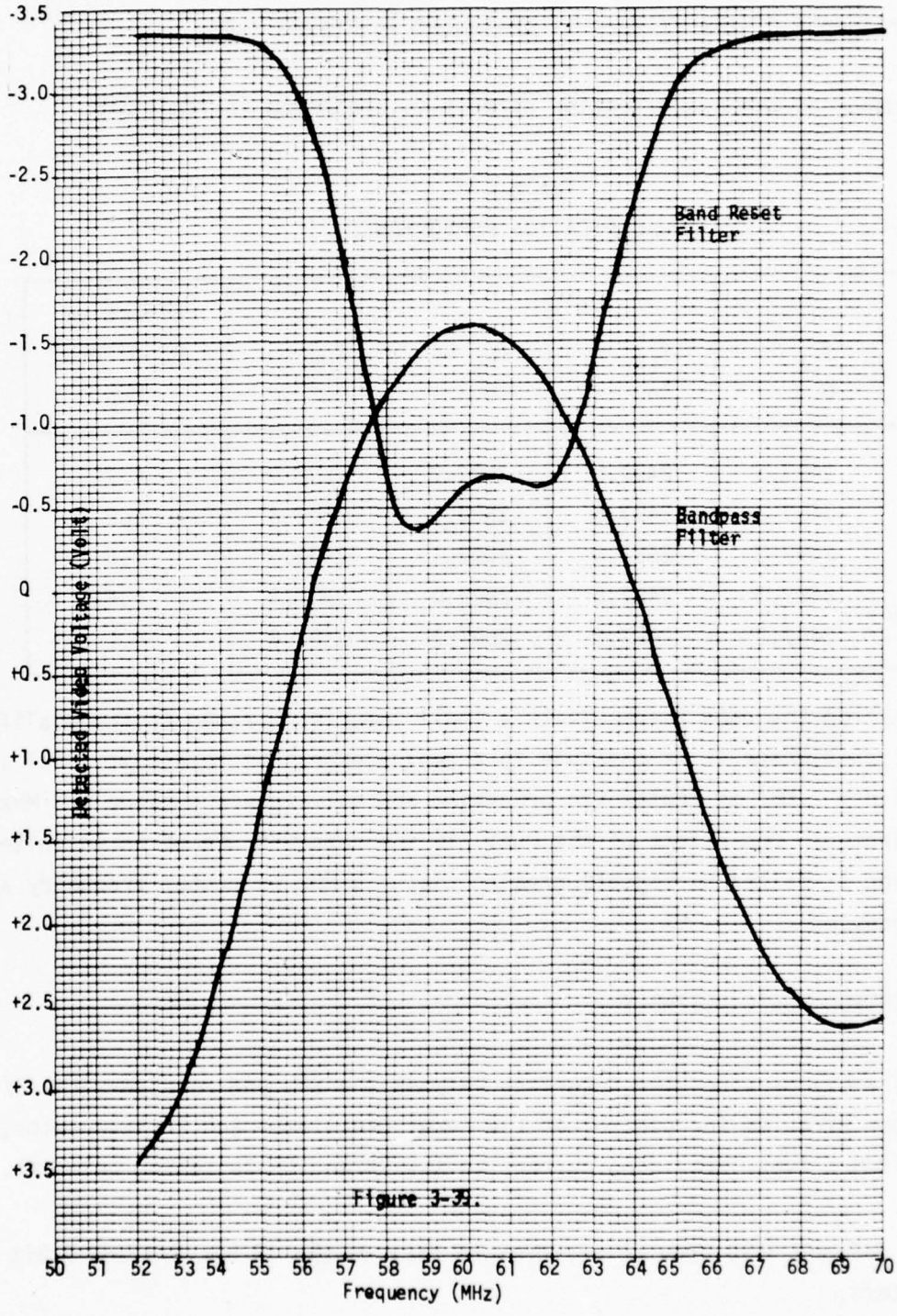


Figure 3-39. Measured Response of FIlters

Table 3-9

12 BIT D/A CONVERTER PERFORMANCE

	Output Voltage vs Temperature		
Bit Weight	+25°C	+70°C	0°C
MSB	5.118	5.119	5.119
	2.558	2.559	2.559
	1.2796	1.2803	1.2797
	0.6398	0.6405	0.6396
	0.3197	0.3204	0.3195
	0.1599	0.1606	0.1596
	0.0800	0.0807	0.0796
	0.0400	0.0407	0.0397
	0.0199	0.0206	0.0195
	0.0100	0.0107	0.0096
	0.0050	0.0057	0.0047
LSB	0.0025	0.0032	0.0022
Offset	0.0000	+0.0008	-0.0003

Table 3-10

8 BIT D/A CONVERTER (TESTED AS 10 BITS) VS TEMPERATURE

	Output Voltage vs Temperature		
Bit Weight	+25°C	+85°C	-10°C
MSB	5.124	5.123	5.125
	2.566	2.566	2.567
	1.287	1.287	1.288
	0.6462	0.6464	0.6463
	0.3242	0.3243	0.3242
	0.1635	0.1636	0.1636
	0.0852	0.0856	0.0851
	0.0451	0.0455	0.0449
	0.0251	0.0256	0.0249
LSB	0.0148	0.0152	0.0146
Offset	+0.004	+0.005	+0.004

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Appendix B

SCHANS PULSE CONVERSION UNIT (PCU)
FINAL REPORT

Prepared by

Richard E. Dreska

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LIST OF TABLES

1.0 PULSE CONVERSION UNIT CHARACTERISTICS

1.1 FUNCTION OF PULSE CONVERSION UNIT

The function of the Pulse Conversion Unit (PCU) is to digitize the video pulse outputs of the Interferometric Landmark Tracker (ILT) Receiver and output this digital data to the Signal Processing Unit (SPU). The PCU also receives mode control and receiver tuning words from the SPU to control the mode of operation of its self and the receiver, and to tune the receiver to the proper frequency.

1.2 INPUTS AND OUTPUTS OF THE PCU

The inputs to the PCU from the receiver are one log video signal (LV), one fine frequency (FRF), one accept pulse (QUAL), and four phase signals (sinA, CosA, SinB, CosB). Signal processing starts upon the receipt of a LV pulse that has sufficient amplitude to exceed the minimum threshold level. When the LV signal has settle to its final level a hold gate and qual strobe are generated. The hold gate causes sample and hold circuits connected to the LV, FRF and phase inputs to hold the value of those input signals at that instant of time. The qual strobe interrogates the qual signal to determine if the input should be accepted or rejected. The held values are serially multiplexed to an eight bit A/D converter who's output is held in a digital register until all the parameters are converted. The Time of Arrival (TOA) of the input RF pulse is also stored in these registers. The TOA is determined by an Adaptive Threshold Detector (ATD) which indicates when the log video is at its minus six dB point on the rise time. At this point, the count of a 32 bit 60 MHz counter is strobed into the storage register to indicate TOA for that particular pulse.

When all of this data is in the storage register it is transferred to the SPU via a 16 bit data ready, data acknowledge parallel interface.

The PCU also receives inputs from the SPU which is a 16 bit data ready, data acknowledge interface. This interface transfers the mode of operation that the PCU and receiver should be operating in and the tuning word that tunes the receiver to the correct frequency for processing landmarks.

1.3 MODES OF OPERATION

The PCU operates in four different modes which are Normal, RF Frequency Calibration, IF Calibration and Standby. The SPU commands both the PCU and receiver to operate in a particular mode by issuing a specific mode control word or descrete signal. The mode control word format is shown in Table 2.5.

1.3.1 Normal Mode

In the normal mode the PCU receives pulse data that represents amplitude,

fine frequency and phase from the receiver. It digitizes these terms and holds them along with the TOA in storage registers. It then commands the receiver to go into a calibration mode where signals of equal phase shift and of the same power level of the pulsed input are injected into the receiver. After 11 us the phase inputs are held and digitized. This phase information is also put into storage registers. The SPU is then given a data ready and the data stored in the registers is transferred to the SPU. After all the data is transferred, the PCU is reset and can process another input.

1.3.2 RF Frequency Calibration Mode

In the RF Frequency Calibration Mode a signal with known frequency and known amplitude and with equal phase shift is injected into the input of the receiver channels. Eleven microseconds after the unit is commanded to go into RF Frequency Calibration Mode the PCU will hold the values of amplitude, fine frequency and phase and will digitize these terms. Also the TOA register will store the TOA at hold time. When all terms are in the storage registers the data will be transferred to the SPU via the data ready acknowledge 16 bit interface. After all data is transferred the PCU is reset, another 11 us time out is generated and the digitizing cycle starts all over again. The PCU will keep cycling in this mode until the SPU comm ads another mode of operation. This mode can be used for the following functions:

1. RF Frequency Calibration
2. RF Phase Calibration
3. Built In Test
4. Real Time Counter for SPU (using the TOA readings)

1.3.3 IF Phase Calibration Mode

In the IF Phase Calibration Mode inputs with known phase shifts of -45°, $+45^{\circ}$, $+135^{\circ}$ and $+225^{\circ}$ are applied to the IF channel inputs. The SPU commands the PCU and receiver to be in the IF Phase Calibration Mode and commands the receiver to apply specific test input. After waiting 11 us for switching and settling the PCU holds the values of amplitude, frequency and phase. It then digitizes the values of the SinA, CosA, SinB and CosB phase terms. After these terms are in the storage registers the data is transferred to the SPU via the 16 bit data ready/acknowledge interface. When the transfer is complete the PCU is reset, it will resample the inputs after an 11 us delay and digitize the phase terms again. The PCV will continue to cycle in this mode until commanded to enter a new mode.

1.3.4 Standby Mode

This mode is entered by the SPU sending a discrete signal to the power supply. The power supply will then turn off all the PCU power except for the voltages going to the TOA Counter/Buffer mib (A12A) and the Oscillator Assembly (A6). The voltages for the A12A and A6 assemblies are on separate mib layers in the backpanel and are supplied by the standby capability of the power supply.

This allows the TOA counter to run while the rest of the unit is off thus keeping an accurate real time measurement.

1.4 PCU PROCESS CYCLE TIMING

The time required to digitize the receiver inputs is dependent upon the mode of operation. For the three modes the time from the generation of hold gate to the time conversion complete is generated is:

Normal	33 us
RF Frequency Cal	26 us
IF Cal	26 us

A timing diagram for these modes is shown in Figures 1.1, 1.2 and 1.3.

1.5 CHANGING BITS IN MODE AND TUNING CONTROL WORDS

When the operation of the PCU requires that the Mode or Tuning Control Words be changed it is required that first just the Process Enable bit be turned off (Bit 15 = "0") and then wait until any pending data be transferred to the SPU.

The time to transfer pending data is the sum of the processing time of the PCU plus the I/O time of the SPU. The processing time of the PCU is mode dependent and is as follows for the three modes:

Normal	34 us for narrow pulse mode, 39 us for wide
RF Freq Cal	28 us
IF Cal	28 us

After this time any number of bits may be changed.

1.6 PCU PROCESSING ERRORS

Table 1.1 shows the errors at room temperature and over the 0¼C to 70¼C temperature range encountered for SCHANS for each of the function in the analog processing chain. For each of the terms processed a slightly different processing chain is encountered. Therefore the PCU processing errors are a function of the term being converted.

1.6.1 Amplitude

The amplitude term (Log Video) chain contain a Sample and Hold, Multiplexer, and A/D converter.

At $25^{o}C$

Error (max) = 5 + 8 = 13 mV

Error (RSS) = $(5)^2 + (8)^2$ = 9.4 mV

0 to 70^{o} C

Error (max) = 10+1.3 to .4 + 12 = 23.7 mV

Error (RSS) = $(10)^2+(1.3)^2+(0.4)^2+(12)^2$ = 15.7 mV

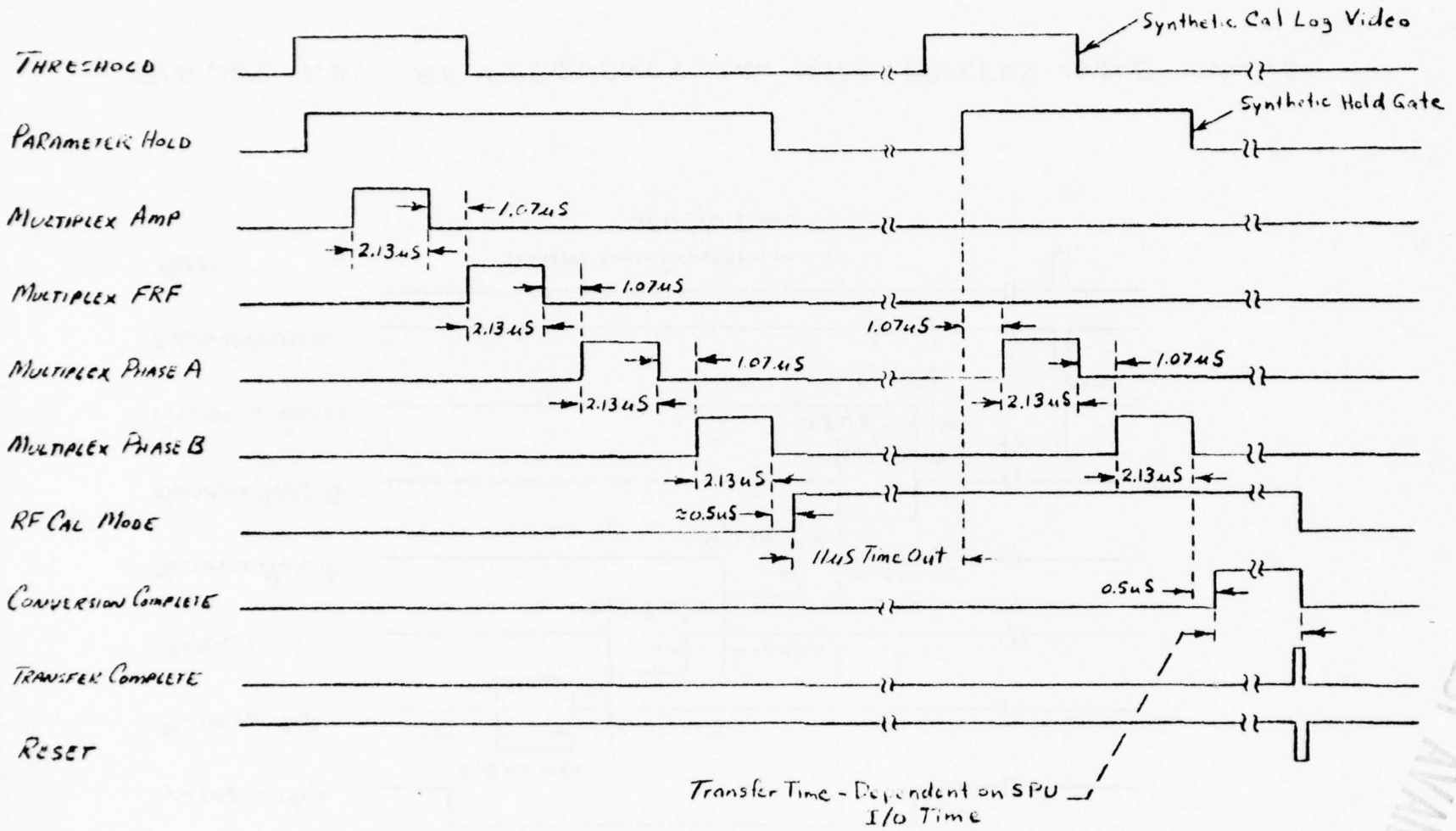


FIGURE 1.1 NORMAL MODE PROCESS CYCLE TIMING

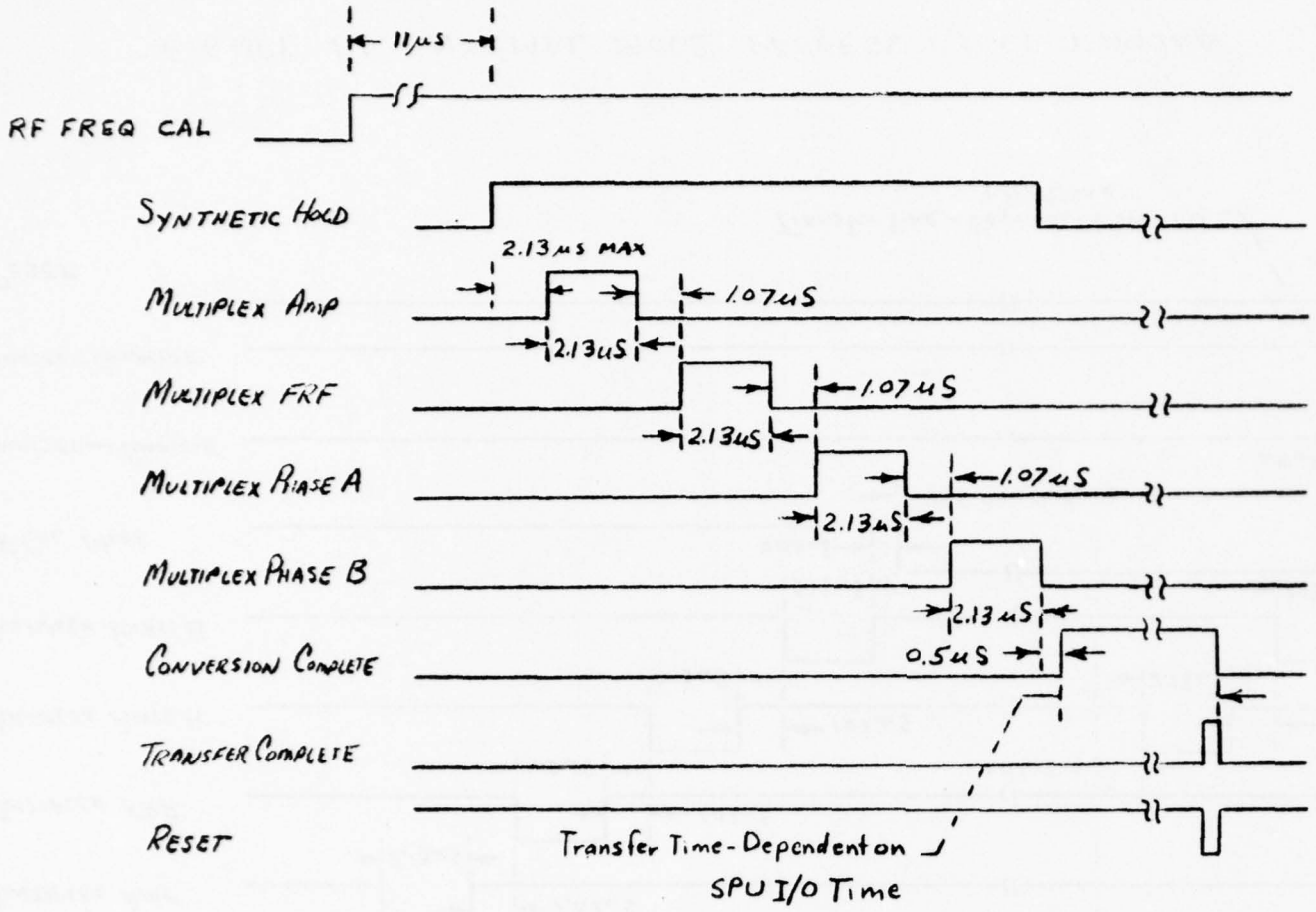


FIGURE 1.2 RF FREQUENCY CAL MODE PROCESS CYCLE TIMING

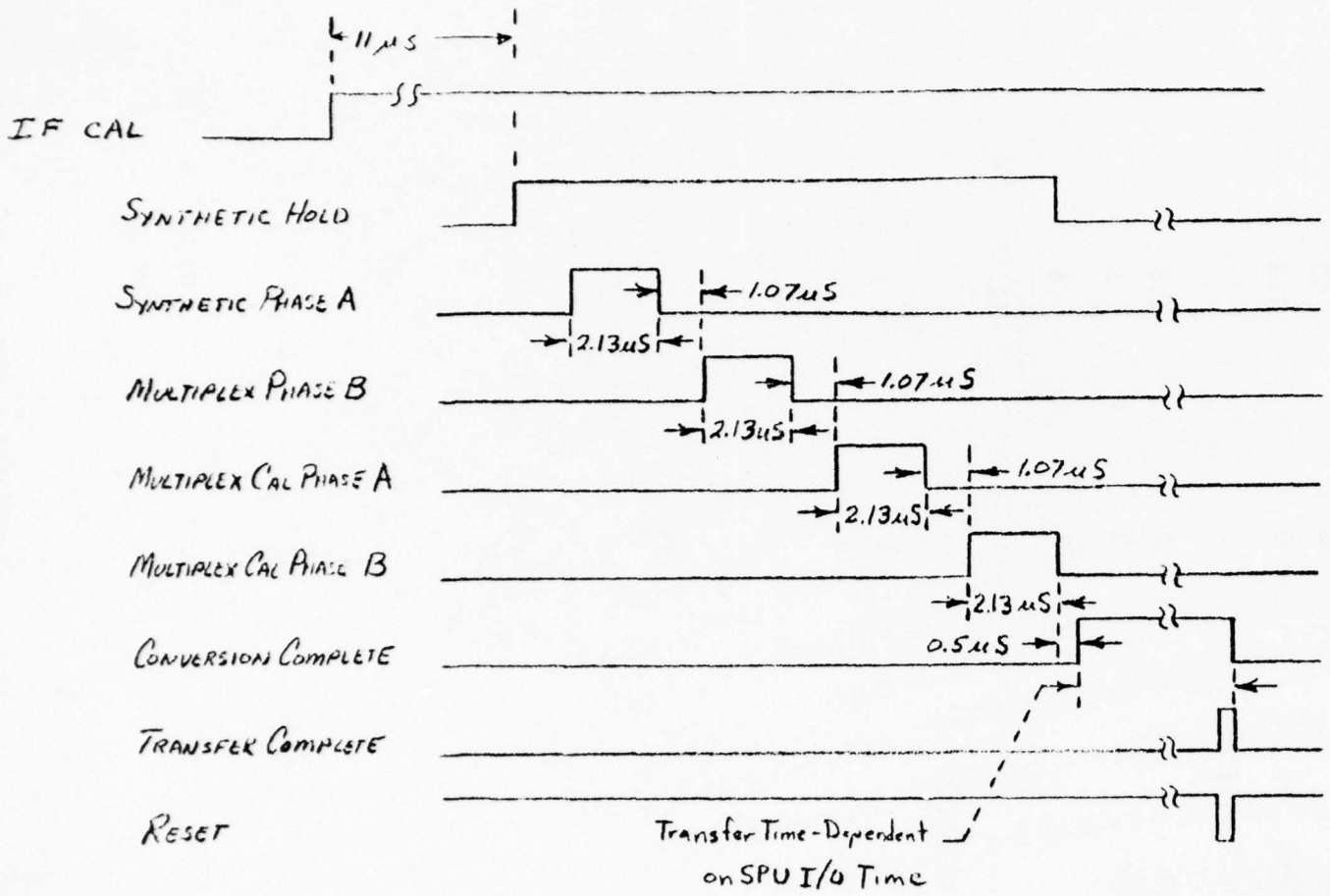


FIGURE 1.3 IF CAL MODE PROCESS CYCLE TIMING

Table 1.1. Errors of Each Function in The Analog Processing Chain

FUNCTION	Error In MV 25°C	0 to 70°C
Sample and Hold		
Gain	5	10
Offset	0	1.3
Absolute Value Amplifier		
Gain	1	1.5
Offset	0	1
Multiplexer	0	.4
A/D	8	12
Frequency Level Shift		
Gain	1	1.5
Offset	0	5

1.6.2 Phase

The phase terms (sine and cosine) have a Sample and Hold, Absolute Value Amplifier, Multiplexer and A/D converter in the processing chain.

At 25°C

Error (max) = $5 + 1 + 8 = 14$ mV
Error (RSS) = $(5)^2+(1)^2+(8)^2 = 9.5$ mV

0 to 70°C

Error (max) = $10 + 1.3 + 1.5 + 1 + .4 + 12 = 26.2$ mV
Error (RSS) = $(10)^2+(1.3)^2+(1.5)^2+(1)^2+(0.4)^2+(12)^2 = 15.8$ mV

1.6.3 Frequency

The frequency processing chain is the Sample and Hold, Level Shift, Multiplexer and A/D Converter.

At 25°C

Error (max) = $5 + 1 + 8 = 14$ mV
Error (RSS) = $(5)^2+(1)^2+(8)^2 = 9.5$ mV

0 to 70°C

Error (max) = $10 + 1.3 + 4 + 1.5 + 5 + 12 = 30.2$ mV
Error (RSS) = $(10)^2+(1.3)^2+(0.4)^2+(1.5)^2+(5)^2+(12)^2 = 16.5$ mV

1.7 PCU POWER SUPPLY REQUIREMENTS

The current required for each power supply voltage is given in Table 1.2 for each mib in the unit. Also the power dissipated for each mib is given in this table. Total power supply current and power dissipation for the PCU is also given in Table 1.2.

TABLE 1.2 PCU Current Requirements and Power Dissipation

Assembly	Function	Current Drain (mA)								Power (W)	
		+5V		-5V		+15V		-15V			
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
A10A	Phase Processing	35.1	59.8	21.0	42.0	68.0	117.0	33.8	49.8	1.81	3.01
A10B	A/D Converter	79.2	141.0	93.8	171.8	125.3	188.6	38.0	59.2	3.31	5.28
A11A	Sample and Hold	--	--	--	--	104.0	115.5	134.5	147.0	3.58	3.94
A11B	Amplitude Processing	122.1	202.2	24.9	43.4	84.1	101.9	100.6	108.8	3.51	4.39
A12A	TOA Counter/ Buffer	651.3	10066	--	--	--	--	--	--	3.26	5.33
A12B	Data Mux	599.8	993.0	--	--	--	--	--	--	3.00	4.97
A13	Mode and Tuning Control	179.1	298.2	--	--	--	--	--	--	.90	1.49
A14	Process Cycle Timing	229.4	420.9	--	--	--	--	--	--	1.15	2.11
A6 - Using Oscillator	Oscillator Assembly	66	109.6	--	--	30	60	--	--	.78	1.45
A6 - Using PLL	Oscillator Assembly	203.5	284.1	89	96	--	--	--	--	1.46	1.90
Total- Using Oscillator		1962	3290.7	139.7	257.2	411.4	583	306.9	364.8	21.3	31.97
Total - Using PLL		2099	3465.2	228.7	353.2	381.4	523	306.9	364.8	21.98	32.42
Standby Using Osc.		717.3	1175.6	--	--	30	60	--	--	4.04	6.78
Standby Using PLL		854.8	1350.1	89	96	--	--	--	--	4.72	7.23

2.0 PCU BLOCK DIAGRAM DESCRIPTION

The ILT Pulse Conversion Unit (PCU) shown in Figure 2.1 is basically a phase and TOA processor. Along with phase and TOA, this processor also digitizes amplitude and frequency. The circuitry is contained on eight 4 Pi mibs with ninety-eight pin connectors.

From a signal flow point of view, the first page A11 consists of the sample and hold mib and the amplitude processing mib. The A side of the A11 page is the sample and hold mib which contains five hybrid sample and hold circuits, four are used for the phase discriminator sine and cosine outputs of baselines A and B and one for the frequency discriminator output. The sample and hold mib also contains a level shifter for the fine RF input. This shifter transforms the ±1V fine RF input voltage range to a 0 to +2V voltage range. Thus making it compatible with the 0 to +2V input range of the A/D converter.

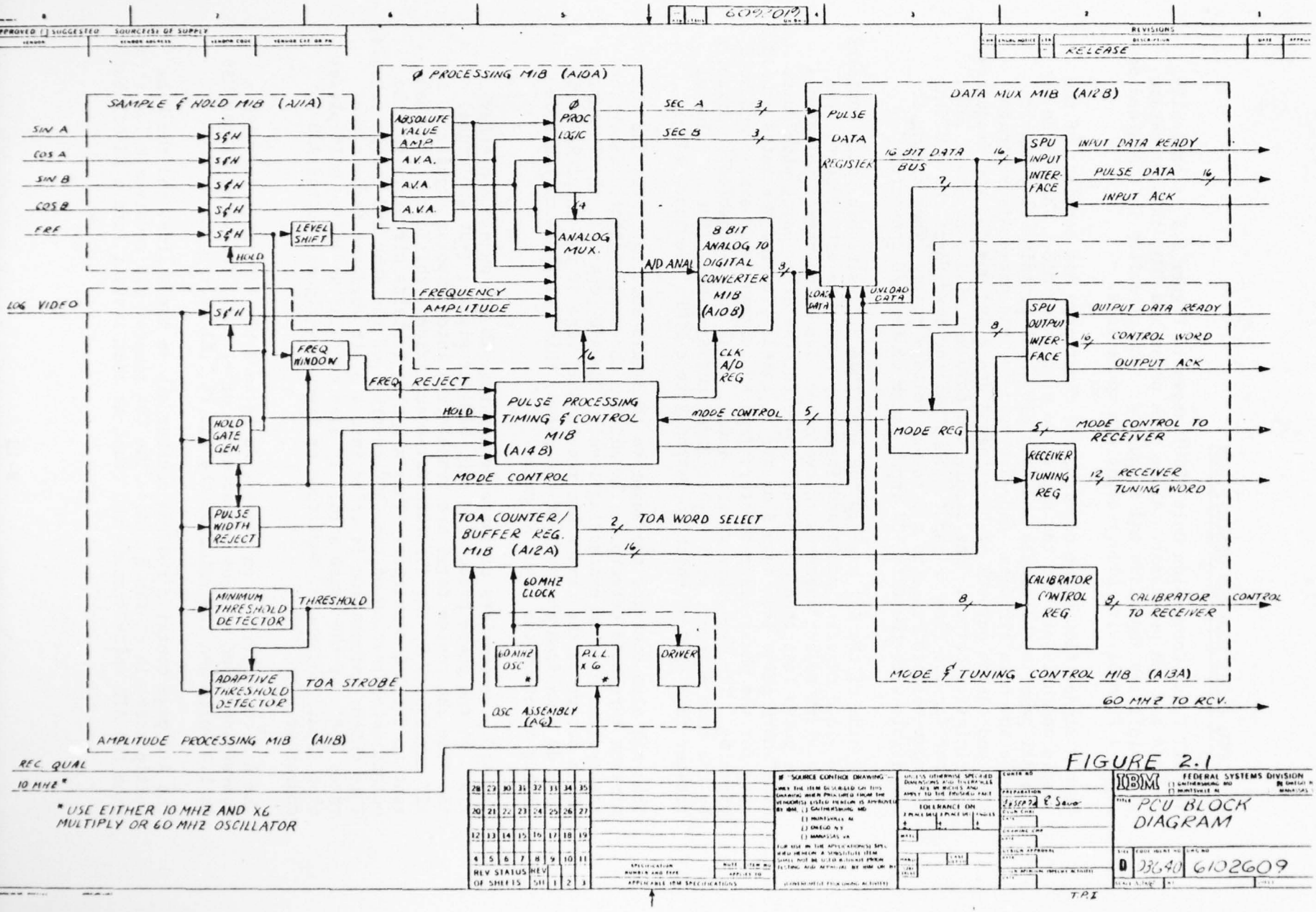
The B side of the A11 page is the amplitude procesing mib which contains pulse width reject circuit and frequency window reject circuit. The pulse width reject operates in two modes, one being narrow pulse mode where pulse less than 0.7 us are rejected, the other being wide pulse mode where pulse less than 5 us are rejected. It also generates a hold gate for the phase discriminator, fine RF and amplitude sample and hold circuits. The frequency reject window, which can be enabled or disabled by the mode control, will reject input pulses with a fine RF value of greater than ±200 mV which corresponds to a 1 MHz frequency range.

This mib also contains the adaptive threshold detector (ATD) and the minimum threshold detector. The minimum threshold detector determines the systems minimum processing level. The ATD generates the TOA strobe which occurs at the time where the leading edge of the input RF pulse is 6 dB down from the peak of the pulse, this being the most stable timing point on the input RF pulse.

The A10 page consists of phase processing mib and an A/D converter mib. On the phase processing mib, bipolar signals (±2V amplitude) of the sine and cosine terms are transformed into unipolar signals (0 to +2V amplitude) by the absolute value amplifiers; this output is then sent to the A/D converter. This mib also contains circuitry for the octant determination of the 360° coverage of the sine and cosine signals. This octant information is coded into a 3 bit word and becomes the three MSB's of the phase word. It also contains an analog multiplexer that inputs the phase, amplitude or frequency signals to the A/D converter.

The A/D converter mib on the B side is an 8-bit A/D converter with a conversion speed of 2 us and accuracy of ±1 LSB. The value of the MSB is 1.0 volts and the value of the LSB is 7.81 mV.

The A12 page contains the TOA counter mib on the A side, and the Data multiplexer mib on the B side. The TOA counter mib receives a TOA strobe from the ATD which strobes the count at that instant into a 32-bit buffer



* USE EITHER 10 MHz AND X6 MULTIPLY OR 60 MHz OSCILLATOR

FIGURE 2.1

PCU BLOCK DIAGRAM

IBM FEDERAL SYSTEMS DIVISION

SIZE D | FSCM NO 33640 | DWG NO 6102609

register. The clock for the counter is generated either by a 60 MHz temperature compensated crystal oscillator or from a phase locked loop, which has the capability of multiplying by six a signal from a 10 MHz atomic clock.

The data multiplexer mib receives the digital data from the A/D converter, the octant bits from the phase processing and the 32 TOA data bits, and formats it into seven, five or four 16-bit words depending upon the mode of operation (Table 2.1). The data formats are shown in Tables 2.2 through 2.4. This data is then sent to the SPU via a data ready/ acknowledge handshaking interface. The interface circuits are National DS7820/30 driver receiver combination.

The A13 page contains the mode and timing control mib and the RF control logic mib which is part of the receiver. The tuning and mode control bits to the PCU. The SPU output word format is shown in Tables 2.5 and 2.6. It also sends a calibrator control word to the receiver which in inversely proportional to the power of the input pulse.

The A14 page contains the process cycle timing circuitry on the B side mib and has a blank mib on the A side as a spare for future growth. The process cycle timing mib generates all the timing signals required to accomplish the analog multiplexing, A/D conversion and loading of the data registers on the data mux mib.

TABLE 2.1

PCU MODES OF OPERATION

MODE	DATA CONVERTED	
NORMAL	TOA	32 BITS
	AMPLITUDE	8
	FREQUENCY	8
	PHASE A	11
	PHASE B	11
	CAL PHASE A	11
	CAL PHASE B	11
RF FREQ CAL	TOA	32 BITS
	CAL AMPLITUDE	8
	CAL FREQUENCY	8
	CAL PHASE A	11
	CAL PHASE B	11
IF CAL	SIN ϕ A	8 BITS
	COS ϕ A	8
	SIN ϕ B	8
	COS ϕ B	8

Table 2.2

SCHANS Input Functions

Normal Mode

0 MSB	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15 LSB
5461 33.33	2730 66.67	1365 33.33	6826 6.67	3413 3.33	1706 6.67	8533.33	TOA 1 (NANOSEC) 4266.67	2133.33	1066.67	533.33	266.67	133.33	66.67	33.33	16.67
3579 1394 130.0	1789 5697 007.0	8947 8485 33.0	4473 9242 67.0	2236 9621 33.0	1118 4810 67.0	5592 4053 3.30	TOA 2 (NANO SEC) 2796 2026 6.70	1398 1013 3.33	6990 5066 .67	3495 2533 .33	1747 6266 .67	8738 133.33	4369 066.67	2184 533.33	1092 266.67
1	0.5	.25	AMPL (V) .125	.0625	.03125	.015 625	.0078 125	1	0.5	.25	FREQ (V) .125	.0625	.03125	.015 625	.0078 125
					OCTANT ØA B_0	B_1	B_2	1	0.5	.25	PHASE A .125	.0625	.03125	.015 625	.0078 125
					OCTANT ØB B_0	B_1	B_2	1	0.5	.25	PHASE B .125	.0625	.03125	.015 625	.0078 125
					OCTANT ØA B_0	B_1	B_2	1	0.5	PHASE A CAL .25	.125	.0625	.03125	.015 625	.0078 125
					OCTANT ØB B_0	B_1	B_2	1	0.5	PHASE B CAL .25	.125	.0625	.03125	.015 625	.0078 125

D.B. 9-30-76

Table 2.3

SCHANS Input Functions

RF Freq. Cal Mode

0 MSB	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15 LSB
5461 33.33	2730 66.67	1365 33.33	6826 6.67	3413 3.33	1706 6.67	8533.33	TOA 1 (NANOSEC) 4266.67	2133.33	1066.67	533.33	266.67	133.33	66.67	33.33	16.67
3579 1394 130.0	1789 5697 007.0	8947 8485 33.0	4473 9242 67.0	2236 9621 33.0	1118 4810 67.0	5592 4053 3.30	TOA 2 (NANO SEC) 2796 2026 6.70	1398 1013 3.33	6990 5066 .67	3495 2533 .33	1747 6266 .67	8738 133.33	4369 066.67	2184 533.33	1092 266.67
			AMPL (V)								FREQ (V)				
1	0.5	.25	.125	.0625	.03125	.015 625	.0078 125	1	0.5	.25	.125	.0625	.03125	.015 625	.0078 125
					OCTANT ØA						PHASE A				
					B_0	B_1	B_2	1	0.5	.25	.125	.0625	.03125	.015 625	.0078 125
					OCTANT ØB						PHASE B				
					B_0	B_1	B_2	1	0.5	.25	.125	.0625	.03125	.015 625	.0078 125

9-30-76 D.B.

Table 2.4

SCHANS Input Functions

IF Ø MODE

0 MSB	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15 LSB
—	—	—	—	—	OCTANT ØA					RAW SIN A AMP.				.015	.0078
					B_0	B_1	B_2	1	0.5	.25	.125	.0625	.03125	625	125
—	—	—	—	—	OCTANT ØA					RAW COS A AMP.				.015	.0078
					B_0	B_1	B_2	1	0.5	.25	.125	.0625	.03125	625	125
—	—	—	—	—	OCTANT ØB					RAW SIN B AMP.				.015	.0078
					B_0	B_1	B_2	1	0.5	.25	.125	.0625	.03125	625	125
—	—	—	—	—	OCTANT ØB					RAW COS B AMP.				.015	.0078
					B_0	B_1	B_2	1	0.5	.25	.125	.0625	.03125	625	125

9-30-76 DB

Table 2.5

SCHANS I/O BIT FORMATION OUTPUT FUNCTION

FUNCTION	BIT															
	ADDRESS		DATA													
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
REC. TUNING	0	0	SPARE	SPARE	MSB 200.0976 MHZ	100.0488 MHZ	50.0224 MHZ	25.0112 MHZ	12.5056 MHZ	6.2528 MHZ	3.1264 MHZ	1.5632 MHZ	.7816 MHZ	.3908 MHZ	.1954 MHZ	LSB .0977 MHZ
MODE REGISTER	0	1	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	USE FREQ WINDOW	WIDE PULSE MODE	IF CAL SEL 2	IF CAL SEL 1	IF CAL MODE	RF FREQ CAL MODE	ANT. SEL.	PROC EN.
SPARE	1	0														
SPARE	1	1														

Table 2.6

SCHANS I/O BIT FORMATION

BIT POSITION	SIGNAL NAME	DEFINITION
BIT 15	PROCESS ENABLE	ϕ PROCESSING DISABLED 1 PROCESSING ENABLED
BIT 14	ANTENNA SELECT	ϕ ANTENNA #1 1 ANTENNA #2
BIT 13	RF FREQ CAL MODE	ϕ RF FREQ CAL MODE 1 NORMAL MODE
BIT 12	IF CAL MODE	ϕ NORMAL MODE 1 IF CAL MODE
BIT 11 BIT 10	IF CAL. SEL. 1 IF CAL. SEL. 2	SEL 1 / SEL 2 / IF CAL SEC. ϕ / ϕ / - 45° ϕ / 1 / + 45° 1 / ϕ / +135° 1 / 1 / +225°
BIT 9	WIDE PULSE MODE	ϕ HOLD AT 0.7 μs 1 HOLD AT 5 μs
BIT 8	USE FREQ WINDOW	ϕ WINDOW DISABLED 1 WINDOW ENABLED

3.0 DETAILED DESCRIPTION OF OPERATION FOR EACH MIB

This section provides a detailed description of the operation of each mib in the PCU. In order to understand the operation the reader will require a set of schematics to follow the description. The drawing numbers for each of the schematics are as follows:

LOCATION	FUNCTION	SCHEMATIC NO.
A10A SIDE	PHASE PROCESSING	6102857
A10B SIDE	A/D CONVERTER	6102867
A11 A SIDE	SAMPLE AND HOLD	6102787
A11 B SIDE	AMPLITUDE PROCESSING	6102797
A12 A SIDE	TOA COUNTER/BUFFER	6102807
A12 B SIDE	DATA MUX	6102817
A13 A SIDE	MODE AND TUNING CONTROL	6102887
A14 B SIDE	PROCESS CYCLE TIMING	6102837
A6	OSCILLATOR ASSEMBLY	6102753

3.1 PHASE PROCESSING MIB (A10 A SIDE)

The functions packaged on this mib are the Absolute Value Amplifiers, Phase Processing Logic and the Analog Multiplexer.

There are 4 Absolute Value Amplifiers (AVA) on the mib, one for each sine and cosine input. When the input is positive the output of U7 goes negative and the output of U8 goes positive causing CR2 to become reversed biased and CR4 to become forward biased. Thus the path from the input to the output of the AVA is thru non inverting amplifier U8. Since CR2 is reversed biased the feedback loop for U7 has been opened thus CR1 is included to prevent the output of U7 to go to negative supply voltage. The output of U7 is clamped to about -.7V. When the input voltage is negative the output of U7 goes positive and the output of U8 goes negative causing CR2 to become forward biased and CR4 to become reversed biased. Thus the path from the input to the output of the AVA is thru the inverting unity gain amplifier U7. The gain of the stage is established by the pair of matched resistors R23A and R23B. The tolerance on the matching of this pair of resistors is 0.05% and the TC tracking is 5 ppm. Under this condition CR4 is reversed biased and the feed back path for U8 thru R24A is open circuited. Thus, CR3 is included to keep the output of U8 from going to the negative supply voltage. The output of U8 is changed to about -.7V.

The offset voltage of U7 and U8 can be compensated for by adjusting R31 and R32 respectively. The offset voltage of U8 is adjusted for zero by applying a small positive input to the AVA input and adjusting R32 until the AVA output voltage is equal to the input voltage. To adjust the offset voltage of U7 to zero a small negative input should be applied to the AVA input and R31 adjusted until the AVA output is equal and of opposite polarity to the input.

Each sine and cosine input has a comparator (U1, U2, U3, U4) associated with it. The function of this comparator is to indicate to the phase decode logic the polarity of each of these inputs. Also the output

of the sine and cosine AVA's are compared to each other by two comparators U5 and U6. This gives an indication to the phase decode logic of the relative magnitudes of the sine and cosine.

The states of these comparators are strobed into registers U15 and U16, by SECTSTR,to be used by the decode logic and to control the phase portion of the analog multiplexer. The strobe occurs at MUX1 time which is at least 1 us after hold gate which gives sufficient time for the AVA and comparator outputs to settle. This data will then be used by the decode logic to determine the octant bits and which input, sine or cosine, to convert.

In order to maintain the highest accuracy in processing the phase data the input that is converter must be on its steepest slope. For example between 0 to 45° the sine should be selected and between 45° to 135° the cosine selected, etc. This decision is made by comparing the absolute value of the sine to the cosine and selecting the one that is smaller. Thus SELSA is a "1" when ACA is greater than ASA and SELCA is a "1" when ASA is greater than ACA.

Figure 3.1 shows the amplitudes of the sine and cosine inputs verses the electrical degrees of phase shift. Actually the sine input is -sineØ. For each octant the following observation can be made:

OCTANT			POLARITY OF SINE	POLARITY OF COSINE	RELATIVE AMPLITUDE OF SINE & COSINE
B0	B1	B2			
0	0	0	-	+	$\|S\| < \|C\|$
0	0	0	-	+	$\|C\| < \|S\|$
0	1	0	-	-	$\|C\| < \|S\|$
0	1	1	-	-	$\|S\| < \|C\|$
1	0	0	+	-	$\|S\| < \|C\|$
1	0	1	+	-	$\|C\| < \|S\|$
1	1	0	+	+	$\|C\| < \|S\|$
1	1	1	+	+	$\|S\| < \|C\|$

Note, B0 is a "0" when the sine is negative and is a "1" when the sine is positive. Thus PHDECØA is the same polarity as SAG.

Also when the sine and cosine are the same polarity B1 is a "1" and when they are opposite polarity B1 is a "0". This function is the not of the exclusive or of the polarities of the sine and cosine. This is accomplished by taking the inverse of SAG (U16 pin 3) and doing an exclusive or with CAG (U16 pin 10) to generate B1 which is PHDEC1A.

To obtain B2 note that whenever $|S| > |C|$ comparator (U6) output and B1 have the same logic state, B2 is a "1" and when they have a different logic state B2 is a "0". Thus the $|S| > |C|$ output of U16 (pin 7) and PH DEC1A are exclusive ored to generate PH DEC2A.

The same logic is repeated for phase B inputs.

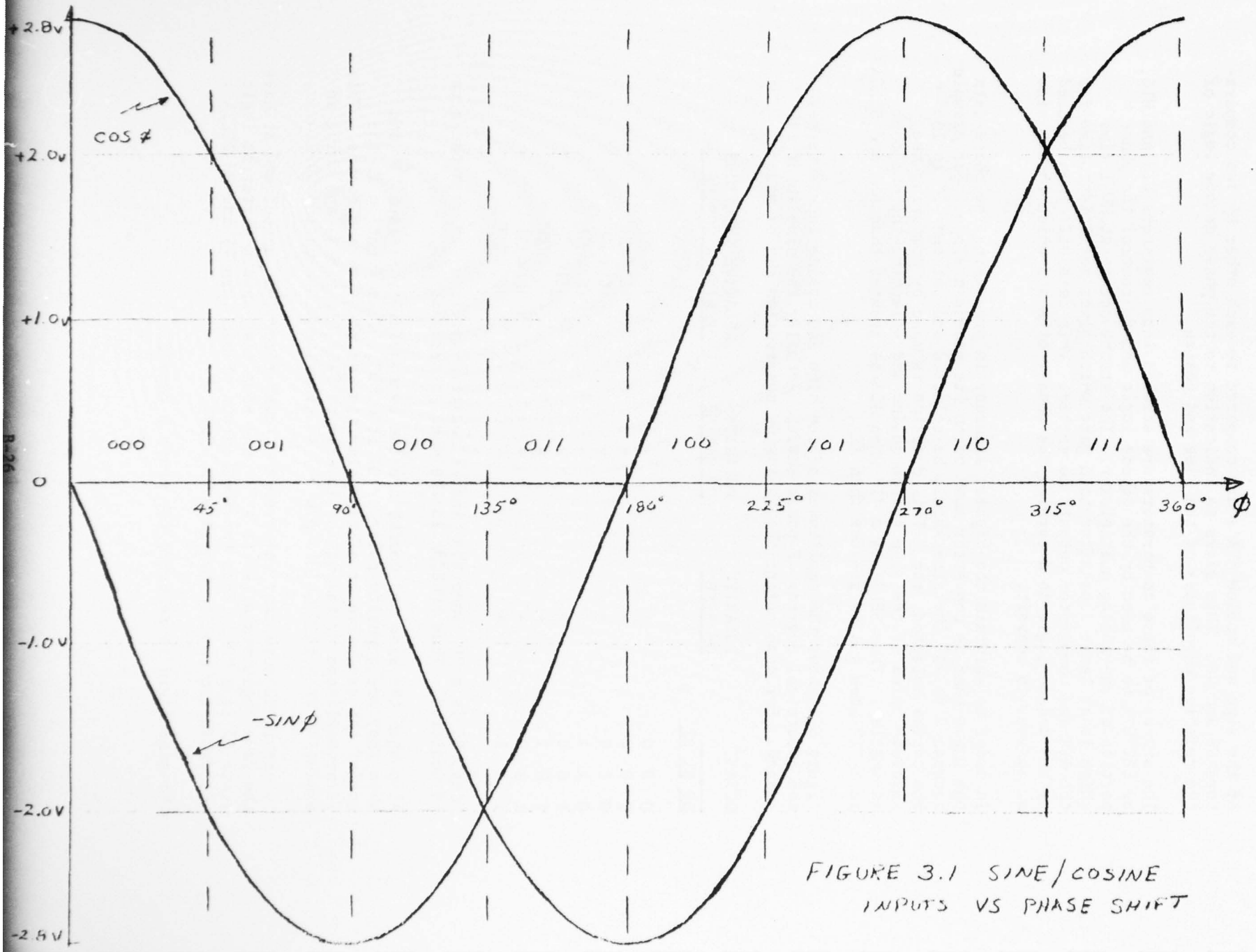


FIGURE 3.1 SINE/COSINE INPUTS VS PHASE SHIFT

The last function on this mib is the analog multiplexer which switches amplitude, frequency and phase voltages to the A/D converter. The multiplexer is comprised of 4 dual JFET switches, U23 thru U26. JFET switches were selected because of the difficulty encountered in radiation hardening MOS circuits. The IH 5004 has a turn on time of less than .3 us and a turn off time of less than .8 us thus the 1.1 us dead time between conversions will ensure that no two switches are fully on simultaneously. The on resistance is 50 ohm thus the error introduced by this series on resistance and the high input impedance voltage follower in the A/D converter is negligible.

One switch in U26 is a shunt switch and connects the A/D input to ground thru a 1K resistor when the multiplexer series switches are not being activated. This will insure that the input stage to the A/D converter is never working from a high output impedance for a long period of time. If the input to the A/D was open circuited the stages could go into saturation causing a long recovery time for the next conversion.

The logic driving the multiplexer is designed such that the conversion are made in the following order for each of the three modes:

ORDER OF CONVERSION	NORMAL	RF FREQ CAL	IF CAL
1	Amplitude	Amplitude	SinØ A
2	Frequency	Frequency	CosØ A
3	SinØA/CosØA	SinØA/CosØA	SinØ B
4	SinØB/CosØB	SinØB/CosØB	CosØ B
5	Cal-SinØA/CosØA		
6	Cal-SinØB/CosØB		

3.2 ANALOG-TO-DIGITAL CONVERTER MIB (A10 B SIDE)

This mib contains an eight bit cyclic analog-to-digital converter, an 8 bit storage register and a gray to binary code converter.

The analog-to-digital converter which has a total conversion time of 800 nanoseconds for eight bits is shown in Figure 3.2 in block diagram form. The full schematic is shown in drawing no. 6102867. The converter is an eight bit cascaded analog to Gray code converter which has an input voltage range of 0 to +2V. In addition to speed, this type of a converter has the following advantages:

AD-A038 490 IBM FEDERAL SYSTEMS DIV OWEGO N Y F/G 17/7
SELF-CONTAINED, HIGH-ALTITUDE NAVIGATION SYSTEM STUDY: PRAIS NA--ETC(U)
JAN 77 R E DRESKA, G A KOOCH, L O SMITH F04701-76-C-0106
UNCLASSIFIED IBM-77-D04-003S SAMSO -TR-77-57-VOL-3 NL

2 OF 3
AD
A038490

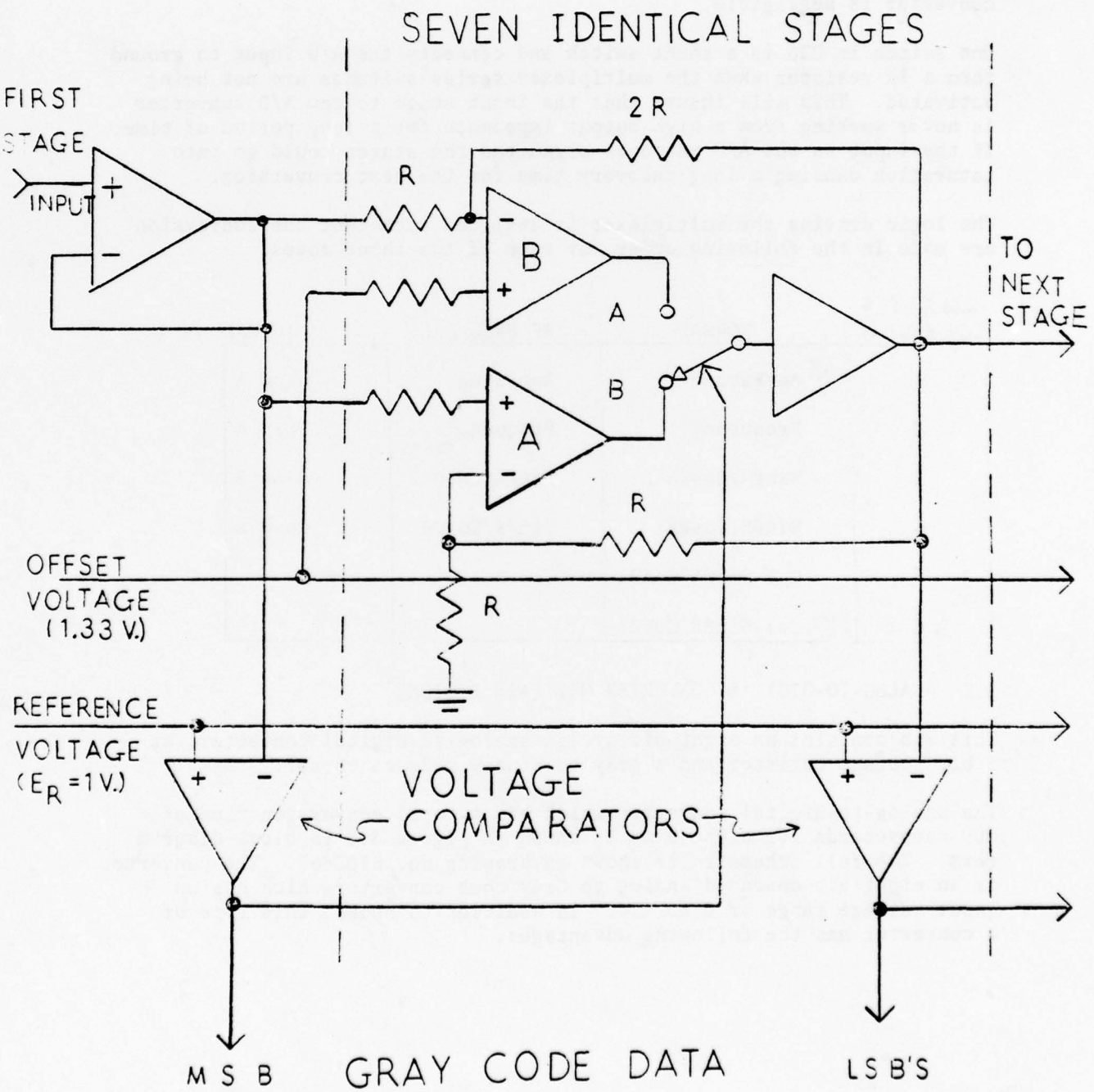
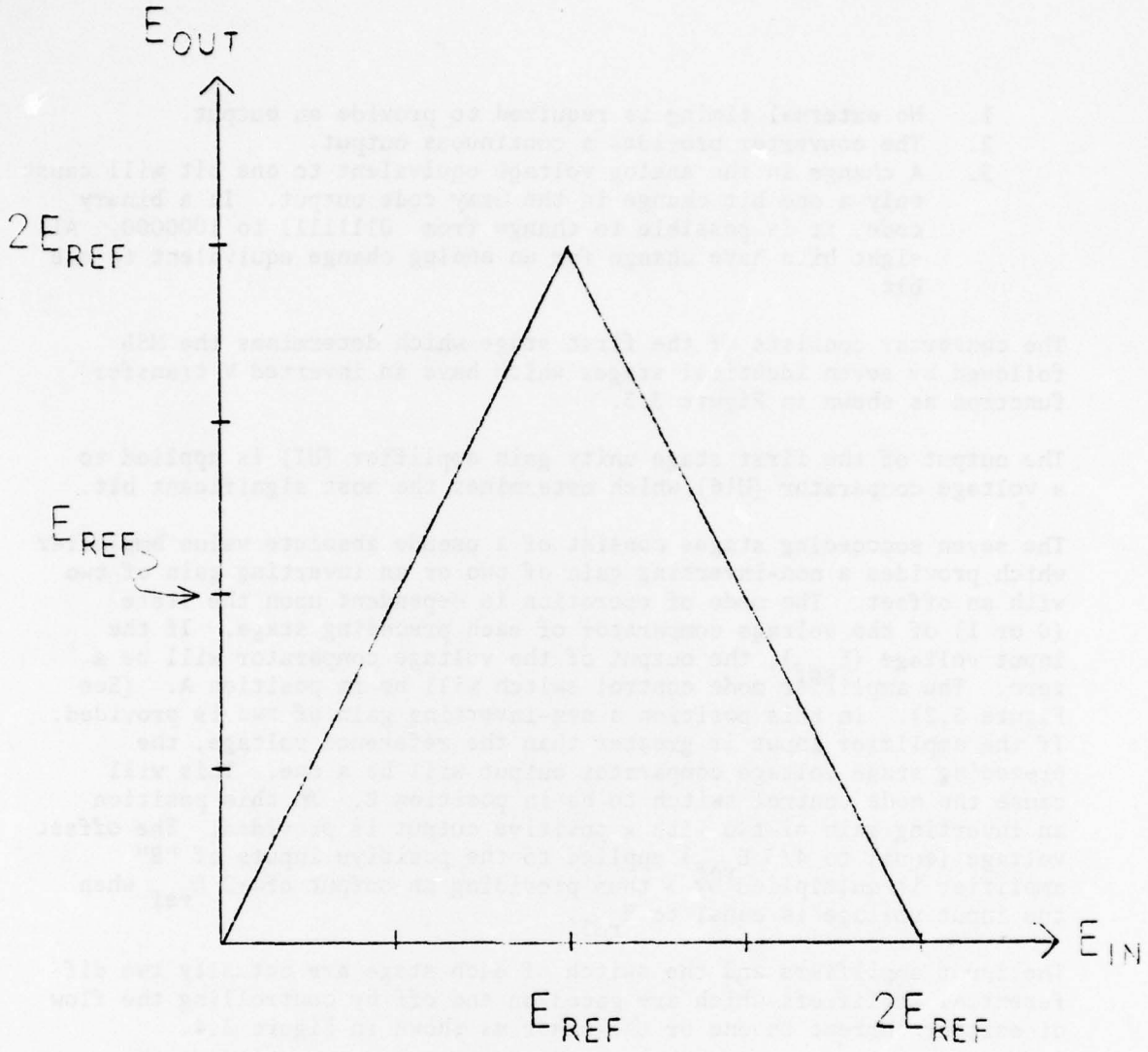


FIGURE 3.2 CASCODED A/D CONVERTER



$$E_{OUT} = 2E_{IN} \Big|_{E_{IN} \leq E_{REF}}$$

$$E_{OUT} = 4E_{REF} - 2E_{IN} \Big|_{E_{IN} \geq E_{REF}}$$

FIGURE 3.3

TRANSFER FUNCTION OF CASCODED A/D CONVERTER AMPLIFIER STAGE

1. No external timing is required to provide an output.
2. The converter provides a continuous output.
3. A change in the analog voltage equivalent to one bit will cause only a one bit change in the Gray code output. In a binary code, it is possible to change from 01111111 to 1000000. All eight bits have change for an analog change equivalent to one bit.

The converter consists of the first stage which determines the MSB followed by seven identical stages which have an inverted V transfer function as shown in Figure 3.3.

The output of the first stage unity gain amplifier (UI) is applied to a voltage comparator (U16) which determines the most significant bit.

The seven succeeding stages consist of a pseudo absolute value amplifier which provides a non-inverting gain of two or an inverting gain of two with an offset. The mode of operation is dependent upon the state (0 or 1) of the voltage comparator of each preceding stage. If the input voltage (E_{ref}), the output of the voltage comparator will be a zero. The amplifier mode control switch will be in position A. (See Figure 3.2). In this position a non-inverting gain of two is provided. If the amplifier input is greater than the reference voltage, the preceding stage voltage comparator output will be a one. This will cause the mode control switch to be in position B. In this position an inverting gain of two with a positive output is provided. The offset voltage (equal to 4/3 E_{ref}) applied to the positive inputs of "B" amplifier is multiplied by 3 thus providing an output of +2 E_{ref} when the input voltage is equal to E_{ref}.

The input amplifiers and the switch of each stage are actually two differential amplifiers which are gated on and off by controlling the flow of emitter current to one or the other as shown in Figure 3.4.

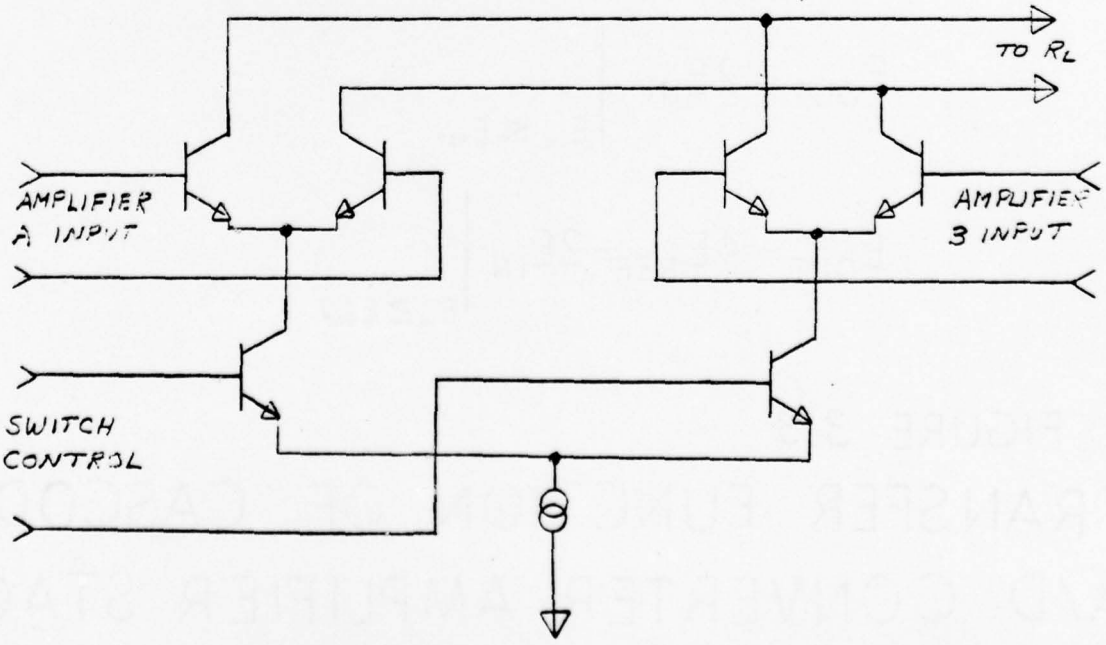


Figure 3.4 AMPLIFIER SWITCHING

This circuitry is available in integrated circuit form as an MC1545.

Figure 3.5 shows the output voltage of the first four stages as a function of the converter input voltage.

The digital output of this converter is in Gray code which is easily converted to a binary code using exclusive or logic. The Gray code is initially stored in a register (U24, U25) before being converted to a binary code by U26 and U27. The registers are loaded with ADCLK which occurs 2.133 us after the analog voltage is applied to the input. The maximum time for the data to ripple thru the Gray to binary converter is about 150 ns. The binary data is strobed into the pulse data registers on A12 B mib 267 ns after the ADCLK so there is sufficient settling time for the Gray to binary conversion.

3.3 SAMPLE AND HOLD MIB (A11 A SIDE)

This mib contains five hybrid sample and hold modules (6088485-7) along with their associated discrete components and a 1V level shifter for the fine RF signal.

The sample and hold modules have the capability of being trimmed for zero offset voltage between the input (pin 15) and the output (pin 29) by adjusting the 1K pot between pins 25 and 26. A 5.1 ohm resistor is connected between pins 21 and 22 thus causing a sample and hold mode of operation. If it is desired to change the mode to a peak detector the resistor should be moved such that it connects pin 21 to the net EHGAT which enters the mib at P1-49.

A schematic of the sample and hold module (6088485-7) is shown in Figure 3.6. The source control drawing for the module is 6088485.

When in the sample mode Q3 is turned off and Q6 is turned on and is the constant current sink for the difference amplifier Q4 and Q5. Also Q7, Q8, and Q9 are turned on and in their quiescent state. When a positive pulse is applied to the input (pin 15) Q4 conducts harder and Q5 turns off. The collector voltage of Q4 decreases and the collector voltages of Q5 increases thus causing Q8 to turn on hard and Q7 and Q9 to turn off. The collector current from Q8 will then flow into the hold capacitor C_H causing it to charge. This capacitor will charge unitl the voltage on it is equal to the input voltage at which time the difference amplifier will become balanced causing Q8 and Q9 to be in their quiescent condition thus ceasing charging of the hold capacitor. If the capacitor should overcharge the difference amplifier will correct for the over voltage by turning on Q7 and Q9, turning off Q8, thus removing charge from the hold capacitor and reducing the voltage stored on it. This continues until the voltage on the hold capacitor and input are equal at which time the circuit returns to its quiescent state and charging of the hold capacitor ceases.

For negative inputs Q5 conducts harder and the charging current flows thru Q9 causing the voltage on the hold capacitor to go negative.

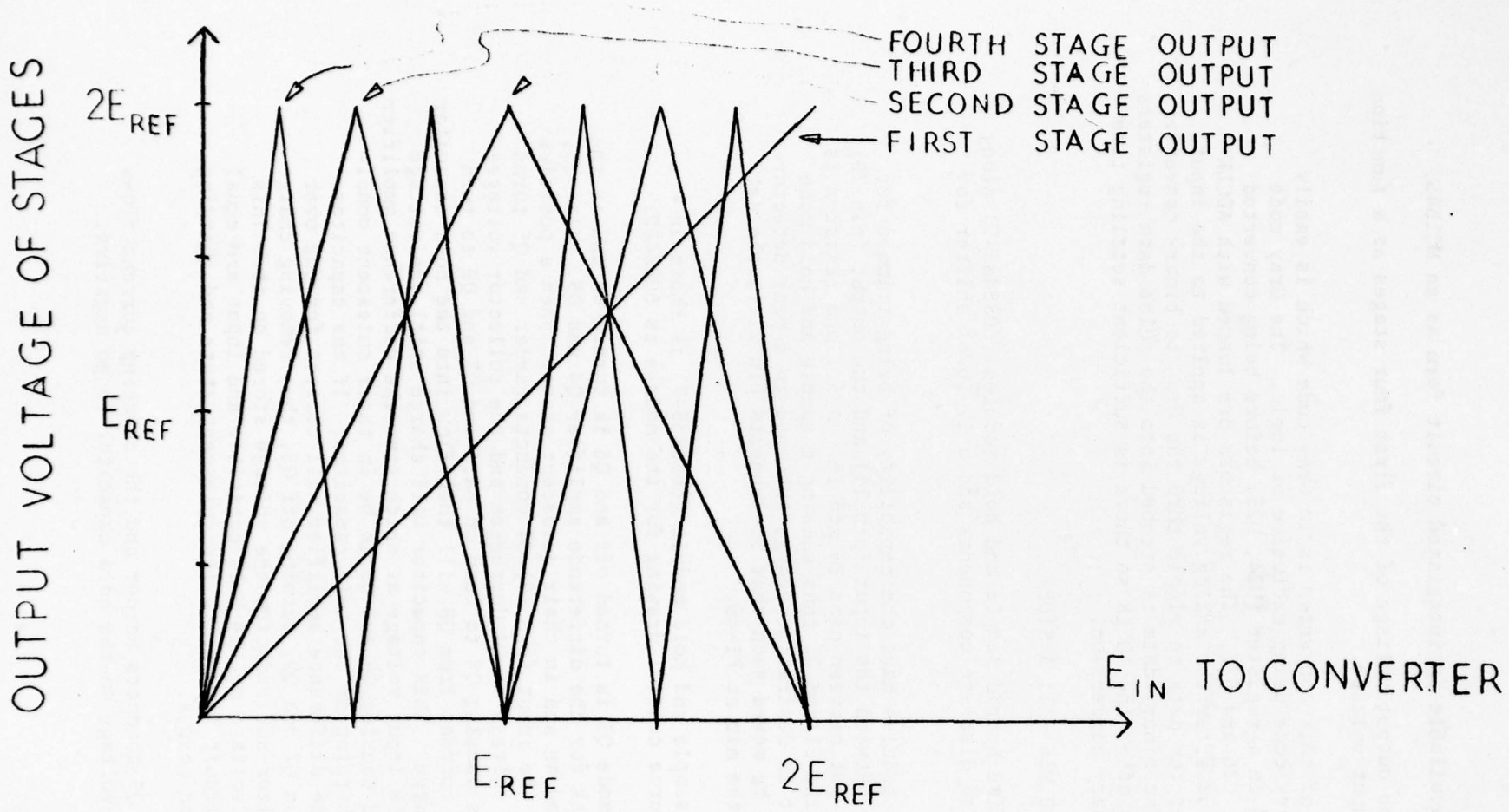


FIGURE 3.5

TRANSFER FUNCTION OF FIRST FOUR STAGES AS A FUNCTION OF CONVERTER INPUT VOLTAGE

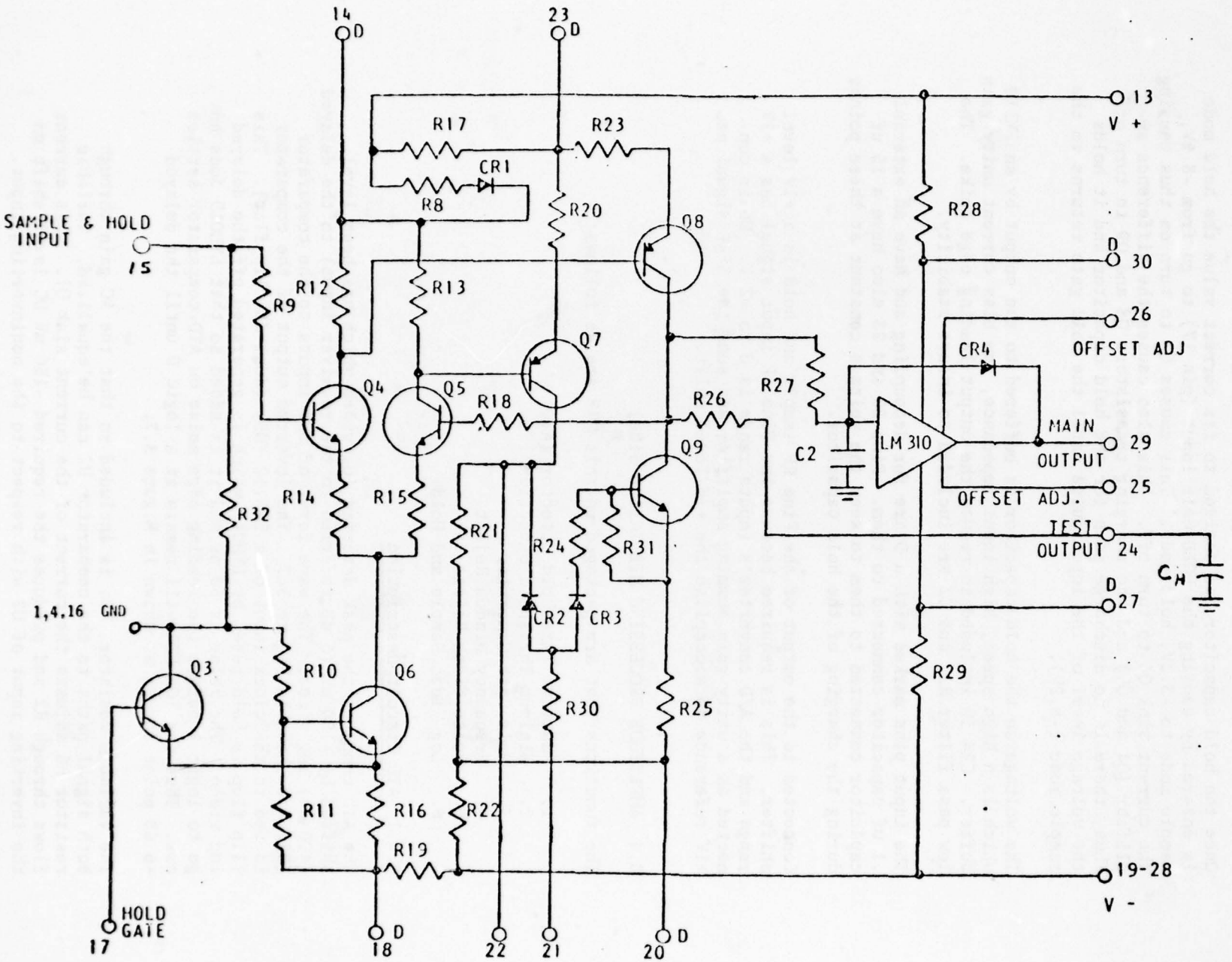


Figure 3.6 Sample & Hold Schematic

Once the hold capacitor has charged to its correct value the hold mode is entered by causing the HOLD GATE input (pin 17) to go from -8.2V, sample mode to -3.2V, hold mode. This causes Q3 to turn on thus causing the current sink Q6 to turn off. This also causes the difference amplifier (Q4 and Q5) and the charging transistors Q8 and Q9 to turn off. Thus, there is no discharge path for the hold capacitor and it holds the voltage level of the input pulse until the hold gate returns to the sample mode (-8.2V).

The voltage on the hold capacitor is buffered to the output by an LM110 which is a high speed, high input impedance, low bias current unity gain buffer. CR4 is included to reduce the output leading edge spike. The low pass filter R27 and C2 are included to insure stability.

The input pins marked with a D are for decoupling and have an external .1 uf capacitor connected to them. Pins 20 and 23 also have a 15 uf capacitor connected to them to keep the voltage constant at these points during the charging of the hold capacitor.

Connected to the output of the Fine RF sample and hold is a +1V level shifter. This is required because the Fine RF input signal has a +1V range and the A/D converter's inputs range is 0 to +2 V. U6 is connected as a unity gain summing amplifier and sums the SFRF signal and +1V reference to accomplish the +1V level shift.

3.4 AMPLITUDE PROCESSING MIB (A11 B Side)

The functions that are packaged on this MIB are as follows:

1. Adaptive Threshold Detector (ATD)
2. Minimum Threshold Detection
3. Hold Gate Generator
4. Frequency Window Reject
5. Pulse Width Reject
6. Log Video Sample and Hold

3.4.1 ATD Circuit Description

The ATD compares the peak detected log video which has been level shifted by -150 mV (6 dB referred to the receiver input) to the delayed (400 ns) log video. The wave forms of the inputs to the comparator (U2) are shown in Figure 3.7. The inverted output of the comparator is fed to the clock input of a 54S112 (U5) (dual JK flip flop). This flip flop is held reset by LTHOLD which is generated off the delayed log video. The delay is 50 ns and it is added so that LTHOLD does not go to logic 1 before the leading edge noise on ATD comparator settles out. Thus the TOA STR will remain at a logic 0 until the delayed -6 dB point occurs as shown in Figure 3.7.

The variable resistor, R2, is included so that the AC gain through both signal paths to the comparator U2 can be equalized. Variable resistor R6 adjusts the current of the current sink Q1. This current flows through R2 and produces the required -150 mV DC level shift on the inverting input of U2 with respect to the noninverting input.

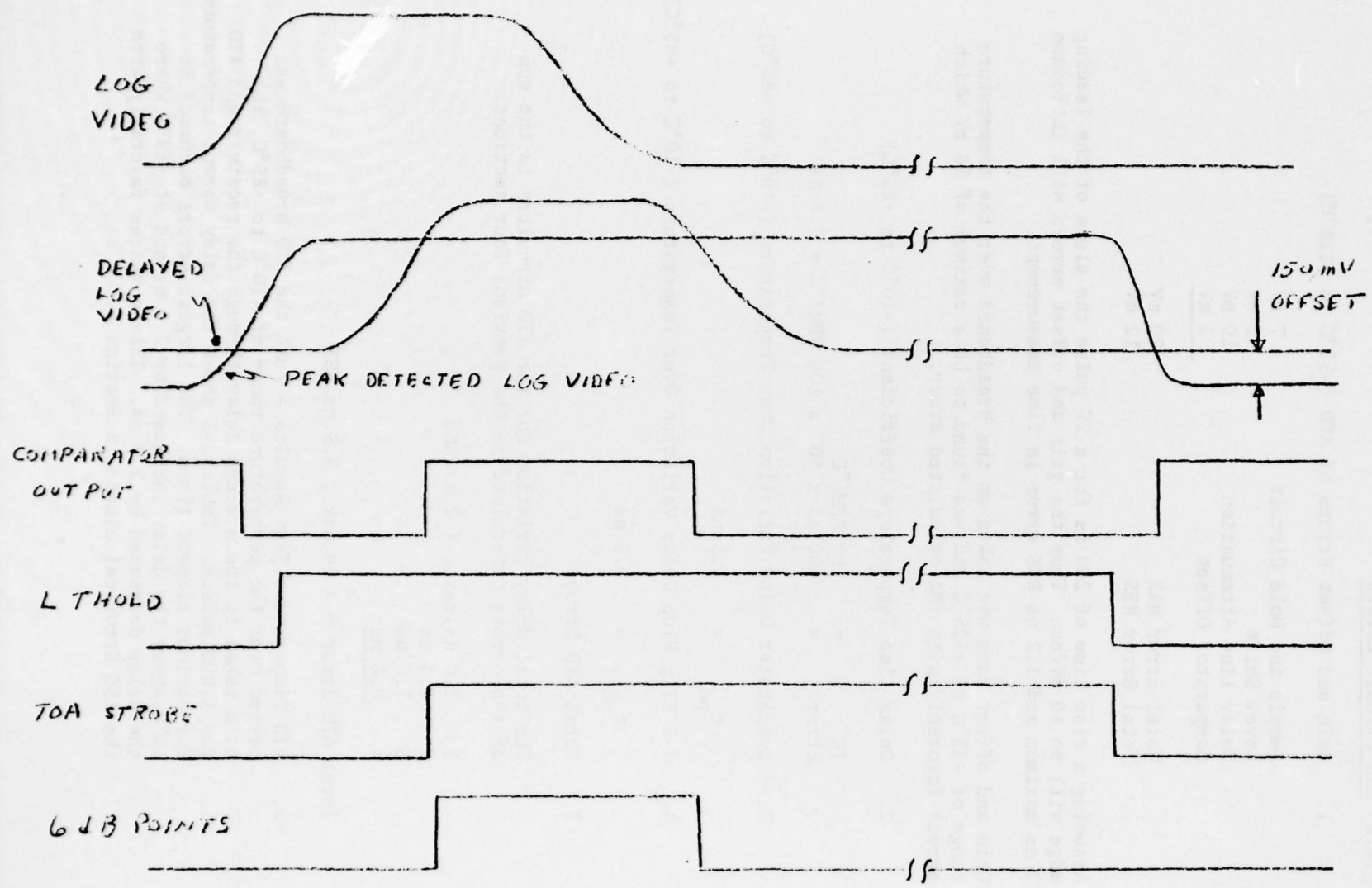


FIGURE 3.7 A/D SIGNAL WAVE FORMS

3.4.2 ATD Circuit Errors

1. Gain and Offset Errors of ATD (-55°C to +125°C)

Sample and Hold Circuit	7 mV
Level Shift	2 mV
Delay Line Attenuation	10 mV
Comparator Offset	1 mV
Total Error MAX	20 mV
Total Error RSS	12 mV

Assuming a rise time of 200 ns for a 2V pulse the slope of the leading edge will be 10 mV/ns. Thus the gain and offset errors will introduce 2 ns maximum and 1.2 ns RSS error in time measurement.

Gain and offset data was taken on the breadboard over the temperature range of -55°C to +125°C and was found to be a maximum of 10 mV which agrees favorably with the calculated error.

2. Delay Line Temperature Coefficient (-10°C to +85°C)

TC = 100 PPM/°C
Error = 400 ns x 60° x 100 PPM/°C = 2.4 ns

3. Comparator Delay Variation Over Temperature (-10°C to +85°C)

t_{pd} = 1.5 ns

4. J-K Flip Flop Delay Variation Over Temperature (-10°C to +85°C)

t_{pd} = 0.5 ns

5. Total ATD Error

The total delay variation for the ATD circuitry is the sum of the errors determined in the previous four sections:

1	2.0 ns max., 1.2 ns RSS
2	2.4 ns
3	1.5 ns
4	0.5 ns

Total ATD Error 6.4 ns max., 3.5 ns RSS

6. ATD Temperature Test Results - Just the ATD breadboard was tested over the temperature range of -10°C to +85°C, the data taken is the average delay through the receiver and ATD for 1,000 pulses. Table 3-1 shows the delay versus temperature for various elapsed times. The largest errors occurred at 10°C where the delay increased by 2.4 ns and at +85°C where the delay decreased by 2.4 ns. This compares favorably with the RSS Error calculated in Section 5.

TABLE 3.1 ATD TEMPERATURE DATA

ELAPSED TIME (HRS:MIN)	TEMPERATURE (^{o}C)	DELAY (NS)
00:00*	-10	863.4
00:05	-10	863.6
00:10	-10	863.6
00:30	+25	861.5
00:35	+25	861.2
00:45	+50	860.6
00:50	+50	860.6
00:55	+70	859.6
01:00	+85	859.2
01:05	+85	859.1
01:10	+85	859.2
01:15	+85	859.0
01:20	+85	858.8

*After 15 minutes at -10^{o}C ambient.

7. ATD Breadboard Test Results - Figure 3.8 has two pictures that show the delay variation of the ATD output as the temperature changed from +25°C to +80°C. The change appears to be about 2 ns which correlates with the 2.4 ns shown in the data in Table 3.1.

3.4.3 Minimum Threshold Detector

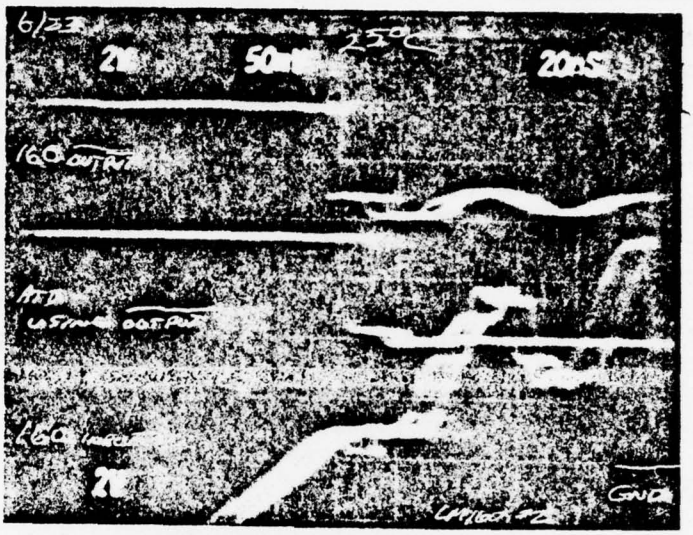
Detection of an input pulse exceeding the minimum threshold of the system is indicated by the uA 710 comparator U8. The threshold level is set at about 250 mV on pin 3 of U8 by the variable resistor R29. Resistors R30, 31, and R36 provide hysteresis for the threshold detector. Hysteresis is introduced by the action of U9 output going to a logic 0 when the log video pulse initially breaks threshold. This causes the reference voltage on U8 pin 3 to decrease by 30 mV due to the feedbakc path through R31. The delay in the threshold required for the ATD is provided by the 50 ns delay line (DL2). The signal RTHOLD is the raw threshold that is not degated by any of the control signals and is used to indicate to the PCT mib the input pulse has ended, thus a reset can be made. Thresholds can be disabled by PROCEN (mode control from SPU), PBUSYN (from PCT indicating a signal is being processed), RCVBLKN (from receiver indicating a signal is being processed or receiver is tuning a new frequency), or NORMAL (threshold can only be generated in normal mode). Latched threshold (LTHOLD) is generated by clocking a DFF (U10). This signal is sent to the ATD circuitry and to the 95% circuitry.

3.4.4 Hold Gate Generator

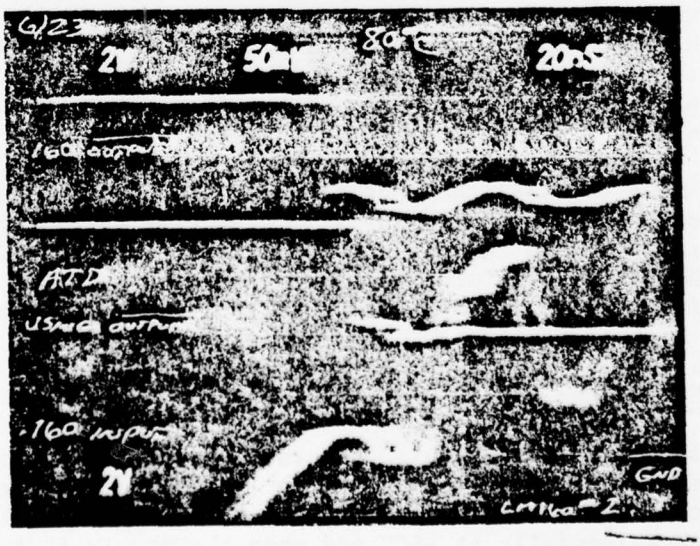
The comparator U7 compares the output of a 50 ns delay to the output of an attenuator with a 5% attenuation. Thus when the log video has reached 95% of its final value, the comparator output goes to a logic 1 indicating the 95% point on the log video pulse. This point is used to start the timing for the generation of the hold gates for the sample and hold circuits. In the narrow pulse mode (NNPN) a delay of about 400 ns (U12 Pin 12) is introduced before LHOLD is issued by U14. In the wide pulse mode (NWPN) a delay of about 5 us (U12 Pin 4) is introduced between the breaking of threshold (LTHOLD) and the generation of LHOLD. LHOLD is reset by RSTHLDN which occurs after the radar pulse processing is complete or after the process cycle is complete. It can be set by CALMSN which is generated by the process cycle timing mib to generate a hold gate when the time out has expired for the settling of the receiver circuits when the unit is in one of the calibration modes.

The 95% point signal also goes to U13 which introduces about a 500 ns delay to generate STRQUAL. This signal strobes the receiver qual signal which indicates an in band signal. There is more delay in the receiver for the qual signal than for the log video, phase or frequency signals therefore the qual strobe has to be delayed more than the hold gate.

Two separate hold gates are generated, one for the phase and frequency sample and holds (HOLDGPF); the other for the log video sample and hold (HOLDGLV). The sample and holds require a hold gate that is a -8.3V in the sample mode and at -3.3V in the hold mode. These levels are generated by the level shifters Q5, VR2 and Q6 for HOLDGPF and Q7, VR3 and Q8 for HOLDGLV. Two hold gates are generated as a precaution in



TEMP. = 25°C



TEMP. = 80°C

FIGURE 3.6 ATD DELAY CHANGE OVER TEMPATURE

the case where the receiver timing would be such that one hold point would not be sufficient to sample all the pulse data at the optimal point. Should the case arise that all pulse data could be sampled at one time, one of the hold gates can be eliminated thus saving components and power.

3.4.5 Frequency Window Reject

This circuit indicates when frequency discriminator signal is outisde of a ±200 mV window. The output of the frequency sample and hold (SFRF) is applied to the inverting input of one comparator in the dual comparator U11 and the non-inverting input is connected to a voltage divider (R40, R43) which is the lower bound. If the lower bound is greater than SFRF the output of U11 will go up indicating the signal is out of range (RFOOR). The other half of the dual comparator non-inverting input is connected to SFRF and the inverting input connected to the upper bound derived from the voltage divider R41 and R42. Thus when SFRF exceeds the upper bound the output of the comparator U11 will also go up indicating an out of range condition. The out of range signal (RFOOR) is sent to the PCT mib where the pulse being processed will be rejected, and the PCU will look for a new pulse, if the PCU is in the Use Frequency Window Mode and if the signal is out of range.

3.4.6 Pulse Width Reject

The pulse width reject circuitry operates in two modes; one being the narrow pulse mode the other being the wide pulse mode. When in the narrow pulse mode (NNPN=0) the minimum pulse width is checked between the 6 dB points and is tested for a minimum width of 600 ns. The signal NNPN="0" enables the 600 ns time out single shot U15 and resets the DFF U16 such that wide pulse accept (WPACC) is a logic 1. The leading edge of the signal 6 dB points triggers the single shot U15 such that it times out 600 ns. When the time out ends the rising edge of U15 pin 4 clocks the DFF U16 such that if the signal 6 dB points is still present a "1" is clocked into U16 pin 5, thus indicating the pulse width is greater than 600 ns (NPACC="1"). If the pulse is less than 600 ns wide then NPACC will be a "0" and the PCT mib will reject the pulse.

In the wide pulse mode (NWPN=0) the 5 us time out of U15 is enabled and NPACC is forced to an accept (NPACC="1"). The time out is started by LTHOLD and if after 4.5 us the pulse still exceeds threshold (RTHOLDN ="0") then U16 pin 9 (WPACC) is clocked to a 1. If the pulse is less than 5 us wide WPACC will be a "0" and the PCT mib will reject the pulse.

3.4.7 Log Video Sample and Hold

The sample and hold hybrid circuit used for the log video term is connected such that it operates as a peak detector. Thus the module requires an end of hold gate (EHGAT) to reset the output to zero after all processing is complete. EHGAT is normally at -14V and when the module is to be reset this signal becomes -1V. It is connected by placing R12 between U4 pin 21 and the EHGAT line. The hold capacitor is C21 and the resistor R13 is added to roll off the response. The offset between the input log video

(LV) and the output amplitude (LVAMP) is adjusted to zero by the variable resistor R14.

EHGAT is generated by ARSTN driving the saturated switch Q2 whose collector switches between ground and -15V supply. The push/pull emitter follower Q3 and Q4 drive this signal to the sample and hold modules.

3.5 TOA COUNTER/BUFFER MIB (A12A SIDE)

The TOA mib is made up of three basic circuits, TOA SAMPLER, TOA COUNTER and TOA STORAGE REGISTERS.

The TOA COUNTER counts from 16.7 ns to approximately 35.7 ns in 32 bits. With a clock frequency of 60 MHz, the counter counts continuously. The first four bits of the TOA counter are made up of four J-K Flip-Flops (A3, A5, B5). Due to the high speed of the clock, the use of Schottky logic for the four LSB bits was necessary. The TOA SAMPLER circuit is a negative edge triggered input. The TOASTRN clocks the J-K (C2) which caused the input of the next J-K (C2) to go High. The second half of J-K (C2) and both sections of J-K (C3) form a three bit shift register which is reset after the Third 60 MHz clock. The output of the third stage of the shift register is ANDed with the 60 MHz clock. The output of the AND circuit strobes the four bit storage register with the instantaneous data from the TOA COUNTER. 60 MHz Buf is run through the same gates as the TOA Sampler STGS 1 & 2. This is done so that the 60 MHz TOA and TOA Sampler STGS 1 & 2 have the same amount of delay.

The outputs of the first four TOA COUNTER stages are used to generate a TOA SAMPLER N strobe which in turn strobes the remaining 28 bits of TOA data from the counter.

The outputs of the first four counter stages are called TOA STG1, TOASTG2, TOASTG3, and TOASTG4. TOASTG1, TOASTG3 and TOASTG4 are ANDed with Q3 RSTN and then go to the K input of the J-K (A3). TOASTG2 is used as a clock for J-K (A3). Q3RSTN sets the J-K (A3) to a "1" after the clock has clocked a "0" on the Q output. It is the negative going edge that clocks the eight storage registers with 28 bits of TOA COUNTER Data. This strobe for the 28 MSB's (TOA SAMPLER N) occurs just as these stages are going to be clocked and all stages would have been settled out at this time causing no transition errors in these bits.

3.5.1 TOA Counter Breadboard Test Results

The TOA Counter/Buffer breadboard was tested as described in the "SCHANS Critical Component Test Plan" IBM No. 76-L74-007S "B". A pair of pulses (TOA1, TOA2) strobes the TOA counter at a 200 KHz rate. The test circuitry takes the difference between TOA1 and TOA2 to generate a ΔTOA which is compared to an upper and lower bound to determine the error rate of the TOA Counter/Buffer.

The delay was generated by a shift register that was eight stages long with a shift clock of 12.5 MHz. TOA1 was taken off of Stage 1 and TOA2 was taken off of Stage 8. Thus the delay generated between TOA1 and TOA2

was $7/12.5 \times 10^6$ or 560 ns. This corresponds to 33.6 counts of the TOA counter and the nominal ΔTOA observed was alternating between 00100001 (33) and 00100010 (34).

In test #1 the acceptable window was set at 00100000 (32) and 00100011 (35). The test was run for the required time and 19 ΔTOA measurements were observed outside these limits. The ΔTOA measurements were made at a 200 KHz rate for 6 days.

For test #2 the window was increased to a lower bound of 00011111 (31) and an upper bound of 00100100 (36). After running the test for the required time no ΔTOA measurements occurred outside these limits.

For test #3 the window was decreased to a lower bound of 00100001 (33) and an upper bound of 00100010 (34) and it was observed that on an average 32 ΔTOA measurements were outisde the window every 61 seconds. At a ΔTOA measurement rate of 200 KHz this corresponds to an error rate of 2.62×10^{-6}.

The results of these tests are summarized in Table 3-2.

The errors falling outside the limits of the least significant bit (i.e., 00100001 and 00100010) are apparently caused by noise on the TOA-2 trigger pulse. If the trigger noise is assumed Gaussian, then the error rate of 2.62×10^{-6} corresponds to 4.7σ. For a least significant bit error of ± 8.33 nanoseconds (1σ), a 4.7σ value implies a jitter of ± 1.77 nanoseconds (ns). This jitter, combined with an oscilloscope jitter of ± 1.1 ns, results in an expected jitter in the TOA-2 trigger pulse of ± 2 ns. Figure 3.9 is an oscilloscope trace photograph that shows the TOA-2 jitter and suggests that the observed error rate is due to noise on the TOA-2 test equipment pulse.

The TOA counter/buffer was placed in a temperature chamber with the test circuitry and delay circuitry mounted outside the chamber. This was done to eliminate any temperature effects of the test or delay circuits. At room temperature the time to observe 32 ΔTOA readings outside the upper bound of 00100010 and lower bound of 00100001 was recorded and the average time was 40.5 seconds. Two-hundred thousand (200,000) measurements were made each second, hence the error rate is $32 \div 40.5 \times 200 \times 10^3$ or 3.96×10^{-6}. The tests were rerun at the temperature extremes of the commercial grade logic used in the breadboard (0°C and 70°C). At 0°C the average time was 29.7 seconds and at 70°C the average time was 44 seconds. Thus the error rates and contributions to the SCHANS error budget (ERX 16.67 ns) are as shown in Table 3.3. The increase in error rate at room temperature is attributed to noise pickup on the long lines between the test circuits and the TOA counter/buffer in the oven.

3.6 DATA MUX AND CONTROL (A12 B SIDE)

The function of the Data Mux and Control mib is to format the Amplitude, Fine Frequency, Phase and TOA information into a series of 16 bit words and transfer all or part of these words to the SPU depending upon the

Table 3.2

TOA TEST SUMMARY

Window	Number of ΔTOA Measurements Outside Window	Total Number of ΔTOA Measurements	Date
Test #1 LB = 00100000 UB = 00100011	19	1.04×10^{11}	08/10, 19
Test #2 LB = 00011111 UB = 00100100	0	0.915×10^{11}	08/24, 30
Test #3 LB = 00100001 UB = 00100010	32 Errors	Every 60 seconds 59 seconds 59 seconds 61 seconds 75 seconds 72 seconds 68 seconds 61 seconds 58 seconds 47 seconds 52 seconds	08/31

Average of 32 errors each 61 seconds.

$$\text{Error Rate} = \frac{32}{200 \text{ kHz} \times 60 \text{ seconds}} = 2.62 \times 10^{-6}$$

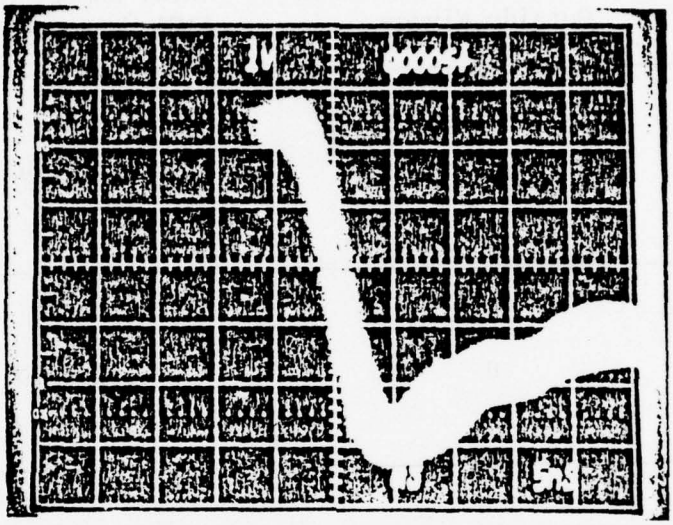


Figure 3.9. TOA-2 Pulse Leading Edge Jitter

Table 3.3

TC/B ERROR RATES

Test Temperature (^{o}C)	Error Rate	Error Budget (ns)
0	5.38×10^{-6}	8.97×10^{-5}
25	3.96×10^{-6}	6.60×10^{-5}
70	3.64×10^{-6}	6.07×10^{-5}

mode of operation. The modes of operation are NORMAL, RF FREQ CAL and IF CAL. Table 2.1 shows the data converted in each mode and Tables 2.2 thru 2.4 shows the format of the data in each mode.

In all three modes the Process Cycle Timing mib sends the proper load pulse at the proper time to the storage registers to load the A/D converter outputs into these register. CLK LVN loads the amplitude term into registers E4 and C4. CLK FRFN loads the frequency term into registers R4 and P4. CLKPHAN loads Phase A data into registers D4, B4, and A4. CLKPHBN loads Phase B data into registers N4, Q4, and S4. CLKCPHAN loads Phase A calibration data into registers F4, G4, and H4. CLKCPHBN loads Phase B calibration data into registers M4, L4, and K4 into registers M4, L4, and K4.

The outputs of these registers along with the outputs of the TOA Buffer registers are tied together and become I BUS bits Ø thru 16. These 16 lines become the inputs for the 16 differential drivers (DS7830) that sends the data to the SPU. Unloading the data from the storage registers to the I Bus is dependent upon the mode of operation and is accomplished as follows for the three modes of operation.

NORMAL MODE

Normal mode of operation is selected by decoding mode control bits 12 and 13. A bit combination of Ø1 will set the outputs of two multiplexers 54LS153 (N1, P1) to 1ØØØ. This data is present at the inputs of a 54LS174 hex DFF (G1). The address bits will not be transferred to the input of an up/down counter 54LS191 (F1) until the rising edge of CNVCMP is sent from the Process Cycle Timing (PCT) mib indicating that all data has been loaded in the registers and is ready to be transferred to the SPU.

When the PCT mib sends the CNVCMP pulse, the Hex DFF (G1) clocks the address bits to the up/down counter (F1) presetting the inputs to a 1ØØØ, and switches the 7WDSEL line to a logic "1". At the same time an up level is sent to the Data input of a 3 bit shift register (H1, J1). The outputs of the register is used to set up the proper loading conditions for the up/down counter (F1). The enable input will go to a logic "Ø", next the LDCNTR is decoded to go to a logic "0" one half clock cycle after the enable has gone to a "0". The down time of the load gate is equal to one half clock cycle. The output of the up/down counter (F1) will now be 1ØØØ. This count is decoded by decoder 54LS138 (C1) and SEL 1 will go to a logic "1".

AOI 54L551 (B2) decodes SEL 1 and 7WDSEL and its output (TOA1 SELN) goes to a logic "0".

The data in registers A9, B9, C9, and D9 is put on the data bus when TOA1SELN goes to a "0". Then the data is transferred to the output I/O thru drivers (DS7830).

IDRDY is generated two clocks later than the CNTR CLK. IDRDY is sent to the output I/O thru a driver. At this point in time no new CNTR CLKS will be generated and the IDRDY is at a logic "1" level. Nothing

will happen until an IACK is received to cause IDRDY to go to a logic "0". This is done by resetting the 3 bit shift register (L1, M1) to a logic "0". Since LD CLK GATE is still at "1" level the next rising edge of the 3.75 MHz clock will cause CNTR CLK to go to a "1" level. Two clocks later IDRDY rises and IACK causes the IDRDY to drop to a logic "0". This sequence continues until all 7 words have been transferred to the I/O output.

When the last word has been transferred one more CNTR CLK is generated, causing EOWN to drop to a "0" level. When EOWN dropped to "0", XFRCMP went to a "1" and was sent to the PCT mib indicating that a transfer of 7 words was completed and control registers were reset to zero.

RF FREQ CAL MODE

RF FREQ CAL mode of operation is selected by decoding mode control bits 12 and 13. A bit combination of ØØ will set the outputs of two multiplexers 54LS153 (N1, P1) to Ø11Ø.

The sequence of events after the RF freq cal mode has been selected is similar to the NORMAL Mode, except 5 words will be transferred instead of 7.

IF CAL MODE

IF CAL MODE of operation is selected by decoding mode control bits 12 and 13. A bit combination of 11 will set the outputs of two multiplexers 54LS153 (N1, P1) to Ø1Ø1.

The sequence of events after the IF CAL mode has been selected is similar to the Normal Mode, except 4 words will be transferred instead of 7.

3.7 MODE AND TUNING CONTROL (A13 A Side)

The functions contained on this mib are the SPU interface, mode control register, receiver tuning register, and the calibration control register. The interface between the SPU and PCU is provided by a data ready, data acknowledge transfer of 16 bits of data. The ground rules for the interface are that the data must precede data ready by at least 100 ns and the leading edge of data acknowledge loads the data into the storage register and resets the data ready line which in turn resets the data acknowledge line.

On the mode and tuning control mib the data and data ready are received by DS7820 double ended receivers. Data acknowledge is sent to the SPU by a DS7830 double ended driver.

When receiver tuning data is being sent to the PCU the address bits BOBUSØØ and BOBUSØ1 are both logic "0" (see Table 2.5 for data format). In this mode a logic"0"signal has to be sent to the receiver at least 125 ns before the data is changed in the receiver tuning word register. This is accomplished by applying a logic "1" to the data of U7 and

clocking the FREQ CHG line to a logic "0" with the data ready pulse. The REC TUN CK is not generated until the delay introduced by the shift register U6 is complete. This delay is a minimum of 133 ns and a maximum of 266 ns. A REC TUN CK is only generated when the decoder U4 recognizes the "ØØ" state for BOBUSØØ and BOBUSØ1. When these bits are a Ø1 combination the MO REG CK is generated. The data acknowledge (OACK) is generated when either of these two clocks is issued by clocking the DFF U7. The Q output of this DFF then goes to the DS7830 (U10) double ended driver. The acknowledge is reset to zero by the action of the DATRDY going to a zero thus resetting U7 and the acknowledge line to zero. Acknowledge is also reset by power on reset (IMSN) when ever it is issued.

Data bits BOBUSØ2 through BOBUS15 are inputs for the double ended receivers U17 through U23 and these outputs are the inputs (CDATB02 through CDATB15) for the tuning registers U2, U11, U12 which are clocked by RECTUNCK. The tuning bits TUNBØ2 through TUNB15 to go the receiver control mib via the E pins on the top of the page. TUNBØ2 and TUNBØ3 are spare tuning bits and are not populated at this time but the circuit lines are in the mib for future use if required.

The CDATBØ4 through CDATB15 also go to the mode control registers U13, U14, and U24 and are loaded by MOREGCK. The eight mode bits stored in U13 and U14 are defined in Table 2.6. U24 is a spare 4 bit mode register and can be populated should the requirement arise.

Another function of this mib is to provide the control word for the RF calibration. When the amplitude of the log video pulse is a maximum for the received radar pulse the attenuator in the RF calibrator should be set for a minimum attenuation during the RF calibration portion of the processing cycle. Also when the log video is a minimum the attenuator should be set for a maximum attenuation. A number of examples for various log amp input voltages to the PCU and required attenuator control word input code are given in Table 3.4.

From this table one can see that the algorithm is to invert the log video binary output of the A/D converter and add 1 LSB. If we neglect to add the 1 LSB, thus saving the adder, the error in controlling the calibrator will only increase by 0.234 dB which is considered negligible. Therefore the binary A/D outputs will just be inverted, eliminating the requirement for the 8 bit adder.

In summary the RF calibrator is controlled by holding and inverting in registers U15 and U16 the binary value of the amplitude term (Log Video output) out of the A/D.

3.8 PROCESS CYCLE TIMING MIB (A14 B Side)

The process cycle timing (PCT) mib is mainly responsible, as the mib name indicates, for coordinating the various timing functions throughout the processing cycle for each input log video pulse. The various input

TABLE 3.4 EXAMPLES OF LOG AMP INPUTS VS. CALIBRATOR CONTROL WORD

INPUT POWER	LOG AMP OUTPUT VOLTAGE	A/D OUTPUT CODE	REQUIRED CALIBRATOR ATTENUATION	CALIBRATOR INPUT CODE
		MSB LSB		MSB LSB
dB	VOLTS		dB	
-26.234	1.992	1 1 1 1 1 1 1 1	.234	0 0 0 0 0 0 0 1
-26.468	1.984	1 1 1 1 1 1 1 0	.468	0 0 0 0 0 0 1 0
-33.734	1.742	1 1 0 1 1 1 1 1	7.734	0 0 1 0 0 0 0 1
-41.234	1.492	1 0 1 1 1 1 1 1	15.234	0 1 0 0 0 0 0 1
-56	1.000	1 0 0 0 0 0 0 0	30.	1 0 0 0 0 0 0 0
-56.234	0.992	0 1 1 1 1 1 1 1	30.234	1 0 0 0 0 0 0 1
-63.5	0.750	0 1 1 0 0 0 0 0	37.5	1 0 1 0 0 0 0 0
-73.234	0.492	0 0 1 1 1 1 1 1	45.234	1 1 0 0 0 0 0 1
-78.5	0.250	0 0 1 0 0 0 0 0	52.5	1 1 1 0 0 0 0 0

and output signals can be seen in Figure 3.10, PCT MIB I/O. At the beginning of the process cycle analog signals representing phase, log video amplitude, and fine RF are input to peak detector or sample and holds. One function of the PCT circuitry is to multiplex these parameters into a pulse data register (located on the Data Mux mib - A12B).

The multiplexing operation is handled differently depending on which mode of operation is desired. Figure 3.11 shows the normal mode timing for multiplexing through log video, fine RF, phase A and phase B parameters, respectively. The signal "MUX1" is used to gate the log video parameter through to the Analog to Digital Converter (ADC). After approximately 2 us the digital bits of the converted log video parameter are clocked into a holding register by the signal "ADCLK". At this point the bits are in gray code. On the output of this holding register is a gray to binary converter, which converts the gray code bit pattern to the proper binary pattern in less than 200 ns. Once enough time has been allowed for this gray to binary conversion, the signal "CLKLVN" clocks the binary representation of the log video amplitude into the PULSE DATA REGISTER.

Upon completion of this data transfer, the "MUX2" and "ADCLK" signals are sent out to multiplex through and convert the fine RF data and it is loaded into the proper location in the PULSE DATA REGISTER by CLKFRFN. Following this phase A and phase B data are controlled by "MUX 3" - "ADCLK" - "CLKPHAN" and "MUX 4" - "ADCLK" - "CLKPHBN" signal group respectively just as described for the log video above.

When the fourth parameter, phase B, has been loaded into the PULSE DATA REGISTER, a signal, "CALRCV", is sent to the receiver to begin a phase calibration operation, an operation that occurs for each acceptable incoming log video pulse in the normal mode of operation. After a period of approximately 11 us (to allow for necessary switching, etc. in the receiver), a signal, "CALMS" is generated which indicates to the analog processing circuitry that the calibration parameters are settled out and can be held in the sample and holds. Held values of CAL PHASE A and CAL PHASE B are then multiplexed, A to D converted and loaded into the pulse data register by the signal combinations "MUX 1" - "ADCLK" - "CLKCPHAN" and "MUX 2" - "ADCLK" - "CLKCPHBN" respectively in a manner exactly as described for normal mode log video previously.

Once all the parameters have been loaded into the pulse data register, a signal "CNVCMP" is sent to the DATA MUX circuitry (A12B) to indicate that all the data is loaded and ready to be transferred to the Signal Processor Unit (SPU). Once the transfer is completed, the DATA MUX circuitry will send back a signal "XFRCMP" to indicate the successful transfer of all the data. At this point, analog and digital reset signals will be generated to reset all the circuitry and prepare it for the next incoming set of data parameters if the log video amplitude of the incoming pulse has fallen below threshold. If not, once the log video amplitude does fall below threshold, the resets will then be generated.

One thing that will interrupt the process cycle operation is a reject signal. There may be a reject signal for any of three reasons: (1) frequency reject, (2) qual reject, or (3) pulse width reject. Should

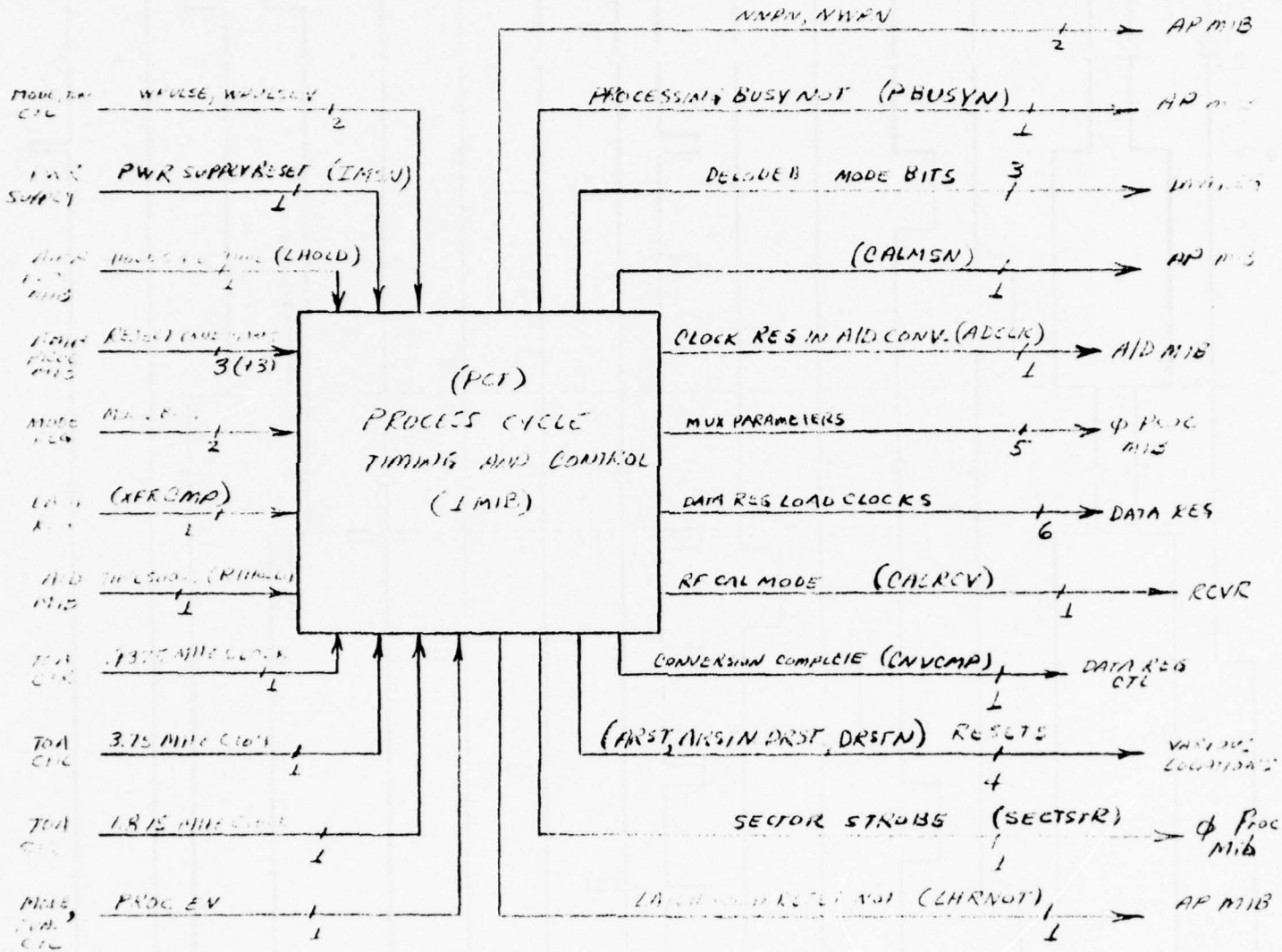
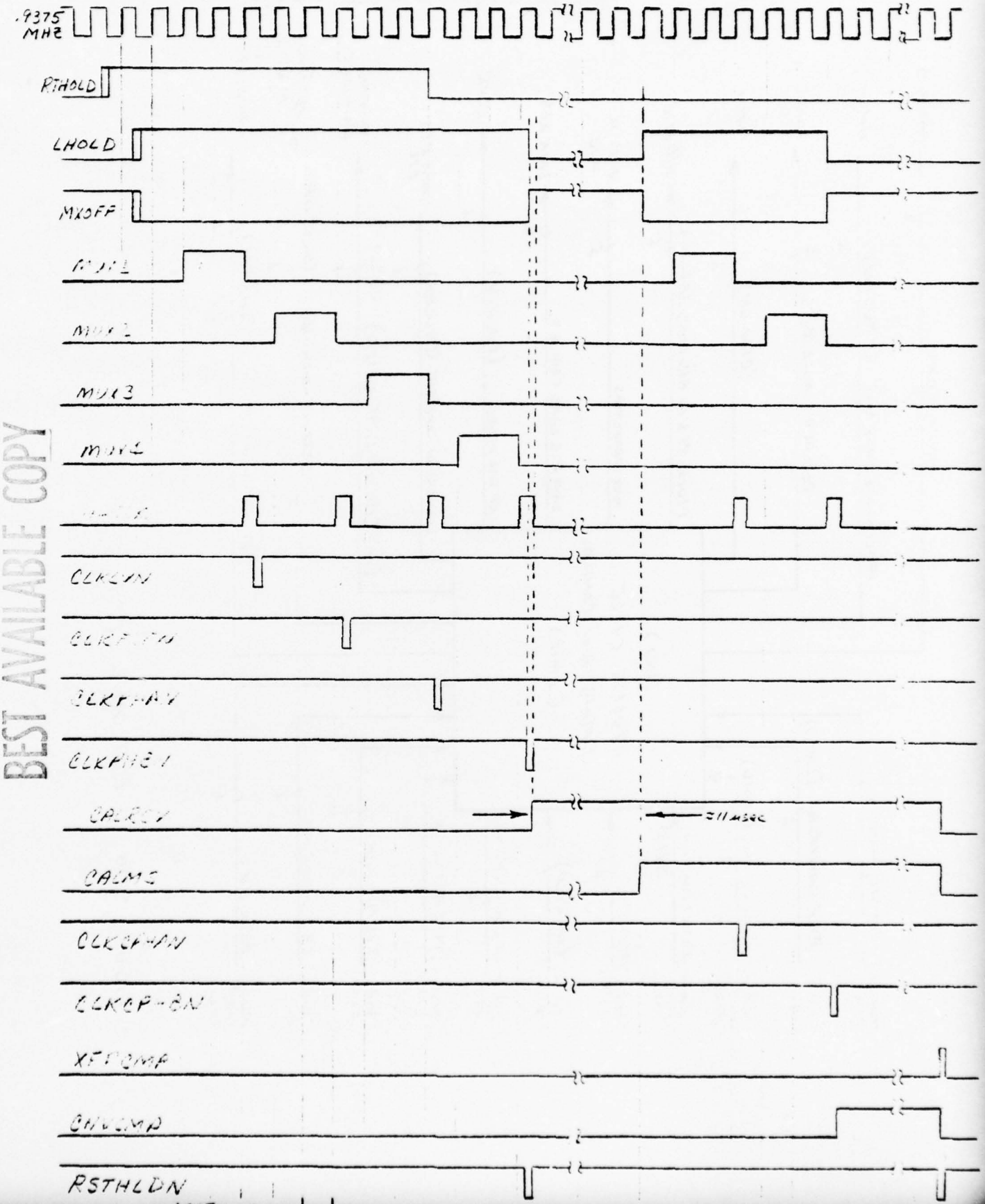


FIGURE 3.10 PCT MIL I/O

FIGURE 3.11 NORMAL MODE CYCLE



any of these rejects occur in normal mode, the pulse processing will be stopped. At this time it will generate the analog and digital resets to end the process cycle (unless the log video pulse is not yet below threshold; in which case the RESET will not occur until the log video does go below threshold).

When in the IF CAL MODE, only phase data is being converted and sent to the SPU (see Figure 3.12 IF CAL MODE Cycle). The four parameters are sin Phase A, cos Phase A, sin Phase B, cos Phase B, respectively; the multiplexing and conversion being done in the same manner as described in the NORMAL mode at operation. After being converted to binary data, the four parameters are loaded into the PULSE DATA REGISTER by "CLKPHAN", "CLKPHBN", "CLKCPHAN", and "CLKCPHBN", respectively.

For RF FREQUENCY CAL MODE, the four parameters being processed are log video, fine RF, Phase A and Phase B (see Figure 3.13 - RF FREQUENCY MODE Cycle). Again these are multiplexed and converted in the same manner as that described in the NORMAL mode of operation. The four parameters are loaded into the PULSE DATA REGISTER by "CLKLVN", "CLKFRFN", "CLKPHAN", and "CLKPHBN", respectively.

Schematic Sheet PCT-Ø1 - This circuitry generates the signals "MUX1" through "MUX4" which multiplex the various parameters into the analog to digital (A to D) converter. These same signals also create timing reference points for generation of the PULSE DATA REGISTER load clocks on schematic sheet PCT-Ø2.

The basic clocks which are used for this circuitry are the .9375 MHz and 1.875 MHz clocks brought over from the TOA counter (A12A mib). The synchronous UP/DOWN counter U16 (54LS191), preset to a count of 1, generates a clock to the 4-bit parallel access shift register U149 (54LS95A) each time its output reaches a count of 2 (QB="1"). This causes the shift register to clock one of the four DFFs, U162 or U163 responsible for generating the "MUX1", "MUX2", "MUX3", or "MUX4" signals mentioned above. When the counter U116 output reaches a count of 4 (QC="1"), a reset for the DFFs is generated, thus making each "MUX" signal two .9375 MHz periods (or 2.133 usec) long. The above sequence is initiated by the signal LHOLD, coming over from the analog processing mib (A11B), going to a logical "1" level. This occurs at the time the hold gate is being initiated for the phase and frequency sample and holds (on the A11A mib).

At the same time the reset of the "MUX1" through "MUX4" signals occur, the signal "SUM4" is generated by U132 (54LS74 Q-Pin 9) which initiates a positive going "ADCLK" pulse on schematic sheet PCT-Ø4.

When LHOLD is a logical Ø, "MXOFF" is a logical 1 (Pin 12 of U128). This grounds the input to the A to D converter (U1-Pin 5 of the A10B MIB) through the analog multiplexer (U26 of the A10A mib) to allow the A to D converter to respond more quickly to the next parameter to be converted.

The one other output from this circuitry is the SECTOR STROBE ("SECTSTR") which is used to clock the phase sector bits into registers (U15 and U16

FIGURE 3.12 IF CAL MODE CYCLE

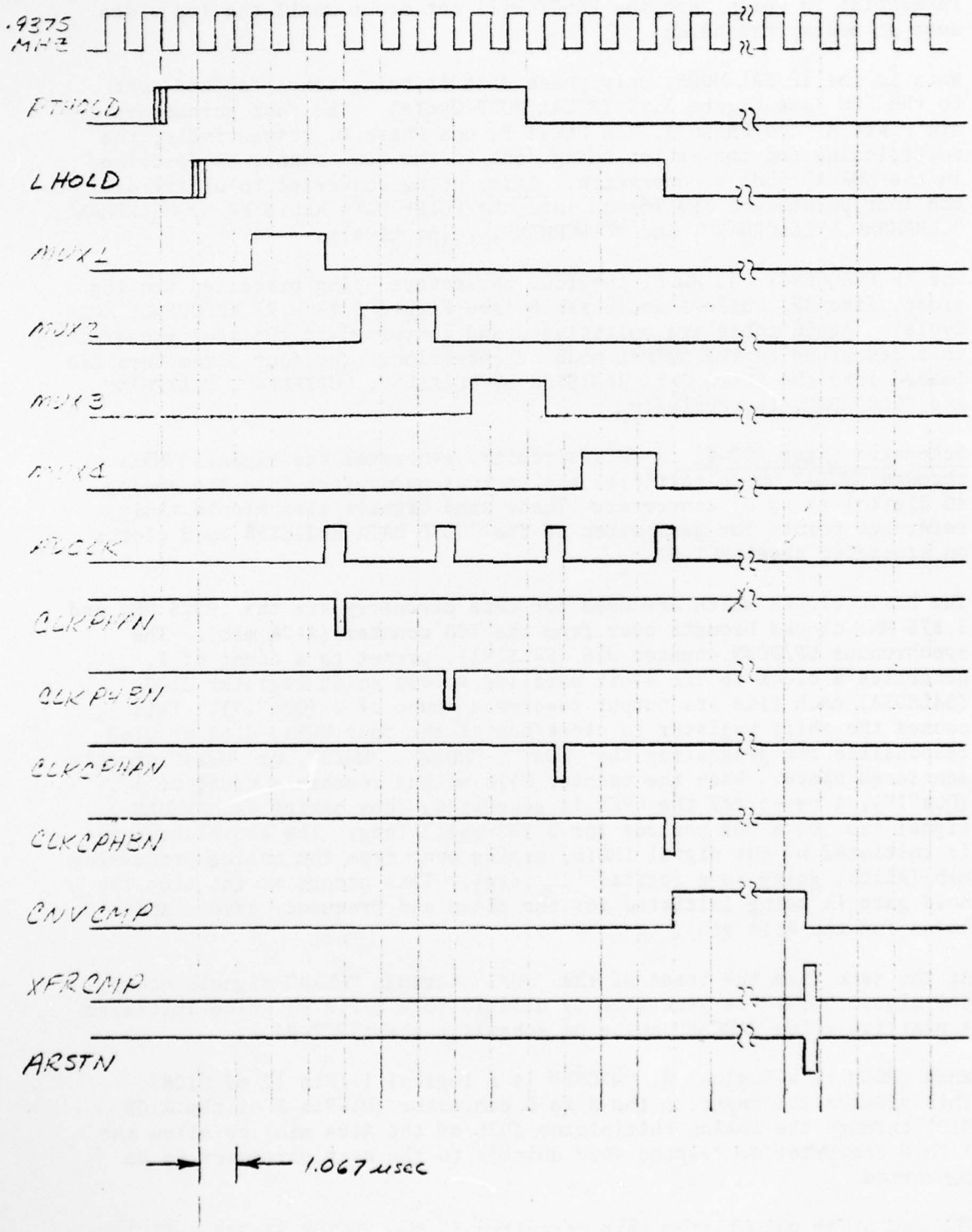
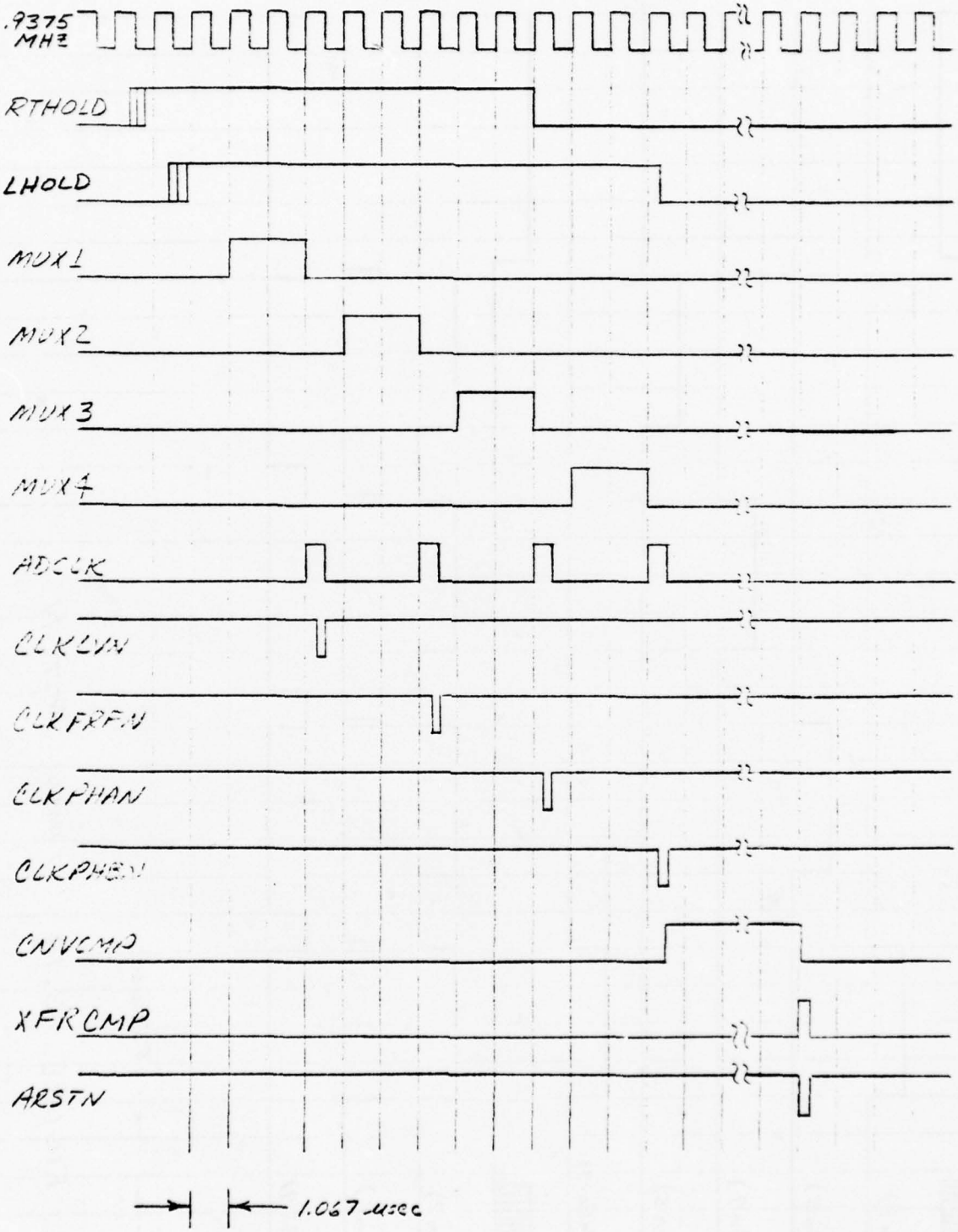


FIGURE 3.13 RF FEED CAL MODE CYCLE



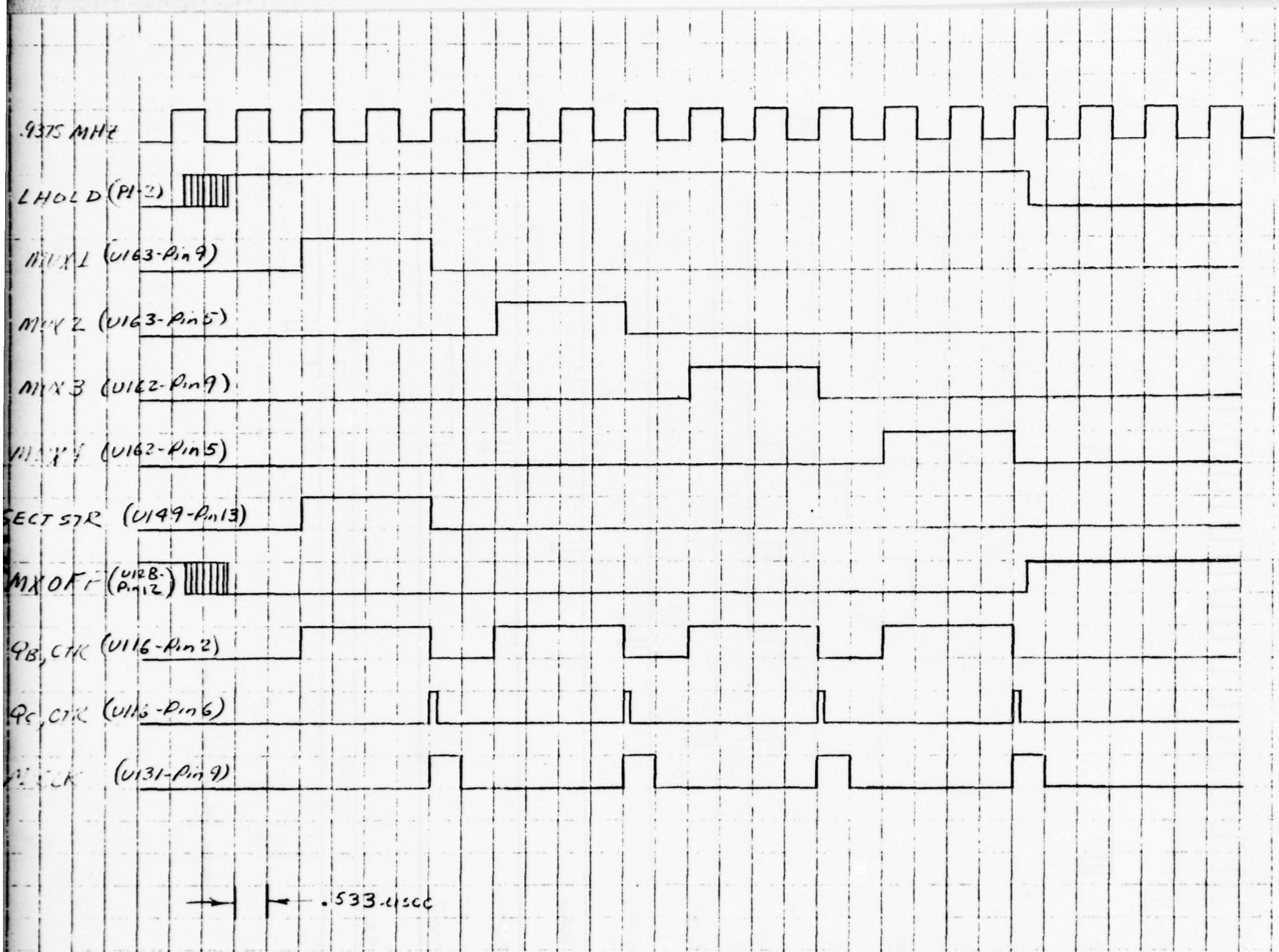


FIGURE 3.17 TIMING PLT Φ1

on A10A mib) on the positive going edge of "MUX1". Then they will be available for clocking into the PULSE DATA REGISTER (D4 and N4 on the A12B mib) later by the signals "CLKPHAN" and "CLKPHBN" (signals which will be described on Schematic Sheet PCT-Ø2).

Schematic Sheet PCT-Ø2 - This circuitry generates the load clocks to the PULSE DATA REGISTER (A12B mib) for each of the three modes of operation, using the "MUX" signals generated on Schematic sheet PCT-Ø1 for basic timing. (See Figure 3.15 - for PCT-Ø2 Timing Diagram - NORMAL MODE).

Each time the positive going edge of an "ADCLK" pulse occurs, the parameter being converted through the A to D converted is loading into a holding register (A10B mib). After a small delay time these bits, which were stored as gray code bits, are output from the GRAY TO BINARY CONVERTER (U26 and U27 of A10B mib). At this time the binary bits, DATB$\overline{\text{ØØ}}$ through DATBØ7, are ready to be loaded into the PULSE DATA REGISTER.

The purpose of the DFFs (U130) on Sheet PCT-Ø2 is to allow a delay of at least one 3.75 MHz clock cycle (267 ns) after "ADCLK" goes high before sending out the appropriate load clock. The remaining circuitry decodes which parameter order is used for the specific mode desired.

The following is the order of parameter multiplexing for the various modes.

	ORDER	PARAMETER	LOAD CLOCK
NORMAL MODE	1	LOG VIDEO	CLKLVN
	2	FINE RF	CLKFRFN
	3	PHASE A	CLKPHAN
	4	PHASE B	CLKPHBN
	5	CAL PHASE A	CLKCPHAN
	6	CAL PHASE B	CLKCPHBN
IF CAL MODE	1	PHASE A	CLKPHAN
	2	PHASE B	CLKPHBN
	3	CAL PHASE A	CLKCPHAN
	4	CAL PHASE B	CLKCPHBN
RF FREQUENCY CAL MODE	1	LOG VIDEO	CLKLVN
	2	FINE RF	CLKFRFN
	3	PHASE A	CLKPHAN
	4	PHASE B	CLKPHBN

The first parameter load clock to be generated is gated on by U147-Pin 8 going high, the second by U147-Pin 6, the third by U147-Pin 12, and the fourth by U129-Pin 12. The mode bit "IFCALM" determines if you are in IF CAL MODE. If not the first four parameters transferred are the same (for NORMAL or RF FREQUENCY CAL MODE). Then, in the case of NORMAL MODE, after the first four parameters are transferred, the signal "CALRCV" goes high and CAL PHASE A and CAL PHASE B parameter load clocks are subsequently gated through.

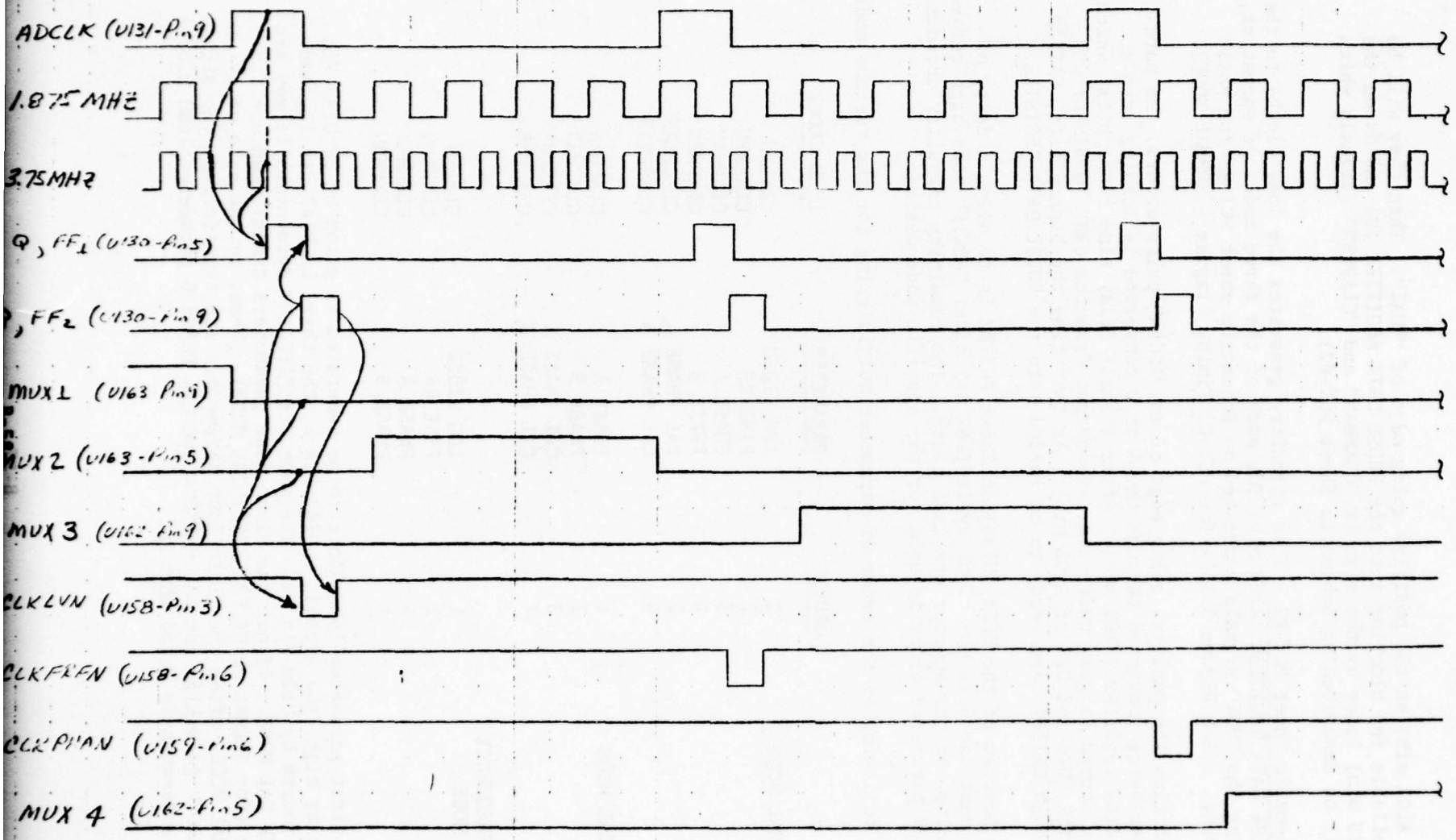


FIGURE 3.15 TIMING PCT #2

TIMING FOR [illegible] GENERATOR

(1 of 3)

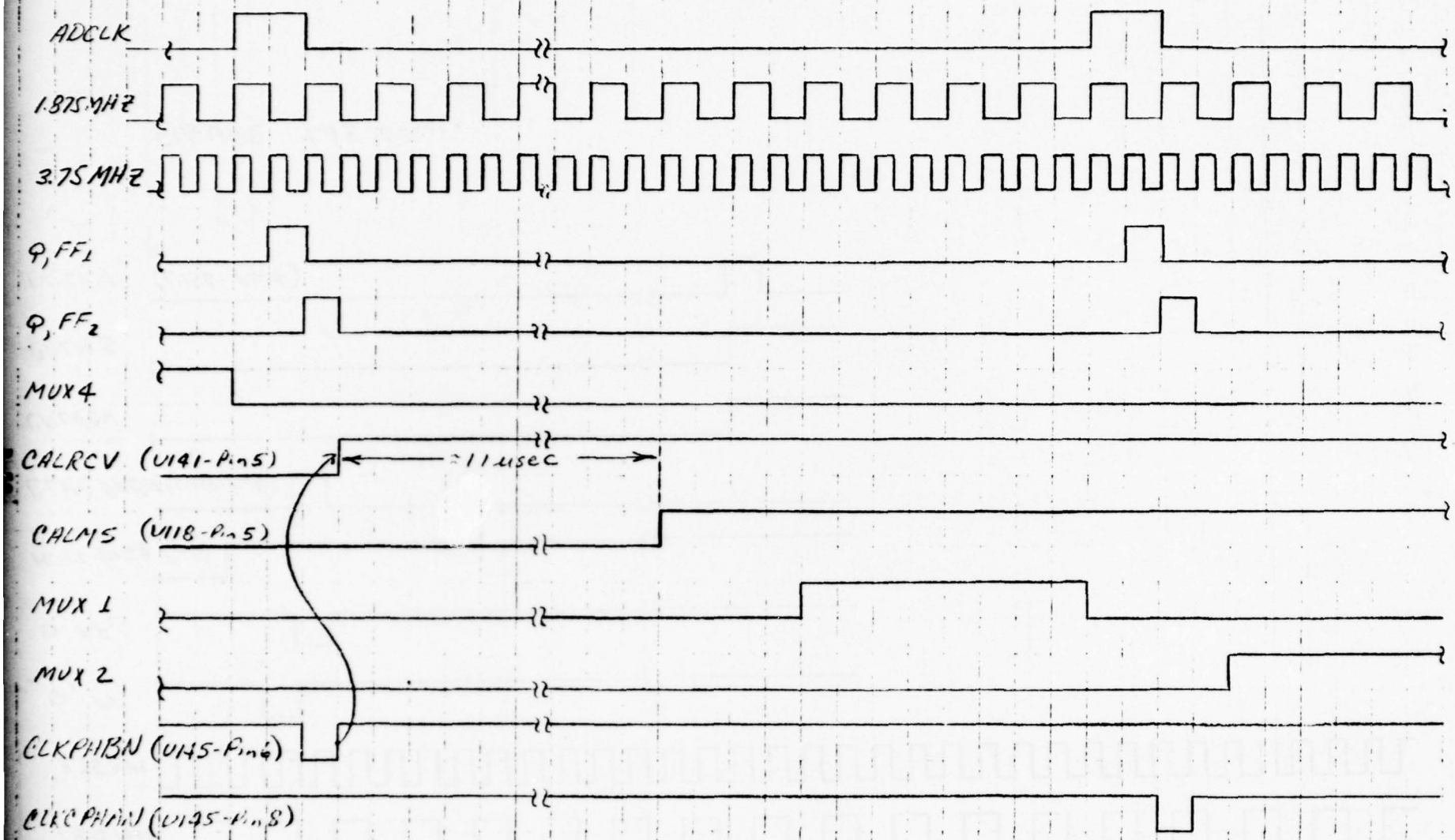


FIGURE 3.15 CONT.

TIMING FOR LOAD STROBE GENERATOR
(2 of 3)

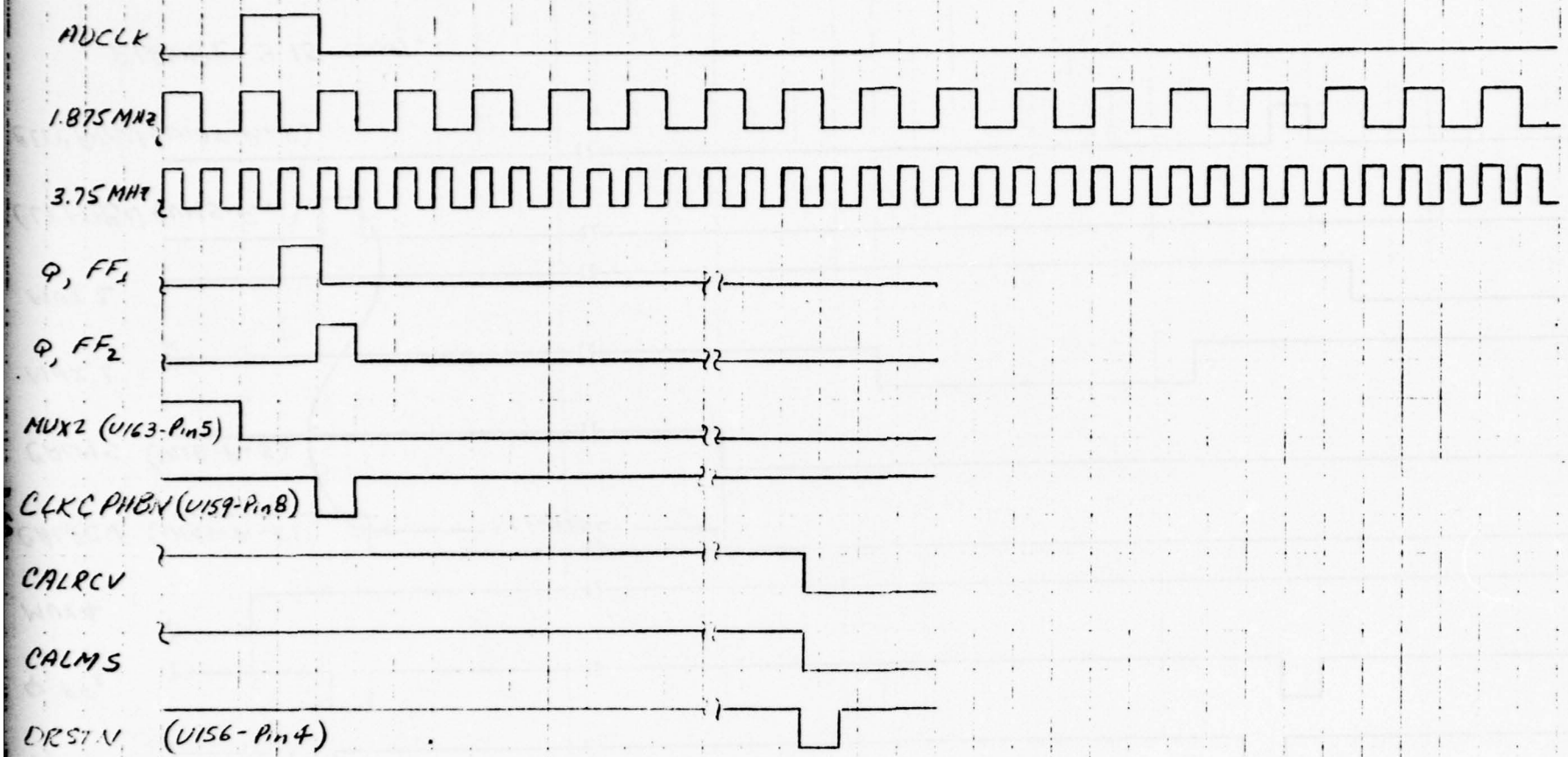


FIGURE 3.15 CONT.

TIMING FOR LOAD STROBE GENERATOR

(3 of 3)

Schematic Sheet PCT-Ø3 - This circuitry generates the signal "CNVCMP" (154-Pin 5) when all the parameters for the given mode have been A to D converted and loaded in the PULSE DATA REGISTER (A12B mib). In NORMAL MODE and IFCAL MODE this occurs when "CLKCPHBN" goes low, while in RF FREQ CAL MODE this occurs when CLKPHBN goes low.

The one other signal generated by this MIB is "PBUSYN" (U155-Pin 6). This signal goes low when LHOLD goes high and remains there until ARSTN goes low at the end of the process cycle, at which time it returns to a high level.

Schematic Sheet PCT-04 - This circuitry generates the signal "ADCLK" (U131-Pin 9) which goes positive and clocks the two DFFs U24 and U25 (54LS175) on the A10B mib each time a parameter has been converted by the A to D converter to a gray code output. Then, on the next positive edge of the 1.875 MHz clock, the "ADCLK" signal drops back to a logical Ø level.

An additional signal generated is "CALRCV", which goes to a high level, only in NORMAL MODE, when the signal CLKPHBN transitions to a logical 1 level, clocking U141-Pin 5 (54LS74) to a logical 1 level. The "CALRCV" signal remains a logical 1 level until the end of the process cycle, at which time it is reset by DRSTN.

Schematic Sheet PCT-Ø5 - This circuitry provides a time out of approximately 11 us between the rising edge of CALRCV and the falling edge of CALMSN (U118-Pin 6). In NORMAL MODE this occurs (after conversion of LOG VIDEO, FINE RF, PHASE A and PHASE B) before going into PHASE CAL for each pulse.

In IF CAL MODE and RF FREQUENCY CAL MODE the circuitry provides this same 11 us delay time before the pulse processing can begin (see Figure 3.16 for NORMAL MODE operation of this circuitry).

Schematic Sheet PCT-Ø6 - This circuitry decodes the two mode bits from the A13A mib into a bit for each of the three modes of operation as follows:

INPUT		OUTPUT		
RFFREQC	IFCAL	FREQCM	NORMAL	IFCALM
Ø	Ø	1	Ø	Ø
Ø	1	Ø	Ø	Ø
1	Ø	Ø	1	Ø
1	1	Ø	Ø	1

The three timing clocks, 3.75 MHz, 1.875 MHz, and 0.9375 MHz, are an input from the A12A mib and buffered, the buffered signals being called "CLK375", "CLK1875", and "CLK9375", respectively.

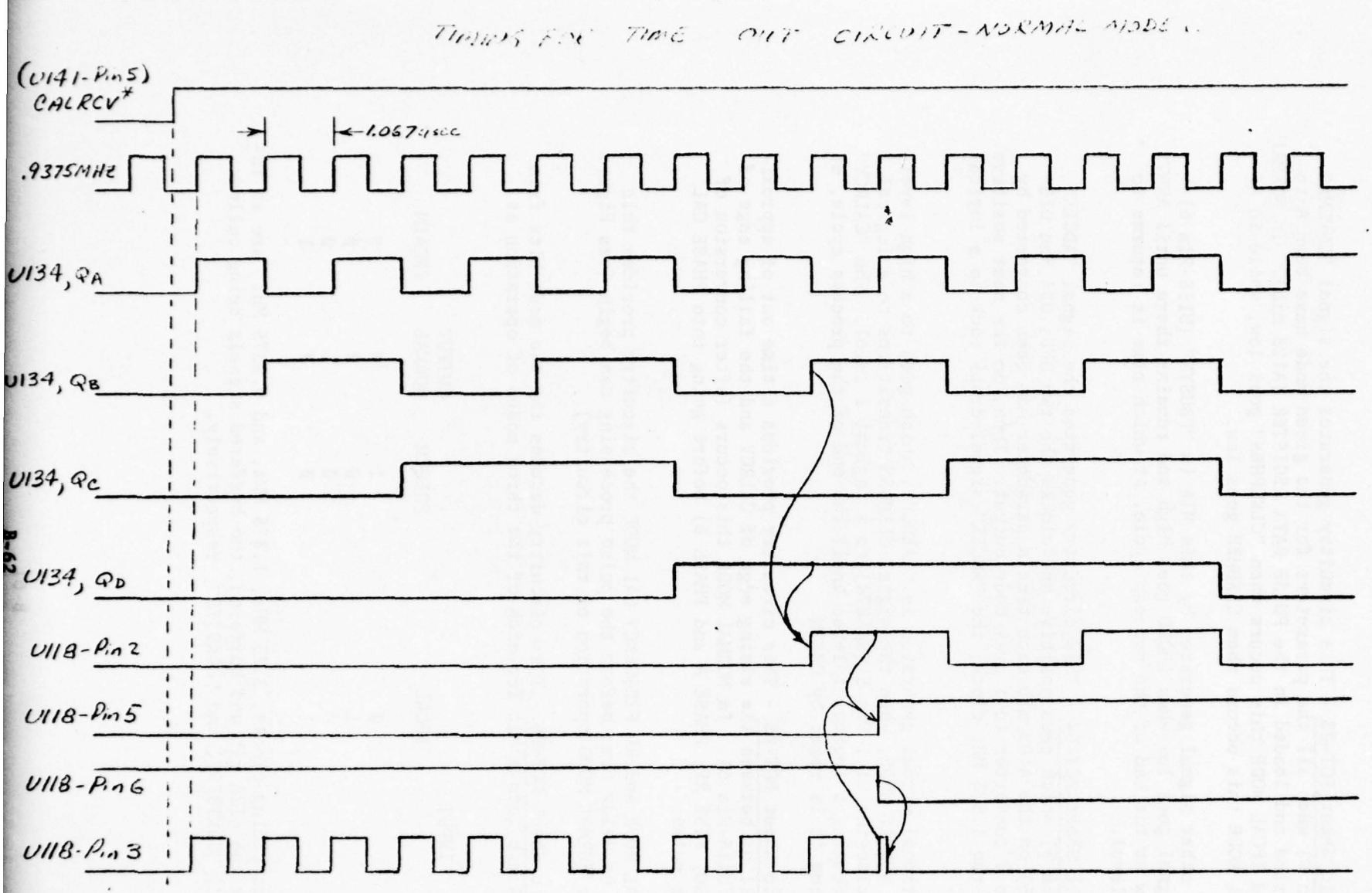


FIGURE 3.16 TIMING PCT #5

Schematic Sheet PCT-Ø7 - This circuitry generates the analog and digital resets for the PCU. The various conditions which cause the resets to be issued are as follows:

1. "XFRCMP" going high (with "RTHOLD" already low) - end of pulse processing - converted data already transferred out of the PCU to the Signal Processor (SPU).

2. "RTHOLD" going low (with "XFRCMP" already high) - data already converted and transferred to the SPU but log video pulse has just gone below threshold.

3. "SUMRJT" going low followed by log video going below threshold - a reject has occurred which immediately stops pulse processing. As soon after this as the log video goes below threshold, the rejects are generated. (For a short log video pulse with "RTHOLD" low before the reject occurs, the resets initiated immediately after "SUMRJT" goes low).

   NOTE: Above occurs only for NORMAL MODE with "CALRCV" a logical Ø.

4. IMSN goes to a logical Ø level - this is the reset command from the POWER SUPPLY.

See Figure 3.17 for timing diagrams for the above conditions.

Schematic Sheet PCT-Ø8 - The circuitry on this sheet generates one signal, "NNPN" (U125-Pin 11), which is a logical Ø when in NORMAL NARROW PULSE MODE; and a signal, "NWPN" (U126-Pin 11), which is a logical Ø when in NORMAL WIDE PULSE MODE. These signals are sent to the Analog Processing mib (A11B).

Another signal generated by the circuitry on PCT-Ø8 is "RSTHLDN" (U91-Pin 12), which is a negative going pulse when "ARSTN" is negative or when "CLKPHBN" is negative during normal mode. The purpose of "RSTHLDN" is to reset the DFF that latches the hold gate signal for the PHASE AND FREQUENCY SAMPLE AND HOLDS.

The remaining circuitry on PCT-Ø8 is the reject circuitry. The signal "SUMRJT", U92-Pin 8, transitions to a logical 1 whenever the pulse being processed is rejected. This can be for one of four reasons. First, the reject could be due to the frequency being outside the frequency window when the window is being used in normal mode (U108-Pin 8 will be a logical Ø). A reject will be generated when a "QUAL" reject signal is sent from the receiver (data input, Pin 12, of U109 being a logical Ø). The remaining two reject conditions are for the pulse width being narrower than a given minimum. In narrow pulse mode a pulse width less than 600 ns will cause a reject ("NPACC", U92-Pin 12, being a logical Ø). For wide pulse mode, a pulse with a pulse width less than 5 usec will be rejected ("WPACC", U92-Pin 13, being a logical Ø).

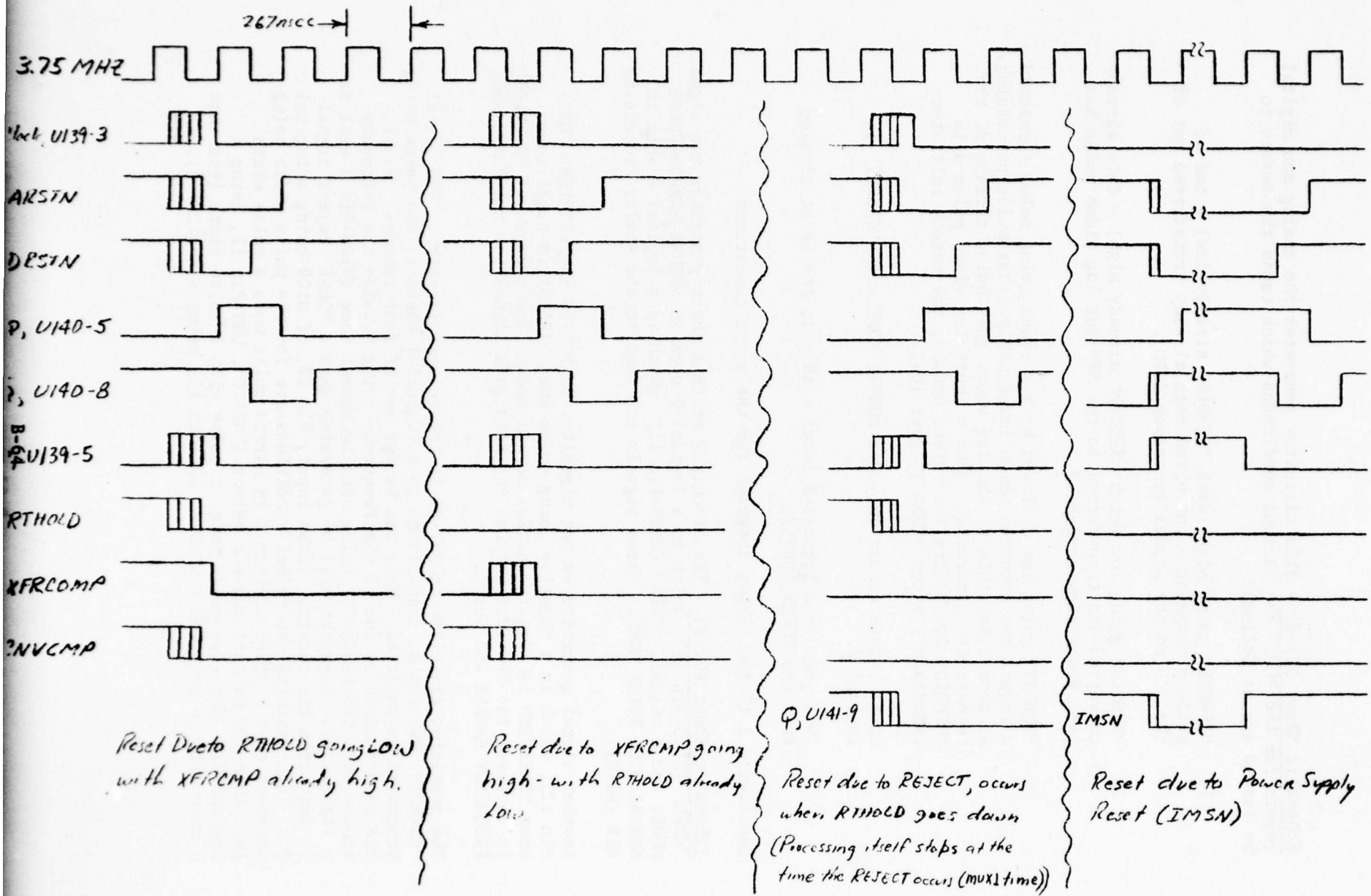


FIGURE 3.17 TIMING PCT Ø7 RESET LOGIC

3.9 OSCILLATOR ASSEMBLY (A6)

The function of the oscillator assembly is to supply the 60 MHz clock for the TOA counter and a 60 MHz test signal for the receiver. Two options for generating the 60 MHz are available. One uses a 60 MHz oscillator, the other a phase locked loop that multiplies a 10 MHz atomic clock input by six.

The 60 MHz oscillator is a temperature compensated crystal oscillator made by Vectron. The oscillator, part number CO-254-4B, has a temperature stability of $\pm 2 \times 10^{-6}$ over the temperature range of -55°C to +85°C. The input voltage is +15VDC and the output level is TTL.

The phase locked loop accepts a 10 MHz 0.5 VPP input signal and multiplies it by 6 to provide the 60 MHz TTL signal.

Either of these options is selected when the PCB for the A6 assembly is populated.

The 60 MHz is buffered by SN54S40 extended drive nand gates to provide the 60 MHz required for the TOA counter. This signal has to be driven about 6" over shielded wire that is terminated in a SN54S04 inverter and a 270 ohm resistor on the TOA Counter/Buffer mib. The 130 ohm pull up resistor on the output of the SN54S40 provides added up level current to drive this load.

The 60 MHz signal also goes to a SN54S20 nand gate which allows the 60 MHz signal to pass to an IF buffer stage in the IF CAL MODE. When the unit is not in the IF CAL MODE the 60 MHz is disabled so that there will not be any interference in the IF section. The following stage provides drive for the 60 MHz CAL signal to drive the coaxial cable to the IF section.

APPENDIX

A.1 Component Stress

Tables A1.1 through A1.9 give the power dissipated by active components and the voltage across capacitors for each MIB in the PCU.

Table A1.1 Phase Processing MIB (A10A) Component Stresses

Resistors

Resistor No.	Power Dissipation Typ (mW)	Max (mW)	Resistor No.	Power Dissipation Typ (mW)	Max (mW)
R1	0.1	0.1	R31	0.1	0.1
R2	0.1	0.1	R32	0.1	0.1
R3	0.1	0.1	R33	0.1	0.1
R4	0.1	0.1	R34	0.1	0.1
R5	0.1	0.1	R35	0.1	0.1
R6	0.1	0.1	R36	0.1	0.1
R7	0.82	1.8	R37	0.1	0.1
R8	0.82	1.8	R38	0.1	0.1
R9	0.82	1.8	R39	0.2	4.0
R10	0.82	1.8	R40	0.2	4.0
R11	0.82	1.8	R41	0.2	4.0
R12	0.82	1.8	R42	0.2	4.0
R13	0.82	1.8	R43	3.3	3.3
R14	0.82	1.8	R44	0.1	0.1
R15	0.82	1.8	R45	0.1	0.1
R16	0.82	1.8	R46	0.1	0.1
R17	0.82	1.8	R47	0.1	0.1
R18	0.82	1.8	R48	0.1	0.1
R19	0.82	1.8	R49	2.5	4.9
R20	0.82	1.8	R50	2.5	4.9
R21	0.82	1.8	R51	2.5	4.9
R22	0.82	1.8	R52	2.5	4.9
R23	2.0	2.0	R53	2.5	4.9
R24	4.0	8.0	R54	2.5	4.9
R25	2.0	2.0	R55	2.5	4.9
R26	4.0	8.0			
R27	2.0	2.0			
R28	4.0	8.0			
R29	2.0	2.0			
R30	4.0	8.0			

Component Stresses (A.10A)

Capacitors

Capacitor No.	Voltage Typ(v)	Voltage Max(v)	Capacitor No.	Voltage Typ(v)	Voltage Max(v)
C1	12.0	12.36	C26	15.0	15.45
C2	5.0	5.15	C27	15.0	15.45
C3	15.0	15.45	C28	15.0	15.45
C4	15.0	15.45	C29	15.0	15.45
C5	15.0	15.45	C30	15.0	15.45
C6	15.0	15.45	C31	15.0	15.45
C7	12.0	12.36	C32	15.0	15.45
C8	5.0	5.15	C33	5.0	5.15
C9	15.0	15.45	C34	5.0	5.15
C10	15.0	15.45	C35	15.0	15.45
C11	15.0	15.45	C36	15.0	15.45
C12	15.0	15.45	C37	5.0	5.15
C13	5.0	5.15	C38	5.0	5.15
C14	15.0	15.45	C39	15.0	15.45
C15	15.0	15.45	C40	15.0	15.45
C16	15.0	15.45	C41	15.0	15.45
C17	15.0	15.45	C42	15.0	15.45
C18	5.0	5.15	C43	15.0	15.45
C19	15.0	15.45	C44	15.0	15.45
C20	15.0	15.45	C45	15.0	15.45
C21	15.0	15.45	C46	15.0	15.45
C22	15.0	15.45	C47	15.0	15.45
C23	5.0	5.15	C48	15.0	15.45
C24	5.0	5.15			
C25	15.0	15.45			

Component Stresses (A10A)

Integrated Circuits

I.C. No.	Power Dissipation Typ (mW)	Max (mW)	I.C. No.	Power Dissipation Typ (mW)	Max (mW)
U1	83.5	143	U16	44.0	75.0
U2	83.5	143	U17	30.5	50.0
U3	83.5	143	U18	6.0	11.2
U4	83.5	143	U19	6.0	11.2
U5	83.5	143	U20	6.0	11.2
U6	83.5	143	U21	12.0	22.5
U7	120	180	U22	8.0	15.0
U8	120	180	U23	20.0	20.0
U9	120	180	U24	20.0	20.0
U10	120	180	U25	20.0	20.0
U11	120	180	U26	20.0	20.0
U12	120	180	U27	6.0	11.2
U13	120	180	U28	6.0	11.2
U14	120	180			
U15	44	75			

Diodes

Diode No.	Power Dissipation Typ (mW)	Max (mW)	Diode No.	Power Dissipation Typ (mW)	Max (mW)
CR1	0.1	0.1	CR13	0.1	0.1
CR2	0.1	0.1	CR14	0.1	0.1
CR3	0.1	0.1	CR15	0.1	0.1
CR4	0.1	0.1			
CR5	0.1	0.1			
CR6	0.1	0.1			
CR7	0.1	0.1	VR1	49.5	81.0
CR8	0.1	0.1	VR2	49.5	81.0
CR9	0.1	0.1			
CR10	0.1	0.1			
CR11	0.1	0.1			
CR12	0.1	0.1			

Table A1.2 A/D Converter (A10B) Component Stresses

Resistors

Resistor No.	Power Dissipation Typ(mW)	Max(mW)	Resistor No.	Power Dissipation Typ(mW)	Max(mW)
R1	1.0	1.0	R33	0.1	3.7
R2	0.1	0.5	R34	0.1	3.7
R3	0.1	0.5	R35	0.1	3.7
R4	0.1	0.5	R35	0.1	3.7
R5	0.1	0.5	R37	0.1	3.7
R6	1.0	1.0	R38	0.1	3.7
R7	0.1	0.5	R39	0.1	3.7
R8	0.1	0.5	R40	0.1	3.7
R9	0.1	0.5	R41	0.1	3.7
R10	0.1	0.5	R42	0.1	3.7
R11	1.0	1.0	R43	0.44	0.44
R12	0.1	0.5	R44	0.44	0.44
R13	0.1	0.5	R45	0.44	0.44
R14	0.1	0.5	R46	0.44	0.44
R15	0.1	0.5	R47	0.44	0.44
R16	1.0	1.0	R48	0.44	0.44
R17	0.1	0.5	R49	0.44	0.44
R18	0.1	0.5	R50	0.1	0.4
R19	1.0	1.0	R51	0.1	0.4
R20	1.0	1.0	R52	0.1	0.4
R21	1.0	1.0	R53	0.1	0.4
R22	0.1	0.1	R54	0.1	0.4
R23	0.1	0.1	R55	0.1	0.4
R24	0.1	0.1	R56	0.1	0.4
R25	0.1	0.1	R57	0.1	0.4
R26	0.1	0.1	R58	0.1	0.4
R27	0.1	0.1	R59	0.1	0.4
R28	0.1	0.1	R60	0.1	0.4
R29	0.1	3.7	R61	0.1	0.4
R30	0.1	3.7	R62	0.1	0.4
R31	0.1	3.7	R63	0.1	0.4
R32	0.1	3.7	R64	24.4	24.4

Component Stresses (A103)

Resistors (cont'd)

Resistor No.	Power Dissipation Typ(mW)	Max(mW)	Resistor No.	Power Dissipation Typ(mW)	Max(mW)
R65	15.6	15.6	R81	10.6	23.1
R66	1.7	1.7	R82	10.6	23.1
R67	19.2	19.2	R83	10.6	23.1
R68	9.6	9.6	R84	0.1	0.1
R69	0.1	0.1	R85	0.1	0.1
R70	0.3	0.3	R86	.72	.72
R71	52.5	52.5	R87	0.1	0.1
R72	0.1	0.1	R88	0.1	0.1
R73	0.1	0.1	R89	0.1	0.1
R74	4.8	11.3	R90	0.1	0.1
R75	1.9	6.4	R91	0.1	0.1
R76	10.6	23.1	R92	0.1	0.1
R77	10.6	23.1	R93	0.1	0.1
R78	10.6	23.1	R94	0.1	0.1
R79	10.6	23.1	R95	0.1	0.1
R80	10.6	23.1			

Component Stresses (A108)

Capacitors

Capacitor No.	Voltage Typ(V)	Voltage Max(V)	Capacitor No.	Voltage Typ(V)	Voltage Max(V)
C1	15.0	15.45	C33	5.0	5.15
C2	15.0	15.45	C34	15.0	15.45
C3	1.33	1.33	C35	1.00	1.00
C4	1.00	1.00	C36	15.0	15.45
C5	5.0	5.15	C37	5.0	5.15
C6	12.0	12.36	C38	15.0	15.45
C7	5.0	5.15	C39	5.0	5.15
C8	5.0	5.15	C40	15.0	15.45
C9	15.0	15.45	C41	12.0	12.36
C10	15.0	15.45	C42	15.0	15.45
C11	5.0	5.15	C43	15.0	15.45
C12	1.33	1.33	C44	5.0	5.15
C13	5.0	5.15	C45	5.0	5.15
C14	15.0	15.45	C46	15.0	15.45
C15	1.00	1.00	C47	15.0	15.45
C16	15.0	15.45	C48	5.0	5.15
C17	5.0	5.15	C49	5.0	5.15
C18	15.0	15.45	C50	15.0	15.45
C19	5.0	5.15	C51	15.0	15.45
C20	15.0	15.45	C52	15.0	15.45
C21	5.0	5.15	C53	15.0	15.45
C22	1.33	1.33	C54	15.0	15.45
C23	5.0	5.15	C55	15.0	15.45
C24	15.0	15.45	C56	15.0	15.45
C25	1.00	1.00	C57	15.0	15.45
C26	15.0	15.45	C58	15.0	15.45
C27	5.0	5.15	C59	15.0	15.45
C28	15.0	15.45	C60	1.33	1.33
C29	5.0	5.15	C61	0.0	1.0
C30	15.0	15.45	C62	1.33	1.33
C31	5.0	5.15	C63	0.0	1.0
C32	1.33	1.33	C64	1.33	1.33

Component Stresses (A ICB)

Capacitors (Cont'd)

Capacitor No.	Voltage Typ(V)	Max(V)	Capacitor No.	Voltage Typ(V)	Max(V)
C65	0.0	1.0	C76	1.33	1.33
C66	1.33	1.33	C77	1.00	1.00
C67	0.0	1.0	C78	1.33	1.33
C68	1.33	1.33	C79	1.0	1.0c
C69	0.0	1.0	C80	1.33	1.33
C70	1.33	1.33	C81	1.00	1.00
C71	0.0	1.0	C82	15.0	15.45
C72	1.33	1.33	C83	15.0	15.45
C73	0.0	1.0			
C74	1.05	1.24			
C75	1.00	1.00			

Component Stresses (A10B)

Integrated Circuits

Flatpack No.	Power Dissipation Typ(mW)	Max(mW)	Flatpack No.	Power Dissipation Typ(mW)	Max(mW)
U1	120	180	U16	83.5	143
U2	120	180	U17	83.5	143
U3	120	180	U18	83.5	143
U4	120	180	U19	83.5	143
U5	120	180	U20	83.5	143
U6	120	180	U21	83.5	143
U7	120	180	U22	83.5	143
U8	120	180	U23	83.5	143
U9	70	110	U24	44	75
U10	70	110	U25	44	75
U11	70	110	U26	30.5	50
U12	70	110	U27	30.5	50
U13	70	110	U28	90	168
U14	70	110	U29	90	168
U15	70	110			

Diodes

Diode No.	Power Dissipation Typ(mW)	Max(mW)	Diode No.	Power Dissipation Typ(mW)	Max(mW)
CR1	0.1	0.1	VR1	91.2	108.9
CR2	0.1	0.1	VR2	91.2	108.9
CR3	0.1	0.1	VR3	49	49
CR4	0.1	0.1			
CR5	0.1	0.1			
CR6	0.1	0.1			
CR7	0.1	0.1			
CR8	0.1	0.1			

Table A1.3 Sample and Hold (A11A) Component Stresses

Resistors

Resistor No.	Power Dissipation Typ(mW)	Max(mW)	Resistor No.	Power Dissipation Typ(mW)	Max(mW)
R1	2.9	2.9	R11	0.82	1.84
R2	2.9	2.9	R12	0.82	1.84
R3	2.9	2.9	R13	0.1	0.1
R4	2.9	2.9	R14	0.1	0.1
R5	2.9	2.9	R15	0.1	0.1
R6	0.1	0.1	R16	0.1	0.1
R7	0.1	0.1	R17	0.1	0.1
R8	0.1	0.1	R18	0.1	0.1
R9	0.1	0.1	R19	0.1	0.1
R10	0.1	0.1	R20	0.1	0.1

Integrated Circuits

Flatpack No.	Power Dissipation Typ(mW)	Max(mW)
U1	660	743.1
U2	660	743.1
U3	660	743.1
U4	660	743.1
U5	660	743.1
U6	120	180

Component Stresses (A11A)

Capacitors

Capacitor No.	Voltage Typ(V)	Voltage Max(V)	Capacitor No.	Voltage Typ(V)	Voltage Max(V)
C1	15.0	15.45	C29	15.0	15.45
C2	15.0	15.45	C30	15.0	15.45
C3	15.0	15.45	C31	1.0	1.00
C4	15.0	15.45	C32	15.0	15.45
C5	15.0	15.45	C33	15.0	15.45
C6	15.0	15.45	C34	15.0	15.45
C7	15.0	15.45	C35	15.0	15.45
C8	15.0	15.45	C36	15.0	15.45
C9	15.0	15.45	C37	15.0	15.45
C10	15.0	15.45	C38	15.0	15.45
C11	15.0	15.45	C39	15.0	15.45
C12	15.0	15.45	C40	15.0	15.45
C13	15.0	15.45	C41	15.0	15.45
C14	15.0	15.45	C42	15.0	15.45
C15	15.0	15.45	C43	15.0	15.45
C16	15.0	15.45	C44	15.0	15.45
C17	15.0	15.45	C45	15.0	15.45
C18	15.0	15.45	C46	15.0	15.45
C19	15.0	15.45	C47	15.0	15.45
C20	15.0	15.45	C48	15.0	15.45
C21	15.0	15.45	C49	2.0	3.0
C22	15.0	15.45	C50	2.0	3.0
C23	15.0	15.45	C51	2.0	3.0
C24	15.0	15.45	C52	2.0	3.0
C25	15.0	15.45	C53	2.0	3.0
C26	15.0	15.45	C54	15.0	15.45
C27	15.0	15.45	C55	15.0	15.45
C28	15.0	15.45	C56	1.00	1.00

Table A1.4 Amplitude Processing (A11B) Component Stresses

Resistors

Resistor No.	Power Dissipation Typ(mW)	Max(mW)	Resistor No.	Power Dissipation Typ(mW)	Max(mW)
R1	1.26	12.65	R36	0.56	0.63
R2	0.4	1.60	R37	3.77	8.89
R3	0.12	0.48	R38	0.10	0.10
R4	15.5	17.00	R39	0.10	0.10
R5	52.0	57.10	R40	32.28	35.43
R6	6.00	7.00	R41	32.28	35.43
R7	6.00	25.59	R42	0.44	0.48
R8	5.10	7.20	R43	0.44	0.48
R9	1.78	7.13	R44	0.10	0.18
R10	1.65	5.22	R45	0.10	0.10
R11	0.41	1.31	R46	0.10	0.10
R12	0.10	0.10	R47	0.10	0.10
R13	0.10	0.10	R48	0.10	0.10
R14	0.10	0.10	R49	0.10	0.10
R15	21.43	22.85	R50	0.10	0.10
R16	1.09	1.17	R51	0.10	0.10
R17	64.3	68.50	R52	0.10	0.10
R18	0.11	0.12	R53	0.10	0.10
R19	0.10	0.10	R54	0.10	0.10
R20	0.10	0.10	R55	28.13	79.69
R21	0.10	0.10	R56	0.10	0.10
R22	31.61	35.10	R57	37.50	44.16
R23	5.00	19.98	R58	1.10	1.78
R24	0.19	0.19	R59	43.25	69.62
R25	0.90	3.61	R60	0.28	0.80
R26	3.26	8.23	R61	28.13	79.69
R27	5.62	11.78	R62	0.10	0.10
R28	36.60	38.64	R63	37.50	44.16
R29	1.27	1.34	R64	1.10	1.78
R30	0.10	0.10	R65	43.25	69.62
R31	0.82	0.92	R66	0.28	0.80
R32	0.18	0.58	R67	60.00	92.93
R33	0.18	0.58	R68	49.00	49.00
R34	12.50	27.38	R69	49.00	49.00
R35	12.50	27.38			

Component Stresses (A II B)

Capacitors

Capacitor No.	Voltage Typ(V)	Voltage Max(V)	Capacitor No.	Voltage Typ(V)	Voltage Max(V)
C1	15.0	15.5	C28	0.25	0.52
C2	15.0	15.5	C29	5.0	5.15
C3	15.0	15.5	C30	12.0	12.4
C4	15.0	15.5	C31	0.20	0.21
C5	15.0	15.5	C32	0.20	0.21
C6	5.0	5.15	C33	5.00	5.15
C7	5.0	5.15	C34	5.00	5.15
C8	5.0	5.15	C35	5.00	5.15
C9	15.0	15.5	C36	5.00	5.15
C10	5.0	5.15	C37	5.00	5.15
C11	15.0	15.5	C38	5.00	5.15
C12	2.0	3.0	C39	5.00	5.15
C13	15.0	15.5	C40	5.00	5.15
C14	15.0	15.5	C41	5.00	5.15
C15	15.0	15.5	C42	5.00	5.15
C16	15.0	15.5	C43	5.00	5.15
C17	15.0	15.5	C44	11.20	11.60
C18	15.0	15.5	C45	15.00	15.50
C19	15.0	15.5	C46	11.20	11.60
C20	15.0	15.5	C47	15.00	15.50
C21	2.00	3.00	C48	15.00	15.50
C22	5.0	5.15	C49	15.00	15.50
C23	15.0	15.5	C50	5.0	5.15
C24	15.0	15.5	C51	5.0	5.15
C25	12.00	12.40	C53	15.0	15.5
C26	5.00	5.15	C54	15.0	15.5
C27	12.00	12.40			

Component Stresses (A11B)

Integrated Circuits

I.C. No.	Power Dissipation Typ(mW)	Max(mW)	I.C. No.	Power Dissipation Typ(mW)	Max(mW)
U1	660.0	743.1	U9	2.5	4.0
U2	135.0	240.0	U10	85.0	150.0
U3	17.0	33.0	U11	148.5	188.4
U4	660.0	743.1	U12	30.7	63.0
U5	150.0	250.0	U13	30.7	63.0
U6	12.0	22.5	U14	20.0	40.0
U7	83.5	143.0	U15	30.7	63.0
U8	83.5	143.0	U16	20.0	40.0

Diodes and Transistors

Transistor No.	Power Dissipation Typ(mW)	Max(mW)	Diode No.	Power Dissipation Typ(mW)	Max(mW)
Q1	14.1	48.2	CR1	2.78	2.78
Q2	0.1	7.1	CR2	2.78	2.78
Q3	0.1	0.4			
Q4	4.90	4.90	VR1	46.5	46.5
Q5	78.8	78.8	VR2	34.0	36.3
Q6	27.9	27.9	VR3	34.0	36.3
Q7	78.8	78.8	VR4	87.3	129.3
Q8	27.9	27.9			

TABLE A1.5 TOA MIB (A12A)

Component Stresses

RESISTORS			CAPACITORS		
Resistor	Power Dissipation		Capacitor	Voltage	
	Typ. (MW)	Max. (MW)		Typ. (V)	Max. (V)
R1	23	43	C1	4.85	5.15
			C2	↓	↓
			C3		
			C4		
			C5		
			C6		

Integrated Circuits

Integrated Circuits	Power Dissipation Typ. (MW)	Max. (MW)	Integrated Circuits	Power Dissipation Typ. (MW)	Max. (MW)
U1	150	270	U16	12	22.5
U2	150	270	U17	90	145
U3	300	500	U18	325	425
U4	300	500	U19	95	160
U5	75	130	U20	95	160
U6	37.5	65	U21	90	145
U7	300	500	U22	90	145
U8	150	270	U23	12	22.5
U9	300	500	U24	95	160
U10	300	500	U25	90	145
U11	12	22.5	U26	95	160
U12	300	500	U27	90	145
U13	300	500	U28	95	160
U14	150	270	U29	90	145
U15	95	160	U30	95	160
			U31	90	145

Table A1.6 Data Mux MIB (A12B)

Component Stresses

Integrated Circuits

Integrated Circuits	Power Dissipation Typ (MW)	Max (MW)	Integrated Circuits	Power Dissipation Typ (MW)	Max (MW)
U2	18	36	U52	90	140
U3	31.5	50	U53		
U4	18	36	U54		
U5	31.5	50	U55		
U6	90	160	U56		
U7	65	110	U57		
U8	20	40	U58		
U9	20	40	U59		
U10	12	22	U61		
U11	20	40	U62		
U12	20	40	U63		
U13	31	50	U64		
U14	31	50	U65		
U15	5	10	U66		
U16	7	14	U67		
U17	110	180	U68		
U19	7	14	U70	110	180
U20	7	14	U71		
U21	5	10	U72		
U25	18	36	U73		
U26	14	27	U81		
U27	17	34	U82		
U28	20	40	U83		
U29	14	27	U84		
U30	18	36			
U34	29	51			

Data Mux MIB (A12B)

Capacitors

Capacitors	Voltage Min. (V)	Max. (v)
C1	4.85	5.15
C2		
C3		
C4		
C5		
C6		
C7		
C8	.2	3.3

Table A1.7 Mode & Tuning Control (A13A)

Component Stresses

Integrated Circuits

Integrated Circuits	Power Dissipation Typ (MW)	Max (MW)	Integrated Circuits	Power Dissipation Typ (MW)	Max (MW)
U1	29	51	U13	65	110
U2	20	40	U14		
U3	29	51	U15		
U4	31	50	U16		
U5	18	33	U17	29	51
U6	20	40	U18		
U7	20	40	U19		
U8	14	27	U20		
U9	12	22	U21		
U10	110	180	U22		
U11	65	110	U23		
U12	65	110	U24	65	110

Capacitors

Capacitors	Voltage Typ (V)	Max (V)	Capacitors	Voltage Typ (V)	Max (V)
C1	.2	3.3	C21	4.85	5.15
C2			C22		
C3			C23		
C4			C24		
C5			C25		
C6			C26		
C7			C27		
C8			C28		
C9			C29		
C10			C30		
C11			C31		
C12			C32		
C13			C33		
C14			C34		
C15			C35		
C16			C36		
C17			C37		
C18	4.85	5.15	C38		
C19	4.85	5.15	C39		
C20	4.85	5.15	C40		

Table A1.8 Process Cycle Timing (A14B) Component Stresses

Integrated Circuits

I.C. No.	Power Dissipation Typ(mW)	Max(mW)	I.C. No.	Power Dissipation Typ(mW)	Max(mW)
U91	12.0	22.5	U138	6.0	11.2
U92	4.0	7.5	U139	20.0	40.0
U108	6.0	11.2	U140	20.0	40.0
U109	20.0	40.0	U141	20.0	40.0
U115	13.5	27.0	U145	5.5	11.0
U116	90.0	160.0	U146	17.0	33.0
U118	150.0	250.0	U147	13.0	25.5
U119	6.0	11.2	U148	50.0	85.0
U121	1.0	2.0	U149	50.0	85.0
U122	17.0	33.0	U150	20.0	40.0
U123	12.0	22.5	U152	12.0	22.5
U125	75.0	130.0	U153	12.0	22.5
U126	8.0	15.0	U154	20.0	40.0
U128	12.0	22.5	U155	20.0	40.0
U129	13.0	25.5	U156	112.5	195.0
U130	20.0	40.0	U157	8.0	15.0
U131	20.0	40.0	U158	8.0	15.0
U132	20.0	40.0	U159	5.5	11.0
U133	17.0	33.0	U160	20.0	40.0
U134	90.0	160.0	U161	20.0	40.0
U135	17.0	33.0	U162	20.0	40.0
U136	17.0	33.0	U163	20.0	40.0
U137	8.0	15.0			

Capacitors

Capacitor No.	Voltage Typ(V)	Max(V)	Capacitor No.	Voltage Typ(V)	Max(V)
C1	5.0	5.15	C4	5.0	5.15
C2	5.0	5.15	C5	5.0	5.15
C3	5.0	5.15	C6	5.0	5.15

Table A1.9 Oscillator - (A6)

Component Stresses

Resistors	Power Dissipation Typ (mW)	Max (mW)	Capacitors	Voltage Typ (V)	Max (V)
R1	4.6	5.2	C1	14.55	15.45
R2	90.0	102.0	C2	14.55	15.45
R3	12.0	20.0	C3	4.85	5.15
R4	.95	1.1	C4	4.85	5.15
R5	4.3	4.96	C5	0.70	5.15
R6	12.0	20.0	C6	0.70	5.15
R7	5.8	8.0	C7	0.10	4.0
R8	19.0	26.0	C8	4.85	5.15
R9	9.4	9.8	C9	4.85	5.15
R10	34.6	39.0	C10	0.10	5.15
R11	34.6	39.0	C11	4.85	5.15
R12	5.0	6.0	C12	2.57	5.15
R13	4.6	5.2	C13	4.85	5.15
R14	16.5	52.2	C14	4.85	5.15
R15	.195	.22	C15	4.85	5.15
R16	4.0	13.0	C16	4.85	5.15
R17	46.0	52.0	C17	2.4	5.15
R18	46.0	52.0	C18	4.85	5.15
R19	1.0	3.4	C19	4.85	5.15
R20	1.0	3.4	C20	3.0	5.15
R21	1.0	3.7	C21	.1	5.15
R22	14.7	40.0	C22	.1	5.15
R23	1.0	3.7			
R24	14.7	40.0			

Oscillator - A6

Integrated Circuits	Power Dissipation Typ(mW)	Max(mW)	Transistor	Power Dissipation Typ(mW)	Max(mW)
U1	62.5	110	Q1	86	200
U2	200.0	220			
U3	200.0	260			
U4	9.0	16.5			
U5	150.0	250			
U6	150.0	250			
U7	112.5	195			
U8	36.5	65			
U9	194	206			
U10	8.5	14			
U11	175	240			

Appendix C

SCHANS OPERATIONAL SOFTWARE

COMPUTER PROGRAM DEVELOPMENT SPECIFICATION

Prepared by

G. A. Kooch

This specification is the end product of study Task 5 and is attached to the Final Report in accordance with instructions contained in the contract Statement of Work.

IBM FORM NO. 952-5260-5

REVISIONS

CHK	ENGRG NOTICE	LTR	DESCRIPTION	DATE	APPROVED
		-	RELEASE	8/13/76	

4	5	6	7	8
REV				
SH	1	2	3	

REV STATUS OF SHEETS

CONTR NO.

PREPARATION

DSGN CHK

DWG CHK

DSGN APPROVAL

OTHER APPROVAL (SPECIFY ACTIVITY)

IBM

FEDERAL SYSTEMS DIVISION

☐ GAITHERSBURG, MD ☒ OWEGO, N Y

☐ HUNTSVILLE, AL ☐ MANASSAS, VA

TITLE

Computer Program Development Specification for SCHANS Operational Program

SIZE	CODE IDENT NO.	DWG NO.
A		76-L02-011

SCALE	WT	SHEET

460H

LIST OF EFFECTIVE PAGES

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76-L02-011

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ORIGINAL						

CONFIGURATION CHART

SPECIFICATION ISSUE	ECP/PTR	PROGRAM LEVEL
76-L02-011		Release

1.0 SCOPE.

1.1 Identification. This Computer Program Development Specification (CPDS) defines the requirements for the Self-Contained High Altitude Navigation System (SCHANS) Operational Program.

1.2 Functional Summary. The SCHANS Operational Program shall be divided into two subprograms: (1) the RF Signal Processing and Executive Program and (2) the Navigation and Attitude Determination Program (NADP). The RF Signal Processing and Executive Program shall perform the following functions:

a. Antenna selection through RF switch control

b. Receiver frequency tuning in accordance with the SCHANS Operational Program landmark selection

c. Receiver calibration control and data processing

d. Reduction of landmark emitter parameter measurements to determine baseline phase angles, frequency, amplitude, and pulse times of arrival

e. Provision of landmark emitter parameter measurements to the NADP

f. Executive control of the SCHANS Operational Program including external equipment interfacing.

The NADP shall perform the following functions:

a. Processing of landmark emitter parameter measurements supplied by the RF Signal Processing and Executive Program.

b. Provision of estimates of current spacecraft position, velocity, and attitude based on past measurements.

2.0 APPLICABLE DOCUMENTS. The following documents, of exact issue shown, form a part of this specification to the extent specified herein:

(TBD)

3.0 REQUIREMENTS.

3.1 Program Definition.

3.1.1 System Description.

3.1.1.1 General. The SCHANS measures range and angles to E/F band radar landmarks of known position, and, using these measurements, performs precise self-contained navigation of high altitude spacecraft.

A block diagram of the SCHANS appears in Figure 3-1. The SCHANS consists of:

a. An Antenna/RF Calibrator Unit which includes five 2.1 inch diameter planar spiral antennas (Figure 3-2) mounted on the earth pointing face of the spacecraft and circuitry permitting RF phase measurement calibration of the system (Figure 3-3).

b. An Interferometric Landmark Tracker/Pulse Conversion Unit (ILT/PCU) (Figures 3-4 and 3-5) containing circuitry for superheterodyne receiving, receiver control, analog signal processing, A/D conversion interfacing with the SPU and a power supply.

c. A Signal Processor Unit (SPU) for digital signal processing and navigation computations.

3.1.1.2 Functional Description.

3.1.1.2.1 Antennas. The five antenna array is mounted on an Earth viewing surface of the spacecraft and provides two interferometer baselines required for determination of line of sight to the emitter. The antennas receive radiation from radar landmarks and couple it to the ILT/PCU Unit through the RF calibrator circuitry using semirigid coaxial cables. Three antennas are provided on each baseline to permit resolution of phase measurement ambiguities.

3.1.1.2.2 Receiving Circuitry.

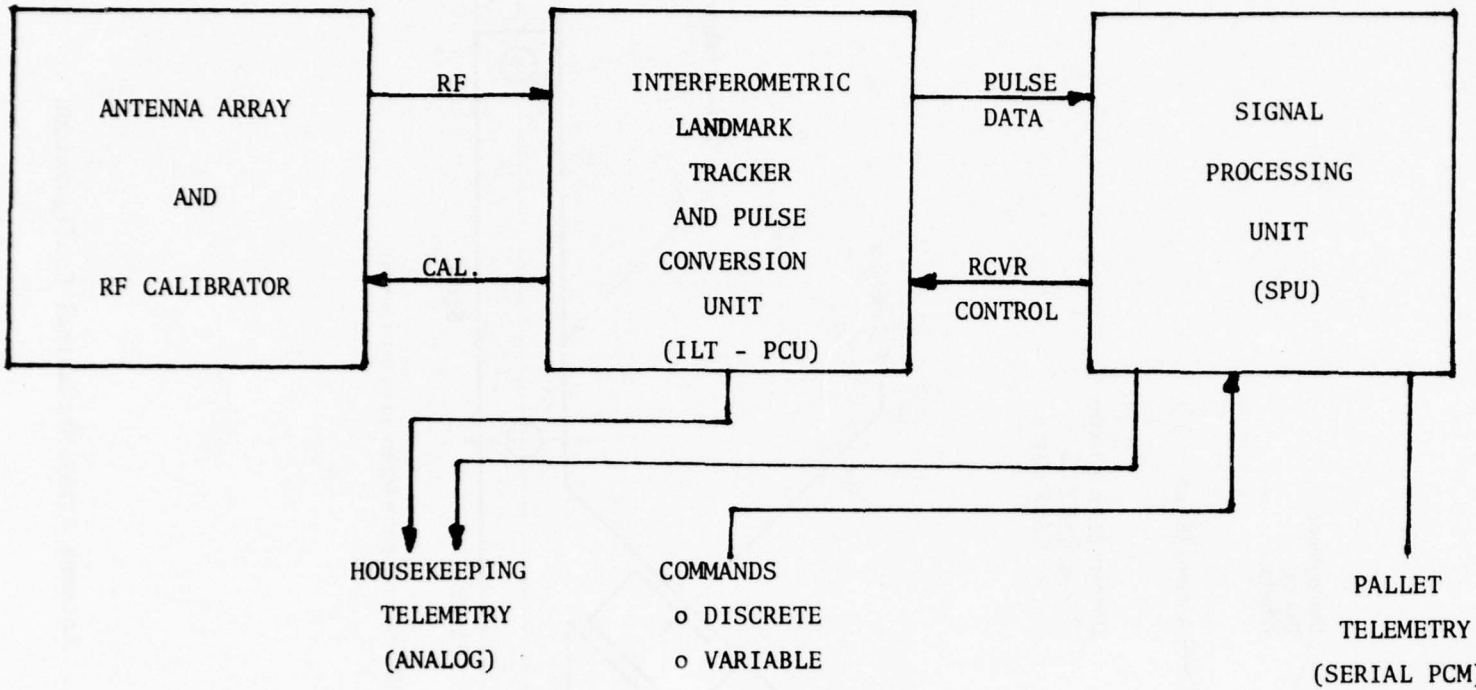
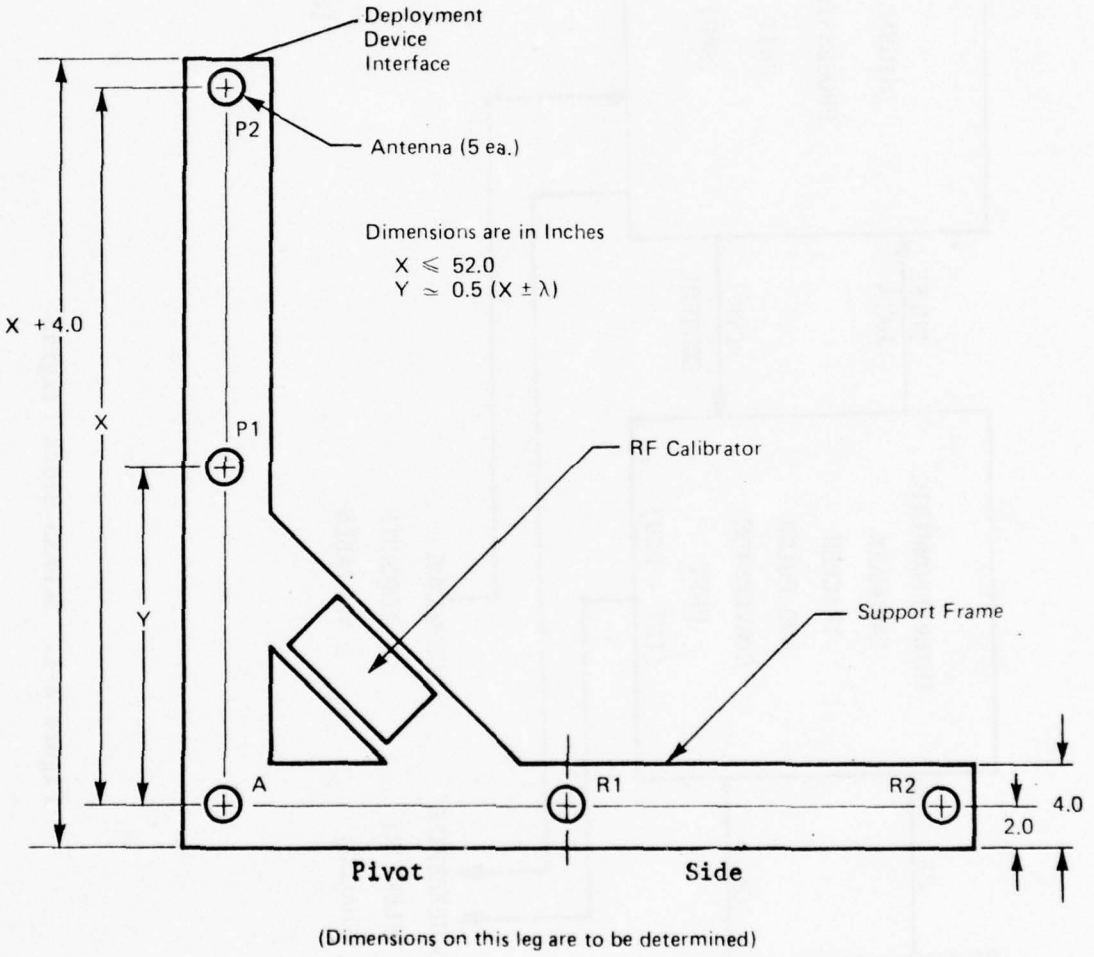


Figure 3-1. SCHANS Block Diagram



(Dimensions on this leg are to be determined)

Figure 3-2. Antenna Array Mechanical Configuration

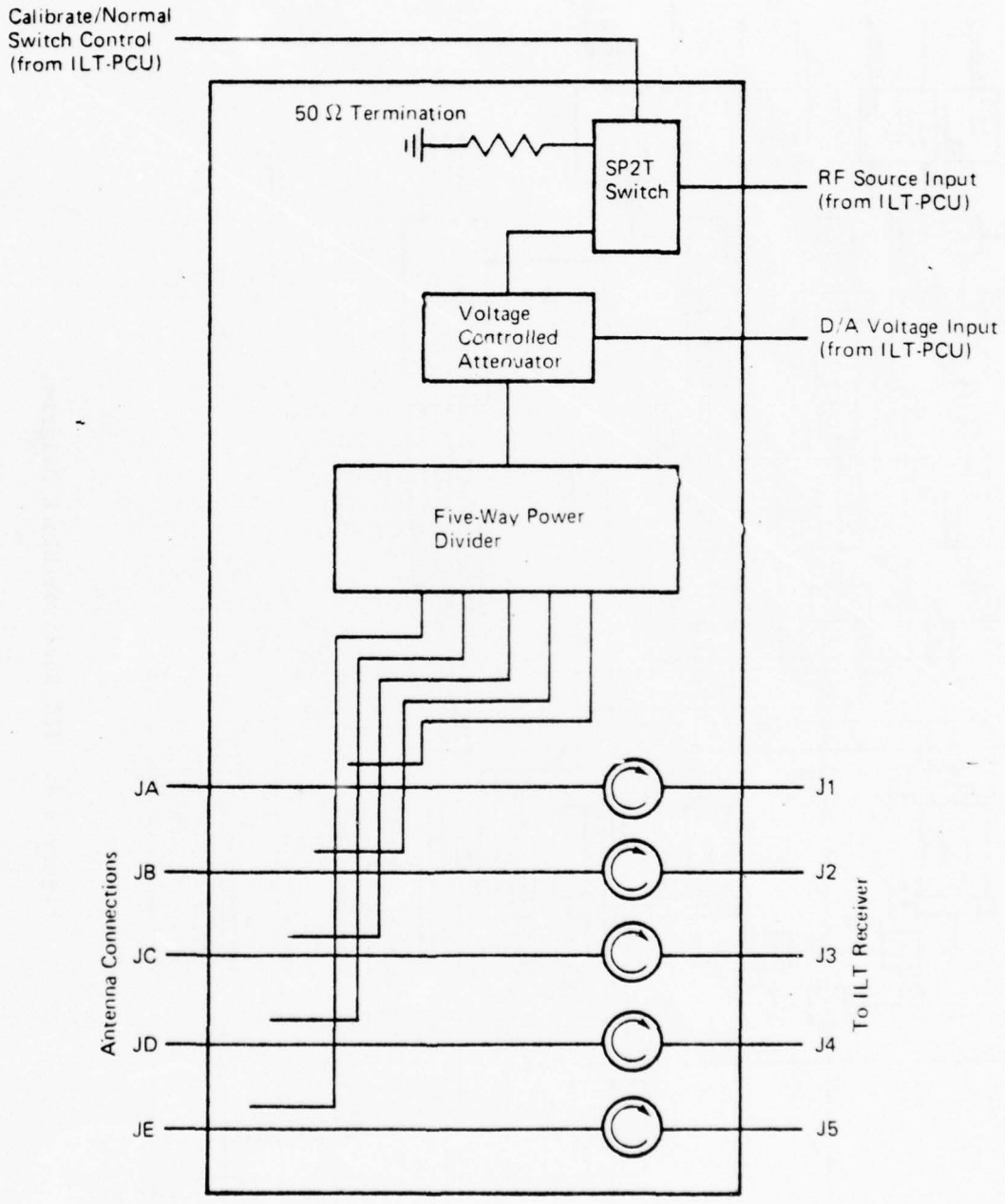


Figure 3-3. RF Calibrator Block Diagram

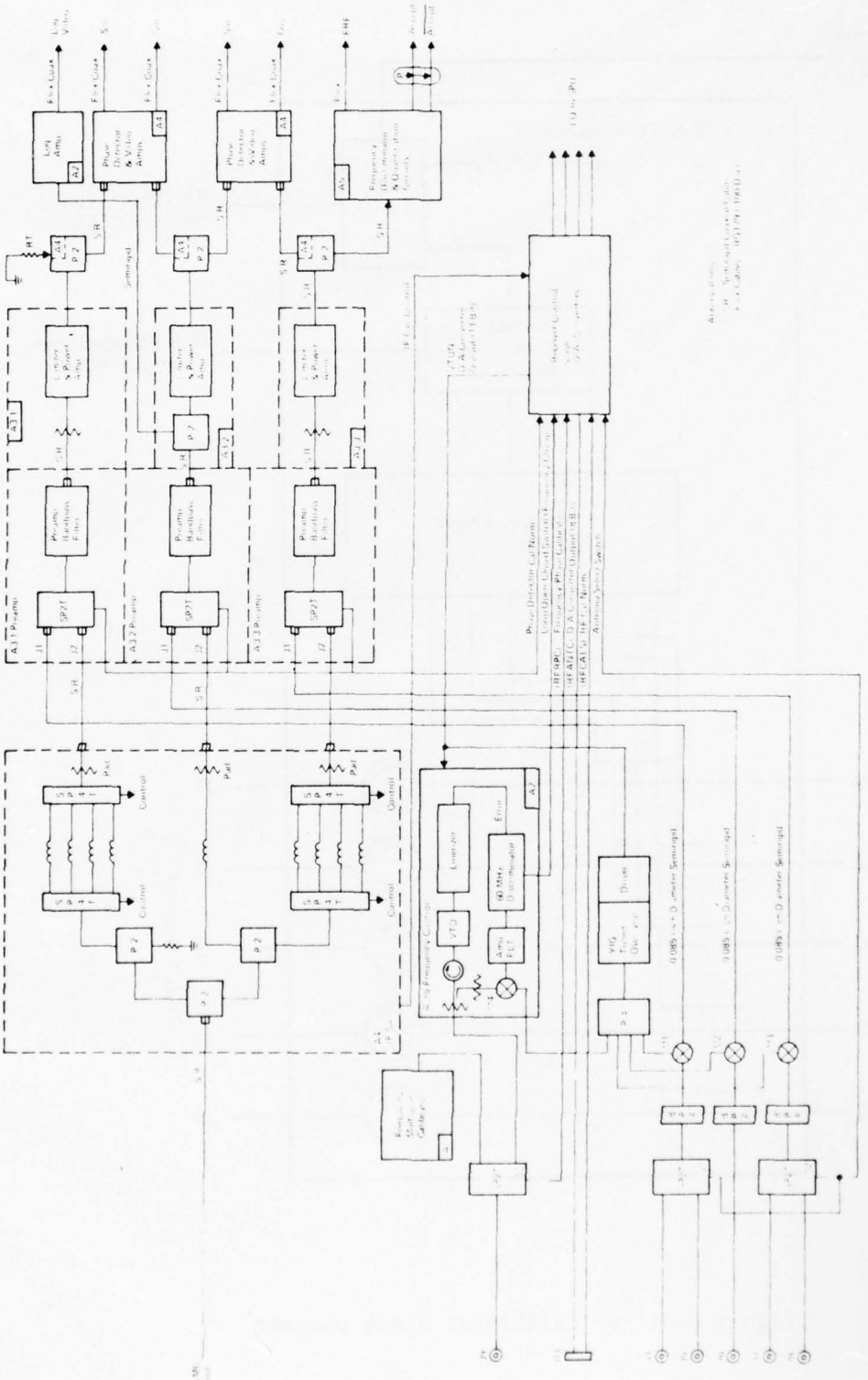


Figure 3-4. ILT Receiver Block Diagram

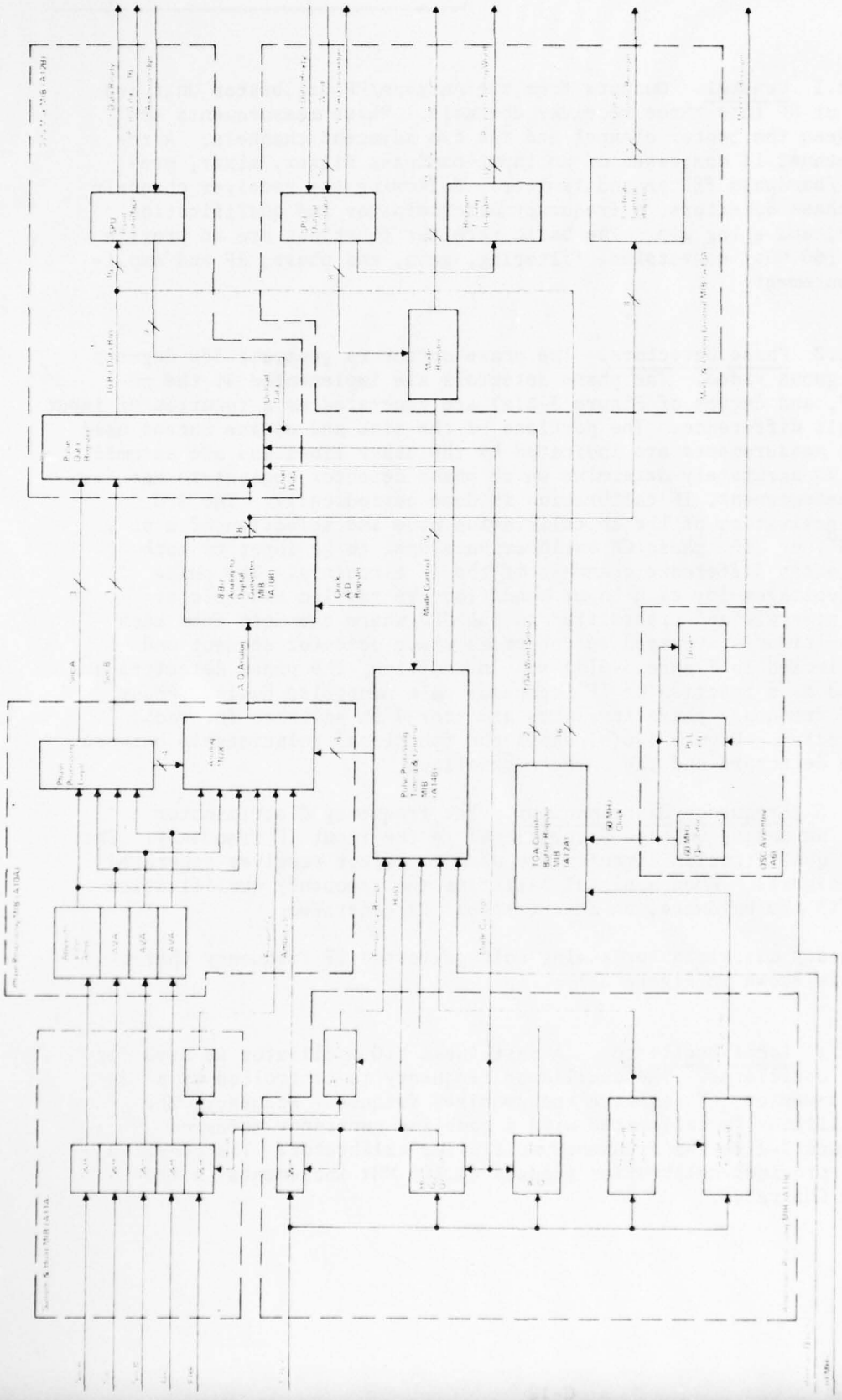


Figure 3-5. PCU Block Diagram

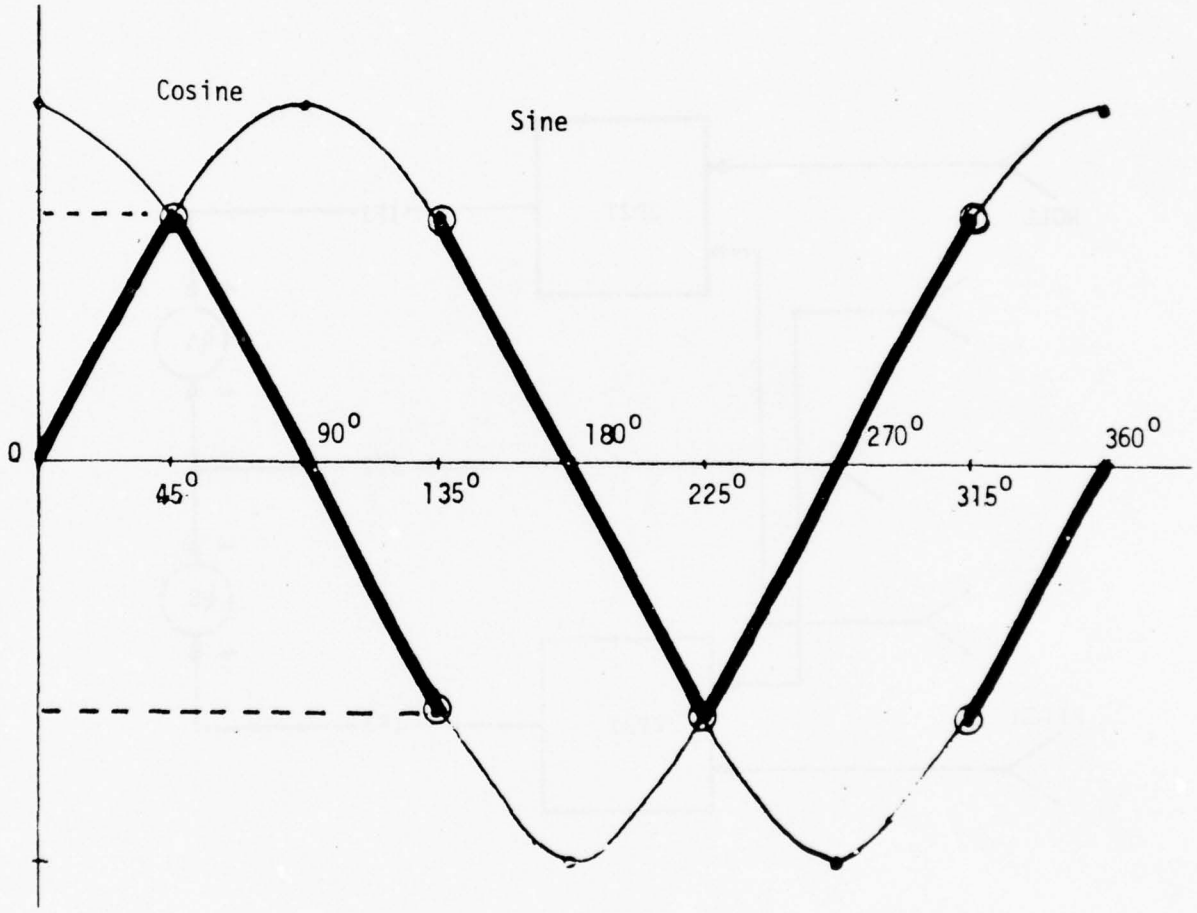
3.1.1.2.2.1 General. Outputs from the Antenna/RF Calibrator Unit are switched at RF into three receiver channels. Phase measurements are made between the center channel and the two adjacent channels. A receiver channel is comprised of an input bandpass filter, mixer, preamplifier/bandpass filter and limiter. Following the receiver channels are two phase detectors, a frequency discriminator and qualification circuitry, and a log amp. The basic receiver functions are to provide RF to IF (60 MHz) conversion, filtering, gain, and phase, RF and amplitude measurement.

3.1.1.2.2.2 Phase Detectors. The phase detectors generate 360 degrees of unambiguous video. The phase detectors are implemented at the receiver IF, and curves of Figure 3-6(a) are generated as a function of input phase angle difference. The portions of the sine and cosine curves used for phase measurements are indicated by the heavy lines and are assumed linear. To accurately determine which phase detector segment to use for a phase measurement, IF calibration is done periodically. The SPU controls activation of the IF calibration mode and selection of a 45^{o}, 135^{o}, 225^{o}, or 315^{o} phase CW calibration signal to be input to both pairs of phase difference channels of the IF circuitry. The phase detector voltages for each input condition are sampled and held at 25 usec intervals and transmitted to the SPU where the data from each input condition is averaged to determine phase detector segment end points (circled in Figure 3-6(a)). In addition, the phase detectors are calibrated as a function of IF frequency on a monopulse basis. Phase versus IF frequency characteristics are stored in software for each phase detector. Figure 3-6(b) shows the functional relationship between the phase detectors and the antenna baselines.

3.1.1.2.2.3 Frequency Discriminator. The frequency discriminator generates an analog voltage proportional to the input IF frequency. The frequency qualification circuits are used to reject receiver generated spurious signals. When a signal satisfies the frequency qualification criteria in the hardware, an accept signal is generated.

The frequency discriminator analog voltage versus IF frequency characteristic is shown in Figure 3-7.

3.1.1.2.2.4 Local Oscillator. A fast tuned YIG oscillator is used for the local oscillator. The oscillator frequency is controlled by a 12-bit D/A converter. To achieve the required frequency accuracy, the local oscillator is calibrated with a combline generator referred to in Figure 3-4 as the frequency multiplier calibrator. The combline generator provides calibration signals at 100 MHz increments in the 2.5 - 2.9 GHz range.



Circles indicate Calibration Points.

Figure 3-6(a). Phase Detector Response

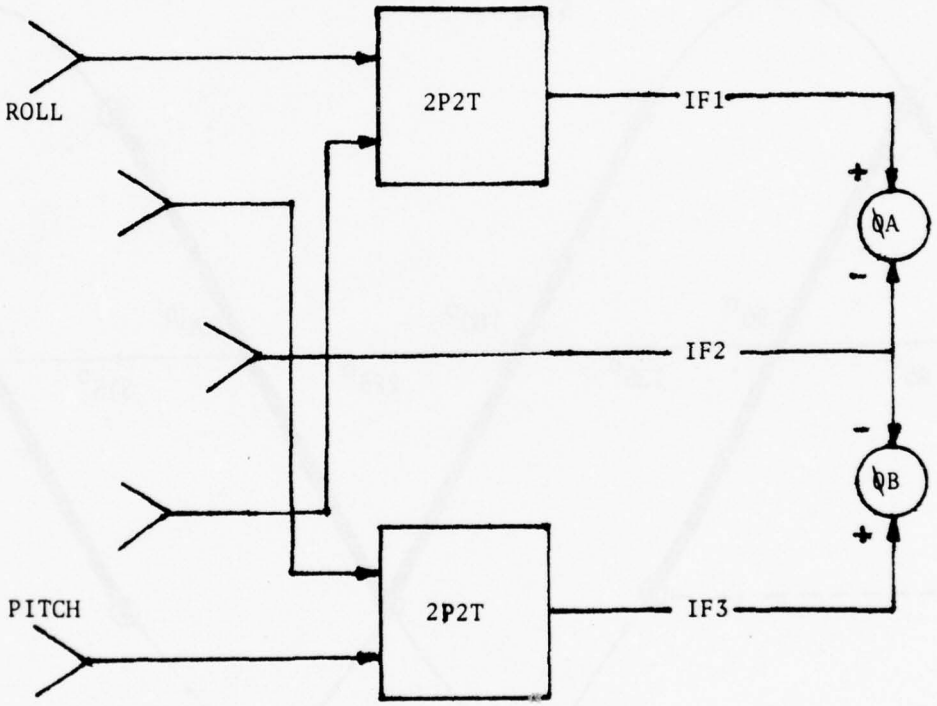


Figure 3-6(b). Antenna Baseline/Phase Detector Functional Relationship

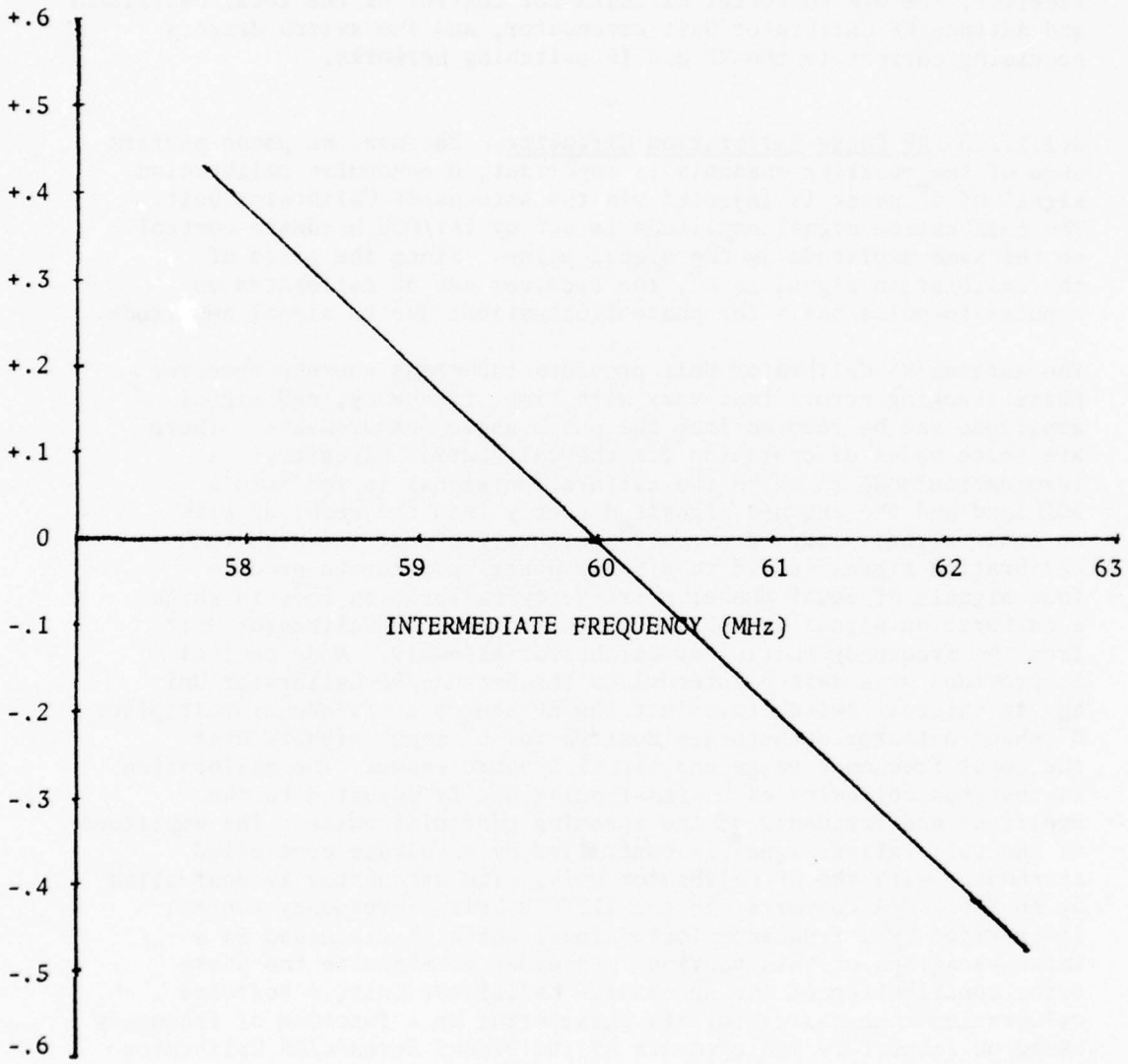


Figure 3-7. Frequency Discriminator
Detected Video Versus Frequency

3.1.1.2.2.5 Control Logic. The control logic assembly provides the interface between the analog signal processing circuitry and receiver, the D/A converter circuits for control of the local oscillator and Antenna/RF Calibrator Unit attenuator, and the switch drivers providing current to the RF and IF switching networks.

3.1.1.2.3 RF Phase Calibration Circuitry. Because the phase performance of the receiver channels is important, a monopulse calibration signal of 0^{o} phase is injected via the Antenna/RF Calibrator Unit. The calibration signal amplitude is set by ILT/PCU hardware control to the same amplitude as the signal pulse. Since the phase of the calibration signal is 0^{o}, the receiver can be calibrated on a pulse-to-pulse basis for phase fluctuations due to signal amplitude.

The Antenna/RF Calibrator Unit provides the means whereby receiver phase tracking errors that vary with time, frequency, and signal amplitude can be removed from the phase angle measurements. There are three modes of operation for the calibration circuitry: a termination mode in which the calibration signal is fed into a 50Ω load and the antenna signals directly into the receiver with no other signals coupled in; a 0^{o} calibration mode in which the calibration signal is fed to a 5-way power splitter to produce four signals of equal phase; a frequency calibration mode in which a calibration signal is applied to the Antenna/RF Calibrator Unit from the frequency multiplier calibrator assembly. Mode control is provided by a switch internal to the Antenna/RF Calibrator Unit and an external switch to select the RF source or frequency multiplier. 0^{o} phase detector outputs are desired for 0^{o} input signals over the input frequency range and signal dynamic range. The calibration is inserted following each signal pulse and is adjusted to the amplitude and frequency of the incoming preceding pulse. The amplitude of the calibration signal is controlled by a voltage controlled attenuator with the RF Calibrator Unit. The attenuator is controlled by an 8-bit D/A converter in the ILT/PCU Unit. Frequency control is provided by a frequency locked loop, which is discussed in a later paragraph of this section. In order to minimize the phase error contribution of the Antenna/RF Calibrator Unit, a software calibration compensates for its phase error as a function of frequency based on laboratory measurements of individual Antenna/RF Calibrator Units.

The auto frequency control loop is a frequency locked loop whose function is to lock the voltage tuned oscillator exactly 60 MHz above the local oscillator frequency. This oscillator is tuned in conjunction with the LO and is used to provide the RF signal for the RF calibration circuitry.

3.1.1.2.4 Analog Signal Processing and Parameter Measurement Circuitry. The ILT/PCU analog signal processing circuitry interfaces with the receiver circuitry and processes the receiver video signals to determine baseline phase angles, frequency, amplitude and pulse times of arrival. The receiver sends the analog signal processing circuitry one log video signal (LV), one fine frequency signal (FRF), one accept pulse (QUAL), and four phase signals (COS A, SIN A, COS B, SIN B). Signal processing starts upon receipt of a LV pulse that has a sufficient signal-to-noise ratio. The LV pulse initiates timing for strobing the QUAL line, holding the FRF and phase measurements. The LV pulse is peak detected for amplitude measurement. Because there is only one A/D converter, analog parameters are serially mutliplexed. While one parameter is being A/D converted, processing continues in parallel on other parameters, i.e., check of reject conditions (QUAL, minimum pulsewidth or FRF out of processing range), calculation of the absolute value of phase measurements, phase measurement octant determinations, and selection of phase measurements to be converted. The converted data is held in a digital register until transfer to the SPU. Upon receipt of a receiver LV pulse, the ILT/PCU starts a 16.5 μsec cycle to digitize and hold the pulse data. Then, the RF phase calibration signal is activated, and, after 10.5 usec, the RF phase calibration mode is enabled by the ILT/PCU hardware. In the RF phase calibration mode, the digitized signal strength of the LV that was just processed and the calibration frequency tuning voltage are sent to the receiver circuitry. The calibration signal phases are sampled, and the measured phases only are digitized and held. Upon completion of the RF phase calibration mode, the ILT/PCU generates an interrupt to the SPU causing all the data digitized during the normal and RF phase calibration modes to be sent to the SPU in 16 bit parallel word messages.

3.1.1.2.5 Signal Processor Unit (SPU). The Signal Processor Unit (SPU), in which the SCHANS Operational Program resides, provides the necessary logical operations to sort the desired signals from the multiple emitter environment, collect and calibrate the emitter data on a pulse by pulse basis and input smoothed angle and TOA data to the navigation filter. The SPU also computes navigation and attitude for the spacecraft in real time. It provides the point of interface between the ILT/PCU and the spacecraft telemetry and command systems, the Digital Interface Unit (DIU) and the Inertial Measurement Unit (IMU).

3.1.2 SPU Interface.

3.1.2.1 SPU Interface Block Diagram. Figure 3-8 is the SPU Interface Block Diagram.

3.1.2.2 SPU I/O Utilization Table. Table 3-1 is the SPU I/O Utilization Table.

3.1.2.3 SPU/(ILT/PCU) Interface. The SPU/(ILT/PCU) interface is a 16-bit, two-way, parallel data channel and appropriate discrete lines to effect the data exchange. Also contained in the interface is a discrete line for ILT/PCU power ON/STANDBY control by the SPU.

3.1.2.3.1 SPU to ILT/PCU Data Transfer. The SPU to ILT/PCU data transfer format is shown in Table 3-2. The bit definition is presented in Table 3-3.

3.1.2.3.2 ILT/PCU to SPU Data Transfer. The ILT/PCU to SPU data transfer formats are shown in Tables 3-4, 3-5, and 3-6. Selection of one of the three data transfer modes is under RF Signal Processing Program control.

3.1.2.4 SPU/DIU Interface. The SPU/DIU interface is a 16-bit, two-way serial data channel and appropriate discrete lines to effect the data exchange. Interface data formats are TBD.

3.1.2.5 SPU/Telemetry Interface.

3.1.2.5.1 SPU to Telemetry Data Transfer. SPU to Telemetry data is transferred over a 16-bit serial interface. The data format is described in IBM Document Number TBD, SCHANS Program Data Item A014.

3.1.2.5.2 Telemetry to SPU Data Transfer. Telemetry to SPU data is transferred over an 8-bit parallel interface. The data format for this interface is TBD.

Telemetry to SPU data is also transferred by eight discretes, defined as follows:

a. SPU Power ON. (Initiate SPU power on sequence.)

b. Start. (Initialize software timing and hardware.)

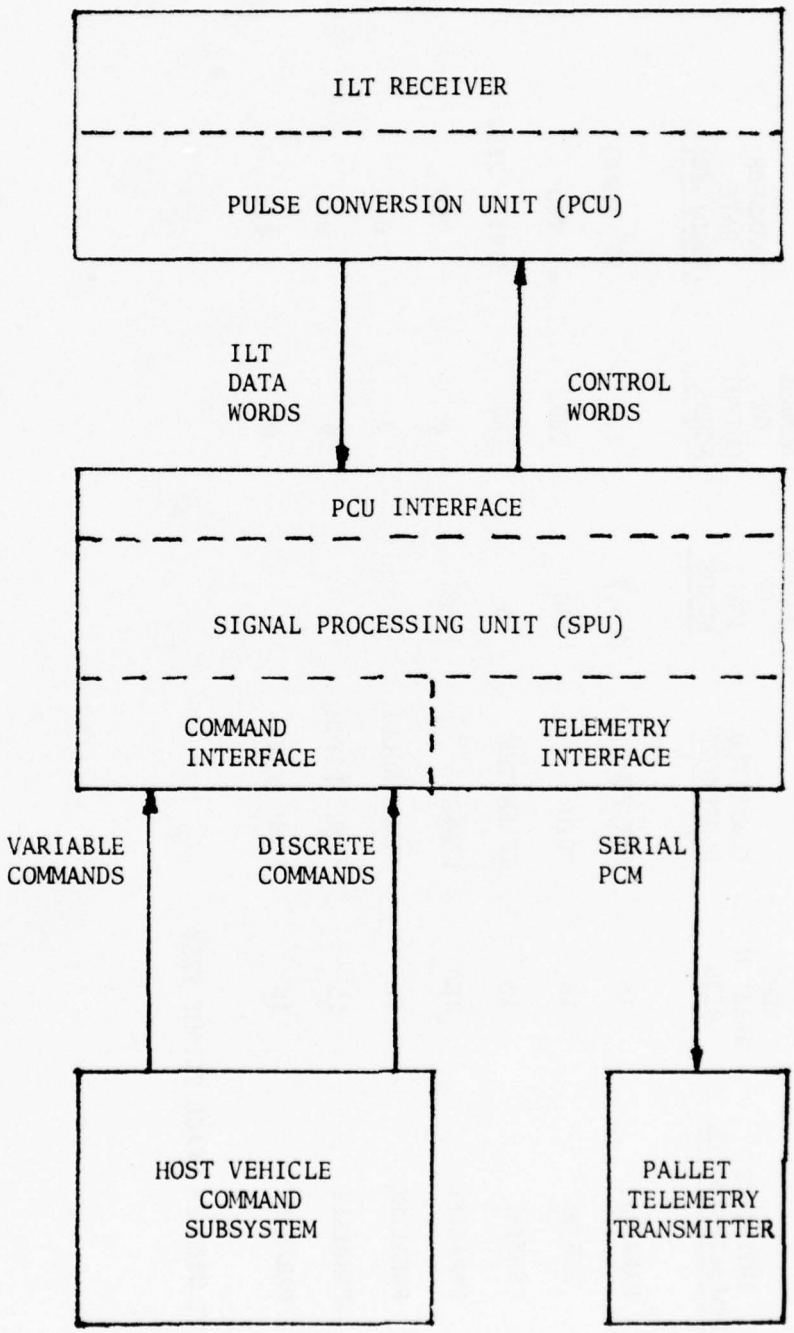


Figure 3-8. SPU Interface Diagram

Table 3-1

SPU I/O UTILIZATION TABLE (ENCODED DATA)

HEX DEVICE NUMBER	INTERFACE CHARACTERISTICS	WORD SIZE IN BITS	CONNECTED EQUIPMENT	NUMBER OF INPUT WORDS	NUMBER OF OUTPUT WORDS	TRANSFER RATE (WORD/SEC)
TBD	PARALLEL	16	ILT/PCU	4,5,7	1,2	10^7 (MAX)
TBD	SERIAL	16	*DIU	TBD	TBD	TBD
TBD	SERIAL	16	TELEMETRY	0	TBD	3125 - 7500
TBD	PARALLEL	TBD	COMMAND	TBD	0	TBD
TBD	PARALLEL	16	*IMU (ROLL)	1	0	0.5
TBD	PARALLEL	16	*IMU (PITCH)	1	0	0.5
TBD	PARALLEL	16	*IMU (YAW)	1	0	0.5

* NOT USED IN SPACE FLIGHT TEST

Table 3-2

SPU TO ILT/PCU DATA TRANSFER FORMAT

FUNCTION	ADDRESS		BIT DATA													
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
					MSB											LSB
REC. TUNING	0	0	SPARE	SPARE	200.0896 MHz	100.0448 MHz	50.0224 MHz	25.0112 MHz	12.5056 MHz	6.2528 MHz	3.1264 MHz	1.5632 MHz	.7816 MHz	.3908 MHz	.1954 MHz	.0977 MHz
MODE REGISTER	0	1	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	USE FREQ WINDOW	WIDE PULSE MODE	IF CAL SEL 2	IF CAL SEL 1	IF CAL MODE	RE FREQ CAL MODE	ANT. SEL.	PROC. EN.
SPARE	1	0														
SPARE	1	1														

Table 3-3

SPU to ILT/PCU DATA TRANSFER BIT DEFINITION

Bit Position	Signal Name	Definition
BIT 15	PROCESS ENABLE	0 PROCESSING DISABLED 1 PROCESSING ENABLED
BIT 14	ANTENNA SELECT	0 ANTENNA #1 1 ANTENNA #2
BIT 13	RF FREQ CAL MODE	0 RF CAL MODE 1 NORMAL MODE
BIT 12	IF CAL MODE	0 NORMAL MODE 1 IF CAL MODE
BIT 11 BIT 10	IF CAL SEL 1 IF CAL SEL 2	Sel 1 / Sel 2 / IF CAL SEC 0 / 0 / -45^{o} 0 / 1 / $+45^{o}$ 1 / 0 / $+135^{o}$ 1 / 1 / $+225^{o}$
BIT 9	WIDE PULSE MODE	0 HOLD AT 0.7 µs 1 HOLD AT 5 µs
BIT 8	USE FREQ WINDOW	0 WINDOW DISABLED 1 WINDOW ENABLED

Table 3-4

ILT/PCU TO SPU NORMAL MODE DATA TRANSFER FORMAT

WORD	BIT 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	543948.8	TOA 1 (nanoseconds)														16.6
2	35651584	TOA 2 (microseconds)														1088
3	1	AMPL. (V)						.0078125	1	FREQ (V)						.0078125
4						OCTANT A B_0	B_1	B_2	1	PHASE A						.0078125
5						OCTANT B B_0	B_1	B_2	1	PHASE B						.0078125
6						OCTANT A B_0	B_1	B_2	1	PHASE A CAL						.0078125
7						OCTANT B B_0	B_1	B_2	1	PHASE B CAL						.0078125

Table 3-5

ILT/PCU TO SPU RF FREQUENCY CALIBRATION MODE DATA TRANSFER FORMAT

WORD	BIT 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	543948.8	TOA 1 (nanoseconds)														16.6
2	35651584	TOA 2 (microseconds)														1088
3	1	AMPL. (V)							1	FREQ (V)						.0078125
						OCTANT A										
4						B_0	B_1	B_2	1	PHASE A						.0078125
						OCTANT B										
5						B_0	B_1	B_2	1	PHASE B						.0078125

Table 3-6

ILT/PCU TO SPU IF PHASE CALIBRATION MODE DATA TRANSFER FORMAT

	BIT															
WORD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1						B_0	OCTANT B_1	A B_2	1	RAW SIN A AMP (V)						.0078125
2						B_0	OCTANT B_1	A B_2	1	RAW COS A AMP (V)						.0078125
3						B_0	OCTANT B_1	B B_2	1	RAW SIN B AMP (V)						.0078125
4						B_0	OCTANT B_1	B B_2	1	RAW COS B AMP (V)						.0078125

c. Telemetry Transmit. (Initiate transmission of stored telemetry data.)

d. Real Time Mode. (Transmit real time telemetry data immediately following transmission of stored telemetry data.)

e. Ambiguity Resolution Mode. (Operate autonomously using phase ambiguity resolution algorithms.)

f. A Priori Mode. (Operate using a priori landmark location data rather than phase ambiguity resolution.)

g. SPU Power OFF. (Initiate SPU power off sequence.)

h. Spare.

3.1.3 Program Interface. The SCHANS Operational Program shall be a self-contained program with no requirement to interface with other programs within the spacecraft.

3.1.4 Program Description. The SCHANS Operational Program structure shall be as shown in Figure 3-9. The program shall be divided into two subprograms: the RF Signal Processing and Executive Program and the Navigation and Altitude Determenation Program (NADP). Coresident in the SPU shall be the two subprograms and a block of memory for storage of SCHANS measured and computed data which will be periodically dumped via telemetry link.

3.1.4.1 RF Signal Processing and Executive Program. The RF Signal Processing and Executive Program shall contain the receiver control and parameter measurement portion of the SCHANS Operational Program. Its major purposes will be to obtain the SCHANS equipment measurements required by the NADP and to store this data in the SPU memory where it will be retrieved by the NADP. The format of data placed in computer memory shall be as shown in Table 3-7.

The RF Signal Processing and Executive Subprogram shall also process the following interrupts:

a. Machine Check. This interrupt indicates a main store parity error.

b. Inertial Measurement Unit (IMU). This interrupt indicates that reading of the IMU attitude inputs is required.

c. Telemetry. This interrupt indicates that transmission of data collected for telemetry is required.

d. DIU. This interrupt indicates that DIU servicing is required.

e. Program Loadable Counter 1 (PLC1).

f. Program Loadable Counter 2 (PLC2).

g. Program Loadable Counter 3 (PLC3).

h. ILT/PCU Data Store (Pulse Detected). This interrupt indicates that a 4, 5, or 7 word ILT/PCU data message is ready for input to the SPU.

3.1.4.2 Navigation and Attitude Determination Program (NADP). The NADP shall retrieve SCHANS equipment measurement data placed in memory by the RF Signal Processing and Executive Program and process it to

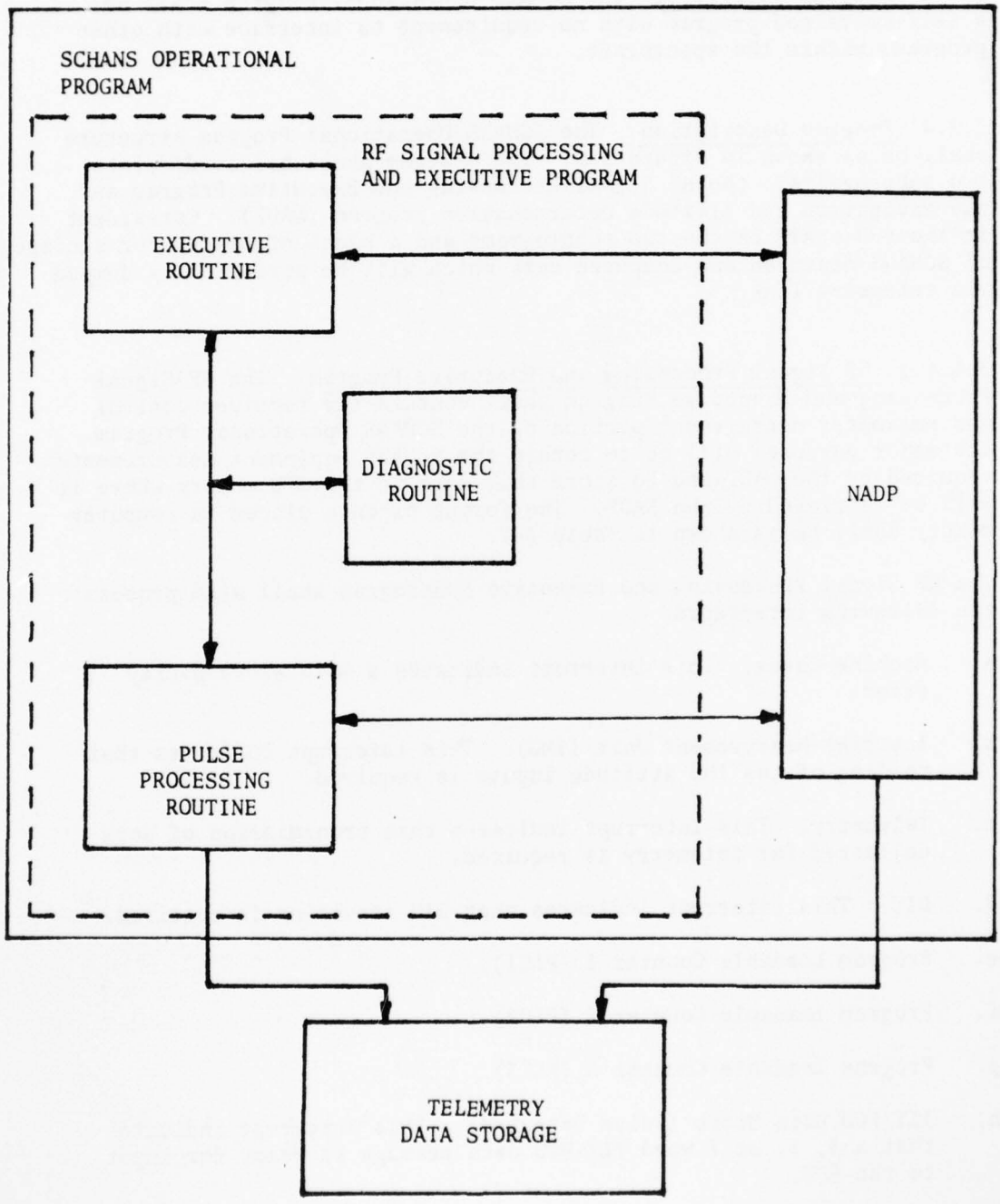


Figure 3-9. SCHANS Operational Program Structure

Table 3-7

RF SIGNAL PROCESSING AND EXECUTIVE PROGRAM

MEASUREMENT DATA FORMAT

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TOA	543 938.8	—	—	—	—	—	nanoseconds	—	—	—	—	—	—	—	—	16.6
TOA	35 651 584	—	—	—	—	—	microseconds	—	—	—	—	—	—	—	—	1088
AMPLITUDE						1	—	—	—	volts	—	—	—	—	—	~.001
FREQUENCY	327.68	—	—	—	—	—	MHz	—	—	—	—	—	—	—	—	~.01
ROLL PHASE ANGLE			180	—	—	—	—	—	degrees	—	—	—	—	—	—	~.0225
PITCH PHASE ANGLE			180	—	—	—	—	—	degrees	—	—	—	—	—	—	~.0225
LANDMARK NUMBER								256	—	—	—	—	—	—	—	1
*FLAGS	SBF	DCF	LNDF		DFF		SSF		LAF							
IMU (ROLL)	|	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TBD
IMU (PITCH)	|	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TBD
IMU (TAW)	|	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TBD
ATTITUDE UPDATE TIME	|	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TBD

* SBF = Short baseline flag
DCF = Data complete flag
LNDF = Landmark not detected flag
DFF = Diagnostic fail flag
SSF = Scan synchronization flag
LAF = Landmark acquired flag

provide estimates of current spacecraft position, velocity, and attitude based on past measurements.

The NADP shall also place in memory data for control of the RF Signal Processing and Executive Program. The format of this data shall be as shown in Table 3-8.

Table 3-8

NADP CONTROL DATA FORMAT

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LANDMARK ROLL PHASE (LBL)	180^{o}															
LANDMARK ROLL PHASE (SBL)	180^{o}															
LANDMARK PITCH PHASE (LBL)	180^{o}															
LANDMARK PITCH PHASE (SBL)	180^{o}															
LANDMARK LINE-OF-SIGHT PROPAGATION DELAY	10,000 µsec															
FLAGS	SCHF*															
TIME UNTIL MEASUREMENT	1 HOUR															
LANDMARK NUMBER FOR DATA COLLECTION								256								1
LANDMARK NUMBER FOR DELETION								256								1

* 400 MHz search flag

CODE IDENT NO.	SPECIFICATION NO.	REV

3.2 Detailed Functional Requirements.

3.2.1 RF Signal Processing and Executive Program. The RF Signal Processing and Executive Program shall consist of three major routines: the Executive Routine, the Pulse Processing Routine, and the Diagnostic Routine. The relationship among these routines shall be as shown in Figure 3-9.

3.2.1.1 Executive Routine. The Executive Routine, including its called subroutines, shall perform system power sequencing, initialization, calibration and interface data transfer control. Specific tasks of the Executive Routine and its called subroutines shall be as follows:

a. Control system power-up sequencing from the power off and standby power conditions.

b. Initialize the RF Signal Processing and Executive Program, NADP and hardware control registers.

c. Calibrate LO.

d. Calibrate phase detectors.

e. Keep real time.

f. Service IMU.

g. Service Telemetry.

h. Control system power-down sequencing from the power-on to standby conditions.

i. Process hardware interrupts.

j. Load memory via telemetry.

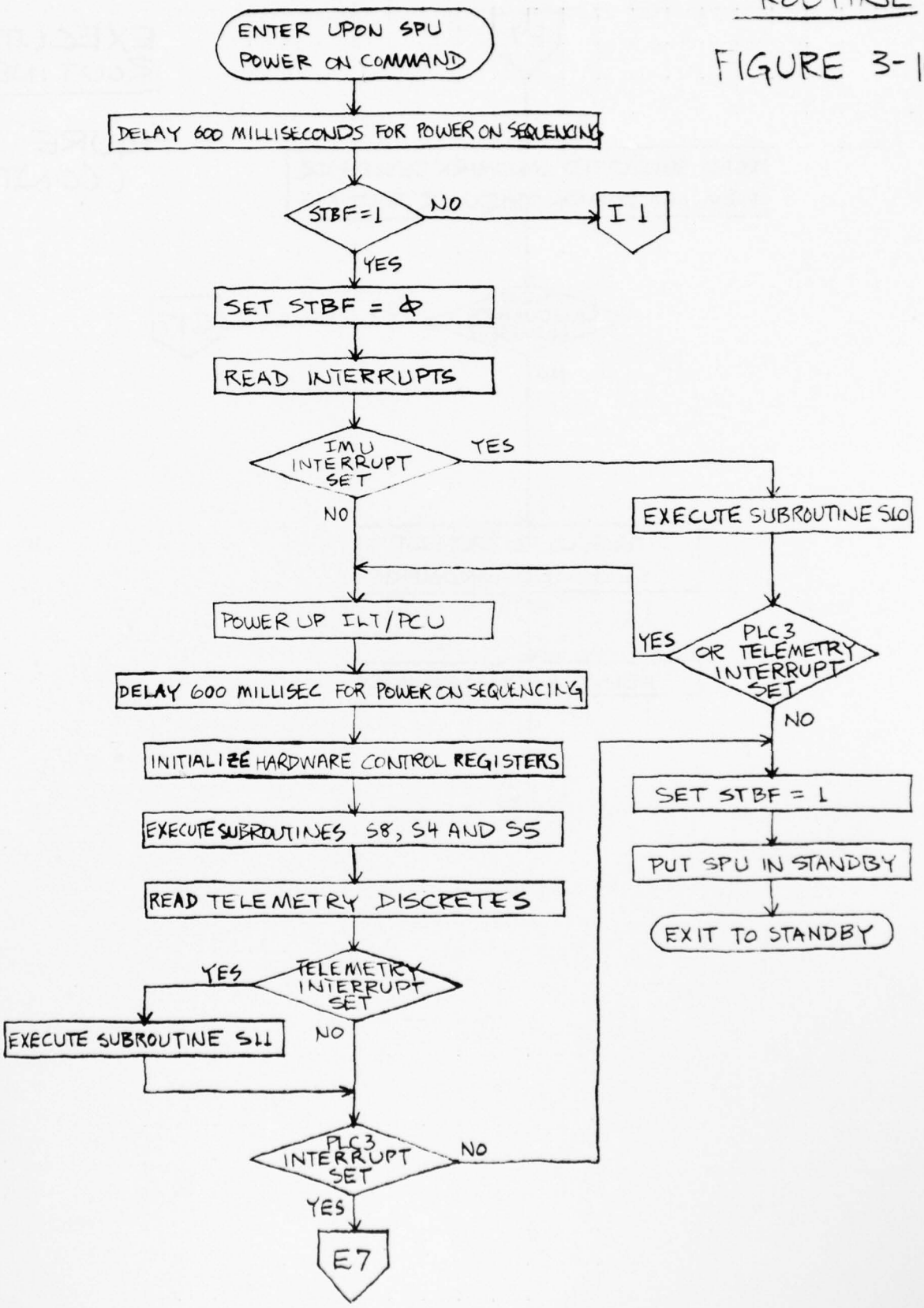
k. Dump memory via telemetry.

3.2.1.1.1 Routine Functional Flow Diagram. The functional flow diagram for the Executive Routine is shown in Figure 3-10. Functional flow diagrams for the subroutines called by the Executive Routine are shown in Figures 3-11 through 3-19.

3.2.1.1.2 Inputs. The Executive Routine or one of its called subroutines shall receive the following inputs:

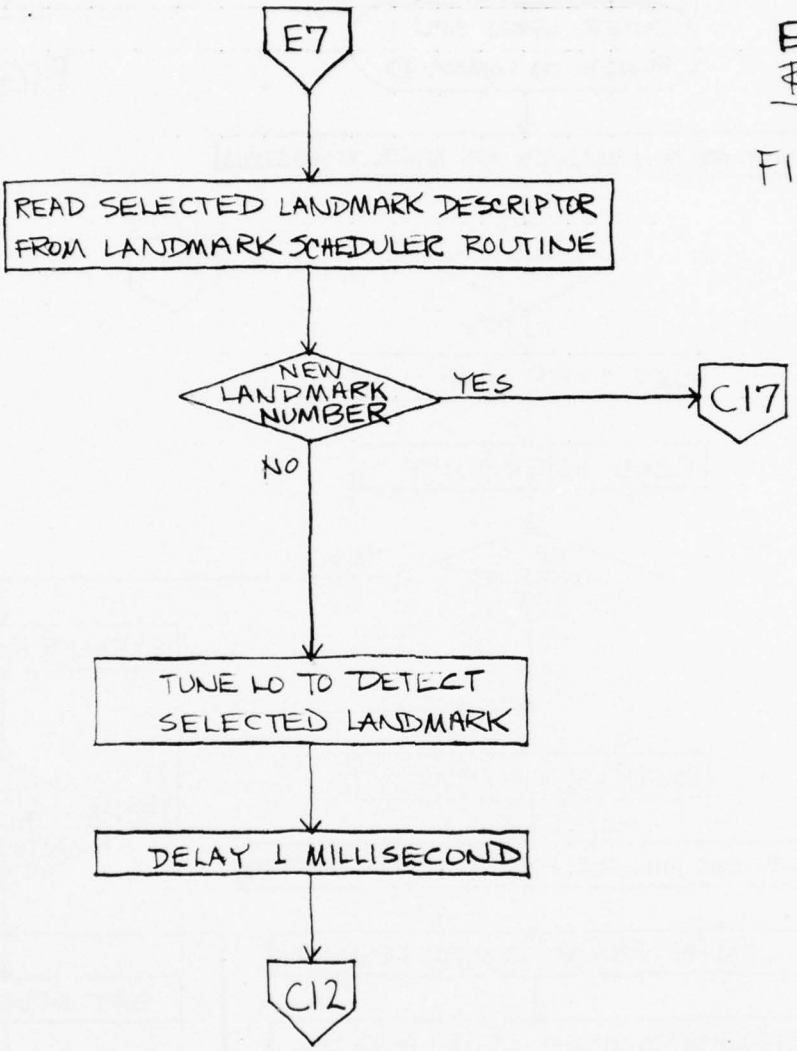
EXECUTIVE ROUTINE

FIGURE 3-10



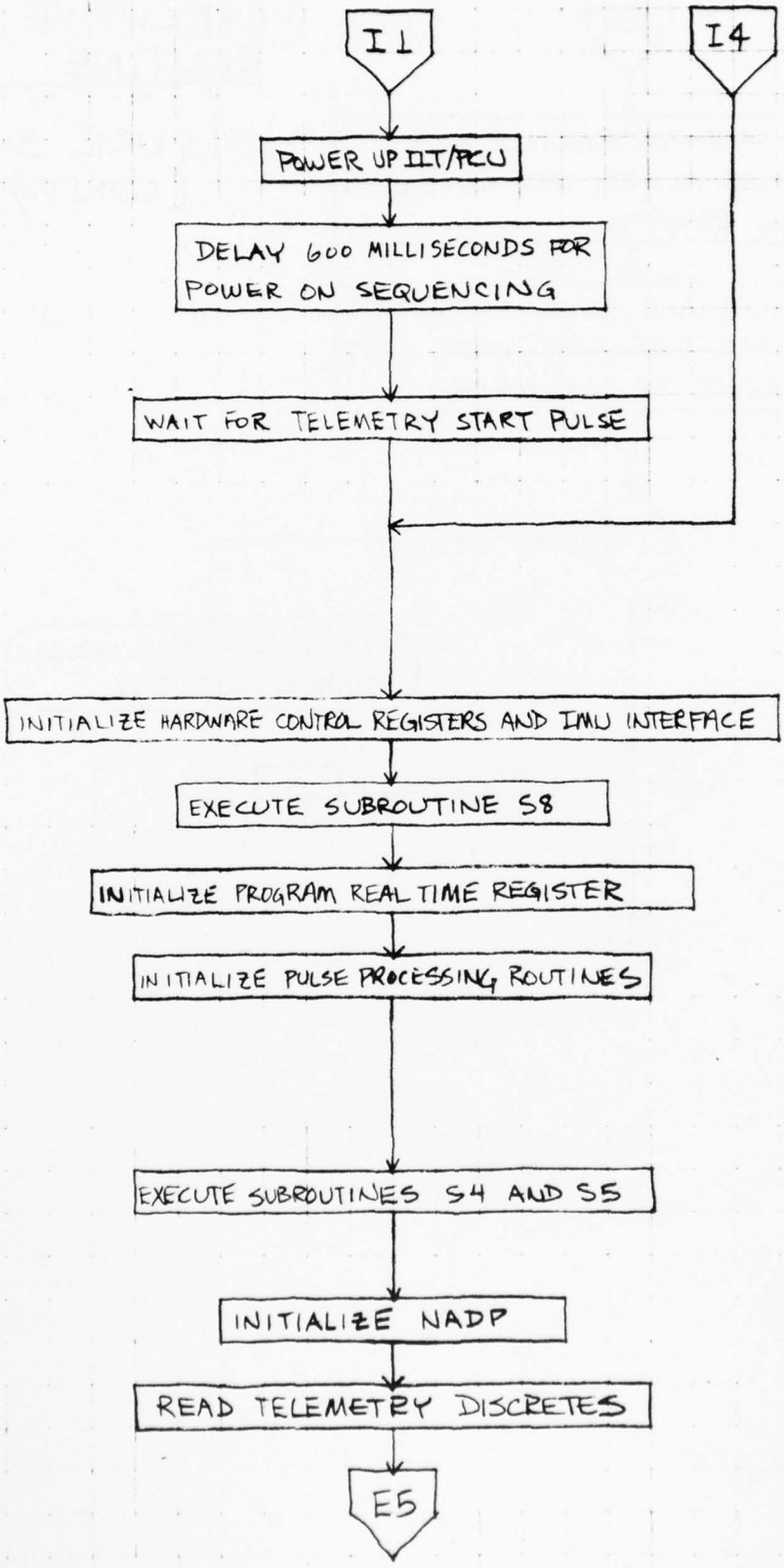
EXECUTIVE ROUTINE

FIGURE 3-10 (CONT.)



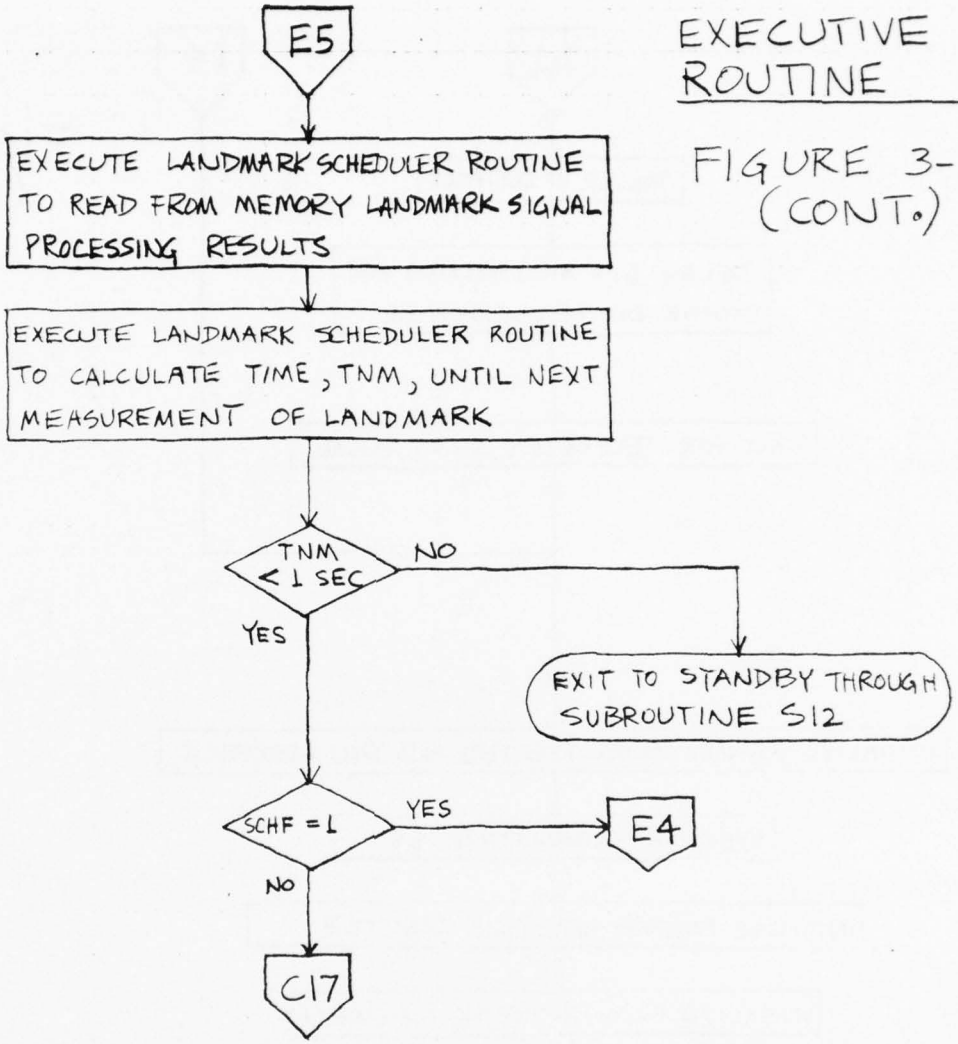
EXECUTIVE ROUTINE

FIGURE 3-10 (CONT.)



EXECUTIVE ROUTINE

FIGURE 3-10 (CONT.)



EXECUTIVE ROUTINE

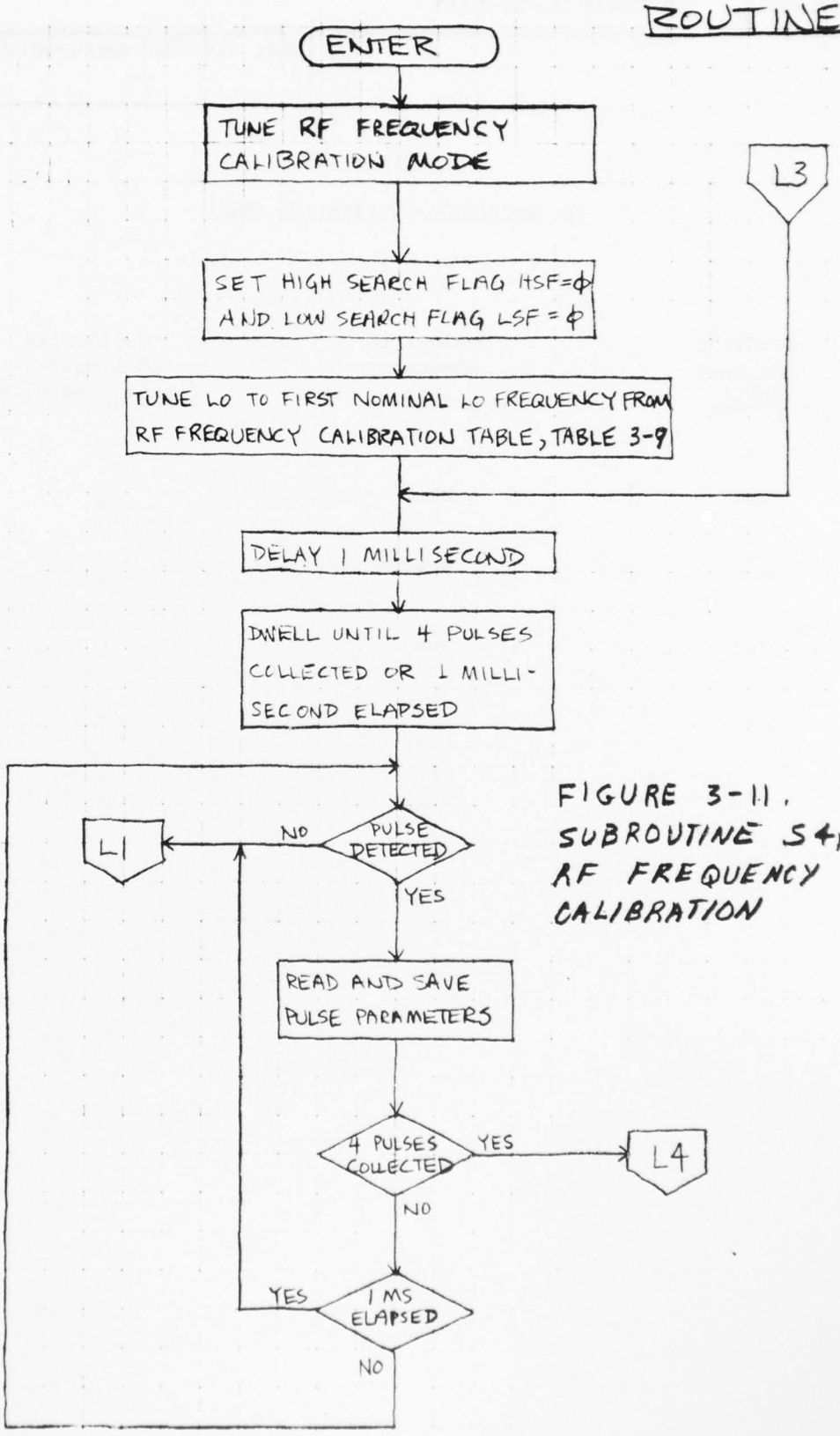


FIGURE 3-11. SUBROUTINE S4, RF FREQUENCY CALIBRATION

Table 3-9

RF FREQUENCY CALIBRATION TABLE

Combline Frequency (MHz)	Nominal LO Frequency (MHz)	Calibrated LO Frequency (Local Freq's) MHz
2500	2400	X
2600	2540	X
2700	2640	X
2800	2740	X
2900	2840	X

AD-A038 490 IBM FEDERAL SYSTEMS DIV OWEGO N Y F/G 17/7
SELF-CONTAINED, HIGH-ALTITUDE NAVIGATION SYSTEM STUDY: PRAIS NA--ETC(U)
JAN 77 R E DRESKA, G A KOOCH, L O SMITH F04701-76-C-0106
UNCLASSIFIED IBM-77-D04-003S SAMSO -TR-77-57-VOL-3 NL

3 OF 3
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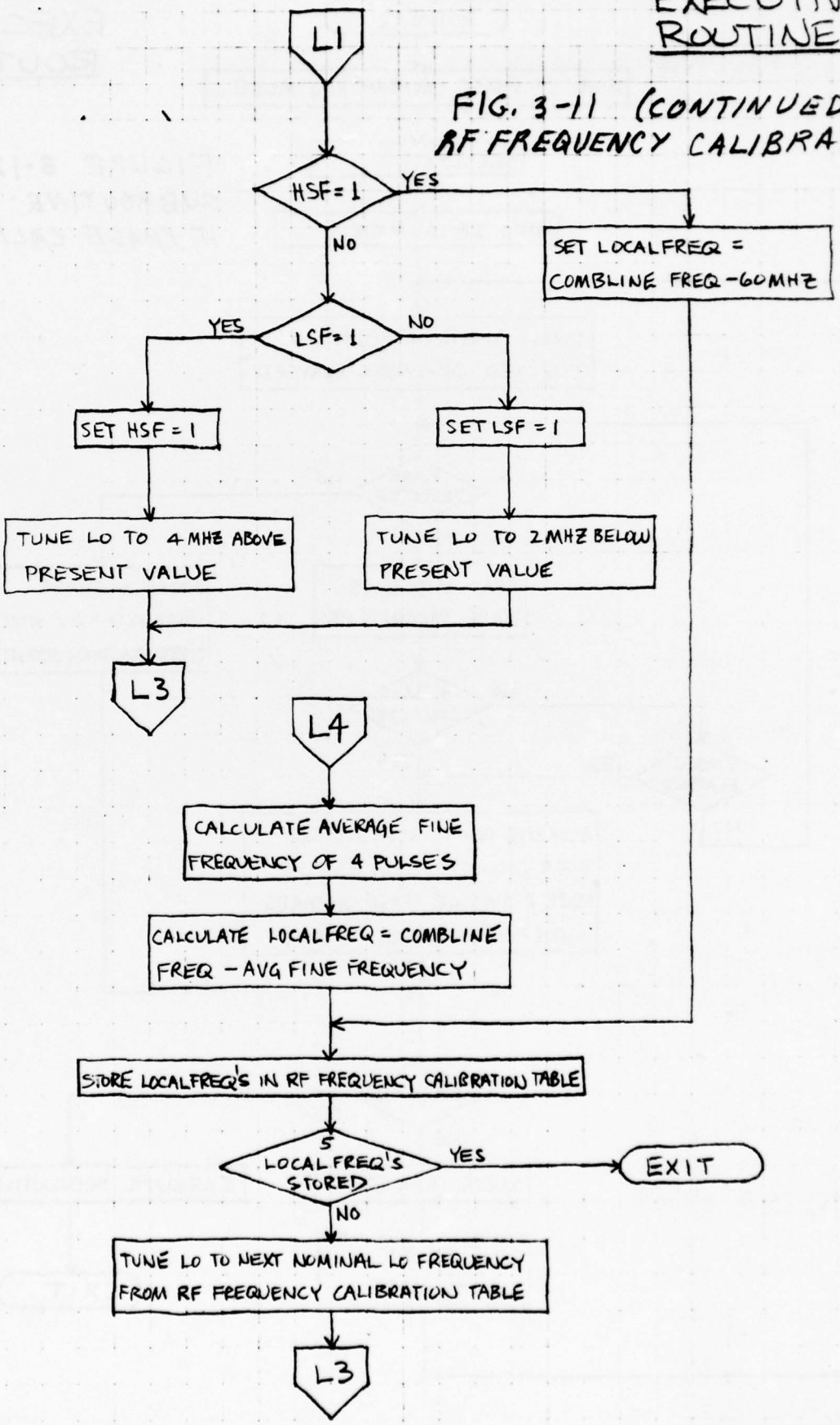
EXECUTIVE ROUTINE

FIG. 3-11 (CONTINUED)
RF FREQUENCY CALIBRATION, S4



EXECUTIVE ROUTINE

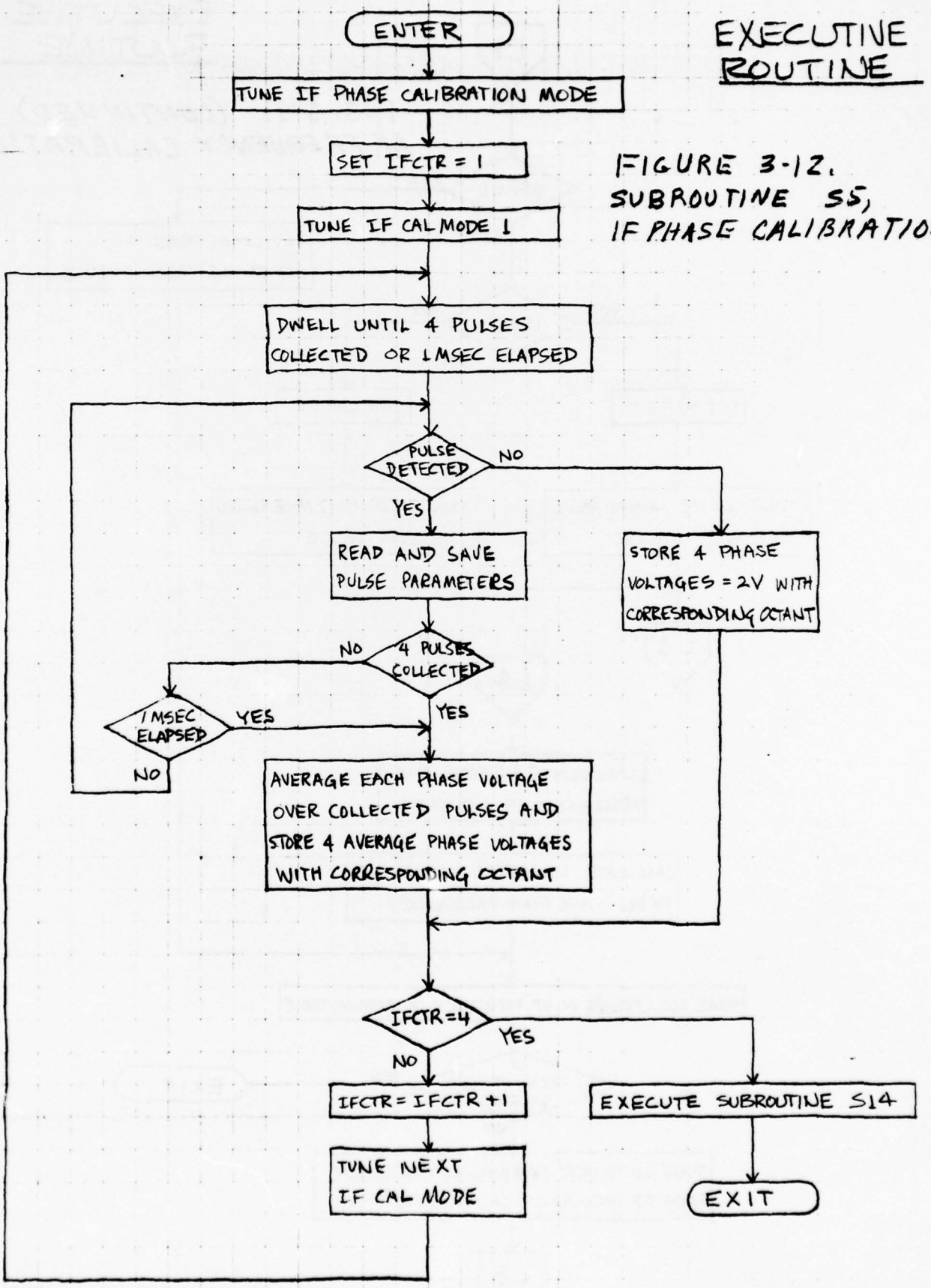


FIGURE 3-12. SUBROUTINE S5, IF PHASE CALIBRATION

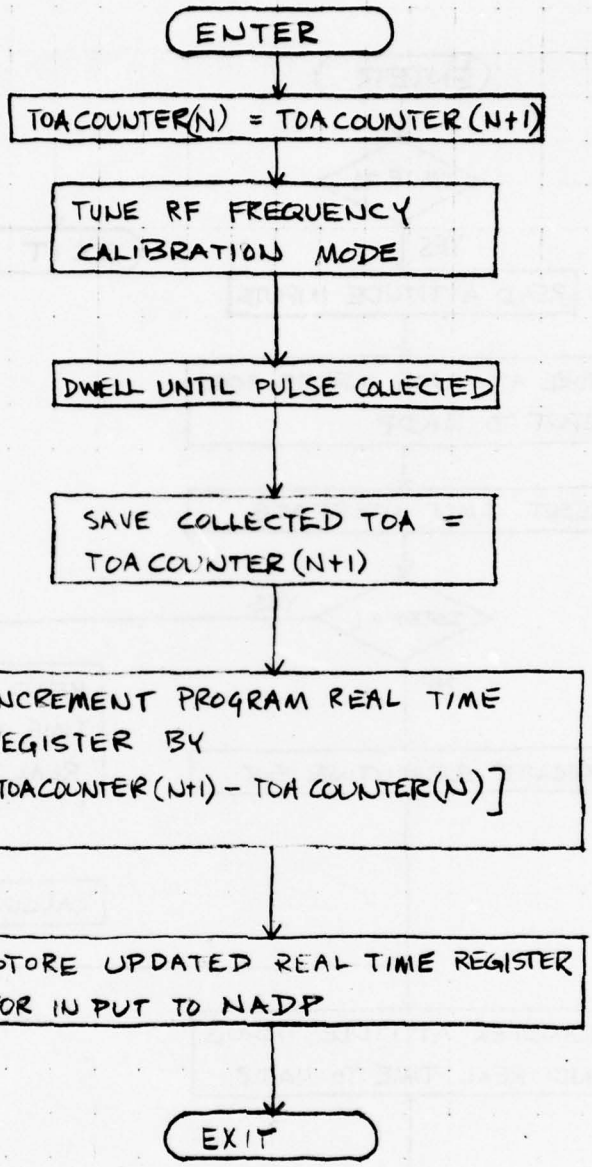


FIGURE 3-13. SUBROUTINE S8, REAL TIME UPDATE

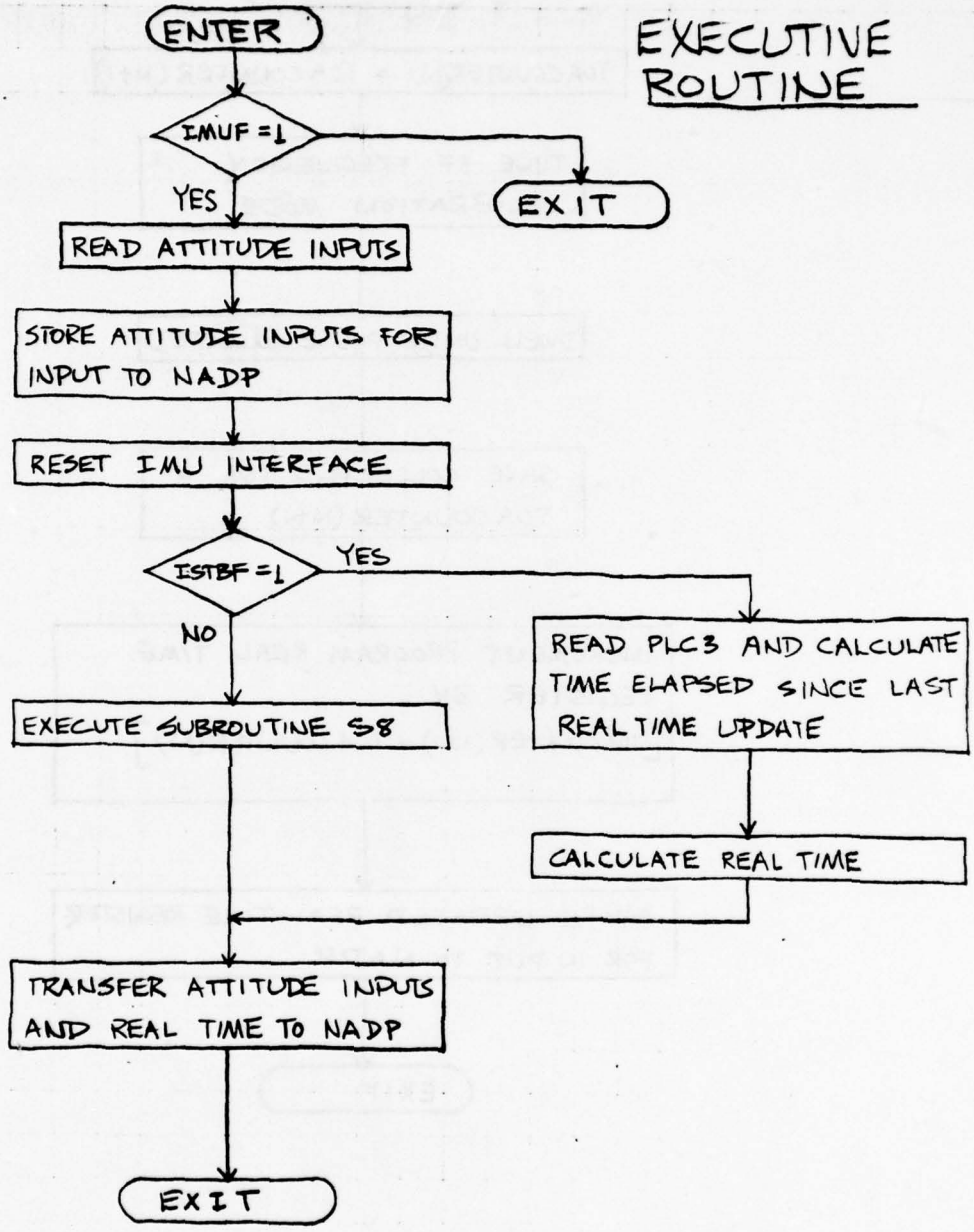


FIGURE 3-14. SUBROUTINE S10, IMU SERVICE

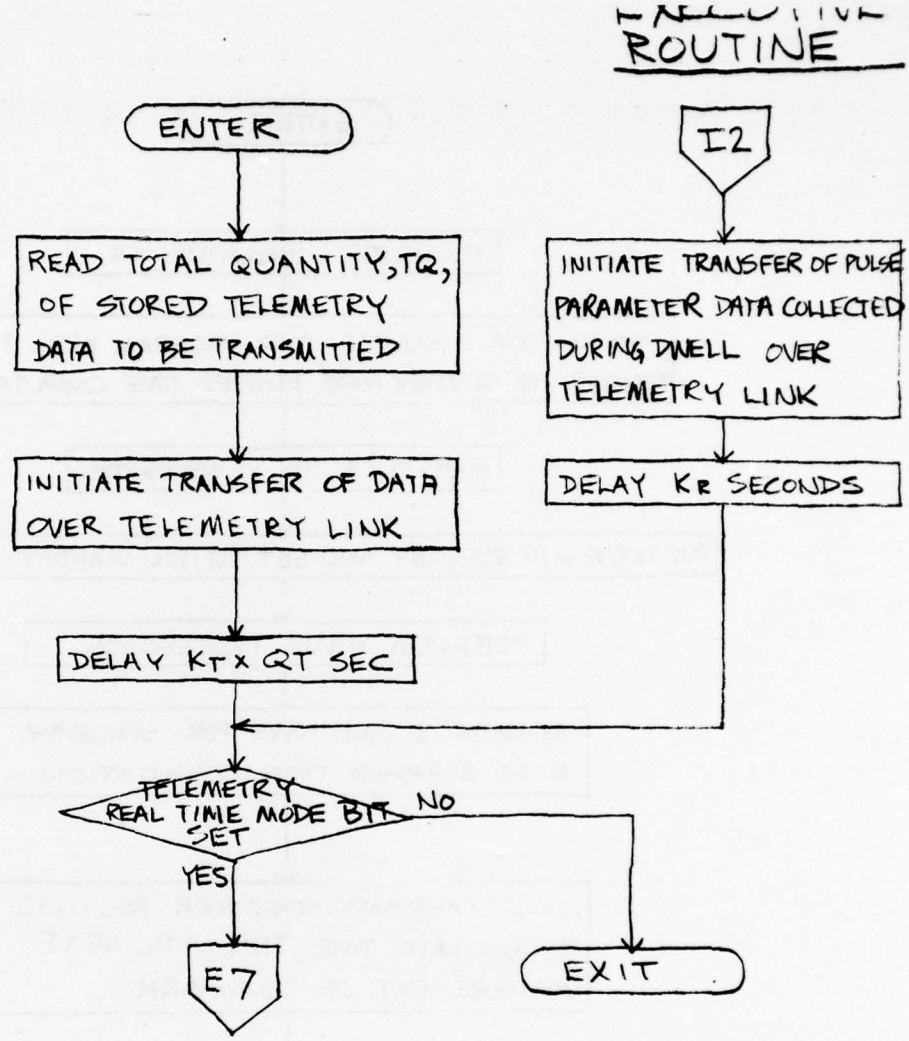


FIGURE 3-15, SUBROUTINE S11, TELEMETRY SERVICE

EXECUTIVE ROUTINE

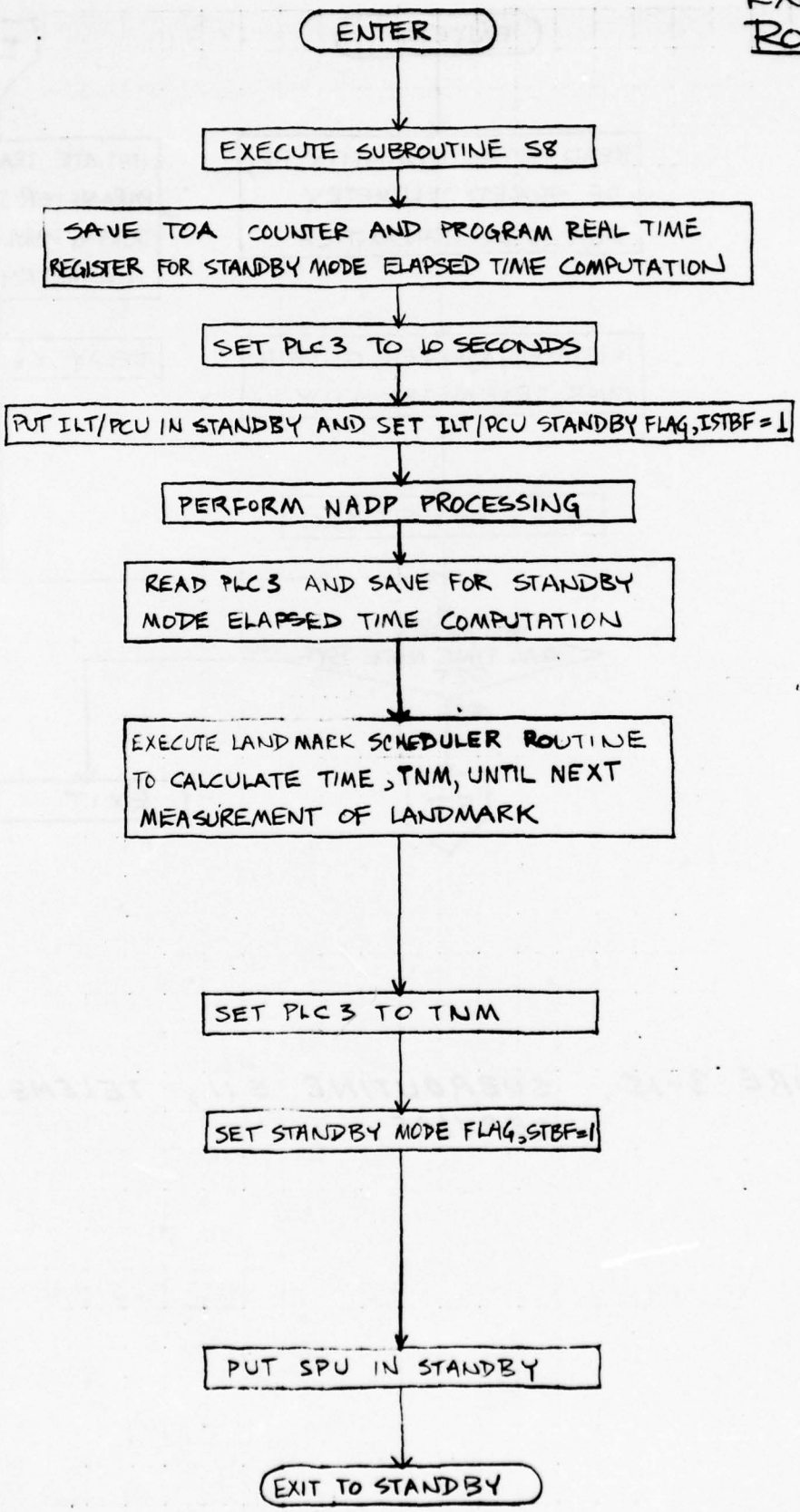


FIGURE 3-16. SUBROUTINE S12, POWER ON TO STANDBY

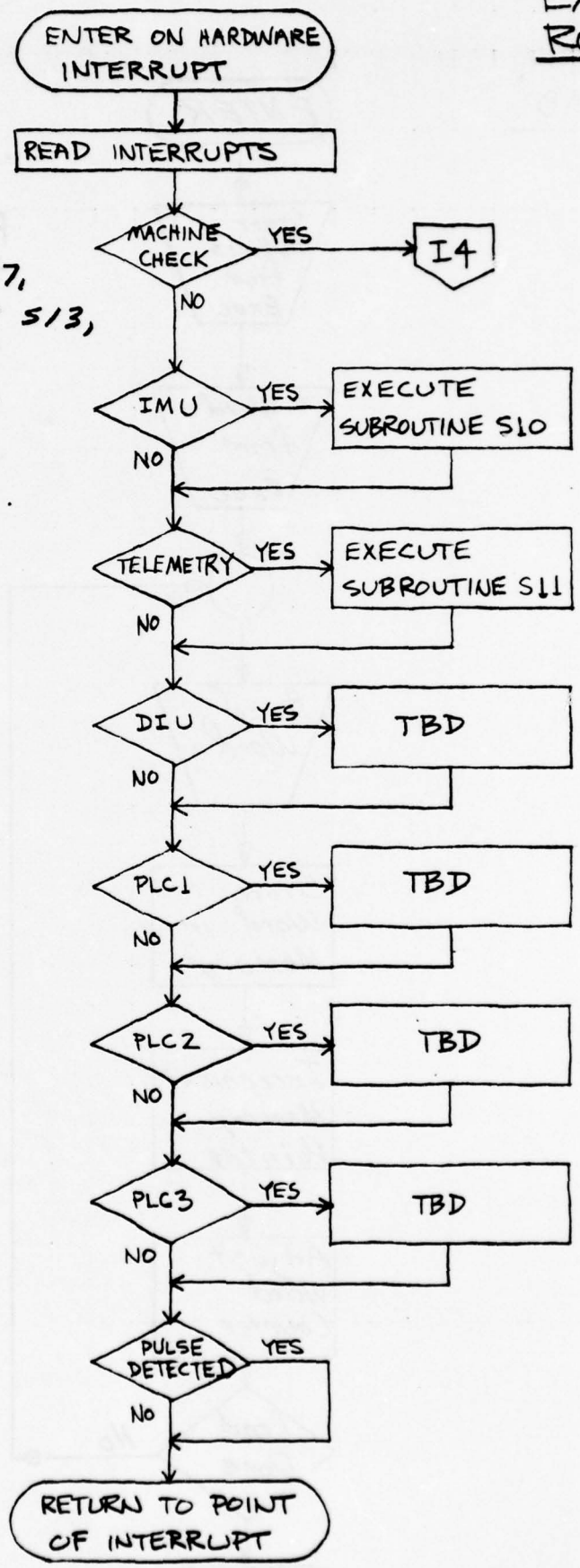


FIGURE 3-17, SUBROUTINE S13, INTERRUPT PROCESSING

EXECUTIVE ROUTINE

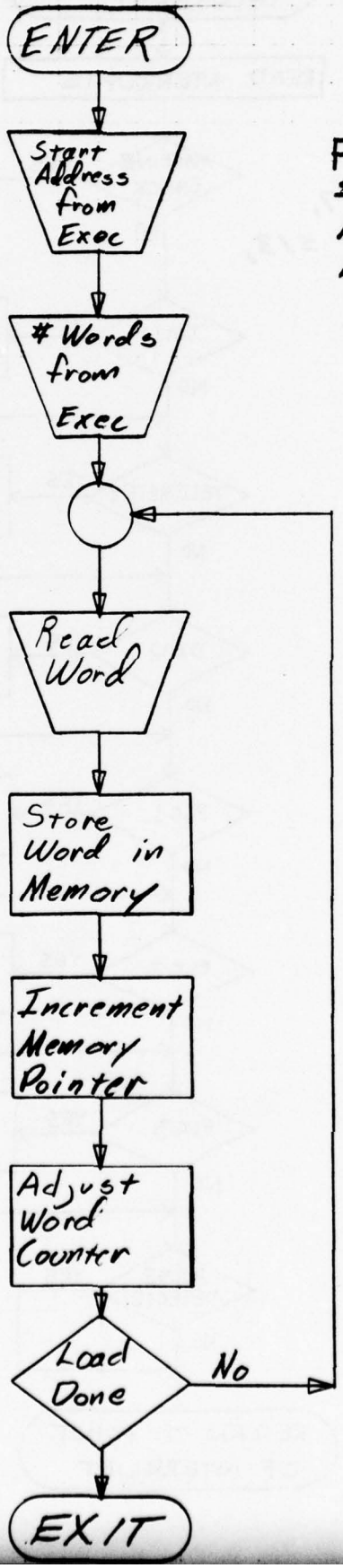


FIGURE 3-18, SUBROUTINE S17, MEMORY LOAD

EXECUTIVE ROUTINE

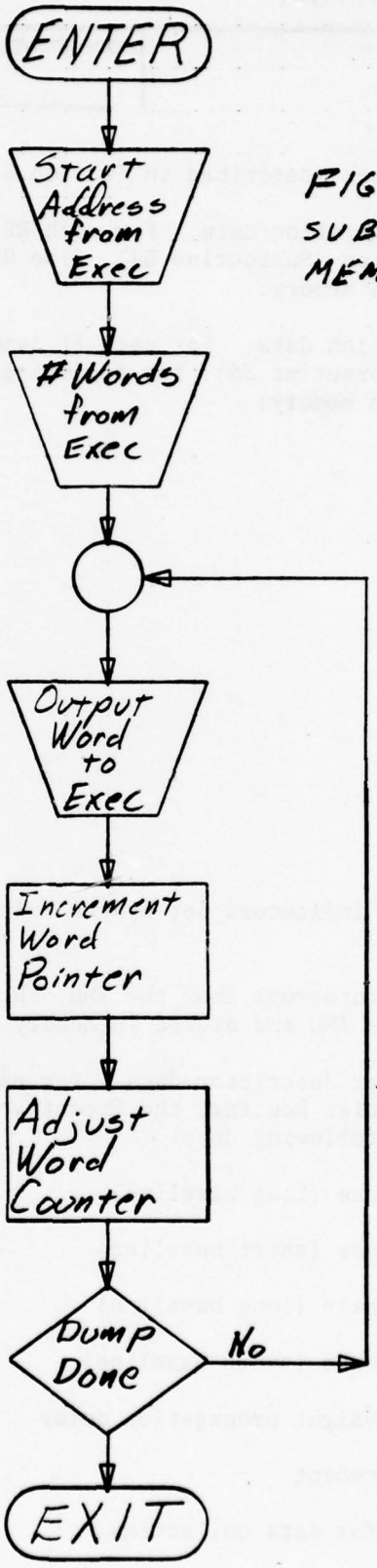


FIGURE 3-19. SUBROUTINE S18, MEMORY DUMP

a. Telemetry discretes (described in Section 3.1.2.5).

b. RF frequency calibration data. For each RF sample processed for RF frequency calibration (Subroutine S4), fine RF voltage shall be measured and stored in memory.

c. IF phase calibration data. For each IF sample processed for IF phase calibration (Subroutine S5), the following parameters shall be measured and stored in memory:

1. Sin A voltage

2. Sin A octant

3. Cos A voltage

4. Cos A octant

5. Sin B voltage

6. Sin B octant

7. Cos B voltage

8. Cos B octant

d. Flags and status indicators set by the Pulse Processing and Diagnostic Routines.

e. Attitude. Upon interrupt from the IMU, three-axis attitude inputs shall be read from the IMU and stored in memory.

f. Landmark scheduler descriptor data. For each landmark selected by the Landmark Scheduler Routine, the Executive Routine shall read read from memory the following data:

1. Landmark roll phase (long baseline)

2. Landmark roll phase (short baseline)

3. Landmark pitch phase (long baseline)

4. Landmark pitch phase (short baseline)

5. Landmark line-of-sight propagation delay

6. Time until measurement

7. Landmark number for data collection

8. Landmark number for deletion

9. RF

10. PRI

11. Stagger

12. Flags

g. Hardware interrupts (described in Section 3.1.4.2.2).

h. Real time update. For each RF sample processed for real time update (Subroutine S8), Sample TOA shall be measured and stored in memory.

i. Memory load control data. Start address and number of words to be loaded.

j. Memory dump control data. Start address and number of words to be dumped.

3.2.1.1.3 Processing. The Executive Routine, including its called subroutines shall perform the following processing functions:

a. Power up sequencing. The Executive Routine shall power up the system from the power off condition or the standby condition. From the power off condition, the power on sequence will be initiated by the SPU Power ON telemetry discrete which will power up the SPU. The Executive Routine shall recognize this discrete and power up the ILT/PCU. From the standby condition, the power on sequence will be initiated by an IMU, Telemetry Transmit or PLC3 underflow interrupt. The Executive Routine shall recognize and service these interrupts.

b. Initialization. The executive Routine shall, following the power-up sequence, initialize the RF Signal Processing and Executive Program, the NADP and hardware control registers.

c. LO calibration. Subroutine S4, RF Frequency Calibration shall be executed to perform LO calibration. Under program control, RF signals at five predetermined frequencies will be injected into the ILT/PCU front end and sequentially processed. Fine frequency of the test signal shall be used to determine local oscillator calibration frequencies.

d. Real timekeeping. The RF Frequency Calibration Mode shall also be used to obtain a TOA counter reading. The TOA counter reading shall be used to update the program real time register which shall keep real time during both the power on and standby conditions. During standby operation, the TOA counter will run. It shall be read through execution of Subroutine S8 upon underflow of PLC3 which shall be set prior to program exit to the standby mode.

e. Phase detector calibration. The phase detectors shall be calibrated through execution of Subroutine S5, IF Phase Calibration. Under software control, an IF signal simulating four predetermined baseline phase angles will be injected into the ILT/PCU IF circuitry and sequentially processed. Phase measurements of the test signals shall be used to calibrate the voltage versus phase response of the phase detectors.

f. Attitude input processing. Upon receipt of the IMU Service Interrupt the Executive Routine shall execute S10, IMU Service Subroutine. Attitude inputs from the IMU shall be read, stored, and transferred to the NADP. A real time associated with the attitude inputs shall be calculated and transferred to the NADP.

g. Telemetry down link processing. Upon receipt of the Telemetry Transmit Interrupt, the Executive Routine shall execute S11, Telemetry Service Subroutine. Stored telemetry data collected on previously processed landmarks shall be transmitted over the telemetry link. After transmission is completed, the Executive Routine shall read the Real Time Mode telemetry discrete. If the Real Time Mode discrete is activated, the program shall then collect and transmit real time landmark data. The format of the data to be transmitted is described in Section 3.1.2.5.1. The Executive Routine shall also control memory block diagnostic data for telemetry down link transmission via Subroutine S18.

h. Telemetry up link processing. The Executive Routine shall process data available at the up link telemetry interface such that the data may be placed in memory. The up link telemetry interface is TBD.

i. Power down sequencing. Upon completion of ILT/PCU processing, the Executive Routine shall place the ILT/PCU in standby power mode. Upon completion of SPU processing the Executive Routine shall place the SPU in standby power mode. Prior to placing the SPU in standby, PLC3 shall be set such that PLC underflows at the time when landmark pulse collection is next required.

j. Interrupt processing. Upon receipt of a hardware interrupt, Subroutine S13, Interrupt Processing shall be executed. Interrupts shall be prioritized as specified in the subroutine. Interrupts occurring during servicing of another interrupt shall be honored at the conclusion of servicing the first interrupt.

k. Memory load. The Memory Load Subroutine, S17, shall be called by the Executive Routine, shall load into memory data made available by the Executive Routine, and shall return control to the Executive Routine at completion of load.

1. Memory dump. The Memory Dump Subroutine, shall be called by the Executive Routine, shall output to the Executive Routine data specified by the Executive Routine, and shall return control to the Executive Routine.

3.2.1.1.4 Outputs. The Executive Routine or one of its called subroutines shall place in memory the following data:

a. Local oscillator calibration frequencies.

b. IF phase calibration constrants; four pulse averaged phase voltages with corresponding octant.

c. Real time updates.

d. IMU attitude measurements and corresponding real time.

e. Flags and status indicators.

3.2.1.2 Pulse Processing Routine. The Pulse Processing Routine, including its called subroutines, shall perform all processing functions required to reduce signals intercepted by the ILT/PCU to landmark report data suitable for input to the NADP. The Pulse Processing Routine shall also provide ILT/PCU tuning and control as required to insure intercept of desired landmark signals. The Pulse Processing routine and its called subroutines shall perform the following functions:

a. Tune LO to search for and center landmark frequency in IF passband; compute landmark RF.

b. Measure landmark signal pitch and roll phase angles; sort and qualify signals based on these measurements.

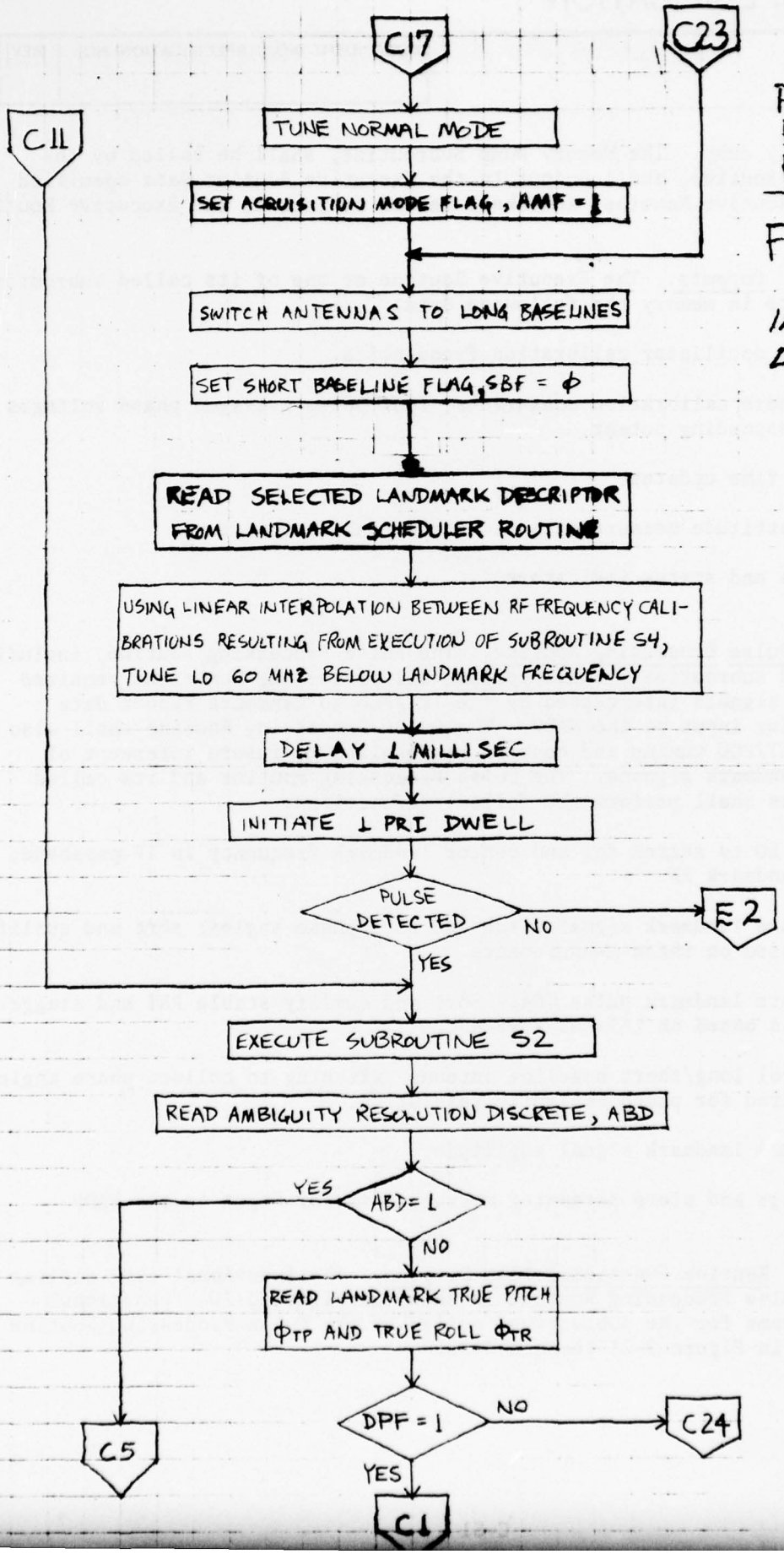
c. Measure landmark pulse TOA. Sort and qualify stable PRI and staggered PRI signals based on this measurement.

d. Control long/short baseline antenna switching to collect phase angle data required for phase ambiguity resolution.

e. Measure landmark signal amplitude.

f. Average and store parameter measurements for input to the NADP.

3.2.1.2.1 Routine Functional Flow Diagram. The functional flow diagram for the Pulse Processing Routine is shown in Figure 3-20. Functional flow diagrams for the subroutines called by the Pulse Processing Routine are shown in Figure 3-21 through 3-26.



PULSE PROCESSING ROUTINE

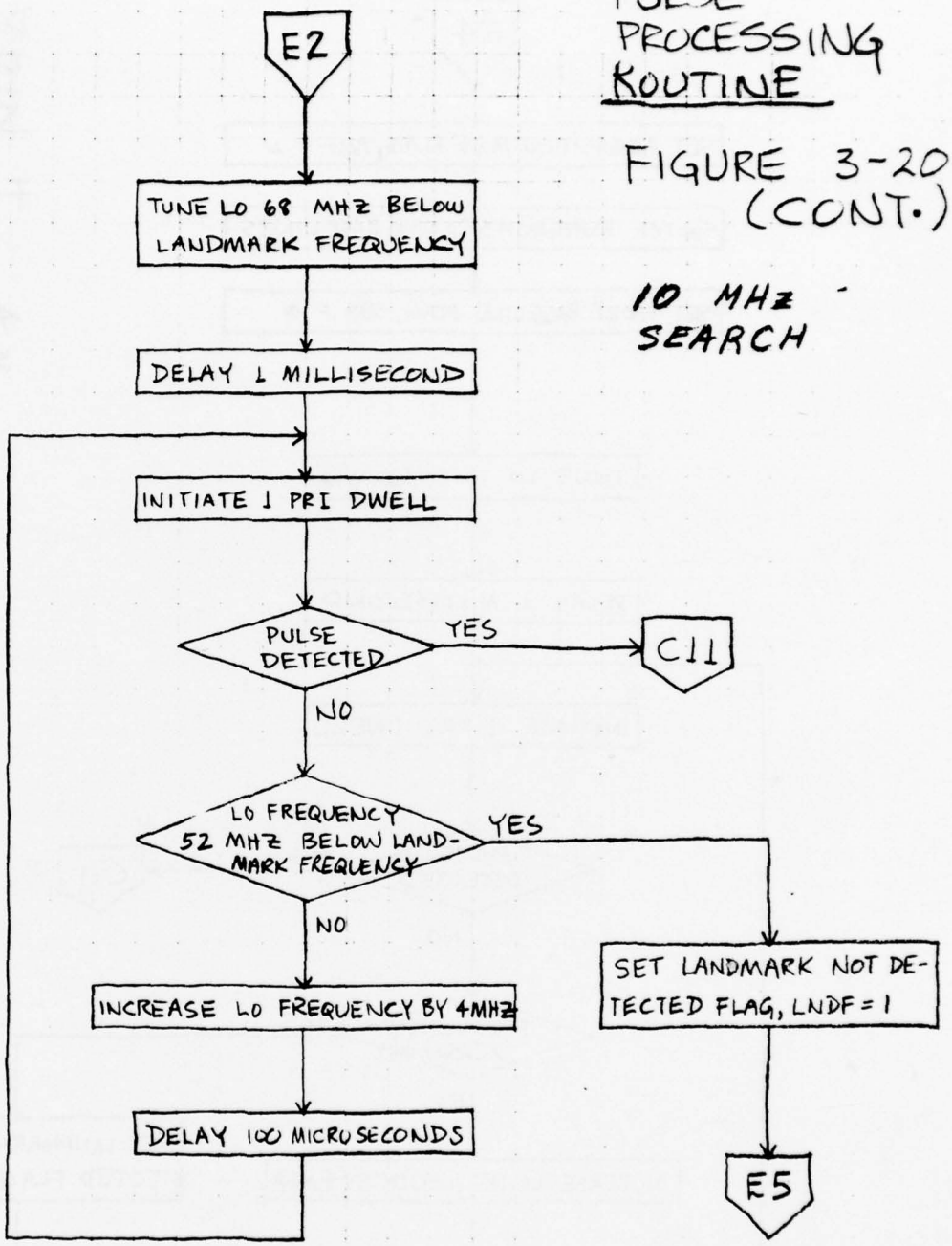
FIGURE 3-20

INITIAL PULSE DETECTION

PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)

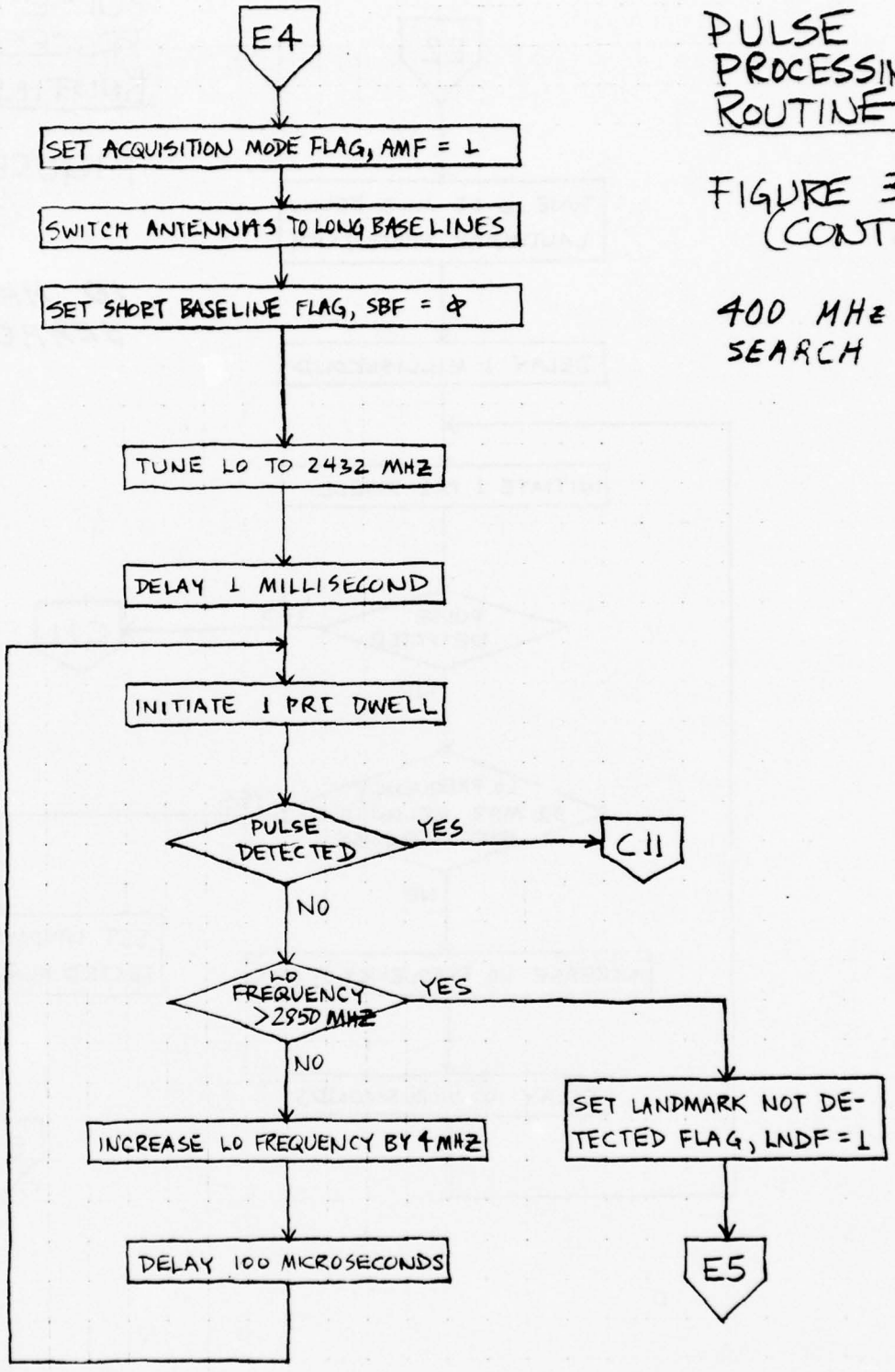
10 MHz SEARCH



PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)

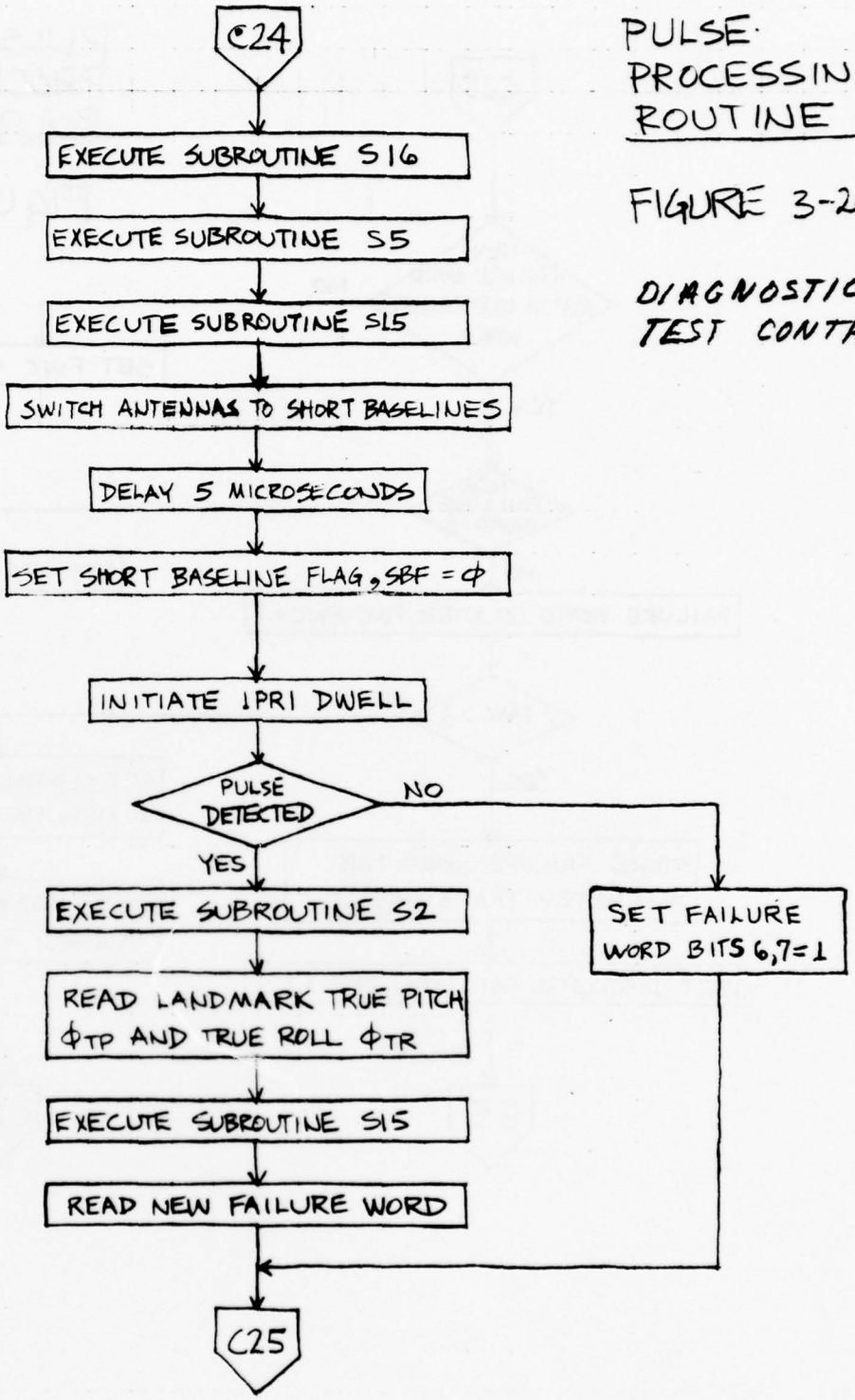
400 MHz SEARCH



PULSE PROCESSING ROUTINE

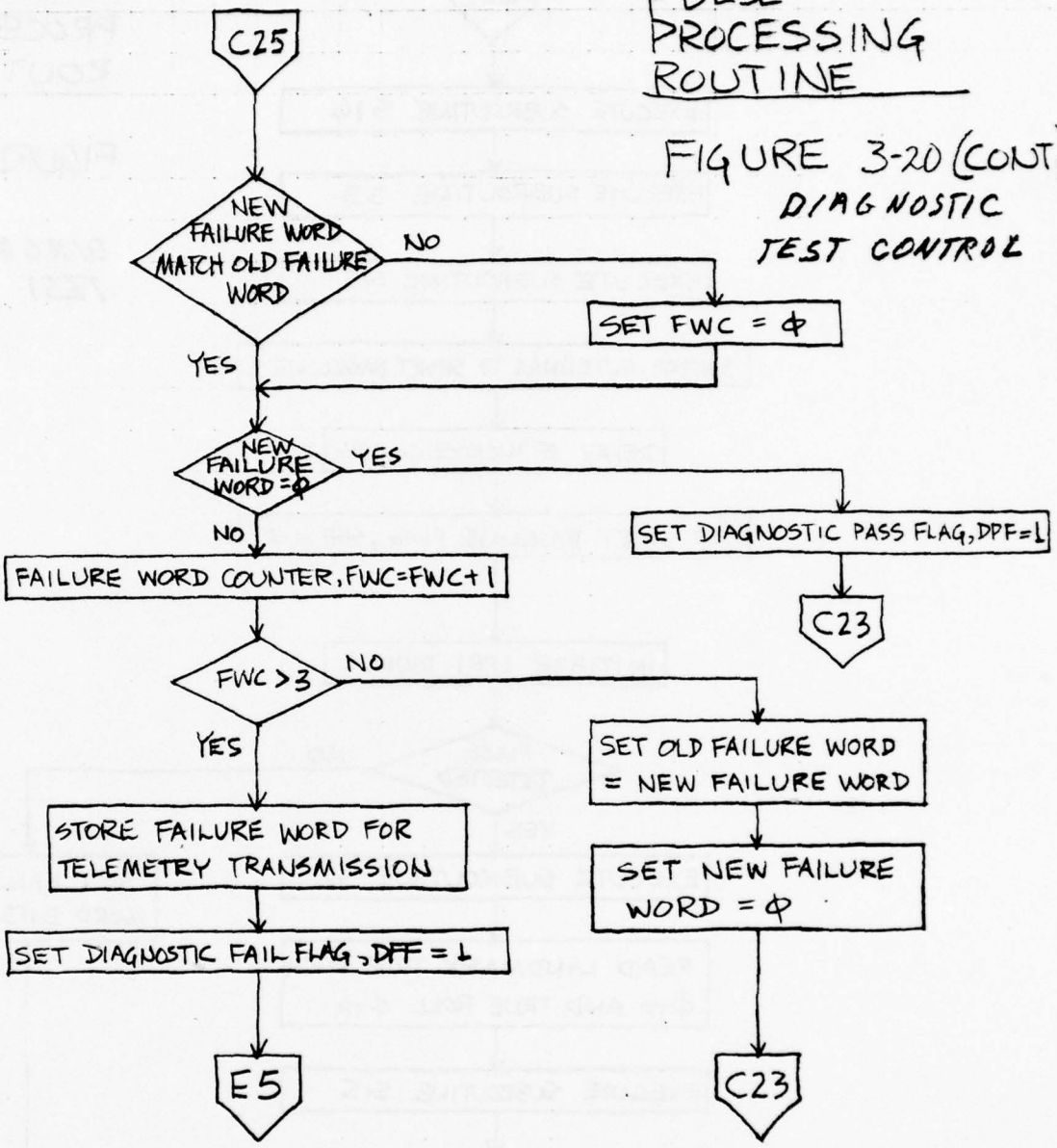
FIGURE 3-20(CONT.)

DIAGNOSTIC TEST CONTROL



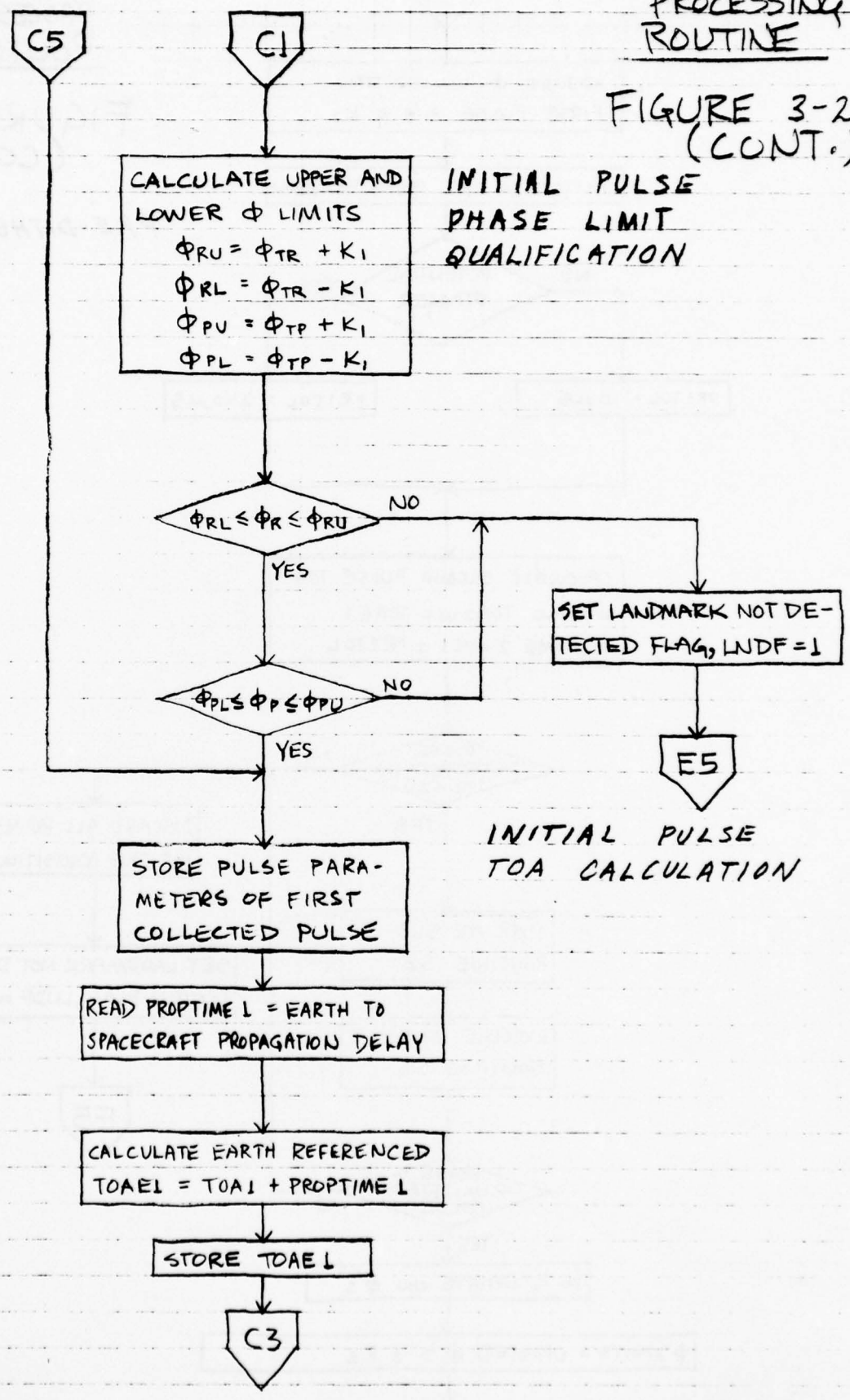
PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)
DIAGNOSTIC TEST CONTROL



PULSE PROCESSING ROUTINE

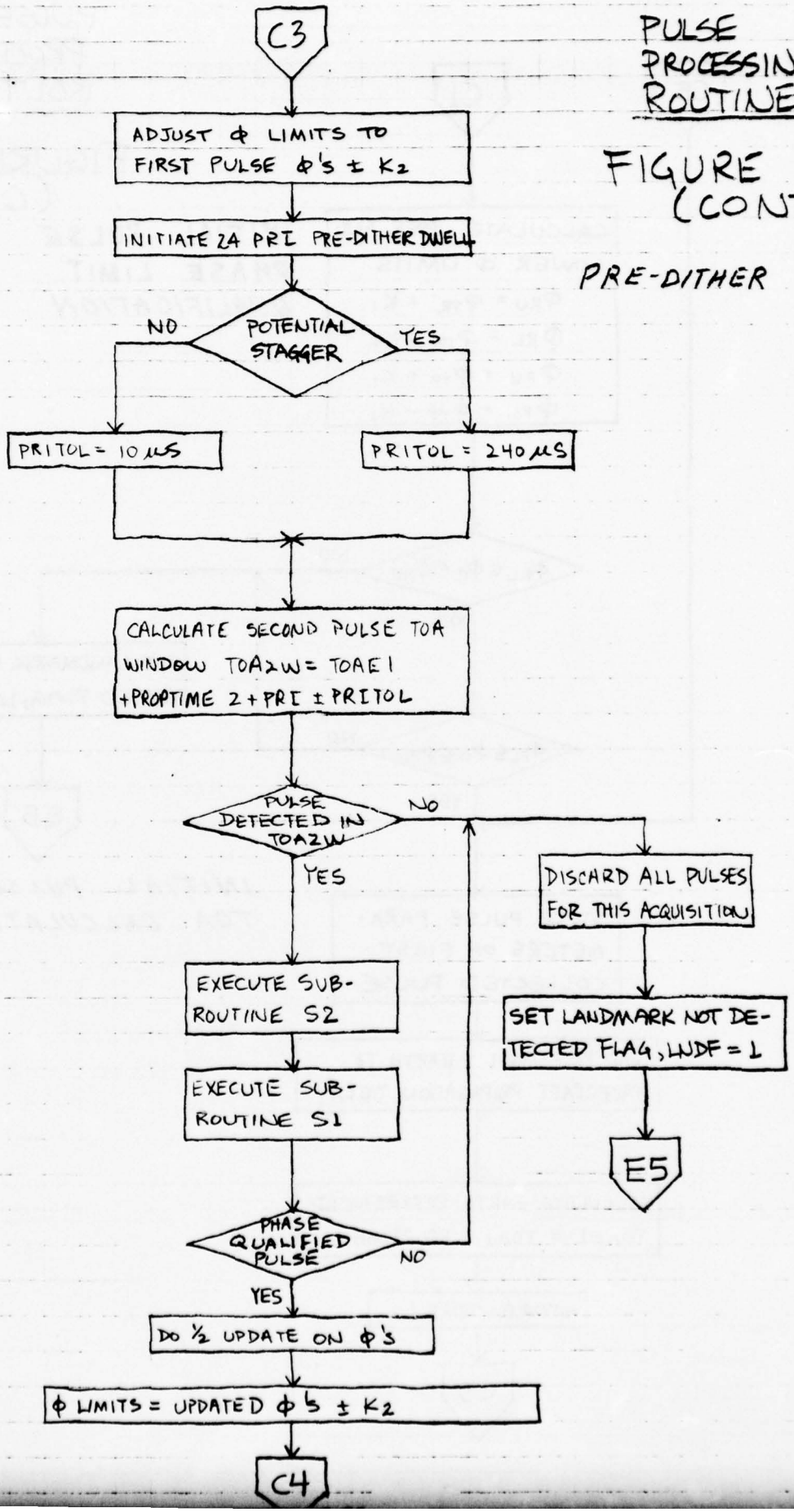
FIGURE 3-20 (CONT.)



PULSE PROCESSING ROUTINE

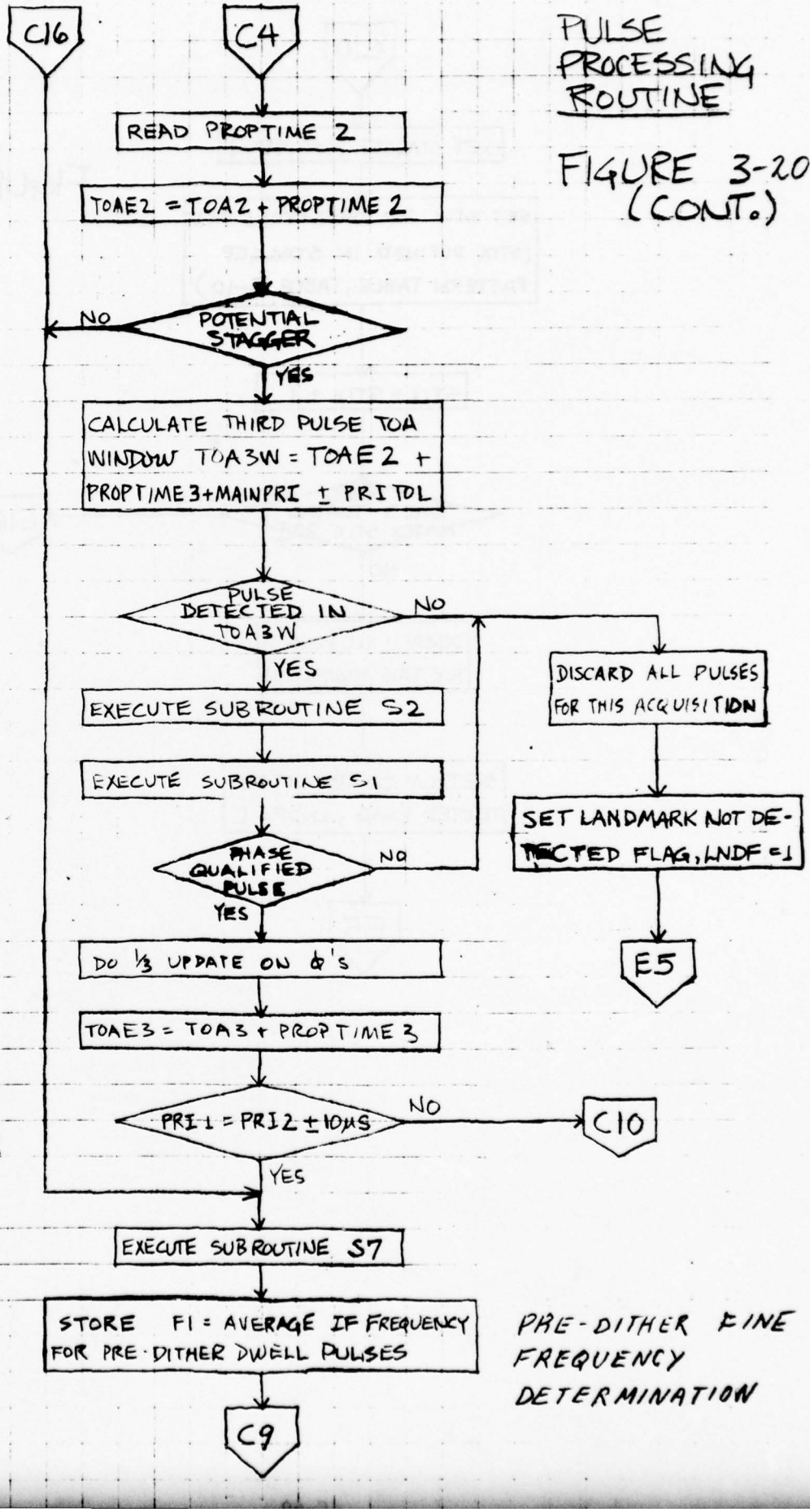
FIGURE 3-20 (CONT.)

PRE-DITHER



PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)



DETERMINATION OF STAGGER OR STABLE PRI

PRE-DITHER FINE FREQUENCY DETERMINATION

PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)

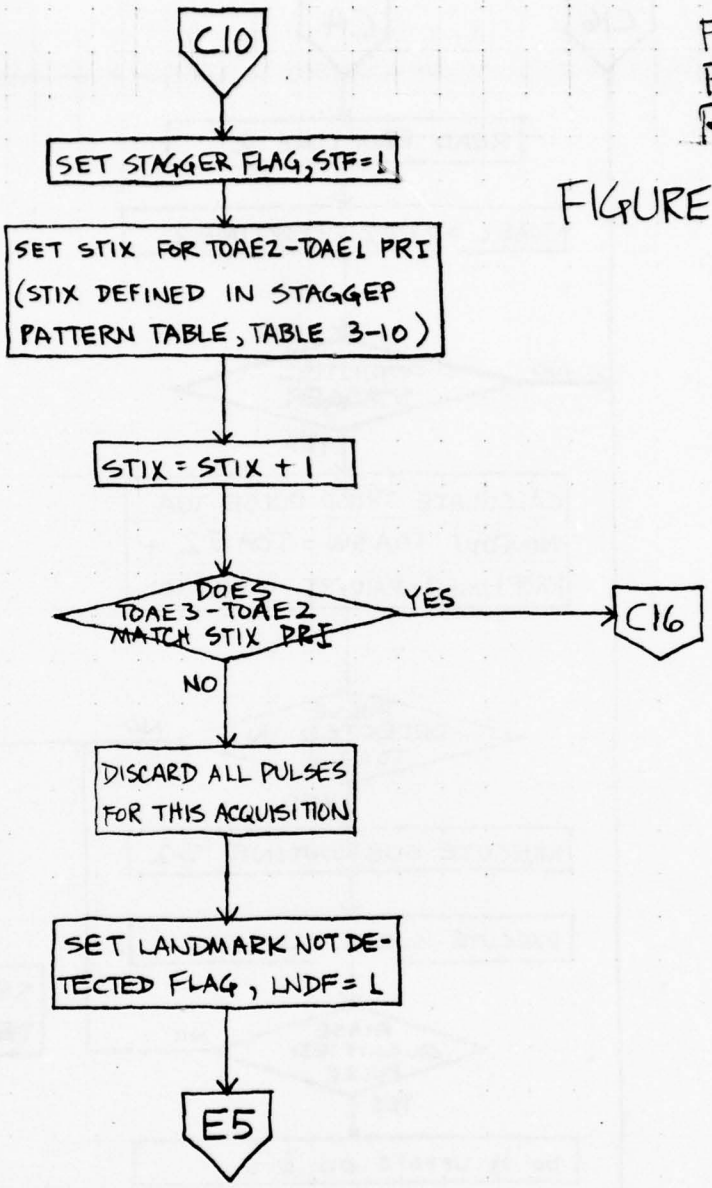


Table 3-10

STAGGER PATTERN TABLE

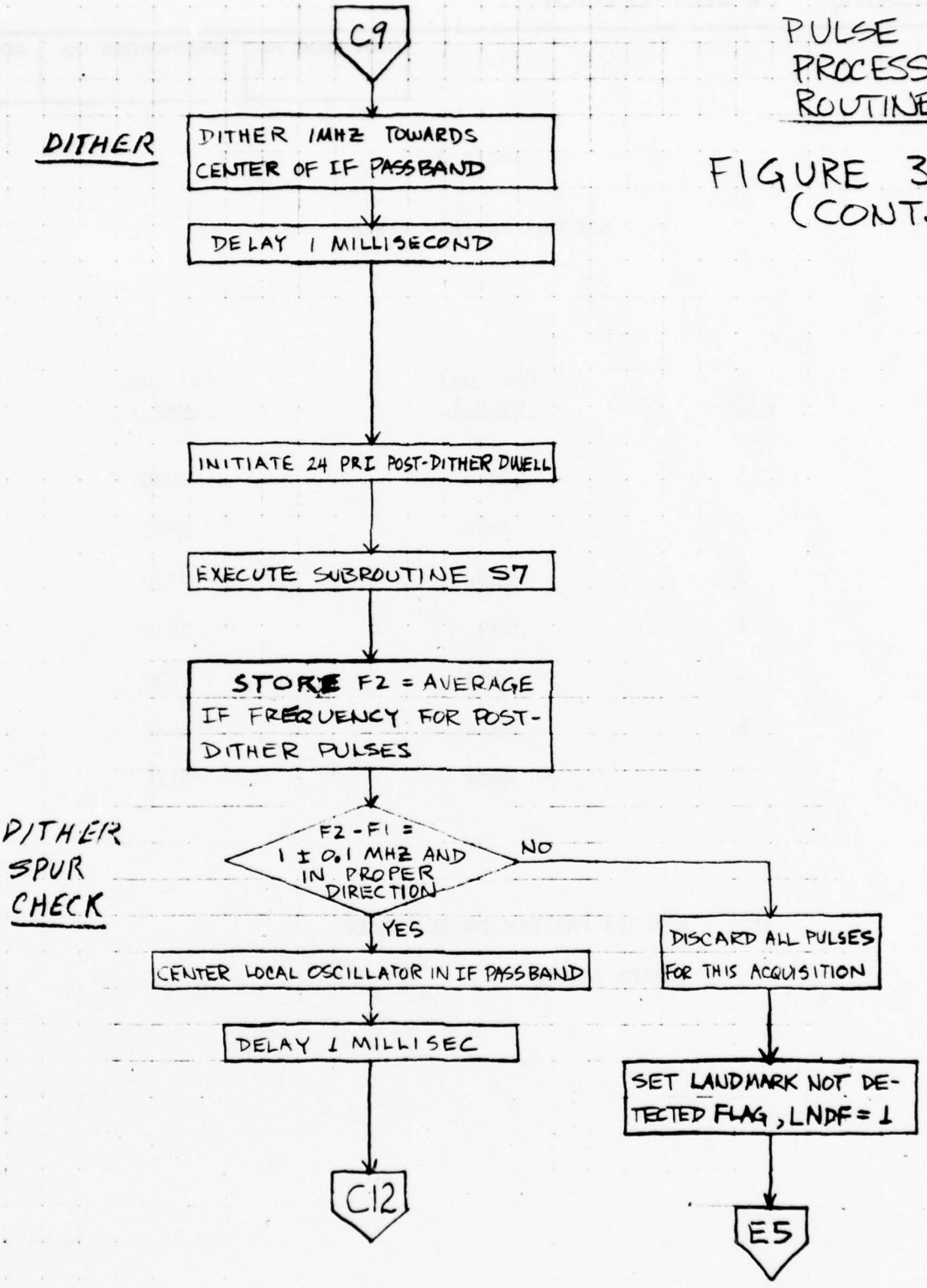
STIX	PRI (μs) Code 1	PRI (μs) Code 2
1	3040	3080
2	2800	2840
3	3280	3320
4	2896	2936
5	3184	3224
6	2992	3032
7	3088	3128

STIX = STAGGER PATTERN INDEX NUMBER

(WRAPS AROUND > 7)

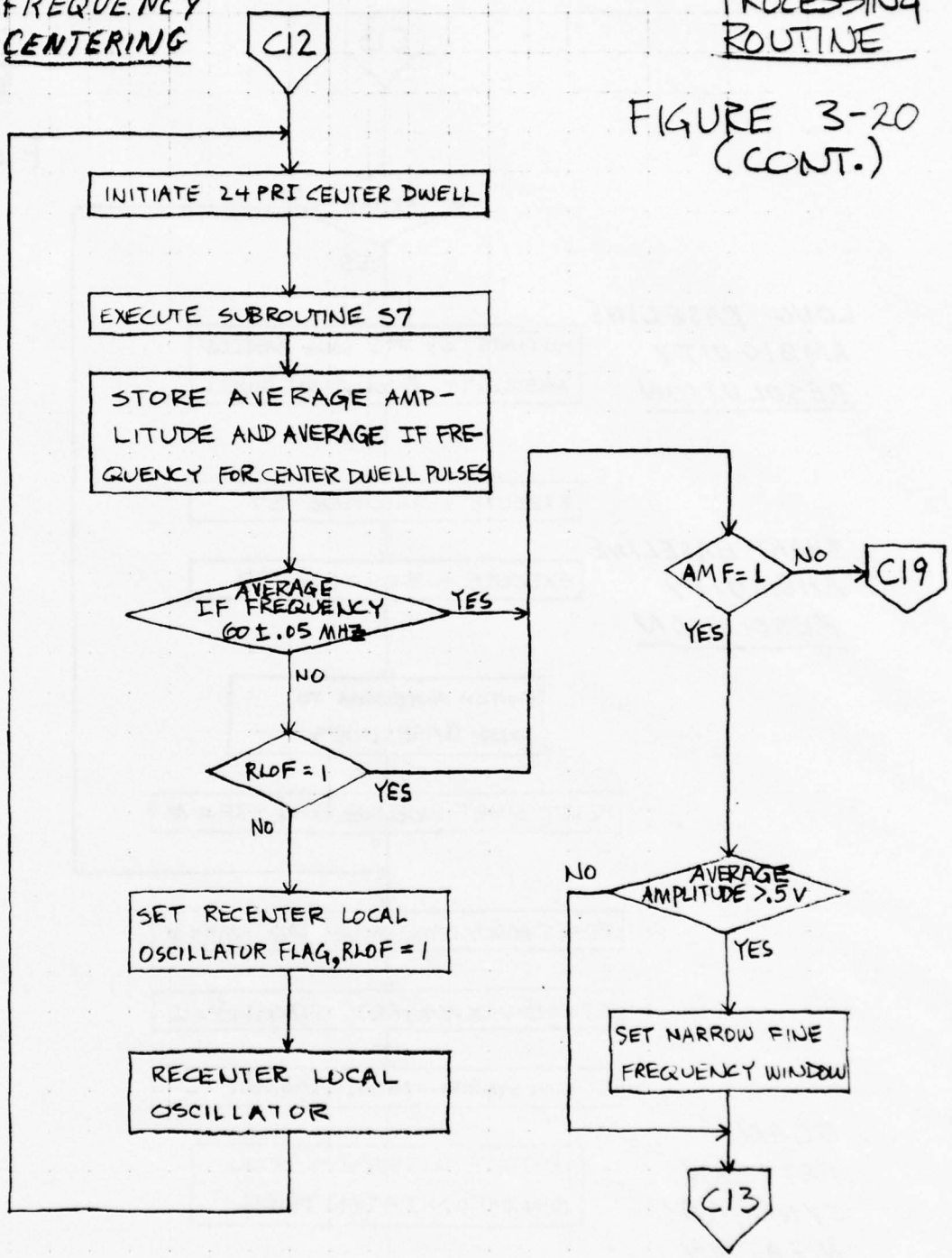
PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)



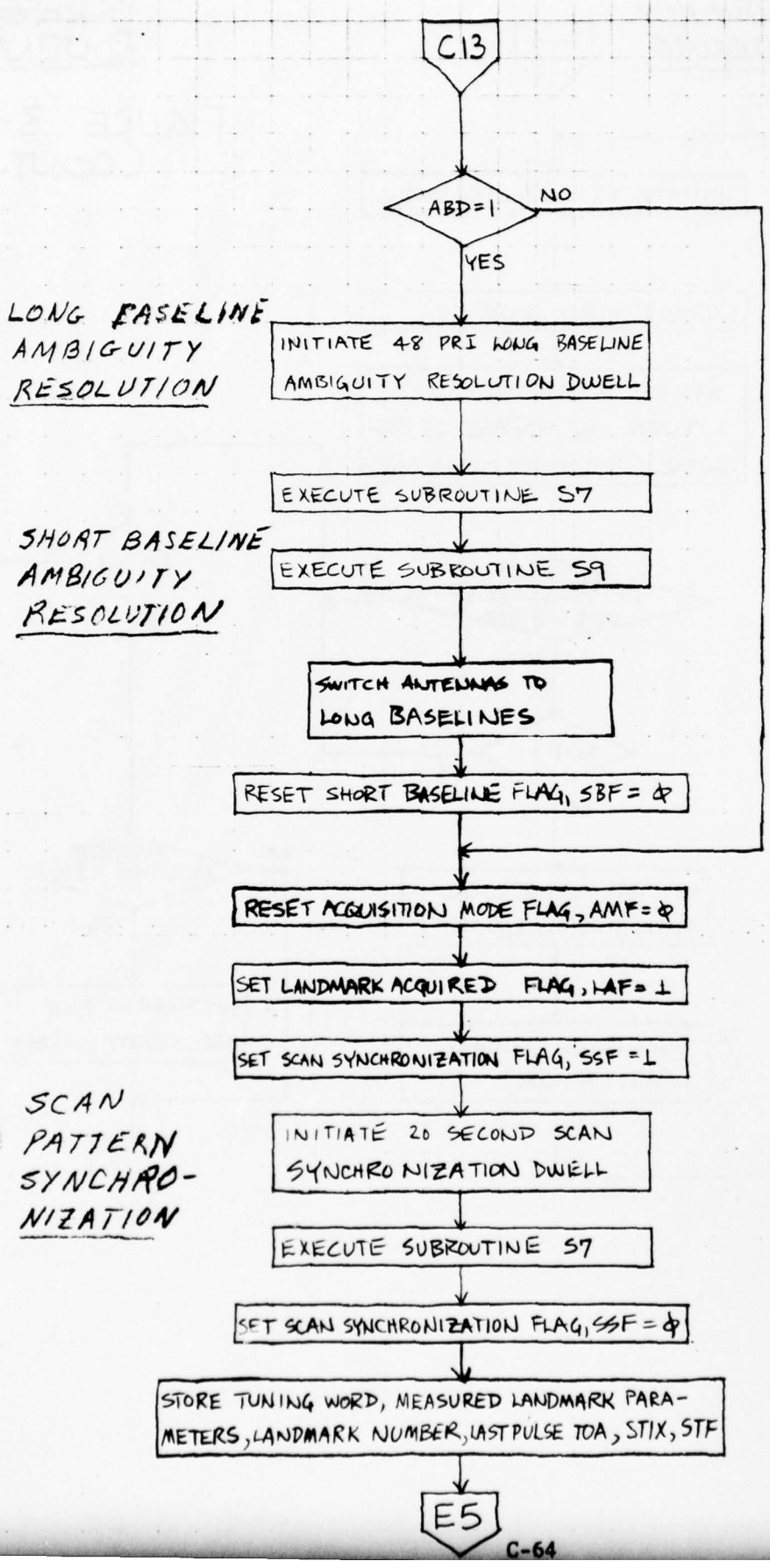
PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)



PULSE PROCESSING ROUTINE

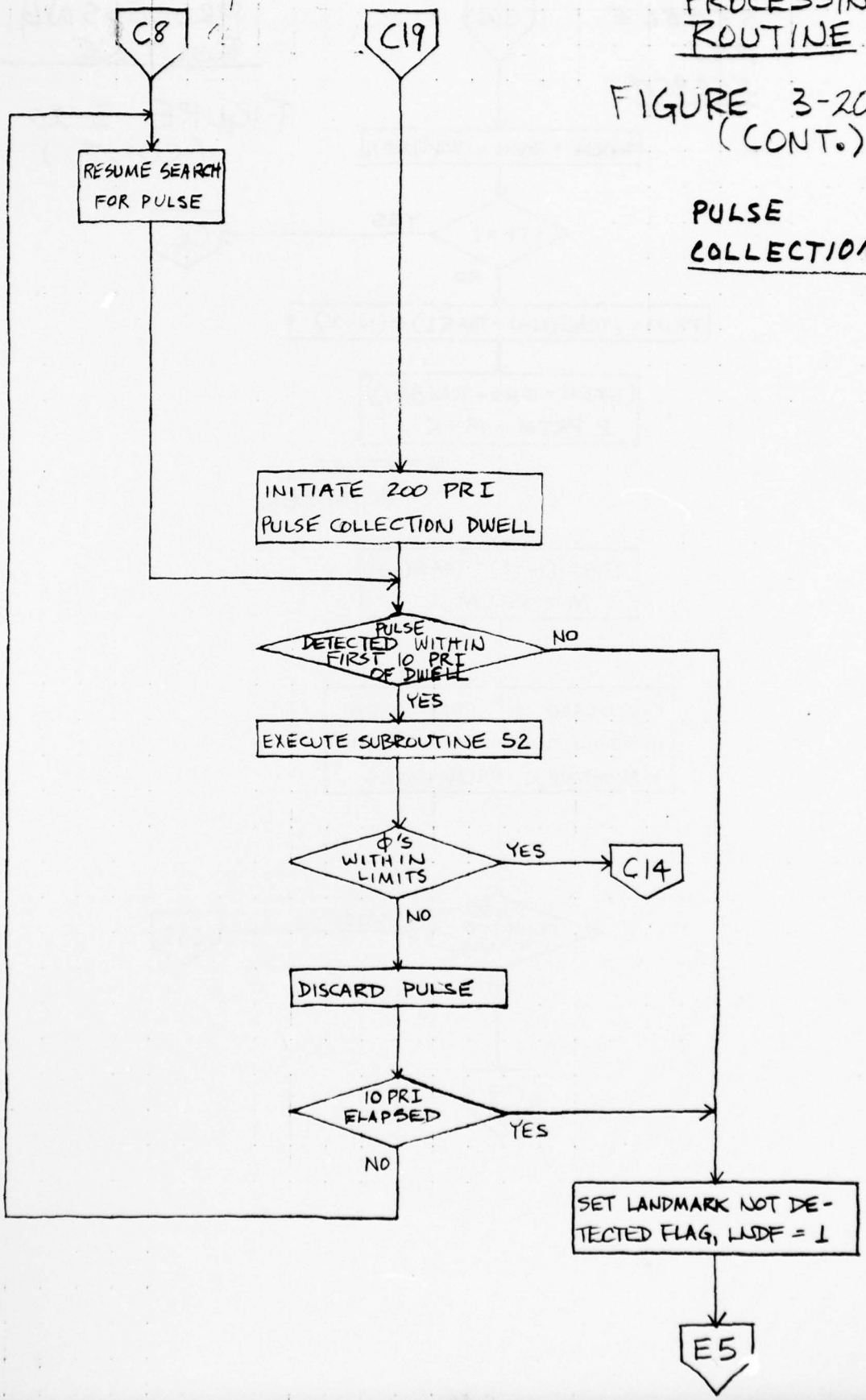
FIGURE 3-20 (CONT.)



PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)

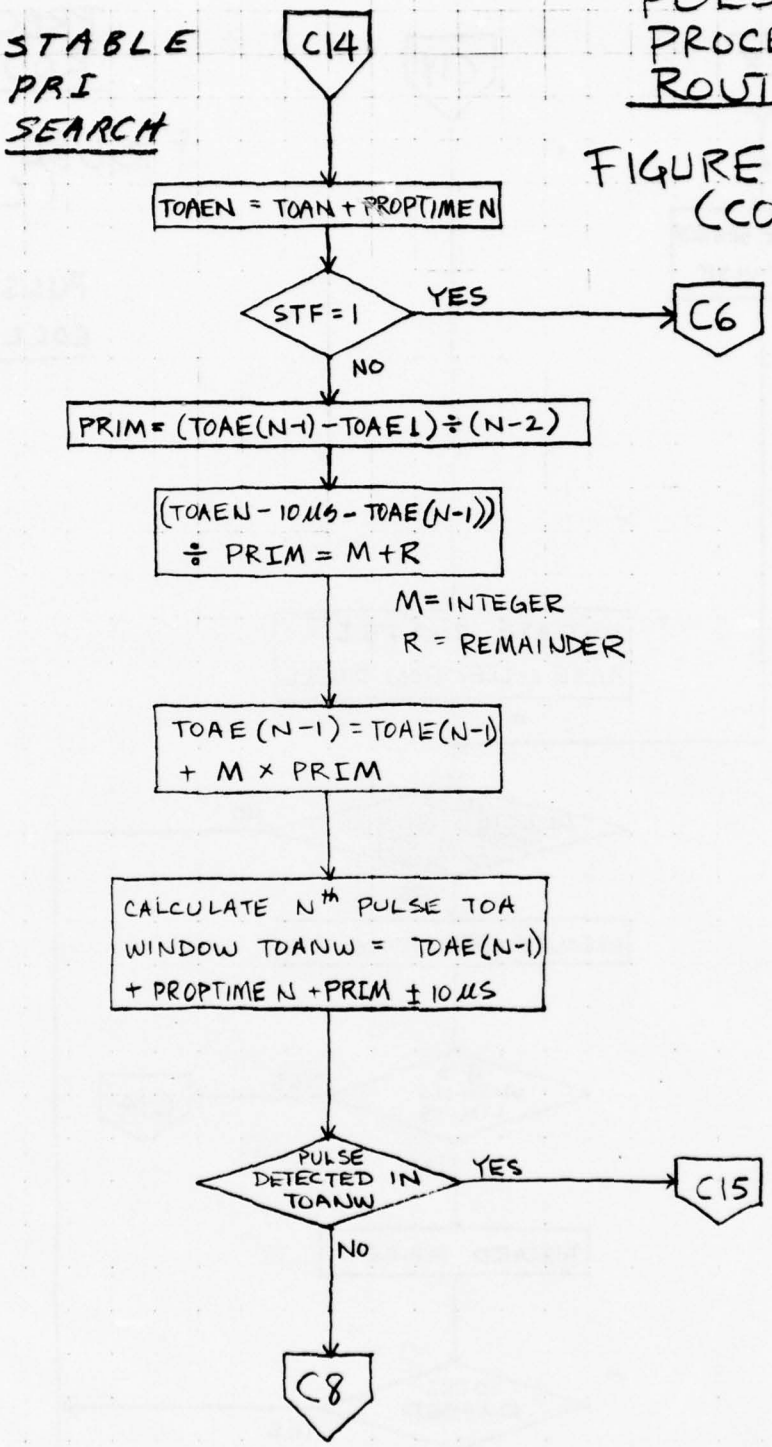
PULSE COLLECTION



PULSE PROCESSING ROUTINE

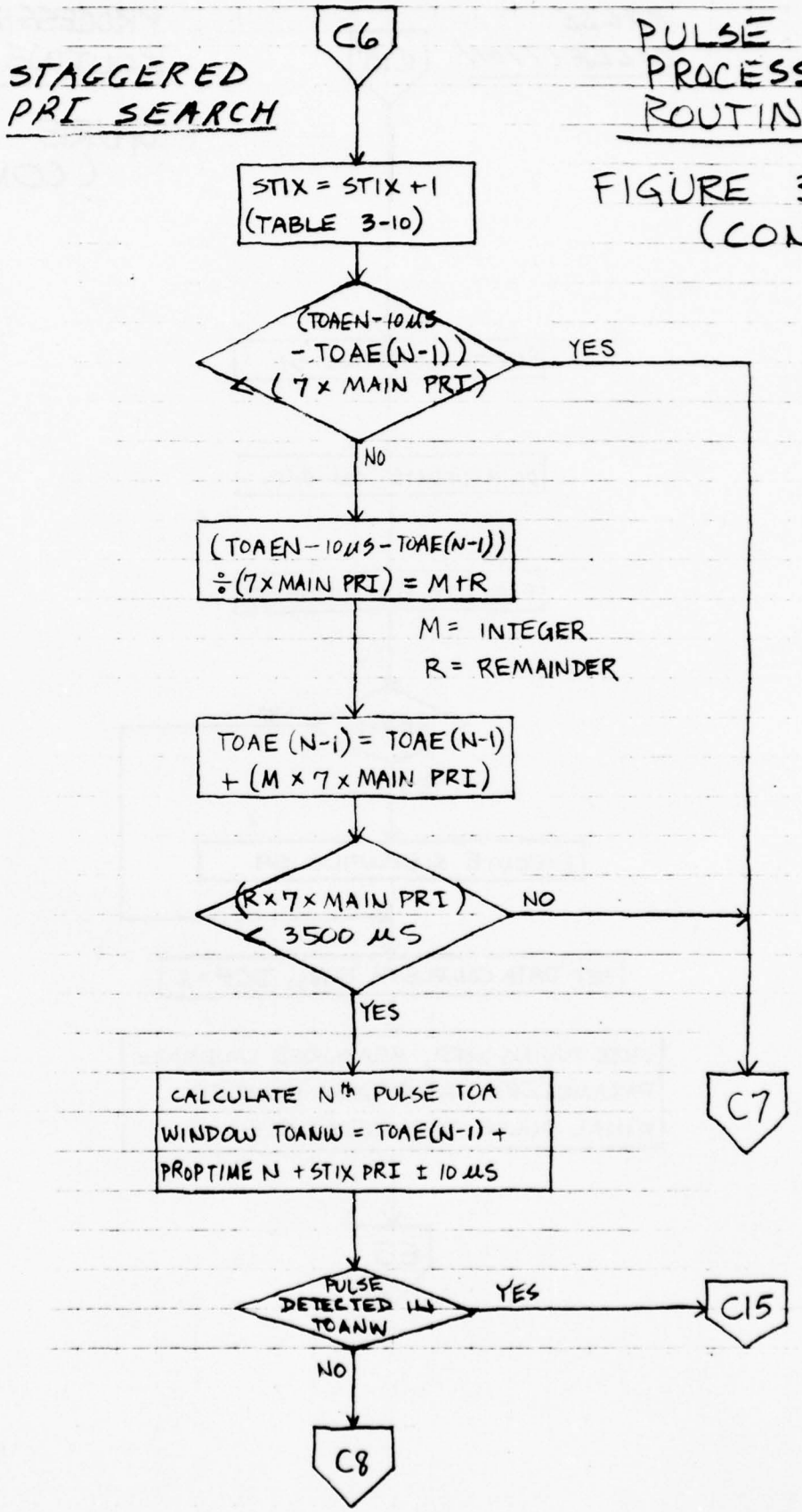
FIGURE 3-20 (CONT.)

STABLE PRI SEARCH



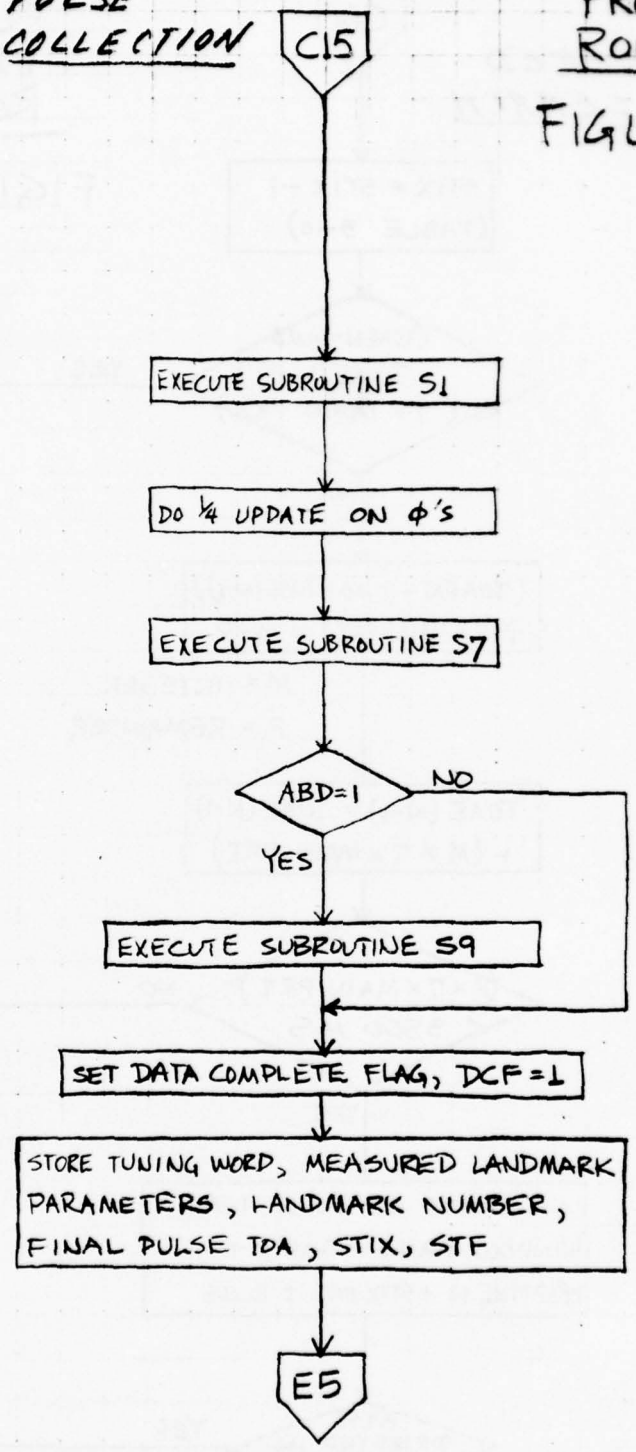
PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)



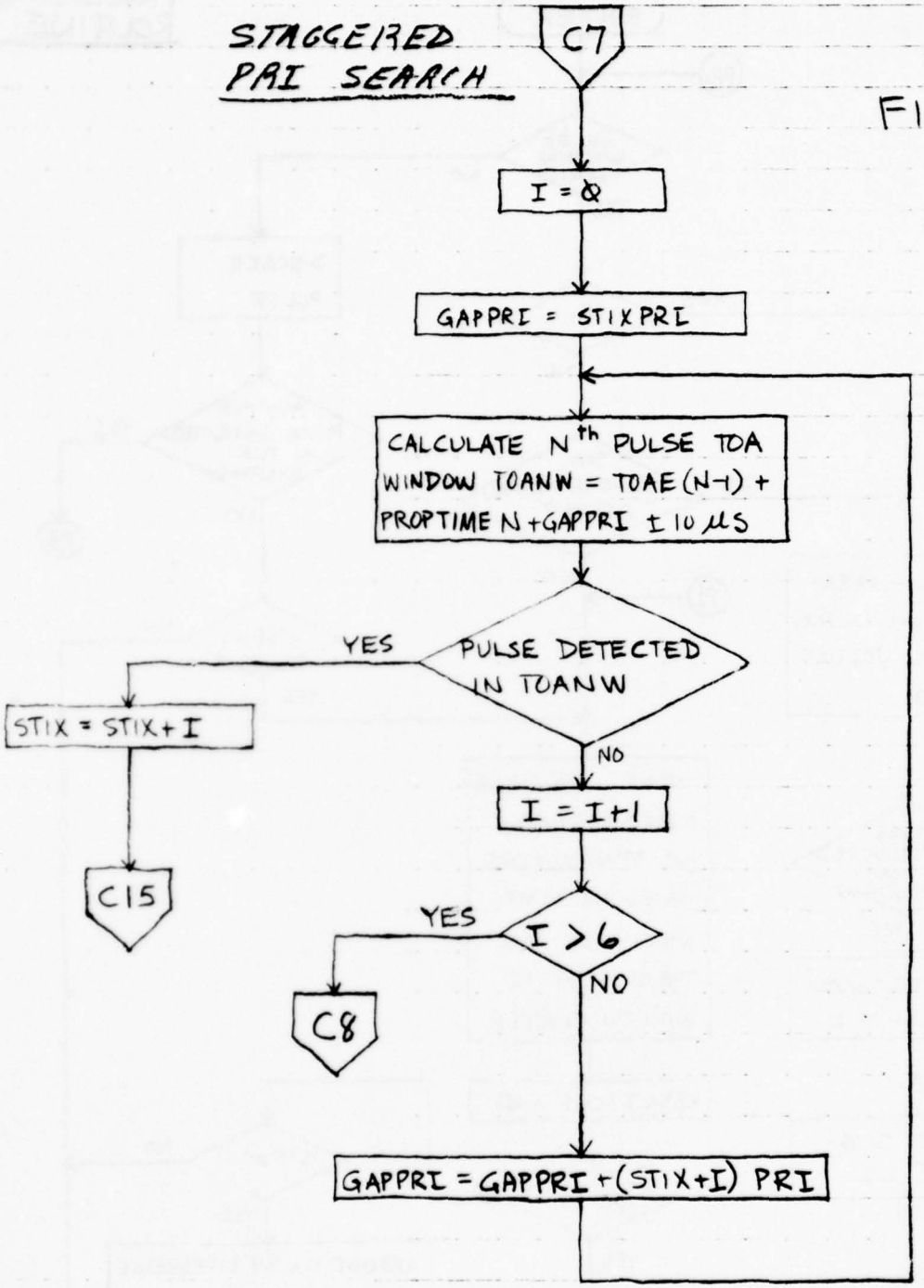
PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)



PULSE PROCESSING ROUTINE

FIGURE 3-20 (CONT.)



PULSE PROCESSING ROUTINE

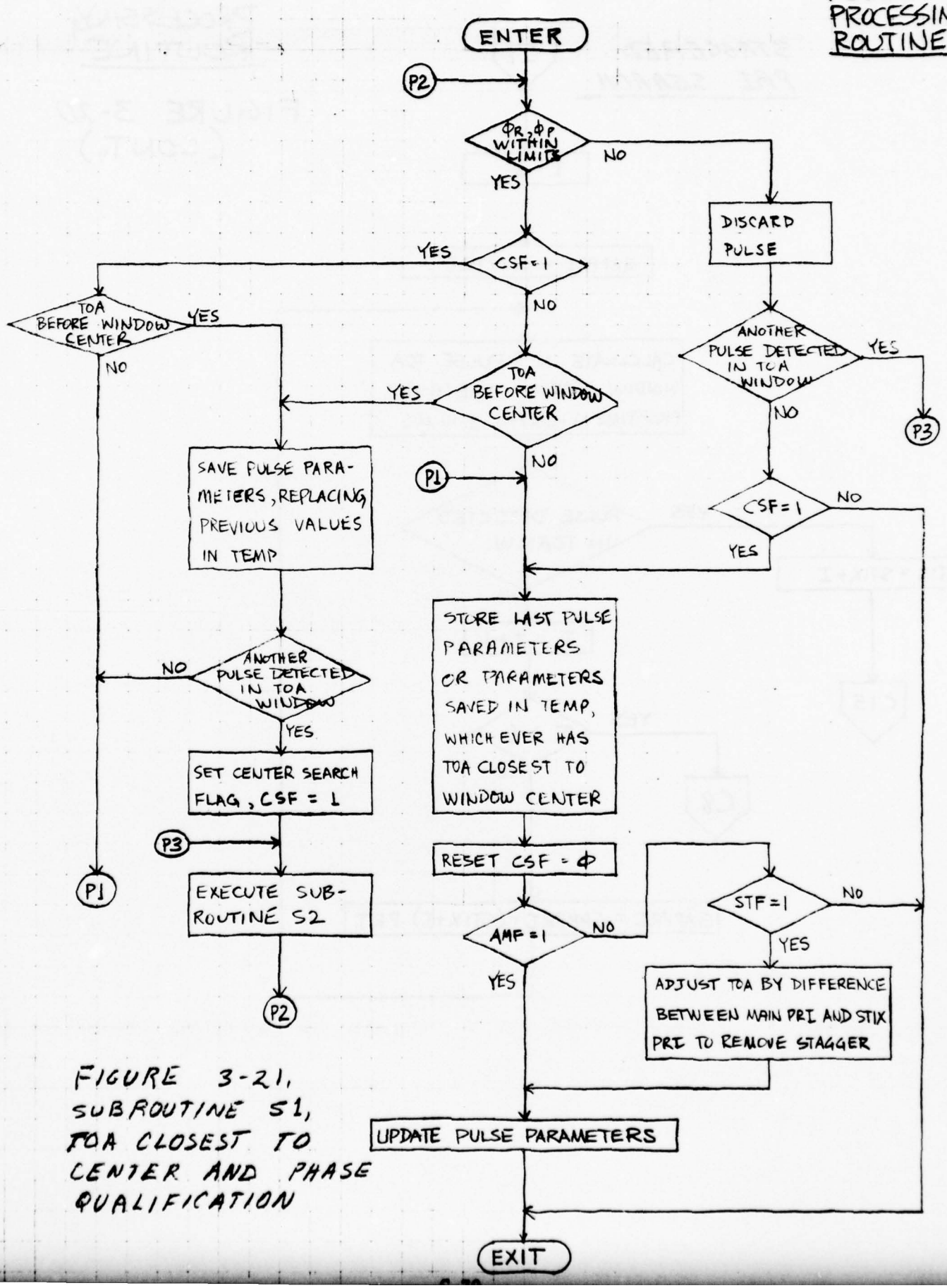


FIGURE 3-21, SUBROUTINE S1, TOA CLOSEST TO CENTER AND PHASE QUALIFICATION

PULSE PROCESSING ROUTINE

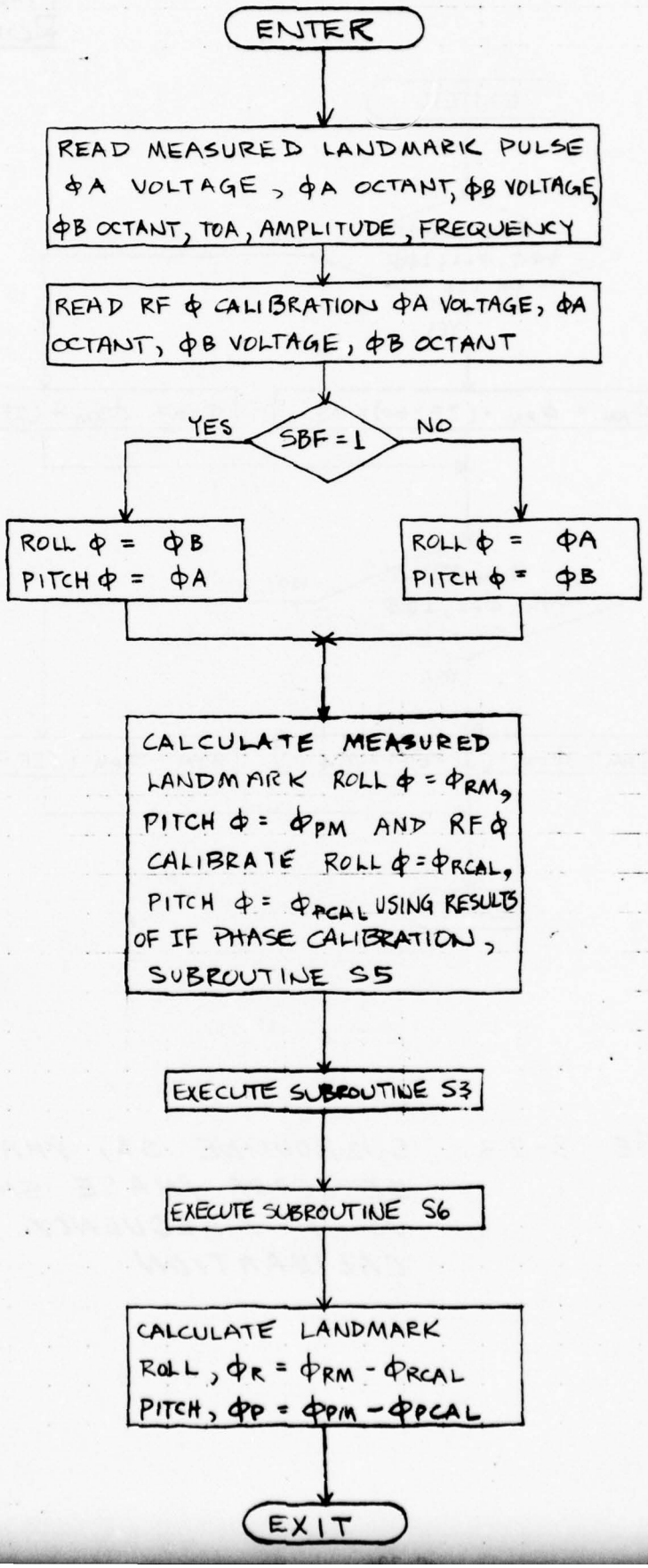


FIGURE 3-22 SUBROUTINE S2, READ PULSE PARAMETERS

PULSE PROCESSING ROUTINE

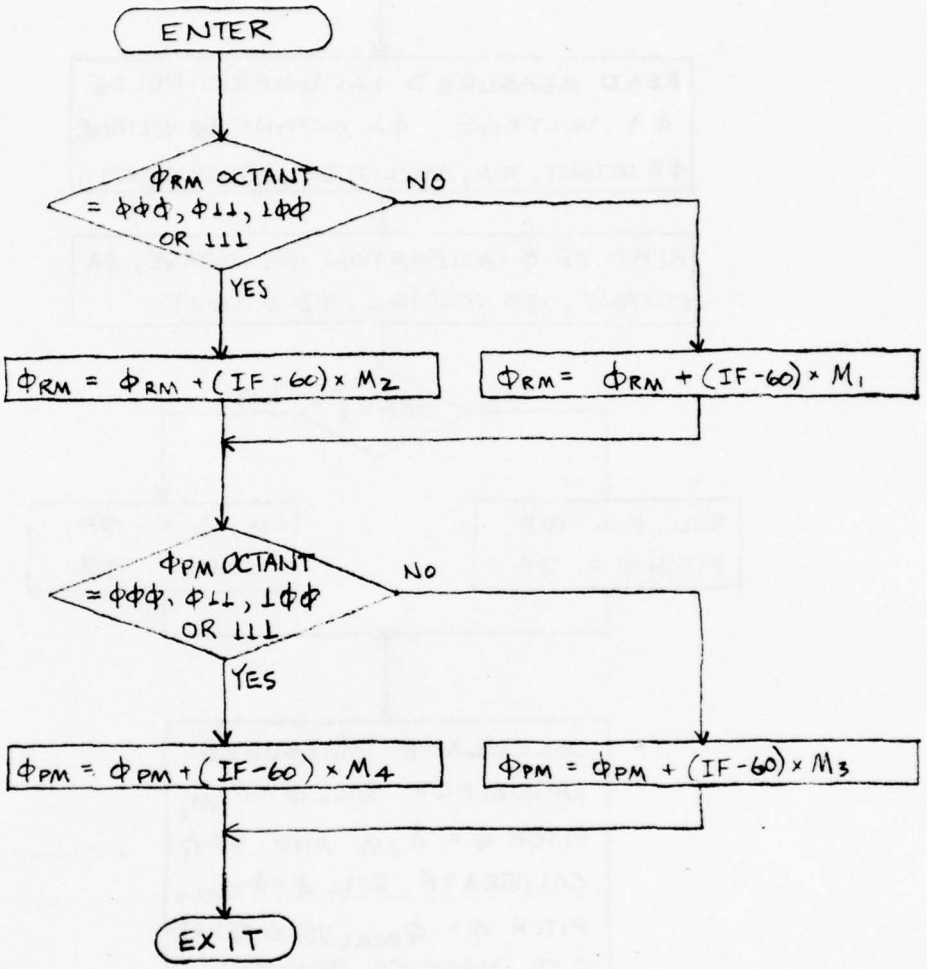


FIGURE 3-23. SUBROUTINE 53, PHASE DETECTOR PHASE SHIFT VS IF FREQUENCY CALIBRATION

PULSE PROCESSING ROUTINE

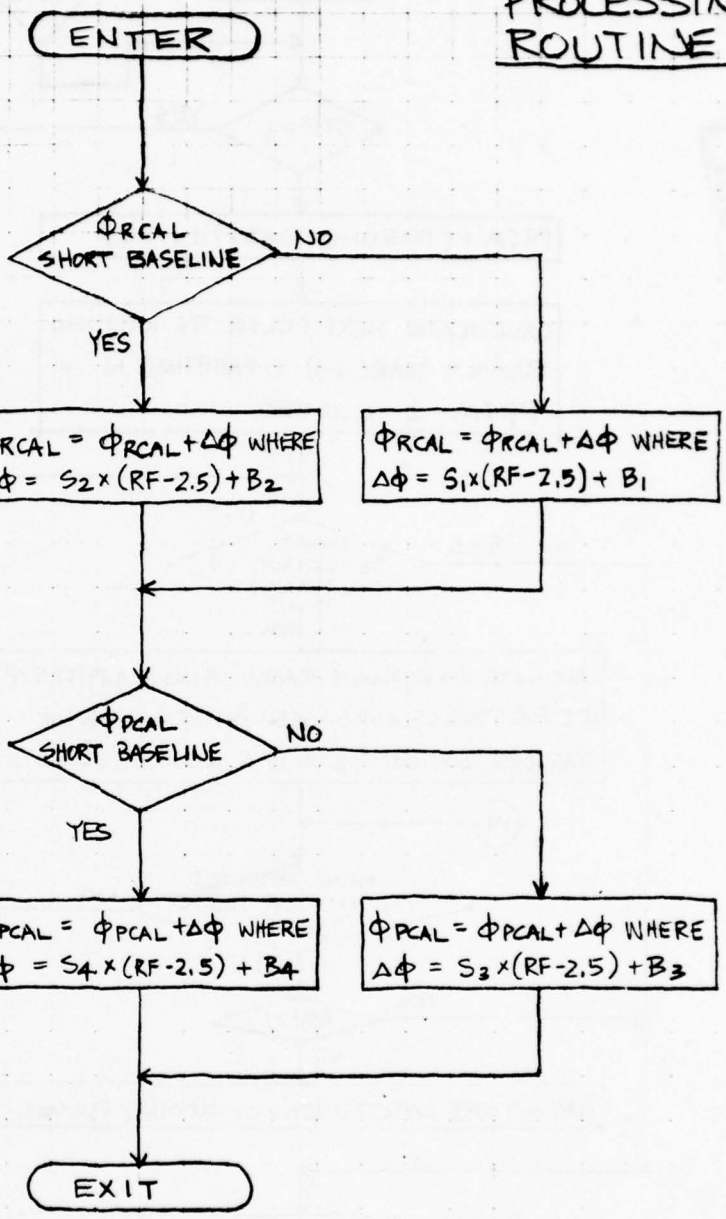


FIGURE 3-24. SUBROUTINE S6, RF CALIBRATION

PULSE PROCESSING ROUTINE

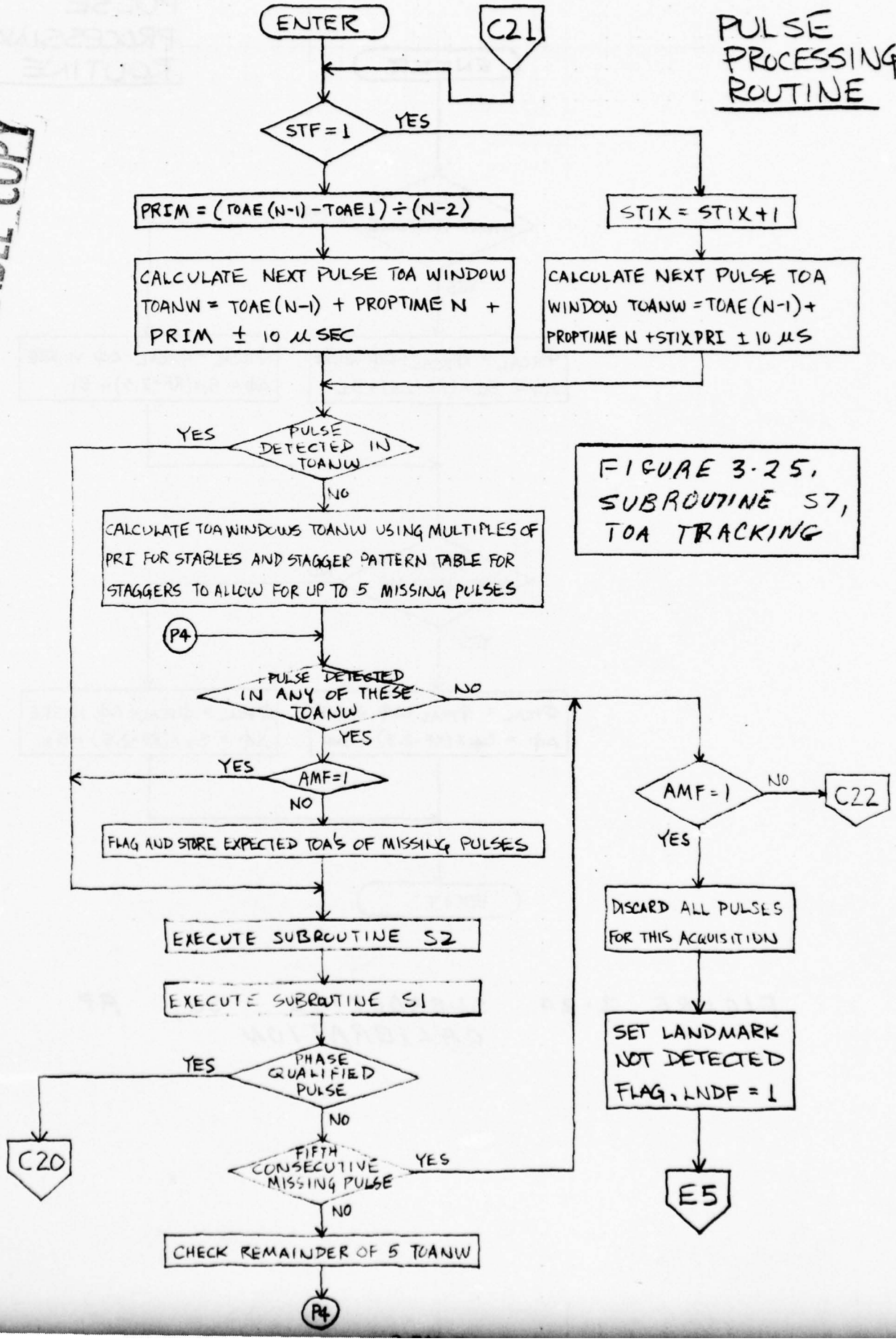


FIGURE 3-25. SUBROUTINE S7, TOA TRACKING

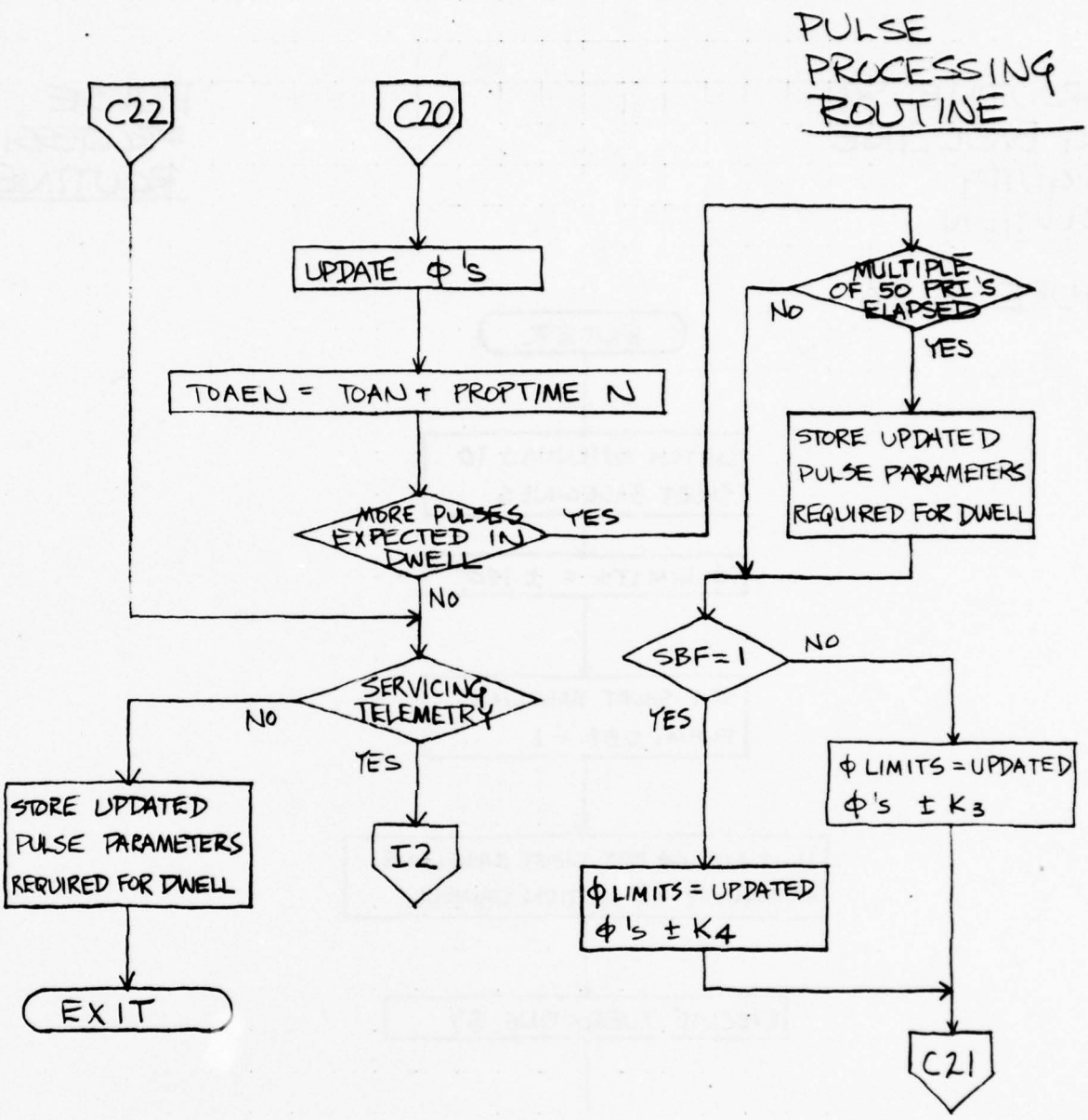


FIGURE 3-25 (CONTINUED). SUBROUTINE 57, TOA TRACKING

SUBROUTINE S9,
SHORT BASELINE
AMBIGUITY
RESOLUTION

PULSE
PROCESSING
ROUTINE

FIGURE 3-26

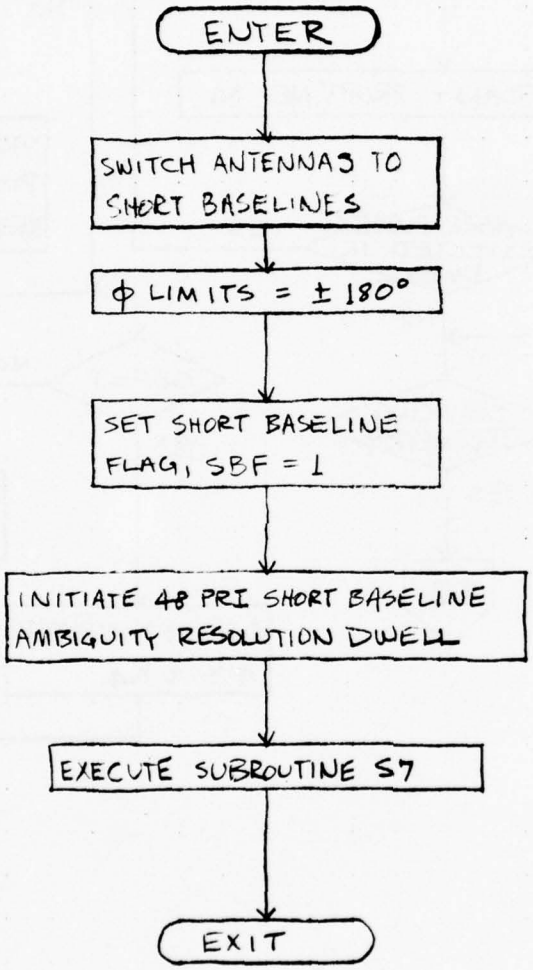


FIGURE 3-26. SUBROUTINE S9, SHORT BASELINE AMBIGUITY RESOLUTION

3.2.1.2.2 Inputs. The Pulse Processing Routine or one of its called subroutines shall receive the following inputs:

a. Monopulse encoded data. For each RF pulse detected by the ILT/PCU, the following parameters shall be measured and stored in memory:

1. Pulse time-of-arrival

2. Signal amplitude

3. Fine RF voltage

4. Phase A voltage (landmark)

5. Phase A octant (landmark)

6. Phase B voltage (landmark)

7. Phase B octant (landmark)

8. Phase A voltage (calibration signal)

9. Phase A octant (calibration signal)

10. Phase B voltage (calibration signal)

11. Phase B octant (calibration signal)

b. Landmark scheduler descriptor data. For each landmark selected by the Landmark Scheduler Routine, the Pulse Processing Routine shall read from memory the following data:

1. Landmark roll phase (long baseline)

2. Landmark roll phase (short baseline)

3. Landmark roll pitch phase (long baseline)

4. Landmark pitch phase (short baseline)

5. Landmark line-of-sight propagation delay

6. Time until measurement

7. Landmark number for data collection

8. Landmark number for deletion

9. RF

10. PRI

11. Stagger

c. Flags and status indicators set by the Executive and Diagnostic Routines.

3.2.1.2.3 Processing. The Pulse Processing Routine, including its called subroutines, shall perform the following processing functions:

a. Initial pulse detection and processing. Upon receipt of a Landmark Scheduler Routine request for processing, the Pulse Processing Routine shall initially tune the local oscillator 60 MHz below the landmark frequency and dwell for one PRI. If a detection is made, the signal shall be phase qualified using landmark true phase if autonomous system operation (phase ambiguity resolution) is not designated via a telemetry input. Received TOA shall be stored and earth referenced TOA shall be calculated using earth to spacecraft propagation delay provided by the NADP.

b. Pre-dither processing. The dwell shall be extended 24 PRI's. Each detected pulse shall first be TOA qualified including verification that it is the pulse closest to TOA window center (Subroutine S1). Each pulse shall then be phase qualified and the landmark parameters updated on a monopulse basis.* If the landmark parameters indicate that the PRI may be staggered, the consistency of PRI between the first two PRI's shall be checked to determine if the stagger condition exists.

c. Dither Processing. The local oscillator shall be dithered 1 MHz in a direction such that the signal is shifted toward the center of the IF passband. Pulses shall be collected and qualified, and parameters shall be updated over a 24 PRI dwell. Correctness of the relative pre-dither and dither average fine frequencies shall be verified to eliminate spurious RF signal processing.

d. Frequency centering. The local oscillator shall be adjusted such that the signal is centered in the IF passband and a 24 PRI dwell initiated. Pulses shall be collected and qualified, and parameters shall be updated over the dwell. At the end of the dwell, the fine RF average shall be verified to be within 50 KHz of center frequency. The centering shall be repeated one time if necessary. At the conclusion of the centering procedure, if the average signal amplitude is greater than 0.5 volts, the narrow fine frequency window shall be activated.

* Monopulse parameter updating for this dwell and all other signal processing dwells shall be such that at the end of a dwell or other specified period of time within the dwell, updated parameter values represent the running parameter average during the dwell. Updated parameters shall include TOA, amplitude, frequency and two baseline phase angles.

e. Phase ambiguity resolution pulse collection. If phase ambiguity resolution is designated, a 48 PRI long baseline dwell followed by a 48 PRI short baseline dwell shall be executed, during which pulses will be collected and qualified, and parameters shall be updated. Averaged pulse parameters for this dwell shall be placed in memory where it will be available to the NADP.

NOTE: Initiation of the following pulse collection dwells marks termination of the acquisition mode of the Pulse Processing Routine.

f. Scan measurement pulse collection. Pulses for scan pattern recognition shall be collected, qualified, reduced, and stored during a 20 second dwell. Averaged pulse parameters for each 50 PRI segment of this dwell shall be placed in memory where they shall be available to the NADP.

g. Frequency recentering. The local oscillator shall be tuned to the frequency to which it was last tuned for processing of the same emitter, and a 24 PRI dwell shall be initiated. Pulses shall be collected and qualified and parameters shall be updated over the dwell. At the end of the dwell, the Fine RF average shall be verified to be within 50 KHz of center frequency. If centering is required, the centering shall be done and the 24 PRI dwell repeated one time to confirm centering.

h. Pulse collection for navigation filter inputs. A 200 PRI pulse collection dwell shall be initiated with a 10 PRI pulse detection dwell. If no phase qualified pulses are detected within the 10 PRI dwell, control shall be returned to the Executive Routine. If a phase qualified pulse is detected, the pulse shall be TOA qualified. TOA qualification shall be accomplished by comparing the received pulse TOA with expected pulse TOA projections based on the last previously received pulse from the train. Such TOA qualification shall be performed for pulse trains with either stable or staggered PRI's. Averaged pulse parameters for each 50 PRI segment of this dwell shall be placed in memory where they shall be available to the NADP.

i. Resolution verification. If phase ambiguity resolution is designated, a 48 PRI short baseline dwell shall be executed during which pulses will be collected and qualified and parameters shall be updated. Averaged pulse parameters for this dwell shall be placed in memory where they shall be available to the NADP.

3.2.1.2.4 Outputs. The Pulse Processing Routine or one if its called subroutines shall place in memory the following data:

a. Parameter measurements and data for each 50 PRI or otherwise specified group of pulses, for input to the NADP.

1. Pulse time-of-arrival, stagger removed.

2. Signal amplitude.

3. Signal RF. Fine RF shall be computed from the LO tuning word and the discriminator fine RF measurement.

4. Roll phase angle.

5. Pitch phase angle.

6. Landmark number.

7. Flags. The following flags shall be placed in memory with each 50 PRI parameter data group.

a) SBF. Short Baseline Flag. Parameter data collected with short baseline antenna configuration.

b) DCF. Data Complete Flag. Parameter data collection task assigned to RF Signal Processing and Executive Program by Landmark Scheduler Routine is complete.

c) LNDF. Landmark Not Detected Flag. Acquisition sequence could not be completed or insufficient pulses for landmark update.

d) SSF. Scan Synchronization Flag. Parameter data collected for purpose of scan synchronization.

e) LAF. Landmark Acquired Flag. Completed acquisition sequence. (During the acquisition sequence, when this flag is set, no parameter measurement data shall be placed in memory for processing by the NADP).

b. Parameter measurements and data for input to the telemetry buffer. Format TBD.

c. Tuning and control commands to the ILT/PCU.

d. Flags and status indicators.

3.2.1.3 Diagnostic Routine. The Diagnostic Routine, including its called subroutines shall perform hardware control and data analysis to accomplish internal self-test of the system. Within system configuration constraints, the Diagnostic Routine shall maximize failure isolation and report the results of the self-test. The Diagnostic Routine shall perform the following functions:

a. Checksum memory testing.

b. IF calibrator testing.

c. Channel testing.

d. RF phase calibrator testing.

e. Failure word determination and reporting.

3.2.1.3.1 Routine Functional Flow Diagram. The functional flow diagrams for the subroutines comprising the Diagnostic Routine are shown in
Figures 3-27 through 3-29.

3.2.1.3.2 Inputs. The Diagnostic Routine shall receive encoded phase data in the IF calibration mode, the RF θ calibration mode and the normal (landmark data) mode.

3.2.1.3.3 Processing. The Diagnostic Routine shall perform the following processing functions:

a. Checksum memory testing. The Checksum Memory Test Subroutine, S16, shall perform a checksum on individual blocks of memory of less than 1024 words to determine if a change or failure has occurred in program memory. The subroutine shall compute a checksum for each memory block and compare the checksum to a stored table of correct checksum results. A checksum error shall be flagged and the start address and member of words for the discrepant block shall be reported.

b. IF calibrator testing. The results of IF phase calibration, subroutine S5, (phase detector A and B measurements) shall be verified to be within a tolerance about an expected value.

c. Channel testing and RF phase calibrator testing. Phase detector A and B measurements shall be verified to be within a tolerance of expected values for both the RF phase calibration mode and the normal (landmark data) processing mode. Expected values will be specified in the format of Table 3-11 for the RF phase calibration mode. Expected values in the normal mode will be determined through a prior knowledge of landmark location.

d. Diagnostic Failure Word determination and reporting. Failures detected in IF calibrator testing, channel testing or RF phase calibrator testing shall be recorded in the Diagnostic Failure Word, defined in Table 3-12.

3.2.1.3.4 Outputs. The Diagnostic Routine shall place in memory the following data:

a. Diagnostic Failure Word. The Diagnostic Failure Word shall be maintained in memory in its updated state, available for telemetry downlink transmission.

b. Diagnostic fail flag. Upon occurrence of any diagnostic test failure, the diagnostic fail flag, DFF, shall be set, and shall be available in memory to the NADP.

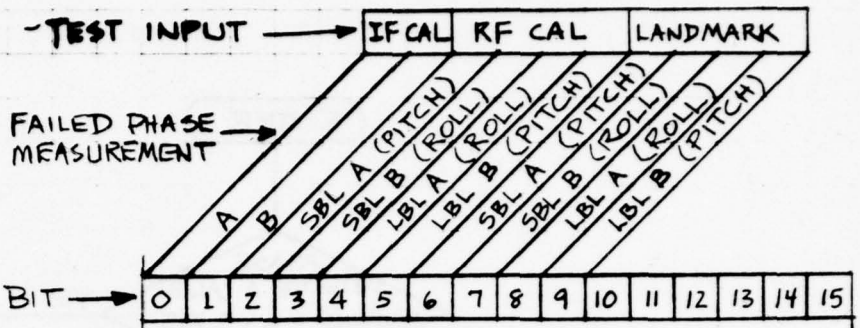
Table 3-11. Nominal RF

Calibration Versus Frequency

	Phase (Degrees)			
Frequency (MHz)	Long Baseline Roll	Long Baseline Pitch	Short Baseline Roll	Short Baseline Pitch
2500				
2600				
2700				
2800				
2900				

DIAGNOSTIC FAILURE WORD DEFINITION

TABLE 3-12



FAILURE WORD BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FAILURE																
IF CALIBRATOR — CHANNEL 1	1	Φ	Φ	Φ	Φ	Φ	Φ	Φ	Φ	Φ						
" " " 2	1	1	Φ	Φ	Φ	Φ	Φ	Φ	Φ	Φ						
" " " 3	Φ	1	Φ	Φ	Φ	Φ	Φ	Φ	Φ	Φ						
IF - CHANNEL 1	1	Φ	1	Φ	1	Φ	1	Φ	1	Φ						
" " 2	1	1	1	1	1	1	1	1	1	1						
" " 3	Φ	1	Φ	1	Φ	1	Φ	1	Φ	1						
RF - CHANNEL 2	Φ	Φ	1	Φ	1	Φ	1	Φ	1	Φ						
" " 1	Φ	Φ	1	1	1	1	1	1	1	1						
" " 3	Φ	Φ	Φ	1	Φ	1	Φ	1	Φ	1						
RF CALIBRATOR, CAL ONLY - LBL, ROLL	Φ	Φ	Φ	Φ	1	Φ	Φ	Φ	Φ	Φ						
" " " " SBL, PITCH	Φ	Φ	1	Φ	Φ	Φ	Φ	Φ	Φ	Φ						
" " " " CENTER	Φ	Φ	1	1	1	1	Φ	Φ	Φ	Φ						
" " " " LBL, PITCH	Φ	Φ	Φ	Φ	Φ	1	Φ	Φ	Φ	Φ						
" " " " SBL, ROLL	Φ	Φ	Φ	1	Φ	Φ	Φ	Φ	Φ	Φ						
ANTENNA OR RF CALIBRATOR, ANT ONLY - LBL, ROLL	Φ	Φ	Φ	Φ	Φ	Φ	Φ	Φ	1	Φ						
" " " " " " SBL, PITCH	Φ	Φ	Φ	Φ	Φ	Φ	1	Φ	Φ	Φ						
" " " " " " CENTER	Φ	Φ	Φ	Φ	Φ	Φ	1	1	1	1						
" " " " " " LBL, PITCH	Φ	Φ	Φ	Φ	Φ	Φ	Φ	Φ	Φ	1						
" " " " " " SBL, ROLL	Φ	Φ	Φ	Φ	Φ	Φ	Φ	1	Φ	Φ						
RF CALIBRATOR, CAL & ANT - LBL, ROLL	Φ	Φ	Φ	Φ	1	Φ	Φ	Φ	1	Φ						
" " " " SBL, PITCH	Φ	Φ	1	Φ	Φ	Φ	1	Φ	Φ	Φ						
" " " " CENTER	Φ	Φ	1	1	1	1	1	1	1	1						
" " " " LBL, PITCH	Φ	Φ	Φ	Φ	Φ	1	Φ	Φ	Φ	1						
" " " " SBL, ROLL	Φ	Φ	Φ	1	Φ	Φ	Φ	1	Φ	Φ						
NO SHORT BASELINE DETECTION	Φ	Φ	Φ	Φ	Φ	Φ	1	1	Φ	Φ						

DIAGNOSTIC ROUTINE

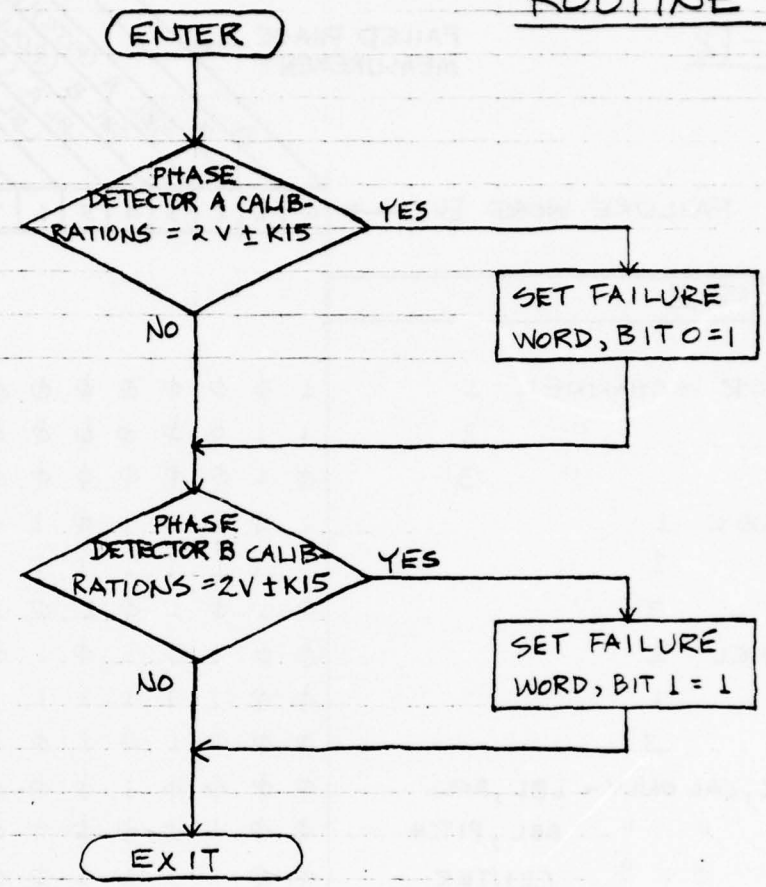


FIGURE 3-27. SUBROUTINE S14, IF CALIBRATOR TEST

FIGURE 3-28

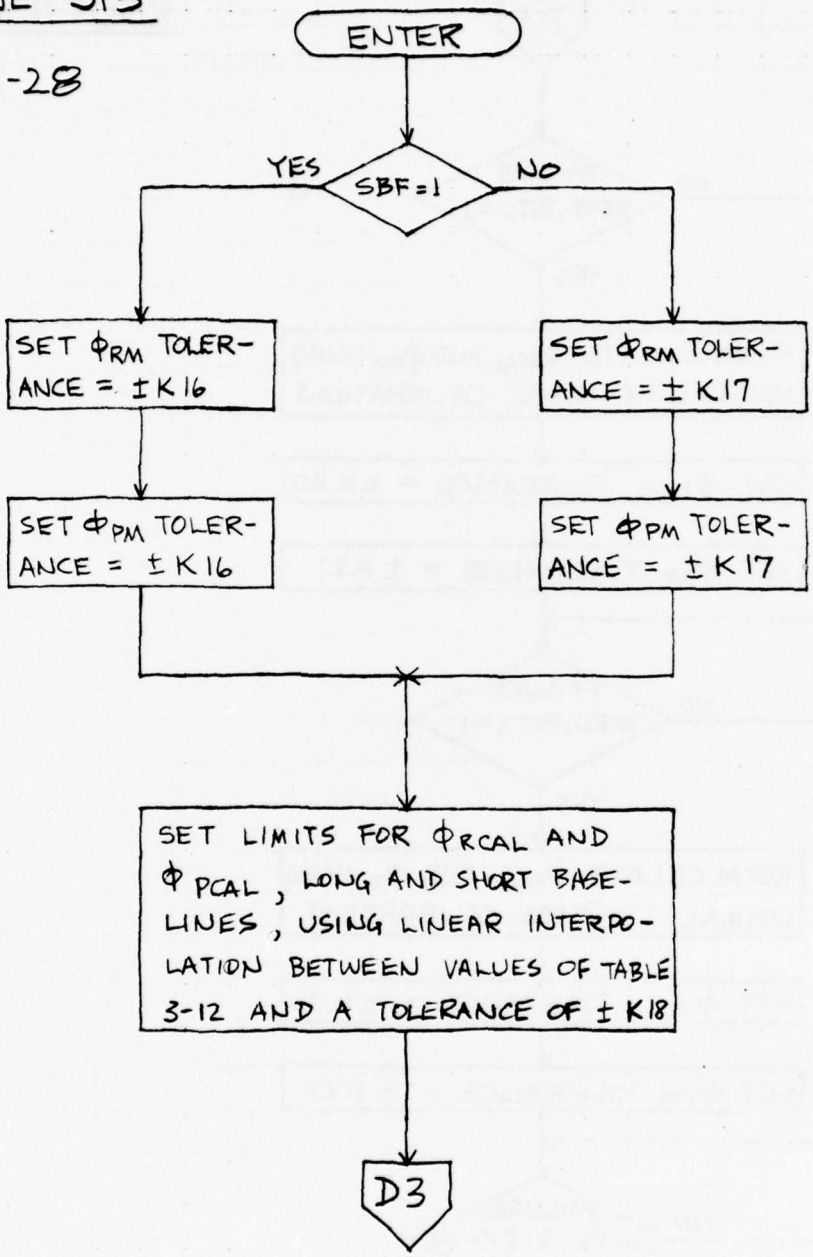
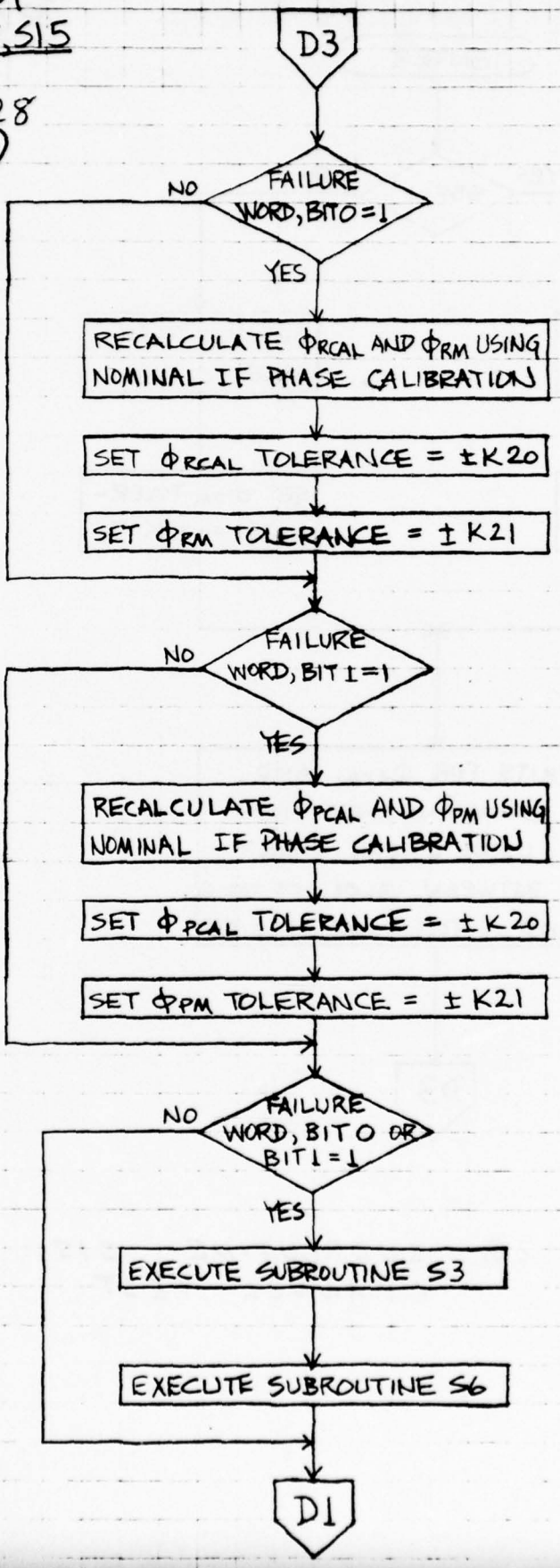


FIGURE 3-28. SUBROUTINE S15, CHANNEL TEST

CHANNEL TEST SUBROUTINE, S15

DIAGNOSTIC ROUTINE

FIGURE 3-28 (CONT.)



DIAGNOSTIC ROUTINE

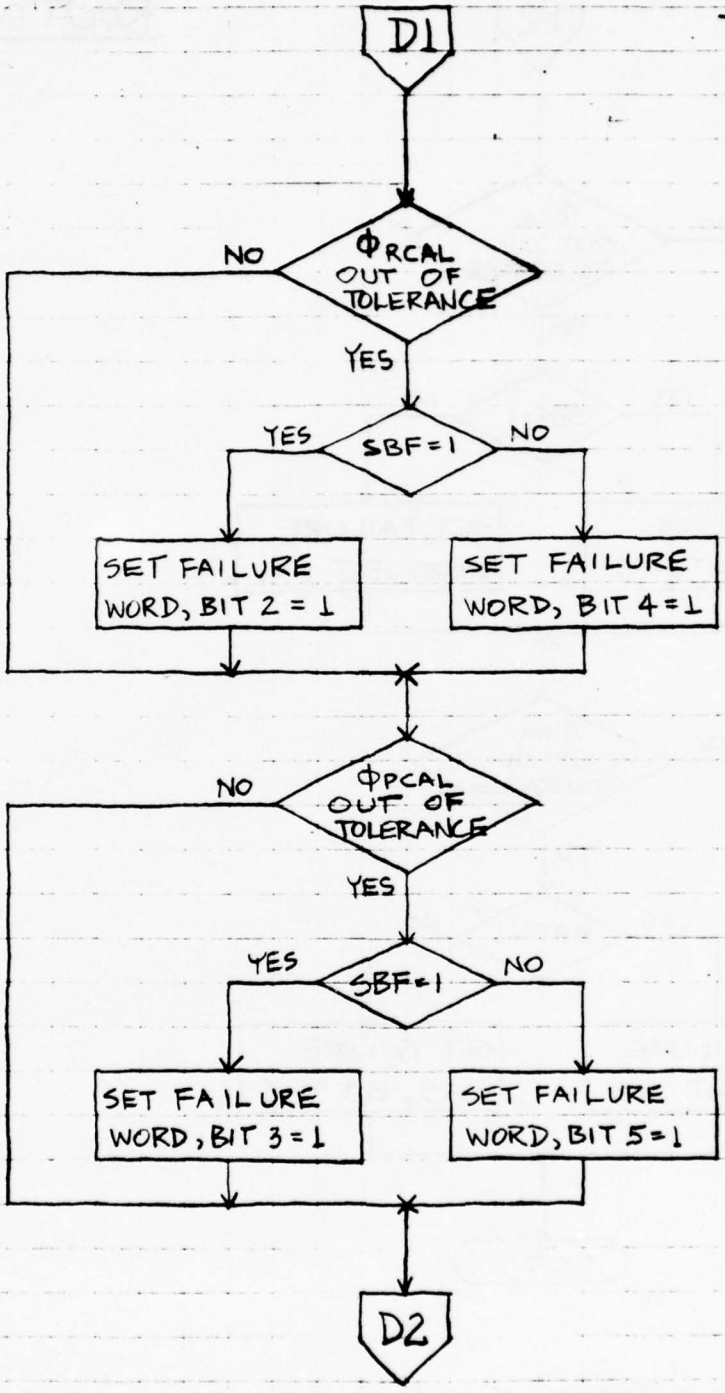


FIGURE 3-28 (CONTINUED), SUBROUTINE S15, CHANNEL TEST

CHANNEL TEST
SUBROUTINE, S15

DIAGNOSTIC
ROUTINE

FIGURE 3-28
(CONT.)

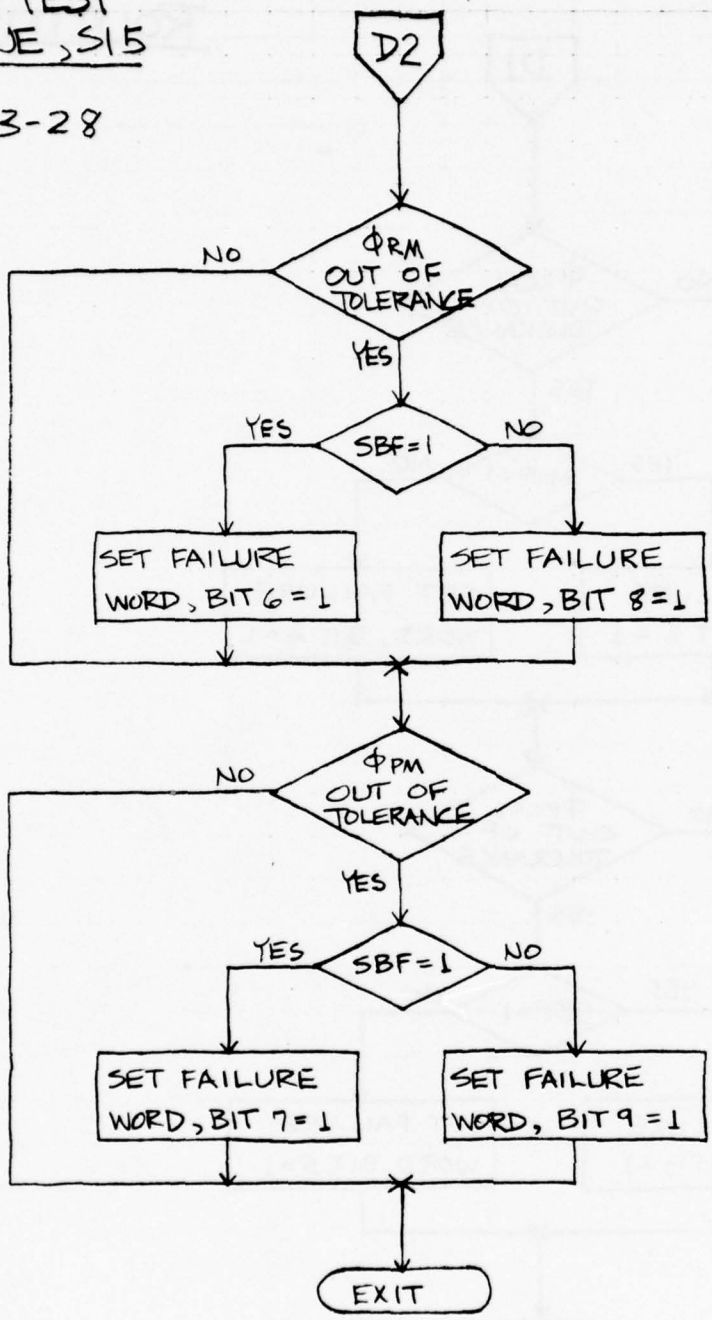


FIGURE 3-28 (CONTINUED) SUBROUTINE S15,
CHANNEL TEST

DIAGNOSTIC ROUTINE

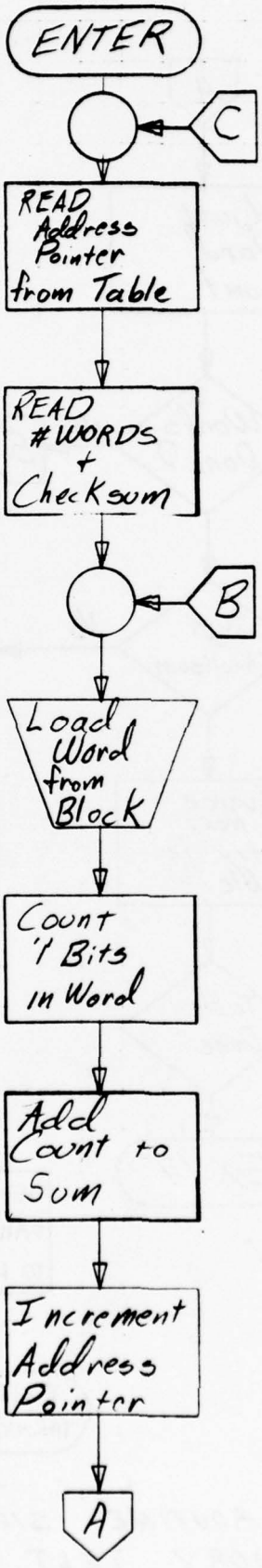


FIGURE 3-29.
SUBROUTINE S16
CHECKSUM
MEMORY TEST

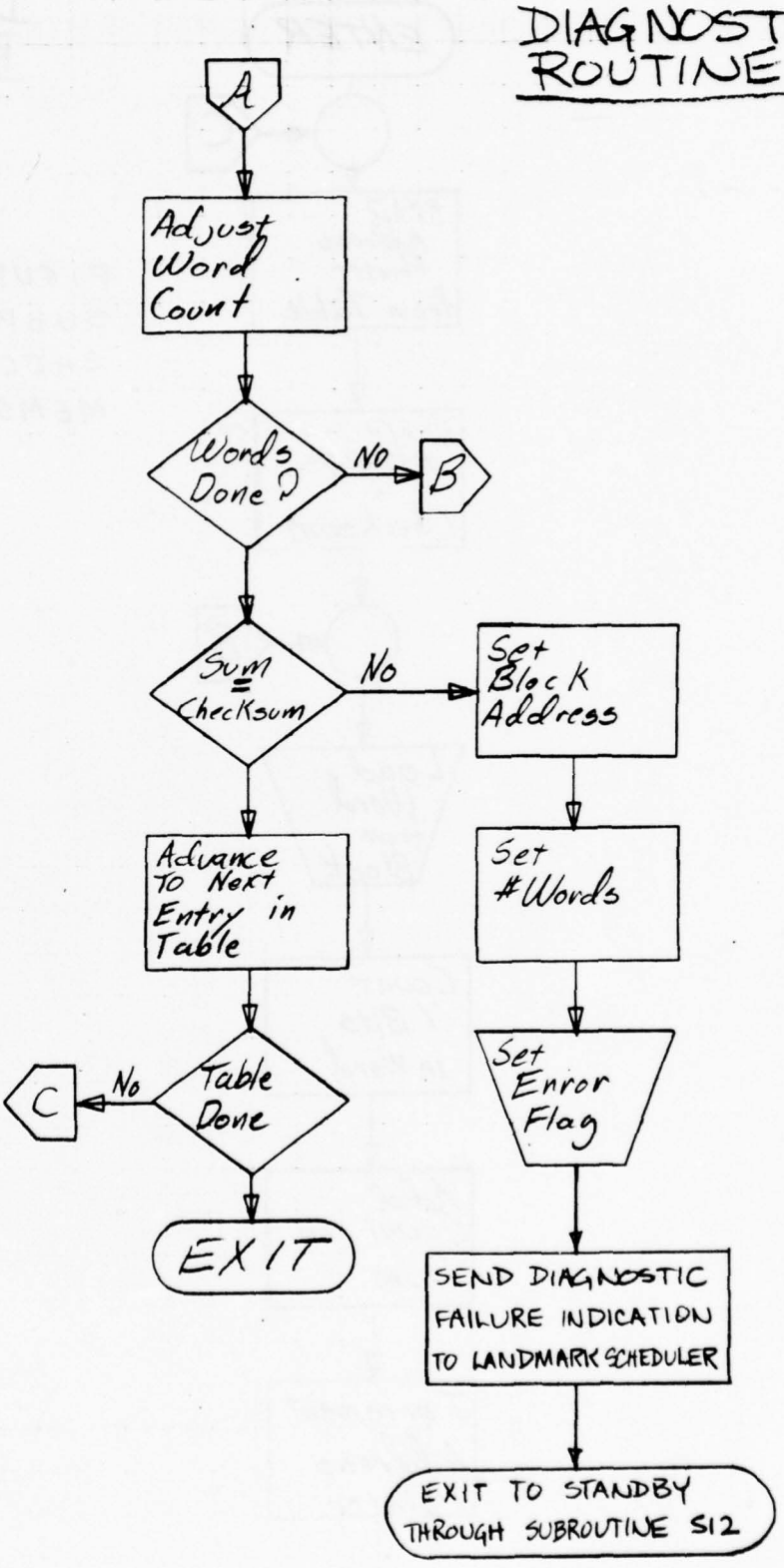


FIGURE 3-29. SUBROUTINE S16, CHECKSUM MEMORY TEST (CONTINUED

3.2.2 Navigation and Attitude Determination Program (NADP). There shall be two major processes operating simultaneously in the Navigation and Attitude Determination Program. The first process shall consist of a series of functions performed by the Kalman filter. These functions shall include:

a. Propagation of the state vector and set-up of the State Transition Matrix (STM).

b. Propagation of the Covariance Matrix.

c. Calculation of estimated measurements and measurement gradient.

d. Calculation of filter weights.

e. Update of the estimated state vector.

f. Update of the Covariance Matrix.

These functions shall be exercised sequentially whenever there are measurements available. The inter-relationship of these functions is shown in Figure 3-30.

The second process shall be performed by the Landmark Scheduler Routine. The Landmark Scheduler Routine, upon the basis of spacecraft landmark geometry, shall initiate the tracker observations which provide the filter with SCHANS equipment measurements.

Prior to starting the program tables of landmark data, initial estimates of the phemeris and the Covariance Matrix, and tables of constants required for navigation computations shall be loaded.

3.2.2.1 Propagate State Vector and Set Up STM. This function shall calculate the estimated values of the state vector variables at the time of the next observation, and shall set up the State Transition Matrix required for propagation of the Covariance Matrix (See Paragraph 3.2.2.2). There shall be 24 elements in the state vector. These elements are listed in Table 3-13.

3.2.2.1.1 Inputs. The prime input to this function shall be updated estimated state vector from the previous measurement, $\hat{X}_{K-1}(+)$, and the time interval between measurements. Other inputs shall be tables of parameters used for ephemeris perturbations and the updated quaternion from the previous measurement.

3.2.2.1.2 Processing. The following state variables shall be propagated by this function:

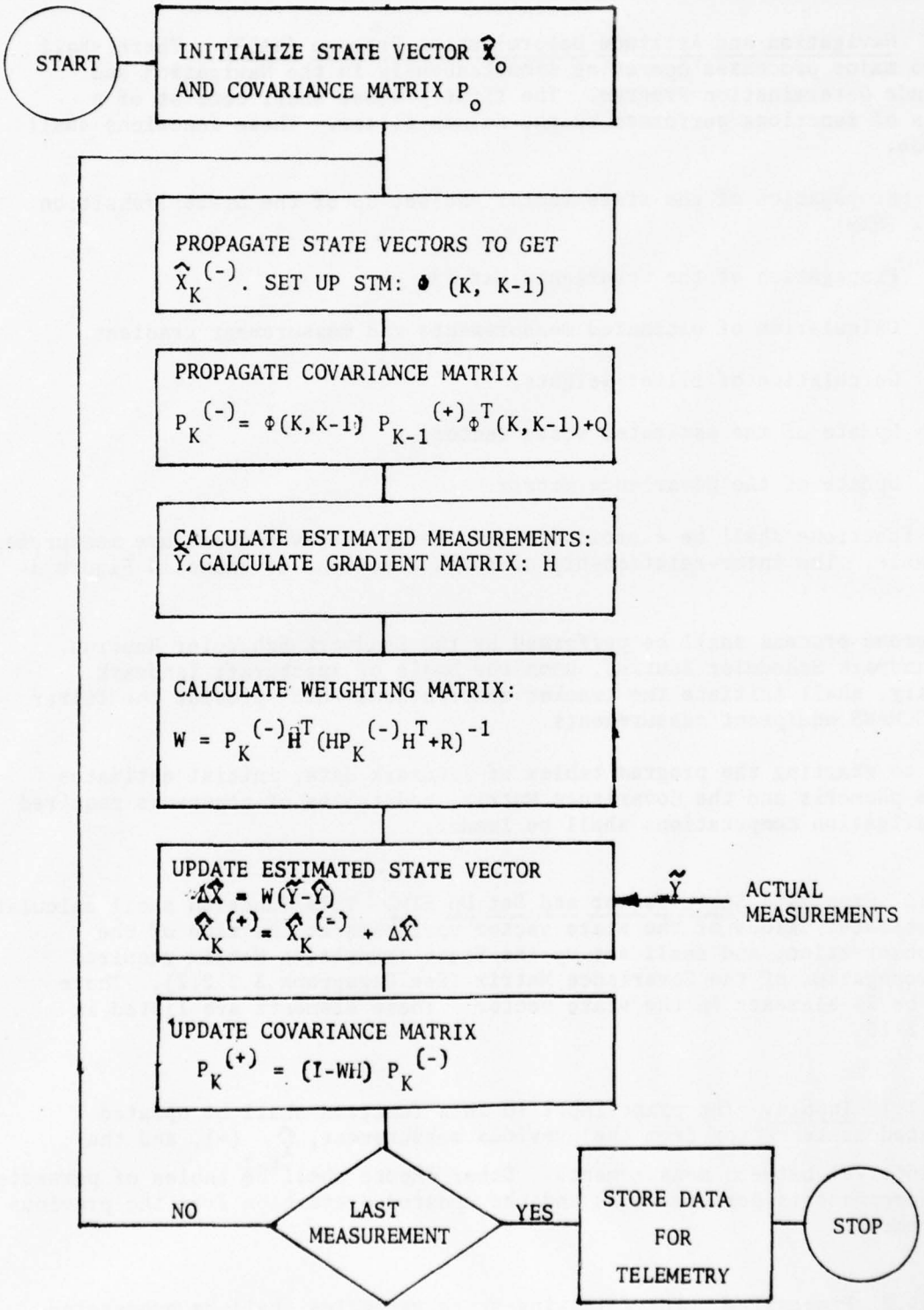


Figure 3-30. NADP Functional Flow Diagram

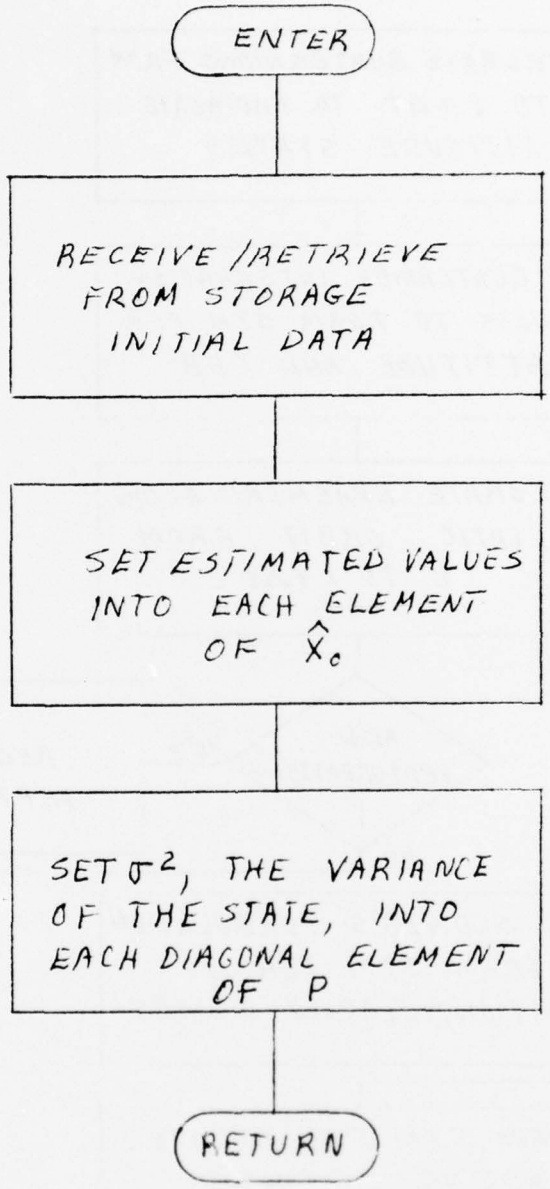


Figure 3-30a. Initialize State Vector and Covariance Matrix

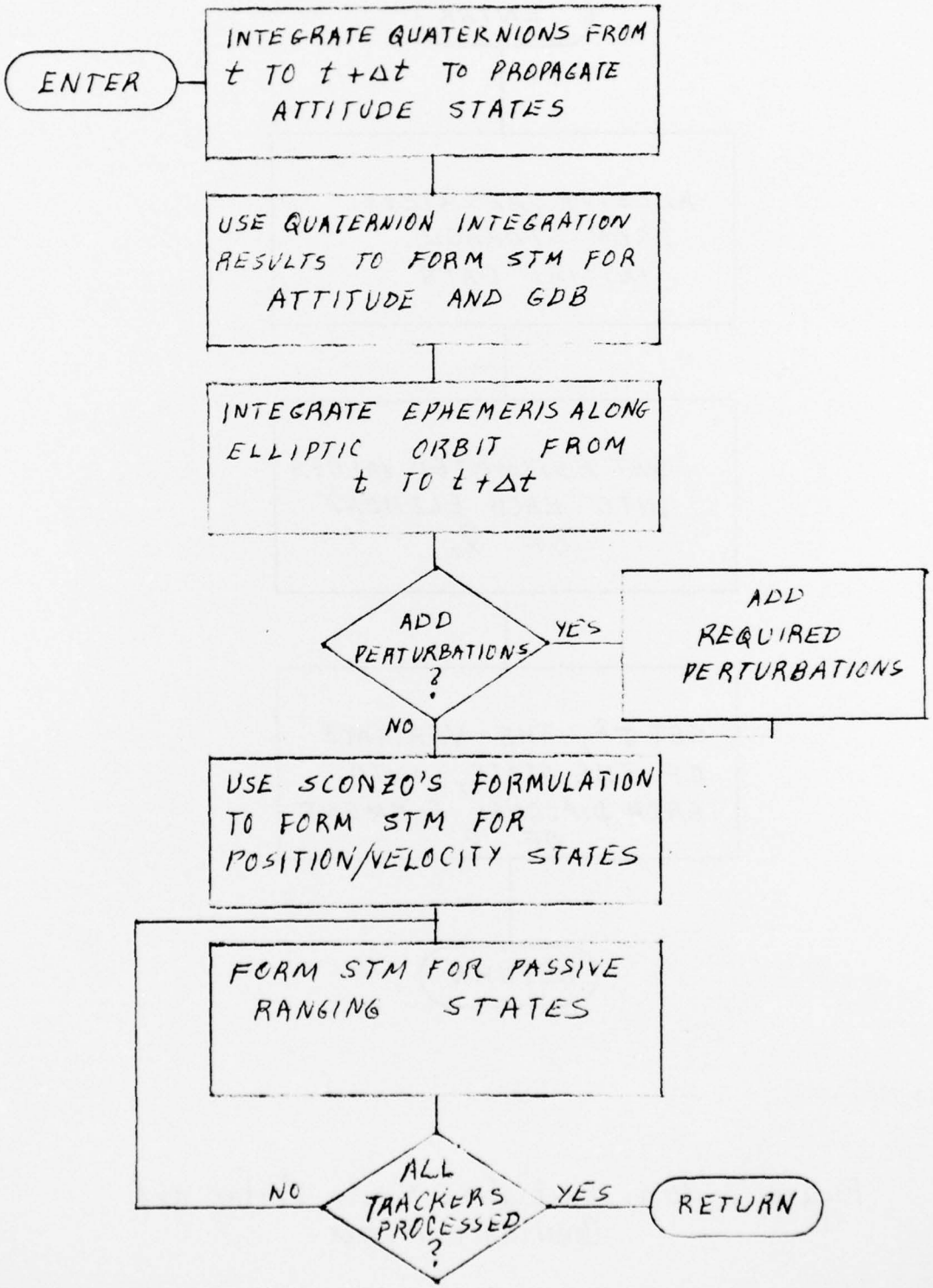


Figure 3-30b. Propagate Estimated State Vector and Set Up STM

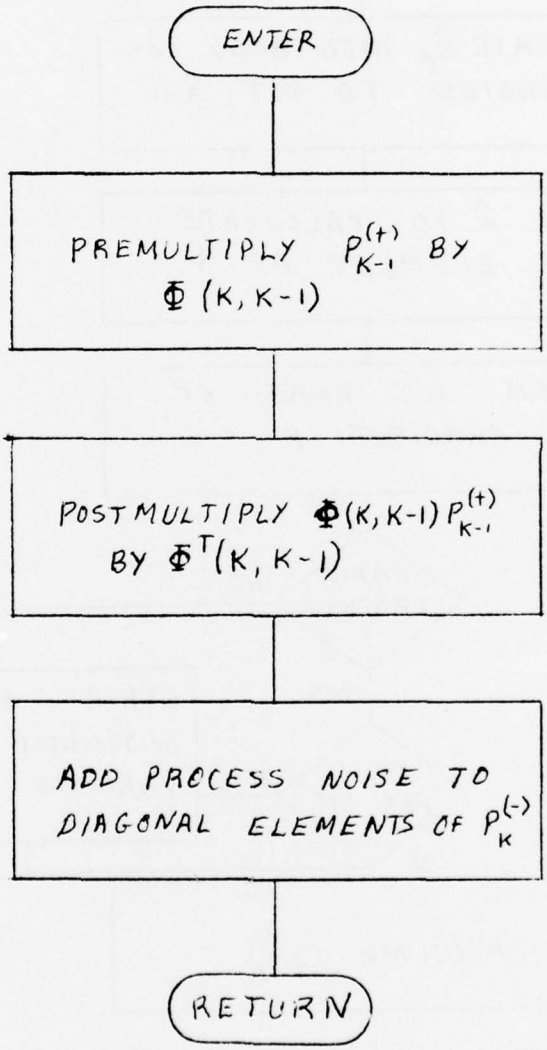


Figure 3-30c. Propagate Covariance Matrix

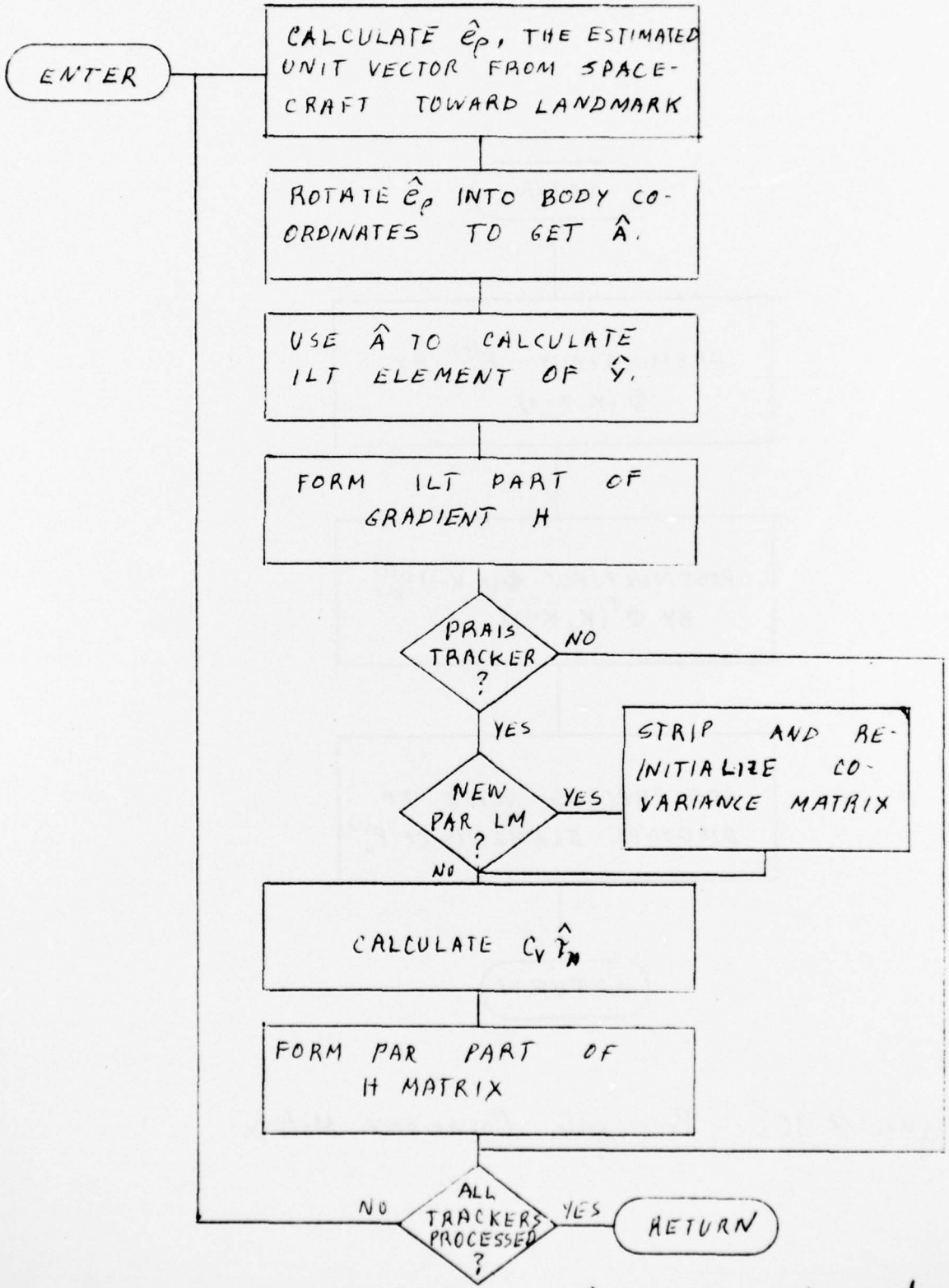


Figure 3-30d. Calculate Estimated Measurements and Gradient Matrix

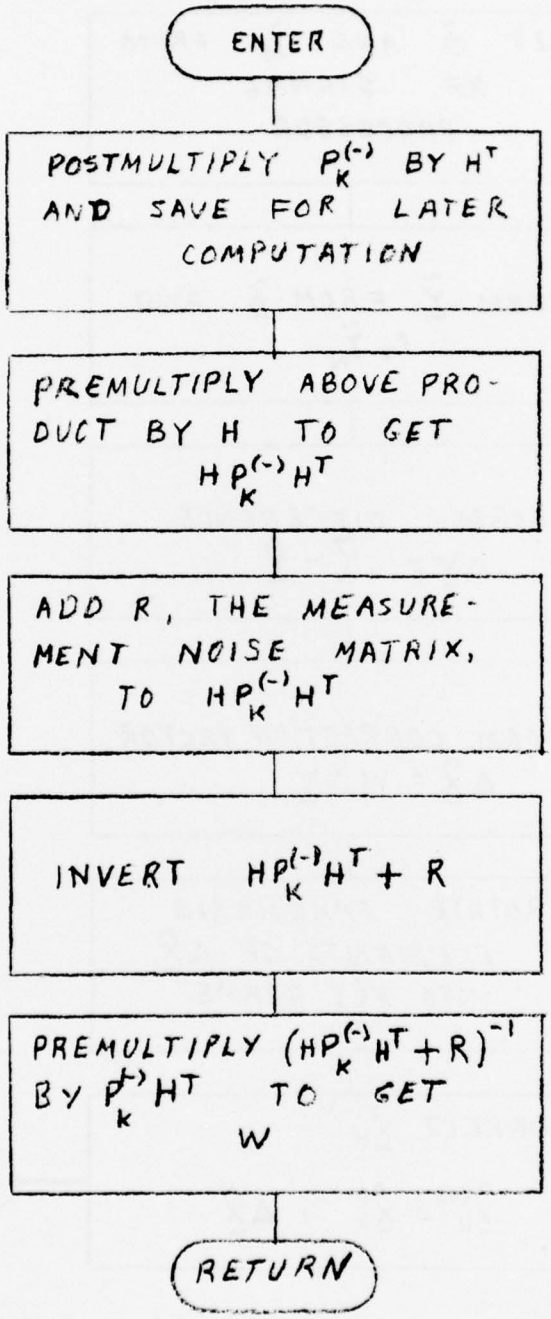


Figure 3-30e. Calculate Weighting Matrix

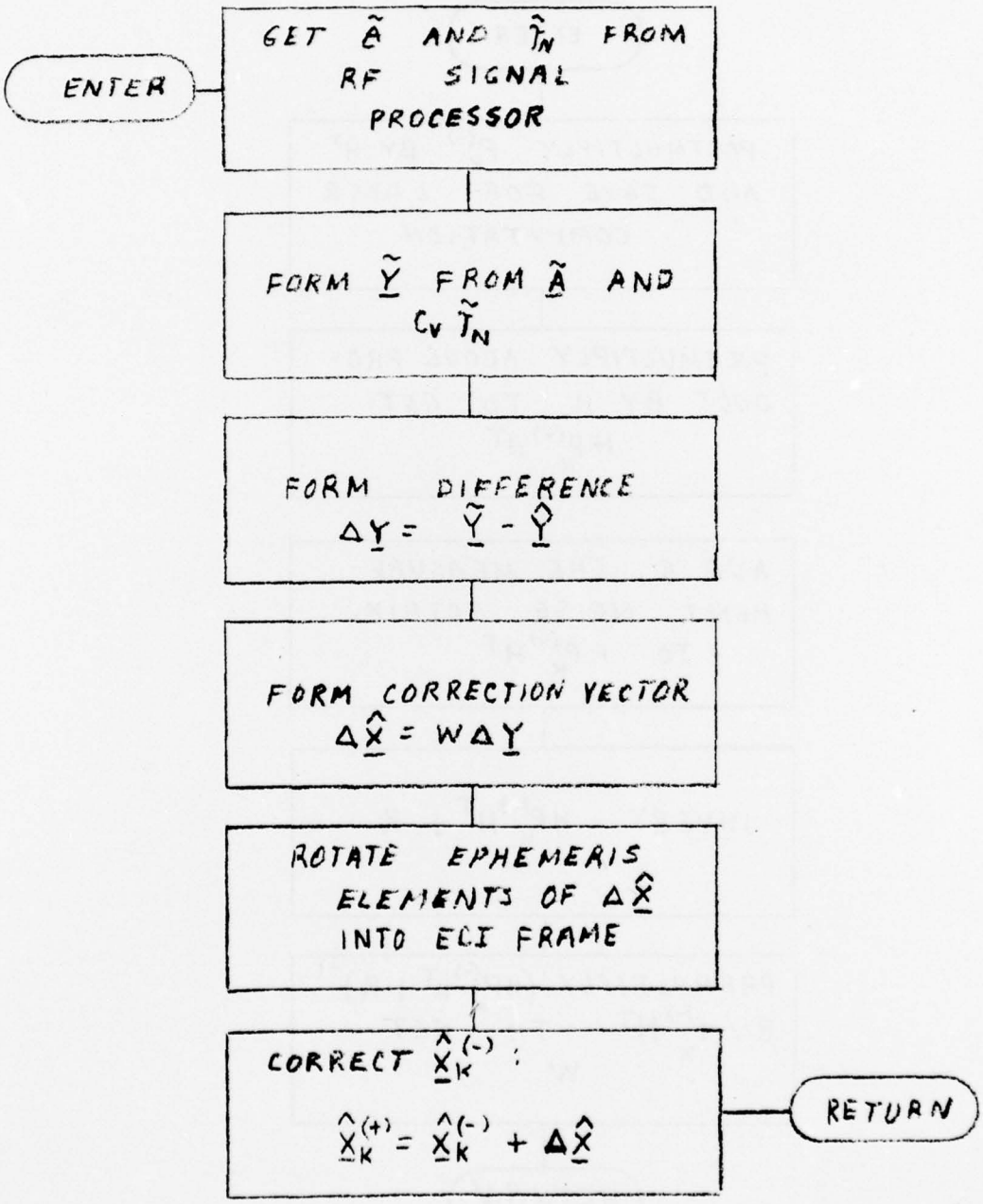


Figure 3-30f. Update Estimated State Vector

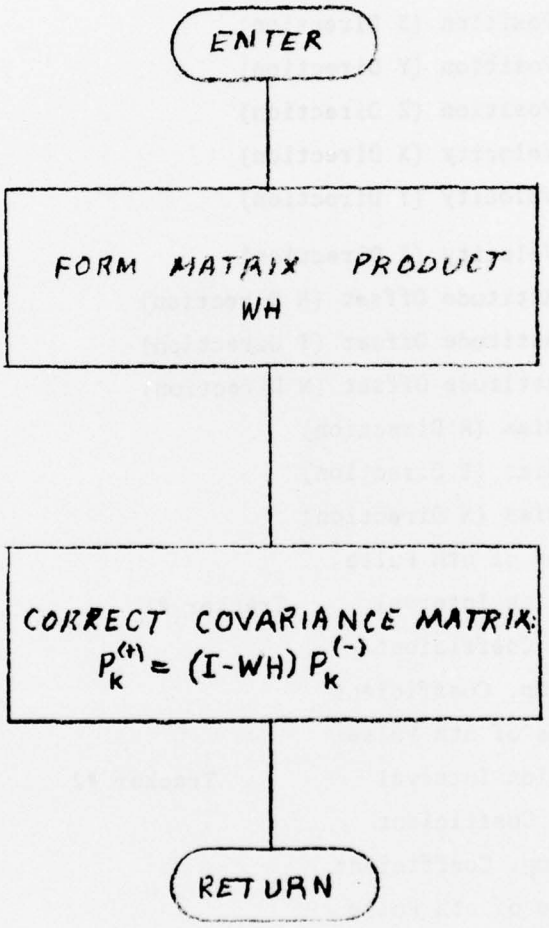


Figure 3-30g. Update Covariance Matrix

Table 3-13. State Variables Used in SCHANS

State	Name	Symbol
1	Spacecraft Position (X Direction)	X
2	Spacecraft Position (Y Direction)	Y
3	Spacecraft Position (Z Direction)	Z
4	Spacecraft Velocity (X Direction)	X
5	Spacecraft Velocity (Y Direction)	Y
6	Spacecraft Velocity (Z Direction)	Z
7	Spacecraft Attitude Offset (R Direction)	Y_1
8	Spacecraft Attitude Offset (T Direction)	Y_2
9	Spacecraft Attitude Offset (N Direction)	Y_3
10	Gyro Drift Bias (R Direction)	g_{d1}
11	Gyro Drift Bias (T Direction)	g_{d2}
12	Gyro Drift Bias (N Direction)	g_{d3}
13	Emission Time of nth Pulse	t_N
14	Pulse Rejection Interval Tracker #1	T
15	Linear Temp. Coefficient	a
16	Quadratic Temp. Coefficient	b
17	Emission Time of nth Pulse	t_N
18	Pulse Rejection Interval Tracker #2	T
19	Linear Temp. Coefficient	a
20	Quadratic Temp. Coefficient	b
21	Emission Time of nth Pulse	t_N
22	Pulse Rejection Interval Tracker #3	T
23	Linear Temp. Coefficient	a
24	Quadratic Temp. Coefficient	b

a. Position and velocity states. These states shall be propagated by integrating the ephemeris using a numerical stable method and a "μ, J_2" potential model which shall yield, in addition to propagation along an elliptic orbit, perturbations necessary to maintain navigational accuracy.

b. Attitude states. The updates in the attitude state variables shall be represented by infinitestimal rotations, which shall be changed into a quaternion. The output of the gyros shall be used to integrate the quaternion to the time of the next observation, rather than employing Euler angles or the elements of the spacecraft direction cosine matrix.

c. In states for each of the trackers.

All other variables shall not be propagated.

The State Transition Matrix, Φ (K, K-1) shall be a 24 x 24 block diagonal matrix, with blocks allocated as follows:

a. Block 1 (6 x 6): position and velocity.

b. Block 2 (6 x 6): attitude and gyro drift bias.

c. Block 3 (4 x 4): passive ranging (PAR) states for tracker 1.

d. Block 4 (4 x 4): PAR states for tracker 2.

e. Block 5 (4 x 4): PAR states for tracker 3.

There shall be, in Φ (K, K-1), no dependencies among any states not in the same block.

3.2.2.1.3 Outputs. Outputs of this function shall be the propagated estimated state vector, $X_K(-)$, the STM, Φ (K, K-1), and the pseudo process noise matrix, Q.

3.2.2.2 Propagate Covariance Matrix. This function shall calculate the elements of the Covariance Matrix at the time of the next observation.

3.2.2.2.1 Inputs. Inputs to this function shall be the updated Covariance Matrix from the previous measurement, $P_{K-1}(+)$, and the STM Φ (K, K-1).

3.2.2.2.2 Processing. The propagated Covariance Matrix, $P_K(-)$ shall be calculated by the matrix equation:

$$P_K^{(-)} = \Phi\,(K, K-1)\; P_{K-1}^{(+)}\; \Phi^T\,(K, K-1) + Q.$$

3.2.2.2.3 Outputs. The output of this function shall be the propagated Covariance Matrix, $P_K(-)$.

3.2.2.3 Calculate Estimated Measurements and Gradient Matrix. This function shall calculate the values of the estimated measurements, $\hat{Y}$, and a Gradient H, for each measurement used in the Kalman filter.

3.2.2.3.1 Inputs. Inputs to this function shall be the propagated estimated state vector $\hat{X}_K(-)$, and the positions of the landmark used by the tracker making the measurements.

3.2.2.3.2 Processing. The estimated measurements to be calculated shall be the two ILT measurements and, if the landmark is a PRAIS landmark, the PAR measurement. For each measurement to be used in the update (see Paragraph 3.2.2.5) a gradient vector shall also be calculated.

3.2.2.3.3 Outputs. Outputs from this function shall be the estimated measurements, $\hat{Y}$, and the measurement gradient H.

3.2.2.4 Calculate Filter Weights. This function shall calculate the Weighting Matrix, W, which shall be used in the updates of the estimated state vector and the Covariance Matrix (see Paragraph 3.2.2.5 and 3.2.2.6).

3.2.2.4.1 Inputs. Inputs to this function shall be the propagated Covariance Matrix, $P_K(-)$, the Gradient Matrix, H, and a matrix R, the noise of the measuring instruments.

3.2.2.4.2 Processing. The Weighting Matrix shall be calculated by the matrix equation:

$$W = P_K(-)\, H^T (HP_K(-)H^T + R)^{-1}$$

3.2.2.4.3 Outputs. The output of this function shall be the Weighting Matrix, W.

3.2.2.5 Update of Estimated State Vector. This function shall calculate the filter corrections to the estimated state vector and shall use these corrections to adjust the state vector.

3.2.2.5.1 Inputs. Inputs to this function shall be the estimated state vector, $\hat{X}_K(-)$, the Weighting Matrix, W, the estimated measurements, $\hat{Y}$, the propagated quaternion, and the SCHANS equipment measurements, $\tilde{Y}$.

3.2.2.5.2 Processing. The filter corrections shall be calculated by:

$\hat{\Delta X} = W(\tilde{Y} - \hat{Y})$.

From this calculation, the updated estimated state vector shall be calculated by:

$\hat{X}_K(+) = \hat{X}_K(-) + \hat{\Delta X}$.

The elements of $\hat{\Delta X}$ corresponding to the attitude states shall be used to update the quaternion.

3.2.2.5.3 Outputs. Outputs of this function shall be the updated estimated state vector, $\hat{X}_K(+)$, and the updated quaternion.

3.2.2.6 Update Covariance Matrix. This function shall modify the Covariance Matrix to reflect incorporation of the latest error measurements.

3.2.2.6.1 Inputs. Inputs to this function shall be the propagated Covariance Matrix, $P_K(-)$, the Weighting Matrix, W, and the Gradient Matrix, H.

3.2.2.6.2 Processing. The Covariance Matrix shall be updated by the matrix equation:

$P_K^{(+)} = (I - WH)\, P_K^{(-)}$

where I is the 24 x 24 Idenity Matrix.

3.2.2.6.3 Outputs. The output from this function shall be the updated Covariance Matrix, $P_K(+)$.

3.2.2.7 Landmark Scheduler Routine. The Landmark Scheduler Routine, including its called subroutines, shall determine landmark availability, perform landmark selection and interface with the RF Signal Processing and Executive Subprogram. Specific tasks of the Landmark Scheduler Routine and its called subroutines shall be as follows:

a. Determine available landmarks throuth geometric filtering.

b. Select landmarks for data collection.

c. Generate schedule for landmark pulse collection.

d. Interface with the RF Signal Processing and Executive Subprogram.

3.2.2.7.1 Routine Functional Flow Diagram. The functional flow diagram for the Landmark Scheduler Routine is shown in Figure 3-31.

3.2.2.7.2 Inputs. The Landmark Scheduler Routine or one of its called subroutines shall receive the following inputs:

a. Processing results from the RF Signal Processing and Executive Subprogram as specified in Table 3-7.

b. S/C attitude and position from memory.

c. Landmark table (Table 3-14) from memory.

3.2.2.7.3 Processing. The Landmark Scheduler Routine, including its called subroutines, shall perform the following processing functions:

a. Geometric filtering. The Landmark Scheduler Routine shall call from the landmark table those landmarks falling into the field of view of the SCHANS antennas and meeting landmark elevation angle requirements.

b. Landmark Selection. Up to three landmarks shall be selected for sequential pulse collection. Landmarks shall be selected to maximize geometric spread among the three landmarks.

c. Schedule Generation. The landmark for which pulse collection will be next executed shall be selected. A landmark descriptor shall be developed, including the time at which pulse collection will be initiated.

d. Scheduler Operation. Landmark descriptors shall be transmitted to the RF Signal Processing and Executive Subprogram. Processing results from the RF Signal Processing and Executive Subprogram shall be received and processed to permit continual updating and operation of the landmark scheduler.

3.2.2.7.4 Outputs. The Landmark Scheduler Routine or one of its called subroutines shall place in memory data as specified in Table 3-8.

LANDMARK SCHEDULER ROUTINE, FIGURE 3-31

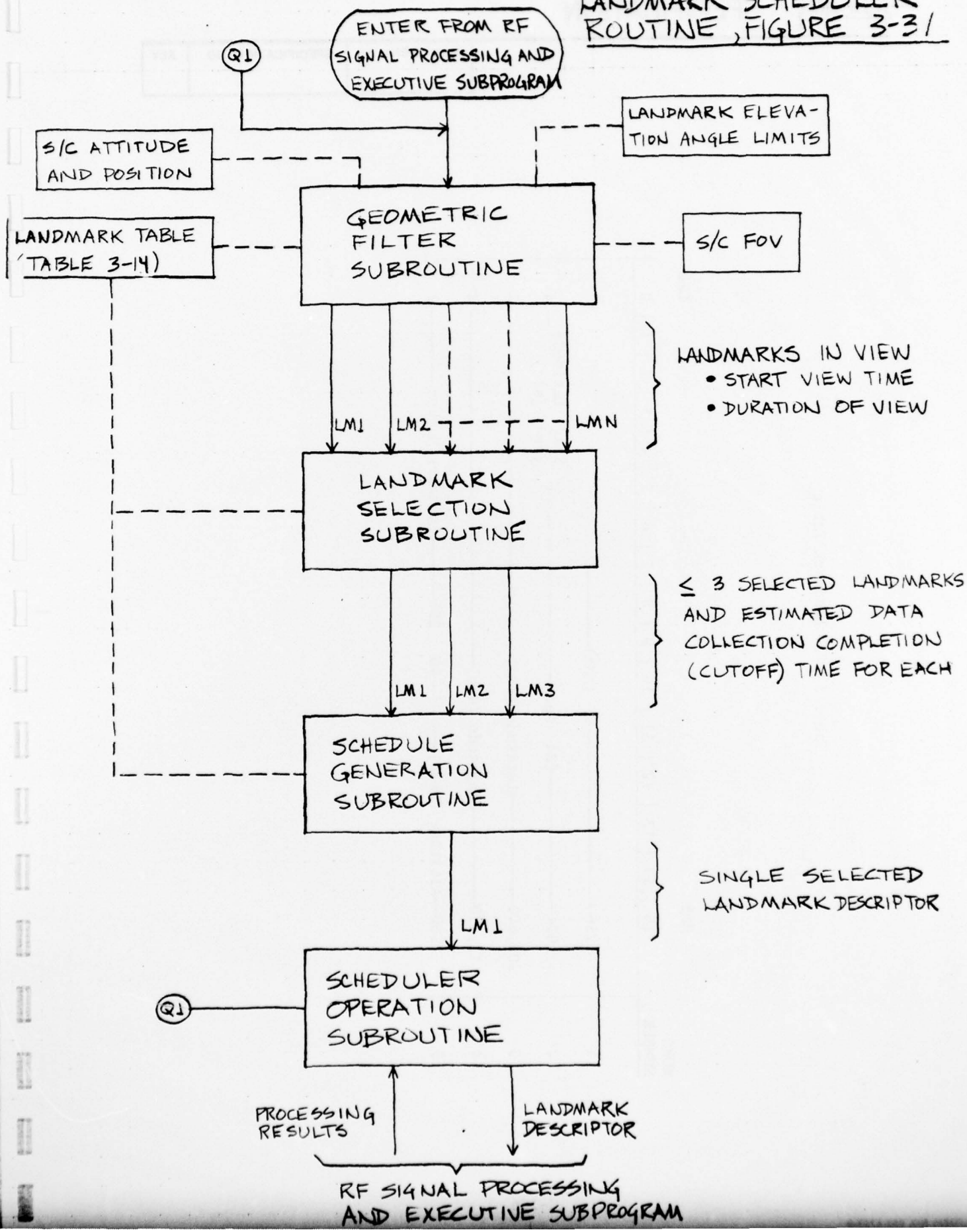


Table 3-14. Landmark Table

WORD NUMBER	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
1	256				RF (MHz)				1							
2	1024			PRI sec							1	Stag-ger	Latitude (sec)			.4
3	209,600			Latitude (sec)												
4	13,100			Longitude (sec)												.4
5	2560	Altitude (Feet)				40		256		Landmark Number						1