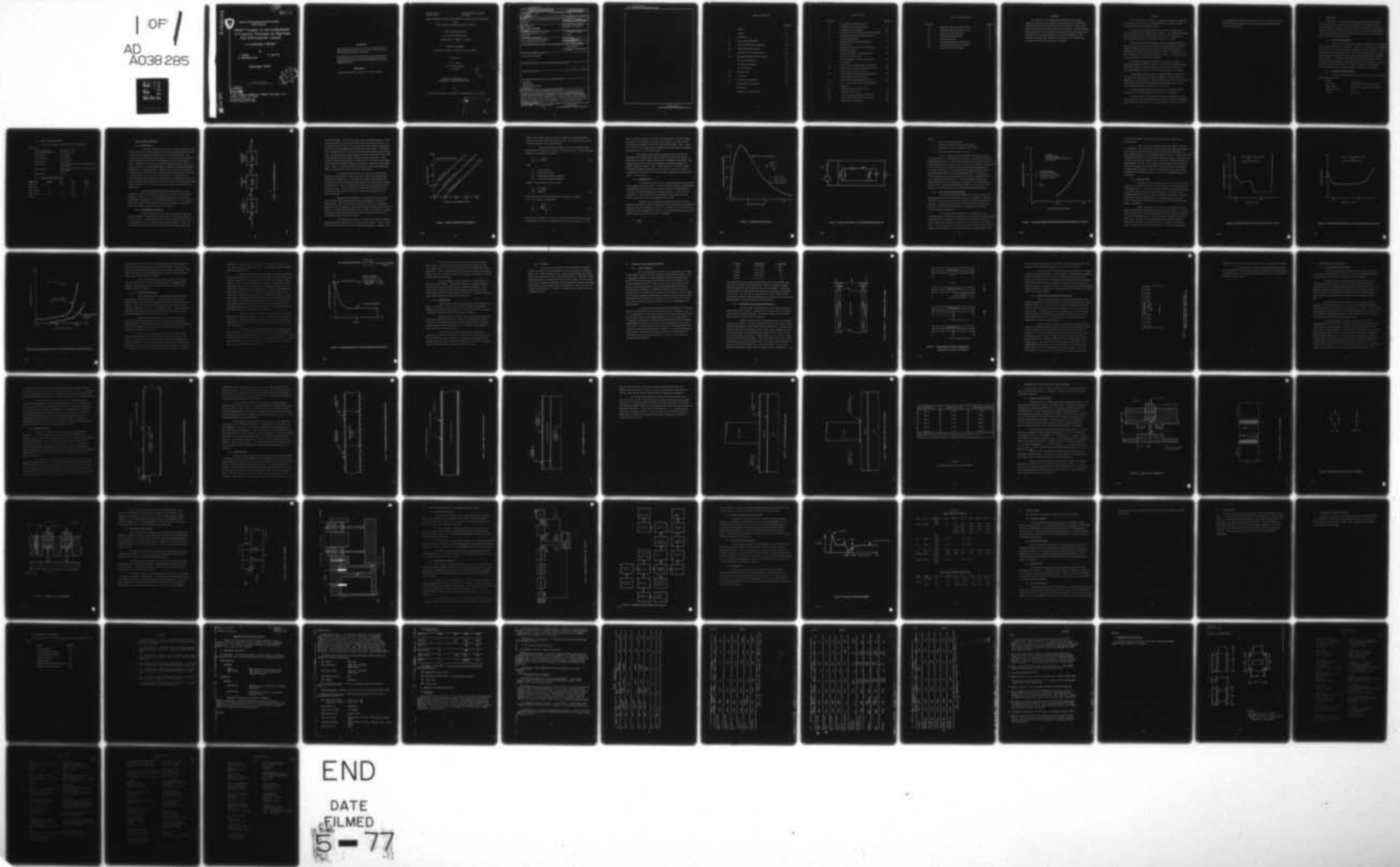
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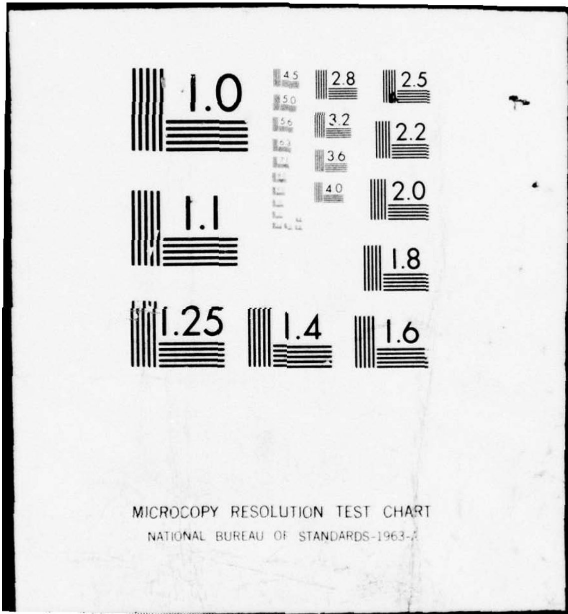
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ECOM-0039-1

MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

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By

Y. ANAND R. BILOTTA
P. BAKEMAN (RRC)

November 1976

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The objective of this Manufacturing Methods and Technology Engineering Program is to establish the producibility of the X-band semiconductor bulk limiter and the X-band bulk semiconductor - lower power diode multistage limiter by mass production techniques. During the quarter, X-band semiconductor bulk limiters and multistage clean up limiters were manufactured and were characterized for their RF performance. First engineering samples (Item 0001AA) consisting of five bulk limiters and one clean up limiter will be shipped on schedule.

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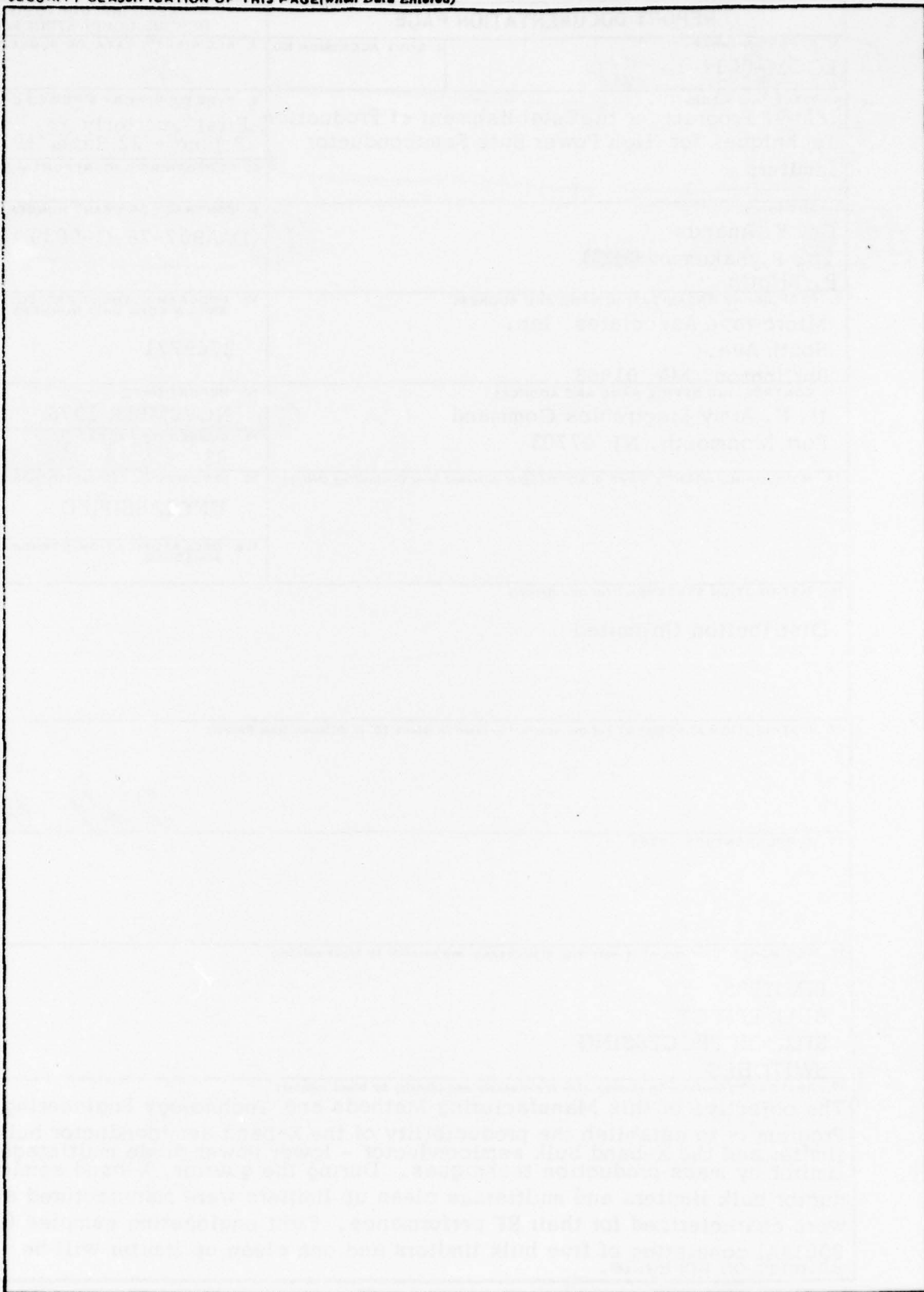

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ABSTRACT

The objective of this Manufacturing Methods and Technology Engineering Program is to establish the producibility of the X-band semiconductor bulk limiter and the X-band bulk semiconductor - lower power diode multistage limiter by mass production techniques. During the quarter, X-band semiconductor bulk limiters and multistage clean up limiters were manufactured and were characterized for their RF performance. First engineering samples (Item 0001AA) consisting of five bulk limiters and one clean up limiter will be shipped on schedule.

PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per Electronics Command Technical requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time, (2) high power capability, (3) insertion loss and (4) VSWR.

A total of 15 engineering sample limiters, 20 confirmatory sample limiters and 50 pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G, and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR, No. 15, dated December 1975, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include iris formation, circuit configuration, material characterization and chip mounting. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phase II, III, and IV a single device design will be produced.

The major effort of this program will be the realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually, any of the goals described can be currently obtained. Recognizably, it is

the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

I. OBJECTIVES

The objective of the current Manufacturing Methods and Technology Engineering program is to establish the producibility of the X-band bulk semiconductor limiter and the X-band bulk semiconductor-lower power diode multistage limiter by mass production techniques. Achieving the performance goals of the program represents a formidable engineering task. These goals, from SCS-486 are summarized below.

A. Functional Description

The high power, solid state, limiter described herein will operate in the frequency band 9.0 - 9.65 GHz. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

B. Mechanical Characteristics

The bulk semiconductor limiter structure will have the following performance objectives:

Weight	7.0 oz max
Input flange	mates with UG-40B/U choke flange
Output flange	mates with UG-135/U cover flange
Mounting position	any
Cooling	conduction

C. Electrical Characteristics

The bulk semiconductor limiter will have the following objectives:

Peak RF input power 1 μsec pulses continuous	30 kW, Du = .001 10 kW, Du = .01
Insertion loss	0.7 dB (max)
Low level VSWR	1.4:1 (max)
Recovery time	0.8 μsec (max)
Flat leakage	50 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
Spike leakage	750 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
External bias	none

D. Absolute Rating Objectives

PARAMETER	SYMBOL	MIN	MAX	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P		30	kW
Average Power	P_a		100	W
Ambient Temp.	T_A	-55	+85	^oC
Altitude	--		50,000	ft

II. BASIC LIMITER PARAMETERS

A. Introduction

Microwave limiters serve two essential system functions. The primary function is to protect sensitive receiver input stages from destruction by excessive microwave power levels; that is, receiver protection. The second function often used in radar systems is to act as a switching element to direct microwave power from the transmitter output port to the antenna. Thus, the limiter can be used as an automatic Transmit-Receive switch. All types of limiters are useful to some degree, depending upon their performance parameters, as receiver protectors. However, only non-dissipative limiters can perform the T-R function as the incident microwave power must be directed toward the antenna port. The bulk semiconductor first stage operates by switching from a parallel resonant circuit across the waveguide in the transmit state to a mismatched resistance in the isolation state. The bulk semiconductor limiter, therefore, can be used in both receiver protection and TR switching applications.

Important performance parameters which specify the useful operation of a microwave limiter are frequency of operation, power handling capability, insertion loss, low level VSWR and bandwidth, recovery time, flat leakage, spike leakage, bias requirements and arc loss. The component, which is the subject of this production engineering measure, is an X-band unit with performance specified from 9.0 to 9.65 GHz.

B. Power Handling Capability

In order to achieve the high levels of attenuation needed for receiver protection, microwave limiters are built as multi-stage devices as shown in Figure 1. In the example shown, a 20 kW incident power level must be attenuated to a level of 20 mW before entering the receiver. Thus, the input signal must be attenuated by 60 dB to protect the receiver during the

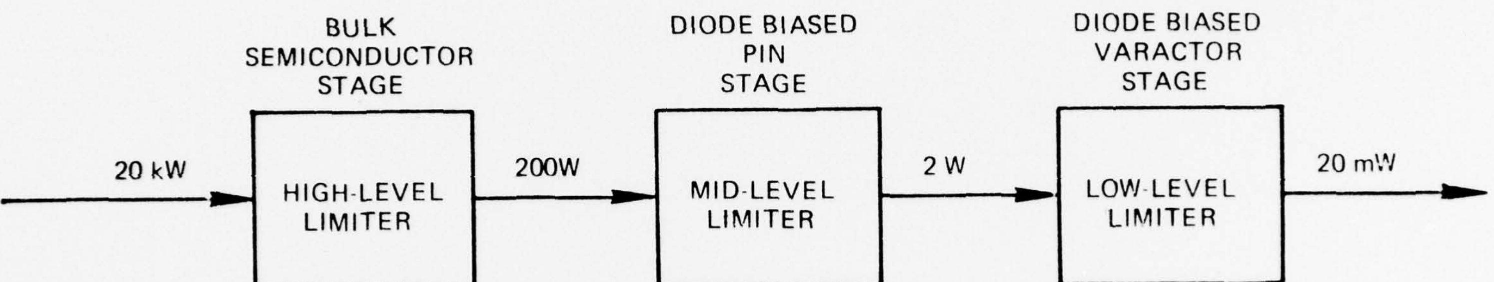

FIGURE 1 MULTI-STAGE MICROWAVE LIMITER

D-15486

transmitting pulse. This is done by using three 20 dB limiter stages. As the power output from the first limiting stage should not exceed 200 watts, it is the performance of the first or input stage that is most critical in determining the power handling capability of the entire multi-stage limiter. Essentially all the incident power must either be reflected or absorbed by the first limiting stage. All stages after the first stage are low power stages which serve only to provide the additional isolation needed to protect the receiver. Since, typically, Schottky mixer diodes can withstand 100 to 150 mW of flat leakage power, the 20 mW example represents an extremely conservative flat leakage value. In fact, a three stage limiter with 18 dB per stage would adequately protect a Schottky mixer from a 20 kW input power level.

The need for protection from very high power levels arises primarily in radar systems. Short, high power, pulses are transmitted at a relatively low repetition rate. The limiter must protect the receiver during each pulse and allow the received echo signals to pass unattenuated between transmit pulses. Thus, the power handling operational requirements pertain to the first stage. They are peak power, pulse energy and repetition rate. These factors also combine to yield an average power capability for the limiter component.

The peak power capability of a high power limiter is limited by two factors, high field breakdown and energy absorption. High field breakdown can occur if the microwave electric field rises to a sufficiently large value to cause dielectric or gaseous breakdown within the limiter circuit structure. With bulk solid state units, this limitation is generally not critical because the conductivity of the silicon element reduces the electric field in the highest field regions of the device.

The incident pulse energy is primarily responsible for limiting the power handling capability of bulk semiconductor limiters. Figure 2 shows the pulse energy for incident pulses of different amplitudes and lengths. The

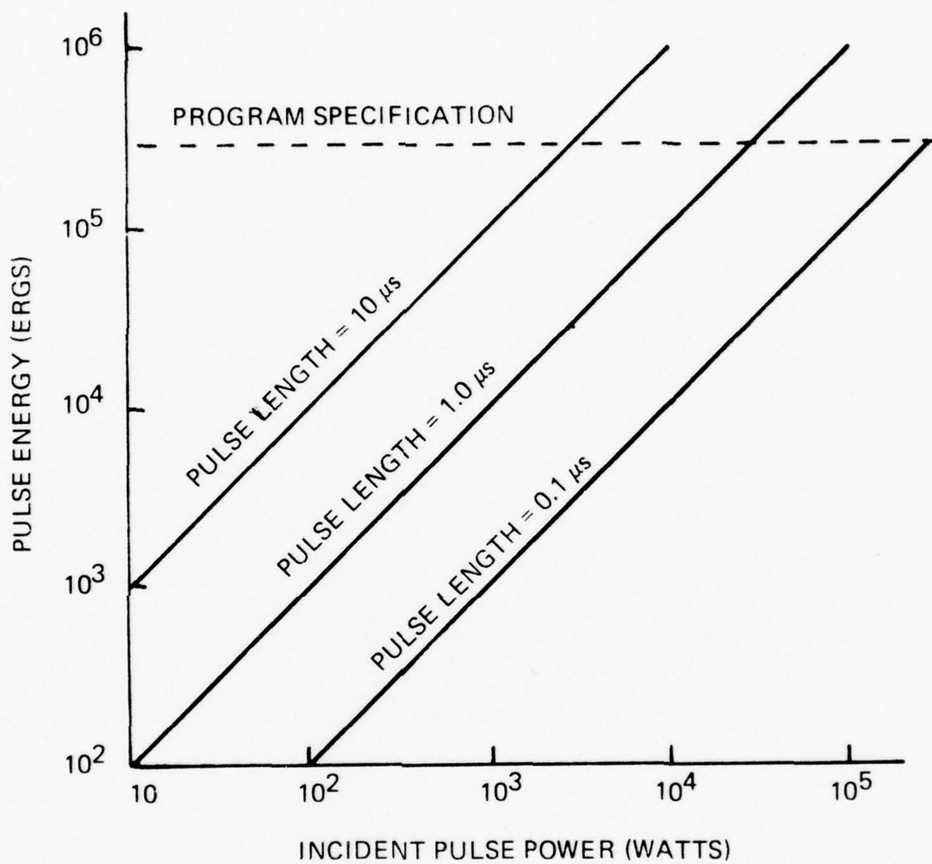

FIGURE 2 INCIDENT MICROWAVE PULSE ENERGY

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incident pulse energy times the fraction dissipated by the limiter element gives the amount absorbed by the element itself. This energy must be stored in the heat capacity of the limiter element.

The bulk limiter forms primarily a resistive mismatch across the waveguide transmission line when in the isolation state. Using normalized impedance, the isolation is given by:

$$\frac{P_i}{P_t} = \left| 1 + \frac{YZo}{2} \right|^2 \tag{1}$$

where

P_i = incident power

P_t = transmitted power

Y = transformed element admittance

Z_o = transmission media impedance

similarly, the dissipated power is given by:

$$\frac{P_i}{P_d} = \frac{\left| 1 + \frac{ZoY}{2} \right|^2}{Re(ZoY)} \tag{2}$$

In the case where the element admittance is primarily conductive ($Y = G + j0$), equation (2) reduces to:

$$\frac{P_d}{P_i} = 2 \frac{\sqrt{\frac{P_i}{P_t} - 1}}{\frac{P_i}{P_t}} \tag{3}$$

Thus, when the element is resistive, the fraction of the incident power which is dissipated in the element is determined only by the isolation level, P_i/P_t.

Figure 3 shows the P_d/P_i as a function of isolation level. The bulk limiters of concern in this manufacturing effort have isolations in excess of 19 dB and therefore dissipate less than 20% of the incident power. Thus, to meet the 3×10^5 erg input pulse energy required by the specification, the element need absorb only 6×10^4 ergs per pulse.

The average power handling capability of the bulk limiter is determined by the thermal conductivity between the active semiconductor region where the pulse energy is dissipated to the ambient environment. This conductivity is determined by the materials and geometric design of the element mounting structure. Thus, a design goal of 1.0 to 2.0°C per watt is required to limit the temperature rise of the active region of the limiter to between 20°C to 40°C at the 100 watt average incident power level (10 kW pulses, .01 duty cycle).

C. Insertion Loss

An equivalent circuit of the bulk semiconductor high power stage of the limiter is shown in Figure 4. The semiconductor element is characterized by parameters C and G while the iris mounting structure is characterized by turns ratio, N; parallel inductance, L; series inductance, LW; and series resistance, R. The input port is the normalized 1 ohm source on the left and the output port is the 1 ohm impedance on the right.

Equation (1) can be used to calculate the insertion loss and isolation of the limiter stage by transforming the element and circuit admittances throught the ideal transformer turns ratio, N. Empirical data have been used to evaluate the circuit parameters of Figure 4. The relationship between low level element capacitance and conductivity is as follows:

$$G = \frac{C}{\epsilon_o \epsilon_r \rho} \quad (4)$$

RESISTIVE LIMITER MISMATCH

$$\frac{P_d}{P_i} = 2\,\frac{\sqrt{\dfrac{P_i}{P_t} - 1}}{\dfrac{P_i}{P_t}}$$

P_i = Power Incident

P_t = Power Transmitted

P_d = Power Dissipated

FRACTIONAL POWER DISSIPATED $\left(\frac{P_d}{P_i}\right)$: 0, 0.1, 0.2, 0.3, 0.4, 0.5

ISOLATION LEVEL (dB): 0, 10, 20, 30

FIGURE 3 DISSIPATION VS. ISOLATION

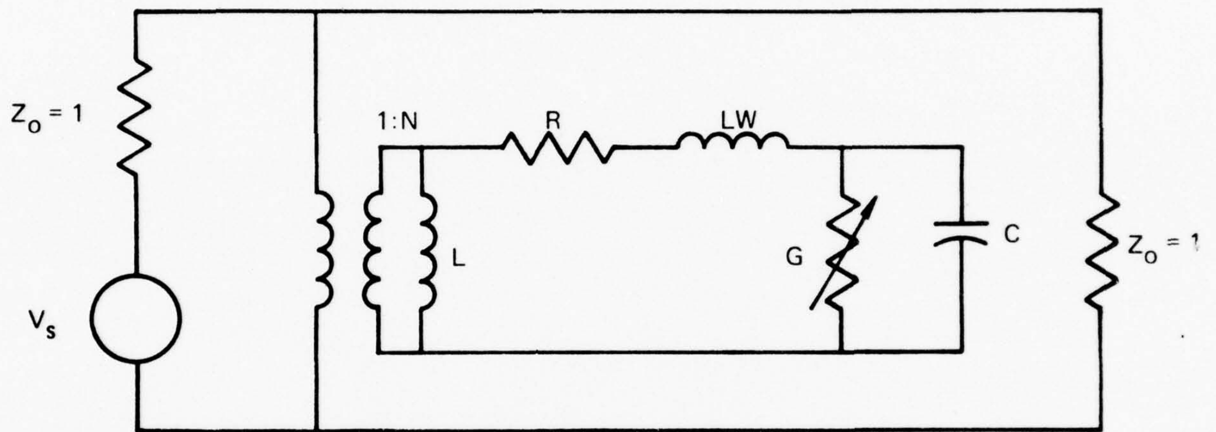

FIGURE 4 EQUIVALENT CIRCUIT OF BULK SEMICONDUCTOR LIMITER

D-15489

where

G = element conductance (mhos)

ρ = element bulk resistivity (ohm centimeters)

ϵ_o = permitivity of free space (8.85×10^{-14} f/cm)

ϵ_r = relative permitivity of silicon (11.8)

Figure 5 shows a plot of calculated insertion loss for bulk semiconductor limiters fabricated from 4,000 ohm-cm material as a function of element capacitance. These values of insertion loss are valid for a bulk semiconductor limiter mounted in the center of a 1/16 inch thich iris plate with a 1/16 inch high iris slot tuned to resonate the element capacitance of 9.5 GHz. Lower values of turns ratio can be obtained by moving the iris vertically toward either top or bottom waveguide wall. A typical value for the single element turn ratio squared is a 2300 and a variation of 15% can be obtained by moving the iris. This has the effect of permitting larger capacitance limiter elements to be utilized with the same values of insertion loss. Higher power handling capability can be achieved in this fashion, as the higher capacitance element can dissipate more energy.

D. Low Level VSWR and Bandwidth

The low level VSWR and bandwidth of a limiter determine the frequency range over which the device is useful. At frequencies where the input VSWR is high, the insertion loss between the antenna and receiver is also high. High insertion loss caused by either resistive or reactive mismatch of the limiter component degrades the system noise figure and therefore limits its usefulness.

In multistage limiter components, the bandwidth of each individual stage is of secondary importance to the bandwidth of the assembled multi-stage limiter component. The reason for this is that the bandwidth of a two or three stage limiter can be wider than the bandwidth of each stage alone. The wide bandwidth is accomplished by using the off center frequency reactance of one stage to tune out the reactance of the other stages. Thus,

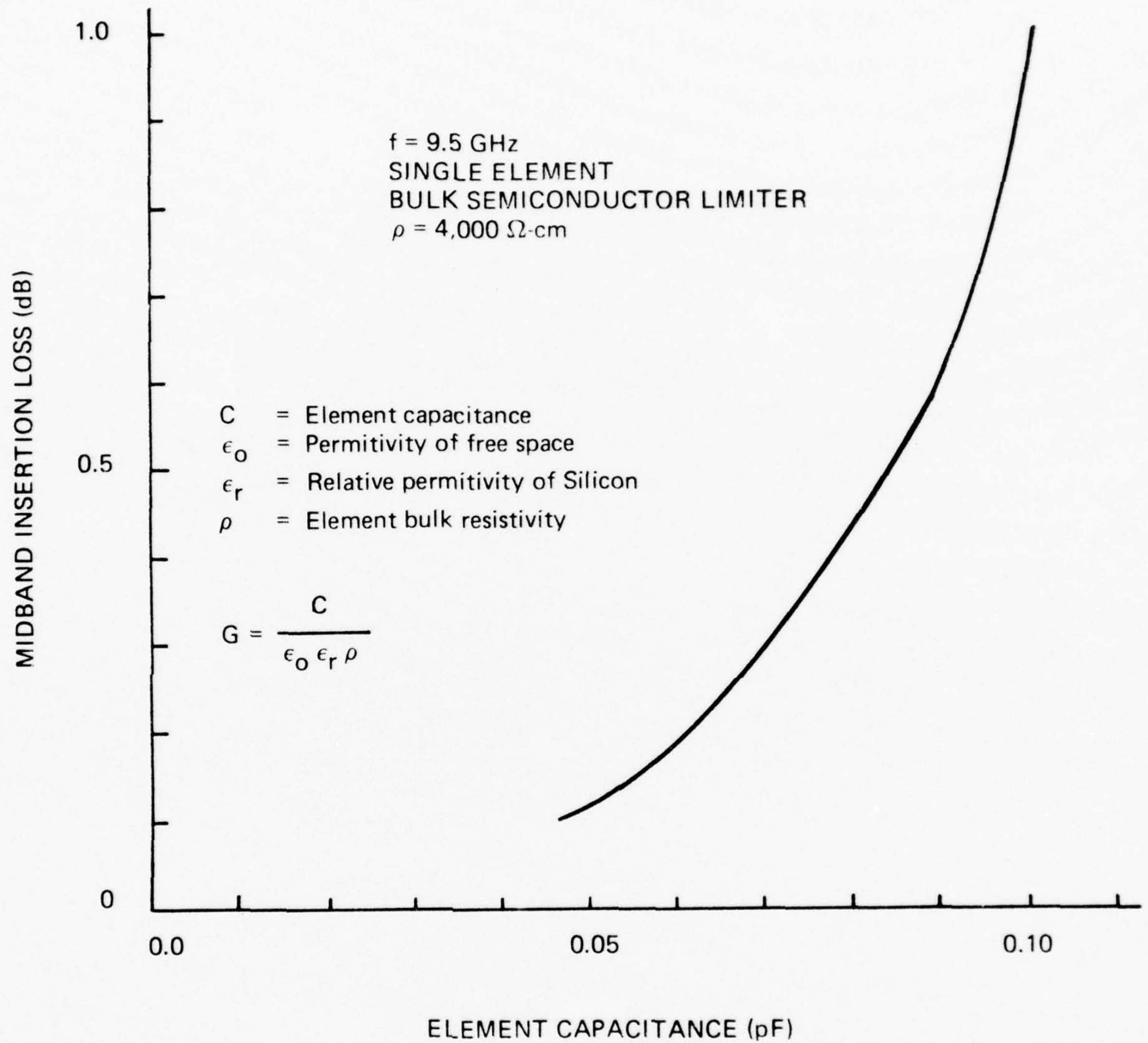

FIGURE 5 CALCULATED INSERTION LOSS VERSUS LIMITER ELEMENT CAPACITANCE

D-15490

a three stage limiter is designed as a band pass filter structure for the low level case.

Figure 6 shows the VSWR of a three stage limiter consisting of a single iris bulk semiconductor limiter stage built by RRC International, Inc. and a two stage PIN-varactor limiter built by Microwave Associates, Inc. The assembled limiter was successfully tuned to meet the 9.0 GHz to 9.65 GHz VSWR design specification for the current production program. The bulk semiconductor stage had an insertion loss of 0.3 dB and a 3 dB loss bandwidth of approximately 1.32 GHz. The 0.7 dB absolute bandwidth of the solid state unit when measured alone was 450 MHz. However, when combined with a two stage low power diode limiter, the complete three stage unit provided insertion loss performance as shown in Figure 7 and VSWR performance as noted above.

E. Recovery Time

The recovery time of a microwave limiter is the period of time required by the limiter to return to its low insertion loss state after limiting a high power pulse. As all types of limiters exhibit quasi-exponential decay in low level insertion loss from the limiting state, the recovery time is generally defined as the time to reach an insertion loss which is 3 dB above steady state low level insertion loss. The measured recovery time of a limiter is a function of both the limiter component and the conditions under which it is measured.

Figure 8 shows the 3 dB recovery time required by a single stage bulk semiconductor limiter as a function of pulse power for 1 μs pulses with 0.001 duty cycle. The increase in recovery time at higher input powers is the result of thermal heating of the semiconductor volume by the microwave pulse. Recovery can be shortened and power handling capability increased by adjusting the element geometry to minimize the temperature rise in the element during a high power pulse. The recovery mechanism in

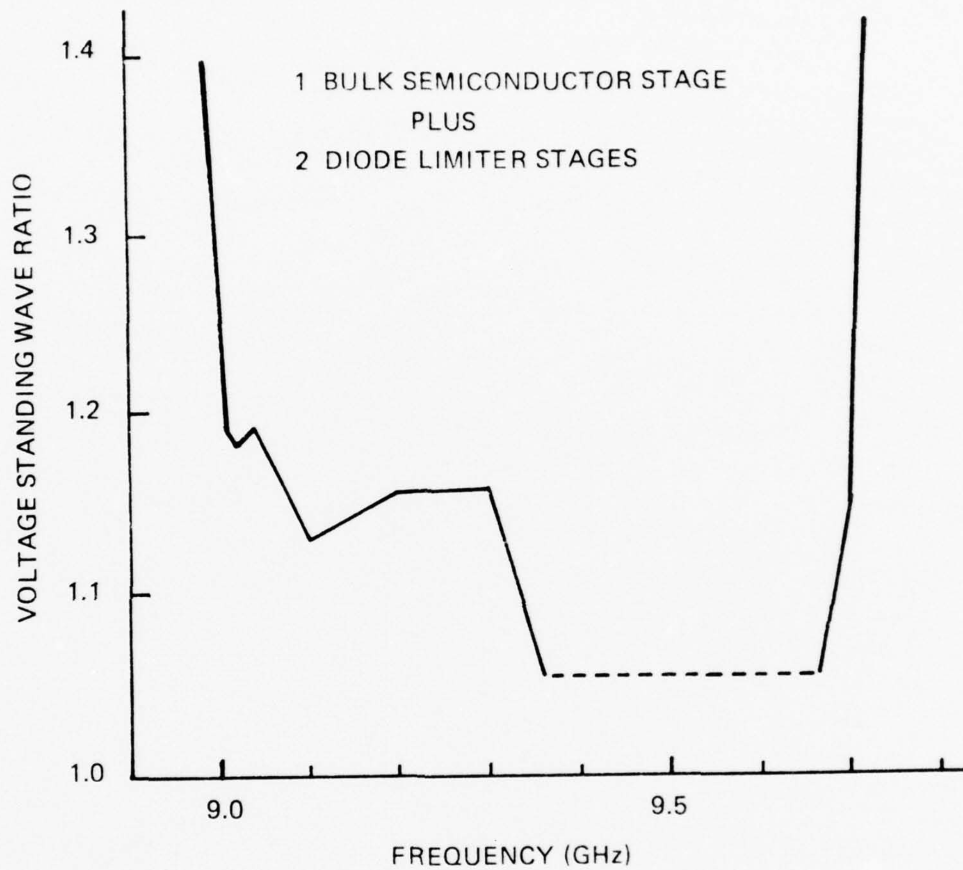

FIGURE 6 MEASURED VSWR OF THREE STAGE SOLID STATE LIMITER

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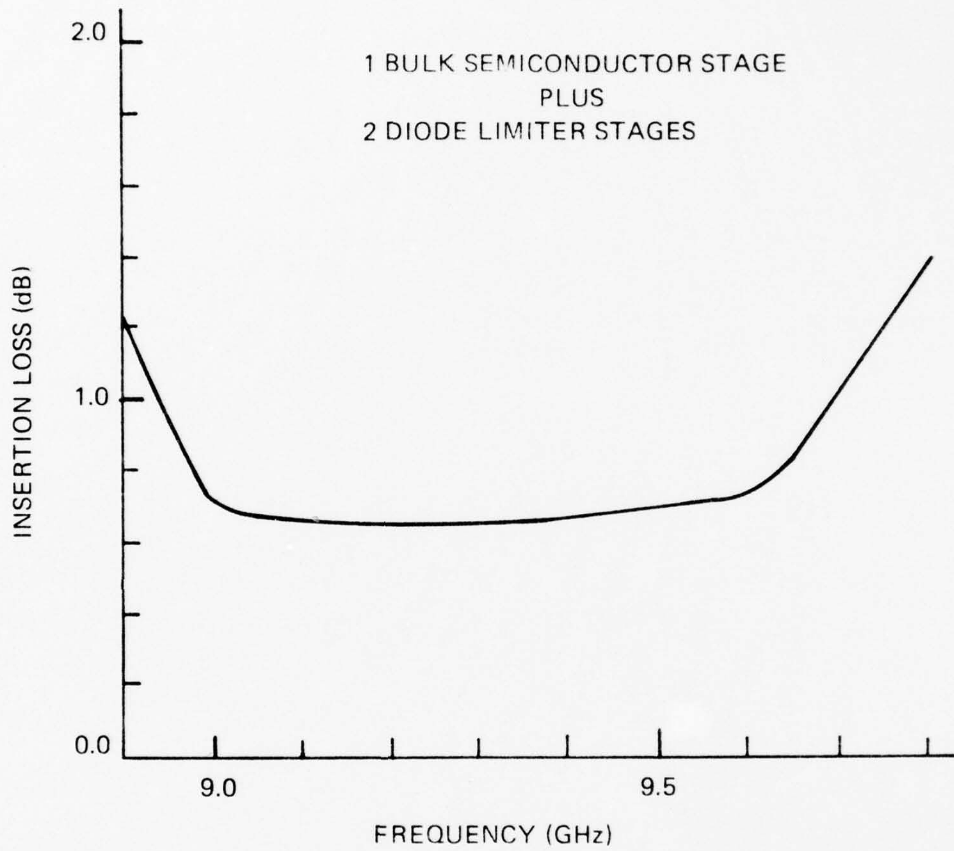


FIGURE 7 MEASURED INSERTION LOSS OF THREE STAGE SOLID STATE LIMITER

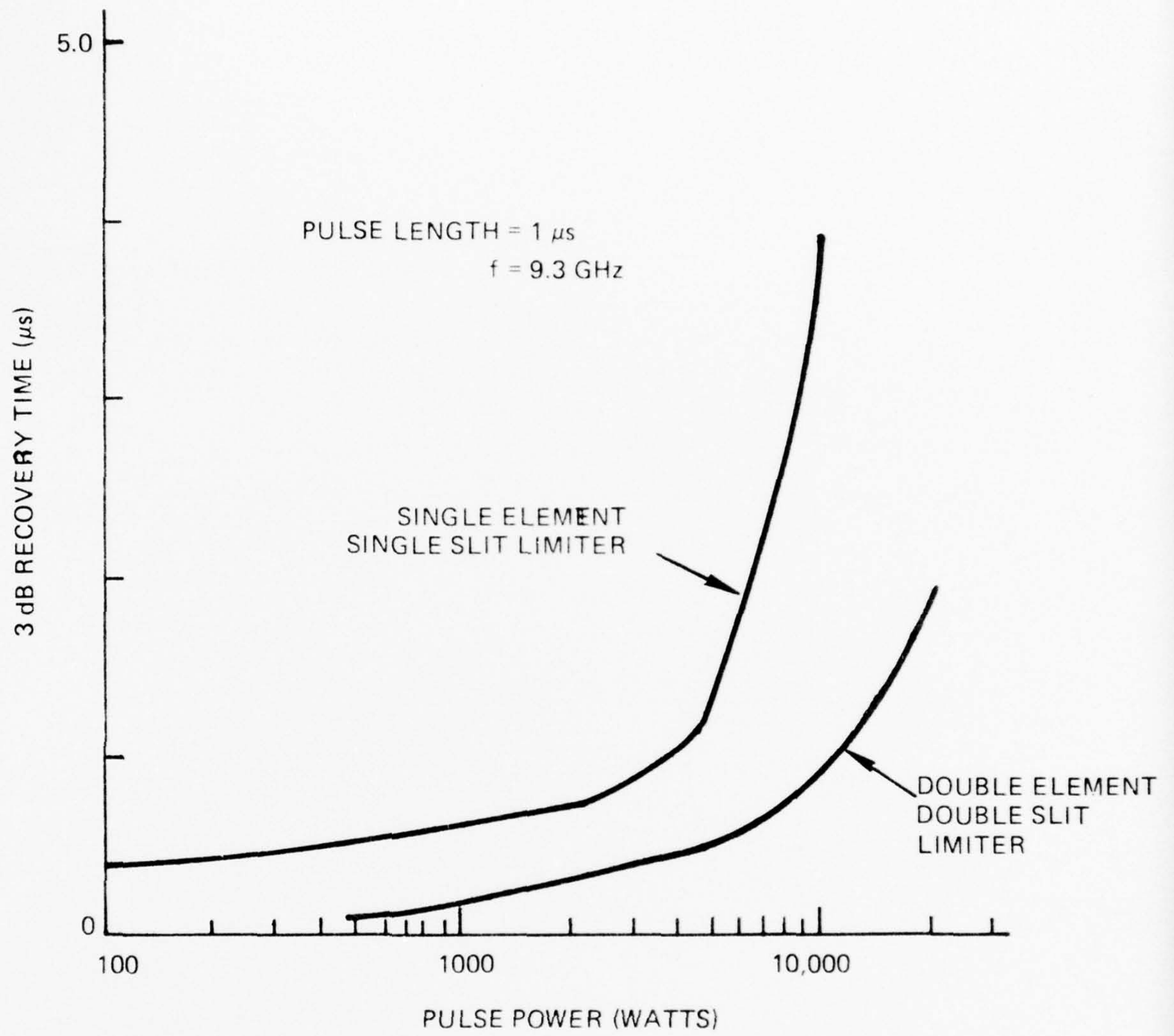


FIGURE 8 BULK SEMICONDUCTOR LIMITER MEASURED RECOVERY CHARACTERISTICS

D-15493

the bulk semiconductor limiter is the recombination of holes and electrons within the bulk and at the contacts of the limiter element. Therefore, processes which accelerate recombination of carriers, such as gold doping, will reduce recovery time, although perhaps at the expense of increasing dissipation loss under the transmit conditions.

The low level PIN varactor limiting stages use drift fields throughout the device to achieve carrier recombination. Therefore, their recovery is rapid and does not materially affect the 3 dB recovery of the complete multistage component.

F. Flat and Spike Leakage

The power transmitted by a microwave limiter during a high power pulse is called leakage power. At the beginning of a high power microwave pulse, the limiter must change from a low loss to high loss circuit element. Thus, there is a short period of time at the beginning of a pulse when the isolation is increasing to a steady state value. During this period, the leakage power (spike leakage) is higher than the steady state leakage power (flat leakage) which occurs later in the pulse.

Spike and flat leakage powers are extremely important as they are the factors that determine if mixer burnout or noise figure degradation will occur in a microwave system. All stages must provide high levels of isolation on both the spike and flat if excessive power levels are to be prevented from entering the receiver.

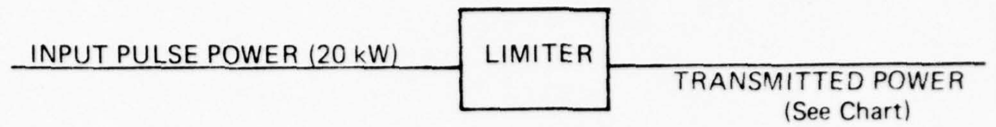
The bulk semiconductor limiter is unique in that it shows highly reliable attenuation of the leading edge of microwave pulses. This feature is in contrast to gass TR tube devices or gas TR tube-semiconductor limiter combinations. The gas TR tube requires either a keep-alive electrode or a radioactive keep-alive source to minimize spike amplitude. Keep-alive is necessary because a very high field is necessary to create a gas plasma

discharge in the absence of free electrons. The plasma must build up in an avalanche fashion over many RF cycles. It is during this build up period that spike leakage occurs.

The bulk semiconductor limiter differs from the gas TR device in two important respects. First, there is a background density of holes and electrons which has a minimum value of 10^{10} carriers/cc in silicon limiter elements. Thus, carriers are present at all times as a starting point for the avalanche process to occur. In effect, these carriers represent a constant high-level of "keep-alive" in the solid device. Second, the avalanche process is much faster in the solid state than in the gaseous state. In the solid state, an electron (or hole) has a lower effective mass than in the gas plasma state. The distance the carrier must travel before reaching an ionizing energy level under avalanche conditions is only 1,000 Å. Thus, the solid state avalanche process is faster than the driving microwave field oscillations and passage of high level unattenuated spikes throught the bulk semiconductor limiter is fundamentally not possible.

Figure 9 shows the pulse shape transmitted by a typical bulk semiconductor limiter as a function of time. The amplitude of the "spike" is only a few dB over the flat leakage amplitude. In double slit limiter units, the attenuation of the spike was measured at greater than 16 dB with 20 kW input pulse powers.

Gas TR tubes permit narrower but higher spike leakage powers to be transmitted. They have no physical mechanism which fundamentally prevents narrow high power spikes from occurring. Spike leakage is controlled by keep-alive design, gas mixture composition, pressure, and so forth. These factors vary with the age and the operating conditions of the tube. This results in unpredictable spike attenuation.



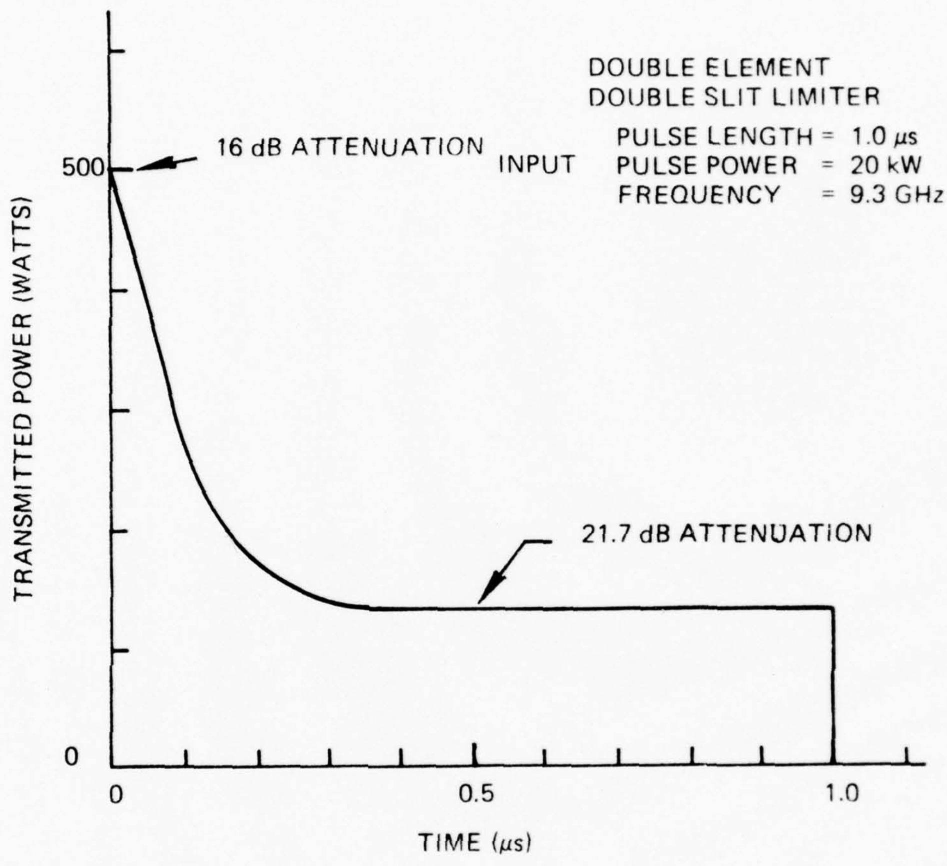


FIGURE 9 BULK SEMICONDUCTOR LIMITER TRANSMITTED PULSE SHAPE

D-15494

It has been found that modern low noise Schottky barrier mixer burnout is a function of maximum (spike) leakage power more than spike energy content. The bulk semiconductor limiter provides high spike attenuation. When combined with a two stage low level diode semiconductor limiter, which also features excellent spike attenuation, absolute, long-life receiver protection will result.

The flat leakage is also important but is not as difficult to achieve as spike leakage. Three limiter stages each capable of providing 20 dB of limiting will more than guarantee adequate flat leakage. A two stage limiter, composed of one bulk semiconductor stage and one diode limiter stage could also provide adequate flat leakage. However, the three stage unit would provide superior spike attenuation.

G. External Bias

External bias is required in older types of gas discharge TR tubes. Its purpose is to provide a "keep-alive" plasma level amplitude required to initiate gas plasma breakdown. Hence, keep-alive is required to reduce spike leakage amplitude and prevent misfiring.

External bias keep-alive has been replaced in newer gas TR designs with radioactive keep-alive. Thus, no external bias is required. It should be noted that radioactive keep-alive does not provide as high an electron density as does biased keep-alive. Therefore, spike leakage is greater with the more recent designs.

The bulk semiconductor limiter requires no keep-alive excitation in any form for its operation. Both the bulk semiconductor stage and subsequent low power stages derive all energy for operation from the incident microwave pulse. There are, therefore, no service life limitations caused by electrode sputtering or radioactive source decay.

H. Arc Loss

The arc loss is the amount of power incident on a limiter divided by the amount of power reflected by the limiter during a high power pulse. It is usually expressed in dB. Absorptive limiters have high values of arc loss and cannot be used as TR switching elements. Reflective limiters absorb some power, but reflect most of the incident power. Arc loss values of 1 dB and 0.5 dB are anticipated for bulk semiconductor limiters which have 20 dB and 25.5 dB flat isolation levels, respectively. Thus, the bulk semiconductor-diode limiter is a useful as a transmit-receive switch as well as a receiver protector.

III. THEORY OF BULK LIMITER OPERATION

A. Basic Operation

The bulk semiconductor limiter in its early stages was a piece of high resistivity silicon with two sintered or diffused ohmic contacts. The contacts were connected to a high impedance microwave transmission line circuit.[1-3] The device has since been developed with improved passivation, circuit and thermal designs.[4-7] A major change in the contact surfaces of the device, checkerboard contacts,[4] has been developed which improves the isolation state performance by permitting microwave fields to cause holes and electrons to be injected into the high resistivity silicon. The new contact structure also accelerates recombination of holes and electrons after a microwave pulse has terminated; thus, it reduces the recovery time of the device to the order of one microsecond from previous values of approximately ten microseconds.

In operation at low microwave field intensities the bulk limiter element with checkerboard contacts behaves as a high Q capacitor. Thus, if it is incorporated into a parallel resonant circuit shunting a waveguide, microwave signals will pass with minimal attenuation at the resonant frequency. At higher power levels the microwave electric field across the device causes both electrons and holes to be injected into the high resistivity bulk region of the device. These carriers reduce the resistivity of the bulk element and changes its characteristics from a high Q capacitor to a capacitor with shunt conductance. The table below shows conductivity values calculated from microwave limiting data of bulk limiters at 9.3 GHz as a function of rms microwave field intensity.[7]

E (V/cm)	θ (mho/cm)	ρ (ohm/cm)
100	3.33×10^{-4}	3000
1,000	1.12×10^{-3}	891
10,000	1.48×10^{-2}	67.7
20,000	4.76×10^{-2}	21
40,000	3.0×10^{-1}	3.3

The isolation state with increased conductance is a non-equilibrium state much like a PIN diode under forward bias. The major difference between the bulk limiter and a thick based PIN diode is the contacts. The checkerboard limiter can be self-biased into conduction by a microwave field while a PIN can not. For this reason a thick based PIP, NIN, or PIN structure would all be expected to perform similarly with no limiting until an avalanche field intensity is reached somewhere within the device.

B. Microwave Field Conductivity Modulation

Figure 10 shows an exploded view of a section of a checkerboard contact limiter element. Checkerboard P-N doped contacts are present on each side of the limiter element. The central region is high resistivity silicon which is typically about 3 mils thick.

Figure 11 shows the effect of applying a high level microwave field across the device. Only the top contact is shown, but it will be understood that the bottom contact functions in the same manner. In Figure 11 the excess mobile carrier distribution is shown before bias is applied; there are no excess carriers. In Figure 11 the carrier distribution as a result of the first positive half cycle is shown. Mobile carriers, holes, build up a space charge within the intrinsic material. During the negative half cycle, most of the holes are removed by the electric field. The holes near the shorted P-N junction of the contact surface are not removed, however, as their space charge is neutralized by extra electrons injected by the N doped region. This

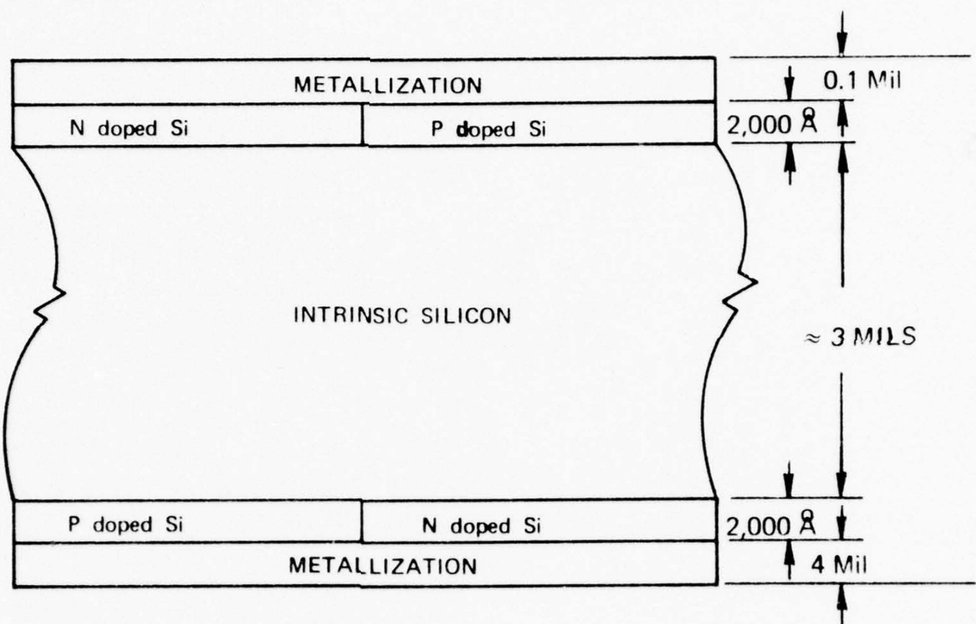
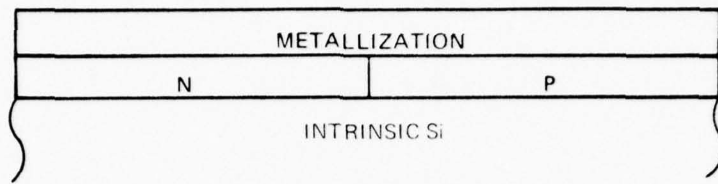


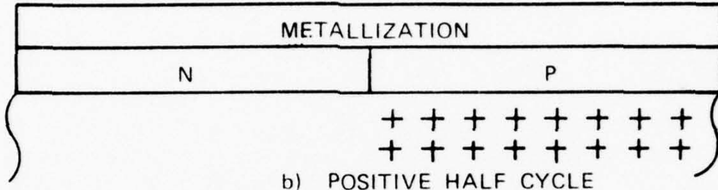
FIGURE 10 SECTION OF A CHECKERBOARD LIMITER ELEMENT

D–15312

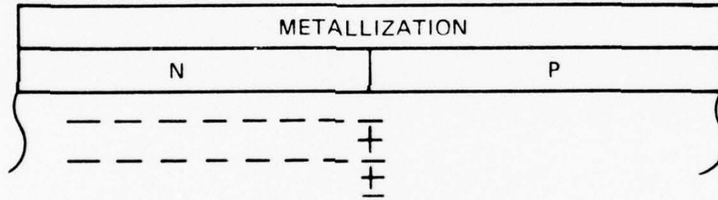


a) NO BIAS

E

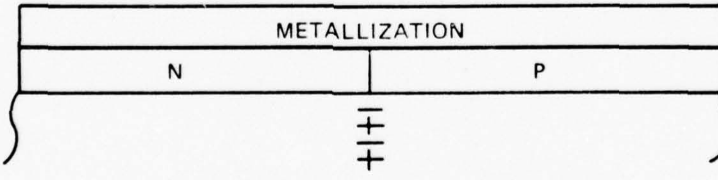


b) POSITIVE HALF CYCLE



E

c) NEGATIVE HALF CYCLE



d) AFTER ONE COMPLETE CYCLE

FIGURE 11 EXCESS MOBILE CHARGE DISTRIBUTION CAUSED BY HIGH LEVEL MICROWAVE

D–15311

effect is shown schematically in Figure 11c. At the end of a complete cycle the excess mobile carrier distribution is as shown in Figure 11d.

The net effect of the checkerboard contact structure is to permit a neutral hole-electron plasma of excess carriers to be injected at the shorted surface P-N junctions in response to an applied microwave electric field. This plasma has the effect of modulating the bulk conductivity of the intrinsic region so the increase in shunt conductivity across the device terminals can be used to produce a limiting phenomenon. After a short turn-on (spike leakage) period, the plasma is distributed substantially uniformly throughout the intrinsic region of the limiter element.

C. Recovery from the Plasma Limiting State

The hole-electron plasma which causes the limiter to exhibit isolation performance is present at the end of the high power microwave pulse. After the pulse is over, the plasma must recombine or otherwise be removed from the intrinsic region before the device can return to its low level transmission state. In a PIN diode the built in electric field at the P-I interface prevents electrons from entering the degenerate P region and recombining. Also a similar field at the N-I junction prevents holes from entering the degenerate N region and recombining there.

Figure 12 shows the electric field distribution that is always present at the interface between intrinsic silicon and a checkerboard contact. Far from the shorted surface junction the fields are as they would be in a normal N-I or P-I junction; hence, little recombination occurs there. Near the shorted junction, however, a large electric field exists which drifts excess holes into the P doped contact region and excess electrons into the n doped region. This carrier flow causes an equal current to flow in the metallization layer which shorts the N and P region. The contact surface behaves very much like a shorted silicon photo cell junction. Thus, the checkerboard contact has a matrix of shorted P-N junctions whose built-in

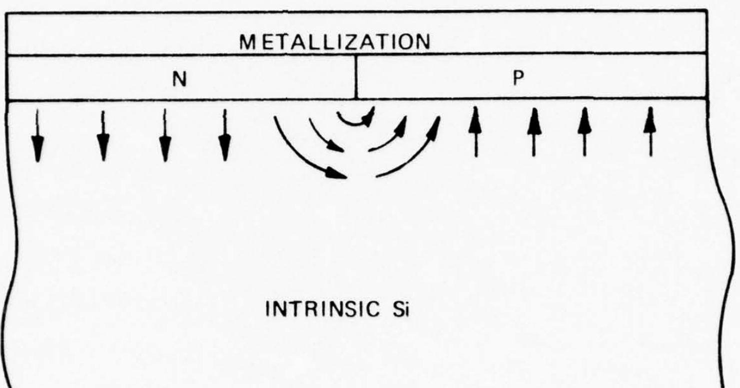


FIGURE 12 BUILT IN ELECTRIC FIELD DISTRIBUTION AROUND CHECKERBOARD CONTACT STRUCTURE

D-15313

potential recombines holes and electrons when no microwave field is present.

It is this high rate of surface carrier recombination caused by the checkerboard's shorted junctions that is responsible for the rapid recovery of the bulk limiter to the dielectric transmission state from the conductivity modulated isolation state.

IV. FABRICATION OF BULK LIMITERS

A. Limiter Fabrication Constraints

The theory of bulk limiter operation was presented in Section III of this report. The object of this section is to present the overall fabrication processing which must be done to build functional bulk limiters.

At the outset, it is important to realize that the structure and materials requirements dictated by the bulk limiter's eventual microwave specifications rule out certain fabrication procedures and mandate others. For example, recovery time specifications together with the diffusion and drift of non-equilibrium carriers toward the contact surfaces for recombination at those surfaces require that the device thickness be on the order of 3 mils or less.

At the same time a requirement exists for extremely high bulk resistivity in the bulk intrinsic layer. The bulk resistivity should be greater than 8000 ohm cm in order to meet low level insertion loss goals. High resistivity uncompensated silicon cannot be grown by epitaxial processes. Thus, the use of epi wafers in bulk limiter fabrication is ruled out and all processing must be done using very thin float zone refined silicon wafers.

A second constraint is imposed by the nature of the power dissipation pulses within the limiter element. The power is dissipated in short high power pulses whose energy is largely stored in the heat capacity of the silicon and is slowly removed from the device by thermal conduction in the long period between pulses. Thus, the junction thermal resistance is important for average power considerations, but has little effect on peak power capability. For peak power, it is much more important that the metal contact material have a combination of high thermal conductivity and high specific heat. If this is the case, the contacts will store a significant fraction of pulse dissipated energy <u>during</u> the pulse, prevent high power burnout due to high temperature metal

semiconductor junctions and provide low temperature surfaces which recombine excess holes and electrons after the microwave pulse has terminated. Consequently, the bulk limiter fabrication process uses plated gold heat sinks on the plane side of the limiter and a diffusion bonded gold wire on the dot side of the limiter element.

A third constraint on bulk limiter design is imposed by the high electric fields surrounding the device during a high power pulse. The geometry in the region between the dot contact and the exposed high resistivity surface must be controlled to prevent surface, encapsulant, or air breakdown in this region. It is also found that excess parasitic capacitance of encapsulant in this region results in a direct trade-off with bulk limiter bandwidth and insertion loss, or alternately a direct trade-off with power handling capability. Hence, the fabrication technology used must minimize parasitic capacitance and field concentrations around the dot contact on dot-plane limiter elements.

B. Wafer Processing

During the last quarter, 15 high resistivity silicon wafers with resistivity ρ = 8000-10000 Ωcm were processed for the fabrication of bulk limiters. First, silicon wafers were thinned down to 3.0 mil thickness by polishing and etching techniques. Then, the wafers were phosphorous diffused (900°C 1050°C) for 30 minutes using $POCl_3$ diffusion system. After the completion of phosphorous diffusion, the phosphorous doped glass on the wafer surface was etched in hydroflouric acid and 1000 Å of a silicon dioxide (SiO_2) glass was thermally grown at 1000°C. At this point the two surfaces of the wafers are identical as shown in Figure 13.

Both surfaces of the wafer were then photo-processed in sequential operations which transfer the 0.5 mil checkerboard pattern of the photoresist mask to the silicon wafer. The checkerboard pattern windows were then etched through the SiO_2 and phosphorous doped silicon layers by using buffered hydroflouric acid and 12:1:1 (HNO_3:HF:CH_3COOH) respectively. After the silicon etching, the wafer surface had elevated squares of phosphorous doped silicon covered with glass

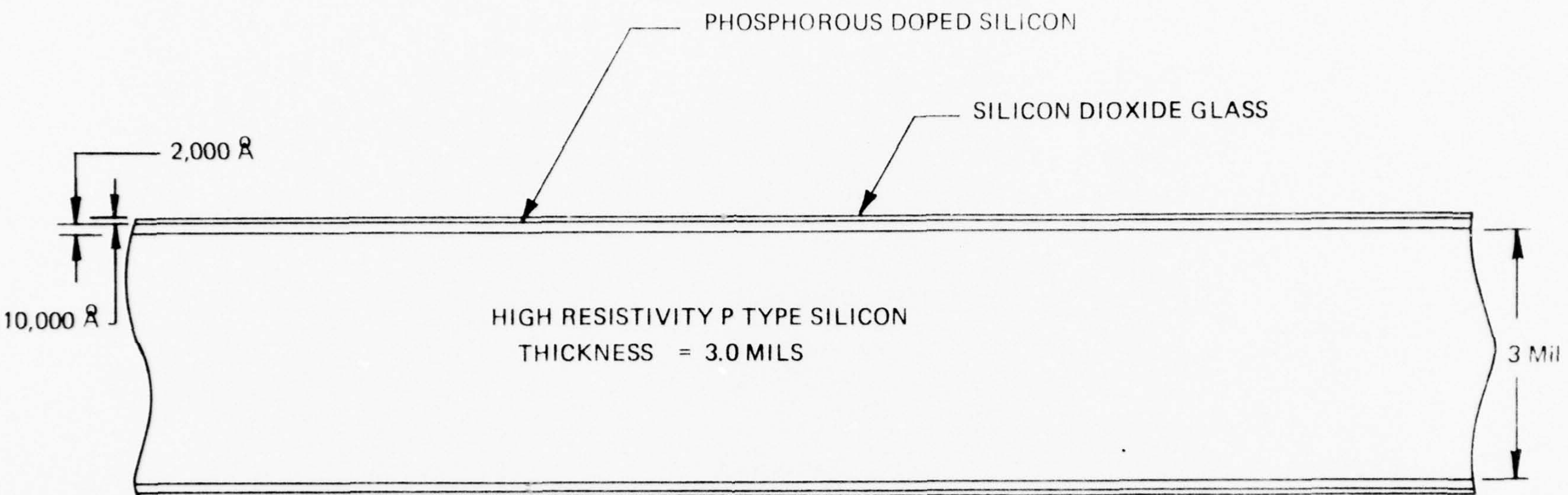


FIGURE 13 **LIMITER WAFER AFTER OXIDATION PROCESS**

D-15322

and depressed areas of exposed undoped silicon. The wafer was then diffused with boron at 1000°C for 20 minutes using a BN source. The boron diffused wafer was then etched in hydroflouric acid to remove all glass from the wafer surfaces. The wafer at this processing stage is shown in Figure 14 with raised phosphorous doped layers and depressed boron doped layers.

The fact that the two types of dopant are on squares at slightly different levels into the silicon is the result of fabrication convenience rather than design necessity. In fact, it can be shown that if the levels of the two dopants are too widely separated, the microwave injection and recombination characteristics of the resulting devices will be degraded. Small level variations, however, should not adversely affect microwave performance.

Both surfaces of a wafer were metallized with 500 - 1000 Å layer of chromium and 2000 - 3000 Å layer of gold. The evaporation was conducted in an NRC evaporator, Model #3117, and wafer was held at a temperature between 80°C and 120°C during the evaporation. Figure 15 shows the limiter wafer after chrome-gold metallization and at this stage both surfaces are identical. The thin evaporated gold layer on each surface of the wafer was then chemically electroplated with pure gold. One surface was plated to a thickness of 0.1 mil while the other was plated to a thickness of 4.0 mils. The bulk limiter wafers were then saw cut into 40 mils squares, and were separated into individual limiter chips as shown in Figure 16.

C. Chip Fabrication

The limiter chip of Figure 16 has a thick gold plate on one side which is used as a heat sink and heat spreader in the completed chip. The opposite gold plated surface has a thin layer of gold to which a gold wire (nominal diameter equals 8 mils) is duffusion bonded using heat and pressure. The bonding technique is similar to TC or nail head bonding with the exception that the forces used in making the bond are significantly below those required to perform the more conventional bonds. The peak bonding pressure is 25,000 psi. The prime advantage of this technique is that only minimal deformation occurs during the bonding process. Thus,

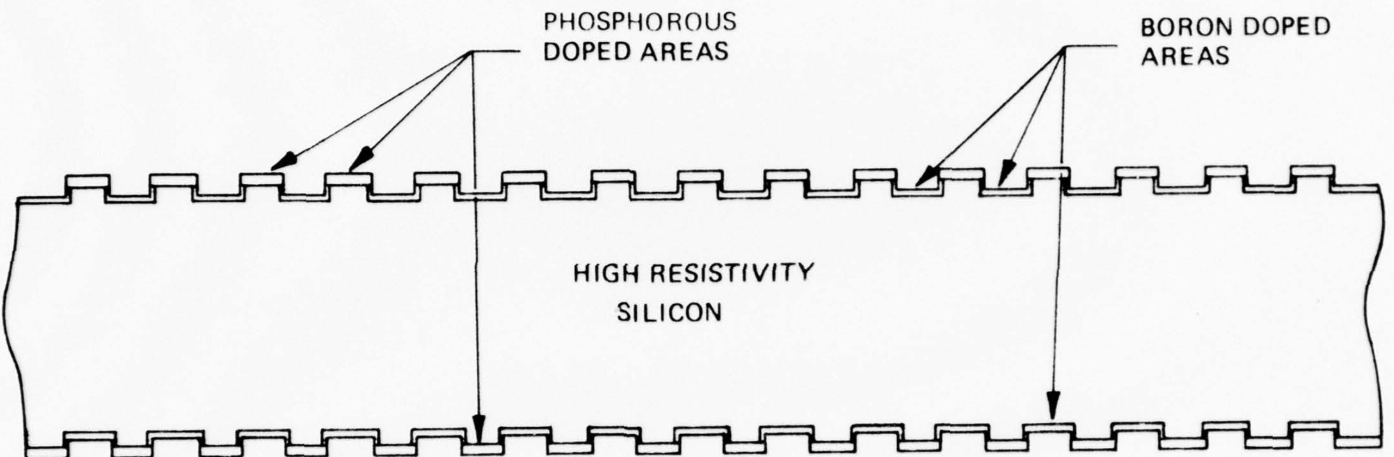


FIGURE 14 **SILICON WAFER WITH DIFFUSED CHECKERBOARD CONTACTS**

D-15321

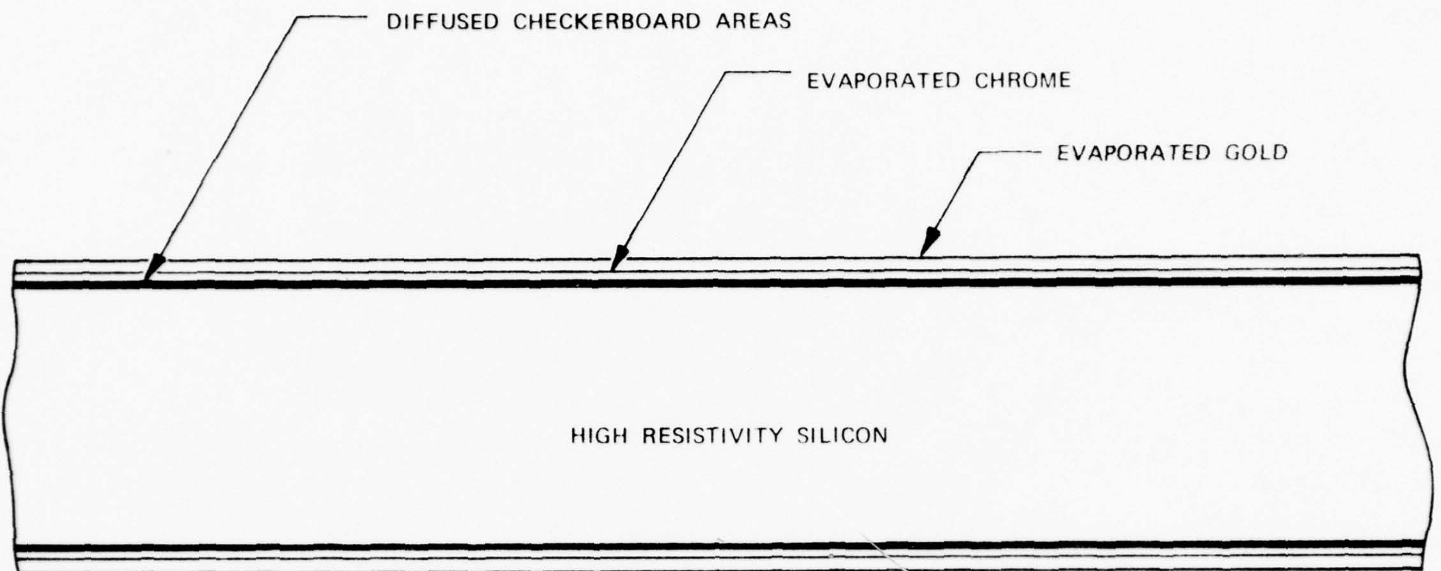


FIGURE 15 LIMITER WAFER AFTER METALLIZATION

D-15314

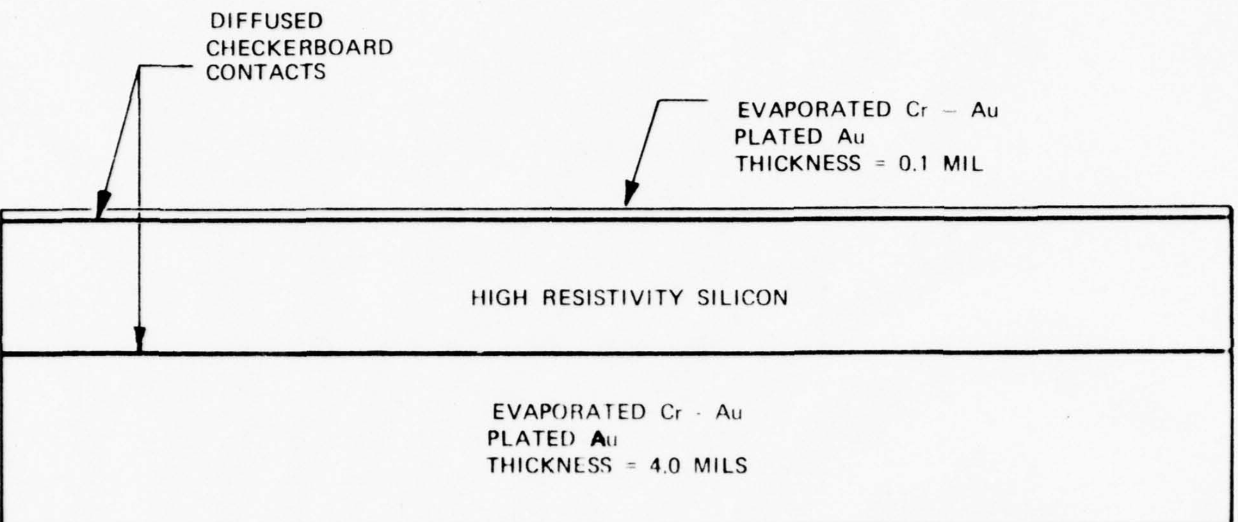


FIGURE 16 **SEPARATED LIMITER CHIP**

D – 15320

accurate control of the bond area and geometry can be maintained using the diffusion bonding technique. Figure 17 shows a bulk limiter chip after diffusion bonding. Note that the original plated gold-wire interface has disappeared.

The chip with its gold diffusion bonded wire was then etched in a sequence of gold, chrome, and silicon etches to produce the mesa structure shown in Figure 18. A passivation glass of silicon nitride was deposited on the exposed high resistivity silicon surface to prevent inversion layer conductivity from degrading microwave performance. The typical DC characteristics, i.e., capacitance and conductance, are given in Table I. The bulk limiter chip was then mounted in an X-band brass iris and was also coated with polymide encapsulation to prevent arcing under high RF power.

FIGURE 17 CHIP WITH DIFFUSION BONDED GOLD WIRE

D–15319

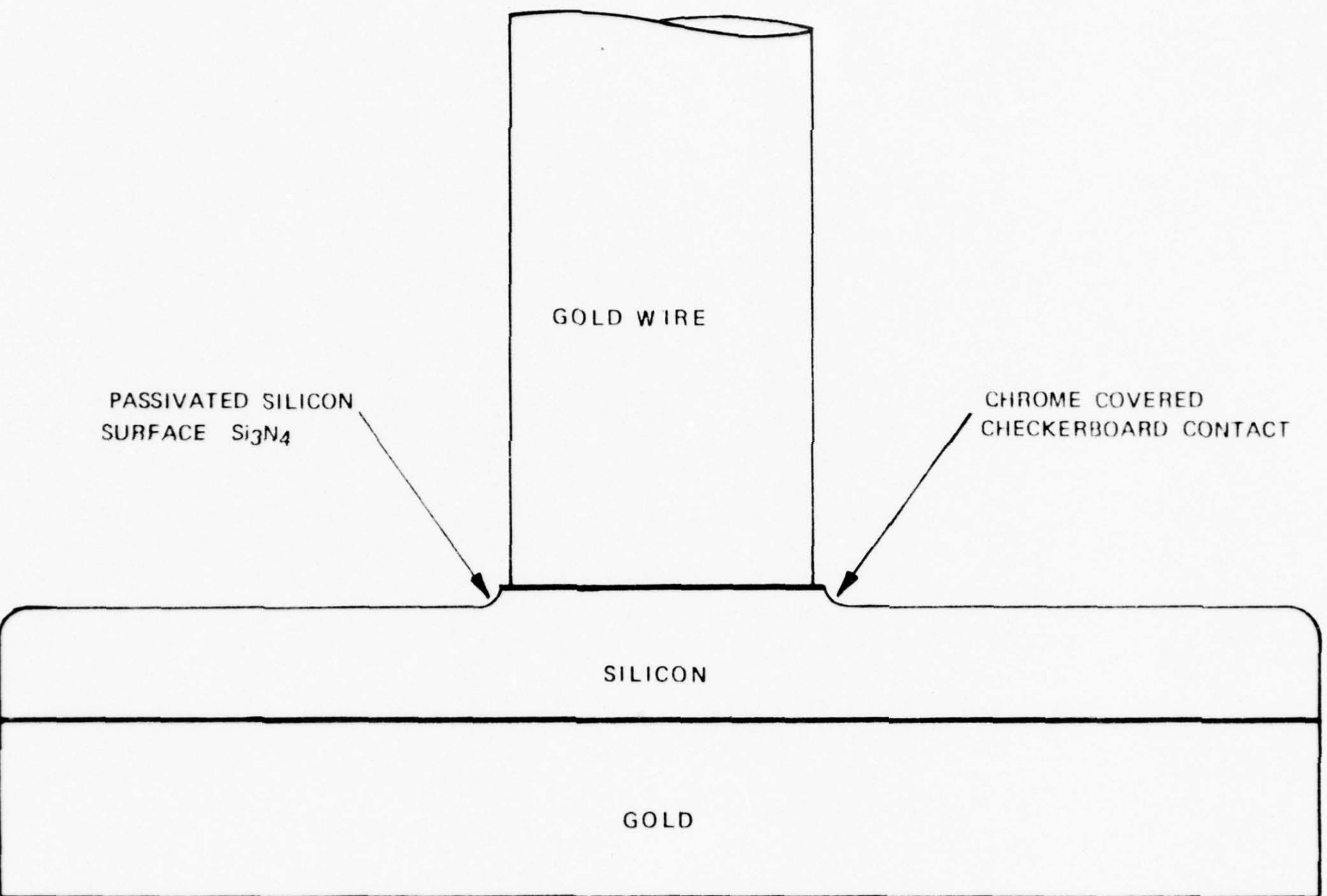


FIGURE 18 COMPLETED CHIP READY FOR IRIS MOUNTING

D-15318

BULK LIMITER NO.	CAPACITANCE IN pF*	RESISTANCE IN OHMS*
BL1-3	0.125	700 K
BL1-4	0.160	2000 K
BL1-5	0.145	1800 K
BL1-6	0.150	1500 K
BL1-7	0.160	1500 K
BL1-8	0.165	1200 K

*Zero Bias at 1 MHz using Boonton Capacitance Bridge Model No. 75D

TABLE I

DC CHARACTERISTICS OF BULK LIMITERS

V. FABRICATION OF THE BULK-DIODE LIMITER ASSEMBLY

The bulk-diode limiter assembly consists of the bulk limiter followed by a two stage diode cleanup limiter. In addition, tuning screws are used to achieve broadband performance.

A. Cleanup Limiter Assembly

The diode limiter is a widely used and thoroughly proven device. The main switching element in a limiter is the diode itself. The parasitic reactances associated with the packaged diodes must be resonated out with opposite ones. One way to do this is to use a waveguide to coaxial transformation which can be designed to both match and broadband the device. Figure 19 shows a sectional view of a diode limiter. The abrupt step to reduced height guide and the shunt mounted post form the transformation. The diode is placed in the coaxial line. The line continues through a folded, radial RF choke to a bypass arrangement which RF shorts the line to ground while allowing the diode to be DC biased.

Figure 20 shows an equivalent circuit of the diode mount. The abrupt reduction in waveguide height represents capacitance C_R. This is followed by a short length of line, L_I, of impedance Z_R. Transformers, T, match this line to the coaxial line of effective impedance Z_o, with the diode transformed to appear in shunt with the transmission line. The diode consists of a package capacitance, C_p, a junction capacitance, C_j, series resistance, R_s, and series inductance L_s. C_s and L_p are the tuning reactances obtained by adjusting lines l_3 and l_2 shown in Fig. 19.

Figure 21 shows a simplified equivalent circuit of the diode in the forward and zero bias states. Thus, tuning of the diode limiter involves adjusting the position of the RF choke and the diode's parasitic reactances.

Figure 22 shows the actual diode limiter being used for this program. Two stages of limiting are used in order to achieve enough isolation. The input stage is a high power PIN diode which does the main limiting job. The output stage is a low power varactor used for additional cleanup isolation. A detector diode is used to provide DC bias to the limiter diodes.

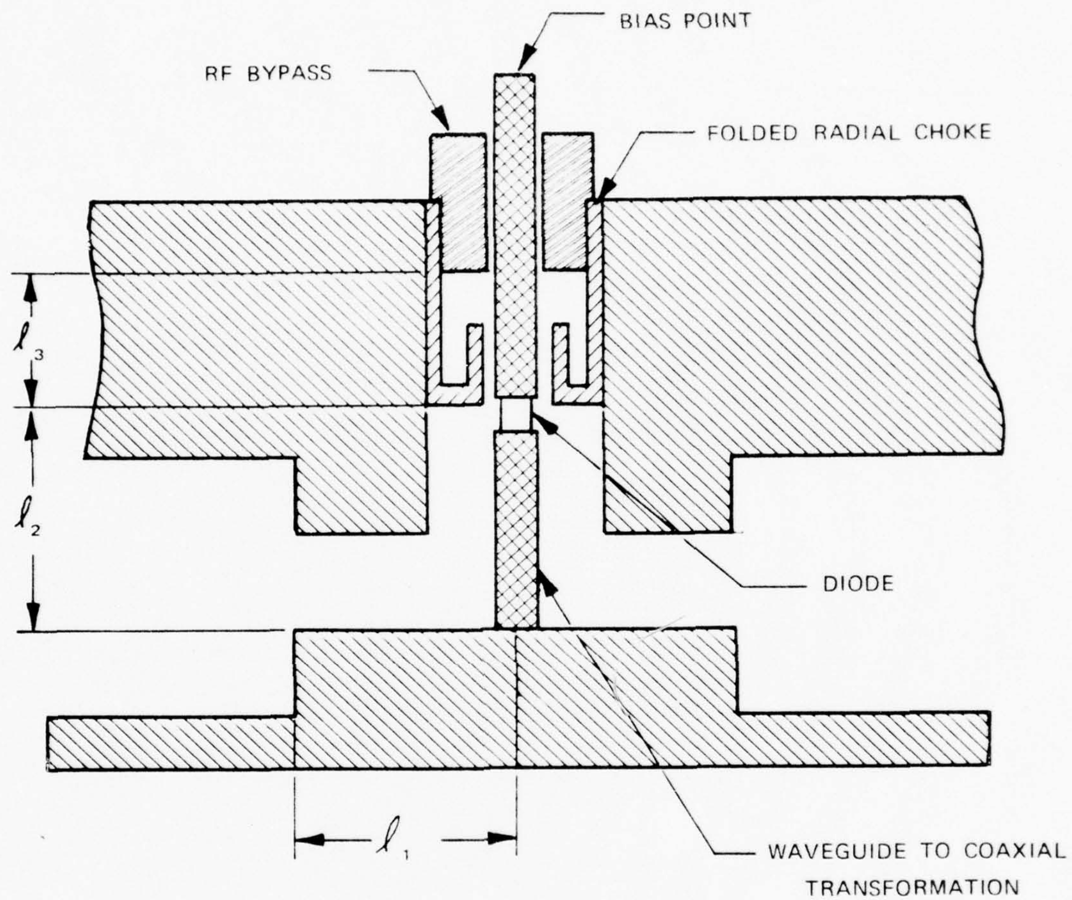


FIGURE 19 DIODE LIMITER CROSSECTION

D–15309

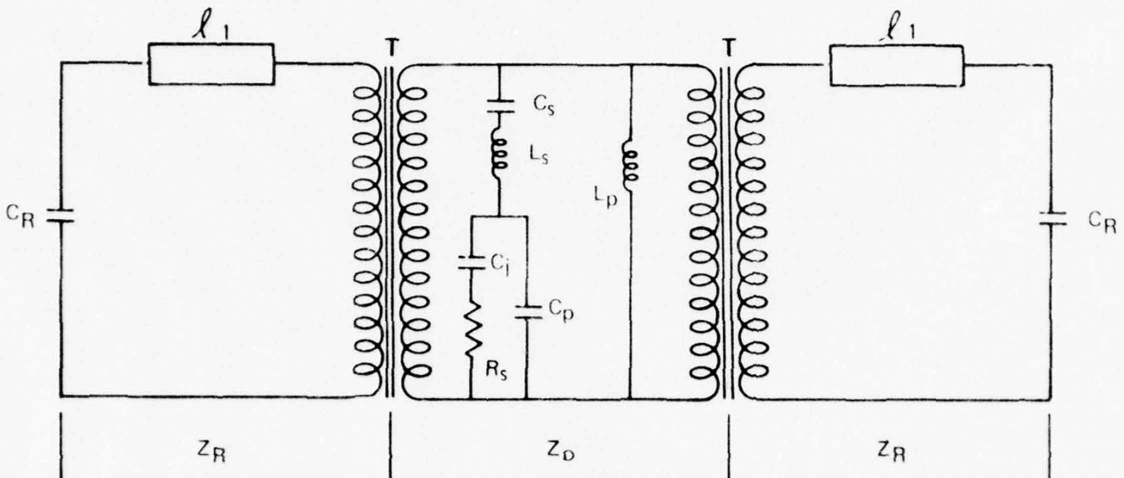
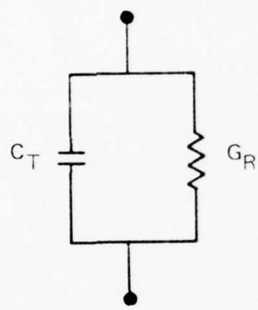


FIGURE 20 EQUIVALENT CIRCUIT OF A DIODE MOUNT



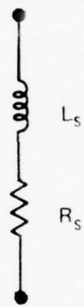


FIGURE 21 SIMPLIFIED DIODE EQUIVALENT CIRCUITS

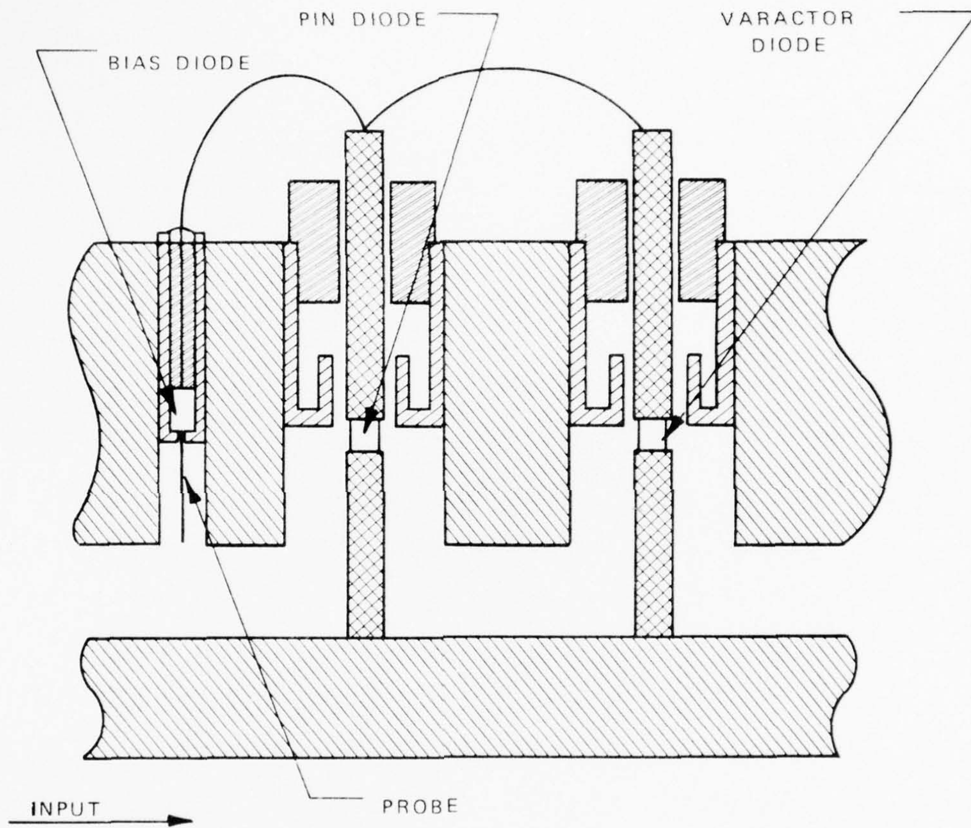


FIGURE 22 CLEANUP LIMITER CROSSECTION

Figure 23 shows a schematic of the biasing arrangement. The resistor is used to provide the diodes with a discharge path to ground. This is necessary to shorten the recovery time. This type of limiter design is a highly reliable one. It will withstand environmental extremes of temperature, shock, vibration, humidity, etc. without degradation. Its insertion loss is only 0.4 dB while it provides a minimum of 40 dB isolation across the band.

B. Bulk-Diode Limiter Package

The bulk-diode limiter package which comprises the first engineering samples is shown in Figure 24. In combining the bulk limiter with the diode limiter, it was necessary to use tuning screws to achieve optimal broadband performance. The bulk limiter is a very narrow band device. The effect of the tuning screws is to transform into and out of the bulk limiter stage. Thus, it becomes better matched across the band.

The relative spacings of the screws, the bulk limiter and the cleanup limiter are also critical. Much time was spent in experimentally determining the spacings which would give optimal broadband performance.

One of the goals of this program is to be able to replace bulk limiters without the need for retuning the package. Some experimentation has been done along these lines. It has been found that, in order to achieve this goal, the bulk limiters must be very consistent and uniform.

The technique used to obtain replaceable bulk limiters is to tune each bulk limiter in a standard, fixed package. Unfortunately, once the bulk limiter has been constructed, the only tuneable parameter is its center frequency. Thus, care must be taken in the manufacture of the bulk limiters to ensure a consistent and uniform quality in such untuneable parameters as insertion loss and bandwidth.

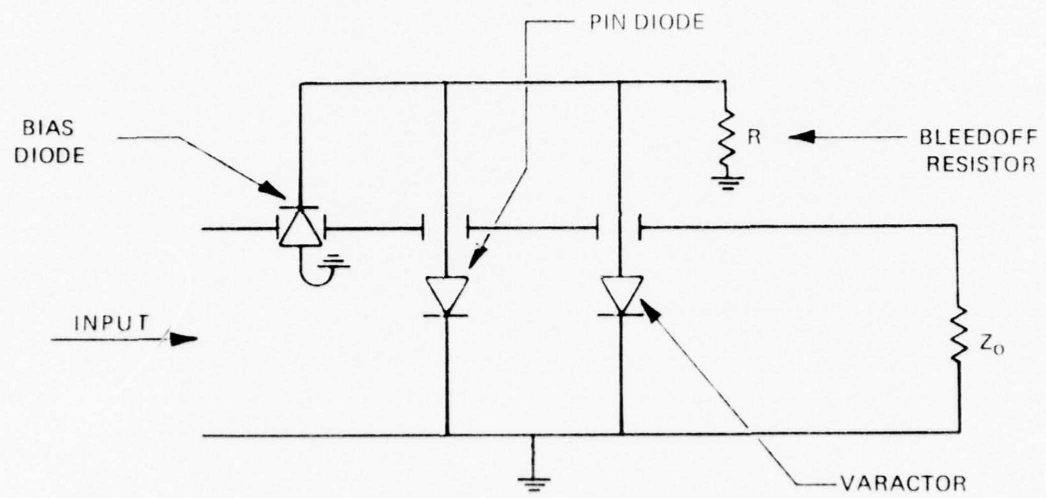


FIGURE 23 **CLEANUP LIMITER SCHEMATIC**

D–15315

FIGURE 24 **BULK DIODE LIMITER**

D-15307

VI. MICROWAVE MEASUREMENT FACILITIES AND TEST RESULTS

A. Low Power Test Facility

The low power microwave test is shown in Figure 25. It consists mainly of an X-band Alfred sweep oscillator (Model #8000/7051) and an Alfred network analyzer (Model #650). This test set up is used to tune the device for center frequency, low VSWR and insertion loss.

The sweep oscillator generates an output which covers the 9.0 - 9.65 GHz band. It also provides a horizontal sweep for the network analyzer. The precision attenuator is set so that the power incident upon the device under test is generally below 1 mW.

The two 10 dB directional couplers measure the incident and reflected power of the device under test. The network analyzer compares these two signals to measure return loss. Then VSWR is calculated from the return loss measurement.

The 10 dB coupler behind the device under test samples the power transmitted through it. The network analyzer then compares this signal with the incident power to measure insertion loss.

B. High Power Test Facility

The high power test facility is shown in Figure 26. It consists of a high power X-band magnetron, Model WE 2J51 and a modulator (Model MA 12330) this system is capable of generating 40 kW with .001 duty cycle. The magnetron generates the microwave power while the modulator controls the pulse and duty cycle conditions.

The circulator serves two functions. First, it protects the magnetron from the power reflected by the device under test. Second, it provides a way of injecting the echo source (Varian Klystron Model No. X-13) signal into the main line. The echo signal permits recovery time measurements to be made. The echo signal enters the circulator and is reflected from the magnetron out to the device under test.

The amount of power in the main RF line is sampled by means of the crossguide coupler. The power meter measures average power. The peak power in

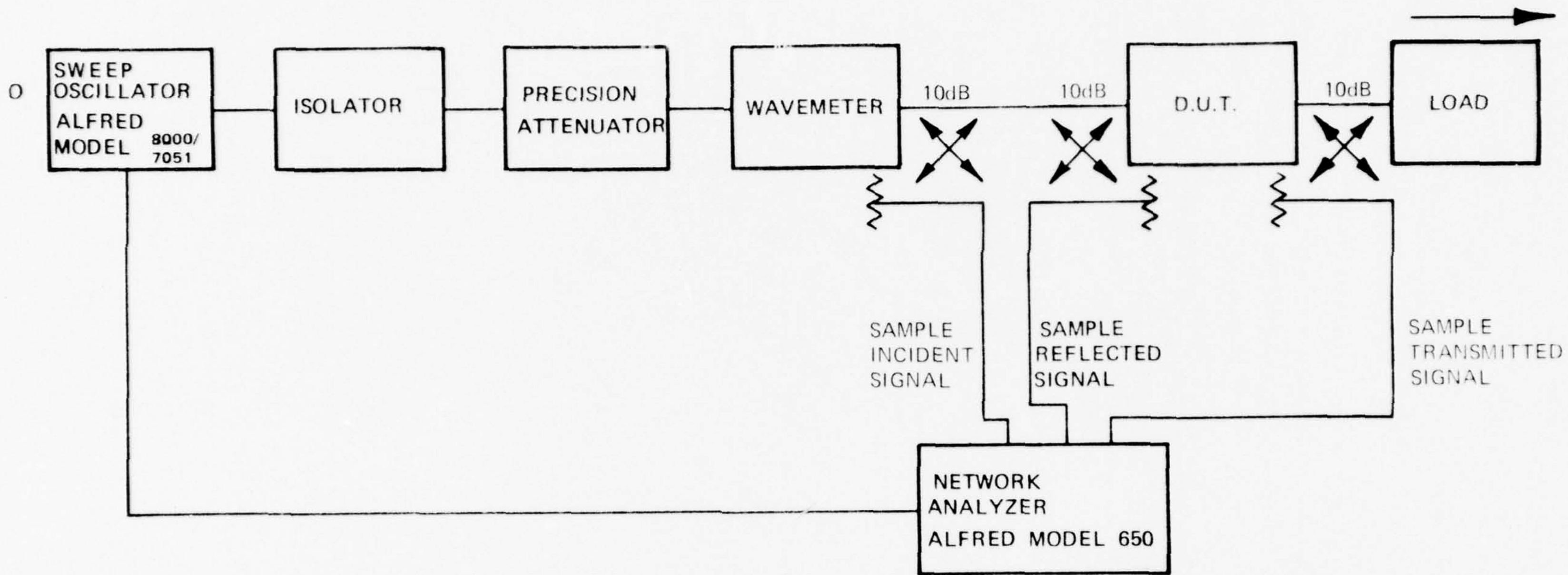


FIGURE 25 **LOW LEVEL MICROWAVE TEST FACILITY**

D – 15317

OSCILLOSCOPE

POWER METER

DETECTOR

TRANSITION

THERMISTOR MOUNT

PRECISION ATTENUATOR

FREQUENCY METER

HIGH POWER TERMINATION

D.U.T.

TRANSITION

MAGNETRON WE 2J51

CIRCULATOR

CROSSGUIDE COUPLER

ATTENUATOR

MODULATOR MA 12330

ISOLATOR

HIGH POWER TERMINATION

TRANSITION

ECHO SOURCE VARIAN X13

FIGURE 26 MICROWAVE HIGH POWER TEST FACILITY

D-15320

the main line is calculated by dividing the average power by the duty cycle. The frequency meter is used to measure the RF frequency in the main line.

C. Flat and Spike Leakage Measurement

Following the device under test are a precision attenuator and a detector. The detector is calibrated so as to give an arbitrary deflection on the oscilloscope for a 10 mW input. The spike and flat leakage through the device under test are determined by adjusting the precision attenuator such that the oscilloscope presentation is returned to the previously determined reference level. The amount of leakage power being measured is then equal to the precision attenuator setting (dB) above 10 mW.

D. Recovery Time Measurement

Recovery time is defined as the time between the end of the RF pulse and the point at which the device under test has returned to within 3 dB of its insertion loss state. For this measurement, echo signal is introduced along with the magnetron power. The oscilloscope presentation for the recovery measurement is shown in Figure 27. The precision attenuator is varied so as to determine a point which is 3 dB below the steady state level of the echo signal. The recovery time is measured using the calibrated oscilloscope.

E. Test Results

A number of bulk limiters were tested for their RF performance using the techniques and test set ups described above. These results and test results of a bulk-diode limiter package are shown in Table II. As can be seen from Table II, the bulk limiters can handle from 10 - 25 kW RF power, however, the recovery time and insertion loss are higher than desired and will be investigated during the second quarter.

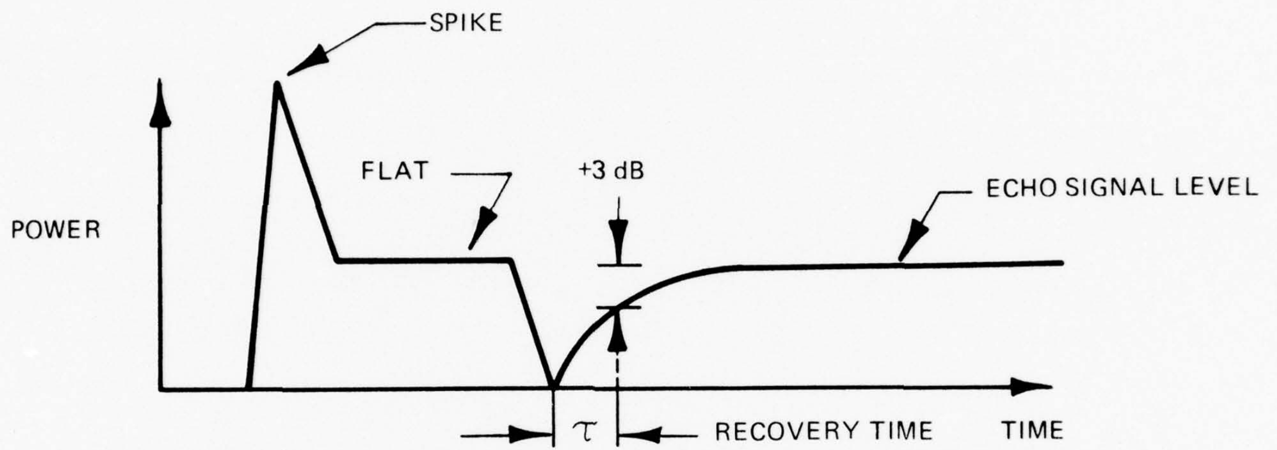


FIGURE 27 RECOVERY TIME MEASUREMENT

D-15333

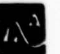


TABLE II

BULK LIMITER TEST RESULTS

S/N	fo	3 dB B.W.	Li	Pin	Pf	Ps	ts	Rt
		9560						
30 - R	9280	8990	.9 dB	5 KW	10 W	45 W	25 ns	.75 μs
				7.5 KW	12 W	55 W	25 ns	.75 μs
				10 KW	16 W	65 W	25 ns	1.0 μs
				30 KW	30 W	100 W		2.4 μs
		9670						
21	9290	8950	1.7 dB		ARC $<$ 1 KW			
		9280						
13	8980	8650	1.1 dB		B.O. @ 4 KW			
		9490						
1	9090	8680	1.0 dB	5 KW	16 W	60 W	20 ns	1.0 μs
BL1B-1	10705	11140	.8 dB	2.5KW	40 W	200 W	20 ns	1.0 μs
		10230						
BL1B-2	10600	11090	1.0 dB		B.O. $\approx$1 KW			
		10100						

BULK-DIODE LIMITER TEST RESULTS

S/N	Freq.	Li	VSWR	Pin	Pf	Ps	ts	Rt
	9.0 GHz	1.0	1.20	15 KW	50 mW	1.6 W	8 ns	2 μs
30-R	9.3	1.0	1.32	8 KW	20 mW	1.0 W	5 ns	2 μs
	9.65	1.1	1.46	10 KW	$<$10 mW	.5 W	5 ns	2 μs

VII. PROBLEM AREAS

Several problem areas become apparent during the first quarter.

A. Diffusion Bonding

First, poor initial yields were obtained in the diffusion bonding process, where the gold wire is bonded to the bulk limiter chip area. Identification of pressure, temperature, and time parameters improved the yield significantly, but the process is still slow and limits production capability. A batch fabrication process has been outlined and will be further developed during the second quarter to eliminate this problem.

B. Surface Passivation

The low temperature pyrolytic silicon oxide passivation on the wire bonded bulk limiter was found to be difficult to duplicate due to the low process temperatures required. This problem has apparently been solved by replacing the pyrolytic SiO_2 with an RF sputtered layer approximately 1000 Å thick. Both DC shunt conductance and microwave insertion loss stability indicate that the passivation is acceptable.

C. Encapsulation

Problems were encountered with the polyimide encapsulant used in the device high field region. The problem centers around the difficulty in obtaining proper adhesion to the passivated device surface. Methods are under investigation to improve encapsulant yield by using addition cureable polymide resin as opposed to a solvent based resin system.

D. Bulk Limiter Tuning

Broadband tuning of the bulk limiter stage was successfully accomplished using tuning screws on each side of the bulk limiter. However, it was noted that by using this technique the peak power handling capability was reduced by approximately a factor of two. A new matching structure will be investigated during the next quarter

which should increase bandwidth without sacrificing power handling capability so severely.

VIII. CONCLUSION

X-band bulk limiters have been fabricated using high resistivity silicon with ρ = 8000 ohm cm p-type uncompensated <111> orientation using the process technology developed by RRC Internation, Inc. The processes were optimized to make better use of Microwave Associates' facilities. Process changes were incorporated which are well suited to mass production techniques. The initial test results show that the devices do handle between 10 KW to 20 KW pulsed RF power. However, insertion loss and recovery time require additional improvement.

IX. PROGRAM FOR THE NEXT QUARTER

During the next quarter, we will fabricate devices with improved yield and performance. We will ship 5 bulk limiters before 25 October 1976, as First Engineering Samples (Item 0001AA). Also, copper irises for mounting bulk limiters will be evaluated.

X. IDENTIFICATION OF PERSONNEL

During this quarter, the following technical personnel contributed to this program

TITLE	HOURS
Project Manager	300
Silicon Materials Manager	20
Senior Processing Engineer	15
Processing Engineer	50
Limiter Engineer	95
Engineering Assistant (Fabrication)	400
Engineering Assistant (Test)	290

REFERENCES

1. K. E. Mortenson and J. F. White, "Non-Refrigerated, Bulk Semiconductor, Microwave Limiters", IEEE Journal of Solid State Circuits, SC-3, pp. 5-11, 1968.

2. K. E. Mortenson et al, "Microwave Solid State Limiting Phenomena", Final Report for AFAL, Contract No. F33615-67-C-1858, November 1968.

3. K. E. Mortenson et al, "A Review of Bulk Semiconductor Microwave Control Components", IEEE Proc., Vol. 59, No. 8, pg. 1191-1200, August 1971.

4. K. E. Mortenson et al, "Bulk Semiconductor Limiters", Final Report for U.S. Army ECDM, Technical Report ECOM-0186-F, August 1970.

5. A. L. Armstrong et al, "Bulk Semiconductor Limiters", Final Report for U. S. Army ECOM, Technical Report ECOM-0195-F, October 1971.

6. A. L. Armstrong et al, "Bulk Semiconductor Limiters", Semiannual Report for Contract DAAB07-72-C-0292, March 1973.

7. A. L. Armstrong et al, "Bulk Semiconductor Limiters", Final Report for Contract DAAB07-72-C-0292, March 1974.

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts
MIL-STD-1311A	Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

FSC 5961

REQUIREMENTS:

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed turned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-40B/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1 μsec pulses continuous	:	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss	:	0.7dB (max)
(c)	Low Level VSWR	:	1.4:1 (max)
(d)	Recovery Time	:	0.8 μsec (max)
(e)	Flat Leakage	:	50 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(f)	Spike Leakage	:	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias	:	none

3.4 Absolute Ratings

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

4.1.2 Test equipment c inspection facilities. - Test equi, ent and inspection facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance Inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection, tightened inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance number of zero (0). For purposes of inspection, the lot size shall be one (1) month's production.

4.4.3 Quality conformance inspection - Part 3 (QCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures shall be permitted.

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance Inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

Test Conditions

P[illegible]meter Unit	T_A °C	Fo GHZ	Po Watts	μ sec	P_{RR} Pulses/sec	Du	Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 – 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

Table I

	Mil Standard	Application Method	Test Conditi	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μsec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Quality Conformance Inspection - Part 1 (QC 1.1)

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Table II

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	Nc
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_i Δf_s $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_i Δf_s $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_i Δf_s $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_i Δf_s $\Delta \tau$	—	0 0 0	db mw μ sec	10

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Table III

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_i		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	τ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC III-3)

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NOTES:

1. e maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4452 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

2. The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

3. Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

4. A swept frequency may be used.

5. Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

The firming power shall be defined as a db increase of limiter insertion loss mpared to the "cold" insertion loss.

7. Quality conformance test to be made using bulk semiconductor stage only.

8. For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

9. The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5μsec from the cessation of 1μsec input pulse.

10. Measurement of parameters cited will follow the procedures outlined in QCI -1.

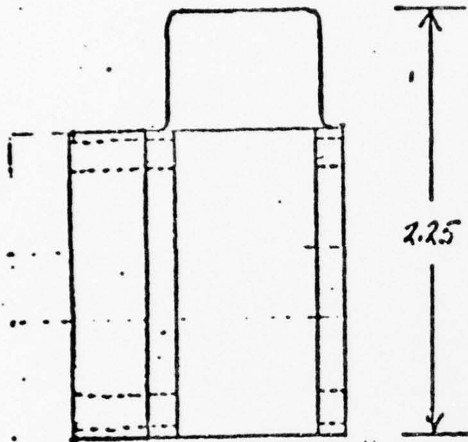
11. The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage (P_s), will be periodically monitored. Life test will be interrupted each 720 ± 20 hours intervals to permit testing of end of life test end points.

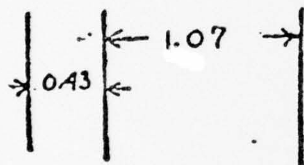
5. PREPARATION FOR DELIVERY

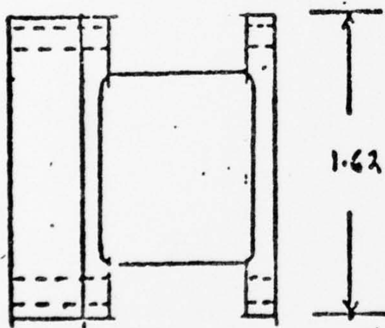
5.1 Packaging, Packing and Marking. - Packaging, packing and package marking shall be specified in the contract.

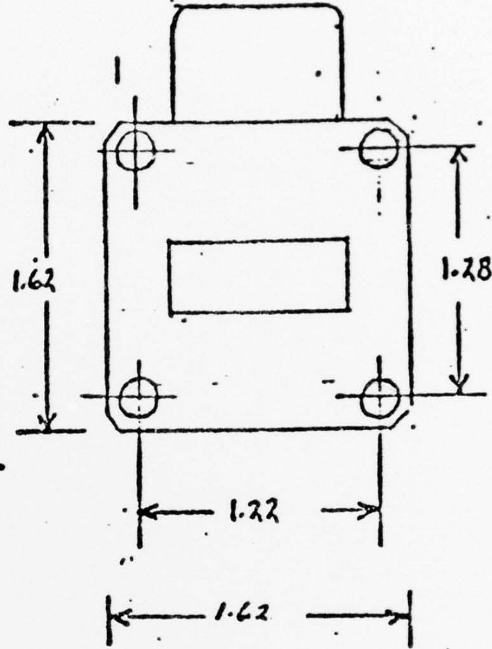
FIGURE 1

TLINE DRAWING









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Notes:

a) all dimensions in inches

b) all tolerances ± 0.01 unless otherwise specified

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