

AD-A038 052

ROME AIR DEVELOPMENT CENTER GRIFFISS AFB N Y

F/G 20/12

GALLIUM ARSENIDE DEVELOPMENT FOR HIGH POWER MICROWAVE SOURCES (U)

FEB 77 J M MILAN

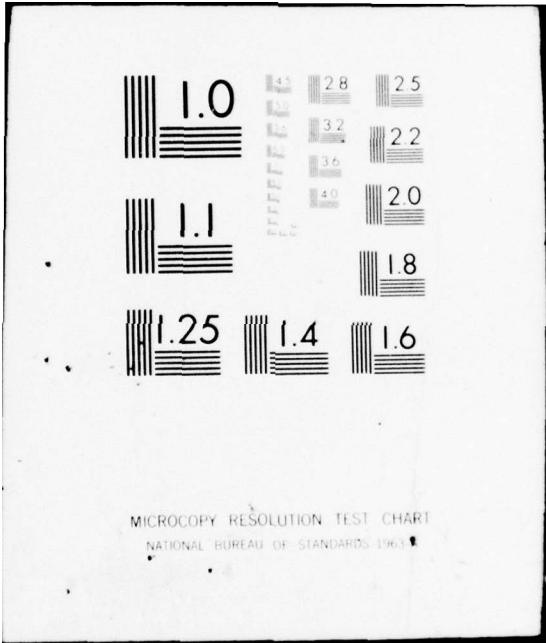
UNCLASSIFIED

RADC-TR-76-407

NL

1 of 1  
AD  
A038052





MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A

AD A 038052

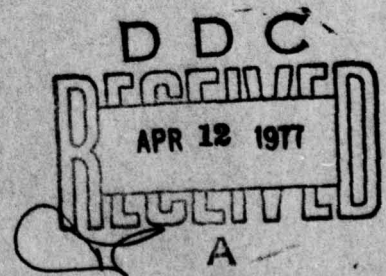
RADC-TR-76-407  
In-house Report  
February 1977



GALLIUM ARSENIDE DEVELOPMENT FOR HIGH POWER MICROWAVE SOURCES

1/Lt Joseph M. Milan

Approved for public release; distribution unlimited.



ROME AIR DEVELOPMENT CENTER  
AIR FORCE SYSTEMS COMMAND  
GRIFFISS AIR FORCE BASE, NEW YORK 13441

AD No. \_\_\_\_\_  
DDC FILE COPY

This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be available to the general public, including foreign nations.

This report has been reviewed and is approved for publication.

APPROVED: *Frank J. Rehm*

FRANK J. REHM  
Assistant Chief, Techniques Branch  
Surveillance Division

APPROVED: *Joseph L. Ryerson*

JOSEPH L. RYERSON  
Technical Director  
Surveillance Division

FOR THE COMMANDER:

*John P. Huss*

JOHN P. HUSS  
Acting Chief, Plans Office

ACQUISITION by	
DTIC	RESTRICTED <input checked="" type="checkbox"/>
DDC	DATE <input checked="" type="checkbox"/>
UNCLASSIFIED	<input type="checkbox"/>
JUSTIFICATION:	
BY:	
DATE:	
<i>A</i>	

Do not return this copy. Retain or destroy.



UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
14 1. REPORT NUMBER RADC-TR-76-407 ✓	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
16 4. TITLE (and Subtitle) GALLIUM ARSENIDE DEVELOPMENT FOR HIGH POWER MICROWAVE SOURCES		5. TYPE OF REPORT & PERIOD COVERED In-house Report ✓
10 7. AUTHOR(s) Joseph M. Milan 1/Lt, USAF		6. PERFORMING ORG. REPORT NUMBER N/A
		8. CONTRACT OR GRANT NUMBER(s) N/A
9. PERFORMING ORGANIZATION NAME AND ADDRESS Rome Air Development Center (OCTE) Griffiss AFB NY 13441 ✓		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62702F 55730388
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (OCTE) Griffiss AFB NY 13441	11 12. REPORT DATE February 1977 ✓	13. NUMBER OF PAGES 37
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Same (12) 42p.		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) Same (16) 5573 (17) 03		
18. SUPPLEMENTARY NOTES None		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Solid State                      Crystal Growth Microwave Generation          Liquid Phase Epitaxy Gallium Arsenide		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Liquid phase epitaxy (LPE) of Gallium Arsenide conducted at RADC beginning in FY 74 is summarized. A detailed description of the growth procedures using a graphite slider boat is presented. The results of various growth schedules using the graphite slider are given with the conclusion that growth above 800°C is too highly compensated (yields material with too many impurities).		

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

309050

Y/B

**UNCLASSIFIED**

**SECURITY CLASSIFICATION OF THIS PAGE(When Data Entered)**

[A large rectangular area containing a very faint, illegible document or form, possibly a table or report, with some faint markings and text visible.]

**UNCLASSIFIED**

**SECURITY CLASSIFICATION OF THIS PAGE(When Data Entered)**

## TABLE OF CONTENTS

1. INTRODUCTION	1
2. LIQUID PHASE EPITAXY	2
3. PROGRAM SUMMARY	4
4. CONCLUSIONS	14
APPENDIX A. SUMMARY OF RESULTS	
APPENDIX B. GROWTH TECHNOLOGY	
A. SIZING	B-3
B. LAPPING	B-4
C. POLISHING	B-5
D. CLEANING	B-7
E. THE GRAPHITE SLIDER	B-9
F. GROWTH SCHEDULES	B-11
G. PROCEDURE FOR ANALYSIS OF RESULTS	B-13

1. INTRODUCTION:

At the heart of the semiconductor industry is the ability to construct areas of different impurity levels within a single crystal. There are several methods in existence which accomplish this "doping". Diffusion and ion implantation are the methods by which impurities are added to an already existing semiconductor crystal, while liquid phase and vapor phase epitaxy are the procedures by which doped layers are grown on top of semiconductor crystals (called substrates). Layers grown on top of a substrate maintain the crystal structure of the substrate and thus are called epitaxial (single crystal) layers.

The subject of this report is the use of the liquid phase epitaxial system at Rome Air Development Center. This system has been used specifically for the liquid phase epitaxial growth of Gallium Arsenide (GaAs) for microwave devices. The mission of this effort was to support RADC's microwave device efforts by providing in-the-house experience in GaAs epitaxy.

A goal of the current effort was to modify the GaAs liquid phase epitaxial (LPE) capability and then to use this capability to produce certain state-of-the-art devices. The LPE laboratory was not meant to be a production facility or a full-scale research facility, but rather a problem-solving laboratory.



## 2. LIQUID PHASE EPITAXY:

Liquid phase epitaxy is simply epitaxial growth by precipitation from a saturated melt in physical contact with the substrate. In the system at RADC, an ultra pure gallium melt was saturated at about 800°C with arsenic by dissolving GaAs source material into the melt. Dopants such as tin were also dissolved into the gallium to achieve proper impurity profiles. The melt was then cooled and a substrate was moved under the melt. Crystal growth occurred because, as the temperature of the melt decreased, the melt could no longer contain as much arsenic and so some of it was precipitated out in the form of GaAs.

Gallium Arsenide is doped in order to achieve different electrical characteristics. Highly doped GaAs is used to make electrical contact to the less conductive (and less doped) active layer. It is also used to transition mechanically from the highly doped substrate to the active layer. When speaking of an active layer in microwave GaAs, we simply mean the area where the microwave energy is produced. For a Gunn-type device, this area is lightly doped and about 10 microns thick. Figure 1 shows the Gunn-type profile which was the most recent short-term goal of this effort.

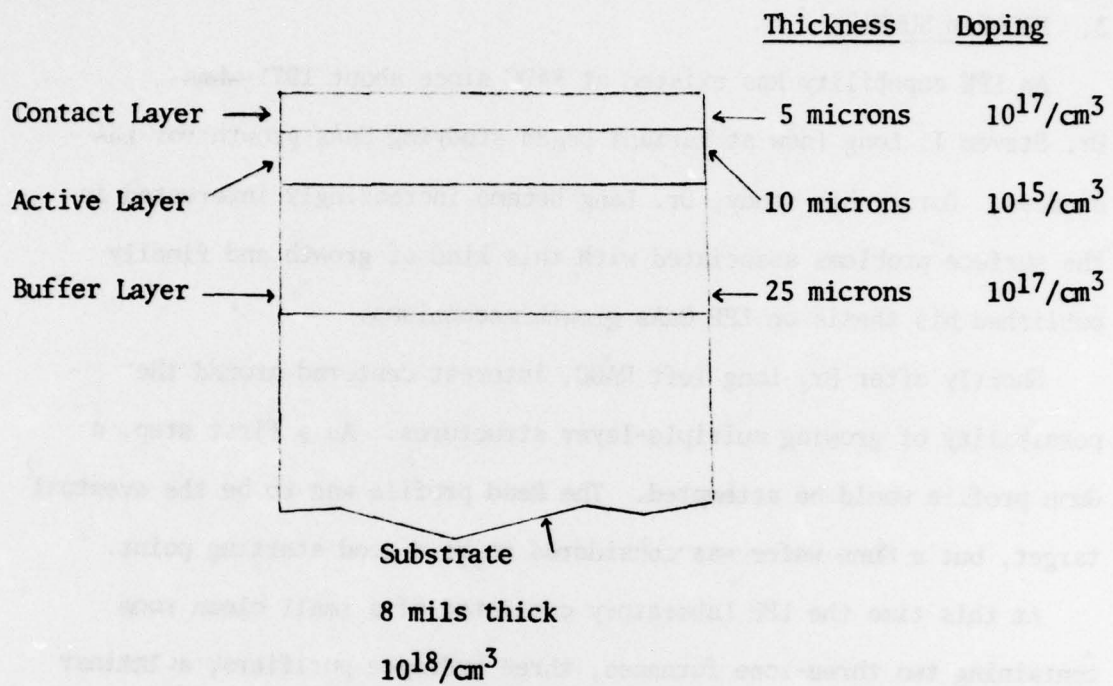


Figure 1

GUNN-TYPE PROFILE FOR GALLIUM ARSENIDE

### 3. PROGRAM SUMMARY:

An LPE capability has existed at RADC since about 1971 when Dr. Steven I. Long (now at Varian) began studying GaAs growth for LSA devices. During his study, Dr. Long became increasingly interested in the surface problems associated with this kind of growth and finally published his thesis on LPE GaAs growth mechanisms.

Shortly after Dr. Long left RADC, interest centered around the possibility of growing multiple-layer structures. As a first step, a Gunn profile would be attempted. The Read profile was to be the eventual target, but a Gunn wafer was considered to be a good starting point.

At this time the LPE Laboratory consisted of a small clean room containing two three-zone furnaces, three hydrogen purifiers, a laminar flow hood, and a hygrometer. A portion of the lab is shown in Figure 2. In order to make the facility applicable to multiple-layer growth, it was necessary to modify the furnace tube and to construct a new graphite boat.

During the planning stage of the program, the help of Dr. Varley Wrick (then of Cornell University) was secured through the RADC Post Doctoral Program. Before coming to RADC, Dr. Wrick arranged for the construction of the graphite slider boat and the modification of the furnace tube. Early in the project, the substrates to be used for LPE growth were purchased from Laser Diode Laboratories, Incorporated. Preliminary cleaning and organizing was done at RADC in preparation for the active part of the program.

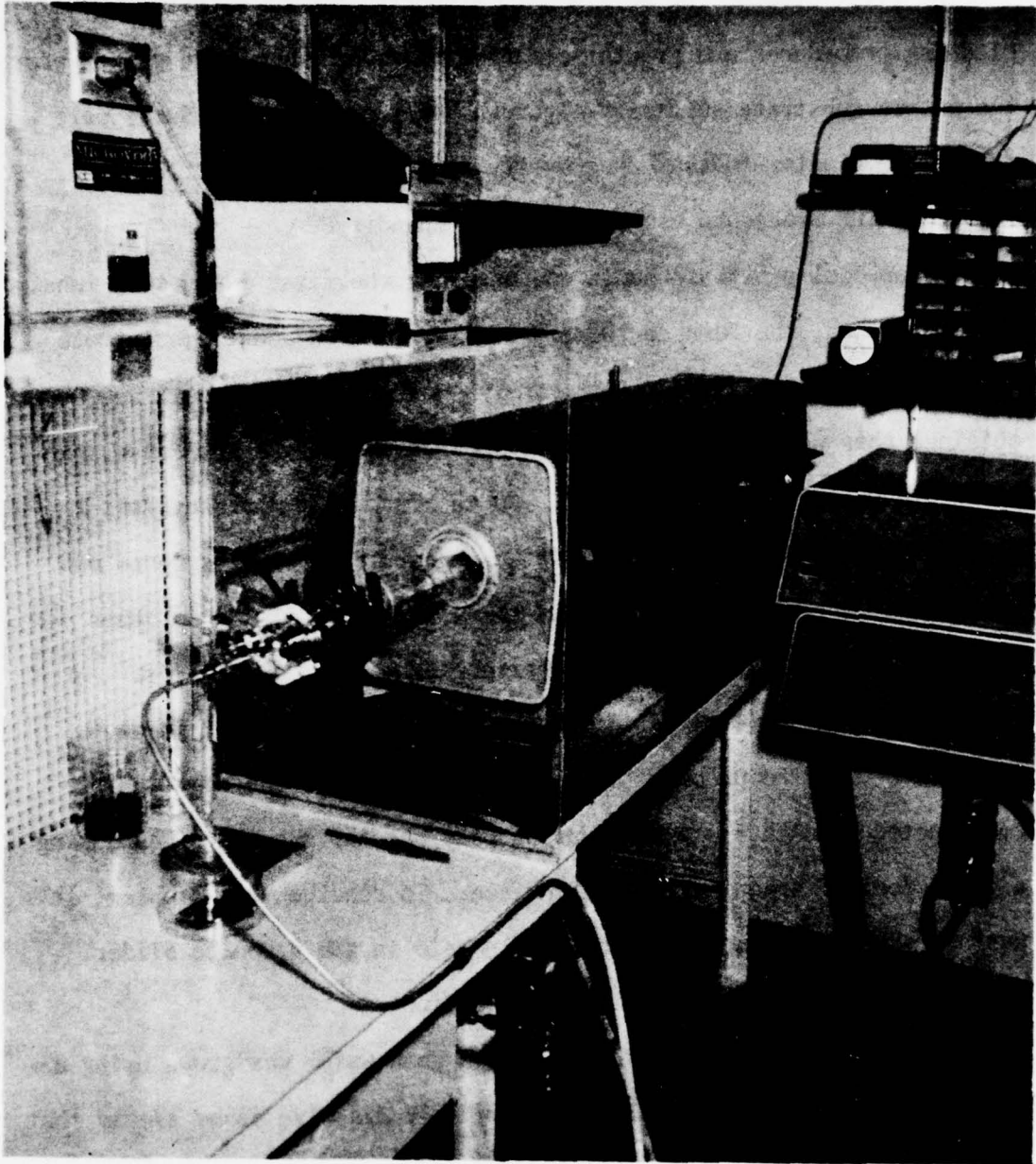


Figure 2

LPE LABORATORY



The first step of the work was to establish proper substrate cleaning procedures and growth schedules in order to achieve growth over the entire substrate surface. Although other cleaning schedules were tried, one similar to that used by Dr. Long was finally settled upon. This cleaning procedure can be found in Appendix B.

A step-cool growth schedule was used for the first few growth runs. In this method, the furnace temperature was lowered and the substrate was slid under the melt. Unfortunately, uniform wetting could not be obtained this way, so a ramp-cool method was tried. In this case, the substrate was slid under the melt, and the furnace temperature was gradually lowered at the rate of  $18^{\circ}$  per hour. The results up to now were still very poor (an example is shown in Figure 3) and so other possible problem sources were investigated.

After trying several variations in the growth schedule, it was determined that the problem lay in the boat design. The boat was constructed in such a way that during bake out the substrate was losing a great deal of arsenic from its surface. To resolve this problem, it was necessary for us to plug the middle hole in the graphite slider. Figure 3A shows the boat and its modification.

Once the modification was complete, a good wafer was grown using a back dissolve and a ramp-cool. The term back dissolve means simply that the furnace temperature was raised a few degrees as the substrate was moved under the well. This allowed some of the top layer of GaAs (along with any oxidation, excess gallium, or surface impurities) to dissolve



Figure 3

Photomicrograph of a typical area on SC-1. The coarse surface is the substrate and the mesas are islands of growth of epitaxial GaAs 5 to 10 microns high. This result is typical of those achieved early in the program. Modifications of the boat and elevated growth temperatures solved this problem. The magnification of this photograph is 200X.

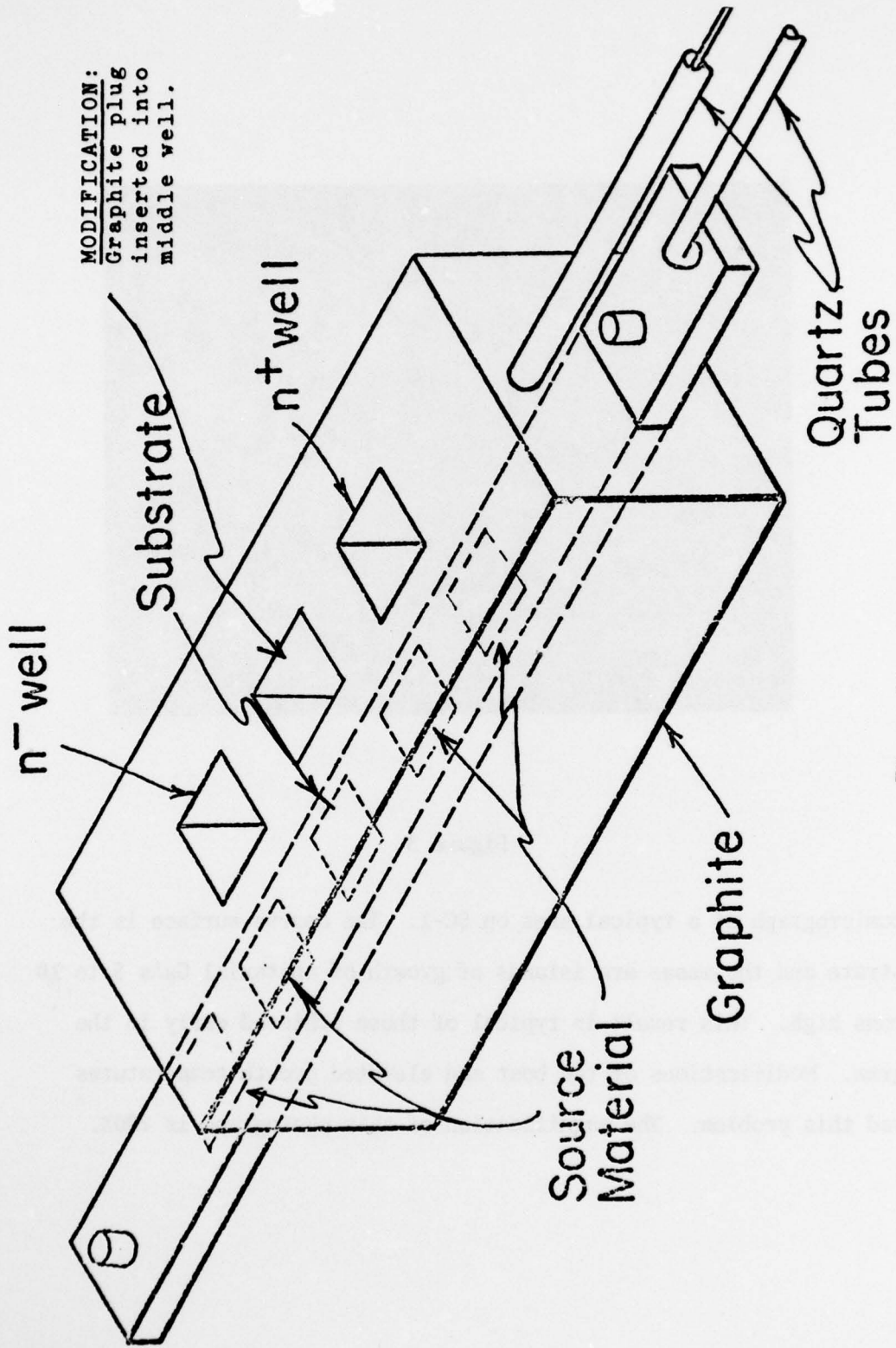


Figure 3A

into the melt. This technique has the obvious handicap of incorporating impurities into the epitaxial layer.

It was also necessary to grow at elevated temperatures (about 800°C) in order to achieve uniform wetting. Unfortunately, the same high temperatures which allowed uniform growth, gave highly compensated (containing relatively large amounts of both n-type and p-type impurities) material.

Once uniform wetting was achieved, considerable time and effort were expended improving the surface quality of the epitaxial layers. Thickness control was also studied and after a year into the program was achieved + 10%.

Single layers were grown at first using several different temperature schedules. The most common schedule was that using both a back-dissolve and a ramp-cool. Other methods used were a ramp-cool without a back-dissolve and a ramp-cool with a super-cooling technique. In the super-cooling technique, the temperature was lowered and the melt was allowed to cool while it was positioned over graphite (or in a few cases over a source crystal). Then the substrate was moved under the super-saturated melt and the temperature ramp was initiated. After good surface quality was achieved with a single layer, multiple layers were grown by using two melts with different dopant concentrations.

Results of one triple layer are shown in the photomicrographs which follow. Since the epitaxial growth was not linear with time, it took a few iterations to achieve the desired profile. A wafer with a profile



close to the one shown in Figure 1 was grown and then taken to Cornell University for complete evaluation. It was this result plus some measurements done on Hall samples which led to the conclusion that the material grown at 800°C was too highly compensated.

In order to resolve this problem, it was necessary to lower the growth temperature. At lower temperatures and using the same growth schedules and cleaning procedures, some good results were obtained. At this time, a new step was introduced into the cleaning process for some growth runs. This step, a preferential etch, showed some promise. The program drew to a close owing to redirection of effort within RADC.

The complete results of this program are given in a tabulated form in Appendix A.

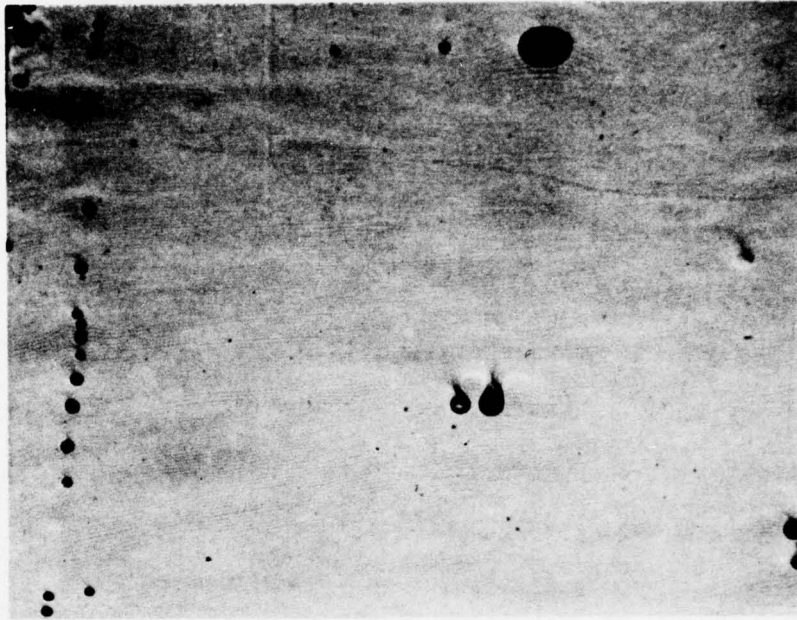


Figure 4

Typical area on wafer 5148 at 50X magnification. This surface is rippled, but still of device quality. It is representative of the good quality surfaces obtained at about a year into the project. This epitaxial layer is a triple layer about 48 microns thick and the black areas are either inclusions of some foreign material in the crystal or areas where growth did not occur.



Figure 5

Photomicrograph of wafer 5155 at 50X magnification. This wafer is another triple layer. The area to the right shows a surface of definite device quality. The dark area to the left shows the edge of the wafer with some non-uniform growth. The thickness of the epitaxial layer in the center area was about 45 microns.

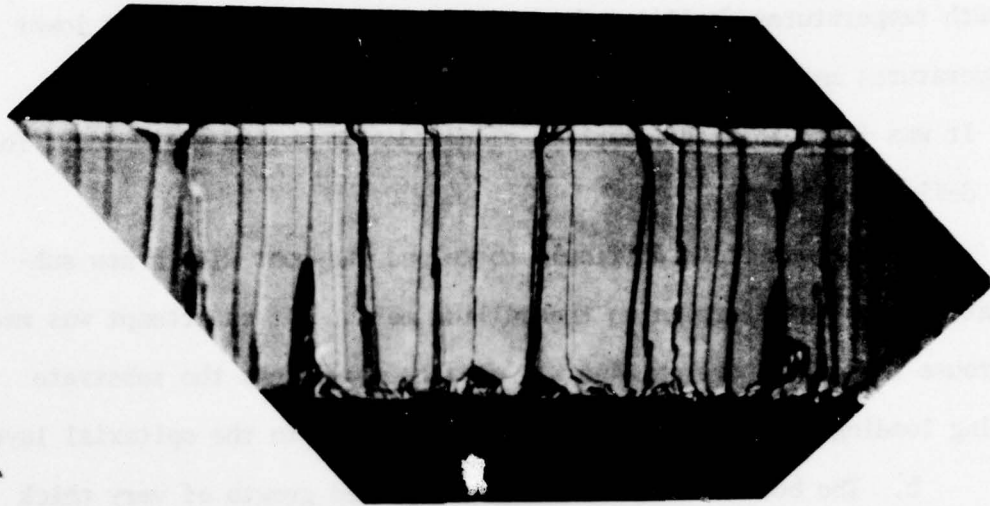


Figure 6

Photomicrograph of wafer number 5155 at 200X magnification. This is an edge-on view of 5155 after it was cleaved and stained. The first layer (buffer layer) is 25 microns thick, the middle layer (active layer) is about 9 microns thick, and the final layer (contact layer) is about 15 microns thick. All layers are quite uniform and the surface of this wafer was also good. Unfortunately, the contact layer is too thick, and the material was too highly compensated to be useful.



#### 4. CONCLUSIONS:

As demonstrated, growth at about 800°C was too highly compensated and therefore growth must be initiated at lower temperatures. High growth temperatures facilitated wetting and uniform growth, but lower temperatures made these problems more difficult.

It was found that the graphite slider design worked well except for two definite problems.

a. It was quite difficult to reload the boat with a new substrate without also replacing the gallium melts. If an attempt was made to reuse the melt, some gallium was usually wiped onto the substrate during loading and caused surface nonuniformities in the epitaxial layer.

b. The boat cannot be used for repeated growth of very thick layers. The buffer layer together with the active and contact layers used in making a Gunn wafer virtually destroyed the boat over a period of several runs. The newly grown layers together with crystallites formed along the sides and edges of the well scraped and gouged both the slider tongue and the underside of the boat. These gouges allowed excess gallium melt to remain on the substrate and caused growth to proceed to room temperature. Areas of prolonged growth are not only worthless for devices but cause further degradation of the boat.

APPENDIX A

SUMMARY OF RESULTS

TABLE 1. SUMMARY OF DATA

Date	Wafer Number	Back-out Temp(°C)	Growth Method	Growth Time/min	Comments
05/05/74	SC-1	775	A step-cool procedure was used; temp reduced to 760°C and growth started.	60	Scaly surface of 5-10 micron-high crystallites.
06/12/74	SC-2	775	Same as UC-1.	60	Same as SC-1.
06/25/74	SC-3	800	Step-cool procedure used; temp reduced to 785°C and growth started.	60	Same as SC-1.
06/27/74	UC-4	800	Temp ramp started; two minutes later growth started (ramp = 18°/M).	90	Better surface, but still patchy.
07/01/74	UC-5	800	Same as UC-4.	90	Substrate broke during growth cycle - no results.
07/09/74	UC-6	780	Raise temp 5° and slide on; 5 min later start ramp (5°/5 min back dissolve).	60	Surface still poor, scaly.
07/16/74	UC-7	780	5°/10 min back dissolve (B.D.) then ramp cool.	120	Mottled, scaly surface.
07/18/74	NC-8	780	No cool; left substrate under melt for 10 min.		No change - surface remained highly polished.
07/19/74	UC-9	780	Slide on; left substrate under melt for 10 min then started ramp.	30	Sparsely, patchy growth.

TABLE 1. SUMMARY OF DATA (Continued)

Date	Wafer Number	Bake-out Temp(°C)	Growth Method	Growth Time/Min	Comments
07/25/ 74	NC-10	780	10°/15 min B.D., no ramp.		Severe back dissolve; rough surface.
07/29/ 74	UC-11	790	10°/10 min B.D., and ramp cool.	90	Better surface, but still scaly.
08/02/ 74			Boat modified - middle well plugged.		(Now as in Figure 2)
08/06/ 74	UC-12	780	2°/10 min B.D., ramp cool.	60	Scaly surface.
08/08/ 74	UC-13	820	3°/10 min super saturation (lower temp 8°) ramp cool.	60	Better surface, but not completely covering substrate.
08/12/ 74	UC-14	825	2°/10 min B.D., ramp cool.	60	Good result - covered surface some "orange peel" effect.
08/14/ 74	UC-15	825	2°/10 min B.D., ramp cool.	130	Same as UC-14.
08/16/ 74	UC-16	825	2°/10 min B.D., ramp cool, triple layer.	120	45 min buffer, 60 min active, 15 min contact; (45-60-15) complete triple layer.
08/20/ 74	UC-17	825	2°/17min B.D., ramp cool; Cr-doped substrate.	120	Broke up the boat during growth.



TABLE 1. SUMMARY OF DATA (Continued)

Date	Wafer Number	Bake-out Temp (°C)	Growth Method	Growth Time/Min	Comments
08/22/ 74	UC-18	825	2°/15 min B.D., ramp cool; Cr-doped substrate.	120	Good surface - Hall measurement attempt.
08/27/ 74	UC-19	825	2°/10 min B.D., ramp cool; Cr-doped substrate.	60	Good surface, broken while unloading.
08/29/ 74	UC-20	825	No back dissolve, ramp cool.	60	Rippled surface, but covered substrate
09/04/ 74	UC-21	825	2°/10 min B.D., ramp cool.	60	Non-uniform growth.
09/11/ 74	UC-22	825	2°/10 min B.D., ramp cool; Cr-doped substrate.	60	Good surface - Hall attempt.
09/13/ 74	UC-23	825	15°/10 min super saturation.	60	Rippled surface.
09/19/ 74	UC-24	825	2°/10 min B.D., ramp cool.	60	Good surface; layer thickness = 12 microns.
09/24/ 74	UC-25	825	5°/5 min super saturation (S.S.) ramp cool.	60	Surface good, broke while cleaving.
10/10/ 74	UC-26	825	5°/5 min S.S.; ramp cool.	60	Good surface; Shottky barrier test indicated doping = 10 <sup>15</sup> cm <sup>-3</sup> .

TABLE 1. SUMMARY OF DATA (Continued)

Date	Wafer Number	Bake-out Temp (°C)	Growth Method	Growth Time/Min	Comments
10/18/ 74	UC-27	825	5°/5 min S.S., ramp cool.	60	Substrate broken during growth.
10/31/ 74	UC-28	825	5°/5 min S.S., ramp cool.	60	Good surface.
02/04/ 75	75-2	825	2°/10 min S.S., ramp cool, triple layer (30-40-30)	100	Terraced - only 2 layers for sure.
04/18/ 75	18475	825	2°/10 min B.D., ramp cool, triple layer (40-50-60).	150	Double layer grew - broke while unloading.
05/14/ 75	5134	825	2°/10 min S.S., ramp cool, triple layer (160-90-60).	310	Rough surface, but complete triple layer.
05/20/ 75	5139	825	Left under melt 20 min, 2°/20 min S.S., ramp cool, triple layer (130-60-30).	220	Some areas with rough surface, triple layer grew.
05/28/ 75	5148	825	Same as 5139 except times (90-60-30).	180	Surface good, triple layer.
06/04/ 75	5155	825	Same as 5139 only S.S. over source material and times (105-60-30).	195	Surface good, triple layer grew.
06/11/ 75	5161	825	2°/15 min S.S. over source used preferential etch (105-75-10).	190	Substrate broke, surface poor quality.

TABLE 1. SUMMARY OF DATA (Continued)

Date	Wafer Number	Bake-out Temp(°C)	Growth Method	Growth Time/Min	Comments
07/03/ 75	5184	825	Same as 5155 except times (105-75-10).	190	Broke up during growth.
07/16/ 75	5194	825	2°/2 min S.S. over source (105-75-14).	194	Broke up during growth.
07/23/ 75	5204	825	Same procedure as 5184.	190	Some growth to room temp, non-uniform surface.
09/09/ 75	H75-1	814	2°/20 min S.S. over source, all Cr-doped substrate from now on.	85	Good surface - Hall sample indicated highly compensated material.
09/16/ 75	H75-2	794	Same as H75-1.	85	Poor surface.
09/22/ 75	H75-3	794	Same as H75-1.	85	No growth; boat malfunctioned.
09/29/ 75	H75-5	794	Same as H75-1.	85	Poor growth; scaly surface.
10/02/ 75	H75-6	760	Same as H75-1.	85	Poor surface.
10/07/ 75	H75-7	740	Same as H75-1.	85	Very good surface.

TABLE 1. SUMMARY OF DATA (Continued)

Date	Wafer Number	Bake-out Temp (°C)	Growth Method	Growth Time/Min	Comments
10/09/75	H75-8	720	Same as H75-1.	85	Patchy, poor growth.
10/16/75	H75-9	794	1°/2 min S.S., ramp cool.	60	Fairly good surface - one corner poor.
10/21/75	H75-10	794	1°/2 min S.S., ramp cool.	60	Poor growth.
10/28/75	H75-11	760	2°/2 min S.S., ramp cool.	65	Poor surface.
10/30/75	H75-12	780	1°/2 min S.S., ramp cool.	65	Good surface.



**APPENDIX B**

**GROWTH TECHNOLOGY**

#### GROWTH TECHNOLOGY:

Substrate preparation for epitaxial growth is one of the major areas of GaAs technology. In order for high quality epitaxial growth to take place, the growth surfaces of the substrates must be extremely smooth, clean, and without physical damage. GaAs substrate preparation is a long, arduous process which usually begins with the bulk growth of single crystal GaAs.

This bulk growth is often done by companies specifically organized for that purpose. After a single crystal (called a boule) is grown, it is sawed (usually by the same company) into substrates of the appropriate thickness. In this work, the substrates, purchased from Laser Diode Laboratories, Inc., were 20 to 24 mils thick and had surface areas of about 5 square centimeters each.

Once the substrates were secured from the vendor, they were sized to fit the growth apparatus by cleaving or sawing to the correct length and width. At first all substrates were sawed, but later it was found that cleaving was simpler and quicker. Next the substrates were lapped to their pre-polish thickness (16 mils in this case). They were then polished using a hypochlorite etch and a pellaon polishing pad. Four mils of GaAs were polished off each side of the substrate in order to achieve a surface with minimal crystal strain and work damage. This process left a shiny, mirror-like surface.

The highly polished substrates were then ultrasonically rinsed in organic solvents, etched to remove any oxide layers, and blown dry with

dry nitrogen or other clean, non-reactive gas. The cleaned and polished substrates were then loaded into the graphite boat in the tube furnace. At this time, source crystals were also loaded into the boat. These crystals, which were 40 mils thick and had the same area as substrates, were sized and cleaned in the same manner as the substrates.

Although the furnace had an ultra-pure hydrogen atmosphere, the loading process allowed some air to enter the furnace. Once this air had been purged from the system by ultra-pure hydrogen, the growth cycle was begun. The first part of the growth cycle was an overnight bakeout period. During this time, the furnace was set to the growth temperature and all parts of the system were allowed to reach thermal equilibrium. Next, the actual growth process took place by means of a predetermined cooling schedule. After the substrate was moved out from under the melt, the furnace was allowed to cool to room temperature, and the wafer - substrate plus epitaxial layer - was unloaded and cleaned of any excess gallium. Finally, the wafer was inspected and tested.

The following pages contain a more detailed discussion of each part of GaAs growth technology.

## A. Sizing of Substrates and Source Crystals

### 1. Sawing

- a. A 20-24 mil thick GaAs substrate was chosen.
- b. It was waxed down to a graphite block using a hot plate to melt the wax (the graphite block was actually part of the saw).
- c. With the wire saw and abrasive (mixed in 9:1 H<sub>2</sub>O and glycerin), the substrates were sawed to the proper size.
- d. All cuts were made parallel or perpendicular to flat edge of substrate.
- e. The size of the substrate was to be 385 x 385 mils.

### 2. Cleaving

- a. A 20-24 mil thick GaAs substrate was chosen.
- b. Using diamond scribe and ruler, the substrate was scribed perpendicular or parallel to a flat edge scribing exactly where the substrate was to be cleaved.
- c. The substrate was scribed all the way across its width several times.
- d. Three microscope slides were used to cleave the crystal as follows:
  - (1) The substrate was placed on one slide;
  - (2) Another slide was placed on top to form a sandwich;
  - (3) The sandwich was adjusted so that the slide edges and scribe line were all in line.



- (4) While holding the sandwich, even pressure was applied to the uncovered area of the substrate with the third slide until the substrate cleaved along the scribe line.

#### B. Lapping

1. Substrates were lapped to a thickness 8 mils greater than the final required thickness (final thickness was 8 mils).
2. The substrates were mounted on a 5 inch glass disc as follows:
  - a. White wax (glycol phthalate wax) was used;
  - b. The disc was heated to 120°C (melting point of white wax);
  - c. White wax was melted onto the disc where the substrates were to be positioned; only 3 or 4 substrates of similar thickness were used each time, and they were evenly spaced at about 1 cm from the edge of the disc;
  - d. The substrates were placed on the melted wax and gently pressed down with a teflon-tipped tool (or other flat, clean surface);
  - e. Excess wax was removed with acetone.
3. The lapping mixture consisting of 5 micron  $\text{Al}_2\text{O}_3$  abrasive (Buehler or AO 305) mixed in deionized water and 10% glycerine was poured onto a large piece of plateglass using enough of the mixture to form a puddle about half the size of the glass disc.
4. The disc was placed substrate-side down and was moved in a circular manner applying a minimal amount of downward pressure.
5. Every few minutes the thickness of the substrates was checked.

6. Equal amounts of GaAs were lapped from each side of the substrates. After one-half of the total thickness to be removed was lapped from the first side, the disc was heated to 120°C and the substrates were carefully removed from the disc. The substrates were flipped over and remounted as in step 2.
7. The remaining thickness to be removed from this side was lapped as before, then the substrates were removed from the disc and rinsed in acetone.
8. Last of all, the disc and the piece of plateglass were cleaned of any GaAs residue or leftover abrasive.

#### C. Polishing

The polishing of GaAs is actually a chemical etch procedure. The etch forms an oxide layer on the substrate surface which is then wiped off by the polishing pad.

The polishing apparatus used for this effort consisted of two plexiglass discs; one with an eight inch diameter which shall be called the polishing wheel, and the other with a diameter of about 5 inches. The polishing wheel was slanted at about 60° from horizontal and a pellow PAN-W polishing pad was attached to it. The substrates were mounted on the smaller disc and this disc was placed face-down on the polishing wheel while hypochlorite etch was dripped onto the pellow pad. The smaller disc was positioned so that its edge did not quite touch the center of the polishing wheel. The polishing machine was constructed in such a way that both discs rotated at 50 to 60 RPM in the

same direction. Using a pressure of about  $250 \text{ g/cm}^2$ , a polishing rate of about one mil per second was observed.

Following is the step-by-step procedure for substrate polishing:

1. Fresh hypochlorite etch was prepared by mixing deionized water and Chlorox (5% NaOCl) in a 15:1 ratio;
2. The substrates were mounted onto a 5 inch disc using the same procedure as for lapping;
3. A fresh pellow pad was placed onto the polishing wheel following the procedure below:
  - a. The old pad was peeled off;
  - b. The polishing wheel was dried thoroughly;
  - c. The wax paper backing from a new pad was peeled off while the pad was being attached to the wheel;
  - d. Using a beaker or some other clean, smooth instrument, the pad was pressed down firmly.
4. The polishing pad was rinsed with deionized water and the small disc was mounted on the polishing machine;
5. The polishing machine was turned on;
6. The echant flow was adjusted so that about 1 drop fell onto the pad every second;
7. After the first 15 minutes of polishing, both the polishing wheel and the substrate were rinsed thoroughly with deionized water;
8. The disc was periodically removed and the substrate thickness

was measured. Also, the polishing pad was examined to make sure that it was firmly attached to the wheel;

9. The first side of the substrates was polished until 4 mils were removed (about 4 hours);
10. Then the substrates were removed from the disc, flipped over, and remounted as before;
11. This remaining side was polished until the last 4 mils were removed;
12. Finally, the substrates were removed from the disc carefully and rinsed thoroughly in acetone and then in water.

#### D. Cleaning

The next step in preparing GaAs crystals for epitaxial growth is that of cleaning. It is extremely important that substrates and source crystals be free of wax, grease, and dust. In addition, they must be etched in order to remove their oxide layers which have formed during storage and polishing.

The following schedule was followed using only room temperature electronic grade solvents and acids:

1. Two ultrasonic rinses in trichloroethylene;
2. Two ultrasonic rinses in acetone;
3. Two ultrasonic rinses in deionized water (resistivity greater than  $10^8$  ohm cm);
4. An etch consisting of a mixture of sulfuric acid, hydrogen peroxide, and water in the following proportions:



- a. 7:1:1 for substrates;
- b. 5:1:1 for source crystals;

The substrates were etched for five minutes with agitation; The 5:1:1 etch was used at first for substrates, but it left a rough surface so the 7:1:1 was used since it was less violent and left a very smooth surface;

5. Four rinses in deionized water;
6. Two ultrasonic rinses in deionized water;
7. Two ultrasonic rinses in methyl alcohol;
8. Two ultrasonic rinses in isopropyl alcohol;
9. Two methods were used to finally prepare the substrates for loading into the growth furnace:
  - a. Substrates were placed in isopropyl alcohol while in transit to furnace, then blown dry with dry nitrogen or a "microduster". All source crystals and dopants and most substrates were carried to the furnace and loaded in this manner;
  - b. Substrates were placed in deionized water for 30 minutes, then etched in hydrochloric acid and deionized water (1:1) for 1 minute. They were then rinsed with deionized water and placed in isopropyl alcohol as in part a. Some good results were achieved late in the project using this method;
10. The same cleaning procedure as above was used for dopant preparation with the exception of the etch. For this effort

99.9999% pure tin was used as a dopant and it was etched in concentrated hydrochloric acid for 5 minutes.

#### E. Graphite Slider

In LPE a pyrolytic graphite boat is used to accomplish the growth procedures. It holds the arsenic-saturated melt, the source crystals, and the substrate. The mechanical design of the boat must allow for movement of the substrate and source crystals with respect to the gallium melt. Some method must also be devised to keep arsenic from subliming from the surface of the substrate.

The solution to these problems for our effort was the graphite slider shown in Figure 7. This boat was machined out of ultra-pure pyrolytic graphite by the Cornell University Engineering Machine Shop and care was taken during the machining process to keep the boat free of grease and oil. After machining, it was ultrasonically cleaned with organic solvents and then baked in an induction-heated furnace at 1400°C for 30 minutes. The graphite slider was next brought to RADC and subsequently baked at 900°C for 24 hours in the pure hydrogen atmosphere of the tube furnace.

After bakeout, the boat was loaded in the following manner:

1. Lightly doped, 40 mil thick GaAs source crystals were placed in the four outside slots in the tongue of the slider;
2. A cleaned and polished substrate was placed in the center slot (this slot was machined to a depth of only 8 mils);
3. Five grams of ultra-pure gallium and just enough lightly doped

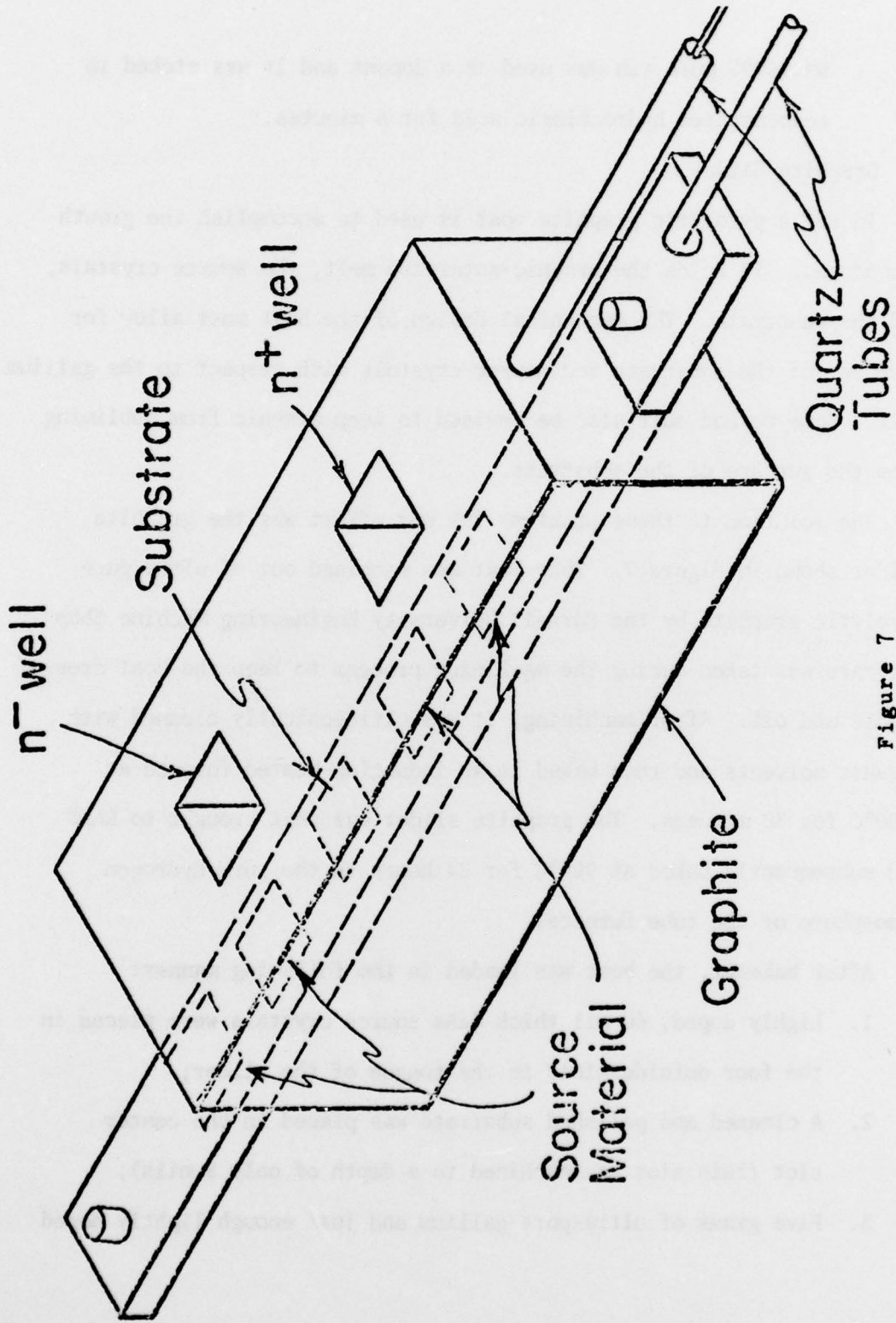


Figure 7

GaAs to saturate the gallium at the growth temperature were placed in the first well;

4. The same amount of gallium and GaAs plus the desired amount of dopant were placed in the second well.

The boat was then put back into the furnace with care to keep the tongue of the slider in the correct position.

During the growth procedure, the boat was held in position by a quartz positioning rod which forced the boat against another quartz rod fused into the wall of the furnace tube perpendicular to the axis of the tube. The tongue of the slider was moved using another quartz rod (control rod) which hooked into a hole in the tongue of the slider. Both the positioning rod and the control rod exited the furnace tube through Swagelok fittings and so could be manipulated during the growth procedure.

#### F. Growth Procedures

Immediately after the boat was put back into the furnace, the system was allowed to flush for a few hours. This forced the pure hydrogen to replace any oxygen which entered the system during loading. As soon as a very low concentration of oxygen - ideally less than one part per million - was reached, the furnace was turned on. The presence of oxygen in the furnace tube is monitored using a hygrometer (this instrument actually measures the water vapor concentration which, of course, is the form that oxygen takes in a hydrogen atmosphere).

The furnace was left on overnight in order for the growth environ-



ment to achieve thermal equilibrium. The growth process took place the next day, following the procedures below:

1. Graphite spaces in the slider tongue were positioned under both wells during overnight bakeout;
2. Approximately four hours before step 3, the source crystals were moved under the wells to insure that the substrate-melt interface would be saturated;
3. Substrate was slid under the doped melt for 20 minutes, keeping the temperature constant; this step allowed for some cleaning of the substrate surface;
4. Source crystals were positioned under the melts, the temperature was lowered 2°C, followed by a 20 minute wait before the next step. An alternative step here was to decrease the temperature 1°C with the melts over graphite and wait 2 minutes. The purpose of this step was to accomplish supersaturation of the melt;
5. The substrate was slid under the melt and the cooling was begun. The cooling was done by attaching motors to the temperature controller knobs. A cooling rate of 18° per hour was achieved using this method;
6. Depending on what doping profile and layer thickness were desired, the substrate was moved after some period of time to the other well and then moved back again;
7. Growth was terminated by placing the slider tongue in the same position as in step 1; the furnace was then turned off and

allowed to cool to room temperature.

Early in the program, several other growth schedules were attempted. A step cooling procedure was used in which the temperature was lowered in two steps, one for supersaturation and one for growth. A back dissolve technique was also used. In this process, the substrate was slid under the melt and the temperature was raised a few degrees before the cooling ramp was started. Various other combinations of times and temperatures were used, but the two given in step 4 were the most successful.

Several single-layer wafers were also grown to analyze growth quality and also to attempt to solve growth problems. The growth schedule was the same as above, but step 6 was omitted.

#### G. Procedure for Analysis of Results

After growth, the furnace was allowed to cool to room temperature. The boat was then taken from the furnace and the wafer was unloaded from the boat. A new substrate was usually loaded and the boat was put back into the furnace for another growth cycle. The wafer was cleaned of excess gallium by using a warm, concentrated hydrochloric acid etch. Finally, the wafer was inspected in several different ways.

First, the wafer was visually inspected to determine the macroscopic qualities of the epitaxial layer. It could usually be determined whether or not the epitaxial layer contiguously covered the substrate. One could also tell whether or not excess gallium melt had allowed growth to proceed all the way to room temperature.

Secondly, the wafer was inspected under a microscope using 50X to

200X magnification. Pictures were taken of typical areas on the epitaxial surface and were placed in the laboratory notebook. One could easily observe non-uniformities using this technique.

The next test was that of determining layer thickness. In order to accomplish this task, a thin slice was cleaved from the wafer in a manner similar to techniques already described. The thin slice was then subjected to an etch (called a stain) which made the different layers visible. This etch attacked highly doped layers differently than undoped layers and therefore left a step which, when viewed from the front, appeared as a line. This junction etch was made by mixing 10 milliliters of 12.5% Potassium Ferricyanide with 10 milliliters of 12.5% Potassium Hydroxide. The wafer to be etched was then immersed in a freshly mixed solution of junction etch for 15 to 30 seconds and rinsed thoroughly with deionized water. The thickness could then be observed and measured under a calibrated microscope.

Doping measurements and doping profile measurements were also done. Hall measurements were performed on epitaxial layers grown on semi-insulating substrates to determine the mobility and doping of the layers. Schottky barriers were sputtered or evaporated onto layers grown on n-type material and capacitance-voltage measurements were taken. These measurements determine the doping versus the depth into the wafer. Measurements of this type were done both at RADC and at Cornell University.

Finally, some wafers were tested by constructing diodes from the material and testing them in a special test jig. This test was done

exclusively at Cornell University. Owing to excess compensation (large amounts of both n-type and p-type impurities), the samples tested were not considered to be of microwave device quality.



## METRIC SYSTEM

### BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

### SUPPLEMENTARY UNITS:

plane angle	radian	rad	...
solid angle	steradian	sr	...

### DERIVED UNITS:

Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	square metre	...	m <sup>2</sup>
density	kilogram per cubic metre	...	kg/m <sup>3</sup>
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm	...	V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m <sup>2</sup>
luminance	candela per square metre	...	cd/m <sup>2</sup>
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m <sup>2</sup>
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m <sup>2</sup>
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m <sup>2</sup>
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m <sup>2</sup> /s
voltage	volt	V	W/A
volume	cubic metre	...	m <sup>3</sup>
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

### SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
1 000 000 000 000 = 10 <sup>12</sup>	tera	T
1 000 000 000 = 10 <sup>9</sup>	giga	G
1 000 000 = 10 <sup>6</sup>	mega	M
1 000 = 10 <sup>3</sup>	kilo	k
100 = 10 <sup>2</sup>	hecto*	h
10 = 10 <sup>1</sup>	deka*	da
0.1 = 10 <sup>-1</sup>	deci*	d
0.01 = 10 <sup>-2</sup>	centi*	c
0.001 = 10 <sup>-3</sup>	milli	m
0.000 001 = 10 <sup>-6</sup>	micro	μ
0.000 000 001 = 10 <sup>-9</sup>	nano	n
0.000 000 000 001 = 10 <sup>-12</sup>	pico	p
0.000 000 000 000 001 = 10 <sup>-15</sup>	femto	f
0.000 000 000 000 000 001 = 10 <sup>-18</sup>	atto	a

\* To be avoided where possible.

**MISSION**  
*of*  
**Rome Air Development Center**

RADC plans and conducts research, exploratory and advanced development programs in command, control, and communications (C<sup>3</sup>) activities, and in the C<sup>3</sup> areas of information sciences and intelligence. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

