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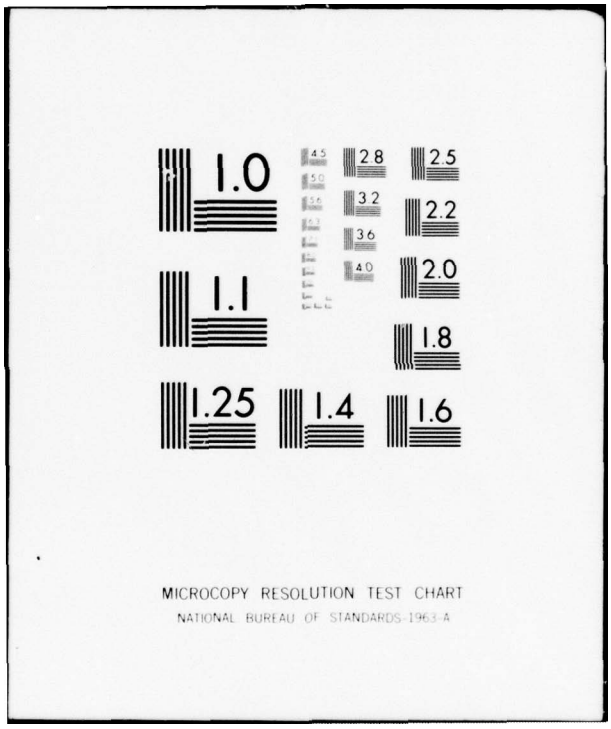
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PLANAR CMOS/SOS ARRAY DEVELOPMENT

C. E. Weitzel
RCA Laboratories
Princeton, NJ 08540

DECEMBER 1976

FINAL REPORT
for the period 1 April 1975 to 31 August 1976

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This Final Report was submitted by RCA Laboratories, Princeton, New Jersey 08540, under Contract No. F33615-72-C-1291, with the Air Force Avionics Laboratory, Wright-Patterson AFB, Ohio 45433.

This technical report has been reviewed and is approved for publication.

Robert M. Werner

ROBERT M. WERNER
Project Engineer

GARY L. MALLALEY, LT
Actg Chief, Processor Technology Gp
Microelectronics Branch

FOR THE COMMANDER

STANLEY E. WAGNER, Chief
Microelectronics Branch
Electronic Technology Division

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Silicon on sapphire	Local oxidation	Silicon nitride
Ion-beam milling	Sulfur hexafluoride	

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Three techniques for planarizing silicon-on-sapphire epitaxial islands are investigated. These three approaches are thermal oxidation isolation, ion-implantation isolation, and SIS (silicon-in-sapphire). N-channel MOS transistors fabricated using thermal oxidation isolation exhibit large edge leakage currents and are bias-temperature unstable. Stable p-channel MOS transistors can be fabricated if the

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field oxide is grown below 950°C in HCl steam. Test transistors fabricated using ion-implantation isolation show very large edge leakage current. Although implantation doses of 2×10^{17} atoms/cm^2 in 0.6-μm-thick films are used, very little isolation is achieved. With SIS, holes are ion milled or gas-phase etched with SF_6 in the sapphire substrate prior to being filled with silicon. Data showing the interrelationship between etchant masks, dimensional control, and transistor characteristics are presented.

PREFACE

The research reported herein was conducted at RCA Laboratories, Princeton, New Jersey 08540 in the Integrated Circuit Technology Center, J. H. Scott, Jr., Director, under Air Force Contract No. F33615-72-C-1291 during the period 1 April to 31 December 1975. N. Goldsmith was the Project Supervisor, and C. E. Weitzel was the Project Scientist. Robert M. Werner was the Air Force Project Engineer.

The author is deeply indebted to the following people for their contributions to the successful completion of this work: D. Capewell -- wafer preparation, gas-phase etching and epitaxial silicon growth; Z. Turski -- ion-beam milling; E. C. Douglas -- ion implantation; B. Seabury -- scanning electron microscope; G. Auth -- talysurf; L. Barlow and P. Messineo -- polishing; A. Herrgott, J. Sokoloski, W. Salt, T. Pawlick, and M. Jones -- wafer processing; and A. C. Ipri, N. Goldsmith, J. Cartwright, and S. T. Hsu -- technical assistance.

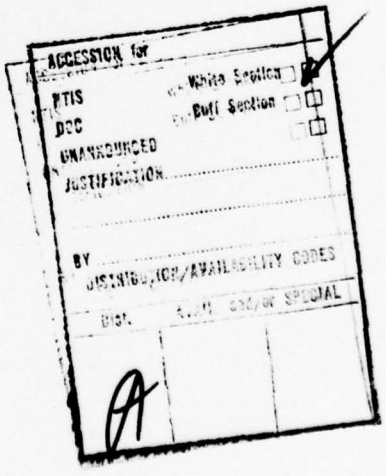

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

Section I
INTRODUCTION

In recent years CMOS/SOS (Complementary Metal Oxide Semiconductor/Silicon On Sapphire) has been heralded as the next step in the evolution of CMOS integrated circuits (ICs). CMOS/SOS offers the advantages of CMOS, low power consumption and high noise immunity, and in addition offers higher speed and better isolation. The better isolation is inherent in the process because the silicon which is not incorporated into transistors is etched away leaving bare sapphire. It was thought that this better isolation could be translated into higher packing density. Unfortunately, the increase in packing density has only been partially achieved because of problems related to the nonplanarity of the wafers following the etching of the silicon epitaxial film to obtain isolation. Present technology calls for the silicon film to be no less than 0.6 μm thick. Therefore, conductors (polysilicon or metal) must traverse two 0.6-μm steps everytime they cross a silicon island. Studies have shown that if the conductor widths and/or spacings are reduced much below present design rules, problems with open-circuits and/or short-circuits occur. These problems have also necessitated the present design rules on minimum island spacings. Moreover, in high-reliability circuits, problems with metal making contact to the island edges were perceived, so that contact holes were opened only on the top of the island. Thus, the silicon islands must be tenths of a mil larger than if the surface were planar. In addition, with IC technology progressing to smaller and smaller devices with gate lengths as small as 1.0 μm, the development of a planar SOS technology is imperative.

In this work three approaches to achieving a planar SOS technology were investigated. In the thermal oxidation isolation approach, the silicon that is not to be incorporated into transistors is converted to SiO_2. A variation on this approach involves partially etching the silicon before oxidation. The second technology investigated involves implanting the silicon between the transistors with nitrogen or oxygen to make this part of the SOS film semi-insulating. The third technology, called SIS (silicon-in-sapphire) because following island isolation, the silicon epi is actually in the sapphire substrate, is accomplished by creating holes in the substrate where the transistors are to be and then refilling with epitaxial silicon.

The three approaches are compared on the basis of electrical characterization of test transistors and potential for use as a high-density LSI technology. Considerable data are presented showing the leakage current and bias-temperature (B-T) stability of test transistors fabricated by each technique. Scanning electron micrographs (SEMs) are used to show the degree of planarity achieved.

SECTION II
EXPERIMENTAL PROCEDURE

All of the devices discussed in this report were fabricated in nominally 0.6-μm silicon epitaxial film grown on $(1\bar{1}02)$ Czochralski sapphire wafers supplied by Union Carbide. Prior to H_2 firing at 1200°C for 30 min, the wafers were cleaned and scrubbed. The epitaxial film was deposited on the 1.5-in.-diameter wafers in a five-sided barrel reactor by the pyrolysis of SiH_4 at approximately 970°C. The films for the deep-depletion process were doped approximately 1×10^{15} n-type during growth. Films for the enhancement process were doped approximately 1×10^{15} p-type and then counter-doped n-type using implantation in the appropriate area.

Since the planarization processing steps were done first, all subsequent processing steps were identical. The test transistors were fabricated using the p+ polysilicon gate deep-depletion or enhancement process [1,2]. Processing lots consisted of five wafers, one of which was always a control wafer. The silicon islands on this state-of-the-art wafer were defined by growing a thin oxide in HCl steam. The oxide was defined and etched so that it remained only over the silicon that was to be the silicon islands. The unprotected silicon was etched away in KOH, and the thin SiO_2 was removed in buffered HF. At this point in the process the control wafer was ready for channel oxidation. Since the planarization process results in island definition, the first common processing step for the control and planarized wafers was the 1200-Å channel oxide growth which was done at 900°C or 950°C in HCl steam. This was followed by polysilicon deposition at nominally 700°C in SiH_4. The polysilicon was then selectively doped from a boron-doped oxide driven-in at 1050°C in helium. Following selective doping, the polysilicon was selectively etched in KOH, and the channel oxide was self-align etched. Next, phosphorus-doped oxide was deposited and defined for sources and drains, and then boron-doped oxide was deposited for sources and drains. The source and drain dopant was driven-in at 1050°C in helium, followed by postdiffusion oxidation and hydrogen annealing. The contact holes were then opened, and aluminum was evaporated and defined. The final processing step was alloying the aluminum.

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1. J. C. Sarace and A. C. Ipri, Electrochemical Society, Fall Meeting 1974, Abstract #197.
2. A. C. Ipri and J. C. Sarace, IEEE J. Solid State Circuits SC-11, 329 (1976).

After the device fabrication, the planarity and electrical characteristics of the transistors were studied. The planarity was studied by scanning electron microscopy. Of particular importance in the electrical characterization was the field-effect transistor (FET) mobility, leakage current, and B-T stability. The FET mobility can be inferred by comparing the threshold voltage of devices fabricated by one of the planar techniques and those on the control wafer. In general, none of the wafers studied in this program showed severe mobility degradation.

The bulk of the experimental data to be presented in this report deals with the leakage current and B-T stability of planar structures. As a basis for comparison, typical results for the test transistors fabricated on the control wafers are presented in Fig. 1. These data show the transfer characteristics for a p-channel enhancement-mode device and an n-channel deep-depletion device. Together they form a CMOS inverter. The drain current (log scale) is plotted as a function of the gate voltage (linear scale) for a source-drain voltage of 5 V. The p-channel and n-channel transistors are 1.0 mil wide with a source-drain spacing of 0.4 mil. The data were taken both before and after B-T stress. The solid line shows the data before stressing and the dashed line shows data after stressing. The B-T stress consisted of heating the device to 250°C, and then applying +10.0 V or -10.0 V to the gate of n-channel or p-channel transistors, respectively, for 15 min with the source and drain grounded. After the stressing, the bias was removed, and the transistors were cooled to room temperature in several minutes. The transfer characteristic was then measured exactly as before stressing. Typical results for control devices fabricated by the p+ polysilicon gate deep-depletion process are shown in Fig. 1. The p-channel device is essentially unchanged following B-T stress. The n-channel device, on the other hand, shows a small decrease in edge current following B-T stress. The leakage current in n-channel devices in this low-current range is referred to as edge leakage current because the leakage occurs along the silicon island edge. Edgeless MOS/SOS transistors, wherein the drain completely surrounds the channel and source regions, do not exhibit edge leakage current and typically also show no change following B-T stress. The problem of edge leakage currents in SOS/MOS

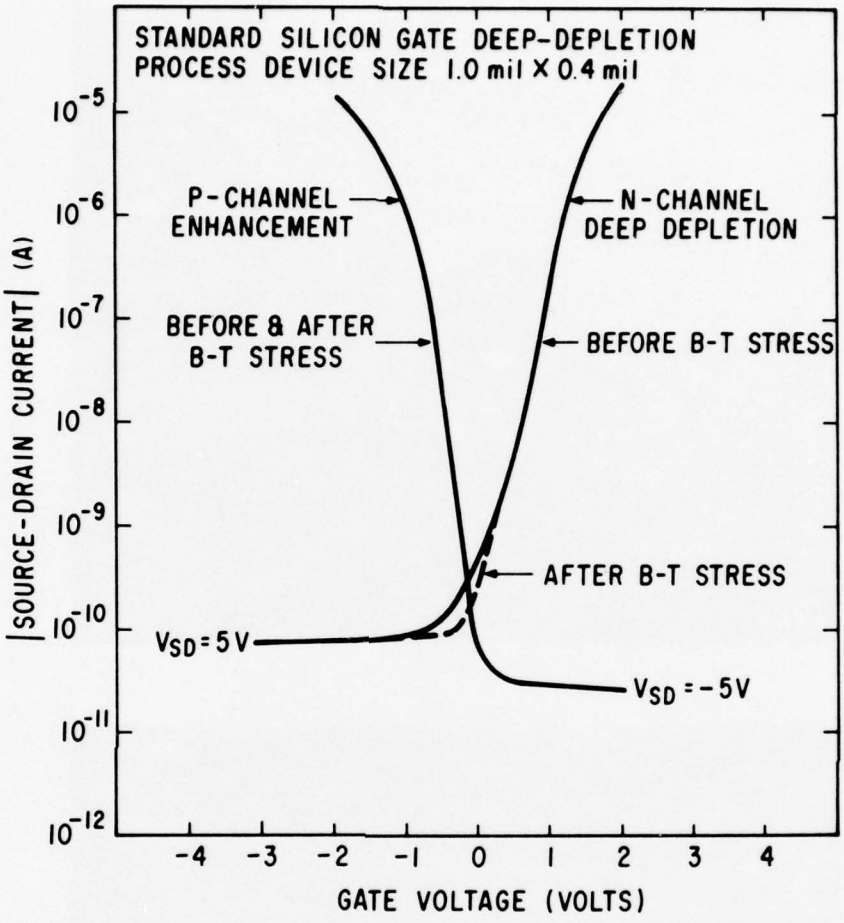
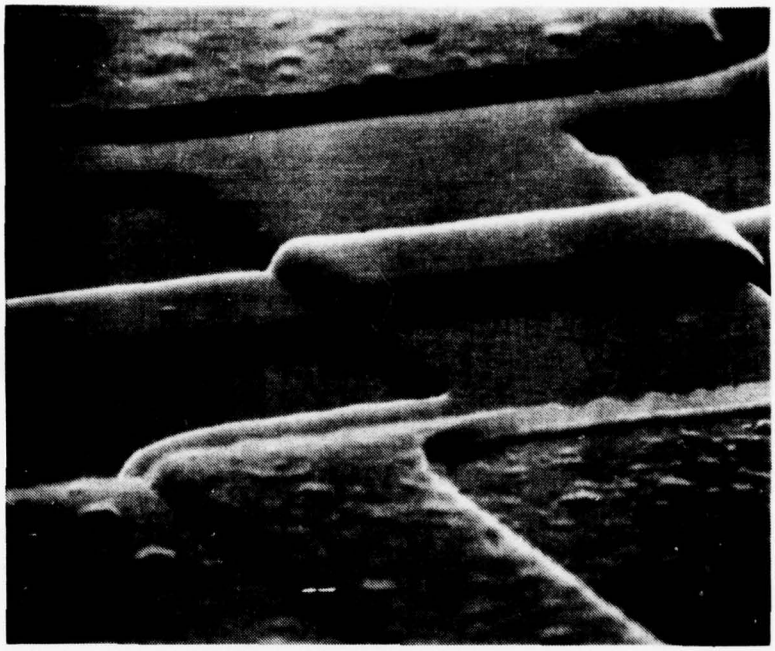


Figure 1. Transfer characteristics of n-channel deep-depletion transistor and p-channel enhancement transistor on control wafer.

transistors has received much attention [3,4]. The data presented in Fig. 1 form the basis of comparison for devices fabricated by the planar techniques that are discussed later in this report.

The topology of transistors fabricated on the control wafers is shown in Fig. 2. Figure 2(a) shows the finished device magnified 5000X. At the top and bottom of the picture are the source and drain contacts, respectively.

3. D. W. Flatley and W. E. Ham, Electrochemical Society, Fall Meeting 1974, Abstract #198.
4. J. L. Gates and O. K. Griffin, Appl. Phys. Letters 27, 43 (1975).



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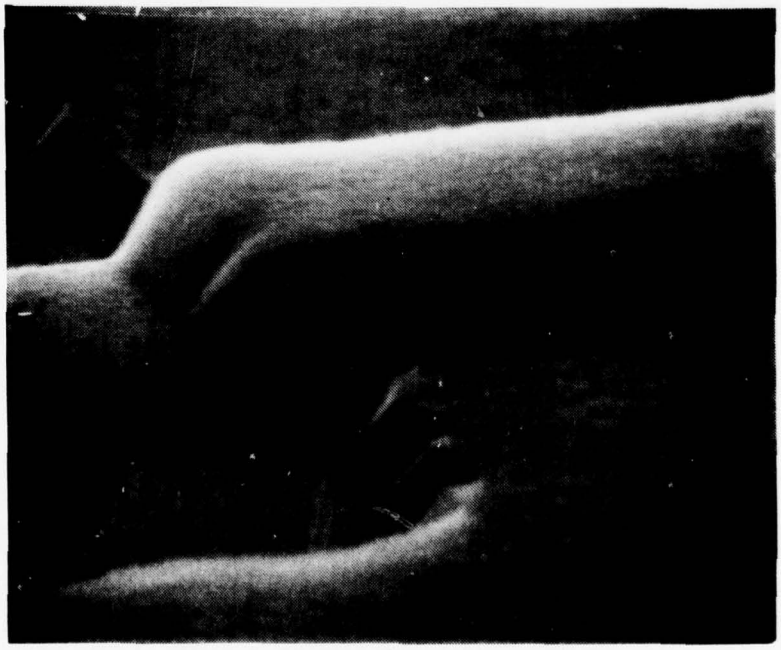


(b)

Figure 2. (a) SOS/MOS transistor on control wafer (5000X). (b) Polysilicon gate crossing silicon epitaxial island on control wafer (20,000X).

The source and drain are part of the same silicon island. The band running from left to right is the polysilicon gate. To the left and right of the silicon island the polysilicon is on the sapphire substrate and encounters two 0.6-μm steps in crossing the silicon island. A cross section of an MOS transistor fabricated on a control wafer is shown in Fig. 3. In Fig. 2(a) the doped oxides cover the finished device. However, in Fig. 2(b) the doped oxides (at 20,000X) have been removed. The material in the lower left corner is the Al_2O_3 substrate. The p+ polysilicon gate runs across the substrate, up the silicon island edge in the center of the picture, and across the top of the silicon island. The shadowed region between the silicon island and the polysilicon gate is the undercut channel oxide, 1200 Å thick. The raggedness of the silicon epi island is also shown. Similar pictures of devices fabricated by the various planar technologies are presented in the next section.

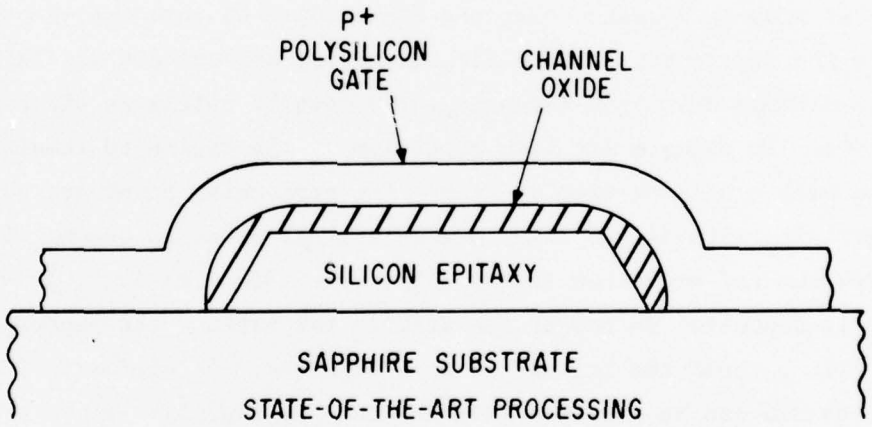


Figure 3. Cross section of SOS/MOS transistor fabricated using state-of-the-art processing.

SECTION III
EXPERIMENTAL RESULTS

A. THERMAL OXIDATION ISOLATION

This planarization technology basically involves oxidizing all or part of the SOS film between the silicon islands. Since a silicon film of thickness t_o converts to a SiO_2 film of thickness 2.22 t_o, planarity would result only if 0.33 μm of the original 0.6-μm silicon film between the islands were etched before oxidation. Since, typically, the silicon epi thickness varies across each wafer, from wafer to wafer in the same deposition lot and even from wafer to wafer in different processing lots, routine achievement of perfect planarity is difficult. Thus, instead of achieving perfect planarity, a more meaningful goal would be to reduce in height or alter the slope of the steps at the silicon island edge so that problems with step coverage of polysilicon or metal would be minimized.

The first step in investigating the feasibility of this approach to pseudo-planarity is the development of the technology for selectively oxidizing silicon. The previously developed technology for locally oxidizing silicon [5] was applied to SOS. To oxidize the film selectively, the region to remain silicon is protected with a silicon nitride film. The processing steps are shown in Fig. 4. Beginning with an SOS film, a thin thermal oxide is grown. The SiO_2 is only a few hundred angstroms thick, after which 500 Å of Si_3N_4 is deposited. A SiO_2 film is deposited on top of the nitride for masking the phosphoric acid etch. The film between the islands is then oxidized. An estimate of the oxidation time required can be obtained from the data in Fig. 5. From a processing standpoint it would be preferrable to do the field oxidation at as high a temperature as possible to minimize the oxidation time. Test transistors were studied wherein the field oxidations were done at 900°C, 950°C, 1000°C, and 1050°C. To completely convert a 0.6-μm SOS film to SiO_2 would require approximately 5 hours in HCl steam at 1050°C. At lower temperatures the time would be much longer. Following oxidation the masking materials are removed; the resulting structure is shown at the bottom of Fig. 4. From this point on the

5. J. A. Oppels and M. M. Paffin, Philips Research Report 26, 157 (1971).

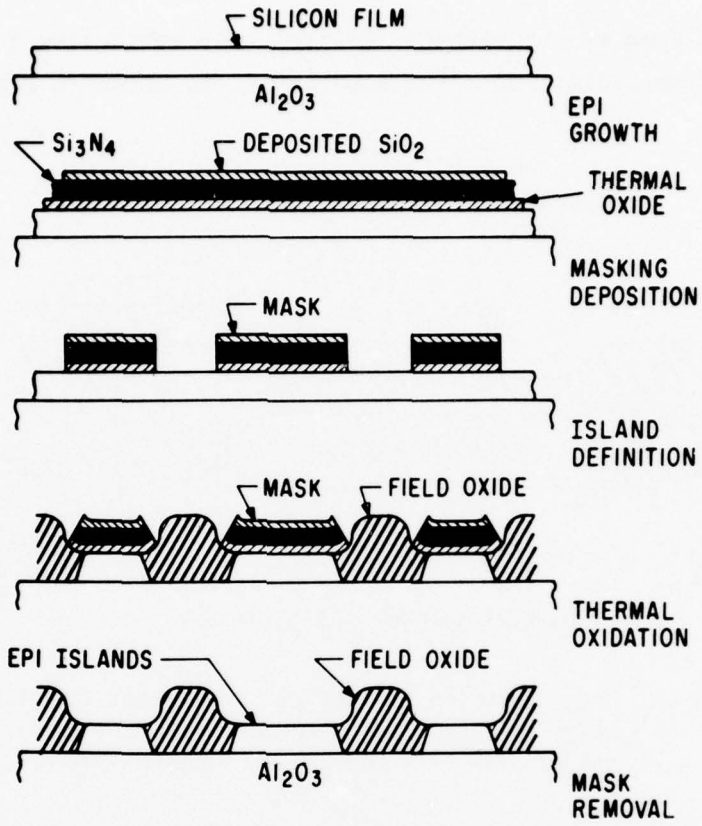


Figure 4. Processing sequence for thermal oxidation isolation wherein the the entire SOS film around the transistors is oxidized.

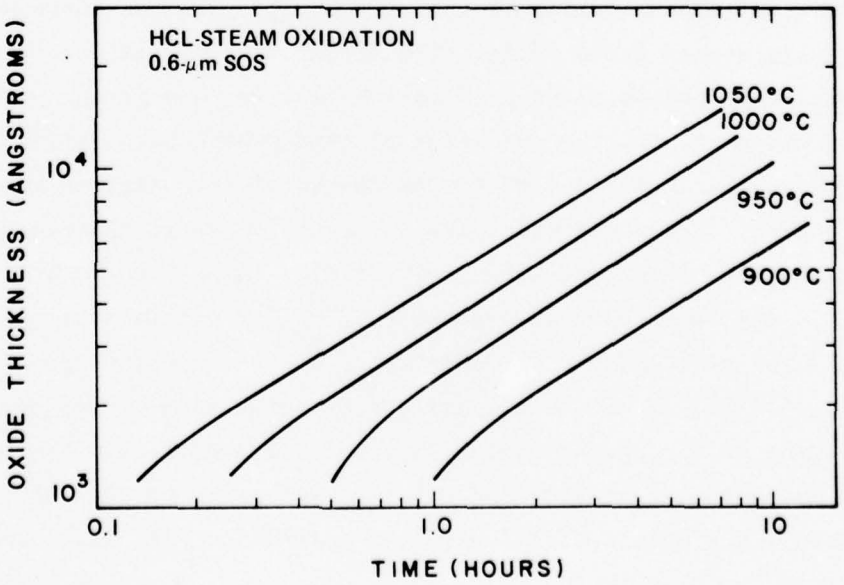


Figure 5. SiO_2 growth rate in HCl steam.

processing is the same as the standard silicon gate processing steps discussed previously. A cross section of a finished device is shown in Fig. 6.

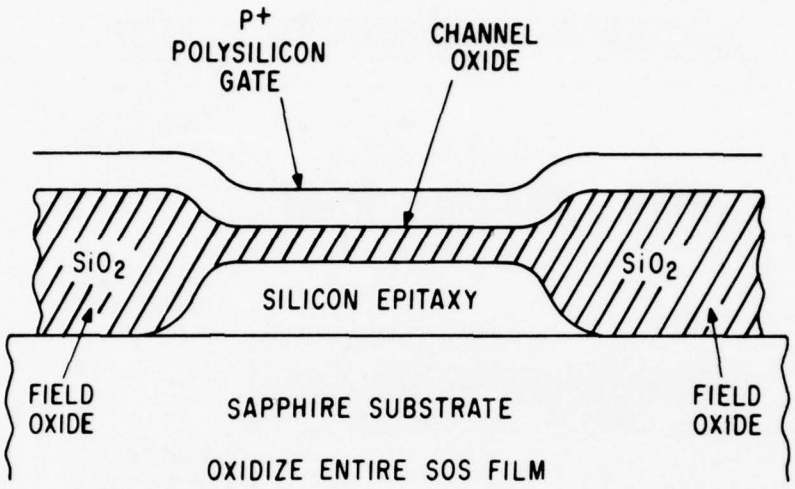
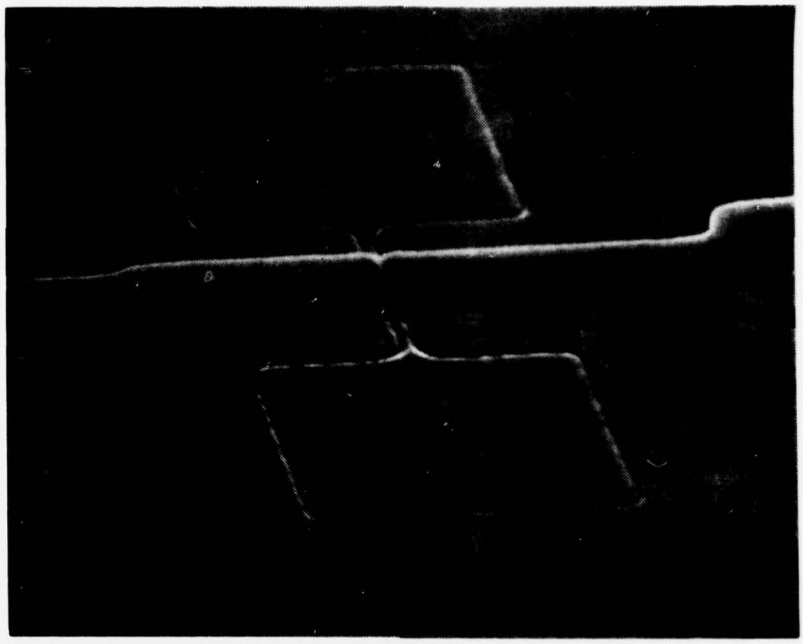


Figure 6. Cross section of SOS/MOS transistor fabricated using thermal oxidation isolation wherein the entire SOS film around the transistors is oxidized.

SEM photographs of finished devices, which have had the doped oxides removed, are shown in Fig. 7. Figure 7(a) shows a very narrow MOS/SOS transistor. The dumbbell-shaped region is the silicon epi, and the surrounding region is the partially etched field oxide. The horizontal band is the polysilicon gate. This picture points out a problem inherent in this planar process. During field oxide growth, the oxidation process occurs both vertically and horizontally, so that the sides of the protected silicon regions are slowly converted to SiO_2. The areas which are to be transistors, therefore, slowly shrink in size. For the transistor shown in Fig. 7(a), the width of the channel, originally 0.1 mil, was reduced to about 0.03 mil by the lateral oxidation of the silicon. For wide transistors this would not be a serious problem. Figure 7(b) (20,000X) shows the polysilicon dropping from on top of the field oxide to the top of the channel oxide, which is 1200 Å thick. The remaining field oxide is on the right side and the silicon epi is on the left side of the photograph. The undercutting under the polysilicon resulted from removing



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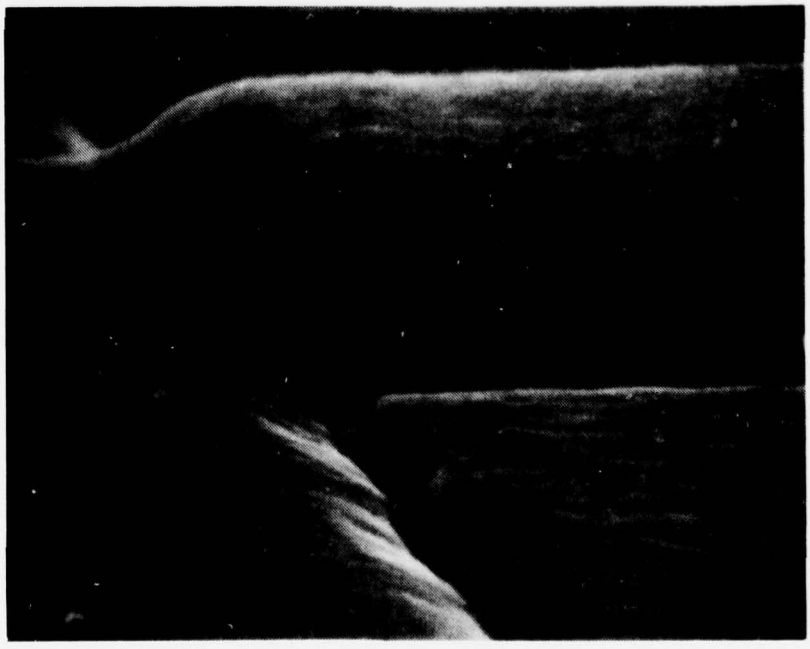


(b)

Figure 7. (a) SOS/MOS transistor on wafer wherein the entire epi film around the transistor has been oxidized (2000X). (b) Polysilicon gate crossing field oxide and dropping to silicon epi island (20,000X).

the doped oxide in buffered HF. Although this approach has resulted in a polysilicon step of equal magnitude to the control wafer, it is conceivable that this step may present fewer step coverage problems than the silicon epi island step.

The electrical characterization of the MOS transistors fabricated by this process indicates that although the p-channel enhancement-mode transistors show no mobility degradation, low leakage, and B-T stability, the n-channel

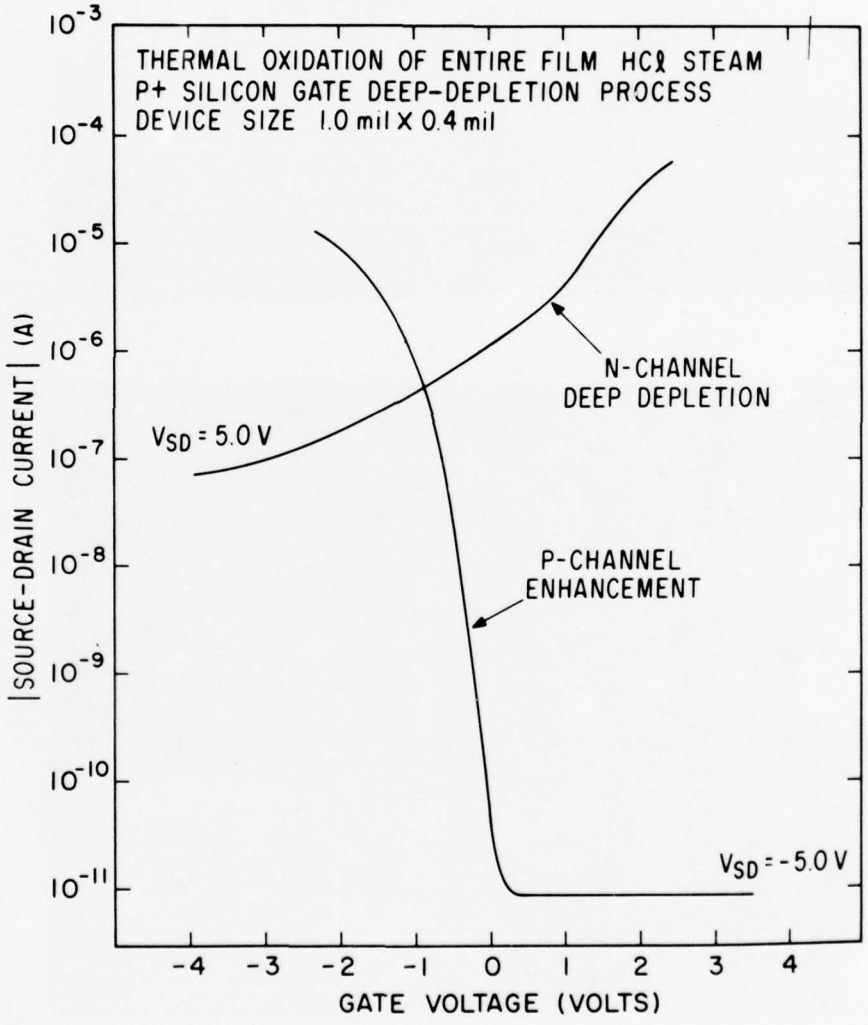


Figure 8. Transfer characteristics of n-channel deep-depletion transistor and p-channel enhancement transistor from a wafer wherein the entire epi film around the transistors has been oxidized.

deep-depletion transistors have large edge leakage currents. The transfer characteristics of these transistors are shown in Fig. 8. The drain current is plotted as a function of the gate voltage. The source-drain voltage is 5.0 V. Even reverse-biasing the gate of the n-channel device does not reduce the leakage current to the level of the control device shown in Fig. 1. Edgeless n-channel devices in which the channel region does not include the silicon island edge did not show this high leakage current. These results should not be surprising, however, because the effect of the work function difference between the p+ polysilicon gate and the silicon epi is significantly reduced by the thicker oxide on the island edge. The positive oxide charge would tend to accumulate the n-type epi. This would prevent leakage between source and drain in the p-channel device but permit considerable leakage between source and drain in the n-channel device.

One technique for improving the planarity of the above approach is to etch part of the silicon epi away prior to field oxidation. If the thickness of the film is uniform across the wafer and if just the right amount of silicon is etched away, the polysilicon encounters no steps in crossing the silicon islands. The processing steps are shown in Fig. 9. The only difference between this processing sequence and that shown in Fig. 4 is the partial etch of the silicon epi. Unfortunately, even etching the silicon does not result in a perfectly planar surface because of the oxide ridging problem [5]. By referring to the partial etch step in Fig. 9, it is easily seen that the surface area of the silicon to be oxidized is larger than the surface area to be covered with SiO_2. This causes the oxide ridging around the silicon island. A more detailed cross-sectional drawing of an MOS fabricated by this process is shown in Fig. 10. Recent work has been directed at minimizing this ridging [6]. In the work reported here no effort was made to minimize the ridging.

Because of the nonuniform epi thickness it is difficult to uniformly etch just the right amount of silicon. Figure 11 shows the best results that were obtained. In Fig. 11(a) the polysilicon gate is shown (10,000X) crossing the silicon epi island. The field oxide has been removed. Since the epi island

5. J. A. Oppels and M. M. Paffin, Philips Research Report 26, 157 (1971).
6. E. Bassous, H. N. Yu, and V. Maniscolco, Electrochemical Society, Fall Meeting 1975, Abstract #175.

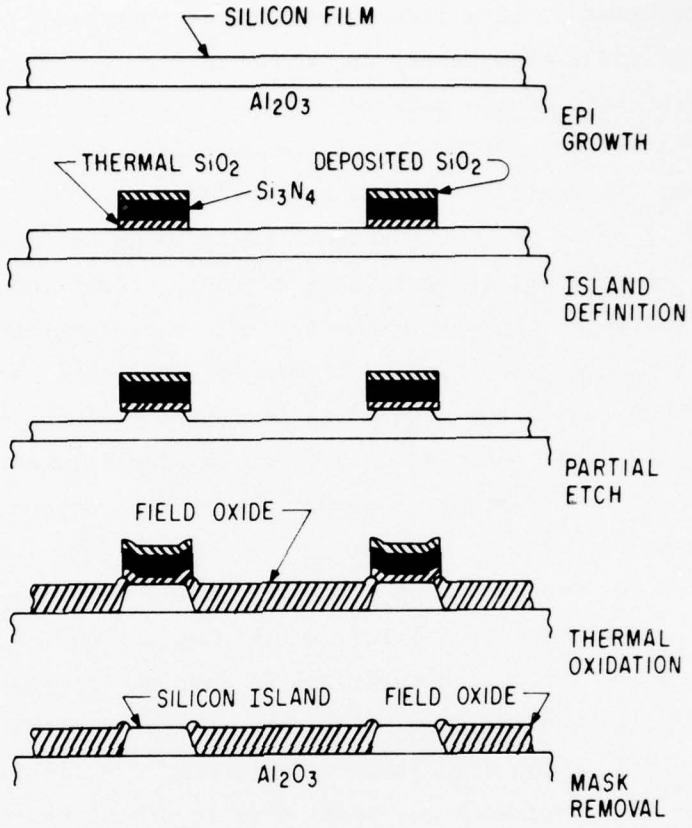


Figure 9. Processing sequence for thermal oxidation isolation wherein the SOS film around the transistors is partially etched before being oxidized.

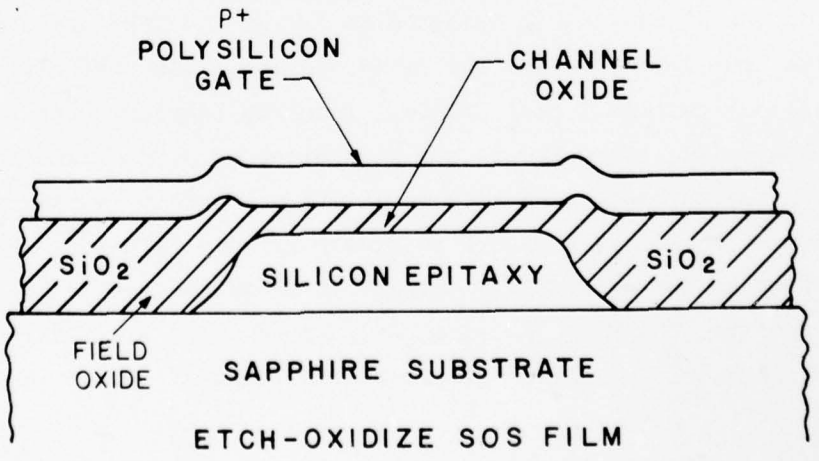
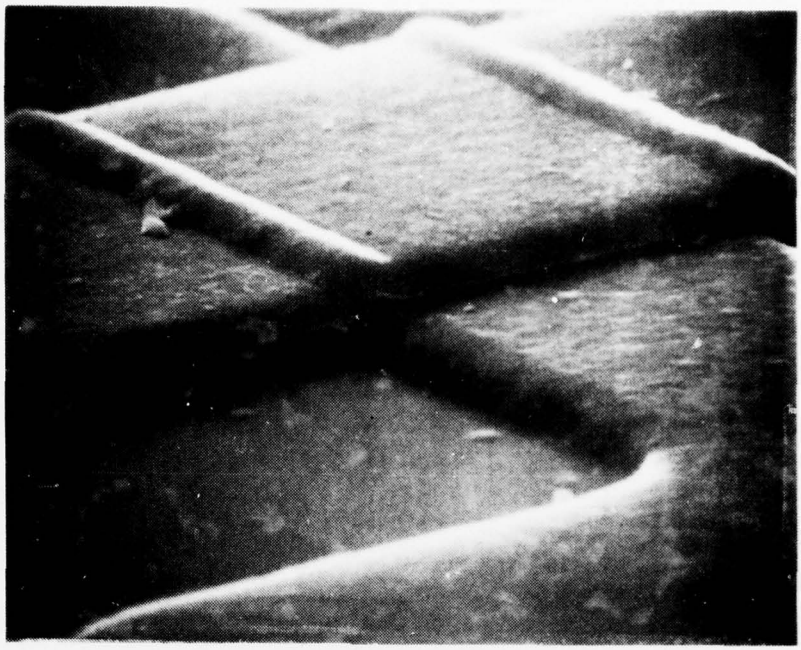


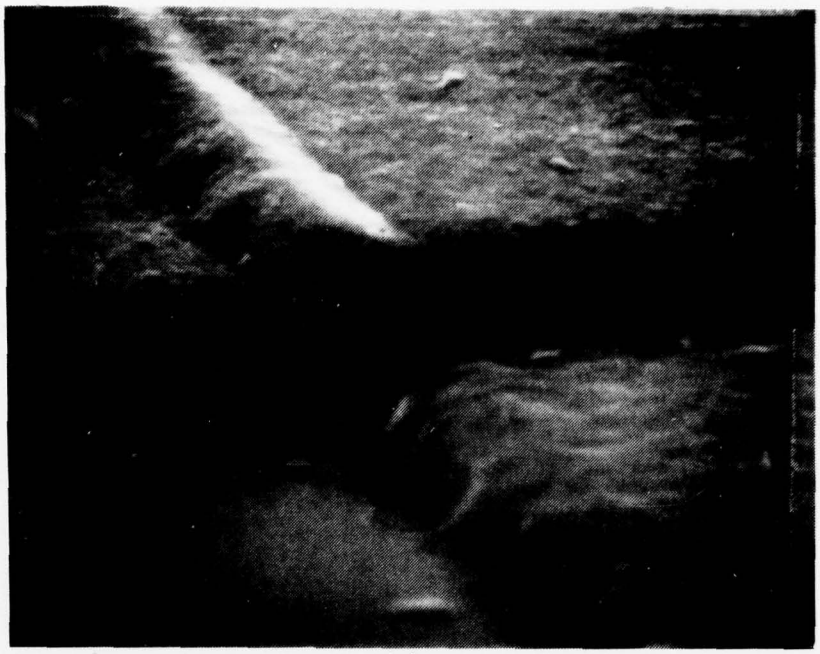
Figure 10. Cross section of SOS/MOS transistor fabricated using thermal oxidation isolation wherein the SOS film around the transistors is partially etched before being oxidized.



(a)

(b)

Figure 11. (a) SOS/MOS transistor on wafer wherein epi film between transistors was partially etched before oxidation (10,000X). (b) Polysilicon gate crossing field oxide and silicon epi island (20,000X). Oxide ridging caused by partially etching SOS film before oxidation.



(c)

Figure 11. (c) Polysilicon gate crossing field and silicon epi island (20,000X). Oxide ridging caused by partially etching SOS film before oxidation.

is 6000 Å thick and the channel oxide is 1200 Å thick, the polysilicon undergoes a level translation of less than 2000 Å, excluding the ridging. Figure 11(b) shows the oxide ridging magnified 20,000X. The sapphire substrate is shown in the lower left corner, the silicon epi island to the right. The polysilicon runs across the top half of the picture. The undercutting between the polysilicon and the epi silicon shows the location and thickness of the 1200-Å channel oxide. Figure 11(c) shows the same region at a slightly different angle; the contour of the silicon island edge and the polysilicon step is easier to see. The transfer characteristics of the devices pictured in Fig. 11 are shown in Fig. 12. The field oxide on this wafer was grown at 1050°C in HCl steam. These data show that there is no FET mobility degradation, and, more importantly, the problem with the large edge leakage current found for devices fabricated in films that were completely oxidized is not present. The leakage current for a source-drain voltage of 15 V is less than 1 nA/mil. These leakage current levels compare very favorably with those of devices fabricated on control wafers such as that shown in Fig. 1.

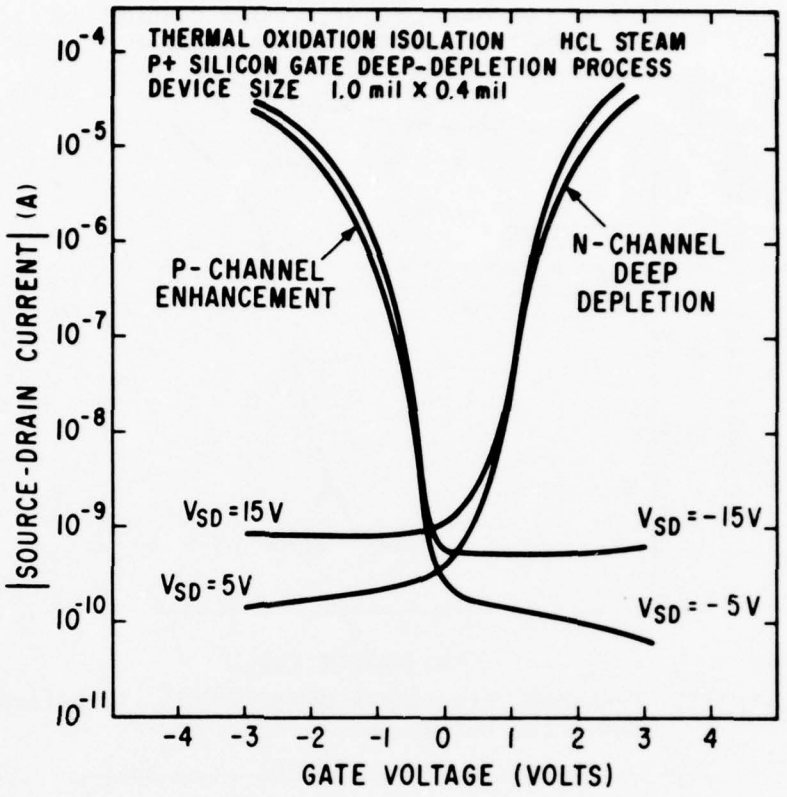


Figure 12. Transfer characteristics of n-channel and p-channel transistors from wafer wherein the epi film around the transistors was partially etched before oxidation at 1050°C in HCl steam.

Despite the encouraging results for as-processed devices, the data in Figs. 13 and 14 show that neither the n-channel deep-depletion transistors nor the p-channel enhancement transistors are B-T stable. The B-T stress consists of heating the device to 250°C, applying +10.0 V to the gate of the n-channel device or -10.0 V to the gate of the p-channel device for 15 min, and then removing the bias and cooling the device rapidly to room temperature. The transfer characteristics are remeasured with the same source-drain voltage, 5 V. During B-T stress the source and drain are grounded. After the B-T stress the n-channel device is almost totally insensitive to changes in gate voltage, conducting well in excess of 10 μA. Edgeless transistors fabricated

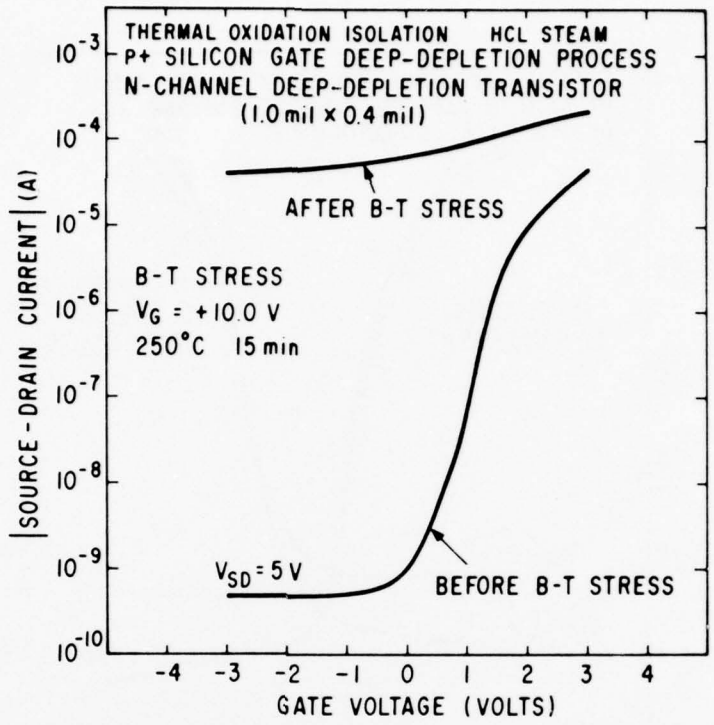


Figure 13. N-channel transistor shown in Fig. 12 before and after B-T stress.

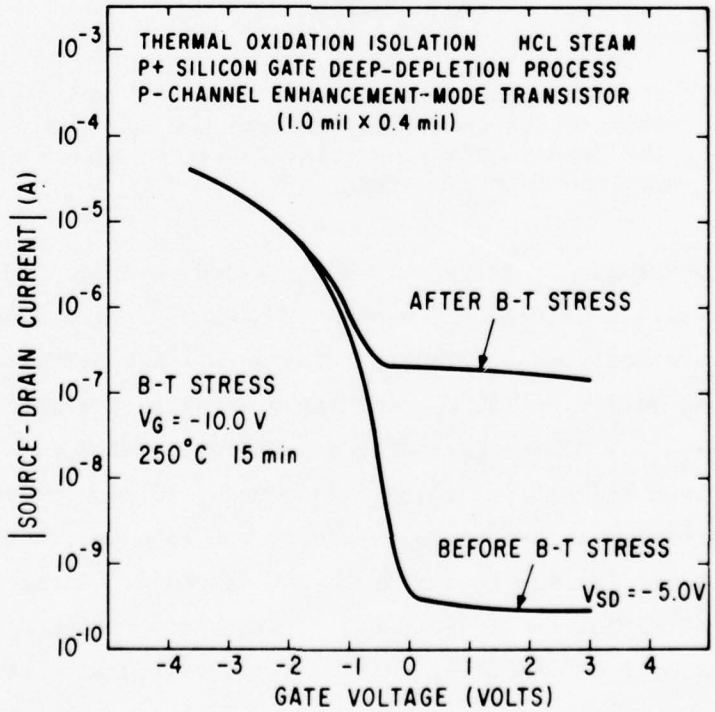


Figure 14. P-channel transistor shown in Fig. 12 before and after B-T stress.

on the same wafer as these edge transistors have no B-T instability. Therefore, the instability is a result of the silicon island edge being part of the channel region. The p-channel device also shows an edge instability as illustrated in Fig. 14, but not quite as severe as that of the n-channel device. The edgeless p-channel transistors do not display the instability.

P-channel transistors fabricated on wafers wherein the field oxidation is done at lower temperatures show a steady improvement in edge stability. Figure 15 depicts the transfer characteristics of a p-channel device whose

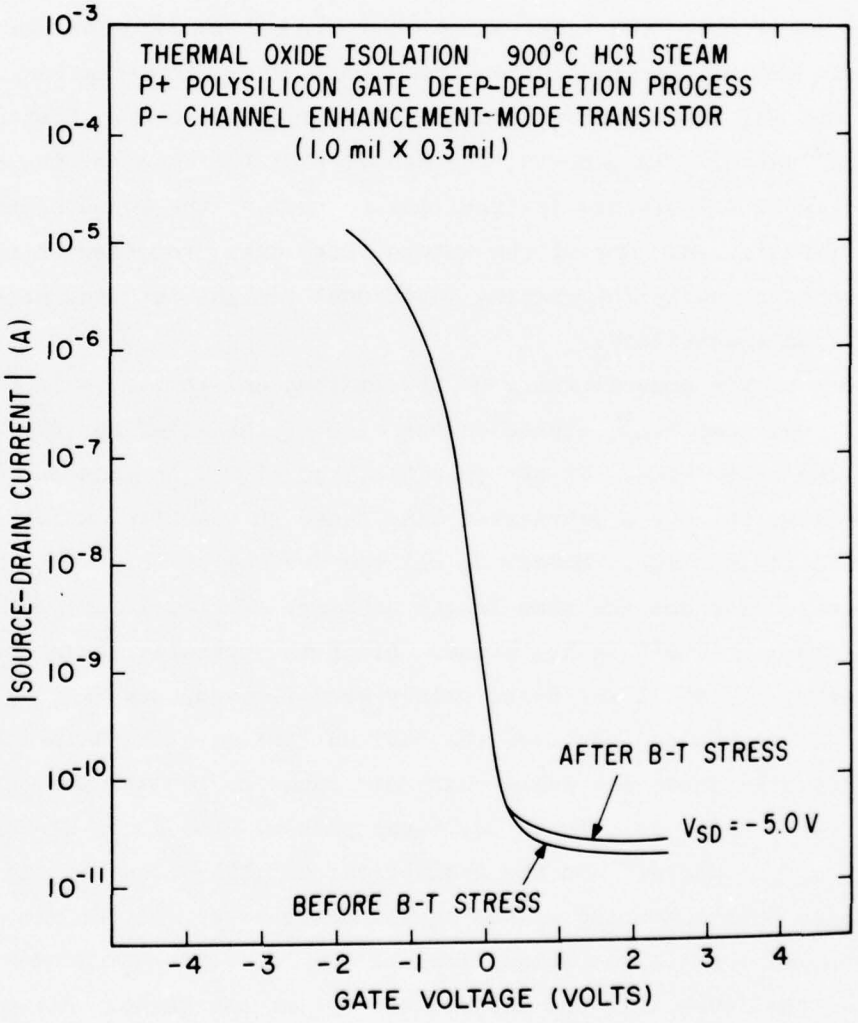


Figure 15. Transfer characteristic of p-channel transistor before and after B-T stress. After partially etching SOS film between transistors, the field oxidation was done at 900°C in HCl steam.

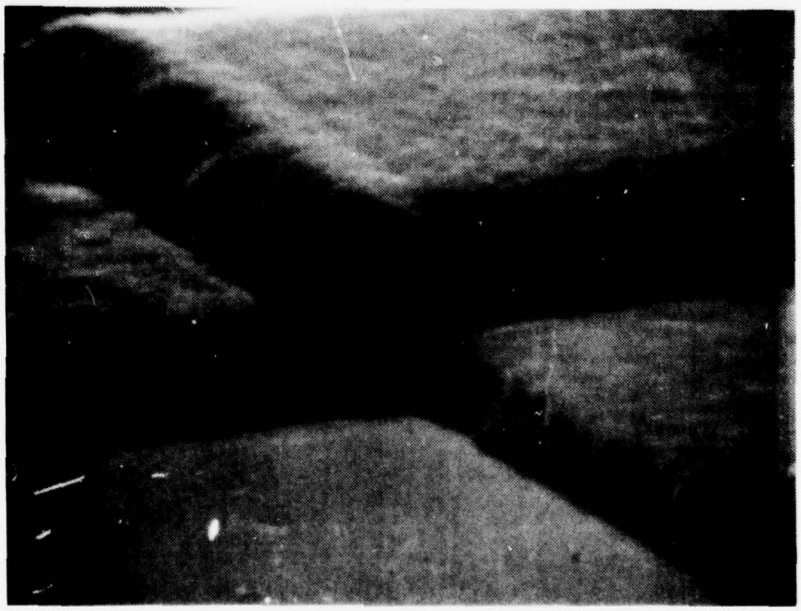
field oxide was grown at 900°C in HCl steam. The data indicate that the transistor is B-T stable. However, n-channel devices fabricated on the same wafer as this p-channel transistor show the same edge instability as that shown in Fig. 13. Lowering the field oxidation temperature did not reduce the n-channel edge in stability.

Since the experimental data indicate that stable p-channel devices could be made if the field oxidation were done at 900°C in HCl steam, the stability of n-channel enhancement MOS transistors was also studied. It was hoped that since the epitaxial film would be doped p-type it would be less sensitive to charges in the oxide. The fabrication of n-channel enhancement transistors is identical to that of deep-depletion transistors with the exception of the doping of the SOS film. For enhancement-mode transistors the film is doped $1 \times 10^{15}/cm^3$ p-type. In general, the behavior of the edges of the n-channel enhancement-mode transistors is identical to that of the edges of the deep-depletion transistors. One of the wafers which were processed in this study provided an opportunity for gaining additional insight into the problem of n-channel edge instability.

Because of the nonuniformity of the silicon epi thickness on this wafer, the silicon was completely etched on one side of the wafer and only partially etched on the other side. It was possible, therefore, on this one wafer, to compare devices which are fabricated like those on a control wafer and devices which have a field oxide. Moreover, all the devices on this wafer were in the field oxidation furnace the same length of time. The field oxide on this wafer was grown at 900°C in HCl steam. After the transfer characteristics were measured, the metal and doped oxides were removed, and SEM photographs were taken of the island edges of the devices that were characterized electrically. Figure 16 shows the edges that correspond to the transfer characteristics shown in Figs. 17 through 20, respectively. The small black speck in the center of the picture and the smaller one slightly above it are the result of burn spots in the coating of the oscilloscope screen of the SEM.

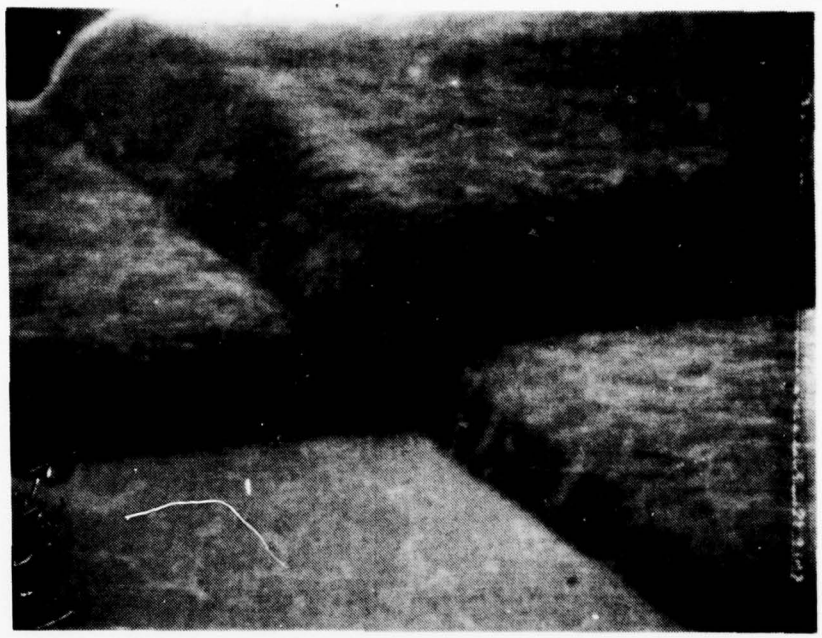
Figure 16(a) shows the polysilicon at the top of the picture with bare sapphire at the lower left and the silicon epi at the right. All of these SEMs were taken at 20,000X. The channel oxide, 1200 Å thick, fills the region between the polysilicon and the epi. This region is undercut because buffered HF was used to remove the doped oxide. The oxide on the edge of the island is

(a)

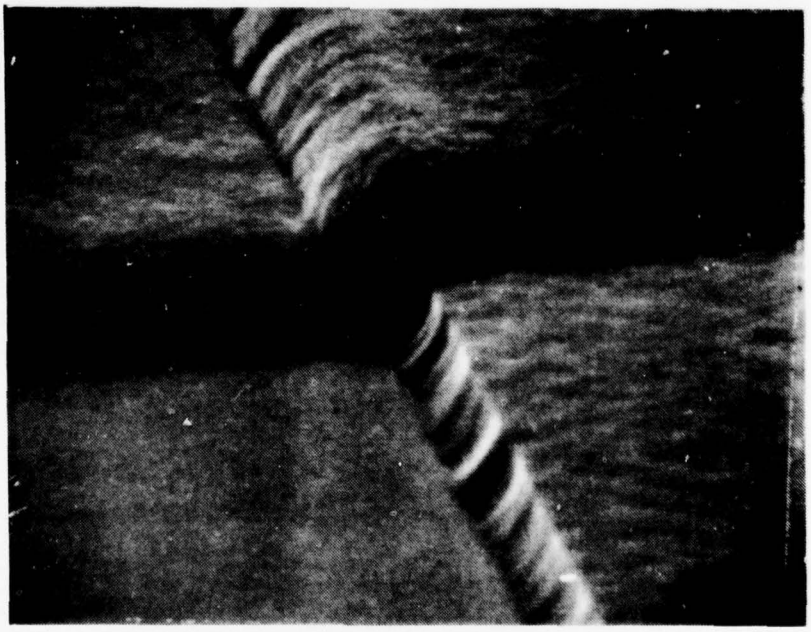


(b)

Figure 16. (a) Polysilicon gate crossing silicon epitaxial island. There is no undercutting between polysilicon and sapphire substrate. (b) Polysilicon gate crossing silicon epitaxial island. There is very slight undercutting between polysilicon and sapphire.



(c)



(d)

Figure 16. (c) Polysilicon gate crossing silicon epitaxial island. Undercutting between polysilicon and sapphire is clearly visible. (d) Polysilicon gate crossing silicon epitaxial island. Polysilicon is separated from the sapphire by more than 1000 Å.

slightly thicker than on a typical control wafer (Fig. 2), which has not been subjected to any field oxidation. Slight ridging of the polysilicon gate can also be seen. Of particular importance is the fact that the polysilicon comes into contact with the sapphire directly opposite the bottom of the edge of the silicon island. The transfer characteristic of the transistor shown in Fig. 16(a) is given in Fig. 17. In comparing this characteristic with that of a typical control device, shown in Fig. 1, we note the effect of the change in epi doping from 1 x 10^{15} n-type to 1 x 10^{15} p-type on the threshold voltage.

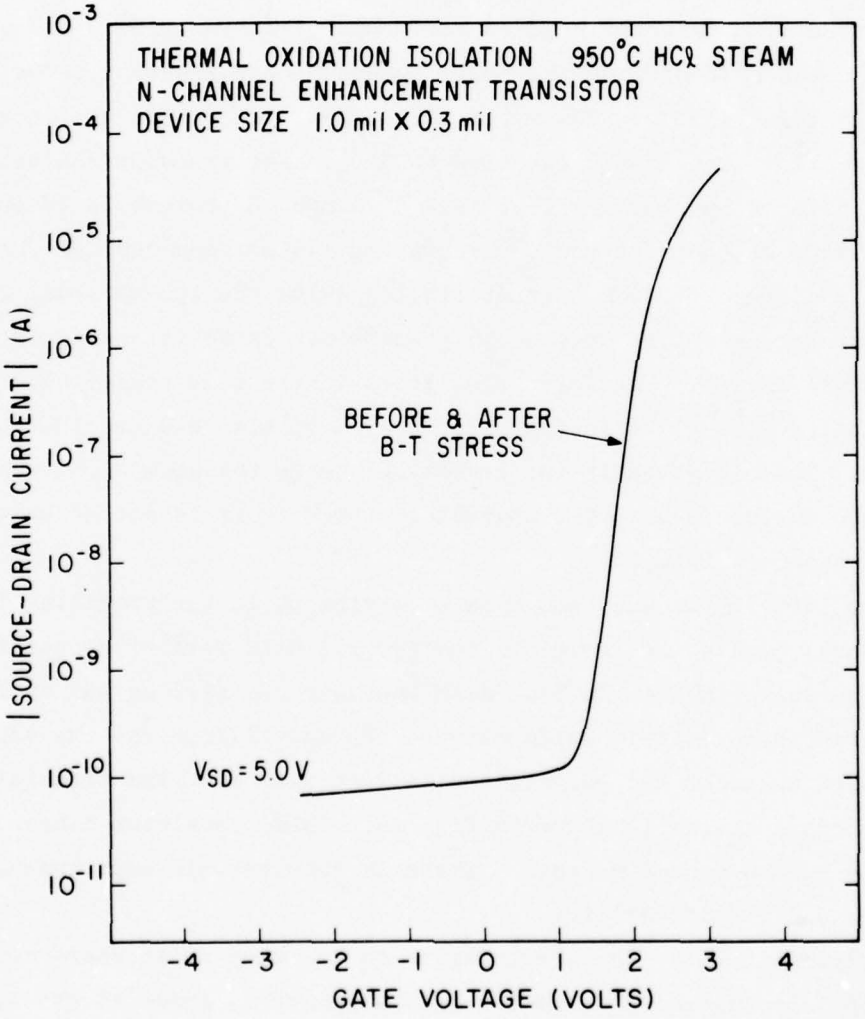


Figure 17. Transfer characteristic of n-channel enhancement transistor shown in Fig. 16(a) before and after B-T stress.

If the gate voltage necessary to achieve 1 μA of channel current is used as the threshold voltage, the V_{TH} of the enhancement-mode device is 2.05 V, whereas that of the deep-depletion device in Fig. 1 is 1.30 V. The result of B-T stressing this enhancement device is also shown in Fig. 17. The transistor is B-T stable just like the control device.

Figure 16(b) shows the polysilicon gate, sapphire substrate, and silicon epi island just as in Fig. 16(a). This transistor, however, is located 192 mils from the one shown in Fig. 16(a). Careful examination of this picture indicates that the polysilicon is not in contact with the sapphire but is separated from it by several hundred angstroms of field oxide. The presence of this oxide is evident from the small amount of undercutting under the polysilicon. In this region of the wafer all of the silicon was not etched. During film oxidation it was converted to SiO_2. The transfer characteristic of this transistor is shown in Fig. 18. Although the threshold voltage is almost the same as that for the device in Fig. 16(a), the rest of the curve is radically different. The current flowing below the 100-nA level is called edge current because it is present in transistors whose island edges are part of the channel region. Edgeless transistors in the same pellet show transfer characteristics like those in Fig. 17. The curve also has considerable hysteresis. This is probably the result of charge trapping along the edge region. The device is also B-T unstable. However, it is not as unstable as the device shown in Fig. 13.

Figure 16(c) shows the same type of device as in the preceding illustrations; however, again the device is located 192 mils further across the wafer from the one shown in Fig. 16(b). Here the unetched silicon was even thicker. This resulted in more field oxide between the polysilicon and the sapphire. The undercutting under the polysilicon is very obvious. The transfer characteristic of this device is shown in Fig. 19. This transistor behaves almost identically to the preceding one. There is considerable edge leakage current, hysteresis, and B-T instability.

Finally, Fig. 16(d) shows a location on the same wafer where even more silicon was left unetched. Here the bare sapphire is shown at the lower left, the silicon island on the right, and the polysilicon gate across the top of the

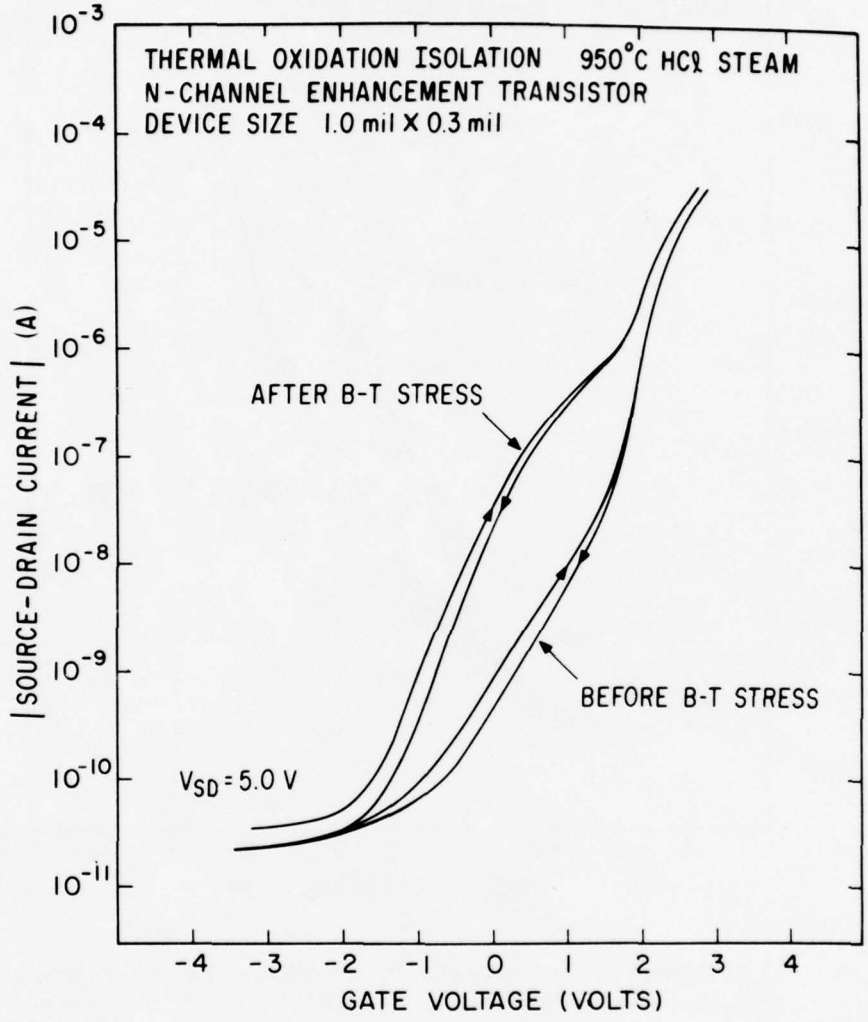


Figure 18. Transfer characteristics of n-channel enhancement transistor shown in Fig. 16(b) before and after B-T stress.

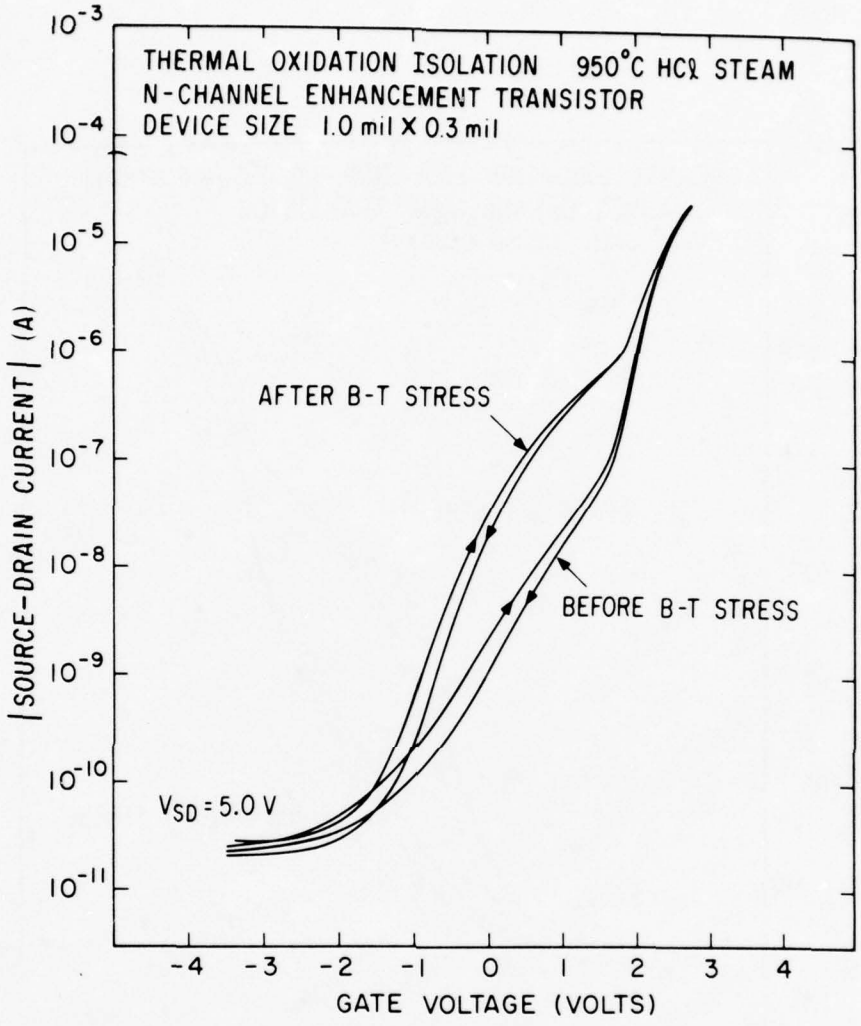


Figure 19. Transfer characteristic of n-channel enhancement transistor shown in Fig. 16(c) before and after B-T stress.

picture. Figure 20 shows the transfer characteristics of this transistor. This device is the most unstable of the four devices studied. This device also has the thickest field oxide. The device, however, is not as unstable as the device shown in Fig. 11; that one has even more field oxide than this device.

Another interesting phenomenon which the unstable n-channel devices exhibit is that the transfer characteristic after B-T stress can be relaxed to its pre-stressed state. This is accomplished by temperature stressing a device which

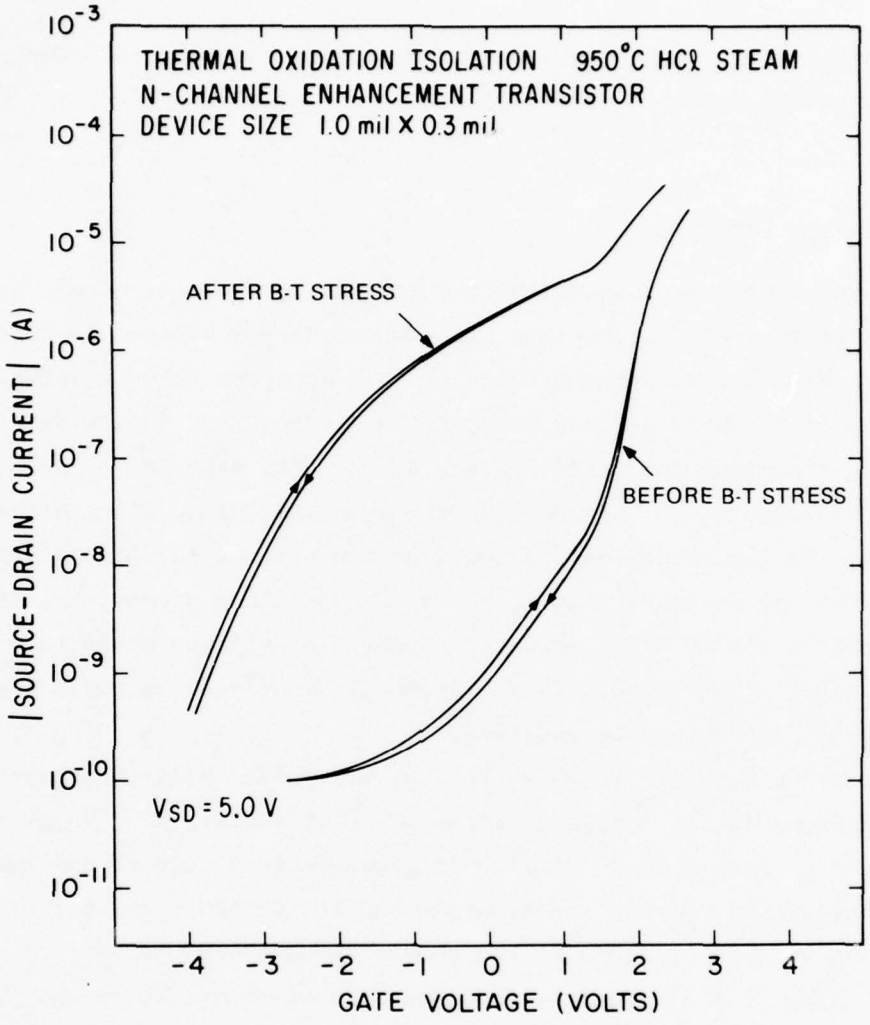


Figure 20. Transfer characteristic of n-channel enhancement transistor shown in Fig. 16(d) before and after B-T stress.

has been B-T stressed. In temperature stressing, the device is merely heated to 250°C for 15 min with no bias applied. On cooling the device to room temperature, the transfer characteristic has either partially or completely relaxed to its pre-stressed state. The device can then be B-T stressed again, in which case the transfer characteristic moves as before, and on temperature stressing the device relaxes again. This phenomenon, along with the observations regarding the relationship between the amount of instability and the

field oxide thickness, suggests a model to explain this effect. The proposed model is discussed later in this report.

B. IMPLANTATION ISOLATION

This planarization technique involves implanting the silicon epi between the silicon islands with atoms that will cause the epi silicon to become semi-insulating. From a conceptual standpoint this approach is very appealing. The silicon epi is never etched, and all that is required is the development of a masking technique for large implant doses. The other major problem is obtaining the large doses. To achieve the semi-insulating film, either nitrogen or oxygen is implanted. An estimate on the size of the implantation dose can be obtained by assuming that to get semi-insulating properties, the silicon must contain $5 \times 10^{21}/cm^3$ impurity atoms. The silicon would then contain about 10% oxygen or nitrogen. In a 0.6-mm-thick SOS film an implantation dose of $3 \times 10^{17}/cm^2$ would be required.

The processing sequence is shown in Fig. 21. After silicon epi growth, the implantation mask is applied. First 500 Å of thermal SiO_2 is grown on top of the silicon. Then 1 μm of aluminum is evaporated on top of the oxide. The oxide was sandwiched between the aluminum and silicon to prevent the aluminum from alloying with the silicon if the sample becomes very hot during the implantation step. The aluminum is then defined and etched where the implantation is to be permitted. Next, the wafer is implanted, following which the masking materials are removed. Prior to processing some of the wafers were annealed in helium.

No problems were encountered in using this masking scheme. Aluminum lines only 0.1 mil wide were routinely defined. However, considerable difficulty was encountered in obtaining large implantation doses. Initially, attempts were made at implanting the entire surface of a 1.5-in.-diameter wafer. With a beam current of 10/μA, implantation doses of over $1 \times 10^{16}/cm^2$ required unacceptably long times. To obtain larger doses, the area implanted was reduced to 1-cm-diameter area in the center of a 1.5-in. wafer. It was decided that meaningful experiments could be conducted using this small area and that, should the results prove promising, the technology could be easily

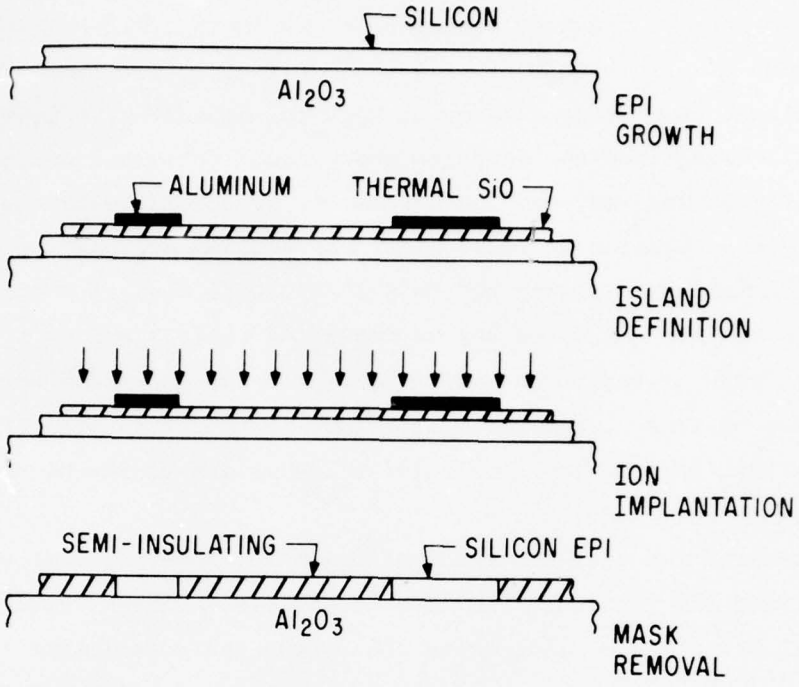


Figure 21. Processing sequence for implantation isolation.

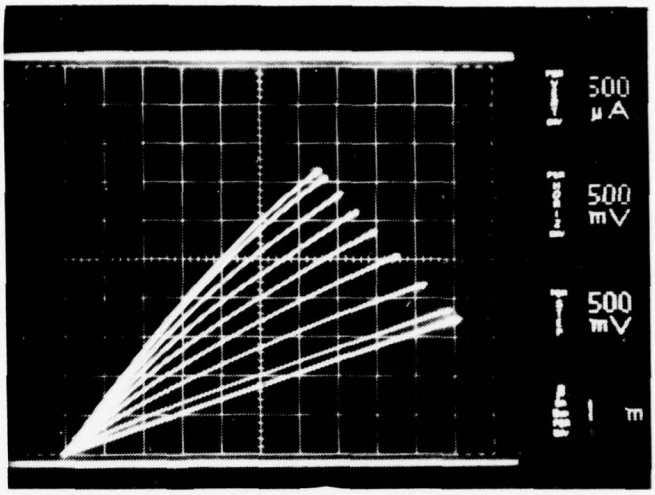
transferred to 3-in.-diameter wafers using state-of-the-art high-current ion-implantation equipment. The time required to implant 3-in.-diameter wafers would be commercially attractive.

During ion implantation two doses of $1 \times 10^{17}/cm^2$ are given each wafer. The doses are implanted at energies of 130 keV and 240 keV to distribute the nitrogen or oxygen throughout the 0.6-μm-thick SOS film. From a practical standpoint the nitrogen implant is much preferred, because implanting oxygen with a hot filament greatly limits filament life. Following implantation the implanted epi appears black when viewed in room light, whereas the aluminum mask, viewed through a microscope, is pitted, similar to the appearance of aluminum following alloying. This implies that the aluminum probably would have alloyed with the silicon epi if the oxide had not been present. The etch rate of the aluminum is much slower following implantation and therefore was removed in Caro's acid. Following removal of the oxide, 1000 Å of SiO_2 is deposited on the wafer. This oxide is used to prevent out-diffusion during annealing. Wafers are annealed for four hours at 1100°, 1050°, or 1000°C in

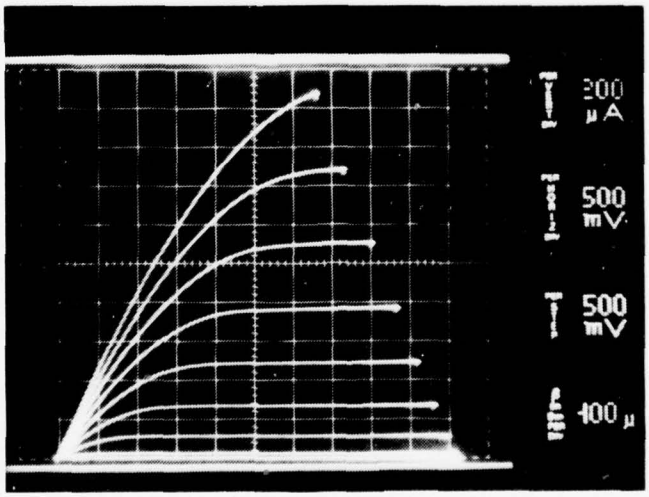
helium. Recent work [7] indicates that nitrogen implants in silicon resulted in the formation of a thin film of Si_3N_4 but only after the sample was annealed at 1200°C. Higher temperatures were not used for annealing implanted SOS films because of autodoping from the sapphire substrate. Following annealing the protective oxide is removed, and the wafers are processed using the p+ polysilicon gate deep-depletion process. The only problem encountered in processing was a difficulty in aligning the polysilicon gate mask with the silicon islands. Although the implanted and un-implanted regions are easily discerned in room light, when viewed through an aligner the implanted and un-implanted regions are not obvious. Therefore great care is needed in the first photoresist step after implantation. This is an indication of the planarity which this technology offers.

Examination of the test transistors indicates, however, that very little isolation between the transistor islands is achieved. These results are documented in Fig. 22. Figure 22(a) shows the output characteristics for an n-channel deep-depletion edge transistor 12.54 mils wide with a source-drain spacing of 0.4 mil. The vertical scale is 0.5 mA/div and the horizontal scale is 0.5 V/div. The gate voltage step is 0.5 V/step. The $V_G = 0$ line shows the leakage current between source and drain through implanted silicon epi, which is not depleted by the gate. At $V_{SD} = 5.0$ V, the leakage current is 1.7 mA. The results in Fig. 22(a) can be compared with those in Fig. 22(b) which were obtained from an edgeless transistor of the same size in the same pellet as the preceding device. The vertical scale in Fig. 22(b) is 0.2 mA/div. The only difference between the transistors is that one is edgeless and the other is a standard edge transistor wherein edge leakage current between source and drain can flow. Unfortunately, the results presented in Fig. 22(a) are the best which were achieved. This particular wafer was implanted with oxygen and annealed at 1100°C in helium for four hours. All wafers implanted with nitrogen and those implanted with oxygen but annealed at lower temperatures show higher leakage current. The prospects of achieving the desired isolation with this technology are discussed later in this report.

7. R. J. Dexter, S. B. Watelski, and S. T. Picraux, Appl. Phys. Letters 23, 455 (1973).



(a)



(b)

Figure 22. (a) Output characteristics of n-channel deep-depletion edge transistor fabricated on wafer wherein implantation isolation is used. (b) Output characteristics of n-channel deep-depletion edgeless transistor on same wafer as device shown in Fig. 22(a).

C. SIS (SILICON-IN-SAPPHIRE)

1. Ion Milling

This planarization technology is distinct from the preceding two because in this approach the silicon islands are imbedded into the sapphire substrate. This is accomplished by creating holes in the sapphire substrate prior to epi growth. The silicon epi is then grown in the standard manner, and the silicon which is not in a hole is polished away. This results in a perfectly planar surface.

There are several techniques for creating the holes. The technique which damages the sapphire substrate the least is to ion-beam-mill the holes [8]. The processing sequence is shown in Fig. 23. First an appropriate milling mask

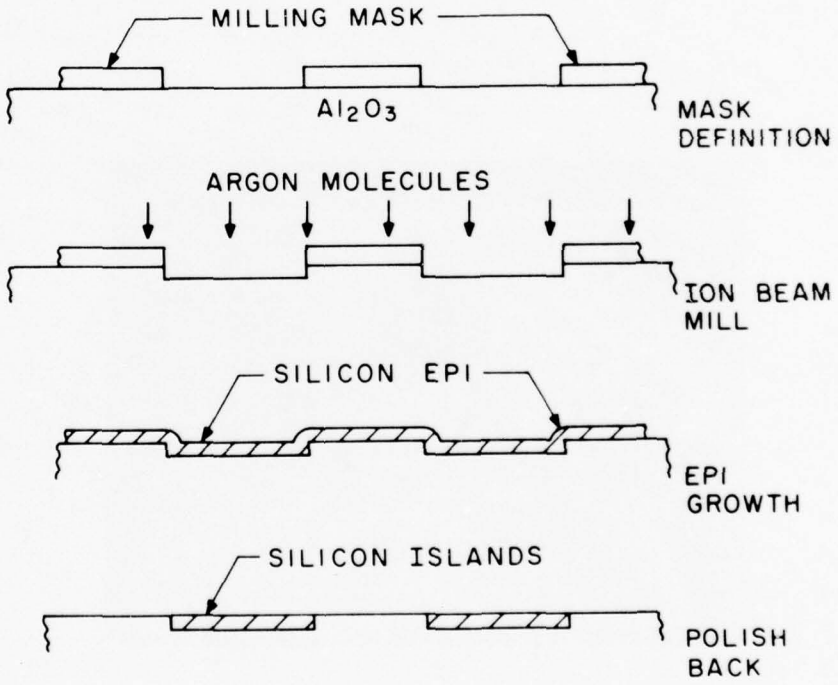


Figure 23. Processing sequence for ion-milled SIS

8. E. C. Spencer and P. H. Schmidt, J. Vacuum Science and Technology 8, 552 (1971).

is defined on the sapphire substrate. The wafer is then ion-milled. After milling, any remaining masking material is chemically removed. The wafer is then H_2-fired prior to growing the silicon epi. The silicon which is not in the holes is polished away. The wafer can now be processed normally using the p+ polysilicon gate process. A cross-sectional view of a finished transistor is shown in Fig. 24. If the silicon is polished perfectly flat with the surface of the sapphire substrate, the polysilicon will encounter a step of 500 Å in traversing the silicon island. This results because 500 Å of silicon is consumed in growing about 1000 Å of channel oxide.

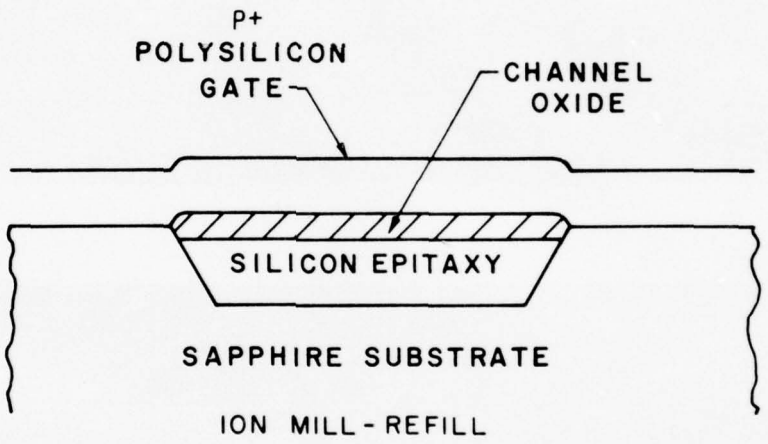
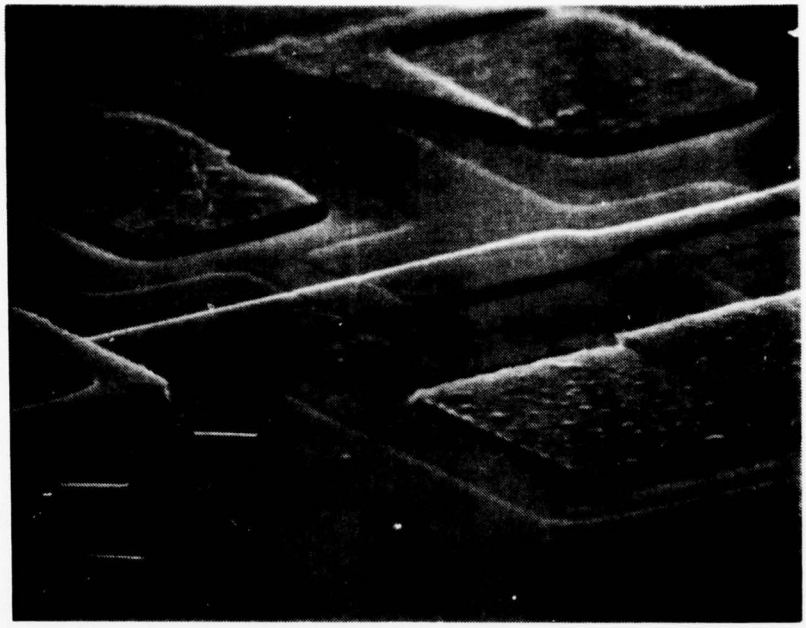


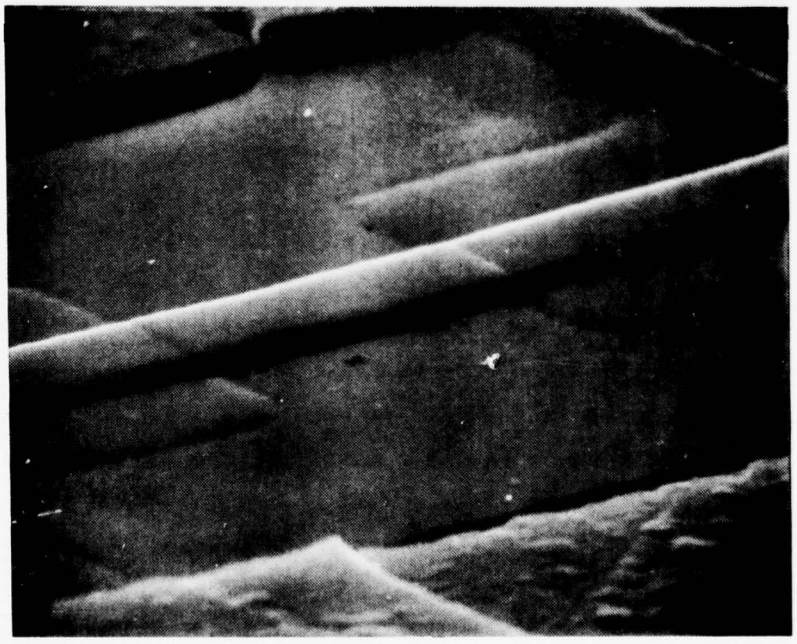
Figure 24. Cross section of ion-milled SIS/MOS transistor.

The planarity of the structure can be determined from the SEM pictures shown in Fig. 25. Figure 25(a) shows fabricated MOS transistors at 2000X. The metal and doped oxides prevent direct viewing of the channel oxide and polysilicon gate. The rough textured material at the top and right side of the picture is the aluminum contacts to the source and drain regions. Traversing the picture is the polysilicon gate. The dumbbell-shaped region is the silicon epi island. This photograph should be compared with Fig. 2(a) which shows the same type of structure on a standard-processed control wafer. Figure 25(b) shows the same device but at 5000X. The polysilicon gate lies across a negligibly small step at the island edge.

Figure 26 shows the transistors with the aluminum and doped oxides removed. Figure 26(a) is an overview of four small SIS/MOS transistors. The

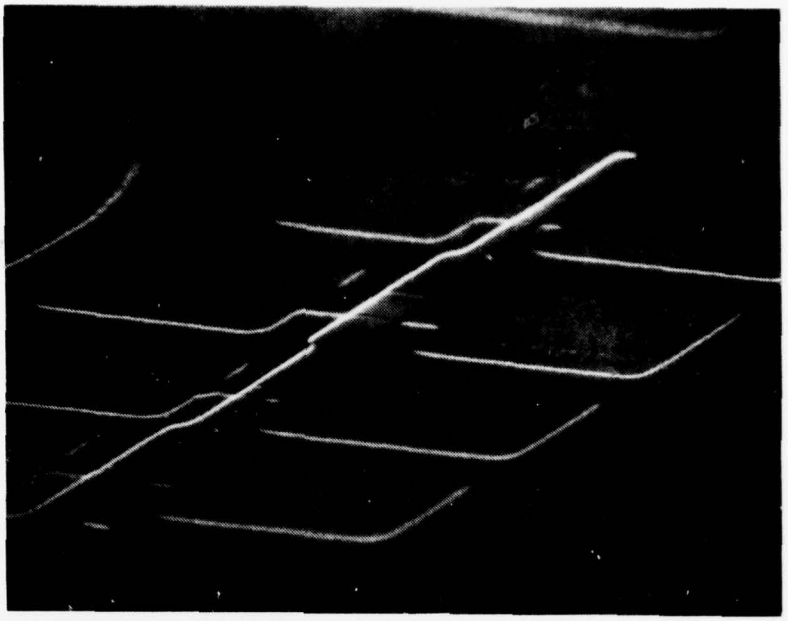


(a)

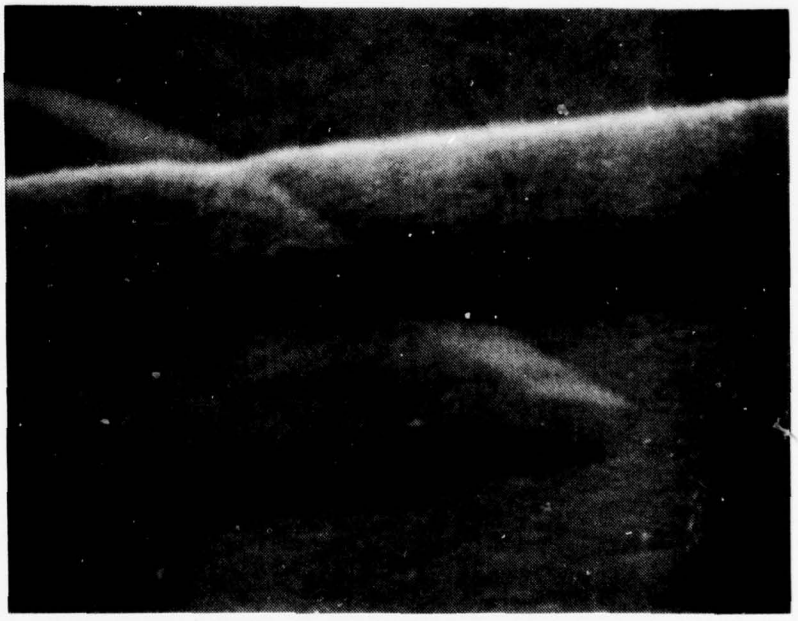


(b)

Figure 25. (a) Ion-milled SIS/MOS transistor (2000X). (b) Ion-milled SIS/MOS transistor (5000X).

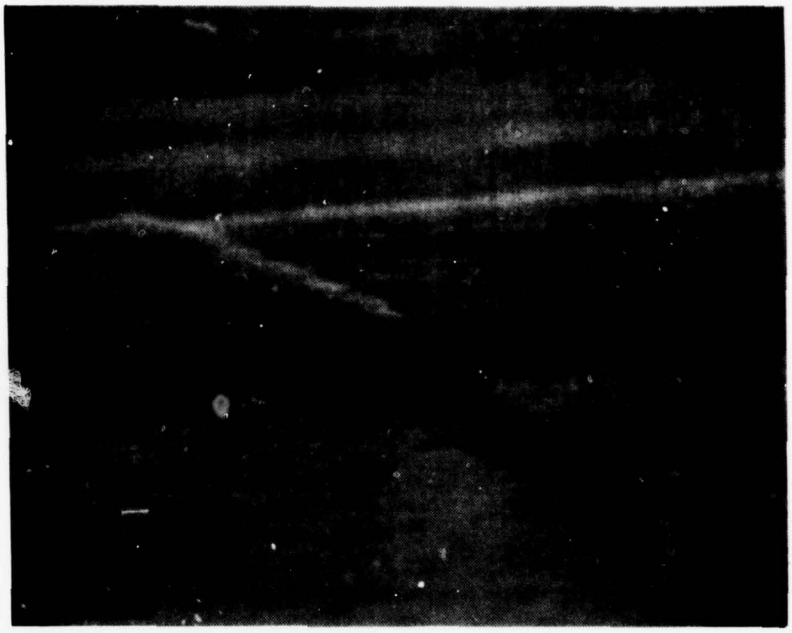


(a)

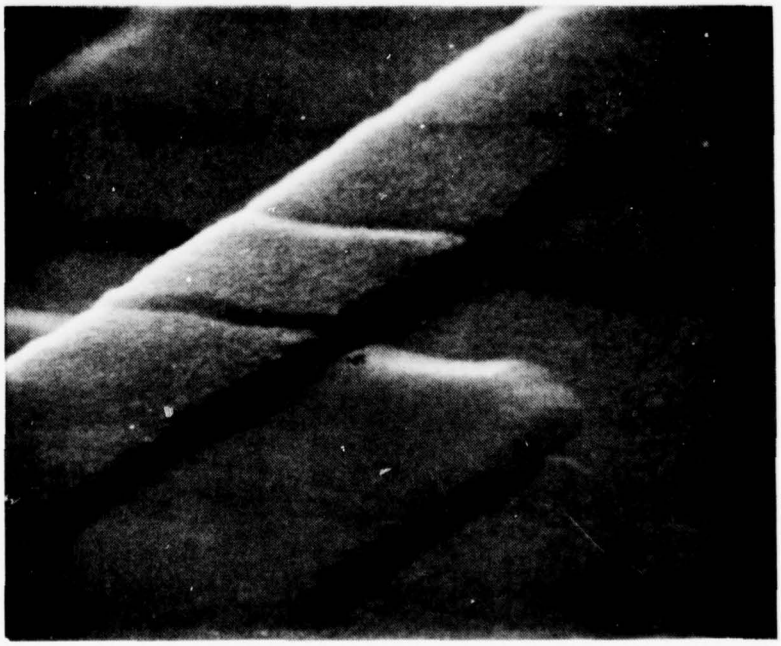


(b)

Figure 26. (a) Small ion-milled SIS/MOS transistors (1000X). (b) Polysilicon gate crossing silicon epitaxial region on ion-milled SIS wafer (20,000X).



(c)



(d)

Figure 26. (c) Polysilicon gate crossing silicon epitaxial region on ion-milled SIS wafer (20,000X). (d) Polysilicon gate crossing silicon epitaxial region on ion-milled SIS wafer (10,000X).

sources and drains are at the right and left. The polysilicon gate cuts across the picture at about a 45° angle. The silicon islands, the dumbbell-shaped regions, are recessed because the silicon has been oxidized and the oxide removed in buffered HF. Figure 26(b) shows one of the above transistors at 20,000X. The recessed region at the bottom and right side is the silicon epi. Bare sapphire is exposed on the left side; it is slightly higher than the silicon. Across the picture from left to right is the polysilicon gate. On the left it is in contact with the Al_2O_3, and on the right it is separated from the silicon epi by the channel oxide, 1200 Å thick. The polysilicon is about 5000 Å thick. Note the gentle slope of the side of the hole. Figure 26(c) shows the other side of the same channel region. In this picture it can be clearly seen that the oxide is thickest at the edge of the silicon island region. Figure 26(d) shows another MOS transistor at 10,000X. The sides of the hole milled in the substrate are inclined at a shallow angle. Attempts were made to get SEMs of the wafers just after polishing. Because of the almost perfect planarity, however, there were no surface features on which to focus.

The transfer characteristics of MOS transistors fabricated in these wafers are shown in Fig. 27. The data are for an n-channel deep-depletion transistor and a p-channel enhancement-mode transistor. Data taken with V_{SD} = 5.0 and 15.0 V are presented; they show that the only obvious problem is the increase in edge leakage current of the n-channel device. N-channel edgeless transistors do not show this edge leakage current. The background leakage level, FET mobility, gate dielectric strength, and threshold voltage are certainly acceptable. More importantly, as shown in Figs. 28 and 29, both the n-channel and p-channel transistors are B-T stable. The B-T stressing was done exactly as described previously. In Fig. 28, the edge leakage current decreases as a result of B-T stressing. N-channel devices fabricated on control wafers also show this type of behavior, if they initially have edge leakage current. This result can be compared with those presented for n-channel transistors that were planarized with thermally grown oxide (see Fig. 13). The p-channel devices are essentially unchanged following B-T stress. The small change in leakage current may have resulted from not returning the transistor to exactly the same temperature following B-T stress.

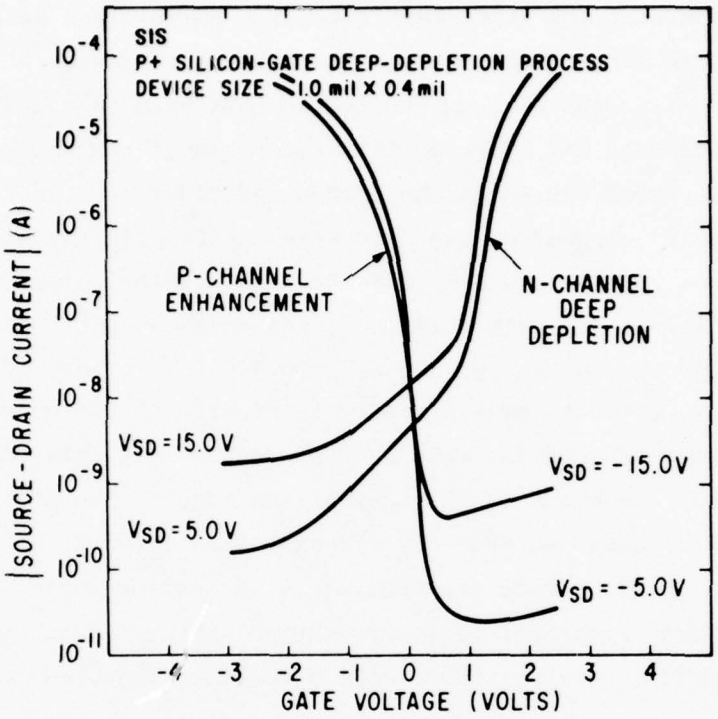


Figure 27. Transfer characteristics of an n-channel deep-depletion transistor and a p-channel enhancement transistor fabricated using ion-milled SIS.

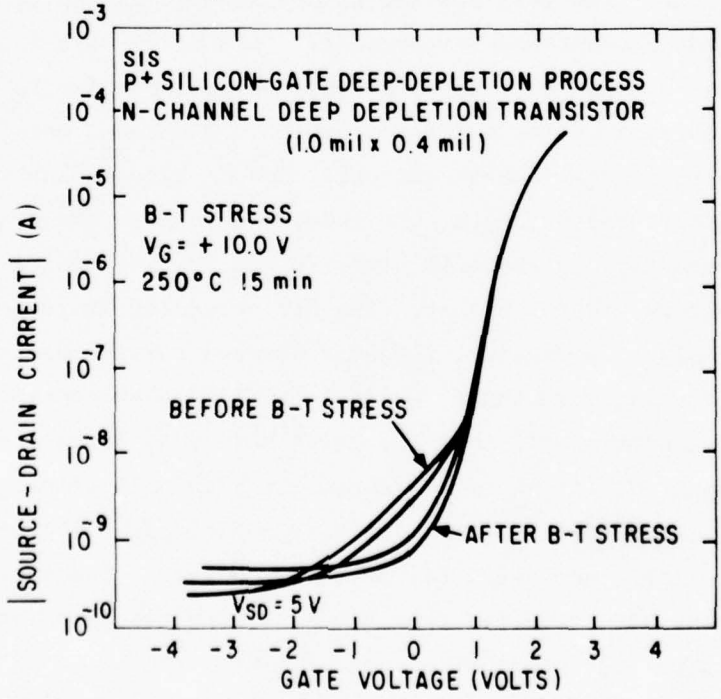


Figure 28. N-channel transistor shown in Fig. 27 before and after B-T stress.

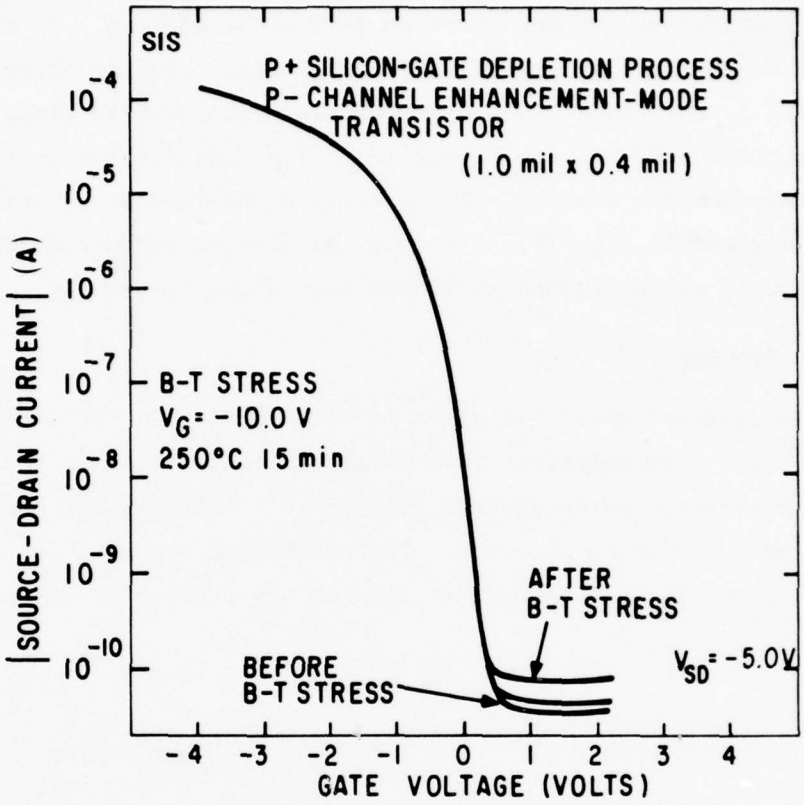


Figure 29. P-channel transistor shown in Fig. 27 before and after B-T stress.

In a continuing effort to evaluate this technology, a small integrated circuit (7-stage counter) was fabricated with SIS. SIS wafers were processed together with control wafers. At wafer probe, the SIS wafers showed slightly higher yields than the control wafers. While fabricating these IC's, the main problem with this planar technology became obvious: the areas being milled increase in size. This results from the fact that readily available masking materials mill at about three times the rate of the sapphire substrate. Therefore, to mill a 0.6-μm-deep hole, the masking material must be at least 2.0 μm thick. With the mask this thick, it becomes very difficult to define 0.1-mil lines. Evaporated aluminum, polysilicon, and epitaxial silicon were investigated as milling masks. None offered the desired dimensional control. Various photoresists were also investigated as possible milling masks. In

general, the photoresist did not stand up during the milling. To mill the 0.6-μm-deep holes holes required milling for 90 minutes using argon atoms with an accelerating potential of 750 V. The photoresists usually broke down (cracked) after about 30 minutes of milling. Not only did the holes increase in surface area, but the sides of the holes were inclined at a very shallow angle, as is obvious in Fig. 26. A simple calculation indicated that the angle is 9 degrees which is much shallower than shown in Fig. 24.

2. Gas-Phase Etching

Since the devices fabricated using ion-milled SIS had desirable characteristics and were only deficient in dimensional control, other techniques for creating the holes were investigated. Gas-phase etching of the holes with SF_6 was found to be a promising approach. The processing sequence for this approach is shown in Fig. 30. The first step in the process is to define the

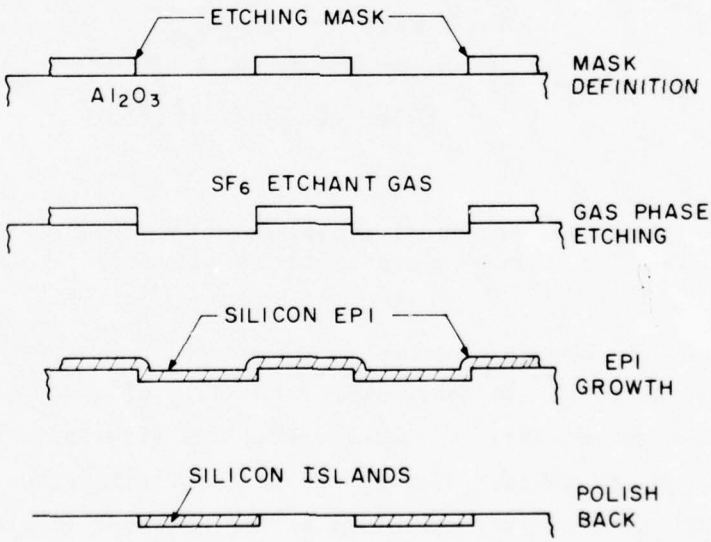


Figure 30. Processing sequence for SIS using gas-phase etching.

etchant mask. Several masking materials were investigated, and the results are presented later in this report. After mask definition, the wafers are etched with SF_6. After etching, the remaining masking material is removed. The wafers are fired in H_2 at 1200°C, and the silicon epitaxial film is grown

in the standard way. The silicon that is not in the holes is polished away leaving a planar surface. The wafers are then processed using the p+ polysilicon gate deep-depletion process [1,2].

Although the steps are very similar to those in Fig. 23 for ion milling, considerably more work needed to be done. The technology for etching patterns in sapphire substrates did not exist. Therefore, it was necessary to determine the optimum etching mask, and etching parameters, and the characteristics of devices fabricated in SF_6 etched wafers. Manasevit [9] proposed the use of SF_6 to remove work damage in sapphire substrates. To accomplish this, large removal rates (μm/min) were required. In our work slower removal rates (μm/h) are needed; therefore, Manasevit's results were of limited usefulness. A paper concerning selective etching of bulk silicon with SF_6 came to our attention only recently [10]. The problems of dimensional control with SiO_2 masking discussed in this paper were similar to those that we encountered. Therefore, the available information in the literature was very limited.

The first step in the SIS process is to define the SF_6 etchant mask. SiO_2, Si_3N_4, and combinations of the two have been used; and these materials are defined using standard photolithographic techniques and etchants. Following mask definition, the etching of the sapphire substrates is done in a rf-heated, air-cooled, horizontal reactor. The cross section of the rectangular reactor tube is 5 cm x 10 cm. The rf coils are wrapped around the glass reactor tube with sufficient spacing to allow sighting of the susceptor with an optical pyrometer. The susceptor coated with SiC is rectilinear 7.5 cm x 30 cm x 1.25 cm. After considerable experimentation it was found that the most uniform etch rates across a 1-1/2-in.-diameter wafer could be achieved by placing the wafer in a 12-mil-deep recess in the susceptor. The diameter of the recess is slightly larger than the wafer diameter. Sapphire 1-1/2-in.-diameter wafers are typically 13 to 14 mils thick. Following these observations, susceptors with 5 equally spaced, centered recesses were used.

9. H. M. Manasevit and F. L. Monitz, J. Electrochem. Soc. 114, 2041 (1967).
10. L. J. Stinson, J. A. Howard, and R. C. Neville, J. Electrochem. Soc. 123, 551 (1976).

The carrier gas for the etchant is palladium-diffused H_2. The etchant gas is 10% SF_6 99.995% in H_2 99.999%. The steps in the etching cycle are: load wafers, flush with N_2, N_2 off, H_2 on, heat to etch temperature measured by optical pyrometer, turn on etchant gas for pre-specified time, allow to cool with H_2 on, flush with N_2, unload wafers. Carrier gas flow rates of 10 to 50 liters/min with SF_6 concentrations of from 0.5 to 4 mole percent are used. These concentrations were arrived at empirically from numerous etching experiments. The data show that if the etching is not done properly, the etched sapphire areas are pitted and rough. The one factor which influences the amount of pitting or surface roughness is the etch rate. Too high an etch rate yields pitting and roughness; too slow an etch rate makes the process impractical. The etch rate is observed to be directly related to temperature as shown in Fig. 31 where the susceptor temperature is plotted on the abscissa and

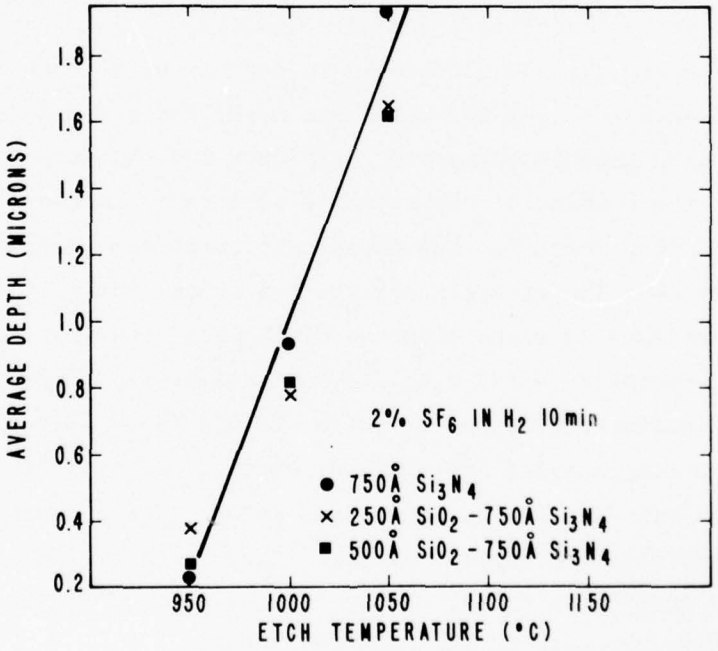


Figure 31. SF_6 etching of $\{1\bar{1}02\}$ sapphire at various temperatures.

the average depth of the etched holes is plotted on the ordinate. The data clearly show that the etch rate is a strong function of the etching temperature. The holes etched for 10 min at 1050°C were pitted and/or rough, whereas the

ones etched for 10 min at 950°C and 1000°C were not. The various points at each temperature were obtained using different masking techniques, which will be discussed later.

The depth of the etched holes is measured using a talysurf instrument. The average hole depth for a wafer is determined by averaging the depth of the pattern at 6 points, 4 points equally spaced around the perimeter of the wafer and 2 near the center. In measuring the hole depth, care is needed because the hole cross section is not a simple trapezoid as shown in Fig. 24 for ion-milled holes. A depth profile for SF_6 etched holes is shown in Fig. 32. The vertical scale is 0.1 μm/division, or 2.5 μm full scale, and the horizontal scale is 50 μm/division. The trace in Fig. 32 shows several interesting features of SF_6 etched holes. First, the contour of the bottom of the hole is dependent on the size of the hole. The small holes (approximately 1 mil wide) have a relatively flat bottom; the larger holes (approximately 6 mils wide) have a convex bottom. This has resulted from faster etching at the side walls than in the center of the hole. The depth of the holes is also a function of the size of the hole. The smaller holes are about 0.65 μm deep whereas the larger holes are about 0.55 μm deep at the side walls and about 0.45 μm deep at the center of the hole. All holes etched with SF_6 show these features.

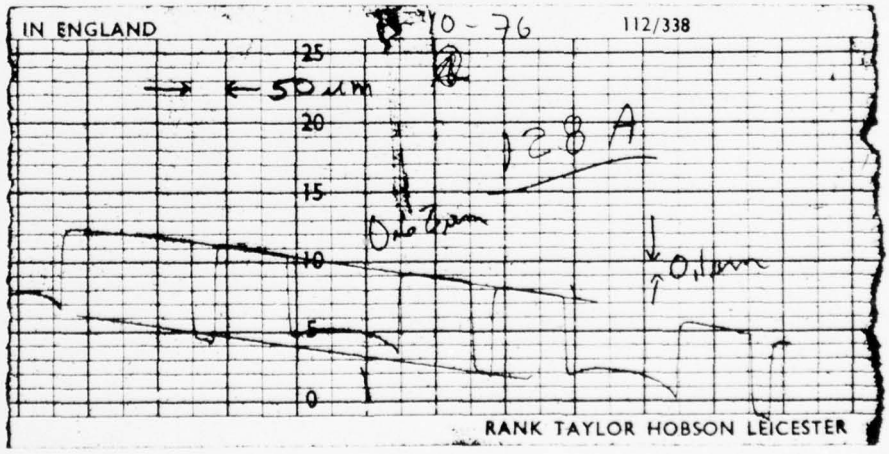


Figure 32. Profile of SF_6 etched holes.

The etch rate is also observed to be directly related to the amount of SF_6 in the carrier gas as shown in Fig. 33. The mole percentage of SF_6 in the

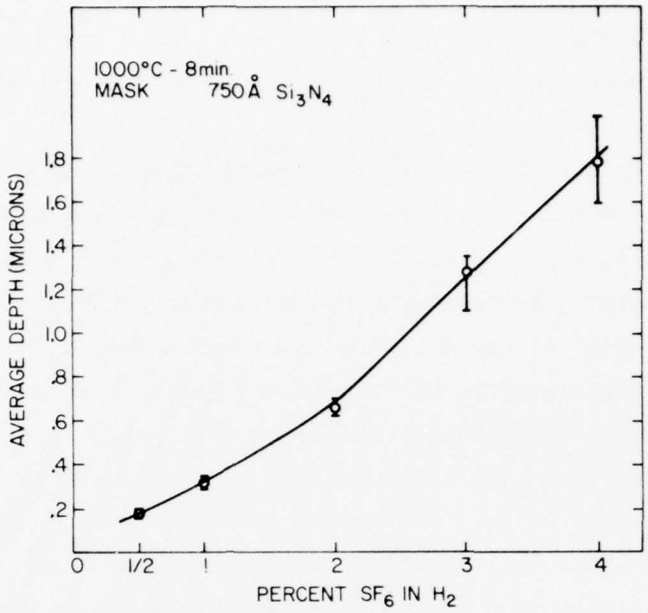


Figure 33. SF_6 etching of $\{1\bar{1}02\}$ sapphire at various concentrations in H_2 carrier gas.

carrier gas is plotted on the abscissa and the average hole depth is plotted on the ordinate. The etching was done at 1000°C for 8 minutes with 750 Å of Si_3N_4 as the mask. The open circle gives the average hole depth, and the vertical bar gives the range in hole depth across the wafer. Increasing the SF_6 concentration by about a factor of 10 increases the etch rate by about a factor of 10. Based on these data and other experimental results, standard etching conditions were established to be 2% SF_6 in H_2 with a total gas flow of 18.9 liters/min at a pyrometer reading of 1000°C. Of course, a different experimental setup may require adjustment of these parameters. Also, it is quite possible that the etching could be done at a lower temperature with increased SF_6 concentration or at a higher temperature with reduced SF_6 concentration.

Although all of the wafers in which devices were made were etched one at a time, a preliminary investigation into the possibility of etching more than one wafer was undertaken. The results indicated that two and possibly three wafers could be etched simultaneously if the wafers were placed at the end of the etchant block near the gas exit port. The etch rate across wafer placed near the gas entrance port was very nonuniform. Since the gas enters the

reactor at room temperature and must be heated to the etching temperature by the block, the nonuniformity probably resulted from a nonuniformity in etchant gas temperature. Preheating the gas would probably increase the number of wafers which could be etched at one time. Although only 1-1/2-in.-diameter wafers were used for all of the work reported, a preliminary study of the etching characteristics of 2-in.-diameter wafers was undertaken. The results suggest that the etching parameters of the 2-in. wafers are almost identical to those of the 1-1/2-in. wafers.

In conjunction with the optimization of etching parameters, a study of various SF_6 etch masks was undertaken. The important considerations in optimizing the etchant mask are: availability, compatibility with standard photolithographic techniques, and inertness in the etching environment to provide good dimensional control of small geometries. One of the most readily available masking materials is deposited SiO_2 which was studied first. The SiO_2 is deposited by the reaction of SiH_4 and O_2 at about 300°C. After some preliminary work it was found that 7000 Å of deposited SiO_2 allowed etching 0.6-μm-deep holes. Figure 34 shows the average depth of etched holes versus

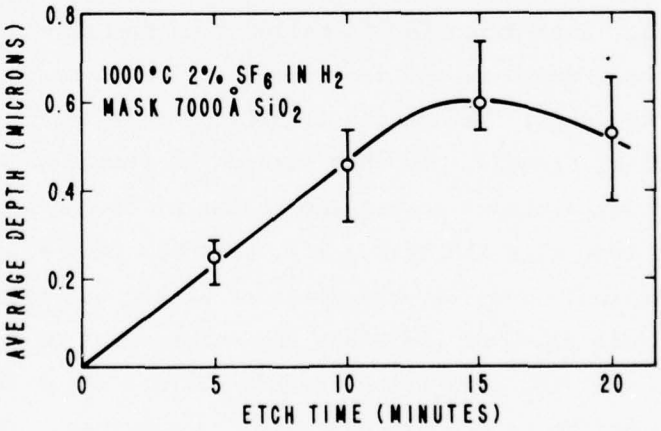
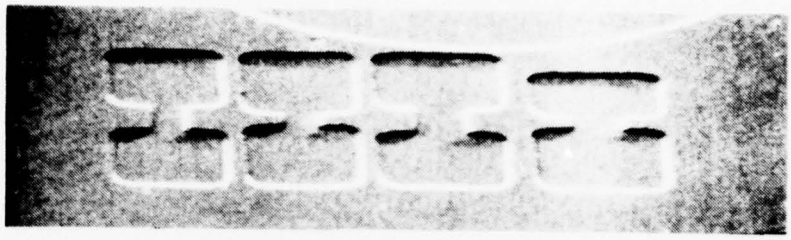


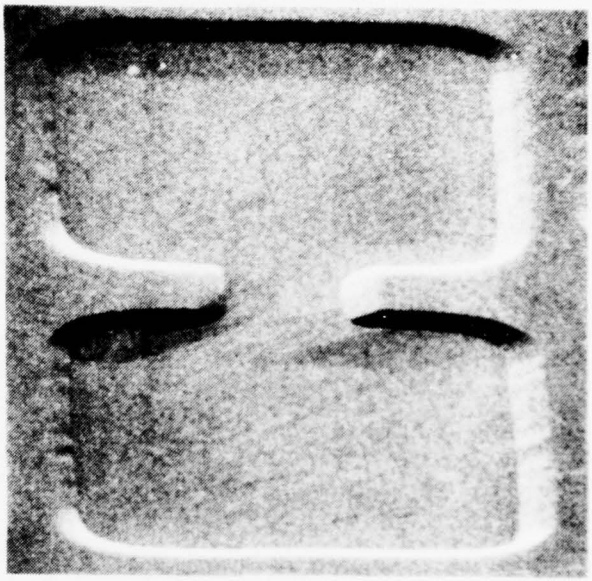
Figure 34. SF_6 etching using SiO_2 mask for various times.

etch time using 7000-Å SiO_2 as the mask. The etching was done at 1000°C pyrometer with 2% SF_6. The open circle gives the average hole depth and the vertical bar shows the range of hole depth across the wafer. The range in

etch depth is worse-case since four of the measurements were taken within 1/8 in. of the wafer periphery. Also, no effort was made to measure the depth of holes of equal surface area. Since holes of different surface area etch at different rates as shown in Fig. 32, some of the variation across a wafer probably results from this phenomenon. Therefore, the worse-case hole depth variation across a wafer is ±0.1 μm. The data in Fig. 34 show that the etch rate is linear with time for about the first 15 minutes. For times longer than 15 minutes the hole depth actually decreases. This decrease is probably caused by the SiO_2 mask being consumed and the top surface of the wafer which was protected by the SiO_2 etching faster than the areas where the holes were etched. SEM photographs of patterns etched in sapphire substrates using SiO_2 masking are shown in Fig. 35. These same patterns fabricated using ion milling are shown in Fig. 26. The enlarged areas at the top and bottom of the dumbbell are the source and drain contacts, and, after fabrication, the polysilicon gate bisects the transistors in the narrow region. These particular test transistors were chosen because they are the smallest devices on this test pattern, and, therefore, the degree of dimensional control achieved with the various masking techniques can be easily determined. The photomask dimensions for the two transistors to the left in Fig. 35(a) (500X) are 0.28 mil and for the two to the right, 0.47 mil. This dimension is called the channel width and when multiplied by the hole depth is the cross-sectional area through which current flows from source to drain. The second transistor from the left in Fig. 35(a) is shown in Fig. 35(b) (2000X). In this figure the sloped sides of the hole are very obvious. The distance across the bottom of the hole in the narrow region as measured from this SEM is 0.3 mil, which is only slightly larger than the mask dimension. However, the distance across the top of the hole is 0.52 mil. The gradual slope of the sides and enlargement of the etch pattern have resulted from the SiO_2 mask being etched. Figure 35(c) (2000X) shows what happens if etched holes are placed too close together. The photomask spacing between these holes is 0.24 mil. As shown in the SEM, because of the gradual slope of the side wall, the holes are no longer separated. The average depth of these holes was measured to be 0.4 μm. Had they been etched deeper to about 0.6 μm, in all probability the pattern enlargement would have been even greater. Therefore, we must conclude that SiO_2 does not provide sufficient dimensional control for etching patterns in sapphire substrates with SF_6.



(a)



(b)

(c)

Figure 35. (a) Holes etched in sapphire substrate using SiO_2 mask (500X). (b) Hole for small transistor etched in sapphire substrate using SiO_2 mask (2000X). (c) Interference between holes etched using SiO_2 mask (2000X).

Despite these problems with dimensional control, test transistors were fabricated in these wafers. After the silcon was polished back, n-channel deep-depletion and p-channel enhancement mode devices were fabricated using the p+ polysilicon gate deep-depletion process [2]. Transfer characteristics of these test transistors are shown in Fig. 36. These curves are very similar

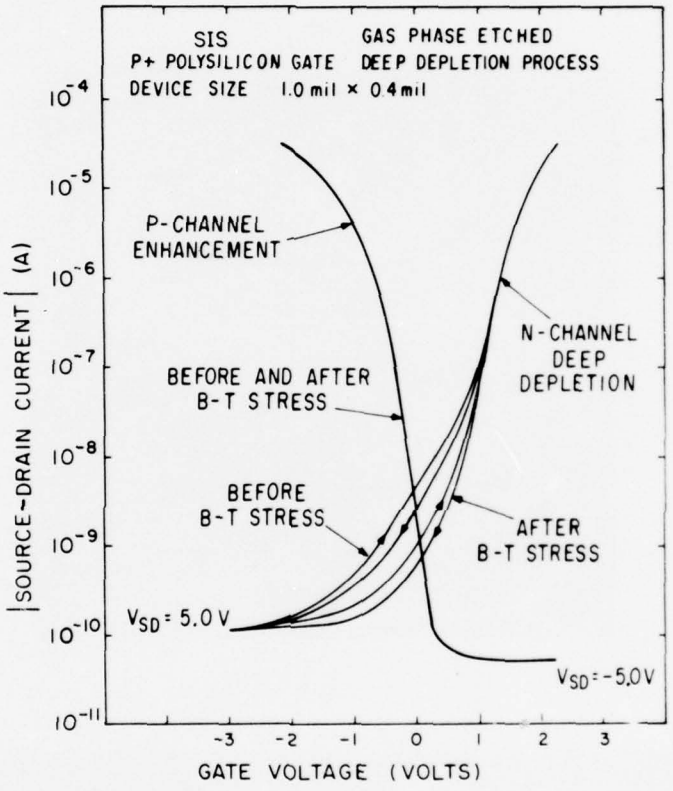


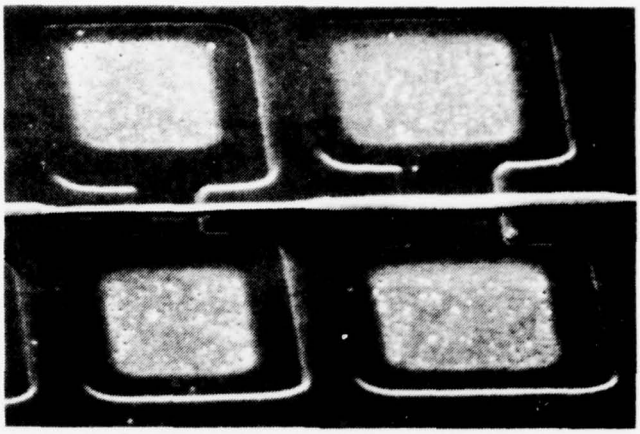
Figure 36. Transfer characteristics of an n-channel deep-depletion transistor and a p-channel enhancement-mode transistor fabricated using gas-phase etching with SiO_2 masking.

to those shown in Figs. 27, 28, and 29. This is not unreasonable since the only difference between the two processes is the manner in which the holes in the substrate were created. The transconductance of the transistors is equivalent to state-of-the-art devices as long as the hole depth is very close to 0.6 μm. Devices fabricated in shallower holes exhibited lower transconductance. The n-channel deep-depletion transistor has a small amount of excess edge leakage current just like the n-channel devices fabricated in ion-milled holes.

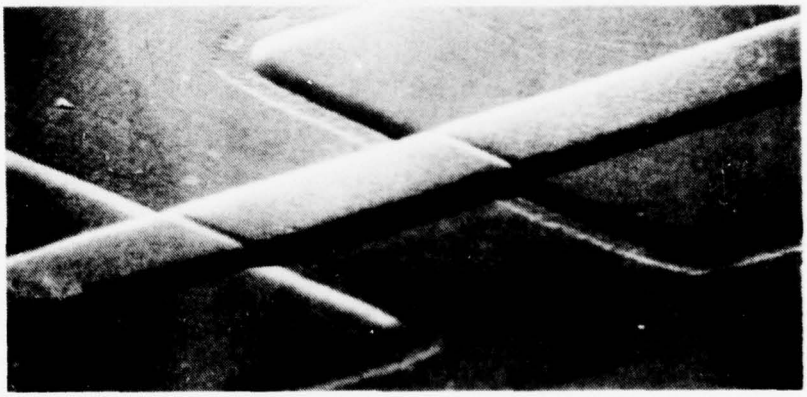
Although this excess edge leakage is undesirable, it is not of sufficient magnitude to prevent circuit operation. Moreover, state-of-the-art processed n-channel devices frequently exhibit excess edge leakage of the same magnitude. The data in Fig. 36 also show that both the n-channel deep-depletion and p-channel enhancement-mode devices are B-T stable. The bias-temperature stressing was done at 250°C for 10 minutes with positive voltage on the n-channel gate and negative voltage on the p-channel gate. These results are again in agreement with those reported for devices fabricated in milled holes. It should be added that of literally hundreds of SIS devices tested, not one has been observed to be B-T unstable.

Figure 37 shows SEM photographs of fabricated transistors with the aluminum and doped oxides removed. Figure 37(a) shows the test devices at 1000X. The dumbbell-shaped region contains the silicon epi and is recessed relative to the surrounding sapphire. This has resulted from oxidation of the silicon and subsequent oxide removal. Figure 37(b) shows the transistor on the right in Fig. 37(a) at 5000X. The silicon epi is the recessed region with the polysilicon gate crossing it. Note the different texture of the epi around the periphery of the etched hole. This may indicate that the silicon around the edge is polycrystalline rather than single-crystal (100) silicon. The pitting in the source and drain contacts is caused by alloying the aluminum metallization. The light strip running across the picture from left to right is the p+ polysilicon gate. Figure 37(c) is an enlargement (20,000X) of the device in Fig. 37(b). The polysilicon gate is directly on top of the sapphire on the right side of the photograph. On the left side of the photograph, the polysilicon is above the recessed epi silicon but separated from it by the channel oxide which is shown undercut. The undercutting resulted from the removal of the doped oxides. The photograph clearly shows the almost perfect planarity which has been achieved. The polysilicon encounters an infinitesimal step in traversing the silicon region.

In hopes of achieving more dimensional control, we used Si_3N_4 as an etchant mask. The Si_3N_4 was deposited from the reaction of NH_3 with SiH_4 at 800°C. After some preliminary work, it was found that 750 Å of Si_3N_4 allowed etching of 0.6-μm-deep holes. The Si_3N_4 was defined with phosphoric acid at 180°C by a deposited SiO_2 film which was defined using standard photolithographic techniques. Figure 38 shows the average depth and variation in



(a)



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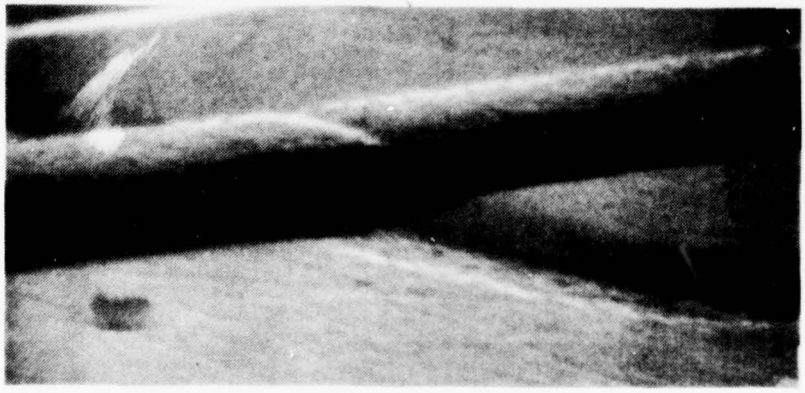


(c)

Figure 37. (a) Small, SiO_2 masked, gas-phase etched SIS/MOS transistors (1000X). (b) Polysilicon gate crossing silicon epitaxial region on SiO_2 masked SIS device (20,000X).

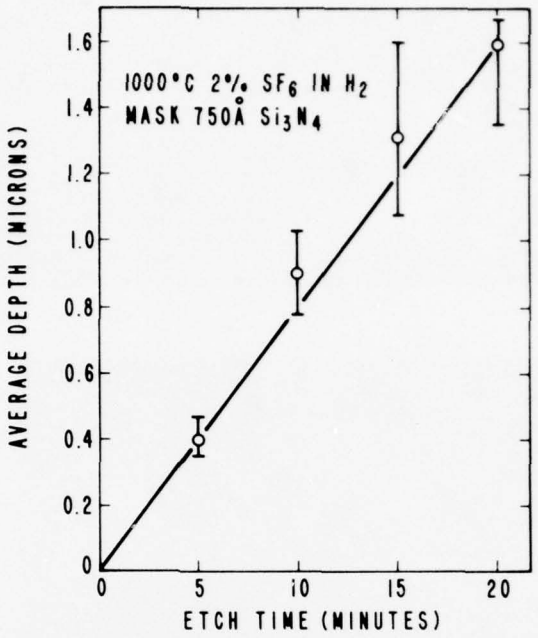
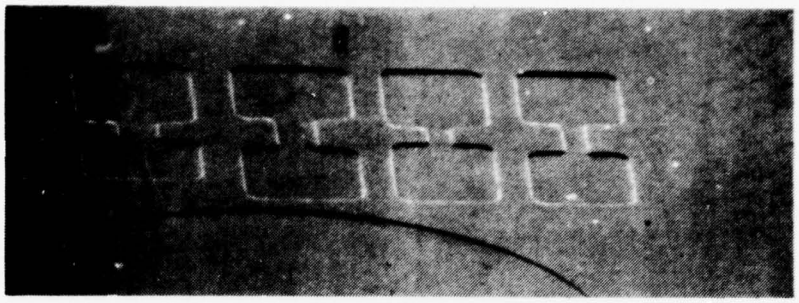
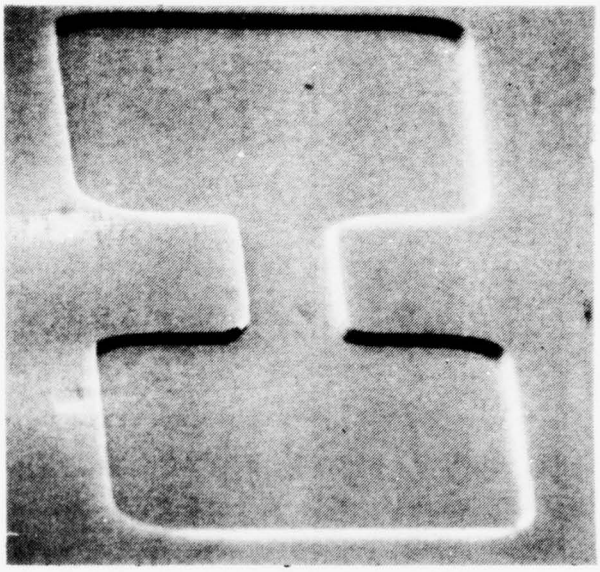


Figure 38. SF_6 etching using Si_3N_4 mask for various times.

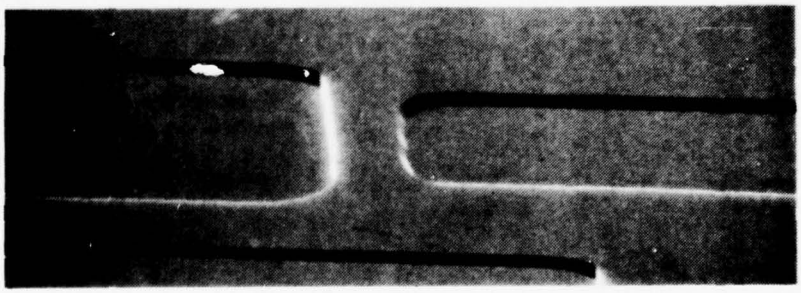
depth across a 1-1/2-in.-diameter wafer versus etch time using 750 Å of Si_3N_4 as the mask. The etching was done with 2% SF_6 in H_2 at 1000°C. Unlike the data in Fig. 34 for the SiO_2 mask, the etch rate is linear with time to 20 minutes indicating that the 750 Å of Si_3N_4 has not been consumed. In addition, the etch rate is faster with Si_3N_4 masking than with the SiO_2 masking, all other conditions being identical. This probably results from the fact that the etchant gas is not depleted by the reaction with the SiO_2, and, therefore, more etchant is available to react with the Al_2O_3. SEM photographs in Fig. 39 also indicate that the Si_3N_4 is considerably more inert in the etching environment. These photographs are of the same devices shown in Fig. 35; however, the photograph was taken from a direction rotated 180° from that in Fig. 35. The photomask dimension for the two transistors to the left in Fig. 39(a) (500X) is 0.47 mil and for the two transistors to the right is 0.28 mil. The transistor on the far right in Fig. 39(a) is shown in Fig. 39(b) at 2000X. The sides of the etched hole are very steep, almost vertical. This has resulted from the inertness of the Si_3N_4 masking layer. This photograph should be compared with Fig. 35(b). The channel width is measured to be 0.27 mil, which is essentially identical to the mask dimension. Only one measurement of the channel width is



(a)



(b)



(c)

Figure 39. (a) Holes etched in sapphire substrate using Si_3N_4 mask (500X). (b) Hole for small transistor etched in sapphire substrate using Si_3N_4 mask (2000X). (c) Interference between holes etched using Si_3N_4 mask (2000X).

possible because of the steepness of the side walls. The measured dimension is slightly smaller than the mask dimension, probably because the photograph was taken at a slight angle. Figure 40(c) (2000X) shows the two etched holes shown in Fig. 35(c). Because of the steepness of the sidewalls, the two holes are separated by 0.19 mil as compared with a photomask dimension of 0.24 mil. The average depth of the holes in Fig. 39 is 0.8 μm compared with 0.4 μm for the holes in Fig. 35. Because the Si_3N_4 is only very slowly etched by the SF_6 in H_2, not only can a thinner masking layer be used, but also the dimensional control of the etched pattern is significantly improved to the point that closely spaced, small geometries can be etched.

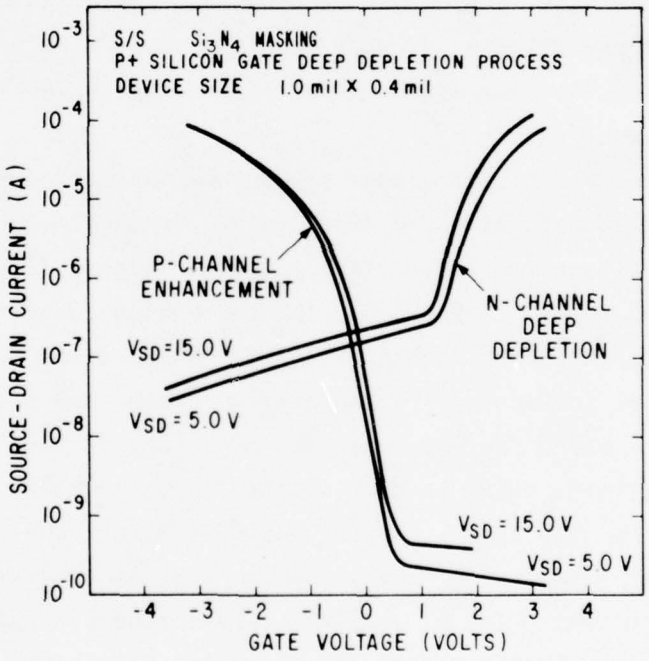


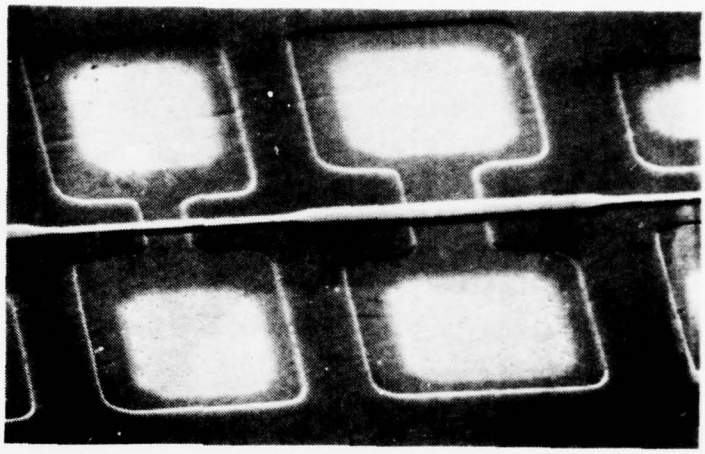
Figure 40. Transfer characteristics of an n-channel deep-depletion transistor and a p-channel enhancement-mode transistor fabricated using gas-phase etching with Si_3N_4 masking.

Test transistors were fabricated in these wafers etched with a Si_3N_4 mask. The transfer characteristics of the n-channel deep-depletion and p-channel enhancement devices are shown in Fig. 40 for source-drain voltages of

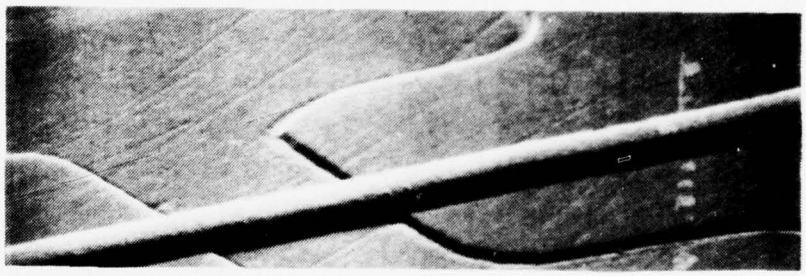
5 and 15 V. The p-channel device has low leakage current; however, the n-channel deep-depletion transistor has leakage current several orders of magnitude above normal. Edgeless devices on the same wafer do not exhibit this high leakage, and, therefore, the leakage probably occurs between source and drain along the side wall of the hole. In numerous experiments designed to verify these results the leakage current was always observed to be significantly higher than in standard processed devices. Enhancement mode n-channel devices fabricated in Si_3N_4 masked wafers also exhibited high edge leakage current. It was thought that the phosphoric acid used to etch the Si_3N_4 might be causing the leakage problem. However, devices fabricated in wafers wherein the Si_3N_4 was plasma etched also showed high edge leakage. Also, SiO_2 was left on top of the Si_3N_4 during SF_6 etching, but again the devices showed high leakage. From these results one must conclude that Si_3N_4 masking, although it provides almost perfect dimensional control, causes the n-channel devices to have high edge leakage current.

Figure 41 shows SEM photographs of devices fabricated in Si_3N_4 masked wafers with the metallization and doped oxides removed. The photographs are of the same pattern shown in the previous figures. Figure 41(a) (1000X) shows the alloyed source and drain contacts and the polysilicon gate. The device on the left in Fig. 41(a) is shown in Fig. 41(b) (5000X). It is worth noting that the width of the rough textured epitaxial silicon around the perimeter of the hole is much smaller. Since the sidewalls are much steeper with Si_3N_4 masking, the width of the inclined region is much smaller. Figure 41(c) is an enlargement (20,000X) of the device in Fig. 41(b). In this figure the polysilicon gate is shown crossing from the top of the sapphire, the raised area on the right, to the top of the channel oxide on the left. Again the channel oxide is undercut and separates the polysilicon from the epitaxial silicon in the hole. In this photograph the polysilicon encounters no step in crossing from one region to the other.

Since SiO_2 masking yielded good devices but poor dimensional control and Si_3N_4 masking yielded good dimensional control but poor devices, a combination of the two was studied. This mask consists of a thin layer of SiO_2 between the sapphire and Si_3N_4. Initially the interposed SiO_2 layer was 1000 Å thick. However, improved dimensional control was achieved by thinning this layer to 250 Å of deposited oxide. The etch depth versus time for a composite mask



(a)



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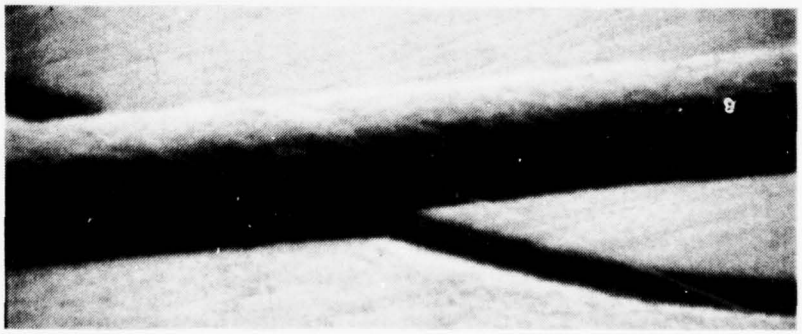


(c)

Figure 41. (a) Small, Si_3N_4 masked, gas-phase etched SIS/MOS transistors (1000X). (b) Polysilicon gate crossing silicon epitaxial region on Si_3N_4 masked SIS device (5000X). (c) Polysilicon gate crossing silicon epitaxial region on Si_3N_4 masked SIS device (20000X).

consisting of 250-Å SiO_2, 750-Å Si_3N_4, and 3000-Å SiO_2 is shown in Fig. 42. The data show the etch rate to be linear with time, but slightly slower than the etch rate for a Si_3N_4 mask. The slower etch rate probably results from the presence of the SiO_2 which depletes the etchant gas. The depth variation across the wafer is about ±0.1 μm. A comparison of the etch depth versus time for the three masking techniques is shown in Fig. 43. The data show the etch rate fastest with the Si_3N_4 mask, slowest with the SiO_2, and between these two extremes for the two composite masks.

SEM photographs of patterns etched with the composite 250-Å SiO_2, 750-Å Si_3N_4, and 3000-Å SiO_2 mask are shown in Fig. 44. These patterns can be compared with those in Figs. 35 and 39 for SiO_2 and Si_3N_4 masking, respectively. The photomask dimensions for the two transistors to the left in Fig. 44(a) (500X) are 0.47 mil and for the two to the right, 0.28 mil. The second transistor from the right in Fig. 44(a) is shown in Fig. 44(b) (2000X). The photograph clearly shows that the side walls of the hole are sloped like those obtained with an SiO_2 mask. This has resulted from the thin SiO_2 which is under the Si_3N_4 being etched laterally as the hole is etched. The distance across the bottom of the hole is 0.34 mil which is close to the mask dimension of 0.28 mil. The distance across the hole at the top is difficult to measure because of the gradual slope of the sides. However, it is probably no greater than 0.63 mil. These results are slightly worse than those obtained with SiO_2 masking. However, this composite mask actually does improve dimensional control because the holes in Fig. 44 are 0.8 μm deep which is twice as deep as the holes shown in Fig. 35. Figure 44(c) (2000X) shows the two holes located 0.24 mil apart interfering with each other following etching.

Data taken comparing various masking techniques can become very confusing unless the interrelationship between hole depth and dimensional control is clearly understood. Since the Si_3N_4 mask is relatively inert in the etching environment, holes as deep as 1.0 μm can be etched with only a small loss in dimensional control. When SiO_2 is used either as the mask or as part of a composite, the situation is different. The SiO_2 etches rapidly in the etching environment both vertically and horizontally. As a result the holes have sloping sides and become larger as etching proceeds. The longer the etch time, the greater the pattern enlargement. Therefore, the SiO_2 mask and composite

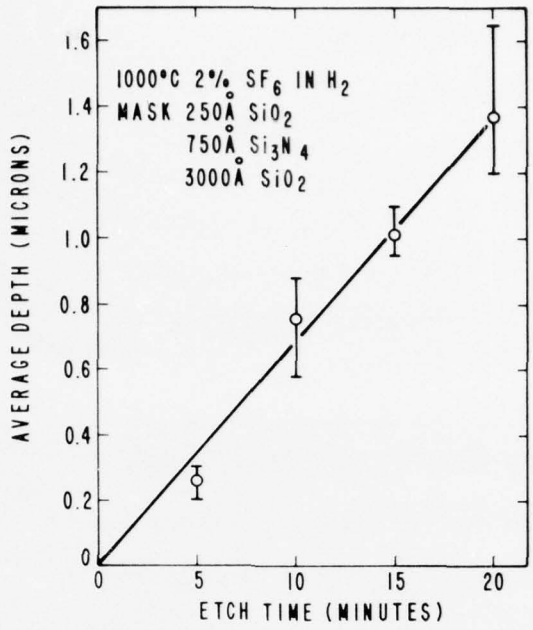


Figure 42. SF_6 etching using composite SiO_2-Si_3N_4-SiO_2 mask for various times.

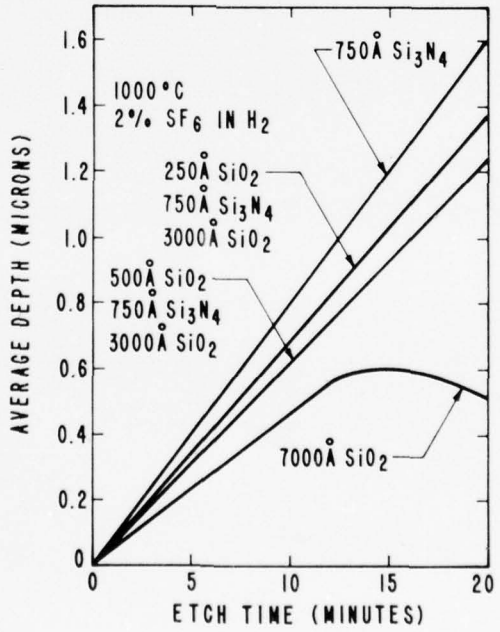
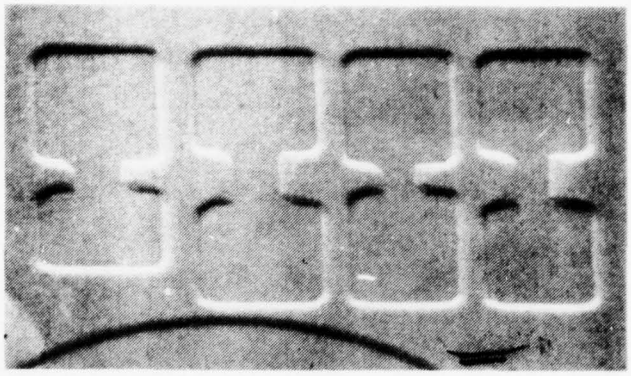
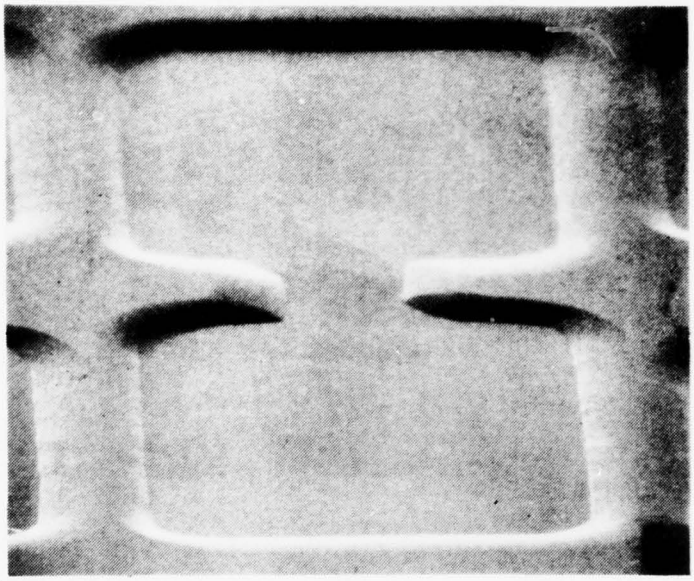


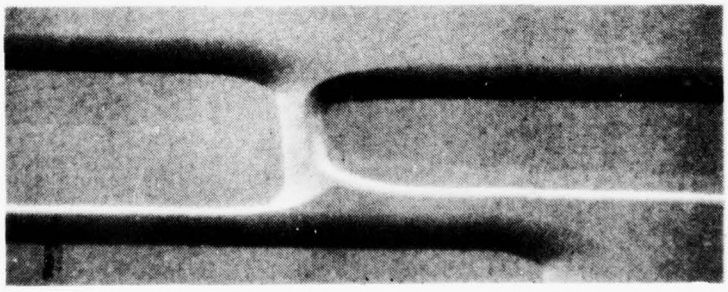
Figure 43. SF_6 etching various masks for times up to 20 minutes.



(a)



(b)



(c)

Figure 44. (a) Holes etched in sapphire substrate using composite SiO_2-Si_3N_4-SiO_2 mask (500X). (b) Hole for small transistor etched in sapphire substrate using composite mask (2000X). (c) Interference between holes etched using composite mask (2000X).

masks can only be compared as to the dimensional control they offer by comparing holes of approximately the same depth. The dimensional control can be quantified by the dimensional control factor (DCF) which is defined as:

$$DCF = \frac{\text{actual dimension}}{\text{photomask dimension}} \times \frac{0.6\ \mu m}{\text{actual depth } (\mu m)}$$

Using the DCF a study of the various masks was done. The data are shown in Table 1. All the wafers were etched at 1000°C 2% SF_6 in H_2. Etch times were

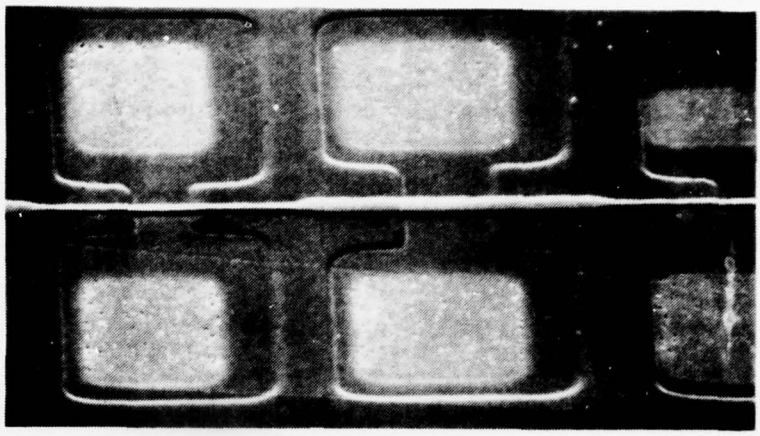
TABLE 1. DIMENSIONAL CONTROL FACTOR (DCF) FOR VARIOUS MASKS

Mask	DCF 0.28-mil Photomask	DCF 0.46-mil Photomask
7000-Å SiO_2	2.15	1.90
1000-Å SiO_2, 500-Å Si_3N_4, 3000-Å SiO_2	2.00	1.68
500-Å SiO_2, 500-Å Si_3N_4, 3000-Å SiO_2	1.97	1.57
250-Å SiO_2, 500-Å Si_3N_4, 3000-Å SiO_2	1.37	1.21
500-Å Si_3N_4	1.28	1.28

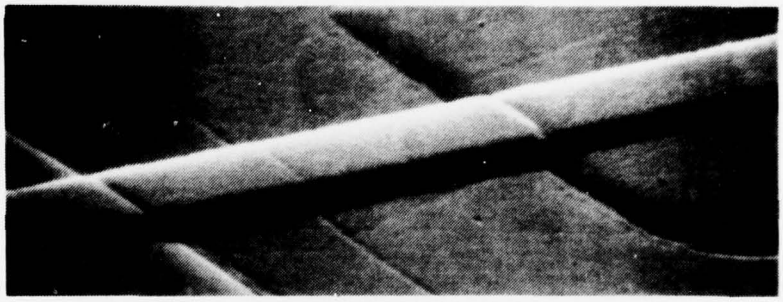
adjusted to achieve almost equal hole depth. The measurements were taken using a filar eyepiece on a standard optical microscope. The DCF gives an indication of how much a surface dimension has increased for a given etch depth. A DCF of 1.00 indicates perfect dimensional control; whereas a DCF>1 indicates the amount of enlargement. The data show that an SiO_2 mask has the highest DCF and an Si_3N_4 mask the smallest. The DCF for the silicon nitride mask is somewhat misleading since holes 1.0 μm deep with almost no loss of dimensional control have been etched. The data from the composite masks indicate that for thick (>1000 Å) SiO_2 layers the DCF approaches that for SiO_2 masks, and for thin (<250 Å) SiO_2 layers the DCF approaches that for Si_3N_4 at an etch depth of 0.6 μm. So as far as dimensional control is concerned, the composite mask is a compromise between the SiO_2 and Si_3N_4 mask.

Test transistors were fabricated in wafers which were etched with an etchant mask consisting of 3000-Å SiO_2, 750-Å Si_3N_4 and either 1000-Å SiO_2, 500-Å SiO_2, or 250-Å SiO_2. In all cases the n-channel devices showed leakage current behavior similar to that shown in Fig. 36. In no case was the leakage current excessive as is observed when Si_3N_4 masking is used. In addition, none of the devices were observed to be B-T unstable under the test conditions discussed earlier. Therefore, the composite mask allows one to fabricate low leakage devices with only a small loss of dimensional control. It is worth noting that a small number of wafers were masked before etching with a composite consisting of a thin SiO_2 layer under the Si_2N_4 and no SiO_2 on top. The n-channel devices from these wafers exhibited high leakage current. These results suggest that the SiO_2 used initially to mask the silicon nitride is an important part of the composite mask.

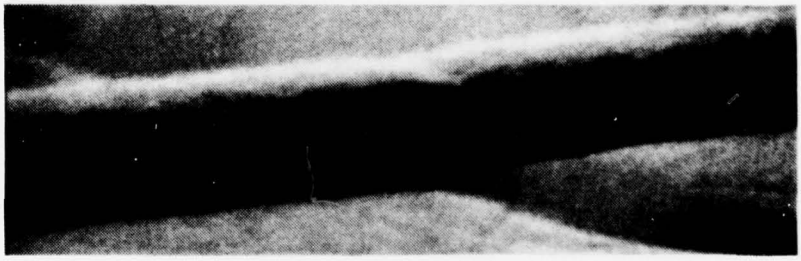
SEM photographs in Fig. 45 show fabricated transistors with the doped oxides and aluminum removed. The holes for these devices were etched using a composite 500-Å SiO_2, 750-Å Si_3N_4, and 3000-Å SiO_2. Figure 45(a) (1000X) shows the two small dumbbell-shaped transistors shown in Figs. 37 and 41. The device on the right in Fig. 45(a) is shown enlarged in Fig. 45(b) at 5000X. The band of material crossing the photograph from left to right is the polysilicon gate. Note the rough textured epitaxial silicon around the perimeter of the hole. The polysilicon encounters almost no step in crossing from the sapphire to the channel oxide. Figure 45(c) shows the polysilicon-channel oxide, epitaxial silicon-sapphire interface at 20,000X. It is interesting to compare the structure of this four-way interface in Figs. 45(c), 41(c), and 37(c) for the different masking techniques. The composite mask and the SiO_2 mask both result in holes with sloped sides while the Si_3N_4 mask causes the holes to have almost vertical sides.



(a)



(b)



(c)

Figure 45. (a) Small, composite SiO_2-Si_3N_4-SiO_2 masked, gas-phase etched SIS/MOS transistors (1000X). (b) Polysilicon gate crossing silicon epitaxial region on composite masked SIS device (5000X). (c) Polysilicon gate crossing silicon epitaxial region on composite masked SIS device (20,000X).

Section IV
DISCUSSION

The experimental data presented in the preceding section give considerable insight into the cause of the edge instabilities of the n-channel transistors isolated by thermal oxidation. The bias-temperature data suggest that the n-channel edge instability is caused by some impurity which behaves somewhat like a sodium ion. However, it must be kept in mind that this ion affects only the oxide on the island edge because edgeless transistors are not B-T unstable even though they have seen the same processing steps as the edge transistors. The data presented in Figs. 16 through 20 show that the polysilicon gate need only be separated from the sapphire by a few hundred angstroms to begin showing edge leakage current, hysteresis, and B-T instability. Therefore, it is proposed that during field oxidation impurities from the sapphire diffuse into the silicon at the bottom of the film and then are incorporated into the field oxide when the silicon is oxidized. If the unetched silicon is thicker, the oxidation requires longer time and more impurities can diffuse into the silicon before conversion of SiO_2. Then under positive B-T stress the field between the gate and the epi island disturbs the equilibrium distribution of the mobile impurity causing it to pile up at the oxide-silicon interface, thereby making the surface heavily n-type. Re-heating the device with no bias causes the impurity distribution to return to equilibrium. This model can be used to explain the dependence of the amount of edge instability on the field oxide thickness. The devices wherein the entire silicon film has been oxidized probably exhibit no B-T instability because the electric field between gate and epi island is concentrated in the part of the field oxide which is most removed from the sapphire interface. In all probability the impurity is concentrated in the field oxide near the SiO_2-Al_2O_3 interface.

At this time we can only speculate as to the impurity, but it is not improbable that it may be aluminum or an aluminum compound or complex. It is well recognized that prolonged high-temperature heat treatment of an SOS film increases the aluminum autodoping from the substrate. Recently, Cullen,

Corboy, and Smith [11] have presented SIMS (Secondary Ion Mass Spectrometry) data showing aluminum in the interfacial region between silicon and sapphire. Thus, there is some evidence to support the hypothesis that the mobile impurity contains aluminum. It is also possible that the mobile impurity is sodium. Recent experiments indicate that just because it is possible to grow 1000 Å of sufficiently clean SiO_2 does not necessarily imply that 5000 Å of sufficiently clean SiO_2 can be grown. For SOS/MOS transistors isolated with thermal oxide, the gate electrode extends out over the field oxide at least several tenths of a mil. Therefore, during B-T stressing impurities can be swept by the electric field between the gate and silicon island from a large volume of oxide. If this oxide is not extremely clean, instabilities can result.

Data recently published by Goodman [12] provide some insight into the cause of the edge leakage current and hysteresis of n-channel devices. Goodman, using the high-voltage C-V technique wherein the sapphire substrate is the gate insulator, has identified interface states at the silicon-sapphire interface. The occupation of these states by either electrons or holes could have a large influence on the surface potential of the silicon at the very bottom of the edge. Therefore, these states could determine the amount of edge leakage current. The influence of the gate potential on the occupation statistics of these states could cause the observed hysteresis. Should this be the case, why do normally processed devices typically show no instability, small or no edge leakage, and little hysteresis? First, a normally processed device does not undergo field oxidation, and therefore the amount of impurities in the channel oxide at the $Si\text{-}SiO_2\text{-}Al_2O_3$ interface is small. Secondly, as can be seen in Figs. 2(b) and 16(a), the oxide thickness between the gate and the silicon epi is much thinner at the silicon-sapphire interface than at other places on the device. Ipri [13] has proposed that there is current flow between gate and epi island along this interface. If this is true, the $SiO_2\text{-}Al_2O_3$ interface states could respond quickly to charges in gate potential, and the lifetime of charges in these states would then be

11. G. W. Cullen, J. F. Corboy, and R. T. Smith, J. Crystal Growth 31, 274 (1975).
12. A. M. Goodman, IEEE Trans. Electron Devices ED-22, 63 (1975).
13. A. C. Ipri, IEEE SOS Technology Workshop, Lake Tahoe, California, 1975.

small. Certainly the concepts discussed here are plausible, but more experimentation is necessary to establish their validity.

The experimental results obtained using ion implantation to achieve isolation were far from encouraging. Faced with such un-promising results, what course should future work in this area take? Before attempting to answer this question, one observation made during this work should be emphasized. At the beginning of this work the proposed goal was to implant sufficient nitrogen or oxygen to make the silicon epi between the transistors semi-insulating. Obviously, implanting an oxygen atom for every 10 silicon atoms was not sufficient. But even more important is the observation that the film between the islands must be more than semi-insulating: it must indeed be a good insulator. This requirement results because in high-density large-scale integrated circuits, the area of the pellet between the transistors usually is doped with high concentrations of phosphorus or boron at the same time as the sources and drains are being doped. These areas must remain insulating even after being doped with more than $1 \times 10^{19}/cm^3$ n-type or p-type impurities. Only a true insulator offers this property.

Whether or not these truly insulating properties can be achieved using implantation is purely speculation at this time. In the present work, if all of the measured impurity were actually implanted in the film, the impurity atoms would be about 10% of the total atoms present in the film. Recently published data on oxygenated polysilicon (SIPOS) give some indication of percentage of oxygen needed to give insulating films [14]. As the oxygen concentration is increased from 0.0% to 50%, the resistivity increases from 10^6 to 10^{11} ohms/cm. This indicates that truly insulating properties can be achieved with doses of $10^{18}/cm^2$ in 0.6-μm-thick films. This dose is five times greater than those used in this work. Whether or not such microchemistry is possible is also pure speculation at this time. Recent work [15] in this area, however, suggests that implantation doses cannot be increased indefinitely because the host material begins to sputter away, removing some of the implanted ions at the same time. Therefore, the number of implanted ions saturates instead of continuing to increase. A dose of $10^{18}/cm^2$ may, therefore, not be achievable.

14. T. Aoki et al., Electrochemical Society, Spring Meeting 1975, Abstract #148.
15. J. H. Freeman, Technical Report #AERE-R 8147, Scientific Administration

Recently published data indicate that even such large doses do not result in sufficient isolation [16].

The only perplexing question concerning the SIS technology is the reason for the large n-channel edge leakage for holes masked with Si_3N_4. If the holes are ion milled or etched with SF_6 using SiO_2 or the composite mask, the n-channel devices have a small amount of edge leakage not unlike state-of-the-art devices. A study of the SEM photographs shows that the only obvious difference in the etched holes is the slope of the side walls. The devices which exhibit low leakage are fabricated in holes which have gradually sloping sides while the high edge leakage devices are fabricated in holes which have almost vertical sides. Until the fundamental cause of this apparent correlation is known, it is unlikely that the edge leakage of devices fabricated in Si_3N_4 masked holes can be reduced. In the meantime, however, the composite mask with a thin, first layer of SiO_2 offers reasonably good dimensional control if holes not much deeper than 0.6 μm are etched.

The electrical characterization of SIS/MOS transistors shows that the only device parameter that is a little degraded is the n-channel edge leakage current as shown in Figs. 27 and 36. Perhaps most important, however, is the fact that no problems with bias-temperature stability have been observed. This is clearly shown by the data in Figs. 28, 29, and 36. One interesting structural feature of the SIS device is clearly shown in Figs. 26(b), 26(c), 37(c), and 45(c). The channel oxide thickness is greatest at the sapphire interface. This is exactly opposite to what is observed on state-of-the-art processed devices as shown in Fig. 26. As a result, the epitaxial silicon not only has oxide above it, but the oxide tends to wrap around the silicon. Therefore, at the edge of the silicon island, the effect of Q_{ss} may be greater. This would lower the threshold voltage at the edge. This phenomenon could explain the early turn-on of the n-channel transistor. Additional experimentation is needed to validate this model.

The development of the selective gas-phase etching of sapphire with SF_6 offers some interesting possibilities for future SOS development. First, because of the planarity offered by SIS, more density-packed CMOS integrated

16. D. M. Jamba et al., Contract Report #N00014-75-C-0080, Naval Research Laboratory, Washington, D.C.

circuits should be achievable. An investigation of this is a natural extension of the present work. Barring some breakthrough in stabilizing the field oxide/silicon epi interface, SIS appears to be an attractive alternative to local oxidation. Secondly, with the ability to etch holes in sapphire substrates, a reexamination of the characteristics of SOS bipolar transistors seems warranted. The thicker epitaxial layers needed to achieve meaningful current amplification can now be recessed into the sapphire.

Section V
SUMMARY

Three techniques for achieving planarity in SOS/MOS integrated circuits are investigated. These approaches are thermal oxidation isolation, ion-implantation isolation, and SIS.

Experimental data indicate that acceptable p-channel enhancement-mode transistors can be fabricated using thermal oxidation isolation if the field oxide is grown at 900° to 950°C in HCl steam. On the other hand, both n-channel deep-depletion and enhancement-mode transistors frequently have large edge leakage currents and are bias-temperature unstable. These instabilities are clearly associated with the silicon island edge, since edgeless transistors do not exhibit these effects. A model based on the instabilities of the field oxide-sapphire-silicon interface is used to explain the observed phenomenon.

Considerable difficulty was encountered in obtaining large implantation doses of oxygen and nitrogen for implantation isolation. By reducing the implanted area, however, doses of 2×10^{17} atoms/cm^2 are achieved. In a 0.7-μm-thick film this translates to about one oxygen or nitrogen atom for every ten silicon atoms. With this dose, however, very little isolation between transistors is achieved. The prospects for obtaining better results with larger doses are discussed.

Experimental results show that devices with excellent electrical characteristics can be fabricated with the SIS technology. In terms of dimensional control and leakage current, the optimum devices are fabricated in holes in the sapphire substrate which have been etched with SF_6 using a composite etching mask consisting of SiO_2 and Si_3N_4. The only anamalous behavior is a small increase in n-channel edge leakage current. Moreover, both n-channel and p-channel devices are B-T stable. In addition, the SIS technology has almost completely eliminated the steps at the silicon island edges. Of the three technologies investigated, only SIS offers low leakage current, B-T stability, and planarity.

REFERENCES

1. J. C. Sarace and A. C. Ipri, Electrochemical Society, Fall Meeting 1974, Abstract #197.
2. A. C. Ipri and J. C. Sarace, IEEE J. Solid State Circuits SC-11, 329 (1976).
3. D. W. Flatley and W. E. Ham, Electrochemical Society, Fall Meeting 1974, Abstract #198.
4. J. L. Gates and O. K. Griffin, Appl. Phys. Letters 27, 43 (1975).
5. J. A. Oppels and M. M. Paffin, Philips Research Reports 26, 157 (1971).
6. E. Bassous, H. N. Yu, and V. Maniscolco, Electrochemical Society, Fall Meeting 1975, Abstract #175.
7. R. J. Dexter, S. B. Watelski, and S. T. Picraux, Appl. Phys. Letters 23, 455 (1973).
8. E. C. Spencer and P. H. Schmidt, J. Vacuum Science and Technology 8, 552 (1971).
9. H. M. Manasevit and F. L. Monitz, J. Electrochem. Soc. 114, 2041 (1967).
10. L. J. Stinson, J. A. Howard, and R. C. Neville, J. Electrochem. Soc. 123, 551 (1976).
11. G. W. Cullen, J. F. Corboy, and R. T. Smith, J. Crystal Growth 31, 274 (1975).
12. A. M. Goodman, IEEE Trans. Electron Devices ED-22, 63 (1975).
13. A. C. Ipri, IEEE SOS Technology Workshop, Lake Tahoe, California, 1975.
14. T. Aoki et al., Electrochemical Society, Spring Meeting 1975, Abstract #148.
15. J. H. Freeman, Technical Report #AERE-R 8147, Scientific Administration Office, AERE Harwell, Oxfordshire, England OX110RA.
16. D. M. Jamba et al., Contract Report #N00014-75-C-0080, Naval Research Laboratory, Washington, D.C.

APPENDIX

As part of this contract, test transistors fabricated by each technology are required. The test transistors are packaged in 14-pin packages and are internally wired as shown below.

Device Description	Dimensions (mils)	Pin Number		
		Gate	Source	Drain
n-channel edge	1 x 0.3	4	7	6
n-channel edge	12.4 x 0.3	4	7	5
n-channel edgeless	18.6 x 0.3	3	1	2
p-channel edge	1 x 0.3	11	8	9
p-channel edge	12.4 x 0.3	11	8	10
p-channel edgeless	18.6 x 0.3	12	14	13

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500 Superior Avenue
Newport Beach, CA 92660
ATTN: Eli Harari

RCA Corporation
Marne Highway
Building 108-104
Moorestown, NJ 08057
ATTN: Dr. Jack Hilibrand

Advanced Micro Devices, Inc.
901 Thompson Place
Sunnyvale, CA 94086
ATTN: Oolep Indreko

Motorola Inc. M104
2200 W. Broadway
Mesa, AZ 85202
ATTN: Bob Jenkins

Department of Defense
Director NSA
R-15
9800 Savage Road
Ft. Meade, MD 20755
ATTN: Ronald T. Jerdonek

RCA Corporation
Bldg, 10-8
Camden, NJ 08102
ATTN: H. W. Kaiser

Tyco Sophikon Div.
16 Hickory Drive
Waltham, MA 02154
ATTN: H. LaBelle

University of Southern California
Seaver Science Center, 303
Los Angeles, CA 90007
ATTN: Kurt Lehovec

Naval Electronic Lab Center
Microelectronics Division
271 Cataline Blvd.
San Diego, CA 92152
ATTN: Olof Lindberg

Hewlett-Packard
11000 Wolfe Road
Cupertino, CA 95014
ATTN: Lawrence Lopp

Rockwell International
3370 Miraloma
Anaheim, CA 92803
ATTN: James Luisi

Raytheon
Hartwell Road
Bedford, MA 01730
ATTN: Richard Lydick

Union Carbide
8888 Balboa Avenue
San Diego, CA 92123
ATTN: Jan Maurits

Newport Beach Research Ctr.
Hughes Aircraft Company
500 Superior Avenue
Bldg. 700, MS A2114
Newport Beach, CA 92663
ATTN: Denis McGreivy

Adolf Meller Company
Box 6001
Providence, RI 02904
ATTN: Max Meller

Rockwell International
3370 Miraloma Avenue
Anaheim, CA 92803
ATTN: F. B. Micheletti

Hewlett-Packard
11000 Wolfe Road
Cupertino, CA 95014
ATTN: Robert Mueller

Westinghouse Electric Corp.
P.O. Box 1521 MS 3527
Baltimore, MD 21203
ATTN: Harry Oehler

INTEL Corp.
3065 Bowers
Santa Clara, CA 95051
ATTN: William Oldham

General Electric R&D
Electronics Park
Box 45, Bldg. 7
Syracuse, NY 13201
ATTN: Earl L. Parks

Rockwell International
4311 Jamboree Road
Newport Beach, CA 92663
ATTN: William Pearce, Jr.

Westinghouse Research Labs
1310 Beulah Road
Pittsburgh, PA 15235
ATTN: P. Rai-Choudhury

Honeywell (SSEC)
12001 State Hwy. 55
Plymouth, MN 55441
ATTN: Amolak R. Ramde

Mission Research Corporation
7650 Convoy Court
San Diego, CA 92111
ATTN: James Patrick Raymond

R & D Associates
4640 Admiralty Way
P.O. Box 9695
Marina del Rey, CA 90291
ATTN: S. Clay Rogers

ITEK
Optical Systems Division
10 Maguire Road
Lexington, MA 02173
ATTN: Dr. J. Burns

Tyco Saphikon Division
16 Hickory Drive
Waltham, MA 02154
ATTN: Ralph Russi

Collins Radio Division
Rockwell International
4311 Jamboree Road
Newport Beach, CA
ATTN: Gary Shaw B503/230

Hughes Aircraft Company
P.O. Box 92919 - Airport Station
Los Angeles, CA 90009
ATTN: Dennis Shumake
Bldg. 377, MS C209

Teledyne
1901 S. Bundy
Los Angeles, CA
ATTN: John T. Spoer

Northrop
3401 W. Broadway
Hawthorne, CA 90250
ATTN: Joseph Srour

RCA
Route 202
Somerville, NJ 08876
ATTN: Roger G. Stewart
MS 111

Aerospace Corp.
P.O. Box 92957
Los Angeles, CA 90009
ATTN: Walter Sturm

American Microsystems Inc.
3800 Homestead Road
Santa Clara, CA 95051
ATTN: Don Trotter

Harris Semiconductor
Box 883
Melbourne, FL 32901
ATTN: N. W. Van Vonno
MS 5195