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SUMMARY REPORT ON USAF SUPER RECEIVER/NAVIGATOR DEVELOPMENT. (U)

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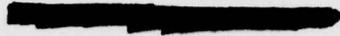
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Technical Memorandum

**SUMMARY REPORT ON USAF SUPER
RECEIVER/NAVIGATOR DEVELOPMENT**

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ABSTRACT

This report summarizes the Phase 1 development work completed in January 1973 on the Super Receiver/Navigator for the US Air Force. The functional design of an improved Loran receiver/navigator that employs new measurement and data processing techniques is described. Design definitions of the Radio Frequency Unit, the Digital Measurement Unit, and the Receiver and Navigator software are provided. Software routines were run on the IBM 360/91 digital computing system at APL using simulated input data. Performance predictions of the Super Receiver/Navigator, based on the results of these runs, are also supplied.

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1. INTRODUCTION

From April 1972 to January 1973, The Applied Physics Laboratory developed the functional design of an improved Loran Receiver/Navigator that employs new measurement and data processing techniques. This Phase 1 development effort defined the Radio Frequency Unit, the Digital Measurement Unit, and the Receiver and Navigator software designs. The software subroutines were run on the IBM 360/91 digital computing system at APL using simulated input data. These runs produced data that permitted some predictions on the performance of a Super Receiver/Navigator in the real-world environment.

This summary report is the last in a series of reports which were issued to describe Phase 1 work. It presents and discusses the current design of the Super Receiver/Navigator. Previous reports (Ref. 1 through 4) describe the design work during development. Where the present design definition differs, the information presented herein supersedes that previously reported.

2. BACKGROUND

In November 1966 The Applied Physics Laboratory (APL) was requested by the Department of Defense to participate in the engineering activities of the Defense Communications Planning Group (DCPG). During the following five years, APL accomplishments included a precision aircraft navigation and delivery system and its environmental support system which are currently operated by the Air Force. These systems are known as Pave Phantom and Sentinel Lock/Loran.

The high-accuracy location and delivery obtained using these systems is attributable to the precision of horizontal location inherent in the Loran-C system of navigation, and to the precision of vertical location inherent in the digital instrumentation of barometric altimetry. Two other precision-navigation, Loran-C systems were developed by DCPG at APL prior to Pave Phantom, each of which used a different Loran-C receiver. The experience gained during this effort indicated that none of the three different Loran-C receivers fully exploited the potential of the Loran-C positioning capability. A study of other operating receivers reinforced the view that the state of the art in Loran receiver design could be advanced.

Following termination of the APL association with DCPG in 1971, APL recorded the navigation and delivery principles in Ref. 5 and initiated exploratory research on the degree to which the transmitted Loran-C wave form can be recovered from the received ground-wave signal in the presence of noise. This research indicated that the application of new signal processing techniques in receiver design could substantially improve both the dynamic and static receiver measurement capability (Ref. 6).

As a result of this research, the Air Force sponsored a Phase 1 task at APL to design a new Loran Receiver/Navigator which would embody new Loran signal processing concepts and incorporate the horizontal navigation principles of Ref. 5. This design has become known as the Super Receiver/Navigator. A Phase 2 task was planned under which

the navigation capability would have been extended to the vertical dimension and the complete design incorporated in an engineering prototype.

The Phase 1 design of the Super Receiver/Navigator was carried out during the period April 1972 to January 1973. The design as of the end of January 1973 is reported herein. The current design has arbitrarily excluded Loran-D to avoid the additional complexity of dual modes during the conceptual development of the signal processing techniques. The extension of the design to include both modes, Loran-C and Loran-D, is now straightforward and can be easily accomplished during Phase 2.

3. SYSTEM SPECIFICATION

The initial task undertaken on the Super Receiver/Navigator design was the assembly of an initial set of specifications which would define the goals, requirements, and boundary conditions applicable to the Phase 1 work to be performed by specialists in the various fields, and at the same time serve as a model for a Phase 2 specification. This preliminary specification was an adaptation of the Air Force specification for the AN/ARN-101 Loran set. As design of the Super Receiver/Navigator progressed, the need for modifications to the preliminary specifications to ensure the full exploitation of the concept in Phase 2 became obvious. The Phase 2 Super Receiver/Navigator specification is in Appendix A.

4. FUNCTIONAL BLOCK DIAGRAM

The Super Receiver/Navigator is divided into three major units: the Radio Frequency Unit (RFU), the Digital Measurement Unit (DMU), and the Computer, Control and Display Unit (CCDU) (see Fig. 1).

The basic function performed by the Radio Frequency Unit is to process the incoming signal, principally by analog means, so that the signal arrives at the Digital Measurement Unit at a specified voltage level with negligible signal distortion. An additional function, under some circumstances, is to cancel continuous wave interference without signal distortion.

The Digital Measurement Unit provides the basic timing oscillator (local clock), the conversion of voltage measurements at sample points of the RF waveform to binary digits, and the control of measurement sequences and transfer of data to the computer. The Digital Measurement Unit operates in three modes; Search, Settle, and Track. When the unit is in the search mode, the binary data are pre-processed before transfer to the computer. In other modes the data are transferred directly.

The Computer, Control and Display Unit consists of the digital computer and the associated input/output interfaces. The computer contains the software programs which embody the Loran receiver functions, the navigation functions, and the overall control program. The input/output interfaces are of two kinds: one is the control/indicator which provides the human interface, and the other is the guidance and control subsystems, such as guidance displays, autopilot, and automatic release of stores.

RADIO FREQUENCY UNIT

Antenna Coupler

Signals received by the antenna are applied to the antenna coupler where they are amplified with only a small amount of filtering. The antenna

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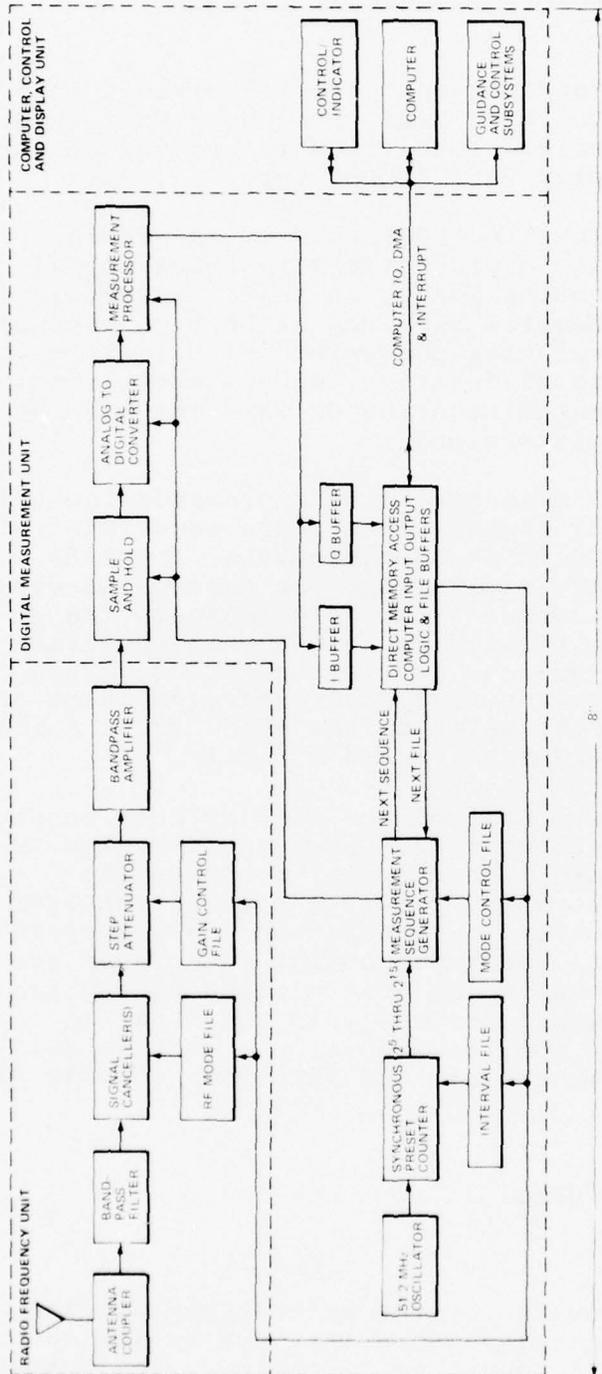


Fig. 1 LORAN SUPER RECEIVER/NAVIGATOR BLOCK DIAGRAM

coupler output is suitable for driving a balanced low impedance transmission line. Therefore, the antenna coupler can be located near the antenna, and signals will be transferred to the receiver section without loss or interference by local undesired signals.

Bandpass Filter

The bandpass filter provides attenuation of undesired signals outside the Loran-C signal bandwidth.

Signal Canceller

The signal canceller is a phase-lock device which attenuates undesired signals within the Loran-C signal bandwidth. When a command to operate is received from the computer through the RF mode file, the signal canceller automatically searches for CW or FSK signals and phase locks to the first signal encountered. The phase lock loop output signal is adjusted to the proper amplitude and added out of phase to the undesired input signal producing attenuation through cancellation. A signal canceller is required for each undesired signal. The Loran-C signal is unaffected by the signal canceller.

Step Attenuator

The step attenuator sets the overall gain of the Radio Frequency Unit by attenuation of the signal. The attenuator setting is controlled by the computer through the gain control file. The step attenuator is a very wide bandwidth device producing extremely small signal phase shift over a large attenuation range.

Bandpass Amplifier

The bandpass amplifier is a fixed gain device which provides the majority of the Radio Frequency Unit signal amplification. The output is suitable for driving the Digital Measurement Unit. The bandpass amplifier also provides additional attenuation of undesired signals outside the Loran-C signal bandwidth.

DIGITAL MEASUREMENT UNIT

Sample and Hold and Analog-to-Digital Converter

The digitizing portion of the measurement unit consists of a sample and hold circuit which selects and holds an analog voltage sample point value, and a 10 bit analog-to-digital converter which converts the sample point value to a negative two's complement binary number.

Measurement Processor and I and Q Buffers

The output of the analog-to-digital converter passes through the measurement processor. The measurement processor is designed specifically for pipeline synchronous preprocessing in the search mode. The output of the measurement processor is transferred to one of two buffer registers. One is labeled I buffer for the in-phase voltage component. The other is labeled Q buffer for the quadrature voltage components. The names do not literally apply until sample point timing adjustments make Q values small and I values large in an absolute sense.

Direct Memory Access, Computer Input/Output Logic, and File Buffers

After each measurement sequence, when signalled by the measurement sequence generator, the I and Q buffers fill, and the direct memory access logic transfers the contents of the buffers to a preselected table in the computer memory. When the table in the computer memory is filled, a counter in the direct memory access logic, which was preset by a computer program, overflows and signals the end of a measurement sequence group file. Each file contains a group of up to four measurement sequences. At this time the next measurement file words are transferred from the file buffers to the gain control, RF mode, interval, and sequence mode control file registers. The transfer of the file buffers to the file registers initiates a new group of measurement sequences. Simultaneously, an interrupt is sent to the computer, signalling that the preselected measurement tables for the preceding sequence group file are filed in the

computer memory, the current sequence group file is in progress, and the computer program must fill the file buffers for the next sequence group.

Timing and Measurement Sequence Generator

Timing is provided by the 51.2 MHz temperature stabilized crystal oscillator. This frequency is chosen to give the simplest interface between the 16-bit synchronous preset counter and the computer search, settle, and track routines which calculate in binary the numbers for the synchronous preset counter. The slower rate counter stages of the synchronous preset counter, 2^5 through 2^{15} , provide the clock and timing signals to the measurement sequence generator. The measurement sequence generator provides the control and clock signals to the sample and hold circuit, analog-to-digital converter, and measurement processor. The measurement sequence generator also signals the direct memory access logic when the end of one measurement sequence and the beginning of the next measurement sequence has occurred, thereby sending the contents of the I and Q buffers to the computer memory. At the end of a measurement sequence, the next mode word in the mode file is selected by the measurement sequence generator and the next interval word is preset into the synchronous preset counter thus beginning a new measurement sequence. If a next file signal is sensed by the measurement sequence generator at the end of a measurement sequence, the next measurement sequence mode word and the next interval word are selected from the file buffers, and the file buffers are transferred to the active files. This initiation of new file data coincides with the interrupt sent to the computer signifying the completion of the measurement tables in computer memory and the requesting of more data for the file buffers.

COMPUTER, CONTROL AND DISPLAY UNIT

Computer

The proposed CCDU computer is a 16-bit digital processor plus memory which is representative of the present state of the art. As presently conceived, the Super Receiver/Navigator requires direct memory access. For a Phase 2 engineering prototype, a commercially available mini-processor would be selected which has adequate peripheral support for the developmental effort required, and which has a memory of 16K, 16-bit words. At the present time, the final design is expected to require about 5000 16-bit words which could be incorporated in a time-shared general purpose computer, if one of adequate performance were available; otherwise in a dedicated computer.

Control/Indicator

The control/indicator permits the operator to exercise control over the system. It accepts inputs from the operator and indicates the status of the system as well as specific data requested by the operator. It is expected that the majority of the non-permanent initial conditions will be inserted into the system by non-manual means, such as cassette-type magnetic tape. If this were the case, the tape reader would be incorporated into the control/indicator.

Guidance and Control Subsystems

The specific types of components which make up the guidance and control subsystems are dependent on the type of aircraft and its mission. In the case of a piloted aircraft, these components would include the attitude/direction indicator (ADI), the horizontal situation indicator (HSI), and displays for numerical information such as distance to go and time to go. Additionally, if the aircraft is equipped with an autopilot, the opportunity is provided for automatic guidance in response to commands from the computer. Providing these commands to the autopilot is optional in the case of piloted aircraft, but mandatory in the case of drone aircraft. If the mission of the

aircraft includes the release of stores or aerial photography, the interface components of these subsystems would include relays for which closure signals would be produced by the computer. The Phase 1 effort has not been concerned with the design of the control/indicator, the specific interface requirements, or the characteristics of guidance and control subsystems. The Phase 1 effort has provided the definition of the computer side of these interfaces. The control/indicator and the interfaces can be completed when Phase 2 is initiated and the aircraft interfaces can be defined.

5. RADIO FREQUENCY UNIT

The primary goal of the Super Receiver/Navigator design is to make meaningful measurements of the differences in times of arrival of signals from any two Loran transmitting stations to the level of a very few nanoseconds without rate aiding. To accommodate the signal strengths of all transmitters throughout the service area, the receiver must be designed for a dynamic range of 100 dB. Therefore, a Radio Frequency Unit is required which can be switched during the off time between two adjacent signals from two transmitters to any level throughout a 100 dB dynamic range without introducing significant phase distortion, or without deviating from a determinable relationship between amplification level and phase. A design has been completed which achieves the first alternative with no appreciable phase distortions.

Another goal of the Super Receiver/Navigator is to achieve significant improvements in receiver performance in any electrical interference environment. A new signal processing technique incorporated in the computer can cope with all natural atmospheric noise and intermittent man-made interference. However, it cannot cope with continuous-wave (CW) interference when the duty factor of the CW is close to 100%. Consequently, the Radio Frequency Unit is required to reject CW interference. Out-of-band interference is rejected by the use of bandpass filtering. For in-band CW interference, a signal canceller has been designed which can reduce in-band CW by at least 30 dB with no appreciable distortion of Loran signals. This device is shown in Fig. 2.

The design of the Radio Frequency Unit in breadboard form is described in Appendix B.

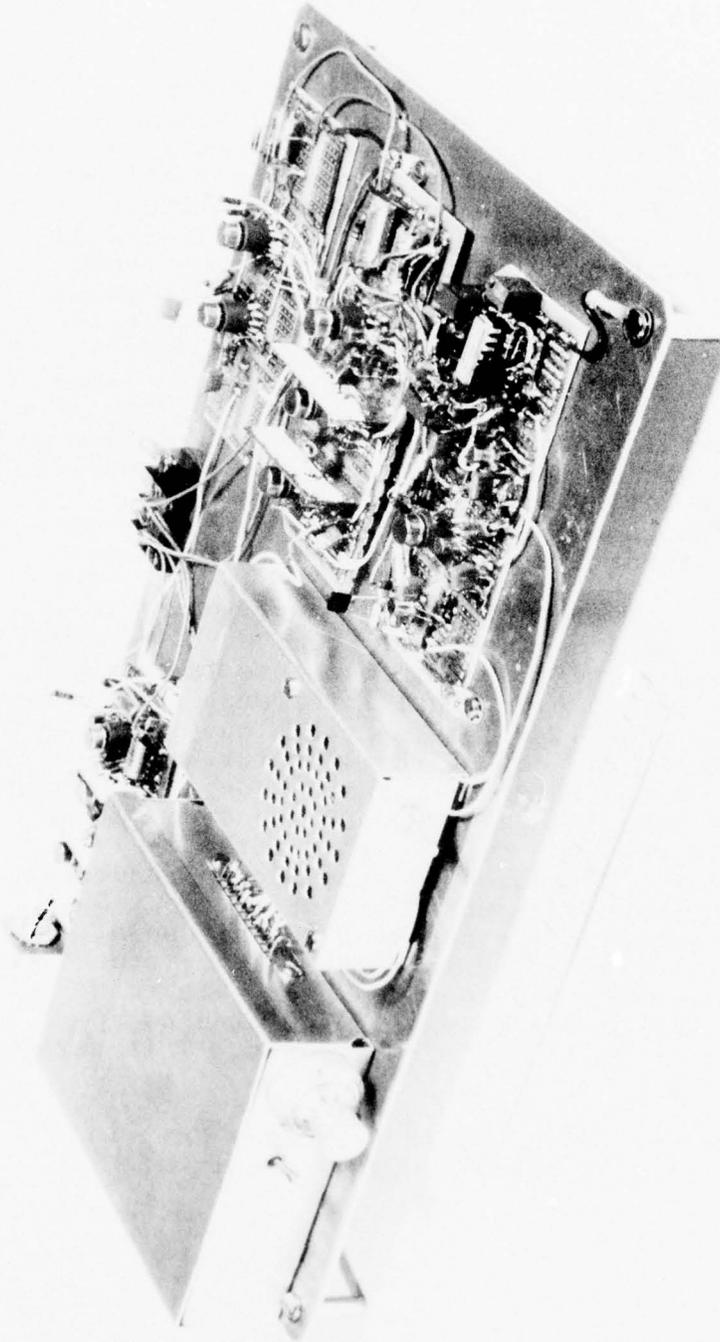


Fig. 2 SIGNAL CANCELLER BREADBOARD

6. DIGITAL MEASUREMENT UNIT

The principal function of the Digital Measurement Unit is to make voltage measurements at computer specified locations on the waveform of each Loran pulse as it is received, digitize these measurements, and transfer the numerical result to the memory of the computer. To obtain useful results, the short-term timing accuracy, the resolution of time, and the resolution of voltage must be consistent with the Super Receiver/Navigator goal of measuring time differences to a very few nanoseconds. In addition, the Digital Measurement Unit must accept instructions from the computer which dictate the time of the measurements and the measurement mode. Finally, the digitized results must be transmitted to the computer at a rate which precludes any loss of data at the most rapid Loran data rate. Assuming that the computer allows direct access to the memory, these requirements can be met with a minimum of hardware.

The design of the Digital Measurement Unit is described in Appendix C.

7. SOFTWARE

All of the Loran receiver functions, except those performed by the Radio Frequency Unit and the Digital Measurement Unit, are embodied in a program of computation and logic instructions. The computer section of the CCDU will contain this program. For convenience, the total program is divided into subroutines and an overall Control Program. The subroutines include the following: Search, Settle, Track, Station Identification, New Track, Navigation, and Warnings. All of the subroutines, except the Control Program and the Warnings Subroutine, have been written in Programming Language 1 (Ref. 7) and tested on an IBM 360/91 computing system. The Control Program has not been written because it is critically dependent on the characteristics of the computer, and the identification of a computer is part of the Phase 2 program. The Warnings subroutine was not written during Phase 1 because self-check features are also computer dependent and the standard warnings are straightforward interpretations of well-defined Loran signal modulations or of other parameters already available in the computer.

The nomenclature and definitions used in the subroutines are presented in Appendix D.

SEARCH

The Search subroutine is designed to achieve a high probability of detecting Loran-C pulses and a low probability of false detections. This is accomplished in a five step process:

1. To initially record a detection of a single pulse, the absolute value of the measured voltage summed coherently over 10 consecutive cycles must exceed a specified threshold.
2. At least six of these detections must be located in the time domain such that they are potential members of a Loran group of eight pulses.

3. The six or more detections that pass these two tests must exhibit either the master or secondary phase code.
4. Those detections that pass these three tests must be found again in the next Group Repetition Interval (GRI) in the same 100 microsecond time slot.
5. If the test is passed in the fourth step, a desired Loran signal has been found and the fifth step is taken. Its phase code and the time of occurrence of the first pulse of the group, along with other pertinent data, are recorded in the Track Table in the chronological order of appearance within the local GRI, and the accompanying track status indicator is changed from Search to Settle.

At the end of each GRI if there are no detections, or at the end of every other GRI if there are, the gain is incremented and the process repeated.

The duration of Search is dependent on the signal strength of the weakest desired transmitter, and on the size of the gain increments which has not yet been finalized. If all of the signals from the desired transmitters are sufficiently strong, search will be completed in the minimum of two GRI's. On the other hand, if the weakest transmitter requires the maximum receiver gain, and the maximum gain of 100 dB is approached in 1 dB steps, and cross-rate interference requires a cross rate check every GRI, then Search will be completed in a maximum of 200 GRI's. In a Loran-C chain using the longest GRI of 0.1 second, this corresponds to 0.2 and 20 seconds, respectively.

The design of the Search subroutine is described in Appendix E.

SETTLE

The output of the Search subroutine allows the quadrature sample points to be placed by the Digital Measurement Unit in the Settle mode to

within a microsecond of a positive going zero crossing of the decoded carrier within the 100 microsecond time slot in which the detection was made.

In the Settle mode, the Digital Measurement Unit makes eight measurements. The first two are a pair of quadrature and in-phase voltage samples (Q_0 and I_0) with Q_0 located within 1 microsecond of a zero crossing of the carrier, and with I_0 located 2.5 microseconds later. The second pair is located 10 microseconds later, the third 20 microseconds later, and the fourth 30 microseconds later than the first. Thus the data obtained for I_0 , I_1 , I_2 , and I_3 are measurements very near the peak of the first half cycle of four contiguous cycles.

Settle is accomplished by iteratively approaching the leading edge of the pulse with the sample points. A decision to move earlier or later on the pulse at each iteration is made as the result of a four step process:

1. The pulses are decoded.
2. The Q and I data are subjected to a consistency test. To pass this test, there must be at least three of the group of eight pulses which are consistent in the corresponding values of both Q and I. If they are not, all the samples are rejected and the measurements repeated. If consistency is found, corresponding Qs and Is are summed for the consistent pulses and the process advances to the third step.
3. The values of Q_3 and I_3 are used to make a fine phase adjustment for the location of the measurements in the next iteration.
4. The values and selected ratios of I_0 , I_1 , I_2 , and I_3 are used to determine how many cycles to move the Q and I sample points earlier or later for the next set of samples.

The process repeats until the four pairs of Q and I samples rest on the first half cycle of the first, second, third, and fourth cycles of the pulse. When this occurs, the track status indicator is changed from Settle to Track.

Tests of the Settle subroutine have shown that Settle will find the leading edge of the pulse in about seven GRIs.

If the pulse were an isolated skywave, Settle would terminate at its leading edge. Consequently, at the conclusion of Settle, it may be necessary to perform a groundwave check. If the pulse is a skywave, sampling can be done ahead of the pulse by placing the Settle or Track sample points to detect the presence of an earlier pulse.

The design of the Settle subroutine is described in Appendix F.

TRACK

Upon completion of the Settle subroutine, the first of the quadrature sample points for Settle is located at the first zero crossing of the first cycle. The desired locations for the quadrature, QT, and in-phase, IT, samples for Track, therefore, are 30 and 32.5 microseconds later, respectively. These locations are recorded in the Track Table.

The QT and IT samples from each pulse are first decoded. Then the values that these samples should have are predicted, based on their expected values and time rates of change determined during the previous GRI. These predictions are compared to the QT and IT samples to determine errors. The error in IT is then compared to a maximum permissible error and, if smaller, QT is then compared to the same maximum permissible error. If either QT or IT exceed the maximum permissible error, both are rejected. If both are smaller, a counter is incremented indicating acceptance, and the values of QT and IT are summed with the accepted values of corresponding samples from other pulses in a group of eight.

When all eight pulses in a group are processed in this manner, the expected values of QT and IT are determined for the current GRI and the locations of the sample points for the next GRI are predicted. In addition, expected values of the gain and the number of pulses accepted are determined.

Next, the expected value of the gain is compared to minimum and maximum limits and the gain for the next GRI adjusted, if required. Finally, the QT and IT error limits for the next GRI are adjusted such that the expected value of the number of pulses accepted in a severe noise environment will be four.

The dynamic characteristics of the tracking loop response can be adjusted by assigning desired values to its time constant and damping coefficient. When these values are 10.5 sec. and 0.707 respectively, the maximum tracking error due to noise is expected to be less than 5 nanoseconds.

The design of the Track subroutine is described in Appendix G.

STATION ID

When three or more transmitting stations of a chain are in track, a positioning capability can be established by computing time differences. To do this, it is first necessary to identify the transmitters so that the desired time differences can be computed. It is not required that the master transmitter be in track.

The Search and Track subroutines produce a table of data regarding transmitters which are being tracked. This Track Table is organized chronologically in the order of the transmitter's appearance in the local GRI. Among other things, this table stores the phase code of each transmitter in track. If the transmitter in track include the master, it can be located in the table by its unique phase codes. If the master is not in track, the earliest transmitters in the GRI can be found by locating the place in the table where the phase code changes from that associated with GRI-A to GRI-B or vice versa.

The Station ID subroutine uses the approximate location of the initial position of the receiver to identify the transmitters. This is done by computing the position of the receiver for each combination of transmitters in track taken three at a time with each combination of transmitters taken three at a time. If the computed receiver position compares favorably with its given location, three of the transmitters in track are identified. The process is repeated until all transmitters in track are examined.

The identities of all transmitters which have been identified as radiating members of the chain are established by recording in an ID table the location in the Track Table of the transmitter's pertinent data and the track status parameter is changed to Track Station. Those transmitters which are in track but not identified are labeled by changing the track status parameter to "Track Spoofer".

The design of the Station ID subroutine is described in Appendix H.

NEWTRACK

As the result of initial search and settle, all transmitters which have sufficient signal strength are in track. As the aircraft flies through the service area, some of the initial transmitter's signals fade and others become trackable as they are approached. These new transmitters bear a known relationship to the transmitters which are in track, and therefore the time of arrival of their signals within a GRI can be predicted.

The computer has stored in memory the locations of all the transmitters in the chain. Of those which are in track, at least three transmitters are used for navigation, one of which is used as the reference. It is therefore possible to compute the times of arrival of signals from transmitters not in track relative to the reference. At the completion of the computation, the new transmitter is entered into the Track Table at a position which bears the correct chronological

order in the local GRI. The track status is set to Settle, indicating that track is not yet established on the correct tracking point.

The design of the Newtrack subroutine is described in Appendix I.

NAVIGATION

When three or more transmitters are in track and the transmitters have been identified, the Super-Receiver/Navigator is ready to navigate. Position data from the signals of any three transmitters in track designated by the Control Program can be used.

The guidance principles embodied in the Navigation subroutine are those which are set forth in Ref. 5 for fixed course guidance between designated waypoints. This reference also describes a number of other possible guidance modes, but these have not been incorporated in the Navigation subroutine pending final definition of Phase 2 applications for the Super-Receiver/Navigator.

Aircraft guidance using the positional data of a hyperbolic grid system involves frequent coordinate conversion to orthogonal aircraft coordinates. To ease the burden of these conversions on an avionic computer, a coordinate conversion technique was developed and published in Ref. 5. It is a spherical hyperbolic to planar orthogonal coordinate transformation and is referred to as Loran Rectangular Coordinates. It is used in the Navigation subroutine.

The Super-Receiver/Navigator must be loaded with data prior to the computation of directional guidance. These data, among other things, define the locations, baseline lengths, and status of the Loran transmitters and the flight program of the aircraft. The transmitter locations are given in earth centered orthogonal coordinates (see Appendix D) and the status is either radiating or non-radiating. The flight program is a chronological tabulation of data which locate each waypoint. The location data consist of all the

time differences, taken with respect to the chain master, that apply to each waypoint. In addition, the input data include the ranges from the initial position of the aircraft to each of the Loran transmitters.

The Navigation subroutine starts by establishing a Loran Rectangular Coordinate system centered at the centroid of the three transmitters designated by the Control Program. Then the Loran Rectangular Coordinates of the Super Receiver are computed corresponding to the measurements of time differences with respect to the reference, i.e., the transmitter associated with the earliest time of arrival of the three. This then allows the proximity to the baseline extensions to be determined. If too close, a warning is activated and the subroutine continues by computing the easting and northing time rates of change and the frequency offset correction as derived from the local clock.

Finally, the subroutine computes the directional guidance for fixed course navigation. First the time differences of the waypoints at the ends of the current leg of the flight are determined with respect to the reference transmitter, so that their Loran Rectangular Coordinates can be determined in the established coordinate system. Having done this, the true course of the path between these waypoints is determined. Subsequently, each time the Super Receiver/Navigator measures its time differences, its cross-track error and along-track distance to the next waypoint and their time rates of change are computed. Heading error is also computed. In Phase 2, values of these parameters would be used to compute manual steering or autopilot commands.

When the along-track distance reaches some minimum value, the flight program advances to the next waypoint and the process repeats until terminated by the Control Program. It is intended that the minimum value of the along-track distance be determined by the geometry of the turn required to intercept the next leg of the flight as described in Ref. 5. This requires air data, and will be accomplished during Phase 2. Consequently, the computational routine required to establish the minimum along-track distance has not yet been written.

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The design of the Phase 1 Navigation subroutine
is described in Appendix J.

8. COMPUTER SYSTEM CHARACTERISTICS

FUNCTIONAL BLOCK DIAGRAMS

A functional block diagram of the engineering prototype Super Receiver/Navigator without the peripheral computer equipment is shown in Fig. 3. The computational software block diagram is shown in Fig. 4.

DATA INPUTS

The data source is a pulsed 100 kHz Loran-C signal. Eight of these 100 kHz pulses, each 25 cycles in length, form a pulse group that is phase coded to distinguish between master and secondary transmitters. As shown in Fig. 5, up to seven Loran-C transmitters can be transmitting in one GRI. Depending on the Loran-C chain, the GRI varies from 39.3 to 100 milliseconds in length. The specific value identifies the chain.

The data sampling points for the three basic data input modes (Search, Settle, and Track) are shown in Fig. 6. The time interval between an amplitude and a phase data sample is 2.5 microseconds, while the time interval between pairs of data samples is ten microseconds. In the case of Search, the data taken at the sample points are preprocessed before transfer to the computer as shown in Fig. 7.

COMPUTER HARDWARE

In order to minimize interrupt processing time associated with each data sample and to minimize buffer storage requirements, two hardware requirements were established. First, direct memory access channels would be used to transmit the digitized data samples, and second, hardware priority interrupts would be used rather than software priority polling of one interrupt.

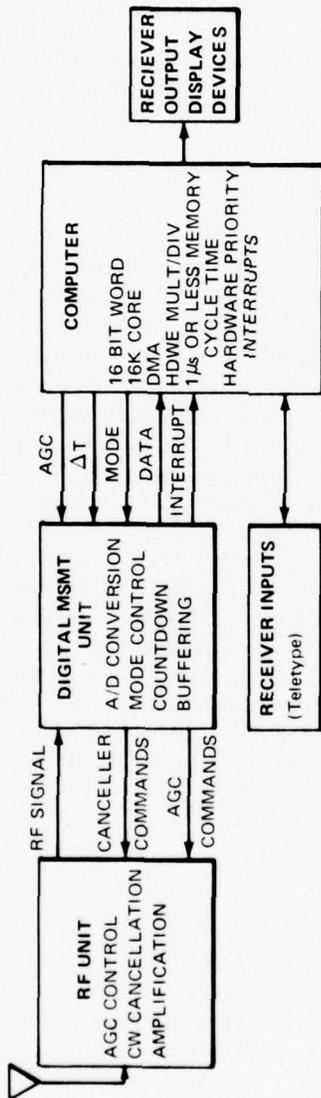


Fig. 3 ENGINEERING PROTOTYPE BLOCK DIAGRAM

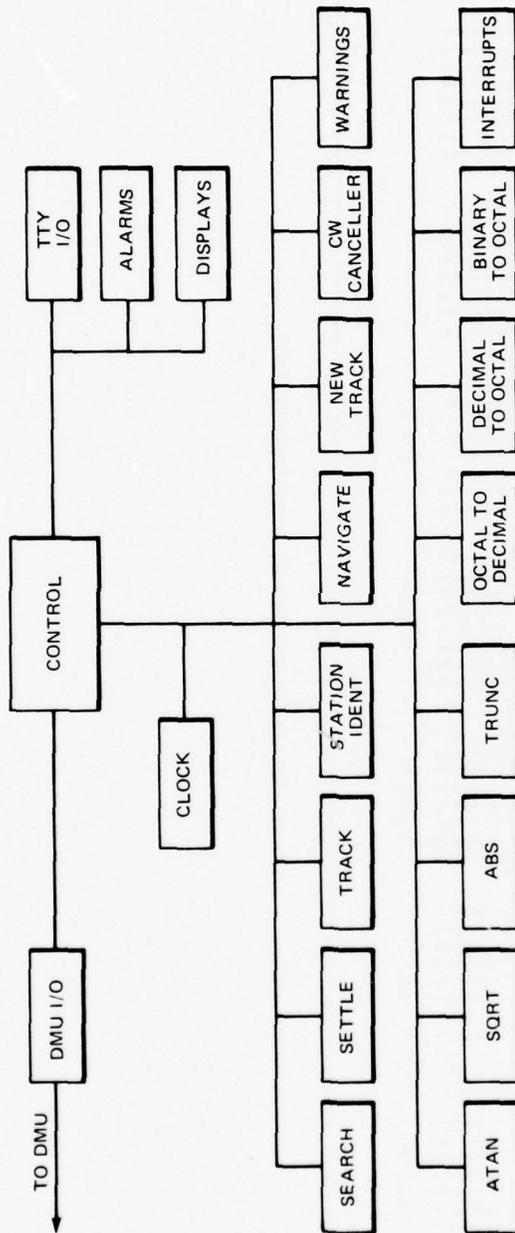


Fig. 4 COMPUTATIONAL SOFTWARE BLOCK DIAGRAM

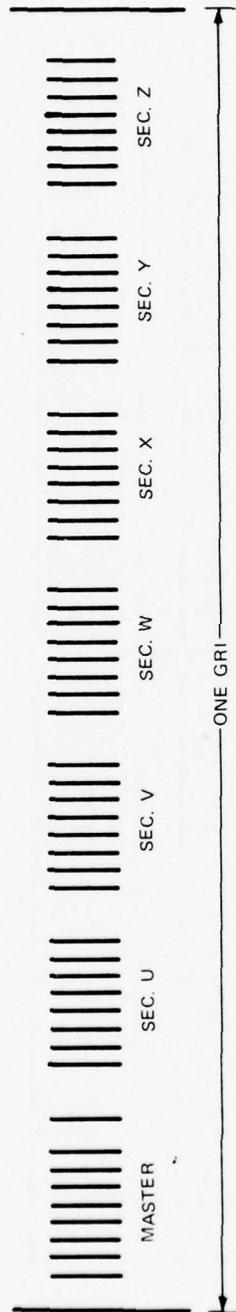
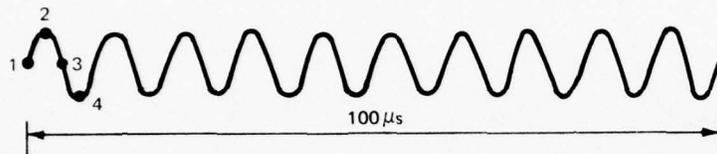


Fig. 5 GRI FILLED BY SEVEN LORAN-C TRANSMITTERS

V_1, V_2, V_3, V_4 FOR EACH CYCLE IS PREPROCESSED IN THE DMU TO GIVE AN I AND A Q INPUT TO SEARCH EVERY $100\mu s$

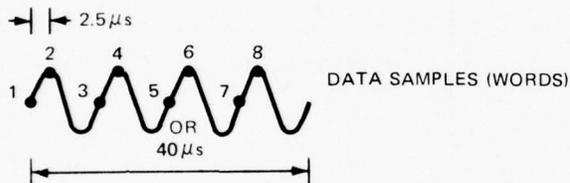
SEE FIGURE 7



SEARCH

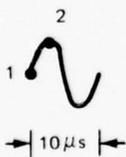
DMA TWO WORDS
 EVERY $100\mu s$,
 CONTINUOUSLY

DATA TRANSMISSION MAY BE 4 WORDS EVERY $200\mu s$ OR 6 WORDS/ $300\mu s$ OR 8 WORDS/ $400\mu s$, ETC.



SETTLE

DMA EIGHT WORDS
 EVERY $1000\mu s$ FOR
 $8000\mu s$



TRACK

DMA TWO WORDS
 EVERY $1000\mu s$ FOR
 $8000\mu s$

Fig. 6 DATA INPUT MODES

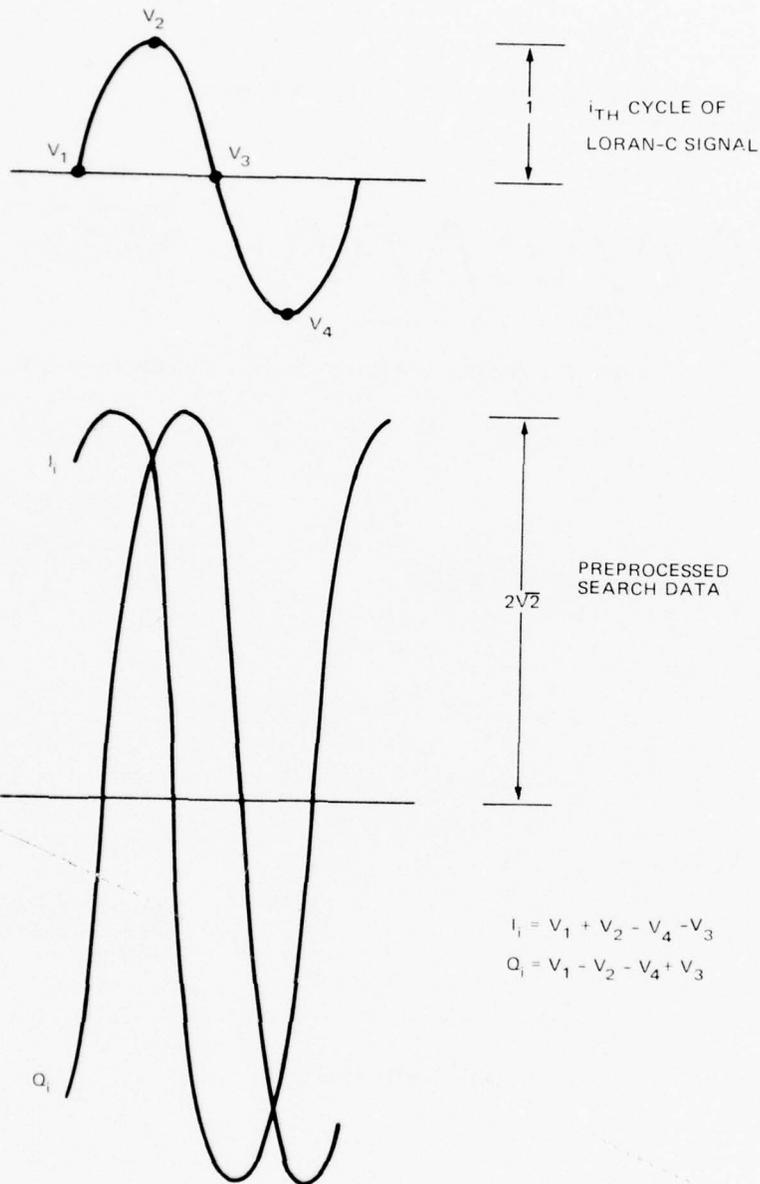


Fig. 7 PREPROCESSED SEARCH DATA

Because of system time requirements, the computer should multiply and divide for fixed point as well as floating point operations. The memory cycle time should be one microsecond or less. To avoid more complicated indirect addressing schemes (and associated overhead) and excessive use of double precision arithmetic, the word length should be not less than 16 bits.

The computer should have a minimum of 16K words of core memory storage according to the estimates in Table 1.

All of the estimates of core storage listed in Table 1 are based upon use in an engineering prototype with the primary goal of rapidly producing a working system. Only minimal attempts were made to produce a minimum core storage version. After the system is debugged and finalized, the program can be revised with minimum core storage as the primary goal.

Insofar as possible, estimates of the program size have been based on subroutine flow charts and digital computer simulations. The estimates for utility, math, and machine routines are based on the core requirements for an existing 16 bit word machine.

For conversion from the language used for the simulations (PL/I) to assembly language of an unknown computer, the number of PL/I statements was multiplied by three and five to produce a minimum and maximum estimate. Then the number of memory locations required for that subroutine was added. The estimates for each subroutine so calculated are shown in Table 1. Estimates for which flow charts or other definitive descriptions do not exist are marked by an asterisk.

PERIPHERAL HARDWARE

The peripheral hardware for the engineering prototype consists of at least the following items:

Table 1

Core Storage Estimates

Item	16-Bit Words
Control Program*	2000
Search	600 to 940
Settle	650 to 910
Track	260 to 370
Station ID	450 to 670
Newtrack	260 to 390
Navigate (Fixed course mode only)	1080 to 1930
Alarms*	200
Signal Canceller*	200
Warnings*	200
Interrupts	150
Programmable Clock	150
Utility Routines: \emptyset to D, D to \emptyset , Bin-Oct, etc.	250
Math Routines: ABS, ATAN, SQRT, etc.	250 to 500
Inputs: Keyboard Parameter Inputs*	1000
Outputs: Keyboard, Digital Displays, Lights, DMU Outputs*	500
Debug	500
Bootstrap Loader	30
Cross Linking Loader	2000
Assembler	1000
Indirect Addresses	500
Totals	12230 to 14390

*Flow charts, etc. have not been prepared.

Card reader

Line printer

Magnetic tape and/or magnetic disc

Keyboard input.

This hardware will allow the prototype computer system to be independent. The system will be capable of executing all input/output functions necessary to assemble programs, list programs, read in new programs, etc. without requiring operations by any other data processing system. For example, the system will be able to:

1. Accept punched cards as input.
2. List the assembled programs on the high speed line printer.
3. Store programs on either the magnetic tape and/or the magnetic disc.
4. Read programs from the tape and/or disc.
5. Assemble programs, etc.

Use of this independent operation feature will free programmer and system check-out personnel from the inevitable, sometimes very lengthy times spent interfacing with other data processing systems. In addition, when the engineering prototype is field tested this feature will permit field support of the technical effort. Without it, intermediate results would have to be mailed or handcarried from a central data processing system to the field test site.

COMPUTER SYSTEM SOFTWARE

The computer selected should have available all software required to allow the computer to communicate with all peripheral equipment such as magnetic tape driver, magnetic discs, line printer, keyboard, etc. In addition, the software should

include at least a cross-linking loader, an assembler, a math package, and an on-line software debugging system (i.e., conversational debugging program).

The conversational debugging program is especially important for the engineering prototype because of the complexity and size of the computational program. Program changes and parameter adjustments are a necessary part of program development of a prototype. While program changes should be fewer for this system than for one with no simulation before system integration and check-out, most of the subroutine simulations have been used to prove a concept rather than to make final adjustments. Integration of the software, both at the subroutine level and with the hardware, begins when the system is turned on. The conversational debugging program is one of the tools that will expedite system integration and check out.

9. PERFORMANCE PREDICTIONS

It has not been possible during Phase 1 to explore in depth all of the performance parameters that normally pertain to Loran receivers. For example, it is not possible to characterize the influence of signal-to-noise ratio in conventional terms because the role that this parameter plays in the Super-Receiver/Navigator signal processing is not conventional. How to characterize it is still an open question, and this question may have to be answered experimentally. Nevertheless, limited experience in computer simulations of the operation of the subroutines permits a few, fairly general performance predictions.

The Search subroutine is called by the Control Program as many times as is necessary to record in the Track Table that the required number of transmitters have been found. Each time it is called, the gain, which starts at the minimum level, is increased, except when a detection has been made in which case the gain is not changed for a cross-rate check. Should the receiver be turned on in an area where the signals of all the desired transmitters are reasonably detectable, search would be complete in two GRIs. If all are not detectable at the minimum gain setting, gain is increased in increments, the size of which is still optional as a design parameter. If the minimum size of 1 dB is selected, the maximum time occupied by search to successfully detect seven transmitters radiating at the slowest Loran rate would be 10.7 seconds assuming no cross rate interference present. If cross rate interference is present and timed so that cross rate signals appear in every GRI, the maximum time occupied by search is 20 seconds. This is the longest search time that could occur. It is expected that search will be complete in 4 or 5 seconds under normal operating conditions in a primary groundwave service area.

The Settle subroutine is called by the Control Program each GRI to process settle data for each transmitter that has been detected. The initial settle data will be obtained from samples of the voltages on the pulse because the sample points

are placed where the search detection was made. However, it is not yet known where the leading edge of the pulse is located. As a result of the tests based on the relative size of the eight consecutive samples of the pulse, the sample points are moved each GRI unless a gain change is required, until the earliest sample point rests on the leading edge of the pulse. Tests of the Settle subroutine indicate that settle will be completed in about seven GRIs, which at the slowest Loran rate occupies 0.7 second.

The Station Identification subroutine successfully identifies all transmitters of a chain in track. It is not necessary that the master transmitter be in track. Station Identification also identifies stations which are not legitimate members of the chain. Station Identification is called only once after the required number of transmitters are in track. Since its operation is not necessarily completed each GRI, its execution time is only dependent on the nature of the computer. Therefore it cannot be estimated at the present time.

Operation of the New Track and Navigation subroutines indicates faultless operation of both can be expected when properly entered in the operational computer. Since operation of neither of these subroutines is tied to the sequence of GRIs, their execution times cannot be estimated until a computer is selected.

Operation of the Track subroutine under real world noise conditions was simulated on the IBM 360/91 computing system. Two cases were run:

1. -6 dB signal to noise ratio
2. 28 dB signal to noise ratio.

Although it was desirable to run many simulations, economy of time and funds dictated that the runs be limited to those which demonstrate the most novel feature of track performance, i.e., the ability to track in real world noise.

A sample signal plus noise is shown in Fig. 8. The data shown were obtained during the investigations reported in Ref. 6. It is clear from the Ref. 6 data and the data presented by the International Telecommunications Union in Ref. 8 that noise in the 90 to 110 kHz band is not Gaussian. In fact, during the Ref. 6 investigations, no evidence of Gaussian noise could be found, even on the quietest days.

It is reasonable to conclude that an assumption of Gaussian noise as the basis for optimization of tracking loop parameters is not valid. Consequently, the Track Subroutine incorporates non-linear time domain filtering of the inputs to the tracking loops to effectively cope with noise.

To test the effectiveness of the filters and the performance of the loops, a Track subroutine signal-plus-noise driver was written which simulates noise; and it was used to drive the subroutine under two conditions. The first is that the signal is 20 dB above Gaussian noise and, when the signal is sampled, there is a 50% probability of an interfering voltage four times greater than the signal. This noise condition results in a signal to noise ratio of -6 dB. The second condition is that the signal is 40 dB above Gaussian noise and, when the signal is sampled, there is a 10% probability of an interfering voltage that is 40% of the signal voltage. This noise condition results in a signal to noise ratio of 28 dB.

The results obtained in the simulation of a stationary receiver driven by noise indicate that the outputs of the tracking loops are essentially the same over the signal-to-noise ratio of -6 to 28 dB. The results also indicate that the phase tracking capability is somewhat better than the capability of current Loran transmitters to control phase. Therefore, it can be predicted that deviations in the output of the tracking loops during operation in the existing Loran-C service will be dominated by the characteristics of the transmitters.

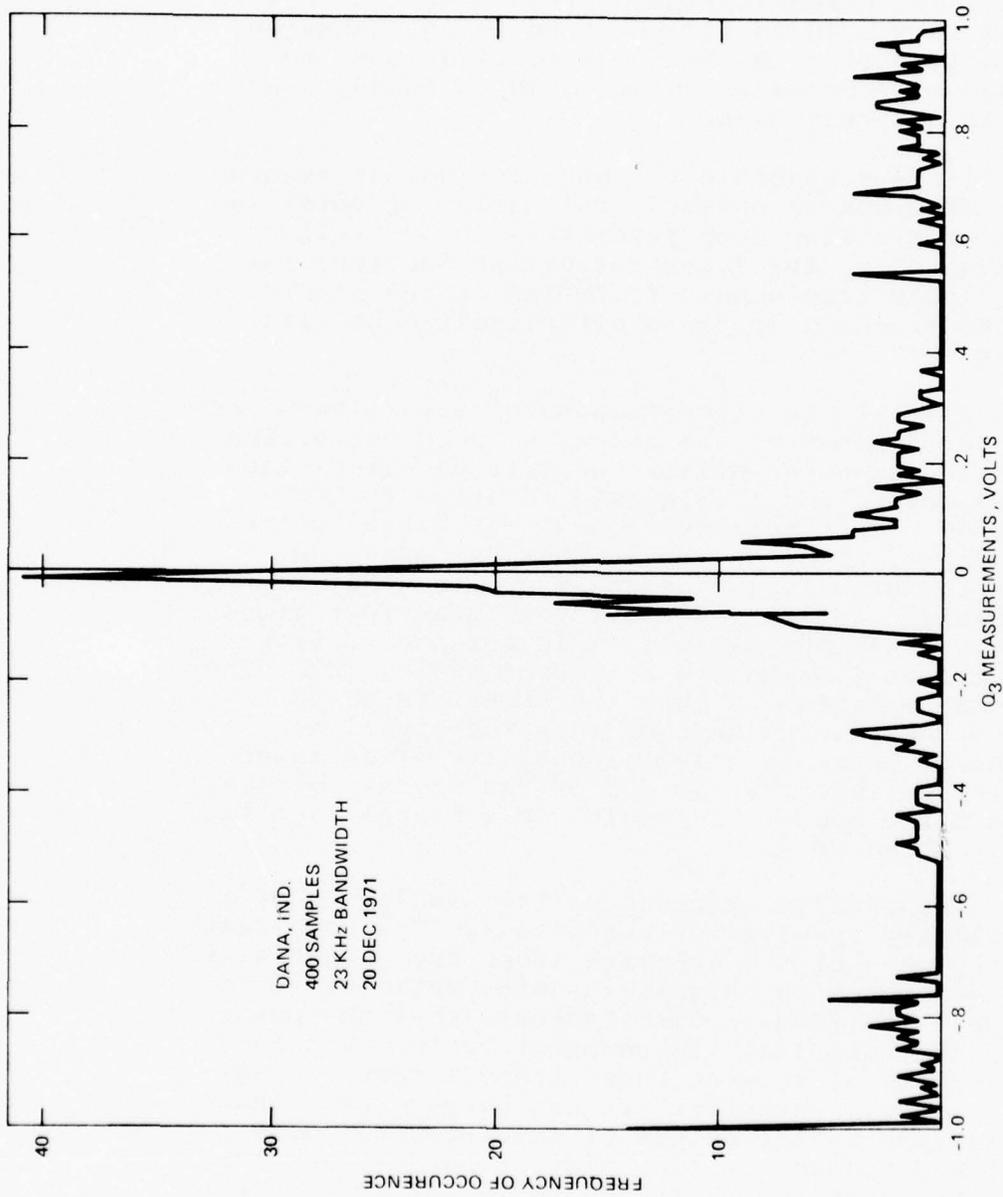


Fig. 8 HISTOGRAM OF O₃

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3. Space Development Department, Report on USAF Loran Super Receiver/Navigator Development, August-September 1972, APL/JHU SDO 3233.3.
4. Space Development Department, Report on USAF Loran Super Receiver/Navigator Development, October-November 1972, APL/JHU SDO 3233.4.
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APPENDIXES

Appendix A

SYSTEM SPECIFICATION FOR THE LORAN SUPER RECEIVER/NAVIGATOR

1. INTRODUCTION

The following paragraphs describe the electrical environment which typifies the Loran-C/D frequency band. Goals for the performance characteristics of various subsystems which constitute the complete Super Receiver/Navigator are also described. The overall goals follow.

1. Data editing: 30 dB advantage.
2. Precision instrumentation: 1 nanosecond resolution.
3. Reliable, rapid lock-on: average time of 5 seconds with $10^{-7}\%$ false lock.
4. Accurate phase track: less than 10 nanoseconds standard deviation.
5. Simplified coordinate conversion: less than 200 words.
6. Relative navigation: position error less than 0.1% distance to go.
7. Enroute altitude: 20 meters standard deviation.
8. Approach and departure altitude: 2 meters plus 2% of height above the ground standard deviation.

2. ELECTRICAL ENVIRONMENT AND DEFINITIONS

2.1 Loran-C. Loran-C is a long-range, high-power, precision navigation system employing automatic envelope and RF cycle comparison techniques. It operates in the frequency band 90 to 110 kHz with a carrier frequency of 100 kHz.

Group pulsing techniques are used in lieu of single pulse transmission to raise the average transmitted power. Eight pulses per group are used at each secondary transmitter and nine pulses per group at the master transmitter. The pulses of the group are phase-coded; i.e., the carrier frequency cycle phase relationship with respect to envelope is changed from pulse to pulse in a group as prescribed for Loran-C. Phase coding provides the signal identification required for automatic signal acquisition and achieves substantial automatic cancellation of skywave interference. A Loran-C chain, consisting of one master and two or more secondary transmitters, operates on a single specific group repetition rate.

2.2 Loran-D. Loran-D is a short-range, low-power navigation system employing the same automatic envelope and RF cycle comparison techniques as Loran-C. It operates in the frequency band of 90 to 110 kHz with a carrier frequency of 100 kHz. It uses group pulsing (sixteen pulses/group) techniques to raise the average transmitted power. The pulses of the group are phase-coded as prescribed for Loran-D.

2.3 Group Repetition Interval (GRI). The GRI is the interval of time between the start of the radiation of a group of pulses from one transmitter to the start of the next group of pulses from the same transmitter. A total of 40 different GRIs are possible, identified by one or two letters and a numeral, e.g., SL-2 signifies a GRI of 79,800 microseconds. The GRIs in microseconds are as follows:

<u>LORAN-C ONLY</u>			<u>LORAN-C AND LORAN-D</u>	
<u>SS</u>	<u>SL</u>	<u>SH</u>	<u>S</u>	<u>L</u>
0	100,000	80,000	60,000	50,000 40,000
1	99,900	79,900	59,900	49,900 39,900
2	99,800	79,800	59,800	49,800 39,800
3	99,700	79,700	59,700	49,700 39,700
4	99,600	79,600	59,600	49,600 39,600

	<u>LORAN-C ONLY</u>			<u>LORAN-C AND LORAN-D</u>	
	<u>SS</u>	<u>SL</u>	<u>SH</u>	<u>S</u>	<u>L</u>
5	99,500	79,500	59,500	49,500	39,500
6	99,400	79,400	59,400	49,400	39,400
7	99,300	79,300	59,300	49,300	39,300

2.4 Master Transmitter. A Loran master transmitter is one of the group of Loran transmitters comprising a single Loran-C chain. It has the burden of precisely maintaining its assigned repetition interval and carrier frequency and of monitoring the synchronization, accuracy, and stability of its paired secondary transmitters.

2.5 Secondary Transmitter. A Loran secondary transmitter and a master transmitter comprise a Loran pair. A secondary has the burden of maintaining an accurate fixed delay between the reception of master and transmission of its own signal, and of monitoring the time difference of the other signals having the same GRI.

2.6 Chain. A Loran chain consists of a master and up to six secondaries. The chain is identified by its GRI.

2.7 Time Difference. Time difference is a measure of the time in microseconds between the reception of the signal designated as the reference and the signal from a secondary in the same GRI.

2.8 Loran-C Pulse Group. A Loran-C pulse group consists of eight phase-coded pulses from any secondary transmitter or nine from a master transmitter. The first eight pulses are spaced every 1000 microseconds within the group. The ninth pulse from a master is spaced 2000 microseconds relative to the eight.

2.9 Loran-D Pulse Group. A Loran-D pulse group consists of 16 phase-coded pulses spaced every 500 microseconds.

2.10 Phase Coding. Phase coding consists of inverting the phase of the RF cycle relative to the transmitter frequency standard from pulse to pulse in accordance with the codes specified in the following tables. In these tables, (+) indicates in phase with the frequency standard, and (-) indicates 180° out of phase. During one GRI, Loran-C transmits the GRI-A phase code; then during the next GRI, the GRI-B phase code. This sequence is then repeated. Loran-D transmits GRI-A, GRI-B, GRI-C, and GRI-D in succession and then repeats.

Loran-C Phase Code

MASTER PULSES	
GRI	1 2 3 4 5 6 7 8 9
A	+ + - - + - + - +
B	+ - - + + + + + -

SECONDARY PULSES	
GRI	1 2 3 4 5 6 7 8
A	+ + + + + - - +
B	+ - + - + + - -

Loran-D Phase Code

MASTER PULSES	
GRI	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
A	+ + + + - + - - + + - + + - - +
B	+ + - + - + + - + - + - + + + -
C	+ - + - - - - + + - - - + + - -
D	+ - - - - - + + + + + + + - + +

SECONDARY PULSES
 (Outside Coding Delay
 22,000 - 32,000 Microsecond Range)

GRI	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	+	+	+	-	+	+	+	+	+	-	-	+	-	+	+	+
B	+	-	-	+	+	-	-	-	+	-	+	+	-	+	-	+
C	+	-	+	+	+	-	+	-	+	+	-	-	-	-	+	-
D	+	+	-	-	+	+	-	+	+	+	+	-	-	-	-	-

SECONDARY PULSES
 (Within Coding Delay)
 22,000 - 32,000 Microsecond Range)

GRI	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	+	+	+	-	+	+	+	+	+	+	-	-	-	-	+	-
B	+	+	-	-	+	+	-	+	+	-	+	+	-	+	-	+
C	+	-	+	+	+	-	+	-	+	-	-	+	-	+	+	+
D	+	-	-	+	+	-	-	-	+	+	+	-	-	-	-	-

2.11 Secondary Transmitter Blink. Secondary blink transmissions indicate a malfunction or discrepancy in ground system timing accuracy. All secondaries in a Loran-C chain have a common blink procedure which consists of dropping the first two of the eight secondary pulses for 0.2 to 0.35 second every four seconds. No position shifts of the pulses occur. Secondary transmitters in the present Loran-D chain drop the first four of the sixteen secondary pulses with no "ON" time.

2.12 Loran-C Pulse Shape. The Loran-C pulse is defined as:

$$S(t) = A(t/tp)^c e^{c(1-t/tp)} \sin(2\pi 10^5 t + \phi + \theta),$$

where:

- A - A parameter which is a function of distance from the radiating antenna and of propagation conditions.

- c - A constant, typically 1.5 to 2.0, assigned by appropriate Coast Guard Operation Order. Current value is 2.0.
- t - Time in microseconds.
- tp - Time of pulse peak, typically 60 - 75 microseconds after start of pulse.
- ϕ - The carrier phase relative to the frequency standard which is set to 0 or π depending on phase code.
- θ - Absolute envelope to cycle phase difference $\theta = 2\pi 10^5(ED_o + ED_p) = 2\pi 10^5(ED)$.
- ED_o - Transmitted absolute envelope delay.
- ED_p - Propagated absolute envelope delay.
- ED - Total observed absolute envelope delay at the receiver location.

The term $\sin(2\pi 10^5 t + \phi + \theta)$ represents the carrier and the term $A(t/t_p)^c e^{c(t-t/t_p)}$ represents the modulation, i.e., pulse shape.

2.13 Loran-D Pulse Shape. The Loran-D pulse is defined by the same equation as Loran-C (par. 2.12) with the values of the coefficients set to Loran-D values. The values of the coefficients are currently under consideration by the Air Force.

2.14 Signal Level. Loran signal level is defined as the RMS voltage of a continuous wave signal having the same amplitude as the peak amplitude of the pulse envelope.

2.15 Peak Radiated Power. The peak radiated power of a Loran transmitter is defined as the power of a continuous wave signal having the same amplitude as the peak amplitude of the pulse envelope. The maximum peak radiated power of

existing Loran-C transmitters, when operating under normal conditions, is 250 kilowatts to 3.0 megawatts. Future Loran-C transmitters/antennas are not expected to exceed 3.0 megawatts peak power. The maximum peak radiated power of existing Loran-D transmitters is 10 kilowatts. Future Loran-D transmitters may radiate substantially more power; 30 kilowatts is currently under discussion in connection with the procurement of new Loran-D equipment.

2.16 Signal-to-Noise Ratio. Signal-to-noise ratio is defined as the square root of the ratio of the power of a continuous wave signal having the same peak-to-peak amplitude as the RF cycles at the peak of the Loran pulse, to the power of the noise signal as measured through a single pole LC band-pass filter of unity gain at 100 kHz and 3dB bandwidth of $20 \text{ kHz} \pm 0.5 \text{ kHz}$.

2.17 Signal-to-Interference Ratio. Signal-to-interference ratio is defined as the square root of the ratio of the power of a continuous wave signal having the same peak-to-peak amplitude as the RF cycles at the peak of the Loran pulse, to the power of the interfering signal.

2.18 Continuous Wave Interference (CWI). CWI includes both unkeyed and keyed signals. Keyed CWI transmits data at a rate of 50 to 100 bits per second with a duty factor of 50%.

2.18.1 Frequency Shift Keying (FSK). FSK signals are considered to be the equivalent of two keyed CWI signals at different frequencies.

2.18.2 Non-Synchronous Interference. Non-synchronous CWI refers to any interfering CW frequency that does not coincide with a spectral line of the Loran pulse. Non-synchronous frequencies include sub-synchronous frequency operation. Both odd and even sub-synchronous frequencies apply. Odd sub-synchronous frequencies are defined as any frequency which appears in the same phase every odd integer of 3 or more repetition rates (3, 5, 7, etc.) Even sub-synchronous frequencies are defined as any

frequency which appears in the same phase every even integer of 4 or more repetition rates (4, 6, 8, etc.).

2.18.3 Synchronous Interference. Synchronous CWI refers to any interfering CW frequency which has a frequency that coincides with one of the spectral lines of the Loran transmission. Odd synchronous interference refers to any interfering frequency that coincides with one of the spectral lines in the transmission of the odd numbered pulses of a pulse group. Even synchronous interference refers to any interfering frequency that coincides with one of the spectral lines of the transmission of the even numbered pulses of a pulse group.

2.19 Search and Settle Time. Search and settle time is defined as the total time necessary after warmup to acquire Loran groundwave signals and provide correct position information in Loran time differences, including any validation time required after the "final" adjustment on each signal.

2.20 Envelope-to-Cycle Delay (ECD). ECD is defined to be the difference in phase of the carrier of the Loran pulse, θ , relative to the phase of the Loran pulse (as defined in par. 2.12) when $\theta = 0$ multiplied by $2\pi 10^5$.

2.21 Differential ECD. Differential ECD is defined to be ECDS-ECDM where ECDM is defined to be ECD of the master and ECDS is the ECD of the secondary.

2.22 Atmospheric Noise. Atmospheric noise consists of the sum of three types of noise as follows:

1. isolated impulses of relatively high amplitude and relatively rare occurrence;

2. randomly occurring bursts of impulses during which time the impulses are of random amplitude and random spacing but generally of lower amplitude and much higher occurrence rate than the isolated impulses; and

3. still lower amplitude, but continuous Gaussian noise.

All impulses which form noise types 1 and 2 are approximately rectangular in shape and have a time width of 14.3 ± 1.0 microseconds in order to deliver nearly constant spectral density of a band-pass filter tuned to 100 kHz. The following description indicates relative amplitude levels and probability of occurrence of all noise generators making up the three types of noise. The absolute levels are related to the reference level through the signal-to-noise ratio and the signal level.

<u>Relative Amplitude, dB</u>		<u>Probability of Occurrence</u>
0	} Isolated impulses (type 1)	2E-20
-8		2E-17
-17		2E-14
-28		2E-11
-38		2E-9
-51		2E-7
-60		2E-6
-10	} Highest levels within bursts of impulses (type 2) having 10dB spread within each burst.	2E-7
-16		2E-6
-21		2E-5
-25		2E-4
-28		2E-3
-30		2E-2
-66	Gaussian (type 3)	Continuous

2.23 Communication. Some Loran-C chains are used for communication at a low data rate by means of phase modulation from pulse to pulse. There are two types of modulation:

1. Clarinet Pilgrim Loran Communications
 - a. $\pm 30^\circ$ to $\pm 45^\circ$ phase shift
 - b. Six and eight pulses modulated
 - c. All transmitters modulated identically each GRI.
2. Coast Guard Loran Communications
 - a. $\pm 27^\circ$ phase shift
 - b. Eight pulses modulated
 - c. One transmitter modulated or all transmitters modulated identically each GRI.

2.24 Cross Rate Signals. Cross rate signals are signals from transmitters operating at pulse repetition intervals different from that of the desired Loran signals. The effect of these cross rate signals is to occasionally be coincident with the desired signals. When the desired rate and cross rate group repetition intervals have no common multiples of 100 microseconds, the effect of the cross rate signal is minimized. For design purposes, one crossing rate signal may be assumed to be present and equal in amplitude to the highest level signal being tracked, and the chain rate of this crossing rate signal is to be incoherent with the chain rate of the signals to be received (i.e., there is no common multiple of 100 microseconds in the group repetition intervals).

2.25 Electronic Countermeasures (ECM). When Loran is used for military purposes, unfriendly forces may attempt to degrade the performance capability of Loran user equipment by intentionally radiating interfering signals. There are three ECM options open to them:

1. Radiate noise in the 90-110 kHz band.
2. Radiate CW interference.
3. Radiate "false" Loran signals.

Whether unfriendly forces would resort to ECM, or what form it would take, is not known.

2.26 Signal Velocity and Acceleration. The maximum rate of change of the time arrival of a Loran pulse from any of the transmitters of a chain is ± 2 microseconds per second. The maximum rate of change of the rate of change of the time of arrival is ± 0.2 microsecond per second per second. These values correspond to an aircraft flying at a true air speed of 600 meters per second toward or away from a transmitter and making at least a 90° , 6 g turn. Since the baselines formed by three transmitters of an operational triad never form a straight line, these maximums are never realized simultaneously with respect to all three transmitters.

2.27 Loran Signal Levels. The signal levels, as measured at the terminals of a receiving antenna, range from 2.7 microvolts to 0.27 volts. The maximum signal level differential between the received signals of any two transmitters is 100 dB. Skywaves may be present having a minimum delay of 35 microseconds and 6 dB greater peak amplitude than the groundwave. Skywaves may be present having a delay of 50 to 60 microseconds and a 14 dB greater peak amplitude than the groundwave.

3. RADIO FREQUENCY UNIT (RFU)

The RFU includes the antenna coupler, band-pass filter, signal canceller, step attenuator, band-pass amplifier, and the required cabling to connect these sections to the antenna, to each other as required, to the Digital Measurement Unit (DMU), and to the computer.

3.1 Phase Distortion. The goal of measuring time differences with less than a 10 nanosecond standard deviation (par. 1) places stringent requirements on phase distortion during signal processing. Consequently, it is required that the time delay through the RFU not vary more than 2 nanoseconds while the signal level varies throughout its range for any frequency between 90 and 110 kHz.

3.2 Antenna Coupler. The antenna coupler is contained in a separate chassis that can be mounted close to the output terminals of the receiving antenna. Its primary purpose is to match the impedance of the antenna to the follow-on cabling so that subsequent noise contamination of the desired signal during transmission is negligible.

3.2.1 Input Signal Voltage Limits. The voltage level of the input Loran signal to the antenna coupler is the level indicated in par. 2.27, attenuated by a minimal length of connecting cable. Typical installations place the antenna coupler within 3 feet of the antenna terminals. The input signal level due to atmospheric noise, such as lightning and precipitation static, is a large but unknown number of dB greater than the maximum Loran signal level.

3.2.2 Gain. The antenna coupler voltage gain is to be 10 to overcome noise contamination during signal transmission to the next section of the RFU and to match the next section input level requirements. The antenna coupler must be capable of driving up to 100 feet of cable.

3.2.3 Impedance Match. The antenna coupler input impedance is to be $30 \mu\Omega$ in parallel with $500 K\Omega$. This impedance is not intended to match the antenna reactance but to present a light load to the antenna and maintain a high signal voltage level. The antenna coupler output impedance is to be 100Ω and is to be capable of driving a 100Ω balanced transmission line.

3.2.4 Saturation Characteristics. Atmospheric noise can be expected to drive the antenna coupler into saturation. It is required that the coupler recover from saturation within 2 microseconds.

3.3 Band-pass Filter. The function of the band-pass filter is to pass the desired Loran-C signals and attenuate signals outside the Loran-C signal bandwidth. The total frequency bandwidth of the RFU and the out-of-band attenuation rate are the sums of the band-pass filter characteristics and the band-pass amplifier characteristics.

3.3.1 Bandwidth. The band-pass filter bandwidth (3 dB) is 85 kHz to 117 kHz.

3.3.2 Ripple in Pass-band. The ripple in the pass-band is to be less than 1 dB.

3.3.3 Out-of-Band Attenuation Rate. The out-of-band attenuation rate is to be such that at least 15 dB attenuation is achieved at 80 kHz and 125 kHz.

3.4 Signal Canceller. The function of the signal canceller is to attenuate undesired CW and FSK signals within a frequency range of 80 kHz to 125 kHz. One signal canceller is required for each interfering signal.

3.4.1 Signal Amplitude Range. The signal canceller is to be effective against undesired signals with amplitudes between 100 μ V and 100 mV RMS measured at the antenna coupler input.

3.4.2 Signal Attenuation. The signal canceller is to provide at least 30 dB attenuation of the undesired signal after the amplitude (CW signal) or frequency (FSK signal) transient is over.

3.4.3 Operation. The signal canceller time of operation is to be controlled by the computer. During operating time, the signal canceller will automatically search and phase lock to the interfering signal.

3.5 Step Attenuator. The RFU total gain is controlled by a step attenuator. The step attenuator attenuation level is to be controlled by the computer.

3.5.1 Range. The step attenuator is to be capable of any attenuation between zero and 100 dB in 1 dB steps.

3.5.2 Switching Time. The time required to change attenuation from one level to another is to be 1 ms or less.

3.5.3 Frequency Range. The frequency range of operations is to be DC to 100 MHz.

3.6 Band-pass Amplifier. The function of the band-pass amplifier is to provide most of the voltage gain and half the frequency selection required in the RFU.

3.6.1 Gain. The band-pass amplifier voltage gain is to be at least 10^5 .

3.6.2 Output Signal. The maximum output signal required is 2 V RMS.

3.6.3 Bandwidth. The band-pass amplifier bandwidth (3 dB) is to be 85 kHz to 117 kHz.

3.6.4 Ripple in Passband. The ripple in the passband is to be less than 1 dB.

3.6.5 Out-of-Band Attenuation Rate. The out-of-band attenuation rate is to be such that at least 15 dB attenuation is achieved at 80 kHz and 125 kHz.

4. DIGITAL MEASUREMENT UNIT

The function of the Digital Measurement Unit (DMU) is to digitize samples of the RFU waveform at selected times and transfer these sample values via a direct memory access channel to tables in the computer memory. The computer processor controls the DMU function by providing the following outputs to data files in the DMU: required time intervals, mode sequence words, memory table addresses, and memory table block lengths. The DMU uses the time interval and mode sequence data to preset a synchronous digital clock driven by the stable oscillator, to control an analog-to-digital converter sample timing, and to control the operation of a measurement processor. The output of the measurement processor representing in-phase (I) and quadrature (Q) components of the RF waveform is then sent to the computer memory using the data in the memory address and memory block length files. The DMU shall allow multiple sample measurements within submillisecond intervals while keeping computer input-output overhead to less than 1%. Sufficient information shall be

accepted by the DMU data files so that the computer need not update these files at intervals of less than 10 milliseconds.

4.1 Analog Signal Voltage Limits. The input voltage range is to be +5 to -5 volts.

4.2 Modes. The DMU is to operate in at least three modes: Search, Settle, and Track. The principal distinctions are that in the search mode the I and Q output data are the pre-processed sums of the voltage measurements of ten consecutive cycles of the signal. In the settle mode, the output data are the voltage measurements of four consecutive cycles. In the track mode, the output data are the voltage measurements of each cycle.

4.3 Measurements. The measurements consist of sampling the signal in such a way that the I and Q components can be determined for at least four consecutive cycles in the settle mode, and for ten consecutive cycles in the search mode. In the settle and track modes, the I and Q measurements of each cycle are to be converted to binary numbers for transfer to the processor, and these binary numbers are to be scaled to the analog voltages in such a way as to allow the resolution of time to about 2.5 nanoseconds. Positioning of the measurements with respect to the signal in any mode is to be controlled by the computer processor. In the search mode, the summed measurements of ten consecutive cycles pre-processed to produce I and Q will be converted to binary form for transfer to the processor.

4.4 Oscillator. The measurement sequences are to be controlled by an oscillator having a frequency of $51.2 \text{ MHz} \pm 1 \text{ Hz}$. This oscillator must not vary in frequency more than 1 part in 10^9 over a period of 4 seconds nor more than 1 part in 10^8 per day.

5. COMPUTER CONTROL, AND DISPLAY UNIT

The Computer Control and Display Unit consists of a digital computer with appropriate memory components, control and indicator components, and the components required to satisfy the interface

requirements of navigation guidance instruments and/or autopilots. The Phase 1 Super Receiver/Navigator design does not include the output interface components, these will be deferred until the instruments and autopilot are defined in connection with the next development phase.

5.1 Computer Algorithms. The program of computations to be performed by the computer will consist of a Control Program and a library of subroutines. These subroutines are Search, Settle, Track, Station Identification, Newtrack, Navigate, and Warnings.

5.1.1 Control Program. The Control Program will call the next subroutine to be executed and specify its initial conditions. It also accepts and stores the initial conditions imposed by external sources and monitors lists of data pertinent to the various functions being executed, e.g., a file of stations in track together with pertinent data. Control signals will be generated to control the signal canceller, the step attenuator, and the DMU. The signal canceller will have three operational states: off, on with Loran signals present, and on with Loran signals absent. On or off will be decided by analysis of the data rejected by Track. The two states of "on" will be controlled by the DMU. The step attenuator will be controlled on the basis of the expected value of I for each signal in track. The Control Program will specify the mode of the DMU and position the measurement gates for each signal in track at the best estimate of the time of arrival of the next signal.

5.1.2 Search. The first subroutine to be called by the Control Program is Search. Search will detect and locate the Loran pulse groups having the required GRI with respect to the local clock. Search is to be completed in the minimum practicable time. Whenever the Search subroutine has located any one of the desired Loran pulse groups, it calls for the Settle subroutine to be initiated with respect to that group. The receiver will operate in the search, settle, and track modes sequentially, as required, with respect to different transmitters of the chain identified by the GRI.

5.1.3 Settle. The Settle subroutine will identify the groundwave and the desired cycle to be tracked and will adjust the timing of the initiation of the measurement sequence generator to establish tracking of the zero crossing of the cycle to be tracked.

5.1.4 Track. Raw data will be edited with respect to both I and Q. If the value of either I or Q of a related pair violate the criterion for goodness, the IQ pair will be rejected. The initial criterion for goodness following receiver turn-on will be "less than a fixed value". Subsequently, this value will be adjusted, based on an assessment of the immediate past performance of the receiver. A lower limit will be placed on the threshold so that the receiver will not reject data because of aircraft maneuver. When called by the Control Program, the Track subroutine produces the best estimates of the time of arrival of the Loran signal.

5.1.5 Station Identification. When three or more signal tracks are established, each track will be labeled with a standard designator indicating that the signal originates from station M, U, V, W, X, Y, or Z. Identification will be based on the computation of the receiver's known initial position from the measured time differences.

5.1.6 Newtrack. As the aircraft flies through a chain, signals currently in track will fade. When the Control Program calls, Newtrack will position the Settle sample points on the stations of the chain which are not in track so that stations can be tracked to replace those which have faded.

5.1.7 Navigate. Horizontal navigation computations will be made in accordance with Ref. 5. The fixed course mode has been included in the Phase 1 development. Other modes given in Ref. 5 will be included in later phases as required. Navigation will be accomplished by steering a pre-selected course with the aid of computed cross track error and its time rate, along track distance to go and its time rate, and the heading error. Time difference for the Loran transmitters

designated by the Control Program for navigation will be computed. These time differences will be adjusted so as to apply to the simultaneous arrival of signals from all transmitters.

5.1.8 Warnings. A warning subroutine will be produced in the later development phases. Warning signals will be generated which indicate at least the following: Internal Malfunction, Transmitter Malfunction, Jamming, Skywave, and Not Ready. Other warnings may be added during development.

5.2 Control Indicator. The requirements for the control indicator appropriate to later development phases will be determined at a later date.

Appendix B

RADIO FREQUENCY UNIT DESIGN

INTRODUCTION

Figure B-1 shows the functional block diagram of the Radio Frequency Unit (RFU). The designs and specifications of the RFU are presented in this appendix.

ANTENNA COUPLER

The antenna coupler amplifies signals received from the antenna and outputs the signals to a balanced 100 Ω transmission line. A block diagram with specifications is shown in Fig. B-2. A limiter preceding the amplifier provides protection from high impulse signals. The balanced transmission line provides low loss signal transmission with protection against contamination from undesired local signals. The antenna coupler input impedance is designed to operate with high impedance type antennas. Power for the preamplifier is supplied through the transmission line.

BAND-PASS FILTER

The band-pass filter shown in Fig. B-3 provides attenuation of undesired signals outside the Loran-C signal bandwidth. The band-pass filter also provides for transmission line termination and amplification to compensate for losses associated with the band-pass filter.

SIGNAL CANCELLER

The signal canceller (Fig. B-4) is a phase lock device which operates to attenuate undesired signals within the Loran-C signal bandwidth. Table B-1 gives the signal canceller specifications. In operation, the signal canceller phase locks to the undesired signal, adjusts the voltage controlled oscillator output signal to the proper amplitude.

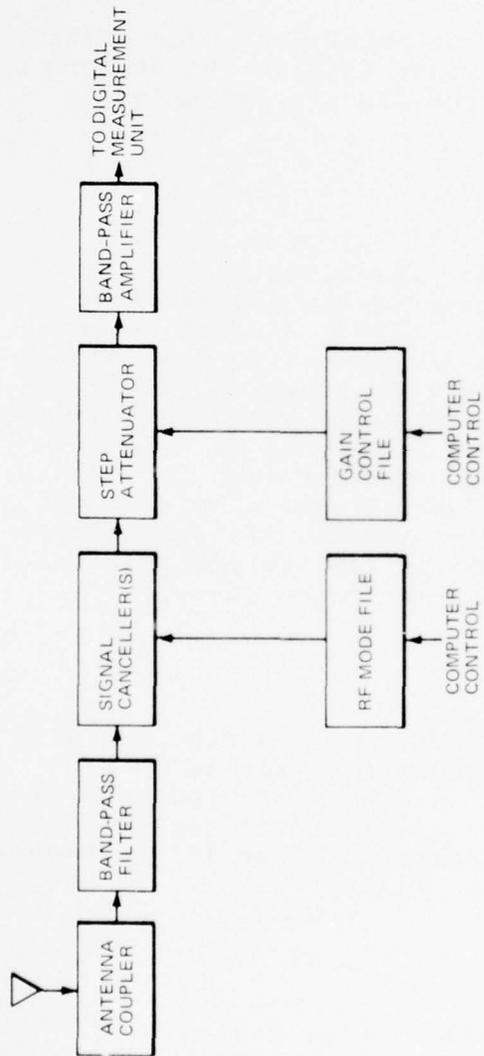
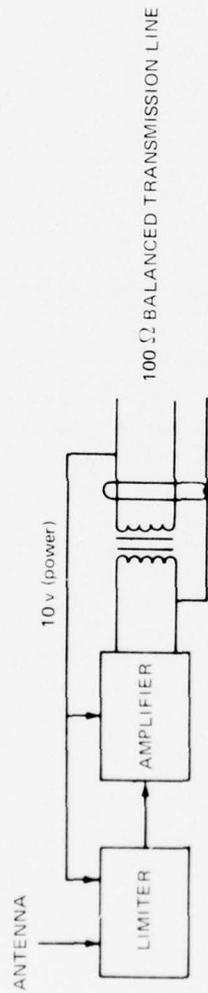


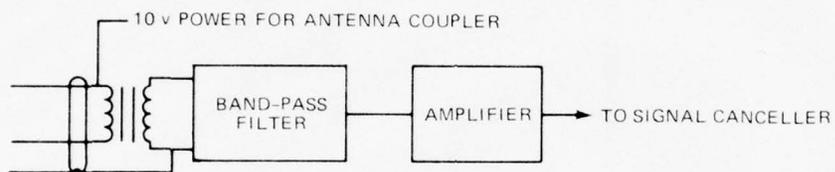
Fig. B-1 RADIO FREQUENCY UNIT BLOCK DIAGRAM



SPECIFICATIONS

- INPUT SIGNAL RANGE: 2.7 μV TO 0.27 VRMS (LORAN-C SIGNAL)
- VOLTAGE GAIN: 10
- NOISE FIGURE: < 5 dB
- BANDWIDTH: 70 KHz TO 140 KHz (3 dB)
- INPUT IMPEDANCE: 30 μΩ IN PARALLEL WITH 500 K Ω
- OUTPUT IMPEDANCE: 100 Ω (SUITABLE FOR DRIVING 100 Ω TRANSMISSION LINE)
- LIMITER OPERATING VOLTAGE: ± 3 VOLTS

Fig. B-2 ANTENNA COUPLER BLOCK DIAGRAM AND SPECIFICATIONS



SPECIFICATIONS

INPUT IMPEDANCE: 100Ω (TO MATCH BALANCED 100Ω TRANSMISSION LINE)

OUTPUT IMPEDANCE: 300Ω

VOLTAGE GAIN: 1.0

BANDWIDTH: 85 KHz to 117 KHz (3 dB POINTS)

SKIRT CHARACTERISTICS: ATTENUATION GREATER THAN 20 dB BELOW 80 KHz
AND ABOVE 125 KHz

RIPPLE IN BAND-PASS: < 1 dB PEAK TO PEAK

Fig. B-3 BAND-PASS FILTER BLOCK DIAGRAM AND SPECIFICATIONS

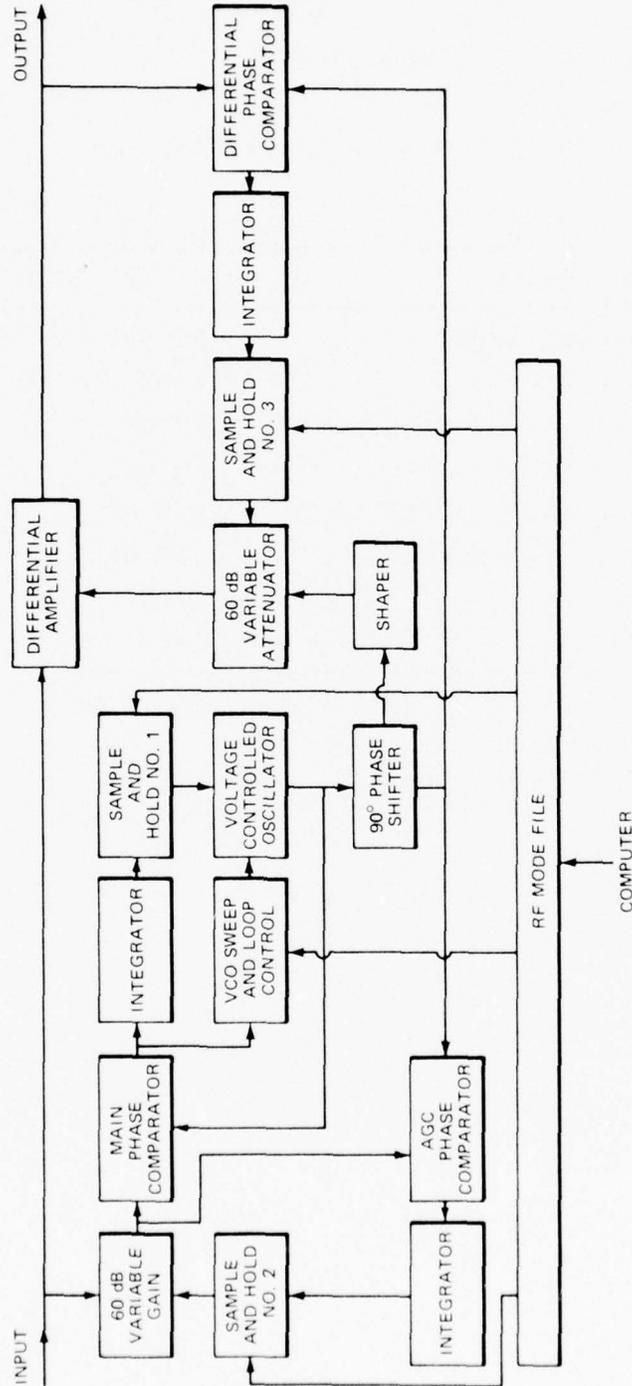


Fig. B-4 SIGNAL CANCELLER BLOCK DIAGRAM

Table B-1

Signal Canceller Specifications

Parameter	Specification
Operating Frequency Range	80 kHz to 125 kHz
Signal Amplitude Range	1 mV RMS to 1 V RMS
Undesired Signal Attenuation	30 dB
Desired Signal Attenuation	0 dB
Loop Bandwidth for 50 Hz FSK Signal	500 Hz
Loop Bandwidth for AM Signal	15 Hz
Input Impedance	1100 Ω
Output Resistance	50 Ω

and differentially amplifies this signal with the undesired input to produce signal cancellation at the output. The RF mode file stores computer generated information which controls the time and mode of signal canceller operation. A detailed description of the signal canceller follows.

The input to the signal canceller is frequency limited to a 85 kHz to 117 kHz bandwidth by the band-pass filter. At 80 kHz and 125 kHz, the signals are attenuated at least 15 dB. When an undesired signal occurs within this bandwidth, the computer commands the signal canceller to operate. The voltage controlled oscillator (VCO) sweep and loop control circuit causes the VCO frequency to sweep the 80 kHz to 125 kHz frequency range. When the VCO frequency is coincident with the undesired frequency, the main phase comparator output frequency becomes zero. This causes the VCO sweep and loop control circuit to stop the VCO sweep and the VCO to phase lock to the undesired signal. The VCO phase locks to the undesired signal through the main phase comparator, integrator, and sample and hold No. 1. The integrator sets the loop bandwidth and sample and hold No. 1 operates in the sample mode (a simple amplifier) as commanded by the computer. Because of the main phase comparator manner of operation, the VCO output signal is 90° out of phase from the input signal. The 90° phase shifter restores the VCO output signal to the input signal phase.

The 90° phase shifter output is applied as a reference to the automatic gain control (AGC) phase comparator. The AGC phase comparator, integrator, sample and hold No. 2, and the 60 dB variable gain form a loop to hold the main phase comparator input signal amplitude constant even though the signal canceller input signal may vary over a 60 dB range. A constant amplitude is required at the main phase comparator input for proper phase lock loop operation. The integrator sets the AGC time constant. Sample and hold No. 2 operates in the sample mode (a simple amplifier) as commanded by the computer. The 90° phase shifter output signal, which is triangular in shape, is applied to a shaper where the triangular wave is shaped into a sine wave. The sine wave is applied

to the differential amplifier through the 60 dB variable attenuator. The signal canceller input signal is applied to the second differential amplifier input. Because the two differential amplifier input signals are in phase and a signal difference is taken in the differential amplifier, the differential amplifier output is a sine wave smaller than either of the two input signals. However, the output signal phase may be either in phase or out of phase with the signal canceller input signal depending on which of the two differential amplifier input signals is larger.

When the 60 dB variable attenuator output signal is larger than the signal canceller input signal, the differential amplifier output signal is out of phase with the signal canceller input signal. This out of phase signal is compared with the 90° phase shifter output signal producing a negative signal at the differential phase comparator output. This negative signal is applied to the 60 dB variable attenuator control input through an integrator and sample and hold No. 3, and reduces the 60 dB variable attenuator output signal. When the 60 dB variable attenuator output signal amplitude is reduced to the signal canceller input signal amplitude, the differential amplifier output amplitude approaches zero and no further correction to the 60 dB variable attenuator control is made. The integrator controls the reaction time in this amplitude control loop and sample and hold No. 3 operates in the sample mode (a simple amplifier) as commanded by the computer. When the two signals applied to the differential amplifier inputs are equal in phase and amplitude, the differential amplifier output, which forms the signal canceller output, is zero and the undesired signal canceller input signal is cancelled. In practice, the output signal can only approach zero since some error must exist in the phase loop and amplitude loop operation.

Only the operation of the signal canceller with regard to a single undesired signal has been described thus far. In actual use, the signal canceller must operate in the presence of the desired Loran-C signal which could influence the cancelling action on the undesired signal. Therefore, the

signal canceller operating mode is changed during the Loran-C pulse reception time. A description of this mode of operation follows.

After the settle mode is completed, a computer control signal is available to command the signal canceller to ignore any further input signals including Loran-C pulse reception. Timing diagrams shown in Fig. B-5 indicate the relationship between the Loran-C pulse, the undesired signal, and the computer control signal.

Assume that the signal canceller is phase locked to the undesired signal and cancellation has occurred. When a Loran-C pulse is received, the main and differential phase comparator output signals could include some of the Loran-C signal thereby causing disturbance of the phase and amplitude loops and a reduction of the amount of undesired signal cancellation. In order to prevent a reduction of undesired signal cancellation, all sample and hold circuits are commanded by the computer, through the RF mode file, to the hold mode a few microseconds before the beginning of the Loran-C pulse. Therefore, the 60 dB variable attenuator output signal is held at the same phase and amplitude as observed at the end of the sample mode and cancellation of the undesired signal is maintained. When the Loran pulse has ended, the sample and hold circuits are commanded back to the sample mode and any errors that may have accumulated in the phase or amplitude loops are corrected. The sequence is repeated for the next Loran pulse.

BREADBOARD SIGNAL CANCELLER

During Phase 1, a breadboard model of a signal canceller without computer control capability was constructed and tested. A photograph of the signal canceller is shown in Fig. B-6, and schematic diagrams of the breadboard are shown in Figs. B-7 through B-15. After circuit adjustments were completed, a test of the signal canceller response to several fixed frequency signals was made. A block diagram of the test condition is shown in Fig. B-16. The test signal amplitude

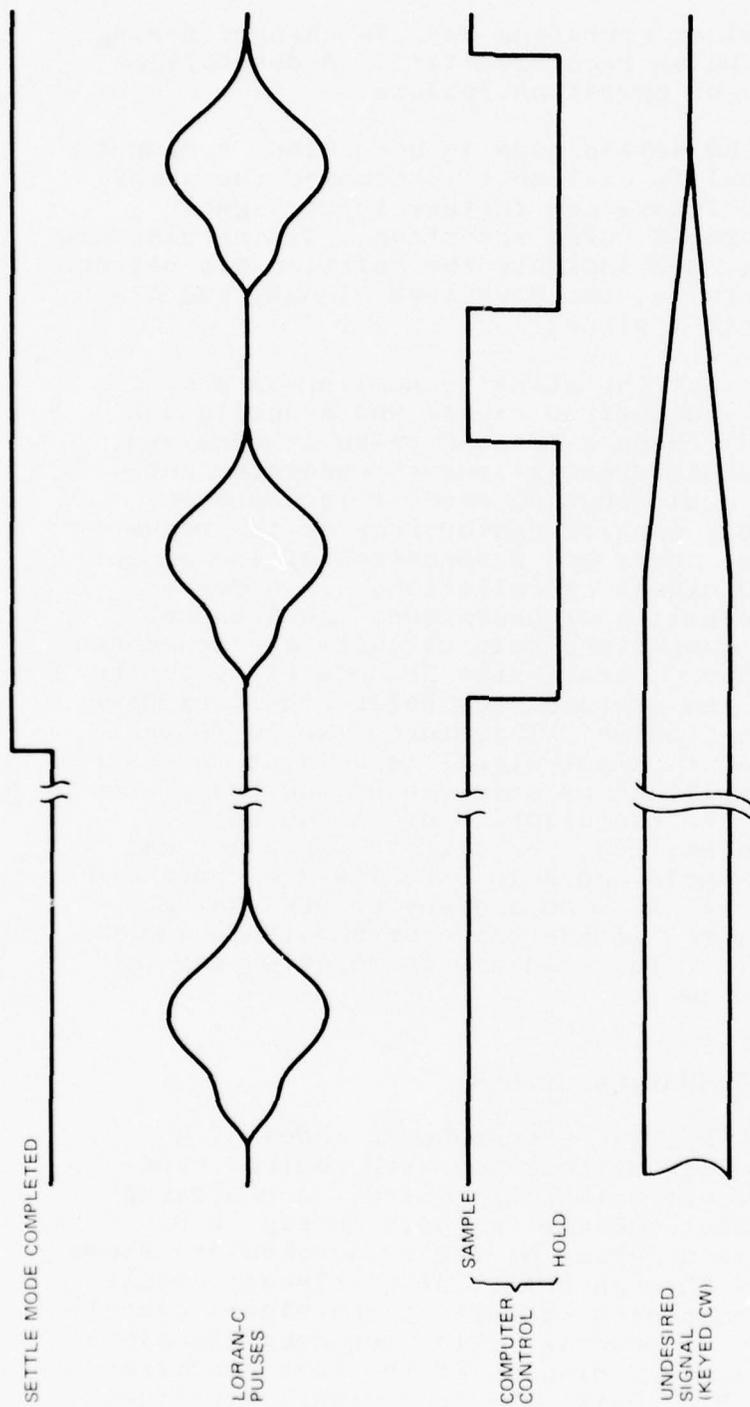


Fig. B-5 SIGNAL CANCELLER TIMING DIAGRAM

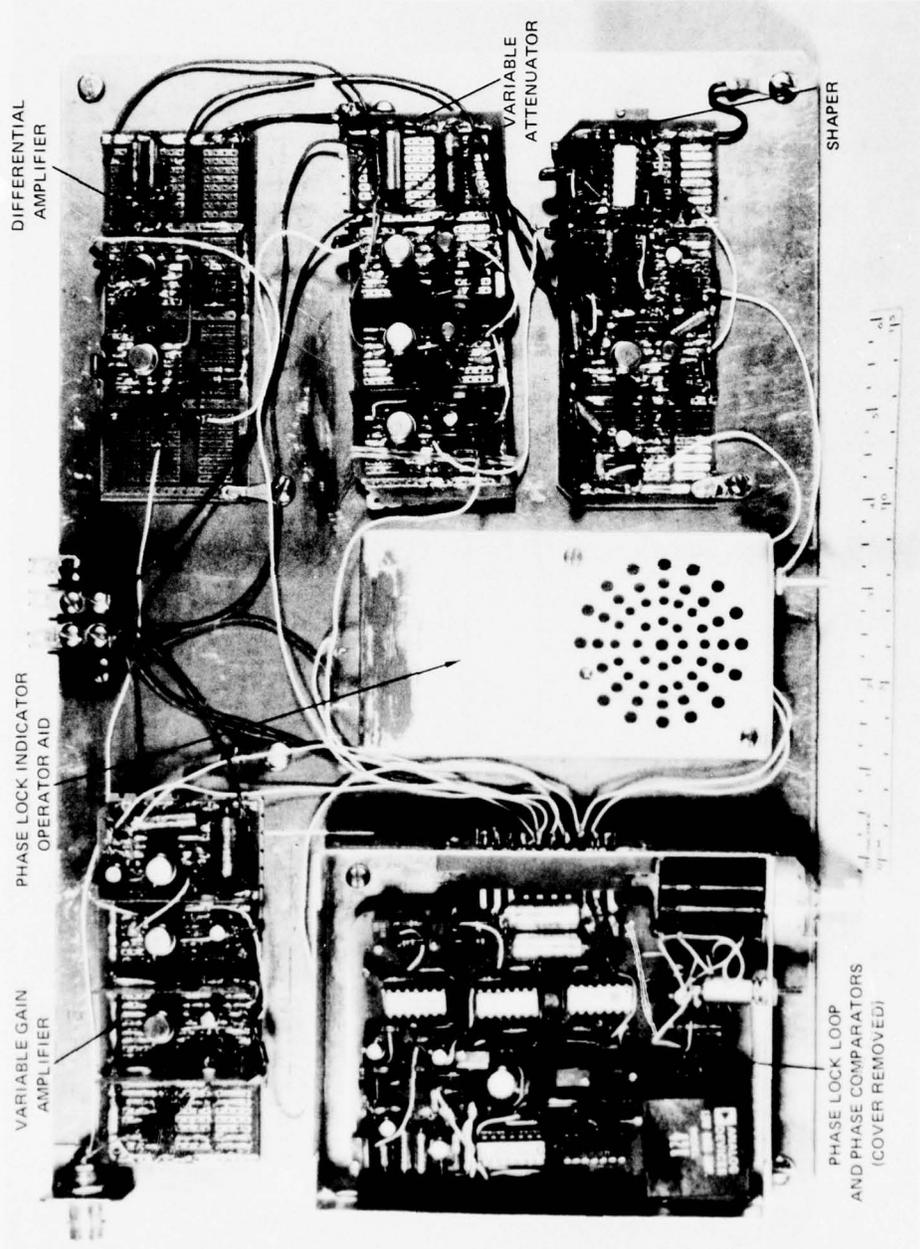


Fig. B-6 SIGNAL CANCELLER BREADBOARD

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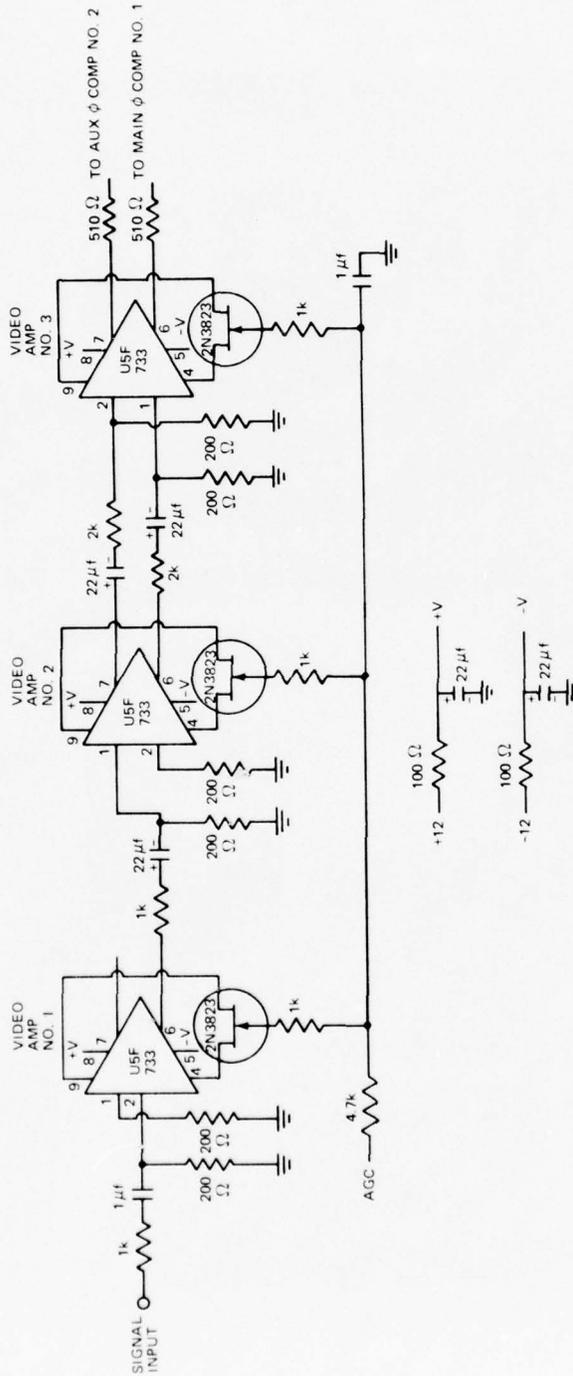


Fig. B-7 60 dB AMPLIFIER

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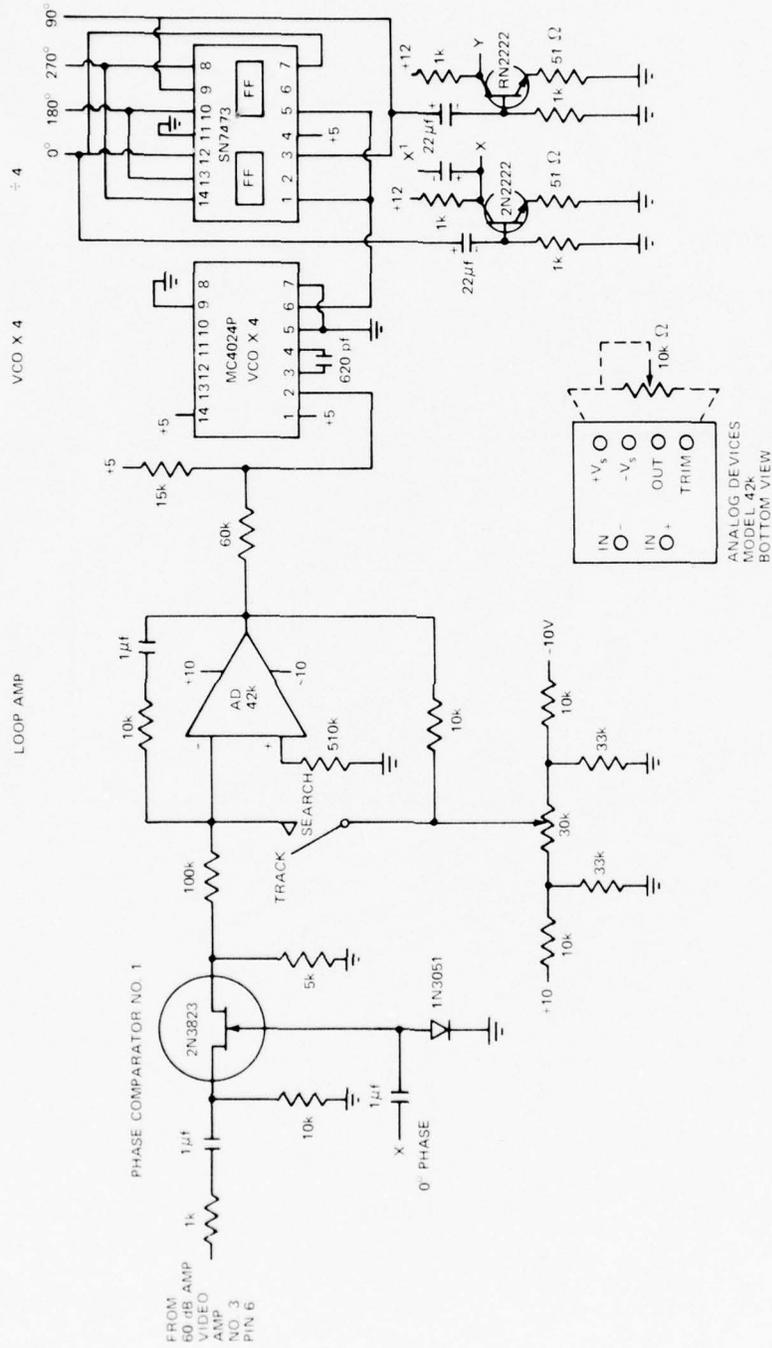


Fig. B-8 MAIN PHASE LOCK LOOP

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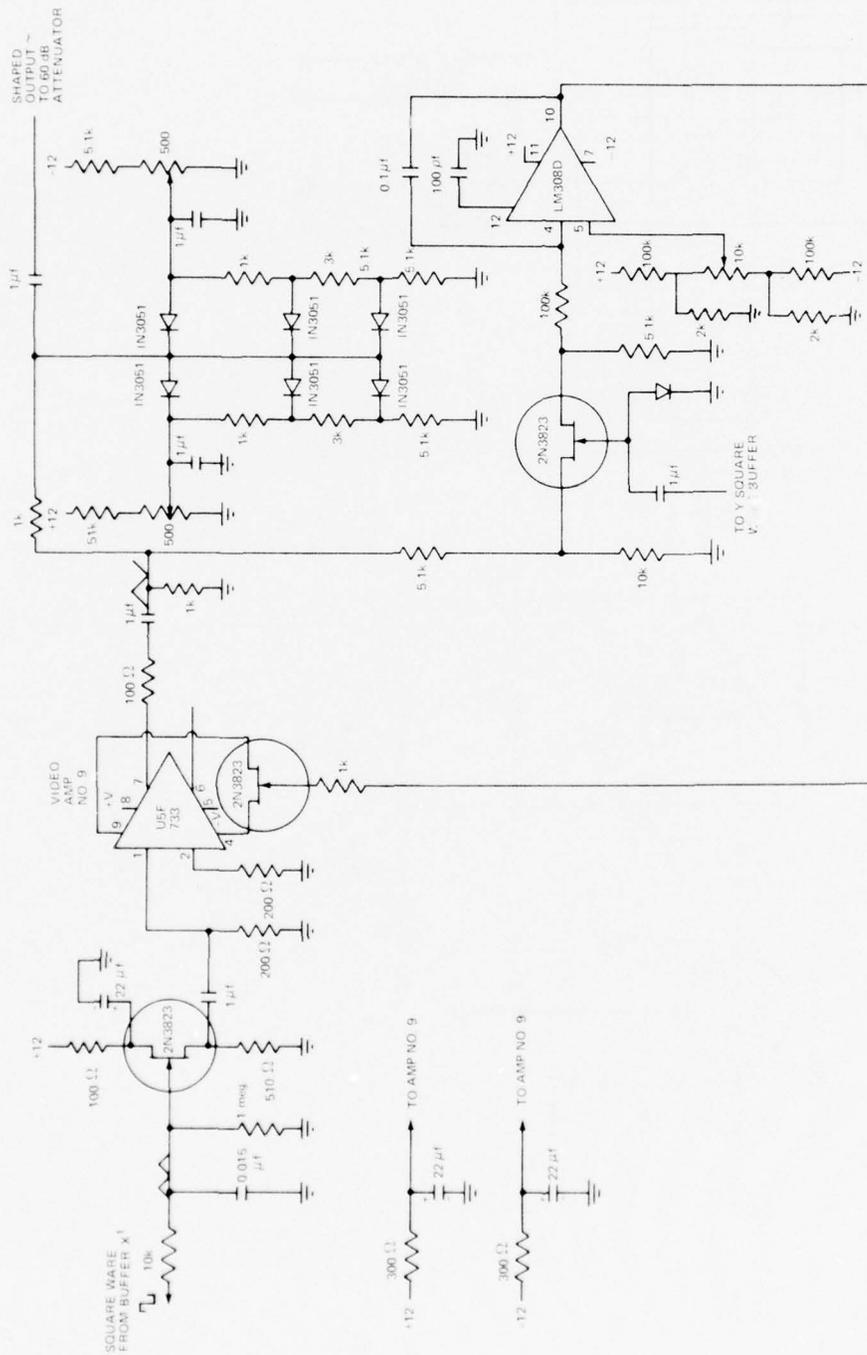


Fig. B-9 SHAPER

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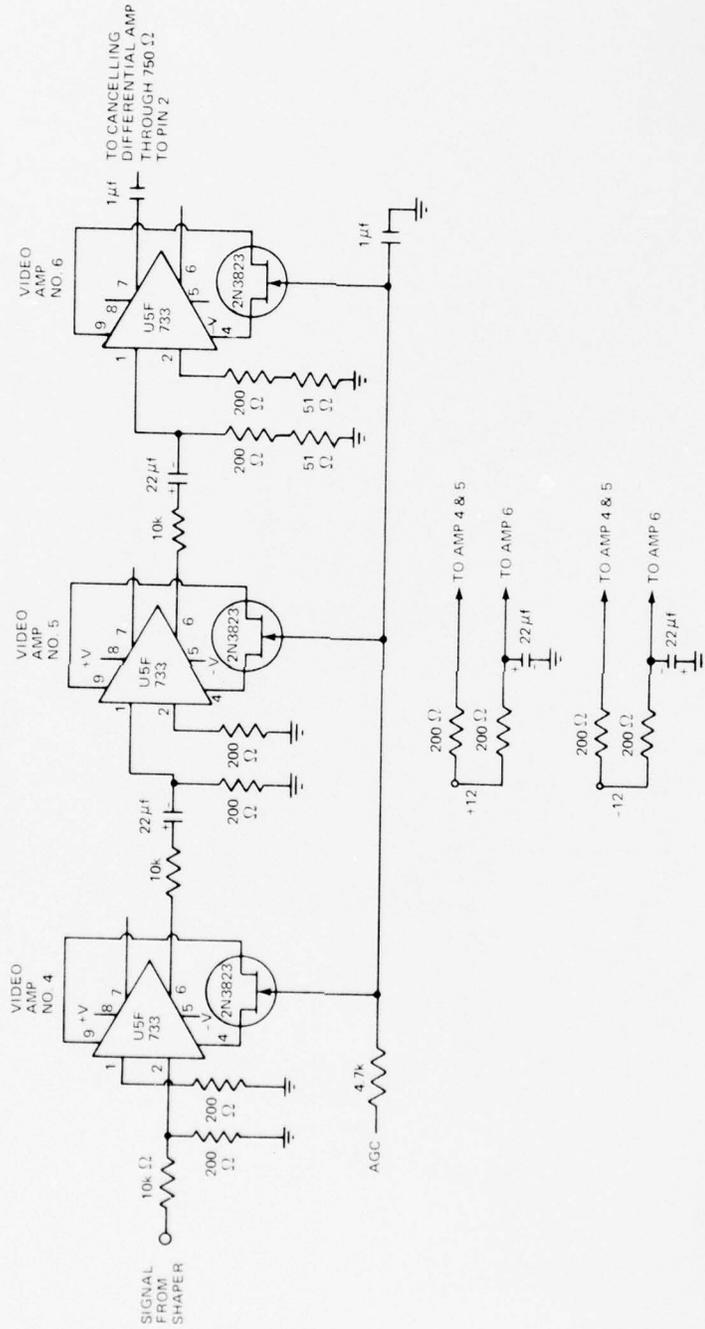


Fig. B-10 60 dB ATTENUATOR

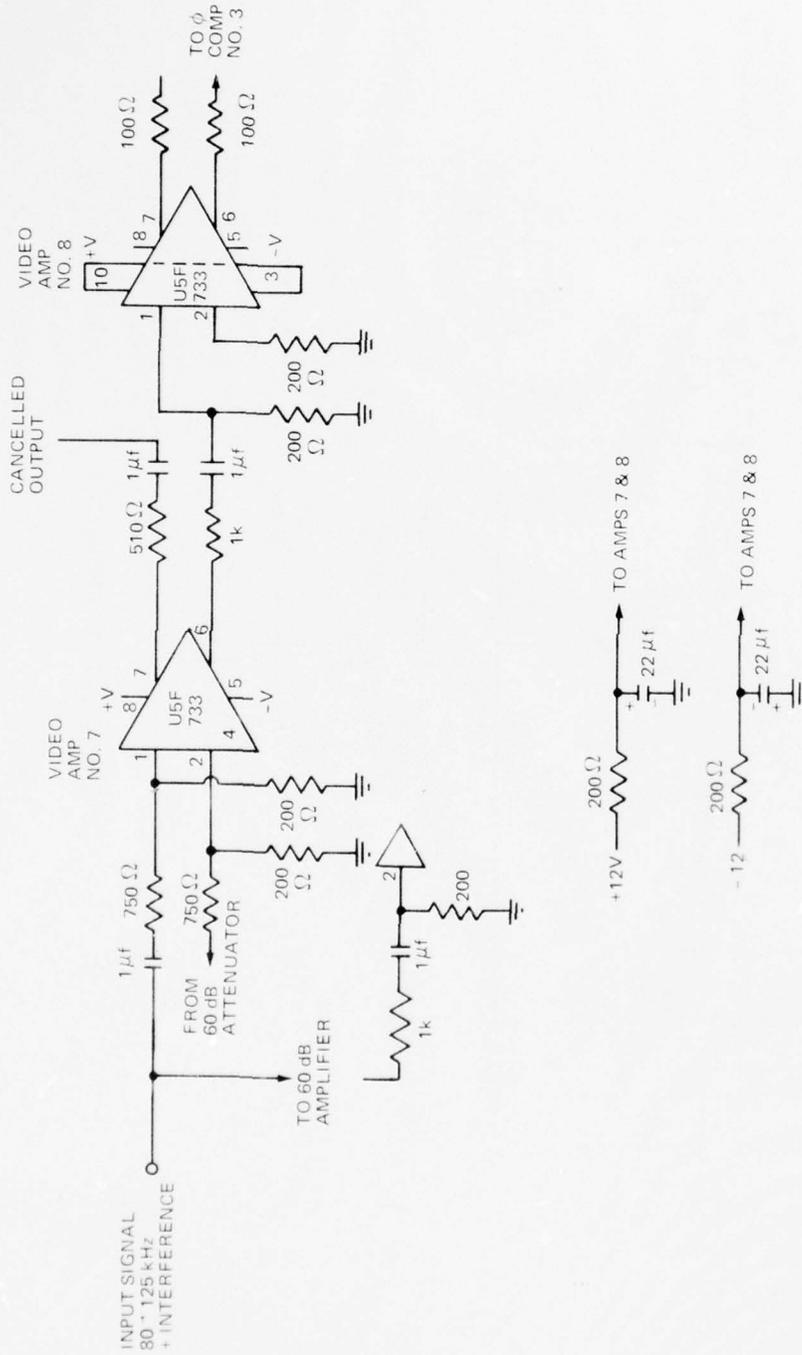


Fig. B-11 DIFFERENTIAL AMPLIFIER AND 20 dB GAIN AMPLIFIER

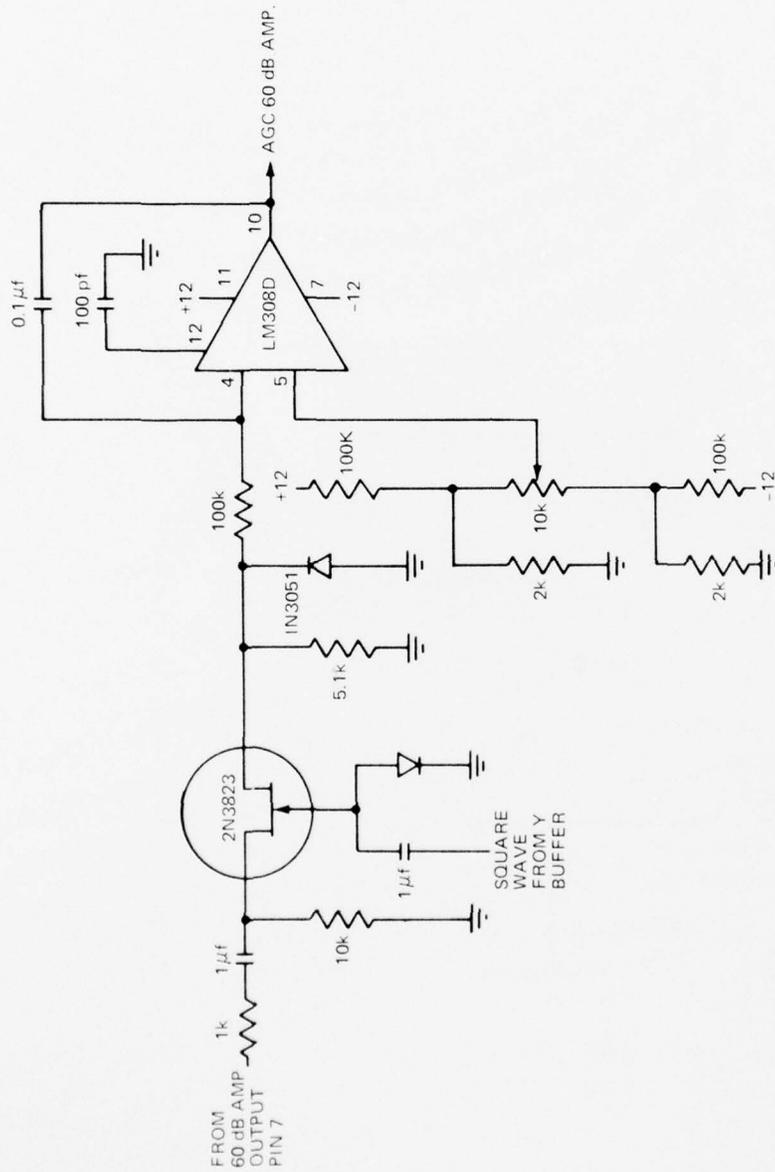


Fig. B-12 AGC FOR 60 dB AMPLIFIER AUXILIARY PHASE COMPARATOR NO. 2

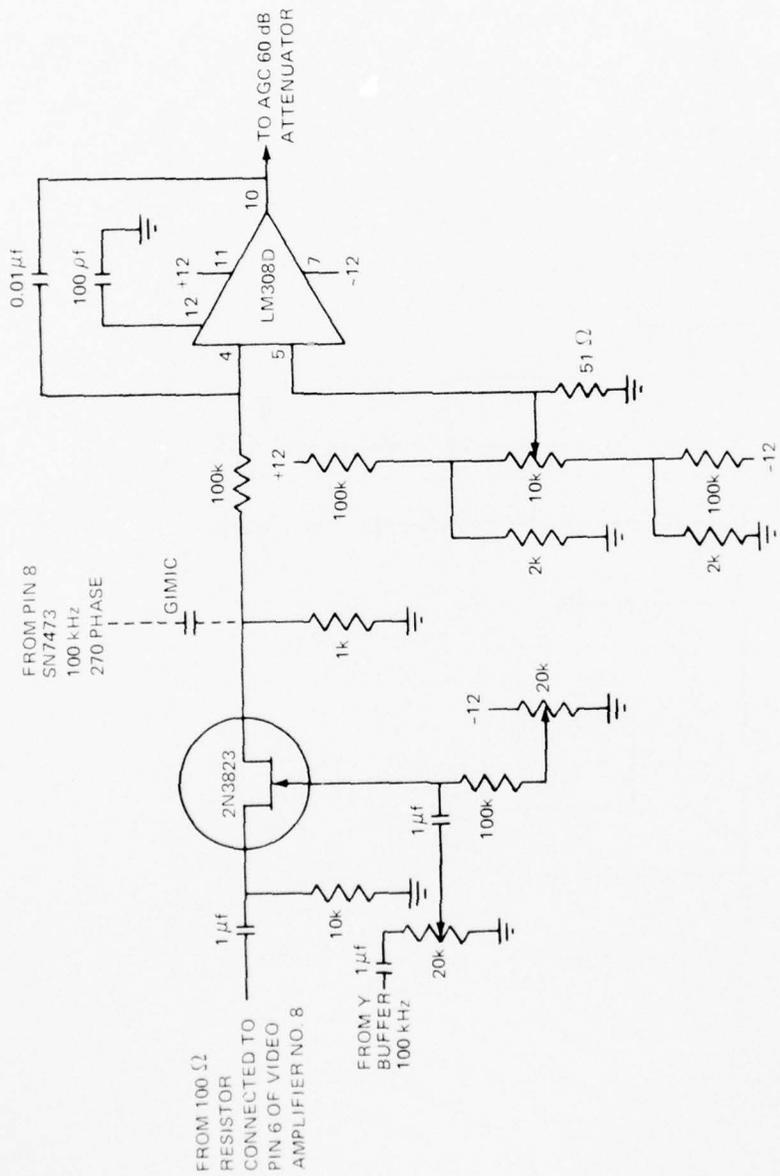


Fig. B-13 AGC OF 60 dB ATTENUATOR PHASE COMPARETOR NO. 3

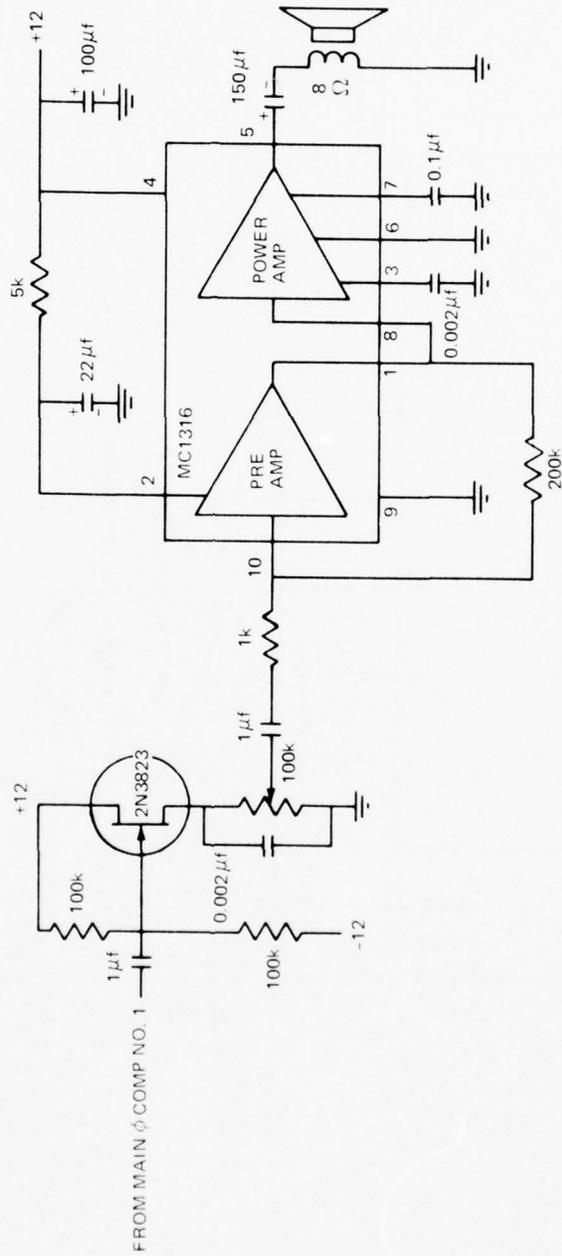


Fig. B-14 AUDIO AMPLIFIER

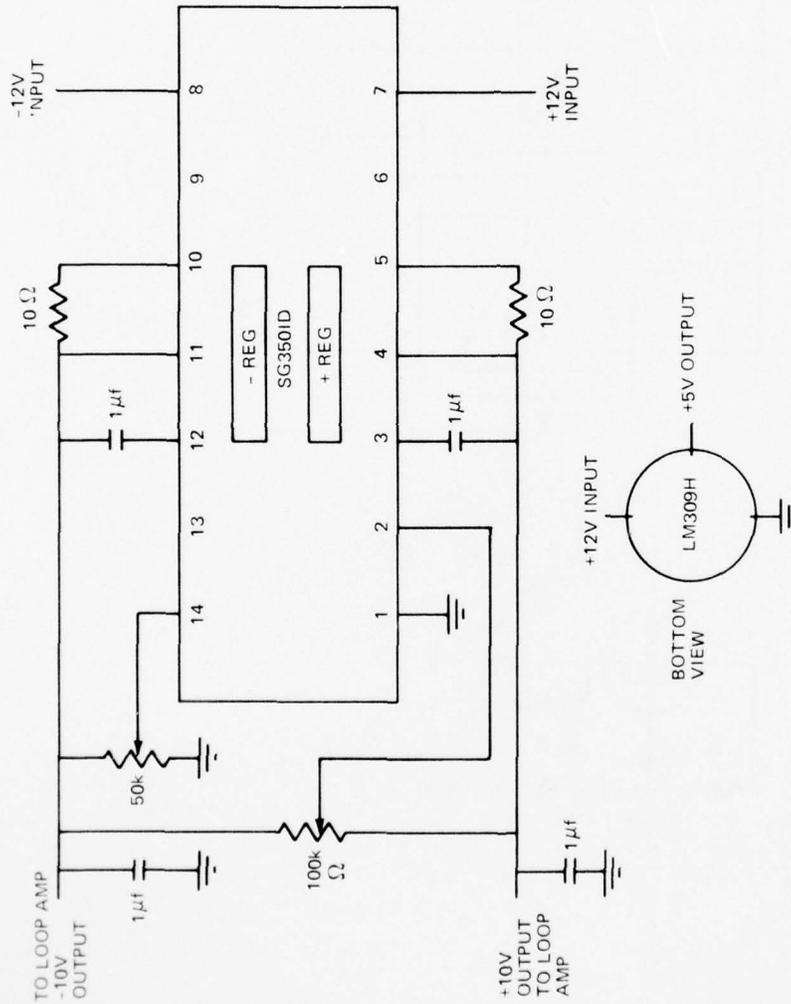


Fig. B-15 POWER FOR MAIN PHASE LOCK LOOP

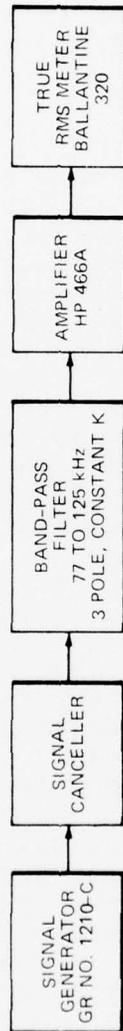


Fig. B-16 SIGNAL CANCELLER TEST SET-UP

was set to 1, 10, 100, and 1000 mV. At each amplitude, the frequency was set to 80 kHz, 100 kHz, and 125 kHz. The resulting attenuation provided by the signal canceller is given in Table B-2. The test results indicate that further refinement of the amplitude control loop is required to meet the specifications given in Table B-1.

STEP ATTENUATOR

The step attenuator sets the overall voltage gain of the RFU by means of attenuating the Loran-C signal. A block diagram with specifications is shown in Fig. B-17. The attenuator setting is controlled by the computer through the gain control file. The attenuation and, therefore, the RFU gain, can be adjusted to any value from zero to 103 dB in one dB steps by selecting combinations of attenuators. The attenuator method of gain control is used to ensure no more than one ten-thousandth of a cycle phase shift at 100 kHz over the entire attenuation range. At least two commercial sources of electrically suitable step attenuators have been found.

BAND-PASS AMPLIFIER

The band-pass amplifier is a fixed gain frequency selective amplifier providing more than 80% of the overall RFU voltage gain. A block diagram with specifications is shown in Fig. B-18. The amplification shown is accomplished in three stages. The total gain of the individual amplifier stages is greater than that specified to provide for losses in the band-pass filter and coupling losses between the signal canceller and step attenuator. The band-pass filter sets the amplifier noise bandwidth and provides for further attenuation of out-of-band undesired signals and attenuation of signal canceller harmonics. The band-pass amplifier output forms the RFU output and is suitable for driving the measurement unit.

Table B-2

Signal Canceller Test Data

Signal Generator		Signal Canceller Attenuation (dB)
Frequency (kHz)	Amplitude (mV)	
80	1.0	22
100	1.0	28
125	1.0	25
80	10	35
100	10	37
125	10	38
80	100	41
100	100	43
125	100	42
80	1000	47
100	1000	47
125	1000	46

Note: Phase lock loop bandwidth: 400 Hz.

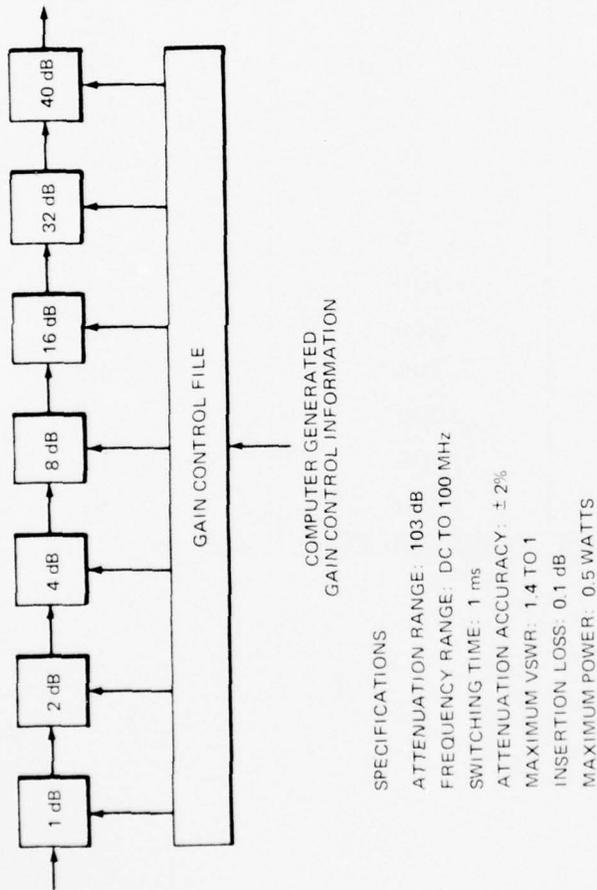


Fig. B-17 STEP ATTENUATOR BLOCK DIAGRAM AND SPECIFICATIONS



Fig. B-18 BAND-PASS AMPLIFIER BLOCK DIAGRAM AND SPECIFICATIONS

Appendix C

DIGITAL MEASUREMENT UNIT DESIGN

INTRODUCTION

The functional block diagram of the Digital Measurement Unit (DMU), Fig. C-1, is discussed in this appendix.

SAMPLE AND HOLD CIRCUIT AND ANALOG-TO-DIGITAL CONVERTER

The sample and hold circuit and analog-to-digital converter portion of the DMU form the signal interface between the RFU and the DMU portions of the Super/Receiver/Navigator. The purpose of the sample and hold circuit is to select a sample point value of the RF waveform and hold the value until the analog-to-digital converter can convert the analog sample to a binary number. The total time available for sample and hold settling and analog-to-digital conversion is 2.5 microseconds. The use of only one sample and hold circuit and analog-to-digital converter for all RF samples produces reasonably constant short term delays and linear offsets due to temperature and supply voltage variations for all measurements.

Circuit implementation required to obtain the digital values of the point samples may be accomplished via three options. The first option is to purchase an entire data acquisition system in a rack mounted, self-contained assembly which includes the sample and hold circuit, analog-to-digital converter, power supplies, front panel monitor, and analog multiplexers for conversion of other signals possibly not related to the Loran receiver. The accuracy, speed, and cost of this equipment are much greater than required by an optimized design of a large-production Loran DMU. An example of the first option is given in Table C-1. The second option is to purchase the sample and hold circuit and analog-to-digital converter separately as modular components suitable for mounting

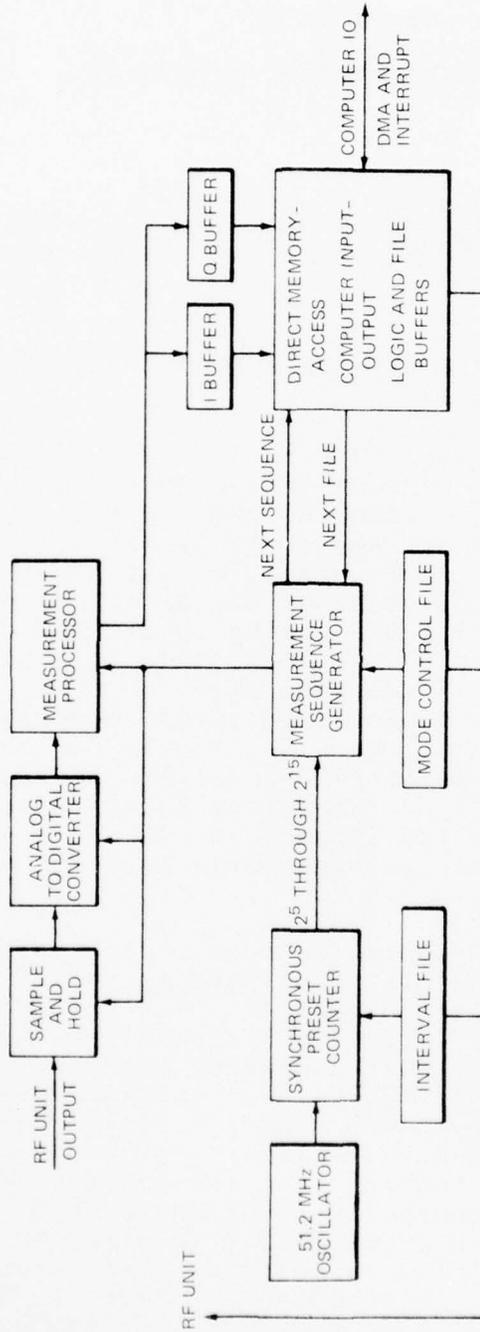


Fig. C-1 DIGITAL MEASUREMENT UNIT BLOCK DIAGRAM

Table C-1

Sample And Hold And Analog-to-Digital Converter Specifications,
 Option 1

Parameter	Specification
Manufacturer	Preston
Type	Rack mounted sample and hold and A-to-D converter system with built-in power supplies and front panel monitor: Room for multichannel multiplexers and instrumentation amplifiers.
Model	GMAD-1
Temperature	0°C to 50°C
Bits	15
Conversion	Total sample and hold for 15 bit conversion = 1.5 microseconds.
Accuracy	Total $\pm 0.01\% \pm 1/2$ LSB over 0°C to +50°C range.
Aperture	Less than 10 nanoseconds.
Linearity	$\pm 0.01\%$ of full scale.
Noise	0.5 millivolt peak to peak.
Voltage Range	± 10 volts
Input Impedance	10 megohms
Price	\$8,555.00
Options	EMI chassis draw. with line filters, meeting general requirements of MIL STD 8264, Type F, Class GP.

on printed circuit boards. This option requires sharing power supplies and chassis housing with other related equipment. Examples of option two are given in Table C-2. The third option is to design the sample and hold circuit and analog-to-digital converter tailored to the receiver environmental and performance requirements at minimum production cost starting with basic components such as operational amplifiers, comparators, integrated circuit digital-to-analog converters, digital circuits, transistor switches, and bulk components. The third option may be most suitable for production design if the second option does not yield a sufficiently close match of performance requirements and price. If the first option is not available for the prototype design, the second option will yield the required analog-to-digital converter circuitry at a modest cost.

MEASUREMENT PROCESSOR

Figure C-2 shows the organization of the measurement processor. Since no shift operations are required, the one bit position shown defines the logic for the remaining 15 bits. The only linkage between bits is the carry output (C out) of each adder bit position, which is connected to the carry input (C in) of the next higher order bit position. The carry output of the highest bit position is now used. The carry input of the lowest bit position is raised when the inverted input of the D register is passed through the adder to form the two's complement of the contents of the D register. Separate adders are used for the I and Q processors to minimize sequence control logic complexity.

Data paths through the measurement processor are controlled by the mode control sequence logic via processor control instructions. A list of these control instructions follows.

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JOHNS HOPKINS UNIV LAUREL MD APPLIED PHYSICS LAB F/G 17/7
SUMMARY REPORT ON USAF SUPER RECEIVER/NAVIGATOR DEVELOPMENT.(U)
JUN 73 L F FEHLNER, R G ROLL, T W JERARDI N00017-72-C-4401
APL/JHU/TG-1220 NL

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Table C-2

Sample And Hold And Analog-to-Digital Converter Specifications,
 Option 2

Parameter	Specification
Manufacturer	Datel Systems, Inc.
Type	Modular Sample and Hold Circuit
Model	SHM-2
Input Voltage Range	Up to $\pm 10V$ FS
Module Control Input	DTL/TTL compatible. Sample - Logic "0" Hold-Logic "1".
Output Voltage Range	Up to $\pm 10V$ FS
Bandwidth	DC to 500k Hz 3dB point
Acquisition Time	100 nanosec to $\pm 0.1\%$ FS
Aperture Time	10 nanosec
Settling Time	1 microsecond
Hold Decay Rate	50 μV /usec
Output Slewing Rate	30 V/usec
Gain	+1.00
Accuracy	$\pm 0.025\%$ of FS
Linearity	$\pm 0.01\%$
Temperature Coefficient	± 20 ppm/ $^{\circ}C$
Power Requirements	+15V DC at 35 ma, -15V DC at 35 ma
Size	2"L x 1"W x 0.4"H
Price	\$109.00

Table C-2 (Continued)

Sample And Hold And Analog-to-Digital Converter Specifications,
 Option 2

Parameters	Specification
Manufacturer	Analog Devices
Type	Modular Sample and Hold Circuit
Model	SHA-2A
Input Voltage Range	0 to $\pm 10V$ FS
Mode Control Input	DTL/TTL compatible Sample - Logic "1", Hold - Logic "0".
Output Voltage Range	Up to $\pm 10 V$ FS
Gain Nonlinearity	0.01% max.
Input Impedance	10" ohms and 7 pf
Offset vs. Temperature	.1 mv $^{\circ}C$ max.
Slewing Rate	100 V/us
Settling Time	to 0.01% in 0.5 us max.
Noise	100 uV rms 100 Hz - 1 MHz Bandwidth
Aperture Delay Time	10 nanosec.
Aperture Jitter	0.25 nanosec.
Drop Rate	.1mV/us max.
Power Requirements	+15V $\pm 2\%$ at 100 ma, -15V $\pm 2\%$ at 100 ma
Temperature Range	0 $^{\circ}C$ to +70 $^{\circ}C$ operating -25 $^{\circ}C$ to +85 $^{\circ}C$ storage
Size	3"L x 2"W x .4"H
Price	\$225.00

Table C-2 (Continued)

Sample And Hold And Analog-to-Digital Converter Specifications,
 Option 2

Parameter	Specification
Manufacturer	Datel Systems, Inc.
Type	Modular A-to-D Converter
Model	ADC-H10B-EX
Temperature	0°C to +70°C for ADC-H10B -25°C to +85°C for ADC-H10B-EX
Bits	10
Voltage Range Options	0 to -5 V, 0 to -10 V, ± 5 V, ± 10 V
Input Impedance	2,000 ohms
Conversion Time	1 microsecond
Maximum sample rate	1,000,000/sec.
Digital Outputs	Parallel output data, serial output data, end of conversion, clock
Accuracy (Incl Quantizing Error)	$\pm 0.1\%$ of FS $\pm 1/2$ LSB
Linearity	$\pm 1/2$ LSB
Temperature Coefficient	± 20 ppm/°C
Power Requirements	+5 V DC at 380 ma, +15 V DC at 45 ma, -15 V DC at 25 ma
Size	4"L x 2"W x 1.0"H
Price	\$995.00 for ADC-H10B, 1,300.00 for ADC-H10B-EX

Table C-2 (Concluded)

Sample And Hold And Analog-to-Digital Converter Specifications,
 Option 2

Parameter	Specification
Manufacturer	Analog Devices
Type	Modular A-to-D Converter
Temperature	0°C to 70°C
Bits	10
Voltage Range	0 to +10 V
Input Impedance	2,500 ohm
Conversion Time	1 microsecond
Maximum Sample Rate	1,000,000/sec.
Digital Outputs	Binary, Parallel all bits and complements
Accuracy	0.05%
Linearity	± 1/2 LS
Temperature Coefficient	50 ppm/°C from 0°C to 70°C
Power Requirements	+5 V DC, +15 V DC, -15 V DC
Size	4.6"L x 2.3"W x 1"H
Price	\$1,990.00

Instructions	Explanation*
Load D in I	$(D) \rightarrow I$
Add D to I	$(D) + (I) \rightarrow I$
Load minus D in I	$-(D) \rightarrow I$
Subtract D from I	$-(D) + (I) \rightarrow I$
Load D in Q	$(D) \rightarrow Q$
Add D to Q	$(D) + (Q) \rightarrow Q$
Load minus D in Q	$-(D) \rightarrow Q$
Subtract D from Q	$-(D) + (Q) \rightarrow Q$

*A register symbol in parentheses refers to the contents of that register.

The control instructions activate various combinations of processor direct control lines called microinstructions. The microinstructions for the processor follow.

Microinstructions	Abbr.	Explanation
Inverted D to Σ_I	NDI	$\neg (D) \rightarrow \Sigma_I$, (otherwise $(D) \rightarrow \Sigma_I$)
Inverted D to Σ_Q	NDQ	$\neg (D) \rightarrow \Sigma_Q$, (otherwise $(D) \rightarrow \Sigma_Q$)
Cin I = 1	CNI	1 \rightarrow Cin I (otherwise 0 \rightarrow Cin I)
Cin Q = 1	CNQ	1 \rightarrow Cin Q (otherwise 0 \rightarrow Cin Q)
I to Σ_I	ADI	$(I) \rightarrow \Sigma_I$ (otherwise 0 $\rightarrow \Sigma_I$)
Q to Σ_Q	ADQ	$(Q) \rightarrow \Sigma_Q$ (otherwise 0 $\rightarrow \Sigma_Q$)
Σ_I to I	CKI	$(\Sigma_I) \rightarrow I$ (otherwise I unchanged)
Σ_Q to Q	CKQ	$(\Sigma_Q) \rightarrow Q$ (otherwise Q unchanged)

The D register is continuously clocked at the end of each 2.5 microsecond interval in synchronism with 2^6 bit position of the synchronous preset counter. The processor instructions are defined in terms of the direct control microinstructions as follows.

Instruction	Microinstruction
$(D) \rightarrow I$	CKI
$(D) + (I) \rightarrow I$	ADI, CKI
$-(D) \rightarrow I$	NDI, CNI, CKI
$-(D) + (I) \rightarrow I$	NDI, CNI, ADI, CKI
$(D) \rightarrow Q$	CKQ
$(D) + (Q) \rightarrow Q$	ADQ, CKQ
$-(D) \rightarrow Q$	NDQ, CNQ, CKQ
$-(D) + (Q) \rightarrow Q$	NDQ, CNQ, ADQ, CKQ

Inspection of the preceding list shows that two sets of microinstrumentation always appear together. They are NDI with CNI, and NDQ with CNQ. The number of microinstructions may therefore be reduced by two by redefining NDI with CNI as MDI (for minus D to Σ_I) and NDQ with CNQ as MDQ (for minus D to Σ_Q). Two additional microinstructions which pertain to the I buffer and Q buffer which serve as interface buffers between the measurement processor and direct memory access logic may be defined. They are as follows:

Microinstructions	Abbr.	Explanation
Σ_I to I Buffer	CIB	$\Sigma_I \rightarrow IB$ (otherwise IB unchanged)
Σ_Q to Q Buffer	CQB	$\Sigma_Q \rightarrow QB$ (otherwise QB unchanged)

On the last two clock pulses of a processor measurement, the output of the adder for the I component is clocked into the I buffer and the output of the adder for the Q component is clocked into the Q buffer for transfer to the computer memory via the direct memory access channel. The measurement processor consists of 39 integrated circuits; 12 type 5495, 16 type 54157, 8 type 5483, and 3 type 5404.

FILES AND FILE BUFFERS

All files and file buffers are identical. This includes the interval, mode, address, and block length. The most convenient form for the RF mode and gain buffers are also the same as these files and file buffers. The bit length of each file word is 16, the same as the computer word length. Each file and file buffer is made up of four 4-bit sections. One 4-bit section is shown in Fig. C-3.

Each 54170 MSI circuit is a four word by four bit file. The outputs are ORed together with pullup resistors contained in one-third of a pull-up resistor IC network. The two 54170 circuits alternate roles as file and file buffer. The 54170 which is being used as the active file, either the ODD file or EVEN file, has its read enable signal activated by the sequence control logic.

Write control is different for the interval mode, address, and block length files. Only the current buffer file is written into by the Direct Memory Access output logic during a mode sequence. Writing may take place simultaneously in the active and buffer address and block length files. The active address or block length files must change as a table in computer memory is filed. The detailed operation of the address and block length file is dependent upon the computer selected. A total of 38 integrated circuits are required for the interval, mode, address and block length, file, and file buffers; 32 type 54170 ICs and 6 resistor network ICs.

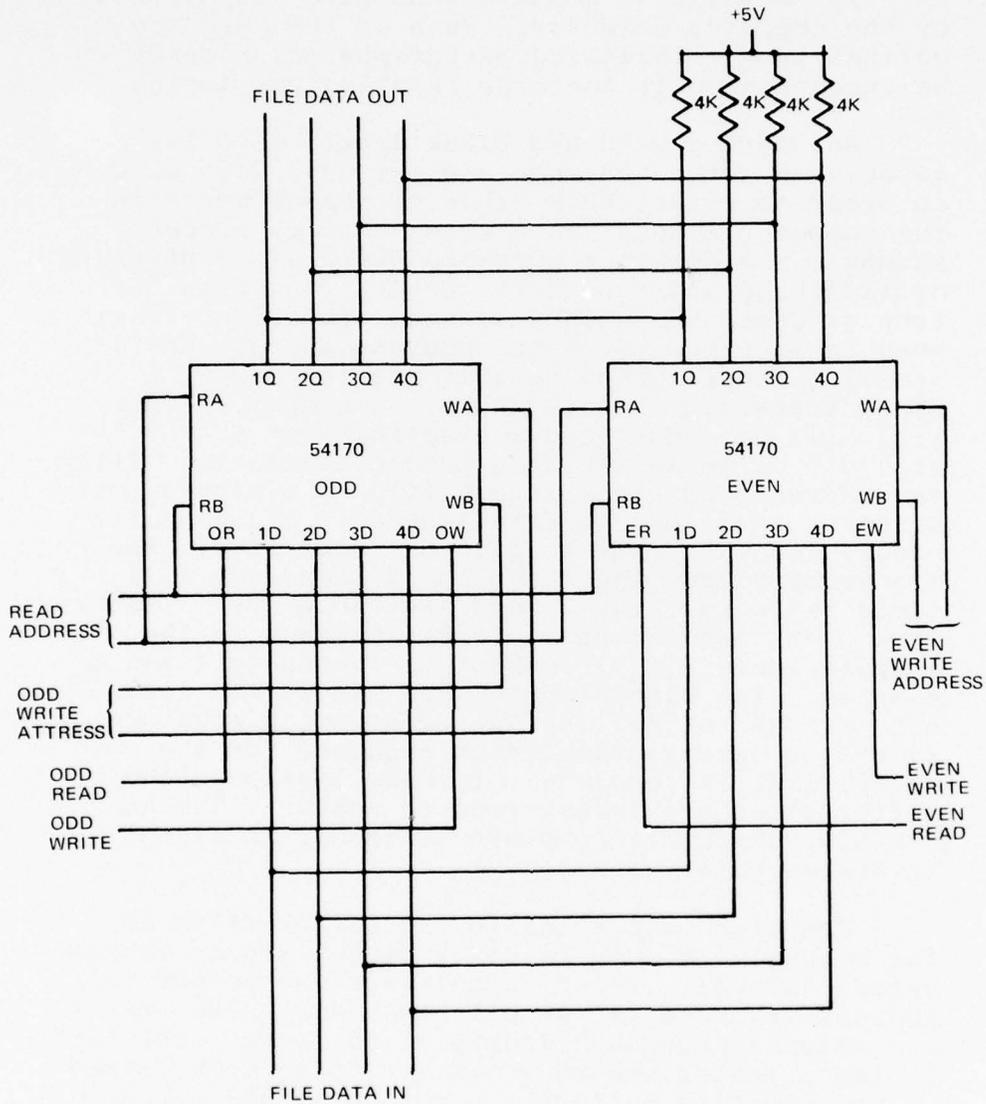


Fig. C-3 FOUR BITS OF FOUR WORD FILE REGISTER AND BUFFER

DIRECT MEMORY ACCESS (DMA), COMPUTER INPUT-OUTPUT

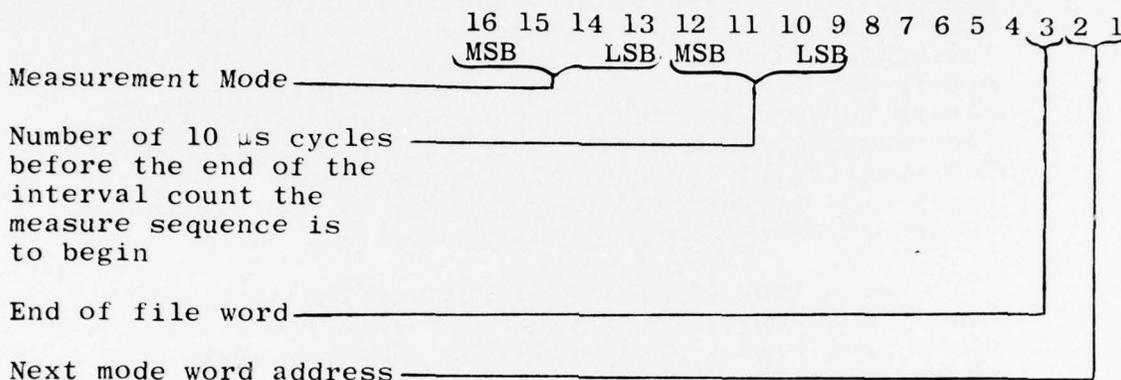
The details of a DMA channel are established by the computer selected. Much of the hardware defined in the following paragraphs may already be incorporated in computer input-output logic.

An address word and block length word is associated with each mode and interval file word. In order to establish a table of measurements in the computer memory via a direct memory access channel, the computer software outputs the starting or finishing address of the table along with the true or complement block length. The block length word is incremented as the address changes until overflow occurs which establishes the end of a block transfer. The table in the computer memory will fill by memory cycle stealing from the background program as the data become available. Using the address and block length file, a separate measurement table may be established in the computer memory for each mode word in the mode file. Each measurement from the measurement processor will yield two words, the I word and the Q word. Therefore each measurement table established in the computer memory will consist of alternate I and Q samples. The block length word serves the alternate purpose of telling the measurement sequence generator when a measurement sequence for the active file is complete. In this instance, the buffer files are transferred to active files and the block transfer complete interrupt is sent to the computer.

Computer outputting to the buffer files in the measurement unit is via a direct memory access output channel. First, a software convenient file address sequence is established. Next, the starting address and block length of the words contained in the computer memory which are to be transferred to the DMU file buffers are set up in DMA output address and block length registers. The output sequence then proceeds by memory cycle stealing from the background program.

MODE WORD FORMAT

The measurement sequence generator interprets the mode control word in the following manner:



The measurement mode bit positions 16 through 13 allows for 16 measurement modes. Four basic mode types, wait, search, track, and settle have been defined although it may not be necessary to use wait. Also several other measurement modes will be required for test and calibration. Bits 12 through 9 define the number of 10 microsecond cycle intervals before the synchronous preset counter overflows and the measure sequence begins. This number may be as large as the total number of cycles in the measurement interval. Bit position 3 is set to a one if a measurement sequence may end when the measurement is complete. The end of the sequence is conditional upon the end of a DMA and block transfer. Bit positions 2 and 1 give the address of the next mode word in the four word mode file. It may address itself or any of the other three words. The mode control words contain no information that must be changed or packed by computer programming as the result of information derived from samples of the signal. Once a measurement sequence is decided upon the mode word file for that sequence is established. The length of a mode file for a measurement sequence may be from one to four words.

MEASUREMENT SEQUENCE GENERATOR

Figure C-4 shows the organization of the measurement sequence generator. The main component of the measurement sequence generator is a 256 word by 8 bit read only memory. Suitable integrated circuits for constructing the read only memory are readily available. The read only memory is used as the microprogram controller for the measurement processor and the I and Q buffers. The function of the control outputs, shown on the right side of the read only memory, is defined in the measurement processor section.

The number of address inputs to the read only memory determines the number of combinations, or words, required. The first four address inputs shown on the left side of the read only memory are the mode control word bits 16 through 13 which define the type of measurement mode. This allows for 16 possible types of measurement modes. The next two address lines are the two outputs of the synchronous preset counter, 2^7 and 2^8 , which define the four possible sample points in one cycle of the Loran signal. The last two address inputs to the read only memory are labeled first cycle and last cycle. The control sequence for a measurement may be different for the first cycle than for intermediate cycles or the last cycle. If the measurement sequence only occurs over one cycle, the first and last cycles are the same.

The enable input to the read only memory is the logic OR function of first cycle signal, the run flip flop, and the last cycle signal. The first cycle signal is generated by the start comparator. A suitable integrated circuit for the start comparator is the 5485 gated 4-bit comparator. The enable input to the start comparator is activated by the logical AND of the last three stages of the synchronous preset counter 2^{15} , 2^{14} , and 2^{13} . The next four stages of the synchronous preset counter, 2^{12} , 2^{11} , 2^{10} , and 2^9 are the four inputs to one side of the comparator. The mode control word bits 12, 11, 10, and 9 are the four inputs to the other side of the comparator. This arrangement allows the first cycle signal to be generated under control of the mode control

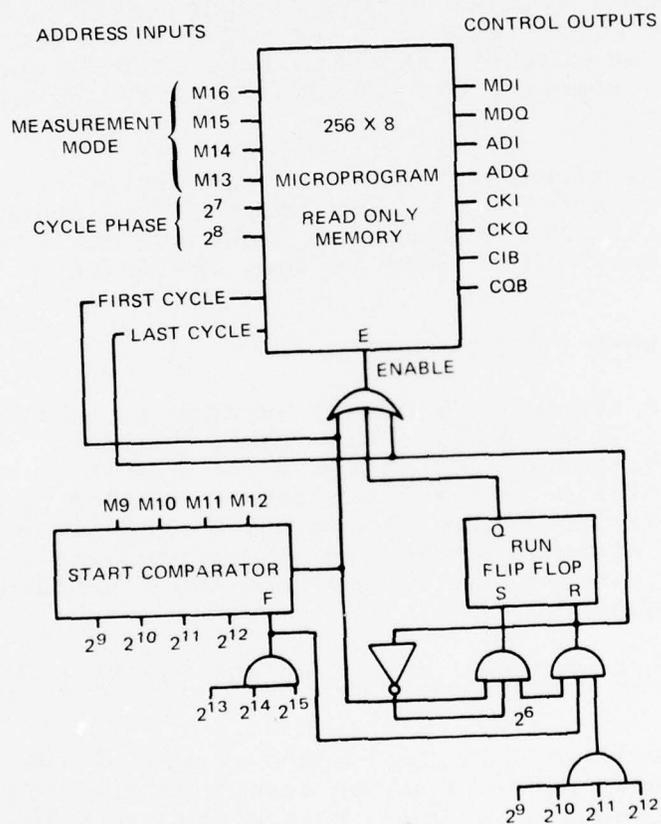


Fig. C-4 MEASUREMENT SEQUENCE GENERATOR

word at from one cycle to 16 cycles before the end of the measurement interval. The number of cycles before the end of the measurement interval cannot be made longer than the number of cycles in the measurement interval.

The first cycle signal, in addition to addressing and enabling the microprogram read only memory, sets the run flip flop. The run flip flop is reset by the last cycle signal. The last cycle signal is generated by the logical AND of synchronous preset counter stages 2^{15} through 2^{29} . Synchronous preset counter stage 2^6 acts as the clock for the measurement sequence generator as well as the measurement processor and the I and Q buffer registers.

This measurement sequence generator organization accommodates all presently defined measurement sequences. New measurement sequences may be added to the read only memory as they are defined.

SYNCHRONOUS PRESET COUNTER

The synchronous preset counter is a 16-bit device. It is divided into three sections: the first section describes the first four high speed stages of the counter, the second section describes the remaining twelve slower speed stages, and the third section describes the logic required to transfer the interval file word into the synchronous preset counter.

The Four High Speed Stages of the Synchronous Preset Counter

The first four high speed stages of the synchronous preset counter accept parallel input data by count deletion. This method is used to allow wide speed margins using series 54 Schottky logic. Basic operation is shown in Fig. C-5, which shows one count stage of logic.

The 54S112 flip-flops on the negative going edge of the clock, CK, will toggle if both the J and K inputs are high, set if the J input is high and the K input is low, clear if the K input is

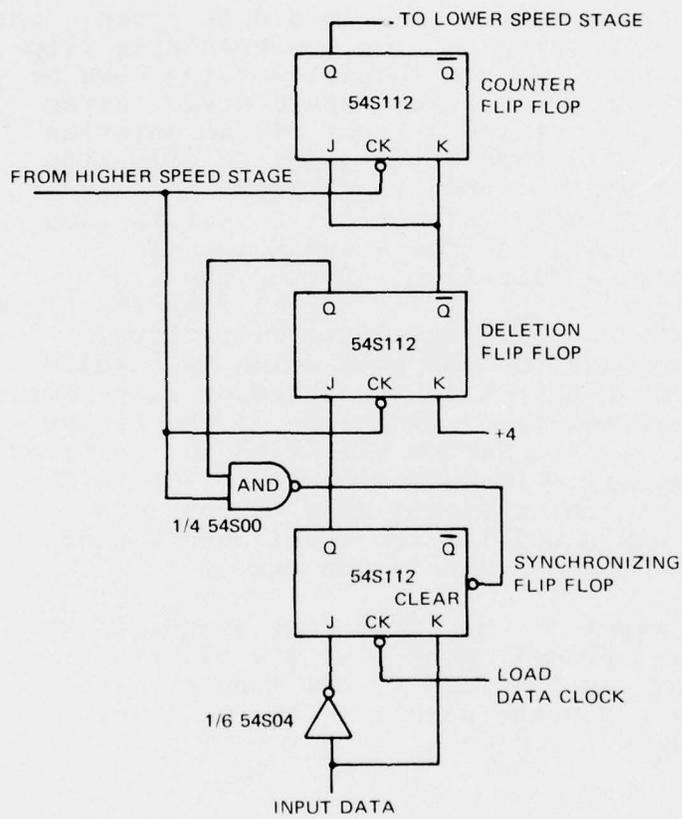


Fig. C-5 ONE HIGH SPEED STAGE OF SYNCHRONOUS PRESET COUNTER

high and the J input is low, and not respond to the clock if both the J and K inputs have been low for the duration of the positive clock pulse. The 54S112 flip-flops also have direct clear and preset inputs which function independent of the clock input.

The complement of the input data is transferred to the Synchronization flip-flop on the negative going edge of the load data clock. When the set, or Q output of the synchronizing flip-flop goes high the next negative going edge of the signal from the higher speed stage, after the setup time of the J input of the deletion flip-flop, will toggle the deletion flip-flop to the set state. When toggling to the set state, the \bar{Q} output of the deletion flip-flop goes down inhibiting the J and K inputs of the counter flip-flop. During the next positive going edge of the signal from the higher speed stage, the synchronizing flip-flop is cleared through the AND gate which is enabled by the high Q output of the deletion flip-flop. On the next negative going edge of the higher speed stage, the counter flip-flop is inhibited from toggling as the deletion flip-flop, with its J input low, switches back to the zero stage. This completes the count deletion of one cycle of the higher speed stage.

The input to the first four stages of the synchronous preset counter is the 51.2 MHz oscillator and the four preset inputs. The output is a 3.2 MHz signal to the 12 lower speed stages.

The Twelve Lower Speed Stages of the Synchronous Preset Counter

The remaining 12 stages of the synchronous preset counter are constructed from three synchronous four bit counters. This, shown in Fig. C-6, consists of three type 54163 MSI circuits.

These three circuits form a 12 stage synchronous binary up counter with 12 individual stage outputs, an all one overflow carry output, 12 parallel data inputs, 3.2 MHz clock input, and count/preset mode control inputs.

Data Transfer Logic for the Synchronous Preset Counter

The logic required for data transfer from the internal file to the synchronous preset counter are determined by several factors. The first consideration is that positive true binary is the most convenient form for the computer software to generate the interval numbers. The second consideration is that the first four stages are up counters and their parallel data inputs to the delete logic are in effect subtracted from their count value. The final consideration is that the last 12 counters are up counters and their parallel data inputs directly preset their next count value. Also, the entire 16 bit count overflow condition is all ones, which is equivalent to minus one in negative two's complement notation, and is about to overflow to zero when the data transfer of the next interval word is to occur.

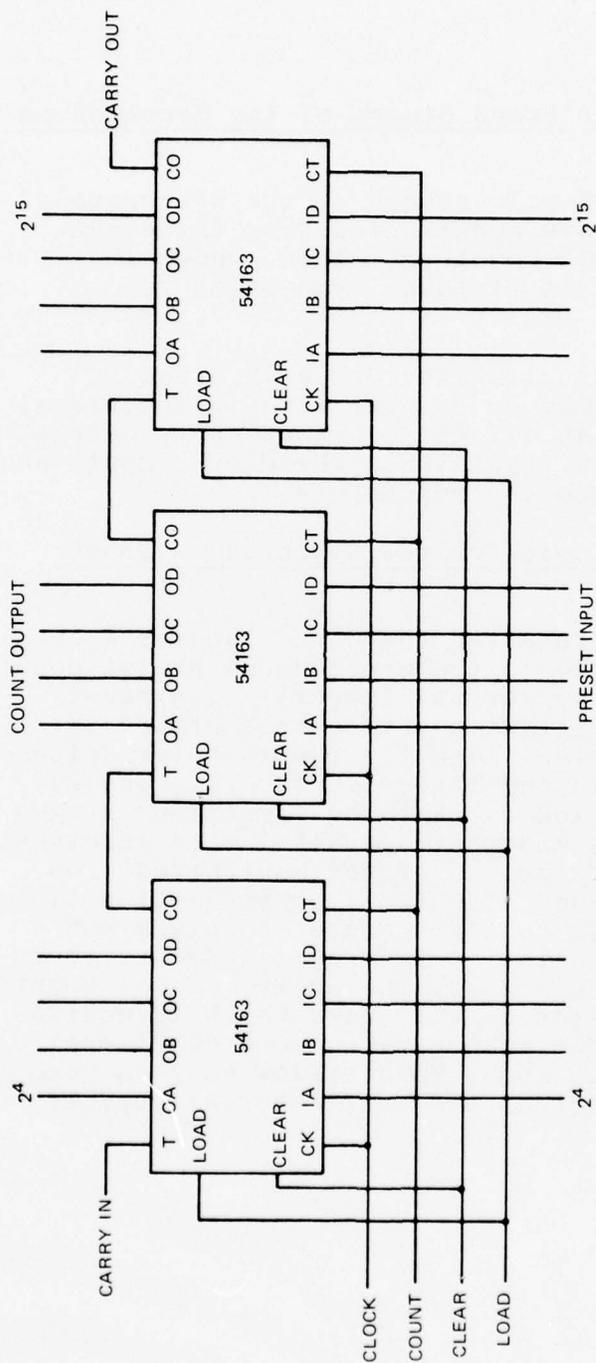


Fig. C-6 TWELVE LOWER SPEED STAGES OF SYNCHRONOUS PRESET COUNTER

To arrive at the proper transfer logic, first consider the case of a 16 bit up counter with the overflow condition of all ones. Data are directly transferred to the first four stages as with the last 12 stages. It is necessary to load the negative two's complement of the interval value desired into the counter on the clock interval pre-setting the counter overflow to all zeros. This could be accomplished (Fig. C-7) by transferring the one's complement, or bit by bit inversion of the next positive interval word through one input side of a 16-bit parallel adder and raising the carry input of the adder to convert the output from the negative one's complement of the interval to the negative two's complement.

However, the first four stages always overflow to all zeros creating an interval length of at least 16 counts of the 51.2 MHz oscillator. Therefore 16 counts must be subtracted from the remaining 12 bit positions of the positive interval word, or added to the negative interval word before it is transferred to the last 12 stages of the up counter. Since the deletion method employed in the first four high speed stages amounts to direct subtraction, the four least significant bits of the interval word need not be complemented. The resultant transfer logic consists of a 12-bit parallel adder and 12 inverters as shown in Fig. C-8 with the high speed delete counter and low speed preset counter.

The 12 inverters complement the 12 most significant bits of the interval word while the adder with the raised carry input adds 16 counts to the complement interval number. The 12 inverters require two type 5404 integrated circuit packages, (six inverters per package), while the adder requires three type 5483 four bit parallel adder integrated circuit packages. These five integrated circuits form part of the 16 bit synchronous preset counter block shown on the measurement unit block diagram. The synchronous preset counter block contains 16 integrated circuits.

The one possible limitation of this synchronous preset counter design is that the minimum interval word value must be greater than 16 oscillator counts or 0.3125 microseconds. Since the

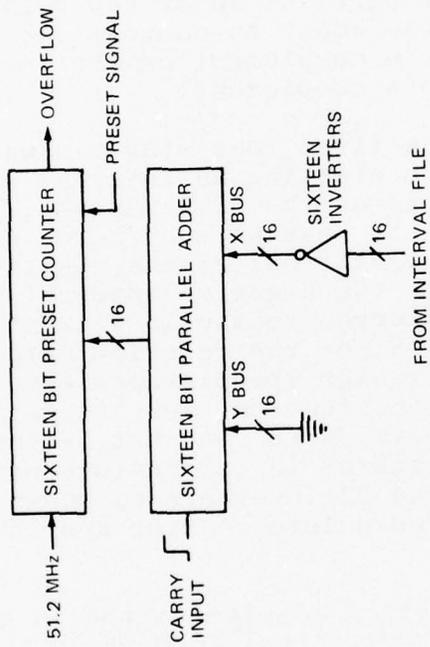


Fig. C-7 INTERVAL COUNTER WITH LOGIC FOR LOADING TWO'S
COMPLEMENT OF INTERVAL FILE WORD

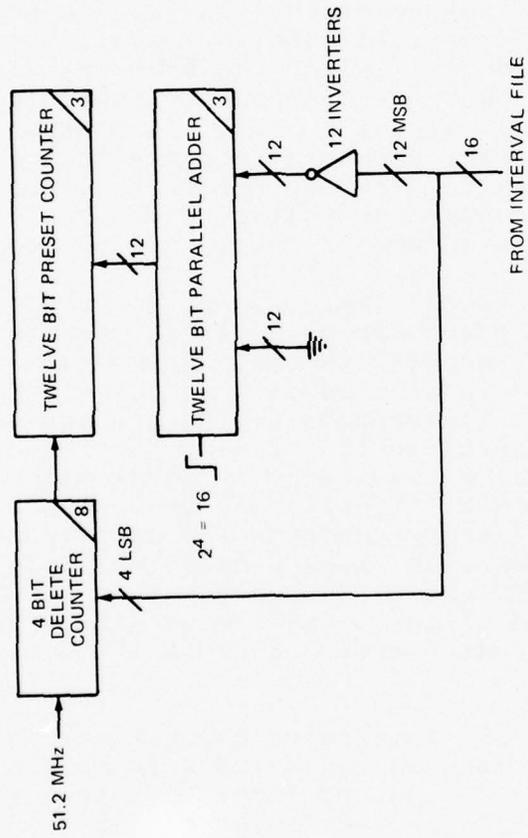


Fig. C-8 16-BIT SYNCHRONOUS PRESET COUNTER

minimum sample interval is 2.5 microseconds, interval word values less than this minimum will not be required.

SELECTION OF LOGIC CIRCUITS

In the selection of logic circuits for the prototype design of the DMU, cost, established reliability, and availability were considered. Standard power series 54 bipolar transistor-transistor logic was selected. The continued use of integrated circuit functions available in 14 pin and 16 pin dual inline packages was also decided. These packages are readily assembled on standard matrix layout boards. In portions of the DMU where higher speed is required than standard series 54 logic affords, Schottky clamped series 54 logic, which is voltage and signal compatible with standard 54 logic, can be used.

In an operational design where lower power is desired than standard series 54 logic requires for ease of high density thermal design, low power series 54L logic and low power Schottky clamped series 54L logic may be substituted for the standard power series 54 logic. A micropower measurement unit utilizing complementary metal oxide semiconductor, CMOS, circuits may be designed which could be battery powered. If an extremely high density, low cost, high production design is required, the DMU can be packaged with a few large scale integrated circuits (LSI) most likely using P channel metal oxide semiconductors (PMOS) techniques.

Manufacturers' integrated circuit catalogs and application manuals can be used to obtain detailed information on the individual series 54 logic elements used in the design of DMU.

OSCILLATOR

Table C-3 gives a manufacturer's specification of an oscillator suitable for the prototype Super Receiver/Navigator. Several other choices of manufacturers are available. The oscillator

Table C-3

Oscillator Specifications

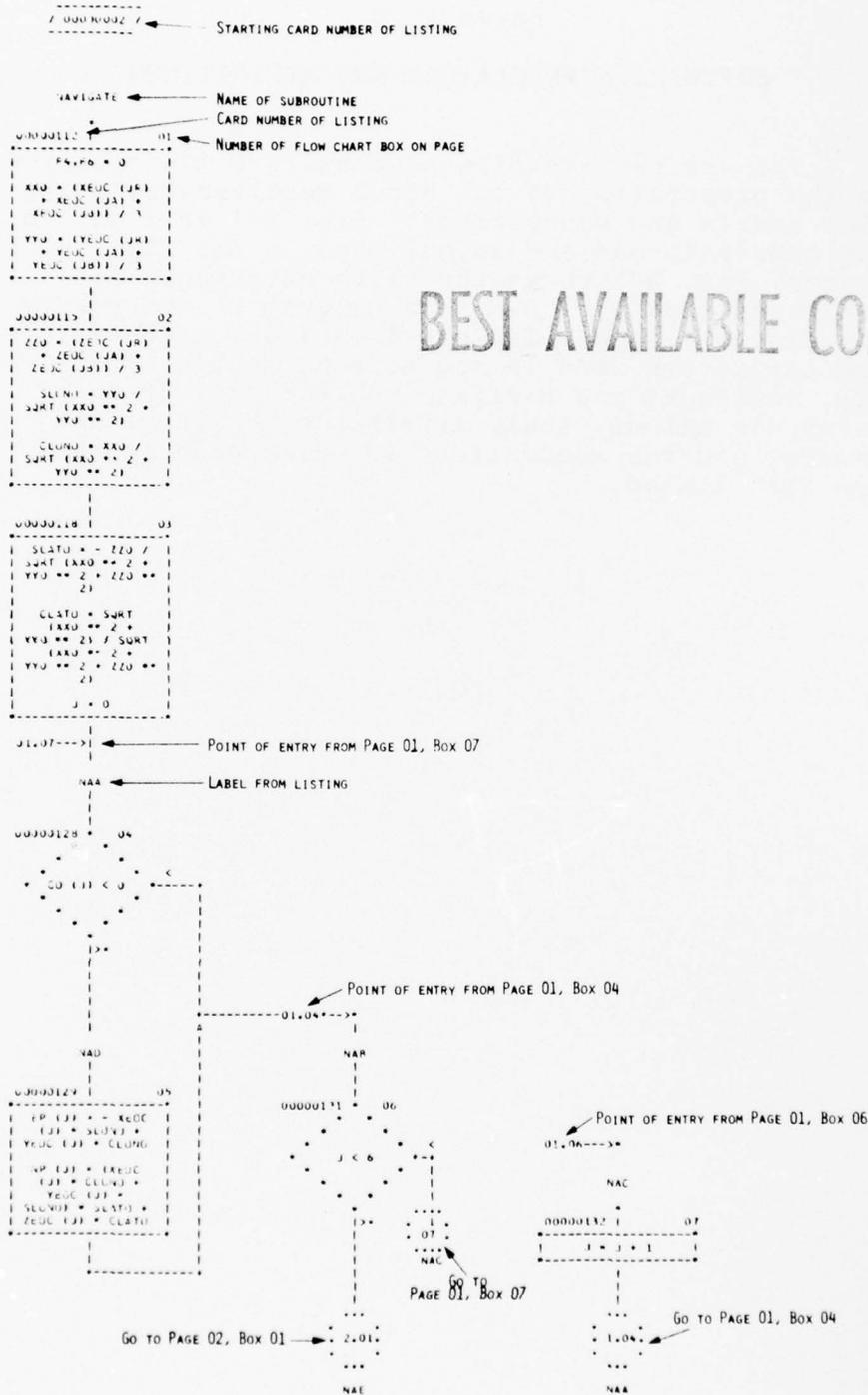
Parameters	Specification
Type	VHF High Stability Frequency Source
Manufacturer	Greenray Industries, Inc.
Model No.	YH-522-45
Frequency Range	20.1 MHz to 120 MHz (specify exact frequency desired)
Stability at Fixed Ambient	$\pm 5 \times 10^{-8}$ per week $\pm 1 \times 10^{-9}$ per 70 milliseconds $\pm 1 \times 10^{-9}$ per second $\pm 1 \times 10^{-8}$ per 24 hours
Stability Over Temperature Range	$\pm 5 \times 10^{-8}$
Temperature Range	0°C to 50°C
Output	0.22 V RMS minimum (1 milliwatt) into 50 ohms
Output Waveform	Sine, harmonics, and subharmonics down -20 dB minimum
Spurious Non-Harmonical Related Noise	Down -60 dB minimum
Input	+28 V DC $\pm 2\%$ regulation for oscillator and oven. RF input filters on DC leads.
Size	2-1/8" x 2-1/8" x 4-1/4" high
Connector	05M style
Note	Meets military specifications
Price	\$489.00 1-3 units \$199.00 100 units

specified is of the proportional oven-temperature-controlled crystal type. Oscillators of this type have a frequency adjustment located atop the unit to set the oscillator exactly on frequency and compensate for long term aging. Thirty days of crystal aging is recommended before final frequency adjustments are made.

Appendix D

SOFTWARE NOMENCLATURE AND DEFINITIONS

The use of extensive nomenclature was required in the preparation of the Super Receiver/Navigator flow charts and subroutines. Fig. D-1 is a key to the abbreviations and layout used in the flow charts, Fig. D-2 shows the earth orthogonal coordinates, and Fig. D-3 is a diagram of the planar coordinate system. Table D-1 includes nomenclature for parameters used in the Search, Settle, Track, SID, Newtrack, and Navigate subroutines. Parameter dimensions, scale attributes, definitions, values, and the subroutines in which each appears are also listed.



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Fig. D-1 KEY TO FLOW CHARTS

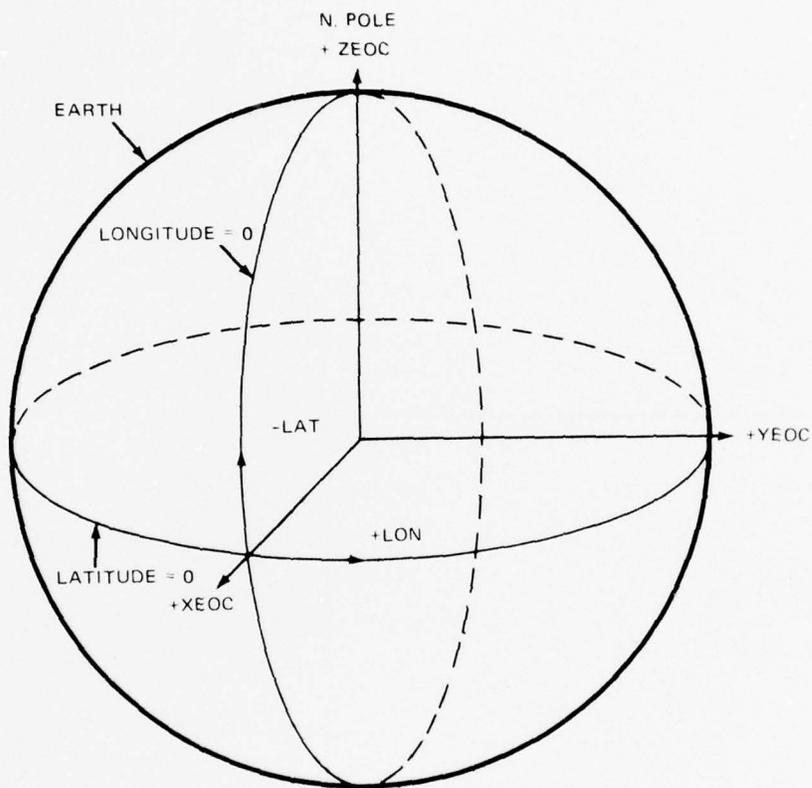


Fig. D-2 EARTH ORTHOGONAL COORDINATES

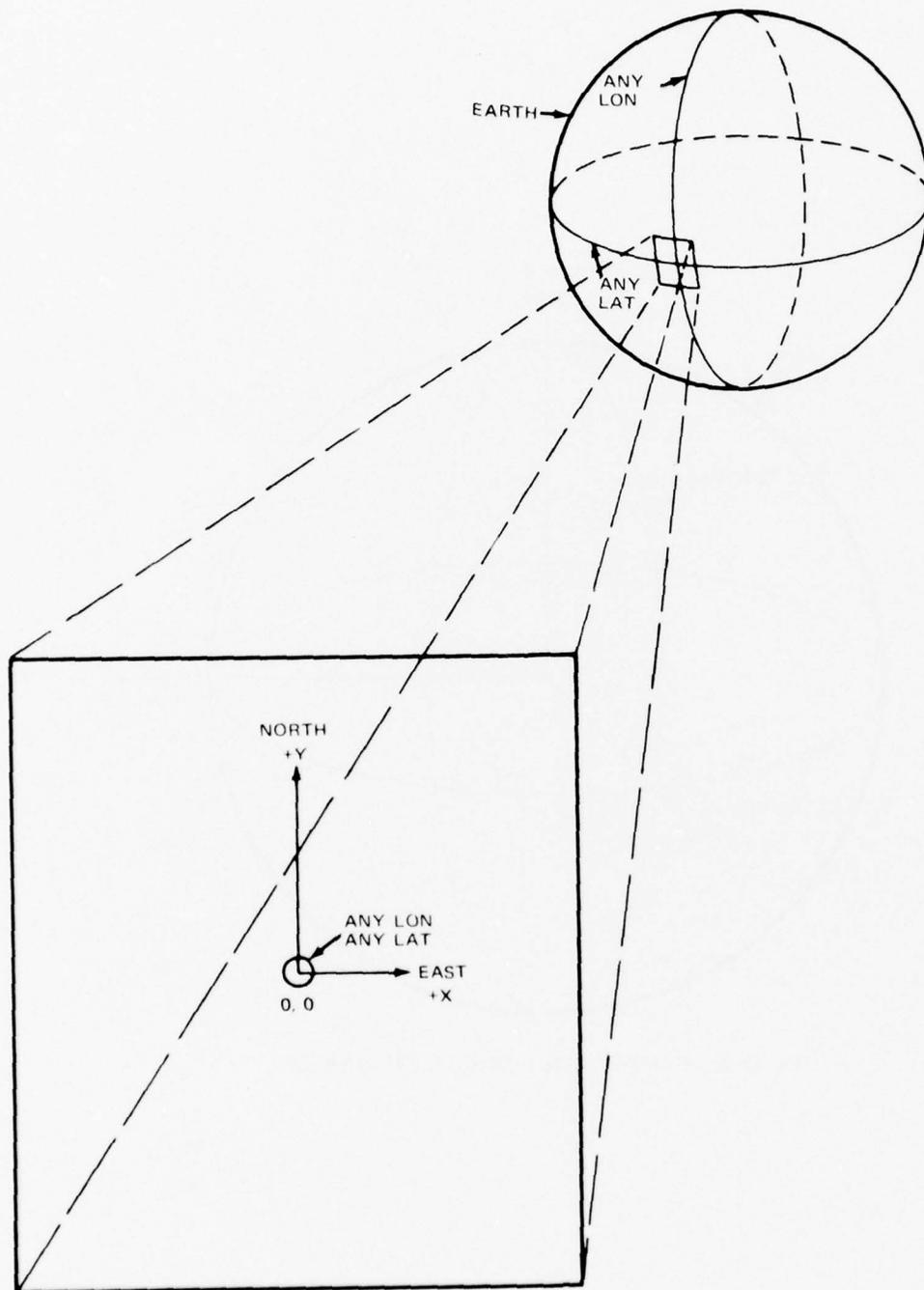


Fig. D-3 PLANAR COORDINATE SYSTEM

Table D-1

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
A	TRACK	Radians/Second Floating Point	Second order filter equation constant; two times the damping factor times the natural radian frequency. Value is $2 \cdot 707 \cdot 02 \cdot 3.14159$.
AA	TRACK	Dimensionless Floating Point	Low pass filter gain constant for expected value of 'I' voltage used in AGC loop. Value is one.
AAA	SID	Meters Floating Point	Parameter A, page 18 of Ref. 5. The value is computed.
AAS	SETTLE	Dimensionless Fixed Point	Temporary stored value of parameter AS.
ALPHA	TRACK	Radians Floating Point	Second order filter equation scale factor. The value is A times TAU.
ALPHAC	SID	Meters Floating Point	Parameter (Greek letter alpha), page 18 of Ref. 5. The value is computed.
ALPHAN	NAVIGATE	Meters Floating Point	Parameter (Greek letter alpha), page 18 of Ref. 5. The value is computed.
AM	SETTLE	Dimensionless Fixed Point	Temporary stored value of parameter AS.
AN	NAVIGATE	Meters Floating Point	Parameter A, page 18 of Ref. 5. The value is computed.
AS	SETTLE	Dimensionless Fixed Point	Counter of number of successful amplitude consistency tests for 'I' signal component.
ATD	NAVIGATE	Meters Floating Point	Along-track-distance to go. The value is computed.
ATDMIN	NAVIGATE	Meters Floating Point	Minimum value of ATD at which turn maneuver begins. The value is initialized.
ATDR	NAVIGATE	Meters/Second Floating Point	Along-track-distance to go rate. The value is computed.
B	TRACK	(RAD/SEC) ² Floating Point	Second order filter equation constant; natural radian frequency squared. Value is $(02 \cdot 3.14159)^2$.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
BBB	SID	Meters Floating Point	Parameter B, page 18 of Ref. 5. The value is computed.
BETA	TRACK	Radians Floating Point	Second order filter equation scale factor. The value is B times TAU.
BETAC	SID	Dimensionless Floating Point	Parameter (Greek letter beta), page 18 of Ref. 5. The value is computed.
BETAN	NAVIGATE	Dimensionless Floating Point	Parameter (Greek letter beta), page 18 of Ref. 5. The value is computed.
BL	SID NAVIGATE NEWTRACK	Microseconds Floating Point	An array of all baseline lengths from transmitter to transmitter in a chain. The values are ground computed.
BM	SETTLE	Dimensionless Fixed Point	Temporary stored value of parameter BS.
BN	NAVIGATE	Meters Floating Point	Parameter B, page 18 of Ref. 5. The value is computed.
BS	SETTLE	Dimensionless Fixed Point	Counter of number of successful amplitude consistency tests for 'Q' signal component.
C	TRACK SEARCH SETTLE NEWTRACK	Counts Fixed Point	The number of 51.2 MHz clock pulses from the start of the local GRI to the time the Loran signal is received. The value is computed.
CCC	SID	Meters Floating Point	Parameter C, page 18 of Ref. 5. The value is computed.
CD	SID NAVIGATE NEWTRACK	Microseconds Floating Point	An array of coding delays for each transmitter. The values are ground computed.
CLAT	NEWTRACK	Dimensionless Floating Point	Cosine of the latitude of the centroid of the triad used for navigation. The value is computed.
CLAT	SID	Dimensionless Floating Point	Cosine of the latitude of the centroid of all transmitting stations of a chain. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
CLATO	NAVIGATE	Dimensionless Floating Point	Cosine of the latitude of the centroid of the triad used for navigation. The value is computed.
CLON	NEWTRACK	Dimensionless Floating Point	Cosine of the longitude of the centroid of the triad used for navigation. The value is computed.
CLON	SID	Dimensionless Floating Point	Cosine of the longitude of the centroid of all transmitting stations of a chain. The value is computed.
CLONO	NAVIGATE	Dimensionless Floating Point	Cosine of the longitude of the centroid of the triad used for navigation. The value is computed.
CN	NAVIGATE	Meters Floating Point	Parameter C, page 18 of Ref. 5. The value is computed.
CPSIA	NAVIGATE	Dimensionless Floating Point	Cosine of the azimuth of the receiver with respect to transmitter "A" location. The value is computed.
CPSIB	NAVIGATE	Dimensionless Floating Point	Cosine of the azimuth of the receiver with respect to transmitter "B" location. The value is computed.
CPSIR	NAVIGATE	Dimensionless Floating Point	Cosine of the azimuth of the receiver with respect to reference transmitter "R" location. The value is computed.
CTC	NAVIGATE	Dimensionless Floating Point	Cosine of true course. The value is computed.
CTE	NAVIGATE	Meters Floating Point	Cross-track-error. The value is computed.
CTER	NAVIGATE	Meters/Second Floating Point	Cross-track-error rate. The value is computed.
D	SEARCH	Dimensionless Fixed Point	Circular table subscript. The value ranges from zero to eighty.
DD	SEARCH	Dimensionless Fixed Point	Stored value of D at time of pulse detection. The value ranges from zero to eighty.
DDA	SID	Meters Floating Point	Parameter (Greek letter mu sub A), page 18 of Ref. 5. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
DDAN	NAVIGATE	Meters Floating Point	Parameter (Greek letter mu sub A), page 18 of Ref. 5. The value is computed.
DDB	SID	Meters Floating Point	Parameter (Greek letter mu sub B), page 18 of Ref. 5. The value is computed.
DCBN	NAVIGATE	Meters Floating Point	Parameter (Greek letter mu sub B), page 18 of Ref. 5. The value is computed.
DDD	SID	Meters Floating Point	Parameter D, page 18 of Ref. 5. The value is computed.
DDN	NAVIGATE	Meters Floating Point	Transmitter-to-receiver distance differences computed from time differences.
DEL	SID	Meters Squared Floating Point	Parameter (Greek letter delta), page 18 of Ref. 5. The value is computed.
DELE	NAVIGATE	Meters Floating Point	Easting distance difference between receiver and next waypoint. Value is computed.
DELN	NAVIGATE	Meters Squared Floating Point	Parameter (Greek letter delta), Page 18 of Ref. 5. The value is computed.
DELNN	NAVIGATE	Meters Floating Point	Northing distance difference between receiver and next waypoint. The value is computed.
DELR	NAVIGATE	Meters Floating Point	Range difference tolerance between known and computed receiver positions. The value is 20,000.
DELTA	SEARCH	Volts Floating Point	Tolerance used in amplitude consistency tests. The value is 0.1.
DELTAN	SEARCH	Counts Floating Point	Increment in the number of 51.2 MHz clock pulses, N. The value is computed.
DELTAS	SETTLE	Volts Floating Point	Tolerance between two data samples. The value is 0.1.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
DELTAT	TRACK NEWTRACK	Volts Floating Point	Tolerance used in rejecting TRACK input data. The value is computed.
DELX	NAVIGATE	Meters Floating Point	The easting difference between two adjacent waypoints. The value is computed.
DELX	SID	Meters Floating Point	Tolerance between known and computed receiver locations. The value is 10,000.
DELY	NAVIGATE	Meters Floating Point	The northing difference between two adjacent waypoints. The value is computed.
DLTATO	SEARCH NEWTRACK	Volts Floating Point	Minimum value of DELTAT. The value is one.
DLTMIN	TRACK	Volts Floating Point	Minimum value of tolerance used in rejecting TRACK input data. The value is 0.25.
DN	NAVIGATE	Meters Floating Point	Parameter D, page 18 of Ref. 5. The value is computed.
DT	NAVIGATE	Seconds Floating Point	Delay time. The value is zero.
DTHMT	NAVIGATE	Dimensionless Floating Point	Determinant of geometric dilution of precision. The value is computed.
EEE	SID	Meters Squared Floating Point	Parameter E, page 18 of Ref. 5. The value is computed.
EI	TRACK SEARCH NAVIGATE NEWTRACK	Volts Floating Point	An array of values of the smoothed values of the 'I' component of the data sample. The value is computed.
EIG	TRACK	Volts Floating Point	The expected value of the EI used for gain control. The value is computed.
EIP	TRACK	Volts Floating Point	The predicted value of the 'I' component of the data sample. The value is computed.
EN	NAVIGATE	Meters Squared Floating Point	Parameter E, page 18 of Ref. 5. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
EP	NAVIGATE	Meters Floating Point	An array of easting planar coordinates for each transmitter. The values are computed.
EP	TRACK SEARCH NEWTRACK	Dimensionless Floating Point	The expected number of Loran pulses accepted. The value is computed and ranges from zero to eight.
EQ	TRACK SEARCH NEWTRACK	Volts Floating Point	An array of values of the smoothed values of the 'Q' component of the data sample. The value is computed.
EQP	TRACK	Volts Floating Point	The predicted value of the 'Q' component of the data sample. The value is computed.
ERR	NAVIGATE	Dimensionless Floating Point	Easting rate ratio to propagation velocity. The value is computed.
ES	TRACK SEARCH SETTLE SID NAVIGATE NEWTRACK	Dimensionless Fixed Point	Station subscript (identifier). The value of ES ranges from zero to ten.
ETA	SID	Dimensionless Floating Point	Parameter (Greek letter eta), page 18 of Ref. 5. The value is computed.
ETAN	NAVIGATE	Dimensionless Floating Point	Parameter (Greek letter eta), page 18 of Ref. 5. The value is computed.
EX	NEWTRACK	Meters Floating Point	An array of easting planar coordinates for each transmitter. The values are computed.
F1	SEARCH	Dimensionless Fixed Point	Flag. F1=0 one time only to set local epoch; otherwise value is 1.
F2	SEARCH	Dimensionless Fixed Point	Flag. F2=0 when 'I' signal component values are larger in amplitude than 'Q' signal component values; otherwise value is one.
F3	SEARCH	Dimensionless Fixed Point	Flag. F3=0 for even labeled GRI, and 1 for odd labeled GRI.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
F4	NAVIGATE	Dimensionless Fixed Point	Flag. F4=0 one time to check sign of square root for each triad; otherwise value is one.
F5	NAVIGATE	Dimensionless Fixed Point	Flag. F5=0 when DTRMT is worse than good limit.
F6	NAVIGATE	Dimensionless Fixed Point	Flag. F6=0 one time after each waypoint change; otherwise value is one.
FFF	SID	Meters Squared Floating Point	Parameter F, page 18 of Ref. 5. The value is computed.
FOC	NAVIGATE	Dimensionless Floating Point	Frequency offset correction. First value set to one, then value is computed.
FN	NAVIGATE	Meters Squared Floating Point	Parameter F, page 18 of Ref. 5. The value is computed.
G	TRACK SEARCH SETTLE NEWTRACK	Decibels Fixed Point	An array of values denoting the gain setting required for each transmitter. The values are computed and lie between GMAX and GMIN.
GAIN	SEARCH	Decibel Fixed Point	Value of GAIN for this transmitter. The value ranges from zero to 100.
GAMMA	SID	Meters Floating Point	Parameter (Greek letter gamma), page 18 of Ref. 5. The value is computed.
GAMMAN	NAVIGATE	Meters Floating Point	Parameter (Greek letter gamma), page 18 of Ref. 5. The value is computed.
GDLIM	NAVIGATE	Dimensionless Floating Point	Goodness limit on geometric dilution of precision. The value is 0.1.
GGG	SID	Meters Squared Floating Point	Parameter G, page 18 of Ref. 5. The value is computed.
GMAX	SEARCH NEWTRACK	Decibel Fixed Point	The maximum value of GAIN. The value is 100.
GMIN	SEARCH	Decibel Fixed Point	The minimum value of GAIN. The value is 0.
GN	NAVIGATE	Meters Squared Floating Point	Parameter G, page 18 of Ref. 5. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
GRI	TRACK SEARCH SID NAVIGATE NEWTRACK	Seconds Floating Point	Length of group repetition interval. Value depends on Loran chain used. Values range from 0.0393 second to 0.1000 second.
H1	SEARCH NEWTRACK	Dimensionless Fixed Point	Temporary storage for parameter P.
H1	SID	Microseconds Floating Point	Temporary storage for parameter T.
H2	SEARCH NEWTRACK	Counts Fixed Point	Temporary storage for parameter C.
H2	SID	Volts/Sec Floating Point	Temporary storage for parameter QR.
H3	SEARCH NEWTRACK	Decibel Fixed Point	Temporary storage for parameter G.
H4	SEARCH NEWTRACK	Dimensionless Fixed Point	Temporary storage for parameter TR.
H5	SEARCH NEWTRACK	Volts Floating Point	Temporary storage for parameter EI.
H6	SEARCH NEWTRACK	Volts Floating Point	Temporary storage for parameter EQ.
H7	SEARCH NEWTRACK	Volts Floating Point	Temporary storage for parameter EP.
H8	SEARCH NEWTRACK	Volts/Sec Floating Point	Temporary storage for parameter IR.
H9	SEARCH NEWTRACK	Volts/Sec Floating Point	Temporary storage for parameter QR.
H10	SEARCH NEWTRACK	Volts Floating Point	Temporary storage for parameter DELTAT.
H11	SEARCH NEWTRACK	Microseconds Floating Point	Temporary storage for parameter T.
HE	NAVIGATE	Radians Floating Point	Heading error. The value is computed.
HHH	SID	Meters Squared Floating Point	Parameter H, page 18 of Ref. 5. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE AND VALUE OF PARAMETER
HN	NAVIGATE	Meters Squared Floating Point	Parameter H, page 18 of Ref. 5. The value is computed.
I	SEARCH SETTLE	Volts Floating Point	A circular array of 'I' signal component data samples. Value is from zero to five.
ILLIM	SETTLE	Volts Floating Point	AGC lower limit voltage. Value is 2.0.
I0	SETTLE	Volts Floating Point	Value of first SETTLE data sample for 'I' signal component. Value ranges from zero to five.
I1	SETTLE	Volts Floating Point	Value of second SETTLE data sample for 'I' signal component. Value ranges from zero to five.
I2	SETTLE	Volts Floating Point	Value of third SETTLE data sample for 'I' signal component. Value ranges from zero to five.
I3	SETTLE	Volts Floating Point	Value of fourth SETTLE data sample for 'I' signal component. Value ranges from zero to five.
ID	SID NAVIGATE NEWTRACK	Dimensionless Fixed Point	An array identifying each transmitting station. Values range from zero to nine.
II	SEARCH	Volts Floating Point	The 'I' signal component input to SEARCH. Value is from zero to five.
II3	SETTLE	Volts Squared Floating Point	Summed squared I3 voltages from a pulse group. The value is computed.
IMAX	TRACK	Volts Floating Point	Maximum value used in AGC voltage window. The value is 2.825.
IMIN	TRACK SEARCH NAVIGATE NEWTRACK	Volts Floating Point	Minimum value used in AGC voltage window. The value is 2.5.
IR	TRACK SEARCH NEWTRACK	Volts/Second Floating Point	The rate of change of the 'I' signal component. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
IT	TRACK	Volts Floating Point	The value of the data sample for the 'I' component of the Loran signal. The value is between zero and five.
ITE	TRACK	Volts Floating Point	The error between predicted and instantaneous values of the 'I' signal component. The value is computed.
IULIM	SETTLE	Volts Floating Point	AGC upper limit voltage. The value is 4.9.
J	SID NEWTRACK	Dimensionless Fixed Point	An index denoting reference transmitter. The values range from 0 to 6. Zero denotes master.
JO	TRACK SEARCH SETTLE NEWTRACK	Dimensionless Fixed Point	An index denoting role of each transmitter and GRI. The value is 0, 8, 16, or 24. 0=master, 8=secondary, both for GRI-A; 16=master, 24=secondary, both for GRI-B.
J1	SID	Dimensionless Fixed Point	An index denoting first secondary transmitter.
J2	SID	Dimensionless Fixed Point	An index denoting the second secondary transmitter.
JA	NAVIGATE	Dimensionless Fixed Point	An index denoting the first secondary transmitter.
JB	NAVIGATE	Dimensionless Fixed Point	An index denoting the second secondary transmitter.
JJ	NEWTRACK	Dimensionless Floating Point	Temporary stored value of parameter J.
JJO	SEARCH	Dimensionless Fixed Point	Temporary stored value of parameter JO.
JR	NAVIGATE NEWTRACK	Dimensionless Fixed Point	An index denoting the reference transmitter.
K	TRACK	Dimensionless Floating Point	The voltage ratio corresponding to the gain change. The value is either 0.8913 or 1.122.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
K3	TRACK SEARCH SID NAVIGATE	Counts/Volt Floating Point	Constant scale factor used in extrapolating exact zero crossing of third cycle. The value is $51.2 \cdot 5 / (3.14159 \cdot 2.5)$.
KK	NAVIGATE	Dimensionless Floating Point	Parameter used in FOC computation. The value is computed.
LA	TRACK	Dimensionless Floating Point	The average-number-of-pulses-accepted low pass filter gain. The value is 0.001.
LEI	SEARCH	Dimensionless Fixed Point	Temporary storage of parameter LII.
LI	SEARCH	Dimensionless Fixed Point	The 100 microsecond time slot counter. Maximum value depends on length of GRI and minimum is zero.
LII	SEARCH	Dimensionless Fixed Point	The location of the first pulse in a pulse group. The value is computed.
LIIS	SEARCH	Dimensionless Fixed Point	Temporary stored value of parameter LIS.
LIMAX	SEARCH	Dimensionless Fixed Point	The maximum number of 100 microsecond intervals in a GRI. The maximum value is 1000.
LIS	SETTLE	Dimensionless Fixed Point	Pulse data selector index. The value ranges from zero to thirty-one.
LISA	SETTLE	Volts Floating Point	An array of consistent 'I' signal component data samples. The value is computed.
LISB	SETTLE	Volts Floating Point	An array of consistent 'Q' signal component data samples. The value is computed.
LJ	TRACK SEARCH SETTLE	Dimensionless Fixed Point	Local counter. The value ranges from one to ten in TRACK, one to 31 in SEARCH, one to ten in SETTLE.
LL	SEARCH SETTLE SID	Dimensionless Fixed Point	Local counter, denotes reference transmitter in SID.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
LL1	SID	Dimensionless Fixed Point	Local index denoting first secondary transmitter.
LL2	SID	Dimensionless Fixed Point	Local index denoting second secondary transmitter.
LM	SEARCH	Dimensionless Fixed Point	Local counter.
LM1	SEARCH	Dimensionless Fixed Point	Local counter.
LN	TRACK SEARCH SID NAVIGATE	Dimensionless Fixed Point	Local counter. The value ranges from zero to eight.
LP	TRACK	Dimensionless Fixed Point	Local counter. The value ranges from zero to seven.
N	TRACK SEARCH NEWTRACK	Counts Fixed Point	Number of the 51.2 MHz clock pulses adjustment to the parameter, C, which is the number of counts from the start of the local GRI to the time the Loran signal is received. The value is computed.
NM	SEARCH	Dimensionless Fixed Point	Number of missed pulses. The value ranges from zero to four.
NR	NEWTRACK	Dimensionless Fixed Point	Local counter denoting number of transmitting stations.
NRR	NAVIGATE	Dimensionless Floating Point	Northing rate ratio to propagation velocity. The value is computed.
NP	NAVIGATE NEWTRACK	Meters Floating Point	An array of Northing planar coordinates for each transmitter. The values are computed.
NX	NEWTRACK	Dimensionless Fixed Point	Local index used in TRACK Status Table.
P	TRACK SEARCH SID NAVIGATE NEWTRACK	Dimensionless Fixed Point	An index denoting role of each transmitter and GRI. The value is 0, 8, 16, or 24. 0=master, 8=secondary, both for GRI-A; 16=master, 24=secondary, both for GRI-B.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
PH	TRACK SEARCH SETTLE	Dimensionless Fixed Point	Array of values of phase codes used to decode the Loran signal. The values are plus or minus 1.
PI	TRACK	Volts Floating Point	The predicted value of the 'I' signal component of the data sample. The value is computed.
PQ	TRACK	Volts Floating Point	The predicted value of the 'Q' signal component of the data sample. The value is computed.
PV	NAVIGATE NEWTRACK	Meters/Micro- second Floating Point	Effective propagation velocity for the triad. The value is computed.
Q	SEARCH SETTLE	Volts Floating Point	A circular array of 'Q' signal component data samples. The value is from zero to five.
Q0	SETTLE	Volts Floating Point	Value of first SETTLE data sample for 'Q' signal component. Value ranges from zero to five.
Q1	SETTLE	Volts Floating Point	Value of second SETTLE data sample for 'Q' signal component. Value ranges from zero to five.
Q2	SETTLE	Volts Floating Point	Value of third SETTLE data sample for 'Q' signal component. The value ranges from zero to five.
Q3	SETTLE	Volts Floating Point	Value of fourth SETTLE data sample for 'Q' signal component. The value ranges from zero to five.
QQ	SEARCH	Volts Floating Point	The 'Q' signal component input to SEARCH. The value is from zero to five.
QQ3	SETTLE	Volts Squared Floating Point	Summed squared Q3 voltages from a pulse group. The value is computed.
QR	TRACK SEARCH 3ID NEWTRACK	Volts/Second Floating Point	The rate of change of the 'Q' signal component. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
QT	TRACK	Volts Floating Point	The value of the data sample for the 'Q' component of the Loran signal. The value is between zero and five.
QTE	TRACK	Volts Floating Point	The error between predicted and instantaneous values of the 'Q' signal component. The value is computed.
RA	SID	Meters Squared Floating Point	Coordinate conversion parameter (Ref. 5). The value is computed.
RAN	NAVIGATE	Meters Squared Floating Point	Coordinate conversion parameter (Ref. 5). The value is computed.
RB	SID	Meters Squared Floating Point	Coordinate conversion parameter (Ref. 5). The value is computed.
RBN	NAVIGATE	Meters Floating Point	Coordinate conversion parameter (Ref. 5). The value is computed.
RTR	NAVIGATE	Meters Floating Point	An array of values listing the ranges from each transmitter to the receiver. The first set of values is ground computed. Following sets are computed.
S	SID	Dimensionless Fixed Point	An array of chronologically ordered transmitter order-of-reception information. The value is computed.
SDEL	SID	Dimensionless Floating Point	Parameter (small Greek letter delta) page 18 of Ref. 5. The value is computed.
SDELN	NAVIGATE	Dimensionless Floating Point	Parameter (small Greek letter delta) page 18 of Ref. 5. The value is computed.
SLAT	NEWTRACK	Dimensionless Floating Point	Sine of the latitude of the centroid of the triad used for navigation. The value is computed.
SLAT	SID	Dimensionless Floating Point	Sine of the latitude of the centroid of all transmitting stations of a chain. The value is computed.
SLATO	NAVIGATE	Dimensionless Floating Point	Sine of the latitude of the centroid of the triad used for navigation. The value is computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
SLON	NEWTRACK	Dimensionless Floating Point	Sine of the longitude of the centroid of the triad used for navigation. The value is computed.
SLON	SID	Dimensionless Floating Point	Sine of the longitude of the centroid of all transmitting stations of a chain. The value is computed.
SLONO	NAVIGATE	Dimensionless Floating Point	Sine of the longitude of the centroid of the triad used for navigation. The value is computed.
SM	SEARCH NEWTRACK SID	Dimensionless Fixed Point	Number of stations in TRACK. The value ranges from zero to ten.
SPSIA	NAVIGATE	Dimensionless Floating Point	Sine of the azimuth of the receiver with respect to transmitter 'A' location. The value is computed.
SPSIB	NAVIGATE	Dimensionless Floating Point	Sine of the azimuth of the receiver with respect to transmitter 'B' location. The value is computed.
SPSIR	NAVIGATE	Dimensionless Floating Point	Sine of the azimuth of the receiver with respect to the reference transmitter 'R'. The value is computed.
SQ	SID	Meters Squared Floating Point	Radical term of parameter (Greek letter theta sub M), page 18 of Ref. 5. The value is computed.
SQN	NAVIGATE	Meters Squared Floating Point	Radical term of parameter (Greek letter theta sub M), page 18 of Ref. 5. The value is computed.
STC	NAVIGATE	Dimensionless Floating Point	Sine of true course. The value is computed.
SUMITE TRACK		Volts Floating Point	The sum of the ITE errors for the pulses. The value is computed.
SUMQTE TRACK		Volts Floating Point	The sum of the QTE errors for the pulses. The value is computed.
SS	NEWTRACK	Dimensionless Fixed Point	Local index used in TRACK Status Table.
SWITCH	SID	Dimensionless Fixed Point	SWITCH=0 when triad is identified, otherwise one.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
SX	NEWTRACK	Dimensionless Fixed Point	Local index used in TRACK Status Table.
T	TRACK SEARCH SID NAVIGATE NEWTRACK	Microseconds Floating Point	An array of values denoting time-of-arrival of Loran signal from the start of a local GRI. The values are computed.
TAU	TRACK	Seconds Floating Point	Time between pulses. The value is computed.
TD	SID NAVIGATE	Microseconds Floating Point	An array of time differences. The values are computed.
TDA	NAVIGATE	Microseconds Floating Point	The 'A' time difference for a way-point with respect to the reference transmitter. The values are computed.
TDB	NAVIGATE	Microseconds Floating Point	The 'B' time difference for a way-point with respect to the reference transmitter. The values are computed.
TDW	NAVIGATE	Microseconds Floating Point	A ground computed array of time differences for each waypoint with respect to the master transmitter.
THETA A	NAVIGATE	Meters Floating Point	Range from receiver to first secondary transmitter. The value is computed.
THETA B	NAVIGATE	Meters Floating Point	Range from receiver to second secondary transmitter. The value is computed.
THETA R	SID NAVIGATE	Meters Floating Point	Range from receiver to reference transmitter. The value is computed.
TI	SEARCH	Volts Floating Point	An array of voltages of detected pulses of 'I' signal component. The values are computed.
TIN	NAVIGATE NEWTRACK	Microseconds Floating Point	An array of values denoting time-of-arrival of Loran signal from the start of a local GRI. The value is computed.
TQ	SEARCH	Volts Floating Point	An array of voltages of detected pulses of 'Q' signal component. The values are computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
TR	SEARCH SETTLE SID NAVIGATE NEWTRACK	Dimensionless Fixed Point	An array denoting the TRACK status of each transmitter. 0=SEARCH, 1=SETTLE, 2=TRACK on unidentified station, 3=TRACK, 4=TRACK spoofer.
U	SEARCH	Volts Floating Point	Phase decoded data accumulator. 'I' value ranges from 0 to 40.
V	SEARCH	Volts Floating Point	Phase decoded data accumulator. 'Q' value ranges from 0 to 40.
VMIN	SEARCH	Volts Floating Point	Data sample pulse detection threshold. The value is 0.1.
W	SEARCH	Volts Floating Point	Difference between present data sample and stored data sample.
WP	NAVIGATE	Dimensionless Fixed Point	An index denoting the waypoint number.
X	SEARCH SETTLE	Volts Floating Point	Interpolated initial value of EQ in SEARCH, temporary value of 'I' data in SETTLE. The values are computed.
X	SID	Meters Floating Point	An array of planar coordinates for each transmitter. The values are computed.
XEOC	NAVIGATE NEWTRACK SID	Meters Floating Point	An array of X-direction earth orthogonal coordinates for each transmitter. The values are ground computed.
XI	SID	Meters Squared Floating Point	Parameter (Greek letter xi), page 18 of Ref. 5. The value is computed.
XIN	NAVIGATE	Meters Squared Floating Point	Parameter (Greek letter xi), page 18 of Ref. 5. The value is computed.
XR	SID NAVIGATE NEWTRACK	Meters Floating Point	X coordinate of receiver position. The value is computed.
XRC	SID	Meters Floating Point	X coordinate of receiver position. The value is ground computed.
XRR	NAVIGATE	Meters/Second Floating Point	The speed of the receiver in the X direction. The value is computed.
XW	NAVIGATE	Meters Floating Point	An array of X coordinates of each waypoint. The values are computed.

Table D-1 (Continued)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
XXO	NAVIGATE	Meters Floating Point	The X coordinate of the centroid of the triad used for navigation. The value is computed.
XXO	SID	Meters Floating Point	The X direction coordinate of the centroid of all the transmitting stations of a chain. The value is computed.
Y	SEARCH SETTLE	Volts Floating Point	Interpolated initial value of E1 in SEARCH, temporary value of 'Q' data in SETTLE. The values are computed.
Y	SID	Meters Floating Point	An array of planar coordinates for each transmitter. The values are computed.
YEOC	NAVIGATE NEWTRACK SID	Meters Floating Point	An array of Y-direction earth orthogonal coordinates for each transmitter. The values are ground computed.
YR	SID NAVIGATE	Meters Floating Point	Y coordinate of receiver position. The value is computed.
YRO	SID	Meters Floating Point	Y coordinate of receiver position. The value is ground computed.
YRR	NAVIGATE	Meters/Second Floating Point	The speed of the receiver in the Y direction. The value is computed.
YW	NAVIGATE	Meters Floating Point	An array of Y coordinates for each waypoint. The values are computed.
YYO	NAVIGATE	Meters Floating Point	The Y coordinate of the centroid of the triad used for navigation. The value is computed.
YYO	SID	Meters Floating Point	The Y coordinate of the centroid of all the transmitting stations of a chain. The value is computed.
Z	SEARCH	Dimensionless Fixed Point	Absolute value of parameters U and V. The values are computed.
ZEOC	NAVIGATE NEWTRACK SID	Meters Floating Point	An array of Z-direction earth orthogonal coordinates for each transmitter. The values are ground computed.

Table D-1 (Concluded)

Subroutine Nomenclature

NAME	USED IN ROUTINE	DIMENSIONS AND SCALE ATTRIBUTE	DEFINITION, USE, AND VALUE OF PARAMETER
ZETAC	SID	Meters Floating Point	Parameter (Greek letter zeta), page 18 of Ref. 5. The value is computed.
ZETAN	NAVIGATE	Meters Floating Point	Parameter (Greek letter zeta), page 18 of Ref. 5. The value is computed.
ZZO	NAVIGATE	Meters Floating Point	The Z coordinate of the centroid of the triad used for navigation. The values are computed.
ZZO	SID	Meters Floating Point	The Z coordinate of the centroid of all the transmitting stations of a chain. The value is computed.

Appendix E

SUBROUTINE SEARCH

INTRODUCTION

The Search subroutine described in this appendix was implemented in PL/I digital computer language and successfully tested. See Appendix D for nomenclature.

PURPOSE

The purpose of Search is to detect Loran pulse groups in the data measured by the Digital Measurement Unit (DMU) and to locate the groups, in time, in the Group Repetition Interval (GRI).

IMPLEMENTATION

In order to complete this task, there are five subtasks which must be performed. When any one of the subtasks cannot be completed, or when all five are completed, program control is returned immediately to the Control program. The five subtasks are:

1. Detection of a pulse.
2. Detection of a pulse group (at least six pulses of the eight available must have been detected).
3. Detection and identification of the Loran pulse group phase code.
4. Detection of the absence of cross rate interference (two pulse groups in time proximity but moving with respect to each other).
5. Filing of data pertinent to the new pulse group detections.

When these subtasks are successfully completed, the Search subroutine assigns a table of values for that detected pulse group in preparation for the execution of subroutine Settle, Track, etc.

The input data to Search consists of two data points from the DMU every 100 microseconds. The data points consist of one I and one Q value of the Loran signal components and are identified as I (amplitude) data and Q (phase) data in Search.

Each pair of input values (one I and one Q value) is subjected to the first subtask, the pulse detection test. If the data fail the test, a zero is stored in the I circular array and a zero is stored in the Q circular array. Control of the program is passed immediately to the Control program. If the data pass the test, the values of I and Q are stored in the circular arrays.

When a pulse has been detected, subtask 2 commences and the circular arrays are scanned in order to find at least six of the eight possible pulses in a pulse group. If six pulses of the group are not detected, program control is returned immediately to the Control program.

When six or more pulses in a pulse group have been detected, subtask 3 tests each detected pulse to ascertain whether the group consists of a master pulse group (GRI-A or GRI-B phase code interval), a secondary pulse group (GRI-A or GRI-B phase code interval), or none of these. If the pulse group does not fall within one of these four categories, program control is returned immediately to the Control program.

When the pulse group passes the phase code test, subtask 4 performs a cross rate test to make certain that two consecutive pulse group detections are not two different transmitters with different GRIs. Only if the two detections occur at the same time into the GRI and are of opposite phase code, can this test be passed.

As with the previous tests, when the cross rate test fails, control returns to the Control program immediately.

When the cross rate test is passed, subtask 5 tests the pulse group detection time of the GRI. If the time of occurrence of the two detections is within ± 200 microseconds, the second pulse group is ignored and control of the program returns to the Control program. If this test is not passed, all pertinent data are stored in the track table in chronological order in the local GRI and control returns to the Control program.

The Search subroutine listing and logical flow chart are shown in Figs. E-1 and E-2, respectively.

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01/07/77	INPUT LISTING	AUTIFLOW CHART SET - SEARCH
PLATE NUMBER	LIST/PAGE	
CARD NO	****	CONTENTS
1		OPTI(0) PRINT(0),TEXT(2,7),RECOMMENTS
2		SEARCH PROCEDURES
3		DECLARE I
4		I(0:9) INIT(0:9)
5		I(10:19) INIT(0:9)
6		I(20:29) INIT(0:9)
7		I(30:39) INIT(0:9)
8		I(40:49) INIT(0:9)
9		I(50:59) INIT(0:9)
10		I(60:69) INIT(0:9)
11		I(70:79) INIT(0:9)
12		I(80:89) INIT(0:9)
13		I(90:99) INIT(0:9)
14		I(100:109) INIT(0:9)
15		I(110:119) INIT(0:9)
16		I(120:129) INIT(0:9)
17		I(130:139) INIT(0:9)
18		I(140:149) INIT(0:9)
19		I(150:159) INIT(0:9)
20		I(160:169) INIT(0:9)
21		I(170:179) INIT(0:9)
22		I(180:189) INIT(0:9)
23		I(190:199) INIT(0:9)
24		I(200:209) INIT(0:9)
25		I(210:219) INIT(0:9)
26		I(220:229) INIT(0:9)
27		I(230:239) INIT(0:9)
28		I(240:249) INIT(0:9)
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30		I(260:269) INIT(0:9)
31		I(270:279) INIT(0:9)
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34		I(300:309) INIT(0:9)
35		I(310:319) INIT(0:9)
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39		I(350:359) INIT(0:9)
40		I(360:369) INIT(0:9)
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45		I(410:419) INIT(0:9)
46		I(420:429) INIT(0:9)
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291		I(2870:2879) INIT(0:9)

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01/04/73      INPUT LISTING      AUTO LOW CHART SET - SEARCH

CARD NO      ***      CONTENTS      ****

187          GO TO SRM1
188
189          SRA1: /* PULSE DETECTED */
190          D*011
191
192          /* MONITOR RD INDEX CONTROL */
193          IF D*010 THEN GO TO SRA1 ELSE GO TO SPQ1
194          SRA1: D*01
195
196          SRA2: /* ENTER VALUE INTO CIRCULAR TABLE */
197          L*0111
198          W*011*01
199
200          /* SET INDICES */
201          L*01
202          NM*01
203
204          /* STORE DETECTED PULSES INTO EIGHT ELEMENT TABLE */
205          T*011*11
206          T*011*01
207          D*01
208
209
210
211
212
213
214          /* START PULSE GROUP DETECTION */
215          /* CHECK FOR THE LARGER OF THE I AND Q DATA */
216          IF ABS(I11) > ABS(Q11) THEN GO TO SRA1
217          P*01
218          GO TO SRA1
219          SRA1: P*01
220
221          SRA2: /* DECREMENT PULSE COUNTER */
222          D*0101
223
224          /* MONITOR RD INDEX CONTROL */
225          IF D*010 THEN GO TO SRA1 ELSE GO TO SRA1
226          SRA2: T*0101
227          SRA2: L*01*01
228          IF P*010 THEN GO TO SRA1
229
230          /* CHECK FOR AMPLITUDE CONSISTENCY */
231          W*ABS(I*011)-ABS(Q*011)
232          GO TO SRA1
233          SRA1: W*ABS(I*011)-ABS(Q*011)
234
235          SRA1: /* AMPLITUDE CONSISTENCY TEST */
236          IF W < DELTA THEN GO TO SRA2
237
238          /* NOT CONSISTENT - SET 8 ELEMENT TABLE ENTRIES TO ZERO */
239          T*011*01
240          T*011*01
241
242          /* COUNT NUMBER OF PULSES MISSED */
243          SRA1: SRA1*11
244          GO TO SRA1
245
246          SRA2: /* CONSISTENT - SET 8 ELEMENT TABLE EQUAL TO VALUE OF PULSE */
247          T*011*011
248          T*011*011
249
250          SRA3: /* NUMBER OF MISSED PULSES CHECK */
251          IF SRA1 THEN GO TO SRA3
252          IF L*010 THEN GO TO SRA1 ELSE GO TO SPT1
253
254          SRA3: /* TOO MANY MISSES - PULSE GROUP DETECTION FAILED */
255          SRA3: D*01
256          GO TO SRA2
257
258
259
260
261          SRA4: /* PULSE GROUP DETECTED */
262          /* START PHASE CODE IDENTIFICATION */
263          /* SET INDICES FOR DETECTION OF MASTER A */
264          J*01
265          L*012
266          L*010
267          J*01
268          SRA4: L*011
269
270          SRA5: /* INITIALIZE ACCUMULATORS */
271          U*01
272          V*01
273
274          SRA6: /* ACCUMULATE PHASE DECODED DATA */
275          U*V*H*H*J*SIGN*T*011
276          V*V*H*H*J*SIGN*T*011
277          IF L*017 THEN GO TO SRA11
278          L*011*11
279          L*011*11
280          GO TO SRA6
281
282          SRA11: /* DATA ACCUMULATED */
283          IF P*010 THEN GO TO SRA6
284          Z*0101
285          GO TO SRA6
286          Z*0101
287
288          SRA11: /* PHASE CODE TEST */
289          IF Z < R-NM THEN GO TO SRA6 ELSE GO TO SRA4
290
291          SRA11: /* PHASE CODE TEST FAILED */
292          L*011-11
293
294          /* PHASE CODE ADJUSTMENT FOR MISSING LEADING PULSES */
295          IF L*012 THEN GO TO SRA11
296          IF L*011 THEN GO TO SRA11
297
298          /* PHASE CODE TEST FAILED, TRY ALTERNATIVE PHASE CODES */
299          IF L*013 THEN GO TO PCTF
300

```

Fig. E-1 SEARCH SUBROUTINE LISTING (continued)

01/08/73

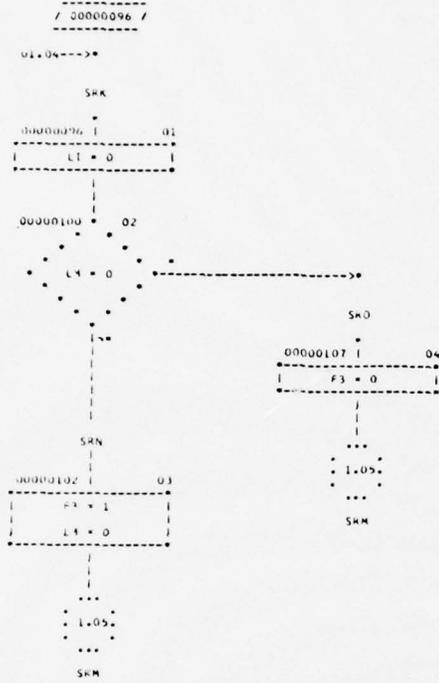
INPUT LISTING

AUTOFLOW CHART SET - SEARCH

CARD NO	****	CONTENTS	****
331		GO TO SRJ1	
332	SF AP1	H1=PIES11	
333		H2=CI ES11	
334		H3=GI ES11	
335		H4=TR IES11	
336		H5=EI ES11	
337		H6=EI ES11	
338		H7=EI ES11	
339		H8=IR IES11	
340		H9=QR IES11	
341		H10=DEL TAT IES11	
342		H11=TI ES11	
343		ES=ES+11	
344		PI ES11=H11	
345		CI ES11=H21	
346		GI ES11=H31	
347		TR IES11=H41	
348		EI ES11=H51	
349		EI ES11=H61	
350		EI ES11=H71	
351		IR IES11=H81	
352		QR IES11=H91	
353		DEL TAT IES11=H101	
354		TI ES11=H111	
355		ES=ES-21	
356		IF ES > 0 THEN GO TO SRAA01	
357	SRAA01	SW=SW+11	
358		ES=ES+11	
359		GO TO SRAA51	
360	END1	RETURN	
361		END SEARCH1	

Fig. E-1 SEARCH SUBROUTINE LISTING, (concluded)

CHART TITLE - PROCEDURE SEARCH



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Fig. E-2 SEARCH SUBROUTINE FLOW CHART (continued)

CHART TITLE - PROCEDURE SEARCH

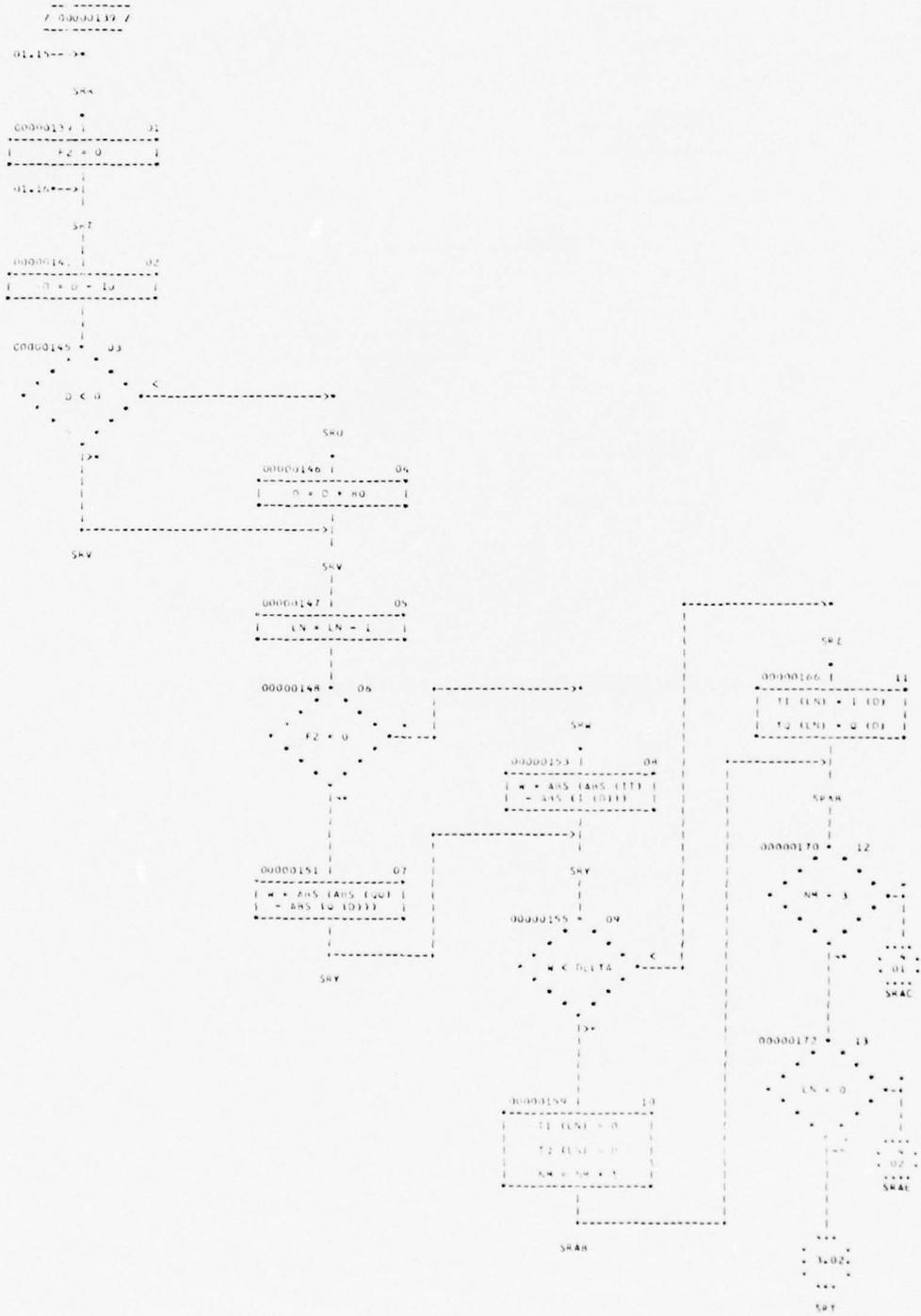


Fig. E-2 SEARCH SUBROUTINE FLOW CHART (continued)

CHART TITLE - PROCEDURE SEARCH

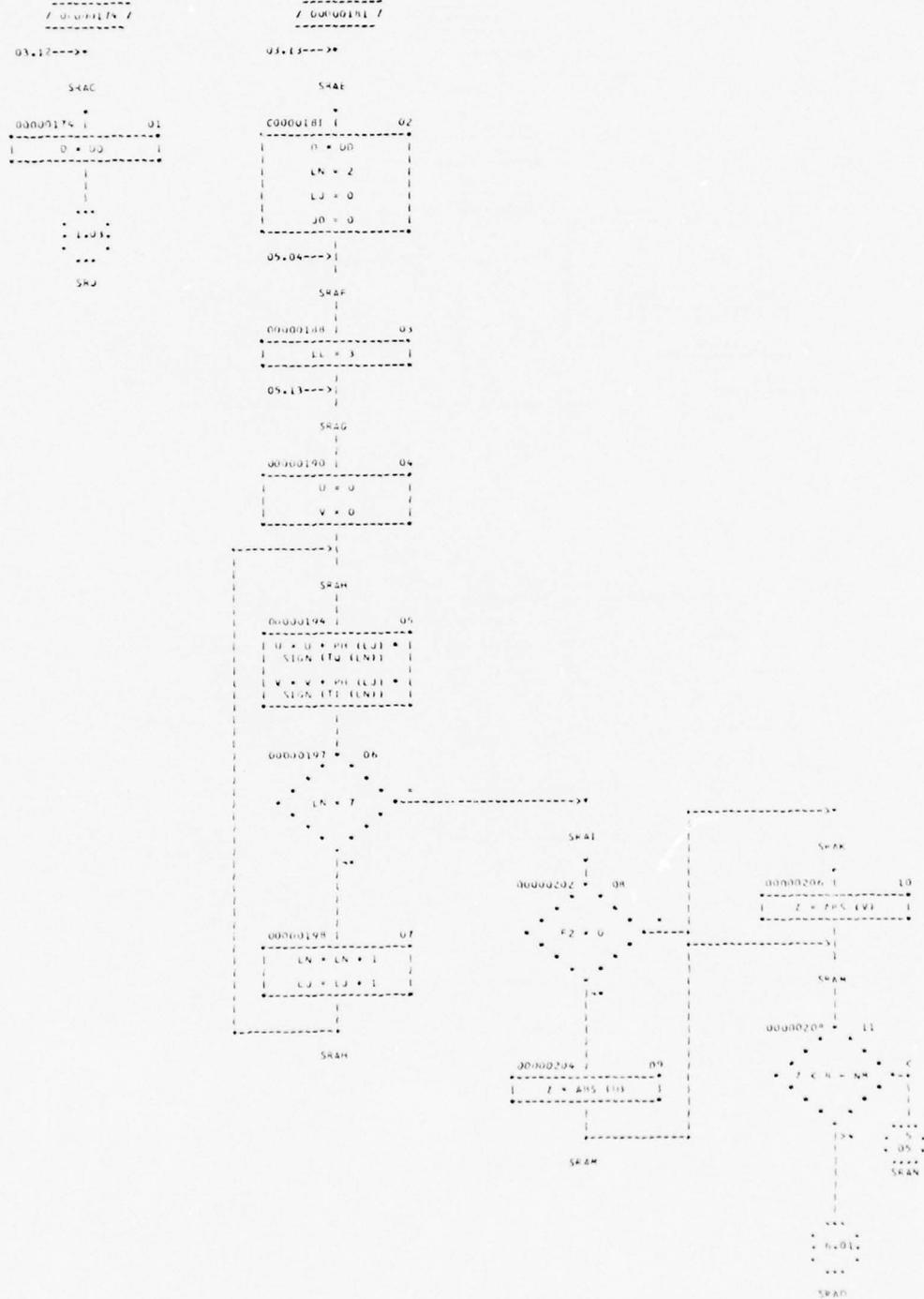


Fig. E 2 SEARCH SUBROUTINE FLOW CHART (continued)

CHART TITLE - PROCEDURE SEARCH

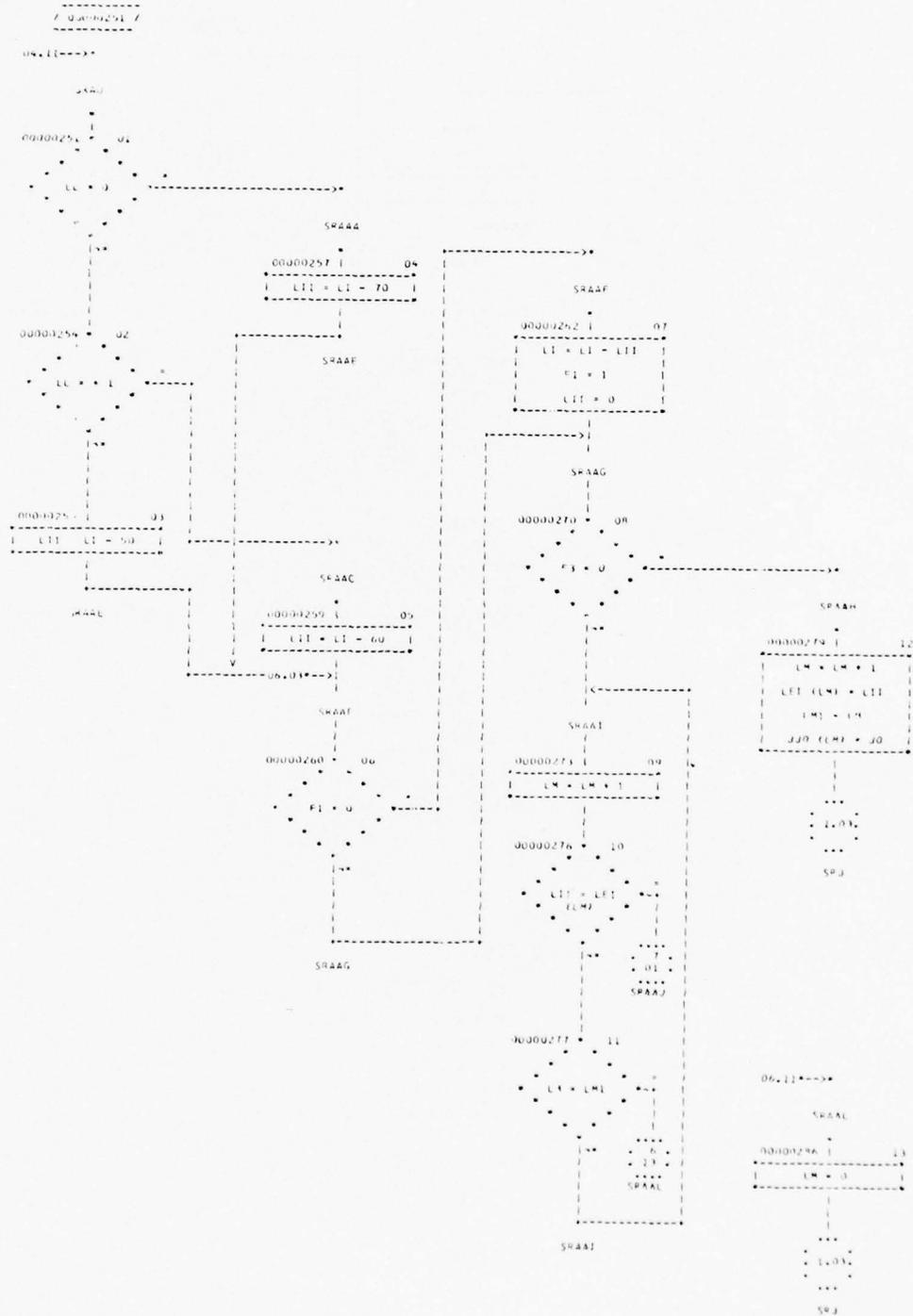


Fig. E-2 SEARCH SUBROUTINE FLOW CHART (continued)

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01/06/73

AUTOFLOW CHART SET - SEARCH

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CHART TITLE - PROCEDURE SEARCH

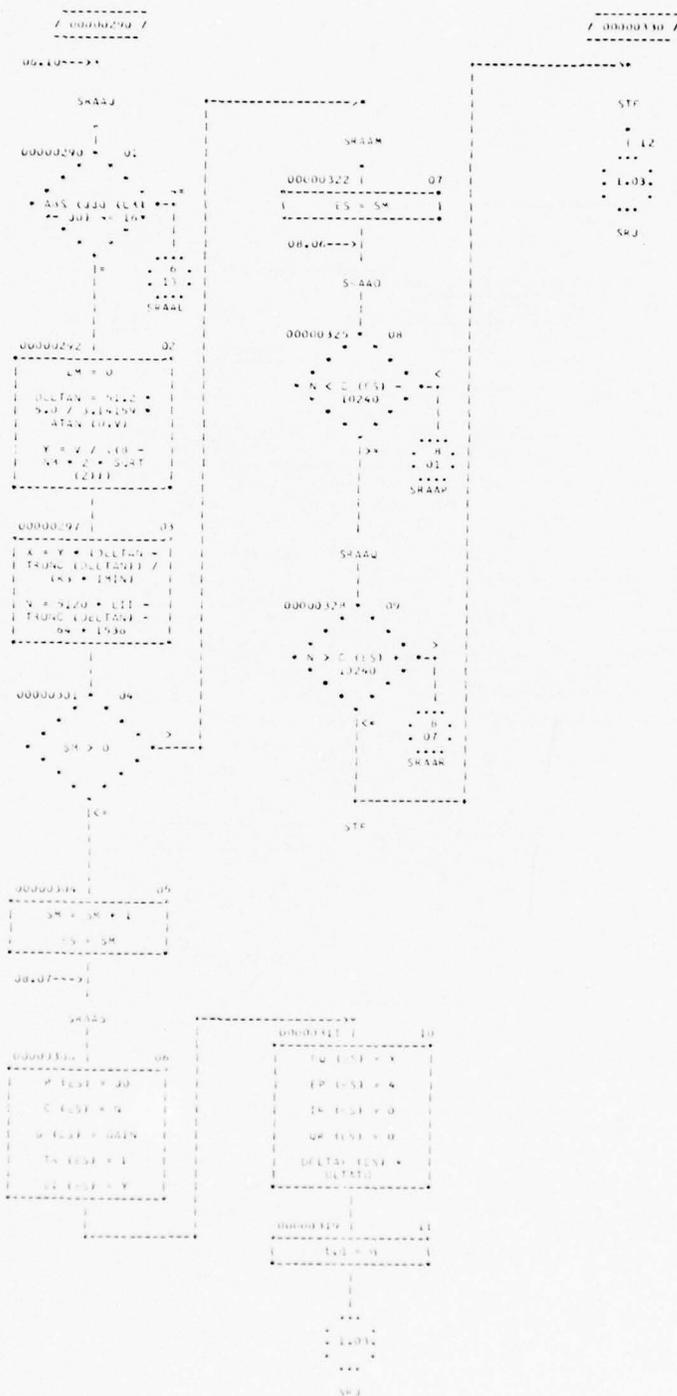


Fig. E-2 SEARCH SUBROUTINE FLOW CHART (continued)

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01/04/77

AUTOFLOW CHART SET - SEARCH

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SEARCH SUBROUTINE FLOW CHART

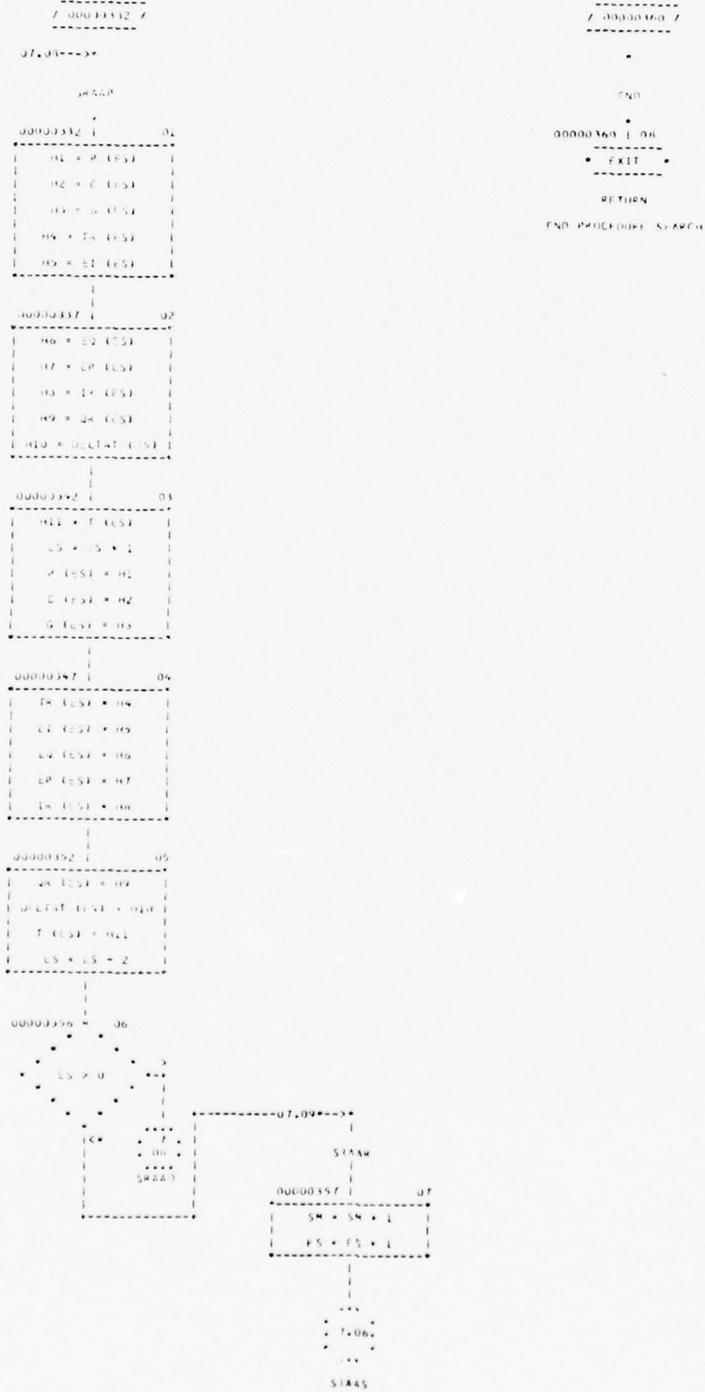


Fig. E-2 SEARCH SUBROUTINE FLOW CHART (concluded)

Appendix F SUBROUTINE SETTLE

INTRODUCTION

The Settle subroutine described in this appendix was implemented in PL/I digital computer language and successfully tested. See Appendix D for nomenclature.

PURPOSE

The purpose of Settle is to position the two Track data sample points at 30 and 32.5 microseconds into the Loran pulse.

IMPLEMENTATION

To accomplish this task, Settle moves a group of eight data sample points, which are initially positioned by Search, forward or backward on the pulse as required until the sample points are located on the first four cycles of the pulse. The position, in time, of the third cycle is then transmitted to Track which then continues to position its pair of sample points so that one precisely tracks the zero crossing at the end of the third cycle of the pulse. The other data point samples the amplitude of the positive half cycle of the fourth cycle.

Settle has the following six subtasks to perform before its main function is completed:

1. Removal of the Loran pulse group phase code.
2. Comparison of the I data for consistency within a tolerance.
3. Comparison of the Q data for consistency within the same tolerance.
4. Summation of both paired sets of four sampled voltages over all accepted pulses.

5. Comparison of summed, squared data to detect the pulse envelope leading edge.
6. Comparison of ratios of summed, squared data to detect pulse shape at the location of the sample points.

When these tasks have been executed, Settle returns control to the control program immediately after setting two parameters in the Track status table.

The input data to Settle consists of four pairs of amplitude and phase data from each Loran pulse. The four pairs of voltages are from four consecutive cycles of a Loran pulse. Each pair of voltage sample points is separated in time by 10 microseconds. Since there are eight pulses per pulse group in Loran-C, Settle operates on two sets of 32 data points per pulse group.

The transmitted pulse group phase code is removed, as the first subtask, for all 32 pairs of input data points.

When all of the data have been decoded, the I (amplitude) data are compared among the pulses for a pulse-to-pulse consistency test on the amplitudes. If any data are inconsistent with respect to the rest of the data, all of the data from the pulse associated with the inconsistent point are deleted from further consideration. Data from at least four pulses (I values) must be consistent, within the tolerance with respect to each other, or this second subtask is deemed to have failed. Control then returns immediately to the Control program.

When subtask 2 is successfully completed, subtask 3 begins. This task performs the same type of comparisons, and pulse rejections, except now the Q (phase) data are tested for only those pulses that passed the I test. The same criteria apply for success and failure as before.

Subtask 4 consists of summing the square of the data from each of the four amplitude samples from all of the pulses that were not rejected due to inconsistencies. I0 is the sum of the first squared voltage samples on four or more pulses; I1 is the sum of the second squared voltage samples on those pulses (10 microseconds later in time); I2 is the sum of the third squared voltage samples on those pulses (10 microseconds later in time than I1); and I3 is the sum of the fourth, and last, squared voltage samples on those pulses (10 microseconds later in time than I2).

When all of the amplitude data have been squared and summed, subtask 5 begins. This task consists of detection of the slope of the envelope of the pulse. If the envelope slope is negative, action is taken to move the group of Settle sample points toward the leading edge of the pulse on the next data taking cycle of the Digital Measurement Unit. If the group of sample points is detected as having progressed forward of the leading edge of the pulse, action is taken to position the group wholly on the leading edge following the next Settle data taking cycle. Completion of this task and progression to task 6 occurs only when the whole group of sample points is located on the leading edge of the pulse. Otherwise, the time position of the sample point is adjusted so that on the next data taking cycle, either that goal is achieved or another adjustment is made. Until the goal is achieved, Settle returns control to the Control program after each adjustment.

Lastly, subtask 6 adjusts the position of the group of sample points on the pulse so that they occur properly located on the first four cycles of the pulse. This is accomplished as before, with ratios of the values of the summed, squared data samples determining the final exact position.

The Settle subroutine listing and logical flow chart are shown in Figs. F-1 and F-2 respectively.

01/03/73

INPUT LISTING

AUTOFLOW CHART SET - SETTLE

CARD NO	****	CONTENTS	****
109		IF L15C3 THEN GO TO SF61 ELSE GO TO SE61	
110			
111			
112			
113			
114			
115			
116	SE61	/* Q CONSISTENCY TEST */	
117		/* FOUR OR MORE I SAMPLES ARE CONSISTENT */	
118		/* SELECT Q SAMPLE FOR COMPARISON TO ALL OTHER Q SAMPLES */	
119		AM=AS1	
120	SF61	BS=Q1	
121		LL=Q1	
122		L15=L15A(EAS1)	
123		AAS=AS1	
124		L15B(LB5)=L151	
125		X=L151	
126	SE61	AS=AS-11	
127		IF AS=Q THEN GO TO SE61 ELSE GO TO SE61	
128	SE61	AS=AS+AM+11	
129			
130	SE61	/* SELECT SAMPLE FOR COMPARISON */	
131		L15=L15A(K1)	
132		Y=L151	
133			
134		/* COUNT COMPARISONS */	
135		LL=LL+1	
136			
137		/* COMPARE TWO SAMPLE VOLTAGES FOR CONSISTENCY WITHIN DELTAS	
138		VOLTS */	
139		IF ABS(X-Y) < DELTAS THEN GO TO SE61 ELSE GO TO SE61	
140			
141	SE61	/* Q CONSISTENT */	
142		/* COUNT CONSISTENT COMPARISONS */	
143		BS=BS+1	
144		L15B(LB5)=L151	
145	SE61	IF LL=AM THEN GO TO SE61 ELSE GO TO SE61	
146			
147	SE61	/* SAME NUMBER OF COMPARISONS COMPLETED FOR Q AS WERE	
148		CONSISTENT FOR I */	
149		IF BS=2 THEN GO TO SE61	
150		AS=AS-11	
151		IF AS=Q THEN GO TO SF61 ELSE GO TO SE61	
152	SE61	BM=BS1	
153			
154			
155			
156			
157			
158			
159	SE61	/* VOLTAGE PROF. SUMMATION */	
160		/* CLEAR SAMPLE SUMMERS */	
161		I1=I1+L151	
162	SF61	L15=L15B(LB5)	
163			
164		/* ALL ON FOURTH I SAMPLE */	
165		IF ABS(I1-L151) >= JULIM THEN GO TO BBY1	
166		IF ABS(I1-L151) <= ILLIM THEN GO TO BBY1 ELSE GO TO BBNN1	
167			
168	BBY1	/* DECREASE GAIN BY A DR */	
169		G151=G151-1	
170		GO TO SF61	
171			
172	BBNN1	/* INCREASE GAIN BY A DR */	
173		G151=G151+1	
174		GO TO SF61	
175			
176	BBNN1	/* SUM CONSISTENT FOURTH I AND Q SAMPLE VOLTAGES */	
177		I3=I3+I1L151	
178		Q3=Q3+Q1L151	
179			
180		/* STORE SUMMATION FOR FINE PHASE ADJUSTMENT */	
181		I13=I3	
182		Q13=Q3	
183		BS=BS-11	
184		IF BS=Q THEN GO TO SF61 ELSE GO TO SE61	
185	SE61	BS=BS+1	
186			
187	SEAA1	/* SUM CONSISTENT THIRD I AND Q SAMPLE VOLTAGES */	
188		L15=L15B(LB5)-11	
189		I2=I2+I1L151	
190		Q2=Q2+Q1L151	
191		BS=BS-11	
192		IF BS=Q THEN GO TO SF61 ELSE GO TO SEAA1	
193	SF61	BS=BS+1	
194			
195	SEAH1	/* SUM CONSISTENT SECOND I AND Q SAMPLE VOLTAGES */	
196		L15=L15B(LB5)-21	
197		I1=I1+I1L151	
198		Q1=Q1+Q1L151	
199		BS=BS-11	
200		IF BS=Q THEN GO TO SF61 ELSE GO TO SEAH1	
201	SEAC1	BS=BS+1	
202			
203	SEAD1	/* SUM CONSISTENT FIRST I AND Q SAMPLE VOLTAGES */	
204		L15=L15B(LB5)-31	
205		I0=I0+I1L151	
206		Q0=Q0+Q1L151	
207		BS=BS-11	
208		IF BS=Q THEN GO TO SF61 ELSE GO TO SEAD1	
209			
210			
211			
212			
213			
214	SEAE1	/* FINE PHASE ADJUSTMENT */	
215		IMP1=Q03/I131	
216		L15=L151-TRUNC(I1,24573,1415926*ATAN(IMP1))	
217			
218			
219		/* COMPUTE MEASURE OF RESULTANT VOLTAGE */	

Fig. F-1 SETTLE SUBROUTINE LISTING (continued)

CHART TITLE - PROCEDURE SETTLE

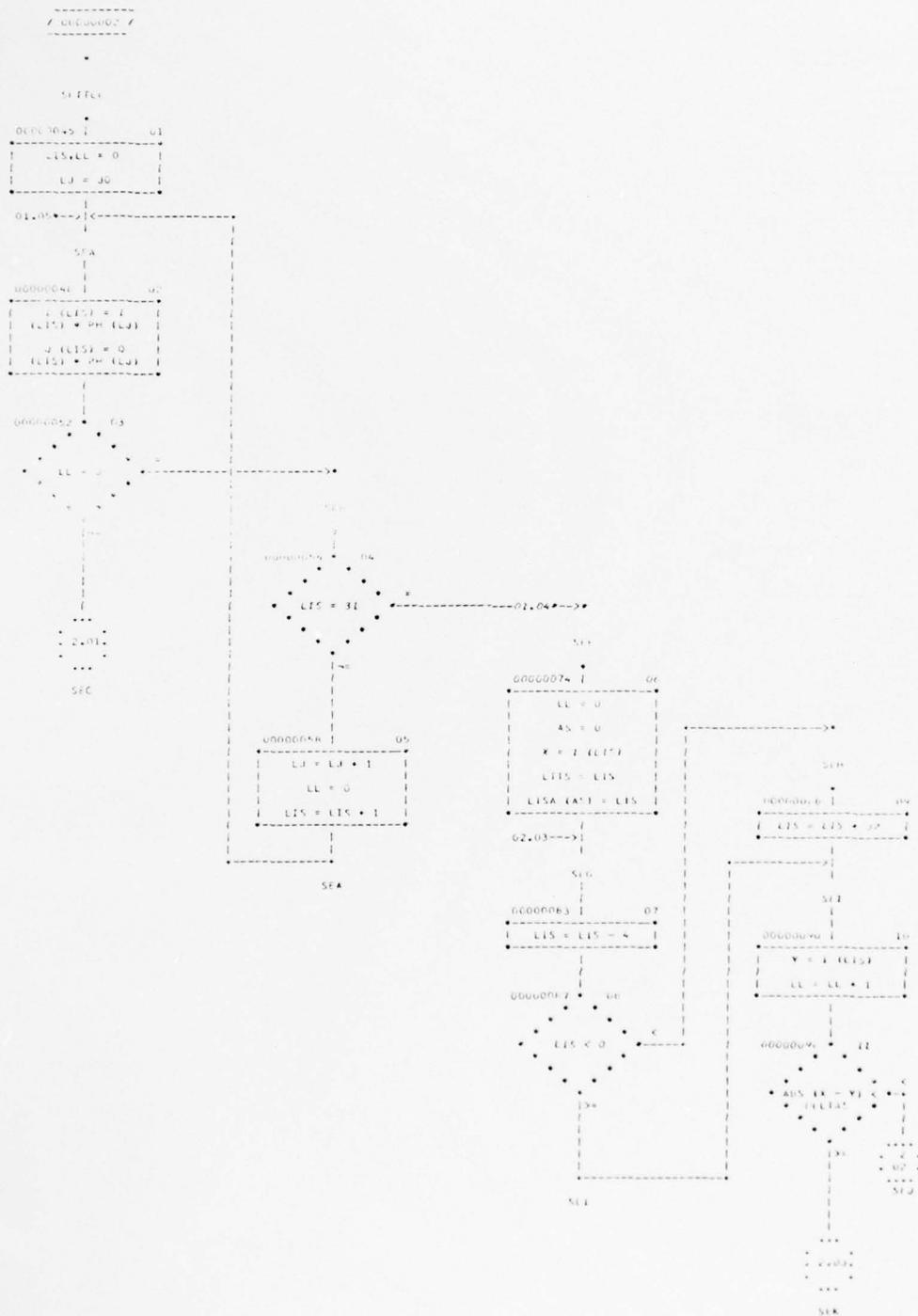


CHART TITLE - PROCEDURE SETTLE

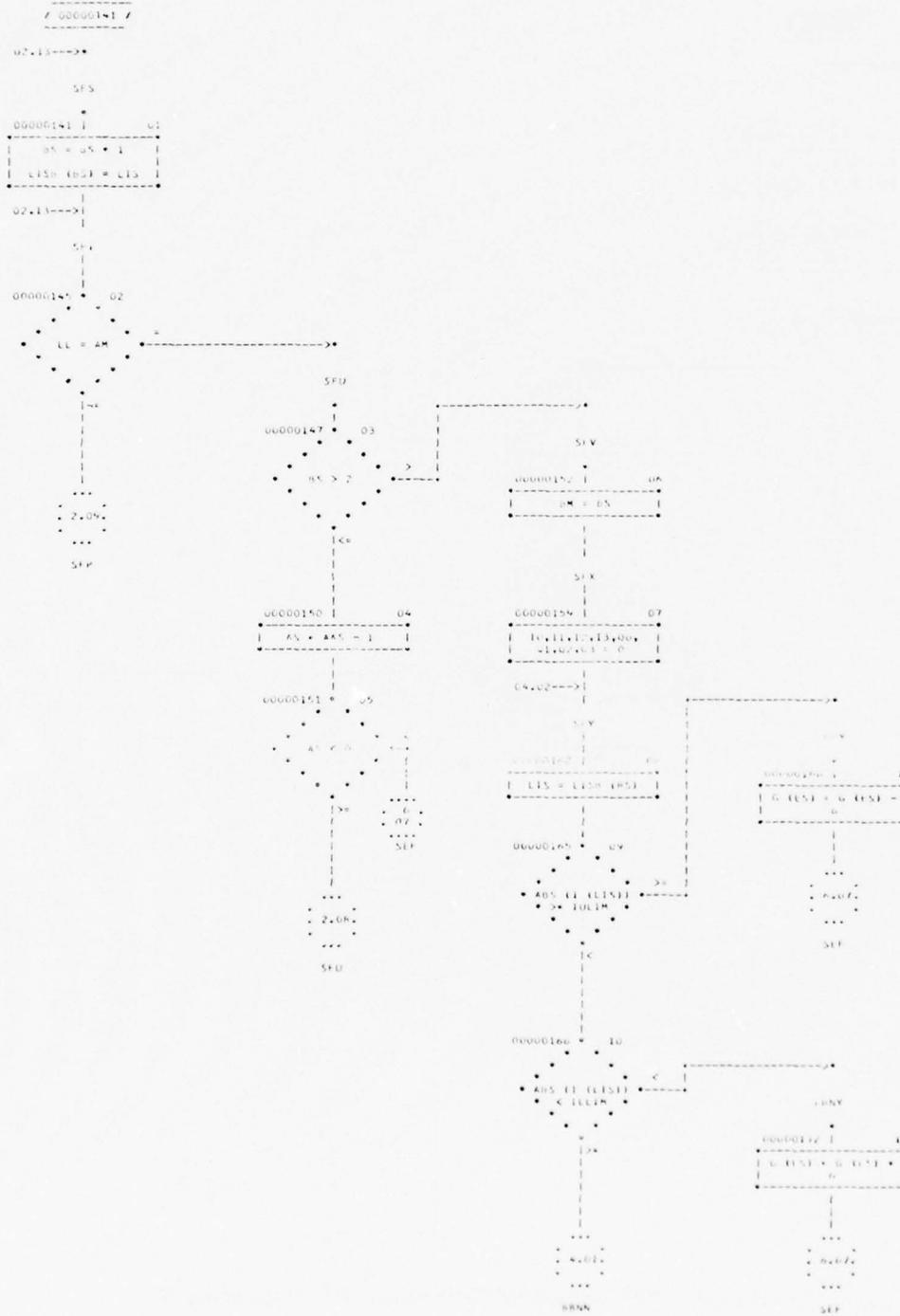


Fig. F-2 SETTLE SUBROUTINE FLOW CHART (continued)

CHART TITLE - PROCEDURE SETTLE

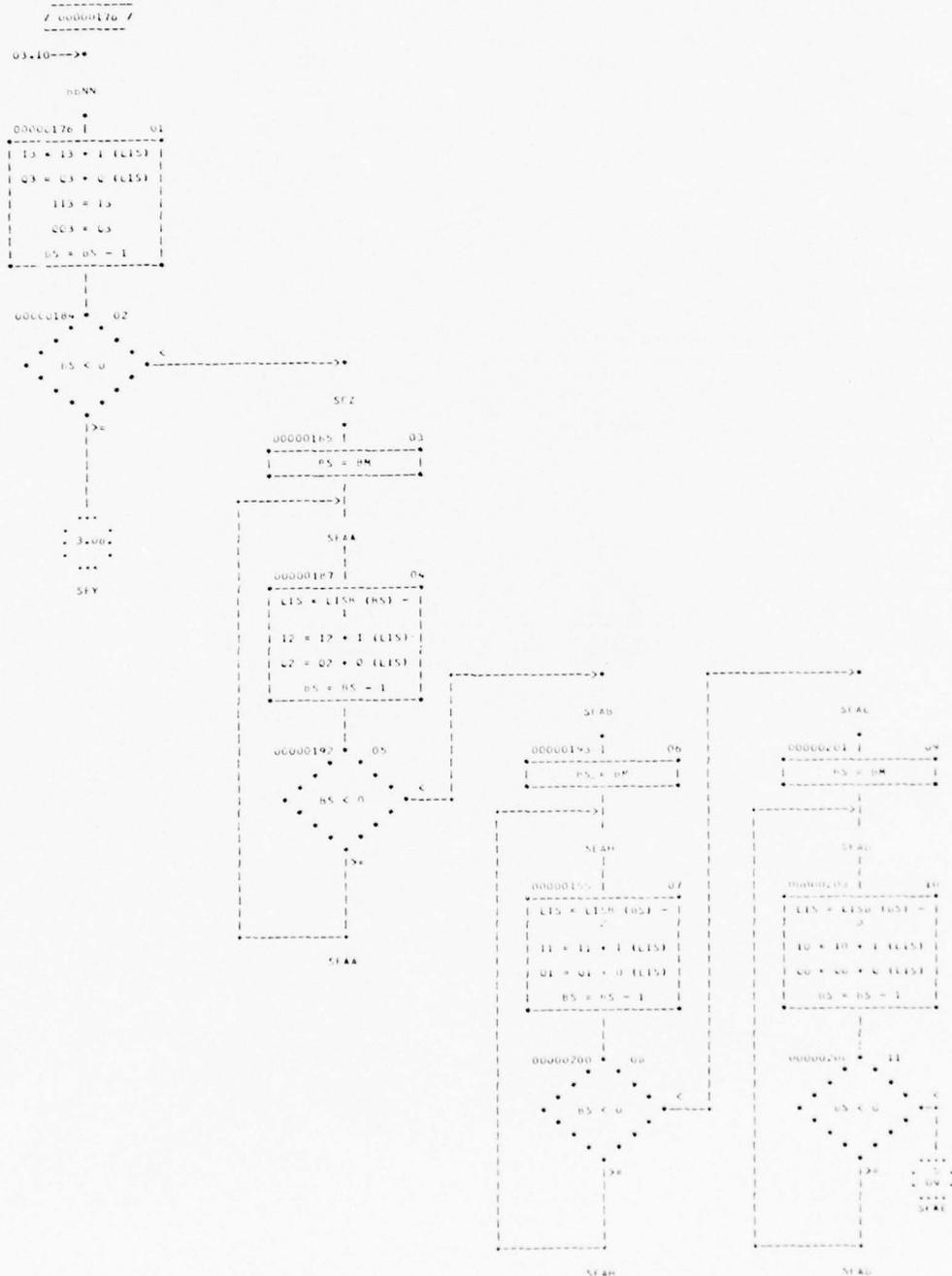


Fig. F-2 SETTLE SUBROUTINE FLOW CHART (continued)

Appendix G

SUBROUTINE TRACK

INTRODUCTION

The Track subroutine described in this appendix was implemented in PL/I digital computer language and successfully tested. See Appendix D for nomenclature.

PURPOSE

The purpose of Track is to produce the best possible estimate of the time of a zero crossing at the end of the third cycle of the Loran-C 100 kHz carrier frequency.

IMPLEMENTATION

To accomplish this task, Track moves a set of two data sample points, which is initially positioned by Settle, forward or backward on the pulse as required until the quadrature data sample point is as close to the zero crossing as possible. The other data sample point samples the amplitude of the positive half of the fourth cycle.

Track must perform the following subtasks to accomplish its function:

1. Removal of the Loran pulse group phase code.
2. Computation of predicted values of in-phase and quadrature data sample voltages.
3. Computation of the errors between actual and predicted values.
4. Comparison of the computed errors to a tolerance and rejecting or accepting the pulses (editing).
5. Summation of the computed errors and the counting of the number of accepted pulses.

6. Computation of the smoothed values of in-phase and quadrature voltages and voltage rates according to the second order filter equations.
7. Adjusting, if necessary, the time position of the next set of data sample points for the next voltage measurement.
8. Setting, if necessary, the AGC level of the R.F. unit; and adjusting, if necessary the expected values of the data sample points for the next measurement cycle.
9. Adjusting, if necessary, the tolerance between predicted and measured voltage samples.

When these tasks have been completed, Track returns control to the Control program.

Subtask 1 consists of multiplying the in-phase and quadrature data sample points by the appropriate Loran pulse group phase code so that the effects of the phase code are removed.

Subtask 2 takes into account the time step between this pulse and the reference pulse in the previous GRI and computes the predicted values for both in-phase and quadrature voltages.

In subtask 3, the errors for each component are computed using the new data just read in.

In subtask 4, the I and Q component errors are each compared to a voltage tolerance. If either component voltage falls outside this tolerance, the pulse is rejected; i.e., subtask 5 is skipped for this pulse and data from the next pulse are processed starting with subtask 1.

When the I and Q component errors fall within the tolerance, the component errors are summed in subtask 5.

After all pulses in a pulse group have been processed, the smoothed values of in-phase and quadrature voltages and voltage rates are computed in subtask 6.

Subtask 7 adjusts, if necessary, the time position of the next set of data sample points for the next voltage measurement.

The low pass filtered value of the in-phase voltage is tested against the AGC "window", and the RF gain is adjusted, if necessary, so that the in-phase data will be within the AGC voltage window. In this step (subtask 8), the RF gain is adjusted in 1 dB steps and the window width is 1.1 dB. The expected values of the data sample points are adjusted accordingly, in synchronism with the RF gain adjustment.

Finally subtask 9 consists of adjusting, if necessary, the tolerance between computed and measured data sample voltages, according to the average number of pulses accepted.

The Track subroutine program listing and logical flow chart are shown in Figs. G-1 and G-2 respectively.

05/01/71

INPUT LISTING

AUTOPLOM CHART SET - 111

PLZT MODULE	(LIST, PARAM)	CONTENTS	****
1	OPTION PRINTDCL, TEST(2,72), NOCOMMENTS		
2	TRACK: PROCEDURE OPTIONS(MAIN):		
3	DECLAR (
4	A,		
5	AA,		
6	B,		
7	C(0:9) FIXED BINARY(31),		
8	DELTA(0:9),		
9	DELTA1,		
10	DT	FLOAT DEC(14),	
11	EIC(0:9),		
12	EIP,		
13	EP(0:9),		
14	EQ	FLOAT DEC(14),	
15	ES,		
16	G(0:9),		
17	GRI,		
18	IMAI	FLOAT,	
19	IMIN	FLOAT DEC(14),	
20	IT(0:9)	FLOAT,	
21	IT	FLOAT,	
22	ITP	FLOAT,	
23	JO,		
24	K	FLOAT,	
25	KI	FLOAT DEC(14),	
26	LA	FLOAT,	
27	LP	FLOAT DEC(14),	
28	LJ	FLOAT,	
29	LW	FLOAT,	
30	LLW	INIT(0),	
31	LP	FLOAT,	
32	N,		
33	P(0:9),		
34	PH(0:31)		
35	PI(0:9)	INIT((10)2.6625),	
36	PQ(0:9),		
37	QR(0:9),		
38	QT,		
39	QTE,		
40	SUMITE,		
41	SUMQTE,		
42	T(0:9)	FLOAT DEC(14),	
43	TAU		
44		EXTERNAL:	
45			
46	TR: /* INITIALIZE INDICES */		
47	LW=0;		
48	LP=0;		
49	LJ=0;		
50			
51	/* CLEAR ERROR SUMMERS */		
52	SUMITE=0;		
53	SUMQTE=0;		
54			
55	TRC: /* IT AND Q ARE INPUT VOLTAGES FROM DRU */		
56			
57	/* DPCODE PHASE CODE */		
58	IT=PH(LJ)*IT;		
59	QT=PH(LJ)*QT;		
60			
61	/* COMPUTE TIME STEP, TAU, FOR EACH PULSE (SECONDS) */		
62	TAU=.001*EP;		
63			
64	/* ERRORS FOR I AND Q (VOLTS) */		
65	ITE=IT-PI(P5)-TAU*IR(P5);		
66	QTE=QT-PQ(P5)-TAU*QR(P5);		
67			
68	/* ERROR EDITOR */		
69	IF ABS(ITE) > DELTA(ES) THEN GO TO TRM;		
70	IF ABS(QTE) > DELTA(QS) THEN GO TO TRM;		
71			
72	/* ACCEPTED PULSE COUNTER */		
73	IN=IN+1;		
74			
75	/* PULSE GROUP ERROR SUMMER (VOLTS) */		
76	SUMITE=SUMITE+ITE;		
77	SUMQTE=SUMQTE+QTE;		
78			
79	TRM: /* PROCESS EIGHT PULSES */		
80	IF LP=7 THEN GO TO TRJ;		
81	LJ=LJ+1;		
82	LP=LP+1;		
83	GO TO TRC;		
84			
85	TRJ: /* DO NOT DIVIDE BY ZERO */		
86	IF IN=0 THEN IN=1;		
87			
88	/* COMPUTE EXPECTED VALUE OF I SIGNAL COMPONENT (VOLTS) */		
89	PI=PI(P5)**GRI*SUMITE/SQRT(IN);		
90			
91	/* COMPUTE EXPECTED VALUE OF Q SIGNAL COMPONENT (VOLTS) */		
92	PQ=PQ(P5)**GRI*SUMQTE/SQRT(IN);		
93			
94	/* COMPUTE EXPECTED VALUE OF RATE OF CHANGE OF I (VOLTS/SEC) */		
95	IR(P5)=IR(P5)+GRI*SUMITE;		
96			
97	/* COMPUTE EXPECTED VALUE OF RATE OF CHANGE OF Q (VOLTS/SEC) */		
98	QR(P5)=QR(P5)+GRI*SUMQTE;		
99			
100	/* COMPUTE PREDICTED I FOR NEXT GRI (VOLTS) */		
101	PI(P5)= PI +IR(P5)*GRI;		
102			
103	/* COMPUTE PREDICTED Q FOR NEXT GRI (VOLTS) */		
104	PQ(P5)= PQ +QR(P5)*GRI;		
105			
106	/* COMPUTE CHANGE IN NUMBER OF CLOCK PULSES TO Q SAMPLE POINT */		
107	W=1+(IN*PQ(P5)/PI(P5));		
108			

Fig. G-1 TRACK SUBROUTINE LISTING

05/03/73

INPUT LISTING

AUTOPLOW CHART SET - TRACK

```

CARD NO      ****                                COMMENTS                                ****
100
101          /* COMPUTE TIME FROM START OF NEXT GRI (MICROSECONDS) */
102          LFF=512E-1;
103          T(PS)=(C(ES)-EQ*K3)*MIN/EI/LFF;
104
105          /* COMPUTE CLOCK PULSES (COUNTS) FROM START OF NEXT GRI */
106          C(PS)=C(PS)-N;
107
108          /* CORRECT PREDICTED Q FOR CHANGE IN SAMPLE POINT */
109          PQ(ES)=-N/K3*(P1(ES)/TRIM)+PQ(PS);
110
111          /* COMPUTE AVERAGE NUMBER OF PULSES ACCEPTED PER GROUP */
112          EP(PS)=(1-IA)*EP(PS)+LA*LN;
113
114          /* AGC LOW PASS FILTER ON EXPECTED VALUE OF I COMPONENT (VOLTS) */
115          EIG(PS)=(1-AA)*EIG(ES)+AA*EI;
116
117          /* AGC WINDOW CHECK */
118          IF EIG(PS)>IMAX THEN GO TO TRM; ELSE GO TO TRQ;
119
120 TRM: /* DECREASE GAIN BY 1 DB */
121       G(ES)=G(ES)-1;
122       K=.8913;
123       GO TO TRP;
124
125 TRQ: /* AGC WINDOW CHECK */
126       IF EIG(PS)<MIN THEN GO TO TRP; ELSE GO TO TRQ;
127
128 TRP: /* INCREASE GAIN BY 1 DB */
129       G(ES)=G(ES)+1;
130       K=1.122;
131
132 /* ADJUST PREDICTED VALUES FOR GAIN CHANGES */
133 P1(ES)=K*P1(ES);
134 PQ(ES)=K*PQ(ES);
135
136 /* COMPUTE NEW ERROR ERROR BOX SIZE (VOLTS) */
137 DELTAT(ES)=DELTAT(ES)*(2-EP(ES)/4);
138
139 /* CHECK FOR MINIMUM BOX SIZE (VOLTS) */
140 IF DELTAT(ES) > DLTMIN THEN GO TO TRR;
141 DELTAT(ES)=DLTMIN;
142 TRR:
143     RPTLN;
144     END TRACK;
145
146
147
148
149
150
151
152

```

Fig. G-1 TRACK SUBROUTINE LISTING (concluded)

CHART TITLE - PROCEDURE TRACK OPTIONS (MAIN)

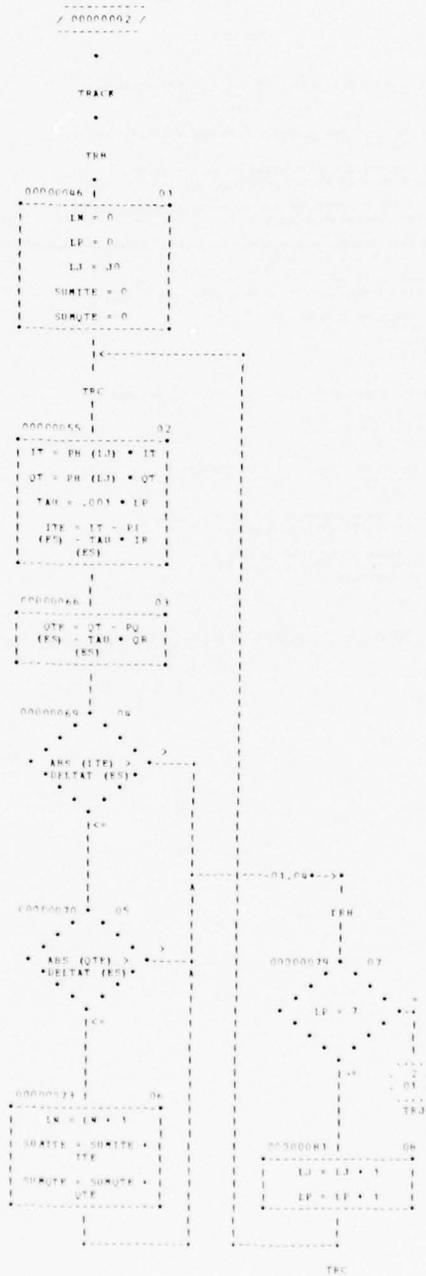


CHART TITLE - PROCEDURE TRACK OPTIONS (MAIN)

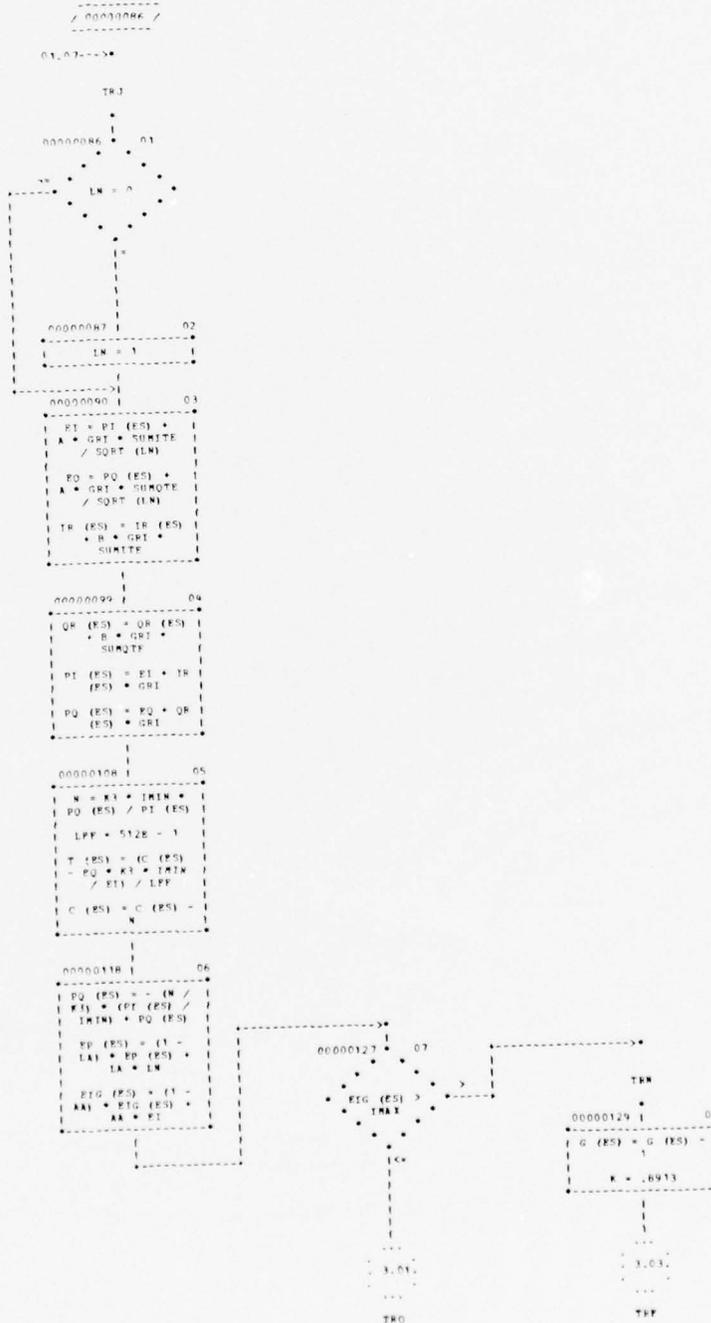


Fig. G-2 TRACK SUBROUTINE FLOW CHART (continued)

CHART TITLE - PROCDURK TRACK OPTIONS (MAIN)

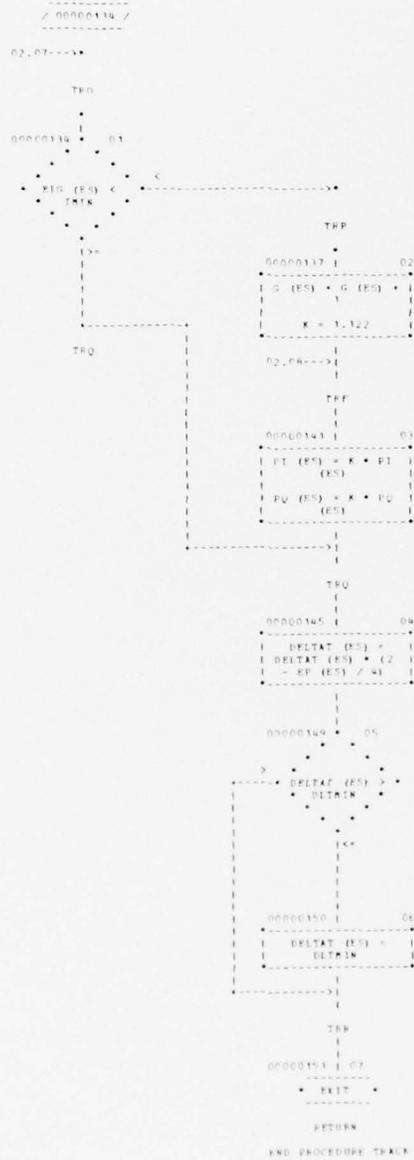


Fig. G-2 TRACK SUBROUTINE FLOW CHART (concluded)

Appendix H

SUBROUTINE STATION IDENTIFICATION (SID)

INTRODUCTION

The Station Identification (SID) subroutine described in this appendix was implemented in PL/I digital computer language and successfully tested. See appendix D for nomenclature.

PURPOSE

The purpose of subroutine SID is to create a table of values, designated ID, that identifies the transmitting stations being tracked by the Track subroutine.

IMPLEMENTATION

In order to accomplish SID, the following three subtasks must be completed successfully:

1. Generation of a table of transmitters organized chronologically in the order of the transmitting station's reception after the reception of the reference transmitter.
2. Computation of the time differences for these transmitters.
3. Identifying the transmitters by comparing the computed position of the Super Receiver/Navigator for each combination of transmitters in track taken three at a time, within a tolerance, to the known location of the receiver.

The identities of the transmitters which satisfy this test are stored in the table called ID.

Subtask 1 begins by searching the phase codes of the transmitters in track for the Loran master transmitter. If the master is present, a chronologically ordered transmitter table is created with the master as the first entry. If a master

is not present, all the secondary's phase codes are searched for a change in phase code between transmitters. If a phase code change is found, a chronologically ordered transmitter table is created with the first secondary that exhibits the phase code change as the first entry. If both a phase code change and the master are not detected, the first transmission received in the local GRI is the first entry in the chronologically ordered transmitter table.

Subtask 2 consists of the computation of two time differences using the first entry in the chronologically ordered transmitter table as the reference transmitter and two other transmitters as the secondaries. These time differences are used in subtask 3 in the computation of the position of the receiver.

Subtask 3 selects combinations of three transmitters at a time, and using the time differences computed in subtask 2, computes the present location of the receiver. The computed location is compared to the known location previously entered or updated into the computer. If the computed position of the receiver does not agree with the known location of the receiver for a given combination of three transmitters another combination is selected and the receiver location is recomputed for another comparison. When the two locations agree within a tolerance, the transmitters have been identified and are entered into the ID table created for this purpose. This process continues until all transmitters in track have been identified. Control is then returned to the Control program.

The SID subroutine listing and logical flow chart are shown in Figs. H-1 and H-2, respectively.

```

PL/1 MODULE      (LIST,PARM)
CARD NO         ****          CONTENTS          ****
1              OPTION PRINTDCI,TEXT=(2,72),NOCOMMENTS
2              SID: PROCEDURE;
3              DECLARE (
4                  AAA      INT(0),
5                  ALPHAAC  INT(0),
6                  BBB      INT(0),
7                  BBTAC    INT(0),
8                  BL(0:7)  INT(100)0,
9                  CCC      INT(0),
10             CD(0:7)  INT(10)1,
11             DDA      INT(0),
12             DDB      INT(0),
13             DDD      INT(0),
14             DEL      INT(0),
15             DELX      INT(20000),
16             FFE      INT(0),
17             FF      INT(0),
18             FFA      INT(0),
19             PFF      INT(0),
20             GAMMA      INT(0),
21             GGG      INT(0),
22             GTI      INT(100)0,
23             H1      INT(0),
24             H2      INT(0),
25             HRR      INT(0),
26             K1,
27             L(0:7)  INT(10)1,
28             OM(0:7) INT(10)0,
29             RA      INT(0),
30             RL      INT(0),
31             S(0:7)  INT(10)0,
32             TDFE      INT(0),
33             SM      INT(0),
34             SO      INT(0),
35             SWITCH      INT(0),
36             T(0:7)  INT(10)0,
37             TD(0:7) INT(10)0,
38             TDFE1     INT(0),
39             TFF(0:7) INT(10)0,
40             Y(0:7)  INT(10)0,
41             Y1      INT(0),
42             XR      INT(0),
43             ZDG      INT(0),
44             Y(0:7)  INT(10)0,
45             Y1      INT(0),
46             ZBTAC    INT(0),
47             ZFO      INT(0),
48             YFO      INT(0)
49             ) FLOAT(6) EXTERNAL;
50
51             DECLARE (
52                 TD(0:7) INT(10)0,
53                 J1 INT(0),
54                 J2 INT(0),
55                 L1 INT(0),
56                 L2 INT(0),
57                 L3 INT(0),
58                 L4 INT(0),
59                 N1      INT(0)
60                 ) EXTERNAL;
61
62
63
64
65
66
67             /* COMPUTE CENTROID OF RADIATING TRANSMITTERS */
68             NEXT:
69             X=0;
70             Y=0;
71             Z=0;
72             IF CD(3) GT THEN GO TO SIDC; ELSE GO TO SIDD;
73             SIDB:
74             X=X+YD*ZDC(J);
75             Y=Y+YD*ZDC(J);
76             Z=Z+YD*ZDC(J);
77             IF J=6 THEN GO TO SIDD;
78             X=X+1;
79             GO TO SIDA;
80             SIDC:
81             Y=Y+1;
82             IF J=6 THEN GO TO SIDD; ELSE GO TO SIDA;
83             SIDD:
84             X=X+ZDC(J);
85             Y=Y+ZDC(J);
86             Z=Z+ZDC(J);
87             X=X+YD*ZDC(J);
88             Y=Y+YD*ZDC(J);
89             Z=Z+YD*ZDC(J);
90             Z=Z+ZDC(J);
91             X=X+ZDC(J);
92             Y=Y+ZDC(J);
93             Z=Z+ZDC(J);
94             X=X+YD*ZDC(J);
95             Y=Y+YD*ZDC(J);
96             Z=Z+YD*ZDC(J);
97             X=X+ZDC(J);
98             Y=Y+ZDC(J);
99             Z=Z+ZDC(J);
100            X=X+YD*ZDC(J);
101            Y=Y+YD*ZDC(J);
102            Z=Z+YD*ZDC(J);
103            Z=Z+ZDC(J);
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107            X=X+YD*ZDC(J);
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114            X=X+YD*ZDC(J);
115            Y=Y+YD*ZDC(J);
116            Z=Z+YD*ZDC(J);
117            Z=Z+ZDC(J);
118            X=X+ZDC(J);
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120            Z=Z+ZDC(J);
121            X=X+YD*ZDC(J);
122            Y=Y+YD*ZDC(J);
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125            X=X+ZDC(J);
126            Y=Y+ZDC(J);
127            Z=Z+ZDC(J);
128            X=X+YD*ZDC(J);
129            Y=Y+YD*ZDC(J);
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131            Z=Z+ZDC(J);
132            X=X+ZDC(J);
133            Y=Y+ZDC(J);
134            Z=Z+ZDC(J);
135            X=X+YD*ZDC(J);
136            Y=Y+YD*ZDC(J);
137            Z=Z+YD*ZDC(J);
138            Z=Z+ZDC(J);
139            X=X+ZDC(J);
140            Y=Y+ZDC(J);
141            Z=Z+ZDC(J);
142            X=X+YD*ZDC(J);
143            Y=Y+YD*ZDC(J);
144            Z=Z+YD*ZDC(J);
145            Z=Z+ZDC(J);
146            X=X+ZDC(J);
147            Y=Y+ZDC(J);
148            Z=Z+ZDC(J);
149            X=X+YD*ZDC(J);
150            Y=Y+YD*ZDC(J);
151            Z=Z+YD*ZDC(J);
152            Z=Z+ZDC(J);
153            X=X+ZDC(J);
154            Y=Y+ZDC(J);
155            Z=Z+ZDC(J);
156            X=X+YD*ZDC(J);
157            Y=Y+YD*ZDC(J);
158            Z=Z+YD*ZDC(J);
159            Z=Z+ZDC(J);
160            X=X+ZDC(J);
161            Y=Y+ZDC(J);
162            Z=Z+ZDC(J);
163            X=X+YD*ZDC(J);
164            Y=Y+YD*ZDC(J);
165            Z=Z+YD*ZDC(J);
166            Z=Z+ZDC(J);
167            X=X+ZDC(J);
168            Y=Y+ZDC(J);
169            Z=Z+ZDC(J);
170            X=X+YD*ZDC(J);
171            Y=Y+YD*ZDC(J);
172            Z=Z+YD*ZDC(J);
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174            X=X+ZDC(J);
175            Y=Y+ZDC(J);
176            Z=Z+ZDC(J);
177            X=X+YD*ZDC(J);
178            Y=Y+YD*ZDC(J);
179            Z=Z+YD*ZDC(J);
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182            Y=Y+ZDC(J);
183            Z=Z+ZDC(J);
184            X=X+YD*ZDC(J);
185            Y=Y+YD*ZDC(J);
186            Z=Z+YD*ZDC(J);
187            Z=Z+ZDC(J);
188            X=X+ZDC(J);
189            Y=Y+ZDC(J);
190            Z=Z+ZDC(J);
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192            Y=Y+YD*ZDC(J);
193            Z=Z+YD*ZDC(J);
194            Z=Z+ZDC(J);
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203            Y=Y+ZDC(J);
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206            Y=Y+YD*ZDC(J);
207            Z=Z+YD*ZDC(J);
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209            X=X+ZDC(J);
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212            X=X+YD*ZDC(J);
213            Y=Y+YD*ZDC(J);
214            Z=Z+YD*ZDC(J);
215            Z=Z+ZDC(J);
216            X=X+ZDC(J);
217            Y=Y+ZDC(J);
218            Z=Z+ZDC(J);
219            X=X+YD*ZDC(J);
220            Y=Y+YD*ZDC(J);
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224            Y=Y+ZDC(J);
225            Z=Z+ZDC(J);
226            X=X+YD*ZDC(J);
227            Y=Y+YD*ZDC(J);
228            Z=Z+YD*ZDC(J);
229            Z=Z+ZDC(J);
230            X=X+ZDC(J);
231            Y=Y+ZDC(J);
232            Z=Z+ZDC(J);
233            X=X+YD*ZDC(J);
234            Y=Y+YD*ZDC(J);
235            Z=Z+YD*ZDC(J);
236            Z=Z+ZDC(J);
237            X=X+ZDC(J);
238            Y=Y+ZDC(J);
239            Z=Z+ZDC(J);
240            X=X+YD*ZDC(J);
241            Y=Y+YD*ZDC(J);
242            Z=Z+YD*ZDC(J);
243            Z=Z+ZDC(J);
244            X=X+ZDC(J);
245            Y=Y+ZDC(J);
246            Z=Z+ZDC(J);
247            X=X+YD*ZDC(J);
248            Y=Y+YD*ZDC(J);
249            Z=Z+YD*ZDC(J);
250            Z=Z+ZDC(J);
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252            Y=Y+ZDC(J);
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256            Z=Z+YD*ZDC(J);
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264            Z=Z+ZDC(J);
265            X=X+ZDC(J);
266            Y=Y+ZDC(J);
267            Z=Z+ZDC(J);
268            X=X+YD*ZDC(J);
269            Y=Y+YD*ZDC(J);
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273            Y=Y+ZDC(J);
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280            Y=Y+ZDC(J);
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284            Z=Z+YD*ZDC(J);
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293            X=X+ZDC(J);
294            Y=Y+ZDC(J);
295            Z=Z+ZDC(J);
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300            X=X+ZDC(J);
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302            Z=Z+ZDC(J);
303            X=X+YD*ZDC(J);
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318            Y=Y+YD*ZDC(J);
319            Z=Z+YD*ZDC(J);
320            Z=Z+ZDC(J);
321            X=X+ZDC(J);
322            Y=Y+ZDC(J);
323            Z=Z+ZDC(J);
324            X=X+YD*ZDC(J);
325            Y=Y+YD*ZDC(J);
326            Z=Z+YD*ZDC(J);
327            Z=Z+ZDC(J);
328            X=X+ZDC(J);
329            Y=Y+ZDC(J);
330            Z=Z+ZDC(J);
331            X=X+YD*ZDC(J);
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334            Z=Z+ZDC(J);
335            X=X+ZDC(J);
336            Y=Y+ZDC(J);
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338            X=X+YD*ZDC(J);
339            Y=Y+YD*ZDC(J);
340            Z=Z+YD*ZDC(J);
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343            Y=Y+ZDC(J);
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376            Z=Z+ZDC(J);
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406            Y=Y+ZDC(J);
407            Z=Z+ZDC(J);
408            X=X+YD*ZDC(J);
409            Y=Y+YD*ZDC(J);
410            Z=Z+YD*ZDC(J);
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433            X=X+ZDC(J);
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444            Y=Y+YD*ZDC(J);
445            Z=Z+YD*ZDC(J);
446            Z=Z+ZDC(J);
447            X=X+ZDC(J);
448            Y=Y+ZDC(J);
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523            Z=Z+ZDC(J);
524            X=X+ZDC(J);
525            Y=Y+ZDC(J);
526            Z=Z+ZDC(J);
527            X=X+YD*ZDC(J);
528            Y=Y+YD*ZDC(J);
529            Z=Z+YD*ZDC(J);
530            Z=Z+ZDC(J);
531            X=X+ZDC(J);
532            Y=Y+ZDC(J);
533            Z=Z+ZDC(J);
534            X=X+YD*ZDC(J);
535            Y=Y+YD*ZDC(J);
536            Z=Z+YD*ZDC(J);
537            Z=Z+ZDC(J);
538            X=X+ZDC(J);
539            Y=Y+ZDC(J);
540            Z=Z+ZDC(J);
541            X=X+YD*ZDC(J);
542            Y=Y+YD*ZDC(J);
543            Z=Z+YD*ZDC(J);
544            Z=Z+ZDC(J);
545            X=X+ZDC(J);
546            Y=Y+ZDC(J);
547            Z=Z+ZDC(J);
548            X=X+YD*ZDC(J);
549            Y=Y+YD*ZDC(J);
550            Z=Z+YD*ZDC(J);
551            Z=Z+ZDC(J);
552            X=X+ZDC(J);
553            Y=Y+ZDC(J);
554            Z=Z+ZDC(J);
555            X=X+YD*ZDC(J);
556            Y=Y+YD*ZDC(J);
557            Z=Z+YD*ZDC(J);
558            Z=Z+ZDC(J);
559            X=X+ZDC(J);
560            Y=Y+ZDC(J);
561            Z=Z+ZDC(J);
562            X=X+YD*ZDC(J);
563            Y=Y+YD*ZDC(J);
564            Z=Z+YD*ZDC(J);
565            Z=Z+ZDC(J);
566            X=X+ZDC(J);
567            Y=Y+ZDC(J);
568            Z=Z+ZDC(J);
569            X=X+YD*ZDC(J);
570            Y=Y+YD*ZDC(J);
571            Z=Z+YD*ZDC(J);
572            Z=Z+ZDC(J);
573            X=X+ZDC(J);
574            Y=Y+ZDC(J);
575            Z=Z+ZDC(J);
576            X=X+YD*ZDC(J);
577            Y=Y+YD*ZDC(J);
578            Z=Z+YD*ZDC(J);
579            Z=Z+ZDC(J);
580            X=X+ZDC(J);
581            Y=Y+ZDC(J);
582            Z=Z+ZDC(J);
583            X=X+YD*ZDC(J);
584            Y=Y+YD*ZDC(J);
585            Z=Z+YD*ZDC(J);
586            Z=Z+ZDC(J);
587            X=X+ZDC(J);
588            Y=Y+ZDC(J);
589            Z=Z+ZDC(J);
590            X=X+YD*ZDC(J);
591            Y=Y+YD*ZDC(J);
592            Z=Z+YD*ZDC(J);
593            Z=Z+ZDC(J);
594            X=X+ZDC(J);
595            Y=Y+ZDC(J);
596            Z=Z+ZDC(J);
597            X=X+YD*ZDC(J);
598            Y=Y+YD*ZDC(J);
599            Z=Z+YD*ZDC(J);
600            Z=Z+ZDC(J);
601            X=X+ZDC(J);
602            Y=Y+ZDC(J);
603            Z=Z+ZDC(J);
604            X=X+YD*ZDC(J);
605            Y=Y+YD*ZDC(J);
606            Z=Z+YD*ZDC(J);
607            Z=Z+ZDC(J);
608            X=X+ZDC(J);
609            Y=Y+ZDC(J);
610            Z=Z+ZDC(J);
611            X=X+YD*ZDC(J);
612            Y=Y+YD*ZDC(J);
613            Z=Z+YD*ZDC(J);
614            Z=Z+ZDC(J);
615            X=X+ZDC(J);
616            Y=Y+ZDC(J);
617            Z=Z+ZDC(J);
618            X=X+YD*ZDC(J);
619            Y=Y+YD*ZDC(J);
620            Z=Z+YD*ZDC(J);
621            Z=Z+ZDC(J);
622            X=X+ZDC(J);
623            Y=Y+ZDC(J);
624            Z=Z+ZDC(J);
625            X=X+YD*ZDC(J);
626            Y=Y+YD*ZDC(J);
627            Z=Z+YD*ZDC(J);
628            Z=Z+ZDC(J);
629            X=X+ZDC(J);
630            Y=Y+ZDC(J);
631            Z=Z+ZDC(J);
632            X=X+YD*ZDC(J);
633            Y=Y+YD*ZDC(J);
634            Z=Z+YD*ZDC(J);
635            Z=Z+ZDC(J);
636            X=X+ZDC(J);
637            Y=Y+ZDC(J);
638            Z=Z+ZDC(J);
639            X=X+YD*ZDC(J);
640            Y=Y+YD*ZDC(J);
641            Z=Z+YD*ZDC(J);
642            Z=Z+ZDC(J);
643            X=X+ZDC(J);
644            Y=Y+ZDC(J);
645            Z=Z+ZDC(J);
646            X=X+YD*ZDC(J);
647            Y=Y+YD*ZDC(J);
648            Z=Z+YD*ZDC(J);
649            Z=Z+ZDC(J);
650            X=X+ZDC(J);
651            Y=Y+ZDC(J);
652            Z=Z+ZDC(J);
653            X=X+YD*ZDC(J);
654            Y=Y+YD*ZDC(J);
655            Z=Z+YD*ZDC(J);
656            Z=Z+ZDC(J);
657            X=X+ZDC(J);
658            Y=Y+ZDC(J);
659            Z=Z+ZDC(J);
660            X=X+YD*ZDC(J);
661            Y=Y+YD*ZDC(J);
662            Z=Z+YD*ZDC(J);
663            Z=Z+ZDC(J);
664            X=X+ZDC(J);
665            Y=Y+ZDC(J);
666            Z=Z+ZDC(J);
667            X=X+YD*ZDC(J);
668            Y=Y+YD*ZDC(J);
669            Z=Z+YD*ZDC(J);
670            Z=Z+ZDC(J);
671            X=X+ZDC(J);
672            Y=Y+ZDC(J);
673            Z=Z+ZDC(J);
674            X=X+YD*ZDC(J);
675            Y=Y+YD*ZDC(J);
676            Z=Z+YD*ZDC(J);
677            Z=Z+ZDC(J);
678            X=X+ZDC(J);
679            Y=Y+ZDC(J);
680            Z=Z+ZDC(J);
681            X=X+YD*ZDC(J);
682            Y=Y+YD*ZDC(J);
683            Z=Z+YD*ZDC(J);
684            Z=Z+ZDC(J);
685            X=X+ZDC(J);
686            Y=Y+ZDC(J);
687            Z=Z+ZDC(J);
688            X=X+YD*ZDC(J);
689            Y=Y+YD*ZDC(J);
690            Z=Z+YD*ZDC(J);
691            Z=Z+ZDC(J);
692            X=X+ZDC(J);
693            Y=Y+ZDC(J);
694            Z=Z+ZDC(J);
695            X=X+YD*ZDC(J);
696            Y=Y+YD*ZDC(J);
697            Z=Z+YD*ZDC(J);
698            Z=Z+ZDC(J);
699            X=X+ZDC(J);
700            Y=Y+ZDC(J);
701            Z=Z+ZDC(J);
702            X=X+YD*ZDC(J);
703            Y=Y+YD*ZDC(J);
704            Z=Z+YD*ZDC(J);
705            Z=Z+ZDC(J);
706            X=X+ZDC(J);
707            Y=Y+ZDC(J);
708            Z=Z+ZDC(J);
709            X=X+YD*ZDC(J);
710            Y=Y+YD*ZDC(J);
711            Z=Z+YD*ZDC(J);
712            Z=Z+ZDC(J);
713            X=X+ZDC(J);
714            Y=Y+ZDC(J);
715            Z=Z+ZDC(J);
716            X=X+YD*ZDC(J);
717            Y=Y+YD*ZDC(J);
718            Z=Z+YD*ZDC(J);
719            Z=Z+ZDC(J);
720            X=X+ZDC(J);
721            Y=Y+ZDC(J);
722            Z=Z+ZDC(J);
723            X=X+YD*ZDC(J);
724            Y=Y+YD*ZDC(J);
725            Z=Z+YD*ZDC(J);
726            Z=Z+ZDC(J);
727            X=X+ZDC(J);
728            Y=Y+ZDC(J);
729            Z=Z+ZDC(J);
730            X=X+YD*ZDC(J);
731            Y=Y+YD*ZDC(J);
732            Z=Z+YD*ZDC(J);
733            Z=Z+ZDC(J);
734            X=X+ZDC(J);
735            Y=Y+ZDC(J);
736            Z=Z+ZDC(J);
737            X=X+YD*ZDC(J);
738            Y=Y+YD*ZDC(J);
739            Z=Z+YD*ZDC(J);
740            Z=Z+ZDC(J);
741            X=X+ZDC(J);
742            Y=Y+ZDC(J);
743            Z=Z+ZDC(J);
744            X=X+YD*ZDC(J);
745            Y=Y+YD*ZDC(J);
746            Z=Z+YD*ZDC(J);
747            Z=Z+ZDC(J);
748            X=X+ZDC(J);
749            Y=Y+ZDC(J);
750            Z=Z+ZDC(J);
751            X=X+YD*ZDC(J);
752            Y=Y+YD*ZDC(J);
753            Z=Z+YD*ZDC(J);
754            Z=Z+ZDC(J);
755            X=X+ZDC(J);
756            Y=Y+ZDC(J);
757            Z=Z+ZDC(J);
758            X=X+YD*ZDC(J);
759            Y=Y+YD*ZDC(J);
760            Z=Z+YD*ZDC(J);
761            Z=Z+ZDC(J);
762            X=X+ZDC(J);
763            Y=Y+ZDC(J);
764            Z=Z+ZDC(J);
765            X=X+YD*ZDC(J);
766            Y=Y+YD*ZDC(J);
767            Z=Z+YD*ZDC(J);
768            Z=Z+ZDC(J);
769            X=X+ZDC(J);
770            Y=Y+ZDC(J);
771            Z=Z+ZDC(J);
772            X=X+YD*ZDC(J);
773            Y=Y+YD*ZDC(J);
774            Z=Z+YD*ZDC(J);
775            Z=Z+ZDC(J);
776            X=X+ZDC(J);
777            Y=Y+ZDC(J);
778            Z=Z+ZDC(J);
779            X=X+YD*ZDC(J);
780            Y=Y+YD*ZDC(J);
781            Z=Z+YD*ZDC(J);
782            Z=Z+ZDC(J);
783            X=X+ZDC(J);
784            Y=Y+ZDC(J);
785            Z=Z+ZDC(J);
786            X=X+YD*ZDC(J);
787            Y=Y+YD*ZDC(J);
788            Z=Z+YD*ZDC(J);
789            Z=Z+ZDC(J);
790            X=X+ZDC(J);
791            Y=Y+ZDC(J);
792            Z=Z+ZDC(J);
793            X=X+YD*ZDC(J);
794            Y=Y+YD*ZDC(J);
795            Z=Z+YD*ZDC(J);
796            Z=Z+ZDC(J);
797            X=X+ZDC(J);
798            Y=Y+ZDC(J);
799            Z=Z+ZDC(J);
800            X=X+YD*ZDC(J);
801            Y=Y+YD*ZDC(J);
802            Z=Z+YD*ZDC(J);
803            Z=Z+ZDC(J);
804            X=X+ZDC(J);
805            Y=Y+ZDC(J);
806            Z=Z+ZDC(J);
807            X=X+YD*ZDC(J);
808            Y=Y+YD*ZDC(J);
809            Z=Z+YD*ZDC(J);
810            Z=Z+ZDC(J);
811            X=X+ZDC(J);
812            Y=Y+ZDC(J);
813            Z=Z+ZDC(J);
814            X=X+YD*ZDC(J);
815            Y=Y+YD*ZDC(J);
816            Z=Z+YD*ZDC(J);
817            Z=Z+ZDC(J);
818            X=X+ZDC(J);
819            Y=Y+ZDC(J);
820            Z=Z+ZDC(J);
821            X=X+YD*ZDC(J);
822            Y=Y+YD*ZDC(J);
823            Z=Z+YD*ZDC(J);
824            Z=Z+ZDC(J);
825            X=X+ZDC(J);
826            Y=Y+ZDC(J);
827            Z=Z+ZDC(J);
828            X=X+YD*ZDC(J);
829            Y=Y+YD*ZDC(J);
830            Z=Z+YD*ZDC(J);
831            Z=Z+ZDC(J);
832            X=X+ZDC(J);
833            Y=Y+ZDC(J);
834            Z=Z+ZDC(J);
835            X=X+YD*ZDC(J);
836            Y=Y+YD*ZDC(J);
837            Z=Z+YD*ZDC(J);
838            Z=Z+ZDC(J);
839            X=X+ZDC(J);
840            Y=Y+ZDC(J);
841            Z=Z+ZDC(J);
842            X=X+YD*ZDC(J);
843            Y=Y+YD*ZDC(J);
844            Z=Z+YD*ZDC(J);
845            Z=Z+ZDC(J);
846            X=X+ZDC(J);
847            Y=Y+ZDC(J);
848            Z=Z+ZDC(J);
849            X=X+YD*ZDC(J);
850            Y=Y+YD*ZDC(J);
851            Z=Z+YD*ZDC(J);
852            Z=Z+ZDC(J);
853            X=X+ZDC(J);
854            Y=Y+ZDC(J);
855            Z=Z+ZDC(J);
856            X=X+YD*ZDC(J);
857            Y=Y+YD*ZDC(J);
858            Z=Z+YD*ZDC(J);
859            Z=Z+ZDC(J);
860            X=X+ZDC(J);
861            Y=Y+ZDC(J);
862            Z=Z+ZDC(J);
863            X=X+YD*ZDC(J);
864            Y=Y+YD*ZDC(J);
865            Z=Z+YD*ZDC(J);
866            Z=Z+ZDC(J);
867            X=X+ZDC(J);
868            Y=Y+ZDC(J);
869            Z=Z+ZDC(J);
870            X=X+YD*ZDC(J);
871            Y=Y+YD*ZDC(J);
872            Z=Z+YD*ZDC(J);
873            Z=Z+ZDC(J);
874            X=X+ZDC(J);
875            Y=Y+ZDC(J);
876            Z=Z+ZDC(J);
877            X=X+YD*ZDC(J);
878            Y=Y+YD*ZDC(J);
879            Z=Z+YD*ZDC(J);
880            Z=Z+ZDC(J);
881            X=X+ZDC(J);
882            Y=Y+ZDC(J);
883            Z=Z+ZDC(J);
884            X=X+YD*ZDC(J);
885            Y=Y+YD*ZDC(J);
886            Z=Z+YD*ZDC(J);
887            Z=Z+ZDC(J);
888            X=X+ZDC(J);
889            Y=Y+ZDC(J);
890            Z=Z+ZDC(J);
891            X=X+YD*ZDC(J);
892            Y=Y+YD*ZDC(J);
893            Z=Z+YD*ZDC(J);
894            Z=Z+ZDC(J);
895            X=X+ZDC(J);
896            Y=Y+ZDC(J);
897            Z=Z+ZDC(J);
898            X=X+YD*ZDC(J);
899            Y=Y+YD*ZDC(J);
900            Z=Z+YD*ZDC(J);
901            Z=Z+ZDC(J);
902            X=X+ZDC(J);
903            Y=Y+ZDC(J);
904            Z=Z+ZDC(J);
905            X=X+YD*ZDC(J);
906            Y=Y+YD*ZDC(J);
907            Z=Z+YD*ZDC(J);
908            Z=Z+ZDC(J);
909            X=X+ZDC(J);
910            Y=Y+ZDC(J);
911            Z=Z+ZDC(J);
912            X=X+YD*ZDC(J);
9
```

```

CARD NO      ****      CONTENTS      ****
100          *ACQDP, FROM START OF LOCAL CRT, OR FROM A CHANGE IN
101          PHASE CODE **
102          I=0;
103          I=0;
104          I=0;
105          I=0;
106          I=0;
107          I=0;
108          I=0;
109          I=0;
110          I=0;
111          I=0;
112          I=0;
113          I=0;
114          I=0;
115          I=0;
116          I=0;
117          I=0;
118          I=0;
119          I=0;
120          I=0;
121          I=0;
122          I=0;
123          I=0;
124          I=0;
125          I=0;
126          I=0;
127          I=0;
128          I=0;
129          I=0;
130          I=0;
131          I=0;
132          I=0;
133          I=0;
134          I=0;
135          I=0;
136          I=0;
137          I=0;
138          I=0;
139          I=0;
140          I=0;
141          I=0;
142          I=0;
143          I=0;
144          I=0;
145          I=0;
146          I=0;
147          I=0;
148          I=0;
149          I=0;
150          I=0;
151          I=0;
152          I=0;
153          I=0;
154          I=0;
155          I=0;
156          I=0;
157          I=0;
158          I=0;
159          I=0;
160          I=0;
161          I=0;
162          I=0;
163          I=0;
164          I=0;
165          I=0;
166          I=0;
167          I=0;
168          I=0;
169          I=0;
170          I=0;
171          I=0;
172          I=0;
173          I=0;
174          I=0;
175          I=0;
176          I=0;
177          I=0;
178          I=0;
179          I=0;
180          I=0;
181          I=0;
182          I=0;
183          I=0;
184          I=0;
185          I=0;
186          I=0;
187          I=0;
188          I=0;
189          I=0;
190          I=0;
191          I=0;
192          I=0;
193          I=0;
194          I=0;
195          I=0;
196          I=0;
197          I=0;
198          I=0;
199          I=0;
200          I=0;
201          I=0;
202          I=0;
203          I=0;
204          I=0;
205          I=0;
206          I=0;
207          I=0;
208          I=0;
209          I=0;
210          I=0;
211          I=0;
212          I=0;
213          I=0;
214          I=0;
215          I=0;
216          I=0;
217          I=0;
218          I=0;
219          I=0;

```

Fig. H-1 SID SUBROUTINE LISTING (continued)

```

CAPD NO      ****      CONTENTS      ****

220          COMPARE COMPUTED RECEIVER LOCATION TO KNOWN LOCATION */
221          AAA=Y (J)-Y (J1);
222          BBB=X (J)-X (J1);
223          CCC=X (J)-Y (J1);
224          DDD=Y (J)-X (J1);
225          DEL=AAA*DDD-BBB*CCC;
226          DDJ=CCC*(CD( 1 )-CD(J1)-BL(0,J1)*CD(J)+BL(0,J1));
227          DDB=YYY*(CD( 2 )-CD(J2)-BL(0,J2)*CD(J)+BL(0,J1));
228          DEE=DDD*DDJ;
229          DFF=CCC*DDB;
230          GA=X(J1)**2-Y(J1)**2-X(J)**2-Y(J)**2;
231          GB=X(J2)**2-Y(J2)**2-X(J)**2-Y(J)**2;
232          ALPHAC=(DDA*DEE-DDD*BA-DDB*FFF+CCC*FB)/(2*DEL);
233          BETA=(G+I-FFF)/DEL;
234          GAMMA=AAA*DDD;
235          HHH=BBB*DDA;
236          GAMMA*(DDJ+GGG+AAA*BB-UDA*HHH+BBB*BA)/(2*DEL);
237          SDEL=(GGG+HHH)/DEL;
238          XT=(Y(J)-ALPHAC)**2+(X(J)-GAMMA)**2;
239          ZPTAC=(ALPHAC*BETAC-Y(J)*BETAC+GAMMA*SDEL-X(J)*SDEL);
240          ETA=ZPTAC**2+SDEL**2-1;
241          SQZPTAC**2+ETA**2;
242          IF SQ<0 THEN DO;
243
244              /* SELECT ANOTHER TRIAD */
245              SWITCH=1;
246              GO TO QUIT;
247          END;
248          THETA=2*ATN(-ZPTAC/SQZPTAC);
249          XR=GAMMA*SDEL*THETA;
250          YR=ALPHAC*BETAC*THETA;
251
252          /* COMPARE KNOWN AND COMPUTED RECEIVER LOCATIONS */
253          IF ABS(XR-XFO)<DELX & ABS(YR-YFO)<DELY THEN DO;
254
255              /* TRIAD FOUND */
256              SWITCH=0;
257              GO TO QUIT;
258          END;
259          IF ETA<0 THEN DO;
260
261              /* SELECT ANOTHER TRIAD */
262              SWITCH=1;
263              GO TO QUIT;
264          END;
265          THETA=2*ATN(-ZPTAC/SQZPTAC);
266          XR=GAMMA*SDEL*THETA;
267          YR=ALPHAC*BETAC*THETA;
268
269          /* COMPARE KNOWN AND COMPUTED RECEIVER LOCATIONS */
270          IF ABS(XR-XFO)<DELX & ABS(YR-YFO)<DELY THEN DO;
271
272              /* TRIAD FOUND */
273              SWITCH=0;
274              GO TO QUIT;
275          END;
276          /* SELECT ANOTHER TRIAD */
277          ELSE SWITCH=1;
278
279          QUIT:  IF SWITCH=1 THEN GO TO IHAM;
280
281
282
283
284
285          IHAQ:  /* CREATE IDENTIFICATION TABLE- TRIAD FOUND */
286          ID(1)=5(11);
287          ID(11)=5(11);
288          ID(2)=5(11);
289          ID(11)=5(11);
290          ID(3)=5(11);
291          ID(11)=5(11);
292          IF ID(1)=5(11) THEN GO TO IHAB;
293          IHAB:  ID(1)=1;
294          ID(11)=1;
295          ID(2)=1;
296          ID(11)=1;
297          GO TO IHAF;
298
299          IHAM:  /* PUT INDICES TO SELECT ANOTHER TRIAD - TRIAD NOT FOUND */
300          IF ID(1)=1 THEN GO TO IHAT;
301          IF ID(11)=1 THEN GO TO IHAY;
302          IF ID(2)=1 THEN GO TO IHAX;
303          IF ID(11)=1 THEN GO TO IHAA;
304
305          IHAT:  ID(11)=4;
306          ID(1)=4;
307          ID(2)=4;
308          ID(11)=4;
309          IF ID(1)=4 THEN GO TO IHAB;
310          IF ID(11)=4 THEN GO TO IHAA;
311          IF ID(2)=4 THEN GO TO IHAX;
312          IF ID(11)=4 THEN GO TO IHAY;
313          GO TO IHAF;
314
315          IHAY:  ID(1)=1;
316          ID(11)=1;
317          ID(2)=1;
318          ID(11)=1;
319          GO TO IHAF;
320
321          IHAX:  ID(1)=1;
322          ID(11)=1;
323          ID(2)=1;
324          ID(11)=1;
325          GO TO IHAF;
326
327          IHAA:  ID(1)=1;
328          ID(11)=1;
329          ID(2)=1;
330          ID(11)=1;
331          GO TO IHAF;
332
333          IHAF:  /* RETURN CONTROL TO CONTROL PROGRAM */
334          P(0)=1;
335          SWITCH=1;
336          END SID;

```

Fig. H-1 SID SUBROUTINE LISTING (concluded)

CHART TITLE - PROCLDRE SID

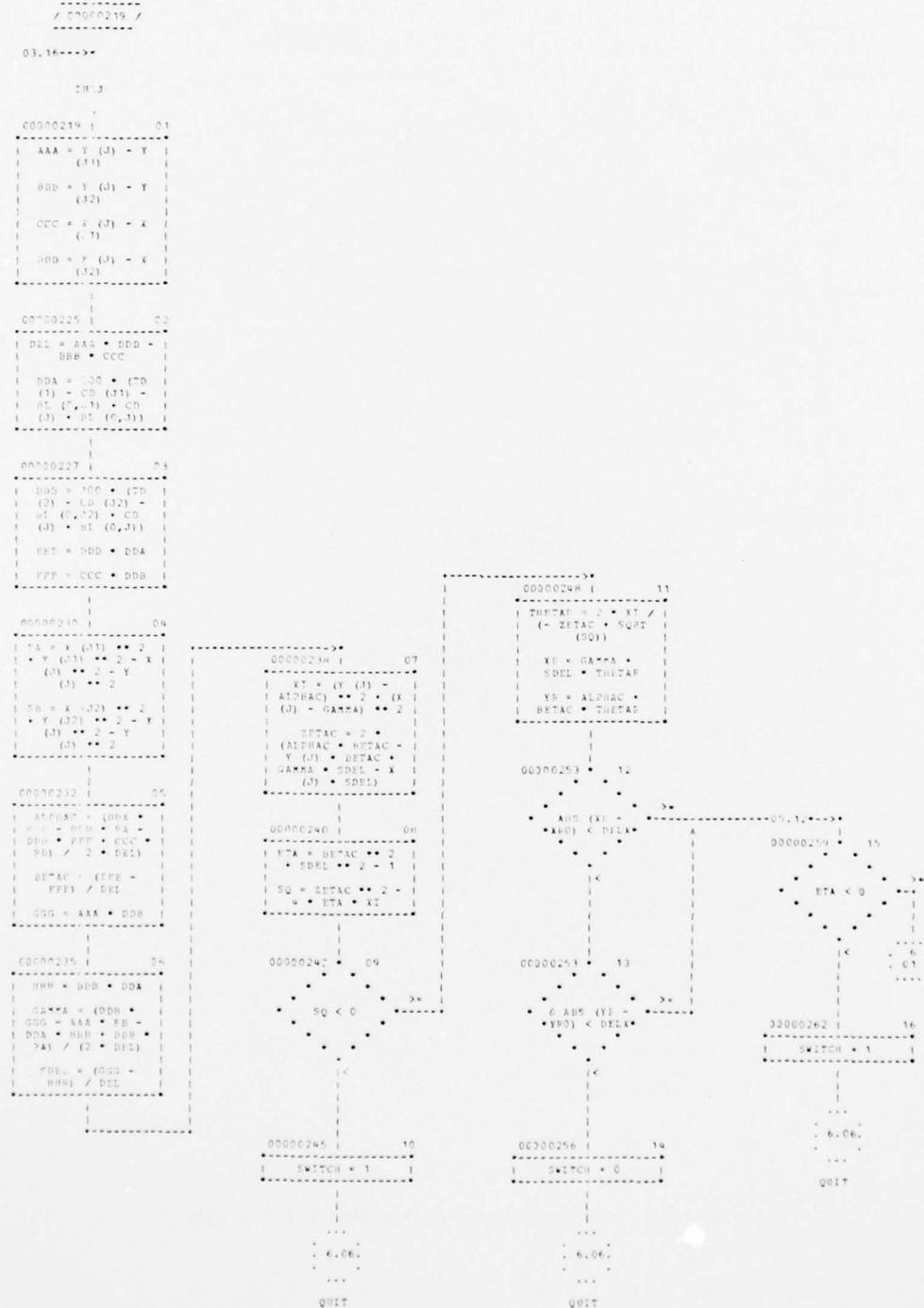


Fig. H-2 SID SUBROUTINE FLOW CHART (continued)

Appendix I

SUBROUTINE NEWTRACK

INTRODUCTION

The Newtrack subroutine described in this appendix was implemented in PL/I digital computer language and successfully tested. See Appendix D for nomenclature.

PURPOSE

The purpose of the Newtrack subroutine is to position the Settle data sample points, at an appropriate time position into the local GRI, of a Loran transmitter in the same chain which is not presently being tracked.

IMPLEMENTATION

To accomplish this function, Newtrack computes the number of clock counts into the local GRI for each transmitter not already in track, re-orders the Track status table, and sets the appropriate parameters so that the Settle data sample points are properly positioned.

Newtrack has the following four subtasks to perform to accomplish its function:

1. Determination of whether a transmitter is scheduled to be transmitting.
2. Computation of time of arrival of a signal at the receiver and number of clock counts into the local GRI.
3. Determination of count and phase code rollover with respect to Loran reference transmitter.
4. Reorganization of the Track status table.

When these tasks have been completed, Newtrack returns control to the Control program.

In subtask 1, the coding delay array is checked for positive values to determine whether a transmitter is transmitting.

If the coding delay is positive, subtask 2 computes the planar coordinates of the transmitter, the time of arrival of the Loran signal from that transmitter to the receiver, and the number of clock counts into the local GRI for that transmitter.

Subtask 3 then tests the clock count number for rollover, modulo the count per GRI. If rollover has occurred, the count for that transmitter is decreased by the count per GRI, and the phase code is increased by 16. The phase code is then tested for rollover and decreased by 32 if rollover has occurred.

Subtask 4 then reorganizes the Track status table when the computed count for this transmitter differs by more than 10240 counts (200 μ s) from all others in the table. In other words, if this occurs before any other in the table, the values for each entry in the table are remembered in time and moved upward until the proper slot is created for the new transmitter. If the new transmitter occurs after the last table entry, the new values are stored directly into the Track status table.

When all transmitters have been processed, control returns to the Control program.

The Newtrack subroutine listing and logical flow chart are shown in Figs. I-1 and I-2, respectively.

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SUMMARY REPORT ON USAF SUPER RECEIVER/NAVIGATOR DEVELOPMENT.(U)
JUN 73 L F FEHLNER, R G ROLL, T W JERARDI N00017-72-C-4401
APL/JHU/TG-1220 NL

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01/31/73      INPUT LISTING      AUTOFLOW CHART SET - NEWTRACK

PLAT MODULE      (ELIST,PAK)

CARD NO      ****      CONTINUES      ****

1      OPTION PAINT,ECCL,EXT=10,70,NO COMMENTS
2      NEWTRACK PROCEDURE:
3      DECLAR E C00191      INIT(1010) FIXED DECIMAL(9,0),
4      PLOC(7,017) INIT(1010),
5      CLOC(7)      INIT(1011),
6      CLAT      INIT(1),
7      CLON      INIT(0),
8      DELTATE(029) INIT(1010),
9      DELTAL      INIT(0),
10     FLOC(29)      INIT(1010),
11     FLOC(9)      INIT(1010),
12     FLOC(4)      INIT(1010),
13     E5      INIT(0),
14     EXLOC(9)      INIT(1010),
15     GLOC(9)      INIT(1010),
16     CMAX      INIT(0),
17     G51      INIT(0.995),
18     H1      INIT(0),
19     H2      INIT(0),
20     H3      INIT(0),
21     H4      INIT(0),
22     H5      INIT(0),
23     H6      INIT(0),
24     H7      INIT(0),
25     H8      INIT(0),
26     H9      INIT(0),
27     H10     INIT(0),
28     H11     INIT(0),
29     IDLOC(1) INIT(1010),
30     IMIN     INIT(0)      FLOAT,
31     IMAX     INIT(1010)  FLOAT,
32     J      INIT(0),
33     JC      INIT(0),
34     JJ      INIT(0),
35     JR      INIT(0),
36     N      INIT(0) DECIMAL(9,0),
37     NLOC(4) INIT(1010)  FLOAT,
38     PLOC(9) INIT(1010),
39     PV      INIT(0),
40     WRLOC(9) INIT(1010),
41     SLAT     INIT(0),
42     SLOW     INIT(0),
43     SW      INIT(0),
44     TLOC(1) INIT(1010),
45     TLOC(7) INIT(1010),
46     TLOC(2) INIT(1010),
47     XLOC(027) INIT(0.10),
48     X8      INIT(0),
49     XYLOC(31) INIT(1010),
50     YLOC(027) INIT(0.10),
51     Y5      INIT(0),
52     ZLOC(027) INIT(0.10),
53     YYLOC(31) INIT(1010),
54     1 EXT:
55
56     IMPLCN=1.2*1000000;
57     J=0;
58
59
60
61
62
63
64
65     NIA:      /* TEST FOR TRANSMITTING LOGAN STATIONS */
66     IF C01J) 24 0 TO SW GO TO NIB;
67     NIB:      /* TEST FOR RECEIVING LOGAN STATIONS */
68     IF J=0 THEN GO TO NID;
69     NID:      /* COMPUTE LOGAN BEARER COORDINATES FOR THIS STATION */
70     J=J+1;
71     GO TO NIA;
72     NIE:      /* COMPUTE LOGAN BEARER COORDINATES FOR THIS STATION */
73     (XLOC)=CLOC(1)*CLON+VLOC(1)*SLW+SLAT +ZLOC(1)*CLAT;
74     J=J+1;
75
76
77
78
79
80     /* COMPUTE TIME OF ARRIVAL FOR THE SIGNAL FROM THIS STATION
81     TO THE RECEIVER */
82     TIME=ZLOC(1)+CLOC(1)*
83     ((XLOC)-X5)**2 + (YLOC)-Y5)**2**0.5/VP;
84
85
86     /* COMPUTE CLOCK COUNTS INTO THE LOCAL ORI */
87     NCC(5)=FLOOR(TIME*FREQ)-TIME*FREQ*51.21;
88     J=J+1;
89
90
91
92
93
94     /* TEST FOR CLOCK COUNT RECEIVED */
95     IF NCC(5) THEN GO TO NIF; ELSE GO TO NIG;
96
97     NIF:      /* SET CLOCK COUNT MODULO COUNT FOR REFERENCE STATION */
98     NCC(5)=NCC(5)-NCC(5)/10;
99     J=J+1;
100
101     /* TEST FOR PHASE CLOCK TAKEOVER */
102     IF J=0 24 THEN GO TO THE FREQ GO TO NIG;
103
104     NIG:      /* SET PHASE CLOCK MODULO COUNT */
105     J=J+1;
106
107
108
109
110

```

Fig. I-1 NEWTRACK SUBROUTINE LISTING

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CARD NO	****	CONTENTS	****
109			
110	NEU1	Z= STAGE RECOGNIZATION OF TRACK STATUS TABLE #Z	
111		ENR0M1	
112		NR01	
113			
114	LCOMP	Z= SORTIN TABLE SORTING #Z	
115		NR01	
116		IF >0 GO THEN GO TO RANGE; ELSE GO TO N111	
117	KA401	CMAR=CEEN+102401	
118		CMIN=CEEN+102401	
119			
120		Z= TEST N AGAINST RANGE TO SEE WHETHER IT IS A NEW STATION #Z	
121		IF >0 MAX THEN GO TO NEWSTAS	
122		IF <0 MIN THEN GO TO DACT	
123		GO TO N111	
124			
125	NEWSTAS	Z= NEW STATION PRESENT - CREATE SLOT #Z	
126		NR01	
127		NR01	
128		NR01	
129			
130		Z= SORTIN TABLE SORTING #Z	
131		IF >0 GO THEN GO TO RANGE; ELSE GO TO N111	
132		CMAR=CEEN+102401	
133		CMIN=CEEN+102401	
134		CMIN=CEEN+102401	
135		CMIN=CEEN+102401	
136		CMIN=CEEN+102401	
137		CMIN=CEEN+102401	
138		CMIN=CEEN+102401	
139		CMIN=CEEN+102401	
140		CMIN=CEEN+102401	
141		CMIN=CEEN+102401	
142		CMIN=CEEN+102401	
143		NR01	
144		NR01	
145			
146		Z= SORTIN DATA FOR NEW STATION #Z	
147		NR01	
148		NR01	
149		NR01	
150		NR01	
151		NR01	
152		NR01	
153		NR01	
154		NR01	
155		NR01	
156		NR01	
157		NR01	
158		NR01	
159		NR01	
160	NR01	NR01	
161		NR01	
162	NR01	NR01	
163		NR01	
164			
165	NR01	Z= SORTIN CONTROL TO OTHER PROGRAM #Z	
166		NR01	
167		NR01	

Fig. I-1 NEWTRACK SUBROUTINE FLOW CHART (concluded)

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START TRACK CALCULATION (CONT.)

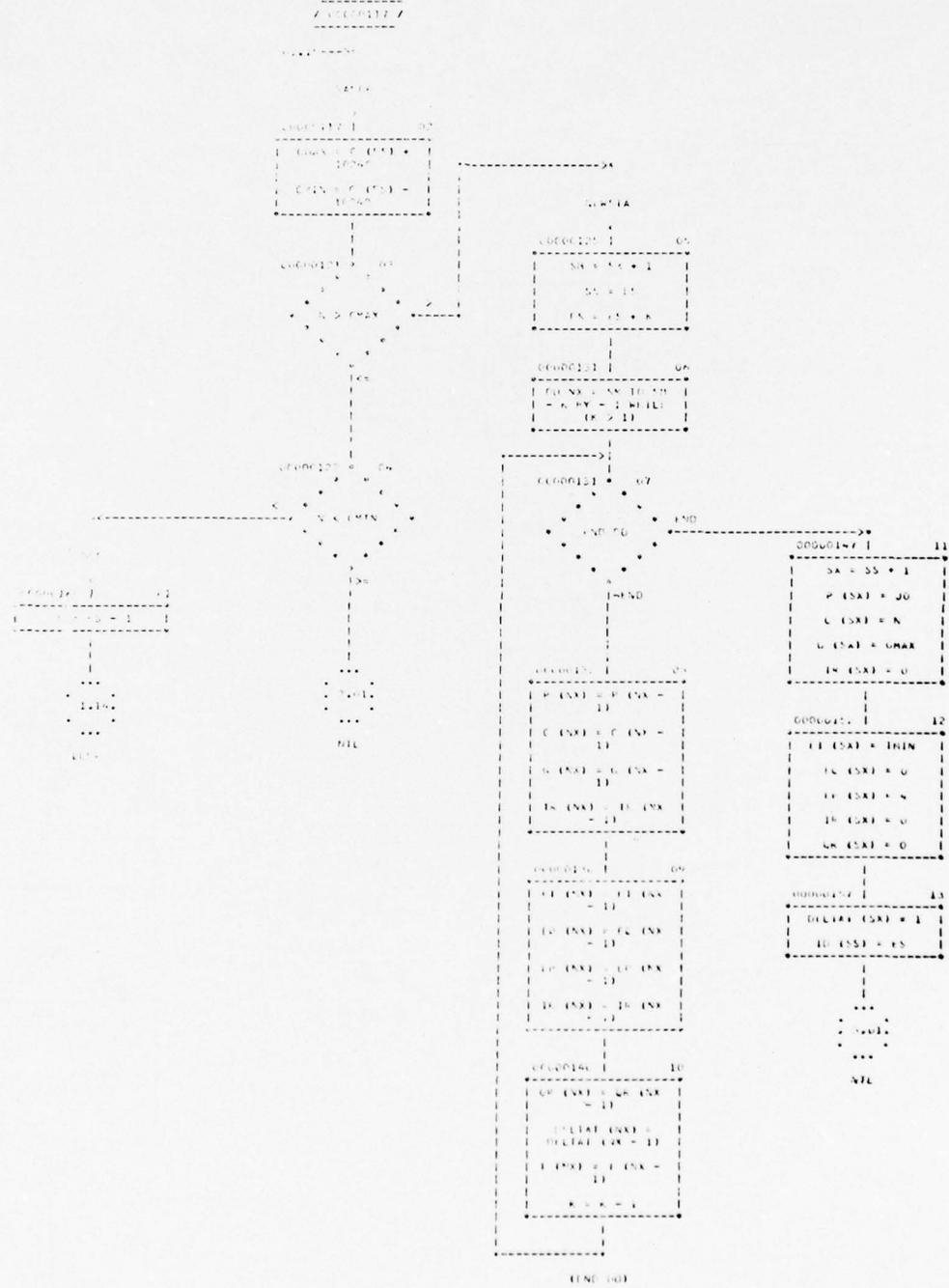


Fig. I-2 NEWTRACK SUBROUTINE FLOW CHART (continued)

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ARTIFLOW CHART 501 - NEWTRACK

PAGE 03

CHART 1-2-1-1 - NEWTRACK SUBROUTINE



Fig. 1-2 NEWTRACK SUBROUTINE FLOW CHART (concluded)

Appendix J

COMPUTER SUBROUTINE NAVIGATE

INTRODUCTION

The Navigate subroutine described in this appendix was implemented in PL/I digital computer language and successfully tested. See Appendix D for nomenclature.

PURPOSE

The purpose of Navigate, as embodied thus far in the Phase 1 design, is to compute fixed course navigational information such as heading error, cross-track error and error rate, along-track distance to go, and along-track distance rate.

IMPLEMENTATION

To accomplish this function, there are 13 subtasks which Navigate executes:

1. Conversion from earth orthogonal coordinates to planar coordinates for each Loran transmitter.
2. Computation of the effective propagation velocity for the Loran signal.
3. Computation of geometry-dependent coordinate conversion parameters.
4. Listing of rate parameters for all transmitters in track.
5. Reorganization of time-of-arrival list so as to be relative to reference.
6. Computation of time and distance differences for all transmitters in track.
7. Conversion from hyperbolic coordinates to Loran Rectangular Coordinates for the present receiver position.

8. Computation of and testing of geometric dilution of precision (GDOP) limit to actuate baseline extension proximity warning.

9. Determination of easting and northing rates and frequency offset correction.

10. Computation of time differences of waypoints.

11. Computation of Loran Rectangular Coordinates of waypoints.

12. Computation of fixed course guidance navigational information.

13. Test for time to switch to next waypoint.

Subtask 1 sets up the triad coordinate system by finding the centroid of the location of all the transmitting stations of the chain and then converting to planar coordinates centered at the centroid.

In subtask 2, the coordinates computed in subtask 1 and the appropriate baseline lengths between transmitters (in microseconds) are used to compute the effective propagation velocity of the Loran signal.

Subtask 3 uses the procedure described in Ref. 5 to compute the geometry dependent coordinate conversion parameters.

Subtask 4 computes the rate parameters for every transmitter being tracked.

Subtask 5 reorganizes the time of arrival of signal list, modulo one GRI time, so as to be relative to the reference transmitter (which need not be the master transmitter).

Subtask 6 computes the time and distance differences for all transmitters in track.

Subtask 7 uses the procedure described in Ref. 5 to convert present receiver position to Loran Rectangular Coordinates. Selection of the proper sign of the square root of SQN to be used is based upon comparison of the three computed receiver-to-transmitter ranges, with three pre-established receiver-to-transmitter ranges. Another set of ranges is then computed for use when the Control program calls for Navigate in a new triad.

In subtask 8, ranges, distances, and Loran Rectangular Coordinates are used to compute the GDOP determinant. The determinant is then tested against a limit to effect a baseline extension proximity warning.

Using previously calculated rate and geometrical parameters, the easting and northing rates and frequency offset computations are performed in subtask 9.

Subtask 10 computes the time differences of the waypoints as a prelude to subtask 11 which is the computation of the Loran Rectangular Coordinates of the waypoints. The number of waypoints which can be used in the Super Receiver/Navigator is limited only by the amount of memory storage available.

Subtask 12 computes the direction of the fixed course and the fixed course guidance navigational information.

Subtask 13 tests the along-track-distance against a limit in order to begin computations on the next fixed course leg.

The Navigate subroutine listing and logical flow chart are shown in Figs. J-1 and J-2, respectively.

02/09/73

INPUT LISTING

AUTOFLOW CHART SET - NAVIGATE

PL/I MODULE

(LIST,PARM)

CARD NO	****	CONTENTS	****
1		OPTION PRINTDC,TEXT=(2,72),NOCOMMENTS	
2		NAVIGATE: PROCEDURE:	
3		DECLARA (
4		ALPHAN INIT (0),	
5		AR INIT (0),	
6		ATD INIT (0),	
7		ATDMLN INIT (0),	
8		ATDML INIT (0),	
9		ATDAN INIT (0),	
10		BC(2:7,0:7) INIT ((64) 0),	
11		BR INIT (0),	
12		CD(0:7) INIT ((4) -1),	
13		CDLX INIT (0),	
14		CDLX INIT (0),	
15		CDLX INIT (0),	
16		CDLX INIT (0),	
17		CDLX INIT (0),	
18		CDLX INIT (0),	
19		CDLX INIT (0),	
20		CDLX INIT (0),	
21		CDLX INIT (0),	
22		CDLX INIT (0),	
23		CDLX INIT (0),	
24		CDLX INIT (0),	
25		CDLX INIT (0),	
26		CDLX INIT (0),	
27		CDLX INIT (0),	
28		CDLX INIT (10000),	
29		CDLX INIT (0),	
30		CDLX INIT (0),	
31		CDLX INIT (0),	
32		CDLX INIT (0),	
33		CDLX INIT (0),	
34		CDLX INIT (0),	
35		CDLX INIT (0),	
36		CDLX INIT (0),	
37		CDLX INIT (0),	
38		CDLX INIT (0),	
39		CDLX INIT (0),	
40		CDLX INIT (0),	
41		CDLX INIT (0),	
42		CDLX INIT (0),	
43		CDLX INIT (0),	
44		CDLX INIT (0),	
45		CDLX INIT (0),	
46		CDLX INIT (0),	
47		CDLX INIT (0),	
48		CDLX INIT (0),	
49		CDLX INIT (0),	
50		CDLX INIT (0),	
51		CDLX INIT (0) C1, FLOAT,	
52		CDLX INIT (0),	
53		CDLX INIT (0),	
54		CDLX INIT (0),	
55		CDLX INIT (0),	
56		CDLX INIT (0),	
57		CDLX INIT (0),	
58		CDLX INIT (0),	
59		CDLX INIT (0),	
60		CDLX INIT (0),	
61		CDLX INIT (0),	
62		CDLX INIT (0),	
63		CDLX INIT (0),	
64		CDLX INIT (0),	
65		CDLX INIT (0),	
66		CDLX INIT (0),	
67		CDLX INIT (0),	
68		CDLX INIT (0),	
69		CDLX INIT (0),	
70		CDLX INIT (0),	
71		CDLX INIT (0),	
72		CDLX INIT (0),	
73		CDLX INIT (0),	
74		CDLX INIT (0),	
75		CDLX INIT (0),	
76		CDLX INIT (0),	
77		CDLX INIT (0),	
78		CDLX INIT (0),	
79		CDLX INIT (0),	
80		CDLX INIT (0),	
81		CDLX INIT (0),	
82		CDLX INIT (0),	
83		CDLX INIT (0),	
84		CDLX INIT (0),	
85		CDLX INIT (0),	
86		CDLX INIT (0),	
87		CDLX INIT (0),	
88		CDLX INIT (0),	
89		CDLX INIT (0),	
90		CDLX INIT (0),	
91		CDLX INIT (0),	
92		CDLX INIT (0),	
93		CDLX INIT (0),	
94		CDLX INIT (0),	
95		CDLX INIT (0),	
96		CDLX INIT (0),	
97		CDLX INIT (0),	
98		CDLX INIT (0),	
99		CDLX INIT (0),	
100		CDLX INIT (0),	
101		CDLX INIT (0),	
102		CDLX INIT (0),	
103		CDLX INIT (0),	
104		CDLX INIT (0),	
105		CDLX INIT (0),	
106		CDLX INIT (0),	
107		CDLX INIT (0),	
108		CDLX INIT (0),	

) EXTERNAL;

Fig. J-1 NAVIGATE SUBROUTINE LISTING

02/09/73

INPUT LISTING

AUTOFLOW CHART SET - NAVIGATE

```

CAR# NO      ****                                CONTENTS                                ****
109
110
111          /* SET UP TRIAD COORDINATE SYSTEM */
112          I4,P6=C;
113          X10=(X10C(JR)*X10C(JA)+X10C(JB))/3;
114          Y10=(Y10C(JR)*Y10C(JA)+Y10C(JB))/3;
115          Z10=(Z10C(JR)*Z10C(JA)+Z10C(JB))/3;
116          S10NO=Y10/SQRT(X10**2+Y10**2);
117          C10NO=X10/SQRT(X10**2+Y10**2);
118          S1LATO=-Z10/SQRT(X10**2+Y10**2+Z10**2);
119          C1LATO=SQRT(X10**2+Y10**2)/SQRT(X10**2+Y10**2+Z10**2);
120
121
122
123
124
125
126          /* COMPUTE PLANAR COORDINATES OF ALL RADIATING STATIONS.
127          IN ONE CHAIN */
128          J=C;
129          IF C0(J)<0 THEN GO TO NAB;
130          NAD:  EP(J)=XEOC(J)*S10NO+YEOC(J)*C10NO;
131          NP(J)=(XEOC(J)*C10NO+YEOC(J)*S10NO+S1LATO+ZEOC(J)*C1LATO;
132          NAB:  IF J<6 THEN GO TO NAC; ELSE GO TO NAE;
133          NAC:  J=J+1;
134          GO TO NAA;
135
136
137
138
139          NAE:  /* COMPUTE EFFECTIVE PROPAGATION VELOCITY */
140          PV=(SQRT((EP(JA)-EP(JB))**2+(NP(JA)-NP(JB))**2)
141          *SQRT((EP(JB)-EP(JA))**2+(NP(JB)-NP(JA))**2)
142          *SQRT((EP(JR)-EP(JB))**2+(NP(JR)-NP(JB))**2))
143          /
144          (BL(JR,JA)+BL(JR,JB)+BL(JA,JB));
145
146
147
148
149
150          /* COMPUTE GEOMETRY DEPENDENT COORDINATE CONVERSION
151          PARAMETERS */
152          AN=NP(JR)-NP(JA);
153          BN=NP(JR)-NP(JB);
154          CN=(EP(JR)-EP(JA));
155          DN=(EP(JR)-EP(JB));
156          DELN=AN*DN-BN*CN;
157
158
159
160
161          NAF:  /* LIST RATE PARAMETERS RE ALL STATIONS IN TRACK */
162          IF TR(TD(J))=3 THEN GO TO NAI;
163          ECTD(J);
164          TIN(J)=T(ES);
165          QR(J)=(QR(ES)*K3*IMIN)/(EI(ES)+51.2);
166          KR(J)=QR(ES)/(EI(ES)+200000*3.1415926*GRI);
167          NAG:  IF J>0 THEN GO TO NAG; ELSE GO TO NAJ;
168          J=J-1;
169          GO TO NAF;
170
171
172
173
174
175
176          NAJ:  /* REORGANIZE TIME-OF-ARRIVAL LIST SO AS TO BE RELATIVE
177          TO REFERENCE */
178          LOOP: DO J=C TO 6;
179          IF ID(J)=0 THEN GO TO END;
180          IF TIN(J)<TIN(JR) THEN GO TO NAF; ELSE GO TO NAJ;
181          NAF:  TIN(J)=TIN(J)+GRI;
182
183
184
185
186
187          NAQ:  /* COMPUTE TIME DIFFERENCE AND DISTANCE DIFFERENCE RE ALL
188          STATIONS IN TRACK */
189          TD(J)=FOC*(TIN(J)*(1-QR(J))-TIN(JR)*(1-QR(JR))
190          *(GRI+DT)*(QR(J)-QR(JR)));
191          DDR(J)=DV*(TD(J)-BL(0,J)+BL(0,JR)-CD(J)*CD(JR));
192          END:  END LOOP;
193
194
195
196
197
198          NAR:  /* START COORDINATE CONVERSION, HYPERBOLIC TO PLANAR, FOR
199          RECEIVER PRESENT POSITION */
200          EN=AN*DDN(JA);
201          FN=CN*DDN(JB);
202          FAN=EI(JA)**2+NF(JA)**2-EP(JB)**2-J(JR)**2;
203          FBN=EI(JB)**2+NF(JB)**2-EP(JR)**2-NF(JR)**2;
204          ALPHAN=(DDN(JA)*EN-FAN*DN-DDN(JB)*FAN*BN*CN)/(2*DELN);
205          BETAN=(FN-FN)/DELN;
206          GN=AN*DDN(JB);
207          HS=DN*DDN(JA);
208          GAMMAN=(DDN(JB)*GN-FBN*AN-DDN(JA)*HN*FAN*BN)/(2*DELN);
209          CDELN=(GN-HN)/DELN;
210          KIN=(NF(JR)-ALPHAN)**2*(EP(JR)-GAMMAN)**2;
211          ZETAN=2*(ALPHAN*BETAN-NF(JR)*BETAN+GAMMAN*SDELN-EP(JR)*
212          SDELN);
213          ETAN=BETAN**2+SDELN**2-1;
214          SQB=ZETAN**2-4*ETAN*KIN;
215
216
217
218
219

```

Fig. J-1 NAVIGATE SUBROUTINE LISTING (continued)

02/09/73

INPUT LISTING

AUTOFLOW CHART SET - NAVIGATE

```

CARD NO      ****      CONTENTS      ****
220          /* SWIP EXCEPT FOR FIRST TIME AFTER EACH WAYPOINT CHANGE */
221          IF P4=0 THEN GO TO NAS; ELSE GO TO NAT;
222          NAS:      P4=1;
223
224          /* TEST FOR IMAGINARY VALUES OF SQUARE ROOT */
225          IF SQNKC THEN GO TO NALARM;
226
227          NAU:      /* DETERMINE SIGN OF SQUARE ROOT */
228                  THETA=2*PI/(-ZETAN*SQRT(SQNK));
229                  IF ABS(THETA-RTE(JR))>DELR THEN GO TO NAV;
230                  THETA=THETA+DDN(JA);
231                  IF ABS(THETA-RTE(JA))>DELR THEN GO TO NAV;
232                  THETA=THETA+DDN(JB);
233                  IF ABS(THETA-RTE(JB))>DELR THEN GO TO NAV;
234                  KA=1;
235                  GO TO NAZ;
236          NAV:      KA=-1;
237
238
239
240
241
242          NAT:      /* COMPUTE DISTANCE TO REFERENCE WITH CORRECT SIGN OF SQUARE
243                  ROOT */
244                  THETA=(2*PI)/(-ZETAN*KA*SQRT(SQNK));
245
246
247
248
249          NAW:      /* COMPUTE PLANE COORDINATE OF RECEIVER */
250                  X=ALPHAN*ZETAN*THETA;
251                  Y=ALPHAN*ZETAN*THETA;
252
253
254
255
256
257
258          /* PREDICT RANGES TO ALL STATIONS IN TRACK */
259          JB=0;
260          IF TR(ID(J))=3 THEN GO TO NAADD;
261          NAAC:      THETA=THETA+DDN(J)+IV*GR(J)*GRI;
262          NAADD:      IF J=6 THEN GO TO NAAD;
263          NAAD:      J=J+1;
264                  GO TO NAAA;
265
266
267
268
269
270
271          NAAD:      /* COMPUTE AZIMUTH OF RECEIVER */
272                  SPSIA=(X(J)-X)/THETA;
273                  CPSII=(Y(J)-Y)/THETA;
274                  TMP1=THETA+DDN(JA);
275                  TMP2=THETA+DDN(JB);
276                  SPSIA=(X(J)-X)/TMP1;
277                  CPSII=(Y(J)-Y)/TMP1;
278                  SPSIB=(X(J)-X)/TMP2;
279                  CPSIB=(Y(J)-Y)/TMP2;
280
281
282
283
284          /* COMPUTE GDOP DETERMINANT */
285          DTRMT=(CPSIA-CPSIB)*(SPSIB-SPSIR)
286                -(CPSIB-CPSIR)*(SPSIA-SPSIR);
287
288
289
290
291
292          /* TEST FOR GDOP LIMIT */
293          /* P5=1: BASELINE EXTENSION PROXIMITY WARNING */
294          /* P5=0: NO BASELINE PROBLEM */
295          IF ABS(DTRMT)<GDOLIM THEN P5=1; ELSE P5=0;
296
297
298
299
300
301          NAAG:      /* DETERMINE EASTING AND NORTHING RATES AND FREQUENCY OFFSET
302                  CORRECTION */
303                  ERR=(KK(JA)-KK(JR))*(SPSIB-SPSIR)
304                    -(KK(JB)-KK(JR))*(SPSIA-SPSIR)
305                    /
306                    DTRMT;
307                  NRR=(KK(JA)-KK(JR)-ERR*(CPSIA-CPSIB))/(SPSIA-SPSIR);
308                  FOC=1-KK(JR)+ERR*(CPSIR+KRS)+SPSIR;
309
310
311
312
313
314          /* DO ONLY ONCE AFTER EACH WAYPOINT CHANGE */
315          IF P6=0 THEN GO TO NAAR; ELSE GO TO NAAL;
316          P6=1;
317          LN=0;
318
319
320
321
322
323          NAAR:      /* ASSIGN MASTER-MASTER TIME DIFFERENCES */
324                  IF JB=0 THEN GO TO NAAR; ELSE GO TO NAAL;
325          NAAL:      TD=(NF,JB)*0;
326                  TD=(NF+1,JB)*0;
327
328
329
330
331

```

Fig. J-1 NAVIGATE SUBROUTINE LISTING (continued)

02/09/73

INPUT LISTING

AUTOFLOW CHART SET - NAVIGATE

```

CARD NO      ****      CONTENTS      ****
331
332          NAAL:      /* COMPUTE TIME DIFFERENCES OF WAYPOINTS */
333              TDA=TD*(WP,JA)-TD*(WP,JB);
334              TDB=TD*(WP,JB)-TD*(WP,JB);
335
336
337
338
339
340          /* COMPUTE PLANAR COORDINATES OF WAY POINTS */
341          DDAN=PV*(TDA-DL(C,JA)*DL(C,JB)-CD(JA)*CD(JB));
342          DDBN=PV*(TDB-DL(C,JB)*DL(C,JP)-CD(JB)*CD(JP));
343          EN=DL*DDAN;
344          FN=DL*DDBN;
345          GAN=LI(JA)**2*NP(JA)**2-EP(JB)**2-NP(JB)**2;
346          GBN=EP(JB)**2*NP(JB)**2-EP(JB)**2-NP(JB)**2;
347          ALPHAN=(DDAN*EN-FAN*DN-DDBN*FN-FBN*CN)/(2*DELN);
348          BETA=(FN-FN)/DELN;
349          GN=AN*DDN;
350          HN=BN*DDN;
351          GAMMAN=(DDN*GN-GN*AN-DDAN*HN-FAN*DN)/(2*DELN);
352          SDELN=(GN-HN)/DELN;
353          XIN=(NP(JB)-ALPHAN)**2+(EP(JB)-GAMMAN)**2;
354          ZETAN=2*(ALPHAN*BETA-NP(JB)*BETA+GAMMAN*SDELN-EP(JB)*SDELN);
355
356          BTAN=BETA**2+SDELN**2-1;
357          CBN=ZETAN**2-4*BTAN*XIN;
358          THETA=(2*XIN)/(-ZETAN+CBN*SQRT(SQB));
359          XW(WP)=GAMMAN+SDELN*THETA;
360          YW(WP)=ALPHAN+BETA*THETA;
361          IF WP=1 THEN GO TO NAAM;
362
363          NAAM:      LN=LN+1;
364                   WP=WP+1;
365                   GO TO NAAL;
366
367
368
369
370          NAAM:      /* DETERMINE DIRECTION OF FIXED COURSE */
371                   WP=WP+1;
372                   DELX=(XW(WP+1)-XW(WP));
373                   DELY=(YW(WP+1)-YW(WP));
374                   TRP1=SQRT(DELX**2+DELY**2);
375                   CTC=DELX/TRP1;
376                   CTC=DELY/TRP1;
377
378
379
380
381          NAAL:      /* COMPUTE FIXED COURSE GUIDANCE */
382                   DELX=XW(WP+1)-XW(WP);
383                   DELY=YW(WP+1)-YW(WP);
384                   CTC=DELX/TRP1;
385                   ATD=DELX*CTC+DELY*CTC;
386                   XTR=DELY*CTC;
387                   YTR=XW(WP+1)-XW(WP);
388                   YTR=XW(WP+1)-XW(WP);
389                   YTR=XW(WP+1)-XW(WP);
390                   ATDR=-XTR*CTC+YTR*CTC;
391                   HE=ATAN(CTE,ATD);
392
393
394
395
396
397          /* INCREMENT WAYPOINT NUMBER */
398          IF ATD*ATDR THEN GO TO NAAL;
399
400          NAAL:      WP=WP+1;
401                   PG=0;
402                   RETURN;
403          NAAL:      STOP;
404          NAAL:      END NAVIGATE;

```

Fig. J-1 NAVIGATE SUBROUTINE LISTING, (concluded)

CHART TITLE - PROCEDURE NAVIGATE

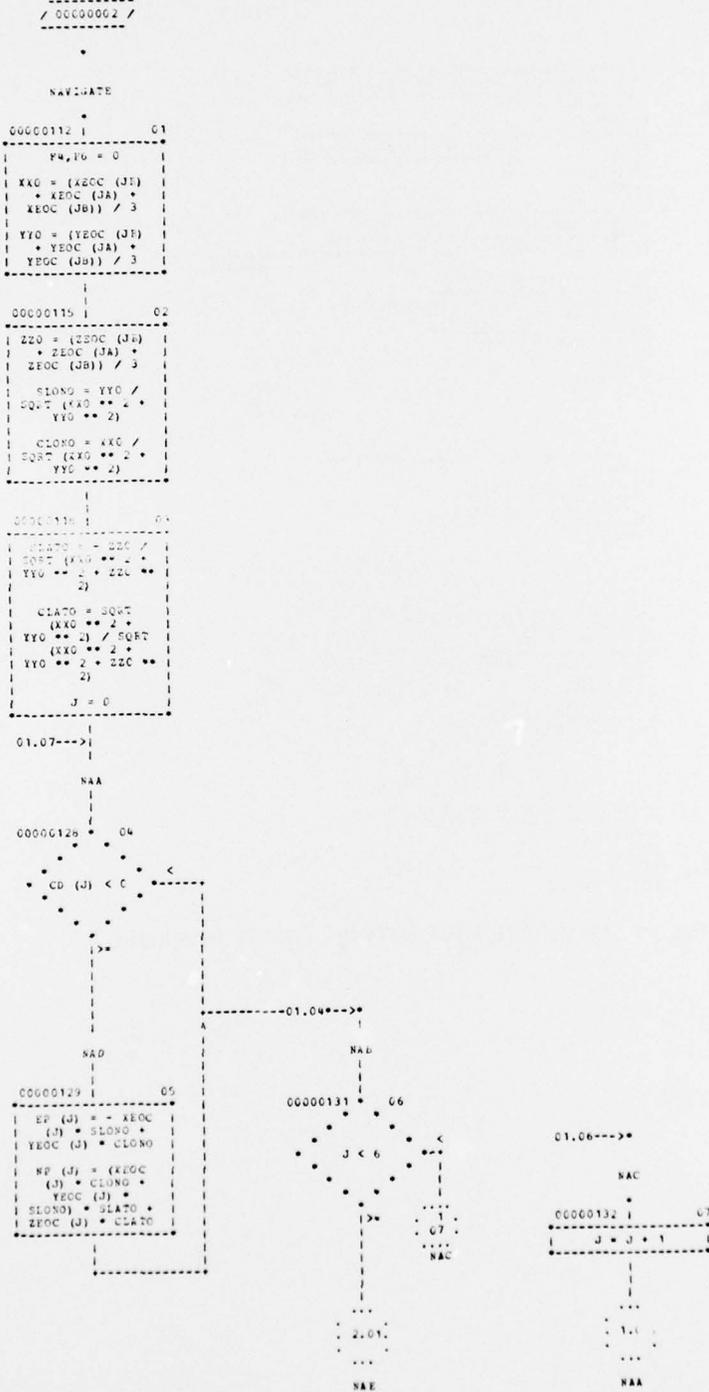


Fig. J-2 NAVIGATE SUBROUTINE FLOW CHART

CHART TITLE - PROCEDURE NAVIGATE

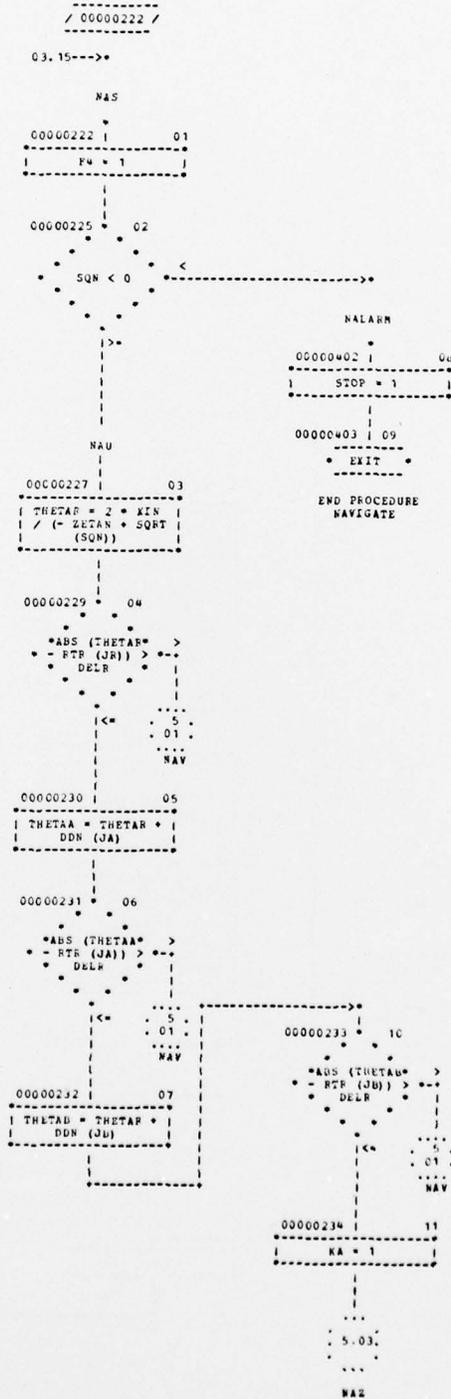


Fig. J-2 NAVIGATE SUBROUTINE FLOW CHART (continued)

CHART TITLE - PROCEDURE NAVIGATE

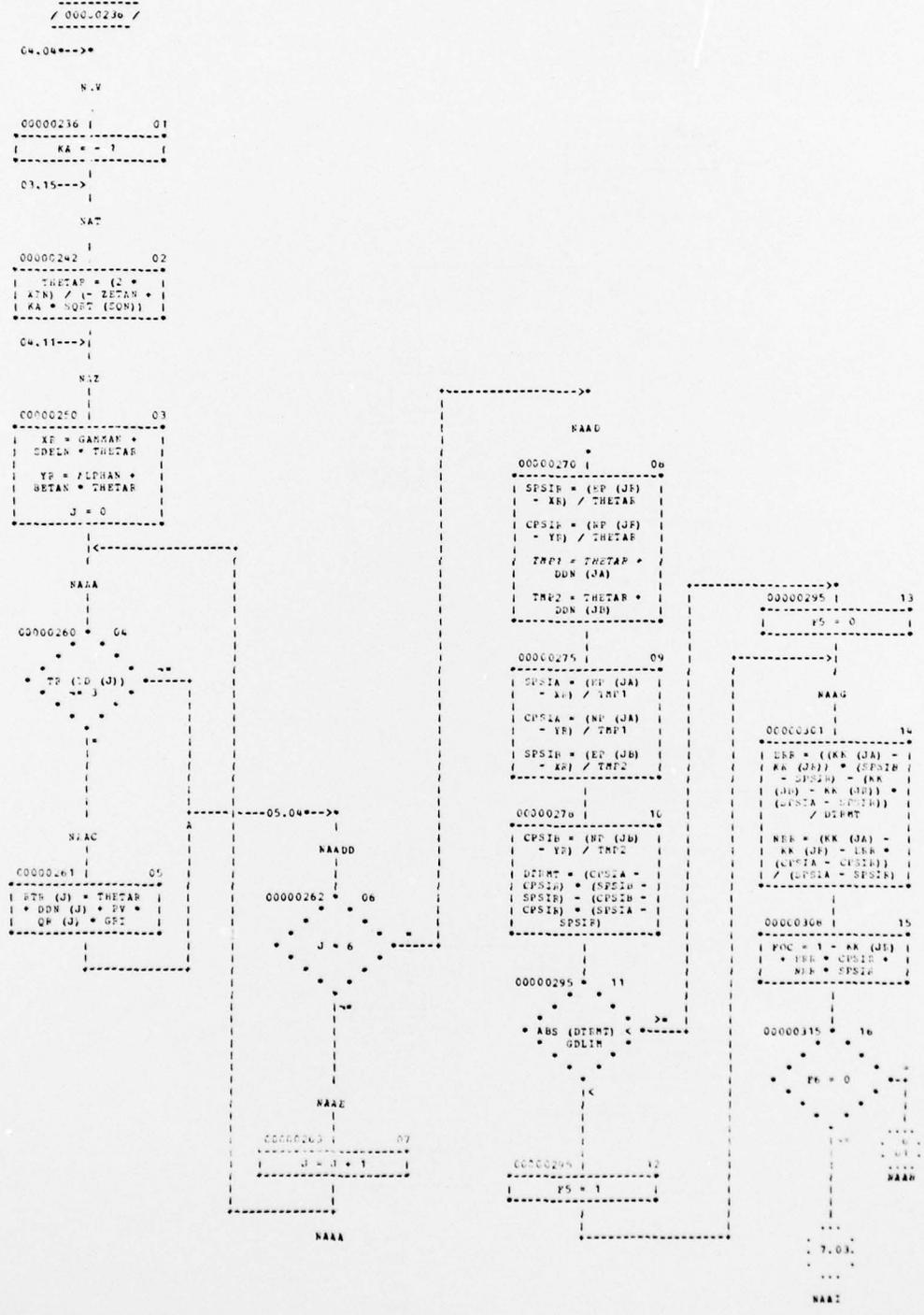


Fig. J-2 NAVIGATE SUBROUTINE FLOW CHART (continued)

CHART TITLE - PROCEDURE NAVIGATE

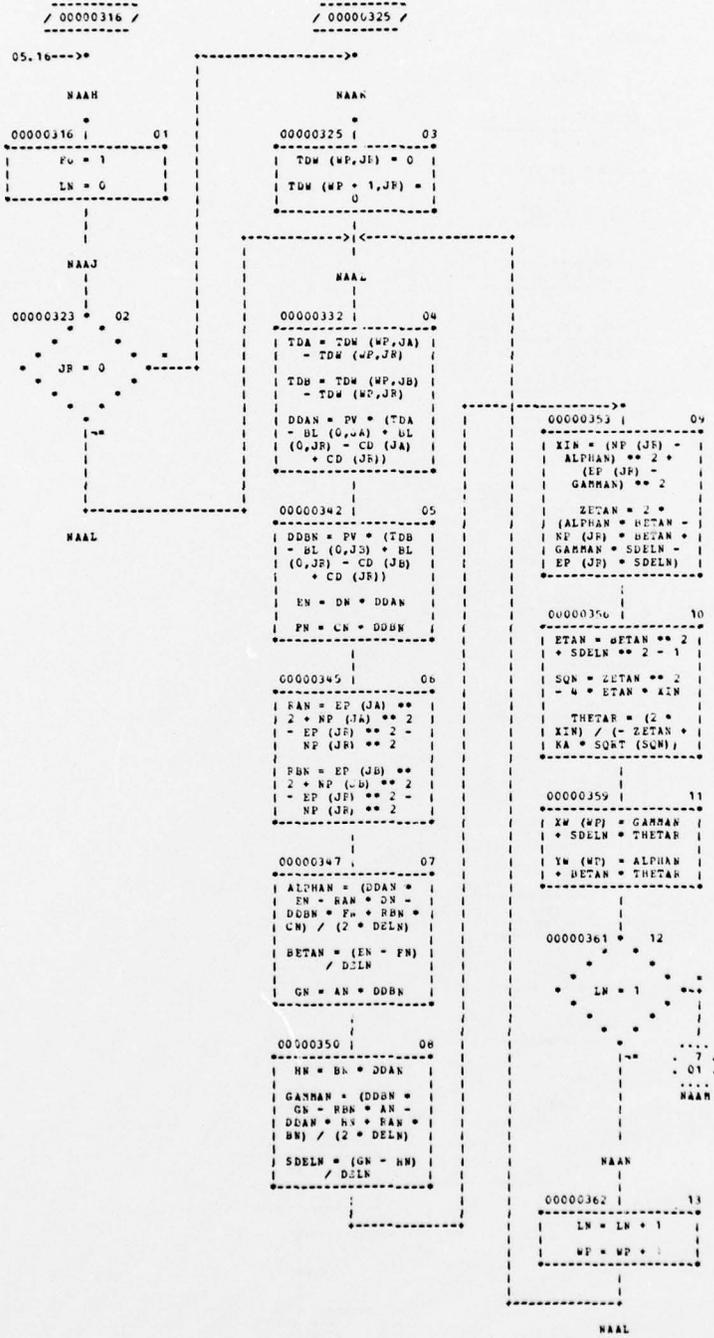


Fig. J-2 NAVIGATE SUBROUTINE FLOW CHART (continued)

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