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OCT 76 R G ABRAHAM, T CSAKVARY, D H DAVIES DAAB07-76-C-0027

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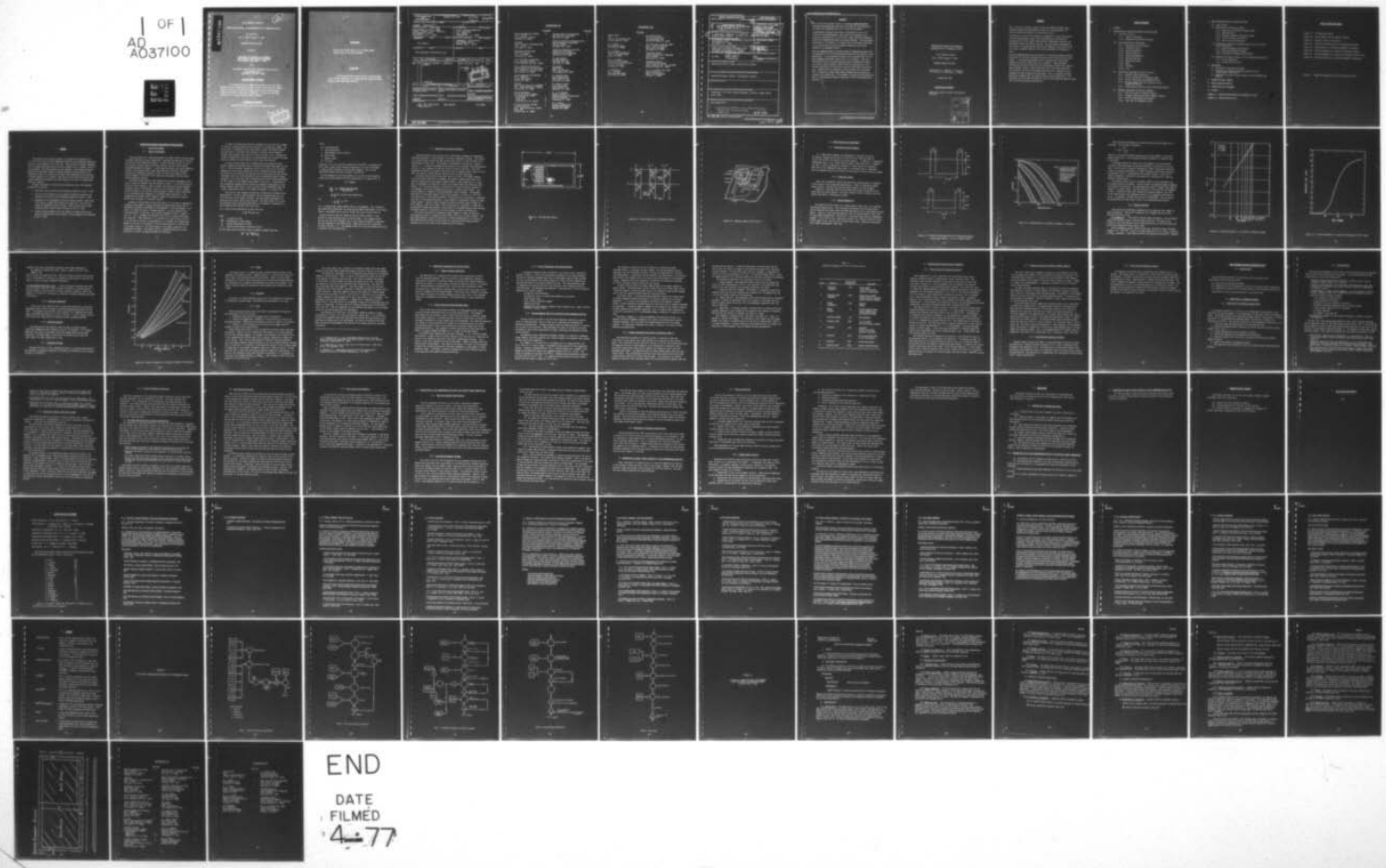

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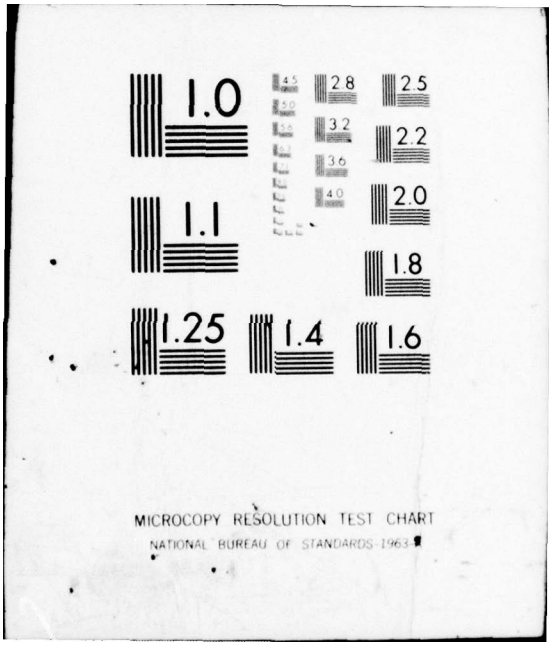
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FIRST QUARTERLY REPORT ON

MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY

for period of

May 7, 1976 to August 6, 1976

CONTRACT DAAB07-76-C-0027

placed by

PROCUREMENT AND PRODUCTION DIRECTORATE
UNITED STATES ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY 07703

with

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WESTINGHOUSE CIRCLE
HORSEHEADS, NEW YORK 14845

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Work has commenced both on the fabrication of Engineering Samples and the preparation of the Pilot Manufacturing Facility for display circuit fabrication. In the Engineering Samples area a complete mask set has been assembled and circuit depositions are in progress. Some unexpected difficulties have been encountered with overheating of masks, but, despite these problems, display circuits have been built containing transistors with excellent electrical performance characteristics. Magnetic pull-up equipment has been designed and constructed. This is required to ensure good contact between mask and substrate during circuit depositions. The equipment has been tested successfully, both in the Engineering Samples system and in the Pilot Manufacturing Facility.

MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR TFT ADDRESSED DISPLAY

First Quarterly Report

May 7, 1976 to August 6, 1976

CONTRACT DAAB07-76-C-0027

Prepared by R. G. Abraham, T. Csakvary,
D. H. Davies, M. Green and W. L. Rogers

October 26, 1976

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1. PURPOSE

The purpose of the present program is to establish the producibility of a Thin Film Transistor (TFT) Addressed Display by mass production techniques and with a mass production pilot facility. Existing quality control procedures will be improved, and where quality control systems are not in effect, they will be introduced. The major objective of the program is to originate production methods and techniques capable of meeting estimated military needs for TFT Addressed Displays for a period of two years after completion of the contract. A further objective is to prepare a base and an action plan which may be used to meet expanded requirements and, when necessary, to assist in establishing additional sources.

The major milestones in attaining these objectives for a TFT Addressed Display are as follows:

1. Fabricate, test and deliver two Engineering Samples by March 7, 1977.
2. Set up a Pilot Production Line, establish production processes and manufacture and deliver two Confirmatory Samples by August 7, 1977.
3. Subsequent to the acceptance of the Confirmatory Samples, operate the Pilot Line at a rate of ten displays per month for a period of two months to manufacture twenty displays. After evaluation and formal acceptance tests, deliver twenty displays by April 7, 1978.
4. Prepare a General Report and a Final Report to record the activity, results and conclusions of the program; these documents to be submitted by May 7, 1978.

2. DESCRIPTION OF DEVICE AND RELATED STATE-OF-THE-ART

2.1 THE TFT-EL DISPLAY

2.1.1 Theory of Operation

The construction of a large multielement flat panel display involves, almost inevitably, some form of matrix addressing. Much work has been done in the past on "passive" matrix-addressed displays. In these displays a grid of X and Y metal busbars extends across the display surface, with the display medium sandwiched between the busbars. In such cases the busbars are simply conductors of power and processed signals while gain producing, switching, and memory functions are provided by external circuits or the display medium itself. Typical examples of displays of this type are plasma panels and the various electroluminescent devices.

The TFT-EL display which is the subject of the present manufacturing program is radically different from the "passive" display. In the TFT-EL display, a grid of X and Y busbars is used to control the individual display elements located at each X-Y intersection, just as in the "passive" display. However, the TFT-EL device is an "active" display because a control curcuit consisting of two transistors and a capacitor is located at each intersection. The presence of the control circuit removes a number of constraints on display medium that are present in "passive" displays.

Another of the functions of the active matrix is to provide a frame-period storage at each element, thereby significantly reducing the voltage and instantaneous brightness requirements of the phosphor. Since the phosphor is ac driven, it cannot be used as a storage capacitor. An extra capacitor and associated switch is required. The resultant elemental circuit is shown in Fig. 2.2. This is probably the simplest circuit that can perform the necessary functions. When transistor T_1 is turned on by a positive gate pulse on Y_j (a whole row is turned on simultaneously), it transfers the voltage which appears at the top of its column X_i to the storage capacitor C_s and the gate of the power switch T_2. The latter controls the ac power supplied to its associated EL element. The element itself is sandwiched between the drain electrode of T_2 and a transparent common top electrode.

In order to specify the electrical parameters for the individual elemental devices, some consideration must be given to the addressing scheme. The array itself is compatible with a wide range of signal distribution methods but does require a periodic signal restore or refresh, and the maximum storage time to access time ratio will have a practical limit. Although the system is designed for data display, for maximum generality standard TV-signal format was chosen for specifications of the signal distribution.

A line-at-a-time rather than an element-at-a-time sequential signal transfer method was selected since it minimized the speed requirements on the TFT's. With this method, information signals for an entire line of display elements are first stored sequentially in an intermediate storage register. The outputs of this register are supplied to the display panel on the vertical information buses (X_i) and transferred to the corresponding element storage capacitors, all at one time, when a switching pulse on the selected horizontal bus (Y_j) closes all the element signal gates in that line. Introduction of the intermediate storage register relaxes the bandwidth requirements of the display element signal gates, as well as those of the information buses, by a factor approximately equal to the number of elements in a display line.

The vertical scan frequency selected has considerable influence on the specification. At 60 Hz, each horizontal line is refreshed every 16.7 ms, the field scan time in normal TV format. The performance requirements imposed upon the circuit can be easily derived. The logic device (T_i) in its ON state must allow the switch capacitance to be charged in a time which is short compared with the dwell time of the scan.

For a line-at-a-time addressing, we must then have

$$T_L \gg R_{ON} (C_G + C_P)$$

where

- T_L line dwelling time
- R_{ON} ON-impedance of logic device
- C_G storage capacitance of switch
- C_P parasitic capacitance in parallel with C_G

and the logic device itself must have a frequency response such that

$$\frac{g_m}{C} = \frac{1}{T_R} = \frac{\mu V_G}{L^2} \gg \frac{1}{T_L}$$

where

g_m transconductance

C input capacitance

μ semiconductor carrier mobility

V_G gate voltage

L channel length

T_R rise time

Assuming L = 2.5 mils and using a mobility of 50 $cm^2/V \cdot s$ as measured in TFT's, then, under typical gate bias conditions, the rise time becomes $\sim$ 0.08 μs which indicates a 2 MHz cutoff frequency. This is also comfortably shorter than the line dwell time (60 μs).

The OFF-impedance of the logic element in turn must be high enough to prevent the stored charge on C_G from leaking away in a frame period T_F

$$T_F < R_{OFF} C_G.$$

Hence,

$$\frac{R_{ON}}{R_{OFF}} \ll \frac{\text{address dwelling time}}{\text{frame period}}$$

$$\ll \frac{T_L}{T_F} \text{ for line-at-a-time addressing}$$

say

$$= \frac{1}{10} \frac{T_L}{T_F} \sim 10^{-3}$$

i.e., a comparatively modest ON/OFF ratio will be adequate. Thus line-at-a-time addressing reduces both the speed and the ON/OFF requirements of the logic device. Such ON/OFF ratios are well within the present state of the art.

During the period when the remaining lines are being scanned, T_1 must prevent C_s from discharging back its stored signal. This leakage current must be less than (C_s X $V_{T2}/\Delta t$), V_{T2} is the T_2 device threshold voltage and Δ t the remainder of the frame period. Under typical circuit conditions, $C_s \sim$20 pF and V_{T2} = 2 V. The leakage current of T_1 must be therefore $<$ 2.5 nA; a difficult, but realizable goal.

2.1.2 Mechanical and Electrical Design

The device which forms the basis of this Manufacturing Methods and Technology Engineering Program is a 256 character flat panel alphanumeric display. The display has an active area of 6.56" by 2.88" and the total device is 7.06" by 3.38" and is approximately 0.125" thick. The mechanical arrangement of the device is shown in Figure 2.1 . In order to manufacture the display in the available Pilot Manufacturing Facility, it was necessary to form the display surface in two parts. The Pilot Manufacturing Facility can handle TFT circuits up to a maximum size of about 4" by 4". Thus, the display is made from two identical 3.53" by 3.38" substrates.

The active display area of the panel consists of 222 X 77 (17,094) elements. In the horizontal direction, the elements are spaced on 750μm centers, and in the vertical direction they are spaced on 950μm centers. Each element has a lit area that is rectangular in shape and is equal to or greater than 0.015 inches by 0.021 inches. If it is found necessary to increase the lit area to improve viewability or brightness, this can be accomplished by using a "second level" process. The display medium is a powder AC electroluminescent (AC-EL) phosphor. The phosphor, which emits in the green region of the visible spectrum, is driven by a thin film transistor matrix. Each display element is controlled by two transistors, a capacitor and a set of interconnecting busbars. Every element is addressable through the edge finger contacts. Typical signal voltages are $\pm$30V, and typical power voltages are 50 to 100V_{rms}. Power (5 to 10kHz, either square wave or sinusoidal) is supplied to the phosphor through edge contacts, and the device is grounded through corner contacts. Brightness control is achieved by EL drive voltage or pulse width modulation.

The circuit design for six adjacent display elements is shown in Figure 2.2. The elemental circuit is repeated at every matrix point over the whole display. The approximate physical layout of the circuit is shown diagrammatically in Figure 2.3. The specific physical layout of the device is a proprietary Westinghouse design completed prior to the start of the present MM and TE Program.

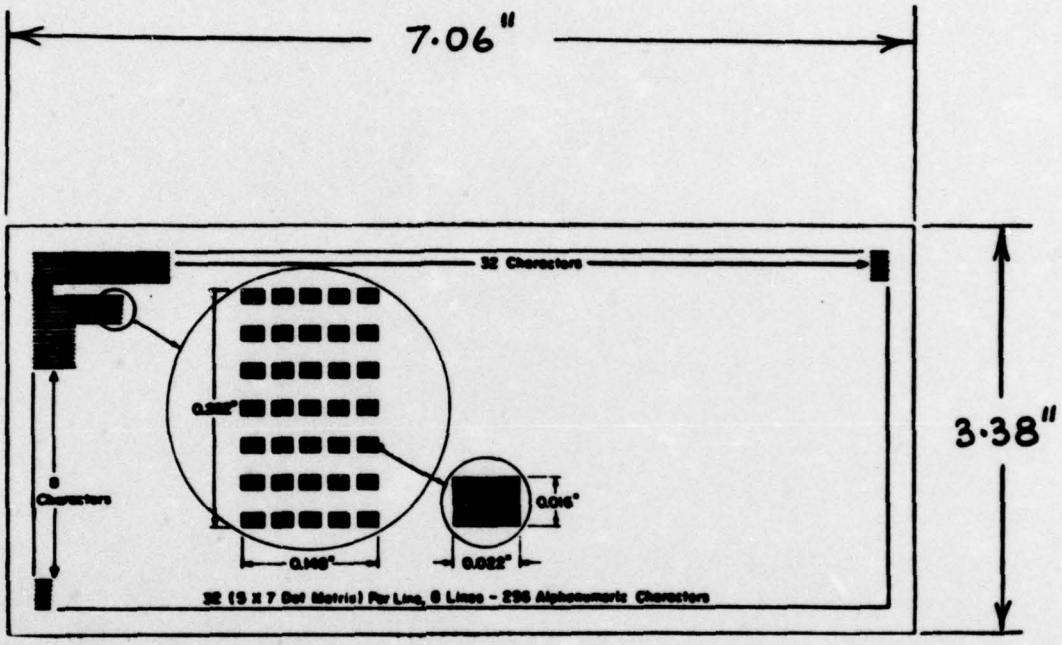


Figure 2.1 TFT Addressed Display

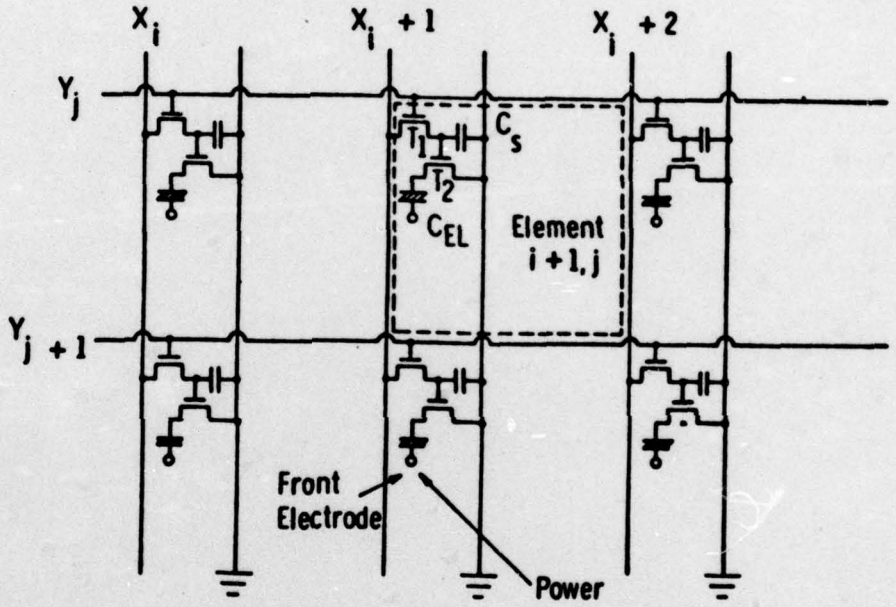


Figure 2.2 - Circuit Design for Six Adjacent Elements

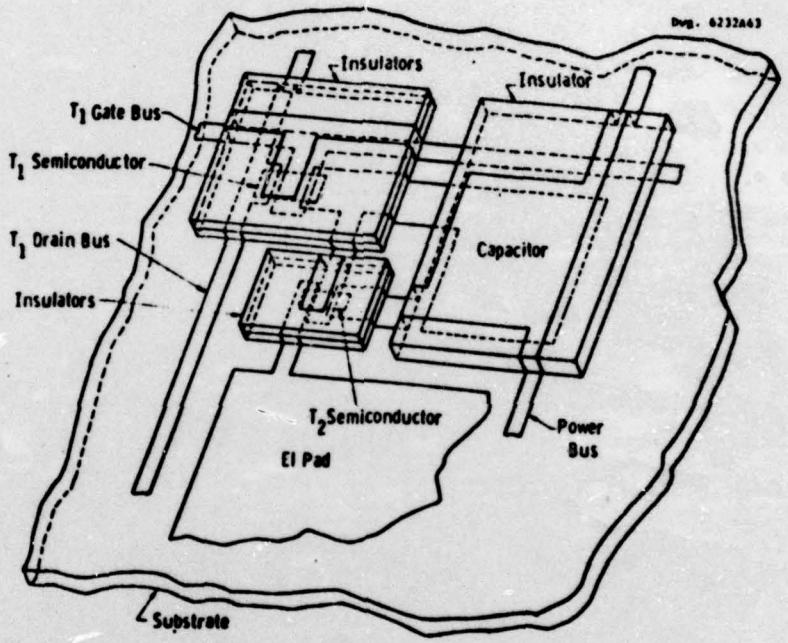


Figure 2.3 - Physical Layout of TFT Circuit

2.2 ANTICIPATED DEVICE PERFORMANCE

2.2.1 Addressable Display Elements

All 17,094 display elements are addressable in the 222 X 77 matrix. The boundary between the two parts of the TFT circuit substrate does not disturb the uniform distribution of display elements. In addition to completely independent access to all 17,094 display elements, 256 blocks of 5 X 7 elements are used to display alphanumeric characters in eight rows of 32 characters. When used in the alphanumeric mode, each 5 X 7 character block is separated from the adjacent block by two columns and three rows of inactive display elements.

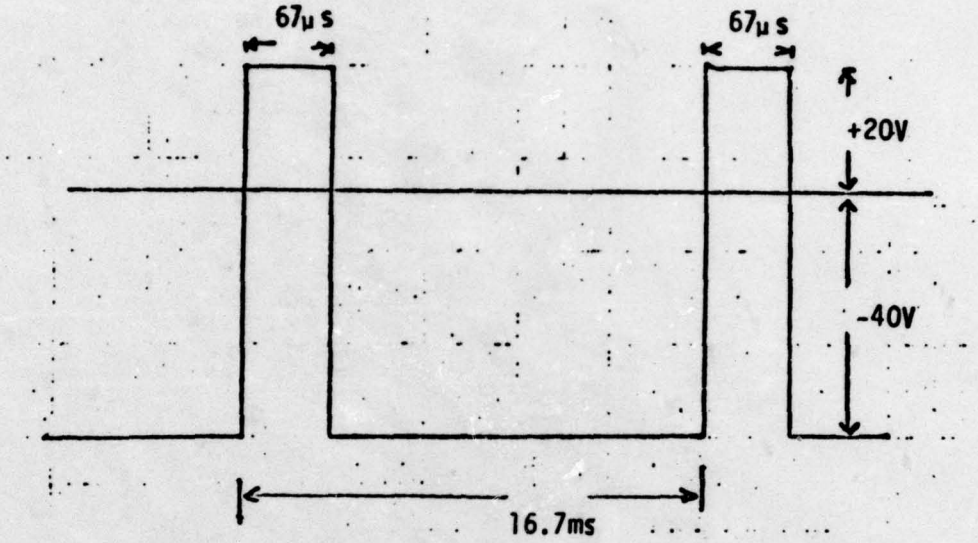
2.2.2 Electrical Inputs

Logic level information (signal gate and source voltage pulses) is supplied to the display via the evaporated edge contacts. Power is supplied by common finger contacts. The gold top electrode makes contact with these fingers.

Figure 2.4 illustrates typical anticipated input pulses as applied to the signal gate and source contacts. The pulse interval varies, of course, with the refresh rate which is nominally 30 to 60Hz.

2.2.3 Display Recognition

The legibility of the display at a 2000fc ambient light level is an important performance characteristic. The anticipated performance of the present device can be predicted from results that have been obtained on similar Westinghouse display panels. Figure 2.5 plots measured contrast ratio (C) against ambient light level for two element brightnesses - 30 and 50 fL - and three simple contrast enhancement schemes - (1) no filter, just a dark blue surround, (2) a Polaroid selective transmission green filter, and (3) a 3M 0° black louver filter. Ambient was generated with a 3200°K photographic flood lamp.



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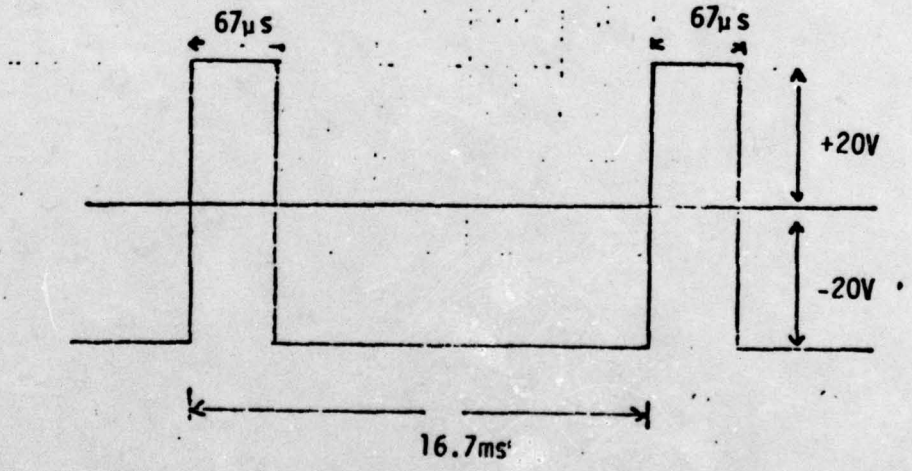

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Figure 2.4 - Electrical Characteristics of TFT Addressed Display.
A, logic gate signals. B, logic source signals.

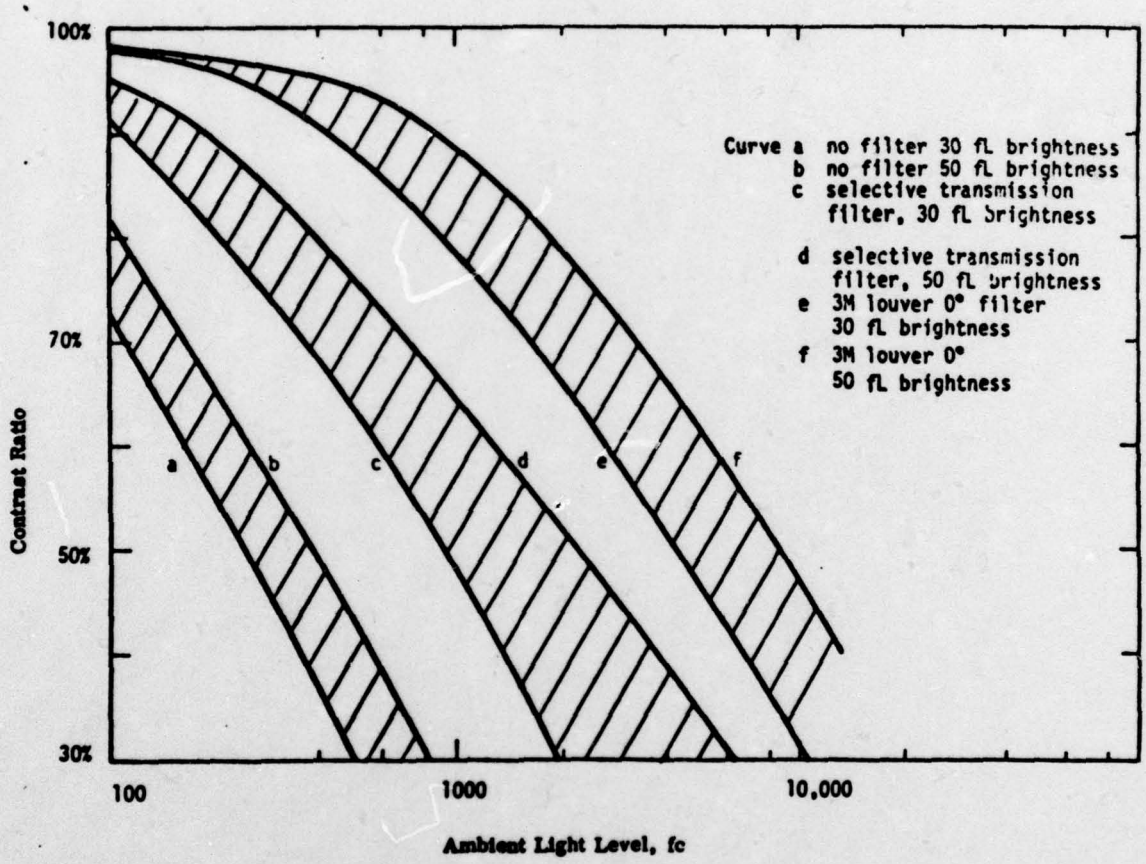

Figure 2.5 - Contrast Ratio as a Function of Ambient Illumination

These contrast measurements give a good evaluation of the legibility of the panel. The contrast is defined as:

$$C = 100 \frac{B_t - S}{B_t} \quad \%$$

where B_t is the total brightness measured on an active element in the given ambient light and S is the scattered brightness measured on a nonactive spot of the panel.

An accepted figure for legibility is that $C \geqslant 30\%$. To be conservative relative to the requirements of the specifications, a 40% value of C will be used. At this level an elemental brightness of 40fL is more than sufficient to meet the required performance at a 2000 fc ambient, providing the selective transmission filter is incorporated on the display surface. Since a 40 fL element brightness is achievable (see Figure 2.6), the display will meet the legibility specification.

The contrast on/off ratio at low ambient (50fc) is also achievable with the present designs and methods. Figure 2.7 shows the measured element brightness as a function of gate bias. This measurement was made in standard room lighting ($\sim$50fc) on a single element. The off brightness is 0.4fL and the on brightness is 40fL. Allowing for some light leakage from adjacent elements, this ratio of 100 should be more than adequate to ensure a real adjacent on/off ratio of $\geqslant 20$. If necessary, a darker surround can be incorporated. This can easily be accomplished with dyed laminar resist or an evaporated black material.

2.2.4 Power Dissipation

Three particular operational configurations are important with respect to power dissipation. They are All Elements On, All Elements Off and All 256 Character Positions in Use.

All Elements On - Two factors influence power dissipation - the dissipation itself and the ohmic losses in the OFF power switch TFT. The latter is not relevant in this consideration since in the ON condition all the TFT switches are ON and the voltage drop across them is small.

With an elemental area of 0.016 by 0.022 mils, the surface area of phosphor element is 22×10^{-4} cm^2. The drive voltage needed for 40 fL is $80V_{rms}$ sinusoidal or $95V_{rms}$ squarewave. Under these conditions the measured dissipation is $50mW/cm^2$.

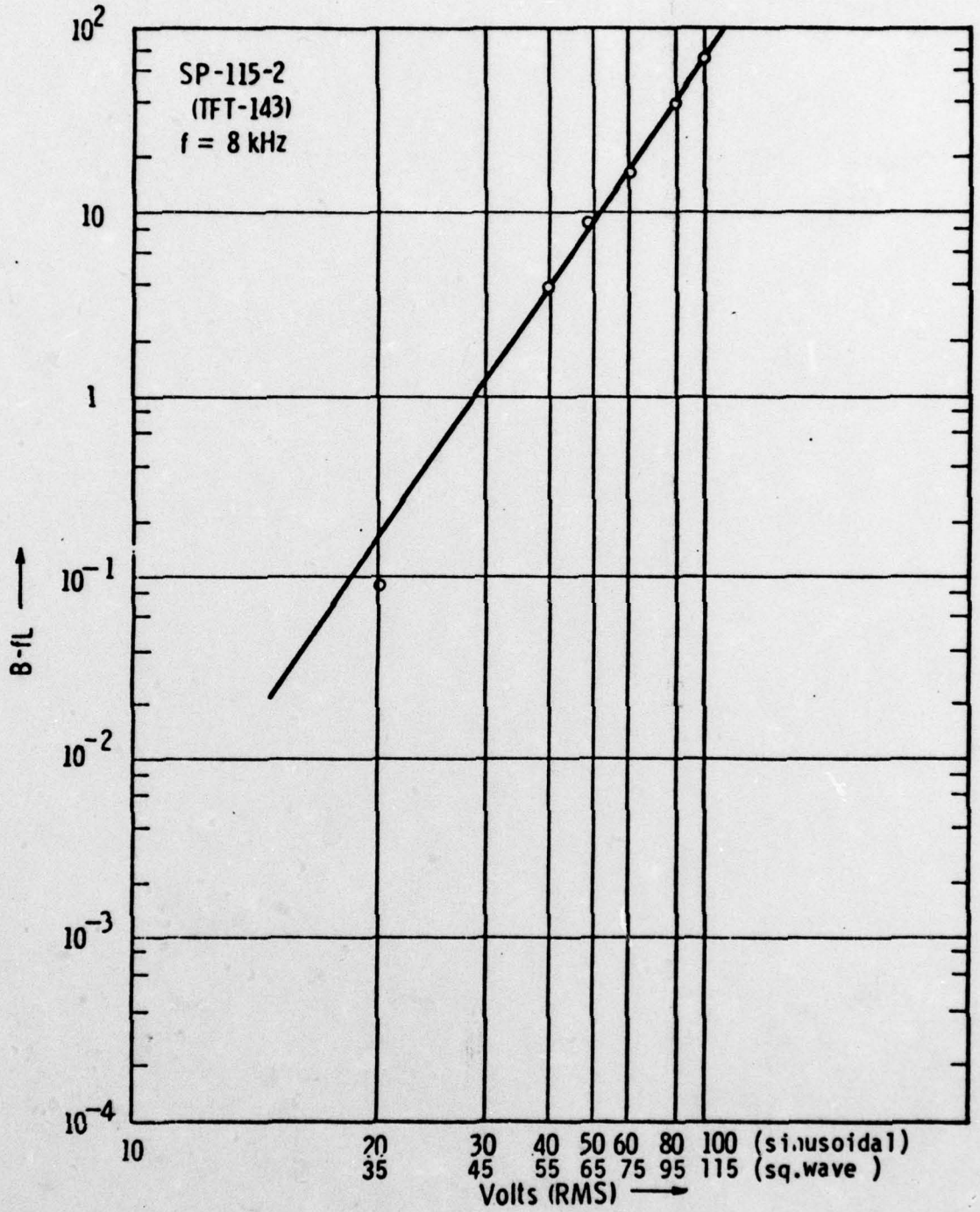

Figure 2.6 - Display Brightness as a Function of Phosphor Voltage

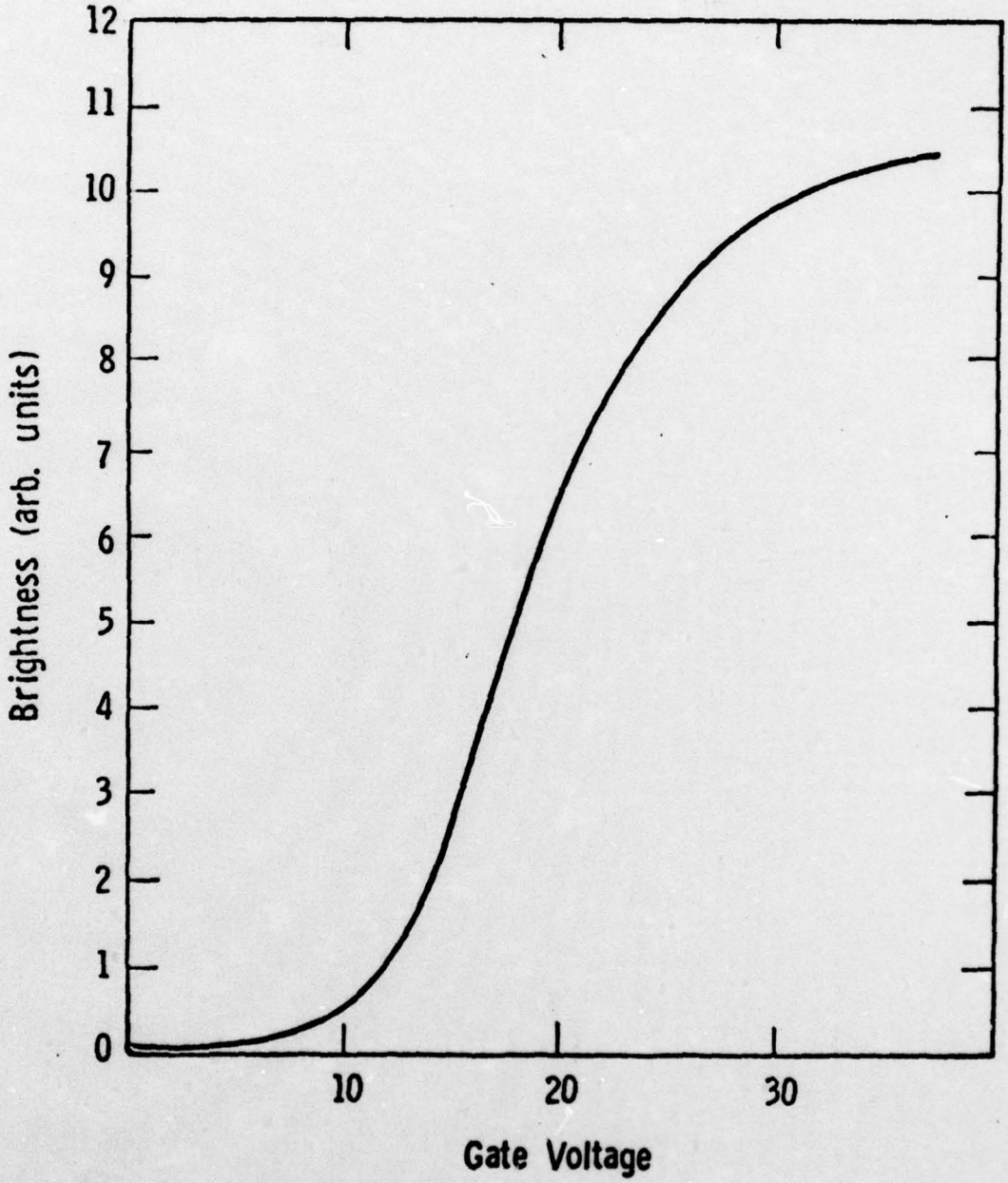

Figure 2.7 - Display Brightness as a Function of Voltage on the TFT Gate

Therefore, the total anticipated dissipation under these conditions is

No. elements x element area (cm^2) x 50mW = 17,094 x 22 x 10^{-4} x 50 = 1880mW = 1.9W

which is within the specified limit. Note this assumes the specification calls for all the elements in the matrix to be ON, even those normally blank when the matrix is used to display alphanumeric characters.

All 256 Character Positions in Use - Similar estimating techniques have been used to generate Figure 2.8, where the power dissipation, including both ON and OFF elements in the matrix and a typical character loading of 35% of the elements in a block ON, is plotted as a function of element brightness and number of characters.

2.2.5 Operating Temperature

Initial tests have indicated that no significant brightness or efficiency degradation occurs within the range of operating temperatures between -45° and +72°C. The phosphor itself suffers little change in this range, and tests have shown no enhanced deterioration or drift in the TFT's. Initial thermal cycling tests within this range have also indicated no major packaging problems.

2.2.6 Operating Humidity

The construction of the display allows the panel to operate without significant degradation after exposure to high or low humidity. Full hermetic edge seals are used, and the double lamination package should provide good protection. The module edge is sealed with the backing plate so that the "path length" for water penetration is long.

2.2.7 Operating Altitude

The panel contains no voids, compressible areas, or gas generating materials and therefore is expected to operate at altitudes up to 30,000 ft. and to survive storage up to 50,000 ft.

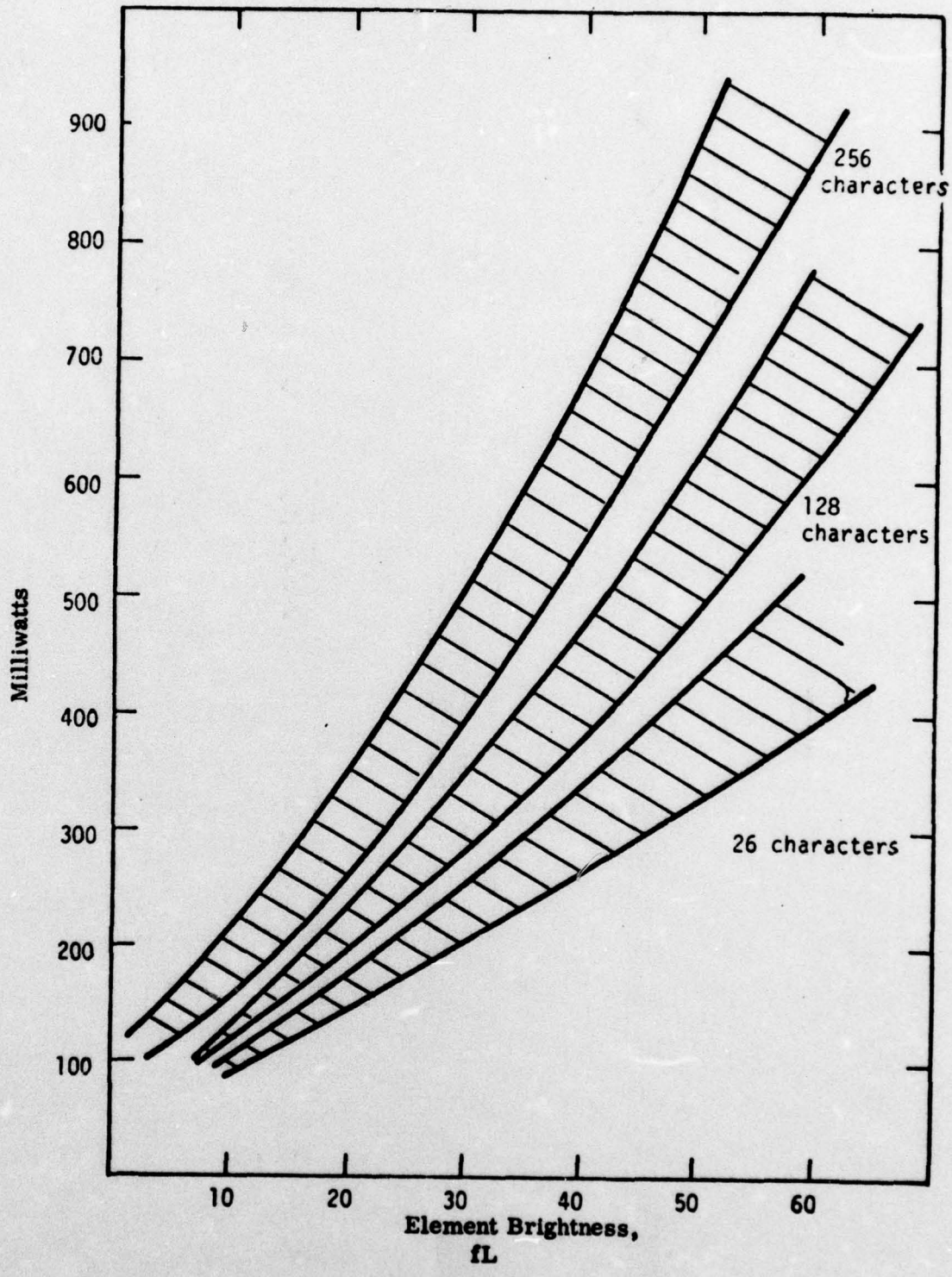

Figure 2.8 - Power Dissipation as a Function of Number of Characters.

2.2.8 Shock

The display panel is a rugged and shock resistant device relative to any comparable glass-based display. Tempered material is used for the front glass cover plate, and the design ensures that the panel is able to survive shock experienced in military vehicle transportation and servicing and bench handling. Our experience with a properly fabricated panel has been very favorable. The double lamination method of fabrication should enhance the resistance to shock damage.

2.2.9 Vibration

The panel is a simple laminated entity with little potential for resonance or destructive vibration modes. No problems are anticipated in this area.

2.2.10 Life

There are three principle areas that should be considered in discussing the anticipated life of the display.

1. Brightness deterioration that will occur with operation.
2. Defects that could occur; elements or lines turning on or off and not being controllable. These could arise because of shorts or opens in the circuit.
3. Changes in the TFT properties with operation that could cause the elements to drift out of specification.

These factors could result in loss of legibility and could affect the power dissipation. However, we are confident that the display will provide adequate life for the following reasons. The change in EL brightness with operating life is well documented and defined under drive conditions comparable to those used in the display. Half lives of approximately 10,000 hours have been observed. Using the known brightness decay characteristic and the voltage-brightness relationship in Figure 26, it is possible to calculate the increase in drive voltage needed to compensate for the phosphor brightness decay over a 600 hour period. We have seen that 40fL is more than sufficient to meet the legibility specification. To maintain this brightness level after 600 hours of operation, it is necessary to raise the drive voltage from $80V_{rms}$ to $88V_{rms}$. This increase is well within the capability of the TFT circuit.

This surprisingly small increase in the maximum voltage rating comes about because of the superlinear brightness/voltage relationship inherent in EL phosphor.

The legibility requirement is also influenced by the possibility of elemental defects in the dot matrix. These, of course, can potentially reduce the ability of an observer to correctly read the data. Two classes of defects are present in the display - initial defects and those that appear during life. The former are counted as scrap and are not therefore under consideration. The latter we have found come under two categories: those that appear in the first few hours of operation due to poor quality crossovers or devices and those that appear during regular operation. Experience suggests that the vast majority of defects appear during the first few hours of life. After this it is relatively rare to observe a defect appearing if the voltage used in the initial burn-in is not exceeded. This phenomenon, called "infant mortality", is common to all integrated circuitry. Based on this, a two hour burn-in at the maximum voltage will be conducted after each display is fabricated. A failure here will then be considered part of fabrication yield, not life. With this condition, we are confident that defects will be minimal and we will be able to meet the life requirement.

The effect of TFT drift over life has been treated at length in various publications[1],[2],[3], and it will not be discussed in detail here. It is sufficient to state that extensive tests over many years have proven that the devices, in the mode they are being used in this application, are free of significant drift that could influence the performance of the device in any respect during the specified life period.

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1. E. W. Greeneich and F. C. Luo, "Performance Characteristics of TFTs used in Large Area Integrated Solid State Displays," Proc. 24th IEEE/ECC Conference, (Washington, D.C. 1974).

2. T. P. Brody et al., "A 6 x 6 inch, 20 lpi EL Display Panel," IEEE Trans. ED-22, 739 (September 1975).

3. E. Schlam et al., "Step-Stress Testing of Thin Film Transistors," Proceeding of the 24th IEEE/ECC Conference, p. 43 (1974).

2.3 FABRICATION TECHNIQUES FOR THE TFT CIRCUIT

2.3.1 General Process Description

The fabrication of a complete TFT-EL Display can be conveniently divided into two separate processes. The first consists of the deposition, through a succession of apertures of different shapes, of the thin film elements needed to make the TFT circuit. In this process a variety of materials, metals, an insulator and a semiconductor, are evaporated onto a glass substrate through metal masks. The second step in fabricating a complete TFT-EL display takes place after the TFT circuit is removed from the vacuum chamber in which the circuit elements are formed. This second step adds an insulating coating to protect the circuit, an EL phosphor layer and a transparent top electrode. The complete device is then hermetically sealed.

2.3.2 Circuit Fabrication with Moveable Masks

Prior to the start of the present contract, all Westinghouse TFT-EL display circuits had been fabricated using a set of two moveable masks. The moveable mask method uses two identical stencil masks each consisting of a regularly spaced set of square apertures. By moving the masks relative to each other, an array of rectangular apertures of various proportions can be generated. By placing the apertures thus formed in varying positions with respect to the substrate glass, the entire interconnected matrix circuit can be generated by successive depositions of the appropriate materials. This approach to circuit fabrication has been described in reports on Contract DAAB07-72-C-0061 and in a number of published papers.

The moveable mask technique has one major advantage. It is a universal method which permits a large variety of circuit layouts to be tried and yet it requires only one set of two identical metal masks with easily formed, square openings. This is clearly a very useful approach for device development. However, moveable masks have some practical disadvantages. They require the talents of a highly skilled operator to ensure the correct positioning of the masks throughout a large number of linked deposition steps. Furthermore, successive evaporations of many different materials on the same mask often leads to flaking and peeling.

2.3.3 Circuit Fabrication with Dedicated Masks

An important change has been introduced in the display circuit fabrication process to adapt it to the pilot production environment of the present contract. The pair of identical moveable masks used for development work has been replaced by a set of ten different masks each containing an array of fairly complex mask openings dedicated to one specific deposition step. This dedicated mask system is designed to be used with the Thin Film Transistor Pilot Production Facility described below. The dedicated mask approach is considered well suited for quantity production for several reasons:

No need for skilled operator.

No scope for errors in setting mask apertures or positions.

Fewer process steps.

Fewer cleaning operations needed.

Reduced cycle time.

Compatibility with forming irregular circuit patterns (e.g., logic, circuits peripheral scanners, etc.).

2.3.4 The Westinghouse Thin Film Transistor Pilot Production Facility

Display circuits are made in the TFT Pilot Production Facility by placing a series of dedicated masks, one at a time, over a substrate and performing the appropriate evaporations. Alignment between successive masking operations is assured by a system of pins and holes. Both substrates and masks are carried by rotating turntables so that various combinations of masks, substrates and deposition sources can be achieved.

The complete circuit fabrication equipment consists of a large fully automated vacuum chamber, electronic controls and a control computer with powerful data storage and data acquisition capability.

The chamber is a cylinder 40 in. in diameter and 10 in deep, with four 8 by 10 in. wells 22 in. deep to permit a reasonable "throw pattern" for the evaporation sources. Pumping is accomplished by a 10 in. diffusion pump with a cryogenic trap, backed by two mechanical pumps with a combined capacity of 27 cu. ft./min. The system can operate in the range of 10^{-8} Torr, although desired evaporation pressures are only from 10^{-7} to 10^{-5} Torr. An automatic pressure controller permits stable backfilling with argon or oxygen up to 10^{-2} Torr.

The evaporation sources consist of a high-rate rf sputtering system (aluminum oxide), a resistance crucible (indium), and two four-hearth electron beam guns, one with fixed-beam for metals and one with swept-beam for insulators and semiconductors. Evaporation rate and thickness are controlled by a rate monitor which detects the frequency shift of a quartz crystal positioned in the evaporant stream. Evaporant flow to the substrate is controlled by electrically operated air-driven trap door shutters placed over the sources.

Internal tooling consists of three stepping motor-driven wheels mounted on coaxial shafts. The bottom wheel carries 12 mask holders; the middle wheel carries 8 substrate holders; and the top wheel holds an air-operated, water-cooled actuator used to push the substrate holders down onto the mask holders.

The control panel is a human-engineered combination control and display panel. It permits complete push-button control of all tooling, pumping and valving, and deposition. It is used as the man-machine interface to the computer to permit process "recipe" generation and modification by individuals with no computer knowledge or experience. It displays computer commands to the system and the system's response to those commands during computer operation. Also, it permits human intervention in case of a malfunction or if an unforeseen change in operation is required at run-time.

The control computer is a 16-bit minicomputer with 32K words of core, a 5-megabyte fixed and 5-megabyte removable disc, digital and analog process control interface equipment, and a real-time disc swapping executive with file manager software. All applications programs are written in Fortran IV for ease of understanding and modification.

2.3.5 Process Description for Circuit Fabrication (Step 1)

The manufacturing process for display circuits is required to form two transistors (a logic device and a power switch) and a capacitor at each picture point, The transistors are dual gate TFT's similar to silicon field effect transistors. The capacitor consists of two conductive films separated by a dielectric layer. As we have already seen, these circuit elements are formed by using a series of dedicated metal masks. The dedicated masks are photo-etched copper which have been nickel plated. They are mounted on stainless steel mask holders which have bullet-n osed precision dowel pins pressed into the edges. The substrates are securely mounted to stainless steel substrate holders with precision-bored alignment holes and

machined Teflon bushings. As the substrate holder is pressed down onto the mask holder, the dowel pins engage in the bushings and provide fine substrate-to-mask alignment. Our experience shows that this alignment is repeatable to within one to two ten-thousands of an inch. To eliminate shadow effect, a powerful magnet mounted in the substrate holder pulls the mask up against the substrate.

The sequence of operations for a particular layer is as follows:

1. Rough Alignment: The appropriate mask is moved over the evaporation source to within approximately 1/16 in.; the substrate is also moved over the source to the same tolerance; the actuator is moved over the source.

2. Actuation and Fine Alignment: The actuator is energized, pushing the substrate down onto the mask, engaging the alignment pins; the magnet pulls the mask up into direct contact with the substrate.

3. Source Power Up: The evaporation source (electron-beam gun or resistance crucible) is heated to evaporation point with a power vs. time ramp; the rate monitor assumes closed loop control for a preprogrammed evaporation rate; the rate is stabilized.

4. Deposition: A trap-door shutter is opened under the substrate and mask, allowing evaporant to pass through the mask apertures and condense on substrate. When the desired thickness is reached, the shutter is closed.

This sequence is repeated for all ten layers (see Table 2.1). Step 1 of Appendix A itemizes the process. The substrate is then removed from the vacuum chamber and placed in an annealing oven for ten hours at approximately 350°C in a nitrogen atmosphere. The main function of the annealing step is to permit the migration of indium (dopant) into the cadmium selenide semiconductor.

TABLE 2.1

Deposition Sequence for Thin Film Display Circuit

Layer	Material	Approximate Thickness, Å	Functions
1	Aluminum (conductor)	1000	Bottom gates Partial interconnects Capacitor (bottom plate)
2	Aluminum oxide (insulator)	5000	Bottom gate insulator Partial crossover insulator Partial capacitor insulator
3	Copper (conductor)	1000	Sources Drains
4	Indium (dopant)	60	Sources adhesion layer Drains adhesion layer Semiconductor dopant
5	Cadmium selenide	120	Semiconductor
6	Aluminum oxide	5000	Cover insulator Partial crossover insulator
7	Aluminum	1000	Top gates Partial interconnect Capacitor (top plate)
8	Aluminum	1000	Electroluminescent pad Partial interconnect
9	Aluminum	1000	Partial interconnect
10	Aluminum oxide	2000	Surface passivation layer

2.4 PHOSPHOR DEPOSITION AND DISPLAY PACKAGING

2.4.1 Thin Film Circuit Insulation (Step 2)

After completion of circuit fabrication and annealing, the next step in forming a complete display is providing the circuit insulation layer. The insulation layer must have openings to the display circuit only in the EL pad area shown in Figure 2.3. This pad together with the phosphor top electrode provides the contacts to the electroluminescent phosphor. The insulation layer is formed from laminar photoresist material. To apply the photoresist, the operating temperature of the laminator equipment is set at 210°F. The tested and approved thin film circuit is then cleaned with ionizing air and brush, and is laminated with a laminar photoresist material between the pressure rollers. Extraneous material is cut off, and the coated circuit examined for ripples, bubbles and other imperfections. If not passable, the photoresist material can be peeled, and the circuit relaminated. The material presently being used is DuPont Riston 110F.

The coated circuit is held for 30 min. in the dark to allow the surface active adhesion promoters to cure at the interface. It is then placed on the bed of the exposure unit which has previously been lit for at least 15 min. The photoplate is placed over the circuit, aligned to it, and clamped with a vacuum pull-down. It is inserted into the unit and a preset time started; at the end of the period (30 sec.), it is automatically ejected from the unit. The exposed plate is now held in the dark for 15 min., the cover Mylar sheet is manually peeled off, and the plate is placed in a holder and developed in 1, 1, 1 trichloroethane. The spray developer consists of three stages: a spray for coarse developing, an isolated chamber for second clean-up developing and a final deionized water rinse. Preset spray timers and pressures (30psi) are used.

The "opened" photoresist coated thin film circuit is now dried with clean air and examined visually. Four parameters are looked for: (1) complete coverage, (2) good clean opening of the apertures over the entire area, (3) a graduated "edge" to the aperture and (4) the absence of blemish and other defects. A negative test result requires recycling of the circuit after a strip and peel operation. A visual check in this step is made for residual resist and for integrity of the thin film deposits. Appendix A gives an itemized list of this process step and the other packaging process described below.

2.4.2 Phosphor Screening and Module Assembly (Step 3)

The first process step subsequent to approval of the photoresist circuit is the abutment and assembly of the two modules that make up the display. The individual module design will, of course, be such that there is 180° symmetry, so that one module turned around is the exact mirror image of the other. Hence, all modules are interchangeable, an important consideration for yield and production considerations.

One edge, the module abutment edge, is polished and straight as purchased. Both modules are placed in a frame assembly and the module locations aligned so that linearity is maintained across the module edge. The assembly is then checked optically for the line linearity and module edge parallelism. A reject here can be corrected by realignment. The pair of modules in their frame are then cemented to the rear backing glass plate.

The curved plates are now loaded onto a movable support that is moved back and forth with a geared drive. A phosphor/binder spray mix is prepared and a controlled spray procedure employed. Our present process utilizes a Devilbis compressed air spray with fixed setting of nozzle and atomizing pressure. A six-layer sequence is now employed with an air brake (135°C) between each step to ensure that each layer is dried. This method has been found to result in smooth, consistent and uniform coatings. The substrate makes several automatic passes across the spray gun, which is fixed in location. All distances, angles, time of spray, etc. are fixed to ensure reproducibility. After completion of the phosphor spray, the surface is treated with a filming resin (methylmethacrylate) to ensure a smooth top electrode surface. This is now accomplished with an aerosol spray of commercial "clear coat" for a controllable time, followed by a final 135°C bake.

2.4.3 Top Electrode Evaporation (Step 4)

Phosphor coated displays from Step 3 are now electroded following our normal procedures with a substrate-to-boat distance of 18 in., PbO is evaporated first, followed by the evaporation of Au. The evaporation is monitored by measuring the resistance of the deposited layer on a microscope slide or by using a quartz crystal thickness monitor. The evaporation is stopped when this resistance on the microscope slide is about 50 ohms/square.

2.4.4 Final Seal and Packaging (Step 5)

The sequence of processes used to provide the final hermetic seal is as follows. The tested display is sprayed with a "clear coat" resin, and the edges are shielded. The epoxy is poured over the panel and the top plate placed over it and compressed in place. Excess material is wiped off and the panel cured. The frame is removed, the contacts covered and the frit squeezed over the edges. The low temperature frit seal is then melted down with a directed heat source. The contacts are then chemically cleaned and solder dipped to improve the contact reliability for spring insertion contacts or to provide a bond for solder contacts. The display is now ready for final test.

3. WORK PERFORMED DURING THE REPORTING PERIOD

3.1 SCOPE OF WORK

Work performed during the first three months of the program may be conveniently divided into three tasks:

(a.) Fabrication of Engineering Samples

(b.) Preparation of Pilot Manufacturing Facility for Display Circuit Fabrication

(c.) Adaptation of Display Circuit Process Recipe to Pilot Manufacturing Facility

The activity in each of these three areas is described below:

3.2 FABRICATION OF ENGINEERING SAMPLES

3.2.1 Objectives of Engineering Samples Phase

As we noted in Sections 2.3.2 and 2.3.3, the alphanumeric display which is the subject of the present program is to be fabricated with dedicated rather than moveable masks. The primary purpose of the Engineering Samples Phase of the program is to check the details of the dedicated mask approach before starting work with the Pilot Manufacturing Facility. More specific objectives of the Engineering Samples Phase are:

1. Prove the design and fabrication of the dedicated mask set.
2. Confirm the expected device properties to ensure that the preliminary process recipe is still valid.
3. Confirm the operation of the alignment fixturing.
4. Confirm the operation of the magnetic pull-up function.
5. Fabricate several thin film circuits and check the functioning of module abutment process.
6. Confirm the phosphor and packaging process.
7. Fabricate two initial displays as close to a required design specification as possible.

3.2.2 Dedicated Masks

The design and procurement of the display circuit dedicated masks were completed prior to start of the present MM and TE program. The following guidelines were incorporated in the circuit design process.

- Optimally determined tolerances to maximize available area for circuit components without added risk of shorting.
- Correctly dimensioned thin film transistors (TFT) (source/drain gap, gate overlap, etc.) to achieve the required electronic function as determined by previous results.
- Incorporation of "jumper" pattern segments, i.e., the insertion of certain material segments to ensure no incompatible material problems at joints.
- Choice of materials known to produce:
  - A low incidence of overlap shorts.
  - A low incidence of TFT shorts.
  - No material junction intermetallic problems.
  - No material expansion properties that can produce "opens".
  - A high voltage, stable thin film transistor.
  - A reliable capacitor.
  - Low leakage in the logic TFT.
- Maintenance of symmetry so that maximum efficiency is achieved in making the photoplate.

The next step in the design process, after a circuit layout had been developed, was to reduce that layout to individual dedicated mask levels. This is the partioning of the segments so that a single metal aperture mask (equivalent to one level) can be made and a single material deposited through it. The assembly of these masks creates the total pattern. Each level was designed with the following constraints in mind:

- Mask physical integrity must be maintained, i.e. enough metal is left and in the right places to ensure no potential weak spots and good overall mask stability.
- Photoplate fabrication rules are maintained, i.e., the limiting apertures, dimensions, travel and tolerances of the MANN photoplate generator. Also machine time is minimized by the use of "integral" (machine number) dimensions.
- Metal mask fabrication rules are maintained; these are complex and involve compensations, correct aperture sizes, relief angles, minimum bridge areas, core thickness rules, etc.

- The set of masks forms a sequence that follows the thin film fabrication rules, viz., maximum efficiency in material selection and sequence, one material per mask in the sequence.

- One complete thin film circuit can be made with ten or fewer masks. This allows several circuits per single pump-down in the pilot fabrication process.

- The process can be "broken" after six depositions without loss of device integrity, i.e., the sensitive surfaces are covered before vacuum is released. This allows us to use the six station Engineering Samples Fabrication System.

3.2.3 Engineering Samples Fabrication System

The Engineering Samples fabrication is being conducted with a vacuum deposition system that is interchangeable in its format, mechanisms and deposition sources with the Pilot Manufacturing Facility.

The mask holder and substrate dimensions are exactly the same, the only difference lies in its overall size, capability (6 mask positions vs. 12 in the pilot line,) and, of course, absence of computer control. The pump configuration is a standard 6 in. diffusion with high vacuum automatic valve and cold trap. The chamber is 24 in. diameter and fitted with two thermal evaporation sources and a rotatable four-pocket Airco 270° 8kW electron beam gun. The control of the deposition is fully automated with crystal rate monitors, Inficon deposition rate and sequence controls, X-Y electron beam sweep controllers and pressure monitoring. The masks are held in the lower wheel and the substrate in an upper wheel, both of which are rotatable. Mask and substrate alignment is achieved with pins and apertures exactly as in the Pilot Facility.

An important feature of the Engineering Samples Fabrication System is the magnetic pull-up equipment used to ensure good contact between the mask and the substrate. After a mask has been placed in intimate contact with the glass substrate, a powerful multipole magnet is lowered so that it comes close to the back of the substrate (on the opposite side of the substrate from the mask). Since the mask is partly made from magnetic material, it is pulled by the magnet into even closer contact with the substrate to ensure sharp pattern outlines during deposition of the circuit components. After a particular deposition step has been completed, the magnet is raised from the rear of the substrate prior to the disengagement of the mask and the substrate to ensure that magnetic forces are not present during the separation process.

3.2.4 Circuit Problems and Solutions

After the preparation of the Engineering Samples System for circuit fabrication had been completed, the first deposition were made. Two major problems were encountered. First, though most of the evaporations gave sharp patterns, the insulator step (Al_2O_3) produced poor edge definition with material scattered into the metal contact regions. Second, after some progress had been made in resolving the first problem, it was found that the bus-bars used to control the transistors located at each picture element were exhibiting very high resistance. In the circuit area the investigation and correction of these problems was the main activity during the present reporting period.

(a) Poor edge definition with insulator evaporations

The association of poor edge definition with only the Al_2O_3 evaporation, suggested that the general mask registration processes were working well for the metal evaporations and that it was necessary to find a cause unique to the insulator deposition. Temperature measurements at the insulator mask during evaporation finally pinpointed the anomaly. It was found that the high power needed to evaporate Al_2O_3 was causing the insulator mask to reach temperatures of over 100°C. This rise in turn caused buckling of the mask with separation of the mask and substrate leading to poor pattern definition. The following steps have been taken to reduce the heating of the mask and to alleviate mask buckling.

- Add an extension cylinder to the Engineering Samples System to increase the throw distance between the Al_2O_3 source and the substrate and mask.
- Rearrange the baffle structure in the evaporator to eliminate heat focussing effects.
- Use slower evaporation rates to reduce power dissipation in insulator source.
- Release one side of the insulator mask so that some expansion can occur without the much more serious buckling effects that occur when all sides of the mask are held.

Experiments are also currently in progress to test the use of thicker masks and magnetic support masks to see if these approaches will have a beneficial effect on the pattern resolution. Results obtained to date show that the definition of the insulator has definitely improved, and this problem is expected to be completely resolved early in the next reporting period.

(b) High Resistance Bus-bars

After the worst effects of the insulator mask distortion had been corrected, display circuits were fabricated containing good working transistors. At this point, it was expected that operable displays would be obtained. However, it was found that the transistors located at each picture could not be controlled even though the transistors themselves were functional. Test and analysis showed that the bus-bars providing the X-Y connections to each picture element had abnormally high resistance which prevented the control signal reaching the transistors.

The source of this difficulty proved to lie in the modifications made in the circuit deposition sequence to adapt it to the available equipment. As noted in Section 3.2.3, the Engineering Samples Fabrication System has six mask positions, and thus the full mask set (10) needed to make a complete circuit cannot be loaded at one time. It is, therefore, necessary to break the fabrication sequence and expose the half-completed circuit to air in order to reload the mask wheel. (This had not proved necessary in previous display circuit work since moveable mask systems had been used). Just prior to breaking vacuum, half completed aluminum bus-bars are deposited. Each of these consist of approximately 80 short sections interrupted by gaps of about the same size. When the process is resumed, after reloading the mask wheel, the gaps are bridged to make complete bus-bars. Unfortunately, a thin layer of aluminum oxide is accumulated on each of the incomplete bus-bar sections by exposure to air. On one junction this oxide layer would not be sufficient to cause a serious problem. However, with almost 160 junctions involved, the resulting resistance of the bus-bars proved to be very high and made the display circutis inoperable.

A relatively simple solution was devised to solve the high resistance bus-bar problem. It involved the deposition of a metallic layer at the junctions of the bus-bar sections. Originally, copper was used and proved moderately successful. The evaluation of the copper technique was complicated by difficulties with the quartz crystal monitor. Eventually, gold was selected to replace copper and has proved entirely successful in producing low resistance bus-bars. The only item remaining for evaluatbn is the possible effect of gold on other performance characteristics of the circuit. This will be investigated when complete displays are built early in the next reporting period.

3.2.5 Panel Sealing and Packaging

In the original sealing and packaging process described in Section 2.4.4, poured epoxy was used to seal the circuit modules to the backing plate. One significant accomplishment has been the identification of some difficulties with this approach and the development of an improved technique for the packaging and sealing of the display.

When the sealing was accomplished with poured epoxy, the epoxy material would sometimes flow into the module joint and interfere with the accuracy of the module abutment. In the new method, the backing plate is covered with a sheet of double sided adhesive tape. The composition of this tape is important. Polyester or polyinide TEMP-R-TAPE is used. Other similar high temperature industrial tapes can be used. The adhesive is a high contact strength siliconematerial supplied by the 3M Company or the Connecticut Hard Rubber Company. The tape covered backing plate is placed in a holding jig to ensure that the circuit modules are in the correct location when the cementing action occurs. Slight pressure is applied to the assembly to get better adhesion.

The entire assembly is now coated with RISTON, and the phosphor is applied by spraying. The top is sealed on with epoxy. A final novel feature is the use of a low melting point glass (such as Electroscience 4008B, 350°C) as a seal along the entire panel edge. With these sealing techniques, it is not possible to pull or lever the assembled panel apart. According to the manufacturer's literature, a force of over 600 lbs. would be needed to pull the tape sealed plates apart.

3.3 PREPARATION OF PILOT MANUFACTURING FACILITY FOR DISPLAY CIRCUIT FABRICATION

3.3.1 Required Equipment Modifications

The Pilot Manufacturing Facility to be used in the present program is described in Section 2.3.4 of this report. The facility was designed to manufacture Thin Film Transistor logic circuits rather than displays and some modifications are required to make it suitable for display manufacturing.

From a process or tooling point of view, logic circuits differ from display circuits primarily in that close spacing of circuit components is not an essential requirement for logic circuits. Logic circuits also have a much smaller total size than a display. As a result, logic circuit masks can be designed with relatively large in-active areas (without apertures), yielding physically stronger, flatter masks and permitting the use of thick back-up plates to maintain flatness and mask-to-substrate contact. The display masks cannot have these large strengthening areas and so do not permit such a general use of back-up plates; some other technique must be used to assure intimate mask-to-substrate contact. The only practical technique demonstrated so far is magnetic pull-up.

The first modification to the equipment, then, was a tooling change to permit magnetic mask pull-up. Several prototype magnetic pull-up substrate holders were made, internal machine tooling was modified to be compatible with these new substrate holders, and production runs using a logic test circuit were made to check operation and effectiveness.

3.3.2 Associated Equipment Problems

The initial test runs with the magnetic pull-up equipment revealed that this modification had placed extra requirements on the mask-substrate alignment mechanism. Before the magnetic pull-up changes, rather large excursions could be tolerated in the initial alignment between the precision dowel pins in the mask holders and the precision Teflon bushings in the substrate holders. Misalignments, perhaps as much as 1/8 of an inch, could be handled without degraded performance. However, after the introduction of magnetic pull-up, the system was found to be intolerant of these initial errors, and produced gross mask-to-substrate misalignment (.010" to .020" errors) and sometimes complete loss of contact between mask and substrate. It

was estimated that this initial misalignment must be reduced to approximately 1/32 of an inch.

The major sources of error were traced to poor reliability (or repeatibility) of the cam detector microswitches, less than optimum design of the switch sensing logic and less than optimum cam alignment and spacing. All three of these sources or error were attacked,and preliminary results indicate that gross misalignment problems using magnetic pull-up substrate holders have been eliminated.

First, the lever arms on the cam sensing switches were replaced with longer, double-acting spring levers to increase the reliability of the switch action and to reduce the effects of slight radial error in accidental cam movement.

Second, three major modifications to the control circuitry were made:

(i) The comparison "window" positioning trigger was shifted from the lead edge of the index cam to the leading edge of the first data cam. (The index cams precede the data cams by about 1/2 inch, but not repeatably).

(ii) The delay between the window positioning trigger and the window was made travel-dependent instead of time-dependent.

The result of the above two changes is that the comparison window now always occurs at the same position on the data cams, regardless of speed. Time-dependent window positioning meant that the on-station comparison was made earlier (in position) on the data cam if the wheel had not completed its acceleration ramp. This required virtually perfect radial alignment of all cams for virtually their entire length, rather than at only two points, as now.

(iii) Acceleration and deceleration circuitry was modified for smoother, more linear and longer ramp functions, to decrease shock forces acting on the drive mechanisms and to reduce over and under travel.

Third, a new procedure was developed to locate and align accurately the cams in the tangential direction. The original cam alignment procedure , used in conjunction with the magnetless substrate holder, consisted of installing a gauge block in the place of the microswitch block and aligning the cam to the gauge block. This procedure allowed the positioning of the cams accurately only in the radial and axial directions, but the alignment in the tangential direction was only approximate. This approximate positioning was quite satisfactory with the relatively stiff logic circuit masks and back-up plates, but became marginal with the use of the new display panel masks. To provide an accurate cam alignment method in the tangential direction, two new set-up gauges were designed and made. It is now possible to locate the cams accurately relative to the substrate and mask holders.

Using the new set-up gauges, all the cams were on the mask wheel and substrate wheel. On the mask wheel, all cams lined up properly, but the spacing between cam #19 and #20 on the substrate wheel showed 0.150 inch deviation. When additional measurements were made on the wheel, it was found that the position of the eight substrate nests (which are supposed to be equally spaced) were machined erroneously in the wheel. While seven positions showed equal spacing ($\pm$ 0.005 inch), the eighth position was off by 0.150 inch. The error was corrected by adding 0.006 inch to each cam position.

Finally, the accuracy of mask and substrate registration was further increased by replacing all the Teflon bushings in the substrate holders with a new type of bushing. By eliminating the entrance cone on the new bushings (which was possible because of the more accurate wheel positioning), the pin and bushing contact area have become significantly larger.

3.3.3 Evaluation of Equipment Modifications

During the month of July 1976, 26 production runs of test devices were made on the Thin Film Pilot Facility to evaluate the magnetic pull-up equipment. Each run represents 21 masked depositions. Of these 546 masking operations, all were within tolerance except three. This is considered well within the acceptable error limits for the machine. Purchase orders have been released for mask holders and magnetic pull-up substrate holders. A complete set of masks has been ordered, although a temporary "hold" has been placed on these until the optimal metal thickness and "bow" problem is clarified.

3.4 ADAPTATION OF DISPLAY CIRCUIT PROCESS TO PILOT MANUFACTURING FACILITY

Actual fabrication of display circuits in the Pilot Manufacturing Facility is not planned to take place until later in the program. However, work has been started to adapt the display circuit process for the Pilot Facility. Two areas that have received attention are described below.

3.4.1 Bus-bar Continuity

Results were reported in Section 3.2.4 (b) concerning the adverse effect on bus-bar electrical continuity of opening the Engineering Samples System during the circuit fabrication process. This was thought to be a trivial problem for the Pilot Manufacturing Facility since it has enough mask positions for all depositons to be made in one pumpdown. However, the circuit recipe requires Al_2O_3 insulator depositions between the interconnect layers, and oxygen backfilling during Al_2O_3 deposition may be required to eliminate dissociation and the resultant trapping of charged aluminum ions in the insulator layers. Consequently, the same problem of insulating interfaces could occur in the Pilot Manufacturing Facility. Several potential solutions have been identified.

1. Eliminate oxygen backfilling - display transistors may not be as susceptible to low-level ion trapping as are logic circuit transistors.

2. Backfill with argon - the dissociation phenomenon may be more sensitive to total pressure than to oxygen partial pressure.

3. Backfill with a mixture of argon and oxygen - perhaps a partial pressure value for oxygen can be found that reduces dissociation without oxidizing existing aluminum films.

4. Change the masks and deposition sequences to eliminate any Al_2O_3 evaporation while partial interconnect layers are on the substrate.

These approaches will be used should bus-bar continuity prove a problem with the Pilot Manufacturing Facility.

3.4.2 Internal Short Circuits

Experience with both TFT logic and display circuits has shown that internal short circuits are a significant yield factor. In preparation for display circuit fabrication, a systematic approach is being used to identify all the possible causative factors and then experimentally determine the relevance of each. The most probable of these are as follows:

1. Contaminants or dust in the chamber initially. These could be deposited on the substrates and masks during roughing or during evaporation.

2. Contaminants and surface defects on the substrates (including glass chips).

3. Contamination of the Al_2O_3 insulator during evaporation by CdSe semiconductor (which is evaporated by the same electron beam gun).

4. Poor quality insulator due to evaporation problems (sputtering and electron-beam centering).

5. Structure or geometry of the crossovers or transistors or both.

6. Deposition materials.

7. Interaction between deposition materials.

8. Lack of repeatability of annealing conditions.

Production runs of test circuits made after very rigorous cleaning of all internal surfaces of the vacuum chamger of the Pilot Manufacturing Facility show a statistically significant decrease in shorts over the same circuits made without any cleaning. However, the short count remained relatively high in both cases. Similar results were achieved by bevelling the substrates to eliminate chipping and then physically scrubbing and inspecting them; the short count was reduced but remained high. Another slight improvement was made by evaporating CdSe semiconductor from a resistance source in another well and evaporating Al_2O_3 exclusively in the first electron beam gun well. Insulator film quality seems to have been improved by proper electron beam centering and by reducing "spitting" during evaporation.

A glass cleaning procedure developed in the laboratory for the engineering samples work was introduced into the pilot facility. It is felt that this technique, which involves mechanical, ultrasonic and chemical cleaning, can have an important bearing on reducing shorts. Dust counts were also made in both the laboratory and pilot facility to assess general room cleanliness. Overall the results were satisfactory though some areas required attention.

Experiments were run in the pilot facility using test circuits in which certain circuit components were omitted. They did not prove completely conclusive, but they did tend to point away from structural problems. Other experiments were run where individual materials were omitted. It was found that extremely low short counts can be achieved by omitting either the CdSe semiconductor or the In, which is used as an adhesion layer and as a semiconductor dopant.

Calibration checks of the annealing furnace have shown that it is functioning properly.

The results of this work are, first, that sound manufacturing techniques and procedures have been developed to reduce or eliminate many second-order causes of short circuits, and second, that the logical choice for the first-order cause has been narrowed considerably to material interaction, specifically indium and cadmium selenide either with each other, or with other materials.

The experiments in which In and CdSe were omitted showed such promise that they were repeated. The results were the same: almost no shorts. Future experimental work will be aimed at pinpointing the specific short mechanism and reducing or eliminating it, and performing more sensitivity analysis to quantify the seriousness of the various short-causing mechanisms.

4. CONCLUSIONS

The progress made during the first three months of the program and the conclusions to be drawn can be most easily summarized by using areas of work designated in Section 3.

4.1 FABRICATION OF ENGINEERING SAMPLES

(a) A complete mask set has been assembled and circuit fabrication is in progress.

(b) Substrate holders, mask holders and magnetic pull-up equipment have been designed and built for the Engineering Samples System and are working successfully.

(c) Some unexpected difficulties have been encountered with overheating of masks leading to buckling and with bus-bar continuity. Solutions to both problems have been found and are in the final stages of being implemented.

(d) Despite these problems, display circuits have been built containing transistors with excellent electrical performance characteristics.

(e) Improved packaging techniques have been developed for the completed display. Adhesive tape has overcome difficulties associated with epoxy cement.

(f) Any delays that have been encountered during the present reporting period are not expected to affect the delivery of two Engineering Samples by March 7, 1977 as specified in the contract.

4.2 PREPARATION OF THE PILOT MANUFACTURING FACILITY FOR DISPLAY CIRCUIT FABRICATION

(a) The magnetic pull-up equipment has been tested in the Pilot Facility.

(b) Modifications were required in the mask and substrate fixturing and the other parts of the facility as a consequence of installing the magnetic pick-up equipment.

(c) These modifications have been completed and verified by a run of test logic circuits.

(d) As a result, fabrication of display circuits will begin on schedule in October.

4.3 ADAPTATION OF DISPLAY CIRCUIT PROCESS TO PILOT MANUFACTURING FACILITY

(a) Work has begun on analyzing bus-bar continuity and internal short circuits in as much as these areas of concern may affect circuit processing in the Pilot Facility.

5. PROGRAM FOR NEXT INTERVAL

The planned activities for the next three months, August, September and October 1976, are listed below:

(a) Fabricate and test Engineering Samples.

(b) Initiate fabrication of displays on Pilot Facility.

(c) Continue design, procurement and debugging of equipment for circuit fabrication, packaging and final test of displays.

6. PUBLICATIONS AND REPORTS

None

7. IDENTIFICATION OF PERSONNEL

Overall supervison - Dr. M. Green and Dr. D. H. Davies

Pilot operation - T. Csakvary, W. L. Rogers, R. E. Stapleton, R. Abraham, S. Burkholder and J. Gessner

Laboratory ES fabrication - Dr. H. Y. Wey and S. Younck

Laboratory ES fabrication (X-Y) - Dr. F. C. Luo and D. W. Yanda

Packaging and performance test - Dr. Z Szepesi and D. Leksell

New mask design and fabrication - L. Siekiewicz and M. Cresswell

Circuit test - P. R. Malmberg and others listed above

Consultation - Dr. T. P. Brody and Dr. F. T. Thompson

During the three months reported here the following personnel worked for the approximate number of hours listed below:

M. Green	100
D. H. Davies	100
T. Csakvary	200
W. L. Rogers	200
R. E. Stapleton	5
R. Abraham	10
S. Burkholder	50
J. Gessner	100
H. Y. Wey	200
S. Younck	100
Z. Szepesi	10
D. Leksell	15
L. Siekiewicz	5
M. Cresswell	5
P. R. Malmberg	5
T. P. Brody	5
F. T. Thompson	5

Note F. C. Luo and D. Yanda (X-Y fabrication of displays) are not directly part of the MMT and E program.

R. G. Abraham, Program Manager, Advanced Manufacturing Technology

M.S., electrical engineering, University of Pittsburgh, completed course work for Ph.D. E.E.

Member, IEEE, ISA, SME, Eta Kappa Nu, Tau Beta Pi.

Mr. Abraham has 17 years' experience in the engineering fields. His present responsibility includes factory automation, adaptive control, computer controlled welding, thin film circuit pilot facility, and automatic inspections. From 1967 to 1971, Mr. Abraham worked at Westinghouse Information Systems Laboratory on automated systems for traffic control, transit systems, laboratory automation, and environmental control. Prior to 1967, Mr. Abraham's engineering activities included power plant modeling simulation, control and testing, on-line computers, metal processing lines, and color tube manufacturing.

Publications:

"Modelling, Control, and Testing of a Large Control Station," proceedings of Intl. Sem. on Automatic Control in Production and Distribution of Electric Power, 1966.

"Digital Simulation Techniques," Westinghouse Software Symposium, 1967.

"Simulation of a Large Central Station," IEEE Convention Record, 1967.

"System Analysis by Digital Computer," a book review, IEEE G-AC Trans., 1967.

"Hybrid Simulation of a Large Central Station," Mideastern Simulation Council, 1968.

"Power Plant Control System Design Using Hybrid Simulation," Simulation Magazine, 1969.

"Simulation of Large Power Plants," Process Automation Symposium, 1969.

"How Data Systems Are Affecting Decision Making," Automation Magazine, 1969.

"How Data Systems Are Affecting Decision Making," Power and Plant Magazine, 1971.

"Westinghouse Progress in Adaptive Control," Westinghouse Machine Tool Forum, 1973.

Westinghouse

R. G. Abraham (Continued)

"Computer-Controlled Welding," Westinghouse Welding Technology Seminar, 1973.

"Derivation of Economic Dispatch Equations — A Step in Automation of Gas Transmission Systems," Trans. AIEE, 1961.

T. P. Brody, Manager, Thin Film Devices

B.Sc. (special), physics; Ph.D., mathematical physics, University of London.

American Physical Society, Institute of Electrical and Electronics Engineers, Society for Information Display.

Dr. Brody has 18 years of experience in industrial research and 3 years as a lecturer in physics at British universities. His technical contributions have been in the area of resistivity, lifetime, surface preparation, field effect and surface barrier transistors, pulse measurements on single crystals, diodes and transistors, tunnel diodes, and solar cells. Dr. Brody has also made contributions in carrier transport, luminescence, information theory, and tunneling in thin insulating films. His recent work has been concerned with thin film active devices, circuits, displays, and pattern recognition.

Technical publications include:

"Impurity Band Conduction and the Problem of Excess Current in Tunnel Diodes," J. Appl. Phys., 32: 746 (1961).

"The Evaluation of Esaki Integrals and an Approximate Expression for the Tunnel Diode Characteristic," with R. H. Boyer, Solid-State Electronics, 2: 209 (1961).

"An Alternative Approach to the Solution of Added Carrier Transport Problems in Semiconductors," with J. P. McKelvey and R. Longini, Phys. Rev., 123: 51 (1961).

"On the Nature of the Valley Current in Tunnel Diodes," J. Appl. Phys., 33: 100 (1962).

"Flux Analysis of a Transistor Structure," Proc. IRE, 50: 1524 (1962).

"Thin Film Active Devices—Some Current Physical and Technological Problems," Proc. 10th International Congress on Electronics, Rome, Italy (1963).

"Double Injection Luminescence in CdS," with D. J. Page, presented at IEEE Solid State Device Research Conference, Boulder, Colo. (1964).

"Saturating Rate Law in Chemisorption and Oxidation," with R. Hooke, J. Chem. Phys., 42: 4310 (1965); 45: 2337 (1966).

"A High Gain InAs Thin-Film Transistor," with H.E. Kunig, Appl. Phys. Letters, 9: 259 (1966).

T. P. Brody (Continued)

"Flexible Thin Film Transistors," with D. J. Page, Electronics (Aug. 19, 1968).

"A Transformation with Invariance under Cyclic Permutation for Applications in Pattern Recognition," with H. J. Reitboeck, Information and Control, 15:130 (1969).

"Flexible Transistors, Large Scale Integration and Displays," with D. J. Page, Proc. 1969 Govt. Microcircuits Applications Conf., Sept. 1969.

"Flexible Transistors: Cost vs. Performance," with D. J. Page, Int. Electron Devices Conf., Washington, 1969.

"Thin Film Active Devices — Present and Future," Proc. 26th NEC, Chicago, 1970.

"Design of a Liquid Crystal Color TV Panel," with A. G. Fischer and W. Escott, IEEE Conf. on Display Devices, 1972.

"A 6 × 6 inch, 20 Lines per Inch Liquid Crystal Display Panel," with J. A. Asars and G. D. Dixon, IEEE Trans. ED, 20:995 (1973).

"Alignment Mechanism in Twisted Nematic Layers," with G. D. Dixon and W. A. Hester, Appl. Phys. Lett., 24:47 (1974).

"Prognosis for CdS Solar Cells," with F. A. Shirland, in Proc. Symp. on Material Science Aspects of Thin Film Systems for Solar Energy Conversion, p. 170, Tucson, Ariz. (1974).

"Performance of a 6 × 6 inch, 20 lpi Liquid Crystal Display Panel," with F. C. Luo, D. H. Davies, and E. Greeneich, SID Int. Symposium, San Diego, 1974.

"Experimental Realization of Floating Gate Memory Thin Film Transistors," with P. C. Y. Chen and K. K. Yu, Proc. IEEE, 63: 826 (1975).

"A 6 × 6 inch, 20 lpi Electroluminescent Display Panel," with F. C. Luo, Z. P. Szepesi, and D. H. Davies, IEEE Trans., ED-22: 739 (1975).

"Electroluminescent Display with Nonvolatile Storage," with K. K. Yu and L. Sienkiewicz, SID Int. Symposium, Washington (1975).

"Large Scale Integration for Display Screens," IEEE Trans., CE-21: 260 (1975).

"Integrated Electrooptic Displays," in BBC Symposium on Nonemissive Electrooptic Displays, Baden, Switzerland, 1975 (to be published).

T. Csakvary, Fellow Engineer, Advanced Manufacturing Technology

B.S., mechanical engineering, Polytechnic University of Budapest, Hungary; M.S., metallurgical engineering, University of Pittsburgh.

Mr. Csakvary has 21 years of experience in manufacturing, materials engineering, and advanced manufacturing development, of which 9 years were spent in the Westinghouse Semiconductor Division. Currently, he is involved in the development of computer-controlled automatic equipment, process and low-cost packaging methods for flexible substrate thin-film integrated circuits. Previous assignments included: development of non-conventional manufacturing techniques, such as hot machining, adaptive control for EDM, electrochemical grinding and electron beam welding; design and development of automatic vacuum equipment for testing lighting arrester and high voltage switchgears; development of equipment and manufacturing methods for high volume production of semiconductor (SiC) high temperature sensor; and consulting service for different Westinghouse Divisions.

Prior to transferring to the R&D Center, Mr. Csakvary was Senior Engineer at the Westinghouse Semiconductor Division's Advanced Manufacturing Development Department. His activities included: Improvement of the processing of silicon crystal (I.D. cutting, high speed lapping, large batch alloying); development of high reliability semiconductor devices; high volume low-cost production of automotive semiconductor devices; low-cost powder metal substrate development for semiconductors; material evaluation; and failure analysis.

Patents:

Low Melting Point Brazing Alloy
Electrical Contact for Semiconductor Devices
Sintered Electrical Contact Members
Method of Making Semiconductor Devices
Semiconductor Device Base Assembly
Semiconductor Crystal Slicing Device

D. H. Davies, Manager, Thin Film Materials

B.Sc., chemistry, University College, London, with first class honors; Ph.D., physical chemistry, University College, London; M.B.A., University of Pittsburgh.

Member, Institute of Electrical and Electronics Engineers, Electrochemical Society.

Dr. Davies has 8 years of experience with Westinghouse in the fields of photo-organic interactions, fluorescent materials, and display technology. Three years prior experience included fundamental studies of physical-organic mechanisms in the gas phase.

Dr. Davies has devoted considerable effort to studies of the interactions of phosphors with various organic and inorganic materials. This work has led to a number of improved Westinghouse products including fluorescent lamps and color picture tubes. A major area of study has been photoinitiated processes. Currently Dr. Davies has responsibility for the area of thin film solid state display systems and photovoltaic technology. He is directly involved in research on high resolution thin film transistor circuits, display and optoelectronic logic.

Dr. Davies has several issued and pending patents in the display area and has 28 published papers. Examples of his published papers are:

"A 6 × 6 in. 20 lpi Electroluminescent Display Panel," with T. P. Brody, F. C. Luo, and Z. P. Szepesi, IEEE Trans. Electron Devices, 20:739 (1975); also SID Digest, Spring Meeting, 1975.

"A 350 Character TFT-EL Display," with T. P. Brody, F. C. Luo, and Z. P. Szepesi, to be presented at the IEDM Conference, Washington, December 1975.

"TFT Matrices for Parallel Optical Logic, the Image Negator," with T. P. Brody and Z. P. Szepesi, to be presented at the IEDM Conference, Washington, December 1975.

"PC-EL Radiographic Image Converters," with Z. P. Szepesi, to be presented at Scientific Assembly of the Radiological Society of N. America, December 1975.

"Photodepolymerization of Hydroxy Propylmethyl Cellulose," with G. D. Dixon, J. Applied Poly. Sci., 16:2449 (1972).

D. H. Davies (Continued)

"Copolymerization of Styrene and Diethylfumarate with Zinc Bromide. Part III. Electroinitiation at Low Current Densities," with D. C. Phillips and J. D. B. Smith, J. Poly. Sci. (A1), 10:3267 (1972).

"Copolymerization of Styrene and Diethyl Fumarate with Zinc Bromide. Part IV. Comparison between Photo- and Electroinitiation," with D. C. Phillips and J. D. B. Smith, J. Poly. Sci. (A1), 10:3253 (1972).

"Polymerization of N-vinyl Carbazole. Part II. The Kinetics of Polymerization," with D. C. Phillips and J. D. B. Smith, Makromol. chemie., 177:169 (1973).

"Copolymerization of Substituted Imidazoles with Acrylic Acid," Macromolecules, 6:163 (1973).

"The Electro-cyclodimerization of N-vinyl Carbazole," with D. C. Phillips and J. D. B. Smith, J. Organic Chem., 38:2562 (1973).

"The Copolymerization of Styrene and Diethyl Fumarate with Zinc Bromide. Part V. Electroinitiation at High Current Densities," with D. C. Phillips and J. D. B. Smith, J. Poly. Sci., 1867:11 (1973).

"A Cumulative Chemical Lightmeter," with G. D. Dixon, Environmental Science and Technology, 234:9 (1975).

"The Phosphor Coating Process for Lamps," with R. G. Young, Electrochemical Society Symposium, Keynote Address, 1974 ECS Conference, San Francisco.

"Dichromate Resists for CRT Screen Processes," with M. E. Cekoric, H. M. Patel, and D. O. Griswold, ECS Symposium on Phosphor Screens, 1974 ECS Conference, San Francisco.

"Performance Characteristics of a 6 in. × 6 in., TFT, liquid crystal display Panel," with T. P. Brody, F. C. Luo and E. W. Greeneich, S.I.D. Spring Meeting, San Diego, Calif., May 1974.

Westinghouse

M. Green, Advisory Engineer, Industrial and Government Tube Division

B.A., M.A., and Ph.D., physics, University of Cambridge, Cambridge, England.

American Physical Society, American Astronomical Society, Member of NASA Advanced Imagery and Scanner Working Group for Earth Resource Technology.

Dr. Green has 15 years of experience including three years of teaching experience at the undergraduate level. His postgraduate research at Cavendish Laboratory, Cambridge, England, including studies of electron scattering, x-ray production, and x-ray detection and correction procedures in quantitative x-ray microprobe analysis.

He joined Westinghouse Research Laboratories in 1962 and investigated field enhanced secondary emission related to the development of sensitive image intensifiers and camera tubes. Since 1964 he has been with the Electronic Tube Division where he has conducted research work with secondary electron conduction targets emphasizing characteristics related to resolution performance in practical devices. Other projects concerned the engineering and customer applications aspects of Westinghouse image sensors including the SEC tubes used in the Apollo color television cameras; the design, development and manufacture of the WX-31381 zoom camera tube employed in the B-57G and B-52 aircraft and the WL-30691N low-light-level sensor used in the scientific instrument packages of the OSO-7 and Skylab satellites; and production of Westinghouse image tubes including the WX-31381 and the WX-31683 color broadcast camera tube.

Recent work has focused on development of electron bombarded silicon target devices, and special SEC camera tubes for the International Ultraviolet Explorer and Large Space Telescope satellites, for the Space Shuttle, and for a variety of military aircraft avionics systems.

He is the author or co-author of 12 publications; a few are referenced below.

"Field Enhanced Secondary Electron Emission from Films of Low Density," with co-author, J. of Appl. Phys., 35:482 (1964).

"Point-Source Imaging with the SEC Target," Advances in Electronics and Electron Physics, 22:251 (1966).

"The Application of SEC Camera Tubes and Electrostatic Image Intensifiers to Astronomy," with co-author, Advances in Electronics and Electron Physics, Vol. 28, p. 807, Academic Press, London and New York, 1969.

F. C. Luo, Senior Engineer

B.S., electrical engineering, Cheng Kung University; M.S., Ph.D., electrical engineering, Northwestern University.

Institute of Electrical and Electronics Engineers.

Dr. Luo has six years of research experience in the field of thin film devices. He has done research in the areas of very high mobility InSb thin films, electrical and piezoelectric characteristics of InSb thin film transistors, and CdS and CdSe thin-film-transistor applications. Since 1973, he has been responsible for the development of active thin film matrix circuits for LC and EL display panels.

Publications include:

"Coplanar-Electrode Thin Film InSb Transistor," with M. Epstein, Proc. IEEE, 60:997 (1972).

"Strain Sensitivity of Thin Film Transistor," with M. Epstein, Proc. IEEE, 61:129 (1973).

"Surface Depletion of InSb by SiO and CaF_2," with M. Epstein, Appl. Phys. Lett., 22:101 (1973).

"A 6 × 6 Inch TFT Addressed Electroluminescent Display Panel," with T. P. Brody, D. H. Davies, and Z. P. Szepesi, presented at Int. Electron Devices Meeting, Washington, December 1973.

"Performance of a 6 × 6 Inch 20 Lines Per Inch Liquid Crystal Display Panel," with T. P. Brody et al., presented at SID Int. Symposium, San Diego, 1974; and WESCON, Los Angeles, 1974.

"Performance Characteristics of Thin-Film Transistors Used in Large-Area Integrated Solid-State Displays," with E. W. Greeneich, Proc. 24th IEEE/ ECC Conf., Washington, 1974.

"A 6 × 6-in. 20 lpi Electroluminescent Display Panel," with T. P. Brody et al., IEEE Trans. Electron Devices, 20:739 (1975).

"A 350 Character TFT-EL Display," with T. P. Brody et al., to be presented at Int. Electron Devices Meeting, Washington, December 1975.

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William L. Rogers, Senior Engineer, Advanced Manufacturing Technology

B., electrical engineering, Ohio State University.

Mr. Rogers has 14 years of engineering experience, primarily in the area of electronic and electrical systems. Currently he is project engineer for the Thin Film Pilot Production Facility. He is responsible for the technical project management, all electrical and electronic systems including control computer hardware and software, transistor and circuit test procedures, and data acquisition and interpretation.

Most of his recent work has been in computer control and instrumentation, and includes a computer-controlled, learn-and-repeat MIG welder, a computer-controlled theatre stage lighting system, adaptive control for electrical discharge machining, a computer control and interpreting system for a pathology laboratory blood-analysis machine, a final test system for distribution transformers, and a data acquisition and test system for nuclear rocket fuel cores.

Prior to joining Advanced Manufacturing Technology, Mr. Rogers was an instrumentation engineer in the Molecular Electronics Division for six years. There he was responsible for dynamic testing of all digital integrated circuits. He organized the procedures for maintenance of production-line test-program integrity, calibration standards, and machine verification; and improved the in-line wafer testing area by instituting automatic testing equipment. He designed and built a computer-operated dynamic test system for high-speed, digital integrated circuits that could resolve nanosecond switching times with a high degree of repeatability.

Mr. Rogers joined Westinghouse in the Development Engineering Section of the Westinghouse Room Air-Conditioner Division in 1961. His primary areas of responsibility were product development and testing. In 1964, he transferred to the Engineering Services Group and was responsible for the automated data-acquisition system of the Refrigerator and Water Cooler Divisions.

Westinghouse

Z. P. J. Szepesi, Fellow Scientist

B.S., M.S., mathematics-physics-pedagogy, University of Szeged (Hungary); Ph.D., physics, University of Budapest (Hungary).

Member, Société Française de Physique; Canadian Association of Physicists.

Thirty-seven years of research experience in the fields of atomic physics, electron physics, microwaves, and semiconductors. He proved experimentally the validity of the Klein-Nischina formula for the distribution of Compton-scattering of γ-rays; proved the theoretical formula of Schottky and Thompson on the space-charge limited shot noise; developed a high-gain microwave slot antenna system on circular waveguide; developed a fabrication method for high gain evaporated CdS photoconductive cells; and developed solid state image intensifiers and storage and nonstorage type radiographic converter screens. Dr. Szepesi has eight patents.

Dr. Szepesi is the author of papers in English, German, French and Hungarian; he has presented papers at technical societies and conferences. In addition, he is the author of over 80 technical reports on research and development work. A few of his publications are listed below.

"Über die Streuung von γ-Strahlen," with Z. Bay and G. Papp, Naturwissenschaften, 25: 366 (1937).

"Repartition of the Intensity of Compton-scattering," Doctor's thesis, presented to the Hungarian Academy of Sciences at Budapest, June 7, 1937; Matematikai és Term. - tud. Ért., 56: 637-654 (1937).

"Über die Intensitätsverteilung der Compton - Streuung von γ-Strahlen," with Z. Bay, Zs. für Physik, 112: 20-28 (1939).

"Noise of Frequency Changer Valves," with E. Lukács-P. Preisach, Wireless Eng., 15: 611 (1938); Wireless Eng., 16: 135 (1939).

"The Temperature Response of the Shot-effect of Valves with Oxide-coated Cathode," Wireless Eng., 16: 67-71 (1939).

"Système de fentes sur la paroi d'une guide circulaire ayant une diagramme de rayonnement en fuseau," C.R. Ac.Sc. Paris, 226: 883-885 (1948).

"Circular-ring Filters in Round Waveguide," Wireless Eng., 26: 345 (1949).

"Rôle du circuit cathodique dans les oscillateurs a triode en hyperfréquence," J. Phys. et Rad., 11: 488-498 (1950).

Z. P. J. Szepesi (Continued)

"Filtre en anneau pour les ondes de type H_{11} dans les guides circulaire," Onde Electrique, 30: 230-234 (1950); Onde Electrique, 30: 293-298 (1950).

"Antennes directives pour ondes centimetriques," with J. Benoit, P. V. Mens. de la Soc. Sci. du Dauphiné, 63: 34-40 (1948).

"Cadmium Sulphide Photoconductive Cells with High Dissipation Rating," with D. A. Anderson, Electronics and Comm., 3 (3): 27 (1955).

"Comparison of the Electrical Characteristics of Cadmium Sulphide Evaporated Layers and Grown Crystals," Report on Sixteenth Annual Conf. Phys. Electronics, MIT, 1956.

"Time Constants in Photoconductive Cells," Bull. APS, 2: 186 (1957).

"Characteristics of Evaporated Cadmium Sulfide-Cadmium Selenide Photoconductive Layers on Various Substrates," Report on Twentieth Annual Conf. Phys. Electronics, MIT, March 1960.

"Photoconductor-Electroluminescent Display Panels on Fotoform Glass," paper presented at 1962 International Solid State Circuit Conference, p. 86-87.

"Solid State Image Intensifiers, Radiographic Amplifiers and Infrared Converters," Electro-Technology, 84: 47-53 (1969).

"Solid State Radiographic Amplifiers and Infrared Converters," with M. Novice, in Advances in Electronics and Electron Physics, Vol. 28B, pp. 1087-1098, Academic Press, London and New York, 1969.

"Improvements in Solid State Radiographic Converter Screens," in Proc. of Society of Photo-optical Instrumentation Engineers, Vol. 29, Imaging Techniques, pp. 31-37, SPIE, Los Angeles, 1972.

"Thin Film PC-EL Sandwich Type Image Intensifiers," Thin Solid Films, 13:397-400 (1972).

"A 6 × 6-in. 20-lpi Electroluminescent Display Panel," with T. P. Brody, C. Luo, and D. H. Davies, in IEEE Trans. Electron Dev., ED-22:739-748 (1975).

Westinghouse

H. Y. Wey, Senior Scientist

B.S., physics, National Taiwan University, Taiwan; M.S., Ph.D., physics, The University of Chicago.

American Physical Society.

Dr. Wey has 5 years of research experience in the field of photoelectric, surface, and interface properties of amorphous semiconductors. Dr. Wey has investigated the properties of contacts between a variety of metals and amorphous semiconductors under various preparation conditions. He also studied the space charge region near the free surface of amorphous semiconductors by measuring contact photovoltage, surface photovoltage, and space charge capacitance. Since joining Westinghouse Dr. Wey has been studying the contact properties of CdSe thin film transistors (TFT) and has been involved in the development of a TFT-EL panel display.

Publications include:

"Photovoltaic Effect and Space Charge Capacitance of Amorphous Semiconductors-Metal Contacts," with H. Fritzsche, J. Non-Cryst. Solids, 8-10: 336 (1972).

"Properties of Amorphous Semiconductor Contacts," with H. Fritzsche, Bull. APS II, 17: 345 (1972).

"Contact and Surface Photovoltage of Amorphous Semiconductors," with H. Fritzsche, Proc. of XI Intl. Conf. on the Physics of Semiconductors, Warsaw, p. 555, 1972.

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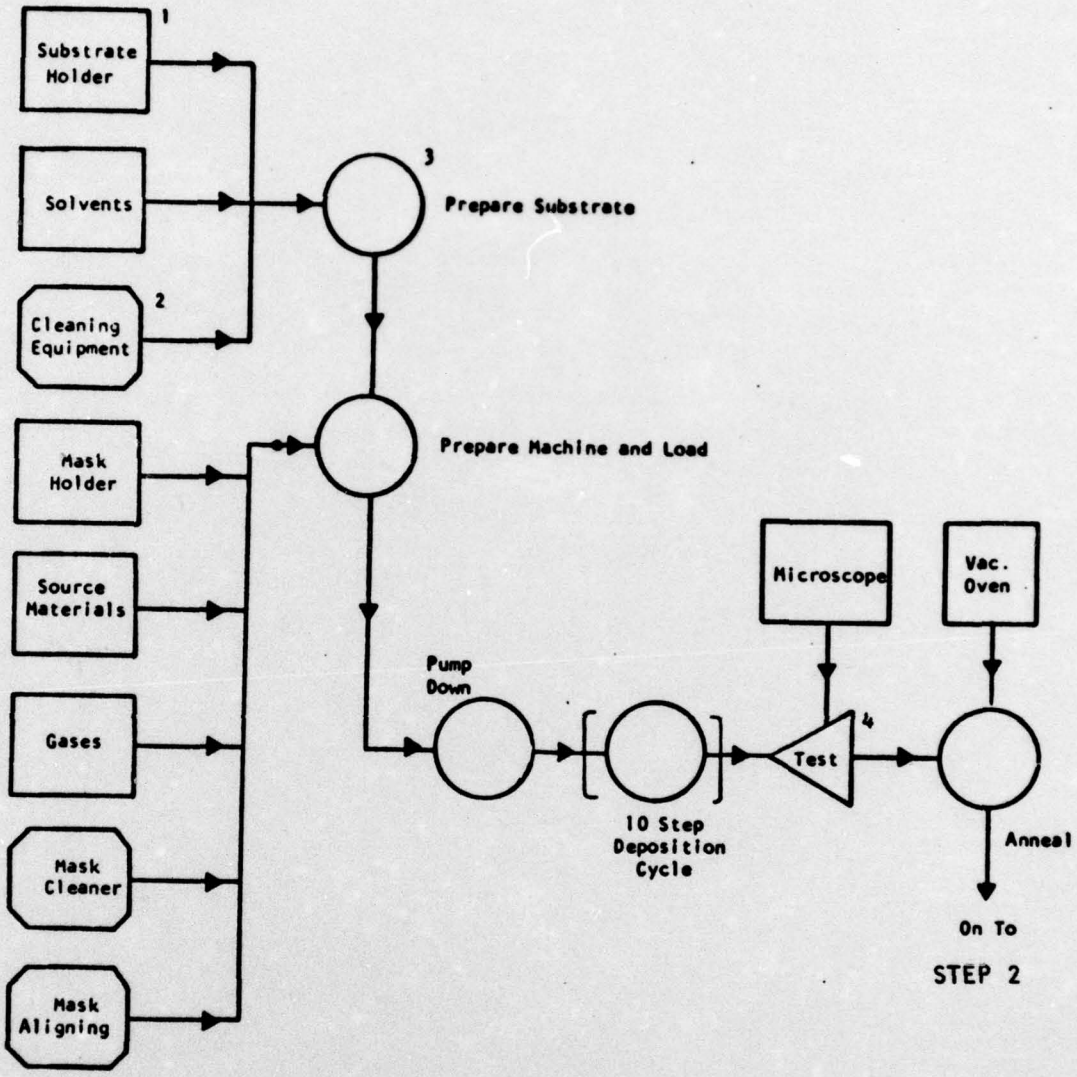
"Surface of Amorphous Semiconductors and Their Contacts with Metals," Ph.D. thesis, to be published in Physical Review.

8. GLOSSARY

Dedicated Masks	- A set of metal aperture masks (usually 12) each with a segment of the overall thin film pattern. One mask is equivalent to one evaporation step.
X-Y Masks	- A pair of contacting masks that are moved over each other to generate a complete set of thin film patterns. The one mask pair is used for all of the evaporation steps.
Packaging Process	- This term is used to summarize all the steps that are needed to take the complete thin film film transistor circuit through to a complete display. It includes laminar photoresist (RISTON(R)), phosphor spray and seal of the top plate.
RISTON(R)	- This is a Dupont trade-name for their laminar (sheet) photoresist. We use the term to cover the process of applying the material through a laminator, exposing and developing the pattern of phosphor apertures.
APPLICON(R)	- This is a trade-name (Applicon Co.) that is used to summarize the computer aided design (CAD) system. This interactive design tool is used for pattern layout and to generate magnetic tape to control the MANN photorepeater.
MANN(R) Photorepeater	- A commercial unit that generates exposed, patterned, photographic plates of ultra high quality. These plates are used to generate the metal masks.
Anneal	- A long, high temperature bake, given to the thin film circuits as part of their fabrication process.
TFT-EL Display	- A solid state flat panel display in which the electroluminescent (EL) display elements are controlled by an array of thin film transistors (TFT).

APPENDIX A

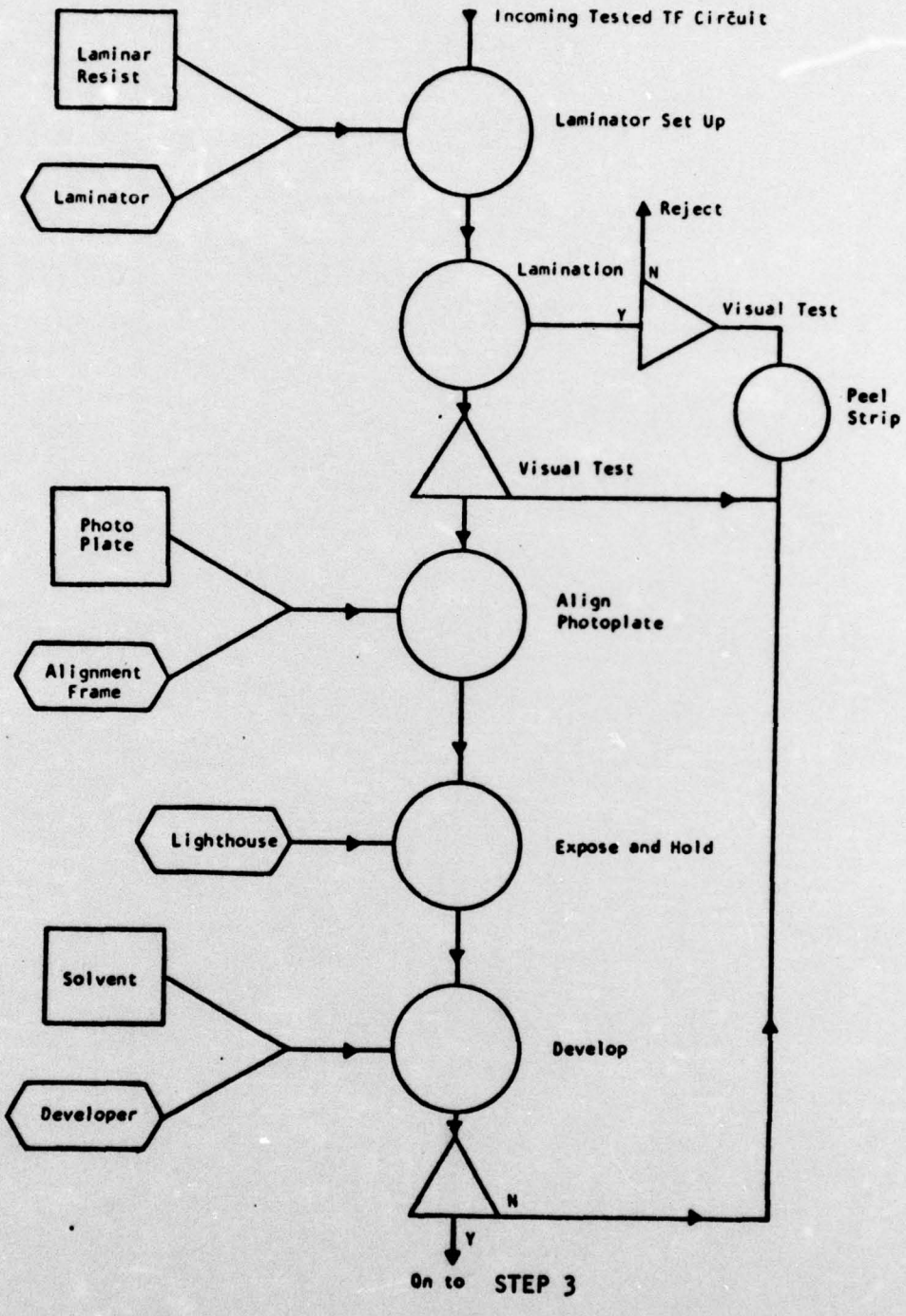
FLOW CHART OF MANUFACTURING PROCESS FOR TFT ADDRESSED DISPLAY



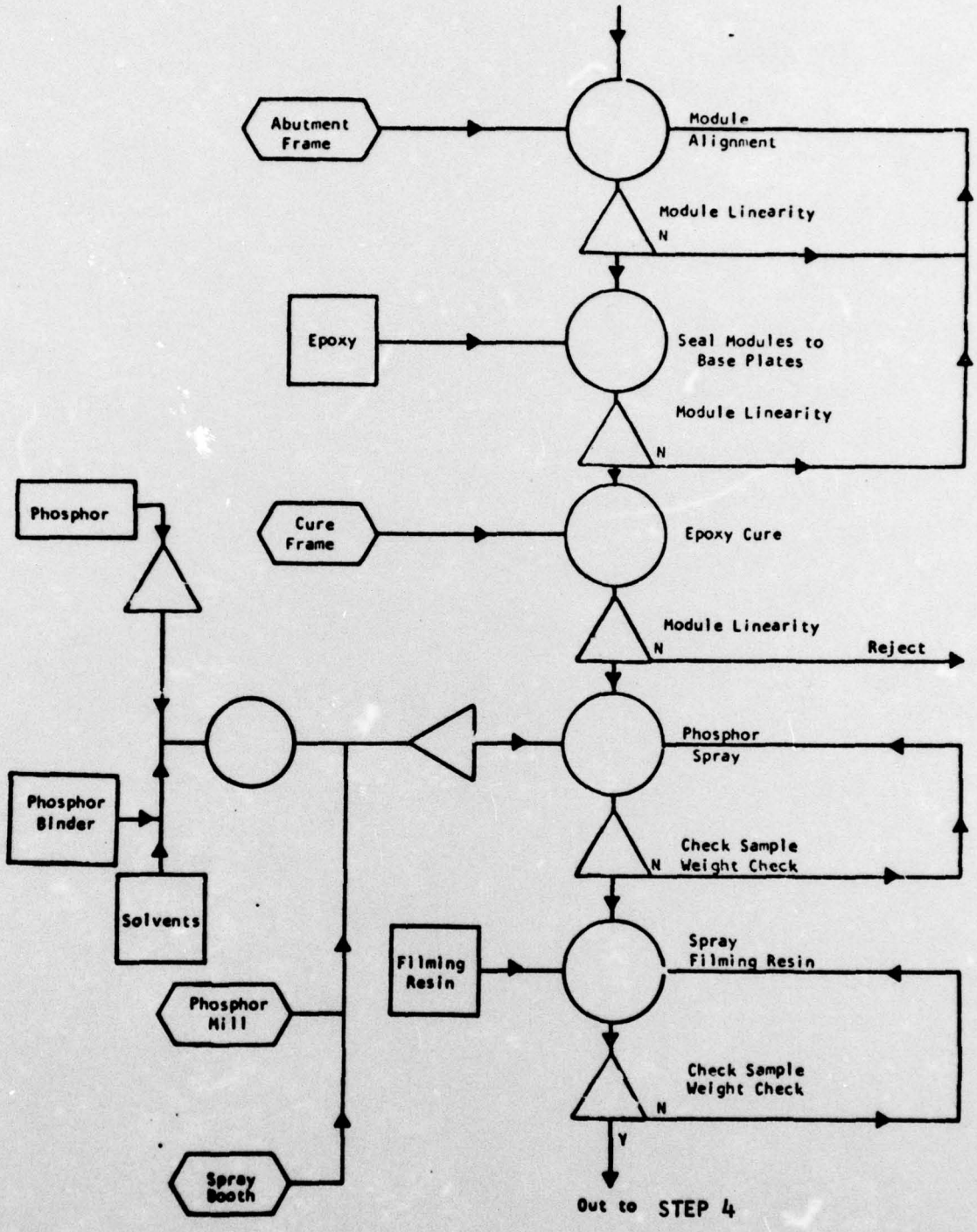
Symbol Indications:

1. Material
2. Equipment
3. Process Step
4. Test Position

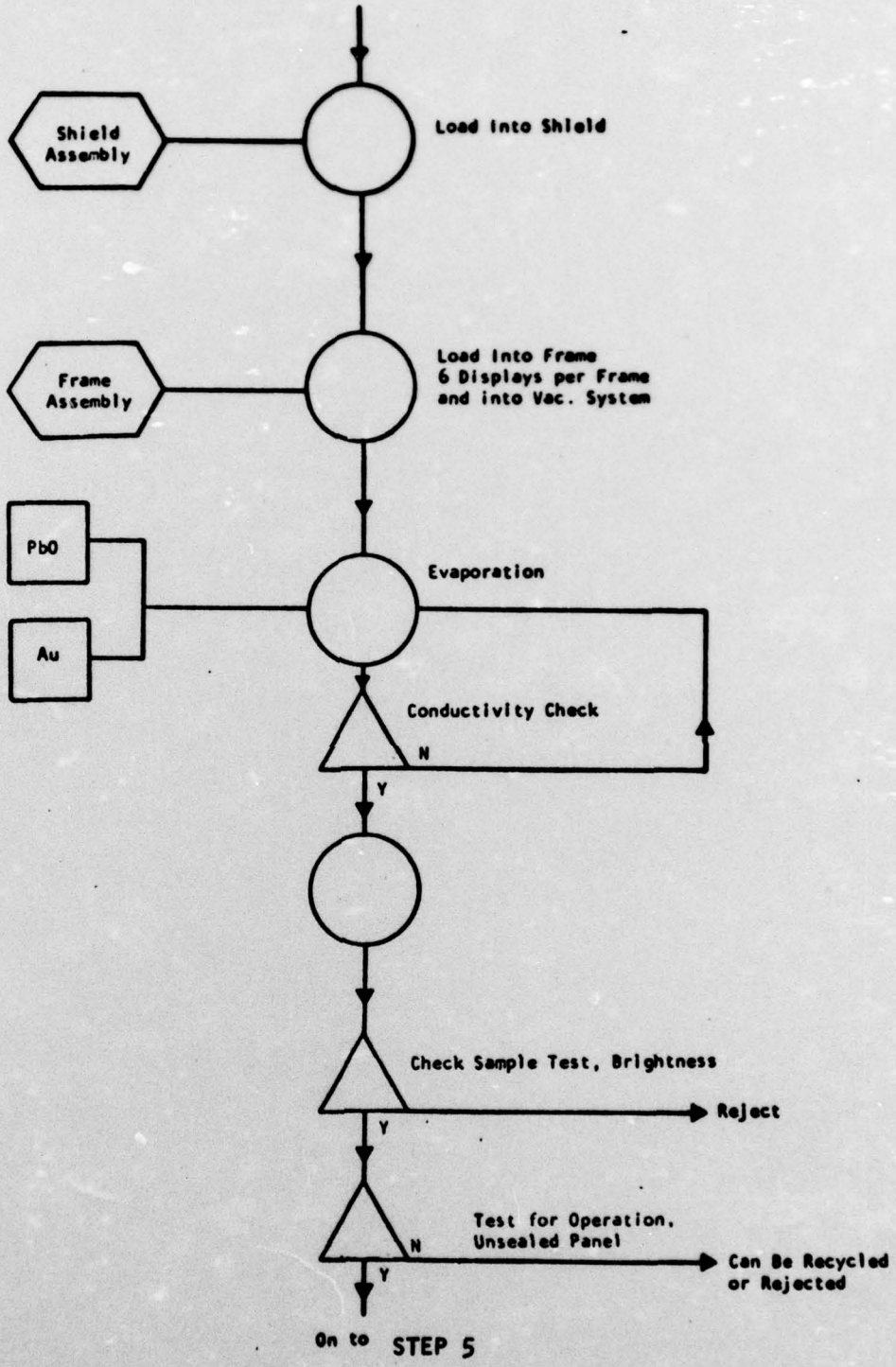
Step 1 - Thin Film Circuit Fabrication



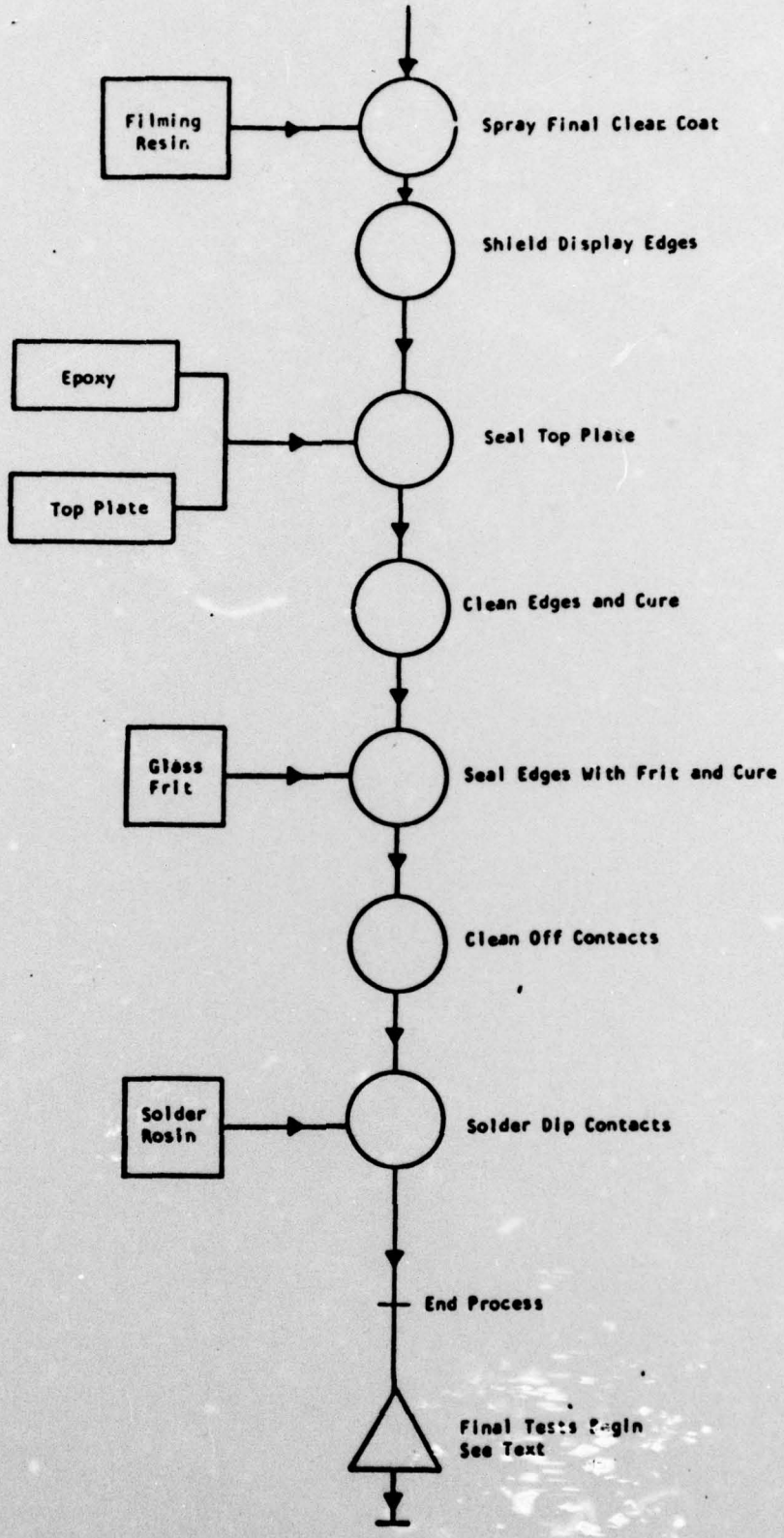
Step 2 - Thin Film Circuit Insulation



Step 3 - Phosphor Screening and Module Assembly



Step 4 - Top Electrode Deposition



Step 5 - Final Seal

APPENDIX B

ELECTRONICS COMMAND TECHNICAL REQUIREMENTS
THIN FILM TRANSISTOR ADDRESSED DISPLAY
(SCS-501; MAY 2, 1975)

ELECTRONICS COMMAND
TECHNICAL REQUIREMENTS

SCS-501
2 May 1975

THIN FILM TRANSISTOR ADDRESSED DISPLAY

1. SCOPE

1.1 This specification covers the detailed requirements for flat panel alphanumeric displays incorporating an electroluminescent light emitting medium, electrically addressed by an array of thin film transistors.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on the date of invitation for bids or request for proposal unless otherwise specified, form a part of this specification to the extent specified herein.

STANDARDS

MILITARY

MIL-STD-810B Environmental Test Methods

COMMERCIAL

ASCII Characters - American Standard Code for Information Interchange.

(Copies of standards and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the Contracting Officer).

3. REQUIREMENTS

3.1 Display Size. - The display shall consist of two 3.40" ±.05" x 3.55" ±.05" glass substrates containing the display elements, butted together and adhered to an approximate 2.90" x 6.60" glass cover sheet sized to overlap the display area. The display area on each substrate shall be a rectangle, 2.90" ±.05" by 3.30" ±.03" situated in such a manner that there shall be a minimum 0.25" border around a 2.90" ±.05" by 6.60" ±.06"actual display area when the two substrates are butted together. (See Fig. 1). An optional backing sheet is permissible.

3.2 Display Format. - The display shall contain 77 by 222 display elements. Each element shall be a rectangle, with the rectangles uniformly distributed in each dimension. The dimensions of each rectangular light emitting element shall be a minimum of .015" by .021". This results in the capability for 256 alphanumeric characters with a 5 by 7 dot configuration. The boundry between substrates shall not disturb this format.

3.3 Alphanumeric Characters. - Each of the 256 5 by 7 dot configurations shall be capable of displaying a full set of 128 ASCII characters.

3.4 Weight. - Display weight shall be a maximum of 5 oz.

3.5 Operational Characteristics. -

3.5.1 Electrical Input. - Signal and power input shall be accomplished by means of evaporated electrodes on the left and right sides and top or bottom of the display.

3.5.2 Display Recognition. - Display characters shall be viewable and recognizable in an ambient light intensity of 2000 foot candle (fc) impingent upon the display. In normal room lighting (50 fc impingent upon the display) the display contrast ratio, defined as the ratio of the luminance of an "on" light emitting element in darkness, to the luminance of a neighboring "off" element or neighboring dark space (whichever is greater) should be 20 as a minimum. This shall be measured in accordance with the provisions of Paragraph 4.5.2.

3.5.3 Power Dissipation. - At the luminances set to satisfy 3.5.2 with all resolution elements "on", power dissipation in the display panel shall not exceed 2.0 watts. With full power supplied to the panel, and all elements "off", power dissipation shall not exceed 1.0 watts. Thus with all 256 characters "on" total power dissipation in the display will be less than 1.5 watt. This shall be measured in accordance with the provisions of Paragraph 4.5.3.

3.5.4 Electrical Drive. - The side and bottom electrodes represent x-y addressing of any of the 77 by 222 or 17,094 resolution elements. Each resolution element shall contain two thin film transistors and one storage capacitor to provide the x-y function, to provide the electroluminescent drive, and to provide short term storage. The display shall be capable of presenting all 256 characters at a repetition rate as low as 30 frames per second.

3.6 Operating Temperature. - The display shall be capable of operation over an ambient temperature range of -45°C to 72°C without degradation of operational characteristics of 3.5 (See 4.5.4).

3.7 Operating Humidity. - The display shall be capable of operation at a relative humidity of up to 95% without degradation of operational characteristics of 3.5 (See 4.5.5).

3.8 Operating Altitude. - The display shall be capable of operation at an altitude of 30,000 feet and storage at an altitude of 50,000 feet without degradatio of operational characteristics of 3.5 (See 4.5.6).

3.9 Shock. - The display shall withstand shock when tested in accordance with Paragraph 4.5.7. The display shall not chip, crack or shatter as a result of the drops.

3.10 Vibration. - The display shall withstand vibration when tested in accorda with Paragraph 4.5.8. The display shall be free of vibrational resonance below 55 H

3.11 Life Test. - Display shall meet all requirements of 3.5.2 after 600 hours life test as described in 4.5.9.

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. - The contractor is responsible for the performa of all inspections specified herein. The contractor may utilize his own facilities or a commercial laboratory acceptable to the government. Inspection records of the examin tions and tests shall be kept complete and available to the government as specified in the contract. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.2 Classification of inspection. - Inspection shall be classified as follows:

(a) First article inspection (does not include preparation for delivery) (See 4.

(b) Quality conformance inspection. (See 4.4).

3.6 Operating Temperature. - The display shall be capable of operation over an ambient temperature range of -45°C to 72°C without degradation of operational characteristics of 3.5 (See 4.5.4).

3.7 Operating Humidity. - The display shall be capable of operation at a relative humidity of up to 95% without degradation of operational characteristics of 3.5 (See 4.5.5).

3.8 Operating Altitude. - The display shall be capable of operation at an altitude of 30,000 feet and storage at an altitude of 50,000 feet without degradation of operational characteristics of 3.5 (See 4.5.6).

3.9 Shock. - The display shall withstand shock when tested in accordance with Paragraph 4.5.7. The display shall not chip, crack or shatter as a result of the drops.

3.10 Vibration. - The display shall withstand vibration when tested in accordance with Paragraph 4.5.8. The display shall be free of vibrational resonance below 55 Hz.

3.11 Life Test. - Display shall meet all requirements of 3.5.2 after 600 hours life test as described in 4.5.9.

4. QUALITY ASSURANCE PROVISIONS

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4.2 Classification of inspection. - Inspection shall be classified as follows:

(a) First article inspection (does not include preparation for delivery) (See 4.3).

(b) Quality conformance inspection. (See 4.4).

4.3 First Article inspection. - First article testing shall be as follows:

(a) Two displays shall be subjected to the tests of 4.5.1, 4.5.2 and 4.5.3.

(b) One of these displays shall be subjected to the tests of 4.5.4 thru 4.5.8

(c) Both displays shall then be subjected to the life test of 4.5.9.

4.3.1 Failures. - No failures are allowed in first article displays.

4.4 Quality conformance inspection. - This inspection shall be performed on 8 displays selected from the pilot production.

4.4.1 Group A inspection. - Group A inspection shall consist of the tests of 4.5.1, 4.5.2 and 4.5.3. All eight displays shall be subjected to Group A inspection. No failures are allowed.

4.4.2 Group B inspection. - 3 of the 8 samples which have been subjected to Group A inspection shall undergo life test in accordance with 4.5.9. One each of the remaining 5 samples shall be subjected to Temperature (4.5.4), Humidity (4.5.5), Altitude (4.5.6), Shock (4.5.7) and Vibration (4.5.8). No failures are allowed.

4.5 Methods of examination and test. - Methods of examination and test shall be as specified in 4.5.1 thru 4.5.9.

4.5.1 Visual and mechanical inspection. - Displays shall be inspected for conformance with Paragraphs 3.1, 3.2, 3.3, 3.4 and 3.5.4.

4.5.2 Display viewability.

4.5.2.1 Display characters shall be inspected for recognition in an ambient light intensity of 2000 foot candles (fc) impingent on the display. All of the 256 available 5x7 dot configurations shall be checked for at least 2 of the set of 128 ASCII characters so that all characters are viewed and all dot configurations are checked. (See 3.5.2). Recognition shall be measured by presenting the ASCII characters on the display to 6 objective subjects, with no vision deficiencies. The characters shall be displayed in a random manner and a score of correct readings made. A maximum error rate of 3% is acceptable.

4.5.2.2 One of the 256, 5x7 dot configurations shall be checked for all ASCII characters. (See 3.5.2).

4.5.2.3 In normal room lighting, 50 fc impingent upon the display, the display contrast ratio (defined as ratio of luminance of an "on" light emitting element in darkness to luminance of neighboring "off" element) shall be inspected at 9 positions equally spaced in the display. (See 3.5.2)

4.5.3 Power Dissipation test. - With all elements of the display turned on to satisfy 3.5.2 requirements, total power dissipated by the display shall be measured. With all elements off, and full power supplied to the display, power dissipation shall be measured. (See 3.5.3).

4.5.4 Operating Temperature. - Displays will be placed in a chamber and the temperature lowered to -45°C, +0°, -5°C. After temperature equilibrium is reached, the displays will be operated and power dissipation shall be measured in accordance with 4.5.3. Following this, the displays will be returned to 25°C ± 3°C and allowed to reach temperature equilibrium after which the test of 4.5.2 will be run. The displays will then be brought to 72°C +5,° -0°C and allowed to reach equilibrium after which power dissipation will be measured in accordance with 4.5.3. Following this measurement, the displays will be returned to 25° ±3°C and allowed to reach equilibrium after which they shall be subjected to the tests of 4.5.2. Power shall be off during change from one temperature to another. (See 3.6).

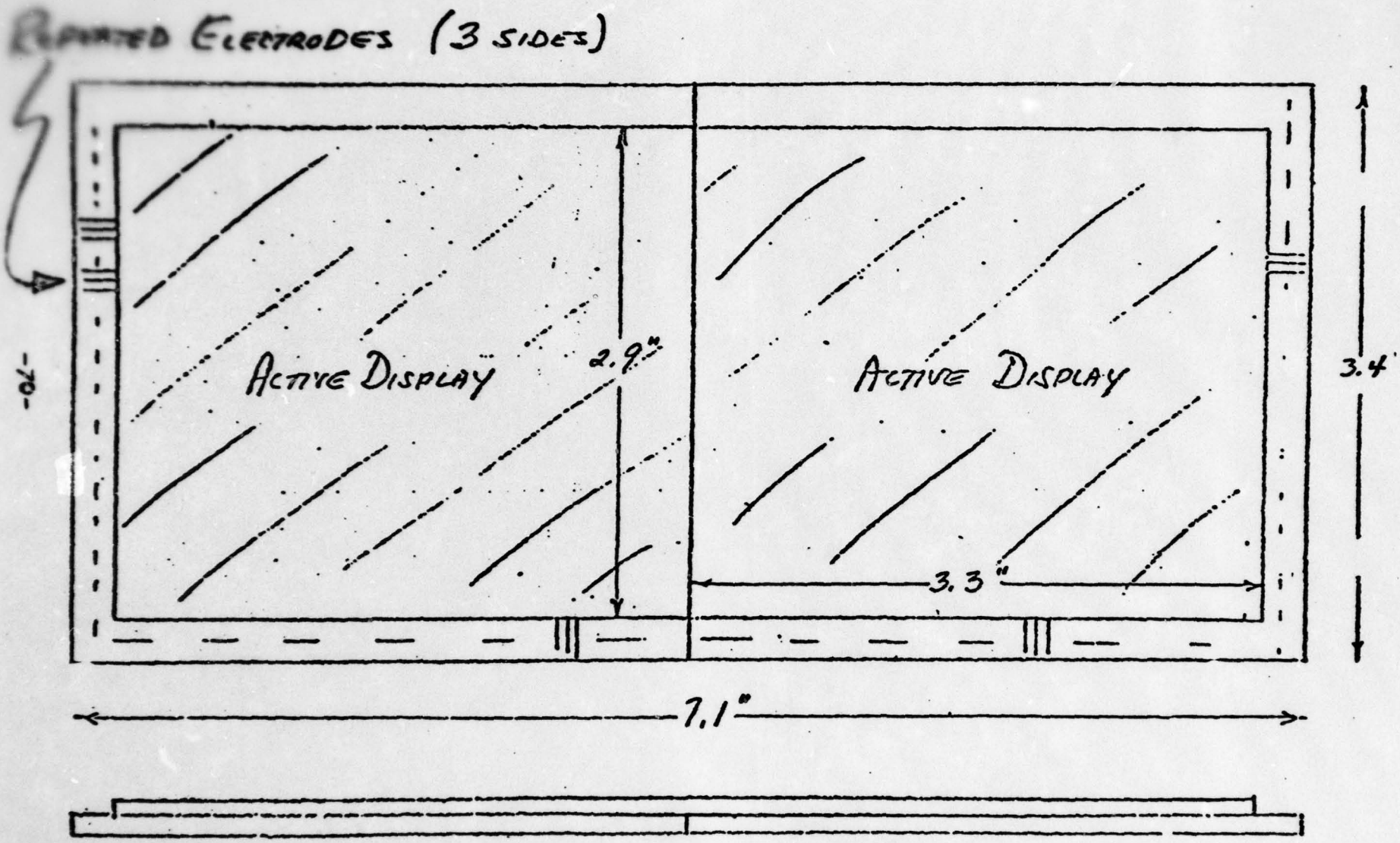
4.5.5 Humidity. - Displays shall be maintained at 40°C ± 2°C and a relative humidity of 90-95% for 96 hours. While still in the chamber power dissipation will be measured after which displays will be removed and tested in accordance with 4.5.2. (See 3.7).

4.5.6 Altitude. - Displays shall be brought to a pressure equivalent to 30,000 feet and maintained for 5 minutes after which the power dissipation shall be measured in accordance with 4.5.3. Following this, the displays shall be turned off and the pressure lowered to simulate an altitude of 50,000 feet. The displays shall be maintained at this pressure for 5 minutes and then lowered to room ambient conditions at which pressure the displays shall be subjected to the tests of 4.5.2 (See 3.8).

4.5.7 Shock. - The displays shall be subjected to the test of Method 516.2, procedure V of MIL-STD-810B. (See 3.9).

4.5.8 Vibration. - The displays shall be subjected to the test of Method 514.1 procedure XI of MIL-STD-810B. (See 3.10).

4.5.9 Steady state life. - Displays shall be operated in an ambient of 72°C +5°C -0°C for 600 hours. The displays will be cycled by turning all elements "on" for 50 minutes of each hour and "off" for 10 minutes of each hour. Power dissipation shall be measured at least once each day. After the 600 hours has elapsed, displays will be tested in accordance with 4.5.2. (See 3.11).


RAISED ELECTRODES (3 SIDES)
ACTIVE DISPLAY
2.9"
ACTIVE DISPLAY
3.4"
3.3"
7.1"

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FILM
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