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RADC-TR-76-357
Final Technical Report
November 1976

INFRARED RESPONSE OF IMPURITY DOPED SILICON MOSFET's (IRFET's)

University of Arkansas
Department of Electrical Engineering

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Sponsored by Defense Advanced Research Projects Agency (DOD)
ARPA Order No. 2794

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
GRIFFISS AIR FORCE BASE, NEW YORK 13441

ARPA Order Number

2794

Program Code Number

61101E

Name of Contractor

Board of Trustees, Univ. of Ark. for University of Arkansas, Fayetteville

Effective Date of Contract

1 August 1974

Contract Number

F19628-75-C-0071

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Contract Expiration Date

31 July 1976

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This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

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Jacques E. Ludman

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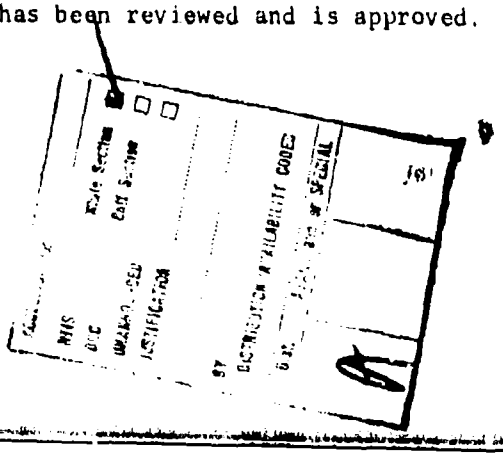

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: RADC-TR-76-357	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): INFRARED RESPONSE OF IMPURITY DOPED SILICON MOSFET'S (IRFET'S): Gold, Indium, and Gallium Doped and Applications	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Rept. 1 Aug 74 - 1 Aug 76
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Dr. Leonard Forbes, Dept. of Elect. Engineering University of California, Davis, California 95616 (Formerly at Univ. of Ark. until 76 JAN 06)	8. CONTRACT OR GRANT NUMBER(s): F19628-75-C-0071; ARPA Order -2794
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Board of Trustees University of Arkansas Fayetteville, Arkansas 72701	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 61101E 563801-01
11. CONTROLLING OFFICE NAME AND ADDRESS: Defense Advanced Research Projects Agency 1400 Wilson Blvd. Arlington, VA 22209	12. REPORT DATE: November 1976
	13. NUMBER OF PAGES: 163
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Deputy for Electronic Technology, RADC/ETSD, Hanscom AFB, MA 01731 Monitor/J.E.Ludman/ETSD	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; Distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

This research was sponsored by the Defense Advanced Research Projects Agency, ARPA Order No. 2794.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Extrinsic silicon infrared detectors.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Operation and characteristics of the impurity doped infrared sensing MOSFET (IRFET) are described. Responsivities of over 10^3 amps/joule have been observed with only small channel width to length ratios and large area devices. Much higher responsivities would be possible with smaller area devices.

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In the case of indium- and gallium-doped devices it has been shown that quantum efficiencies in the range 1.0 to 10.0% can be achieved by using substrates with low boron dopings.

The infrared sensing MOSFET (IRFET) is a detector, integrating element, and amplifier all combined in one device structure. As such it is distinctly different than other types of infrared detectors and possesses many very unique characteristics. When compared to CCD scanned photoconductors two of these are:

(i) the responsivity of the IRFET and uniformity of responsivity do not depend upon carrier life-time and residual impurity concentrations

(ii) the IRFET has a nondestructive D.C. or static memory type readout as opposed to the A.C. or dynamic memory type of CCD's.

This report describes in detail the experimental results obtained on gold-, indium-, and gallium-doped devices for use in the near, middle, and far infrared wavelength regions respectively. Equations describing the operation of the devices have been compared to the observed thermal and optical response characteristics. A good correspondence has been found in all cases. This allows an understanding of the design considerations involved in the MOSFET detector element itself.

An investigation of the noise characteristics of the detector has been presented and a description given of the considerations involved in the design and application of large scale arrays.

It is proposed that the IRFET might be particularly useful in some types of infrared imaging applications.

Apart from application of the MOSFET device structure as an infrared detector the experimental results have also demonstrated the usefulness of the device structure in characterizing impurity levels in silicon. The measurement of the thermal and optical emission characteristics of indium and gallium in silicon constitutes (to the author's best knowledge) the first direct observation of these quantities.

TECHNICAL REPORT SUMMARY

The infrared sensing MOSFET operates on the principle of an indirect observation of impurity charge states in the surface depletion region of the MOSFET device structure. Modulation of the charge state of the impurity center, either gold, indium or gallium, in the space charge region causes a change in the MOSFET threshold voltage and modulation of its conductivity. The device is an integrating detector and must be periodically reset by turning the MOSFET off by accumulating the surface. The device works much like a static or D.C. read only memory element. Low temperature operation, 100°K, 50°K, or 20°K respectively for each impurity is required to avoid thermal emission and ionization of the impurity centers. At low temperatures in a depletion region then, only optical emission or photoionization is possible as a means for the impurity centers to change charge state. This photoionization is then the basis for device operation.

In operation as an infrared detector, the device is first reset by accumulating the surface and filling all the impurity centers with holes and leaving them in the neutral charge state in the case of simple acceptor centers as indium and gallium. The MOSFET is then operated in the on conduction state by applying an inversion voltage to the gate. This inversion voltage and any back-gate or substrate bias forms a surface depletion region. If the neutral acceptor centers subsequently change charge states from neutral or negative the number of electrons or amount of negative charge in the inversion layer or channel must decrease, resulting in a lower conductivity.

The results presented describe the fabrication, operation and characterization of gold-, indium-, and gallium-doped devices. Not only was operation of the devices demonstrated, but it was also shown that the MOSFET device structure possesses some unique abilities in the characterization of impurity centers in

silicon. Specifically, measurements have been made of the thermal emission rates, thermal ionization energies, and field-enhanced thermal emission by the Poole-Frenkel effect for the gallium center.

The photoionization cross sections of gold, indium, and gallium in silicon, which determine the spectral response characteristics of the detector have been measured. A strong field enhancement has been observed in both the thermal and optical emission from the gallium center.

It has been found that optimum device performance can be achieved with substrates with low boron concentrations of the order $1x10^{13}$ to $1x10^{14}/cm^3$ and indium or gallium concentrations of the order $5x10^{16}/cm^3$. Such devices will give quantum efficiencies of the order 1.0 to 10.0% and responsivities in the range $1x10^4$ Amps/Joule for large area devices and $1x10^9$ Amps/Joule for small area devices.

A comparison has been made of the gallium doped MOSFET characteristics to results published for CCD scanned gallium doped photoconductors. While the quantum efficiency of the IRFET might be somewhat lower, on the other hand, it has a much higher responsivity and the theoretical signal to noise ratio under high flux conditions is at least comparable to, if not larger than, that for CCD scanned photoconductors. The optical responsivity and unformity of responsivity of the IRFET is distinctly different than the photoconductive detectors, in that the IRFET characteristics do not depend upon carrier lifetimes and concentrations of residual impurities in the wafers.

As a consequence of the unique characteristics, the infrared sensing MOSFET (IRFET) might be particularly useful in some large scale integrated infrared imaging array applications.

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*Based on material which has been previously published or submitted for publication in the IEEE Trans. on Electron Devices, the 1974 and 1975 International Electron Device Meetings, and 2nd International Conference on Solid-State Devices. See footnotes and publication list in Appendix E.

**Based on material in a proposal which has been submitted to DARPA by L. Forbes at the Univ. of Calif. at Davis and Hughes Research Laboratories, Malibu, Calif.

THE INFRARED SENSING MOSFET (IRFET)

I. INTRODUCTION

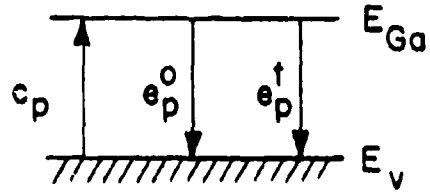
DEVICE DESIGN*

A design is described for an infrared sensing MOSFET (IRFET). This type of device has been designed for infrared imaging employing a read only memory (ROM) array where individual sense MOSFET's are employed at the intersections of the X-Y address lines. The X-Y selection is provided by decode circuits at the edge of the array [1]. The resistance of each IRFET in the array is measured by circuitry external to the array, and this information is then converted to a digital signal for processing, storage, or display.

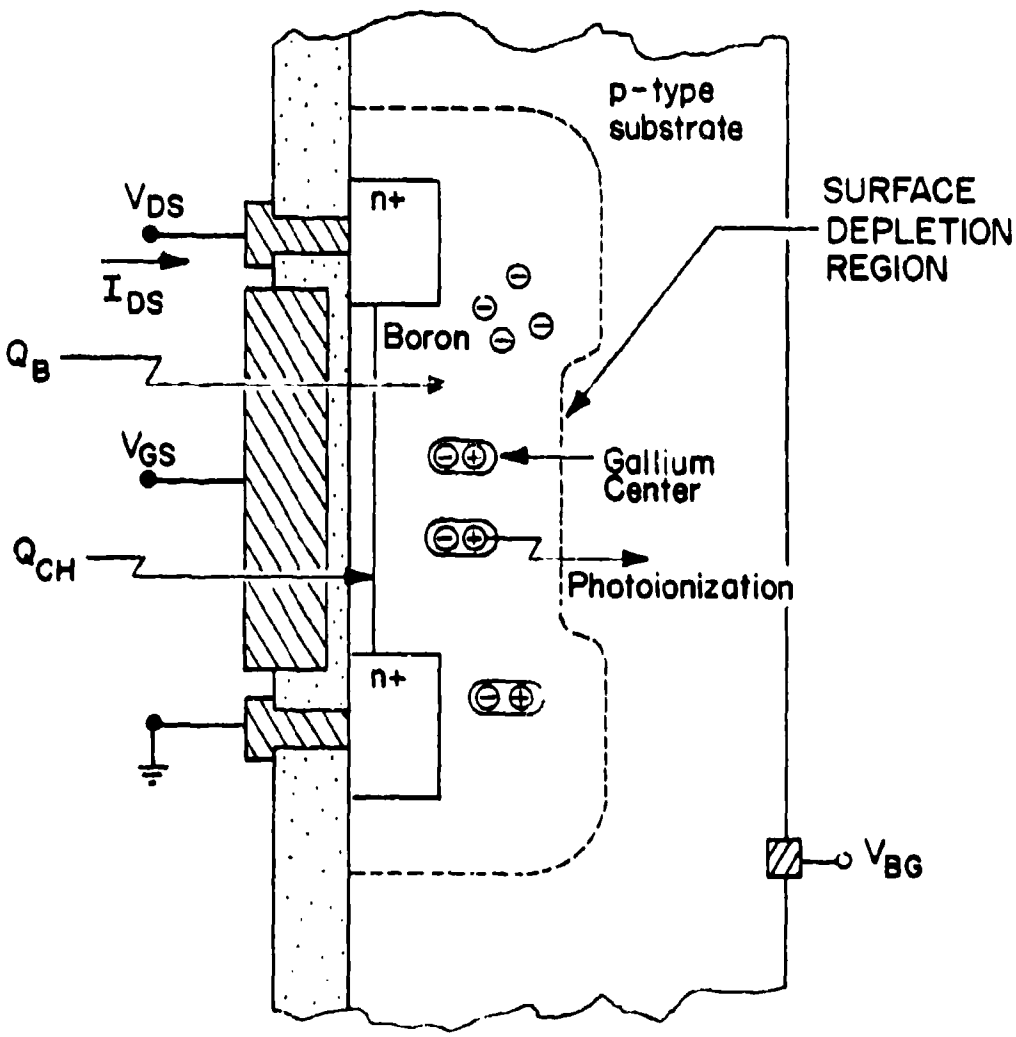
The IRFET is operated at low temperature and impurity photoionization [2], employed to modulate the conductance of each IRFET. An individual IRFET is shown in Fig. 1(b). In the example illustrated, n-channel devices are employed and the substrate is p-type. The p-type substrate is doped with both the shallow level acceptor, boron, and in this example, also by gallium, which has an acceptor level about 0.072 eV above the valence band. At the temperature of operation, $T \simeq 20^{\circ}K$, the relative dopings have been chosen such that the gallium acceptor centers are not ionized [3].

If the MOSFET has been originally preset by turning it off and accumulating the surface, then when the gate voltage V_{GG} is applied, the gallium impurity centers in the surface space charge or depletion region will not be ionized at low temperature [3]. However, the conductance of the MOSFET is a function of the number of ionized impurity centers in the space-charge region since the

*Based on material which has been published in the IEEE Trans. on Electron Devices, Aug. 1974, pp. 459-462, L.Forbes and J.R. Yeargan.



(A)



(B)

Fig. 1. (a) Capture and emission at an impurity center. (b) The Infrared sensing MOSFET(IRFET).

threshold voltage is a function of this space charge [4],[5]. If infrared radiation $8 < \lambda < 14\ \mu$, illuminates the array, then the gallium centers in the space-charge region can be photoionized by the emission of a hole to the valence band [3].

Photoionization of the gallium impurity centers in the space-charge region will change the space charge and modulate the resistance of the IRFET. The advantage of this technique for infrared imaging is the large-scale integrated ROM arrays can be constructed with silicon technology. This is an integrating type imaging array; each device integrates a fraction of the total number of photons incident before the resistance of the IRFET is sampled by the location being addressed.

The basic physical mechanism employed by the IRFET is impurity photoionization. Fig. 1(a) shows the important processes for an impurity center with an energy level near the valence band edge. Three processes are demonstrated: e_p^0 is the optical emission; e_p is the thermal emission; and c_p is the hole capture [6]. Capture, c_p, is important only during the reset operation of the device. At all other times, the impurity centers of interest are in a depletion region and there are no free holes present to be captured [3].

The optical emission, e_p^0, and the thermal emission, e_p, are competitive processes; the thermal emission rate, e_p, is, however, an extremely strong function of temperature [7]. The energy level of some impurity centers of interest in silicon are shown in Fig. 2. In this application, it would probably be most convenient to use p-type substrates because of the convenient placement of impurity energy levels with respect to the valence band. For the gold donor level, the thermal emission rate is very small or the level is stable at the temperature $T \approx 110$ K [7], and for indium and gallium, the levels

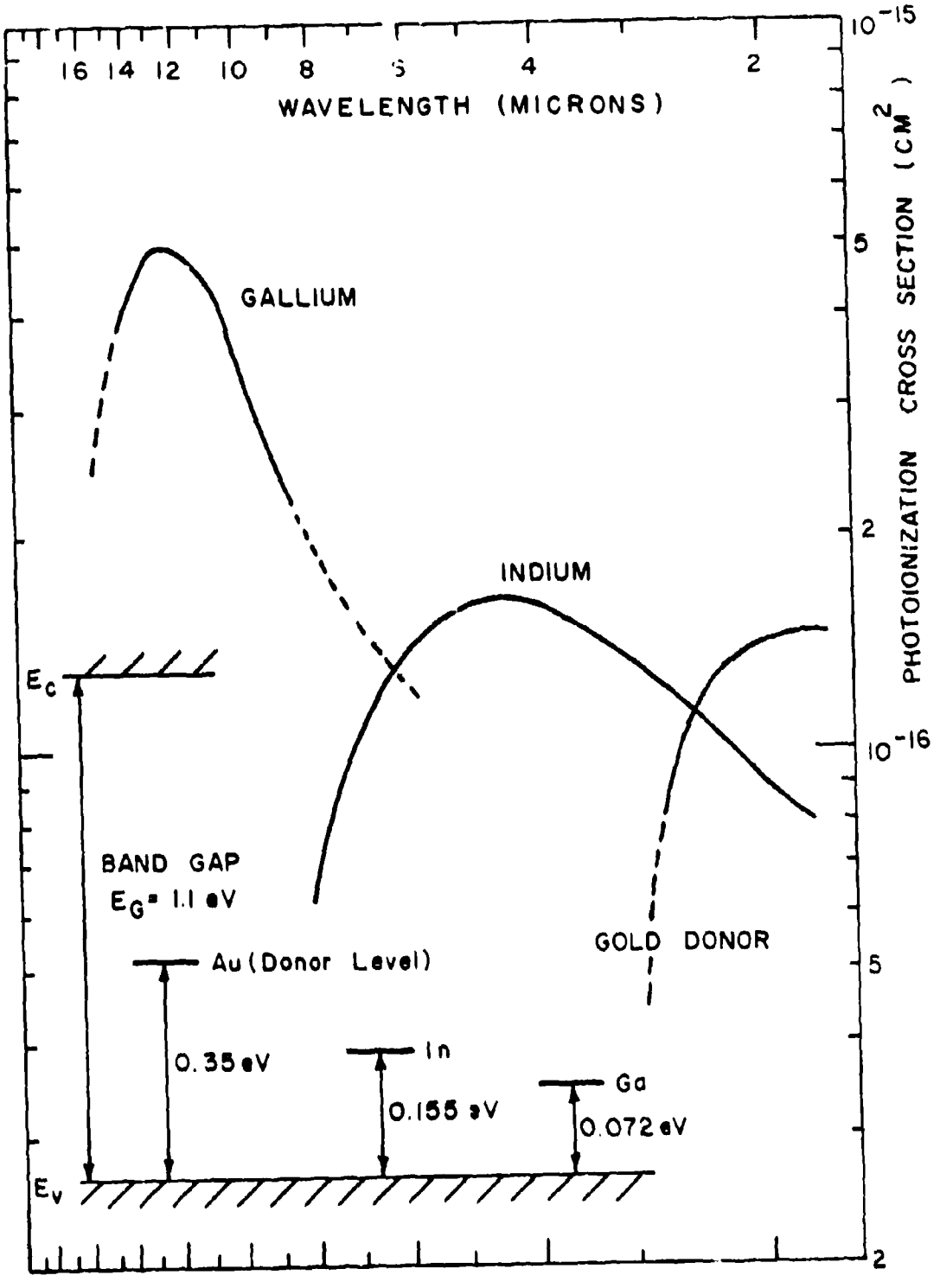


Fig. 2. Photoionization cross section of selected impurities in silicon; the results for gallium and indium have been taken from Bebb and Chapman, ref. [2], those for the gold donor are from Forbes, ref. [8].

should be stable at 50 and 20 K, respectively. In the IRFET, the temperature must be low enough to effectively eliminate thermal emission. The only means available for the impurity center to change charge state is then photoionization.

Fig. 2 shows the photoionization cross sections, $\sigma^0(\hbar\omega)$, of the three selected impurity centers in silicon. The data for gallium and indium have been taken from Bebb and Chapman [2], while the data for the gold donor level is taken from results obtained by the author [8]. Each of these impurities are most useful over different portions of the infrared spectrum.

DEVICE EQUATIONS

The basic equations describing MOSFET operation in the saturation region are: [1, 4, 5]

$$I_{DS} = (\mu C_o)(W/L)(V_{GS} - V_T)^2/2 \tag{1}$$

and

$$V_T = A + B(N_B)^{1/2} \tag{2}$$

where I_{DS} is the drain to source current, μ the effective surface mobility, C_o the oxide capacitance, W/L the channel width to length ratio, V_{GS} the gate to source voltage, V_T the threshold voltage, and A and B are parameters which depend upon the design and processing of the MOSFET, N_B is the number of ionized impurity centers in the surface space charge or depletion region. In the case of gold, indium and gallium doped devices operated at low temperatures, N_B can be time dependent and is the combination of the number of shallow level impurity centers, N_A, as for instance boron, and ionized deep level centers;

$$N_B = N_A + N_I[1 - \exp(-t/\tau)] \tag{3}$$

where all of the deep level impurity centers, N_I, are neutral or not ionized at time t = 0 and subsequently become ionized by thermal emission of holes with time constant $\tau = 1/e_p^t$, where e_p^t is the thermal emission rate. [3,6]

There are three distinctly different experimental conditions which may exist depending upon the ratio of concentration of deep level impurities to shallow level impurities and depending upon the magnitude of the excess of gate voltage above threshold in comparison to the change in threshold voltage, ΔV_T, as the impurity centers change charge state.

Case 1. $N_I << N_A$ and $\Delta V_T << (V_{GS} - V_T)$

If $N_I << N_A$, then;

$$\Delta V_T(t) = V_T(t) - V_T^i \text{ , where } V_T^i = V_T(0) \tag{4}$$

and

$$\Delta V_T(t) = B[N_I/(2N_A^{1/2})][1 - \exp(-t/\tau)] \tag{5}$$

where

$$\Delta V_T^{max} = B[N_I/(2N_A^{1/2})]. \tag{6}$$

If

$$\Delta V_T << (V_{GS} - V_T), \tag{7}$$

then

$$I_{DS} = (\mu C_o)(W/L)(V_{GS} - V_T^i)\,[1 - 2\Delta V_T(t)]/2 \tag{8}$$

and if the change in drain to source current is defined as,

$$\Delta I_{DS}(t) = I_{DS}(t) - I_{DS}^f \tag{9}$$

then;

$$\Delta I_{DS}(t) = (\mu C_o)(W/L)(V_{GS} - V_T^i)[\Delta V_T^{max} - \Delta V_T(t)] \tag{10}$$

and

$$\Delta I_{DS}(t) = \beta(V_{GS} - V_T^i)\Delta V_T^{max} \exp(-t/\tau) \tag{11}$$

where

$$\beta = (\mu C_o)(W/L) \tag{12}$$

and the change in drain current follows a simple exponential time dependence. This corresponds to the case of gold-doped devices which will be discussed in more detail later. The change in threshold voltage and drain to source current have been illustrated in Fig. 3.

Case 2. $N_I >> N_A$

In the case of devices fabricated on substrates which are doped primarily with the deep level impurity, N_I, and the shallow level impurity concentration is low, $N_A << N_I$, two approaches are possible. The first approach is to deal directly with the problem at hand and obtain an exact, if somewhat inconvenient, expression for the time dependence, and the second to approximate the time dependence by exponential decays. The indium-doped and gallium-doped devices employed are of the type $N_I >> N_A$.

If we let $U(t) = [I_{DS}(t)]^{1/2}$ then;

$$U(t) = (\beta/2)^{1/2}[V_{GS} - V_T(t)] \tag{13}$$

and

$$U(t) = (\beta/2)^{1/2}(V_{GS} - A - B[N_A + N_I(1 - \exp(-t/\tau))]^{1/2}) \tag{14}$$

and for times such that

$$N_I[1 - \exp(-t/\tau)] >> N_A \ , \tag{15}$$

and if

$$\Delta U^{max} = U(0) - U(\infty) = (I_{DS}^i)^{1/2} - (I_{DS}^f)^{1/2} \tag{16}$$

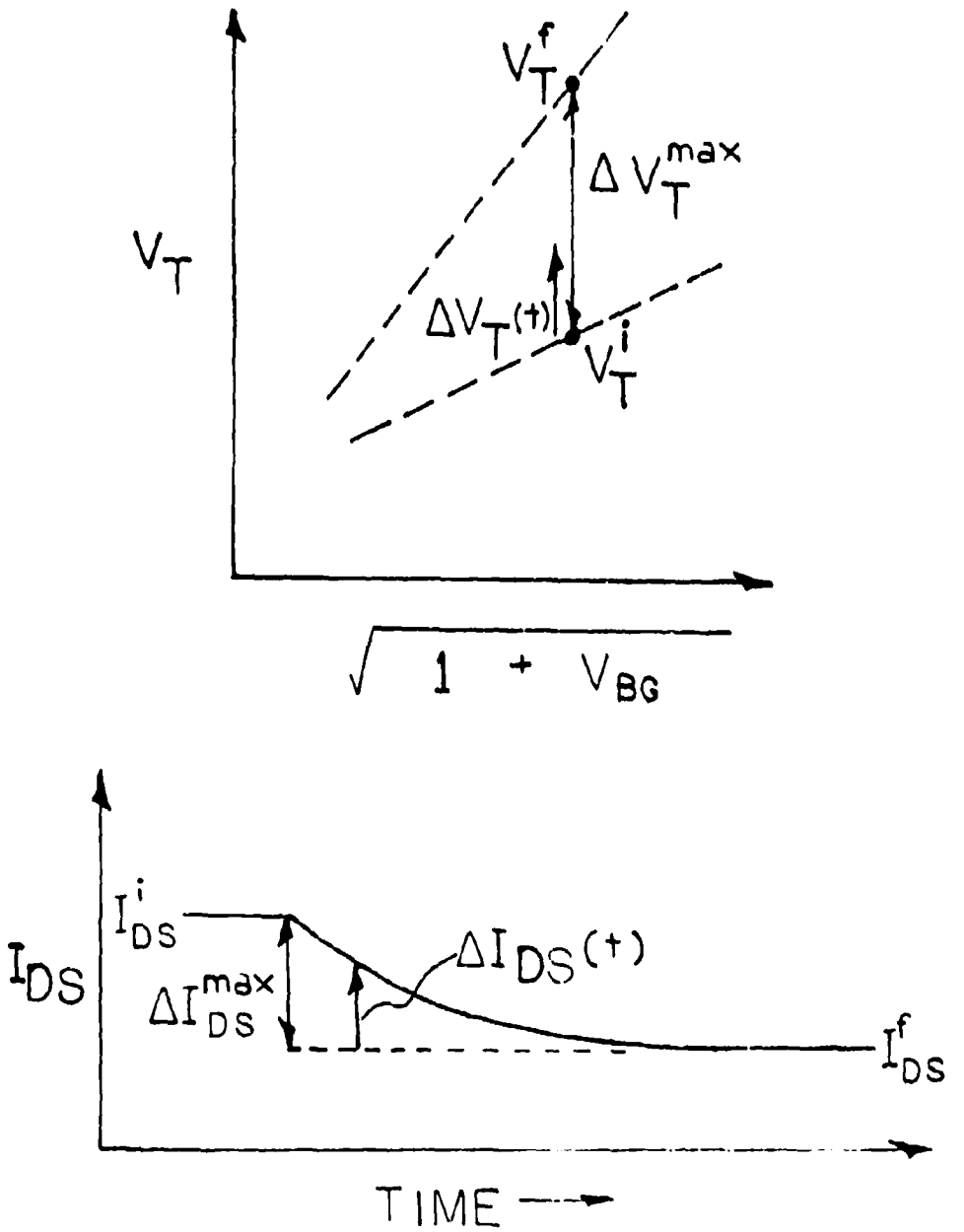


Fig.3. Illustration of the time dependent change in threshold voltage and drain to source current of the infrared sensing MOSFET.

then

$$\Delta U(t) = \Delta U^{max}[1 - (1 - \exp(-t/\tau))^{1/2}] \tag{17}$$

and

$$-t/\tau = \ln[1 - (1 - \Delta U(t)/\Delta U^{max})^2]. \tag{18}$$

This last expression can be used to determine the time constant, τ, associated with the change in impurity charge state by plotting on semilogarithmic paper. This technique has been used in the analysis of gallium doped devices.

Another approach is to look directly at the equation

$$I_{DS}(t) = \beta[V_{GS} - V_T^i - \Delta V_T(t)]^2/2 \tag{19}$$

where

$$\Delta V_T(t) = \beta(N_I)^{1/2}[1 - \exp(t/\tau)]^{1/2} \tag{20}$$

for times such that

$$N_I[1 - \exp(-t/\tau)] >> N_A \ . \tag{21}$$

Then

$$I_{DS}(t) = (\beta/2)(V_{GS} - V_T^i)^2[1 - (\Delta V_T^{max}/(V_{GS} - V_T^i))(1 - \exp(-t/\tau))^{1/2}]^2 \tag{22}$$

where

$$\Delta V_T^{max} = \beta(N_I)^{1/2} \tag{23}$$

and this can again be broken down into two limiting cases. It in the special case

$$\Delta V_T^{max} = (V_{GS} - V_T^i) \ ; \tag{24}$$

or in other words

$$I_{DS}^f = 0 \ , \tag{25}$$

then

$$\Delta I_{DS}(t) = I_{DS}(t) - I_{DS}^{f} = I_{DS}(t) \tag{26}$$

$$\Delta I_{DS}(t) = (\beta/2)(V_{GS} - V_T^i)^2(1 - [1 - \exp(-t/\tau)]^{1/2})^2 \ . \tag{27}$$

This last expression can be approximated by an exponential decay with a time constant of about one quarter of the time constant of the change in impurity change state, τ. If on the other hand

$$\Delta V_T << (V_{GS} - V_T) \ , \tag{28}$$

but still

$$N_I >> N_A \tag{29}$$

then

$$\Delta I_{DS}(t) = I_{DS}(t) - I_{DS}^{f} \tag{30}$$

$$\Delta I_{DS}(t) = (\beta/2)(V_{GS} - V_T^i)^2 \ (2\Delta V_T max / (V_{GS} - V_T^i))(1-(1-\exp(-t/\tau))^{1/2}) \tag{31}$$

and now the decay in the current is approximately exponential with a time constant one half that of τ.

Case 3. $\Delta V_T << (V_{GS} - V_T)$; but the doping may vary

In the situations where ΔV_T, the change in threshold voltage, is always small in comparison to the excess of gate voltage above threshold, then

$$\Delta I_{DS} = (\mu C_o)(W/L)(V_{GS} - V_T)(\Delta V_T) \tag{32}$$

and

$$\Delta V_T(t) = B(N_A + N_I)^{1/2}(1 - (1 - (N_I/(N_I + N_A))\exp(-t/\tau))^{1/2}) \tag{33}$$

then, if $N_I << N_A$, this just reduces to Case 1, where the decay in the current is exponential with time constant τ. If $N_I = N_A$, it is also found that the decay in current is very closely approximated by an exponential with time

constant τ, the same time constant as the change in impurity charge state.

For the case $N_I >> N_A$, it is found that the decay in current has a time constant one half that of τ, but just again like Case 2 where $N_I >> N_A$ and $\Delta V_T << (V_{GS} - V_T)$.

GOLD, INDIUM, AND GALLIUM DOPED DEVICES [8-30]

Because of the prior experience of the principal investigator with gold-doping of silicon [8], the initial work was conducted on gold-doped devices. The objective of this work was to demonstrate that the infrared sensing MOSFET would work in the manner described in the original proposal. In doing so, however, care was exercised not to overcompensate the substrate with gold which may cause the substrate to change conductivity type, or at least become nearly intrinsic and highly resistive even at room temperature. As a consequence the gold-doped devices are of the type $N_I << N_A$, or have an impurity or gold concentration, N_I less than the boron concentration, N_A. In this case the simple model discussed in the previous section applies.

Subsequently it was realised that much higher quantum efficiencies could be achieved in the case of indium and gallium doped devices by using substrates with low boron concentrations. This, however, results in a difference in the time constant between the decay of the impurity charge state and the time constant in the decay of drain current. In the case of indium doped devices a numerical solution was used to determine this difference as exactly as possible.

In the case of the gallium doped devices the approximate solutions presented in the previous section where employed and specifically $I_{DS}^{1/2}$ was plotted for devices where $N_I >> N_A$ to determine the time constant of the

change in gallium charge state.

Appendices, A, B, and C give a detailed treatment of each impurity. In the Appendices each impurity is being treated starting from a different view point. This treatment reflects the historical development of the work and reflects the realization about one half way through the project that many objections about low quantum efficiency might be overcome by using devices with $N_I >> N_A$. The price in doing so however is a considerable comp--lication in the device model and equations describing its operation.

In addition, the gold doping is considerably different than the indium and gallium doping. Indium and gallium are simple acceptors, no amount of indium and gallium doping will cause a boron doped wafer to become highly resistive at room temperature. Gold on the other hand is a double level impurity with both a deep acceptor and deep donor level. As a result gold doping will cause either p-type or n-type wafers to become highly resistive even at room temperature. As a result gold-doped devices must be of the type $N_I < N_A$ while indium and gallium doped devices should be of the type $N_I >> N_A$.

The particular technique used in the analysis of the experimental results is as follows:

(i) gold-doped; $N_I < N_A$, decays analyzed using eqn. (11). The change in drain current is a simple exponential time constant.

(i,) indium-doped; $N_I >> N_A$, this corresponds to Case. 2. on page 7. The data has been analyzed using numerical techniques to determine the relationship between the time constant of the change in indium charge state and

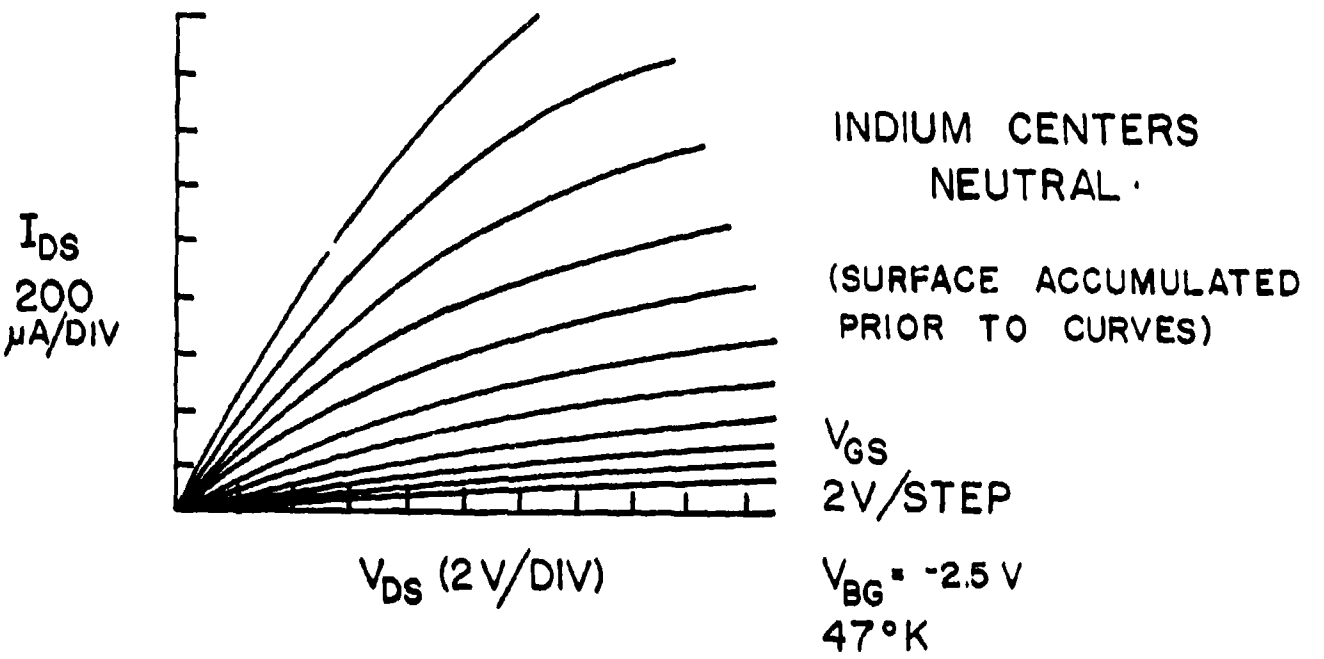
the time constant of the change in drain current. These results were checked using the approximations following eqn. (27) and (31).

(iii) gallium-doped; the work reported here is for devices where $N_I >> N_A$, and eqn. (17) was employed. These results were checked on devices which had $N_I < N_A$.

The techniques which have been employed then in each case are quite different. This section has covered all of these possibilities, the details relating to the each doping are covered in the Appendices on each impurity. Figure 4 shows the observed curve tracer characteristics for an indium-doped device under the two limiting cases where the indium in the surface space charge region is either neutral or negative. Obviously large changes in conductivity can result by the change in impurity charge state.

The next sections will summarize the utilization of these changes in characterizing impurity centers and in the fabrication and operation of infrared detectors.

INDIUM DOPED MOSFET



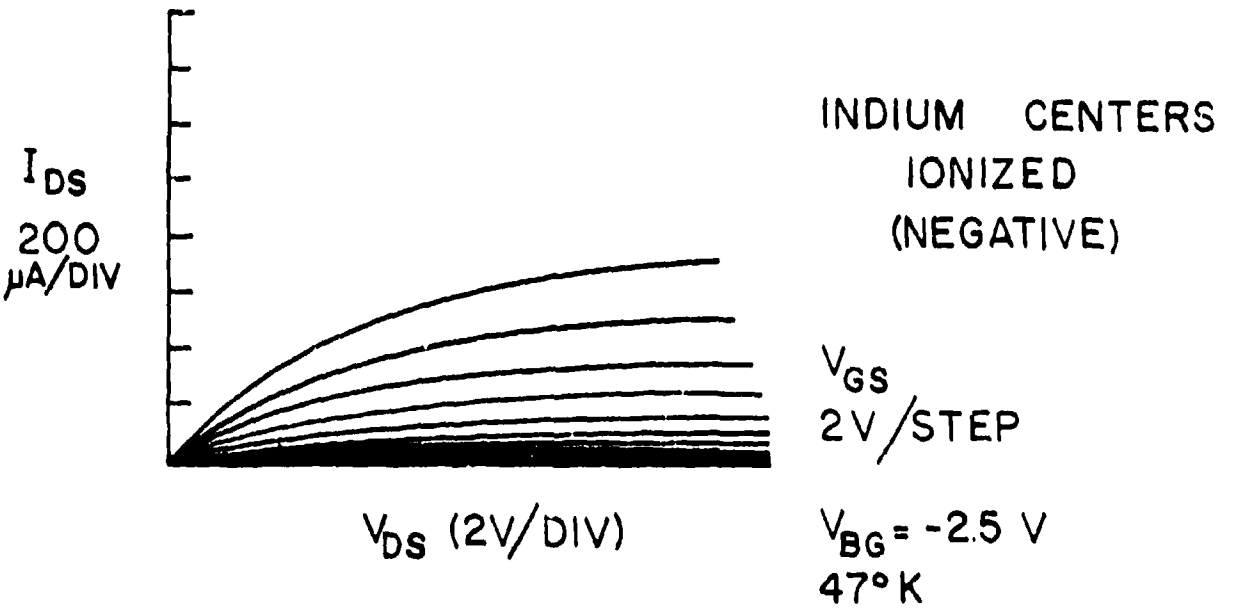


Fig. 4 Illustration of the two limiting conductivity states of an indium-doped MOSFET when the indium is neutral and then negative.

II. APPLICATION OF THE MOSFET DEVICE STRUCTURE IN CHARACTERIZING* IMPURITY CENTERS

Identification of impurity center concentrations, emission rates and capture coefficients using pulsed capacitance techniques on p-n junctions, Schottky barrier junctions, and MIS capacitors are low temperature measurements. As shown in Fig. 5 , these structures are two terminal devices which are in series with the substrate resistance. [3]

In the case of indium and gallium doped devices, the required temperatures of operation are in the range of 50°K to 20°K and a very significant deionization will occur in the substrate. This results in a very high series impedance, $R_{substrate}$, which makes pulsed high frequency capacitance measurements virtually impossible. While such capacitance measurements can be made on a double indium-boron doped substrate, in the case of gallium, however, even a double gallium-boron doped substrate will not work since even deionization of the boron becomes appreciable at the required temperatures of operation resulting in an excessive substrate impedance.

The MOSFET structure on the other hand is a 3 terminal measurement (exclusive of the gate) where the surface conductivity between source and drain is measured. The substrate contact serves only to establish the substrate potential and at low temperatures only an unmeasureably small leakage current is drawn through this substrate contact. As a consequence, measurements can still be easily made on the MOSFET structure when the substrate is deionized and high impedance (~ 1 megohm or more) since almost no potential drop occurs across the substrate. The MOSFET structure is thus ideally suited for measurements on single indium-doped or gallium-doped materials with only residual impurity dopings of shallow level acceptors or donors as boron or phosphorus, such as ones used in extrinsic silicon photoconductive detectors. In fact, the concentration of such residual impurities can be easily determined

*Based on material contained in a proposal submitted to ARPA by L.Forbes.

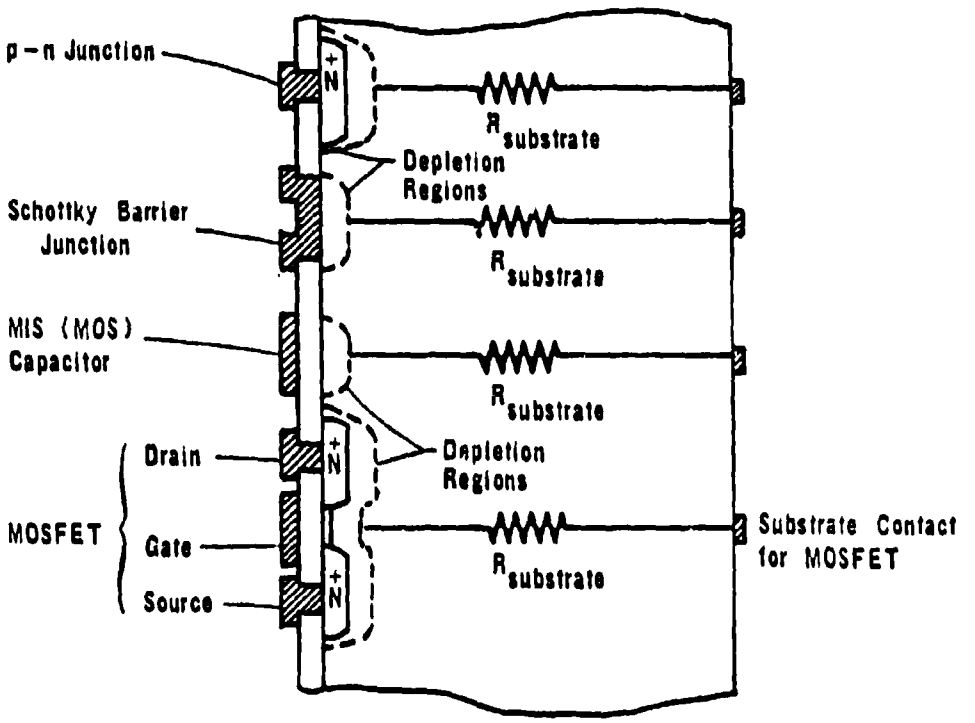


Figure 5 Devices Used for the Characterization of Impurities in Silicon; In the upper three, p-n junction, Schottky Barrier Junction, and MIS capacitor the capacitance of the device is in series with the substrate resistance which becomes much larger than the impedance of the depletion region capacitance at low temperatures on a deionized substrate, making capacitance measurements very difficult.

In the MOSFET structure essentially no current is drawn through the substrate resistance and substrate contact.

as will be discussed.

The results reviewed in this section were obtained on a single indium doped silicon substrate such as that which might well be employed in a extrinsic silicon photoconductive detector for the middle, 3 to 5 micrometer, infrared wavelength range. Specifically, results are shown for a characterization of the indium center in silicon and since these results have been treated to some extent in the literature, a detailed description will not be given. The last section describes the proposed technique which could be employed to determine the carrier capture coefficient or cross section of an impurity center using the MOSFET structure.

IMPURITY CONCENTRATIONS

Impurity concentrations are easily determined employing the MOSFET structure by measuring the dependence of threshold voltage on back-gate basis. Fig. 6 (from Appendix B) is an illustration of this technique on an indium doped substrate. This particular sample has an indium concentration of $8.92 \times 10^{15}/cm^3$ and a net residual shallow level acceptor concentration of $4.95 \times 10^{14}/cm^3$.

THERMAL EMISSION RATES

Fig. 7 and Appendix B show a determination of the thermal emission rate by measuring the temperature dependence of the time constant of

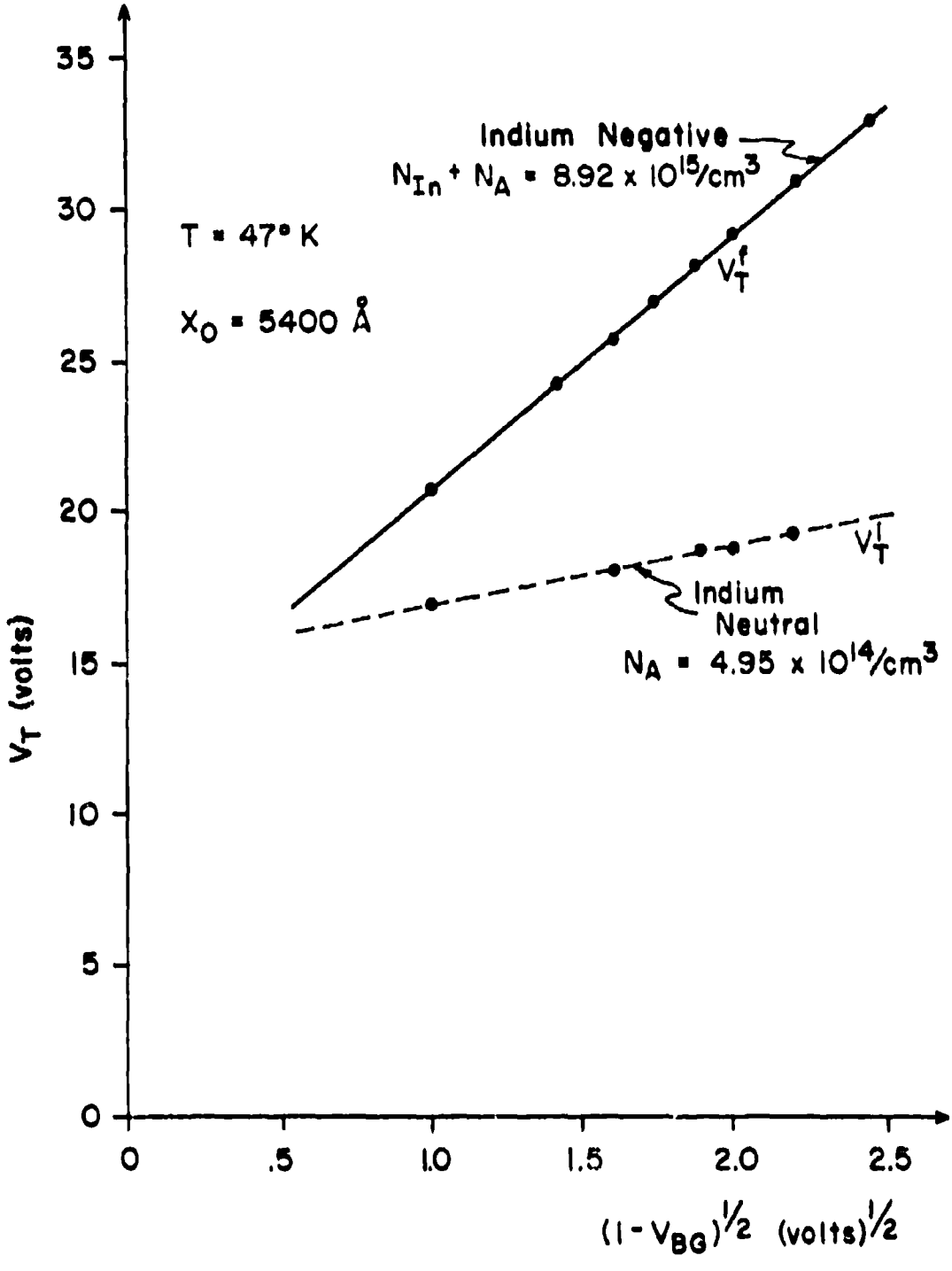


Fig. 6 Determination of the Indium Impurity Concentration.

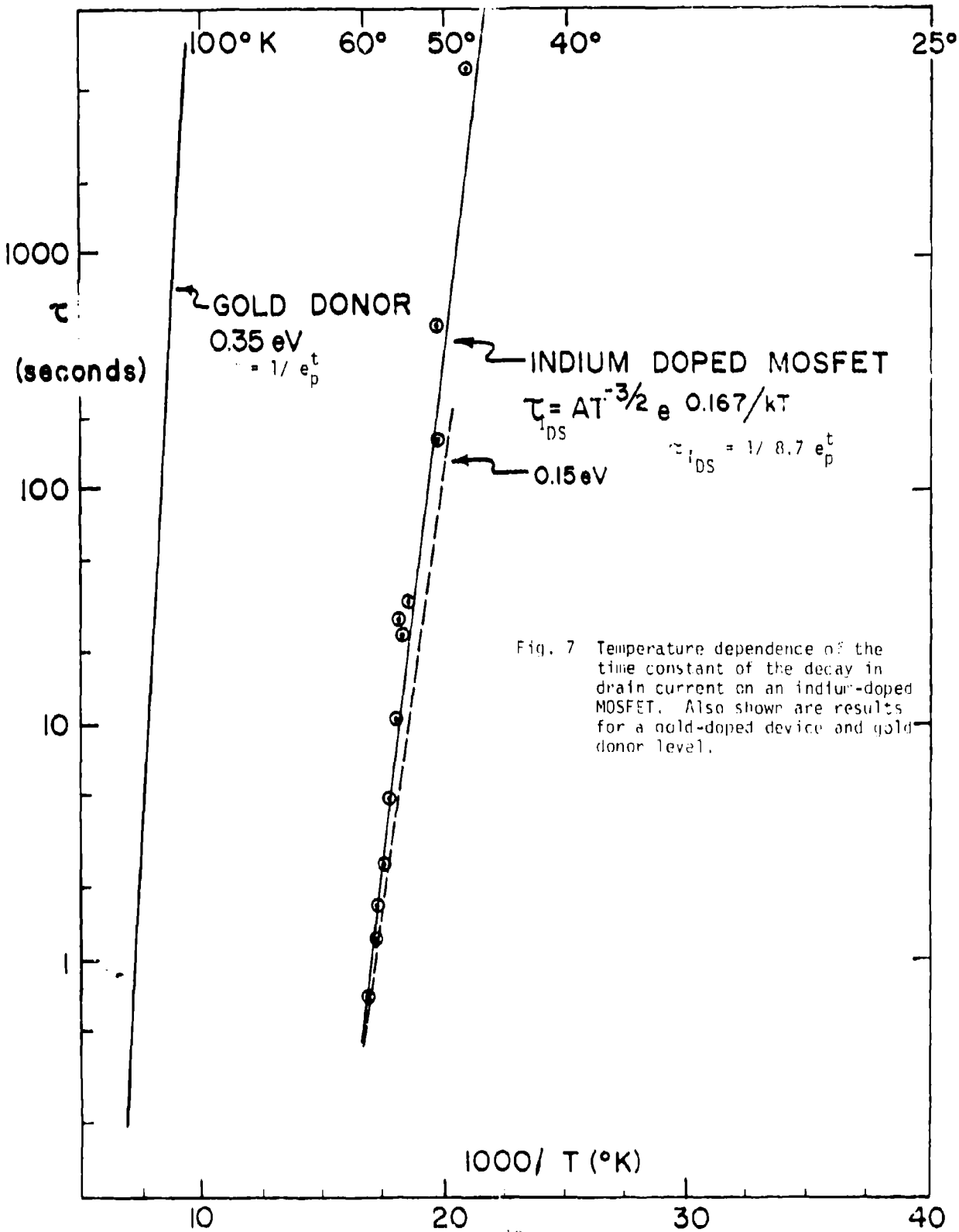


Fig. 7 Temperature dependence of the time constant of the decay in drain current on an indium-doped MOSFET. Also shown are results for a gold-doped device and gold donor level.

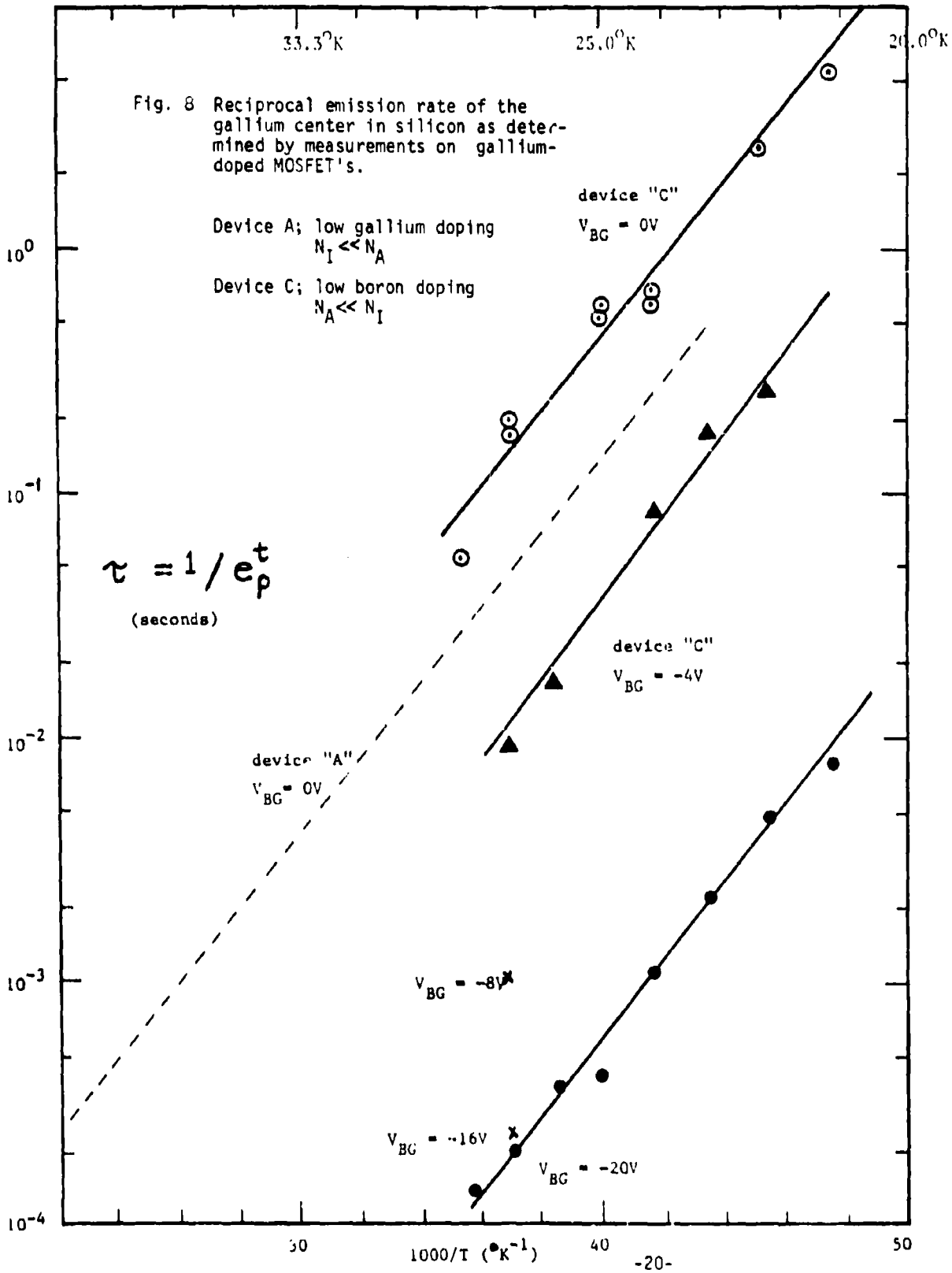


Fig. 8 Reciprocal emission rate of the gallium center in silicon as determined by measurements on gallium-doped MOSFET's.

the dark decay between the two limiting conductivity states. The slope of the line, 0.167eV, is appropriate to the thermal activation energy of the indium center in silicon and provides a unique determination and identification of the indium center. [2, 19-24]

The emission rate of shallow level centers determines the rate of ionization of the centers as a function of temperature in photoconductive detectors and in general have not been previously determined, although obviously very important.

This sample was very carefully checked for other levels, as for instance the 0.11eV level reported by Hughes in indium doped samples, however no such other levels were found in our samples. The MOSFET structure is particularly convenient for such measurements. Fig. 8 , and Appendix C show the results for gallium doped devices, or the thermal emission rate of gallium in silicon. The dependence on back gate bias is due to the Poole-Frenkel effect. [2,19-28]

PHOTOIONIZATION CROSS SECTIONS

The photoionization cross section of the indium center has been determined by measuring the time constant of the decay under illumination between the two limiting conductivity states of the MOSFET structure. These results are shown in Fig. 9 and in Appendix B. In making some of these measurements, we have employed a unique arrangement using a circularly variable filter and globar source. [2, 19-24]

Such measurements could also be readily extended to other impurity centers, such as the 0.11eV level reported by Hughes in their indium doped samples. Such measurements can provide an important optical verification, in addition to the thermal measurements, of these type of levels.

Fig. 10 and Appendix C give the results for the gallium impurity center. [2, 19-24].

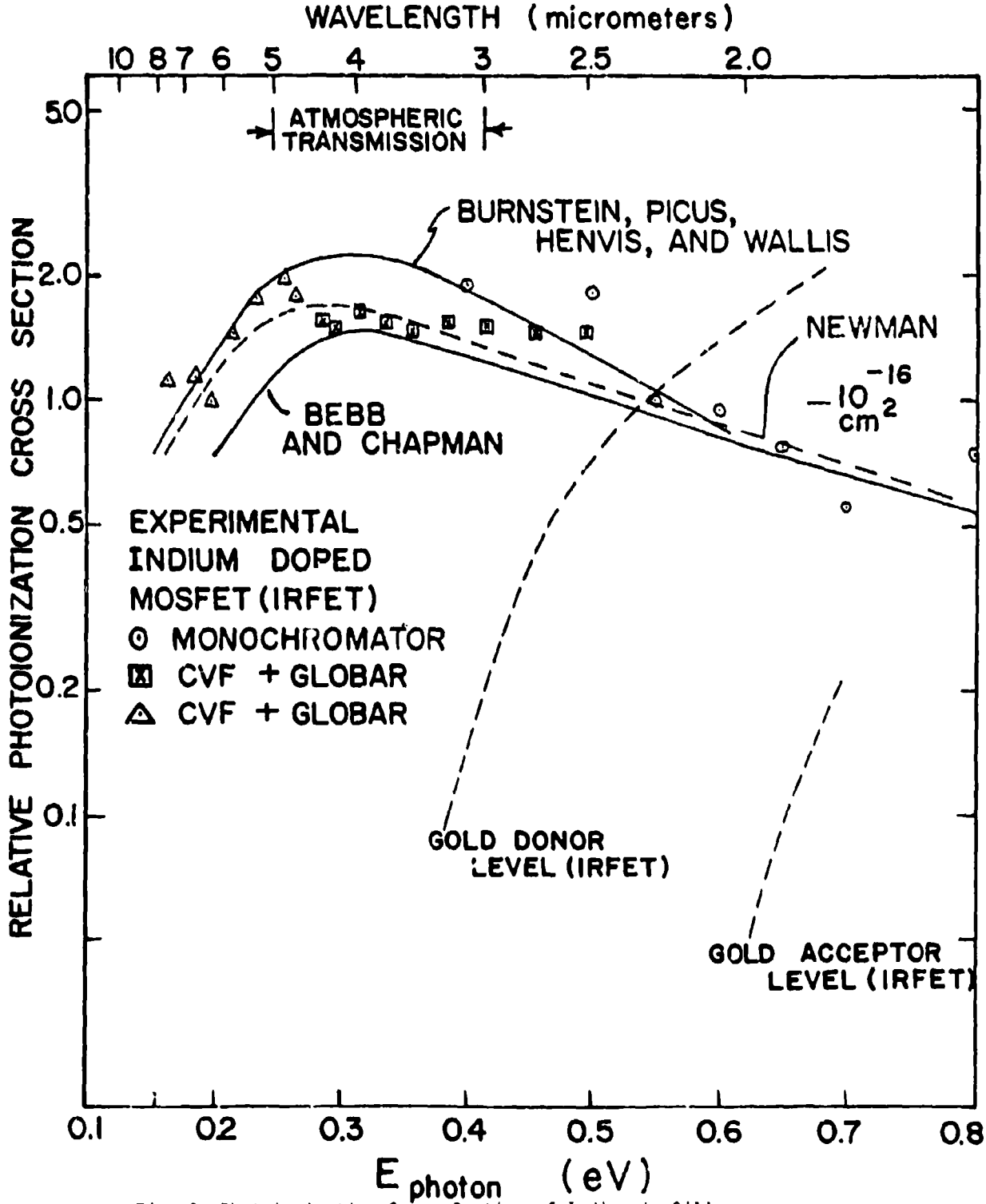


Fig. 9 Photoionization Cross Section of Indium in Silicon.

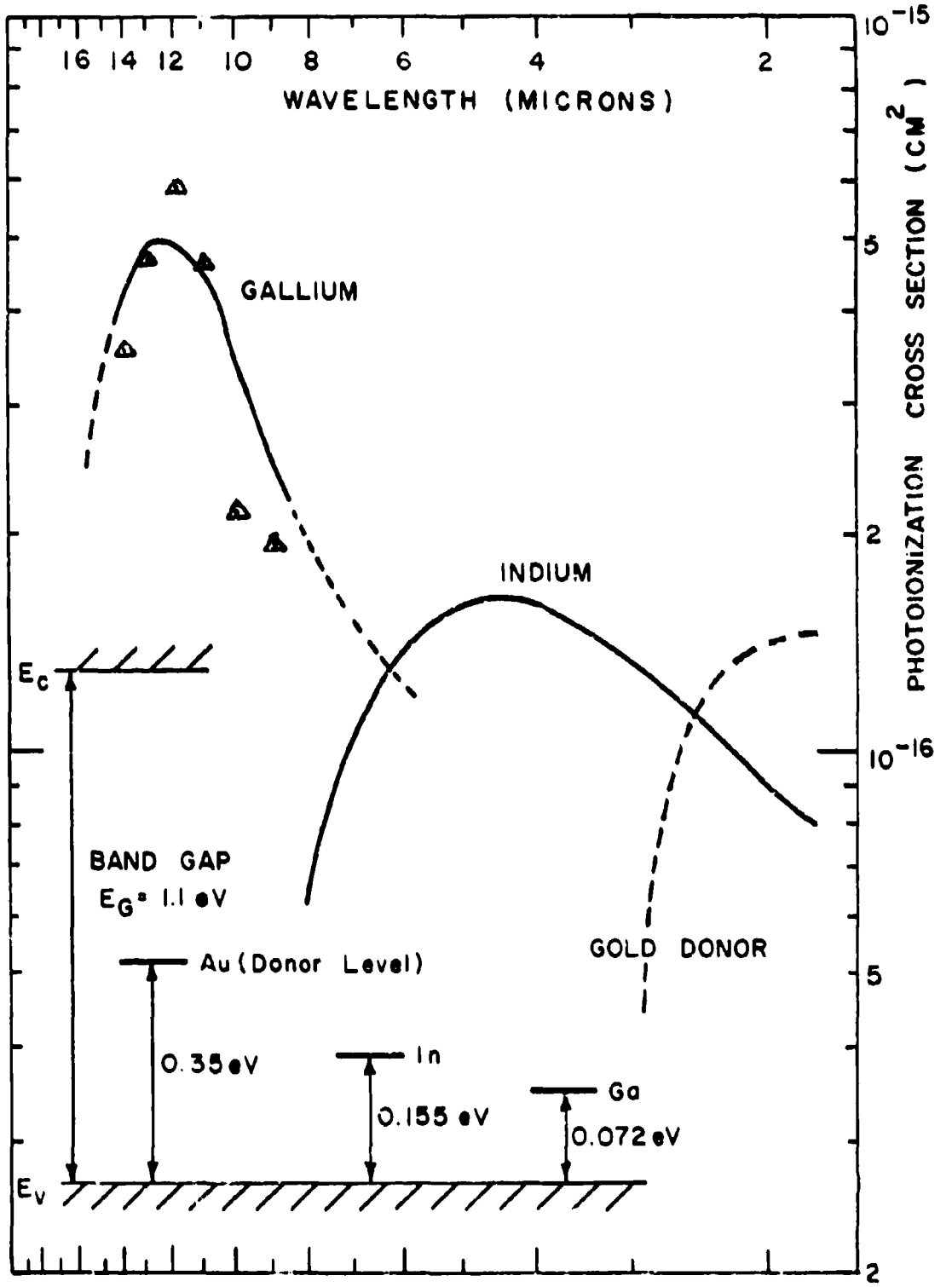


Fig. 10 Experimentally measured points for the Photoionization Cross Section of Gallium superimposed upon the curves of Fig. 2.

CARRIER CAPTURE CROSS SECTIONS

Capture cross sections and capture coefficients can be measured using the MOSFET structure by employing an extension of techniques used previously on p-n junction devices. These techniques can be employed to determine both the "small signal" capture coefficient or capture cross section when the carrier is nearly in thermal equilibrium with the lattice and the capture cross section when the carriers and impurity centers are under the influence of electric fields. Both situations are relevant to photoconductive detectors which operate over a range of applied voltage and electric field conditions. In addition relatively high field conditions may exist at the p^+ contacts formed on the photoconductor. [3]

Figure11 shows the proposed technique for the determination of the capture cross sections near equilibrium. The impurity centers in the MOSFET surface depletion region have been arranged to be in the negative charge state and the initial conductivity of the MOSFET, I_{DS}^{i} , is low. The surface is then accumulated for short periods of time attracting holes to the surface. If this accumulation time period is short then only a fraction of the negative impurity centers can capture holes;

$$t_{acc} = t_{accumulation} << 1/(c_p \cdot p) \tag{34}$$

and on each accumulation cycle

$$d(N_T)/dt = -c_p \, p \cdot N_T \tag{35}$$

and since $dt = t_{acc}$ then

$$dN_T/N_T = -c_p \, p \cdot t_{acc} \tag{36}$$

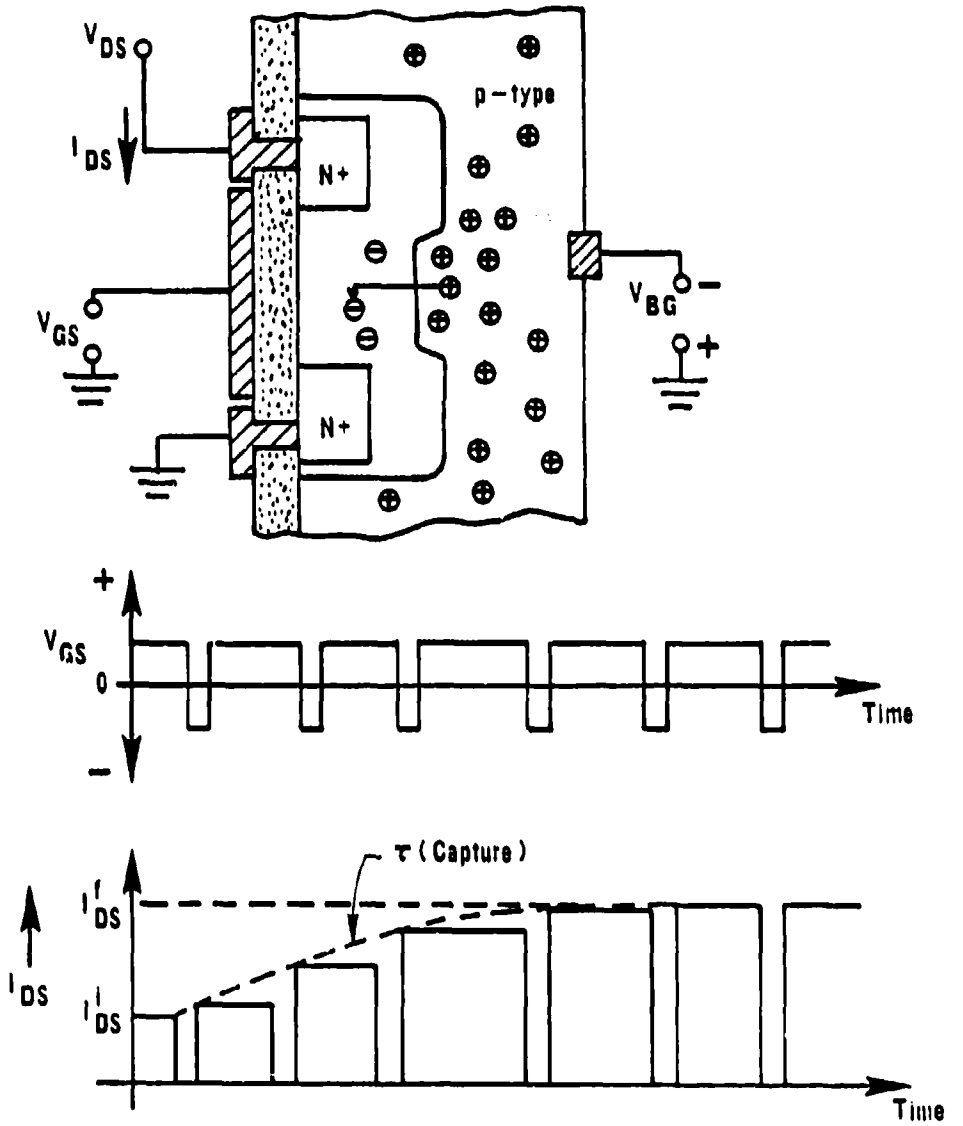


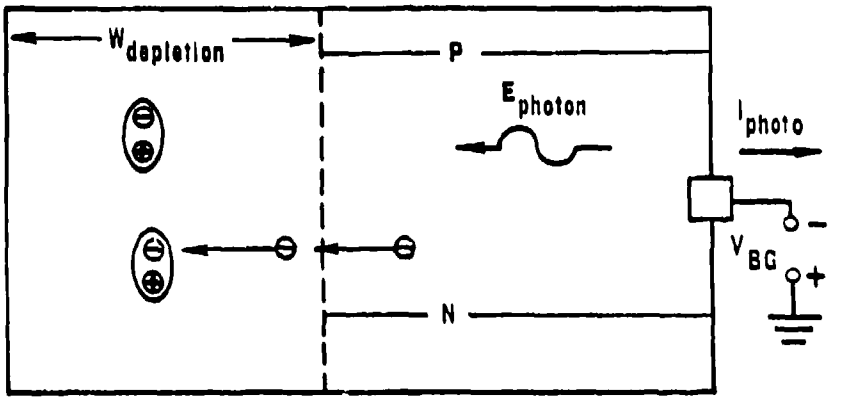
Figure 11 Technique for Determining Hole Capture Cross Section at Negative Acceptor Center using MOSFET Device

Knowing the hole concentration in the substrate from the resistivity of the photoconductor then one can determine the capture coefficient c_p by observing the number of pulses required to completely fill all the negative centers with holes leaving them in a neutral charge state and consequently the MOSFET with a much higher conductivity.

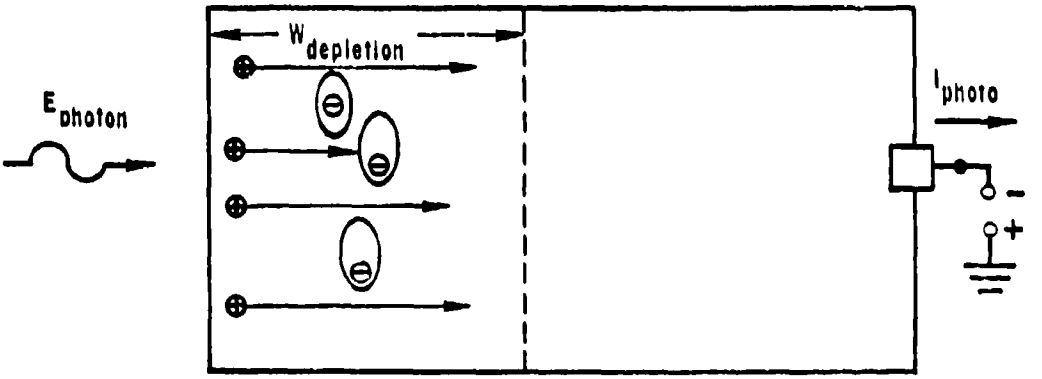
The capture of both minority carriers, electrons, and majority carriers, holes, can be observed under high electric field conditions by a direct application of techniques used previously on p-n junctions, except here capture will be observed in the surface depletion or space charge region of the MOSFET rather than in the depletion region of a p-n junction. This is illustrated in Fig. 12. The impurity centers, either indium or gallium, will be arranged to be either in the neutral or negative charge state. In the first case shown, the centers are in the neutral charge state and minority carriers are injected from the substrate by illumination with light which absorbed in the substrate generating minority carriers or electrons. These electrons diffuse and then are collected and swept across the depletion region and can be captured by neutral centers. By measuring the photocurrent, I_{photo}, and observing the time constant associated with the change in impurity charge state one can determine the capture coefficient, c_n.

In the second case, the impurity centers have been arranged to be in the negative charge state and holes injected by illumination of the surface with very short wavelength light which is strongly absorbed. Holes then drift across the depletion region and can be captured by negative centers, the change in charge state of the impurity centers will modulate the conductivity of the MOSFET. By again observing the time constant associated with the change in conductivity and the photocurrent, I_{photo}, one can determine the capture coefficient c_p under high electric field conditions.

FIELD DEPENDENT CAPTURE PHENOMENA



Minority Carrier Injection and Capture



Majority Carrier Injection and Capture

Figure 12 Determination of the Field Dependence of the Captur Cross Sections for Electrons and Holes at Acceptor Centers

Note that in all cases discussed the capture coefficient determined DOES NOT REQUIRE A KNOWLEDGE OF THE IMPURITY CONCENTRATION. In this respect the above techniques are distinctly different than most previously applied techniques which also required a knowledge of the impurity concentration which at best,was known only on the basis of an indirect determination. These techniques and particularly the first for the determination of the hole capture coefficient under near equilibrium conditions should enable an accurate result to be obtained without the uncertainties of other less direct techniques. [3]

III. APPLICATION OF THE MOSFET AS AN INFRARED DETECTOR

RESPONSIVITY

As shown in Figure 3 an infrared signal incident on the MOSFET device structure will cause a change in the drain to source current. If the temperature is low enough such that thermal emission of carriers from the impurity center can be ignored then this effect can be used to detect an infrared signal.

Figure 13 is an illustration of the technique used to determine the reponsivity of the MOSFET device structure as an infrared detector. This particular example is taken from Appendix B. Since the MOSFET device is an integrating detector the following definition of responsivity has been used,

$$\text{Responsivity} = \Delta I_{DS} \;/\; \text{Incident Energy} \tag{37}$$

$$\text{Responsivity} = \Delta I_{DS} \;/\; \hbar\omega\, \Phi\, A\, t_I \quad \text{Amps/Joule} \tag{38}$$

where I_{DS} is the observed change in drain current, $\hbar\omega$ the photon energy, A the active area of the device, and t_I is the length of the integration period. Φ is the photon flux in terms of $\#/cm^2$ sec.

The change in drain to source current depends on the width to length ratio of the channel of the MOSFET, W/L, but not at all upon the area of the device, A = W x L. As a result smaller area devices will have a much higher responsivity. Our devices are relatively large area. In addition the change in drain current is also a function of the oxide thickness and dopings of the MOSFET device structure.

However, since many detectors have responsivities quoted in terms of the units Amps/Watt in summarizing our results we have also included this quantity. The results are summarized in Table I. [33-40]

IRFET RESPONSIVITY

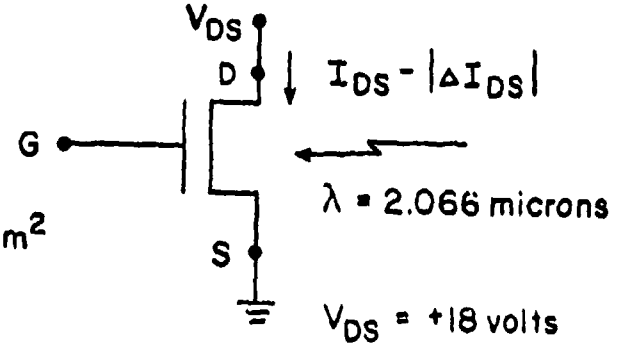
INDIUM DOPED

$T = 42°K$

$W/L = 9.32$

$AREA = 1.362 \times 10^{-2}\ cm^2$

$X_o = 5400\ Å$



INPUT ENERGY AND POWER

$\sigma° = 8.4 \times 10^{-17}\ cm^2$

$\tau°_{I_{DS}} = 3.35$ sec, $\Phi = 4.09 \times 10^{14}\ /cm^2\ sec$

$P = 5.35 \times 10^{-7}$ watts

$E_{in}\ (t = \tau°_{I_{DS}}/10) = 1.79 \times 10^{-7}$ Joules

CHANGE IN OUTPUT CURRENT $t \cong \tau°_{I_{DS}}/10$

$|\Delta I_{DS}| = .86$ mA

$$\text{RESPONSIVITY} = \frac{\text{PHOTOCURRENT}}{\text{INPUT ENERGY}}$$

$$= \frac{\text{4.8 milliamps}}{\text{microjoule}}$$

Fig. 13 Determination of the responsivity of the MOSFET as an Infrared Detector. (from Appendix B)

RESPONSIVITY OF THE MOSFET AS AN INFRARED DETECTOR

Type of Device:	GOLD	INDIUM	GALLIUM
Impurity Doping: (#/cm^3)	2.0×10^{15}	8.9×10^{15}	3.4×10^{16}
Boron Doping: (#/cm^3)	1.0×10^{16}	5.0×10^{14}	5.0×10^{13}
Oxide Thickness: (Angstroms)	4000	5400	1750
Channel W/L Ratio:	8.0	9.32	6.7
Area, A = W x L: (cm^2)	2.5×10^{-3}	1.4×10^{-2}	3.5×10^{-3}
Incident Flux, ϕ : (#/cm^2 sec.)	3.33×10^{14}	4.0×10^{14}	3.0×10^{16}
Wavelength, λ : (microns)	2.066	2.066	14.3
Time Constant of Change in Impurity Charge State, $\tau = 1/e_p^o$: (sec.)	20	29.0	6.7×10^{-2}
Time Constant of Decay in Drain Current, $\tau_{I_{DS}}$: (sec.)	20	3.35	6.7×10^{-2}
Integration Time, t_I : (sec.)	2.0	0.335	5.0×10^{-2}
Change in Drain Current: (Amps)	4.0×10^{-5}	8.6×10^{-4}	1.42×10^{-3}
RESPONSIVITY (Amps/Watt)	5.0×10^{2}	1.6×10^{3}	1.6×10^{2}
RESPONSIVITY (Amps/Joule)	2.5×10^{2}	4.8×10^{3}	3.5×10^{3}
Initial Width of Depletion Region: (microns)			11.5
Quantum Efficiency: (%)			2.8

Table I. Summary of results on the Responsivity of the MOSFET device structure as an Infrared Detector.

The gold-doped devices have a lower responsivity as a result of the fact that the gold doping is low and the boron concentration is high. This results in a small change in threshold voltage, small change in current and low reponsivity and quantum efficiency.

NOISE

Appendix D presents a detailed description of the theory and measurement of the noise characteristics of the MOSFET device structure itself.

Two noise sources are important, firstly the shot noise associated with in incident infrared flux and the 1/f surface noise of the MOSFET.[31, 32] It has been shown that for sort integration periods the shot noise associated with the incident infrared flux is the limiting factor on signal detection. As such then the infrared sensing MOSFET (IRFET) can be operated under background limited conditions. The experimental results shown are for gold-doped devices where no special efforts were made to reduce surface state densities. In this case it was found that integration periods of less than ten seconds resulted in shot noise limited operation. Similar results would be expected to apply to indium and gallium doped devices.

Starting from basic principles, it has also been shown in Appendix D that apart from possible factors of two that this shot noise is just the square root of the total number of stored charges. In this respect then all semiconductor devices are similar including CID's and CCD's. The maximum stored charge in all semiconductor devices is limited by breakdown in the substrate or the dielectric strength of the gate insulators. Devices as CID's, CCD's, or IRFET's of comparable area will have comparable maximum obtainable signal to noise ratios under shot noise limited or background limited operation. [33-35]

The selection of a particular detector for any application must then be made on the basis of other considerations.

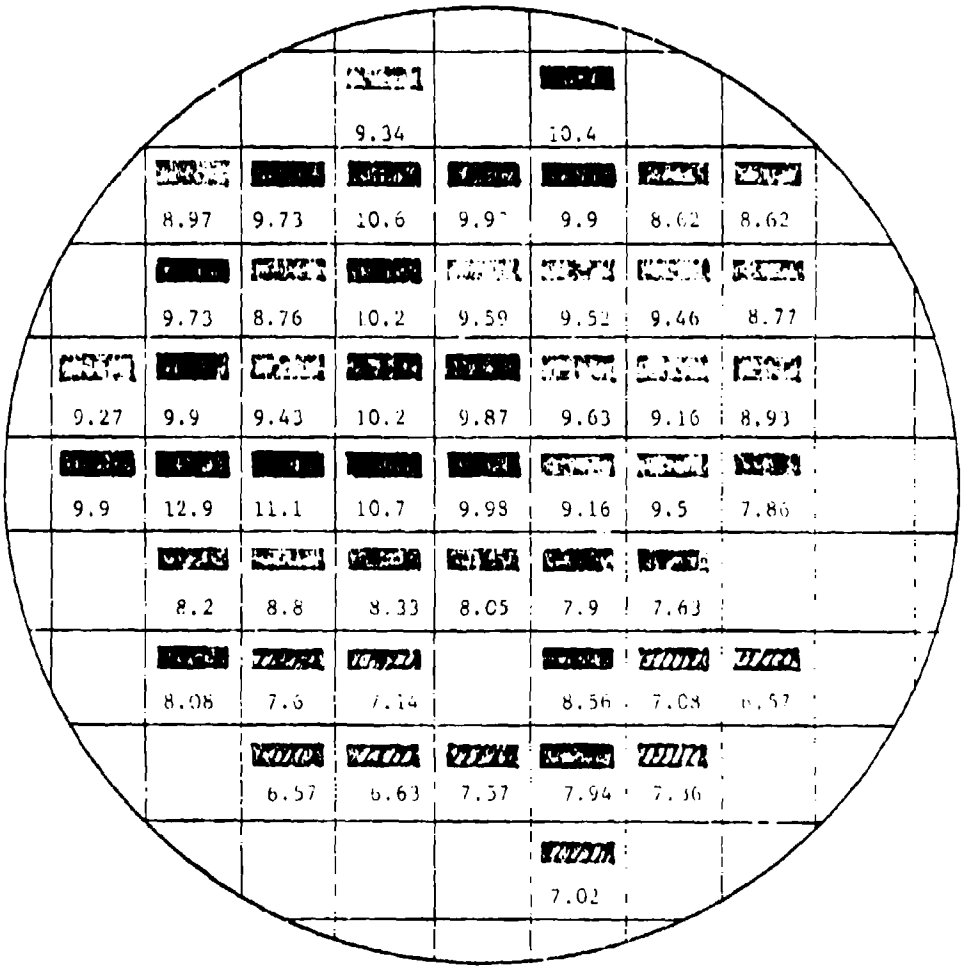
UNIFORMITY OF DOPINGS

A number of indium- and gallium-doped wafers were oxidized and detailed measurements made on MOS capacitors to determine the uniformity of dopings being achieved in the wafers since the device reponse depends directly on this doping. The IRFET is, however, not like photoconductors in that in the IRFET the responsivity does not depend upon carrier lifetimes and concentrations of residual impurities in the wafers. As such then it is only necessary to determine the uniformity of the main or majority dopant in the wafer, either indium or gallium.

Fig.14 shows the spatial variation of doping across a gallium-doped wafer. Fig.15 presents histograms of the variation in doping concentrations on both indium- and gallium-doped wafers. The results show that a variation in doping by a factor of "two" is observed across both types of wafers.

The indium-doped wafers were obtained from General Diode, Framingham, Mass. as an off the self stock item. The gallium doped wafers were received from a DOD contractor which had some left over from a prior project. In both cases no special care was taken to insure a uniform radial distribution of dopings on the wafer. These results correspond to the previous integrated circuit's experience of the Principal Investigator where it was found in commercial boron-doped wafers used in MOSFET integrated circuits that there was in general a variation of dopings by a factor of "two" in wafers of the same lot and radial variations of a factor of "two".

In addition to doping variations the MOSFET device structure is also sensitive to variations in threshold voltage. Experience has shown that even on the same chip threshold voltages would vary by 0.1 Volt. As such then the level of uniformity of responsivity which can probably be achieved with some care for MOSFET detectors on the same chip is of the order 10.0%. Clearly in most applications signal processing will be required; as was proposed originally this would involve the use of auxiliary memory planes.



concentration	color
$6.57\text{-}7.60\ 10^{15}$	
$7.61\text{-}8.62\ 10^{15}$	
$8.63\text{-}9.63\ 10^{15}$	
$9.63\text{-}12.9\ 10^{15}$	

Fig. 14 Variation of gallium doping across a wafer.

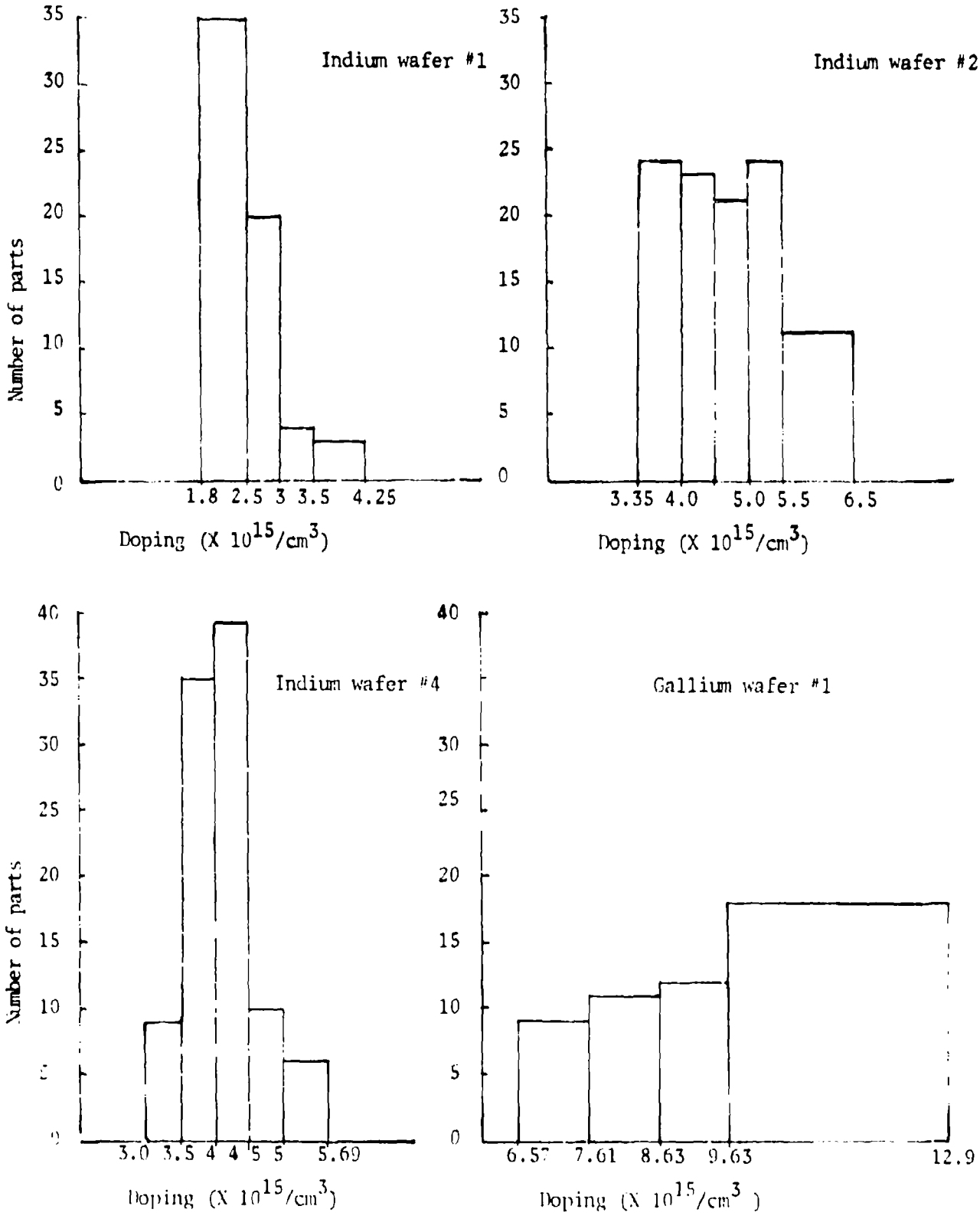


Fig. 15 Variation of Dopings on Indium- and Gallium-Doped Wafers

The considerations on uniformity can be put in quantitative terms by considering Eqn. (2); which for an industrial type n-channel process with 500 A° oxide thicknesses becomes[5]:

$$V_T = -1.0 + 0.9 (1 + V_{BG})^{1/2} (N_I / 10^{16})^{1/2} \text{Volts} . \quad (39)$$

Variations in oxide charge, boron dopings, and impurity dopings will be reflected in threshold variations in the MOSFET detector elements which will result in responsivity variations. N_I is the total ionized impurity concentration.

Initially the ionized impurity concentration will just be due to boron, if the boron concentration is low the surface depletion region will be very wide. However, if the boron concentration is low it will be difficult to control this doping uniformily. Suppose as an example the boron concentration is $10^{14}/cm^3$, and a back-gate bias of 25.0 Volts is used, then Eqn. (39) becomes;

$$V_T = -1.0 + 0.9 (5) (10^{-1}) = -1.0 + 0.45 \text{ Volts}. \quad (40)$$

A variation in background boron doping by a factor of four will cause a variation in threshold voltage of ± 0.45 Volts.

At the end of the transient decay there will have been a large increase in the threshold voltage due to the ionization of the deeper level impurity as indium or gallium, the boron then becomes an insignificant consideration. Consider the Consider the case where the deeper level ionized impurity concentration has reached a value of $10^{16}/cm^3$, then Eqn. (39) becomes,

$$V_T = -1.0 + 0.9 (5) = -1.0 + 4.5 \text{ Volts}. \quad (41)$$

A change in impurity concentration of 30% will cause a change in threshold voltage of about 10% or ± 0.45 Volts.

In addition changes in oxide charge by amounts of $10^{11}/cm^2$ will cause threshold voltage variations on this oxide thickness of ± 0.25 Volts. The total result might thus be threshold voltage variations of the order 1.0 Volt. If the excess of gate voltage above threshold, $V_{GS}-V_T$, is of the order 10.0 Volts then variations in conductivity and responsivity of the order 10% might be anticipated.

APPLICATION TECHNIQUES

As was described at previous points in the text the IRFET detector would be employed in an X-Y addressed array as shown in Fig. 16. This imaging array essentially constitutes a read-only memory plane where the conductance of each device is a function of the infrared flux incident on that particular location. Associated with this imaging memory plane would be off-chip logical control elements and auxiliary memory planes for signal processing as shown in Fig. 17.

The conductance of each element in the imaging array would be read on an analog basis both before and after illumination and converted to a digital format by the A/D converter shown in Fig. 17. In doing so, note that since the IRFET is a static or D.C. memory element the read operation can be suppressed until the address location becomes stable. Following this the length of the read operation, or sample time, is determined by the precision which is desired or required in reading the conductance of the element. In theory these sample periods could be made very long allthough at the expense of long frame times.

The random-access memories (RAM's) in Fig. 17 would be used to store the conductance of each imaging element or IRFET before and after illumination. The programable read-only memory (p-ROM) would be used to compensate for any non-uniformities in the responsivity of elements in the array. The net result would be to allow a very high degree of resolution between different flux intensities at different imaging elements to be achieved.

This signal processing in some senses is analogous to the "time-delay and integration (TDI)" used in CCD scanned photoconductors. The difference here is due to the fact that the IRFET works on a static as opposed to dynamic memory concept. Note also that the IRFET array could achieve a very high resolution in a full staring mode. The IRFET array and signal processing technique does not require mechanical motion of either the target or the array, as opposed to TDI techniques which require motion. [21, 36-40]

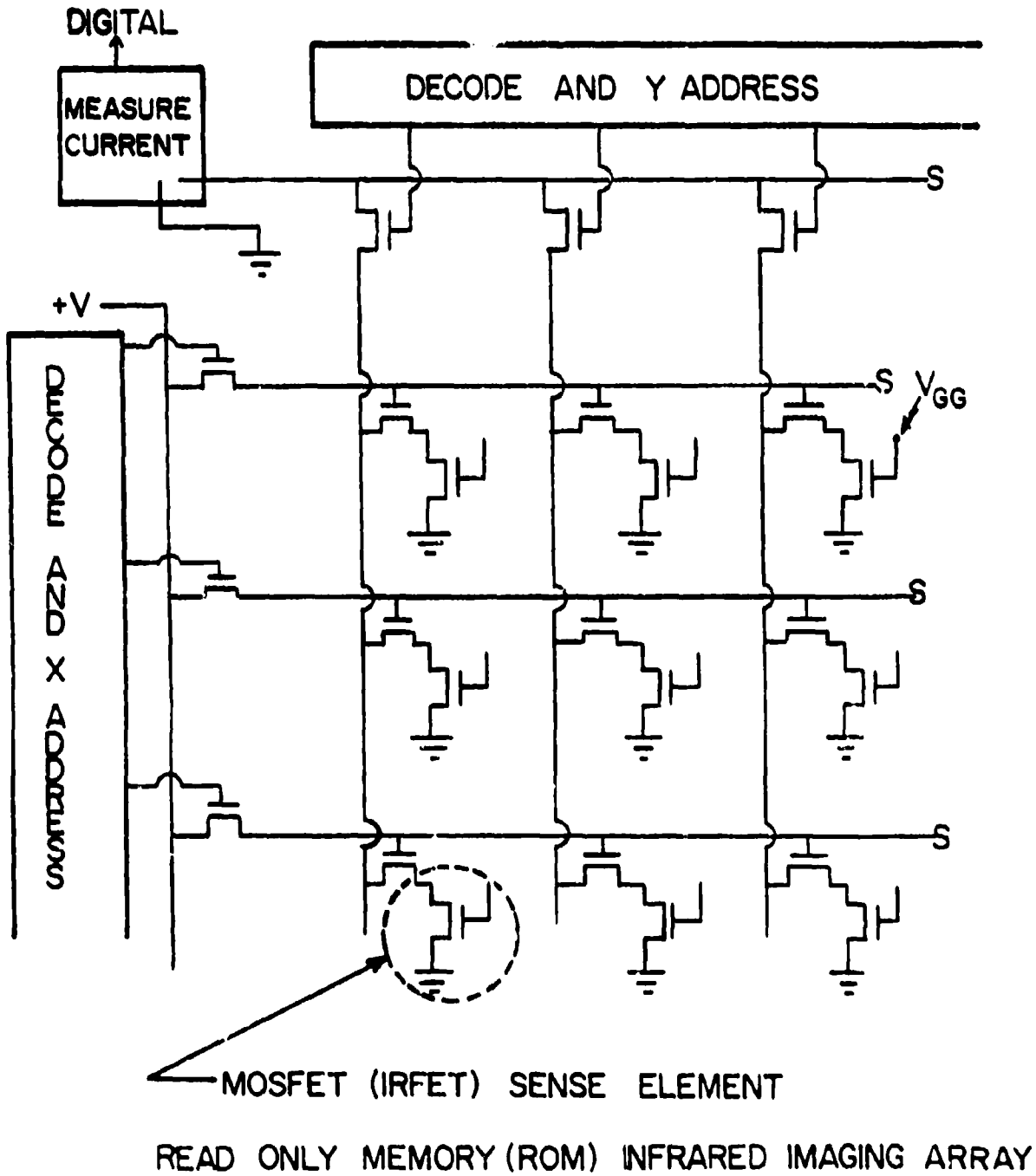
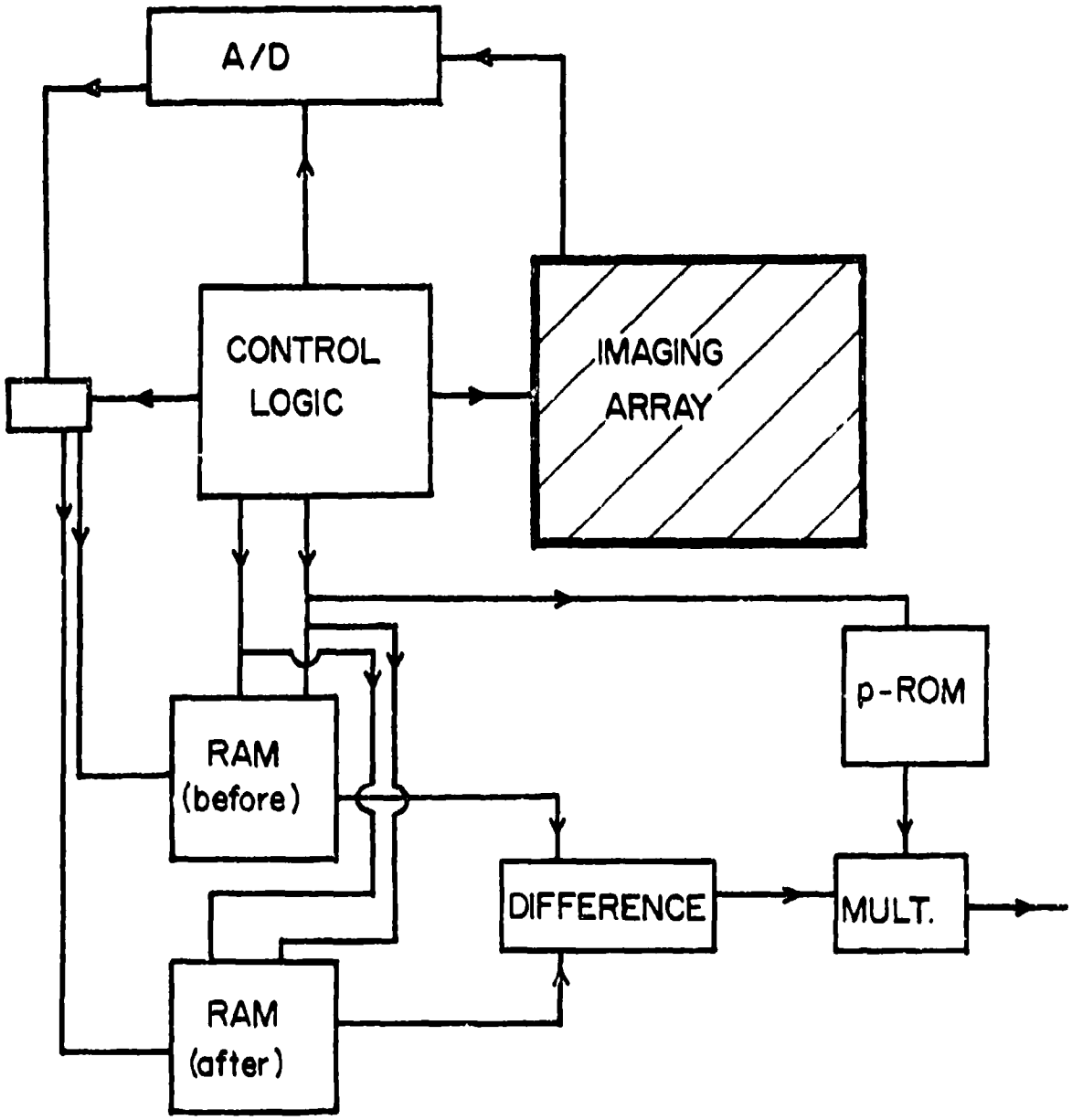


Fig. 16 Application of the MOSFET detection in an imaging array.



POSSIBLE APPLICATION TECHNIQUE
WITH AUXILARY MEMORY PLANES

Fig. 17 Utilization of auxiliary memory planes.

COMPARISON TO CCD SCANNED PHOTOCONDUCTOR ARRAYS

Table II presents a comparison of the operation characteristics of a 32 bit CCD scanned array of gallium-doped photoconductors[39, 40] to the projected characteristics of an IRFET array based on our current devices and based on better smaller area devices. Such a comparison is difficult to make since the two different types of detectors have such different operating principles and it must be kept in mind in doing so how each detector works.

While this Table summarizes a number of points from previous sections a number of points are worthwhile considering again in detail. The most striking feature is that the IRFET detectors have a much higher responsivity, which as was pointed out previously,does not depend upon carrier lifetimes and residual impurity concentrations. Since the IRFET employs only the gallium centers within about one mil from the surface the quantum efficiency is on the other hand somewhat lower.

The theoretically maximum attainable signal to noise ratio in both types of systems is essentially just the square root of the total number of stored electrons. In the IRFET detector the detector and integration element are one and the same and have the same area. In the CCD system the storage is usually smaller than the detector. Consequently the IRFET can acheive at least the same if not a significantly larger signal to noise ratio.

The bottom lines in the Table emphasis the difference in the read-out techniques and the signal at the output of the system. In the CCD system the output is an integrated charge in coulombs; in the IRFET system it would be a current which can be read for an indefinitely long time period on a non-destructive basis. In the IRFET the integrated charge does not flow in the external circuit but rather remains stored in the depletion region of the MOSFET until the reset operation. The Table also indicates that acceptable frame rates could be acheived in most applications using the IRFET detector array.

A COMPARISON OF GALLIUM-DOPED SILICON INFRARED DETECTORS *

	32 BIT CCD SCANNED ARRAY (As published by Hughes Aircraft Co.)39, 40	PROJECTED IRFET ARRAY BASED ON: CURRENT DEVICES		BETTER DEVICES	
		$N_{Ga} = 3\times10^{16}/cm^3$ $\Delta V_T = 2$ Volts $V_{GS} = 7$ Volts		$N_{Ga} = 6\times10^{16}/cm^3$ $\Delta V_T = 18$ Volts $V_{GS} = 18$ Volts $\tau_{I_{DS}} = \tau_{Ga}/8$	
CELL AREA(cm^2)	10^{-4}(4x4 mil)	3.5×10^{-3}		2×10^{-5}	
QUANTUM EFFICIENCY (%)	30	2.8		6.8	
RESPONSIVITY	2.5 Amps/Watt	150.0 Amps/Watt (effective value)		1.4×10^6 Amps/Watt (effective value)	
UNIFORMITY OF RESPONSIVITY		1.5×10^4 Amps/Joule		1.0×10^9 Amps/Joule	
DEPENDS ON:					
Gallium Doping..	Yes ...	Yes		Yes	
Lifetime.....	Yes ...	No		No	
Residual Impurity Concentrat..	Yes ...	No		No	
OPTICS	f=1.5	f=1.5		f=1.5	
300°K BACKGRND	SPECIAL FILTERS	FILTERS	NO FILTER	FILTERS	NO FILTER
(#/ cm^2sec)	10^{13}	2×10^{14}	2×10^{17}	2×10^{14}	2×10^{17}
SIGNAL					
(#/ cm^2sec)	5×10^{13} low flux	low	high	low	high
(watts)	10^{-10}	flux	flux	flux	flux
FRAME TIME	1.5 millisec	10 sec	10 millisec	1.5 sec	1.5 millisec
STORED CHARGE					
(# of electrons)	4×10^6(limited by CCD 1.0x0.4 mil)	10^{11}		3×10^8	
MEMORY TYPE	DYNAMIC(AC)	STATIC(DC)		STATIC(DC)	
NEP (watts)	8.5×10^{-14}	--		--	
D* (cm $Hz^{1/2}/W$)	2×10^{12}	--		--	
SIGNAL/NOISE RATIO	2×10^3	2×10^5		1×10^4	
BLOOMING	Yes	No		No	
SIGNAL	6×10^{-13} coulombs	1.4 milliamp		68 milliamp(max)	
READOUT	Destructive	Nondestructive		Nondestructive	

Table I. A comparison of the characteristics of CCD scanned photoconductors to infrared sensing MOSFET's.

*Based on material presented at the 2nd Int. Conf. on Solid-State Devices, L.Forbes, K.W. Loh, and L.L.Wittmer.

IV. CONCLUSIONS

This report provides a detailed description of the characteristics of gold, indium, and gallium doped MOSFET device structures as infrared detectors. In doing so it also provides a detailed description of the characteristics of these three impurities in silicon. In the case of gold, the results obtained could be compared to those obtained previously by this and other authors. In the case of indium and gallium the work was much more exploratory and this work constitutes to the author's best knowledge the first direct observation of the thermal and optical emission characteristics of these centers.

Work was begun on gold-doped devices first because of the author's prior experience with this impurity center and due to the fact that the measurements could be easily done above 77 ^{o}K. At the beginning of the project facilities existed only for measurements above liquid nitrogen temperatures and the laboratory facility at the University of Arkansas for processing MOSFET devices was just being set-up. This work, on gold-doped devices, served to demonstrate that the device did in fact work according to the original design concepts which had been previously reported in August 1974. The gold-doped devices, however, had a low quantum efficiency; primarily since it was desired not to overcompensate the substrate and make it highly resistive at room temperature.

Following this, work was initiated on indium and gallium doped devices. By this time sufficient experience had been obtained in using the MOSFET device structure as an infrared detector to allow the design and acquisition of the low temperature and long wavelength infrared systems required in characterizing the device. Classical chopped radiation systems are not appropiate for an integrating infrared detector and many of our arrangements are rather unique. In addition the specially doped indium wafers had been obtained and a diffusion source for producing gallium doped wafers identified. At this time, the spring of 1975,

neither indium nor gallium doped wafers were readily available, even from DOD contractors who were also just starting to become actively engaged in work on indium and gallium doped silicon detectors.

The subsequent work on indium and gallium doped detector proceeded in a relatively straightforward manner. A very significant difference was however to occurr in later work with the realization that lightly boron doped substrates could be employed to make a very large improvement in the quantum efficiency of the detectors. One objection to use of the IRFET detector had been the low quantum efficiency reported in the initial work and in the original design proposal. Using devices with a large indium or gallium concentration and a low boron concentration necessitated reworking all equations describing device operation and the development of different analytical techniques. The detailed work is presented in the Appendices, and this introduction serves to outline all the different possibilities for doping ratios and device reponse characteristics and summarize results.

If one is most interested in impurity center characteristics, for the measurements at least, it is more convenient to have a large boron concentration and low indium and gallium concentration. Such crystals would however be hard to grow.

This report we believe demonstrates that the IRFET device structure can in fact be used as a detector in the near, middle, and far infrared wavelength regions. It's very unique characteristics might make it particularily advantageous in some applications.

Besides the participants the author would like to acknowledge the assistance of Prof. C.T. Sah, at the University of Illinois, and the technical contract monitor, Dr. Jacques E. Ludman, of AFCRL, in providing insight and direction to the course of this work.

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APPENDIX A

GOLD-DOPED DEVICES*

Gold has been used most commonly as a deep impurity in silicon diodes and transistors to increase their switching speed. An accurate description of the behavior of gold in silicon is useful in designing these devices and predicting their characteristics; therefore, exhaustive work has been done by several investigators in order to describe the thermal and optical emission and capture of holes and electrons at gold centers in bulk silicon [1,2,3]. This paper discusses an extension of the work carried out so far on the influence of gold in the surface space-charge region of MOS devices. Our work is the first known attempt to fully examine the effects of infrared radiation on the gold impurity centers in a surface depletion region behind the inverted channel of metal-oxide-silicon field-effect transistor (MOSFET).

As a deep two-level impurity in bulk silicon, gold introduces an acceptor level and a donor level in the bandgap [4,5]. The gold center can be ionized by the capture of holes from, and the emission of holes to, the valence band and/or the capture of electrons from, and the emission of electrons to, the conduction band (see Fig. 1[6]). This ionization will occur as a result of any sufficient thermal or optical excitation. Within a depletion region, however, only the emission of carriers from the centers is probable, since there are no free holes or electrons available for recapture until the reverse-bias, or inversion condition, is removed by accumulation. In addition, the thermal emission rate is a very strong function of temperature[7]; thus, thermal emission can be effectively eliminated by adequate cooling.

Gold-doped MOSFETs have been designed and fabricated in the University of Arkansas Solid-State Devices Laboratory for use as infrared detectors

*This section is based on material which has been published in the IEEE Trans. on Electron Devices, Oct. 1975, pp. 916-924, W.C. Parker and L.Forbes.

GOLD IMPURITY CENTER IN SILICON

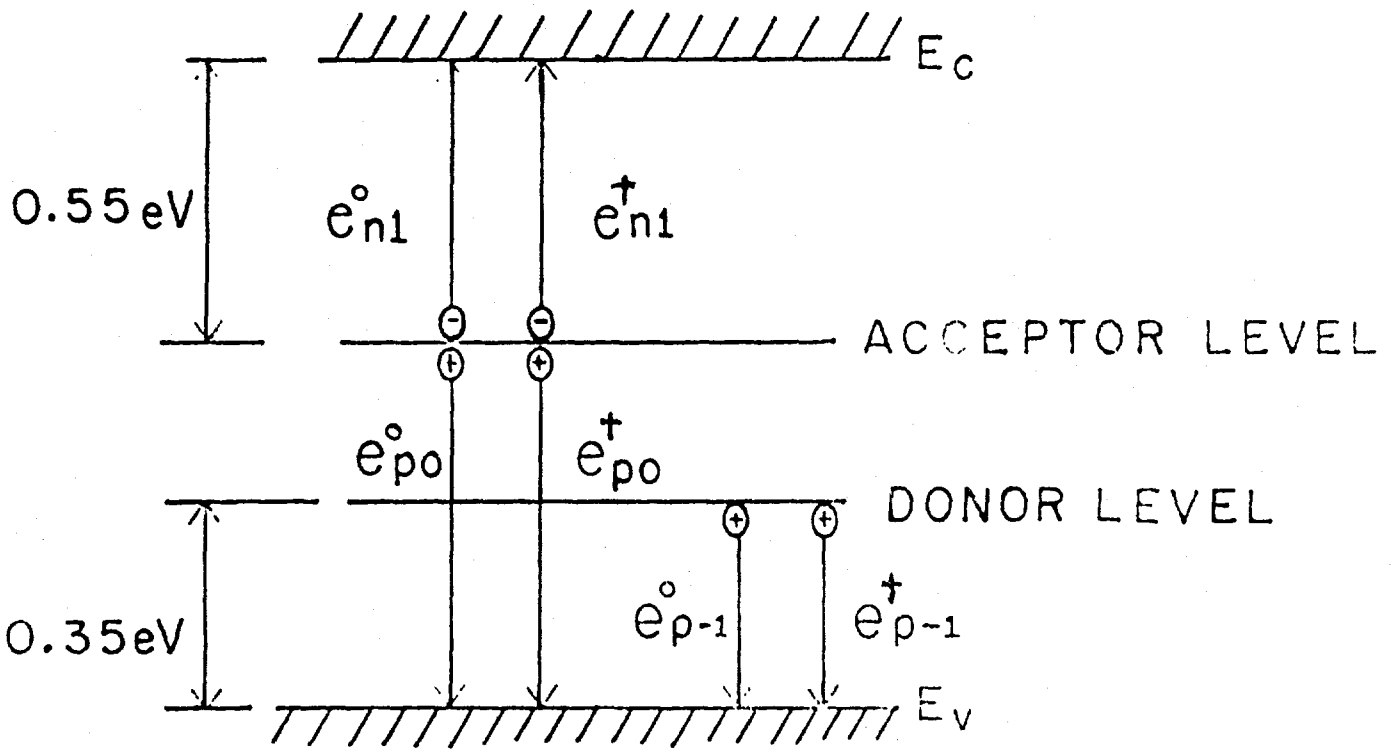


Fig.1. The important carrier emission processes from the energy levels of gold in silicon. In each case the superscripts "t" and "o" denote thermal and optical phenomena, respectively. e_{p-1} is the emission of holes from the gold donor level to the valence band, e_{po} is the emission of holes from the gold accepter level to the valence band, and e_{n1} is the emission of electrons from the acceptor level to the conduction band.

(IRFETs) [8]. The basic research objective was to experimentally characterize the operation of this new type of photon detector [9] when illuminated by near-infrared wavelength radiation, i.e., 1.38 to 3.54 μm. It was also desired to show that IRFET channel conductance depends upon the characteristics previously observed for the gold center in bulk silicon by p-n junction capacitance measurements.

THEORETICAL OPERATION OF IRFETs

The IRFET is operated at low temperatures, and impurity photoionization is employed to modulate the channel conductance. In the schematic diagram of Fig. 2, an n-channel device is shown. The p-type substrate is doped with both the shallow-level acceptor boron, and gold. At the temperature of operation, the relative dopings have been chosen such that all the gold centers are ionized.

If the MOSFET is originally preset by turning it off and accumulating the surface, then the gold impurity centers in the surface space-charge, or depletion, region are ionized by the capture of holes (positive charge state) and remain filled when positive gate voltage is applied. In theory, the conductance of the MOSFET channel is a function of the number of ionized impurity centers in the space-charge region since the threshold voltage is a function of this space charge. If infrared radiation, e.g., 1.77 to 3.54 μm, illuminates the device, then the gold centers in the depletion region can be photoionized or discharged by the emission of holes to the valence band. By restricting the discussion to the donor-level response, analysis of the IRFET is greatly simplified. At higher photon energies, the response involves the combined emission rates of the acceptor and donor levels.

Photoionization of the gold impurity centers in the surface depletion region will change the net space charge and modulate the conductance of the IRFET.

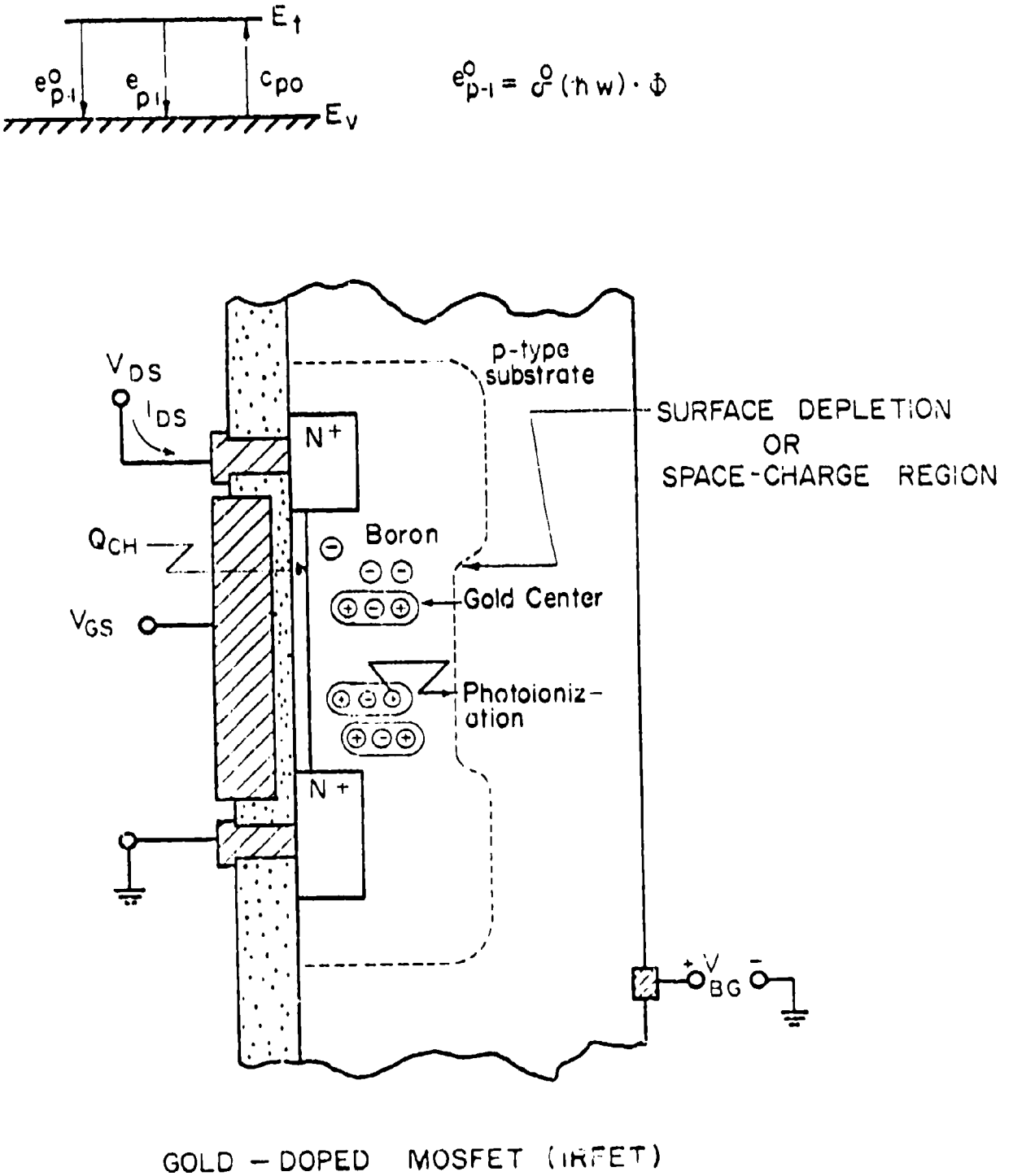


Fig. 2. A schematic diagram of the gold doped, infrared-sensing MOSFET (IRFET). Q_{CH} denotes the charge contributed by electrons in the surface channel.

This basic operating principle may be better understood by writing the charge equation as

$$Q_G + Q_{ss} = - (Q_{CH} + Q_{Au} + Q_B) , \qquad (1)$$

where Q_G is the charge at the gate electrode, Q_{ss} is the fixed positive surface-state charge (which is dependent on crystalline orientation and process) at the Si-SiO_2 interface, Q_{CH} is the charge contributed by electrons in the channel, Q_{Au} is the charge contributed by ionized gold in the oxide or near the silicon surface, and Q_B is the net charge in the surface depletion region generated by ionized doping impurity atoms. Since all terms in Eq. (1) except Q_{CH} and Q_B are constant, the n-channel gold-doped MOSFET must obviously lose electrons from its inversion layer as the net surface space charge becomes more negative by photoionization of the gold centers due to infrared illumination, and channel conductance thus decreases in order to maintain charge neutrality.

The basic physical mechanism of impurity photoionization is also shown in Fig. 2. The important microscopic processes for an impurity center with an energy level near the valence band edge of silicon are optical hole emission e_p^o, thermal hole emission e_p^t (which is negligible at low temperatures), and hole capture c_p. Capture is important only during the reset operation of the IRFET since at all other times the gold impurity centers are in a depletion region where there are no free holes to be captured.

DEVELOPMENT OF A DEVICE MODEL

A. Threshold Voltage

The turn-on voltage V_T of a MOSFET is

$$V_T = V_{FB} + 2\phi_f - Q_B/C_o , \qquad (2)$$

where V_{FB} is the gate voltage required to establish the flat-band condition

(no charge is induced in the silicon substrate) and $2\phi_f - Q_B/C_o$ is the gate voltage required to just bend the bands through an amount equal to twice the Fermi potential ϕ_f. The gate oxide capacitance per unit area, C_o, is defined as

$$C_o = \kappa_{ox}\varepsilon_o/\chi_{ox} , \tag{3}$$

where κ_{ox} is the relative dielectric constant of silicon dioxide, ε_o is the electrical permittivity of free space, and χ_{ox} is the thickness of the oxide. Eq. (2) is well-known and a further definition of terms, or a more detailed derivation, may be found in several reference works [10,11].

The channel conductance of a MOSFET can be modified by application of a reverse-bias voltage V_{BG} to the substrate. This back-gate bias serves to ionize additional dopant impurities in the space-charge region beneath the inversion layer. If boron is the only impurity doping in the silicon substrate, back-gate bias affects the threshold voltage of Eq. (2) through the term Q_B. The expression for the threshold voltage of an n-channel MOS device thus becomes

$$V_T = V_{FB} + 2\phi_f + \sqrt{2\kappa_s\varepsilon_o qN_A(2\phi_f - V_{BG})}\,/C_o , \tag{4}$$

where κ_s is the relative dielectric constant of silicon, q is the electronic charge, and N_A is the number of boron acceptor atoms per unit volume of the substrate. As back-gate bias increases in absolute value, the threshold voltage for a depletion-mode, or normally "ON", device decreases in absolute value.

B. Change in Threshold Voltage

If the substrate is additionally doped with gold, then the net space charge consists of contributions from both the ionized boron centers (negative) and

the gold impurity centers (positive). Eq. (4) may be rewritten as

$$V_T = A + B\sqrt{N_I}\ , \tag{5}$$

where

$$A = V_{FB} + 2\phi_f, \tag{5a}$$

$$B = \sqrt{2\kappa_s\epsilon_o q(2\phi_f - V_{BG})}\ /C_o \tag{5b}$$

and N_I is the effective impurity doping concentration. In Eq. (5), the Fermi potential ϕ_f is assumed to remain approximately constant for a device with substrate bias, independent of temperature.

If the boron doping concentration is much greater than the gold doping concentration, and the cooled ($T < 100°K$) IRFET is preset in the dark, then all the gold centers will be filled with holes, or positively charged. The effective doping concentration is $N_I = N_A - P_D$, where P_D is the total number of ionized gold donor atoms. The gold donor centers in the surface depletion region behind an inverted channel remain in their positive charge state until the device is illuminated with near-infrared radiation. They then become neutral with an average time constant $\tau = 1/e_p^o$ [12], and

$$P_D(t) = N_{TT}\exp(-t/\tau)\ , \tag{6}$$

where N_{TT} is the number of gold impurity atoms per unit volume and $P_D(t)$ is the number of ionized gold donor centers as a function of illumination time [8].

After surface accumulation at $t = 0$, Eq. (5) becomes

$$V_T^i = A + B\sqrt{N_A - N_{TT}}\ , \tag{7}$$

where V_T^i is the initial threshold voltage of the device before illumination. If near-infrared radiation illuminates the IRFET until all the gold centers

emit their holes to the valence band, or discharge, then $P_D = 0$ and Eq. (5) becomes

$$V_T^f = A + B\sqrt{N_A} , \tag{8}$$

where V_T^f is the final threshold voltage of the device with all the gold centers neutral.

The static change in threshold voltage, ΔV_T, can now be determined by subtracting Eq. (7) from Eq. (8):

$$\Delta V_T = V_T^f - V_T^i = B(\sqrt{N_A} - \sqrt{N_A - N_{TT}}) , \tag{9}$$

since $N_{TT} << N_A$ then

$$\Delta V_T = B(N_{TT}/2\sqrt{N_A}) . \tag{9a}$$

An expression for the illumination time dependence of the threshold voltage, $V_T^L(t)$, can be found by combining Eqs. (5), (6), (7), and (9):

$$V_T^L(t) = V_T^i + \Delta V_T^i(t) = V_T^i + \frac{B}{2\sqrt{N_A}} N_{TT}[1 - \exp(-t/\tau)] . \tag{10}$$

C. Statement of Device Equations

The fundamental current-voltage (I-V) characteristics of a MOSFET are

$$I_{DS} = \beta V_{DS}(V_{GS} - V_T - V_{DS}/2) \tag{11}$$

in the linear region where $V_{GS} - V_T > V_{DS}$, and

$$I_{DS} = \beta (V_{GS} - V_T)^2/2 \tag{12}$$

in the saturation region where $V_{GS} - V_T < V_{DS}$. Eqs. (11) and (12) were taken from the derivation of Carr and Mize [10] in which the surface carrier mobility

is assumed to be constant, and I_{DS} is the drain-to-source current flowing in the channel, V_{DS} is the voltage applied between the drain and source, V_{GS} is the applied gate voltage, V_T is the threshold voltage of the MOSFET, and $\beta = \mu C_o W/L$, where μ is the surface electron mobility in an n-channel device and W/L is the geometric width-to-length ratio of the channel.

It can be shown that for a static change in the threshold voltage of a MOSFET, the resulting change in the drain-to-source current, ΔI_{DS}, is

$$\Delta I_{DS} = - \beta(\Delta V_T)V_{DS} \tag{13}$$

in the linear region, where $\beta = \mu C_o W/L$, and

$$\Delta I_{DS} = - \beta(\Delta V_T)(V_{GS} - V_T - \Delta V_T/2) \tag{14}$$

in the saturation region. Solving Eqs. (11) and (12) for β in the linear and saturation regions, respectively, and combining the results with Eqs. (13) and (14) yields two different equations which now specify the static change in threshold voltage in terms of experimentally observable I-V characteristics:

$$\Delta V_T = - \frac{\Delta I_{DS}(V_{GS} - V_T^i - V_{DS}/2)}{I_{DS}^i} \tag{15}$$

in the linear region, and if $\Delta I_{DS} << I_{DS}^i$, then

$$\Delta V_T = - \frac{\Delta I_{DS}(V_{GS} - V_T^i)}{2I_{DS}^i} \tag{16}$$

in the saturation region, where I_{DS}^i is the current before illumination.

A description of the current transients versus time readily follows by substituting Eq. (10) for V_T in Eqs. (11) and (12). Now

$$I_{DS}^{L}(t) = \beta V_{DS}(V_{GS} - V_T^i - \frac{B}{2\sqrt{N_A}} N_{TT}[1 - \exp(-t/\tau)] - V_{DS}/2) \qquad (17)$$

and

$$I_{DS}^{L}(t) = \frac{\beta(V_{GS} - V_T^i - \frac{B}{2\sqrt{N_A}} N_{TT}[1 - \exp(-t/\tau)])^2}{2} \qquad (18)$$

in the linear and saturation regions, respectively, where $I_{DS}^{L}(t)$ is the drain-to-source current in the IRFET as a function of illumination time. Eqs. (17) and (18) are valid only if all the gold centers are in their positive charge state at $t = 0$.

EXPERIMENTAL METHOD

A. Technique of Measurements

Drain current, I_{DS}, and photocurrent, ΔI_{DS}, were measured as functions of drain voltage, gate voltage, temperature, photon energy and illumination time. These results were compared with theoretical calculations in order to evaluate the accuracy of our model. Relative doping concentrations were determined from IRFET threshold voltage versus back-gate bias measurements before and after infrared illumination.

The MOSFET devices were mounted in a temperature-controlled sample chamber, and a Bausch and Lomb high-intensity grating monochromator was employed as the light source. A germanium or silicon filter was used to suppress all stray light and higher orders of diffracted light. All current measurements were performed with a Hewlett-Packard DC Micro Volt-Ammeter 425A in conjunction with a Houston Instrument Omnigraphic 2000 X-Y Recorder. All voltages were measured with Fluke Digital Multimeters 8000A. An iron-constantan thermocouple voltage was monitored with a Keithley Electrometer 602 to determine temperature.

B. Processing of Devices

The n-channel MOSFETs were manufactured on 1- to 2-Ω cm boron-doped silicon wafers of (100) orientation. After the gate oxidation, gold was evaporated on, and diffused for 7 minutes at 1000°C from, the back face of each slice. The devices were then pulled straight out to the end of the furnace and cooled to room temperature. The resulting gold concentration of approximately 2×10^{15} cm^{-3} corresponds to the results of previous work with bulk silicon (p-n junctions) [1]. The gate oxides of the MOSFETs used in the work are 4000 Å thick (estimated by viewing the oxide perpendicularly under white light), and the channels have an 8.17 W/L ratio in a circular geometry. Each device was placed on a TO-5 header and mounted in a reflective cavity to provide for frontside and edge illumination.

RESULTS AND DISCUSSION

A. Results

A typical data curve using monochromatic illumination is shown in Fig. 3. In this case the drain-to-source current is plotted as a function of illumination time, but ΔI_{DS} exhibits similar behavior as a function of temperature. The emission rate of carriers from the gold centers thus can be determined by noting the time τ at which $-\Delta I_{DS}(t)$ reaches a value equal to 1/e of its maximum value.

The thermal time constant associated with emission of holes from the gold donor level, τ_D, is plotted versus 1000/T (°k) in Fig. 4, $\tau_D = A \exp(\Delta E/kT)$, where A is a constant, ΔE is the energy difference, or location, of the level with respect to the valence band, k is Boltzmann's constant, and T is the temperature in degrees Kelvin. The slope of the line now determines ΔE:

$$\Delta E = 0.19842\ \Delta \log_{10} \tau_D / \Delta(1000/T) \qquad (19)$$

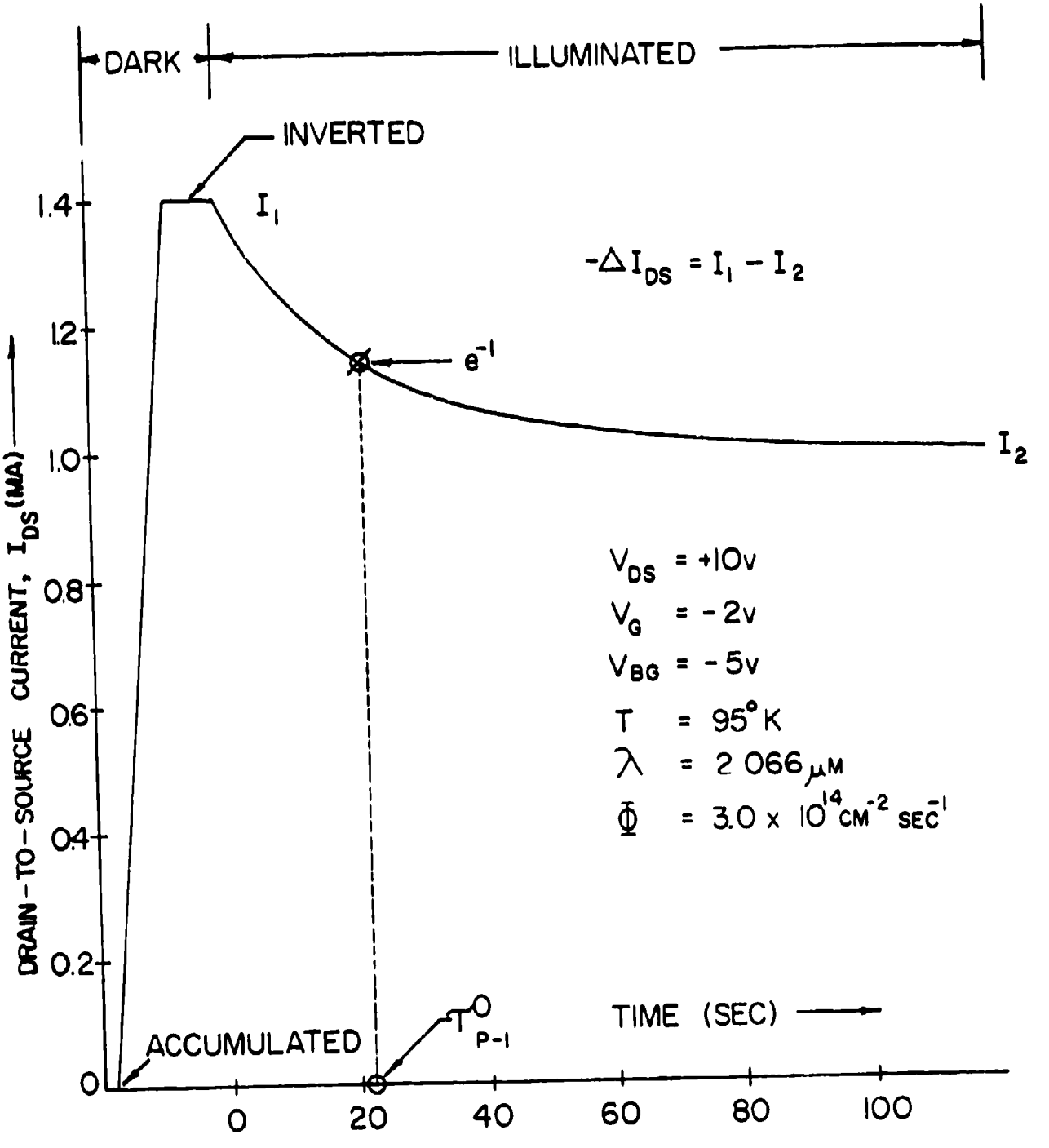


Fig.3. A typical example of the time dependent drain current, I_{DS}, in an IRFET due to infrared illumination.

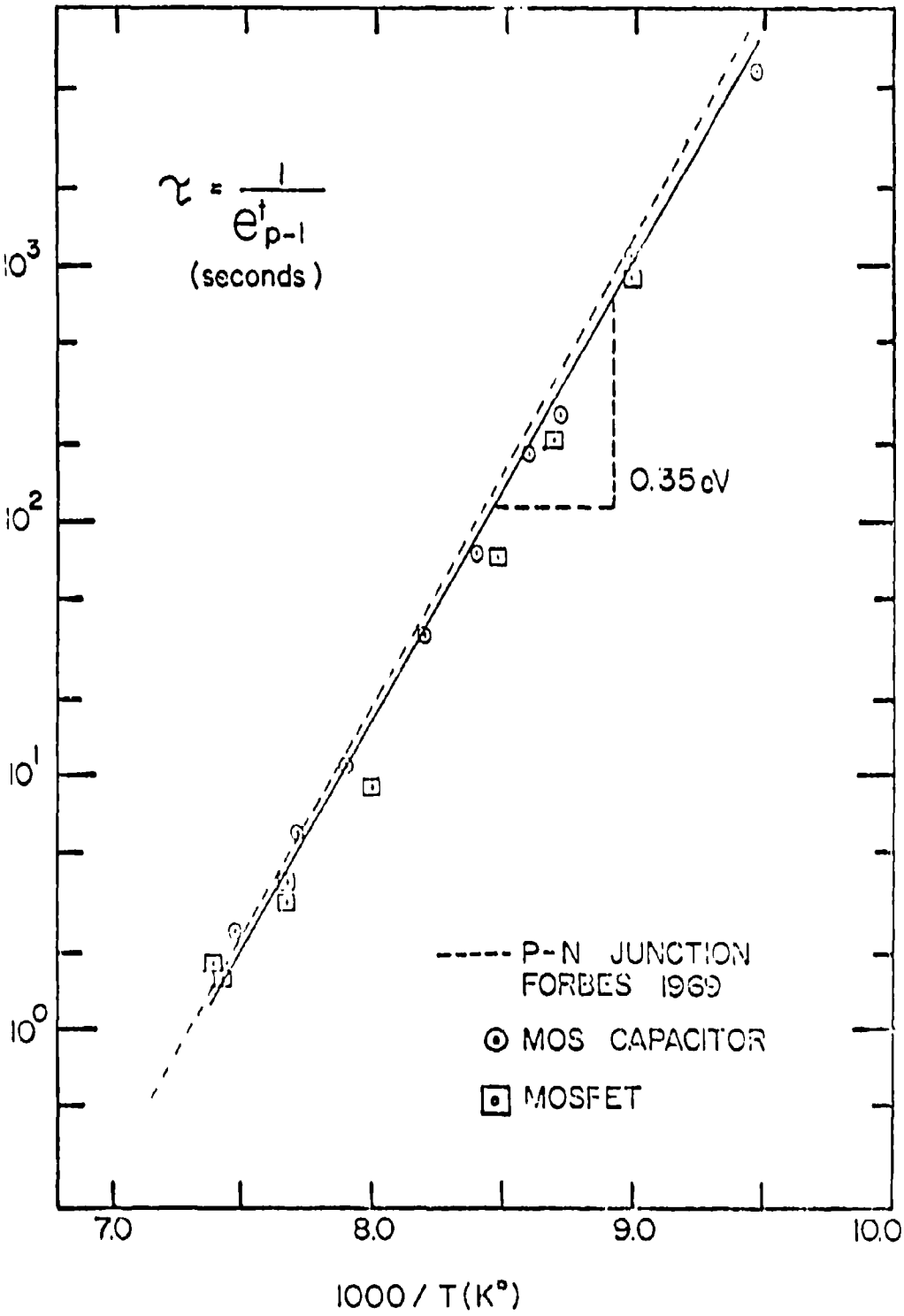


Fig. 4. The thermal time constant for hole emission from the [illegible] different devices.

which for the gold donor level is 0.35 eV [2]. This result is also shown to closely match the results previously obtained for the gold donor level in bulk silicon and in a surface depletion region by measuring capacitance transients on p-n junctions [1] and MOS capacitors [9], respectively. It was therefore concluded that a concentration of gold impurity centers ($N_{TT} < N_A$) was observed in the surface depletion region under the MOSFET channel.

The optical emission of carriers from the gold center is observable if the temperature is low enough such that $e^o >> e^t$. Then $e^o = \sigma^o \Phi$, where σ^o is the photoionization cross section in cm^2 and Φ is the incident photon flux in number per cm^2 per second. However, gold is a double-level impurity in silicon, and optical response can be observed for both the donor and acceptor levels in the near-infrared wavelengths from 1.13 to 3.54 μm.

Fig. 5 shows the relative photoionization cross sections σ^o_{p-1} and $\sigma^o_{p0} + \sigma^o_{n1}$ respectively, of the donor level and the acceptor level as functions of photon energy, i.e. from 0.38 to 0.72 eV and 0.58 to 0.9 eV. The acceptor level response was observed by operating the IRFET at an elevated temperature where e^t_{p-1} is very large, but still cool enough such that e^t_{p0} and e^t_{n1} are small. The optical time constant associated with emission of carriers from the gold acceptor level, τ_A, is given by

$$\tau_A = 1/(e^o_{p0} + e^o_{n1}) = 1/[\Phi(\sigma^o_{p0} + \sigma^o_{n1})] , \qquad (20)$$

where e^o_{p0} is the optical emission rate of holes to the valence band (neutral charge state) and e^o_{n1} is the optical emission rate of electrons to the conduction band (negative charge state). Since the acceptor level is near the center of the bandgap, neither e^o_{p0} nor e^o_{n1} can be assumed negligible. Extrapolation of the curves indicates that the threshold ionization energies of the gold donor and acceptor levels are 0.35 eV and 0.55 eV, respectively.

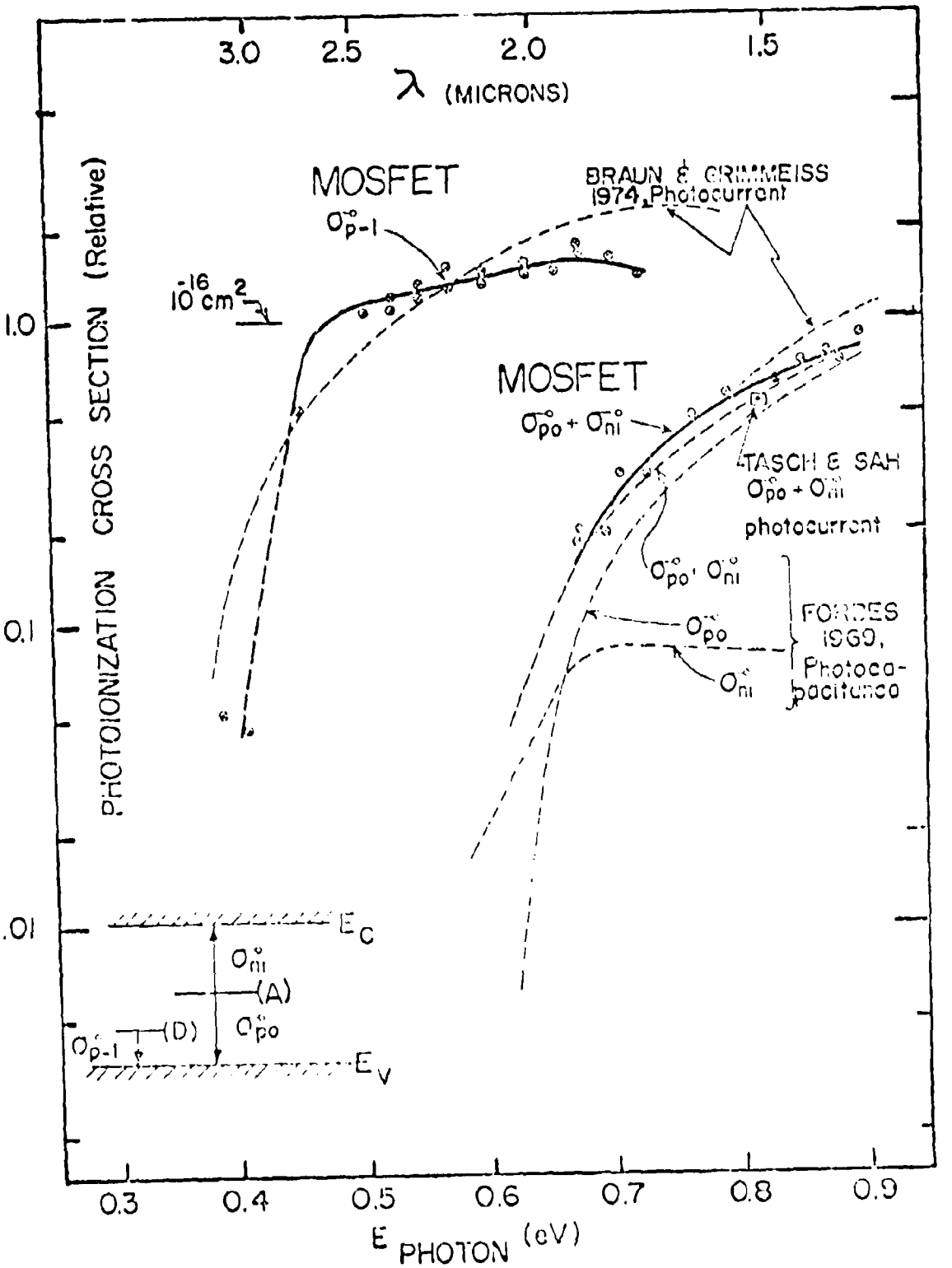


Fig. 5. The photoionization cross section of [illegible]

The normalized results shown in Fig. 5 have been corrected for the spectral characteristics of the monochromator, but our experiment was not calibrated in terms of absolute photon flux. There is considerable difficulty in determining the absolute magnitude of photoionization cross sections because reflections exist within the MOSFET. In fact, large discrepancies in determining optical flux have been reported by several different laboratories that performed identical measurements [13]. The results of our work for gold in the surface depletion region of a MOSFET are compared to the normalized results obtained by other authors [1,14,15] for gold in bulk silicon. A most likely calibration point of $10^{-16} cm^2$ for absolute determinations is indicated. The response of the IRFET to infrared radiation thus is predicted by the photoionization cross sections of gold in silicon.

Knowing the basic MOSFET equations and identifying both the temperature and photon energy dependencies of the gold-center emission rates enables a rather complete mathematical description of the important IRFET characteristics. In Fig. 6, drain current I_{DS} is plotted as a function of gate voltage V_{GS} in the linear region both before and after infrared illumination for a source to drain voltage, V_{DS} = 1.0 V. The theoretical threshold voltage of the device may be found by extrapolating the linear portion of each curve back to an intersection with the gate voltage axis. The intercepts in Fig. 6 are -16.4 V and -14.6 V. According to Eq. (11), $V_{GS} = V_T + V_{DS}/2$ when $I_{DS} = 0$; thus $V_T^i = -16.4 - 1/2 = -16.9$ V, $V_T^f = -14.6 - 0.5 = -15.1$ V, and $\Delta V_T = +1.8$ V.

Most gold-doped devices tested throughout our work exhibited a negative threshold voltage shift. This result contradicts the recent experimental results of Sproul and Nassibian [16] who noted a positive shift of turn-on voltage in gold-doped, n-channel devices and proposed that the gold can remove the fast interface traps of continuous energy distribution and can also add

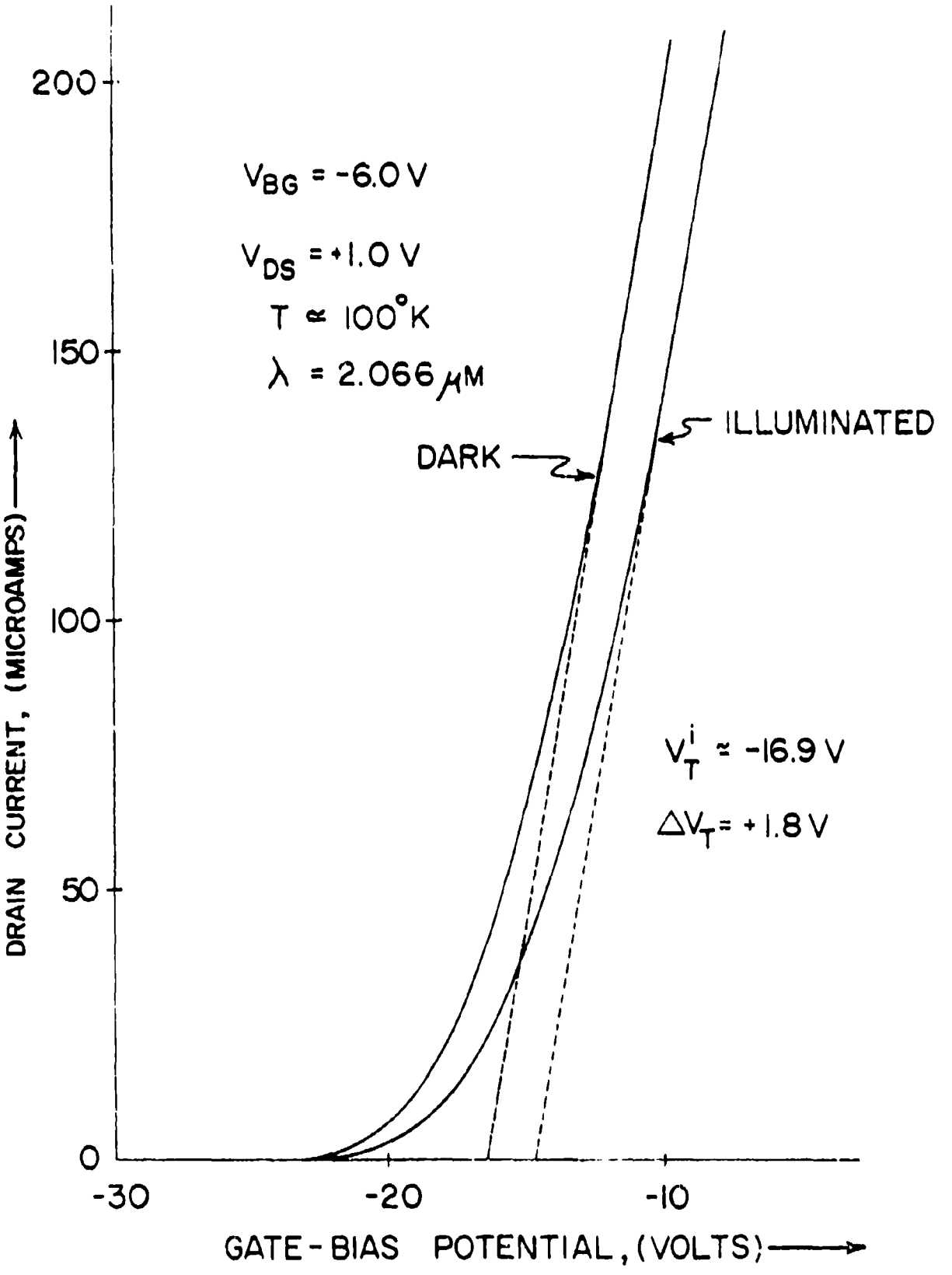


Fig. 6. The determination of IRFL threshold voltage from a plot of drain current versus gate voltage in the linear region before and after illumination.

acceptor interfaces states very close to the valence band edge. Collins et. al [17] suggested that the observed positive shift can also be due to fixed negative gold ions in the oxide very near the oxide-silicon interface. On the other hand, Cagnina and Snow [18] demonstrated the presence of positively charged ions in the oxide near the interface by diffusing gold from the top face through the oxide. When diffusing gold from the silicon side, Brotherton [19] showed, by neutron activation analysis, even higher concentrations of gold in the oxide near the interface than in the silicon. If such concentrations were producing positively charged ions in the gate oxide of the MOSFETs, they would cause a negative shift of threshold voltage as observed in our work. However, a large negative threshold voltage was observed for all our devices both before and after illumination. Such values are inconsistent with (100) orientation, 1- to 2-Ω·cm silicon wafers; therefore, this behavior is possibly due to a high Q_{ss} concentration and/or some sodium contamination during processing. Our MOSFETs were thus depletion-mode devices, but this anomalous result does not affect the outcome of this paper.

If the surface potential $\phi_s = 2\phi_f$ is assumed approximately equal to unity, then Eq. (5) explicitly states that threshold voltage V_T is a function of backgate bias voltage V_{BG} through the term $\sqrt{1 - V_{BG}}$. Differentiating Eqs. (7) and (8) with respect to $\sqrt{1 - V_{BG}}$ gives

$$\frac{dV_T^i}{d\sqrt{1 - V_{BG}}} = C\sqrt{N_A - N_{TT}} \tag{21}$$

and

$$\frac{dV_T^f}{d\sqrt{1 - V_{BG}}} = C\sqrt{N_A}\ , \tag{22}$$

respectively, where $C = B/\sqrt{1 - V_{BG}} = \sqrt{2\kappa_s \varepsilon_o q}/C_o$. Threshold voltage V_T is plotted as a function of $\sqrt{1 - V_{BG}}$ in Fig. 7 for the cases where the IRFET has been preset and all the gold centers are positive ($N_I = N_A - N_{TT}$) before illumination, and where the IRFET has been illuminated and all the gold centers are neutral ($N_I = N_A$). By squaring the ratio of the slopes of the two lines, the ratio of the two effective impurity doping concentrations is given. Thus, from Eqs. (21) and (22),

$$\left[\frac{dV_T^i/d\sqrt{1 - V_{BG}}}{dV_T^f/d\sqrt{1 - V_{BG}}}\right]^2 = \frac{N_A - N_{TT}}{N_A} . \qquad (23)$$

Substituting the values obtained from Fig. 7 into Eq. (23) yields $N_{TT} \approx 0.2\ N_A$. If $N_A = 10^{16}cm^{-3}$, then the gold doping concentration $N_{TT} = 2 \times 10^{15}cm^{-3}$. Furthermore, the oxide thickness x_{ox} is calculated by solving Eq. (22) with the aid of Eq. (3), yielding ≈ 3800 Å. The anticipated maximum change in threshold voltage with $V_{BG} = -6$ V is found now by solving Eq. (9), yielding $\Delta V_T = +1.64$ V. This value is in good agreement with the experimentally observed $\Delta V_T = +1.8$ V (cf. Fig. 6).

B. Model Verification

The experimental I-V characteristics of an IRFET are shown in Fig. 8. By solving Eqs. (11) and (12) for μ_L and μ_S in the linear and saturation regions, respectively, and evaluating at several appropriate points on the curves, an average surface electron mobility of 290 $cm^2/V \cdot sec$ is found. The average μ is used in the device equations to model the IRFET. This result indicates that the effective surface electron mobility in gold-doped n-channel MOSFETs is reduced probably due to additional impurity scattering off the gold sites [20].

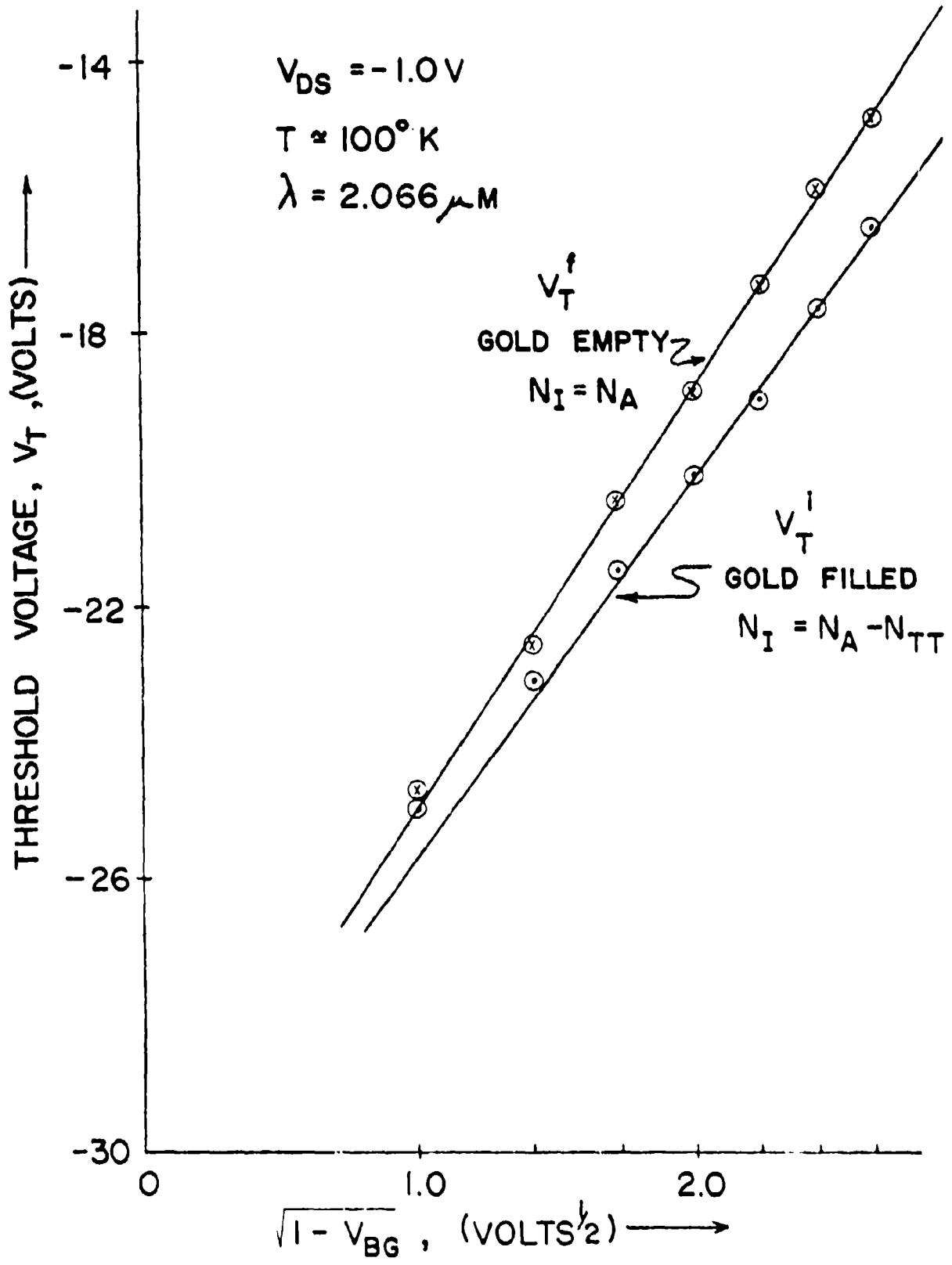


Fig. 7. The dependence of threshold voltage on back-gate bias.

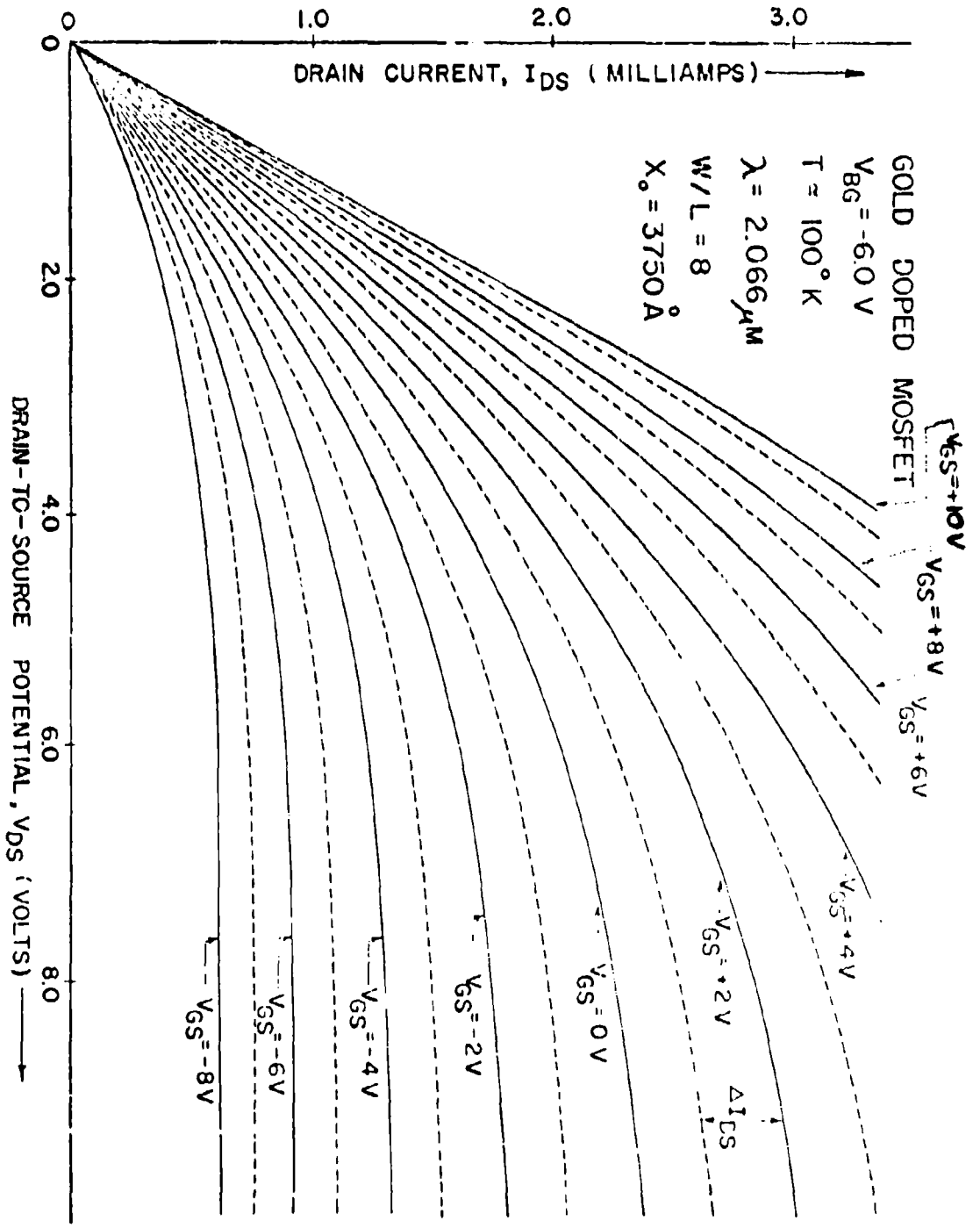


Fig. 8. The I-V characteristics of an IRFET before illumination (solid line) and after illumination (dashed line).

By calculating a set of I-V characteristics and comparing them to experiment, the mathematical model developed in this paper can be shown to describe an IRFET with an accuracy of ±30% under all operating conditions. Surface carrier mobility is not constant, however, and depends on the effective gate voltage $(V_{GS} - V_T)$, as illustrated in Fig. 9. Here the photocurrent, $-\Delta I_{DS}$, is plotted as a function of gate voltage V_{GS} in the linear region. Although the observed characteristics closely follow the functional form of Eq. (13), some decrease is expected near threshold and slight deviation is noted at high effective gate voltages due to field-dependent mobility.

If a set of device equations which more accurately agree with the experimental DC characteristics of Fig. 8 is required, then empirical expressions can be written for mobility and substituted into the fundamental integral of derivation [21]. Also, the simple model makes use of a constant depletion-layer approximation. This assumption of constant Q_B with respect to the gate-bias potential V_{GS} can lead to error in the analysis of MOSFET devices, particularly those operated in the saturation region. A detailed treatment of this second-order effect has been made with the result that the basic device equations are even more extensively modified [22,23]. Fortunately, most IRFET designs can be treated analytically with the model developed in this paper. In Fig. 10, the photocurrent, $-\Delta I_{DS}$, is shown as a function of gate voltage V_{GS} in the saturation region. The curve closely follows the functional form of Eq. (14) with the result that the linear portion of the curve extrapolates to $V_{GS} = V_T^i + V_T/2 = -16$ V when $\Delta I_{DS} = 0$. $\Delta V_T = +1.8$ V, which is again in good agreement with the predicted $\Delta V_T = +1.64$ V. Since the most significant errors are expected in the saturation region of IRFET operation, this result lends much credibility to the simple model.

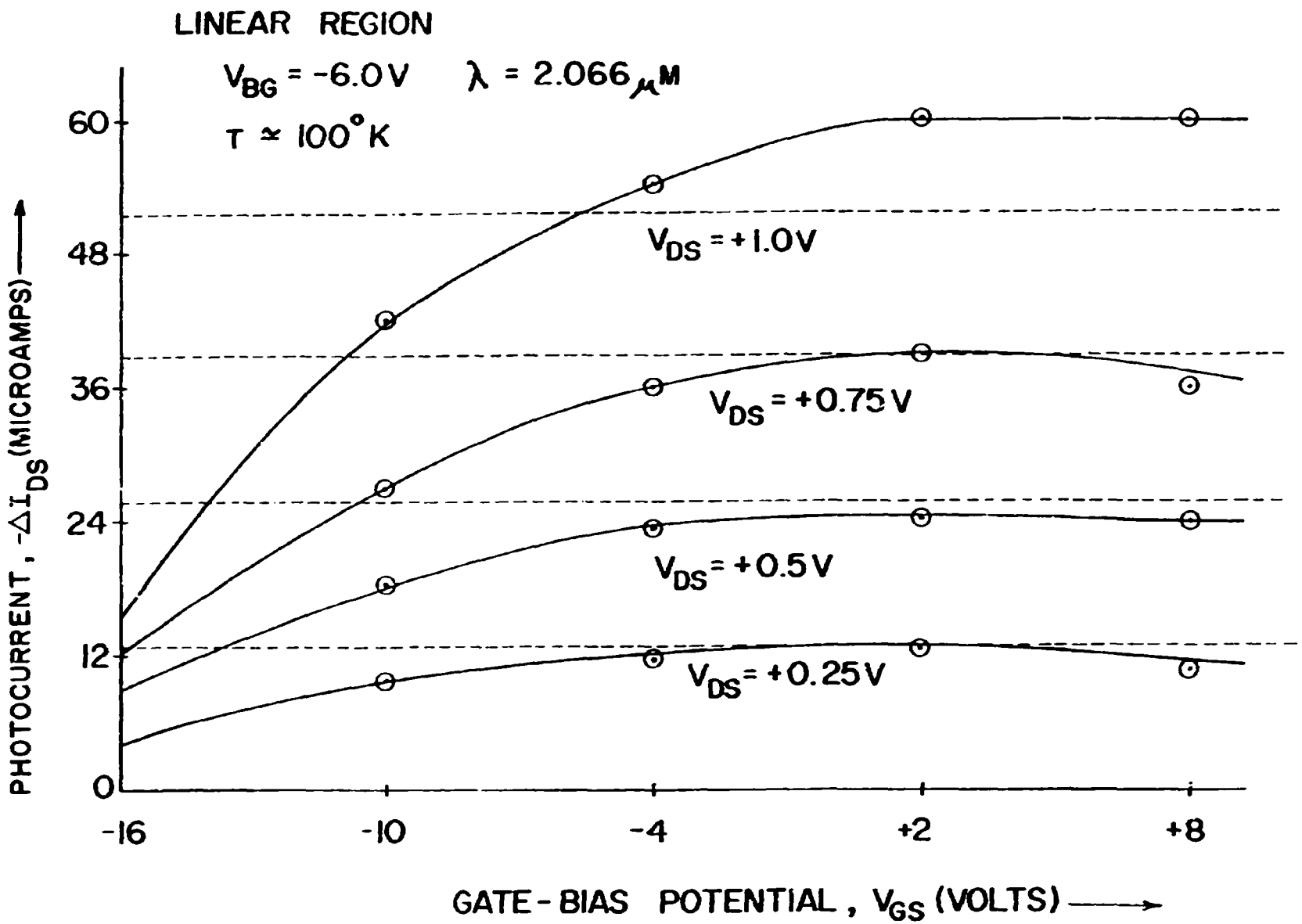


Fig. 9. The photocurrent, $-\Delta I_{DS}$, as a function of gate voltage in the linear region.

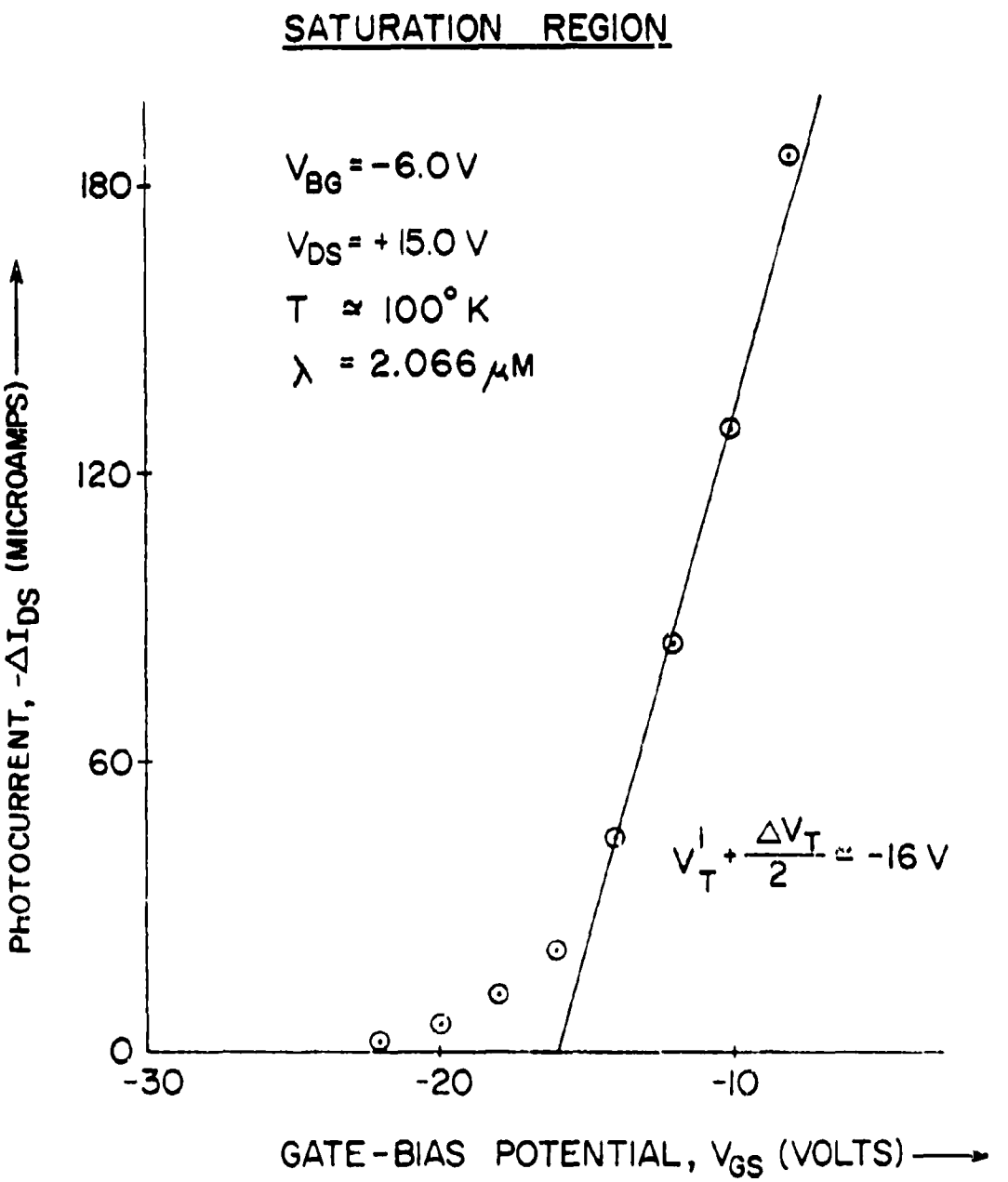


Fig. 10. The determination of the change in threshold voltage, ΔV_T, from a plot of photocurrent versus gate voltage in the saturation region.

C. IRFET Responsivity

The IRFET can be operated in the linear or saturation mode, but to achieve high responsivity it seems most desirable to operate the device in the saturation region where photocurrent, ΔI_{DS} is independent of drain voltage V_{DS}. The time dependence of photocurrent, $\Delta I_{DS}(t)$, in the saturation region is obtained from Eqs. (10) and (14):

$$\Delta I_{DS}(t) = - \beta(V_{GS} - V_T^i)\Delta V_T[1 - \exp(-t/\tau)] \qquad (24)$$

if $\Delta V_T << V_{GS} - V_T$. Also, if the time period t is much less than the time constant τ, then ΔI_{DS} changes linearly with time, or

$$\Delta I_{DS}(t) \simeq \Delta I_{DS\ max} \frac{t}{\tau} , \qquad (25)$$

where $\Delta I_{DS\ max}$ is the maximum static photocurrent at $t = \infty$.

Given that the IRFET integrates the incident infrared signal for a time period $t << \tau$, there will be a total input energy $E_{in} = \Phi_{th}\hbar\omega A$, where $\hbar\omega$ is the average photon energy and A(= WL) is the active area of the device. At the end of the integration period t, the drain-to-source current will have changed an amount $\Delta I_{DS}(t)$. The output power $P_{out} = \Delta I_{DS}(t)\ V_{DS}$, and the output change is permanent until the IRFET is reset. ΔI_{DS} thus can be read for an indefinitely long time. This consideration suggests the following rather unique definition:

$$\text{Responsivity} = \text{Output Power/Input Energy} \qquad (26)$$

An example is given in Fig. 11 where a responsivity of 4mW/nJ has been easily achieved.

$\Delta I_{DS}(t)$ depends on the integration time t, which is much less than τ, the effective gate voltage $V_{GS} - V_T$, which must be less than V_{DS}, and the

IRFET RESPONSIVITY

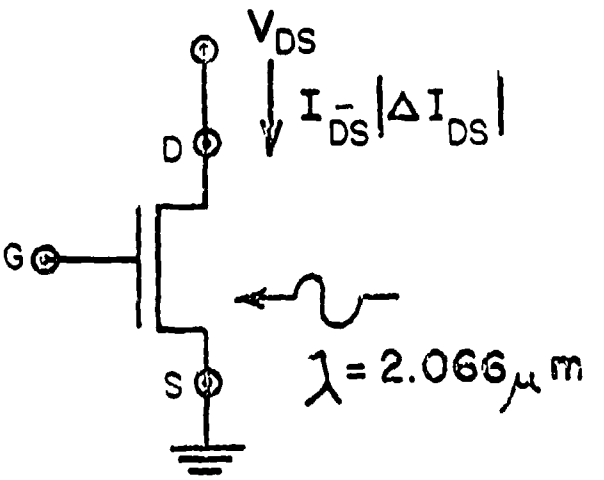
DONOR LEVEL

$T \approx 100^{\circ} K$

$W/L = 8$

AREA $= 2.5 \times 10^{-3}\ cm^2$

$X_o = 4000\ \text{Å}$



INPUT ENERGY

$\sigma^{\circ} = 1.5 \times 10^{-16}\ cm^2$

$\tau = 20$ sec., $\Phi = 3.2 \times 10^{-5}$ Watts/cm^2

$E_{in} = (t = \tau/10) = 1.6 \times 10^{-7}$ Joules

OUTPUT POWER, $t = \tau/10$

$|\Delta I_{DS}| \times V_{DS} = 0.04$ mA x 16 V

$= 0.64$ milli Watts

$$\text{RESPONSIVITY} = \frac{\text{OUTPUT POWER}}{\text{INPUT ENERGY}}$$

$$= \frac{4 \text{ milli Watts}}{\text{micro Joule}}$$

Fig. 11. An example for calculating the responsivity of IRFET.

W/L ratio, which remains constant with decreasing size. Thus $\Delta I_{DS}(t)$ will always be the same for a given photon flux Φ, regardless of the area of the device. Interestingly enough, the output signal power increases directly as the drain voltage V_{DS}, which can be arbitrarily large but less than the reverse-breakdown voltage of the drain junction, while the input signal energy decreases directly as the area (WL). Much higher responsivities are obviously obtainable for smaller devices with the same W/L ratio.

CONCLUSIONS

An analytical model has been developed whereby the gold-doped, infrared-sensing MOSFET (IRFET) can be described with accuracy sufficient for most engineering applications. The experimental results leave little doubt that the energy levels, or threshold ionization energies, and photoionization cross sections of gold in a surface space-charge region correspond to those previously observed in bulk silicon. Furthermore, the IRFET behaves according to previously published design criteria [8]. The infrared-sensing MOSFET has a low quantum efficiency η, i.e., $\eta = \sigma^{o}_{p-1} N_{TT} W_d \approx 1.5(10^{-16})2(10^{15})1.02(10^{-4}) = 3.06 \text{ c } 10^{-5}$, where W_d is the width of the surface depletion region, but has a very high gain G (or ratio of the number of electrons in the external circuit to the number of incident photons, both in the same sample period), e.g., $G = \Delta I_{DS}(t)/(q\Phi A) = 4(10^{-5})/[1.602(10^{-19})3.33(10^{14})2.5(10^{-3})] = 300$ (cf. Fig. 11), when compared to a photoconductive detector [8].

This device is an infrared detector that has some very unique capabilities, namely, a static read-only memory, a negative photoconductivity, an integrating function, and a high responsivity that is limited only by some as yet undetermined noise consideration. In addition, large-scale-integrated detector arrays (with polysilicon gate construction or provisions for backside illumination) should be possible with existing silicon technology.

Determining a suitable noise figure-of-merit and checking device uniformity in array configurations comprise the remaining work to be done with this IRFET. Even though only the near-infrared characteristics of gold-doped IRFET have been investigated in our work so far, there appears to be no reason why response extended through the far-infrared wavelengths, i.e., 3 to 14 μm, is not possible by doping the device with indium or gallium [8].

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APPENDIX B

INDIUM-DOPED DEVICES*

INTRODUCTION

The IRFET [1-5] which operates at low temperatures employs impurity photoionization to modulate its source to drain conductance. An n-channel IRFET is shown in Fig. 1, and is based upon a MOSFET device structure [6,7,8]. The p-type substrate is doped with both indium and a shallow level acceptor, boron. The indium center can exist in two distinctive charge states. The neutral charge state corresponds to the condition when the indium center is occupied by a hole. When the indium center is ionized, the loss of this positive hole to the silicon valence band leaves the indium center in a negative charge state.

The IRFET can be initially preset by turning it off and accumulating the surface. In an n-channel device, this would correspond to the application of a negative voltage to the gate electrode, V_{GS}, which would bend the bands at the silicon surface in such a manner that holes, majority carriers, would accumulate there. The preset operation insures that all of the indium centers capture a hole and thus exist in their neutral charge state.

The IRFET is now "biased on" by the formation of an inversion layer of minority carriers between the source and drain regions and a resulting current flow, I_{DS}, between these regions. For the device under consideration, this corresponds to the application of a gate voltage, V_{GS}, more positive than the threshold voltage, V_T, of the device and a positive drain potential, V_{DS}. As shown in Fig. 1, the application of these voltages produce a surface depletion region within the device. If infrared radiation in the 2.0 to 7.0 micrometer wavelength range now illuminates the device, sufficient energy will be available

*Based on material which has been accepted for publication in the IEEE Trans. on Electron Devices, by L.Forbes, L.L.Wittmer and K.W.Loh.

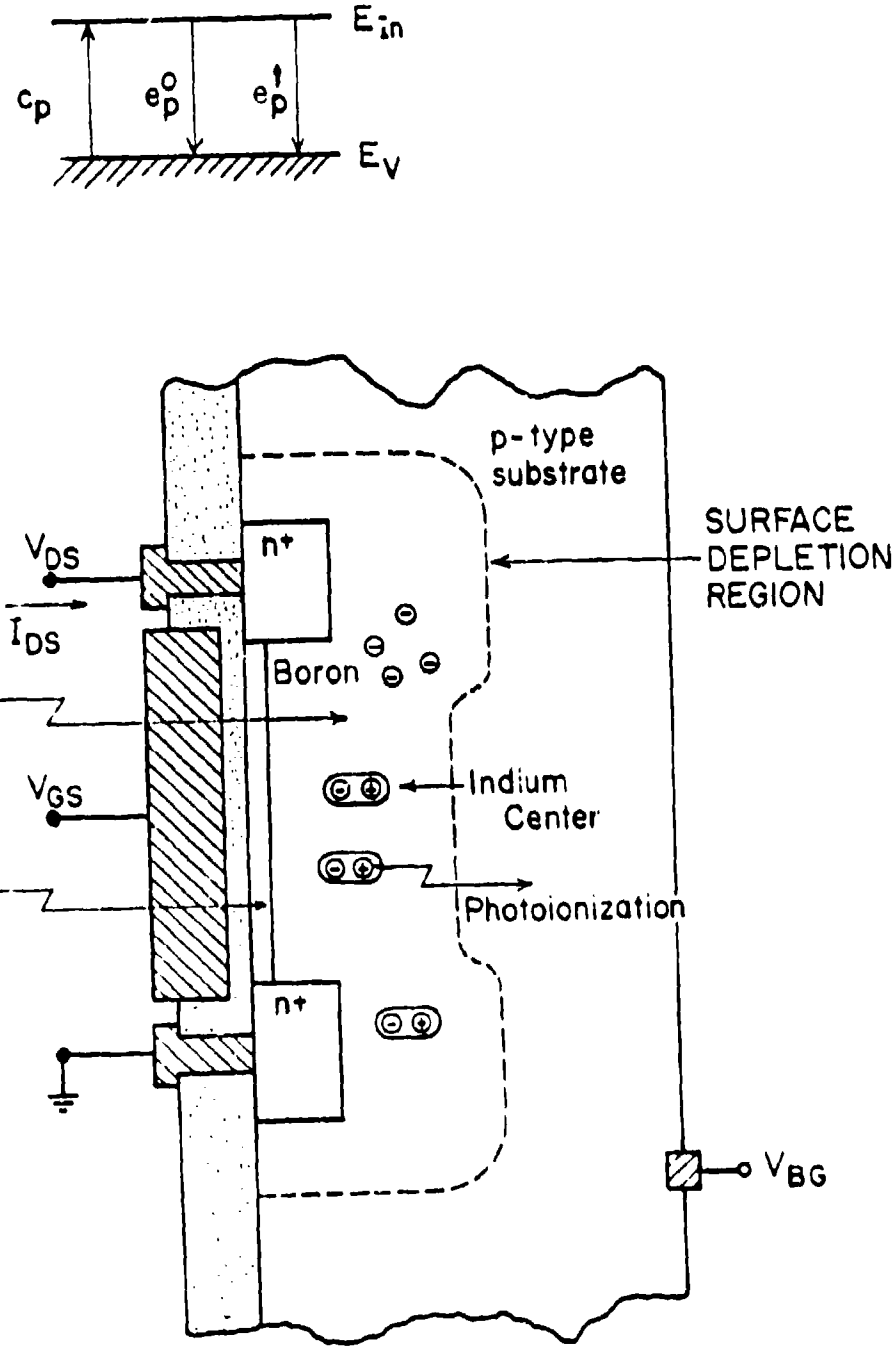


Fig.1. Schematic diagram of the indium-doped MOSFET(IPFET). Q_{CH} denotes the charge contributed by electrons in the surface channel.

to photoionize the indium center by the emission of a hole to the valence band [9,11]. This photoionization process changes the net charge within the surface depletion region to a more negative quantity since the indium centers are being converted from a neutral to a negative charge state. The change in charge state modulates the conductance of the surface inversion channel between source and drain since the conductance is a function of the number of ionized impurity centers, N_I, in the space charge region. Therefore, I_{DS} will be continually changing as the photoionization process progresses up to the point where virtually all of the indium centers are eventually ionized [4,5].

Operation of the indium-doped silicon infrared sensing MOSFET (IRFET) has been previously demonstrated in a short report [5]. This work describes a more detailed characterization of the device for application as an infrared detector which might be particularly useful in the 3 to 5 micrometer wavelength range.

DEVICE EQUATIONS

The two basic operating regions of the MOSFET are the linear and saturation regions. Equations relating drain to source current to drain to source voltage are well known and are found in many solid-state device books [6,7,8]. In the linear region of operation, $V_{GS} - V_T > V_{DS}$, the device equation is expressed as

$$I_{DS} = \beta V_{DS}(V_{GS} - V_T - V_{DS}/2) \qquad (1)$$

where $\beta = \mu C_o W/L$. and where μ is the effective surface electron mobility in an n-channel device and W/L is the geometric width-to-length ratio of the channel. The gate oxide capacitance per unit area, C_o, can be calculated from

$$C_o = \kappa_{ox} \epsilon_o / x_o \qquad (2)$$

where κ_{ox} is the relative dielectric constant of silicon dioxide and x_o is the thickness of the oxide.

In the saturation region of operation, $V_{GS} - V_T \leq V_{DS}$ and $V_{GS} > V_T$, the device equation is expressed as

$$I_{DS} = \beta(V_{GS} - V_T)^2/2. \tag{3}$$

If the final and initial charge states of the indium impurity center are defined as before, an initial and final drain to source current can be expressed as [3]

$$I_{DS}^i = \beta V_{DS}(V_{GS} - V_T^i - V_{DS}/2) \tag{4}$$

and

$$I_{DS}^f = \beta V_{DS}(V_{GS} - V_T^f - V_{DS}/2) \tag{5}$$

in the linear region of operation, where I_{DS}^i and I_{DS}^f correspond to the initial and final values of the drain to source current.

The resulting static change in drain to source current, ΔI_{DS}, may now be found by subtracting Eq. (4) from Eq. (5). Thus

$$\Delta I_{DS} = I_{DS}^f - I_{DS}^i = -\beta(\Delta V_T)V_{DS} \tag{6}$$

where ΔV_T is the maximum change in threshold voltage or $V_T^f - V_T^i$. Following a procedure similar to the above, the static change of drain to source current in the saturation region becomes

$$\Delta I_{DS} = -\beta(\Delta V_T)(V_{GS} - V_T^i - \Delta V_T/2) \ . \tag{7}$$

The negative sign in Eqs. (6) and (7) indicates that I_{DS} decreases in magnitude during photoionization. This result is intuitively reasonable since

the threshold voltage increases as the indium centers ionize and the threshold voltage, V_T, is defined as the applied gate voltage at which drain to source conduction is terminated.

If the IRFET is held at the constant operating temperature, the threshold voltage may be written as [3],

$$V_T = A + B\sqrt{N_I} \ , \tag{8}$$

where $A = V_{FB} + 2\phi_f$, $B = (2\kappa_{Si}\varepsilon_o q(2\phi_f - V_{BG}))^{1/2}/C_o$, $N_I = N_A + N_{In}(t)$, $N_{In}(t)$ is the number of ionized or negative indium centers, and N_A the shallow level acceptor concentration. V_F is the flatband voltage and ϕ_f the fermi potential. If the neutral charge state is defined as the initial condition and the negative charge state as the final condition, the following two expressions may be written:

$$V_T^i = A + B\sqrt{N_A} \tag{9}$$

and

$$V_T^f = A + B\sqrt{N_A + N_{In}} \ , \tag{10}$$

where V_T^i and V_T^f represent the initial and final values of the threshold voltage and N_{In} is the total indium concentration.

The static change in threshold voltage, ΔV_T, can now be determined by subtracting Eq. (9) from Eq. (10):

$$\Delta V_T = V_T^f - V_T^i = B(\sqrt{N_A + N_{In}} - \sqrt{N_A}) \tag{11}$$

If the operating temperature of the IRFET is chosen such that $e_p^o >> e_p^t$ for a given incident photon flux, the increase in threshold voltage given by Eq. (11) will be due only to the photoionization of the indium centers [11]. The indium centers will become negative with respect to time during the photoionization process according to

$$N_{In}(t) = N_{In}[1 - \exp(-t/\tau)] \ , \qquad (12)$$

where in this case τ is $1/e_p^o$. If, on the other hand, thermal emission is dominant, τ is $1/e_p^t$ [11].

An expression which describes the current transients can be obtained by simply replacing V_T by Eq. (8) in Eqs. (1) and (3). Thus

$$I_{DS}^L(t) = \beta V_{DS}(V_{GS} - V_T^i - B(\sqrt{N_A + N_{In}[1 - \exp(-t/\tau)]} - \sqrt{N_A}) - V_{DS}/2) \qquad (13)$$

and

$$I_{DS}^L(t) = (\beta/2)(V_{GS} - V_T^i - B[\sqrt{N_A + N_{In}[1 - \exp(-t/\tau)]} - \sqrt{N_A}])^2. \qquad (14)$$

in the linear and saturation regions, respectively. $I_{DS}^L(t)$ is the drain to source current in the IRFET as a function of illumination time.

The type of decay that I_{DS} will exhibit can be more clearly seen if we expand the square in Eq. (14). Thus

$$I_{DS}^L(t) = (\beta/2)[F^2 - 2FB\sqrt{N_A + N_{In}(t)} + 2FB\sqrt{N_A} + B^2N_A + B^2[N_A + N_{In}(t)] - 2B^2\sqrt{N_A}\sqrt{N_A + N_{In}(t)}] \qquad (15)$$

where $F = V_{GS} - V_T^i$ and $N_{In}(t)$ is given by Eq. (12).

In experimentally characterizing the device, this report will primarily treat the saturation region of operation which corresponds to the most desirable mode of operation due to the higher responsivity and lack of dependence of the photocurrent on drain to source voltage.

DEVICE FABRICATION AND MEASUREMENT TECHNIQUES

The n-channel MOSFETs were fabricated upon 3 to 5 ohm-cm indium-doped silicon wafers obtained from General Diode Corporation, Framingham, Massachusetts. The n^+ source and drain regions were formed by a phosphorous diffusion from a

5 x $10^{20}/cm^3$ "spin-on" source. A three mask process was employed in the fabrication which resulted in the gate oxide being the same thickness as the field oxide. The gate oxides of the experimental devices were approximately 5400 Å thick and the channels had a width to length ratio of 9.32 in a circular geometry. The oxide thickness was verified by measuring the gate capacitance on a Boonton Capacitance Meter.

The IRFET, which is mounted on a TO-5 header, was soldered into a copper sample holder in order to assure good thermal conductivity. This sample holder, which for thermal measurements completely encompassed the IRFET, was then attached to a model AC-2-110, open cycle, cryo-tip refrigerator manufactured by Air Products and Chemicals, Inc. The cryogenic refrigerator incorporates a Joule-Thomson type refrigerator which uses compressed nitrogen and hydrogen as the refrigerant. A radiation shield, which is cooled to 78°K, surrounds the device and coldfinger. A stainless steel shroud is then fitted over this assembly and a vacuum of 2 x 10^{-5} torr is maintained within the shroud in order to thermally isolate the coldfinger from the outside world. Temperature control is achieved by varying the hydrogen pressure at the inlet of the refrigerator.

The operating temperature of the IRFET was determined by monitoring the resistance of a calibrated Cryogenic Platinum Resistor obtained from Weed Instrument Company, Inc.

For optical measurements, a Carborundum Gas Igniter, or Globar, was chosen as the source of infrared radiation. The "Globar Source" was operated with a 110 volt input and reached an operating temperature of 1500°C. The temperature of the globar was determined with an Ircon Radiation Thermometer. The globar is an approximate "blackbody source".

Circular variable filters (CVFs) were employed to produce the monochromatic infrared photon flux. These filters, obtained from Optical Coating Laboratories, Inc., are optical interference coatings, vacuum deposited on circular substrates. The spectral location may then be varied by physical rotation. The two 90° segments which were used in the experiment covered the wavelength range from 2.5 to 8.0 micrometers, have possible half-bandwidths less than 1.35% and have transmission for wavelengths outside of the pass-band of less than or equal to .1%.

In the optical experiments, the IRFET was mounted so that it could be illuminated with infrared radiation from the back-side. This was accomplished by drilling a 1/16 inch hole through the center of the TO-5 header before the IRFET was mounted. A pictoral representation of the optical apparatus is shown in Fig. 2. The CVF was rotated behind a 2 mm slit with the angle of rotation factory calibrated in terms of center wavelength. IRTRAN II, supplied by Eastman Kodak, served as the outer shroud window of the cryo-tip refrigerator.

EXPERIMENTAL RESULTS

The photocurrent in the saturation region of operation is shown plotted as a function of gate voltage in Fig. 3. This plot follows closely the functional form of Eq. (7). The linear portion of the curve is shown extrapolated to $V_{GS} = V_T^i + \Delta V_T/2 = 25$ volts when $\Delta I_{DS} = 0$. According to Eq. (3), V_T^i in the saturation region can be found from a plot of $(I_{DS}^i)^{1/2}$ versus V_{GS} where the V_{GS} axis intercept directly yields V_T^i. Such a plot results in $V_T^i = 19$ volts. Therefore, $\Delta V_T = 2(25-19) = 12$ volts.

The values obtained for V_T^i and V_T^f vary somewhat depending upon whether they were calculated in the linear or saturation regions. This is probably

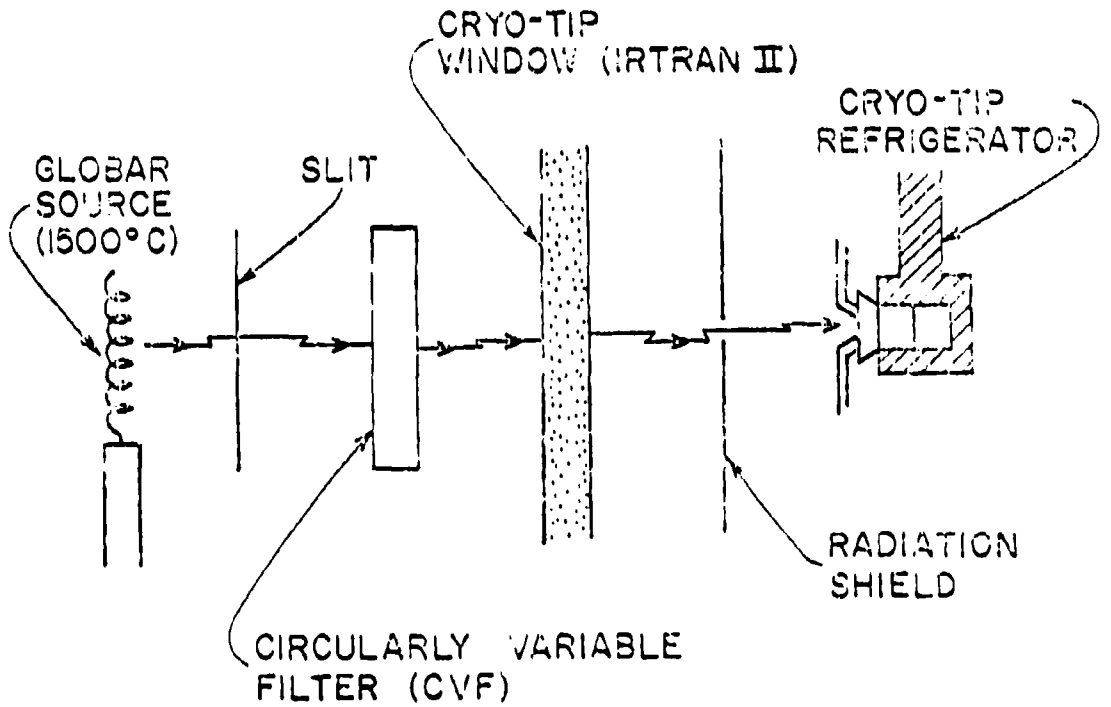


Fig. 2. The infrared source and optics employed in the optical characterization.

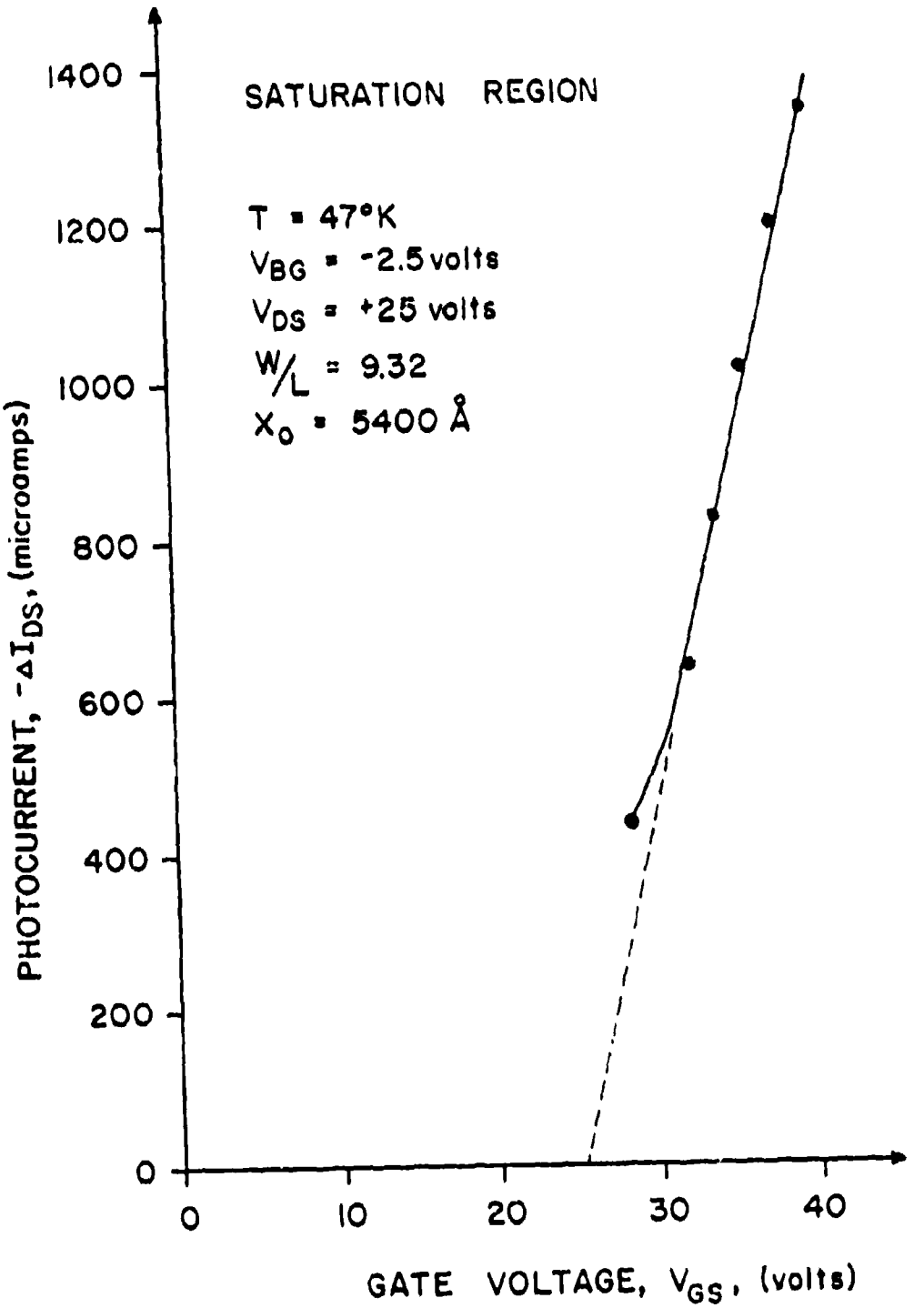


Fig.3. The photocurrent, $-\Delta I_{DS}$, as a function of gate voltage in the saturation region.

due to the fact that the simple model developed makes use of a constant depletion-layer width approximation.

In order to calculate the theoretical change in threshold voltage, Eq. (11) requires a knowledge of the doping concentrations of indium and the residual boron impurities. If the surface potential, $\phi_s = 2\phi_f$, is assumed to be approximately equal to 1 Volt, Eq. (8) states that V_T is a function of V_{BG} through the term $(1 - V_{BG})^{1/2}$. Differentiating Eqs. (9) and (10) with respect to $(1 - V_{BG})^{1/2}$ yields

$$\frac{dV_T^i}{d[(1 - V_{BG})^{1/2}]} = C(N_A)^{1/2} \tag{16}$$

and

$$\frac{dV_T^f}{d[(1 - V_{BG})^{1/2}]} = C(N_A + N_{In})^{1/2} \tag{17}$$

respectively, where $C = (2\kappa_{Si}\varepsilon_o q)^{1/2}/C_o$.

In Fig. 4 a plot of V_T versus $(1 - V_{BG})^{1/2}$ has been made for the cases where the indium centers are neutral (dashed line) and negative (solid line). From an examination of Eqs. (16) and (17), the effective dopings for both charge states can be determined from the slopes of the lines in Fig. 4. Utilizing an oxide thickness of 5400 Å it was determined that $N_A + N_{In} = 8.92 \times 10^{15}/cm^3$ and $N_A = 4.95 \times 10^{14}/cm^3$. Then, with an applied back-gate bias of -2.5 volts, Eq. (11) becomes ΔV_T 1.66 x $10^{-7}(\sqrt{N_A + N_{IN}} - \sqrt{N_A}$ 12.02 volts. This result matches the experimental value of ΔV_T determined in the saturation region almost identically. Note in this case, $N_{In} > N_A$, or the indium impurity concentration exceeds the shallow level acceptor concentration, N_A. The simplifying assumption $N_{TT} \ll N_A$ used previously [1,2,3] cannot be applied in the analysis of device operation to be presented here.

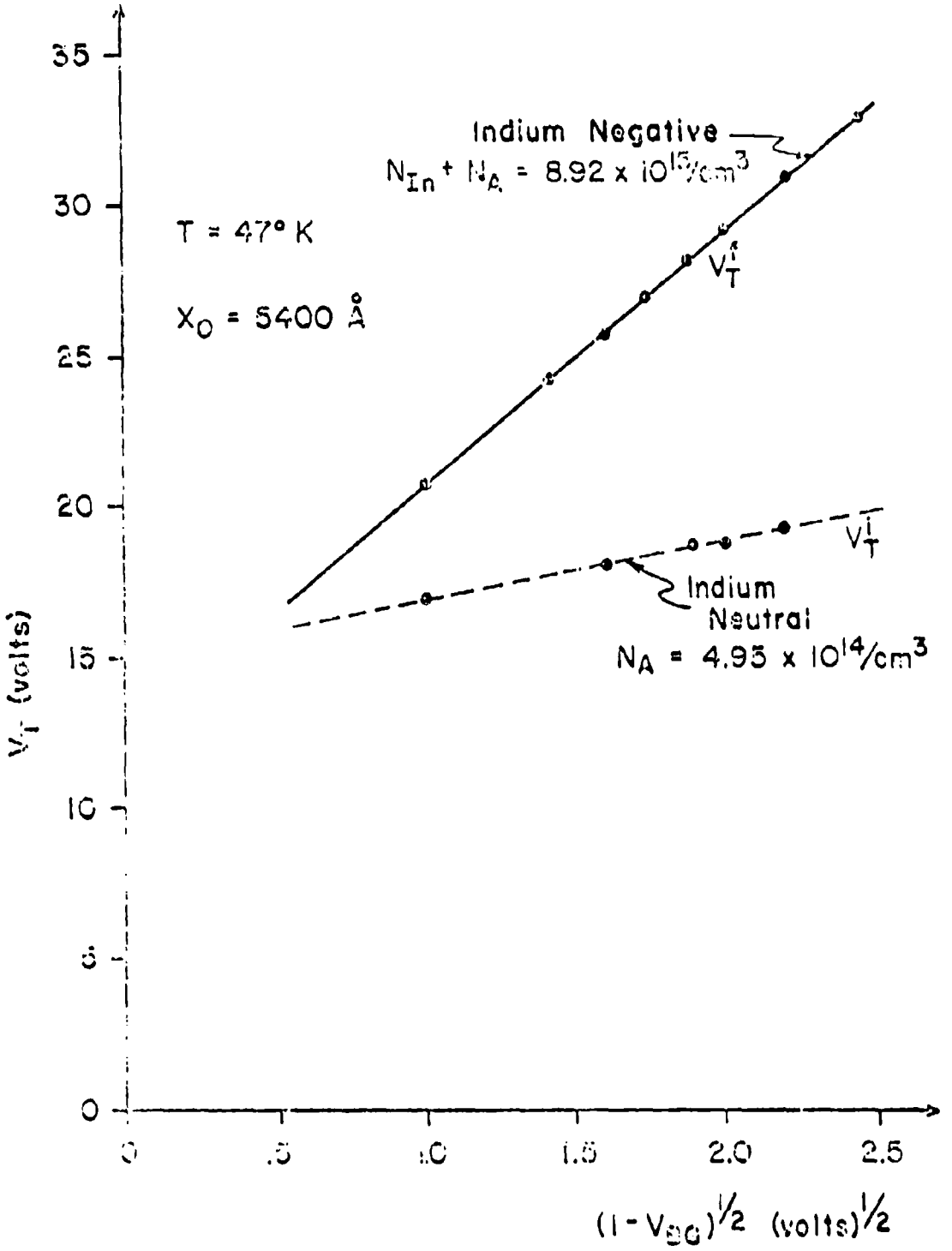


Fig.4. The dependence of threshold voltage on back-gate bias.

A typical plot of I_{DS} in the saturation region versus time as a result of the thermal decay of the indium impurity centers is shown in Fig. 5. At a time before t = 0, an accumulation voltage was applied to the IRFET to insure that all of the indium centers would be in their initial neutral charge state.

A careful study of the resulting curve revealed that $I_{DS}(t)$ obeyed a nearly perfect exponential decay for $t \lesssim \tau_{I_{DS}}$ where $\tau_{I_{DS}}$ represents the time constant of the $I_{DS}(t)$ decay. Therefore, for the sake of experimental convenience $I_{DS}(t)$ was approximated by

$$I_{DS}(t) = S \exp(-t/\tau_{I_{DS}}) + T \tag{18}$$

where $T = I_{DS}(\infty)$ and $S + T = I_{DS}(0)$. The time constant of the current decay can then be determined by noting the time at which $I_{DS}(t)$ has reached a value of exp(-1) of the difference between its maximum and $I_{DS}(\infty)$.

In order to determine the time constant of the indium decay, Eq. (15) can be utilized to solve for τ for a given plot of $I_{DS}(t)$. The IRFETs which were employed in the experimental measurements, had the following representative parameters, t_{ox} = 5400 Å, $2\phi_f \simeq 1.0$, V_{BG} = -3 volts, V_T^i = +19 volts, V_{GS} = +26 volts, $N_A = 4.95 \times 10^{14}/cm^3$, and $N_{In}(\infty) = 8.425 \times 10^{15}/cm^3$, at an operating temperature of 52°K. By employing these parameters, F = 7, $B = 1.78 \times 10^{-7}$, and $\beta = 6.82 \times 10^{-6}$. Incorporating these constants in Eq. (15) yields the relationships

$$I_{DS}(t) = 4.63 \times 10^{-4} + 9.1 \times 10^{-4}[1-\exp(-t/\tau)] - 1.26 \times 10^{-3}[1-.945\exp(-t/\tau)]^{1/2} \tag{19}$$

Eq. (19), which will be utilized in interpreting the experimental data, is valid between $0 < t/\tau \leq .496$ since $V_{GS} < V_T$ at $t/\tau \geq .496$. However, since

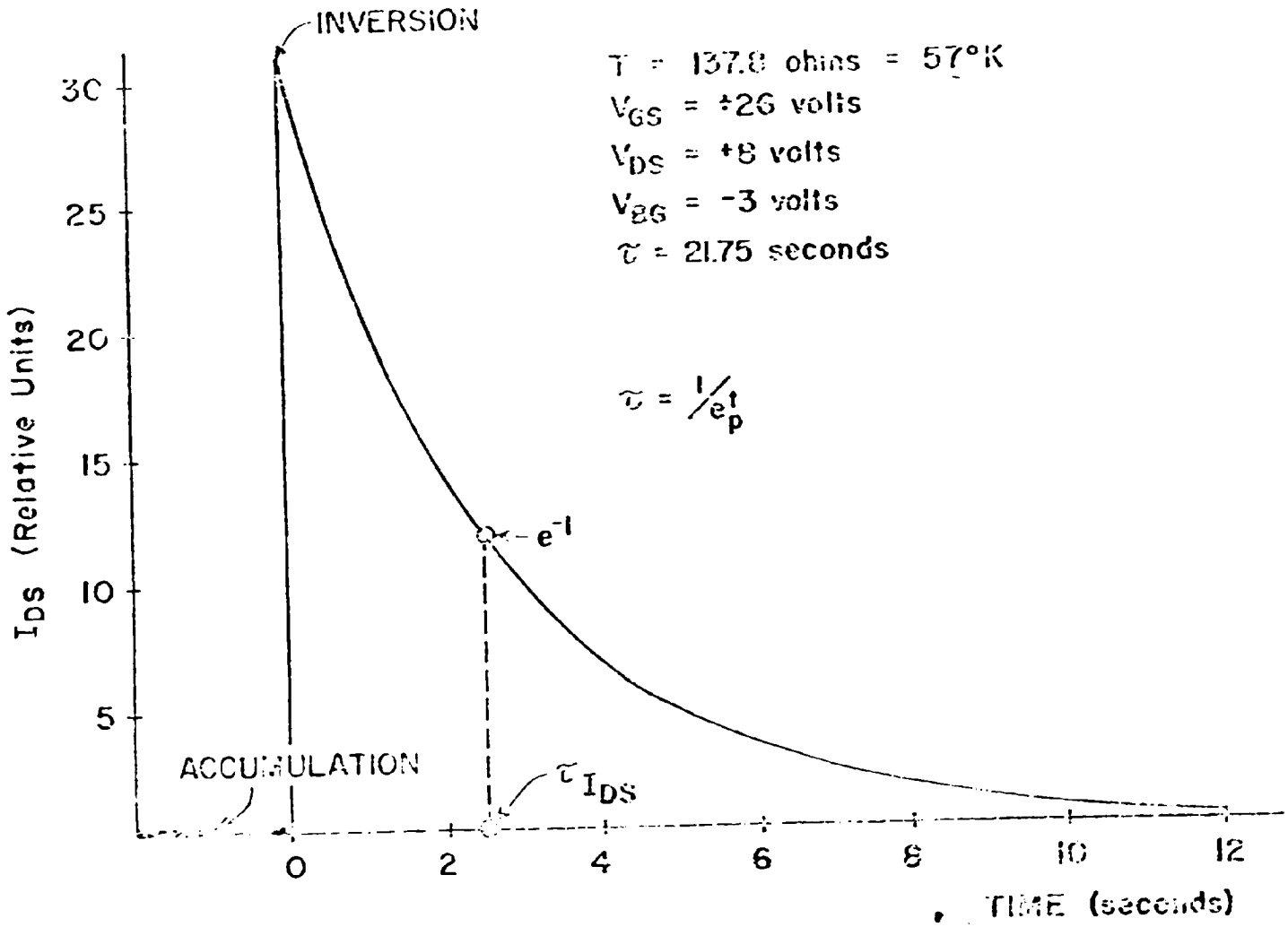


Fig.5. The drain current decay as a function of time due to the thermal excitation of the indium centers.

an experimental observation of $I_{DS}(t)$ was found to be approximated by Eq. (18), a relationship is suggested between $\tau_{I_{DS}}$ in Eq. (18) and τ, the time constant of the indium decay, in Eq. (19). This relationship may be expressed as

$$1/\tau = \alpha/\tau_{I_{DS}} \tag{20}$$

where

$$S \exp(-t/\tau_{I_{DS}}) + T \simeq 4.63 \times 10^{-4} + 9.1 \times 10^{-4}[1-\exp(-\alpha t/\tau_{I_{DS}})] - 1.26 \times 10^{-3}[1-.945\exp(-\alpha t/\tau_{I_{DS}})]^{1/2} , \tag{21}$$

and where α is a constant. The constants S and T, which were defined in Eq. (18), were evaluated assuming the same initial and final values of $I_{DS}(t)$ as given by Eq. (19). A computer numerical integration routine was then employed to find an α such that the mean square error between the two functions in Eq. (21) would be minimized for $t/\tau \leq .496$, the limiting value for which Eq. (19) is valid. The resulting α which makes Eq. (21) true, was found to be .11446. Therefore, Eq. (20) becomes

$$\tau \simeq 8.7\tau_{I_{DS}} . \tag{22}$$

Within the integration limits which were employed, this value of α matched the two expressions in Eq. (21) with an error of less than 2%.

The indium decay time constant may now be obtained by determining $\tau_{I_{DS}}$ from a plot of $I_{DS}(t)$, as in Fig. 5, and by the use of Eq. (22). This procedure was carried out for different temperatures of operation. The resulting time constants were then plotted on a log scale versus 1000/T(°K) as shown in Fig. 6. This difference in the time constant of the current decay, $\tau_{I_{DS}}$, and the time constant of the change in indium charge state ,

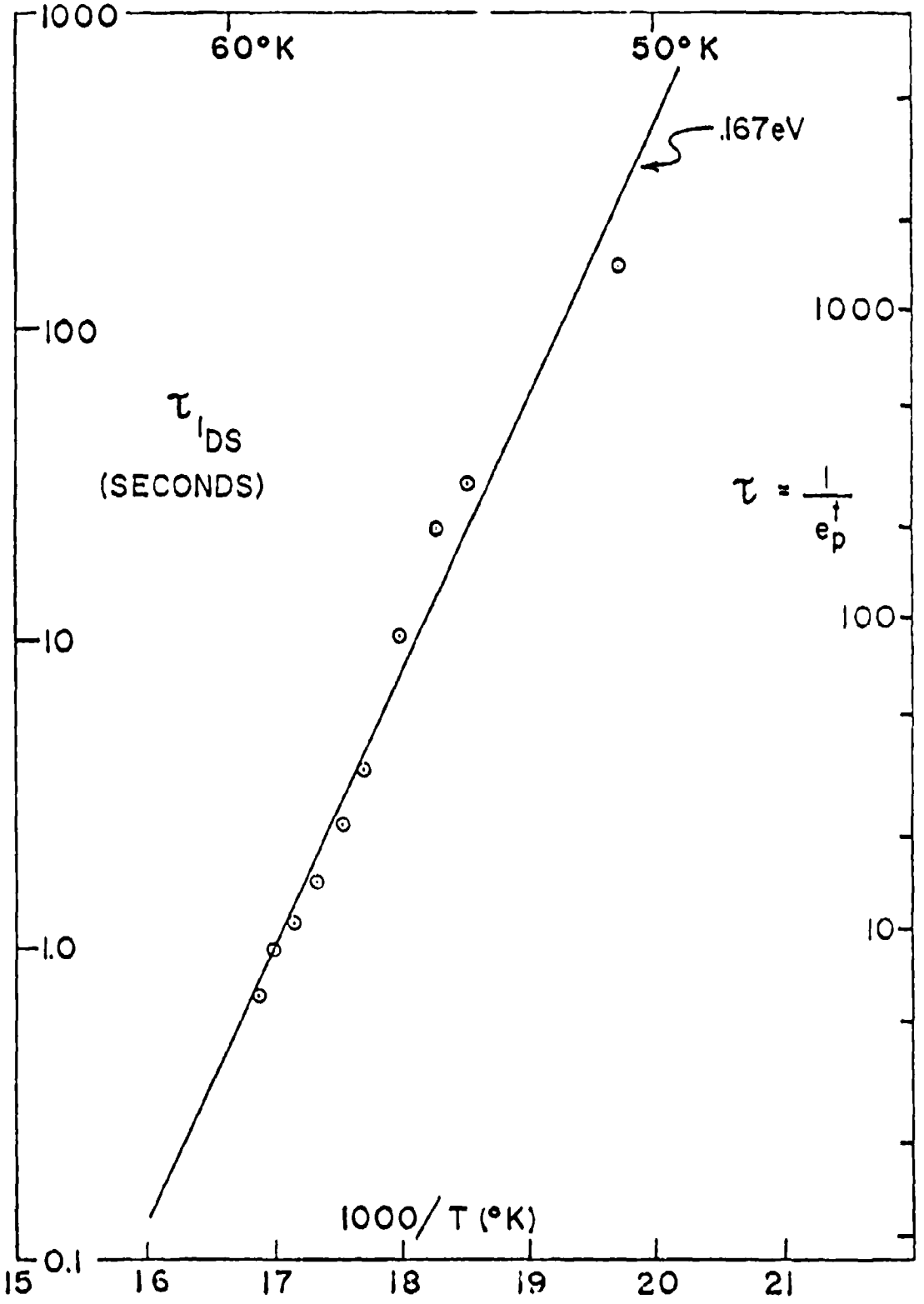


Fig.6. The thermal time constant for hole emission from the indium accepter level for various temperatures as determined in the IRFET.

was incorrectly leftout in previous reports [4,5], the time constant shown there for indium-doped devices with $N_{In} >> N_A$ is $\tau_{I_{DS}}$ not τ.

It has been determined that the time constant associated with the ionization of an impurity level can be expressed as [9,11]

$$\tau = A_1 T^{-1.5} \exp(\Delta E/kT) , \qquad (23)$$

where A_1 is a constant, ΔE represents the location of the impurity level with respect to the valence band, k is Boltzmann's constant, and T is the temperature in degrees Kelvin. A straight line drawn through the data points employing a least mean square error technique then allows a calculation of the ionization energy, ΔE, of indium in silicon,

$$\Delta E = \frac{\Delta \log_e \tau + 1.5 \Delta \log_e T}{11.6047 \Delta (1000/T)} = 0.167 eV . \qquad (24)$$

This value corresponds to the value obtained by other techniques for the energy level of indium in silicon [12-17].

An operating temperature less than 45°K was chosen for the optical measurements so that the thermal emission rate would be very small. With the globar on, a -40 to +40 volt square wave was applied to the gate electrode which caused the silicon surface to alternate between strong accumulation and strong inversion, respectively. As in the thermal measurements, V_{DS} was chosen such that the transistor would be operating in the saturation region during inversion and I_{DS} was monitored. A typical resulting trace is shown in Fig. 7.

The illuminated decay of I_{DS} is caused by two separate hole emission processes; the optical hole emission initiated by the incident 1500°C photon flux, e_p^o, and the optical hole emission initiated by the 25°C "Background" flux incident upon the device, e_R^o. The IRFET is an integrating detector and

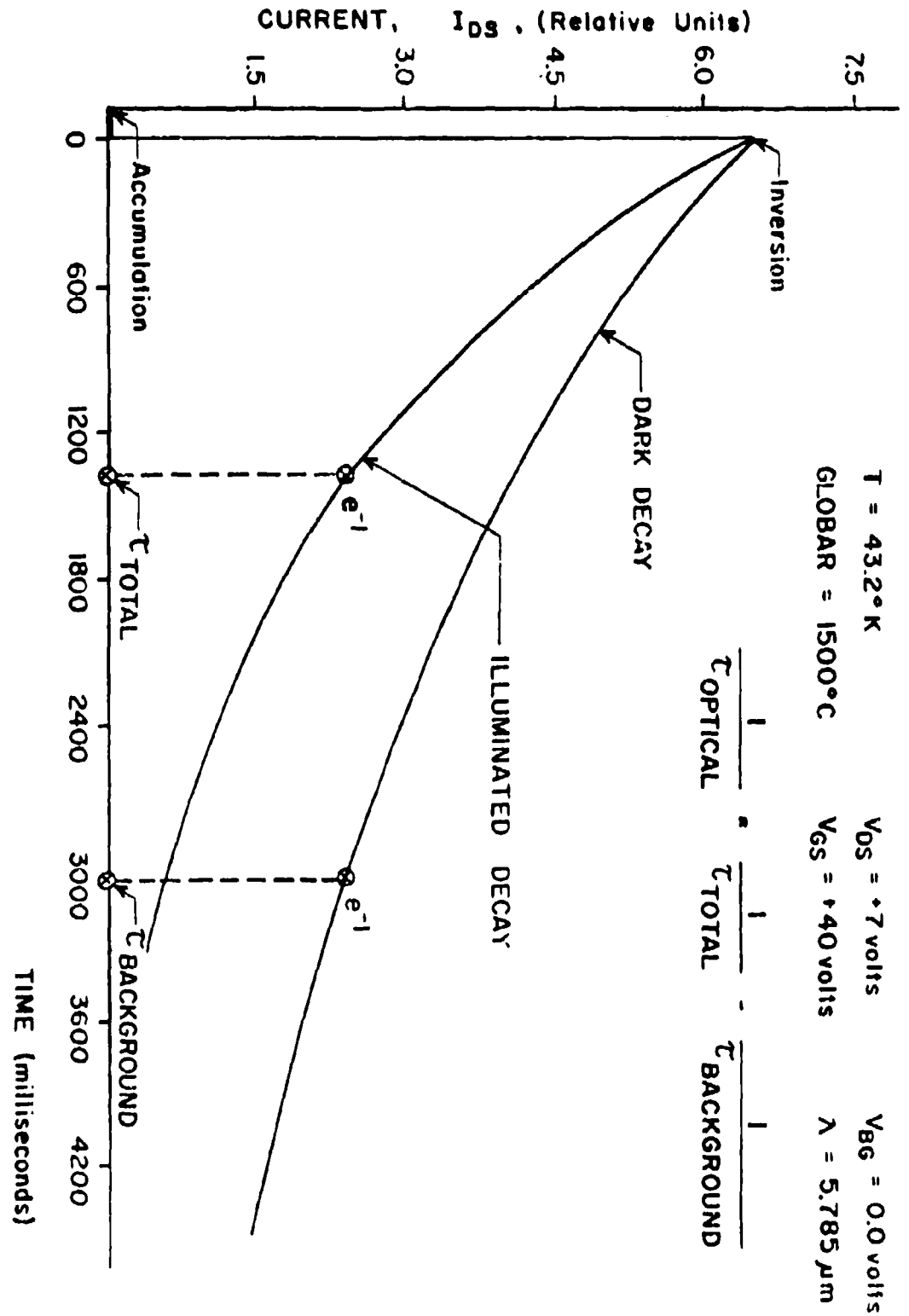


Fig . 7. The drain to source current decay versus time as a result of optical hole emission.

integrates the background flux in the wavelength range out to 8 micrometers as well as the monochromatic signal from the 1500°C source passing through the filter. The total hole emission rate, e_p, for the illuminated decay can now be expressed as [11]

$$e_p = e_p^o + e_B^o \quad . \tag{25}$$

Recalling that $\tau = 1/e_p$, the following expression may be written for $1/\tau_p^o$;

$$1/\tau_p^o = 1/\tau_p - 1/\tau_B^o \quad . \tag{26}$$

With the use of Eq. (26) and Fig. 7, the photoionization cross section can be determined. The results shown in Fig. 8 have been corrected for the spectral characteristics of the globar, transmission of the CVF, and the bandwidth of the CVF, but the experiment was not calibrated in terms of absolute photon flux. Considerable difficulty exists in determining the absolute magnitude of photon flux due to the reflections which exist within the IRFET [3]. The photoionization cross section determined by other authors [16] from measurements on an indium-doped photoconductor is also shown in Fig. 8. In Fig. 8 it can be seen that the general shapes of the curves are similar for both segments 1 and 2 of the CVF. The photoionization cross section of indium in silicon [12-16] thus determines the response of the IRFET to incident infrared radiation.

When Eq. (26) was used to calculate the photoionization cross section, $\tau_{I_{DS}}$, not τ, was the parameter employed. However, since the presented data is in terms of a normalized photoionization cross section, the constant of proportionality which exists between $\tau_{I_{DS}}$ and τ will have no effect upon a normalized representation.

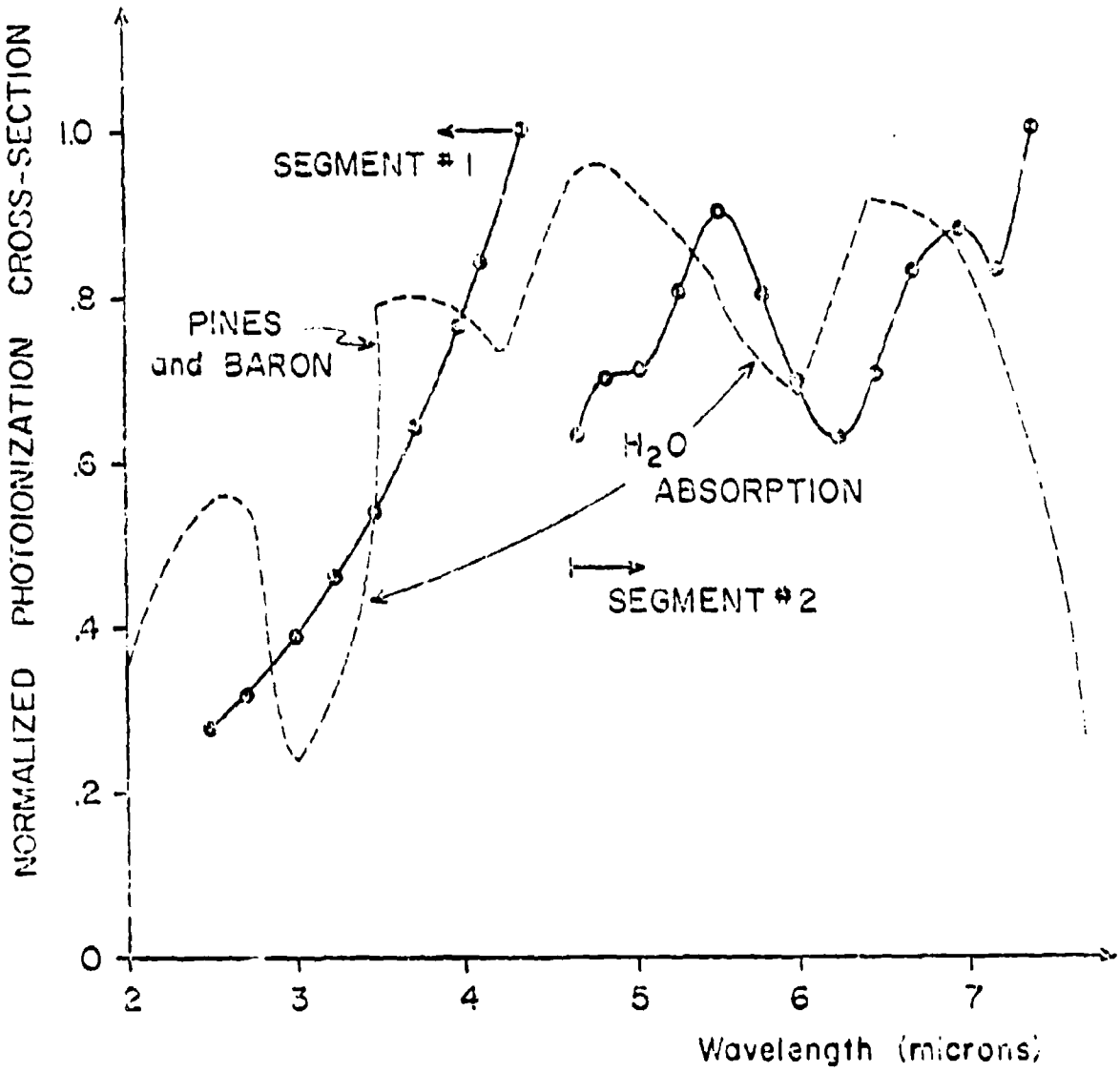


Fig. 8. The experimentally determined photoinzation cross section of indium in silicon (solid line) superimposed upon the result of Pines and Baron [16].

In order to achieve a high responsivity, the IRFET should be operated in the saturation region where the photocurrent, ΔI_{DS}, is independent of the drain to source voltage. Since the IRFET integrates the incident infrared photon flux, an expression for the incident input energy, E_{in}, becomes

$$E_{in} = \phi t h\nu A \ , \tag{27}$$

where t is the length of the integration period, A is the active area of the device, ϕ is the photon flux and $h\nu$ is the photon energy.

At the end of an integration period the drain to source current will have changed by an amount equal to $\Delta I_{DS}(t)$. The fact that $\Delta I_{DS}(t)$ will remain constant until reset and thus can be "read" for an indefinitely long period of time following integration allows the following definition of IRFET responsivity to be proposed [3]:

$$\text{RESPONSIVITY} = \frac{\text{Photocurrent}}{\text{Input Energy}} \tag{28}$$

An example of calculating the responsivity of an IRFET is shown in Fig. 9 [3]. The photoionization cross section of indium at 2.066 μm was taken to be 8.4×10^{-7} cm^2 [12,13,14]. In doing so we have used the results of Bebb and Chapman [13] for the photoionization cross section rather than the smaller value reported by Messenger and Blakemore [15]. The incident photon flux was then determined from the time constant of the optical decay and photoionization cross section as follows:

$$\phi_{inp} = \frac{h\nu}{\tau_{opt}\sigma} = \frac{h(2.998\times10^{8})/(2.066\times10^{-6})}{(8.7\times3.35)(8.4\times10^{-17})} =$$

$$\phi_{inp} = 3.93 \times 10^{-5} \text{ watts/cm}^2 \ , \ \phi = 4.09 \times 10^{14}/\text{cm}^2\text{sec} \tag{29}$$

Values of around 4.8 milliamps/microjoule were obtained for the responsivity. Much higher responsivities are expected at

IRFET RESPONSIVITY

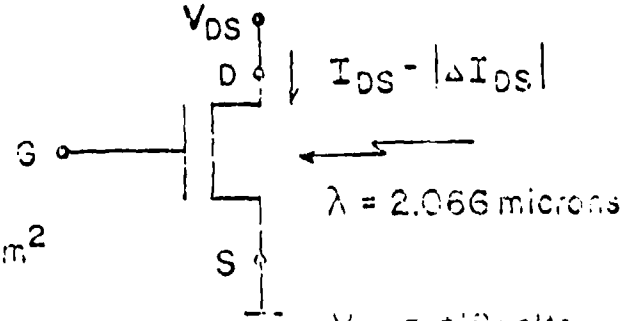
INDIUM DOPED

$T = 42°K$

$W/L = 9.32$

$AREA = 1.362 \times 10^{-2}\ cm^2$

$X_o = 5400\ Å$



$V_{DS} = +16$ volts

$V_{BG} = -3$ volts

$V_{GS} = +26$ volts

INPUT ENERGY AND POWER

$\sigma^\circ = 8.4 \times 10^{-17}\ cm^2$

$\tau^\circ_{DS} = 3.35$ sec, $\bar{\eta} = 4.09 \times 10^{14}\ /cm^2\ sec$

$P = 5.05 \times 10^{-7}$ watts

$E_{in}\ (\tau = \tau^\circ_{DS}/10) = 1.79 \times 10^{-7}$ Joules

CHANGE IN OUTPUT CURRENT $t \cong \tau^\circ_{DS}/10$

$|\Delta I_{DS}| = .86$ mA

$$\text{RESPONSIVITY} = \frac{\text{PHOTOCURRENT}}{\text{INPUT ENERGY}}$$

$$= \frac{4.8 \text{ milliamps}}{\text{microjoule}}$$

Fig. 9. An example for calculating the responsivity of an indium-doped IRFET.

longer wavelengths since the magnitude of the photoionization cross section peaks at approximately 4.6 micrometers. In addition, since the photocurrent depends, in saturation, only upon the integration time, the effective gate voltage, and the W/L ratio, it will always be the same for a given incident photon flux. Therefore, much higher responsivity can be obtained for smaller devices with a constant W/L ratio since the input energy (or input power) decreases as the area (W·L) decreases.

APPLICATION CONSIDERATIONS

Operating temperatures of less than 50°K are required to insure the thermal emission rate of the indium center is orders of magnitude smaller than the optical emission rate when the device is employed as an infrared detector. The lower limit on the temperature of operation is determined by the boron concentration in the substrate and the requirement that sufficient holes are present in the substrate to insure a fast reset operation where $t_{reset} = 1/(c_p p)$ and, c_p, is the capture coefficient of the indium center and, p, the hold concentration [11,9]. For the devices described here, $N_{In} \cdot N_A$, however, while deionization of the indium in the substrate was almost complete, sufficient boron ionization exists such that the reset time in the 20°K to 50 K range was in the microsecond or sub-microsecond time scale and could not be conveniently determined.

Much higher responsivities could be achieved with small area devices, on the other hand, it has been shown that under shot noise or background limited operation the maximum obtainable signal to noise ratio depends only on the surface charge storage density or total number of indium centers ionized in each device. $S/N = (N_{In} W_d A/2)^{1/2}$, where W_d is the depletion region width and A the area [18]. Small areas result in small S/N ratios. In the

case of gold-doped devices operating at 78°K it has been found that shot noise or background limited rather than 1/f noise limited operation can be achieved for integration of less than 10 seconds [18]. The dependence of the maximum obtainable signal to noise ratio on the square root of the total number of stored charges is a common characteristic of all integrating semiconductor infrared detectors and applies equally as well to the CCD scanned photoconductor arrays where the charge is integrated and stored in CCD potential wells [16, 19,20,21]. Since the amount of charge which can be stored in any type of MOS surface device whether MOSFET or CCD is of the same order of magnitude, the selection of the particular type of infrared detector should be made on the basis of other considerations.

CONCLUSIONS

The characteristics of the indium-doped silicon infrared sensing MOSFET (IRFET) operating in the saturation region have been investigated and described in some detail. Again it has been found that the device operation can be described on the basis of a simple model [1] and that the results obtained on gold-doped devices in the near infrared [3] can in fact be extended to shallower level impurities, lower temperatures, and longer wavelengths. This type of infrared detector might be particularly useful for application in large scale integrated infrared imaging arrays operating in the middle infrared or 3.0 to 5.0 μm wavelength range.

The IRFET detector has some unique characteristics when compared to alternate techniques involving CCD scanned arrays of extrinsic silicon photoconductive detectors [16,19,20,21]. In the case of the IRFET, the detector, storage or memory element, and the read-out and output amplifier have essentially been integrated into a single device. In addition, IRFET

arrays would work on a static or D.C. memory concept as opposed to the dynamic or charge storage on capacitive node concept employed in CCD scanned arrays.

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APPENDIX C

GALLIUM-DOPED DEVICES*

INTRODUCTION

The infrared sensing MOSFET (IRFET) with gold and indium doping has been demonstrated as an infrared detector with some unique characteristics for use in the 1-3μ and 3-8μ infrared regions respectively [1-7]. This report deals with the characteristics of gallium-doped MOSFETs for use in the far infrared 8 to 14 μm wavelength range. Each particular infrared region has associated with it particular characteristics, advantages, and problems. Application of gallium-doped silicon MOSFET device structures in the far infrared is no exception. In this case, the background in a 300°K blackbody source emitting a photon flux of the order $2 \times 10^{18}/cm^2 sec$. For imaging, to detect a small temperature variation above the background then requires stringent control of the gallium uniformity.

The operation principle of the IRFET is based upon the photoionization process of a deep level impurity (gallium) in the depletion region of a MOSFET at a temperature below the freeze-out temperature of the gallium center. Upon irradiation, the Ga centers change charge state from neutral to negative with a time constant τ. This changes the threshold voltage which in turn changes the drain to source current and is detected by an external circuit. At the end of the exposure period, it is necessary to place the Ga centers in the neutral state for the next integration. This is achieved by applying an accumulation voltage to the gate and by doping the IRFET with another shallow level impurity (boron). The shallow level boron assures that sufficient holes are available to neutralize the gallium center during the reset period.

The MOSFET structure also provides a convenient tool for the characterization of shallow level impurity centers in silicon [8,9], particularly in

*Based on material submitted for publication, by K.W.Loh, B.M. Hawkins, H.Elabd, and L.Forbes.

the case where there is little or no other shallow level impurities present and the substrate resistance becomes very high at low temperatures.

Equations describing the operation of the device for the case when the density of deep level centers is small compared to shallow level centers and for the case when the density of deep level centers is large compared to the shallow level centers are presented. These situations correspond to doping levels used to characterize the gallium center and to doping levels used to achieve high sensitivity when the MOSFET is used as a detector.

Experimental verification of the device operation including characterization of the Gallium centers as functions of temperature, backgate bias, and photon energy is also presented.

DEVICE EQUATIONS

To obtain large I_{DS} and to avoid dependence on V_{DS}, the device is operated in the saturation region. The basic equations describing MOSFET operation in the saturation regions are [10-12]:

$$I_{DS}(t) = (\beta/2)[V_{GS} - V_T(t)]^2 \qquad (1)$$

and

$$V_T(t) = A + B(1 - V_{BG})^{1/2}[N_B(t)]^{1/2} \qquad (2)$$

where $\beta = \mu C_o W/L$, μ is the effective surface mobility, C_o the oxide capacitance per unit area, W/L the channel width to length ratio, I_{DS} the drain to source current, V_{GS} the gate to source voltage, V_T the threshold voltage, A and B are parameters which depend upon the design and processing of the MOSFET, N_B the number of ionized impurity centers in the depletion region and V_{BG} is the backgate bias. N_B can be time dependent and is the combination of the number

of ionized shallow level impurity centers (boron) and ionized deep level impurity centers (gallium), i.e.,

$$N_B(t) = N_A + N_I[1 - \exp(-t/\tau)] \qquad (3)$$

where N_A and N_I are the boron and gallium concentration respectively. In Eq. (3), all the boron centers are assumed ionized and all the gallium centers are arranged to be neutral at time t=0 and subsequently become ionized by thermal and/or optical hole emission with a time constant $\tau = (e_p^t + e_p^o)^{-1}$ [8], where e_p^t and e_p^o are the thermal and optical hole emission rate. In reality, because the difference in the boron and gallium ionization energies is small, a portion of the boron centers in the depletion region are not ionized at t = 0, and will ionize at a rate $1/\tau_A$. However, for thermal measurements, $\tau \gg \tau_A$, i.e., in the practical sense all the shallow impurity centers can be assumed ionized. For photoionization measurements, the temperature must be arranged such that for the gallium centers $e_p^t \ll e_p^o$. Under this condition, the boron thermal hold emission rate can be comparable to the gallium optical hold emission rate. In other words, accurate determination of the Ga photoionization cross section is difficult unless the boron centers are first ionized with photon flux having energy less than the Ga threshold energy. For convenience, in the following discussion, we shall assume N_A are all ionized in the depletion region at t = 0.

There are two distinctly different experimental conditions which may exist depending upon the ratio of deep to shallow level impurities concentration.

A. Case 1: $N_I \ll N_A$

Defining $\Delta V_T(t) = V_T(t) - V_T(0)$, from Eq. (3) we obtain

$$\Delta V_T(t) = \Delta V_{T,max}[1 - \exp(-t/\tau)] \qquad (4)$$

$$\Delta V_{T,max} = B(1 - V_{BG})^{1/2} N_I / 2\sqrt{N_A} \quad . \tag{5}$$

Since $N_I << N_A$, $\Delta V_{T,max}$ will be small. For any reasonable V_{GS}, $\Delta V_{T,max}$ $<< V_{GS} - V_T(0)$. Eq. (1) becomes

$$I_{DS}(t) = (\beta/2)[V_{GS} - V_T(0)][V_{GS} - V_T(0) - 2\Delta V_T(t)] \quad . \tag{6}$$

If the change in drain to source current is defined as

$$\Delta I_{DS}(t) = I_{DS}(t) - I_{DS}(\infty) \tag{7}$$

then

$$\Delta I_{DS}(t) = (\beta\ \ )[V_{GS} - V_T(0)]\Delta V_{T,max} \exp(-t/\tau) \quad . \tag{8}$$

Equation (8) indicates that $\Delta I_{DS}(t)$ varies exponentially in time with a time constant τ. The thermal and optical emission rates of the deep level impurity centers are readily obtained by measuring the change in drain to source current of the MOSFET, provided the shallow and deep levels are adequately separated. This case, $N_I << N_A$, provides a convenient means of characterizing the centers. For infrared detectors or imaging elements however, ΔI_{DS} is to be as large as possible for high responsivity. In view of Eqs. (5) and (8), large ΔI_{DS} can be obtained if N_I is made much larger than N_A. This is discussed in the following section.

B. Case 2: $N_I >> N_A$

In this case, ΔI_{DS} is not an exponentially decaying function. From Eqs. (1) to (3), we obtain

$$\Delta V_T(t) = B(1 - V_{BG})^{1/2}\{[N_A + N_I(1 - e^{-t/\tau})]^{1/2} - (N_A)^{1/2}\} \tag{9}$$

and

$$\Delta I_{DS}(t) = (\beta/2)\{[V_{GS} - A - B(1 - V_{BG})^{1/2}[N_A + N_I(1 - e^{-t/\tau})^{1/2}]^2 - [V_{GS} - A - B(1 - V_{BG})^{1/2}(N_A + N_I)^{1/2}]^2\} \quad (10)$$

It is informative to obtain $\Delta I_{DS,max}$ which gives a figure of merit of the device and is defined as

$$\begin{aligned}\Delta I_{DS,max} &= I_{DS}(0) - I_{DS}(\infty) \\ &= (\beta/2)\{[V_{GS} - A - B(1 - V_{BG})^{1/2}(N_A)^{1/2}]^2 \\ &\quad - [V_{GS} - A - B(1 - V_{BG})^{1/2}(N_A + N_I)^{1/2}]^2\}. \end{aligned} \quad (11)$$

From Eq. (11) for a given V_{GS}, a larger $\Delta I_{DS,max}$ can be obtained if $I_{DS}(\infty)$ is set to zero which occurs at $V_{GS} = V_T(\infty) = A + B(1 - V_{BG}^{1/2}(N_A + N_I)^{1/2}$. If $(1 - V_{BG})^{1/2}(N_A + N_I)^{1/2}$ is sufficiently large, cutoff can occur before $t = \infty$, i.e., the IRFET response time can be reduced by increasing V_{BG} and/or N_I. Under the condition that $A + B(1 - V_{BG})^{1/2}(N_A + N_I)^{1/2} \geq V_{GS}$,

$$\Delta I_{DS,max} = (\beta/2)[V_{GS} - A - B(1 - V_{BG})^{1/2}(N_A)^{1/2}]^2 . \quad (12)$$

In Eq. (2), $\Delta I_{DS,max}$ can be further increased by keeping N_A small and by increasing V_{GS}. The smallest N_A is determined by the reset time of the IRFET. At 20°K for a reset time of microsecond, $N_A \approx 10^{13}cm^{-3}$. At the present state of the art, A can be made less than a volt [10]. For large V_{GS} and small N_A, from Eq. (12) we have

$$\Delta I_{DS,max} \approx (\beta/2)V_{GS}^2 . \quad (13)$$

For the MOSFET to reamin in the saturation region, we must have $V_{GS} \leq V_{DS} + V_T$ which serves as an upperbound for V_{GS}. Since the largest V_{DS} is limited by the breakdown voltage which decrease as N_I increases, large ΔI_{DS} max can be obtained by judiciously choosing $N_I$and V_{BG} to satisfy the condition $A+B(1-V_{BG})^{1/2}(N_I)^{1/2} \geq V_{GS}$. For $\mu = 600cm^2/V.sec$

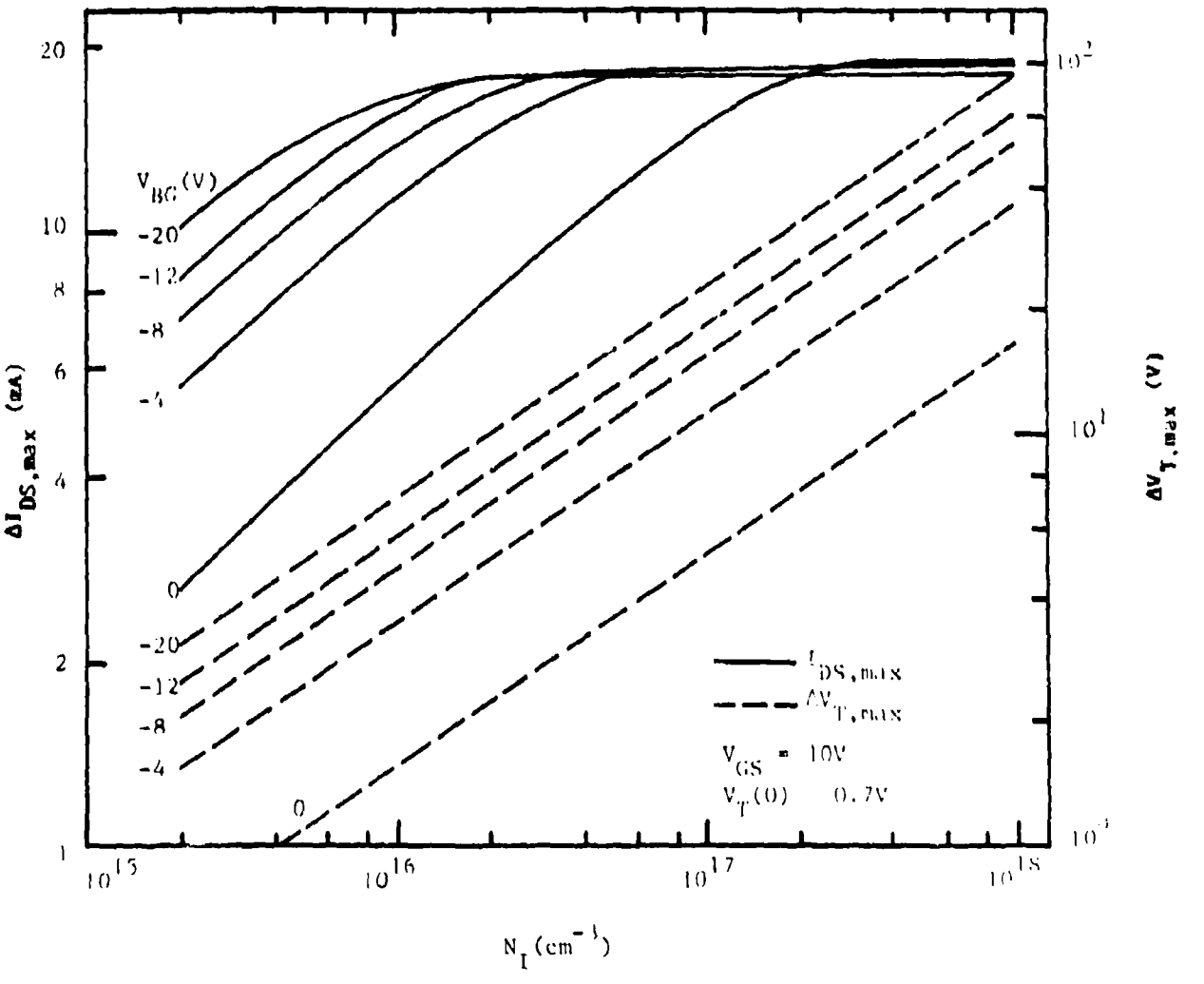

Fig.1. ΔI_{DS}, max versus N_I for various backgate biases. V_{GS}= 10V, W/L= 20, X_0 =1KÅ , μ= 600 cm^2/V.sec, A= 0.6V, $V_T(0)$ ≈0.7V.

X_o = 1 KÅ, W/L = 20, A = 0.6V, $N_A = 10^{13}cm^{-3}$ and V_{GS} = 10V, $\Delta I_{DS,max}$ and $\Delta V_{T,max} = [V_T(\infty) - V_T(0)]$ computed from Eqs. (9) and (11) are presented in Fig. 1. Saturation of $\Delta I_{DS,max}$ is due to cutoff of the MOSFET. From this figure for $N_I = 10^{16}cm^{-3}$, V_{BG} = -20V, a $\Delta I_{DS,max}$ of 16.5 mA and $\Delta V_{T,max}$ of 7V are obtained.

To illustrate the operation of the device, experimental values of ΔV_T versus $(1 - V_{BG})^{1/2}$ and the change in drain to source current with and without radiation for a device with somewhat different parameters are shown in Figure 2A and 2B respectively. In Figure 2A, $\Delta V_{T,max}$ increases from 0.9V at V_{BG} = 0V to 3V at V_{BG} = 12V. The increase in $\Delta V_{T,max}$ is due to the widening of the depletion width by the backgate bias. In Figure 2B, the decrease in time constant is due to optical hole emission caused by the external IR radiation.

EXPERIMENTAL RESULTS

Boron doped 1-3 Ω-cm (100) oriented and 100-300 Ω-cm (111) oriented silicon substrates were employed in this study. Gallium doping is achieved by using Emulsitone* spin-on Galliumsilicafilm. Pitting of the substrate was observed after Ga diffusion. N+ drain and source regions were fabricated in a circular geometry using Emulsitone Phosphorsilicafilm. Finished devices were then mounted on the cryo-tip of a cryo-refrigeration unit (Air Products Model AC-2). The lowest temperature achievable for our unit is 20.4°K.

A. Thermal Emission Rate of the Gallium Center in the Poole-Frenkel Effect

During thermal measurements the device was completely shielded to prevent any leakage of blackbody radiation and stray light. Figure 3 shows the MOSFET characteristics for Ga neutral and Ga negative. The change in I_{DS} is due to thermal hole emission from the Ga centers.

*Trademark of Emulsitone Co., Whippany, N.J.

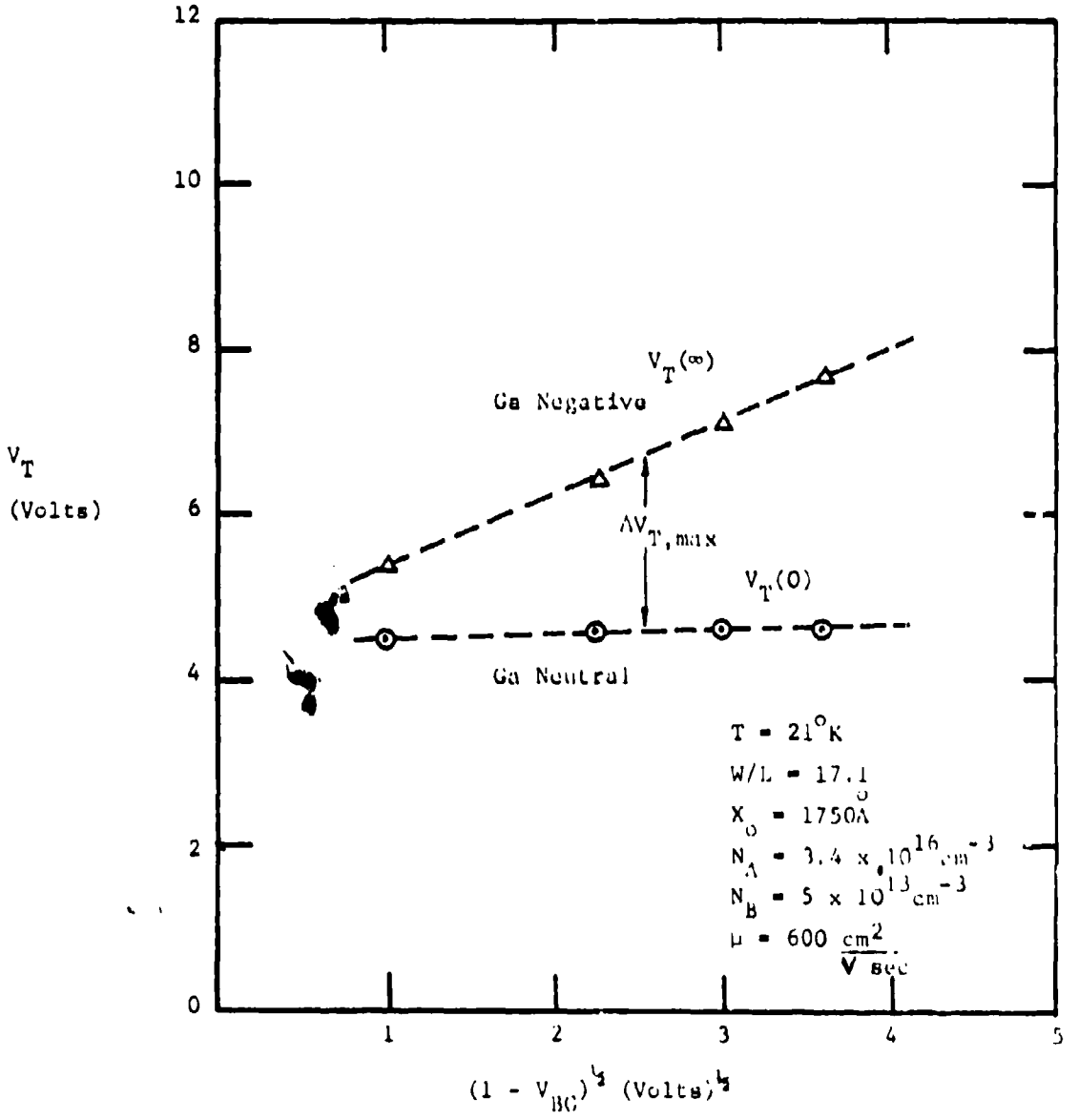

Fig. 2A. Illustration of the change in threshold voltage of the MOSFET for Ga neutral and Ga negative as a function of backage gate bias.

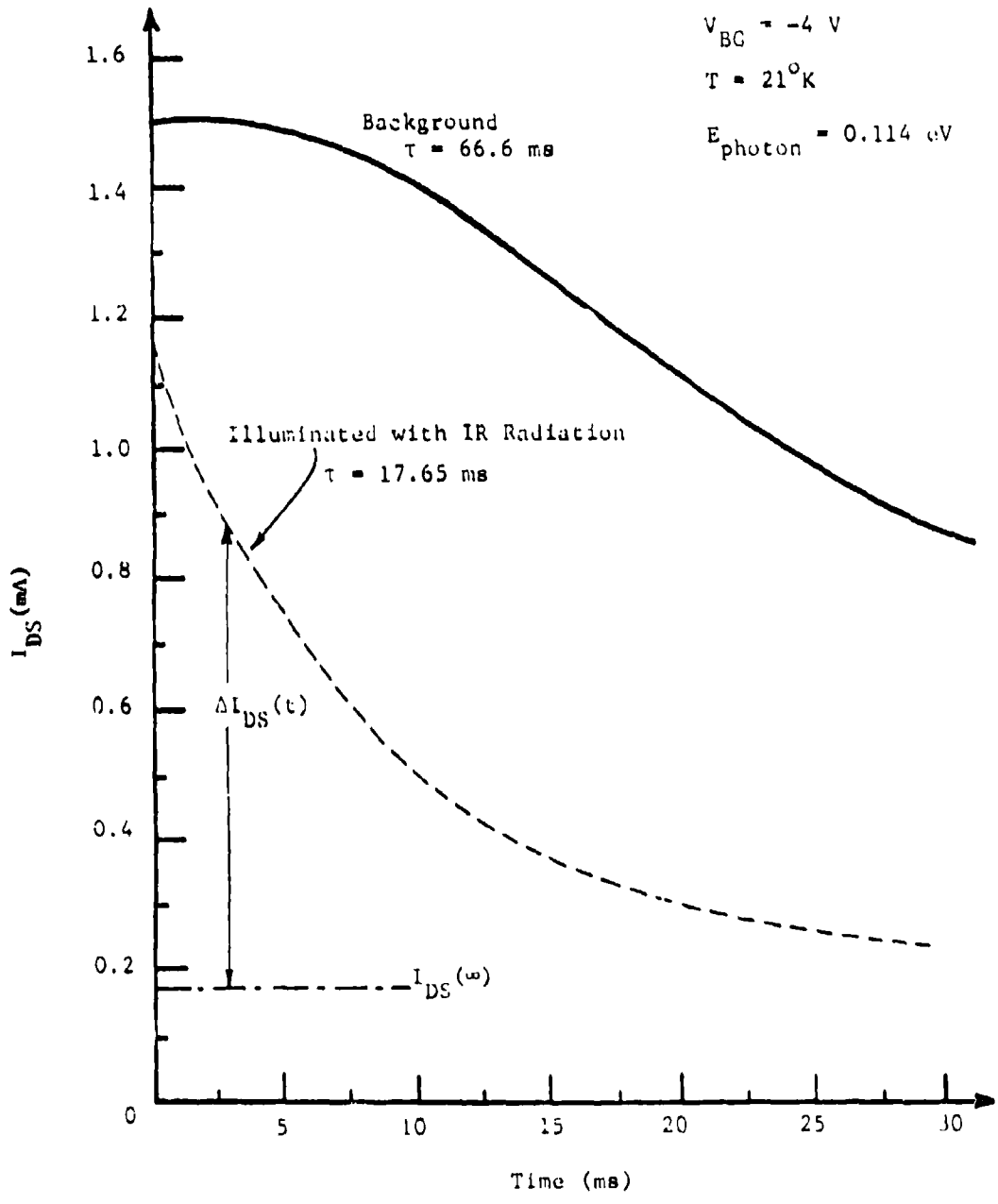

Fig. 2B. Effect of IR radiation on IRFET. Change in ΔI_{DS} is due to photoionization of the Ga centers by infrared photons.

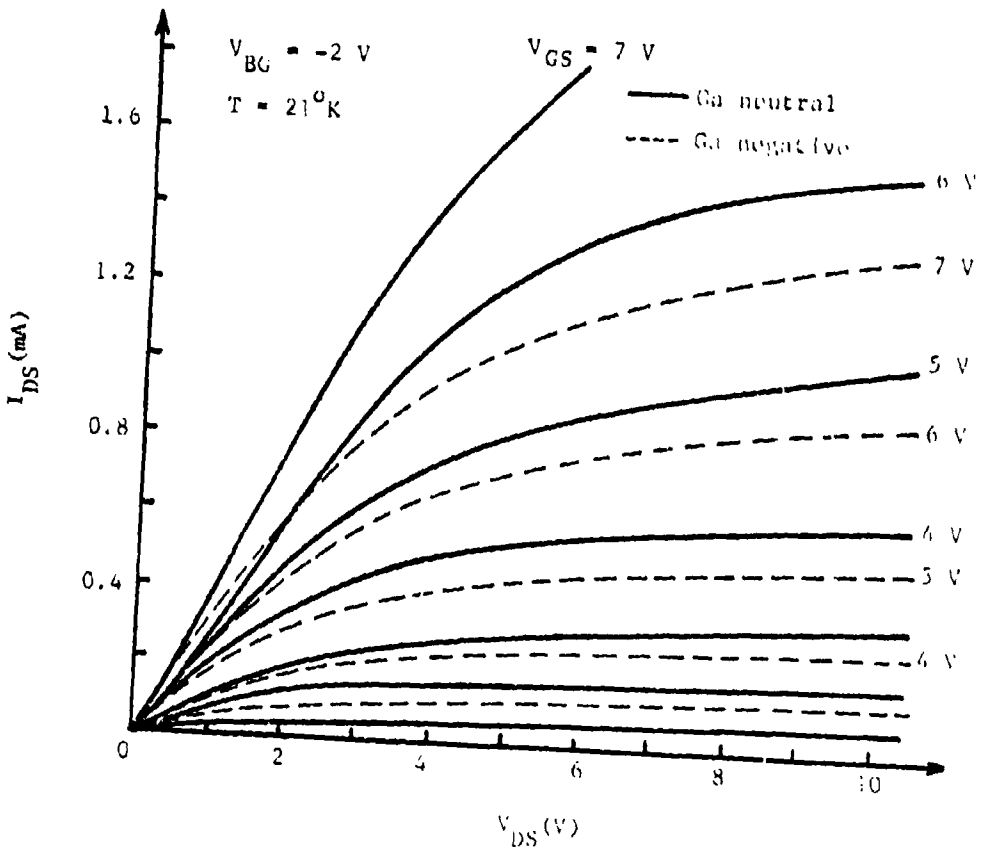

Fig.3. I-V Characteristics of IRFET. Change in I_{DS} is due to thermal hole emission of Ga centers. Solid curves are for t=0 when Ga centers are neutral. Dash curves are for t=∞ when Ga centers are negative.

The hole emission rate as a function of temperature for various backgate bias is presented in Figure 4. The ionization energy of the Ga center can be determined from the relationship [8],

$$e_p^t = AT^{3/2}\exp(-\Delta E/kT) \qquad (14)$$

where ΔE is the observed ionization energy of the Ga centers, k is the Boltzmann constant, T is the temperature, and A' can be regarded as a constant within the range of temperature employed to determine ΔE. ΔE, for different backgate bias, is given in the inset of Figure 4. At a backgate bias of -12V, ΔE = 63.3 meV, which is close to the published value of 65 meV and 71 meV determined by the Hall and optical absorption measurements [13,14].

It is well known that barrier lowering of a columbic potential due to an applied ε field gives rise to field enhanced emission. This is known as the Poole-Frenkel effect [15,16]. The one dimensional Poole-Frenkel effect predicts an enhancement of the emission rate due to the barrier lowering by the electric field of the following form [15],

$$e_p^t(\varepsilon) = e_p^t(\varepsilon = 0)\exp[\beta'\sqrt{\varepsilon}/kT]$$

$$= AT^{3/2}\exp(-[\Delta E(0) - \beta'\sqrt{\varepsilon}]/kT) \qquad (15)$$

where $\beta' = (e^3/\pi K_s \epsilon_o)^{1/2} = 2.2 \times 10^{-4}\text{eV}\sqrt{\text{cm/V}}$, $\Delta E(0)$ is the Ga ionization energy at zero field, K_s the dielectric constant of silicon, and ϵ_o the free space permittivity.

The ε field in the depletion region is a function of both space and time. Since ε is not a constant within the depletion region, an average ε field defined as $\bar{\varepsilon}(t) = \phi_s/W_d(t)$ is used. The surface potential ϕ_s is taken at L/2. $\phi_s = 2\phi_f + V_{DS,sat}/2 - V_{BG}$, where ϕ_f is the Fermi potential in the bulk, $V_{DS,sat}$

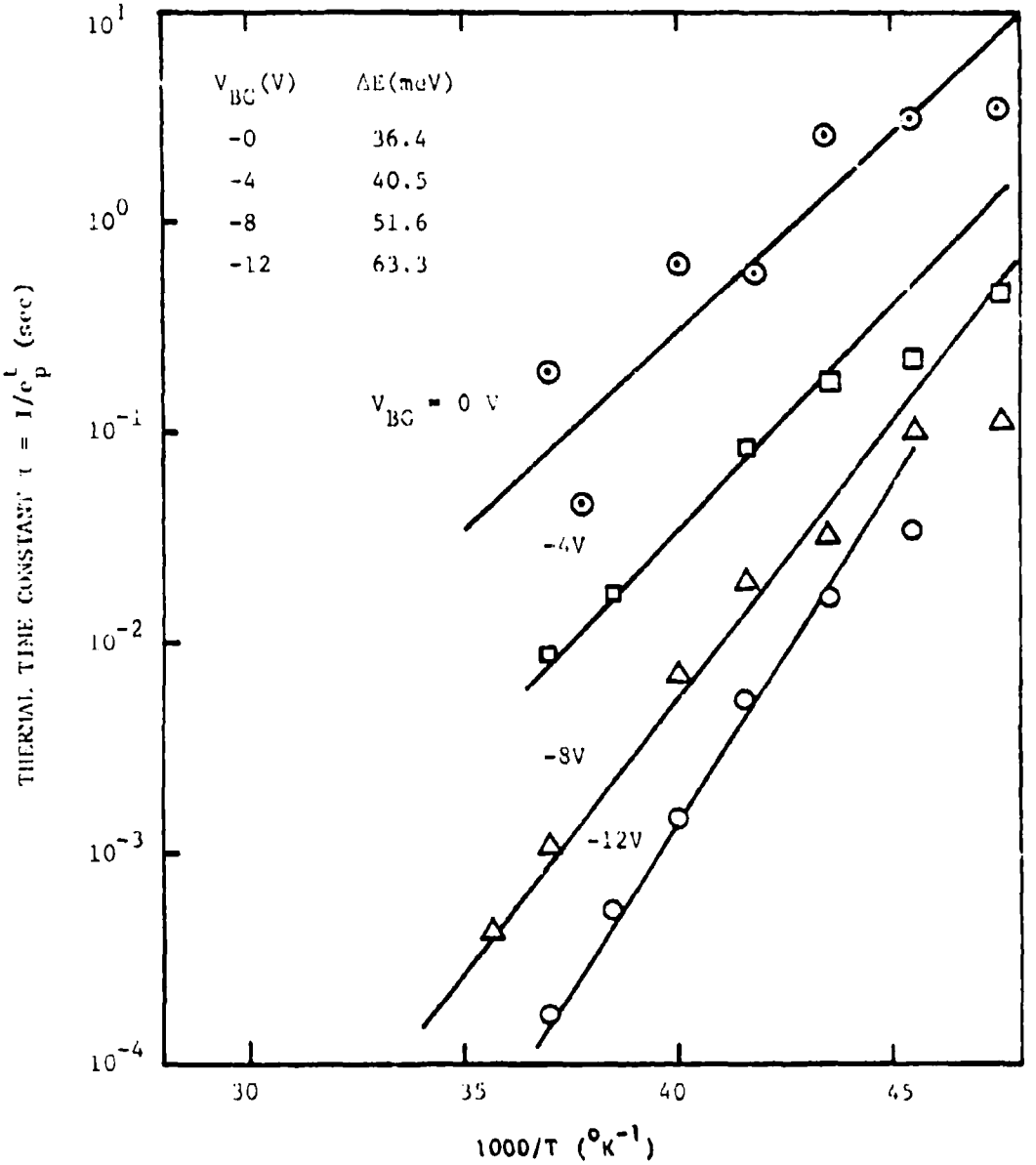

Fig. 4. Thermal time constant vs. 1000/T for various backgate bias.

saturation voltage and W_d is the depletion width. For case (2), because N_B varies from N_A at $t = 0$ to N_I at $t = \infty$, the average ε field is a strong function of time. In view of Eq. (15), the time constant observed in Eq. (10) is weighted at each instant of time by the ε field at that instant. The data were measured between $t = 0.1\tau$ to τ. To show the effect of the ε field, we have used the carrier concentration at $t = \tau/2$ to compute the ε field. The dependence of mobility on the ε field also introduces an additional error in the determination of τ.

The field enhanced hole emission rate as a function of $\sqrt{\varepsilon}$ for various temperatures is presented in Figure 5. β' obtained from Eq. (15) is given in the inset. At 27°K, the measured β' is approximately a factor of 2 higher than that at 21°K. Since the ε field in the depletion region is both a function of space and time, the measured β' is at best an average value which does not exclude the possibility that part of the Ga centers beneath the inversion layer could have tunneled or delocalized under high field. To roughly estimate the barrier lowering at the surface using the theoretical $\beta' = 2.2 \times 10^{-4}$ eV $(cm/V)^{1/2}$ at $V_{BG} = 0$ V and -12 V, the barrier lowering $\beta' \sqrt{\varepsilon_{peak}}$ is calculated to be 79 meV and 108 meV. Compared with the reported gallium ionization energy of 63 meV and 71 meV using the Hall and optical absorption measurements, the barrier is sufficiently lowered to cause tunnelling and delocalization to occur. The actual ε field varies from a maximum below the inversion to zero at the depletion edge. This fact together with the nonuniform gallium distribution due to diffusion, suggests that as the ε field increases only those Ga centers at the smaller value of the ε field (i.e., near the end of the depletion region) are measured. This would explain the increase in measured ΔE as the ε field increases. Because of the time and space variation of the

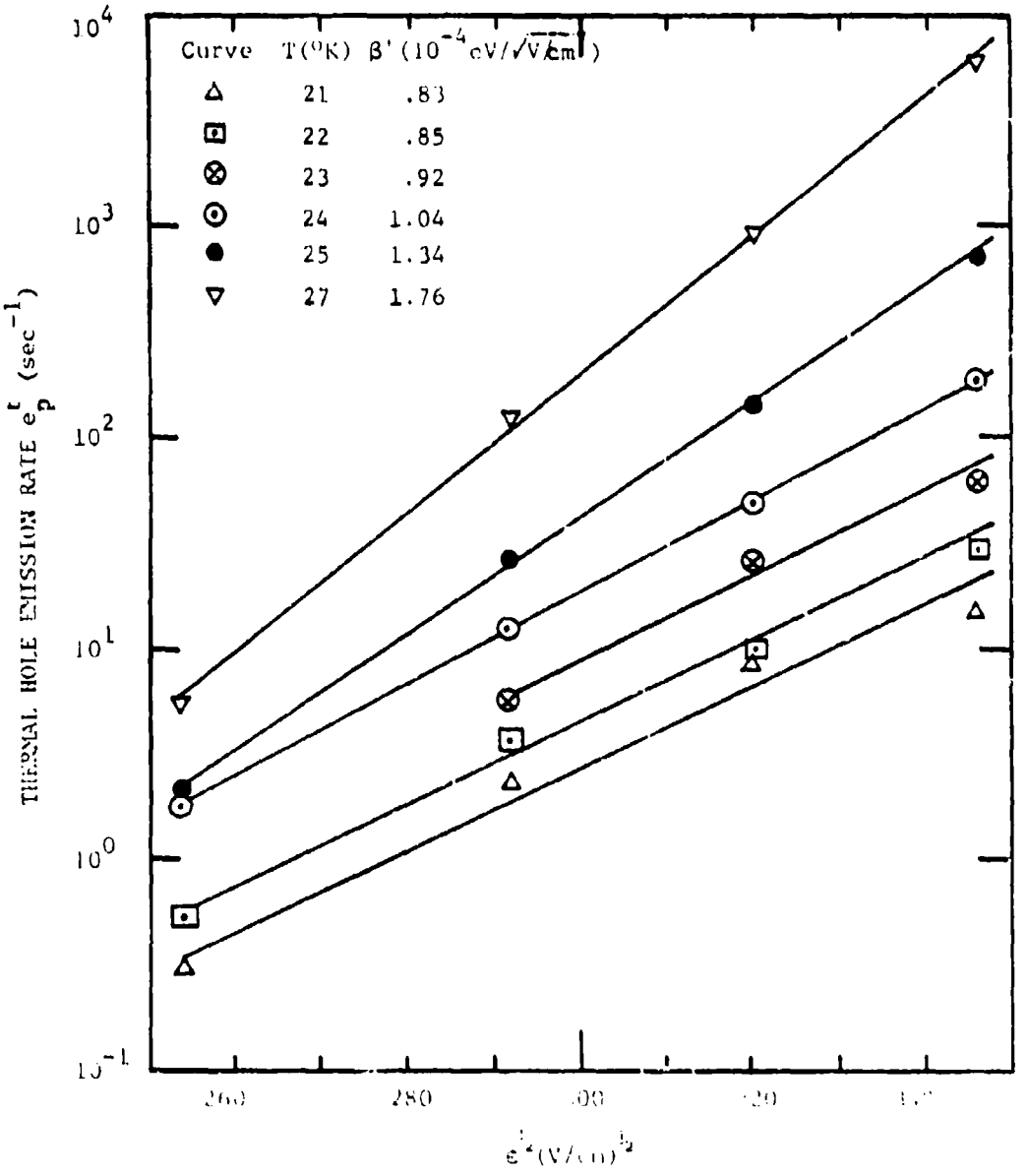

Fig. 5. Thermal hole emission rate of gallium as a function of the square root of electric field in the depletion region of the MOSFET for various temperatures.

electric field, our measurements are not accurate enough to warrant the use of the three dimensional Poole-Frenkel Effect [17].

B. Photoionization of the Gallium Center in Silicon

When the MOSFET device structure is employed as an infrared detector, infrared radiation incident on the gallium centers in the depletion region causes them to change charge state. The limiting cases where all of the gallium is either neutral or negative has been shown in Figure 3. The ability of an impurity center to capture an incident photon is described by the photoionization cross section. In order to more fully characterize the responsivity of the IRFET to infrared radiation, one should determine the photoionization cross section, $\sigma^o(\hbar\omega)$, of the gallium center, which is related to the optical emission rate through [8]:

$$e_p^o = \sigma^o(\hbar\omega)\Phi \tag{16}$$

where Φ is the incident photon flux. Since the observed hole emission rate e_p^{obs} is the sum of the response to not only the incident signal, but also the incident background flux due to blackbody radiation, the [18]

$$e_p^{obs} = e_p^o + e_p^b \tag{17}$$

where e_p^b is the hole emission rate due to the background. To accurately determine the photoionization cross section, the intensity of the incident monochromatic signal must be much larger than the total background flux at all wavelengths to which the gallium center is responsive. The spectral dependence of the photoionization cross section can then be determined by varying the incident photon energy and by Eqs. (1), (2), (3), (16), and (17).

A theoretical value for the photoionization cross section can be calculated using the Lucovsky Model [19,20]

$$\sigma^{o}(\hbar\omega) = \frac{1}{n}(\varepsilon_{eff}/\varepsilon_{o})^{2}(16\pi e^{2}\hbar/3m^{*}c)(\Delta E)^{1/2}(\hbar\omega - \Delta E)^{3/2}/(\hbar\omega)^{3} \qquad (18)$$

where

n = optical index of refraction

$\varepsilon_{eff}/\varepsilon_{o}$ = effective field ratio

m* = effective mass of the trapped carrier

ΔE = observed ionization energy

c = speed of light.

Or in terms of the one dimensional Poole-Frenkel effect:

$$\sigma^{o}(\hbar\omega) = \frac{1}{n}(\varepsilon_{eff}/\varepsilon_{o})^{2}(16\pi e^{2}\hbar/3m^{*}c)[\Delta E(0) - \beta'\sqrt{\varepsilon}]^{1/2}[\hbar\omega-(\Delta E-\beta'\sqrt{\varepsilon})]^{3/2}/(\hbar\omega)^{3}. \qquad (19)$$

As pointed out in the last section, the large electric field in the depletion region causes a reduction of the observed ionization energy. This will undoubtedly reduce the threshold energy of the photoionization cross section. However, it is not clear whether the barrier lowering would simply translate the entire cross section to the lower photon energy region.

For values of ε which give barrier lowering comparable to the activation energy $\Delta E(0)$, tunnelling or delocalization of the gallium center will occur. This means that the surface gallium center under high field can change charge state without absorption of a photon. They become immediately ionized upon the application of an inversion voltage to the gate.

A 300°K background radiates large photon flux beyond 4 microns and will discharge the Gallium IRFET in tenths of milliseconds. Our experimental arrangement for measuring the photoionization cross section consists of a globar source operating at 1350°C and a bandpass filter adjacent to the device.

The bandpass filter is cooled to 21°K and does not constitute a source of background radiation but serves to block off the background radiation outside the bandpass region. This increases the background time constant to the order of ten milliseconds.

Due to equipment limitations we were not able to determine the absolute photoionization cross section and the threshold photon energy. Figure 6 shows the relative photoionization cross section in the 8 to 14 micron wavelength range at 20.4°K for three electric field values. The dependence of the optical emission rate on the average electric field in the surface depletion region is shown in Figure 7. By comparing Figure 5 and Figure 7 we see that the optical emission rate exhibits a field enhancement similar to that observed for the thermal emission rate.

For comparison, measurement of Burnstein, et.al. [14], and theoretical curves using Eq. (18) are also plotted in Figure 6. At high photon energy the measured photoionization cross section decreases more rapidly than the theory predicts. However, the Poole-Frenkel barrier lowering does seem to shift the response to the lower photon energy region.

OPERATION AS AN INFRARED DETECTOR

In previous sections an investigation has been made of the characteristics of the gallium center in silicon. When operating the MOSFET device structure as an infrared detector, the temperature must be low enough so that optical emission or photoionization is the dominant process as opposed to thermal emission. The spectral response will then be determined by spectral dependence of the photoionization cross section of the gallium center.

The important characteristics describing operation of the device as an infrared detector are then the quantum efficiency, responsivity and signal to noise ratio.

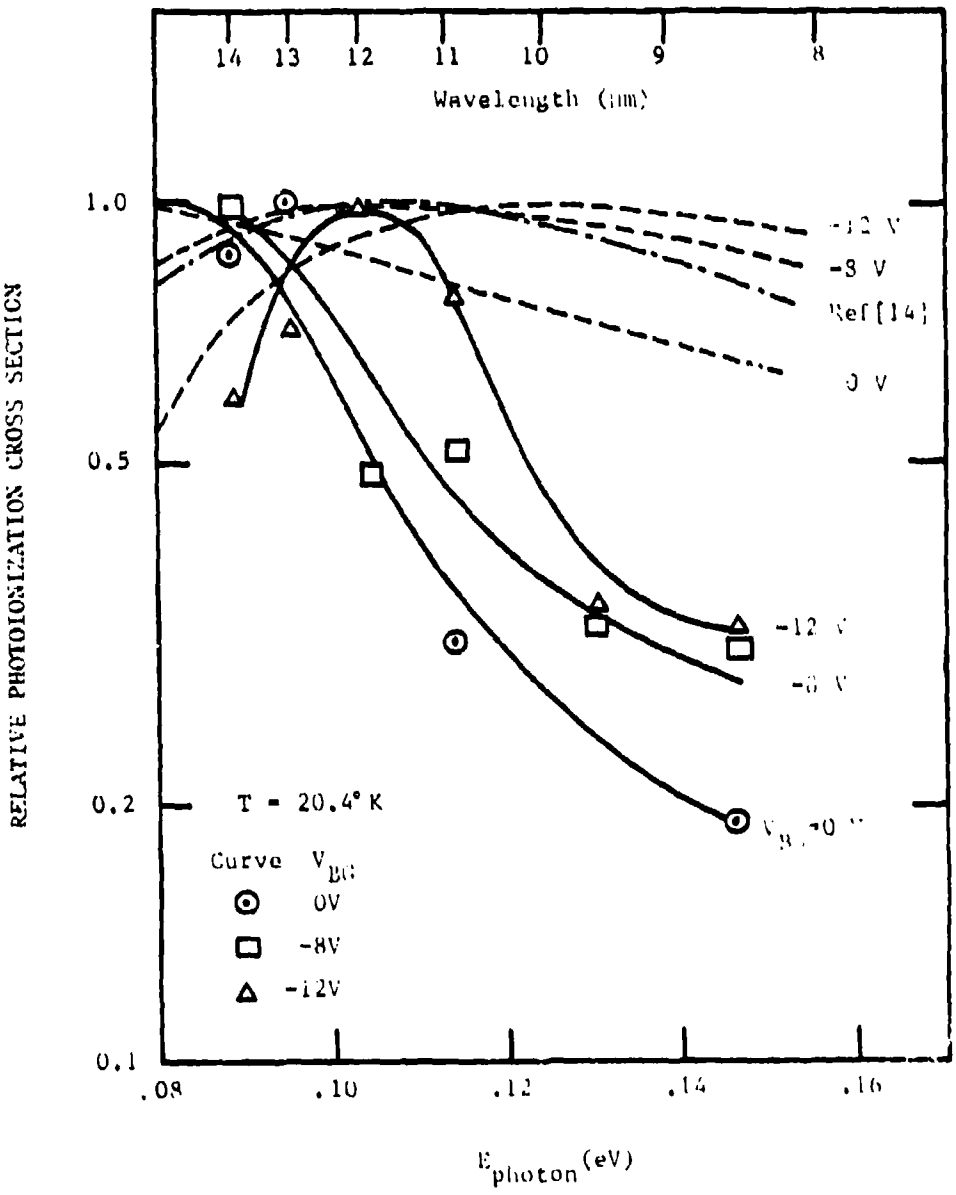

Fig.6. Relative photoionization cross section of the gallium center under various electric field conditions. Solid curves are from measurements. Dashed curves are obtained from Lucovsky Model. Dash and dot curve was measured by Burnstein et. al. [14].

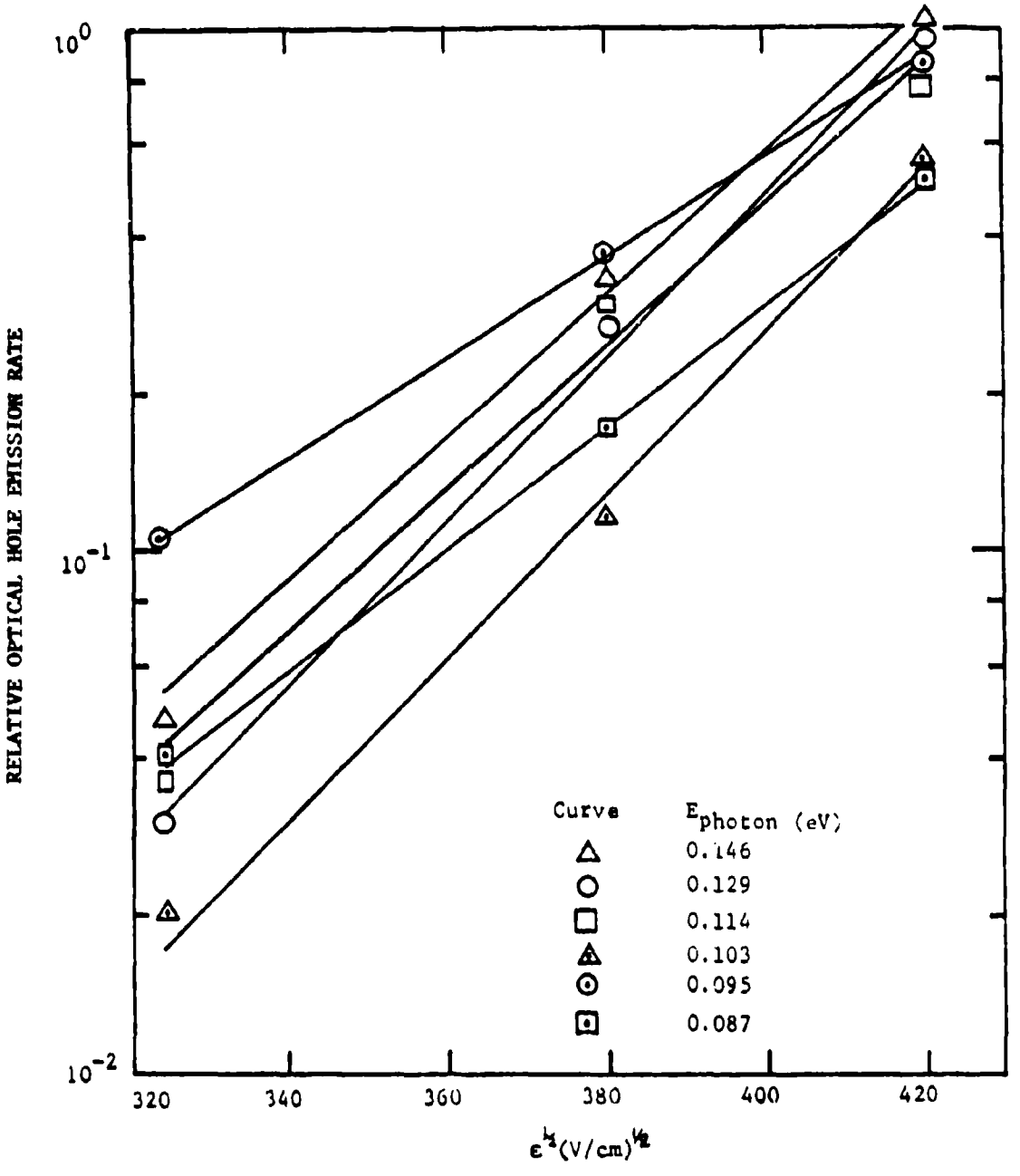

Fig. 7. Field enhanced optical hole emission rate of the gallium center in silicon for various incident photon energies.

When the device is operating, the quantum efficiency η is a function of time. Ignoring reflection loss, for $e_p^o >> e_p^t$, η is given by

$$\eta(t) = 1 - \exp[-\sigma^o N_I e^{-t/\tau} W_d(t)] \tag{20}$$

$$W_d(t) = \{2\varepsilon_o K \phi_s / q[N_A + N_I(1 - e^{-t/\tau})]\}^{1/2} \tag{21}$$

where W_d is the depletion width and ϕ_s is the surface potential.

At time $t = 0$, all the Ga centers are neutral and able to emit holes. At this time, the depletion layer width determined solely by the number of ionized boron atoms is the widest. According to Eqs. (20) and (21) the highest quantum efficiency thus occurs at $t = 0$. Upon absorption of a photon, the neutral Ga emits a hole and becomes negative. As the photoionization process progresses, the number of neutral Ga available reduces and the depletion width decreases. This reduces the quantum efficiency rapidly. Specifically, at time t, such that $N_I(1 - e^{-t/\tau}) >> N_A$, it reduces to

$$\eta(t) \simeq 1 - \exp\{-\sigma^o e^{-t/\tau}[2\varepsilon_o K_s / q(1 - e^{-t/\tau})]^{1/2} \sqrt{N_I \phi_s}\} \ . \tag{22}$$

From Eq. (20) or Eq. (22), $\eta(\infty) = 0$, i.e., all the Ga centers have been ionized and no further photoionization is possible.

Since the information of how many Ga centers have been photoionized is stored in the photocurrent ΔI_{DS} which begins at $t = 0$, the quantum efficiency $\eta(0)$ can be taken as the quantum efficiency of the IRFET. From Eq. (20) to achieve high $\eta(0)$, one needs to have high gallium concentration and wide depletion width, i.e., small N_B and large V_{BG}. This is in agreement with the results obtained in Section II-B by optimizing the photocurrent. For $\sigma^o = 5 \times 10^{-16} cm^2$, $\eta(0)$ as a function of N_I for various N_B and V_{BG} is presented in Figure 8. In this figure, the effects of drain to source voltage, breakdown voltage and impurity level broadening due to high doping levels

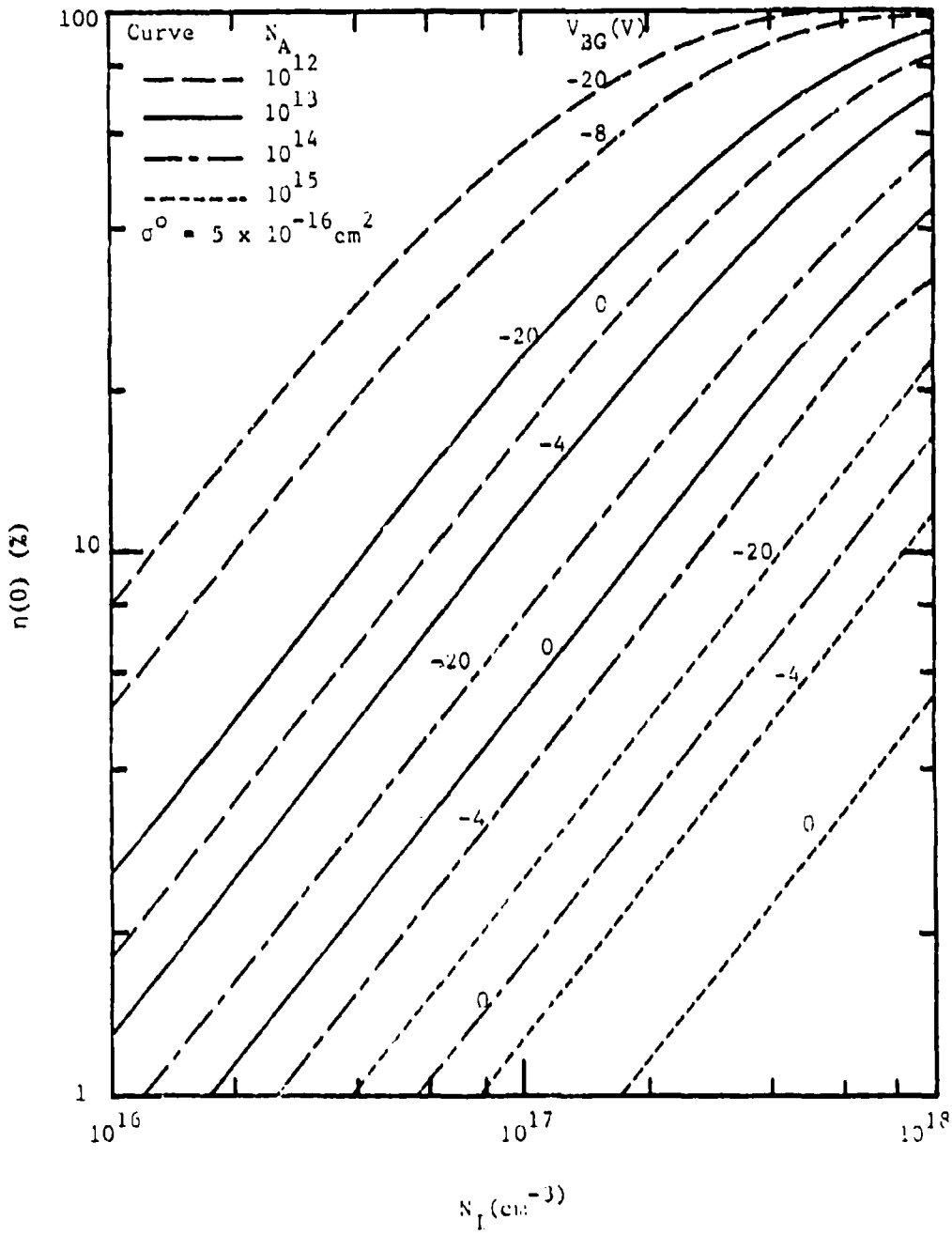

Fig.8. Inital quantum efficiency η(0) versus N_I for various combination of N_A and V_{BG}.

have not been taken into account. Employing $N_I = 10^{17}cm^{-3}$, for $N_A = 10^{13}cm^{-3}$, $V_{BG} = 20V$, an initial quantum efficiency of 23% can be obtained.

Since the amount of change in drain to source current depends on the length of integration time, for a given Φ, the responsivity can be defined as

$$R_1 = \frac{\text{change in photocurrent}}{\text{incident photon energy}}$$

$$= \frac{I_{DS}(t=0) - I_{DS}(t=t_I)}{\hbar\omega\Phi A_1 t_I}$$

$$= \frac{\Delta I_{DS,max} - \Delta I_{DS}(t=t_I)}{\hbar\omega\Phi A_1 t_I} \qquad \text{Amps/Joule} \quad (23)$$

where t_I is the integration time, $\hbar\omega$ is the photon energy and A_1 is the gate area.

To provide comparison to other types of detectors, a responsivity in terms of A/W can be defined as

$$R_2 = \frac{\Delta I_{DS,max}}{\hbar\omega\Phi A_1} \qquad \text{Amps/Watt} \quad (24)$$

where we have assumed that the photons have been incident on the device until all the Ga centers have been ionized. Of course, the responsivity R_2 would be somewhat unrealistic since for a given integration time and incident photon flux, the Ga centers may not be all ionized. Nonetheless, in the event that all the Ga centers will be ionized or that t_I is sufficiently long such that $I_{DS}(C) - I_{DS}(t_I) = \Delta I_{DS,max}$, R_2 does indicate the IRFET's ultimate performance. Since the IRFET can be designed so that cutoff occurs before $t = \infty$, which could be considered as saturation of the IRFET, t_I could be judiciously chosen for a particular application

It has been previously shown that the maximum attainable current signal to noise ratio operating under shot noise limited condition is [7]

$$S/N = (N_S A_I/2)^{1/2} \tag{25}$$

where N_S is the surface charge density stored by the Ga center. Shot noise or signal noise limited operation can be achieved for integration period less than ~10 sec or for short integration periods such that the 1/f noise is smaller than the shot noise.

High responsivity can be achieved by optimizing the photocurrent, $\Delta I_{DS,max}$. As discussed in the previous section, this is obtained by increasing V_{BG} and N_I until ε_{peak} approaches the breakdown field value. On the other hand, too large an ε field will cause tunnelling and delocalization of the Ga center which in turn reduces $\Delta I_{DS,max}$. Heat dissipation and device destruction for large I_{DS}, should also be considered.

From Eq. (10), after $\Delta I_{DS,max}$ has been optimized it can be kept constant while reducing "A_I" by maintaining the same W/L. The smallest L should be large enough so that space-charge-limited current flow will not occur. From Eqs. (23) and (25), reducing A_I will increase R but reduce S/N. The parameter A_I may be reduced to the extent that an acceptable S/N ratio is obtained as required by the system application. The parameters, η, R_I, R_2, and S/N for the test devices are given in Table (1). This device may be improved by reducing the gate area, while maintaining W/L. Parameters for an improved design are also listed for comparison. In the table a flux $\Phi = 3 \times 16$ photons/cm^2·sec at $\lambda = 14.3\mu$ is assumed incident on the device. For the improved design, $\Delta V_{T,max}$ increases to 18.52 V. A current of 69 mA will undoubtedly cause device destruction. Although the responsivities have

$\mu = 600\ cm^2/sec \cdot V$ $\lambda_o = 14.3\ \mu m$

$\sigma = 5 \times 10^{-16} cm^2$ $\Phi = 3 \times 10^{16}\ \#/cm^2 sec$

PARAMETER	PRESENT DEVICE	IMPROVED DEVICE
$X_0(KA)$	1.75	1.0
$W(\mu m)$	1.54×10^3	200
$L(\mu m)$	2.285×10^2	10
$N_A(cm^{-3})$	5×10^{13}	5×10^{13}
$N_I(cm^{-3})$	3.4×10^{16}	6×10^{16}
$\Delta V_{T,max}(V)$	2.66	18.52
$\Delta I_{DS,max}(mA)$	1.42	68.85
R_1 + (A/J)	3.52×10^3	1.68×10^8
R_2 (A/W)	156.8	8.4×10^6
$\eta(o)$ (%)	2.83	6.84
S/N	1.3×10^5	9.2×10^3
$W(0)$ (μm)	11.5	23.6

+ t_1 is taken to be 50 ms.

Table I. Characteristics of the current devices and projected characteristics of a better small area device.

increased by three orders of magnitude to 10 A/μW, the signal to noise ratio has dropped an order of magnitude due to the reduced area. The increase in quantum efficiency is due to the increase in backgate bias.

To design a IRFET, one could start from the required signal to noise ratio dictated by the particular application. From the expected photo flux Φ, the desired responsivity and integration time, the parameters N_I, A, W/L, and V_{GS} are then determined. Finally, N_A can be determined by reset time requirement.

CONCLUSIONS

In conclusion, operation of the gallium-doped MOSFET as an infrared detector in 8 to 14 um wavelength region, has been demonstrated. Both the characteristics of the device and the gallium impurity center have been described. Measurements of the thermal emission rate of the gallium center indicate that for short frame times, operation at 20°K should be acceptable, as long as care is taken not to subject the gallium centers to large electric fields which result in a large enhancement of thermal emission due to the Poole-Frenkel effect. The time constant associated with thermal emission under an electric field of 2×10^4 V/cm is of the order of seconds at 20°K.

The gallium center has a large photoionization cross section in the far infrared region and if exposed to radiation from a 300°K scene in a large aperture or small f/number system will completely discharge in a few milliseconds. This indicates that for imaging applications, integration and frame times in the tens of milliseconds or TV rates could be achieved. The IRFET has been found to possess unique characteristics and can be considered an integrated detector, memory element, and amplifier, all in one device; as

opposed to CCD scanned photoconductor arrays where each component is a separate element of the device [21-24]. As such then, the gallium doped infrared sensing MOSFETs might be particularly suited for large scale integrated infrared imaging focal planes in the 8 to 14 μm wavelength range.

The noise characteristics, uniformity, application techniques, and relative advantages of the infrared sensing MOSFET(IRFET) are discussed in detail in the following section .

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APPENDIX D

NOISE CHARACTERISTICS*

LIST OF SYMBOLS

A	Area of individual detector, cm.^{2}
A_{IP}	Area of image plane, cm.^{2}
$BW, \Delta\nu$	Bandwidth, sec.$^{-1}$
C_o	Oxide or insulator capacitance, farads cm.$^{-2}$
D^*	Detectivity, cm.sec$^{-1/2}$ watt^{-1}
ε_o	Electric permittivity of free space, farad cm.$^{-1}$
e_p^o	Optical emission rate, sec.$^{-1}$
$\hbar\omega_s$	Signal photon energy, joules
$(\bar{i}_N^2)^{1/2}$	Root mean square (RMS) noise current, amps.
$(\bar{i}_{DSN}^2)^{1/2}$	RMS drain to source noise current, amps.
$\bar{I}$	Mean or average current, amps.
I_{DS}	Drain to source current, amps.
κ_s	Relative dielectric constant of silicon
κ_o	Relative dielectric constant of oxide
L	Channel length, cm.
n	Number of point in image
N	Background photon flux, sec.$^{-1}$cm.$^{-2}$
N_A	Acceptor impurity concentration, cm.$^{-3}$
NEP	Noise equivalent power, watts
N_S	Surface charge density, cm.$^{-2}$
N_{TT}	Impurity concentration, cm.$^{-3}$
q	Electronic charge, coulombs
$(\bar{Q}_N^2)^{1/2}$	RMS variation in charge, coulombs
Q_{CH}	Charge in channel, coulombs.

*Based on material submitted for publication by L.Forbes and W.C. Parker.

T_I	Integration time, sec.
T_F	Frame time, sec.
T_S	Sample time, sec.
S/N	Signal to noise current ratio
V_{BG}	Back gate or substrate bias, volts
V_{DS}	Drain to source voltage, volts
V_{GS}	Gate to source voltage, volts
V_T	Threshold voltage, volts
W	Gate or channel width, cm.
W_d	Depletion region width, cm.
x_o	Oxide thickness, cm.
Δ	Indicates change in quantity following symbol
η	Quantum efficiency
μ	Mobility, $cm.^2\ volt^{-1}\ sec.^{-1}$
σ	Photoionization cross section, $cm.^2$
τ	Time constant, sec.
ϕ_f	Fermi potential, volts.
ϕ	Signal photon flux, $sec.^{-1} cm^{-2}$
ϕ_N	Noise equivalent signal photon flux, $sec^{-1}\ cm^{-2}$

INTRODUCTION

The ability of infrared imaging arrays to detect signals from the desired scene is limited in terrestial applications by the noise resulting from the background illumination. Historically, of course, the simplest technique for infrared imaging has been to mechanically scan the scene across a single

detector area, A, where the bandwidth, BW, of the signal amplification system is determined by the number of points in the scene and scan rate. This leads to the definition of a relative figure of merit for comparing detectors as the detectivity or $D^* = (A)^{1/2}(BW)^{1/2}/NEP$, where NEP is the noise equivalent power [1]. In the case of the newer types of devices as for instance, charge-injection diodes, CID's, [2,3], charge coupled devices, CCD's, [3,4,5] or infrared sensing field effect transistors, IRFET's [6,7,8,9,10] there is no well defined single bandwidth, but on the other hand two bandwidths, one associated with the integration period, T_I, and one associated with the sample period, T_S.

The first objective of this report is to derive the noise equivalent signal power, NEP, for an array of IRFETs employed in an infrared imaging array. Since we are dealing first with the theoretical limit on the operation of infrared imaging detectors due to background radiation it will be assumed that the dominant noise mechnism is shot noise due to this background. Photon noise will not be considered since it only introduces a small additional factor similar to the shot noise [1] and other types of noise as 1/f, Johnson, and generation recombination will also not be considered at first. The parameters for the imaging application are the area of the scene in the image plane, A_{IP}, and the frame time, T_F, background photon flux, N, number of points or elements in the scene, n, quantum efficiency, η, and signal photon energy $\hbar\omega_s$. Using these parameters then, the theory for shot noise or background limited operation of the IRFET will be developed, yielding the NEP and signal to noise ratio, S/N.

The theoretical expressions for shot noise limited operation of the IRFET will then be compared to the actual operation of the specific example

of a gold-doped device operated in the near infrared range at 78.8°K. It will be shown that shot noise limited operation can be achieved over a wide range of operating conditions. In reality, however, other types of noise sources are also present in the MOSFET, the most troublesome being 1/f noise. The regions of shot noise and 1/f noise limited operation will then be illustrated.

SHOT NOISE THEORY FOR THE IRFET

The infrared sensing MOSFET, IRFET [6,7,8,9,10] will integrate the incident flux and at the end of this integration period there will be a change in drain to source current, $\Delta I_{DS}(T_I)$, in the linear region given by [6,8];

$$-\Delta I_{DS}(T_I) = \mu C_o (W/L) V_{DS} \Delta V_T T_I \sigma N \qquad (1)$$

where μ is the effective surface mobility, C_o the oxide capacitance, W/L the width to length ratio of the channel, ΔV_T the maximum possible change in threshold voltage, σ the photoionization cross section, T_I the integration period, and N the background flux. However, the change in threshold voltage is due to a change of charge in the channel device and there will be associated with this some uncertainty in this change in charge due to shot noise. As shown in Figure 1, in the infrared sensing MOSFET, the emission of holes from impurity centers in the surface space-charge region will induce a change of charge in the channel or inversion layer. This change in charge, ΔQ_{CH} can be written

$$\Delta Q_{CH} = \bar{I} T_I$$

where $\bar{I}$ is the average source current. By taking into account the displacement

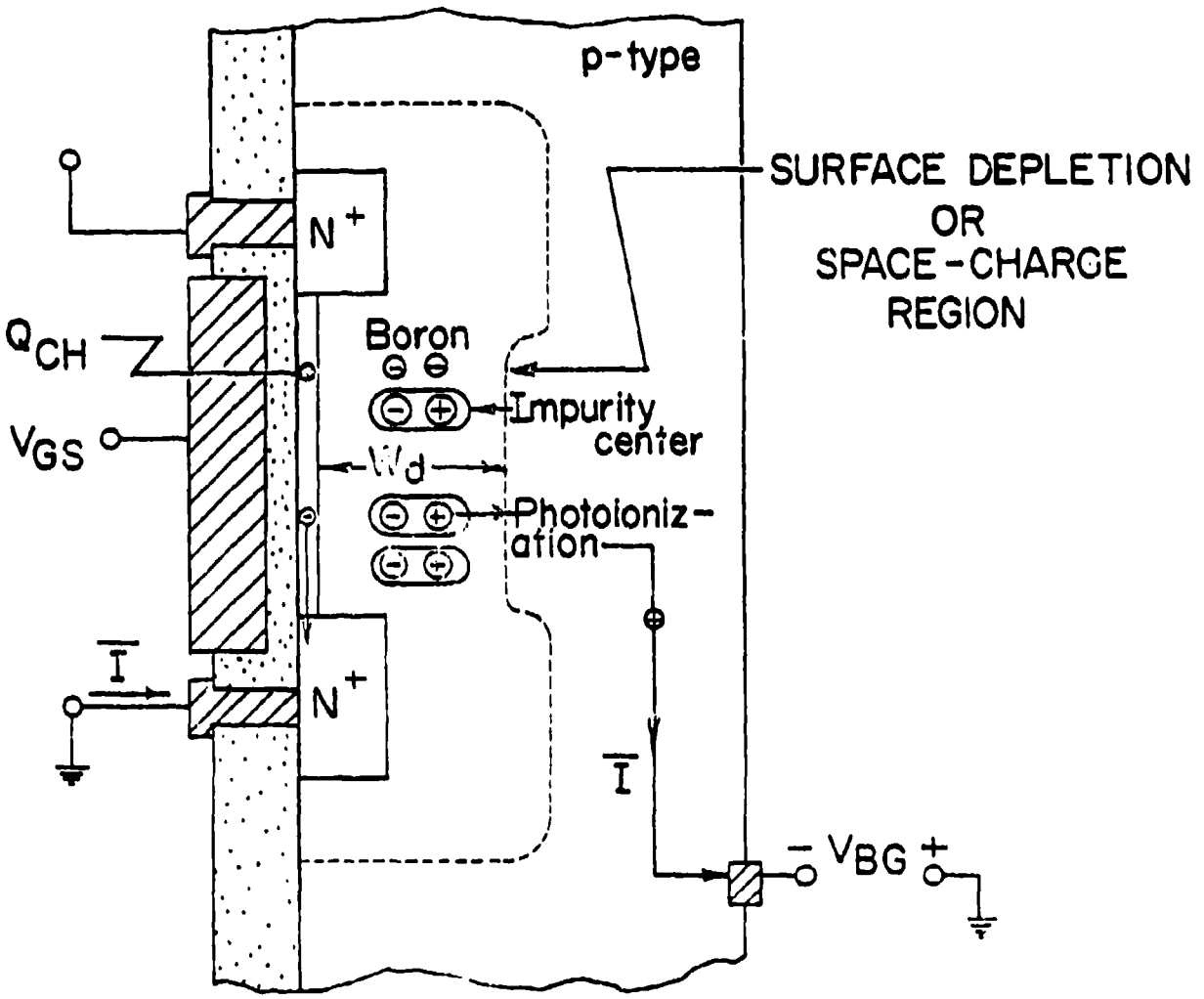

Fig. 1. The Infrared Sensing MOSFET Showing Source and Substrate Current, $\bar{I}$, due to Emission of Holes from Impurity Centers.

current or change in width of the surface depletion region [11], it can be shown;

$$\bar{I} = q\sigma N_{TT} W_d NWL/2 \tag{3}$$

and since the quantum efficiency, η, is just

$$\eta = \sigma N_{TT} W_d \tag{4}$$

then

$$\bar{I} = q\eta WLN/2. \tag{5}$$

Since this is a time dependent process, then by Carson's Theorem there will be a root mean square noise current

$$(\bar{I}_N^2)^{1/2} = (2q\bar{I}\Delta\nu)^{1/2} = (q^2\eta WLN/T_I)^{1/2} \tag{6}$$

and a possible error in the channel charge at the end of this integration period, T_I of

$$(\bar{Q}_N^2)^{1/2} = (q^2\eta WLN/T_I)^{1/2} T_I \, . \tag{7}$$

In the linear region of operation

$$I_{DS} = \mu C_o (W/L)(V_{GS} - V_T)V_{DS} = \mu Q_{CH} V_{DS}/L^2 \tag{8}$$

$$Q_{CH} = C_o(V_{GS} - V_T)WL \text{ coulombs} \tag{9}$$

A possible error of charge in the channel $(\bar{Q}_N^2)^{1/2}$ at the end of the integration period will result, by analogy with Eq. 8, in a root mean square noise current in the sample period of

$$(\bar{I}_{DSN}^2)^{1/2} = \mu(\bar{Q}_N^2)^{1/2} V_{DS}/L^2 \tag{10}$$

$$(\bar{I}_{DSN}^2)^{1/2} = \mu(q^2\eta WLNT_I)^{1/2} V_{DS}/L^2 \tag{11}$$

The signal current, $\Delta I_{DS}(T_I)$ or i_{signal}, due to the signal photon flux Φ will be from Eq. (1)

$$i_{signal} = \mu C_o (W/L) V_{DS} \Delta V_T \sigma \Phi T_I \tag{12}$$

and equating the signal and noise to determine the noise equivalent power yields Φ_N, the signal photon flux which gives an output equal to the noise

$$\Phi_N = [1/(\sigma C_o \Delta V_T)][q^2 \eta N/(WLT_I)]^{1/2} . \tag{13}$$

However, ΔV_T, can be expressed in terms of the oxide thickness and doping densities [6,8]

$$\Delta V_T = (x_o \kappa_s/\kappa_o)[2(2|\phi_f| + |V_{BG}|)qN_A/(\kappa_s \varepsilon_o)]^{1/2}(N_{TT}/2N_A) \tag{14}$$

then

$$\Delta V_T = qW_d N_{TT}/(2C_o) \tag{15}$$

and Φ_N becomes

$$\Phi_N = [4N/(WL\eta T_I)]^{1/2} \tag{16}$$

and the noise equivalent power, NEP = $\Phi_N \hbar\omega_s WL$, for a single detector

$$NEP = \hbar\omega_s [4NA/(\eta T_I)]^{1/2}. \tag{17}$$

This is just a factor of $(2)^{1/2}$ larger than the classical formula for the shot noise limit for background limited operation of a photodiode [1].

In an imaging application, A, the area of each detector can be just $A = A_{IP}/n$, and the integration period T_I can be just the frame time T_F and then $T_I = T_F$. Also in an imaging application $\phi = N$. The NEP for a single detector or element in the scene is then

$$NEP = \hbar\omega_s[4NA_{IP}/(n\eta T_F)]^{1/2} \quad . \tag{18}$$

This is a factor of $(n/2)^{1/2}$ smaller than that for a mechanically scanned single photodiode detector [12].

The signal to noise ratio can be found by taking the ratio of the signal current in the sample period, Eq. 12, to the root mean square noise current in the sample period, Eq. 11, to give

$$S/N = (nA\Phi T_I)^{1/2}/2 \tag{19}$$

The IRFET will saturate if the product of ΦT_I is too large. Saturation will be defined to occur when $T_I = 2\tau = 2/(\Phi\alpha) = 2/e_p^o$, and using $\eta = \varepsilon W_d N_{TT}$ then the maximum attainable signal to noise ratio is

$$S/N_{max} = (W_d N_{TT} A/2)^{1/2}. \tag{20}$$

The product of $W_d N_{TT}$ is just the change in charge density in the surface depletion region, if we let

$$N_s = W_d N_{TT} \tag{21}$$

then

$$S/N_{max} = (N_s A/2)^{1/2} \quad . \tag{22}$$

The maximum attainable signal to noise ratio depends only on the stored surface charge density and area of the device under shot noise or background limited operation. It is independent of the quantum efficiency, integration period, T_I and all other considerations. Furthermore, it can be shown that a similar expression applies to CID's and CCD's as well so that all surface type semiconductor devices have essentially the same maximum attainable signal to noise ratio since they all have comparable surface charge storage densities which are limited by the dielectric strength of the gate insulators or avalanche breakdown in the substrate.

EXPERIMENTAL APPARATUS

The device used in the measurements was made on (100) orientation silicon p-type substrate of 1-2Ω·cm resistivity and doped with a gold concentration of 2×10^{15} cm^{-3}. The gate oxide of the MOSFET is 4000 Å thick and the circular channel has an 8.17 W/L ratio providing an active area of 2.5×10^{-3} cm^2 [7,8]. By mounting the device on a TO-5 header fitted in a tubular reflective cavity, both frontside and edge illumination was possible. The details of operation of this specific example of a gold doped silicon IRFET employing the response of the donor level has been treated in detail in the literature [8]. In this case, τ, the time constant associated with the change in charge state of the gold donor level will be designated as τ_D, which is the reciprocal of the product of the incident photon flux and photoionization cross section [8].

The experimental arrangement and the equipment used in these measurements are shown in Fig. 2. The upper-corner frequency of the Hewlett-Packard DC MicroVolt-Ammeter 425A is 1-Hz(-3db), and the lower-corner frequency of the Krohn-Hite 3750 Filter (high pass) is adjustable from 0.02-Hz; therefore, the two instruments provide for a variable noise bandwidth. A Bausch and Lomb tungsten light source powered from a variac permitted various photon flux intensities. The output signal current and the accompanying noise was measured with the IRFET running continuously and recorded by a Houston Instrument Omnigraphic 2000 X-Y Recorder. A 1-μF DC-blocking capacitor was attached to the input of the X-Y recorder (1-MΩ input impedance) in order to eliminate any drift in the high-pass filter/volt meter output. This circuit attenuated all frequencies below 0.159-Hz, thus limiting the magnitude of the 1/f type noise. The incident photon flux was determined by noting the time t_F required for $|\Delta I_{DS}|$ to increase from 0.1 to 0.9 of its final value and this is shown in Figure 3.

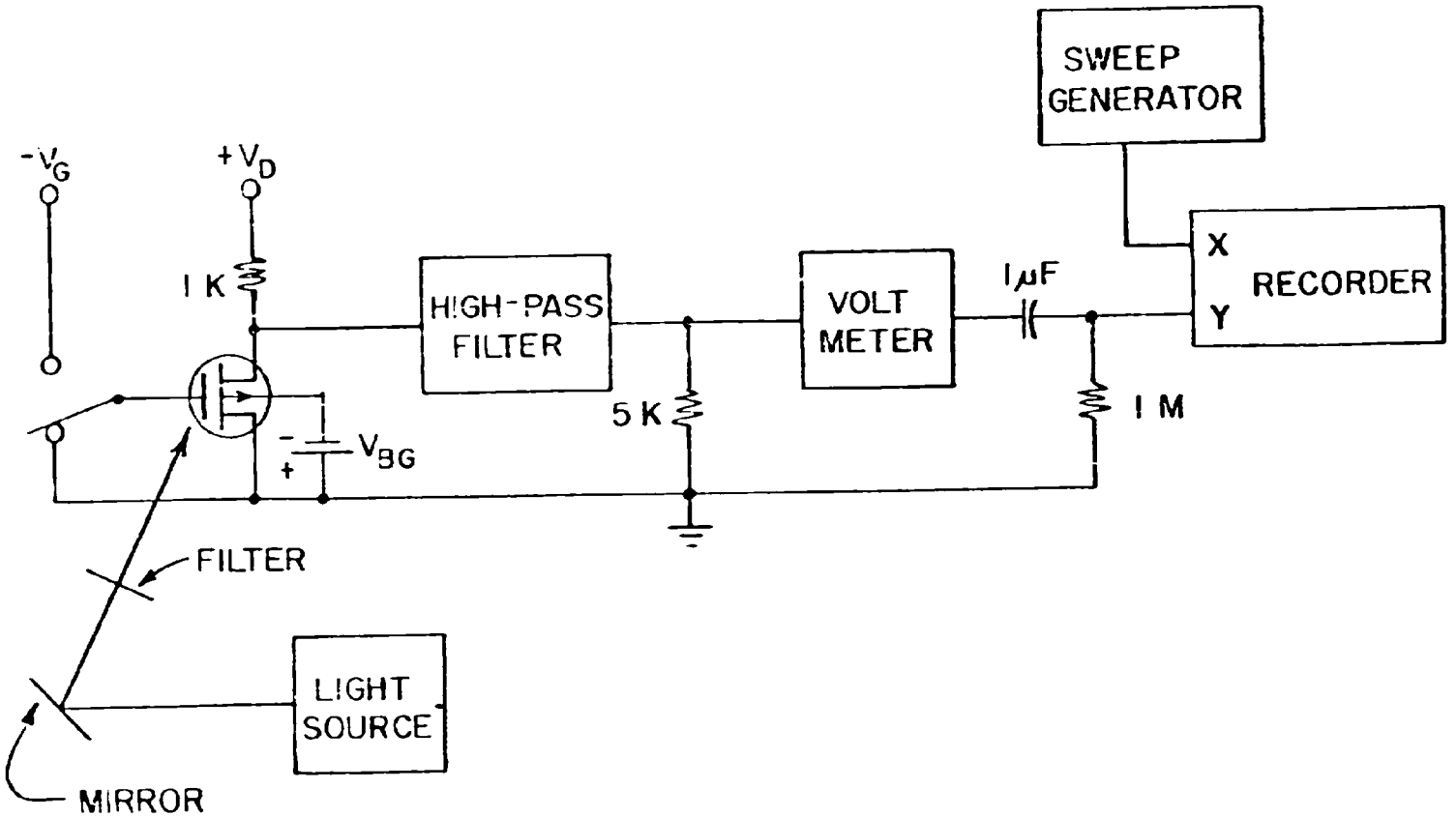

Fig.2. Experimental Apparatus used in the Noise Measurements. The IRFET IS cooled to 78.8°K.

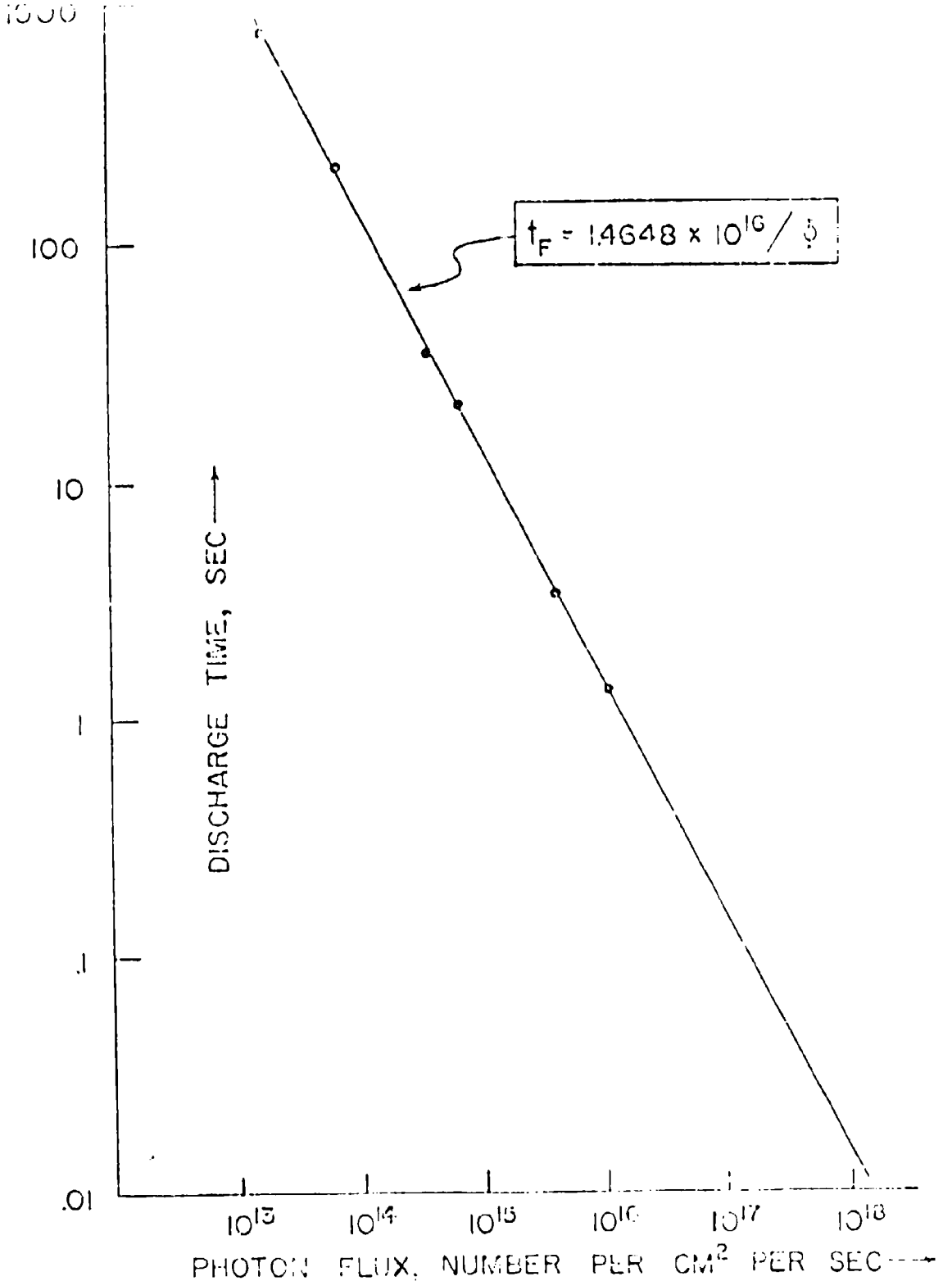

Fig. 3. Time Required for Gold Vectors to Discharge as a Function of Incident Photon Flux.

EXPERIMENTAL RESULTS

The overall system noise with the high-pass filter input shorted was about $8mV_{rms}$ at the voltmeter output. The IRFET was connected in a common source configuration with a precision 1 kΩ load resistor.

A. Interface-State Noise

The flow of electrons from one site to another in the surface channel of a MOSFET is a random process because of trapping and emission of carriers by interface states [13,14]. Slow interface states (oxide states) produce appreciable noise in IRFETs during long integration periods. Whenever the device is active, both fast and slow interface-state noises are present as a dark current with 1/f-type frequency dependence [13,14].

This dark-current noise was observed in different bandwidths for 170 sec by varying the lower corner frequency of the high-pass filter from 0.16 to 4 Hz (10 db gain after 1 Hz) and recording the RMS noise voltage across the 1 kΩ load resistor versus time. By taking the difference in noise current between two observations differing by Δf = 0.2 Hz and dividing by 0.2 Hz, the dark-current noise was specified for a given center frequency in a 0.2 Hz bandwidth. The results of this series of measurements are shown in Figure 4 (note that $1/f = T_I$). Fitting the experimental points to a straight line (method of least squares) indicates that the dark-current noise in a cooled IRFET varies approximately as $(1/f)^{1.8}$.

B. Shot Noise

By illuminating the IRFET with infrared light, the shot (or quantum) noise associated with the optically generated change in the channel-charge could be measured. A typical result comparing the measured dark-noise and

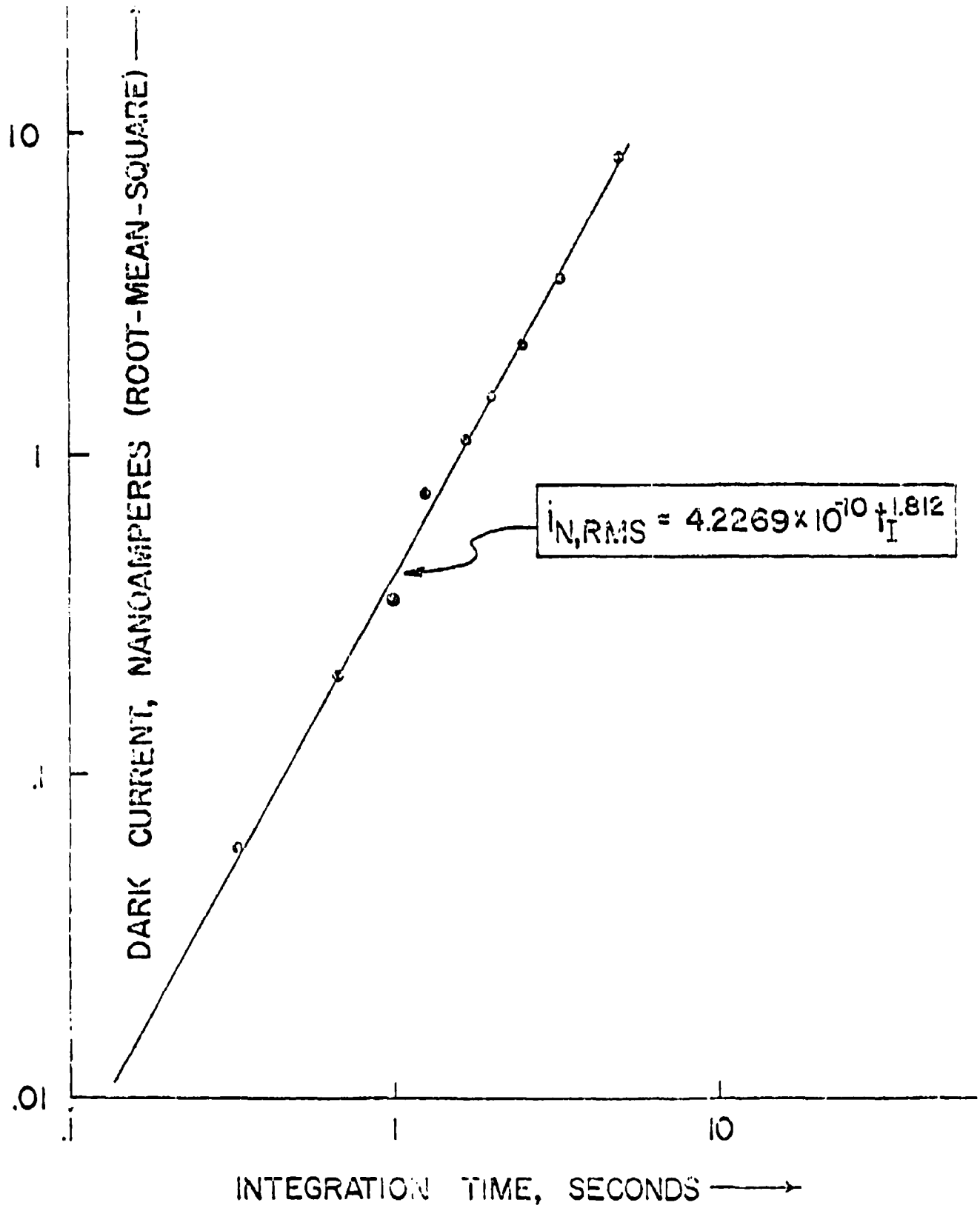

Fig 4. Dark Noise Current (1/f) Observed as a Function of Integration Time.

shot-noise currents in a bandwidth $\Delta\nu$ = 0.2 Hz is shown in Figure 5. During illumination the noise current is seen to eventually approach the dark noise level as the length of the integration time increases and the gold centers discharge. In order to observe the initial shot noise current immediately after the IRFET was illuminated, the time sacle can be expanded.

The expected shot noise current can be calculated by using Eqs. 11 and 4, and the expression for the maximum possible change in drain current [8]

$$\Delta I_{DS}^{m} = \mu C_o (W/L) \Delta V_T V_{DS} \tag{23}$$

which becomes after using Eq. 15

$$\Delta I_{DS}^{m} = \mu C_o (W/L) [q W_d N_{TT} V_{DS}/(2C_o)] \tag{24}$$

and then by using Eq. 11 and 8

$$(\bar{I}_{DSN}^2)^{1/2} = [2q\Delta I_{DS}^{m} I_{DS} (T_I/\tau_D)/(C_o(V_{GS} - V_T)A)]^{1/2}. \tag{25}$$

In reality, this expression has been developed assuming that the IRFET is operating in the linear region and a linear approximation has been applied to describe the time response. However, it will be used to calculate and show that the theoretical shot noise is of the same order as that observed in operation of the device even though the above conditions might not be rigidly adhered to. For Figure 5, I_{DS} is 1.8 mA, ΔI_{DS}^{m} is 0.4 mA, T_I a 100 seconds, τ_D is 100 seconds, C_o can be calculated from the oxide thickness of 4000 Å, the area A is 2.5 x 10^{-3} cm^2, and $(V_{GS} - V_T)$ is 12. 5 volts. This yields a root mean square noise current of 30 nA or a peak to peak noise current of 85 nA, when substitutions are made into Eq. 25. The actual shot noise observed in the first few seconds in Figure 5 after illumination is less than the order 300 nA peak to peak. Note that the time scale over

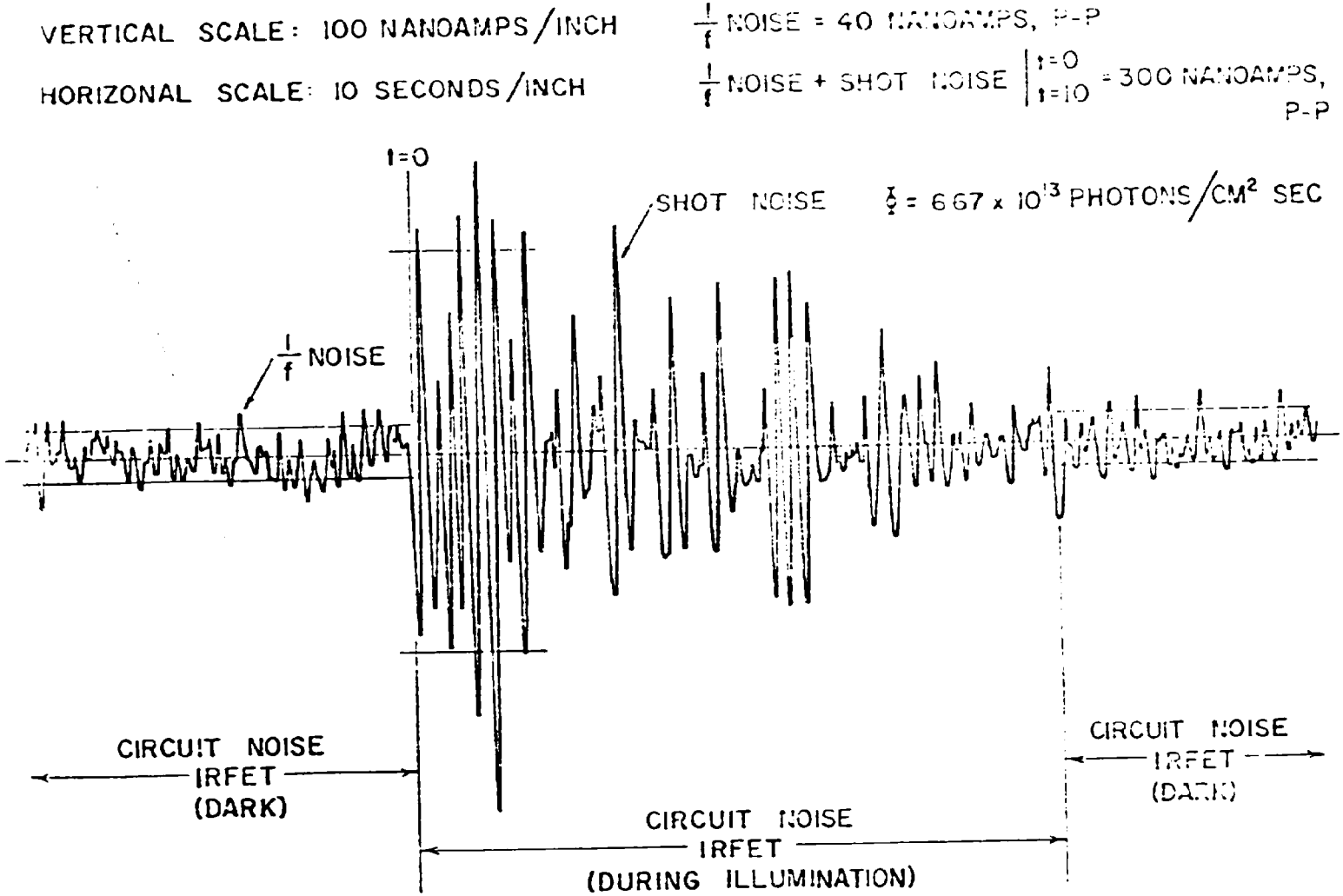

Fig. 5. Circuit Noise (Observed During Illumination and Integration Shot Noise current During Illumination) with Continuous Sampling.

which the current fluctuations are being plotted in Figure 5 is ten sec. per division. This rules out the use of a meter to determine the RMS value of the noise signal. The measured shot noise is expected to be somewhat larger than the calculated value due to the fact that the actual device is being operated in the saturation region rather than the linear region for which the theory has been developed to simplify the analysis.

The quantity $(\bar{I}^2_{DSN})^{1/2}$, given by Eq. 25 represents the uncertainty which occurs in the drain current at the end of the integration period, or at the beginning of a sample period as might occur in an application to read the conductivity state [6]. The fluctuations in Figure 5 during illumination are representative of this uncertainty. Note that the input circuit of the X-Y recorder limits 1/f type circuit noise to 40 nA peak to peak or approximately 12 nA RMS, due to the cut-off frequency of 0.159 Hz or time constant of 6.3 sec. Thus, shot noise could still be observed for long integration periods. The expected actual noise (1/f-type dominant) as would be seen by a static-change (DC) meter is much larger as will be shown in Figure 6.

Note that

$$\tau_D = 1/N\sigma \tag{26}$$

so that in Eq. 25 then, $(\bar{I}^2_{DSN})^{1/2}$ will increase with the incident photon flux. If the photon flux is kept constant, then the noise current increases with integration time in Eq. 25. The apparent decrease in shot noise is due to the actual non-linear time response of the device and discharge of an appreciable number of gold centers for times of the order τ_D. A signal-to-shot noise ratio can be calculated using Eq. 25 and the fact that

$$i_{signal} = \sqrt{I^m_{DS} T_I / \tau_D} \quad (\text{for } T_I \ll \tau_D) \tag{27}$$

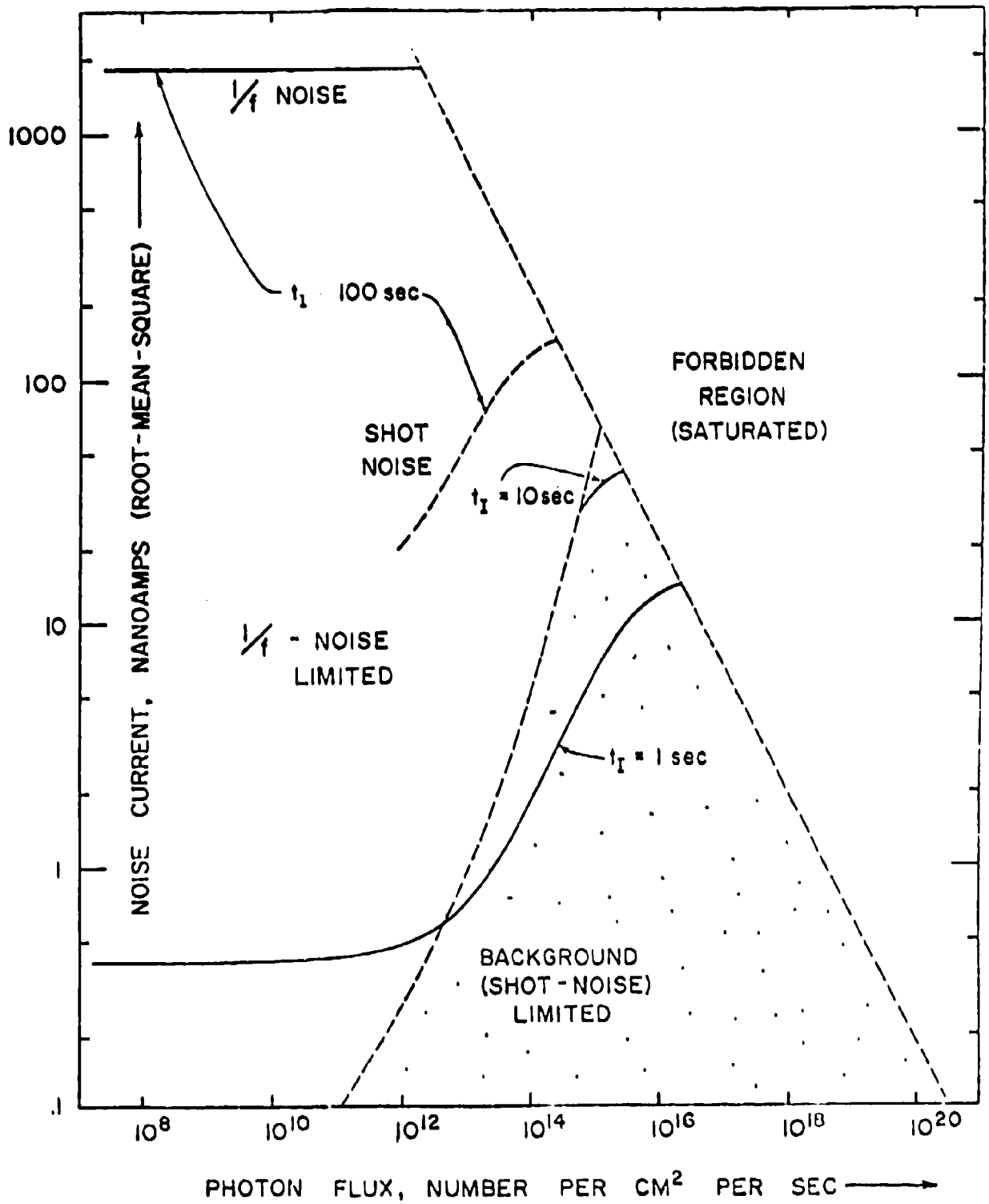

Fig. 6. Output Noise Current as a Function of Incident Photon Flux and Integration Time, Indicating the Three Different Operating Conditions.

to yield

$$S/N = [C_o(V_{GS} - V_T)/2q)(\Delta I^m_{DS}/I_{DS})(T_I/\tau_D)A]^{1/2}. \qquad (28)$$

The signal to noise ratio increases with both the ratio (T_I/τ_D) and the area A of the device. (Note the similarity to Eq. 22 for $T_I = 2\tau_D$.)

The expected drain-to-source RMS noise current has been plotted in Figure 6 for different integration times as a function of incident photon flux. The shot noise for a 100 second integration period is shown as a dotted line and the value of $300/2\sqrt{2}$ nA at a flux of 6.67×10^{13} photons/cm^2 sec. taken from Figure 5. The expected 1/f noise in this case is, however, much larger as obtained from extrapolating Figure 4 as 1800 nA and is shown as a solid line in Figure 6. For shorter integration periods the 1/f noise will be much smaller and the expected noise characteristics for integration periods of 1 and 10 seconds will be shot noise limited at the higher photon fluxes.

Figure 6 has been divided into three distinctly different regions which are representative of the different operating conditions. In the saturated region the photon flux is too large and the integration period too long to allow operation of the device as a photon detector, all the impurity centers discharge before the end of the integration period. In the 1/f noise limited region, which corresponds to low photon fluxes and long integration period, 1/f rather than shot noise is the limiting factor. In the shot noise or background limited region, which corresponds to relatively higher photon fluxes and shorter integration periods, shot noise due to the incident photon flux is the dominant noise mechanism. It is shown that shot noise or background limited operation of the IRFET can be achieved for integration periods of less than about 10 seconds or with photon fluxes above about 10^{15} cm^{-2} sec^{-1}. The results given in Figure 6 are representative of a given device

and similar characteristic curves would apply to other individual devices and no special effort has been made to minimize the surface state density and 1/f noise in these devices.

APPLICATION CONSIDERATIONS

The photon flux incident on a particular detector should be anticipated to vary by orders of magnitude depending upon the wavelength and type of application. In the case of gold-doped devices [8], it might be anticipated that in the near infrared photon fluxes may well be low unless the detector is being employed to localize a very hot source and the 1/f noise limit may be an important consideration. For gallium doped devices, on the other hand [10], employed in terrestial applications, the flux incident on the detector is $N = N_{300}(\lambda_c)/(4F^2)$. $N_{300}(\lambda_c)$ is the blackbody flux from a 300°K source integrated out to the longest wavelength of response of the impurity center, 17 μm in this case [1]. With F = 1.5 optics $N = 2 \times 10^{17}/cm^2$ sec and the time constant of discharge of the gallium centers would be $\tau = 1/(\sigma N)$ or approximately 16 milliseconds if an average photoionization cross section of $\sigma = 3 \times 10^{-16}/cm^2$ is used. In the case of gallium doped devices in terrestial applications, integration periods or frame times might be anticipated to be short and the shot noise or background limit apply. In this case, the 1/f noise limit is of little concern. Indium-doped devices [9,10,15] are intermediate to the above cases. In terrestial applications $N_{300}(8\mu m) = 2 \times 10^{17}$ and using an average photoionization cross section of $1.5 \times 10^{-16}/cm^2$ and F = 1.5 yields a time constant of 300 milliseconds.

Different considerations would of course apply in extra-terrestial applications and low flux densities may be incident at all wavelengths, in which case long integration periods might be employed and the 1/f noise limit applied.

CONCLUSIONS

It has been shown theoretically that under shot noise or background limited operation that the maximum attainable signal to noise ratio in the infrared sensing MOSFET (IRFET) is determined only by the area of the detector and the surface charge storage density. Equations describing the noise characteristics of this new type of integrating infrared detector have been developed and presented, assuming operation of the device in the linear region and employing a linear approximation to the time response of the device.

Noise measurements on a gold doped device empolying response of the gold donor level have identified the shot noise associated with the incident infrared signal and the 1/f noise inherent in the device itself. The regions of shot noise or background limited operation and 1/f noise limited operation have been delineated.

Although measurements have been made only on gold doped devices, similar results might be anticipated for both the indium and gallium doped infrared sensing MOSFETs. These results indicate that for shorter integration periods of around 10 seconds or less, shot noise or background limited operation of the IRFET should be possible in infrared detector and imaging applications.

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APPENDIX E

PUBLICATION LIST

PROFESSIONAL JOURNALS AND CONFERENCES

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United States Air Force
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