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MICROCIRCUIT RELIABILITY BIBLIOGRAPHY

VOLUME III. 1975 ANNUAL REFERENCE SUPPLEMENT

(DOCUMENT NUMBERS 10417-11044)

IIT RESEARCH INSTITUTE
CHICAGO, ILLINOIS

PREPARED FOR
ROME AIR DEVELOPMENT CENTER
GRIFFISS, NEW YORK

APRIL 1975

MRB 0474 Vol. III

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MICROCIRCUIT RELIABILITY BIBLIOGRAPHY

Volume III - 1975 ANNUAL REFERENCE SUPPLEMENT

(DOCUMENT NUMBERS - 10417 - 11044)

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Reliability Analysis Center
ROME AIR DEVELOPMENT CENTER

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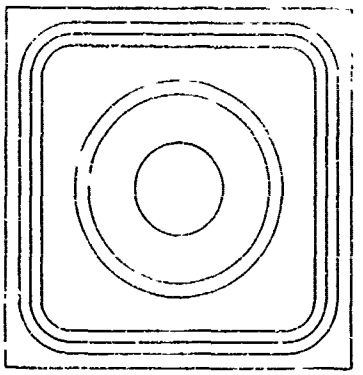

The Reliability Analysis Center (RAC) is a service for the dissemination of reliability and experience information on microcircuit devices, including integrated circuits, thick and thin film circuits, hybrid devices and large scale arrays (LSI) employed in military, space and commercial application.

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MICROCIRCUIT RELIABILITY BIBLIOGRAPHY

MRB 0474 Vol. III

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INTRODUCTION

GENERAL

The **Microcircuit Reliability Bibliography** references literature pertinent to the reliability of microcircuit technology Aspects found herein encompass design, fabrication, quality assurance and application. References are selected for citation from the Reliability Analysis Center document files. The portion of the collection presented here dates from acquisitions made during 1967 (the inception of the RAC) to March of this year. Documents are selected on the basis of informational currency and usefulness, as well as availability to the engineering community. Unpublished data and related matter not generally disseminated by the primary source or through government agencies (e.g. DDC or NTIS) or industry channels are excluded.

FORMAT

Volumes I-A, II and III comprise an updated index and complete set of abstract citations.

MRB Volume I--A: Cumulative Index, April 1975
MRB Volume II: Cumulative References, April 1974
MRB Volume III: 1975 Annual Reference Supplement, April 1975

The reader may discard volume I, MRB Index 1974, without loss since this information is now contained in Volume I-A.

Volume I--A: the Cumulative Index, is an index to material found in both volume II and volume III. Volume I-A (and previously volume I) is prepared in photo-ready format by computerized techniques.

Volume II: MRB Cumulative References provides complete coverage of RAC bibliographic citations through February 1974.

Volume III: MRB 1975 Annual Reference Supplement provides additional bibliographic coverage for the current year.

CONTENT

Volume I-A **Cumulative Index**

The index contains the following four sections:

Term Selection Guide
Subject Term Index
Corporate Author Index
Personal Author Index 1975

Section I **TERM SELECTION GUIDE:** contains subject terms selected from the RAC microcircuit Thesaurus. The terms are arranged in alphabetical order with sub-term description following each main term. Crossreferencing is extensive for the reader's convenience. The Selection Guide has been expanded this year to reflect some of the recent changes in technology.

Section II **SUBJECT TERM INDEX:** cross-references subject terms and the RAC assigned document identification numbers found in Volumes II and III. In addition, all documents are assigned by computer, to one or more of the following reliability related categories.

1. Failure Analysis: Evaluation of defects, and failure analysis techniques.
2. Test Procedures: Reliability Test techniques and procedures, including process control techniques.
3. Fabrication Method and Techniques: Reliability aspects of microcircuit manufacturing.
4. Reliability Studies: Technical reports relating to formal reliability studies and investigations.
5. Computer Analysis: Math Modeling & Prediction: Prediction and modeling, statistical tools, weibull analysis, computer analysis, computer aids, etc.
6. Miscellaneous: Cites references that were not designated in any of the above categories.

Section II is used to select citations from volumes II and III which are pertinent to the subject terms chosen. A Document identification number may appear in more than one category.

Section III **CORPORATE AUTHOR INDEX:** An alphabetical listing of selected corporate authors (i.e. names of organizations) originating documents. Each corporate author is followed by a listing of the appropriate RAC document identification numbers.

Section IV **PERSONAL AUTHOR INDEX 1975:** An alphabetical listing of personal authors found in the Annual Reference Supplement with corresponding citation title and RAC document identification number.

Volume: II and III **CUMULATIVE AND ANNUAL REFERENCES**

Volume II, MRB Cumulative References provides complete coverage of RAC bibliographic citations from 1967 through February 1974. References cited in Volume II are ordered sequentially with RAC assigned document identification numbers 1401 through 10414. Each citation includes (wherever possible) document title, author, source organization, identifying designations, in addition to a fully descriptive abstract of its content.

Volume III, MRB 1975 Annual Reference Supplement provides the additional bibliographic coverage from March 1974 to March 1975. RAC assigned document numbers for this publication are 10417 through 11044. The citation format is the same as is Volume II.

Gaps in the numbering sequence are due to selection. Because hard-to-acquire documents are not included, the cited references for certain subjects are necessarily incomplete. Thus, the RAC files may contain substantially more information or data than indicated in the bibliography. Complete data and guidance information are available from RAC published data compendia or direct consultation with RAC staff personnel.

ORDERING INFORMATION

The reader may order additional copies of the MRB or previously issued Volume II directly from the Reliability Analysis Center. Pricing information follows:

Current issues (Vol. I-A and Vol. III)	**$ 40.**	($80. foreign)
Complete three volume set (Vols. I-A, II, III)	**$ 50.**	($100. foreign)

HOW TO OBTAIN DOCUMENTS REFERENCED IN THIS BIBLIOGRAPHY

Each reference listed herein contains complete bibliographic information including the personal and corporate author with address. Where the document is available from one of the government document distribution centers listed below, the cited reference will include an order number (e.g. AD, N, DP, etc.). Other documents can be obtained from the original source (i.e. author, journal, society, etc.). **DOCUMENTS OTHER THAN THOSE PUBLISHED BY RAC CAN NOT BE OBTAINED FROM RAC.**

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Cameron Station
Alexandria, Virginia 22314
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OR to determine the availability of N documents:

NASA Scientific and Technical Information Facility
Post Office Box 8757
Baltimore/Washington International Airport
Maryland 21240
(301) 796-5300

HOW TO USE THE BIBLIOGRAPHY

PROCEDURE

1) Select a bibliographic term(s) from the **Term Selection Guide (Section I)** that most closely agrees with your subject interest.

2) Look up the selected term(s) in the categorized **Subject Term Index (Section II)** to obtain a list of document numbers.

   a) The terms of interest may be found under one or more categories. By choosing a category pertinent to your subject interest, a two-term logical AND is automatically achieved.

   b) Additional terms may also be utilized in combination for AND/OR logical searches. For an AND situation a document number must appear under EACH of the terms searched in order for it to satisfy the search criteria. For an OR situation, all document numbers appearing under any one of the terms searched satisfy the criteria. The terms may all be in a single category or the search may encompass several categories.

3) If interested in reports issued by a specific organization, locate them in the **Corporate Author Index (Section III)** and read corresponding document numbers. Corporate Author may be combined with subject terms for an AND or OR type search statement.

4) If interested in reports by a specific author issued after March 1, 1974 locate them in the **Personal Author Index (Section IV)** and read the corresponding titles and document numbers.

5) After pertinent document numbers are identified, go to Volume II or Volume III and read bibliographic and abstract information.

EXAMPLE SEARCH

Problem:

Suppose we are interested in locating references to help us evaluate our screening program.

Solution:

1) Scan the **Term Selection Guide** for subject terms related to the problem. We note the term SCREENING EFFECTIVENESS. We choose test procedures as the appropriate category and turn to category 2. of the **Subject Term Index (Section II)**, and read the document numbers under screening effectiveness. These are:

1741	4799	10052	10110	10247	10370	10669	10989
3040	4825	10060	10113	10251	10462	10738	11032
4757	4829	10063	10151	10254	10642	10976	
4759	10014	10095	10162	10258	10647	10980	

2) The bibliographic information and abstracts for the document numbers less than 10415 are found in Volume II. The remaining document numbers are found in Volume III.

3) Because of the number of references identified by this first search one might want to qualify the search further. Assuming we would like references related to a specific technology, such as complementary MOS the same procedure as above can be followed.

a) The **Term Selection Guide** indicates the term CMOS may be used.

b) Refer to Category 2, Test Procedures of the **Subject Term Index** and read the document numbers under CMOS.

c) Compare the two document number lists for common numbers. They are:

10063 10738 10989

These documents contain information pertinent to the combined question. The first citation (10063) is found in Volume II while the others are found in Volume III.

ADDITIONAL INFORMATION

The documents referenced may be acquired from the originator, the publisher or one of the government document dissemination agencies. Ordering details appear under: **HOW TO OBTAIN DOCUMENTS REFERENCED IN THIS BIBLIOGRAPHY.**

Please contact the RAC directly for further information concerning indepth literature searches, published reliability data compendia and technical consulting assistance.

10417

Pichler, H.H. (MIT. Lincoln Lab., Lexington, Mass.)
A BASIC THICK FILM CIRCUIT FOR CUSTOM LAYOUTS. Packaging and Production 10, no. 11, 86-92, Nov. 1970

A way to make a one-square-inch, gridded, thick-film circuit that holds as many as 50 integrated circuit chips and can be produced quickly at reasonable cost, has been developed. The key to the process was the development of a basic circuit board that has reduced the time and cost of producing custom layouts for individual circuit designers.

10418

Prokop, G.S. and Lieng, G. (IBM, System Prod. Div., East Fishkill Facility, Hopewell Junction, N.Y.)
STATISTICAL MODEL FOR ELECTROMIGRATION FAILURE AT ALUMINUM CONTACTS AND TERMINALS. J. of Electronic Matls. 1, no. 4, 474-98, 1972

The statistical model for electromigration failure in stripes developed by Attardo, Rutledge, and Jack has been extended to cover the case of terminals and contacts to silicon. By the use of computer simulation techniques, a model was developed that relates the time-to-failure and the distribution of failures to the magnitude of the structural divergence occuring at the diffusion barrier. The model predicts the previously unknown fact that for a constant grain size, a large standard deviation of the grain size at the contacts will retard electromigration and that the current density distribution at the contact does not affect mean time-to-failure.

10419

Miller, W.C. (Bendix Corp., Electrodynamics Div.) and Chain, D.W. (U.S. Navy, Nav. Undersea Res. and Dev. Center)
RELIABILITY CONSIDERATIONS IN HYBRID MICROCIRCUITS. Microelectronics 5, no. 1, 49-56, 1973

This paper examines some of the more significant reliability considerations that are peculiar to the hybrid-microcircuit industry. The problems that result from the use of specialized materials and processes are discussed, and the manner in which reliability testing and assessment are obscured by the electronic complexity of the hybrid microcircuit is described.

10420

Lutz, R.W., MacDougall, J.D., Hanson, J. W. et al. (Sprague Elec. Co., Worcester, Mass.)
NEW DEVELOPMENTS IN CONSUMER ICs. Microelectronics 4, no. 4, 3-9, Spring 1973. Western Electronics Show and Convention. Los Angeles, Calif., Sept. 1972. Sprague Tech. Paper no. TP 72-3.

The purpose of this paper will be to review present state-of-the-art technology, including the development of ion implantation as a present-day production tool, fully compatible with all present bipolar technology. Continuing development of implantation will be covered, which shows great promise for applications in a VHF varactor tuner, covering the 50 to 200 MH_z range. In addition, the evolvement of implantation makes possible compatible N and P channel MOS as well as CMOS with a minimum of additional processing.

10421

Barrington, J., Larry, J.R., Hicks, W.T. et al. (E. I. Du Pont de Nemours & Co., Inc., Electronic Prod. Div., Wilmington, Del.)
SOLDERABLE AND NON-SOLDERABLE MICROCIRCUIT CONDUCTORS: A STATUS REPORT. Microelectronics 4, no. 4, 10-4, Spring 1973

The thick-film microcircuit has matured rapidly in the last few years. Four basic metallurgies are presently available. Platinum-gold, palladium-gold, gold and palladium-silver have been available in a variety of vitreous binders with formulation changes being made to meet the ever new and unique needs of the industry which are summarized. With the advent of large scale integrated circuitry and the acceptance of hybrid technology as a major circuit manufacturing tool, the level of sophistication required to fabricate an acceptable thick-film conductor has risen sharply.

10422

Hosack, H.H. (GE, Syracuse, N.Y.)
PLATINUM SILICIDE--ALUMINUM SCHOTTKY DIODE CHARACTERISTICS. Appl. Phys. Letters 21, no. 5, 256-7, Sept. 15, 1972

The effects of heat treatment on platinum silicide Schottky diodes with aluminum metal contacts have been investigated. It has been found that the aluminum reacts with the silicide causing a change in the effective metal-semiconductor barrier height over a range of approximately 0.25 eV. Schottky diodes with initial platinum silicide characteristic of aluminum after extended heat treatments.

10423

Hittinger, W.C.
METAL-OXIDE-SEMICONDUCTOR TECHNOLOGY. Sci. Am. 229, no. 2, 48-57, Aug. 1973

The highest component densities are achieved by a fabrication technology known as MOS. The MOS technology produces transistors of the unipolar type in contradistinction to earlier junction transistors, which are bipolar. Bipolar transistors, use both electrons and "holes" (the absence of electrons) as carriers of electric charge; unipolar transistors use either electrons or holes, but not both. Fewer processing steps and a set of smaller minimum dimensions are needed for integrated circuits consisting of unipolar transistors than for circuits consisting of bipolar transistors. Most integrated circuits produced in the 1960's were of the bipolar type, but production of the newer unipolar type is growing rapidly.

10424

Morehead, F.F., Jr. and Crowder, B.L.
ION IMPLANTATION. Sci. Am. 228, no. 4, 65-71, Apr. 1973

The size of microelectronic circuits has decreased to the point where their surface dimensions are measured in microns (thousandths of a millimeter) and their thickness in angstroms (ten-millionths of a millimeter). In general shrinking the surface dimensions of an electronic device such as a transistor also requires shrinking the vertical dimensions. For example, to make transistors with surface dimensions on the order of micron requires the introduction of impurity atoms to within less than a micron of the surface. Such precise "doping" cannot readily be accomplished with the thermal-diffusion techniques that currently dominate the semiconductor market. Now, however, what was once only a research tool of nuclear physicists, the ion accelerator, offers a means of precisely implanting atoms of any desired species.

10425

Amelio, G.F.
CHARGE-COUPLED DEVICES. Sci. Am. 230, no. 2, 22-32, Feb. 1974

Like the transistor, the charge-coupled device is a concept of semiconductor electronics; as such it is su subject to the same physical laws that govern the transistor's dynamics and fabrication. That, however, is where the similarity ends. Although the charge-coupled device shares much the same technological base with its distinguished predecessor, it is a functional concept that focuses on the manipulation of information rather than on active concept that focuses on the modulation of electric currents.

10427

Thomas, R.W. and Moore, B.A. (U.S. Air Force, Griffiss AFB, RADC Reliability and Compatibility Div., Solid State Appl. Sect., Rome, N.Y.)
UNIQUE RELIABILITY ANALYSIS CAPABILITY. 26 pp.

A unique reliability analysis capability has been developed in-house at RADC. The system measures small amounts of gasecus contaminants that may be trapped inside hermetically-sealed microelectronic packages. Generally such containers are filled with pure dry nitrogen. From analysis of field failures, water was identified as a contaminant and essential component in many failure mechanisms. Other contaminants such as hydrogen and oxygen ray have long term degrading effects and are the subject of future research. The system consists of a mass spectrometer, a small dedicated computer and the package opening chamber. Packages are baked out under vacumnn prior to opening. When background gas levels have been established, a steel pin is used to either puncture or split the package open. The computer then samples the gas coming out of the package, applies sensitivity factors, subtracts background and produces a hard copy of the gas analysis.

10428

Harman, G.G. and Kessler, H. (U.S. Dept. of Commerce, Natl. Bur. of Standards, Electronic Technol. Div., Washington, D.C.)
APPLICATION OF CAPACITOR MICROPHONES AND MAGNETIC PICKUPS TO THE TUNING AND TROUBLE SHOOTING OF MICROELECTRONIC ULTRASONIC BONDING EQUIPMENT. NBS Tech. Note 573, 22 pp., May 1971

Microelectronic ultrasonic wire bonding equipment typically welds wires to integrated circuits at frequencies between 50 and 65 kHz. Mechanical vibrations at these frequencies are difficult to measure directly and malfunctions of the system may not be recognized. Two different methods of measuring these vibrations are described. The first method involves use of a capacitor microphone and a tapered tip, and the second method use of a small magnetic pickup. Procedures are given for establishing a specific ultrasonic vibration amplitude, tuning the ultrasonic system to resonance, and diagnosing both mechanical and electrical problems in wire bonding equipment.

10429

Glendinning, W.B. (U.S. Army, ECOM, Electronics Technol. and Devices Lab., Semiconductor Devices and Integrated Electronics Tech. Area, Fort Monmouth, N.J.) and Yarbrough, D.W. (Tenn. Technol. U., Chem. Eng. Dept., Cookeville, Tenn.)
LOW TEMPERATURE FORMATION OF SILICON OXIDE. Rept. no. ECOM-4181, Res. and Dev. Tech. Rept., 7 pp., Dec. 1973. Thin Solid Films 18, 321-7, 1973

Silicon oxide films have been formed at temperatures as low as 25°C, using a reaction of Si with a vapor mixture containing either NO, HF and H_2O or NO, HF, H_2O and O_2. Experimental data relating silicon oxide film growth of silicon oxide films of specific thicknesses are outlined.

10431

Cappon, A. and Wegener, H.A.R. (Sperry Res. Center, Sudbury, Mass.)
ADVANCED SOLID STATE METAL NITRIDE OXIDE SILICON (MNOS) MEMORY.
Rept. no. AFAL-TR-73-191,
Rept. no. SCRC-CR-73-5, Final Rept., June 28, 1971-May 1, 1973, 47 pp., June 1973. AD 912 837L. F33615-71-C-1790

The purpose of this program is the design and fabrication of a random-access memory utilizing fully decoded chips containing 2048 bits of MNOS memory devices. The performance goal for these chips are a read time of 250 ns and a write time of 1.0 µs.

10433

Anderson, R.T. and Schiller, J.J. (IIT Res. Inst., Chicago, Ill.)
RELIABILITY ASSESSMENT OF ELECTRONIC ASSEMBLY OF XM 433 FUZE. Final Rept., 60 pp., Mar. 1974. DAAA 21-74-C-0015

The objective of this study was to quantitatively evaluate Picatinny Electronic Fuze Assembly No. 9260685 and selected alternate packaging approaches. with respect to reliability and cost. Meeting this objective required the performance of several study tasks consisting of combinations of analytical techniques and refined engineering judgments leading to values for reliability and cost for each packaging configuration evaluated.

10434

Rom, J.F. (Grumman Aerospace Corp., Reliability & Maintainability Sect.)
COMPARISON OF MIL-STD-1600 WITH RADC NOTEBOOK FOR MICROCIRCUIT RELIABILITY PREDICTIONS. Tech. Paper no. R&M-73-STP-2*5-14-73, 9 pp.

MIL-STD-1600, reference (a) indirectly draws the conclusion that the failure rate of bipolar microcircuits decreases with equipment operating time. Failure rate calculations performed in accordance with this military standard consider field operating time and equipment level burn-in, but do not specifically consider device complexity, construction, application or environment. Microcircuit reliability predictions using the procedure in reference (a) were compared with those derived from the procedures in the RADC Notebook, reference (b). In general, failure rates of monolithic integrated circuits calculated in accordance with reference (a) are more optimistic than those computer per the procedures of reference (b).

10435

Citrin, D.A. (GE, Ordnance Systems, Pittsfield, Mass.)
ELECTRICAL CHARACTERIZATION OF COMPLEX MICROCIRCUITS. Rept. no. RADC-TR-73-373, Final Rept., June 1972-June 1973, 354 pp., Jan. 1974. F30602-72-C-0474

The objective of this study has been to develop guidelines for the electrical characterization and testing of microcircuits of varying degrees of complexity and to aid in assuring conformance to their detailed specification. The 4000 series of CMOS circuits, 9500 and 10,000 series of ECL circuits, Schottky T^2L circuits, and a Phase Locked Loop were electrically characterized according to their DC, switching and functional characteristics, vendor comparisons, specification guidelines, test circuits and design rules are included for each family where applicable. Studies in sufficient detail were performed to form the basis for the generation of MIL-M-38510 slash sheets for interchangeable parts for military use.

10437

Lampert, M.A., Johnson, W.C. and Bottoms, W.R. (Princeton U., Dept. of Elec. Eng., Princeton, N.J.)
STUDY OF ELECTRONIC TRANSPORT AND BREAKDOWN IN THIN INSULATING FILMS.
Rept. no. AFCRL-TR-73-0263, Semi-Ann. Rept. no. 1, 91 pp., Jan. 1973
Rept. no. AFCRL-TR-74-0076
Rept. no. PU-DPL no. 26, Semi-Ann. Rept. no. 2, 120 pp., July 1973.
F19628-72-C-0298

A comprehensive research program is under way for the characterization of electronic transport and dielectric breakdown properties of thin insulating films on Si which are technologically important, namely SiO_2, Al_2O_3, Si_3N_4 and their composites. The main experimental approaches are:

i) Non-destructive
ii) Locally destructive
iii) Optical charge
iv) Kilovolt electron-beam probe studies

Accompanying theoretical studies initially are concerned with Monte Carlo calculations of hot-electron distributions induced by high electric fields in the film.

10445

Pocock, D.N., Krebs, M.G. and Perkins, C.W. (Northrop Res. and Technol. Center, Hawthorne, Calif.)
SIMPLIFIED MICROCIRCUIT MODELING.
Rept. no. AFWL-TR-73-272, Final Rept., May 31, 1972-Nov. 14, 1973, 260 pp., Mar. 1974. AD 777 896. N74-29607
F29601-72-C-0092

The objective of this program was to evaluate the previously developed simplified modeling procedures by applying the techniques to develop radiation-inclusive models of analog and digital microcircuits of Large-Scale Integrated (LSI) and Medium-Scale Integrated (MSI) complexity for use with the SCEPTRE circuit-analysis program. The microcircuits that were modeled in this program are: 1) four-bit TTL up/down counter, T.I. SN54190; 2) four-bit COS/MOS adder, RCA CD4008; 3) low level amplifier, Rad. Inc. 116313; 4) voltage clamp amplifier, Rad. Inc. 116314; 5) boot-strap amplifier, Rad. Inc. 116315; 6) video/buffer amplifier, Rad. Inc. 116317, and 7) voltage comparator, Rad. Inc. 116316. The goal was to develop simplified models of the above microcircuits that would represent their electrical performance and ionizing radiation vulnerability to within engineering accuracy.(i.e., $\pm$ 20%). The up/down counter and the video/buffer amplifier models were also extended to include neutron degradation.

10449

Lockheed Missiles & Space Co., Inc., Sunnyvale, Calif.
PARTS, MATERIALS, AND PROCESSES EXPERIENCE SUMMARY. Rept. no. CR114391, 374 pp., Feb. 24, 1972. Vol. I & II.
Rept. no. NASA SP-6507, 1973. NAS2-6060

The objective of this summary is to provide users with the accumulated experience resulting from the ALERT reports issued by NASA and the Government-Industry Data Exchange Program (GIDEP). Related industry experience has also been included to provide the user with information available to the contractor at the time of preparation. The ALERT program has as its basic objective the avoidance, or at least the minimization, of the recurrences of parts, materials, and processes problems; thus improving the reliability of equipment produced for and used by the Government. A logical sequence for assistance in the selection and application of parts, materials, and processes is provided.

10452

Engbert, W. (AEG Telefunken, Ger.)
COMPARISON OF MOS AND BIPOLAR LSI-TECHNOLOGY. 10 pp. AGARD Symposium. Hague Neth., Nov. 1970

A flow chart of the production of bipolar and MOS circuits is represented in a comparitive manner. The production actions are classified as to costs and possible sources of failures. Remedial measures can be taken by projection masking, described in detail. Nevertheless the costs of wiring, made discretionary to shunt incorrect areas of the slice, are very high. New techniques are picked out, which promise higher yield, more packing density, better performance of the circuits. These are ion implantation, planoxide structuration, replacement of metal gates in "MOS" circuits by silicon on spinel deposition. The German works are pointed out.

10453

Foss, R.C. (Microsystems Internatl. Ltd., Ottawa, Ontario, Can.)
ECONOMIC CONSIDERATIONS IN L.S.I. DESIGN. 7 pp. AGARD Symposium. Hague Neth., Nov. 1970

It is now economically attractive to manufacture integrated circuits whose complexity far exceeds that of simple standard logic functions. L.S.I. circuits, particularly in M.O.S. form, offer a cost-per-function which is an order of magnitude lower than conventional integrated circuits with greater savings if the special needs for L.S.I. realization are noted. The paper outlines these needs and also shows how the optimum manufacturing cost can occur at levels of integration close to the point of manufacturing impracticability. The significance of this paradox is discussed from the user's viewpoint with reference to problems such as throw-away cost and development time-scales. The paper also compares various design approaches to L.S.I. circuits and concludes that the situation is essentially evolutionary rather than a revolutionary change.

10454

Nakamura, Y.
A NEW GOLD METALLIZATION SYSTEM. NEC Res. & Dev., no. 31, pp. 64-71, Oct. 1973

In order to solve the problems of the beam-lead metallization system, the new gold metallization system has been developed and prospects for its practical use are looking up. The system has been realized by giving chromium a lot of functions. Fabrication features, such as that the ohmic contact to silicon is provided by chromium, and gold plating can be carried out selectively on the platinum layer without masking, have not only contributed to improvement of fabrication yield and quality for devices, but transistor performance and reliability have also improved.

10455

Mojtehedi, I. and Breeding, G. (Monsanto, Electronic Spec. Prod.)
HIGH SPEED AND LOW COST MAKE LED's A TOP CONTENDER. Electronic Prod. 16, no. 10, 5 pp., Mar. 18, 1974

LED's are rugged solid state devices that offer the user reliability and long service life even in atmospheres of vibration and shock. For the designer, LED's have several advantages. TTL compatibility makes them easy to drive and interface; high speed response makes them easy to multplex. Moreover, they come in a variety of colors and are available from multiple sources.

10458

Terrell, B.H. (Tex. Instr. Inc., Semiconductor Group, Dallas, Tex.)
PRODUCTION ENGINEERING MEASURE FOR AN INTEGRATED POWER SWITCH (IPS). Rept. no. 03-74-01, Quart. Rept. no. 2, July 18-Oct. 17, 1973, 26 pp., Jan. 1974. DAAB05-73-C-2063.

This report covers the effort expended and performance achieved in the establishment of a production capability for a universally applicable switching component for use in precision power-conversion equipment. In the past, weight reduction has been achieved through complexity and the associated difficulties of serviceability by semi-skilled personnel. It is hoped that future precision power conditioners will eventually use interchangeable switching components such as the Integrated Power Switch (IPS).

10459

Wegener, H.A.R., Doig, M.B. and Lodi, R. (Sperry Rand Res. Center, Sudbury, Mass.)
HIGH RELIABILITY NON-VOLATILE INTEGRATED MEMORIES. Rept. no. ECOM-0298-1, Rept. no. SRRC-CR-71-13, Quart. Rept. no. 1, July 1-Sept. 30, 1971, 24 pp., Dec. 1971. AD 891 560L
Rept. no. ECOM-0298-2, Rept. no. SRRC-CR-72-8, Quart. Rept. no. 2, Oct. 1-Dec. 31, 1971, 26 pp., June 1972. AD 902 483L Rept. no. ECOM-0298-3, Rept. no. SRRC-72-10, Quart. Rept. no. 3, Jan. 1-Mar. 31, 1972, 33 pp., Sept. 1972. AD 904 517L Rept. no. ECOM-0298-F Rept. no. SCRC-CR-73-4, Final Tech. Rept., July 1, 1971-Dec. 19, 1972, 88 pp., May 1973. AD 910 444L.
DAAB07-71-C-0298

The technical program for this contract can be simply divided into four parts: The first deals with the variation of the properties of silicon nitride in order to improve the memory characteristics of the MNOS transistor. The second part is concerned with the verification of the improvement afforded by new nitrides. This involves the fabrication and testing of memory transistors. The other two parts, the fabrication and testing of 1280-bit circuits were the subject of our effort in the second half of this contract.

10460

RCA, Electronic Components, Harrison, N.J.
A PRODUCTION ENGINEERING MEASURE FOR TWO L-BAND SOLID-STATE MICROWAVE FREQUENCY SOURCES. Rept. no. ECR-428-5, Quart. Rept. no. 5, Feb. 1-Apr. 30, 1973, 33 pp., July 15, 1973. AD 913 796L.
DAAB05-72-C-5830

A Production Engineering Measure (PEM) for two L-Band Solid-State Microwave Frequency Sources has been continued. These two devices are a Radiosonde Modulator/Transmitter and an FM Power Source. Permission was received to initiate work on first article units for the Radiosonde Modulator/Transmitter. Material has been procured and tooling is being fabricated. Delivery of the second set of FM Source engineering models has been delayed by the need to further revise the oscillator/amplifier interface. Two models have been delivered for system evaluation.

10462

Straub, R.J. (Gen. Motors Corp., Delco Electronics Div., Milwaukee, Misc.) and Farrell, J.P. (U.S. Air Force, Griffiss AFB, RADC Rome, N.Y.)
THE EFFECTIVITY OF SCREENING HYBRID MICROCIRCUITS PER MIL-STD-883. pp. 17-26. Proceedings 1971, 21st Electronic Components Conference. Sponsored by the IEEE Parts Material and Packaging Group and the Electronic Industries Association. Statler Hilton, Washington, D.C., 544 pp., May 10-12, 1971

This paper summarizes fallout data acquired from application of Method 5004 screening procedures, first for the Class C level, and then for the Class B and A levels. Results are also shown of a Quality Conformance Inspection of identified Class A-devices. The specimens tested were 2,249 hybrid microcircuits obtained from 3 suppliers in 2 circuit configurations. For each environmental or mechanical exposure, fallout was recorded and failure mechan mechanism determined.

10463

Anon.
SCANNING ELECTRON MICROSCOPY/1970. PROCEEDINGS OF THE 3RD ANNUAL SCANNING ELECTRON MICROSCOPE SYMPOSIUM. Sponsored by IIT Res. Inst., Metals Res. Div., Chicago, Ill., 534 pp., Apr. 28-30, 1970

Presentations:
- Investigation of Current-Induced Mass Transport in Thin Metal Conducting Stripes
- Some Applications of the SEM to the Study of Sputter Etching and Photoresists
- Pseudo-Kikuchi Pattern Degradation of (111) Gallium Arsenide Induced by 60-kev Cadium Ion Bombardment
- A Technique for Accurate Measurement and Display of Applied Potential Distributions Using the Scanning Electron Microscope
- Voltage Measurement in the Scanning Electron Microscope
- Potential Mapping Using Auger Electron Spectroscopy'
- Electron Channeling Effects Using the SEM
- Electron Fractography of Crystalline and Polycrystalline Ti-Mo Wires Using Scanning Electron Microscopy

10464

Devaney, J.R. (JPL, Calif. Inst. of Technol., Pasadena, Calif.)
INVESTIGATION OF CURRENT-INDUCED MASS TRANSPORT IN THIN METAL CONDUCTING STRIPES. pp. 417, 419-24. NAS 7-100. Electron Microscopy/1970. Proceedings of the 3rd Annual Syposium. Sponsored by IIT Res. Inst., Metals Res. Div., Chicago, Ill., 534 pp., Apr. 28-30, 1970

This paper interprets the results obtained when thin metal conducting stripes of molybdenum-gold and aluminum were current stressed while being viewed at high magnifications through the scanning electron microscope. To facilitate this, photographs were taken at a rate of one per minute and then used to produce a motion picture. When viewed, this allows real time study of reactions which occurred over extended periods of time. They study of these motion pictures confirmed some of the existing theories of void formation but has also resulted in a reevaluation of the subsequent movement of the voids along the conductor. The overall result of the experiment has been a greatly enhanced understanding of mass transport in conducting stripes.

10465

Fried, L.J. and Flachbart, R.H. (IBM, Components Div., East Fishkill Facility, Hopewell Junction, N.Y.)
SOME APPLICATIONS OF THE SEM TO THE STUDY OF SPUTTER ETCHING AND PHOTORESISTS. pp. 425, 427-32. Scanning Electron Microscopy/1970. Proceedings of the 3rd Annual Symposium. Sponsored by IIT Res. Inst., Metals Res. Div., Chicago, Ill., 534 pp., Apr. 28-30, 1970

In recent years sputter etching has often replaced chemical etching as a method of forming fine geometry patterns in thin films of composite metallization. This paper describes the use of the SEM to study effects of sputter etching of composite Cr-Cu-Cr films and on the photoresist which was used as a mask. In addition, the observance of fringes in exposed and developed photoresist is discussed, and the mechanism due to standing wave interference is given.

10466

Banbury, J.R. and Nixon, W.C. (Cambridge U., Eng. Dept., Cambridge, Engl.)
VOLTAGE MEASUREMENT IN THE SCANNING ELECTRON MICROSCOPE. pp. 473, 475-80. Electron Microscopy/1970. Proceedings of the 3rd Annual Symposium. Sponsored by IIT Res. Inst., Metals Res. Div., Chicago, Ill., 534 pp., Apr. 28-30, 1970

A new detector has been used in the scanning electron microscope to provide potential contrast, with low sensitivity, to transver electric fields combined with high collection efficiency. The voltage characteristic in monotonic over at least + 20 volts, the range of interest for microcircuit inspection, and represents a step toward calibrated voltage measurement as distinct from simple voltage observation.

10467

MacDonald, N.C. (No. Am. Rockwell, Sci. Center, Thousand Oaks, Calif.)
POTENTIAL MAPPING USING AUGER ELECTRON SPECTROSCOPY. pp. 481, 483-5. Scanning Electron Microscopy/1970. Proceedings of the 3rd Annual Symposium. Sponsored by the IIT Res. Inst., Metals Div., Chicago, Ill., 534 pp., Apr. 28-30 1970

A new method for the measurement of surface potential is described. The shift in the energy of a differentiated Auger electron peak is used to measure the potential on the surface of a specimen. The potential mapping is automated by using an on-line computer to control the primary beam, to record and signal average the Auger peaks, and to display the potential mapping data in printed and graphic formats.

10471

Viswanathan, C.R. (U. of Calif., Dept. of Elec. Sci. and Eng., Los Angeles, Calif.) and Howes, R. and Hinkle, O. (Silicon Gen., Inc., Westminster, Calif.)
MOS-CV TEST SYSTEM FOR IC PROCESS CONTROL AND MONITORING. Solid State Technol. 17, no. 3, 5 pp., Mar. 1974

An MOS-CV system capable of monitoring and evaluating various processing steps and quality of material used in IC technology is described. This system has been found very useful in identifying processing steps giving rise to mobile ion contamination. It permits measurements of various parameters such as the minority carrier lifetime, surface-state density, mobile ion contamination level, and impurity concentration profile.

10472

Abbe, R.C. (ADE Corp., Walertown, Mass.)
SEMICONDUCTOR WAFER MEASUREMENTS. Solid State Technol. 17, no. 3, 47-50, Mar. 1974

The introduction of proven electronic gates and non-contact transducer probes into the high-volume manufacturing of wafers has answered the requirements for a rapid, error free, non-desctructive, non-contaminating dimensional testing technique. Now effective 100% in-process dimensional quality control is a reality, and at reasonable operating costs.

10473

Ardezzone, F.J. (Prove-Rite, Inc., Santa Clara, Calif.)
PROBE PARAMETERS AND CONSIDERATIONS. Solid State Technol. 17, no. 3, 51-7, Mar. 1974

A compilation of data and techniques applicable to semiconductor probing is presented. Comparisons are made among systems tapes and kinds of probes as well as materials in each. Aspects of inking, probe cards, and adjustable probes are discussed. Op Operator pitfalls and preventive techniques are outlined, and system related limitations as well as advantages are pointed out.

10476

Slusser, E.A. (Aerocronic Assoc., Inc., Contoocook, N.H.)
SELECTING A BURN-IN SYSTEM. Evaluation Eng., pp. 20-1, Sept./Oct. 1971

This article briefly covers the screening program, but places emphasis on the burn-in system because the burn-in system has the ability to induce infant failures.

10478

Fletcher, B.C. (JPL, Calif. Inst. of Technol., Pasadena, Calif.)
EVALUATION OF ERRORS IN PRIOR MEAN AND VARIANCE IN THE ESTIMATION OF INTEGRATED CIRCUIT FAILURE RATES USING BAYESIAN METHODS. Rept. no. NASA-CR-133227, JPL Tech. Mem. no. 33-614, 65 pp., June 1, 1972. N73-26203. NAS 7-100

This report is a study of the effects of prior data on a Bayesian analysis. Comparisons of the Maximum Likelihood estimator. The Bayesian estimator and the known failure rate are presented. The results of the many simulated trials are then analyzed to show the region of criticality for prior information being supplied to the Bayesian estimator. In particular, effects of prior mean and variance are determined as a function of the amount of test data available.

10479

Southward, H.D. and Broell, F., Jr. (U. of New Mex., Elec. Eng. Dept., Albuquerque, New Mex.)
MICROELECTRONIC TECHNIQUE AND REQUIREMENTS FOR THE SPECIAL WEAPONS CENTER MICROELECTRONICS FACILITY.
Rept. no. AFSWC-TR-72-53, Tech. Rept., Mar. 15, 1967-Feb. 16, 1971, 89 pp., Nov. 1972. AD 752 216. N73-17216.
F29601-67-C-0057

This report discusses three major topics: (1) the physical limitations of solid state devices in some of the environments in which a circuit would be expected to operate; (2) the major experimental work and procedures which should be recorded for use of facility personnel; and (3) the recommendations on equipment and personnel requirements. The physical limitations of components used in hybrid microcircuits are reviewed. Consideration is given to effects of temperature, ionizing radiation, atomic displacement and pulsed power failure of junctions. Facility objectives and requirements of the microelectronics facility are discussed and recommendations on equipment and personnel requirements are made.

10480

R.M., Kietzer, J.E. and Brandt, [illegible] K. (IIT Res. Inst., Chicago, Ill.)
DIELECTRIC WAVEGUIDE CONTROL SYSTEM DATA BUS SYSTEM. Final Rept., 50 pp., F33615-73-C-0263

The design of the Model 400 Data Bus System is presented along with a description of system components. The results of system evaluation tests are given as well as a detailed explanation of the rationale for selecting this approach. Possible expansion of the demonstration model is also discussed.

10481

Dumin, D.J. (INSELEK, Princeton, N.J.)
SILICON ON SAPPHIRE PHOTO CURRENT DEVICES. 24 pp. F29601-72-C-0094

Silicon-On-Sapphire for photo current experiments have been fabricated using clean SOS/MOS processing techniques. Four device geometries were fabricated in both P and N-type Silicon-on-Sapphire films. These devices included P-channel MOS transistors, N-Channel MOS transistors, Schottky barrier diodes, diffused diodes, capacitors, and adjacent silicon islands. All devices were tested and found to be representative of current state-of-the-art SOS/MOS processing capabilities.

10484

Schwuttke, G.H. (IBM, System Prod. Div., East Fishkill Labs., Hopewell Junction, N.Y.)
DAMAGE PROFILES IN SILICON AND THEIR IMPACT ON DEVICE RELIABILITY. Rept. no. TR 22.1588, June 6-Dec. 30, 1972, 25 pp., Jan. 1, 1973. AD 756 250. N73-22690.
DAHC15-72-C-0274

Standard silicon wafers are shown to frequently contain residual mechanical saw damage in the surface. The damage is identified through TEM analysis as microsplits of the silicon lattice. Microsplits are not detectable by standard inspection, screening or etching techniques. Microsplit dimensions range from 0.1 to 1 μm. The density of the splits can vary from zero to $10^6/cm^2$ or even higher. Microsplits are shown to cause loss of storage time in MOS capacitors.

10485

Anon.
PROCEEDINGS OF THE TECHNICAL PROGRAM. 1970 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

Sessions

I	Connectors and Connection Techniques
II	Printed Circuit and Multilayer Board Design and Manufacture
III	Wafer Fabrication in Monolithic Technology
IV	Systems Approach to Automated Testing
V	Integrated and Hybrid Microcircuit Packaging
VI	Chemicals and Materials for Microcircuits
VII	Packaging of Microwave Devices
VIII	Interfacing with Automated Test Equipment
IX	Packaging of High Speed Computers
X	Innovative Packaging Techniques
XI	Advanced Manufacturing Techniques
XII	Methods and Approaches to Automated Testing
XIII	Packaging for U.S. Super Jet Liners of the '70's

10486

Duffek, E.F. (Fairchild Semiconductor, Packaging Dev., Equip. Eng. Dept.)
AN ELECTROPLATING PROCESS FOR THE FABRICATION OF DOUBLE LAYER METALLIZED CERAMICS. pp. 2-79 - 2-87. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

Resistivity measurements performed on the double-layer substrates gave 1-3mΩ/sq. Via resistances were not noted. Brazed lead peel strengths ranged from 2-6 lbs. Hermeticity valves were within the $1X10^{-8}$cc/s, requirement for the adhesive seal. Feasibility of making a high-conductivity, double-layer substrate was shown by this work. Strict controls were required on all processes but the process does show good manufacturing potential.

10487

Wilson, R.W. and Terry, L.E. (Motorola, Semiconductor Prod. Div., Central Res. Labs., Phoenix, Ariz.)
METALLIZATION SYSTEMS FOR INTEGRATED CIRCUITS. pp. 3-1 - 3-15. A70-44533. NAS12-132. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970. Electronic Packaging and Production 10, no. 10, MC29-MC40, Oct. 1970

A metallization system must satisfy certain conditions if it is to be used in the fabrication of semiconductor devices. These conditions or constraints are as follows:

A. The material should have a high conductivity ($\rho \leq 10$ μ Ω/cm).
B. It should have good adhesion to both the semiconductor material and to thermally grown or deposited dielectric films.
C. The metal or metals should be free from degrading intermetallic compounds not only between metal films, but between the metal and the semiconductor.
D. Should make a good low ohmic contact to both P and N type silicon.
E. Amenable to practical production methods o deposition and delineation.
F. Resistant to current-induced electro-migration.
G. Resistant to electro-chemical corrosion.
H. The deposition of the metal or metals must not introduce surface instabilities in the semiconductor material.
I. The metallization system must be compatible with L.S.I. arrays involving multilayer interconnection processing.

New L.S.I. devices require advanced metallization technologies, but discrete devices operating at high-power levels at microwave frequencies are also limited in their performance and reliability by conventional metallization materials.

10488

Hodgson, R.W. (Western Elec. Co.)
PHOTOLITHOGRAPHIC PROCESSING AS RELATED TO BEAM LEADED INTEGRATED CIRCUIT TECHNOLOGY. pp. 3-16 - 3-25. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

In summary, what has been shown here is a set of known processes which are designed around a given photolithographic material. It is recognized that there are probably many resists which can be used effectively, depending on the image-size required, or the number of images to reproduce in a given area. The characterization of the resist to such problems as coating thickness vs definition and pin-hole generation, and adherence vs amount of edge-lifting or undercutting, will probably be the main, limiting factors in the proper selection of the resist.

10489

Fisher, A.W. and Amick, J.A. (RCA Labs.)
DOPED OXIDE DIFFUSION SOURCES FOR SILICON. pp. 3-26 - 3-37. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

In the fabrication of silicon devices, diffusion processes play an important part. Commonly, diffusion sources are deposited onto the surface of a silicon wafer in essentially pure form, either as phosphorus oxide or boron oxide. Nonuniformities in the phosphorus or boron oxide layers, inadequate removal of the oxide prior to drive-in and irregularities in the process can lead to variations in the dopant concentration in the silicon. Furthermore, since concentrations approaching the solid solubility for the dopant are present after deposition of the oxide, crystalline defects, especially edge dislocations, may be introduced into the silicon in large numbers. These in turn, influence the diffusion coefficient for the dopant as well as the minority carrier lifetime and mobility in the surface regions.

10490

Jackson, D.M., Jr. (Motorola, Inc.)
THE EPITAXIAL PROCESS. pp. 3-38 - 3-48. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

The epitaxial process is subject to automatic control. Precise control is, however, subject to various process perturbations and inaccuracies in electrical or physical evaluation. An epitaxial production area is supported by several service and engineering functions to insure reliable, economical operation and quality which is sufficient for product requirements.

10491

Dicken, H.K. (Integrated Circuit Eng. Corp.)
A SURVEY OF THE MAJOR CHIP INTERCONNECTION TECHNIQUES. pp. 5-1 - 5-11. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

The assembly of complex hybrid integrated circuit packages is one of the major problems facing the microelectronics industry today. The principal problem area involves the chip interconnection or bonding techniques. These same problems also apply to standard silicon monolithic integrated circuits. Assembly not only represents the major cost of producing a silicon monolithic integrated circuit, it also represents the area where approximately one-half of the field failures are reported. Thus, in both single chip silicon monolithic integrated circuits and complex hybrid arrays, the bonding problem is a major factor. The following discussion will concentrate on the major chip interconnection techniques that are either now being used or planned for use in the immediate future by most hybrid assembly operations.

10492

Fehr, G. (Intel Corp.)
A SURVEY OF TODAY'S MICROCIRCUIT PACKAGING. 5-12 - 5-20. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference, Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y. June 16-18, 1970

Efforts are now being made in the assembly and packaging area. The cost element, in particular, brought about a rash of assembly and packaging developments, such as flip-chip, beam lead, spider bond, etc. The package functions include: 1) Chip protection (environment isolation). 2) Compatibility with system requirements. 3) Mechanical configuration. 4) Interfacing between the die and the electronic system. 5) Cost objectives.

10493

Clark, R.J. and Lunden, J.W. (GE)
THE APPLICATION OF THE STD PROCESS TO HYBRID MICROELECTRICS. pp. 5-26 - 5-51. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

The development of the STD process has been directed at overcoming the disadvantages of the individual wire bonding of IC chips. The process begins by fabricating the first level of conductors on the substrate. Standard photolithographic techniques are used for this, when their film conductors are required. The STD process offers many potential advantages in the design of many varieties of electronic circuits. Its main strengths are its compatible metallization system, its flexibility in choice of chip and substrate, and the fact that it is a batch-process utilizing precise photolithographic processes.

10494

Colling, D.A. (Westinghouse Res. Labs.) and Dunn, L.H. and Dowling, T.J. (Westinghouse Specialty Metals Div.)
RECENT DEVELOPMENTS IN ALLOYS UTILIZED IN MICROELECTRONIC PACKAGING. pp. 6-1 - 6-17. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

As part of our continuing effort to provide up-to-date information on the capabilities and limitations of our materials used in the systems engineered IC package, this paper reports recent developments involving Kovar alloys. Specific areas which are discussed include fundamental research on controlled expansion alloys, phase transformations, and stress in glass-to-metal seals. Corrosion, magnetic properties, and shielding effectiveness tests are also covered because of their importance to functional operation of IC devices.

10495

Butt, S.H. (Olin Corp., Brass Div.)
NEW COPPER ALLOYS FOR APPLICATION TO SEMICONDUCTOR PACKAGES. pp. 6-18 - 6-36. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

Copper and copper alloys currently are receiving substantial consideration for use in semiconductor packages as lead frames, and as eyelets and cans. It is the purpose of this paper to discuss the factor relating to the use of copper alloys in these applications. It is the further purpose of this paper to provide comparison between copper alloys adapted for such use and the other materials, principally nickel and high alloys, which are also presently used.

10496

Shew, A.L. (U.S. Navy, Nav. Ammunition Depot, Quality Evaluation Lab., Crane, Ind.)
QUALIFICATION TESTING OF PLASTIC ENCAPSULATED INTEGRATED CIRCUITS FOR MILITARY ENVIRONMENTS. pp. 6-37 - 6-42. A70-44534. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

The refusal of DOD/NASA agencies to accept "plastic" encapsulated integrated circuits over their hermetic counterparts was the cause of considerable concern to the manufacturers of these devices. The governmental agencies, however, had very little, if any, reliability data and few failure analysis techniques for the "plastic" packaged device as compared with the hermetic package. In May 1968, the DOD/NASA working group for Test Methods and Procedures for Plastic Encapsulated Devices was formed with the purpose of developing meaningful and appropriate environmental tests for "plastic" encapsulated semiconductors. The Microelectronics section at NAD Crane, already involved with evaluation of integrated circuits through its preparation and publishing μ-NOTES, was then selected by its sponsoring activity to become a part of the working group.

10496 (CONTD')

This paper will cover NAD Crane's part in this program.

10497

Hirsch, H. (IBM, Components Div.)
RESIN SYSTEMS USED FOR ENCAPSULATION OF MICROELECTRONIC PACKAGES. pp. 6-43 - - 6-58. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970. Solid State Technol. 13, no. 8, 48-54, Aug. 1970

This article describes a program for evaluating epoxy resins for packaging. Emphasis is placed on thermal expansion, effect of curing temperature on second order transition temperatures, effect of reactive diluents, effect of specific fillers, and the effect of temperature and humidity cycling on metallurgical bonds encapsulated with epoxy resin.

10498

Urban, L. (TRW Systems Group)
THE DEVELOPMENT OF A MICROELECTRONIC MICROWAVE RECEIVER. pp. 7-13 - 7-25. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

The need for providing ever-increasing performance capabilities in space and avionics communications systems has been accompanied by a corresponding growth in equipment complexity. This trend generates problems of excessive size, weight and reduced reliability. A possible solution of these problems lies in the application of micro-electronic design techniques to electronic equipment. By these means, more circuitry can be packaged with fewer interconnections in a given volume.

10499

Ciccio, J. (Raytheon Co., Missile Systems Div.)
MICROELECTRONICS PACKAGING FOR HIGH PERFORMANCE MILITARY AIRCRAFT. pp. 9-31 - 9-46. A70-44542. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

This paper describes the packaging techniques employed on the Signal Data Processor (SDC) presently in production and a proposed, next-generation unit that will affect a dramatic weight and volume reduction. The SDC performs launch-control and a signal-command functions for an air-to-air missile on a high performance aircraft. The design objectives are to package for minimum weight, volume and cost coupled with high reliability and maintainability. The SDC has been tested and has successfully met the requirements of MIL-E-5400, including thermal operation between the limits of +132°C and -65°C. Both units feature modular plug-in construction and a dependable, conduction-cooled, thermal system.

10500

Hu, K.C. (Hughes Aircraft Co., Microelectronics Lab., Newport Beach, Calif.)
APPLICATION OF POLYMIDE FILM IN LOW-COST CHIP PACKAGING AND HYBRID SEMICONDUCTOR MEMORIES. pp. 10-1 - 10-14. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

More than just a packaging material, it has been illustrated further, polymide film enables a total package design with the next level and system interconnection in mind. This in itself is significant -- a package design with full consideration of system partitioning instead of just sealing and protection. Advancement of the art of packaging and interconnection from its present standstill state may very well be to start from this basic concept.

10501

Croson, E.B. (U.S. Navy, Nav. Missile Center)
AN IMPROVED PHOTO RESIST PROCESS. pp. 10-15 - 10-24. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

The processing and fabrication requirements for selectively-etched, thin-film microcircuits include extensive applications of photo resist techniques. The high fabrication cost inherent in many thin-film operations can be directly attributed to photo/chemical processing which uses photo resist for pattern masking. Thus, the purpose of this paper is to present an improved photo resist process which can: (a) reduce photo/chemical processing time by at least 25%; (b) ease maskaligning problems; and (c) increase over-all yields in thin-film microcircuits.

10502

Pichler, H.H. (MIT, Lincoln Lab.)
A GRIDDED THICK FILM METALLIZATION STRUCTURE EMPLOYED IN MULTICHIP CIRCUIT FABRICATION. pp. 10-25 - 10-39. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City. N.Y., June 16-18, 1970

A way to make a 1-in^2, gridded, thick-film circuit that holds as many as 49 integrated circuit chips, and can be produced quickly at reasonable cost, has been developed. Key to the process was development of a basic circuit board that has reduced the time and cost of producing custom layouts for individual circuit designers.

10503

Gioia, J.C. (GE)
LOW COST PACKAGING OF THICK-FILM SUBSTRATES WITH CERAMIC GLASS SEALS pp. 10-40 - 10-46. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

Today, the hybrid integrated circuit field is maturing. High competitive semi-conductor companies offer full lines of discrete chips and integrated circuits. The learning curves are peaking out in the filmed substrate production area, assembly skills are at high level, and the equipment and ability to control processes is moving ahead at a rapid-rate - all of which adds up to lower costs. In the light of these declining costs for hybrid integrated circuits, the still high package costs must be studied carefully for lower cost alternatives.

10504

Anjard, R.P. (Gen. Motors Corp., Delco Radio Div.)
LEACHING DURING SOLDER IMMERSION - THICK FILM CONDUCTORS. pp. 11-1 - 11-6. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

Extensive intermixing with the conductive pad metallics results during solder coating of the conductive. If you need a good trouble-shooting tool to check out a suspect system or if you need to compare leaching effects, the technique used here is recommended. You can determine the time to remove 50% of the pad area by actual physical measurements or by electrical resistance and compare these to a baseline or normal time.

10505

Kroehs, A.R. (Alpha Metals, Inc.)
MATERIALS AND TECHNIQUES FOR ATTACHMENT OF ACTIVE AND PASSIVE DEVICES TO HYBRID SUBSTRATES. pp. 11-20 - 11-30. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

In this presentation we will examine the major device mounting techniques and the various bonding materials available while organizing them into a format which will enable the user to decide which procedure will best satisfy his particular requirement. Passive device mounting will be considered first, followed by a discussion of active device mounting. Passives were chosen first because they are simpler in geometry. Many of the materials selection problems also are common to both passive and active devices. By looking at materials without including the complicating factors of different geometries and attachment methods, many of the material selection parameters can be understood readily.

10506

Alonso, R.L. (Adar Assoc., Inc.)
PROBLEMS OF LSI TESTING AND TEST SYSTEMS. pp. 12-23 - 12-36. Proceedings of the Technical Program. 1970 National Electronic Packaging and Production Conference. Anaheim, Calif., Feb. 10-12, 1970, New York City, N.Y., June 16-18, 1970

The advent of LSI has brought along a new set of problems, namely, how to test LSI circuits, and with what sort of equipment. This paper is concerned with LSI testing from the point of view of the test system designer and builder. What tests to perform, and expecially what functional test patterns are required, is a broad subject outside of the present scope. We will be concerned with the problems and trade-offs of certain generally agreed upon testing techniques, and attempt to see how these influence the LSI test equipment currently being designed.

10510

Williams, D. (Westinghouse Elec. Corp., Defense and Electronic Systems Center, Baltimore, Md.)
NONVOLATILE IC TECHNIQUES FOR BORAM. Rept. no. ECOM-0160-1, Rept. no. 74-0396, Semiann. Rept. no. 1, Apr. 30-Oct. 30, 1973, 54 pp., Apr. 1974.
DAABO7-73-C-0160

The objective of this program is to optimize the technology of implementation, circuit design, and physical layout of an integrated circuit nonvolatile MNOS memory array. This development is to provide an advanced basic element for the Block Oriented Random Access Memory (BORAM) system. The goals include optimized technology to provide high performance, lower cost, and higher reliability BORAM memory arrays. The conclusion reached after considering other fabrication techniques is to use the high density double layer aluminum process and high density mask design rules to build a fully decoded 4096-bit MNOS memory array designed for BORAM.

10512

Dale, J.R. (Assoc. Semiconductor Mfrs., Ltd. Mullard Res. Labs.)
ULTRASONIC WIRE BONDING TO SILICON DEVICES. Ann. Rept., 55 pp., Oct. 1973.
AD 915 911

This report outlines work carried out during the past eight months on the operation, stabilization and control of Kullich & Soffa 472 ultrasonic nailhead bonding machines. An optical interferometric technique for measuring the amplitude of the welding capillary is described and an evaluation procedure for the quality assessment of ultrasonic nail head bonds discussed. Details of an accurate electromechanical bond shear testing technique developed for this project are described and its application to the quality control of commercially produced devices discussed.

10513

Anon.
MODERN DIE BONDING: TECHNIQUES AND EQUIPMENT. Electronic Packaging and Production 14, no. 1, 6 pp., Jan. 1974

Today's modern die bonders are designed to accomodate the two major bonding techniques: eutectic and epoxy. The primary emphasis in eutectic die bonding is to provide an adequate electrical, thermal and mechanical connection without damaging the chip. The method is the most widely used, be a serious shortage of virgin wafers. Much of this demand will have to be met by successfully qualified reclaim wafers for use in fabricating MOS and some bipolar products. Shown here among the rejects is a tray of reclaimed wafers ready for reprocessing. whether it be for simple transistor chips or more sophisticated monolithic ICs. Although the resulting eutectic bond is the same, there are variations in the methods of handling, heating, agitation, and in the eutectic materials.

10514

Colman, D. (Tex. Instr. Ltd., Manton Lane, Bedford, Engl.)
INVESTIGATING THE CAUSES OF NOISE IN FIELD EFFECT TRANSISTORS. Rept. no. RP11-1. Ann. Rept., Oct. 31, 1973. AD 915 913

The use of boron doped oxide instead of boron tribromide for the top gate diffusion has resulted in a significant improvement in leakage current. It has been shown that leakage is very sensitive to aluminum overlaying the junction. This aluminum must be very pure. J.F.E.T.s have been manufactured with an ion implanted boron deposition for the top gate. The noise performance of these was inferior to conventionally manufactured devices. Attempts were made to improve the low temperature noise performed by using an epitaxial dopant with shallow energy level. Results which have been obtained did not demonstrate any sensitivity of noise to dopant energy level.

10516

Lawrence, J.E. (Silicon Matl., Inc., Mountain View, Calif.)
THE CASE FOR RECLAIM WAFERS. Electronic Packaging and Production 14, no. 1, 8 pp., Jan. 1974

The semiconductor industry will require over 1 million silicon wafers each week in 1974. Of all wafers processed during a typical production week, about 30% will not complete fabrication. Present indications are: there will be a serious shortage of virgin wafers. Much of this demand will have to be met by successfully fabricating MOS and some bipolar products. Shown here amoung the rejects is a tray of reclaimed wafers ready for reprocessing.

10517

Anon.
ION IMPLANTATION: FROM A SPECIALTY TO A STANDARD METHOD FOR NEW ICS. Electronic Design 22, no. 11, 4 pp., May 24, 1974

During the late 1960s, when ion implantation began to be used as a complementary technique to commercial diffusion processes, it was employed primarily to adjust threshold voltages precisely and to form self-aligned gates in MOS circuits. Today virtually every semiconductor house uses ion implantation in volume production of a growing list of superior standard and custom MOS devices. In addition the technology is making in-roads in the fabrication of bipolar ICs, and its reach is extending well into active and nonactive discrete areas.

10518

Eshleman, R.L., Meyers, A.P., Davidson, W.A. (IIT Res. Inst., Chicago, Ill.)
FEASIBILITY MODEL OF A HIGH RELIABILITY FIVE-YEAR TAPE TRANSPORT. Vol. I, II, III. Jan. 5, 1972-Nov. 5, 1973. NA5-21692

The main objective of this program was the design and fabrication of a spacecraft tape recorder possessing high reliability and long life. The philosophy that life shall predominate over all other requirements led to a set of program goals necessary to achieve this prime objective. These goals were:

- The identification of a transport configuration in which all considerations were made on the basis of long life.
- The identification of life limiting aspects of the transport as a whole.
- The identification of a design procedure, using analytical modeling, to maximize life.

10519

Rapp, A.K. and Ross, E.C. (Inselek Inc., Princeton, N.J.)
SILICON-ON-SAPPHIRE SUBSTRATES OVERCOME MOS LIMITATIONS. Electronics 45, no. 20, 113-6, Sept. 25, 1972

A new family of devices may well be destined to fill the awkward gap between the inexpensive but slow MOS and the fast but costly bipolar technologies. Tests of silicon-on-sapphire substrates show they outperform--yet are just as reliable as--conventional bulk-silicon substrates when used as the basis for MOS devices. And, when topped with complementary deep-depletion mode as well as enhancement-mode devices, SOS chips now coming off the production lines set still higher MOS performance standards.

10520

Reich, B. and Hakim, E.B. (U.S. Army, ECOM, Electronics Technol. & Devices Lab., Fort Monmouth, N.J.)
TEMPERATURE-HUMIDITY ACCELERATION FACTORS FOR PLASTIC TRANSISTORS AND INTEGRATED CIRCUITS. Solid State Technol. 15, no. 9, 65-6, Sept. 1972

The relationship between junction temperature and failure rate for hermetically sealed transistors and integrated circuits is well known and accepted. This article shows that the relationship for plastic encapsulated semiconductors must be modified to include the sum of both temperature and relative humidity. With this modification, accelerated temperature-humidity tests can be applied to predict field failure rates of plastic encapsulated semiconductor devices.

10522

Epstein, A.S. and Trimmer, P.A. (U.S. Army, Harry Diamond Res. Labs., Washington, D.C.)
RADIATION DAMAGE AND ANNEALING EFFECTS IN PHOTON COUPLED ISOLATORS. pp. 391-9. Reprinted from IEEE Trans. on Nuc. Sci. NS-19, no. 6, Dec. 1972

The primary objective of the investigation reported here was to characterize the behavior of photon coupled isolators in a gamma (ionizing) radiation environment and a neutron (non-ionizing) radiation environment. Secondary objectives were to separate the effects on the various components of the isolators and to study the annealing behavior. The emphasis was placed on the gamma irradiations, since some work has been reported on neutron irradiated devices similar to the ones investigated here.

10524

Moore, D.G. and Wheatley, S. (Plessey Co. Ltd., Prod. Assessment Labs., Reliability Res. Group, Titchfield, Fareham)
AN INVESTIGATION INTO THE ENCAPSULATION OF THICK FILM HYBRID MODULES.
Rept. no. 260007, Interim Rept., 25 pp., Nov. 1973. AD 916 511.
N/CP540/73/DC39 (1)

This report summarizes the various aspects of plastic encapsulation of large area thick film hybrid modules. Physical parameters as well as chemical and thermal criteria are included.

10525

Clapp, W.A. (RCA, Advanced Technol. Labs., Camden, N.J.)
LSI COMPUTER DESIGN--SUMC/DV. pp. 80-6.
A73-23795

Advanced Technol. Labs. s designed, built, and tested the first \ JS general-purpose computer. The computer executes 32 instructions that are operation-code compatible with the IBM 360 and RCA Spectra 70 series of computers. The computer is supported by 2k words of main-memory LSI storage and TTY peripheral for input and output operations. Additionally, a simulator, an assembler, and a loader have been constructed to provide software support to the hardware. This paper and its companion in this issue provide an overall picture of this diagram to a debugged, operational computer in 12 months.

10526

Feller, A. (RCA, Advanced Technol. Labs., Advanced Circuit Technol., Camden, N.J.)
LSI COMPUTER FABRICATION--SUMC/DV. pp. 74-9. A73-23794

The SUMC/DV (Space Ultrareliable Modular Computer Demonstration Vehicle), which required the design and fabrication of ten different array types, was designed, partitioned, assembled, tested, and made completely operational in less than one year. The importance of the ATL simulation and design automation programs in achieving these results is discussed. This paper describes the assembly, the physical and electrical characteristics, and the basis electrical testing procedures used on SUMC/DV. The paper includes a description of the packaging concepts, the physical assembly, the fabrication and testing of the various components including the LSI CMOS arrays, the hierarchy of the memory complement, the clock generation and distribution scheme, additional system testing techniques, and the procedure employed in the electrical checkout of the system.

10527

Merriam, A.S. and Zieper, H.S. (RCA, Advanced Technol. Labs., Appl. Computer Systems Lab., Camden, N.J.)
SIMULATION--METHODOLOGY FOR LSI COMPUTER DESIGN. pp. 69-73. A73-23793

The development of LSI technology (arrays of greater than 100 gates of non-regularized logic) requires the availability and use of a variety of design aids to assure competitive cost, schedule, and implementation cycles. Such a system of design aids has been developed by the Applied Computer Systems group of the Advanced Technol. Labs. and was the basis for the successful construction of the first LSI processor using custom C-MOS arrays--the SUMC/DV. A measure of the success of the design approach described in this article is that the demonstration LSI processor, from concept to power-on, took less than one year and was checked out in less than four weeks.

10528

Bell Northern Res. Ltd.
DEFINITIONS OF THICK FILM CIRCUIT TERMS. Std. no. BNR-STD-1028, Final Spec., 17 pp., Feb. 1972. AD 915 162L. IDEP Acc. no. E0045. IDEP 347.10.00.00-CJ-01S

The technical terms listed herein defined and explained in the restricted sense in which they apply to thick film circuits, and particularly as used in BNR Standard 1026, Thick Film Circuit Design Data. This standard is therefore intended to assist in the precise interpretation of Standard 1026, and other documents such as drawings and specifications used in conjunction with such products. Terms which are used in their ordinary sense, as in other branches of engineering, are not defined herein.

10529

Anon.
HIGH VOLUME THICK FILM PRODUCTION/TESTING: AN OVER-THE-SHOULDER VIEW. Electronic Packaging and Production, pp. 36-42, Oct. 1973

Centralab currently produces over 1 million thick film circuits per week. At this volume, wasted time and effort in product handling are anathema. On the other hand, as this walk-through observation attests, a high QA/QC level is stringently maintained.

10531

Anon.
THE PC INDUSTRY: A FADING SONG? PART 2. WIRE WRAPPING TECHNIQUES AND HYBRIDS--REPLACING PCBS? Circuits Mfg., pp. 42-4, Sept. 1973

Wire wrapping techniques and hybrids are compared to PCB's for consumer acceptability. Economic factors are prime issue.

10533

Anon.
SCANNING ELECTRON MICROSCOPY/1971. PROCEEDINGS OF THE 4TH ANNUAL SCANNING ELECTRON MICROSCOPE SYMPOSIUM. PART I. FOURTH ANNUAL SCANNING ELECTRON MICROSCOPE SYMPOSIUM. Sponsored by IIT Res. Inst. PART II. WORKSHOP ON FORENSIC APPLICATIONS OF THE SCANNING ELECTRON MICROSCOPE. Sponsored by the National Institute of Law Enforcement and Criminal Justice (LEAA, U.S. Department of Justice) and IIT Res. Inst. Part I. Apr. 27-29, 1971. Part II. Apr. 30, 1971. IIT Res. Inst., Metals Div., Chicago, Ill., 618 pp.

Presentations:
A Review of Problems of Interpretation of the Scanning Electron Microscope Image with Special Regard to Methods of Specimen Preparation
Fundamentals of Scanning Electron Microscopy
Charging Effects in Scanning Electron Microscopy
Scanning Transmission Electron Microscopy
Dynamic Focusing Technique for Tilted Samples in Scanning Electron Microscopy
After-Lens Deflection and its Uses
Soil Structure Analysis Using Optical Techniques on S.E. Micrographs
High-Resolution Enhancement in Scanning Electron Microscopy by a Posteriori Holographic Image Processing
Progress in the Design and Application of Energy Dispersion X-Ray Analyzers for the SEM
Quantitative Microanalysis in Fe-Cr-Ni and Fe-Cr-Ni-Mn Alloys by Scanning Electron Microscopy Using an Empirical Approach
Energy Dispersive X-Ray Analysis of Thin Films in Integrated Circuits
Auger Electron Spectroscopy for Scanning Electron Microscopy
Observation of Deformation and Fracture in Metals--A Dynamic Application of SEM
A Micromanipulator for the Scanning Electron Microscope
Dynamic Studies of Deformation Mechanisms in the SEM
Application of the SEM to Study of Mechanisms of Metal Fatigue
Use of the SEM in Correlating Acoustic Emissions with Prefracture Processes
Fracture Morphology of Explosively Loaded Steel Cylinders
The Use of Backscattered-Electron Images in Metallographic Analyses of Carbides
The Growth of Colloidal Silica Particles
SEM Investigation of Electro-deposited Tin Surfaces
Study of Metal in the Lunar Soil
Solving Some Problems in Fiber Science with SEM
Interpretation of Some Field-Ion Micrograph Features from SEM Observations
Oxide Platelet Formation in Bulk Tantalum
Mine Dust Characterization Using the Scanning Electron Microscope and Dust Samplers
Investigation of Whisker Growth on Relay Metal Surfaces
The Examination of Biological Material at Low Temperatures
Application of the SEM in Paleobiology
Comparative Examination of Biological Samples by SEM, TEM, and other Techniques
Some Problems of Fixation of Selected Biological Samples for S.E.M. Examination
Scanning Electron Microscopic Observation on Non-Mechanically Cryofractured Biological Tissue
Preparation of Suspended Cells for SEM Examination of Internal Cellular Structures
Skeletal Ultrastructure of Sediment Producing Green Algae
Studying Neuronal Architecture and Organization with the Scanning Electron Microscope
Mammalian Gametes: A Study with the Scanning Electron Microscope
Scanning Electron Microscopy of Chronic Pulmonary Emphysema: A Study of the Equine Model
Surface Morphology of Hypoplastic and Normal Lungs from Newborn Lambs
Specialized Extracellular Structures of the Inner Ear
Scanning Electron Microscopy of Bacterial Colonies
Surface Effects of Cell-Wall-Active Antimicrobial Agents
Morphology of Lipid Rich Organelles in Tissue of Man and Rat
SEM Studies of the Synovial Surfaces of Tendons
Effects of EDTA and HCL Treatments of Enamel Fracture Surfaces
Remineralization of Acid-Softened Human Enamel Studied by the SEM
Scanning Electron Microscopy and Electron Probe Analysis of Congenital Hair Defects
Normal Eggshells and Thin Eggshells Caused by Organochlorine Insecticides Viewed by the Scanning Electron Microscope
Surface Studies of Carbons for Prosthetic Applications
The Applications of Image Analysis Techniques to Scanning Electron Microscopy
Cathodoluminescence Spectra
Cathodoluminescence Studies of Sediments

10533 (Cont'd)

Device Fabrication Using a Scanning Electron Beam System
Characterization of Semiconductor Processes
Applications of Scanning Electron Mirror Microscopy to Electronics
Investigation of Pre-Breakdown Sites in Shallow Diffused Structures with the Scanning Electron Microscope
Low Duty Cycle Stressing of Semiconductors in the SEM
Quantitative Voltage and Temperature Distribution Studies in GaAs Transverse Gunn Diodes Using an SEM
Applications of the SEM Channelling Pattern Technique to Material Problems
Application of the SA-ECP Method to Deformation Studies
A New Method for the Investigation of Crystal Structures Using the Scanning Electron Microscope
SEM Electron Channelling Line Width (Broadening) and Pattern Degradation in Alkali Halide Crystals
Quantitative Crystallographic Orientation Determinations of Microcrystals Present in Solid Specimens Using the SEM
Reduction of Carbon Contamination in the SEM
Scanning and Transmission Electron Microscopy and Microanalysis of Structured Granules in Fischerella Ambigua
SEM Applications in the Study of Volume Defects in Semiconductor Devices (Abstract Only)
Microvision
SEM and Analytical Possibilities
An Evaluation of the SEM with X-Ray Microanalyzer Accessory for Forensic Work
Forensic Applications of Scanning Electron Microscopy
Application of the SEM in Forensic Medicine
Applications of Scanning Electron Microscopy to Forensic Science at Jet Propulsion Laboratory, 1969-1970
Application of the Scanning Electron Microscope to the Examination of Firearms Markings
Scanning Electron Microscopy of Selected Crime Laboratory Specimens
The Scanning Electron Microscopy of Counterfeit Coins (Abstract Only)
Bibliography on the Scanning Electron Microscope

10534

Flutie, R.E. (Harris Semiconductor, Melbourne, Fla.)
ENERGY DISPERSIVE X-RAY ANALYSIS OF THIN FILMS IN INTEGRATED CIRCUITS.
pp. 81-8. Scanning Electron Microscopy/1971. Proceedings of the 4th Annual Scanning Electron Microscope Symposium. Part I. Fourth Annual Scanning Electron Microscope Symposium. Sponsored by IIT Res. Inst. Part II. Workshop on Forensic Applications of the Scanning Electron Microscope. Sponsored by the National Institute of Law Enforcement and Criminal Justice (LEAA, U.S. Department of Justice), and IIT Res. Inst. Part I. Apr. 27-29, 1971. Part II. Apr. 30, 1971. IIT Res. Inst., Metals Div., Chicago, Ill., 618 pp.

X-ray examination of thin films on integrated circuits pose special problems because the x-rays are emitted from a much larger depth compared to the film thickness. The energy dispersive analysis performed satisfactorily for unpassivated Ni Cr films of 600 Å more thickness; line and area scans and semi-quantitative results could be readily obtained. 100 Å thin film in passivated and unpassivated state showed Cr and Ni peaks, but the peak to background ratios were rather low. These thin films, even under 6,000 Å of passivation could be studied in a wavelength dispersive spectrometer to provide x-ray element - distribution photographs. Significance of these results in terms of applications of proper x-ray analysis techniques in thin film analysis is discussed.

10535

Chang, T.H.P. (Cambridge Sci. Instr. Co., Cambridge, Engl.)
DEVICE FABRICATION USING A SCANNING ELECTRON BEAM SYSTEM. pp. 417-24. Scanning Electron Microscopy/1971. Proceedings of the 4th Annual Scanning Electron Microscope Symposium. Part I. Fourth Annual Scanning Electron Microscope Symposium. Sponsored by IIT Res. Inst. Part II. Workshop on Forensic Applications of the Scanning Electron Microscope. Sponsored by the National Institute of Law Enforcement and Criminal Justice (LEAA, U.S. Department of Justice), and IIT Res. Inst. Part I. Apr. 27-29, 1971. Part II. Apr. 30, 1971. IIT Res. Inst., Metals Div., Chicago, Ill., 618 pp.

The two main areas of application for the electron beam machine in microcircuit fabrication are (a) Mask making and (b) Direct device exposure, and it has been shown that complex patterns can be formed reliably for both these two applications using either digital computer control facilities or analogue facilities. It is clear from the results already achieved that there are no major difficulties in developing this machine to the point where it will generate a set of standard size masks inside a working day.

10536

Crosthwait, D.L. (Tex. Instr. Inc., Semiconductor Res. and Dev. Labs., Dallas, Tex.)
CHARACTERIZATION OF SEMICONDUCTOR PROCESSES. pp. 425-32. Scanning Electron Microscopy/1971. Proceedings of the 4th Annual Scanning Electron Microscope Symposium. Part I. Fourth Annual Scanning Electron Microscope Symposium. Sponsored by IIT Res. Inst. Part II. Workshop on Forensic Applications of the Scanning Electron Microscope. Sponsored by the National Institute of Law Enforcement and Criminal Justice (LEAA, U.S. Department of Justice), and IIT Res. Inst. Part I. Apr. 27-29, 1971. Part II. Apr. 30, 1971. IIT Res. Inst., Metals Div., Chicago, Ill., 618 pp.

It was a logical if not necessary step for the semiconductor manufacturer to exploit the SEM in development and monitoring of manufacturing processes. The purpose of this paper is to relate a few examples of this and to describe a sample preparation technique which facilitates timely accurate characterization of the various aspects of semiconductor devices.

10537

Cox, S.B. (U.S. Air Force, Kirtland AFB, Air Force Weapons Lab. (EST), New Mex.)
APPLICATIONS OF SCANNING ELECTRON MIRROR MICROSCOPY TO ELECTRONICS. pp. 433-40. Scanning Electron Microscopy/1971. Proceedings of the 4th Annual Scanning Electron Microscope Symposium. Part I. Fourth Annual Scanning Electron Microscope Symposium. Sponsored by IIT Res. Inst. Part II. Workshop on Forensic Applications of the Scanning Electron Microscope. Sponsored by the National Institute of Law Enforcement and Criminal Justice (LEAA, U.S. Department of Justice) and IIT Res. Inst. Part I. Apr. 27-29, 1971. Part II. Apr. 30, 1971. IIT Res. Inst., Metals Div., Chicago, Ill., 618 pp.

The scanning electron mirror microscope (SEMM) is presently being considered as a potential 100% semiconductor piece-part screen for Air Force systems. Research to date has been centered on screening for potentially weak metallization stripes, although numerous potential failure mechanisms may be screened against at the same time. Data on the usefulness of a SEMM in predicting metallization electrical overstress failures are presented. The potential computerized automatic SEMM screening system for production lines is also discussed.

10538

Varker, C.J. and Ehlenberger, G. (Motorola Inc., Semiconductor Prod. Div., Central Res. Labs., Phoenix, Ariz.)
INVESTIGATION OF PRE-BREAKDOWN SITES IN SHALLOW DIFFUSED STRUCTURES WITH THE SCANNING ELECTRON MICROSCOPE. pp. 441-8. Scanning Electron Microscopy/1971. Proceedings of the 4th Annual Scanning Electron Microscope Symposium. Part. I. Fourth Annual Scanning Electron Microscope Symposium. Sponsored by IIT Res. Inst. Part II. Workshop on Forensic Applications of the Scanning Electron Microscope. Sponsored by the National Institute of Law Enforcement and Criminal Justice (LEAA, U.S. Department of Justice) and IIT Res. Inst. Part I. Apr. 27-29, 1971. Part II. Apr. 30, 1971. IIT Res. Inst., Metals Div., Chicago, Ill., 618 pp.

Utilizing the electron beam induced current mode, pre-breakdown sites associated with regions of local curvature in the depletion field are investigated under voltage bias conditions. A direct correlation is observed between the region of local curvature in the oxide step and the resulting pre-breakdown sites observed in the electron beam induced current mode. The results indicate that the surface sites observed result directly from resolution limits on the edge acuity of the photomask.

10539

Gonzales, A.J. (Motorola,Inc., Central Res. Lab., Phoenix, Ariz.)
LOW DUTY CYCLE STRESSING OF SEMICONDUCTORS IN THE SEM. pp. 451-6. Paper presented at the Scanning Electron Microscopy/1971. Proceedings of the 4th Annual Scanning Electron Microscope Symposium. Part I. Fourth Annual Scanning Electron Microscope Symposium. Sponsored by IIT Res. Inst. Part II. Workshop on Forensic Applications of the Scanning Electron Microscope. Sponsored by the National Institute of Law Enforcement and Criminal Justice (LEAA, U.S. Department of Justice) and IIT Res. Inst. Part I. Apr. 27-29, 1971. Part II. Apr. 30, 1971. IIT Res. Inst., Metals Div., Chicago, Ill., 618 pp.

It is the purpose of this work to illustrate the technique of low duty cycle electrical stressing with particular emphasis on semiconductor applications: the enhancement of voltage contrast by high current pulsing, observation of electron beam induced effects during pulsing, and the high temperature cycling of an aluminum-silicon contact.

10540

Anon.
SCANNING ELECTRON MICROSCOPY/1972. PROCEEDINGS OF THE 5TH ANNUAL SCANNING ELECTRON MICROSCOPE SYMPOSIUM. PART I. FIFTH ANNUAL SCANNING ELECTRON MICROSCOPE SYMPOSIUM. Sponsored by the IIT Res. Inst. PART II. WORKSHOP ON BIOLOGICAL SPECIMEN PREPARATION FOR SCANNING ELECTRON MICROSCOPY. Sponsored by the National Institute of General Medical Sciences (National Institute of Health), and IIT Res. Inst. Part I. Apr. 25-26, 1972. Part II. Apr. 27, 1972. La Salle Hotel, Chicago, Ill., 447 pp.

Presentations:
- Scanning Electron Microscopy: The Next Ten Years
- Scanning Electron Microscopy at Liquid Helium Temperatures
- Scanning Electron Microscopy to 1600°C
- Five Easy Pieces - Aids in Scanning Electron Microscopy
- The Cylindrical Secondary Electron Detector as a Voltage Measuring Device in the Scanning Electron Microscope
- A Storage-Display System for the Scanning Electron Microscope
- Simultaneous Display System of Different Magnification Images in Scanning Electron Microscopy
- Invariance under Transformation: A Useful Concept in the Interpretation of SEM Images
- High Spatial Resolution X-Ray Microanalysis of Thin Specimens in the Scanning Electron Microscope
- Resolution and Sensitivity of X-Ray Microanalysis in Biological Sections by Scanning and Conventional Transmission Electron Microscopy
- Scanning X-Ray Emission Microscopy
- Anomalous Crystallographic Contrast on Rolled and Annealed Specimens
- Absorbed Current Imagery for Surface Studies in the SEM
- Electron Beam Induced Current in Silicon Planar p-n Junctions: Physical Model of Carrier Generation. Determination of some Physical Parameters in Silicon
- Basic Limitations of Probe Forming Systems Due to Electron - Electron Interaction
- Comparison and Evaluation of Specimens for Resolution Standard
- Experimental Resolution Limit in the Secondary Electron Mode for a field Emission Source Scanning Electron Microscope

10540 (Cont'd)

The Rationale and Mode of Application of Thin Films to Non-Conducting Materials
Observations on the Prevention of Specimen Charging
Charging Artifacts in the Scanning Electron Microscope
Observations of Uncoated, Non-conducting or Thermally Sensitive Specimens using a Fast Scanning Field Emission Source SEM
Explanation of the Low-Loss Image in the SEM in Terms of Electron Scattering Theory
A Technique for the Examination of Irradiated Materials in a Scanning Microscope
A Method of Sequential Etching of Passivation for the SEM Inspection of Subsurface Metallic Layers
Scanning Electron Microscopy Techniques for Amorphous Semiconductor Device Studies
Physical Limits in Transmission Scanning Electron Microscopy of Thick Specimens
Theory and Practice of Revealing Crystallographic Defects with the SEM by Means of Diffraction Contrast
The Arizona 1MeV Transmission Scanning Electron Microscope--some Design Features
Methods for Tracing Ray Paths Through Electron Optical Lenses to Investigate Spherical Aberration in the SEM
Comparison of Various Methods for Reducing Measurements from Stereo-Pair Scanning Electron Micrographs to "Real 3-D Data"
Comparison of Height and Depth Measurements with the SEM and TEM using a Shadow Casting Technique
Handling, Mounting, and Examination of Particles for Scanning Electron Microscopy
Biological Specimen Preparation for the Scanning Electron Microscope - An Overview
Comparison of Fixation and Drying Procedures for Preparation of some Cultured Cell Lines for Examination in the SEM
Freezing, Freeze-Drying, and Freeze-Substitution
Evaluation of Microdissected, Unfixed, Freeze-Dried Tissue for Ultramicrochemical Study
Preparation of Red Blood Cells (RBC) for SEM: A Survey of Various Artifacts
Critical Point Drying, Cryofracture, and Serial Sectioning
Stabilization and Replication of Soft Tubular and Alveolar Systems: A Scanning Electron Microscope Study of the Lung
A New Immunologic Marker for Scanning Electron Microscopy
Preparative Techniques for the Successive Examination of Biological Specimens by Light Microscopy, SEM and TEM
Preparation of Fragile Botantical Tissues and Examination of Intracellular Contents by SEM
Evaluation of a New Preparative Technique for Bond Examination in the SEM
Preparative Technique for Platelet Preservation for SEM
Different Replica Methods for Skin Examination and Their Comparison with Direct Studies on Skin
A New Freeze-Dry Technique for Preparation of Marine Biological Specimens for SEM
Total Material Characterization with the Scanning Electron Microscope
Bibliography on the Scanning Electron Microscope

10541

Flutie, R.E. (Harris Semiconductor, Melbourne, Fla.)
A METHOD OF SEQUENTIAL ETCHING OF PASSIVATION FOR THE SEM INSPECTION OF SUBSURFACE METALLIC LAYERS. pp. 185-92. Scanning Electron Microscopy/1972. Proceedings of the 5th Annual Scanning Electron Microscope Symposium. Part I. Fifth Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Biological Specimen Preparation for Scanning Electron Microscopy. Sponsored by the National Institute of General Medical Sciences (National Institute of Health), and IIT Res. Inst. Part I. Apr. 25-26, 1972. Part II. Apr. 27, 1972. La Salle Hotel, Chicago, Ill. 447 pp.

Passivation can be removed with a minimum of disturbance to sublayer metallic films. This must be done with passivated integrated circuits to properly SEM inspect the sublayer metallic films. EDXA at bonding pads where aluminum is present in both the passivated and unpassivated state, helps to indicate when all the passivation has been removed.

10542

Sie, C.H. (Energy Conversion Devices, Inc., Troy, Mich.)
SCANNING ELECTRON MICROSCOPY TECHNIQUES FOR AMORPHOUS SEMICONDUCTOR DEVICE STUDIES. pp. 193-6. Scanning Electron Microscopy/1972. Proceedings of the 5th Annual Scanning Electron Microscope Symposium. Part I. Fifth Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Biological Specimen Preparation for Scanning Electron Microscopy. Sponsored by the National Institute of General Medical Sciences (National Institute of Health) and IIT Res. Inst. Part I. Apr. 25-26, 1972. Part II. Apr. 27, 1972. La Salle Hotel, Chicago, Ill., 447 pp.

In amorphous semiconductor films, particularly for those prepared from chalcogenide systems, the basic mechanism for the bistable resistance switching is a reversible amorphous to crystalline phase transition, actuated by electrical pulses. An electric field-induced crystalline filament formation is responsible for the low resistance state. Due to the size, location and nature of the filament special techniques were developed for SEM studies of these amorphous semiconductor devices. No difference in secondary emission characteristics of the crystalline and amorphous phases was observed at 20 kv. However, a sodium chromate, sulfuric acid, dionized water etchant removed the amorphous phase at a faster rate than the crystalline phase. The etched samples were studied for the morphologies of the amorphous film.

10543

Humphreys, C.J., Spencer, J.P., Woolf, R.J. et al. (U. of Oxford, Dept. of Met., Oxford, Engl.)
THEORY AND PRACTICE OF REVEALING CRYSTALLOGRAPHIC DEFECTS WITH THE SEM BY MEANS OF DIFFRACTION CONTRAST. pp. 205-14. Scanning Electron Microscopy/1972. Proceedings of the 5th Annual Scanning Electron Microscope Symposium. Part I. Fifth Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Biological Specimen Preparation for Scanning Electron Microscopy. Sponsored by the National Institute of General Medical Sciences (National Institute of Health), and IIT Res. Inst. Part I. Apr. 25-26, 1972. Part II. Apr. 27, 1972. La Salle Hotel, Chicago, Ill., 447 pp.

Experimental results demonstrate that satisfactory STEM images of defects can be obtained using conventional electron sources, and that the images show the contrast expected from diffraction theory. On the other hand, SREM images of such defects in both thin foil and solid specimens either cannot be obtained, or are difficult to obtain, using such electron sources. These experimental results are in good agreement with the predicted results.

10544

Wells, O.C. (IBM, Thomas J. Watson Res. Center, Yorktown Heights, N.Y.)
BIBLIOGRAPHY ON THE SCANNING ELECTRON MICROSCOPE. pp. 375-442. Scanning Electron Microscopy/1972. Proceedings of the 5th Annual Scanning Electron Microscope Symposium. Part I. Fifth Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Biological Specimen Preparation for Scanning Electron Microscopy. Sponsored by the National Institute of General Medical Sciences (National Institute of Health), and IIT Res. Inst. Part I. Apr. 25-26, 1972. Part II. Apr. 27, 1972. La Salle Hotel, Chicago, Ill., 447 pp.

Papers published in the IITRI Proceedings from 1968 through 1971 have been included in this bibliography. The list of references was sorted, edited, and cross-referenced using an internal IBM computer program.

10545

Anon.
SCANNING ELECTRON MICROSCOPY/1974. PROCEEDINGS OF THE 7TH ANNUAL SCANNING ELECTRON MICROSCOPE SYMPOSIUM. PART I. SEVENTH ANNUAL SCANNING ELECTRON MICROSCOPE SYMPOSIUM. Sponsored by the IIT Res. Inst. PART II. WORKSHOP ON SCANNING ELECTRON MICROSCOPY AND THE PLANT SCIENCES. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. PART III. WORKSHOP ON ADVANCES IN BIOMEDICAL APPLICATIONS OF THE SEM. Sponsored by the IIT Res. Inst. PART IV. WORKSHOP ON FAILURE ANALYSIS AND THE SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

10546

Crosthwait, D.L. and Ivy, F.W. (Tex. Instr. Inc., Semiconductor Res. & Dev. Labs., Dallas, Tex.)
VOLTAGE CONTRAST METHODS FOR SEMICONDUCTOR DEVICE FAILURE ANALYSIS. pp. 935-40. Scanning Electron Microscopy/1974. Proceedings of the 7th Annual Scanning Electron Microscope Symposium. Part I. Seventh Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Scanning Electron Microscopy and the Plant Sciences. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. Part III. Workshop on Advances in Biomedical Applications of the SEM. Sponsored by the IIT Res. Inst. Part IV. Workshop on Failure Analysis and the SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

The widespread use of the scanning electron microscope (SEM) in semiconductor applications has led to the employment of voltage contrast methods to device failure analysis. The ability to obtain useful voltage contrast information is contingent on both instrument and device features. The purpose of this paper is to present some of the practical considerations of voltage contrast methods. Techniques for increasing the voltage contrast information relating to internal circuit function by dynamic synchronous biasing will also be discussed

10547

Gonzales, A.J. (Motorola Inc., Semiconductor Prod. Div., Semiconductor Analytical Lab., Phoenix, Ariz.)
ON THE ELECTRON BEAM INDUCED CURRENT ANALYSIS OF SEMICONDUCTOR DEVICES. pp. 941-8. Scanning Electron Microscopy/1974. Proceedings of the 7th Annual Scanning Electron Microscope Symposium. Part I. Seventh Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Scanning Electron Microscopy and the Plant Sciences. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. Part III. Workshop on Advances in Biomedical Applications of the SEM. Sponsored by the IIT Res. Inst. Part IV. Workshop on Failure Analysis and the SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

Although a large portion of SEM semiconductor analysis involves the imaging of surfaces, the same electron beam which produces these images can also be used to detect certain subsurface features which affect the fundamental operation of the device. The portion of the electron beam which penetrates into the semiconductor will produce hole-electron pairs that are then free to drift and diffuse through the device to nearby P-N junctions. These charged carriers are separated at the junction thereby producing an electron beam induced current (EBIC) which may be used to modulate the brightness of the SEM cathode ray tube display. By this method, the spatial distribution of defects which influence the EBIC signal magnitude may be displayed.

10548

Schick, J.D. (IBM, System Prod. Div., East Fishkill Facility, Hopewell Junction, N.Y.)
FAILURE ANALYSIS OF INTEGRATED CIRCUITS WITH SEM BEAM INDUCED CURRENTS. pp. 949-54. Scanning Electron Microscopy/1974. Proceedings of the 7th Annual Scanning Electron Microscope Symposium. Part I. Seventh Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Scanning Electron Microscopy and the Plant Sciences. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. Part III. Workshop on Advances in Biomedical Applications of the SEM. Sponsored by the IIT Res. Inst. Part IV. Workshop on Failure Analysis and the SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

When an electron beam strikes a semiconductor material, hole-electron pairs are excited. If these mobile carriers are created within the depletion region of a p-n junction, they are swept out by the existing junction potential giving rise to a reverse current. This current may then be used to modulate a cathode ray tube, producing a maximum signal (either brightness or Y-deflection) when the scanning electron beam strikes the junction. This technique has been used with varying degrees of success in locating failures in high density integrated circuits, identifying leakage paths in devices, measuring junction depths and base widths, and obtaining diffusion concentration profiles. The effect on beam induced current measurements of varying the SEM operating parameters, such as sample orientation, beam current, and acceleration potential will be described.

10549

Nicolas, D.P. (NASA, George C. Marshall SFC, Astrionics Lab., Technol. Div., Huntsville, Ala.)
ROLE OF SEM IN MICROCIRCUIT FAILURE ANALYSIS. pp. 955-62. Scanning Electron Microscopy/1974. Proceedings of the 7th Annual Scanning Electron Microscope Symposium. Part I. Seventh Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Scanning Electron Microscopy and the Plant Sciences. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. Part III. Workshop on Advances in Biomedical Applications of the SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

The SEM provides a number of operational modes that allow the failure analyst to nondestructively examine a circuit and locate the troubled region. Many of the failure mechanisms to be investigated currently require at least the basic features which are provided by the SEM emissive mode. In many cases, simply observing a defect is not the same as confirming a failure mechanism, and to confirm an electrical fault requires the application of voltage contrast and conductive mode techniques. These provide a potential distribution map of the surface and a map of the depletion layers, respectively. Particulate and surface contaminations can be observed with the emissive mode, but their identification usually requires X-ray or Auger electron spectrometers. Despite the great potential of the SEM, the analyst must make an effort to examine a device in a proper perspective to elucidate a possible mechanism such as a lifted bond. The end product of these analyses is corrective action to eliminate or minimize the probability of a recurrence of the failure mechanism in new components.

10550

Flutie, R.E. (Harris Semiconductor, Melbourne, Fla.)
PROPER SEM INSPECTION OF IC STEP COVERAGE USING THE NASA GODDARD S-311-P12-A SPECIFICATION AS CRITERIA. pp. 963-70. Scanning Electron Microscopy/1974. Proceedings of the 7th Annual Scanning Electron Microscope Symposium. Part I. Seventh Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Scanning Electron Microscopy and the Plant Sciences. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. Part III. Workshop on Advances in Biomedical Applications of the SEM. Sponsored by the IIT Res. Inst. Part IV. Workshop on Failure Analysis and the SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

In an effort to help the SEM operator who is responsible for SEM inspecting semiconductor devices to the NASA-311-P12-A specification, proper inspection techniques are pictorially documented. Consistent use of 65° tilt angles can mask deficiencies in step coverage when the improper viewing direction is used. The proper use of 65° tilt angles yields additional information on cross-section reduction. In marginal metallization cases, the viewing direction should be such that the observer is looking along the anomaly and not into it. Through practical experience it has been found that poor substrate step geometry is the major cause of rejected metallization step coverage. When a run of sub-par step coverage is discovered, the slope of the substrate steps should be checked first. A conscientious SEM monitoring of substrate PSG step geometries has yielded a successful 98% prediction of passing the NASA 311-P12-A Specification.

10551

Christou, A. (U.S. Navy, Nav. Res. Lab., Washington, D.C.)
SEM FAILURE ANALYSIS TECHNIQUES FOR THIN FILMS AND MICROWAVE POWER TRANSISTOR METALLIZATIONS. pp. 971-8. Scanning Electron Microscopy/1974. Proceedings of the 7th Annual Scanning Electron Microscope Symposium. Part I. Seventh Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Scanning Electron Microscopy and the Plant Sciences. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. Part III. Workshop on Advances in Biomedical Applications of the SEM. Sponsored by the IIT Res. Inst. Part IV. Workshop on Failure Analysis and the SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

In the present paper we report SEM analysis techniques used to study surface diffusion, intermetallic formation, oxidation and corrosion in microwave power transistor metallizations of Ta/Au, Pt/Ta/Au, Pd/Ta/Au, W/Au and Mo/Au. The oxidation and corrosion reactions were studied in the specimen absorbed current mode (SCA). Interdiffusion reactions in the multilayer films were studied using backscattered electrons (BSE). Contrast variations resulting from intermetallic compound formation can be observed readily because of the dependence of the backscatter coefficient on the atomic number Z. In addition, metallization failures resulting from thin film interdiffusion and intermetallic formation were analyzed with an electron microprobe (EPA) and energy dispersive X-ray (EDXA) analysis attachment.

10552

Clifford, J.R., Sega, R.M. and Foos, G.D. (U.S. Air Force Academy, Dept. of Phys., Colorado Springs, Colo.) and Throckmorton, A.A. (Hewlett-Packard Corp., Colorado Springs, Colo).
SEM EXAMINATION OF THE AU-AL INTERMETALLIC ON IC LEAD BONDS. pp. 979-86. Scanning Electron Microscopy/1974. Proceedings of the 7th Annual Scanning Electron Microscope Symposium. Part I. Seventh Annual Scanning Electron Microscope Symposium. Sponsored by the IIT Res. Inst. Part II. Workshop on Scanning Electron Microscopy and the Plant Sciences. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Biological and Medical Sciences. Part III. Workshop on Advances in Bio-medical Applications of the SEM. Sponsored by the IIT Res. Inst. Part IV. Workshop on Failure Analysis and the SEM. Sponsored by the IIT Res. Inst. and the National Science Foundation--Division of Materials Research. Part I. Apr. 8-9, 1974. Part II, III, IV. Apr. 10-11, 1974. Pick Congress Hotel, Chicago, Ill., 1064 pp.

An investigation of the Al-Au intermetallic formation on integrated circuit (IC) lead bonds has been undertaken using the scanning electron microscope (SEM). Thermocompression bonding techniques were used to attach the Au leads to the Al pads of production ICs. The temperatures of the capillary, through which the Au wire passes, and the stage, on which the chip sets, varies. The secondary electron mode of the SEM was used to observe the intermetallic (commonly called "purple plague") formed on the lead bond at fabrication, during accelerated testing under high temperature, and through 2000 hours of live testing. After fabrication there was little observable plague on the pulse-heated stage ICs and considerably more growth on the hotter-stage ICs. Kirkendall voids and Au migration were observed on several ICs and deterioration of the Au bond occurred within eight hours of 400°C exposure. Heating the ICs to 125°C during live testing caused extensive intermetallic formation within 2000 hours.

10555

Konnowski, S.G. and Hall, R.D. (Westinghouse Defense and Electronic Systems Center, Systems Dev. Div., Baltimore, Md.)
NONPLANAR INTERCONNECTIONS FOR VLSI PACKAGING. Rept. no. 74-0555, Final Rept., June 22, 1973-Apr. 15, 1974, 52 pp., May 1974. N00163-73-C-0524

This program was undertaken to extend the technology of aluminum beam interconnects to the various metallizations found in hybrid VLSI packages. These included electroplated gold on alumina, thick-film gold on alumina, and thin-film aluminum on silicon wafers. All interconnections were made in a nonplanar configuration to simulate the step that occurs from the substrate/wafer upper surface to the package base. Numerous bond samples were made for verification of the approach, and four mechanical and environmental tests were performed on groups of these bonds. The tests were thermal shock, vibration, temperature cycling, and high-temperature storage. The successful results of the techniques, improvements, and environmental testing have indicated that a novel, producible, and quite reliable method for large scale interconnections of all the various materials included in VLSI packages can be achieved.

10558

U.S. Dept. of Commerce, Natl. Bur. of Standards, Electronic Technol. Div., Washington, D.C.
SEMICONDUCTOR MEASUREMENT TECHNOLOGY Rept. no. NBS-SP-400-1, Quart. Prog. Rept. no. 21, July 1-Sept. 30, 1973, 58 pp., Mar. 1974. AD 775 919

Significant technical accomplishments during this reporting period included:

1. extension of the technique for measuring thermally stimulated current and capacitance to include measurements on metal-oxide-semiconductor (MOS) capacitors
2. completion of the development of the thermal response method for evaluation of transistor die attachment
3. analysis of the interlaboratory comparison of transistor scattering parameter measurements, and
4. preliminary review of measurement problems in the photo lithographic aspects of semiconductor device processing, of problems associated with certain hermeticity testing procedures, and of methods for evaluating metallization step coverage.

10559

Polcari, S.M. and Sowe, J.J. (U.S. Dept. of Transportation, Transportation Systems Center, Cambridge, Mass.)
EVALUATION OF NONDESTRUCTIVE TENSILE TESTING. Rept. no. DOT-TSC-NASA-71-10, Tech. Rept., 46 pp., May 1971. N71-37516. NA08

This report presents the results of a series of experiments performed in the evaluation of nondestructive tensile testing of chip and wire bonds. Semiconductor devices were subjected to time-temperature excursions, static-load life testing and multiple pre-stressing loads to determine the feasibility of a nondestructive tensile testing approach. The report emphasizes the importance of the breaking angle in determining the ultimate tensile strength of a wire bond, a factor not generally recognized nor implemented in such determinations.

10560

Stinnett, D., Der Marderosian, A. and Nelson P. (Raytheon Co., Equip. Div., Waltham, Mass.)
WEIGHT TEST METHOD DETECTS GROSS LEAKS IN COMPONENTS. Evaluation Eng., 4 pp., Sept. - Oct. 1976

During the past several years, many attempts have been made to improve or devise new gross leak test methods for electronic components. Various methods listed in different test documents have been evaluated for the purpose of determining the adequacy, sensitivity, and repeatibility of the different gross leak tests.

10561

Dicken, H.K. (Integrated Circuit Eng., Scottsdale, Ariz.)
ENVIRONMENTAL CONDITIONS OF AUTOMOTIVE ELECTRONIC SYSTEMS. 15 pp.

It is expected that the combination of the severe electrical environmental problems along with the extreme temperature ranges and the environmental contaminants such as salt, water, alcohol, ethylene glyco, hot oil, gasoline, etc. will increase semiconductor failure above the present reported levels. New system design and packaging approaches must be utilized to obtain acceptable reliability levels.

10562

Foster, R.C. (Xerox Corp., Rochester, N.Y.)
JUSTIFICATION FOR SCREENING AND TESTING IC'S TO MORE STRINGENT QUALITY LEVELS. 6 pp., Mar. 1, 1972

Cost comparisons are presented as the total number of IC per board varies for three quality screening levels. For the assumptions presented and the added cost for each screen, the results justified the screens.

10566

IEEE
PROCEEDINGS 1974, 24TH ELECTRONIC COMPONENTS CONFERENCE. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

Sessions:

I	Display Technology
II	Reliability
III	Contact Technology
IV	Hybrid Materials
V	ISHM Panel Discussion on Standards
VI	Discrete Components
VII	Academic Microelectronic Programs
VIII	Manufacturing Technology
IX	Capacitors
X	Functional Tuning of Hybrids
XI	Hybrid Packaging

10567

Hall, T.C. and Webster, S.L. (Hughes Aircraft Co., Culver City, Calif.)
RELIABILITY ASPECTS OF MODULE DEFOAMING OPERATION. pp. 25-8. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids, and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

A new and simpler method employing a directed stream of airborne glass beads avoids the hazard of gross mechanical damage, is much faster and more precise in its action and requires only modest skill. In this technique an air-jet driven stream of solid approximately spherical glass beads (diameter = 0.001 inch) is directed at the foam in the desired location. A modified white "Airbrasive" hand held jet tool is used. This paper discusses the effect of this method of foam removal upon the performance and reliability of components in reworked foamed-in modules.

10568

Zatz, S. (Martin Marietta Aerospace, Orlando, Fla.)
A NEW SIMPLIFIED METHOD TO MEASURE MOISTURE IN MICRO ENCLOSURES. pp. 29-33. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

A new technique has been perfected to accurately measure the moisture content in small volumes typified by semiconductor and integrated circuit packages. The methodology uses an inexpensive, easily fabricated moisture monitor that incorporates two bond wires in a standard package. After package seal as part of a production seal run, the dew point can be directly and accurately measured. A recognized direct relationship exists between dew points and moisture content. Comparison with other techniques and life tests of moisture sensitive parts have demonstrated the validity and effectiveness of this approach. The new technique eliminates the gross errors that are introduced when the micro-volume is drawn into a large volume test manifold. This technique is currently being used to certify the process controls and seal effectiveness of critical integrated circuits for a high reliability system. Future effort will be directed at automating this test method and including it in MIL-STD-883.

10569

Vahaviolos, S.J. (Western Elec. Co., Eng. Res. Center, Princeton, N.J.)
REAL TIME DETECTION OF MICROCRACKS IN BRITTLE MATERIALS USING STRESS WAVE EMISSION (SWE). pp. 34-42. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

An attempt was made to explain SWE in brittle materials. Most of the work performed by the author as well as numerous other researchers is heuristic in form. A complete solution to the wave as well as to the vibration equation as it applies to SWEs is not yet known. The boundary conditions are unknown most of the time due to the specimen to be tested. The author believes that accurate prediction of crack growth is possible from equations given.

10570

Azarewicz, J.L. and Wrobel, T.F. (Intelcom Rad. Tech., San Diego, Calif.)
RADIATION-STIMULATED FAILURE MECHANISM IN A DIELECTRICALLY ISOLATED INTEGRATED CIRCUIT. pp. 48-52. F04701-72-C-0322. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

An apparent latchup condition has been observed in a dielectrically isolated integrated circuit. This circuit has been analyzed with nondestructive tests using Linac and laboratory measurements, and the failure mechanism has been identified. The device package was then opened, and the failure path was verified visually. Upon removal of a metalization short, which was the cause of the failure, the device returned to normal operation.

10571

Kobayashi, T. and Murase, K. (Nippon Elec. Co., Ltd., IC Div., Kawasaki, Kanagawa, Japan)
CHARACTERISTICS OF MULTI-LAYERED METALLIZATIONS CONSISTING OF TANTALUM AND ALUMINUM ON SILICON AND OR Si_2. pp. 79-82. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

It is well-known that preferential anodization of aluminum realizes "the Planar Interconnection" for silicon integrated circuits. In order to obtain an improved version of the Planar Interconnection, several multilayered metallization structures have been investigated. As a result, a multilayered structure consisting of Al-Ta or Al-Ta-Al has turned to be the best from the facility point of both evaporation and anodization and from the utility point of Ta gettering action regarding ionic contamination. The object of this paper is to present some characteristics of electrical contacts and passivation effect of these multi-layered metallizations.

10572

Kuo, C.Y. (Engelhard Minerals & Chem. Corp., Engelhard Ind. Div., Electro Metallics Dept., East Newark, N.J.)
AIR FIRABLE NICKEL CONDUCTORS. pp. 83-6. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

The air firable Ni-conductor pastes, fritted and fritless, can be fired from 600 to 1000°C with a sheet resistance of 0.03 to 0.1 ohm per square and a TCR of 6000±600 ppm/°C. After tinning, the sheet resistance and TCR of Ni-conductors reach those of tinned precious metal conductors in the range of 0.004±0.002 ohm per square and 2500±500 ppm/°C. The adhesion, or pull strength, of nickel conductors after soldering is comparable with most of the previous metal conductors (more than 3,000 pounds per square inch). In addition to the advantage of low cost, the leach resistance and resolderability of nickel conductors are unique, and superior to those of most precious metal conductors. The possible applications include partial replacement of Moly-manganese or precious metal conductors, and a number of current and new products in microelectronics.

10573

Bacher, R.J., Sproull, J.F. and Rosenberg, R.M. (E.I. du Pont de Nemours & Co., Electronic Matls. Div., Photo Prod. Dept., Wilmington, Del.)
THICK FILM TEMPERATURE-COMPENSATING CAPACITOR DIELECTRICS. pp. 87-93. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

Two new screen printable temperature compensating (TC) capaciator dielectrics, NPO and N150, have been developed which are cofireable with existing conductor compositions. Both printing technique and dielectric/conductor firing sequence markedly affect the number of electrical shorts that occur. Proper processing can lead to near 100% freedom from shorts.

10574

Burgess, J.F. and Neugebauer, C.A.

10574

Burgess, J.F. and Neugebauer, C.A. (GE, Corporate Res. and Dev., Schenectady, N.Y.) and Flanagan, G.T. (GE, Heavy Military Electronic Systems Prod. Dept., Syracuse, N.Y.)
HYBRID PACKAGES BY THE DIRECT BONDED COPPER PROCESS. pp. 94-7. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

A method of constructing hybrid packages by a metal-ceramic attachment method called Direct Copper Bonding offers ome distinct advantages over the thick film approach and is the subject of this paper. The process and mechanism of the direct bonding process will be discussed, and examples of direct bonded structures and hybrid packages will be given.

10575

Clay, F.A., Panousis, N.T. and Pierce, R.W. (Bendix Corp., Kansas City Div., Kansas City, Mo.)
CHARACTERIZATION OF A CHROMIUM-GOLD DEPOSITION PROCESS FOR THE PRODUCTION OF THIN FILM HYBRID MICROCIRCUITS. pp. 98-104. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

A study was made of adhesion, electrical resistivity, and thermocompression bondability of chromium-gold films which had been deposited on tantalum nitride-coated aluminum oxide substrates. The thin films studied consisted of three layers of metallization: tantalum nitride-chromium-gold. Since the conditions needed to produce good tantalum nitride films has been determined previously, only the chromium and gold deposition process was investigated in this work.

10576

Niwa, K., Nakamura, J., Murakawa, K. et al. (Fujitsu Labs. Ltd., Japan)
NEW ALUMINA SUBSTRATE FOR HYBRID INTEGRATED CIRCUITS. pp. 105-10. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

A new alumina substrate with extremely smooth surface was developed. This new alumina substrate Cr_2O_3 and MgO as the the additives. Tantalum nitride or tantalum and tantalum oxide films were applied as resistor or capacitor to the unglazed (as-fired) new alumina substrates having a surface roughness of less than 0.05μm in CLA. Reliability and characteristics of thin films were examined in comparison with that on the glazed alumina. Experimental results show good reliability and good stressed aging characteristics concerning the sputtered and evaporated tantalum thin film resistors and capacitors on the unglazed (as-fired) alumina substrates having a surface roughness of 0.03μm CLA. Therefore, it is obvious that the alumina substrate with added Cr_2O_3 and MgO having 0.03μm in CLA maintains a good quality and reliability of the thin film capacitors on the unglazed alumina substrate as well as resistors.

10577

Yamazaki, J., Kamo, T. and Nakamura, M. (Fujitsu Labs. Ltd., Japan)
HIGH DENSITY THIN FILM HYBRID IC UTILIZING Ta-Al-N RESISTOR AND Ta_2O_5-MnO_2 CAPACITOR. pp. 111-7. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

A new integration technology has been developed through combining the Ta-Al-N thin film resistor and the Ta_2O_5-MnO_2 capacitor on a smooth-surface alumina substrate. Summarized results obtained by this technology are following:

1) Optimum resistor properties for high density circuit are achieved by the Ta-Al-N system. This gives a high sheet resistance of 500 ohm/sq with controlled TCR in good reproducibility.
2) Ta_2O_5-MnO_2 structure for high density capacitor realizes capacitance per area of 2000 pF/mm^2 holding the good reliability. TCC and loss factor are improved by chemical treatment.
3) RC circuit size is reduced at least to one-fourth compared with that composed of Ta-N resistor and Ta_2O_5 capacitor.

10578

Anon.
ISHM PANEL DISCUSSION ON HYBRID STANDARDS. pp. 118-20. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

ISHM has established a Committee on Standards to create an ISHM activity in the area of specifications and standards for hybrid microelectronic technology to primarily serve the needs of the membership of ISHM. The priority effort of this committee has been to assemble a Specification for Microelectronic Hybrids which covers the industrial, commercial, consumer, military, aerospace, and NASA application requirements. ISHM intends to offer the results of this task to industry and government for their use.

10579

Estep, G.J. (Bendix Corp., Electrodynamics Div.)
HIGH STABILITY MATCHED ACTIVE FILTERS FOR SONAR PROCESSING. pp. 121-9. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

This paper will describe the design, performance and manufacturing procedures used to realize a complex bandpass active filter. Developed for use in sonar processing applications the filter is required to provide a high degree of matching on a paired basis and is constructed for maximum similarity and thermal coupling of complementary components in the two-filter package. A total of 8 sets of filter pairs are required for the current application.

10580

Hukee, V. and Burks, D. (Sprague Elec. Co., North Adams, Mass.)
THE RELIABILITY OF LASER-TRIMMED SCREEN-PRINTED METAL FILM RESISTORS. pp. 138-47. Proceedings 1974, 24 Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

The majority of the failures which have been analyzed are not due to the characteristics of the resistor system or of the trimming technique, but to assembly or encapsulation defects. An example of the data collection technique employed is shown. In summary, it can be concluded in reliability to air-abrasive trimmed resistors, and in some configurations of mechanical design and encapsulant systems they may be superior.

10581

Remke, R.L. and Burdick, G.A. (U. of So. Fla., Dept. of Elec. and Electronic Systems, Tampa, Fla.)
SPIRAL INDUCTORS FOR HYBRID AND MICROWAVE APPLICATIONS. pp. 152-61. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

This paper has presented five different relations for determining the inductance of spiral inductors. It has been shown that three of the inductance relations were based on configurations very different from the spiral case. The accuracy obtained in using these relations appears fortuitous since their limitations were often exceeded. Another inductance relation seems to overlook many important principles which causes it to seriously underestimate the inductance. To overcome many of the shortcomings of the previous equations, a new relation was formulated that accurately determines the inductance. The new relation is based on a general technique that not only determine the inductance of an inductor with or with out a ground plane but is also applicable to such problems as multi-layer spiral inductors.

10582

Hass, B., McLeod, W.W. and Thun, R.E. (Raytheon Co., Bedford, Mass.)
A METHOD FOR THE RAPID AND ECONOMICAL GENERATION OF HYBRID LSI CIRCUITS. pp. 172-6. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

This paper describes advances in the development of high density thick film hybrid circuits achieved by the use of new fritless inks and photolithographic masking techniques. These techniques have been combined with improved beam-lead logic arrays, computerized routing and simpler P.C. boards to provide digital hybrid circuits and modules of considerably lower cost and reduced development time. This new Hybrid LSI technology has been demonstrated in the development of an advanced LSI computer. The paper will provide a functional description of the automatic routing program for hybrid circuits.

10583

Ilgenfritz, R.W., Mogey, L.E. and Walter, D.W. (Raytheon Co., Bedford, Mass.)
A HIGH DENSITY THICK FILM MULTILAYER PROCESS FOR LSI CIRCUITS. pp. 177-80. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

This technology includes a fine-line Multilayering capability which can be used either to decrease the size of hybrid circuits, or conversely, to provide an increase in the number of conductor channels in an ordered "Matrix" interconnect structure - a general requirement of computer aided design and routing programs. The latter application is the subject of this paper and describes the processing methods of the computer routed hybrid LSI circuit.

10584

Gillis, T.B. and Lash, R.E. (Raytheon Co., Quincy, Mass.)
LOW TEMPERATURE PROCESSING FOR HI-REL MULTI-CHIP HYBRIDS. pp. 181-5. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

Testing to date indicates that the proposed low temperature processing is in every respect as reliable as techniques previously used for high-rel, thick-film modules. This process has been introduced into production and four different hybrid module types are being produced using the epoxy die attach, ultrasonic gold ball bonding and welded seal techniques. It is difficult to make a one for one yield comparison between the conventional process and the new, low-temperature process because of all the other variables that affect yields, but at a minimum, there has been a 5% yield improvement on all module types with considerably more improvement on certain complex types. An added advantage, not discussed, is the repairability of modules. Chips that were originally die attached with epoxy are easily removed using a standard die attach machine with a heated collet. In many cases, even after the final seal is made the cover can be machined off, repairs made, module cleaned and a new cover seam-welded on.

10585

Scapple, R.Y. and Keister, F.Z. (Hughes Aircraft Co., Culver City, Calif.)
FABRICATION AID FOR HYBRID MICROCIRCUITS. pp. 186-91. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

The purpose of the Fabrication Aid is to reduce the cost of fabricating thin film hybrid microcircuits. It accomplishes this by reducing labor costs and by minimizing assembly errors. The Fabrication Aid is a means of microprinting fabrication instructions directly on the thin film substrate. The information is permanent and remains throughout the life of the unit. The technique involves the application of a photosensitive material to the substrate, which is then photo-exposed and developed through an appropriate mask. This defines the identification and instruction markings. At this point the photosensitive material is nearly transparent and not legible. As a final step, the pattern is darkened to give the necessary visual contrast with the remainder of the substrate. Darkening is done by a gradual elevated temperature exposure in air. Legibility, when viewed under a microscope, is analogous to conventional printing on a newspaper when viewed by the unaided eye.

10586

Martin, R.E., Stirling, A.J. and L'Archeveque, J.V.R. (Atomic Energy of Can. Ltd., Chalk River Nuc. Labs., Chalk River, Ontario, Can.)
THE FABRICATION OF REPRODUCIBLE THICK FILM RESISTORS. pp. 192-8. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

Parameters affecting the production of thick film resistors have been studied experimentally using volumetric ink transferred to the substrate, effectively controlling resistor values, can be quite insensitive to variations of printer parameters over wide ranges. In practice, resistor batch mean values can be kept within 5% from day to day. A printing process with these characteristics reduces, or even eliminates, trimming requirements. The insensitivity of resistance to printer parameters cannot be explained by generally accepted theories predicting that the quantity of ink pushed into the screen depends heavily on these parameters. However, it has been demonstrated experimentally that the volume of ink deposited on the substrate depends primarily on the interaction forces between the screen, substrate, and ink. An hypothesis is formulated to show that, providing adequate ink is fed into the screen, the equillibrium between these forces acts as a self-compensating mechanism responsible for a uniform deposited volume over a wide range of printer settings.

10587

Scapple, R.Y. (Hughes Aircraft Co., Culver City, Calif.)
A TRIMMABLE PLANAR CAPACITOR FOR HYBRID APPLICATIONS. pp. 203-7. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

In certain high frequency and fast pulse rise time circuits, low value capacitors trimmable to close tolerances are required. This paper describes a technique for designing and fabricating capacitors of this type. It includes the derivation of a simplified design equation that permits a low value capacitor to be designed readily. The capacitor may be integrated directly into the film substrate (no interconnections are required) or it may be fabricated as a chip and added to the hybrid as a discrete component.

10588

Both, E. (U.S. Army, Electronics Technol. and Devices Lab., Fort Monmouth, N.J.)
THERMAL AND RADIATION POLARIZATION IN ORGANIC DIELECTRIC FILMS. pp. 208-15. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

The polarization behavior of poly (ethylene terephthalate), polycarbonate and polysulfone has been determined in response to treatments with applied electric bias at elevated temperature and in a ^{60}cobalt gamma radiation field at room temperature. Characteristic differences are found in the magnitude of the polarization and its stability against thermal discharge for the different materials as well as for the different treatments. The quantitative results are of the interest for the use of capacitors and other dielectric devices in a nuclear radiation environment and provide a basis for worst-case estimates.

10589

Hurtig, III, G. (Kinetic Technol., Inc., Santa Clara, Calif.) and Swensor, E.J. (Electro Sci. Ind., Inc., Portland, Ore.)
AN OVERVIEW OF LASER FUNCTIONAL TRIMMING TECHNIQUES. pp. 240-4. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

Functional trimming using lasers is gaining acceptance throughout the industry for a wide variety of applications. This paper is intended to provide a summary of the most important concepts involved. References are provided to allow the reader to research specific areas in greater detail.

10590

Faber, M., Jr. (Hewlett-Packard, Loveland, Colo.)
ALGORITHMIC TRIMMING ON ACTIVE CIRCUITRY. pp. 248-54. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

An entire digital autoranging multimeter has been manufactured utilizing a single small printed circuit board in conjunction with a hybrid substrate. Thin film resistors on the hybrid substrate are laser trimmed while the multimeter circuitry is operating. This "active trimming" process has been instrumental in making the production of the instrument possible. When the decision is made to trim actively, the trim algorithm becomes an important aspect of the design. This paper outlines three types of trim algorithms, and discusses specific problems concerning the marriage of active circuitry with a laser trim system.

10591

Bingham, K.C. and Naylor, R. (Internatl. Computers Ltd., Res. and Advanced Dev. Centre, Microsystems Sector, Engl.)
MULTILAYER INTERCONNECTION TECHNIQUES APPLIED TO HIGH SPEED COMPUTER SYSTEMS. pp. 255-61. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

Efficiently designed interconnection systems for electronic computers attempt to partition the logic circuits into several hierarchical levels, each containing a degree of complexity which balances the difficulty of manufacture against the cost. Continuity of progress in the semiconductor field has been maintained to the stage where the thermal and volumetric limitations present a packaging problem which can be solved using hybrid methods of assembly.

10592

Bachner, F.J., Cohen, R.A., Mountain, R.W. et al. (MIT, Lincoln Labs., Lexington, Mass.)
A HYBRID INTEGRATED SILICON DIODE ARRAY FOR VISIBLE EARTH-HORIZON SENSING. pp. 262-6. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

An earth-horizon sensing device, operating principally in the visible portion of the spectrum, has been designed, fabricated and tested for use in MIT, Lincoln Laboratory's LES 8/9 communications satellites as part of the system which maintains the satellites orientation with respect to earth. The complete hybrid circuit, shown schematically consists of four .226" x.338" silicon chips mounted on a 2.0" x 2.0" x 0.025", 99.5% alumina substrate. Each of the four silicon chips contains eight photodiodes whose active area is .032" x 0.170". This paper discusses the techniques used in the fabrication of the photodiodes and the thin-film ceramic substrate and in the assembly of the hybrid.

10594

Calkins, R.A. and Hickey, M.T. (Micro Networks Corp., Worcester, Mass.)
A MICROELECTRONIC ANALOG TO DIGITAL CONVERTER. pp. 274-8. Proceedings 1974, 24th Electronic Components Conference. Sponsored by the Electronics Industry Association (EIA) and the Parts, Hybrids and Packaging Group of the IEEE. Statler Hilton, Washington, D.C., May 13-15, 1974

This paper describes a unique 12 Bit Analog to Digital Converter which will convert signals more accurately in a package 1/20th the size of the traditional converter module. The design, operation, and comparison of various D/A approaches are covered. Emphasis is placed on key components such as the D/A converter, logic programmer, and high speed comparator. Error analysis illustrates effects of gain, offset, and speed of critical components on overall performance. The advantages of size, performance, and cost using thin film hybrid assembly and construction techniques are explored.

10596

Kohn, E.S. and Schultz, M.L. (RCA, Princeton, N.J.)
CHARGE-COUPLED SCANNED IR IMAGING SENSORS. Rept. no. AFCRL-TR-74-0056, Rept. no. PRRL-74-CR-1, Semiaan, Tech. Rept., 66 pp., Jan. 14, 1974. F19628-73-C-0282

The purpose of this program is to demonstrate the feasibility of using charge-coupled arrays for sensing images in the infrared. An important use for such arrays is the observation of scenes by their own thermal radiation. Devices which accomplish this are already in existance and, in many cases, perform close to their theoretical limits. These devices (Forward Looking Infrared Radar (FLIR's) use linear arrays of cooled IR detectors with mechanical scanning. The device proposed here is cheaper, smaller, less subject to failure due to mechanical difficulties, and, because it has frame storage, it outperforms, in principle, all existing devices. It has the advantage of vidicontype operation while avoiding the problems of insufficient beam current density and insufficient target capacitance that have, up to now, hampered vidicons for thermal imaging.

10599

Tasca, D.M., Peden, J.C. and Andrews, J.L. (GE, Space Div., Valley Forge SC, Philadelphia, Penn.)
THEORETICAL AND EXPERIMENTAL STUDIES OF SEMICONDUCTOR DEVICE DEGRADATION DUE TO HIGH POWER ELECTRICAL TRANSIENTS. Rept. no. 73SD4289, Final Rept., Mar. 6, 1972-Dec. 31, 1973, 138 pp., Dec. 1973. DAAG39-72C-0066

An objective of the present work was to examine the assumptions made in employing such experimental predictions failure models for complex waveshapes and, in turn, to develop a more refined analytical methodology for the prediction of semiconductor burnout for complex transients based upon test data obtained from rectangular pulse failure experiments. This report summarizes the experimental program, the development of the complex waveform thermal damage model and the correlation of experimental device damage levels with damage levels predicted by the model.

10600

FOCUS ON COOLING ELECTRONIC PACKAGES. Electronic Design 22, no. 14, 62-72 July 5, 1974

It's generally accepted that the semiconductor failure rate is halved for each 10°-C reduction in the junction temperature below maximum. How do you keep electronic components and packages cool? The problem is exacerbated by the trend to higher packaging densities.

10603

SOS DEVICES: NOT YET MAKING IT IN LSI... BUT WAIT TILL NEXT YEAR. Electronic Design 22, no. 16, 3 pp., Aug. 2, 1974

Silicon-on-sapphire technology is not as yet a major factor in the LSI arena but commercialization of SOS is imminent. SOS can be used with most of the semiconductor technologies--PMOS, NMOS and CMOS. Much of the early work is expected to be in CMOS. Several CMOS/SOS devices are now available and more are expected to make their commercial debut in 1975.

10604

Burock, R., Debolt, J.R. and Parente, R.N.
MANUFACTURING BEAM LEAD INSULATED-GATE, FIELD EFFECT TRANSISTOR (IGFET) INTEGRATED CIRCUIT. The Western Elec. Engr. pp. 3-16, July 1973

Insulated-gate field effect transistors, in which the flow of unipolar current between source and drain terminals in a semiconductor gate electrode, offer significant advantages as components of integrated circuits. Beam lead integrated circuits composed entirely of these devices are currently manufactured at the Allentown Works.

10605

SOLDERING VS WELDING FOR LARGE-PACKAGE HERMETIC SEALS. Circuits Mfg., pp. 24-7, Nov. 1972

Efforts to improve hermetic seals on hybrids by Raytheon for ECOM are reported. Factors which lead Raytheon to choose parallel-seam welding and passover other techniques are discussed.

10606

Motorola Semiconductor Prod. Inc., Phoenix, Ariz.
Motorola Solid-State Technol. 3, no. 1, 1-24, 1973

Contents
Metal Gate PMOS: Age-Old Fighting Technique Solves Analog Delay Function
RF Design: Innovations Help 45-Watt, Two-Stage Amplifier Achieve Octave UHF Bandwidth
Metallurgy: Al-1% Si Vs. Al-1% Mg Wire Bond Failure--Testing Techniques and Analysis Yield Reliability Gains
Auger Spectroscopy: Improves Device Reliability
Silicon Gate CMOS: Low Power, Low Voltage Digital Systems Look Beyond Existing Technologies
Power/IC's

10607

Huntington, R. (Motorola Semiconductor Prod. Inc., Phoenix, Ariz.)
RF DESIGN: INNOVATIONS HELP 45-WATT, TWO-STAGE AMPLIFIER ACHIEVE OCTAVE UHF BANDWIDTH. Motorola Solid-State Technol. 3, no. 1, 6-9, 1973

The use of hybrid, integrated circuit technology provided a way to develop an improved amplifier for airborne radio transmitters. Hybrid quandrature couplers and a unique new thin film transmission line impedance transformer were used in a prototype two-stage, 45-watt amplifier providing greater than 12 dB power gain with variation less than +2 dB over the 225-400 MHz band. The design is housed in a hermetic case occupying only 3.8 in^3.

10608

Philofsky, E.M. and Ravi, K.V. (Motorola Semiconductor Prod. Inc., Phoenix, Ariz.)
METALLURGY: Al-1% Si VS. Al-1% Mg WIRE BOND FAILURE--TESTING TECHNIQUES AND ANALYSIS YIELD RELIABILITY GAINS. Motorola Solid-State Technol. 3, no. 1, 10-3, 1973

Operating stresses and high manufacturing temperatures can change silicon distribution in Al-1% Si wire resulting in potential wire bond failures. Studies reveal Al-1% Mg wire retains its strength and elongation after annealing at high temperatures. The result--wire bonds exhibiting superior fatigue resistant characteristics.

10609

Gonzales, A.J. (Motorola Semiconductor Prod. Inc., Phoenix, Ariz.)
AUGER SPECTROSCOPY: IMPROVES DEVICE RELIABILITY. Motorola Solid-State Technol. 3, no. 1, 14-7, 1973

There's a new, highly effective surface analysis technique now in use at Motorola. Auger Electron Spectroscopy a sophisticated system which plays a dramatic role by detecting and identifying impurity concentrations previously unmeasurable.

10610

Weissberger, A.J. (Natl. Semiconductor, Santa Clara, Calif.)
MOS/LSI MICROPROCESSOR SELECTION. Electronic Design 22, no. 12, 100-4, June 7, 1974

There are basic hardware, software and design points to consider before you start a microcomputer design. With the suddenly popular MOS/LSI microprocessor turning up in many new and intriguing applications, some down-to-earth questions are confronting designers: Is a microprocessor right for my application? If it is, which one should I choose? Microprocessors are used primarily to replace or upgrade random-logic designs. Selection problems can be simplified by careful analysis of hardware requirements, software capabilities and the design aids offered by manufacturers.

10611

Wey, S.J. and Lewis, G. (U. of Miss., Graduate Center for Matls. Res. and Dept. of Ceramic Eng., Rolla, Miss.)
MASS SPECTROMETRIC STUDIES OF GOLD-SILICON INTERFACE CONTAMINATION. J. of Vacuum Sci. & Technol. 10, no. 2, 413-5, Mar./Apr. 1973

It is important to remove residual fluoride by subsequent washing in distilled water in order to insure good device characteristics. It is the purpose of this communication to report on the observation of residual fluorine and other contaminants evolved from silicon and gold-silicon substrates.

10613

Simmons, R. (Plessey Co. Ltd., Allen Clark Res. Centre, Great Britain)
FEASIBILITY STUDY ON RADIATION HARDENED DEVICES AND CIRCUITS. Rept. no. RP9-131, Ann. Res. Rept. Nov. 1972-Oct. 1973. 18 pp., Oct. 1973. AD 916 462. N/CP16/1717/67

This report describes the most recent work carried out in the feasibility study phase of a program directed at producing a radiation resistant integrated circuit technology on a junction isolated bipolar process. Experimental results are shown for both neutron and transient ionizing radiation environments. Feasibility to a reasonable degree having been demonstrated, the report describes the program of work being undertaken to design and construct a radiation-hardened amplifier/comparator circuit on this process using breadboard photocurrent simulation techniques.

10614

Watts, B.E. (Plessey Co., Ltd., Allen Clark Res. Center, Great Britain)
THE PREPARATION AND PROPERTIES OF ELEMENTAL SEMICONDUCTOR THIN FILMS. Thin Solid Films 18, no. 1, 1-23, May 14, 1973

This review surveys the preparation and properties of elemental semiconductor thin films, with particular emphasis on material for semiconductor device applications. Epitaxial film deposition techniques are described and recent advances in low temperature epitaxial silicon growth discussed. Work on epitaxial semiconductor films on insulators, and on polycrystalline and amorphous films is also reviewed.

10615

Macey, R.A. (Assoc. Semiconductor Mfr. Ltd. Dev. Lab., Southampton, Great Britain)
INVESTIGATION AND ASSESSMENT OF INJECTION LOGIC FOR L.S.I. FUNCTIONS. Rept. no. RP6-71, Ann. Rept. no. 1, C.V.D. Res. Proj. RP6-71, 21 pp., Oct. 1973. AD 916 168. N/CP1715/67

It has been established that injection logic elements are capable of operation over the military temperature range of -55°C to + 125°C using available diffusion processes. Studies of high speed counting stages in injection logic, TTL compatible input stages, LED display driving, multiplexing to displays, and stabilization of injection logic dynamic performance against supply voltage variations have been undertaken. Logic verification and chip layout have been started on an LSI investigation module; a study of this module will conclude the first phase of the project.

10617

Bower, D.E., Oliver, C.B., Harwood, M.G. et al. (Assoc. Semiconductor Mfr. Ltd. Dev. Res., Southampton, Great Britain)
RELIABILITY OF FLIP CHIP BONDS. Rept. no. RP-72/73, Ann. Rept. no. 1, C.V.D. Res. Proj. no. RP6-72, 16 pp., Oct. 1973. AD 916 830. N/CP1715/67

The project objectives of this report are: The comparison of the reliability of aluminum and solder bump flip chip bonds under various types of stress and to investigate the associated failure mechanisms, and assess the effect of flip chip bonds on the electrical and thermal performance of silicon semiconductor devices. The project emphasis is on the qualitative determination of the good and bad reliability features of a wide range of bonding systems, rather than an exhaustive quantitative study of one or two systems. Test devices and corresponding substrates have been designed and produced. They are being bonded together to produce assemblies for the reliability program.

10618

McDowell, J.J. (Monolithic Memories, Inc., Sunnyvale, Calif.)
IMPROVE ROM SYSTEMS WITH pROMS. Electronic Design 22, no. 14, 92-6, July 5, 1974

With two design techniques that use programmable ROMs--the pROM patch and the pROM wire scrambler--you can alter a masked-ROM system after you're committed to masks. The pROM patch method changes words and handles increased address fields in ROM. The pROM wire-scrambler technique expands memory size simply and by a factor of two through the use of memories that have the same pinout and model number of the PC-board ROMs.

10619

Appelt, D. (Tex. Instr., Inc., Digital Systems Div., Austin, Tex.)
GET STANDBY LSI MEMORY POWER. Electronic Design 22, no. 12, 116-20, June 7, 1974

A small, low-cost battery system can keep a large-scale-integrated memory nonvolatile if the power goes out or is reduced critically. The standby system will provide time bursts of refresh cycles to keep the data intact for more than a month, while consuming a minimum of power from the battery.

10620

Adams, J.D. and Ballew, D.D. (Tex. Instr. Inc., Dallas, Tex.)
INTEGRATED CIRCUIT QUALITY AND RELIABILITY CONSIDERATIONS. pp. 1-7. WESCON '73. Also presented at INTERCON '74. N74-12208

A product maturity graph and cost trade-off examples are presented. Screening techniques are grouped as quality oriented and as reliability oriented. Effectiveness and applicability of screening techniques are discussed with emphasis on the importance of supplier/user interface. A typical failure mechanism chart is presented. Expectation of a two to one failure rate for MSI over SSI is explained with associated screening considerations.

10622

Athanas, T.G. (RCA, Solid State Div., Somerville, N.J.)
DEVELOPMENT OF COS/MCS TECHNOLOGY. Solid State Technol. 17, no. 6, 54-9, June 1974

Developments during the past few years have substantially alleviated the extreme difficulty that previously characterized monolithic fabrication of complementary MOS transistors; reliable and economical COS/MOS integrated circuits are now readily produced in large quantities. This article explains basic design and processing of COS/MOS integrated circuits and the recent technological advances that have made these circuits a production reality with an assured bright future in solid-state circuit applications.

10623

Robe, T. (RCA, Solid State Div., Somerville, N.J.)
TAMING NOISE IN IC OP AMPS: SIGNAL SOURCE IMPEDANCE AND OPERATING FREQUENCY BAND ARE THE KEYS TO SELECTION OF THE RIGHT BIPOLAR OR FET-INPUT OP AMP. Electronic Design 22, no. 15, 64-70, July 19, 1974

The selection of IC op amps for very-low-signal applications depends primarily on two parameters: the impedance of the signal source used and the operating-frequency band. Careful attention ot these parameters can help overcome the noise limitations of the otherwise extremely versatile monolithic op amp.

10625

Bosnell, J.R. and Lloyd, K.H. (Royal Radar Establ., Great Malvern, Worcestershire, Engl.)
A COMPARISON OF MANUFACTURING TECHNIQUES FOR HYBRID MICROWAVE CIRCUITS. pp. 287-91. A72-39496. Proceedings of the Technical Program. 1971 National Electronic Packaging and Production Conference. Brighton, Sussex, Engl., Oct. 19-21, 1971

It can be seen from the results that the dielectric losses are of the order of 1% of the conductor losses. The major influence of the substrate upon the total loss is therefore via its surface finish. Because of this, it is feasible to introduce a debased alumina to enable lower frequency circuits to be manufactured by the cheaper screen printing process. At higher frequencies, where finer lines are required, thin film processes are preferred, particularly when the anomalous behavior of thick film microstrip is taken into account. The most satisfactory thin film manufacturing method was found to be etching before plating, which reduces the amount of undercutting and hence the conductor loss per unit length.

10626

French, R.T. (Rockwell Internatl. Corp., Electronics Res. Div., Anaheim, Calif.)
CHARGE COUPLED MEMORY.
Rept. no. C73-754.9/501, Final Rept., June 28, 1973-Mar. 31, 1974, 35 pp., Apr. 9, 1974. N00163-73-C-0520

Charge-Coupled Memory (CCM) Devices, incorporating the nonvolatile storage features of MNOS structures into the charge-coupled device concept, have been fabricated and tested to determine applicability for BORAM utilization. A new concept, incorporating the MNOS sites as separate from the propagation channel was designed, fabricated, and tested during this phase of the program. Results of the evaluations do not offer a clear-cut indication that the CCM will meet BORAM requirements. Difficulties have been experienced in attaining high transfer efficiency, and in monitoring the results of the storage function.

10627

Ruegg, F. (Beckman Instr. Inc., Microcircuits Eng., Fullerton, Calif.)
WHY NOT USE HYBRIDS? Electronic Design 22, no. 14, 84-9, July 5, 1974

Hybrids provide greater circuit flexibility less problems with parasitics and they have the potential for greater precision, long-term stability and greater freedom in component selection. And hybrids can usually handle higher-power circuitry than monolithics. For small size, long-term reliability, true hermetic sealing and adaptability to the latest technologies.

10628

White, M.L.
ENCAPSULATING INTEGRATED CIRCUITS. Bell Labs. Record 52, no. 3, 78-83, Mar. 1974

Many encapsulating materials will give integrated circuits the protection they need, but only a few will do so and still not deteriorate at high temperatures and humidity. Silicone resins and rubbers-silicon-oxygen-carbon compounds-seem to have the best properties.

10630

Daimon, Y. and McGill, T.C. (Calif. Inst. of Technol., Pasadena, Calif.) and Mohsen, A.M. (Bell Labs., Murray Hill, N.J.)
FINAL STAGE OF THE CHARGE-TRANSFER PROCESS IN CHARGE-COUPLED DEVICES.
IEEE Trans. on Electron Devices ED-21, no. 4, 266-72, Apr. 1974.
Grant no. N00014-67-0094-0032. Grant no. 00173-3-006252

The final stages of transfer of charge from under a storage gate is formulated analytically including both fringing-field induced drift and diffusion. Analytic solutions to these equations for spatially varying fields is developed.

10631

Hu, K.C., Wolfe, G., Jr. and McDowell, W.A. (Hughes Aircraft Co., Aerospace Group, Culver City, Calif.)
MULTILAYER INTERCONNECTIONS TECHNOLOGY INVESTIGATION. Rept. no. AFAL-TR-73-438, Final Rept., June 1972-Nov. 1973, 100 pp., Feb. 1974. F33615-72-C-1926

This program shows that the all aluminum metalization system using the mushroom and EBM (Expendable Bimetal Mask) techniques is a viable method of applying multilayer metalization to full wafer bipolar and MOS LSI. This report also shows that this multilayer system is compatible with thin film resistor, refractory metal and beam lead technologies.

10632

Kjar, R.A. (Rockwell Internatl. Corp., Electronics Res. Div., Anaheim, Calif.)
INVESTIGATION OF CHROMIUM-DOPED OXIDES.
Rept. no. C71-1063/501, Final Rept., Nov. 1, 1971-Nov. 1, 1973, 189 pp., Nov. 1973. N00014-72-C-0017

This report describes results obtained during the investigation of the mechanisms by which chromium-doping of a silicon-dioxide gate insulator may improve the radiation resistance of MOS devices. It details the fabrication and testing of a CMOS/SOS 4-bit adder that employed chrome-doped and aluminum ion-implanted gate oxides to provide improved radiation hardness. The study described here was undertaken to gain an understanding of the effects of chrome-doping and other process variations on the radiation hardness of MOS devices.

10633

Hanlon, E.
WHEN IS AN IC INDUSTRIALLY RELIABLE?
Circuits Mfg. 17, no. 11, 34-5, Nov. 1973

The article deals with integrated circuit failure rates and reliability criteria. Specifically considered are burn-in and screening procedures and economic tradeoffs.

10634

BEAM LEADS? FLIP CHIP? CHIP? WIRE? AN INDUSTRY SURVEY. Circuits Mfg. 13, no. 12, 18-22, Dec. 1973

Developed primarily as alternatives to the chip and wire technique-and claiming to avoid the problems of point-to-point wire bonds-beam leads, flip chips, leadless inverted devices (lids) and other packaging arrangements still seem to reside in a Bali Hai remote from the assembly lines of today's hybrid shops.

10635

BEAM LEADS: SETTING UP AN ASSEMBLY FACILITY. Circuits Mfg. 13, No. 12, 3 pp., Dec. 1973

Of all the problems that beset hybrid-circuit manufacturers, none troubles them more persistently than the difficulty of getting reliable, repeatable gold or aluminum wire bonds to chip and substrate. As the report shows, 41% of the hybrid circuit-makers responding to an ISHM questionnaire cited die and wire bonding ar a problem.

10636

THE DO'S AND DON'TS OF ULTRASONIC BONDING. Circuits Mfg. 13, no. 12, 5 pp., Dec. 1973

Consistent and reliable ultrasonic bonding requires optimizing power, clamping force (pressure), time, mating of tool geometry with wire and bonding pad and package condition. As power and clamping force increase and the physical characteristics of tool and package improve, weldment peel strength increases through bond growth.

10637

HYBRID MICROELECTRONICS: WHERE TO NEXT? Circuits Mfg. 17, no. 11, 20-3, Nov. 1973

This report summarizes current trends in the hybrid microelectronic circuits market. It includes a survey of applications in consumer electronics, art and computer technology and industry. Changes in hybrid design philosophy and economic factors are also considered.

10638

Gray, P.R. (U. of Calif., Dept. of Elec. Eng. and Computer Sci., Berkeley, Calif.) Hamiliton, D.J. (U. of Ariz., Dept. of Elec. Eng., Tuscon, Ariz.) and Lieux, J.D. (Fairchild Camera and Instr. Corp., Palo Alto, Calif.)
ANALYSIS AND DESIGN OF TEMPERATURE STABILIZED SUBSTRATE INTEGRATED CIRCUITS. IEEE J. of Solid State Circuits SC-9, no. 2, 61-9, Apr. 1974. F44620-71-C-0087. GK-31906

A generalized temperature-stabilized substrate integrated circuit system containing heat sources and temperature sensors which are distributed in an arbitrary way in two-dimensions over the surface of the chip is analyzed. A computer-aided technique for optimum placement of these components at the layout stage so as to achieve zero nominal temperature coefficient in the performance parameter of interest is described.

10640

Stokoe, T.Y. and Parrott, J.E. (U. of Wales, Inst. of Sci. and Tech., Cardiff, Wales)
INCLUSION OF CARRIER TEMPERATURE EFFECTS IN A THERMIONIC-DIFFUSION THEORY OF THE SCHOTTKY BARRIER. Solid-State Electronics 17, no. 5, 477-84, May 1974

Recent evidence indicates that thermionic emission is a more important process than conduction-diffusion for current limitation in many Schottky barriers. By choosing suitable momentum and energy conservation equations an expression for the thermionic-diffusion current is obtained where it is assumed that the carrier temperature in the space charge region of the metal semiconductor interface does not differ substantially from the equillibrium temperature.

10641

Melen, R.D. and Meindl, J.D. (Stanford Integrated Circuits Lab., Stanford, Calif.)
A TRANSPARENT ELECTRODE CCD IMAGE SENSOR FOR A READING AID FOR THE BLIND. IEEE J. of Solid-State Circuits SC-9, no. 2, 41-9, Apr. 1974

Transparent polycrystalline silicon capacitor electrodes are presented as the basis of a front-side illuminated CCD image sensor. The influence of this transparent electrode structure on the spectral response of the image sensor is analyzed. Reflection of light from the polycrystalline silicon layer is found to be the most significant factor in the performance of the structure.

10642

Ryerson, C.M. (Hughes Aircraft Co., Equip. Eng. Div. and Prod. Assurance Aerospace Group, Culver City, Calif.)
RELATING FACTORY TEST FAILURE RESULTS TO FIELD RELIABILITY, REQUIRED FIELD MAINTENANCE, AND TO TOTAL LIFE CYCLE COSTS. Microelectronics and Reliability 12, no. 4, 357-84, Oct. 1973. Paper presented at the 29th Military Operations Research Symposium. AF Academy, Colorado Springs, June 27-29, 1972

The importance of this report is that it describes newly developed management tools which now make it possible to provide this improved system performance and low field maintenance. It also provides methods for evaluating specific cost trade-offs between dollars expended in achieving a known inherent reliability and total costs relating to total life cycle maintenance.

10644

Brotherton, S.D. (U. of Southampton, Dept. of Electronics, Southampton, Engl.)
A THEORETICAL ANALYSIS OF C.C.D. OPERATION WITH SQUARE CLOCK PULSES. Solid-State Electronics 17, no. 4, 341-8, Apr. 1974

The consequences of rapidly falling gate voltages are discussed and a simple mathematical model is developed to illustrate the situation. It is shown that if the falling edges of the clock pulses are too steep the operation of the C.C.D. will be degraded in that carriers may be lost by recombination and the overall transfer process will be slowed down due to the smaller electrostatic fields which are developed.

10645

Chan, C.H. and Chamberlain, S.G. (U. of Waterloo, Elec. Eng. Dept. Ontario, Can.)
NUMERICAL METHODS FOR THE CHARGE TRANSFER ANALYSIS OF CHARGE-COUPLED DEVICES. Solid-State Electronics 17, no. 5, 491-9, May 1974

Charge transfer phenomenon in charge-coupled devices is characterized by a non-linear partial differential equation of the parabolic type, usually coupled with a very undesirable nonlinear boundary condition. In this study, special treatment is made to the boundaries such that the non-linear-schemes for this problem are described and results compared.

10646

Kitson, B.R. (Matthey Printed Prod. Ltd. Burslem, Stoke-on-Trent, Engl.)
RELIABILITY COMPARISONS. Microelectronics and Reliability 11, no. 3, 287-92, July 1972

The use of the Wiebull method is an excellent way of discriminating between the reliability of two or more product populations, this method demands complete details of the sampling life tests, which the would-be user may not have. The author offers a method by which the user can approach the Wiebull accuracy if detailed results of the sampling tests are not available.

10647

Blanks, H.S. (U. of South Wales, Sch School of Elec. Eng., Kensington, Australia)
A REVIEW OF NEW METHODS AND ATTITUDES IN RELIABILITY ENGINEERING. Microelectronics and Reliability 12, no. 4, 301-19, Oct. 1973*

The emphasis on reliability physics and reliability improvement programs is discussed, as well as recent work on standard components. Recently investigated failure mechanisms and tools of analysis are reviewed. The U.K. BS9000 scheme and its status are briefly discussed.

*This paper has been previously published by the IFEE (Australia)

10648

Franklin, P. (Monolithic Memories Inc.)
PROGRAMMABLE READ ONLY MEMORY RELIABILITY REPORT II. 35 pp., Apr. 1, 1974

The purpose of this bulletin is to clarify the "Grow-Back" phenomenon. It should be emphasized that this study was isolated from other reliability studies for two reasons:

(1) The phenomena has proven under controlled experiment, as in field to be an early mortality failure and does not appear to impact the long term life (MTBF) of the device.
(2) Since it is a new failure mechanism indigenous to nichrome fuse PROM's, much interest, speculation, and misinformation has been generated in the field.

10649

CAN BURN-IN CAUSE PROBLEMS AS WELL AS SOLVE THEM? Evaluation Eng. 13, no. 2, 2 pp., Mar./Apr. 1974

At incoming inspection we never had any failures. They were all good because they had been 100% tested after they were burned-in. However, after they went over the wave soldering machine the bonds were weakened by overstress. An analysis showed the temperature cycle we were running did eliminate the infant mortality, but it also weakened enough bonds in the process so that we had just as many failures as we would have had without burn-in, only we had the failures two steps farther down the line, where it costs a lot more to fix.

10652

Thomann, D.L. and Hinnah, H.D. (CTS Knights, Inc., Sandwich, Ill.)
TEMPERATURE COMPENSATED MICROCIRCUIT CRYSTAL OSCILLATOR. Quart. Rept. no. 2, 26 pp., June 1-Sept. 1, 1972. AD 914 560
Quart Rept. no. 3, 9 pp., Sept. 1-Nov. 31, 1972. AD 914 561. DAABO5-72-C-5839

The objective of this program is to establish a production capability for a microcircuit temperature compensated oscillator (MCTCXO) suitable for use as the reference oscillator in advanced FM communications equipment. This report discusses the selection of the custom CMOS chip which will use silicon-on-sapphire technology in it's construction. Final CMOS specifications as well as specifications for the hybrid circuitry are included.

10655

Ogdin, J.L. (Software Technique, Inc.)
SURVEY OF MICROPROGRAMMABLE μP's REVEALS ULTIMATE SOFTWARE FLEXIBILITY. EDN 19, no. 14, 69-74, July 20, 1974

We will give several examples of microprogrammable μP's. The price one pays for the flexibility of microprogrammable devices require considerable off-chip support.

10656

Anon.
FOCUS ON MICROPROCESSORS. Electronic Design 22, no. 18, 17 pp., Sept. 1, 1974

A large-scale integration processor does perform many of the functions of the central processing unit in conventional computers. But to use the circuit, many more ICs may be needed to interface with peripheral devices, data-communication lines and even its own memory.

10657

Wei, L.S. and Simmons, J.G. (U. of Toronto, Elec. Eng. Dept., Toronto, Can.)
TRAPPING, EMMISSION AND GENERATION IN MNOS MEMORY DEVICES. Solid-State Electronics 17, no. 6, 591-8, June 1974.

This study is concerned with trapping phenomena occuring at the semiconductor-oxide interface and in the nitride layer of variable-threshold metal-nitride-oxide-semiconductor (MNOS) memory devices. The technique consists of biasing the device in such a manner as to change or discharge either the interface traps or the nitride traps, or both sets of traps simultaneously.

10658

Waterfield, B.C. (Anderman and Ryder Ltd., Great Britain)
DEVELOPMENT OF CERAMIC PACKAGES WITH TRANSPARENT LIDS. Rept. no. DRIC-BR-40235, Ann. Res. Rept. AD 918 866. K/LT31b/1143

The purpose of this contract was to develop methods of offering transparent lids to the Integral Substrate Packages as a replacement for ceramic. The reasons for this requirement were:

A need to inspect circuits after enclosure and final test
For possible use with light sensitive/emitting devices.

10659

Antler, M. (Bell Telephone Labs. Inc., Columbus, Ohio)
WEAR OF GOLD PLATE: EFFECT OF SURFACE FILMS AND POLYMER CODEPOSITS. IEEE Trans. on Parts, Hybrids and Packaging PHP-10, no. 1, 11-7, Mar. 1974

Gold platings obtained from some solutions contain codeposited organic compounds. It is of interest to know whether such materials affect the friction and wear of electro deposits which are used on the contacts of slip rings, connectors, and other devices. Studies were made of the polymer contents of golds and with the scanning electron microscope, their location in the deposits, and the results correlated with sliding properties.

10660

Forte, N.V. (Bendix Corp., Kansas City, Mo.)
THIN-FILM MICROCIRCUIT SUBSTRATE METALLIZATION. Rept. no. BDX-613-760, Rept. no. PDG 6984719, Final Rept., 89 pp., Sept. 1973. AT(29-1)-613USAEC

A thin-film technique for applying gold over tantalum-nitride-coated alumina substrates was developed to permit thermocompression bonding of fine wires, beam-lead devices, and frames. Satisfactory gold adhesion was obtained by depositing a thin layer of chromium over the tantalum nitride before depositing the gold. The system provides guidelines for fabricating hybrid microcircuits that contain beam-lead devices.

10661

Herczog, A. (Corning Glass Works, Corning, N.Y.)
APPLICATION OF GLASS-CERAMICS FOR ELECTRONIC COMPONENTS AND CIRCUITS. IEEE Trans. on Parts, Hybrids, and Packaging PHP-9, no. 4, 247-56, Dec. 1973

Ceramic materials of interest for electronic components, such as ferroelectrics, ferrites, and transition metal oxides have no natural homogeneous glasses. This is the most important requirement for controlling crystallization and phase dispersion, as required for various applications. Materials and methods used for making disk and multilayer capacitors are discussed. Their properties are described for normal and high voltage applications, and hybrid circuits.

10662

Holm-Kennedy, J.W. (U. of Calif. S School of Eng. and Appl. Sci., Los Angeles, Calif.)
LONG TERM MEMORY IN JUNCTION DEVICES USING MULTIVALENT TRAPPING IMPURITIES IN SILICON. Rept. no. ECOM-0306-73-1, Rept. no. UCLA-ENG-7420, Semiann. Rept. no. 1, July 1, 1973-Feb. 28, 1974, 39 pp., June, 1974. DAABO7-73-C-0306

A new electronic instrument has been invented (designed, fabricated, and tested). It permits the automatic x-y recorder plotting of the high voltage pulsed I-V characteristics of test samples. Three new classes of device behavior have been observed: 1) Irreversible switching in n-Si epitaxial structures doped with Cu, 2) Reversible switching of a character different than normally observed in F.I.T. devices, and 3) Large magnitude oscillations (KHz) in Schottky diodes under large forward bias (35 volts.)

10663

Kaiser, H.W., Gehweiler, W.F., Stotz, W.J. et al. (RCA, Advanced Technol. Labs., Signal Processing Lab., Camden, N.J.)
RECENT DEVELOPMENTS IN CMOS/SOS. pp. 60-4. A73-23791

Much has been written over the past several years concerning the complementary metal oxide semiconductor silicon-on-sapphire (CMOS/SOS) technology and its potential to satisfy an ever growing requirement for a high-speed low-power LSI technology. Significant progress has been made during the past year to bring the technology from its laboratory development stage to a viable pilot-production-line process. Aluminum-gate CMOS/SOS has been in pilot production since February 1972. Higher speed operation in the 100- to 200-Mb/s range will be obtained ultimately by the marriage of silicon-gate-technology and the deep-depletion CMOS/SOS process.

10664

Licari, J.J. and Perkins, K.L. (Rockwell Internatl. Corp., Autonetics Div., Huntsville, Ala.) and Caruso, S.V. (NASA Marshall SFC, Astrionics Lab., Huntsville, Ala.)
EVALUATION OF ELECTRICALLY INSULATIVE ADHESIVES FOR USE IN HYBRID MICROCIRCUIT FABRICATION. NAS8-26384. IEEE Trans. on Parts, Hybrids, and Packaging PHP-9, no. 4, 199-207, Dec. 1973

Although it is generally accepted that the use of adhesives in the fabrication of hybrid microcircuits offers advantages over other bonding methods, there currently does not exist a set of guidelines for the selection of adhesives which will ensure sufficient compatibility with micrccircuit components and metallization systems to meet the long use-life, high reliability requirements of military and space applications. The initial results of a study directed to the task of selecting suitable evaluation tests which can form the basis for such guidelines for electrically insulative adhesives are presented.

10665

Hahn, G.J. and Nelson, W. (GE Corporate Res. and Dev. Center, Schenectady, N.Y.)
COMPARISON OF METHODS FOR ANALYZING CENSORED LIFE DATA TO ESTIMATE RELATIONSHIPS BETWEEN STRESS AND PRODUCT LIFE. IEEE Trans. on Reliability R-23, no. 1, 2-11, Apr. 1974

A brief review of graphical, maximum likelihood, and linear estimation methods for analyzing censored life data to estimate relationships between stress and product life, is discussed. Each method is illustrated by an example dealing with accelerated life test data on motor insulation. The advantages and disadvantages of the methods are compared to guide the choice of a method for a given application.

10667

Bowkley, I.G. (Elec. Res. Assoc., Survey, Gt. Britain)
THE ASSESSMENT OF THICK FILM RESISTOR RELIABILITY. Rept. no. ERA-2461/2, Ann. Rept. C.V.D. Res. Proj. RP34/6, 7 pp., Nov. 1973. AD 918 196

In addition to the assessment of ERA resistors, three commercial resistor paste systems have been chosen for testing relationship between voltage pulse testing and load life performance. The systems are JM RF, Du Pont 1300 and Plessey EMD E series. The resistors will be subjected to voltage pulsing, step stress testing and load testing and the results will be correlated in an attempt to establish a relationship between the various test conditions.

10669

Segreto, D. (Datatron, Inc., Microelectronic Testing Labs., Santa Ana, Calif.)
YOU'RE NOT TESTING--RIGHT! PLAGUED BY IC FAILURES. Evaluation Eng. 13, no. 1, 3 pp., Jan/Feb. 1974

Datatron's Microelectronic Testing Laboratory (MTL) is leaning toward the opinion that high-temperature soak will prove just as effective as operating burn-in for industrial Hi-Rel programs. The standard burn-in temperature is 125°C (=150 CT) for NASA and military components, while 100°C (=125-130 CT) is common on plastic or ceramic devices intended for industrial use.

10671

Schamis, R.S. (Solid-State Sci. Montgomeryville Ind. Center, Montgomeryville, Penn.)
REDUCE SYSTEM NOISE WITH CMOS CIRCUITS THAT PROVIDE COMPENSATING WAVESHAPING AND LEVEL DETECTION. THE CIRCUITS ARE SIMPLE AND USE LOW-COST ICs. Electronic Design 25, 1112-15, Dec. 6, 1973

For low-power applications-CMOS is finding increasing applications in systems where a significant amount of noise acoompanies the required signal. The high power gain of CMOS is being used by designers, in various circuit configurations, to reduce substantially the effects of system noise. Circuits provide compensatory waveshaping and level detection, which can be built with readily available low cost CMOS ICs.

10672

D'Heurle, F.M. (IBM, Thomas J. Watson Res. Center, Yorktown Heights, N.Y.)
ELECTROMIGRATION AND FAILURE IN ELECTRONICS: AN INTRODUCTION. Proceedings of the IEEE 59, no. 10, 1409-18, May 1971

Fundamental aspects of electromigration phenomena as they have been studied in "bulk" metallic conductors and thin films are reviewed. In an electric field atoms are subjected to a force due to the field, and to a force which results from the motion of electrical carriers, electrons, or holes. In bulk samples, and at high temperatures, these forces cause the displacement of atoms by a lattice mechanism resulting in the diffusion of atoms in a concentration gradient. In thin films electromigration occurs at lower temperatures by a grain boundary diffusion mechanism. The effects of film purity, orientation, grain size, glass overcoat, and solute additions on lifetime are reviewed. Practical guidelines for the design of thin-film interconnections, and for the interpretation of accelerated test data re given.

10673

Preston, S.B. (GEC Power Eng. Ltd., Whetstone, Leicester, Gt. Britain)
THERMAL PERFORMANCE OF BEAM-LEAD INTEGRATED CIRCUITS. pp. 308-14. A72-39498. International Electronic Packaging and Production Conference. Brighten, Sussex, Engl., Oct. 19-21, 1971

Theoretical analysis has the ability to predict the performance of new designs at the drawing board stage, to highlight bottlenecks, areas for improvement, assessment of design changes without the need for costly experiments with prototypes. The work described is concerned with an existing concept--the beam-lead integrated circuit. Detailed experimental results are now available for beam-leaded chips that may be compared with the theoretical predictions. Designers must be able to predict accurately their temperatures under operating conditions. This paper is concerned with analysis at device level; a companion paper deals with the determination of these thermal resistances at system and subsystem level.

10674

Greenhouse, H.M. and McGill, R.L. (Bendix Corp., Communs. Div., Towson, Md.)
DESIGN OF TEMPERATURE-CONTROLLED SUBSTRATES FOR HYBRID MICROCIRCUITS. IEEE Trans. on Parts, Hybrids and Packaging, PHP-10, no. 2, 137-45, June 1974. Bendix Tech. Journal, pp. 18-27, Winter 1972/73

This paper deals in depth with the criteria that govern the design of temperature-controlled substrates for hybrid microcircuits. Pertinent thermal parameters for the more important microcircuit-fabrication materials are presented in tabular form, along with several useful unit-conversion factors. Control-circuit design is discussed, and consideration is given to power dissipation by circuitry off as well as on the substrate. The effects of changes in ambient temperature on temperature controlled microcircuit performance are analyzed.

10675

Ihochi, T. (Hitachi Takasaki Works, Takasaki, Japan)
SCREENED MULTILAYER CERAMICS FOR THICK FILM HYBRIDS. pp. 204-11 Proceedings 1973, 23rd Electronic Components Conference. Sponsored by the IEEE Parts Material and Packaging Group (GPMP) and the Electronic Industries Association (EIA). Statler Hilton, Washington, D.C., 363 pp., May 14-16, 1973. IEEE Trans. on Parts, Hybrids and Packaging PHP-10, no. 2, 115-9, June 1974

An approach to fabricating multilayer hybrids is described. The newly developed process, designated as the screened multilayer ceramic (SMC) hybrid, has been accomplished by improving green ceramic technology of an alumina-refractory metal system to a state of development similar to thick film screening technology and by developing a unique process that protects against oxidation of refractory metal at high temperature air firing.

10676

Komatinsky, R.R. (Bendix Corp., Elec. Components Div., Sidney, N.Y.)
A HIGH FREQUENCY MICROCIRCUIT PACKAGING AND INTERCONNECTION SYSTEM. pp. 5A-6-1-5A-6-8. 1973 International Microelectronic Symposium. Sponsored by the International Society for Hybrid Microelectronics. Sheraton-Palace Hotel, San Francisco, Calif., Oct. 22-24, 1973. IEEE Trans. on Parts, Hybrids and Packaging PHP-10, no. 2, 110-5, June 2, 1974

This paper describes the development, characteristics, and application of a controlled impedance hermetic package (CIP) for microcircuit applications in microwave and fast-risetime pulse/digital domains. A description is given of this planar package concept which is interfaceable with a strip transmission line motherboard. Pertinent electrical characteristics of the CIP are presented.

10677

GOMAC
1974 GOVERNMENT MICROCIRCUIT APPLICATIONS CONFERENCE DIGEST OF TECHNICAL PAPERS. VOL. V.
Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Sessions:

Nonvolatile Memories
Government Exploitation of LSI Technology
Radiation Effects - Characterization
Surface Acoustic Filter Techniques
Phased Array Technology
Applications of LSI
Radiation Effects - MOS
Packaging Technology
Microwave Components and Techniques
Digital Logic/Memory ICs
Radiation Effects - Vulnerability and Hardening
Approaches to Packaging
Microwave Generation and Amplification
New Techniques for High Density Devices
Device Reliability
Hybrid Microelectronics
Microwave Receiver Technology
Signal Processing
Reliability Tests
Integrated Device Applications

10678

Anderson, W.E., Irons, H.R., Krall, A.D. et al. (U.S. Navy, Nav. Ordnance Lab., Silver Spring, Md.)
CROSSTIES ON MAGNETIC THIN-FILM DOMAIN WALLS FOR SERIAL ACCESS MEMORY.
pp. 14-5. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The crosstie memory described in this paper is expecte? to exhibit data rates up to 20 Mbits/sec at densities of 100,000 bits/in^2. Theoretically, these values can be increased by factors of 10 and 1000. These characteristics place the crosstie memory performance in an area between the highly developed random access and bulk storage methods widely available now. It is non-volatile and non-mechanical in operation, resulting in a rugged unit requiring no standby power. Fabrication is by multilayer thin film techniques resulting in relatively low-cost structures.

10679

Bushunow, E.J. and Cole, D.M. (GE, Aircraft Equip. Div., Utica, N.Y.)
PROBLEMS ASSOCIATED WITH PROGRAMMABLE READ-ONLY MEMORIES. pp. 16-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The experience of the General Electric Aerospace Electronic Systems Department (GE/AESD) with Programmable Read Only Memories (PROMs) began in the early part of 1971 when a 256-bit PROM was designed into a countermeasures equipment, making GE/AESD one of the first users of PROMs in high-reliability equipment. Since that time, GE/AESD experience has expanded to 1024-bit and 2048-bit PROM varieties, including devices of the "nichrome fusible link" and "avalanche induced migration" types packaged in dual-in-line (DIP and in flat packages.

10681

Betz, C.A. (Sperry Rand Corp., Univac Defense Systems Div., St. Paul, Minn.)
MNOS BORAM MEMORY DEVELOPMENT. pp. 20-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A 2048 bit MNOS array is optimized for Block Organized Random Access Memory (BORAM) applications and for development of a 32K word BORAM module to be used in the Navy All Applications Digital Computer System. The MNOS technology was selected for this application because it provides the capability of achieving very high densities and also provides the ability to achieve very low system power dissipation.

10682

Losleben, P. (Natl. Security Agency, Fort George G. Meade, Md.)
ALTERNATIVES TO SOLE SOURCE LSI. pp. 24-5. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Custom LSI components. now beginning to appear in government electronics equipments have brought into focus the problems of sole source parts acquisition. Design costs for custom LSI are relatively high, and to use the same procedure to develop multiple sources would be to seriously constrain custom LSI applications to large volume purchases. A number of alternatives are listed.

10684

Tinklepaugh, N.L. (U.S. Navy, Nav. Electronics Lab. Center, Advanced Digital Systems Architectural Div., San Diego, Calif.)
QED: QUICK AND EASY DESIGN OF SYSTEMS. pp. 28-29. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

QED is a program to define and test high usage functional modules as prototypes of LSI components. Experience with the prototype modules will verify broad utility of the family and lead to orderly exploitation of LSI technology. QED module designs are limited to less than 1000 equivalent gates, with the exception of memory and multiplier arrays, so that they can be fabricated with today's integrated circuit technologies.

10685

Beum, C.O., Jr. and Levin, E. (System Dev. Corp., Santa Monica, Calif.)
IMPACT OF LSI TECHNOLOGY ON FUTURE AVIONICS SYSTEMS. pp. 30-1. DACH-0200-4. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A recently completed study (Standardization of Avionics Information Systems) was performed by the System Development Corporation (SDC) for the Institute for Defense Analysis (IDA) in support of the DoD Electronics-X Project. The overall objectives of that project were to select and recommend techniques and possible institutional alternatives aimed at reducing the life cycle cost and increasing the reliability of defense electronic equipment to be acquired in the 1980-1990 time period. The SDC study concentrated on avionics processing systems.

10686

Witmer, W.H. (Mosfet * Micro * Labs., Inc., Quakertown, Penn.)
CUSTOM MOS/LSI FROM INDEPENDENT VENDORS. pp. 32-3. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The microelectronic companies are now achieving their long awaited success in the commercial sales of MOS/LSI products. High demand for calculator circuits and an assured new market for microprocessor chips are taxing product capacity. For a number of reasons the big microelectronic companies are reluctant to take on custom MOS/LSI. First and foremost is the problem of saddling the production line with a low-volume order. Even when the exact same process requirements are assured the traffic control necessary for a small volume order can hazard the smooth flow of production. This paper describes an alternative to procurement of MOS/LSI from the huge microelectronic company.

10687

Gregory, B.L. and Gwyn, C.W. (Sandia Labs., Albuquerque, New Mex.)
DESIGN REQUIREMENTS FOR RADIATION HARDENED SEMICONDUCTOR DEVICES. pp. 36-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

High energy radiation, incident on a semiconductor device, deposits energy in the semiconductor via the production of atomic displacements and electronic ionization. The relative importance of these two mechanisms in a semiconductor structure depends both on the type of radiation and the nature of the device. The radiation produced changes in a device, for any environment, depend on its sensitivity to both ionization damage and bulk displacement damage.

10688

Raymond, J.P. (Northrop Res. and Technol. Center, Hawthorne, Calif.)
CONSIDERATIONS IN THE EVALUATION OF MSI/LSI RADIATION VULNERABILITY. pp. 40-1. DASA 01-70-C-0093. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The development of a hardened electronic system requires evaluation of component radiation vulnerability. The purpose of this paper is to present data on the measured vulnerability of bipolar and MOS MSI/LSI arrays and to illustrate some aspects of the vulnerability characterization unique to these complex semiconductor devices.

10689

Taylor, S.A. (Martin-Marietta Aerospace, Orlando, Fla.)
FAILURE MECHANISMS AND EFFECTS OF IRRADIATION ON PLASTIC INTEGRATED CIRCUITS. pp. 42-3. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 298 pp., June 25-27, 1974

This paper summarizes the experiment and results of a program to evaluate a failure mechanism in irradiated plastic integrated circuits. The overall test program was devised to evaluate plastic integrated circuits in various types of radiation environments. Hermetic controls were employed throughout the test program so that valid comparisons of hermetic and plastic packaging could be made. To intelligently differentiate the findings representative failures at each step of the test program were failure analyzed. The failure analyses were performed to the requisite depth in order to define the physical mechanism which contributed to the specific mode of failure.

10690

Jones, G. (ARMDA, Huntsville, Ala.)
Palmer, F. (RCA, Moorestown, N.J.)
and Sudbury, R. (MIT, Lincoln Lab., Lexington, Mass.)
MICROWAVE INTEGRATED CIRCUIT TRANSCEIVERS IN L-BAND PHASED-ARRAY APPLICATION. pp. 64-5. F30602-73-C-0179. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The concept of utilizing a microwave integrated circuit transceiver for each radiating element of a phased array radar has formed the basis for an all solid state phased array radar design. The face of the 72 element L-Band array that has been constructed and tested is a representative segment of a large array. The transceivers, associated filtering, beam-steering drivers/combiners are located behind the radiating element. The radiating element design has been described elsewhere.

10691

Feldmanis, C.J. (U.S. Air Force, AFFDL/FEE, Wright-Patterson AFB, Ohio)
and Haws, J.L. (Tex. Instr. Inc., Dallas, Tex.)
THERMAL CONTROL OF AIRBORNE MICROWAVE INTEGRATED CIRCUIT PHASED-ARRAY SYSTEMS. pp. 66-7. 1974 Government Microcircuit Applications Conference Dugest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

By definition an airborne microwave integrated circuit (MIC) phased array system is a grouping of transmit-receive microwave modules which generate, receive and/or control microwave energy. The transmitter and receiver circuits within the module consist of MIC amplifiers, frequency multipliers, low noise amplifiers, voltage regulators, and phasors. Unfortunately, the present state-of-the-art yields microwave devices with inherently low efficiencies.. Thus, each device within the phased array module dissipates power in the form of heat. Removal of this dissipated heat in an efficient and controlled manner and the associated problems are subjects of this paper.

10692

Kaiser, H.W. and Gehweiler, W.F. (RCA, Advanced Technol. Labs., Camden, N.J.)
CMOS/SOS AIRTHEMETIC CIRCUITS. pp. 74-5. F33615-72-C-1291. N00014-73-C-0090. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A family of CMOS/SOS arithmetic circuits was designed that permit signal processors to be built with throughput rates of 10 MHz. The 8-bit multiplier and adder arrays form the basic elements of an FFT complex multiplier. CMOS/SOS allows these circuits to be integrated on single, reasonably-sized chips exhibiting very low power dissipation. Pipelining techniques allow rates of 40 MHz to be achieved. A hybrid 4 by 5 bit pipeline multiplier was developed for use in greater-than-10-MHz throughput rate processors.

10693

Finkel, M. (Hughes Aircraft Co., Culver City, Calif.) and Tuttle, D.B. (U.S. Navy, Nav. Air Systems Command, Washington, D.C.)
THREE TYPES OF LSI DIGITAL PROCESSORS. pp. 82-3. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Hughes Aircraft Co., under contract to Naval Air Systems Command, is currently developing three digital processors which can be combined to form a Digital Computing Subsystem (DCS) for a strapdown inertial navigation and guidance system. A digital differential analyser approach is used for the Coordinate Converter; a whole word distributed arithmetic special purpose processor implements the Digital Autopilot and a general purpose sequential miniprocessor is used to mechanize the Guidance Data Processor.

10694

Buchanan, B., Sheedy, W., Neaman, D.A. et al. (U.S. Air Force, Air Force Cambridge Res. Lab., Bedford, Mass.)
RADIATION HARDENED CMOS. pp. 86-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The status and methods of qualifying radiation hardened CMOS on bulk and on SOS is presented and the remaining hardening problems are put in perspective. In addition to new radiation effects data on numerous hardened gate insulators, new radiation effects and problem areas relating to gate electrodes and substrate dielectrics are presented.

10695

Palkuti, L.J., King, E.E., Nelson, G.P. et al. (U.S. Navy, Nav. Res. Lab., Washington, D.C.) and Kalinowski, J.J (Braddock, Dunn and McDonald, Inc., Vienna, Va.)
ANALYSIS OF THE RADIATION RESPONSE OF CMOS CIRCUITS. pp. 88-9. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Complex circuits can be radiation hardened using standard commercial techniques provided appropriated design rules are incorporated in the circuit design, such as the elimination of the reverse-bias condition in SOS devices. The need for extensive dc and transient circuit characterization is illustrated and the utility of computer-aided simulation is demonstrated.

10696

Killiany, J., Saks, N., Baker, W.D. et al. (U.S. Navy, Nav. Res. Lab., Washington, D.C.)
EFFECTS OF GAMMA RADIATION ON CHARGE-COUPLED DEVICES. pp. 90-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of the Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp.; June 25-27, 1974

In this paper, we discuss the effects of gamma radiation on the operation of a surface-channel charge-coupled device (CCD) and a buried-channel CCD. The devices were irradiated using a Cobalt-60 gamma source. Normal bias and clock voltages were applied during irradiation. No effort was made to optimize the radiation hardness of these devices.

10697

Phillips, D.H. and Kjar, R.A. (Rockwell Internatl. Corp., Anaheim, Calif.)
DESIGN THEORY FOR OPTIMUM RADIATION-HARDENED CMOS/SOS INTEGRATED INVERTER CIRCUIT. pp. 92-3. F29601-73-C- 0055. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Silicon-on-sapphire construction greatly reduces radation-induced junction photocurrents in MOS circuits. The SOS structure, however, is not devoid of transient radiation induced effects since a "resistive" current path through the insulating sapphire becomes partially conductive when radiation generates carriers in the sapphire. Current flowing through this photoresistive path accounts for most of the SOS transistor drain photocurrent observed experimentally and explains the nearly linear dependency of that current on drain voltage.

10698

Neamen, D.A., Shedd, W.M. and Buchanan, B. (U.S. Air Force, Air Force Systems Command, Air Force Cambridge Res. Labs., Bedford, Mass.)
PERMANENT IONIZING RADIATION EFFECTS IN GATE AND ISOLATION DIELECTRICS IN FETs. pp. 94-5. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Dielectric isolation techniques are becoming more prominent in MIS device and integrated circuit fabrication as a means of increasing speed, reducing device area, and reducing the transient photocurrent response. One problem that is not usually significant for dielectrically bounded bipolar structures, but may be very serious for dielectrically bounded FET's, is the effect of total ionizing radiation on the isolation dielectric and/or the interface between the isolation dielectric and semiconductor resulting in charge being induced in the active region of the device causing a permanent change in operating characteristics.

10699

Hampol, D. and Stewart, R.G. (RCA, Govt. Commun. Systems, Somerville, N.J.) and Parks, J. (U.S. Army, Harry Diamond Labs., AMSDO EM, Washington, D.C.)
EMP HARDENED CMOS CIRCUITS. pp. 96-7. DAAG 39-73-C-0254. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

New protection networks on both inputs and outputs of CMOS gates have been integrated and tested. The tolerance of these circuits to injected pulses from a 50-ohm source was increased from a minimum of 65 volts (for standard gates) to 1,221 volts. Corresponding peak-power immunity was increased from 15 watts to 500 watts. The improvements were the result of larger geometry and lower-impedance protection diodes with conductors of wider metallization.

10701

Lindberg, F.A. (Westinghouse Aerospace and Electronic Systems Div., Baltimore, Md.)
RADIATION HARDENED HYBRID PACKAGES. pp. 102-3. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A packaging technique for interconnecting a number of standard integrated circuit chips with aluminum metalization was conceived and evaluated. Round aluminum wire was avoided. The chips were mounted on 3/4 inch square alumina substrates and were electrically connected with beam leads produced by thin film techniques. The official results of the radiation testing are not known as of this writing.

10702

Zatz, S., Malzahn, F.A., Samuelson, H.L. et al. (Martin Marietta Aerospace, Orlando, Fla.)
CHANGES TO INTEGRATED CIRCUIT PACKAGES REDUCE CONTAMINATION AND PROVIDE MAJOR RELIABILITY IMPROVEMENT IN DIELECTRIC ISOLATED DEVICES. pp. 104-5. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The factors governing reliability of integrated ciruits should be investigated independently. This paper explains the controlled experimentation following a technical hypothesis that reliability is directly dependent on the level of contamination within packages. Radiation hardened integrated circuits commonly use nickle-chrome thin film resistors in order to minimize the unwanted photocurrent generated by diffused resistors during gamma ray exposure. Electrolytic corrocion has been determined to be the cause of a major reliability reduction in these integrated circuits. After removing the source of electrolytic contamination, an accelerated life test was successfully conducted.

10703

Leven, S.S. and Feinstein, J.F. (Westinghouse Defense Defense and Electronic Systems Center, Baltimore, Md.)
DETERMINATION OF PRACTICAL SCREENING PROCEDURES FOR SOLDER LEACHING OF THICK-FILM GOLD AND GOLD ALLOY CONDUCTORS. pp. 106-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper discusses an experiment to determine screening procedures to preclude adhesion degradation in gold alloy/solder systems in thick film hybrid microcircuits. Leaching, which occurs after the solder has solidified, is a primary cause of degradation of the adhesion of the soldered thick film gold alloy conductor to the ceramic substrate. Pull tests were employed to determine initial adhesion of several solder-conductor combinations to ceramic substrates, as well as adhesion after environmental testing. Results of these pull tests are presented to show which material combinations to avoid and which environmental test to use as an in-process screening procedure.

10704

McCullough, R.E. (Tex. Instr. Inc., Dallas, Tex.)
INVESTIGATION OF MICROCIRCUIT SEAL TESTING. pp. 108-9. F30602-73-C-0150. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This investigation was conducted to determine the sensitivity ranges of Conditions A and B of Method 1014 and to determine if the ranges could be extended by changes in test parameters or preconditioning of the circuits.

10705

Jesch, R.L. (Natl. Bur. of Standards, Boulder, Colo.) and Bailey, R.A. (U.S. Air Force, Kirtland AFB, Air Force Weapons Lab., New Mex.)
CHARACTERIZATION OF A HF PROBE FOR INTEGRATED CIRCUITS MEASUREMENTS. pp. 120-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The practicality of making accurate HF measurements on individual integrated circuit transistors up to 2.0 GHz has been enhanced by the availability of a special probe assembly. In order to determine and correct for the effects of the probe assembly on the measurements, a technique was developed that determines experimentally the element values in an equivalent circuit representing the probe assembly.

10706

Cooper, R.E. (Tex. Instr. Inc.)
PRODUCT DESIGN OF AN X-BAND MIC NOISE SOURCE. pp. 122-3. F33657-68-C-1271. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Reduction in the extent and complexity of integrated circuits and the use of a novel microstrip RF circuit result in a cost-effective product improvement of an X-band noise source for the airborne APQ-122 radar receiver. The unit produces an excess noise power of 25.2 $\pm$ 1 dB from 9.1 to 9.6 GHz over the temperature range of -55°C to +85°C and is switchable by standard logic signal levels.

10707

Peltier, A.W. (Motorola Integrated Circuits Center, Mesa, Ariz.)
COMPLEMENTARY CONSTANT CURRENT LOGIC: C^3L. pp. 128-9. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards, Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Bipolar logic is undergoing a revolution. New families, such as I^2L, MTL and CHL, offer simplified processing, packing density, performance and efficiency directly competitive to MOS logic forms. C^3L offers similar advantages and better performance. It can also attain a high level of radiation resistance, equivalent to currently available hardened TTL.

10708

Cricchi, J.R., Williams, D.W., Blaha, F.C. et al. (Westinghouse Defense and Electronic Systems Center, Baltimore, Md.)
NONVOLATILE MNOS ARRAYS FOR BORAM. pp. 132-3. DAAB07-72-C-0236. DAAB07-73-C-0160. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

There are a number of mass memory applications that require portability as well as performance and reliability beyond that of conventional mass memory such as disc or drum. The purpose of this paper is to describe nonvolatile Metal Nitride Oxide Semiconductor (MNOS) memory devices designed for Block Oriented Random Access Memory (BORAM) to replace conventional mass memory in military applications.

10709

Gogolinski, J.E., Greetham, D.E. and Thun, R.E. (Raytheon Co., Bedford, Mass.)
A BEAM-LEAD 300-GATE LSI ARRAY IN HIGH-SPEED BIPOLAR TECHNOLOGY. pp. 136-7. 1974 Government Microcircuit Applications cations Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-26, 1974

The use of bipolar LSI for logic applications has, until recently, lagged behind the use of MOS. The prime reasons must be sought in the difficult constraints placed on circuit and device specifications by the demands of high-speed digital architecture in both commercial and military applications. High performance systems of this type tend to use pronounced horizontal partitioning and intricate control logic. They thus require LSI devices with low gate to pin ratios, very high speeds, good drive capability and a lack of sensitivity to varying load conditions.

10710

Mitchell, C.L. (M&S Computing Inc., Huntsville, Ala.) and Gould, J.M. (NASA, Marshall SFC, Huntsville, Ala.)
A USER-CONTROLLED AUTOMATED MASK ANALYSIS PROGRAM. pp. 138-9. NAS8-25621. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The Mask Analysis Program is a v valuable software tool for the analysis and manipulation of any data described spatially. It is particularly useful in integrated circuit design analysis since the user may employ it exactly as required. MAP is a programmable program.

10711

Ipri, A.C. and Sarace, J.C. (RCA Labs., Princeton, N.J.)
CMOS/SOS HIGH-SPEED SEMI-STATIC SHIFT REGISTERS. pp. 140-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Complementary-metal-oxide-semiconductor (CMOS) circuits fabricated on thin silicon films on sapphire (SOS) have been found to exhibit superior performance characteristics to those of either CMOS circuits processed on bulk silicon or comparable TTL circuits. It was the object of this study to design and fabricate a shift register which would be both CMOS and TTL compatible, operate at TTL speeds and have power dissipation levels comparable to bulk CMOS. In addition, the array was to have the capability of storing data indefinitely while still having the capacity of operating at speeds previously only attainable by dynamic (non-storing) registers.

10712

Donovan, R.P., Hauser, J.R. and Simons, M. (Res. Triangle Inst., Res. Triangle Park, N.C.)
RADIATION VULNERABILITY OF CONTEMPORARY SOLID-STATE DEVICES. pp. 144-5. F33615-73-C1115. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper reviews the physics of radiation-induced failure and surveys the radiation vulnerability of major contemporary solid state device types. Three different radiation threats are considered: 1. bulk displacement damage resulting from cumulative neutron exposure; 2. surface damage resulting from cumulative ionizing radiation exposure and 3. photocurrents generated by transient ionizing radiation. Device vulnerability is expressed in terms of the fluence, dose or dose rate required to degrade a selected device electrical parameter by a predetermined percentage. Each threat is considered independently.

10713

Stehlin, R.A. and Hoffman, J. (Tex. Instr. Inc., Dallas, Tex.)
NEUTRON HARDENING OF BIPOLAR TRANSISTORS USING SHARP PROFILES. pp. 146-7. F29601-73-C-0048. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The use of "sharp" emitter profiles has been shown to substantially improve neutron radiation performance. The use of arsenic as an n-type emitter impurity can result in exceptionally steep emitter impurity concentration gradients, and test transistors using four different processes were fabricated using arsenic as an emitter dopant. The purpose of this development program was to establish a viable production method of fabricating arsenic emitter transistors for inclusion in low power digital circuits that incorporate Schottky clamping and gold doping. The combination of these features would: (1) improve neutron performance, (2) increase switching speed, and (3) minimize transient radiation effects over conventional radiation hardened digital circuits.

10714

Clark, L.E. and Saltich, J.L. (Motorola Semiconductor Prod. Div., Phoenix, Ariz.)
SUBSTRATE PHOTOCURRENTS -- RESULTS AND IMPLICATIONS FOR RADIATION-HARDENED DEVICE DESIGN. pp. 148-9. F19628-71-C-0157. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Gold doping is often utilized to minimize photocurrents resulting from the long and highly variable diffusion lengths of lightly doped integrated circuit substrates. In the case of discrete devices fabricated on heavily doped substrates, it is desirable to assign values for the substrate photocurrent contribution in order to properly assess the tradeoffs involved in device design and fabrication. For example, if the substrate diffusion length is already short, then it is undesirable to gold dope to reduce photocurrents because forward gain and yield may be substantially impaired.

10715

Mullis, J.L. and Tallon, R.W. (U.S. Air Force, Kirtland AFB, Air Force Weapons Lab., New Mex.)
DETERMINATION OF OPERATIONAL AMPLIFIER RADIATION HARDNESS FROM ELECTRICAL PARAMETER MEASUREMENTS. pp. 150-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

For integrated circuits which must function in a radiation environment there are few firmly established procedures to assure that the circuits as fabricated on a production line will meet the radiation hardness design goals. This is particularly true for linear circuits such as operational amplifiers. Hardness assurance procedures must be developed and implemented into the production and qualification cycle before the user can have confidence in the radiation hardness. This paper presents the results of an experimental and analytical study to identify externally measurable electrical parameters which can be used to screen for ionizing radiation dose rate effects and neutron degradation in operational amplifiers.

10716

Messenger, G.C.
DESIGN CONSIDERATIONS FOR RADIATION HARDENED MICROCIRCUITS. pp. 152-3. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards, Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 286 pp., June 25-27, 1974

Rapid advances in microcircuit technology have made it extremely important to develop radiation hardening design techniques which are simple, effective, and compatible with production techniques. This presentation will concentrate on nuclear radiation hardening techniques including neutron fluence, total ionizing dose, and prompt ionizing dose rate. A general summary of design techniques will be presented for bipolar logic circuits and MOS/LSI; some new material will be presented for linear bipolar integrated circuits.

10717

Holzschuh, J.E. (U.S. Navy, Nav. Undersea Center, San Diego, Calif.)
PERFORMANCE OF HYBRID CIRCUIT COMPONENTS UNDER DEEP OCEAN PRESSURE. pp. 156-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The objective of the testing described in this paper was to demonstrate the feasibility of using hybrid circuitry in an unprotected, high-pressure environment. The components that were tested, the results of the tests, and the results of the failure analysis were presented. The conclusion reached by the author is that a thin-film hybrid circuitry is indeed usable in a high-pressure environment such as that found in the deep ocean. However, some precautions must be taken.

10718

Makos, W.S. (Sperry Univac, St. Paul, Minn.)
A NEW CONCEPT IN SYSTEM PACKAGING UTILIZING HYBRID TECHNOLOGY. pp. 158-9. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A Ceramic Packaging System concept has been developed in response to projected military and commercial needs for the 1975 timeframe and beyond. It utilizes all known semiconductor technologies. The advantages provided by such a system packaging concept include increased packing densities, lower power requirements, decreased size and weight, lower development cost, greater system ruggedness and reliability, quick turn-around time, and large scale integration. This approach will permit the design and fabrication of standard modules that can be used to configure new computer systems and peripherals likely to develop within the addressed timeframe.

10719

Sutherland, P.G. (Northrop Corp., Electronics Div., Palos Verdes Peninsula, Calif.)
PROCESS CONTROLS, MONITORING AND PRODUCTION SCREENING TECHNIQUES FOR RADIATION-HARDENED MSI/LSI BEAM-LEADED INTERCONNECT PACKAGING. pp. 160-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper discusses Northrop's approach to MSI/LSI packaging and the process controls, monitoring techniques and production screening developed specifically for obtaining high reliability, multilayer, beam leaded, radiation hard circuits. Life test and environmental test data are presented for the radiation hardened nickel beam lead interconnect packaging.

10720

Miley, J.E. (Microwave Assoc., Inc., Burlington, Mass.)
MICROWAVE INTEGRATED CIRCUIT PACKAGING TECHNIQUES. pp. 162-3. DAABO5-72-C-5851. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A family of impact extruded packages has been developed for MIC's including hardware. TIG welding techniques are used to obtain hermeticity and facilitate repairability. All RF hardware developed is capable of operation into Ku-Band.

10721

Polin, D. and Williamson, M. (Boeing Aerospace Co., Seattle, Wash.) HIGH DENSITY MULTIPLEX MODULE PACKAGING. pp. 166-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper describes sophisticated high density packaging techniques utilized in the design of 16 and 32 channel Multiplex Modules for the AWACS (Airborne Warning and Control System) program designed and fabricated by the Boeing Aerospace Company. The package design marries very high density multilayer thick film hybrid microcircuits to the back of an 18 shell size 66 pin round military connector through several layers of Kapton flexcircuits. The total package weighs under three ounces and occupies less than three cubic inches.

10722

Friedmann, E.B. and Livesay, W.R. (Radiant Energy Systems Inc., Newbury, Park, Calif.) ELECTRON BEAM MASK MAKING FOR INDUSTRY. pp. 184-5. F33615-71-C1387. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Electron Beam microfabrication is recognized as a technology available to solve fabrication problems for new devices. It will also improve yield and reduce costs on devices currently manufactured by optical techniques. The EBMG-1200 has been designed to meet these requirements by improved registration accuracy and resolution, reduced distortion and throughput time.

10723

Livesay, W.R. (Radiant Energy Systems, Inc., Newbury Park, Calif.) AN ELECTRON PROJECTION AND ALIGNMENT SYSTEM FOR MICROCIRCUIT PRODUCTION. pp. 186-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The technique of projecting mask patterns onto semiconductor wafers has the potential of becoming a valuable production process in the electronic industry, but for this potential to be realized it is necessary for the process to be feasible at reasonable production rates. One of the major limitations of the process is that each wafer must be individually aligned to a mask inside a vacuum chamber. Therefore, a production electron projection system is being developed with vacuum locks and a conveyor for handling wafers and masks at production throughput rates.

10724

Rodgers, T.J. and Meindl, J.D. (Stanford U., Stanford Electronics Labs., Stanford, Calif.) SHORT-CHANNEL V-GROOVE MOS LOGIC. pp. 188-9. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A new logic structure has been presented which takes advantage of v-groove technology to produce a 1μ channel length n-channel MOS transistor which is well suited for use in high-density, high-speed, 5v-supply applications. VMOS logic in its present form out-performs gold-doped TTL in speed, power-speed product, and density.

10725

Halsor, J.L. (Westinghouse Elec. Corp., Baltimore, Md.) Lin, H.C. (U. of Maryland, College Park, Md.) and Benz, H.F. (NASA, Langley Res. Center, Hampton, Va.)
SILICON GATE DOUBLE-DIFFUSED MOS INTEGRATED CIRCUIT. pp. 190-1. NAS 1-11369. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper describes a method for achieving self-alignment. In addition, a depletion mode load device with self-aligned gate is also incorporated in an integrated structure. The desired structure is achieved by using a polysilicon gate in combination with selective nitride masking.

10726

Mavity, W.C. (Rockwell Internatl., Electronics Res. Div., Rockwell Internatl. Electronics Group, Anaheim, Calif.)
BUBBLE MEMORIES AND GOVERNMENT APPLICATIONS. pp. 192-3. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, 288 pp., June 25-27, 1974

At GOMAC 72 we presented an overview of bubble memory status and trends. In the 20 months since that time the efforts sponsored by the various government agencies has expanded and the results have allowed consideration of specific designs for particular missions. In this update, recent programs will be presented, and predictions on system usage and availability will be made.

10727

Fagan, J.L., Lampe, D.R., White, M.H. et al. (Westinghouse Defense and Space Center, Systems Dev. Div., Advanced Technol. Labs., Baltimore, Md.)
NONVOLATIVE CHARGE ADDRESSED MEMORIES pp. 194-5. DAABO7-73-0259. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

A unique, nonvolatile, charge-addressed memory (NOVCAM) cell has been designed and **evaluated** for high capacity, low energy consumption, and high array bid density. The memory cell is addressed sequentially by a CCD shift register and the data is stored, in a MNOS structure located adjacent to the CCD shift register.

10728

Thomas, D.R. and Presson, R.D. (IBM, Essex Junction, Vt.)
AN ELECTRICAL PHOTOLITHOGRAPHIC ALIGNMENT MONITOR. pp. 196-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The fabrication of integrated circuits requires the accurate alignment of several photolithographic masks to previously defined layers. In the past, the control of this alignment has relied upon visual inspection, which is slow, expensive, and usually results in statistically marginal sample sizes. A method is described to electrically monitor the alignment.

10729

Wagner, N.K., Hart, A.R. and McQuitty, D.W. (U.S. Navy, Nav. Electronics Lab. Center, San Diego, Calif.)
AUGER ELECTRON SPECTROSCOPY APPLIED TO RELIABILITY PROBLEMS IN MICROELECTRONIC PROCESS CONTROL. pp. 200-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Higher levels of complexity and sophistication in integrated circuit technology coupled with stringent reliability requirements for military hardware have fostered increased applications of scientific techniques for semiconductor diagnosis. Prominent among these semiconductor diagnostic techniques is Auger Electron Spectroscopy (AES). AES is currently used at NELC, San Diego, for semiconductor process monitoring and analysis. This paper will illustrate the importance of AES analysis for effective process control of microelectronic devices by presenting new information from recent applications. By way of introduction, the first principles of AES will be discussed followed by several examples of useful applications.

10730

Holland, C.E., Jr. (U.S. Navy, Nav. Electronics Lab. Center, San Diego, Calif.) and Heckman, J.J. and Miller, T.M., Jr. (Georgia Inst. of Technol., Eng. Expt. Sta., Atlanta, Ga.)
MANUFACTURING SCIENCE FOR BUILT-IN RELIABILITY IN LSI DEVICES. pp. 202-3. R137001. N00039-73-C-0261. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Production implementation of emerging beam technologies and their integration into an advanced IC manufacturing science could upgrade the reliability of standard IC products to the level required for use in military electronic systems. Custom LSI with high "built-in" reliability would be available to the DoD at cost levels approaching those of standard mainstream devices. The submicrometer geometries attainable with beam processing could also increase chip complexity by an order of magnitude and decrease speed-power products by the same factor.

10731

Sekhon, K.S. (Hughes Aircraft Co., Fullerton, Calif.)
THERMAL CONSIDERATIONS TO IMPROVE THE RELIABILITY OF MICROCIRCUIT PACKAGES. pp. 204-5. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The most important nonelectrical parameter governing the reliability of a microelectronic component in a package is its operating junction temperature. This study was undertaken to investigate the variables which control the thermal resistance values from junction to case and from case to ambient air by performing thermal resistance measurements. Discussion of results along with thermal design considerations are presented.

10732

Caruso, S.V. (NASA, George C. Marshall SFC, Hunstville, Ala.)
THE DEVELOPMENT AND EVALUATION OF ADHESIVES FOR USE IN HYBRID MICROELECTRONIC PACKAGING. pp. 206-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Hybrid microcircuit technology is currently a dynamic and rapidly expanding field. Indeed, many processing techniques, materials and equipment are becoming generally accepted as established standards. However, one phase of this technology is somewhat varied and controversial, that is, methods and materials for the attachment of discrete chips to ceramic substrates. Today's manufacturers are faced with the choice between using metallic systems such as solder, brazing metals and eutectics or organic materials.

10733

Tapp., C.M. (Sandia Labs., Albuquerques, New Mex.)
A HIGH RELIABILITY THIN-FILM HYBRID DEVELOPMENT PROGRAM. pp. 210-11. 1974 Government Microcircuit Applications Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper summarizes experience at Sandia Labs. in the design, development, and technology transfer (to Bendix Kansas City Div.) of hybrid microelectronic technology for war reserve nuclear weapons. In summary our approach to the hybrid reliability has been to concentrate our internal development efforts to a single technology. Studies and development of this technology are closely coordinated with the production agency. The materials and processes used by the production agency are described in written specification and production travelers assuring that the hardware is consistent and that the devices made in production will be representative of the devices made in early development. Gold thermocompression bonding is utilized wherever possible.

10734

Pullen, K.A., Jr. (U.S. Army Ballistic Res. Labs., Aberdeen Proving Ground, Md.)
ON THE RELATION OF TRANSCONDUCTANCE EFFICIENCY TO MICROCIRCUIT RELIABILITY. pp. 212-3. 1974 Government Microcircuit Applications Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The relation of the transconductance-per-unit-current efficiency (or transconductance efficiency) to design of reliable microcircuits is analyzed and its relation to the minimization of power dissipation in these circuits is developed. Guiding equations for taking advantage of transconductance efficiency are developed.

10735

Nedved, D.B. and Sanberg, G.L. (MERET Inc., Santa Monica, Calif.)
HYBRID OPTOELFCTRONICS: INTEGRATION OF HYBRID MICROCIRCUITS WITH SEMICONDUCTOR SOURCES AND SENSORS. pp. 216-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper will summarize fabrication and performance characteristics of these high power transmitter for ranging applications and compare them with lower units designed to operate at pulse repetition rates in excess of one MHz for communication applications.

10736

Wiley, T.A. (Bendix Corp., Kansas City Div., Kansas City, Mo.)
WEAPON-SYSTEM PRODUCTION USING BEAM-LEAD HYBRIDS. pp. 226-7. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The new technology required to utilize gold beam-lead devices in current hybrid microcircuit production was selected and defined by the Sandia Corporation, Albuquerque, New Mexico, where the early development work was performed. Bendix engineers in residence at Albuquerque, New Mexico, where the early development work was performed. Bendix engineers in residence at Albuquerque during that time assisted in preparing the documents necessary to transfer the technology to Bendix hybrid manufacturing. Although beam-lead semiconductors offer technical advantages over chip-and-wire devices, their smaller size creates special handling and procurement problems.

10737

Hakim, E.B. and Holevinski, R. (U.S. Army, Army Electronics Command Technol. and Devices Lab., Fort Monmouth, N.J.) FIELD FAILURE INVESTIGATIONS OF PLASTIC AND HERMETIC SEMICONDUCTORS. pp. 258-9. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

To determine actual field failure modes and mechanisms of semiconductor devices and integrated circuits, a program has been initiated to obtain failed devices from systems under repair at depots. The two Army systems selected for study were the Automatic Digital Network (AUTODIN), which is a world-wide data communication system and the SLAE (Standard Lightweight Avionic Equipment) system.

10738

Johnson, G. and Stitch, M. (McDonnell Douglas Astronautics Co., East St. Louis, Mo.) and Brauer, J. (U.S. Air Force Griffiss AFB, RADC, N.Y.) HIGH TEMPERATURE OPERATING TESTS: THE KEY TO IMPROVED MICROCIRCUIT RELIABILITY. pp. 260-1. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Present test results from our comprehensive high temperature accelerated test evaluation of microcircuits clearly show that when properly applied, HTOT can be incorporated into MIL-STD-883 as an excellent device/source qualification test method, and should be considered as a production screening method. Applied voltage as well as temperature has also been shown to be a failure accelerating factor, suggesting the use of an Eyring failure model.

10739

Manno, P. (U.S. Air Force, Griffiss AFB, RADC, N.Y.) and Yoder, R. and Schafer, F.E. (Hughes Aircraft Co., Fullerton, Calif.) RELIABILITY EVALUATION OF LARGE HYBRID PACKAGES. pp. 264-5. 1974 Government Microcircuit Applications Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

The purpose of this study was to evaluate the capabilities of large hybrid packages with respect to MIL-STD-883 type environmental tests. Eight package types (intentionally not identified by Vendor name here) were selected and subjected to eight (8) tests:

1. Bombing Pressure and Hermeticity
2. Acceleration
3. Mechanical Shock
4. Thermal Shock
5. Moisture Resistance
6. Vibration, Variable Frequency
7. Lid-Deflection

In addition, a small side experiment was run to determine if vibration could be substituted for centrifuge.

10740

Lauffenburger H.A. and Mirth, L.A. (IIT Res. Inst., Reliability Analysis Center, Griffiss AFB, RADC, N.Y.) RAC: A COMPREHENSIVE MICROCIRCUIT RELIABILITY INFORMATION SERVICE. pp. 268-9. F30602-73-C-0065. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

Assessing and controlling reliability of microelectronic devices is a major concern among producers and users of electronic systems. The Reliability Analysis Center has accumulated extensive resources and staff expertise that is available to government and contractor engineers to augment their own resources. This paper has attempted to provide an overview of the nature of these resources and show how they have been applied to specific problems.

10741

Maddox, R.L. and Ronen, R.S. (Rockwell Internatl. Electronics Res. Div., Anaheim, Calif.)
ON SOME FEATURES AND APPLICATIONS OF BULK AND SOS MOSFETs AT CRYOGENIC TEMPERATURES. pp. 274-5. DA HC 60-73-C-0087. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper describes the performance of bulk silicon and SOS MOSFETs at cryogenic temperatures. Discussed are the temperature dependence of the I-V characteristics, drain breakdown voltage, threshold voltage and leakage current, conductance and transconductance, and field effect mobility. Carefully fabricated P-MOSFETs are shown to be excellent devices for cryogenic applications, down to 4°K.

10742

Kirschman, R.K. (JPL, Calif. Inst. of Technol., Pasadena, Calif.) and Notarys, H.A. and Mercereau, J.E. (Calif. Inst. of Technol., Sloan Lab. of Low Temp. Phys., Pasadena, Calif.)
SUPERCONDUCTING QUANTUM ELECTRONIC MICROCIRCUITS. pp. 276-7. NAS7-100. N00014-67-A-0094-0013. 1974 Government Microcircuit Applications Conference Digest of Technical Papers. Vol. V. Sponsored by the Department of Defense (Army, Navy, Air Force), National Aeronautics and Space Administration, Department of Commerce (Bureau of Standards), Post Office Department, Defense Supply Agency and Atomic Energy Commission. University of Colorado, Boulder, Colo., 288 pp., June 25-27, 1974

This paper summarizes the projected applications for these superconducting microcircuits, their fabrication, characteristics, and some similarities and differences compared to semiconducting microcircuits. As examples of this new technology, two prototype superconducting microcircuits are presented.

10743

Stapper, C.H. (IBM Corp., System Prod. Div., Essex Junction, Vt.)
DEFECT DENSITY DISTRIBUTION FOR LSI YIELD CALCULATIONS. IEEE Trans. on Electron Devices ED-20, no. 7, 655-7, July 1973

The experimental determination of defect density distributions is described. These distributions are needed for calculating LSI yields. The defect densities appear to be distributed according to gamma distributions. An expression for a semiconductor process is derived based on the results.

10744

Frohman-Bentchkowsky, D. (Intel Corp., Santa Clara, Calif.)
FAMOS-A NEW SEMICONDUCTOR CHARGE STORAGE DEVICE. Solid-State Electronics 17, no. 6, 517-29, June 1974

A new non-volatile charge storage device is described. The floating gate avalanche injection MOS (FAMOS) structure is a p-channel silicon gate field effect transistor in which no electric contact is made to the silicon gate. It combines the floating gate concept with avalanche injection of electrons from the surface depletion region of a p-n junction to yield reproducible charging characteristics with long term storage retention.

10745

Moriarty, R.M. (Litton Ind., Inc.)
SURVIVAL IN METALLIZATION BURNOUT. Paper no. 710792, 8 pp., Sept. 1971. National Aeronautic and Space Engineering and Manufacturing Meeting. Los Angeles, Calif., Sept. 28-30, 1971

Electronic systems must be able to withstand certain radiation environmental stresses which could potentially result in significant transient currents to its semiconductors. The reliability of integrated circuits is dependent upon the over stress to which they are exposed in operation. Overstress of the integrated circuit in the form of metallization burnout causes openings in the interconnection paths leading to failure of the connected circuitry. This study seeks to identify the failure mechanism with its corresponding thresholds and magnitude of currents as well as to identify a probability of survival number for the threshold condition.

10747

Durso, J. (Motorola Semiconductors, Ltd., Dielectric Isolated Integrated Circuits, Wembly, Middlesex, Gt. Britain)
THE QUALITY ASSURANCE OF SEMICONDUCTOR DEVICES. Microelectronics and Reliability 11, no. 2, 129-37, Apr. 1972

To assure a high quality of all devices produced by a semiconductor manufacturer, electrical and mechanical testing of samples of devices is performed at every stage of the manufactured product, from its initial design, which takes quality assurance testing requirements into consideration, to the dispatch of devices to customers.

10748

Warner, R.M., Jr. (U. of Minn., Dept. of Elec. Eng., Minneapolis, Minn.)
APPLYING A COMPOSITE MODEL TO THE IC YIELD PROBLEM. IEEE J. of Solid-State Circuits SC-9, no. 3, 86-95, June 1974

The defect density within an integrated circuit (IC) slice often exhibits gross variation, which may vary from center to periphery, or from side to side. It has been erroneously described as "Nonrandom." The term random nonhomogeneous, is more distinctive because it leads to a simple description; the slice area from half a slice to many slices. The total silicon area involved could be divided into as few as two or three subareas. Two methods for accomplishing the decomposition into subareas are described for one example.

10750

Caley, R.W., (Microsystems Internatl. Ltd., Ottawa, Can.)
A THICK AND THIN FILM APPROACH TO FABRICATING MCA SUBSTRATES. Electronic Packaging and Production 13, no. 12, 12 pp., Dec. 1973

If cost is more critical than size the substrate is usually fabricated from thick films; if performance and small size are priorities, thin films are chosen. For multichip arrays (MCAs) however, the future points toward a compromise and hence to a combination of thick and thin film materials.

10752

Anon.
PROCEEDINGS, THE FIRST CANADIAN SRE RELIABILITY SYMPOSIUM. Ottawa, Ontario, Can., 149 pp., May 11, 1974

Contents:
- Computer-Aided Sequential Testing for Equipment Reliability
- A Special Markov Model for Reliability Analysis
- Voltage Measurements in the Scanning Electron Microscope
- Reliability Analysis of Logic Circuits
- An Analytical Model for Maintainability Assessment
- Reliability Targets - Are They Valid and Can They Be Specified
- Upgrading Reliability: An Economic Analysis
- The Hermes Reliability Program
- On the Software Reliability
- Reliability and Maintainability of Transmission Lines
- RMS (Reliability, Maintainability and Supportability) - A Parametric Case Study
- JETS (Joint Enroute/Terminal System)
  Reliability, Availability and Maintainability Considerations for an Air Traffic Control System

10753

Black, T. (Microsystems Internal. Ltd., Ottawa, Ontario, Can.) and Shaw, D.A. (Semco Instr. Co. Ltd., Ottawa, Ontario, Can.)
VOLTAGE MEASUREMENTS IN THE SCANNING ELECTRON MICROSCOPE. pp. 19-30. Proceedings, The First Canadian SRE Reliability Symposium. Ottawa, Ontario, Can., 149 pp., May 11, 1974

A new secondary electron detector system for measuring specimen surface potentials in the Scanning Electron Microscope is described. It consists basically of a simple, magnetic field electron spectrometer with a scinatillator - photomultiplier detector. Preliminary results are presented that show the range and linearity of the detector to be acceptable for some routine integrated circuit failure analysis work.

10754

Deger, E. and Jobe, T.C. (RCA Corp., Consumer Electronics, Indianapolis, Ind.)
FOR THE REAL COST OF A DESIGN, FACTOR IN RELIABILITY. Electronics 46, no. 18, 83-9, Aug. 30, 1973

Extended warranties, plus rising repair costs, are compelling consumer-product engineers to assess component reliability; here's a way to figure total reliability costs into design tradeoffs. Quality emphasizes the initial performance of a component but reliability assures the continuation of performance over a period of time. Reliability tests in addition to quality tests therefore are necessary to ensure that specs are not only met initially but maintained over some specified time.

10755

Douglas, E.C. (RCA Labs., Princeton, N.J.) and Dingwall, A.G.F. (RCA Solid State Tech. Center, Somerville, N.J.)
ION IMPLANTATION FOR THRESHOLD CONTROL IN COSMOS CIRCUITS. IEEE Trans. on Electron Devices ED-21, no. 6, 324-31, June 1974

Experimental determinations of ion-implanted diffusion profiles, sheet resistivities, and threshold voltage, for boron, phosphorus, and arsenic implantations are reported for doses in the range from 1×10^{11} to 1×10^{14} ions/cm^2. Care has been taken to insure accuracy of implanted dose in the 35-150keV range in order to permit direct comparison of experiments with theory.

10757

Gupta, A. (Rockwell Internatl., Microelectronic Div., Anaheim, Calif.), Porter, W.A. (Tex. A. and M. U. Elec. Eng. Dept., Coll. Sta. Tex.) and Lathrop, J.W. (Clemson U., Elec. and Computer Eng. Dept., Clemson, S.C.)
DEFECT ANALYSIS AND YIELD DEGRADATION OF INTEGRATED CIRCUITS. IEEE J. of Solid-State Circuits SC-9, no. 3, 96-103, June 1974

This paper analyzes the yield considering both radial and angular variation in the defect density. The degradation in yield due to point defects, area defects, and defect clusters is considered in detail. Further, a method of optimum chip placement is described, and the results of a computer calculations showing yield as a function of chip size are given assuming different defect density distributions. The results are primarily applicable to large integrated circuit chips.

10758

Prather, J.B., Robertson, S.D. and Slemmons, J.W. (Rockwell Internatl., Anaheim, Calif.)
ALUMINUM WIRE BONDING TO GOLD THICK-FILM CONDUCTORS. Electronic Packaging and Production 14, no. 5, 68-71, May, 1974.

The well-established technique of aluminum ultrasonic wire bonding and the reliability of gold thick-film conductors make them an attractive combination. Interface problems are minimized by the presence of copper and by the use of a 1% silicon aluminum wire.

10759

Vest, R.W. (Purdue U. Layfayette, Ind.)
CONDUCTION MECHANISMS IN THICK FILM MICROCIRCUITS. Semi-Ann. Tech. Rept. July 1-Dec. 31, 1973. 42 pp., Feb. 1, 1974. AD 775 639. DAHC 15-73-G8

Studies of the electrical properties of a single contact between small RuO_2 single crystals gave insight into a charge transport mechanism not involving well sintered contacts. Studies of test resistors made with RuO_2 particles one thousand times greater in diameter than normal for a thick film resistor confirmed the general observations in the single contact studies, namely, that a low resistivity contact with a TCR below that of RuO_2 can be developed without true sintering between RuO_2 particles.

10761

Taketa, Y. and Haradome M. (Nihon U. at Narashino, Phys. Sci. Labs., Narashinodai, Japan)
MECHANISM OF AGING IN Pd-Ag THICK-FILM RESISTORS. IEEE Trans. on Parts, Hybrids and Packaging PHP-9, no. 2, pp. 115-22, June 1973

Accelerated life tests under elevated temperature, and vacuum have been conducted on Pd-Ag thick-film resistors. It is found that the change of resistance under those accelerated life test conditions is mainly caused by oxidation and reduction of the electrically conductive components (Pd and Ag) of Pd-Ag thick-film resistors. Through life tests in vacuum, the effect of absorption was found to be less important than the structural change inside the resistor.

10762

Feller, A., Lombardi, T.J., Ramondetta, P.W. et al. (RCA, Advanced Technol. Labs., Camden, N.J.)
LOW POWER HIGH DENSITY MOS ARRAYS FOR ARMY APPLICATION. Rept. no. ECOM-0216-1, Quart. Rept. no. 1, June 15-Sept. 14, 1973, 31 pp., Oct. 1973. AD 914 365L
Rept. no. ECOM-0216-2, Quart. Rept. no. 2, Sept. 15-Dec. 14, 1973, 21 pp., Apr. 1974. AD 918 609L. DAAB07-73-C-0216

The objective of this program is to develop an optimized CMOS technology which at an operational rate of 1MHz can provide low power, high density arrays which are compatible with low cost, quick turnaround, design automation techniques. These LSI arrays produced should have two orders of magnitude lower dissipation and higher packing densities than the best available PMOS LSI standard cell arrays designed in accordance with established layout rules. In pursuing this objective various CMOS technologies will be investigated and evaluated in terms of their applicability to meeting the short-term and long-term objectives of this program. Among the basic CMOS technologies that will be considered will be the bulk silicon substrate and the insulating substrate types. Within these two basic technologies more than 15 significant variations exist.

10767

Harris, C.M., Marchal, W.G., Zacks, S. et al. (George Wash. U., School of Eng. and Appl. Sci., Inst. for Management Sci. and Eng., Washington, D.C.)
FAILURE-RATE PREDICTION AND WEAROUT DETECTION. Rept. no. T-282, Sci. Rept., 48 pp., May 11, 1973.
Rept. no. T-296, Sci. Rept., 196 pp., May 8, 1974. N00014-67-A-0214-0001

The main purpose of this work has been to provide the Navy with powerful statistical techniques for improved failure pattern prediction, with a particular emphasis on the development of procedures for detecting when devices are first beginning to show signs of ageing. Of course, any improvement in failure prediction has obvious implications for extensive cost savings in both procurement and inventory.

10771

Cullen, G.W., Corboy, J.F. and Kokkas, A.G. (RCA Labs., Princeton, N.J.)
SILICON ON SAPPHIRE TRANSISTOR DEVELOPMENT. Rept. no. AFAL-TR-73-200, Rept. no. PRRL-73-CR-025, Final Rept., Apr. 3, 1972-Mar. 31, 1973, 114 pp., May 1973. AD 912 256L. F33615-72-C-1695

The semiconductor properties of 0.5μm silicon films heteroepitaxially deposited on sapphire and spinel substrates are strongly influenced by the chemical and physical nature of the silicon substrate interface. The nature of the interface is in turn a function of the manner in which the work damage is removed from the fabricated substrate surface, the conditions of the heteroepitaxial growth, and the type and orientation of the substrate. The hall mobilities in the thin silicon films have been measured as a function of these variables in order to develop the optimum preparative conditions. The minority carrier lifetime has been measured in the burst grown and standard grown heteroepitaxial silicon. Improvement in the lifetime has been realized by use of the burst growth technique.

10772

Smith, J.S., Kapfer, V.C. and Doyle, E.A., Jr. (U.S. Air Force, Griffiss AFB, RADC, N.Y.)
RELIABILITY EVALUATION OF 54L20 RADIATION HARDENED DUAL NAND GATES. Rept. no. RADC-TR-73-180, Final In-House Rept., 42 pp., June 1973. AD 765 173

Radiation hardened low power microcircuits using high resistivity thin film chrome silicide resistors were evaluated by subjecting the devices to convertional high temperature stress tests a special low temperature screen test. The predominant failure mechanisms of two failures generated under the high temperature stress tests consisted of oxide defects and surface inversion. Results of this test program indicated that there were no thin film resistor failures in these devices either under high temperature or low temperature test conditions. It appears that the chrome silicide resistors show promise of improving the reliability of hardened circuits, however, other factors may be contributing to these observed results.

10774

Williams, T.D., Wilcox, E.A., Weitzman, C. et al. (System Dev. Corp., Santa Monica, Calif.)
LSI IMPACT ON COMMAND, CONTROL, AND COMMUNICATION SYSTEMS.
Rept. no. SDC-TM-4710/003/00, Tech., Mem., 240 pp., May 27, 1971. AD 912 251L. Rept. no. TM-4710/000/00, Tech. Mem., 23 pp., June 14, 1971. AD 912 252L.
ROMS VS RAMS. Rept. no. TM-4779/001/00, Tech. Mem., 139 pp., Sept. 30, 1971. AD 912 253L. N00123-71-C-0012

New technology can greatly improve a system's responsiveness in terms of cost, performance, schedule, management and even design pholosophy. To effectively assess the impact of new technology in the military environment, one must not only be able to evaluate what this improvement could mean. This report is an overview of the impact of the Large-Scale Integration, (LSI) technology on command, control, and communications (C^3) systems in terms of improved capabilities and what these improvements mean.

10775

Orndorff, R.M. amd Kramer, G.M. (Hughes Aircraft Co., Advanced Technol. Lab., Culver City, Calif.)
RADIATION HARDENED VOLTAGE REGULATOR
Monthly Prog. Rept. no. 14, 3 pp., Aug. 5, 1974.
Monthly Prog. Rept. no. 15, 4 pp., Sept. 3, 1974
Monthly Prog. Rept. no. 16, 4 pp., Oct. 4, 1974. Rept. no. AFAL-TR-74-263, Interim Tech. Rept. June 1973-Apr. 1974, 24 pp., Oct. 1974.
Monthly Prog. Rept. no. 17, 3 pp., Nov. 1, 1974.
Monthly Prog. Rept. no. 18, 4 pp., Dec. 6, 1974.
Monthly Prog. Rept. no. 19, 5 pp., Jan. 8, 1975. F33615-73-C-1284

The objective of the Radiation Hardened Voltage Regulator (RHVR) program is the design, fabrication and testing of a voltage regulator circuit capable of being used in computer systems using Metal-Oxide-Semiconductor (MOS) technology. The voltage regulator will be capable of operating in power supply subsystems having output voltages of either polarity (plus or minus) with amplitudes of 5 Volts or greater.

10780

Givens, S. (Siliconix, Inc.)
USING FETs AS ANALOG SWITCHES. Instr. & Control Systems 47, no. 5, 45-51, May 1974

Trade-offs can affect your designs. Transistors are used as solid-state digitally-controlled switches in an increasing variety of industrial monitoring and control systems. Several types of these switches are available, offering a number or characteristics and trade-offs tc be considered for particular applications.

10781

Roughan, P.E. (Sprague Elec. Co., North Adams, Mass.)
THERMAL RESISTANCE OF IC PACKAGES. Electronic Packaging and Production 14, no. 6, 116-9, June 1974

Determination of IC thermal resistance can be made with thermocouples attached to the device while it is in free air or immersed in a liquid. Greater measurement accuracy is obtained by using an oil bath, especially for epoxy-encapsulated components.

10783

Tapp, C.M. and Traeger, R.K. (Sandia Labs., Albuquerque, New Mex., Livermore, Calif.)
SANDIA LABORATORY HYBRID MICROCIRCUIT AND RELATED THIN FILM TECHNOLOGY. Rept. no. SAND74-0009, Bib., 34 pp., June 1974. AT(29-1)-789

Hybrid circuit applications for nuclear weapons have been considered at Sandia since the mid-60's. However a major commitment was made in 1970 to develop a limited but well understood set of technologies for weapon applications. Development of these technologies and related studies have been documented in a number of publications. This bibliography lists the publications from 1968 to early 1974 for reference by the workers in the field, to initiate further development and to provide hybrid designers an index of available documentation.

10784

O'Donovan, M.V., Kudsia, C.M. and Keyes, L.A. (RCA Ltd., Quebec, Can.)
DESIGN OF A LIGHT-WEIGHT MICROWAVE REPEATER FOR A 24-CHANNEL DOMESTIC SATELLITE SYSTEM. RCA Rev. 34, no. 3, 506-38, Sept. 1973

The transponder described in this paper has 24 channels, each of which has a pass bandwidth of 36 MHz. The receive frequency band is 5925-6425 MHz and the transmit band is 3700-4200 MHz. The wideband receiver-driver portion of the transponder is all solid state. The characteristics of this design are compared with those of a receiver-driver incorporating driver traveling-wave-tube amplifiers; detailed tradeoffs, in terms of performance, weight, reliability and power requirements, are provided. The impact of different communication traffic models on the complexity and weight of the transponder is discussed, and finally, the performance characteristics, weight, and reliability of a baseline 24-channel transponder are presented.

10785

Holmes, P.J. (Royal Aircraft Establ., Radio Dept., Farnborough, Hants, Engl.)
CHANGES IN THICK-FILM RESISTOR VALUES DUE TO SUBSTRATE FLEXURE. Microelectronics and Reliability 12, no. 4, 395-6, Oct. 1973

It has been noted on a number of occasions that stresses set up in the resin-potting of electronic components may be severe enough to distort the package contents, but there appears to be no published information on the changes to be anticipated when thick-film resistors are subjected to deformation by this or any other means. Some Dupont "Birox" resistors were prepared on long narrow alumina substrates to enable "bending beam" experiments to be carried out at curvatures much greater than those which could conceivably occur in normal circumstances. The bending was carried out first with the resistor on the inside of the curve (in compression) and then on the outside (in tension).

10786

Gallace, L.J. and Vara, J.S. (RCA, Solid State Div., Somerville, N.J.)
EVALUATING RELIABILITY OF PLASTIC-PACKAGED POWER TRANSISTORS IN CONSUMER APPLICATIONS. IEEE Trans. on Broadcast and Television Receivers BTR-19, no. 3, 194-204, Aug. 1973

This paper describes reliability-test techniques that are used to determine and control the reliability of plastic-packaged power transistors in consumer applications. The high-volume plastic package was introduced to satisfy the requirement for cost-reduced components in the consumer industry; the small size of the package provides additional important system-cost reductions.

10787

Petersen, J.J. (Collins Radio Group, MOS Div., Newport Group, Calif.)
DESIGN AND DEVELOPMENT OF MOS SCALER INTEGRATED CIRCUIT.
Rept. no. HDL-TR-050-1, Final Rept., Oct. 1972-Oct. 1973, 124 pp., Aug. 1974. DAAG39-73-C-0050

This report discusses the work performed by the Collins Radio Group, MOS Div. during the development of the Harry Diamond Labs MOS Scaler Integrated Circuit. In particular, this effort included verification of the logic design, design of the MOS circuit, layout of the MOS chip, manufacturing of the MOS chip and testing. Each of these tasks is discussed in detail in this report.

10788

Lindholm, F.A., Brodersen, A.J., Chenette, E.R. et al. (U. of Fla., Eng. and Ind. Expt. Sta., Gainesville, Fla.)
SOLID STATE MATERIALS AND DEVICES. Rept. no. AFCRL-TR-74-0044, Final Sci. Rept., Sept. 1, 1972-Aug. 31, 1973, 131 pp., Dec. 1, 1973. AD 781 165.
F19628-72-C-0368

This program involves studies in several different problem areas:

(a) the further development of Schottky-barrier photodiodes made with a new mask structure proposed recently at the U. of Fla., and collateral studies concerned with material properties relevant to photodetection;
(b) inferences from the noise spectrum measured in semiconductor devices, including irradiated junction field-effect transistors;
(c) modeling of semiconductor devices for computer-determined design including characterization for exposure to radiation environments; and
(d) study of the potential of carrier-domain devices in electronic system applications.

The content of this final report includes treatment of each of these subjects

10789

Dickens, L.E. and Littlepage, R. (Westinghouse Elec. Corp., Westinghouse Defense and Space Center, Aerospace Div., Baltimore, Md.)
INTEGRATED PARAMETRIC AMPLIFIERS.
Rept. no. ECOM-0221-2, Semiann. Rept. no. 2, Dec. 8, 1972-June 8, 1973, 41 pp., Nov. 1973. AD 915 584L. DAABO7-72-C-0221

The objectives of this program are the design and development of an all solid state integrated circuit microwave parametric amplifier and low noise down converter and the performance of an amplifier cost analysis which will include a cost/electrical parameter trade-off study and the determination of cost/quantity break points. Also presented are the results of the initial implementation of the proposed design with data on component parts of the breadboard amplifier and converter. This includes data on the microstrip signal circulator, the pump isolator, the pump oscillator, the paramp signal circuit, down converter, and the pump leveler and bias regulator circuit.

10792

Kennan, W.F. and Smith, D.M. (Tex. Instr. Inc., Dallas, Tex.)
PULSE POWER STUDIES OF HARDENED MICROCIRCUITS. Rept. no. RADC-TR-73-367, Final Rept., Nov. 1971-May 1973, 77 pp., Dec. 1973. AD 779 666. F30602-72-C-0077

A significant portion of military microcircuit field failures is due to electrical overstress. The purpose of this study was to identify those processing parameters which have an impact on the susceptibility of a device to failure from a high voltage transient. Of special interest was a greater understanding of the junction shorting mechanisms and thin film resistor burnout. It was shown that by increasing base and emitter sheet resistances a substantial improvement in power handling capabilities could be obtained. This is believed to be accomplished by establishing parallel current paths, thus distributing the power dissipation. It is along these lines that effective hardening efforts can be accomplished. The model for the prediction of thin film resistor burn-out can serve as a design guideline for tailoring these components to any practical over-voltage level.

10794

Fowkes, F.M., Dahlke, W.E. and Butler, S.R. (Lehigh U., Bethlehem, Penn.)
RADIATION EFFECTS IN MOS GATE INSULATORS. Rept. no. HDL-TR-200-1, Final Rept., July-Dec. 1973, 44 pp., Jan. 1974. AD 780 186. DAAB-9-73-C-0200

Impurity metal ions (sodium, aluminum, and gold) were diffused (and grown) into oxide films on silicon which were then exposed to 10^6 rads of ionizing radiation from a cobalt-60 source. The effects of radiation were observed by chemical analysis (to determine ion transport) and by conductance and capacitance measurements (to determine oxide charge and distrubution of surface state density).

10800

Motorola Semiconductor Prod. Inc., Eng. Dept., Phoenix, Ariz.
THE MOTOROLA FLIP CHIP STORY. 17 pp.

Solder bump flip-chips were developed by IBM for internal use. The development of this technology provided them with a low-cost, high-volume assembly method which could be automated. However, even though the flip-chip assembly method is easily automated, it is not necessary to gain the benefits of using them. Additionally, flip-chips can give higher reliability and better yields, because the attachment of the chips to the substrate is not dependent upon an operator or wire bond machine. Consequently, these better yields contribute to a lower total cost per completed circuit.

10801

Wagner, R.C. (Sprague Elec. Co., North Adams, Mass.)
CHIP COMPONENTS FOR HYBRID MICROELECTRONICS: A RELIABILITY STATUS REPORT. Rept. no. TP-74-6, 10 pp., Nov. 1973. Symposium on Reliability in Electronics, in Budapest, 1973

Chip components are generally divided into passive and active types. The passive types comprise capacitors and resistors; virtually no true inductive chips being available or required in hybrid circuits. The capacitor types can further be subdivided into ceramic, tantalum, and film. Both categories of passive components (i.e. capacitors and resistors) can also be divided into thick-film types; the thin film types subject to further breakdown into flip-chip, wire-bond, beam-lead styles. Both categories (discrete and integrated circuits) are subject to similar restraints in terms of manufacturing processes and failure mechanisms. Hence, only discrete semiconductors are included in this discussion.

10803

Foster, T.M. and Digiondomenico, O.J. (Westinghouse Elec. Corp., Systems Dev. Div., Baltimore, Md.)
THICK FILM TECHNIQUES FOR MICROWAVE INTEGRATED CIRCUITS. IEEE Trans. on Parts, Hybrids and Packaging PHP-10 no. 2, 88-94, June 1974. 1973 International Microelectronic Symposium. Sponsosred by the International Society for Hybrid Microelectronics. Sheraton-Palace Hotel San Francisco, Calif. Oct. 22-24, 1973. IEEE Trans. on Parts Hybrids and Packaging PHP-10, no. 2, 88-94, June 1974

A thick film approach to state-of-the-art microwave integrated circuits, which has been used to produce thousands of highly reliable low cost S-band and L-band solid state modules for production radar systems is described. These modules include low-noise amplifiers, double conversion mixers, interdigital filters, multiple port power dividers and switches, phase encoders, and power amplifiers. In summary, it has been noted that thick film MIC's are easy to make, inexpensive, reliable highly repeatable, and for the frequency range of 1 to 4 GHz in which they have been used, excellent microwave performance has been found.

10804

Stalter, J.J., Sideris, G. and Cohler, E.U. (Sylvania Elec. Prod. Inc., Electronic Systems Div., Waltham, Mass.)
THE PACKAGING REVOLUTION. PART II: DESIGN AND MANUFACTURING OVERLAP. PART III: COMPUTERS DESIGN LAYOUT. Electronics 38, 12 pp., Nov. 1, 1965

Assembly of integrated-circuit systems requires special fabrication processes. At an early stage, designers and the manufacturing department must make important decisions such as what package form and lead-joining method to use. For each packaging decision, starting with selection of the IC package form and running through modular size, form of wiring and method of cooling, has its impact on the assembly methods. Designers call on computers for help in obtaining optimum speed and performance. The earliest IC's did not pose serious layout difficulties configurations, a computer can reduce wiring delay and crosstalk.

10805

Seliger, R. (Hughes Aircraft Co., Hughes Res. Labs., Malibu, Calif.)
BEAM TECHNOLOGY FOR THE FABRICATION OF MICROWAVE INTEGRATED CIRCUITS.
Final Tech. Rept., Jan. 2, 1973-Mar. 31, 1974, 98 pp., May 1974. N00019-73-C-0261

This report discusses the progress made during the fourth phase of a multi-year program to demonstrate the feasibility of maskless doping by a focused programmable ion beam. The efforts during the fourth phase were devoted to developing techniques for registering and aligning an ion beam pattern with existing sturcture on a substrate, determining the alignment accuracy and demonstrating the registration capabilities on a prototype microwave device. The ultimate goal of this program is to develop the necessary technology to produce micrometer-sized ion beams for implantation doping that can be registered on, and deflected over, microelectronic circuitry in a programmed manner (i.e., by a computer) to form a precision fabrication step not requiring the use of masks. The technology being developed is ultimately to be compatible with complete vacuum processing of advanced microelectronics circuits, including high frequency microwave semiconductor devices and integrated circuits.

10806

Patel, J.R. (Bell Labs., Murray Hill, N.J.)
X-RAY ANOMALOUS TRANSMISSION AND TOPOGRAPHY OF OXYGEN PRECIPATION IN SILICON.
J. of Appl. Phys. 44, no. 9, 3903-6, Sept. 1973

Presently available highly perfect crystals of silicon do not show any degradation of their perfection after heating at 1000°C. This is in contrast to the earlier observation where in floating-zone dislocation-free crystals the x-ray transmitted intensity could decrease by over an order of magnitude. From present observations on carbon-free and carbon-doped crystals wer conclude that the previous floating-zone crystals contained oxygen below the limits of detection of the infrared method. The defects responsible for the observed decrease in the transmitted intensity have been observed directly by x-ray topography. A better quantitative determination of the size and distribution of defects is necessary for more accurate comparison with theory.

10807

Doerner, R.A., Buckley, R.R., Haszko, S.E. et al. (Bells Labs., Murray Hill, N.J.)
TAPERED WINDOWS IN SiO_2 BY ION IMPLANTATION. Trans. on Electron Devices ED-20, no. 9, p. 840, Sept. 1973. Presented at the 1972 International Electron Devices Meeting, Washington, D.C.

The enhanced etch rate of ion damaged SiO_2 has been used to controllably taper steps in thermally grown SiO_2. A 50-KeV Ar^+ implantation with a dose of $3X10^{13}/cm^2$ produces a uniform taper of 35-45° with no vertical step at the top edge of the window. These results are observed by viewing the sample on edge with a scanning electron microscope (SEM). It appears from the tapered wall for a dose of $3X10^{13}/cm^2$ has a smoother profile than the untapered wall.

10808

Kumar, S. (NCR, Microelectronics Div., Miamisburg, Ohio) and Gregor, L.V. (IBM System Prod. Div., East Fishkill, Hopewell Junction N.Y.) J. of Electrochem. Soc. 120, no. 9,
DISTRIBUTION OF SODIUM IN SPUTTERED SiO_2 AS DETERMINED BY NEUTRON ACTIVATION AND U.V. SPECTROGRAPHIC ANALYSES. 1285-7, Sept. 1973

Contamination in sputtered SiO_2 films can cause an increase in MOS surface leakage current due to surface inversion. Sodium ion is one of the major contaminants that cause this problem. Neutron activation and u.v. spectrographic techniques have been rearly applied to sputtered SiO_2 films. The purpose of this work was to investigate the presence and distribution of sodium in sputtered SiO_2 and to determine the source of the sodium.

10809

Berglund, C.N., Clemens, J.T. and Nicollian, E.H. (Bell Labs., Murray Hill, N.J.)
UNDERCUT ISOLATION-A TECHNIQUE CLOSELY SPACED AND SELF-ALIGNED METALLIZATION PATTERNS FOR MOS INTEGRATED CIRCUITS. J. of Electrochem. Soc. 120, no. 9, 1255-60, Sept. 1973

A new technique for achieving electrically isolated, closely spaced, and self aligned metalization patterns on thin insulating films for integrated circuit applications is described. This scheme takes advantage of the shadowing effect etched in the upper insulator delineates and acts as an etch mask for undercutting and thinning down the second insulator on the semiconductor substrate. The major requirement is that the first insulator be weakly or not at all affected by the etch for the second insulator. Because of the masking effect of undercutting, a thin metal evaporation will be discontinuous at all under cut edges resulting in electrically isolated metalization patterns with virtually zero lateral spacing between them. The silicon dioxide-alumina double insulator system with titanium-palladium-gold metalization was used and the details of the technique, including methods of selectively connecting isolated metal patterns, are described. Experimental data are presented to show that undercut isolation can be achieved with high reliability, undercut edges several centimeters in length being typically observed between unintentional shorts. Advantages and utility of the technique are illustrated by describing the design of a charge-coupled device.

10810

Meek, R.L., Buck, T.M. and Gibbon, C.F. (Bell Labs., Murray Hill, N.J.)
SILICON SURFACE CONTAMINATION: POLISHING AND CLEANING. J. of Electrochem. Soc. 120, no. 9, 1241-6, Sept. 1973

The manner in which polished wafers are treated (precleaned) in removing them from the polishing block is not an important factor in the final observed surface contamination of cleaned wafers. Fe is not an important surface contaminant after silica-sol polishing. S and Cl are present at $\sim 10^{13}$ cm^{-2} after all cleaning procedures studied. Other major contaminants are Ca, Cu, and some species in the Pt-Pb range. The peroxide-ammonia, peroxide-hydrochloric acid cleaning eliminates Ca and Cu much more reliably than does the $HF:HNO_3$ cleaning. $HF:HNO_3$ cleaning leaves a heavy mass impurity in the Pt-Pb range. An added HCl dip removes it. The peroxide-ammonia cleaning procedure removes all surface impurities heavier than Cl to below the level of detectability. Impurities left after silica-sol polishing and preoxidation cleaning do not appear to control diode quality.

10815

Hitch, T.T. and Bube, K.R. (RCA Labs., Process and Appl. Matls. Res. Lab., Princeton, N.J.)
BASIC ADHESION MECHANISMS IN THICK AND THIN FILMS. Rept. no. PRRL-74-CR-63, Quart. Tech. Rept. no. 3, July 1-Sept. 30, 1974, 52 pp., Oct. 31, 1974. N00019-74-C-0270

A principal objective of the study has been to further the overall understanding of thick- and thin-film hybrid conductor films and particularly of thick-film gold on 96 and 99.5 wt pct alumina. Our focus in this work has been on the adhesion of such films, but we realized at the inception of the work that tradeoffs among the properties of adhesion, bondability, conductivity, and perhaps others are inherent in the technology, particularly in frit-bonded systems. Because of that relization, the RCA Labs. hybrid materials research team has applied considerable effort to understanding the development of other important as well as to performing the direct studies on adhesion. In this report, data taken at RCA are presented on the bulk resistivities and on an indicator for bondability - crossed-polarized light metallography.

10816

Heid, K. (Electrotec, Inc., Garland, Tex.)
A THIN-FILM HIGH SHEET RESISTIVITY MATERIAL. Solid-State Technol. 16, no. 9, 56-8, Sept. 1973. 1972 International Microelectronics Symposium. Sponsored by International Society for Hybrid Microelectronics. Shoreham Hotel, Washington, D.C., Oct. 30-31, Nov. 1, 1972.

The use of chromium disilicide ($CrSi_2$) as a thin film resistor material capable of sheet resistivities of 1000 ohms per square or greater is explored. The feasibility of sequential deposition of chromium disilicide and nickel-chromium to achieve 1000 ohms per square and 100 ohms per square resistor films on a single substrate is also investigated.

10818

Markley, R.E. (Bendix Corp., Kansas City Div., Kan.)
BEAM LEAD DEVICE AND HYBRID MICROCIRCUIT TESTING. Rept. no. BDX-613-1113. 38 pp., Mar. 28-9, 1974. AT(29-1)-613

Two levels of automatic testing processes have been developed and are operational. These processes are dedicated to the support of high-volume hybrid microcircuit production. Process development activities are pre-presently underway to expand both process levels to include rf component and rf hybrid testing.

10820

Grieco, M.J. (IBM Components Div., East Fishkill Facility, Hopewell Junction, N.Y.)
INVESTIGATION OF IMPERFECTIONS IN SILICON SUBSTRATES USING COPPER DISPLACEMENT TECHNIQUE. J. of Electrochem. Soc. 121, no. 2, 289-93, Feb. 1974

A copper displacement etching system has been used as an effective and sensitive technique for the delineation and evaluation of crystal imperfections in polished silicon substrates. X-ray topographs of the substrate prior to and after epitaxial deposition show a relationship between subsurface damage and/or contamination and defects in the epitaxial film.

10821

Kulkarni, M.V., Smith, P.J., James, G.A.A. et al. (IBM System Prod. Div., East Fishkill Facility, Hopewell Junction, N.Y.)
STRUCTURE OF ANODICALLY DECORATED npn BIPOLAR TRANSISTORS. J. of Electrochem. Soc. 121. no. 2, 280-6, Feb. 1974

Examining transistors which anodically decorated in HF solution to reveal pipes we found that large different number of leakage paths in each transistor. Resistance associated with each leakage path was in the 12,000-20,000 ohm range; different resistances were detected both electrically by electrochemical etching behavior in the n^+ region. From their behavior during electrochemical etching, it was determined that the leakage paths seemed to consist of narrow regions of n^+ material extending from the emitter through the base into the collector. The leakage paths occurred both in and at the edge of the emitter (at the vertical emitter-base junction). Direct relation between pipes and crystallographic defects could be made, but it is shown that not all crystallographic defects cause serious junction leakages.

10823

Stehlin, R.A., DeVries, D., Bean, K. et al. (Tex. Instr. Inc., Dallas, Tex.)
BIPOLAR MEDIUM-SCALE INTEGRATED CIRCUIT HARDENING. VOL. I. PHASE I. Rept. no. AFWL-TR-73-293, Contractor's Rept. no. 03-73-88, Final Rept., Jan. 1-Sept. 30, 1973, 146 pp., Apr. 1974. AD 783 360. F29601-73-C-0048

Low- or medium-power transistor-transistor logic (TTL) hardening efforts that have been or are presently being conducted require further improvement. The objective of this program is to develop improved radiation-hardening techniques for low-power, Schottky, TTL medium-scale integrated (MSI) circuits. To demonstrate the feasibility of the developed hardening technique, demonstration transistors were produced to allow yield assessment and devices for radiation testing.

10825

Trever, G.W. (U.S. Air Force, Wright-Patterson, AFB, Air Force Inst. of Technol. Ohio)
QUASI-STATIC CAPACITANCE-VOLTAGE CHARACTERISTICS OF MNOS DEVICES. Rept. no. GE/EE/73A-30, Thesis, 91 pp., Dec. 1973. AD 777 586

The quasi-static (low frequency) capacitance-voltage (CV) characteristics of MNOS memory devices are shown to exhibit distinguishable properties associated with "memory" and "nonmemory" behavior. Quasi-static CV analysis procedures, as developed by Kuhn, are applied to the MNOS "nonmemory" characteristics and reveal that the silicon-oxide interface-state densities are 100 times larger than for comparable "nonmemory" capacitor structures. Substrate surface-potential functions are constructed to model ideal "nonmemory" CV behavior and are used to compare with "memory" CV characteristics.

10826

Mize, J.P. (Southern Methodist U., Electronic Sci. Center, Dallas, Tex.)
DEVELOPMENT OF SILICON MONOLITHIC SURFACE-WAVE ARRAYS. Rept. no. AFAL-TR-72-59, Final Rept., July 1-Dec. 31, 1971, 41 pp., Mar. 1972. AD 893 266L. F33615-72-C-1020

The objective of this research is to fabricate silicon device structures capable of generating acoustic surface waves. Realization of this objective would result in silicon programmable surface-wave arrays which would be fully compatible with MOS/LSI technology. The performance and cost effectivenss of MOS/LSI applied to these electronic functions could have a major impact on radar and communication system technology.

10827

U.S. Air Force, Wright-Patterson AFB, Ohio
GENERAL INDEX AND REFERENCE. SERIES 1-0 GENERAL. AFSC Design Handbook no. DH1-1, Third Edn., Dec. 1, 1973

The AFSC Design Handbooks are published as a primary means of documenting and applying Air Force technical knowledge in support of system and equipment acquisition programs. General design criteria and guidance suitable for use in the design and development of Air Force systems and equipment are published in these handbooks. The design handbooks preserve Air Force technical experience, summarize the lessons learned, and present the user with background data and the basis for requirements. This handbook is one of a series of correlated volumes used in the design and development of aerospace systems.

10828

U.S. Air Force, Dept. of the Air Force, Wright-Patterson AFB, Ohio)
CHECKLIST OF GENERAL DESIGN CRITERIA. SERIES 1-0 GENERAL. AFSC Design Handbook no. DH1-X, Second Edn., Jan. 15, 1973
Rev. to Second Edn., Jan. 15, 1974

This handbook contains checklists for each of the Design Handbooks in Series 1-0 General. In general, the checklists are intended for use by systems designers to ensure that all applicable design factors have been examined and all problems have been resolved or otherwise determined unimportant to the design.

10829

U.S. Air Force, Wright-Patterson AFB, Ohio
GENERAL DESIGN FACTORS. SERIES 1-0 GENERAL. AFSC Design Handbook no. DH1-2, Third Edn., Feb. 20, 1974

This handbook, AFSC DH 1-2, "General Design Factors," is one of a series of correlated volumes used in the design and development of aerospace systems. The design Handbooks contain requirements and considerations above the level of general and detail specifications. They are primary source of design criteria and guidance in basic technical areas of aerospace systems design. Design information of a nonmandatory nature is provided to increase understanding of technical problems and to facilitate their solution.

10830

U.S. Air Force, Wright-Patterson AFB, Ohio
MAINTAINABILITY (FOR GROUND ELECTRONIC SYSTEMS). SERIES 1-0 GENERAL. AFSC Design Handbook no. DH1-9, Second Edn., Dec. 20, 1973

This is the second edition of the Air Force Systems Command Design Handbook 1-9, Maintainability (For Ground Electronic Systems). The procedures used and the examples given have been determined to satisfy the requirements of these systems. Many of the procedures described are taken from the general field of maintainability.

10833

Rees, G.H. (Brush Wellman Inc., Cleveland, Ohio
PRODUCTION ENGINEERING MEASURES TO MANUFACTURE SUPER FINE FINISH BERYLLIA. Rept. no. BW-TR-550, Quart. Prog. Rept., June 30-Sept. 30, 1974, 33 pp., Oct. 29, 1974. DAAB07-74-C-0606

Plans were made and initial work started on the development of processes for the manufacturing of beryllia substrates having a surface smoothness not exceeding four microinches per inch by progressive polishing steps. The primary effort centered on studying lapping variables such as pressure, time, abrasive grit size and material on substrate material removal rate and surface smoothness. The first step in the process must provide a flat surface for subsequent polishing while minimizing the degradation of surface smoothness. The results show that 600 grit abrasive, normally used for rough polishing, can be used for this purpose better than other grits examined.

10834

Carroll, B.D. (Auburn U., Auburn, Ala.)
A STUDY OF FAULT DIAGNOSIS OF SEQUENTIAL LOGIC NETWORKS. Final Rept., 24 pp., Oct. 31, 1974. DA-ARD-D-31-124-72-68G. DA-ARO-D-31-124-72-G147

A statement is given of the problem studied along with summaries of the results obtained. A list of reports and papers published is included. Copies of the papers are also included in an appendix.

10835

Patstone, W.
TAPE CARRIER PACKAGING BOASTS ALMOST UNLIMITED POTENTIAL. EDN 19, no. 20, 30-7, Oct. 20, 1974

The tape-carrier microinterconnect system, which has aroused so much interest among semiconductor manufacturers for producing DIP IC's looks like it might have equally great-if-not more-potential for hybrid and higher level circuits. In fact, the concept could signal a major change in how electronic packaging will be conducted in the future. Basically, it boils down to repetitively fabricating miniture printed circuits on a plastic tape that often resembles movie film. From this basic format, there is not limit as to what can be accomplished in terms of circuit complexity and processing automation.

10836

IEEE
12TH ANNUAL PROCEEDINGS, RELIABILITY PHYSICS 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Sessions:
- Analysis Techniques
- Reliability Improvement Through Process Control and Component Design
- High Current Density Effects
- Workshop on Metallurgical Failure Modes
- Metallization, Metallurgical Effects and Bonding
- Packaging and Encapsulation; Hybrid and Passive Components
- Workshop on MOS Drift Mechanisms
- Compound Semiconductor and Microwave Devices

10837

Baitinger, W.E., Winograd, N. and Amy, J.W. (Purdue U., Dept. of Chem., West Lafayette, Ind.) and Munarin, J.A. (U.S. Navy, Nav. Ammunition Depot, Crane, Ind.)
NICHROME RESISTOR FAILURES AS STUDIED BY X-RAY PHOTOELECTRON SPECTROSCOPY (XPS OR ESCA). pp. 1-6. GP-37017X. GH-335741A1. AFOSR-72-2238. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0939-1-PHY.

Depth profiles yielding both information on oxidation state and elemental composition have been obtained for model nichrome films by using X-ray Photoelectron Spectroscopy and argon ion sputtering. Evidence is presented showing the formation of thin insulating films at the interface between two metals caused by solid state reactions occuring between metals and metal oxides.

10838

Weisenberger, W.H., Gray, H., Hubler, G.K. et al. (U.S. Navy, Nav. Res. Lab., Washington, D.C.)
DIRECT COMPARISON OF AUGER, SIMS, AND PROTON RESONANCE PROFILING FOR RELIABILITY STUDIES. pp. -15. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

The purpose of this work was to compare three techniques: AUGER, SIMS, and PROTON RESONANCE PROFILING. Using a set of identically prepared samples, an indication of how these techniques might relate to reliability studies is discussed.

10839

Viele, A.A. (IBM, System Dev. Div., Manassas, Va.)
A FAILURE ANALYSIS TECHNIQUE FOR LOCATING THE FAIL SITE IN MOSFET (LSI) LOGIC CHIPS WITH SPUTTERED SIO_2 PASSIVATION. pp. 16-21. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

This paper describes a technique used successfully to locate the fail site in MOSFET (LSI) Logic Chips. It is used to analyze modules or chips which fail functionally during electrical test. Signal tracing is employed to locate the fail site while dynamically exercising the chip. This technique emphasizes the analysis of AC failures (timing problems) and chips with sputtered $Si0_2$ (Quartz) passivation.

10840

Devaney, J.R. and Sheble, III, A.M. (Hi-Rel Labs., Inc., San Marino, Calif.)
PLASMA ETCHING PROMS AND OTHER PROBLEMS. pp. 22-9. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH-839-1-PHY

Plasma etching or low temperature ashing with an RF field has found numerous applications in semiconductor processing and production. The advantage is a dry procedure with the introduction of no "wet" solutions. If a primary gas containing fluorine is introduced into the field, active fluorine ions are produced, which vigorously attack silicon and silicon dioxide, but, very importantly, do not attack metallic aluminum or nichrome. This selectivity of etch is of great advantage in the removal of glass passivation from atop aluminum interconnects and fusible nichrome links. With the aid of an electron microprobe and a plasma etcher, fused nichrome links in PROMS were studied to determine the location and movement of the metal before and after fusion. Some examples of the use of plasma etching in lieu of wet chemical stripping of glass passivation are presented. Finally, the use of plasma etching to facilitate the study of aluminum alloying into contact windows is described.

10841

Gajda, J.J. (IBM, System Prod. Div., East Fishkill Facility, Hopewell Junction, N.Y.)
TECHNIQUES IN FAILURE ANALYSIS OF MOS DEVICES. pp. 30-7. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

The greatest concern on MOS devices is the physical integrity of the gate oxide. Leakage paths and/or shorts through defect sites in the oxide are a major device reliability problem. Optical microscopy is tedious and often does not resolve the defects. With this in mind, copper decoration techniques were developed that could reveal oxide failures sites to 0.1μm size. The technique has isolated various failure mechanisms on MOS devices. This failure analysis capability has enhanced the ability to control the MOS process.

10842

Angleton, J.L. and Webster, S.L. (Hughes Aircraft Co., Equip. Eng. Div., Components and Matls. Labs., Culver, City, Calif.)
TECHNIQUES FOR STANDARDIZATION OF PARTICLE NOISE IN ELECTRONIC PACKAGES. pp. 38-42. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

A model of the behavior of a particle being virbrated within an enclosed space is presented. This model predicts increased particle detection probabilities by varying vibration parameters. The independent variables of the model are the acceleration level and the package thickness of the device being tested. The dependent variable is the vibration frequency. Support experimental evidence is included A miniature magnetostriction transducer for calibration of the Particle Impact Noise (PIN) system has been developed The device can be fabricated into an easily operated, self contained unit for system testing during production line usage of the PIN system. It has also been valuable in testing individual components of the system.

10843

Jones, W.K. (Charles Stark Draper Lab., Inc., Cambridge, Mass.)
PLASMA ETCHING AS APPLIED TO FAILURE ANALYSIS. pp. 43-7. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Plasma Etching is presently being applied to PROM samples of know fusing history and grow-back susceptibility. STEM analysis will then be used for elemental mapping of the nickel and chrome within the gap region. The purpose of this study is to supply material data which, when coupled with reliability data, will give indications of the fusing mechanism.

10844

Piwczyk, B. and Siu, W. (Bell-Northern Res., Ottawa, Ontario, Can.)
SPECIALIZED SCANNING ELECTRON MICROSCOPY VOLTAGE CONTRAST TECHNIQUES FOR LSI FAILURE ANALYSIS. pp. 49-53. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Several scanning electron microscopy voltage contrast techniques used for integrated circuit failure analysis are compared. A newer, simpler technique permitting the elimination of the topographic image information while retaining the voltage contrast information is described. This technique called Selective Voltage Contrast (SVC) also permits the viewing of voltages in a circuit as imposed by individual input level changes. Examples of the application of the technique are shown using bipolar integrated circuits and a charge coupled memory device.

10845

Speakman, T.S. (Western Elec. Co., Inc., Reading Penn.)
A MODEL FOR THE FAILURE OF BIPOLAR SILICON INTEGRATED CIRCUITS SUBJECTED TO ELECTROSTATIC DISCHARGE. pp. 60-9. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

It has been shown that the failure mechanism for bipolar integrated circuits subjected to an electrostatic discharge is very probably a melting condition caused by localized overheating due to the rapid pulse of current which flows during the Discharge. It has also been shown that the Wunsch-Bell formular which relates power density to pulse duration can be used to predict the threshold power density levels for failure. This in turn can be used to calculate the electrostatic voltage which will produce failure under various conditions through the application of the proper equivalent circuit. Finally, results were presented which show that grounding bracelets and metal handling trays are effective in reducing the number of defects caused by static electricity.

10846

Anolick, E.S., Prosser, J.F. and Remis, B.R. (IBM, System Prod. Div., Fishkill Facility, Hopewell Junction, N.Y.)
RELIABILITY STUDY OF AN N-CHANNEL SILICON GATE FET WITH FIELD SHIELD. pp. 70-3. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grnad Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

A reliability study was performed on an N-channel FET with a self-aligned gate and a field shield. It was found that the field shielf was very successful in reducing leakage and did not add significantly to the failure rate of the structure. It was further found that in terms of dielectric shorts and V_T stability, the silicon gate structure was as good as or better than comparable metal-gate devices.

10847

Barnes, D.E. and Thomas, J.E. (Hughes Aircraft Co., Equip. Eng. Div., Components and Matls. Labs., Culver City, Calif.)
RELIABILITY ASSESSMENT OF A SEMICONDUCTOR MEMORY BY DESIGN ANALYSIS. pp. 74-81. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cag. no. 74CH0839-1-PHY

We have shown how a design review can be used to develop an understanding of the critical areas of a design and to serve as a basis for controlling reliability of an LSI circuit. The programming circuit analysis has been developed to the point where the parameters and process critical to producing the proper energy at the nichrome resistor have been identified. We do not now know the range of energy required for proper programming; we hope studies currently underway will soon be productive in this area. We have also identified all functions and are continuing a search for subtle parasitic elements which may be a problem. None are obvious at this time.

10848

Franklin, P. and Burgess, D. (Monolithic Memories, Inc., Sunnyvale, Calif.)
RELIABILITY ASPECTS OF NICHROME FUSIBLE LINK PROM'S (PROGRAMMABLE READ ONLY MEMORIES). pp. 82-6, 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Reliability aspects of nichrome fusible link PROM's have been investigated and are defined in the areas of manufacturing, screening, testing and programming. Early mortality failure populations are analyzed and long term life considerations explored. The "grow-back" mechanism, a failure mode involving the relinking of fuses, is characterized and discussed in terms of design, programming, screening, testing and reliability.

10849

Eisenberg, P.H. and Nolser, R. (Litton G/CSD, Woodland Hills, Calif.)
NICHROME RESISTORS IN ROGRAMMABLE READ ONLY MEMORY INTEGRATED CIRCUITS. p. 87 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Computer designers whose goals require rapid programming of semiconductor read only memories have utilized large quantities of PROMS (programmable read only memories). The most popular of these devices is programmed by raising the resistance of a nichrome resistor above a threshold value required to change the PROM output logic level.

10850

Parker, G.H., Cornet, J.C. and Pinter, W.S. (Intel Corp., Santa Clara, Calif.)
RELIABILITY CONSIDERATIONS IN THE DESIGN AND FABRICATION OF POLYSILICON FUSIBLE LINK PROM's. pp. 88-9. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

This paper describes some of the design and fabrication considerations in a 1024 bit programmable read only memory. The memory element in the PROM is a fusible link consisting of a notched stripe of polycrystalline silicon. It has been shown that the polysilicon fusible link lends itself to conventional processing and through design and process control, a highly reliability 1024 bit array has been realized.

10851

Cohn, N.S. (U.S. Navy, Nav. Ordnance Lab., Silver Spring, Md.)
SUSCEPTIBILITY OF SEMICONDUCTOR DEVICES TO THERMAL SECOND BREAKDOWN. pp. 90-3. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

A method for determining the susceptibility of semiconductor devices to damage from an electromagnetic pulse (EMP) due to induced thermal second breakdown is described. The method can be used as a nondestructive screening test. It is based on the increase in junction reverse breakdown voltage with temperature and can be used to find the most EMP resistant devices of a given device type. A mathematical explanation is presented, and other tentative applications are proposed.

10852

Gottesfeld, S. (RCA, Solid State Div., Somerville, N.J.)
A LIFE-TEST STUDY OF ELECTROMIGRATION IN MICROWAVE POWER TRANSISTORS. pp. 94-100. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

A life-test study was made of a microwave power transistor employing aluminum metallization. The life tests were conducted under dc overstress conditions to accelerate the rate of failure as a result of electromigration of the metallization system. Analysis of the failures revealed the presence of both aluminum and silicon electromigration, with the latter the primary cause of failure. A failure-rate model was constructed from the data relating MTF to activiation energy, temperature, and current density.

10853

LaCombe, D.J. (GE, Syracuse, N.Y.) and Carroll, J.F. (U.S. Air Force, Griffiss AFB, RADC, Rome, N.Y.)
FAILURE MECHANISMS IN GOLD AND ALUMINUM MICROWAVE POWER TRANSISTORS. pp. 101-8. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

This paper presents the results of controlled CW tests and failure analyses of two L-band transistor types, one gold metallized and one aluminum metallized, and compares their relative capabilities under high temperature operation.

10854

Fresh, D.L. (Aerospace Corp., Los Angeles, Calif.) and Adolphsen, J.W. (NASA, Goddard SFC, Greenbelt, Md.)
SEM EVALUATION OF METALLIZATION ON SEMICONDUCTORS. PP. 118-30. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

A test method for the evaluation of metallization on semiconductors is presented and discussed. The method has been prepared in MIL-STD format for submittal as a proposed addition to MIL-STD-883. It is applicable to discrete devices and to integrated circuits and specifically addresses batch-process oriented defects. Quantitative accept/reject criteria are given for contact windows, other oxide steps, and general interconnecting metallization. Figures are provided that illustrate typical types of defects. Apparatus specifications, sampling plans, and specimen preparation and examination requirements are described. Procedures for glassivated devices and for multi-metal interconnection systems are included.

10855

Harman, G.G. (U.S. Dept. of Commerce, Natl. Bur. of Standards, Inst. for Appl. Technol., Washington, D.C.)
METALLURGICAL FAILURE MODES OF WIRE BONDS. pp. 131-41. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Various metallurgical failure modes of gold and aluminum wire bonds are described. Examples are taken from both low and high power devices. Whenever possible, known methods of avoiding these failure modes are given. Wire bond failure modes can be divided into two categories. The first is comprised of those failure modes that are caused by poorly controlled or poorly designed manufacturing processes that result in lower product yield or higher per unit bonding cost, as well as those processes that predispose the device to early field failure. The second category is comprised of the failure modes of adequately made bonds that are caused to fail by environmental stresses during the operating life of the device. The most frequent causes of failures are discussed in detail.

10856

Black, J.R. (Motorola, Semiconductor Prod. Div., Phoenix, Ariz.)
PHYSICS OF ELECTROMIGRATION. pp. 142-9. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

This survey paper on electromigration describes factors which govern the rate of electromigration and therefore relate to the lifetime of conductors stressed at high current density. These include the type of metal conductor, the conductor cross sectional area, lattice, grain boundary and surface diffusion effects, the addition of alloying elements, temperature and current density as well as the thermal conductivity of the substrate. The effect of gradients in temperature, current density, conductor composition and grain size on conductor lifetime are also discussed.

10857

Johnson, J.E. (Westinghouse Elec. Corp., Semiconductor Div., Youngwood, Penn.)
DIE BOND FAILURE MODES. pp. 150-4 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev. 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

In this paper, we outline several methods of examining die bonds, and consider the factors which give rise to die bond problems, particularly during their formation as part of the device manufacturing process.

10858

Kolesar, S.C. (Tex. Inst., Inc., Matls. Characterization Lab., Dallas, Tex.)
PRINCIPLES OF CORROSION. pp. 155-67. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Metallization corrosion is a common reliability problem in semiconductor devices. A typical integrated circuit corrosion failure is shown. This article is a review of those principles of corrosion which are applicable to corrosion problems commonly encountered in the electronics industry. The discussion, which is descriptive rather than rigorous, is illustrated by examples of circuit and component failures drawn from the available literature as well as from Texas Instrument data.

10859

Koelmans, H. (Philips Res. Labs., Eindhoven, Neth.)
METALLIZATION CORROSION IN SILICON DEVICES BY MOISTURE-INDUCED ELECTROLYSIS. pp. 168-71. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel Las Vegas, Nev., 320 pp., Apr. 2-4, 1974 IEEE Cat. no. 74CH0839-1-PHY

In an investigation of the factors which determine the rate of electrolytic corrosion of the Al metallization in plastic-encapsulated ICs operated in a moist atmosphere, the surface conductivity of thermal SiO_2 was measured as a function of relative humidity and temperature. Electrolysis in the water film absorbed at high relative humidity produces either protection of the Al metallization by anodization or destructive corrosion at the anode and/or cathode. The occurrence of protection or destructive corrosion is mainly determined by the nature and amount of ionic impurities present in the water film and by temperature.

10860

Paulson, W.M. and Kirk, R.W. (Motorola Semiconductor Prod. Div., Matls. Res. Lab., Phoenix, Ariz.)
THE EFFECTS OF PHOSPHORUS-DOPED PASSIVATION GLASS ON THE CORROSION OF ALUMINUM. pp. 172-9. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

The corrosion rate of aluminum metallization under bias was measured as a function of the phosphorus content of the CVD passivation glass under different temperature and humidity conditions. The electrolytic corrosion was the most intense at the negative electrode and the corrosion product was aluminum hydroxide. Changing the phosphorus concentration from 2 to 10 wt. pct. increased the corrosion rate by a factor of 25. Increasing the relative humidity at 85°C from 85 to 100% caused the corrosion rate to increase by two orders of magnitude. A 30°C rise in temperature resulted in five times the corrosion rate. A model to account for the observed corrosion has been proposed.

10861

Holloway, P.H. and Bushmire, D.W. (Sandia Labs., Albuquerque, New Mex.)
DETECTION BY AUGER ELECTRON SPECTROSCOPY AND REMOVAL BY OZONIZATION OF PHOTORESIST RESIDUES. pp. 180-6. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Surface chemical analyses by Auger electron spectroscopy (AES) indicate that hydrocarbon residues are frequent contaminants on gold hybrid microcircuit metallization. The primary electron beam for AES cracks the hydrocarbon contaminants causing a carbonaceous residue. Lead frame bonding data demonstrated that a carbon residue approximately 10 Å thick was indicative of thermocompression bond degradation. Concentrations of two percent ozone in oxygen can remove a photoresist layer approximately 200 Å thick in 100 hours at room temperature. This restores thermcompression bondability of gold surfaces.

10862

Gurev, M.S. (Motorola Semiconductor Prod. Div., Matls. Res. Lab., Phoenix, Ariz.)
SENSITIVITY OF CURRENT PULSE BURN-OUT TESTING TO THE GEOMETRY OF DEFECTS IN ALUMINUM METALLIZATION. pp. 187-95 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

In this paper we will demonstrate that the current pulse test, when properly conducted, will detect defective step coverage. We will present experimental evidence that the worst case for defective metallization step coverage detection by pulse testing, an extremely sharp notch 500 Å wide which reduces minimum metal thickness to only 7% of nominal thickness, can be readily detected by this technique. Such a notch is barely resolvable by SEM inspection and might readily escape routine SEM screening. We will also demonstrate that previously reported failures of the pulse test in detecting defects can be attributed to the use of multiple pulse testing of a single metallization stripe which can heal defects and prevent their detection.

10863

Harman, G.G. (U.S. Dept. of Commerce, Natl. Bur. of Standards, Electronic Technol. Div., Inst. of Appl. Technol., Washington, D.C.)
A METALLURGICAL BASIS FOR THE NON-DESTRUCTIVE WIRE-BOND PULL-TEST. pp. 205-10. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974.
IEEE Cat. no. 74CH0839-1-PHY

Non-destructive wire-bond pull tests are often specified by high-reliability electronic device users in order to eliminate weak, poorly made wire bonds. The main problem with the test has been in establishing a pull-force level which will assure that the bonds are adequately strong but will not damage them during the test. In the present work, factors affecting the non-destructive wire-bond pull-test are examined. The variables, such as wire and bond-loop elongation, bond geometry, bond deformation, and the mean and standard deviation of the destructive bond pull test are studied to determine their influence on the non-destructive test. Different pull-force criteria are derived for wire with high elongation, such as is used in power devices, and for wire with low elongation, typically used for bonding integrated circuits.

10864

Flaskerud, P. and Mann, R. (Electronic Arrays, Inc., Mountain View, Calif.)
"SILVER PLATED LEAD FRAMES" FOR LARGE MOLDED PACKAGES. pp. 211-22. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

This paper discusses the economics of various gold substitute systems. In addition, the paper presents data which demonstrates the reliability of molded packages using silver plated lead frames. Reliability data on Life, Temperature Cycling, 85°C/85% RH and Solderability Testing is presented. Silver plating is an economical and reliable system for use in molded packages for MOS-LSI devices.

10865

Pietrucha, B.M. and Reiss, E.M. (RCA, Solid State Div., Somerville, N.J.)
THE RELIABILITY OF EPOXY AS A DIE ATTACH IN DIGITAL AND LINEAR INTEGRATED CIRCUITS. pp. 234-8. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Mechanical screening has shown that epoxy provides a positive die-to-substrate interface capable of withstanding a high degree of thermal and physical stress. Silver migration and metallization corrosion were not observed during the visual inspection. Histograms of leakage parameters show that outgassing of epoxy does not affect the stability of an integrated circuit, even after 600 hours of exposure to temperature stress. There was no significant degradation in the leakage parameters during test. Analysis of outgassing constituents reveals no substantial concentrations of ionizable compounds which might contribute to contamination-type failure mechanisms.

10866

Stanley, A.G. and Rader, C.M. (MIT, Lincoln Lab., Lexington, Mass.)
LEAK DETECTION OF INTEGRATED CIRCUIT AND OTHER SEMICONDUCTOR DEVICES ON MULTILAYER CIRCUIT BOARDS. pp. 239-42. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

The radioisotope leak test has been modified to detect leaks, in integrated circuits and other devices mounted onto multilayer circuit boards, over the entire range from 10^{-1} to 10^{-8} atm. cc per second. The method combines radiation shielding techniques with three sequential tests using krypton-85. The test program has succeeded in detecting a significant number of leaky components on electronic boards for a high reliability space application.

10867

Lawson, R.W. (British Post Office Telecommun. Headquarters, Res. Dept., Engl.)
THE ACCELERATED TESTING OF PLASTIC ENCAPSULATED SEMICONDUCTOR COMPONENTS. pp. 243-9. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

The primary objective of the test programme was to establish whether a valid acceleration technique is possible for the prediction of the long term reliability of plastic encapsulated bipolar semiconductor components. Most emphasis has been placed on humidity testing but no generally accepted life accelerated test has emerged.

10868

Kriegler, R.J. (Bell-Northern Res., Ottawa, Can.)
ION INSTABILITIES IN MOS STRUCTURES. pp. 250-8. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Reliability Group. MGM Grand Hotel Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

Sodium and a few other alkali metal impurities, introduced during processing into the SiO_2 gate insulator of MOS devices, are easily ionized and are sufficiently mobile even at low temperatures to cause a considerable drift of the electrical characteristics of MOS devices. This paper reviews methods of detecting the presence of mobile ions and discusses techniques for reducing the concentration of impurities or eliminating their deleterious electrical effect.

10869

Woods, M.H. (RCA Labs., Princeton, N.J.)
INSTABILITIES IN DOUBLE DIELECTRIC STRUCTURES. pp. 259-66. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

In this paper we will be concerned with silicon device instabilities due to changes in the electrical properties of the insulator structure. For the most part these instabilities are due to changes in the space charge in the insulators. Instabilities are shown to arise from polarization, alkali migration and fixed interface charges, conductivity differences and the formation of slow and fast oxide states due to the application of high electric fields in memory devices.

10870

Nicollian, E.H. (Bell Labs., Murray Hill, N.J.)
INTERFACE INSTABILITIES. pp. 267-72. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

A review will be given of the instabilities of MOS field effect transistors caused by the time variation of the electrical properties of the $Si-SiO_2$ interface during device life. Changes in interface properties can be accelerated by heating without bias and heating with negative bias applied to the gate. The specific topics discussed will include how fixed oxide charge and interface trap densitities change with accelerated aging, the effects of these changes on the characteristics of MOS field effect transistors, and how these changes can be minimized to achieve better reliability.

10871

Powell, R.J. (RCA Labs., Princeton, N.J.)
ELECTRON INJECTION AND TRAPPING IN PYROLYTIC Al_2O_3. p. 298. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

In this paper, high-field injection and photo-injection into Al_2O_3 are investigated using new experimental techniques which maintain constant the interface field and injection current, thereby permitting independent determination of injection and trapping characteristics. A preliminary model is presented to explain the large difference between thermal and optical trap activation energies.

10872

Fuls, E.N. and MacArthur, D.M. (Bell Labs., Murray Hill, N.J.)
A SEALED TWO-LEVEL METAL SYSTEM USING TUNGSTEN. pp. 299-303. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

A sealed two-level metallization system using tungsten has been developed at Bell Labs., for LSI MOS fabrication. Tungsten is used for both gate and interconnecting metal and is sealed from corrosive environments by an upper layer of Si_3N_4. Beam leads are provided at the periphery through via holes in the nitride for circuit access. Accelerated aging tests were performed to evaluate the chemical, mechanical and electrical stability performance of this system using both test chips and an actual 1024 bit dynamic RAM.

10873

Freeman, E.R. and Beall, J.R. (Martin Marietta Corp., Denver, Colo.)
CONTROL OF ELECTROSTATIC DISCHARGE DAMAGE TO SEMICONDUCTOR. pp. 304-12. 12th Annual Proceedings, Reliability Physics 1974. Sponsored by the IEEE Electron Devices Group and the IEEE Reliability Group. MGM Grand Hotel, Las Vegas, Nev., 320 pp., Apr. 2-4, 1974. IEEE Cat. no. 74CH0839-1-PHY

The possibility of electrostatic discharge to some types of semiconductors is common knowledge. The list of types that are susceptible continues to grow. Three failure mechanisms and susceptibility criteria are identified. Test techniques and results are presented that were used to correlate damage thresholds to field failures. A discharge circuit formulated from empirical test data and pertinent literature is discussed. Survey data demonstrates that stored charges sufficient to produce part damage are present at all levels of production flow. Recommendations are presented for reducing electrostatic discharge exposure of parts during handling, installation, and test.

10874

Anon.
Solid State Technol. 17, no. 4, 120 pp., Apr. 1974
Solid State Technol. 17, no. 7, 56 pp., July 1974
Solid State Technol. 17, no. 9, 98 pp., Sept. 1974
Solid State Technol. 17, no. 10, 98 pp., Oct. 1974

10875

Carnes, J.E. and Kosonocky, W.F. (RCA Labs., Princeton, N.J.)
CHARGE-COUPLED DEVICES AND APPLICATIONS. Solid State Technol. 17, no. 4, 67-77, Apr. 1974

Charge-coupled devices (CCD's) represent a new concept for silicon integrated circuits. This article reviews the basic operation of CCD's including their operating limitations, methods of fabrication, and experimental results. The various potential applications of CCD's are also described.

10876

Kern, W. (RCA Corp., David Sarnoff Res. Center, Princeton, N.J.)
CHARACTERIZATION OF LOCALIZED DEFECTS IN DIELECTRIC FILMS FOR ELECTRON DEVICES (PART II). Solid State Technol. 17, no. 4, 8 pp., Apr. 1974

Capabilities and limitations of various types of analytical methods for detecting and characterizing localized imperfections in typical dielectric films used in present-day silicon semiconductor device technology are surveyed and compared. Dielectrics and insulators of particular interest include thermally grown silicon dioxide and layers of vapor deposited silicon dioxide, silicate glasses, silicon nitride aluminum oxide, and complex silicates in thicknesses ranging from several hundred angstroms to several micrometers. The analytical methods discussed in some detail include optical contrast microscopy, scanning electron microscopy, self-healing dielectric breakdown, selective chemical etching, electrolytic decoration, liquid crystal techniques, electron-probe microanalysis, and ion microprobe mass analysis. Serveral additional methods are briefly noted. Particular emphasis is placed on recent improvements achieved in these analytical methods. Applications are discussed and illustrated with typical examples, and trends in future developments are indicated.

10877

Bishop, R.A. (RCA, Solid State Div., Sudbury-on-Thames, Engl.) and Carley, D.R. (RCA, Solid State Div., Somerville, N.J.)
FUNDAMENTALS OF COS/MOS INTEGRATED CIRCUITS. Solid State Technol. 17, no. 4 85-9 Apr. 1974

The development of the technology that makes possible simultaneous fabrication of n-channel and p-channel metal-oxide semiconductor (MOS) transistors on the same semiconductor pellet has given rise to a new family of monolithic integrated circuits, viz., a series of complementary-symmetry/metal oxide semiconductor (COS/MOS) devices. This article discusses the MOS transistors used in COS/MOS integrated circuits, describes basic COS/MOS building-block elements, and explains the built-in protection against high-voltage transient and inherent high noise impunity of these integrated circuits. In addition, the major performance characteristics of COS/MOS devices are compared with those of other commercially available digital integrated circuits.

10878

Livesay, W.R. (Radiant Energy Systems, Newbury Park, Calif.)
COMPUTER CONTROLLED ELECTRON-BEAM PROJECTION MASK ALIGNER. Solid State Technol. 17, no. 7, 21-6, July 1974

Photolithographic processes in microelectronics have been pushed to their resolution limits and, as a result, new techniques have been proposed both in electron-beam microfabrication and X-ray lithography. However, these new techniques, though demonstrated on an R&D scale, are not readily adaptable to a production process. An electron-beam projection system is described which has been specifically built for production and enables submicron structures to be defined over a large image format (three-inch diameter). The electron projection system described features computer controlled mask-to-wafer alignment and an automatic handling system for processing wafers in vacuum.

10879

Thompson, L.F. (Bell Labs., Murray Hill, N.J.)
DESIGN OF POLYMER RESISTS FOR ELECTRON LITHOGRAPHY (PART I). Solid State Technol. 17, no. 7, 5 pp., July 1974

Electron lithography requires both negative and positive resists which have been designed to capitalize on these advantages such as resolution, line width, control, etc., which the technique offers. Design of polymer materials for electron resists requires a detailed understanding of electron scattering and radiation chemistry. This article describes the application of fundamental theory to the design of a family of negative resists based on copolymers of ethyl acrylate and glycidyl methacrylate and poly (olefin sulfone) positive resists. A review of electron resist development is also included.

10880

Bates, D.J. (Watkins-Johnson Co., Palo Alto, Calif.) and Silzars, A. and Ballonoff, A. (Tektronix Inc., Beaverton, Ore.)
SOME RELIABILITY ASPECTS OF ELECTRON BOMBARDED SEMICONDUCTOR POWER DEVICES. Solid State Technol. 17, no. 7, 31-5, July 1974

Electron Bombarded Semiconductor or EBS power devices have presented some unique reliability problems to the developers. Recently, many of the design and processing difficulties have been overcome and devices have now demonstrated over 12,500 hours of cw operation. With further significant improvements to be expected, increasingly better performance can be anticipated in the future. This article discusses some of the reliability improvements and describes the development of reliable, radiation resistant semiconductor targets.

10881

Cohen, B.G. (Res. Devices, Inc., Berkeley Heights, N.J.)
INFRARED MICROSCOPY-SOME APPLICATIONS TO SOLID STATE DEVICES. Solid State Technol. 17, no. 7, 36-40 pp., July 1974

The differences between infrared and visible light microscopy are described. The optimum region of the infrared for examination of solid state devices at high resolution is the region near 1000 nm. This optimum is determined by the optical properties of the materials and by the technological state of optical glasses and lens elements. Applications of IR microscopy to semiconductor devices are demonstrated. These include the detection of metallization defects, dislocations and microcracks in transistors and integrated circuits.

10882

Ramsey, T.H., Jr. (Tex. Instr. Inc., Dallas, Tex.)
CRITICAL PARAMETERS IN GLASS SEALED CERAMIC PACKAGES. Solid State Technol. 17, no. 9, 6 pp., Sept. 1974

The continued and increased use of crystallizing solder glass or glass-ceramic seals has created a need for a better understanding of seal dependent characteristics in order to improve yields and reliability. One of the main requirements for good quality seals is an effective glass control program based on differential thermal analysis data. In addition, the geometric characterization of the glass and ceramic are equally important and must be precisely controlled, particularly in the critical seal area. By understanding the glass characteristics which are required for a reliable and effective hermetic seal, problems can be pinpointed and corrected within a minimal time. A well controlled sealing process can easily result in 99% or better seal yields.

10883

Thomas, R.W. (U.S. Air Force, Griffiss AFB, RADC, N.Y.) and Meyer, D.E. (Tex. Instr., Inc., Dallas, Tex.)
MOISTURE IN SC PACKAGES. Solid State Technol. 17, no. 9, 56-9, Sept. 1974

Water in SC packages is known to be a necessary condition for many well known failure mechanisms. The measurement of water hermetically sealed into an SC package is a trail planted with many pitfalls. This article discusses the results of a program to establish better measurement procedures and gives the somewhat surprising results from five independent laboratories analyzing packages sealed under controlled conditions.

10884

Bull, D.N. (Motorola, Inc., Commun. Div., Fort Lauderdale, Fla.)
ADVANCES IN LOW TEMPERATURE DIE BONDING TECHNIQUES. Solid State Technol. 17, no. 9, 60-5, Sept. 1974

When hybrid microcircuits were first produced, the active devices were either encapsulated in standard packages or eutectically die bonded to gold plated tabs. During assembly, these packages or tabs were attached to the film circuit with a low temperature solder. Sensitivity of the film resistors to the high temperature associated with eutectic die bonding (epoxy die bonding at this time was not reliable even if applicable) required this prepackaged approach. Since then, circuit density has increased and the requirement of many active devices further complicates the process with die parameter shifts and bond pad leaching (floating) effects. Now several techniques have been developed to attach the die directly to the module which avoids or reduces these affects. Also monolithic device assembly of heat sensitive dice can use these techniques to advantage.

10885

Nufer, R.W. and Pugliese, F.G. (IBM Systems Prod., East Fishkill Facility, Hopewell Junction, N.Y.)
TRANSFER CIRCUITRY MODULE TECHNOLOGY. Solid State Technol. 17, 10, 98 pp., Oct. 1974. 1973 NEPCON-EAST. New York, N.Y.

A new, low-cost plastic packaging technique for semiconductors is discussed, with details relating to substrate fabrication, molding techniques, and selection criteria for encapsulating materials. A description is given of the process by which a precisely plated circuitry pattern is conveyed into a finished substrate by transferring the circuitry from the mold on which it is plated to the substrate during a conventional modling sequence. This transfer circuitry concept and the developments related to defining the plated circuitry by use of permanent dielectric coatings are also presented. Details are provided on a plated-pin-to-circuitry interconnection, circuitry plating, and the mechanisms of the transfer and adhesion of the circuitry to the polymer. The fabrication of pinned DIP modules (and, in particular, area array modules that employ high I/O counts) exemplifies the extendability of this technology.

10886

Miller, L.F. (IBM System Prod. Div., East Fishkill Facility, Hopewell Junction, N.Y.)
SCREENABILITY AND RHEOLOGY. Solid State Technol. 17, no. 10, 54-60, Oct. 1974

A brief summary of some of the characteristics of polymer solutions which affect rheology is presented. Certainly, the rheology of thick film pastes is very pertinent to their screenability. However, rheological phenomena are so complex, and it is so difficult to formulate a universal definition of screenability, that screening performance cannot always be predicted on the basis of rheological measurements. For example, the rates of shear observed in actual screening processes, and the more subtle implications of visoelasticity, which are examined here, can limit predictions of screenability. The article has three purposes: to provide a background on the rheology of polymer solutions, to show how rheology can be modified and controlled, and to provide some examples relating to these considerations in thick film pastes. It is intended to complement recent papers on the prediction of screenability.

10887

Franconville, F. and Kurzweil, K. (Compagnie Honeywell Bull, Saint-Quen, Fr.) and Stalnecker, S.G. (Microcircuit Eng. Corp., Mount Holly, N.J.)
SCREEN: ESSENTIAL TOOL FOR THICK FILM PRINTING. Solid State Technol. 17, no. 10, 61-8, Oct. 1974

Many variables in thick-film printing have been studied and described in the literature. They refer generally to paste behavior and printing conditions. A relatively neglected item in the thick-film process is the stencil screen which must be of high quality for successful, repeatable printing. Different screen types are reviewed, and comparison of the metal mask versus the emulsion screen different applications are presented. The main characteristics and advantages of direct-emulsion type screens are discussed in terms of screen quality control for repeatable printing with special attention to screen tension evolution duing its lifetime and to selection of the proper solvent for screen cleaning. The influence of various screen parameters will be documented by typical printed examples and methods of control of these parameters in production will be described.

10888

Ricker, T. and Schwing, C. (AEG-Telefunken, Ger.)
THIN FILM STRUCTURES WITH A GAP WIDTH COMPARABLE TO THE FILM THICKNESS FABRICATED BY SPUTTER ETCHING. Solid State Technol. 17, no. 10, 69-72, Oct. 1974

For special applications in microwave integrated circuits or optical waveguides, distances between conductors are needed which are on the order of or smaller than the conducting layer thickness. Obviously such a structure cannot be realized by chemical etching because of the undercutting which allows no gap widths smaller than about twice the film thickness. A DC diode sputter etch process is described yielding a sputter etch rate of the insulating masking layer which is considerably smaller than that of the conducting material. With this technique wall angles of about 60° are achieved with no undercutting.

10889

Bonis, S.A. (Raytheon Co., Sudbury, Mass.)
DRYING UP A SEMICONDUCTOR PACKAGE. Electronic Packaging and Production 14, no. 2, 46-56, Feb. 1974

Electrochemical etching of nichrome resistors in sealed ICs is caused by a surface layer of adsorbed moisture from the interior package atmosphere. A technique for preventing this type failure is by the formation of a porous aluminum oxide desiccant inside the lid.

10890

Sharp, H.E. (GE Space Div., Houston, Tex.)
FEASIBILITY OF INVESTIGATION OF ION IMPLANTATION HARDENING OF LINEAR CMIS CIRCUITS. Final Rept., Dec. 1972-June 1974, 133 pp., June 1974.
N00014-73-C-0224

This report documents an eighteen month effort to determine the feasibility of hardening a CMOS linear circuit (operational amplifier) to the effects of steady state ionizing radiation. The hardening techniques investigated were: Al ion implantation of the gate oxide in N-channel devices and "sintering" for P-channel units. Variations in ion energy and fluence, the type of gate metallization, and the sintering temperature of the gate metallization were observed to have significant effects on radiation resistance. The study results show that it is feasible to harden the monlithic operational amplifier against a total does of 10^6 rad (Si). These devices were implanted with 10 Kev Al ions (10^{15} p/cm^2) and had carbon crucible gate metallization sintered at 500°C for 10 minutes. The computer model of the circuit reproduces the observed experimental results and verifies the interpretation of the response.

10891

Stanley, A.G. (MIT Lincoln Lab., Lexington, Mass.)
REVIEW OF HIGH-RELIABILITY PROCUREMENT PRACTICES IN THE SEMICONDUCTOR INDUSTRY. Rept. no. ESD-TR-74-11, Tech. Note 1974-2, 33 pp., Jan 11, 1974.
AD 773 883. F19628-73-C-0002

High-reliability procurement practices in the semiconductor industry have been reviewed in the light of Lincoln Lab. experience over the past two years. The merits and drawbacks of different types of product assurance methods and specification systems are described. A different kind of procurement method is proposed, in which devices are obtained from the vendors in wafer form on the basis of stringent wafer acceptance tests and subsequently processed on a controlled line under strict quality control conditions including in-process quality control tests, positive lot control and exhausitve screens.

10895

Chapman, B.N. (U. of London, Imperial Coll. London, Engl.)
THIN-FILM ADHESION. J. of Vacuum Sci. & Technol. 11, no.1, 106-13, Jan./Feb. 1974

Adhesion is of vital interest in thin-film science because the fragile film relies on the underlying substrate, and the adhesion between the two, for durability. In addition, the formation and structure of the film depend on the adhesive interaction between the depositing material and the substrate. Despite its general relevance, adhesion is one of the aspects of thin-film science about which little is known. A considerable problem arises with the measurement of adhesion, or more precisely with its lack of susceptibility to measurement. The approaches that have been used are reviewed. A further problem is concerned with the meaning and relevance of "adhesion", and this point will be discussed from both the practical and theoretical points of view. Based as much on empiricism as on understanding, some means of modifying adhesion have been found and these also are reviewed.

10896

Haythornthwaite, R.F., Molozzi, A.R. and Sulway, D.V. (Commun. Res. Centre, Dept. of Commun., Ottawa, Ont., Can.)
RELIABILITY ASSURANCE OF INDIVIDUAL SEMICONDUCTOR COMPONENTS. Proceedings of the IEEE 62, no. 2, 260-73, Feb. 1974

Where small numbers of highly reliable semiconductor devices are required, conventional methods of procurement are found to have deficiencies. An approach to procurement is proposed which is cost effective, accommodates new device types, and assures reliability in the individual device. Although principally applied to silicon planar transistors, the approach can be extended to other semiconductor types. A critical evaluation is made of the manufacturer and his technology. The devices obtained from each diffused wafer are grouped into separate lots. Selected tests are performed on these lots in order to discover possible failure mechanisms. Tests may involve simple electrical measurements or detailed techniques such as scanning electron microscopy and X-ray microprobe analysis.

10897

Birey, H. (Istanbul U., Gen. Phys. Dept., Istanbul, Turkey)
METALLIC ALUMINUM PARTICLE CONCENTRATION IN ALUMINUM OXIDE THIN FILMS. J. of Appl. Phys. 45, no. 9, 3946-8, Sept. 1974

Two different methods based on the tunneling junction model and the optical model are used to determine the metallic aluminum particle concentration in aluminum oxide thin films prepared by thermal evaporation of pure aluminum under appropriate vacuum conditions. The concentration determined from these two models agree with each other at high concentrations and show considerable deviation at low concentrations.

10898

Stach, J., Rupprecht, D., Turley, A. et al. (Penn. State U., University Park, Penn.)
BORON NITRIDE DIFFUSION FOR LSI PROCESSING. Rept. no. ECOM-0299-F, Final Rept. 59 pp., Mar. 1973, AD 762 612

This report describes the properties and behavior of boron nitride diffusion wafers for use in LSI processing The results of the investigations conducted include the determination of proper handling procedures, B_2O_3 growth and volatilization kinetics, furnace parameters, and reliability and reproducibility.

10899

Kahl, F.O. (Corning Glass Works, Electronic Matls. Dept., Corning, N.Y.)
ELECTRONIC ENGINEERING WITH GLASS AND GLASS CERAMICS. Reprinted from Ceramic Ind., Apr. & May 1974

Glass has a broad range of properties that has led to its wide use in the electronics industry to contain, control, transmit or block electromagnetic energy in most parts of the spectrum. Many of the specialty glasses used in the semiconductor industry, 2nd the importance of providing adequate protective films for silicon devices and integrated circuits are discussed. The photographic process is basic to the manufacture of semiconductor devices and integrated circuits.

10900

Dalton, R.H. (Corning Glass Works, Appl. Chem. Res., Corning, N.Y.)
HOW TO DESIGN GLASS-TO-METAL JOINTS. Reprinted from Prod. Eng., 10 pp., Apr. 26, 1965

Properties of metal and glass are often complementary; what one lacks, the other has. Together they cover a range from the best conductors to the best insulators, from high transparency to high opacity, from ductile to brittle, from ferromagnetic to diamagnetic, from highly inert to reactive. Many design requirements are solved best by using them together--introducing the problem of joining metal and glass. Five methods are shown: Mechanical, Adhesive, Direct Fused, Solder Glass and Metallized. Primary considerations dictating design are the strength of glass and the factors that affect fracture.

10901

Gleason, W.A. (Corning Glass Works, Corning, N.Y.)
FIVE WAYS TO SEAL GLASS TO METAL. Reprinted from Matls. in Design Eng., 3 pp., Apr. 1960

Five variety of seals are illustrated. 1) Solder glass used to join aluminum to glass tubing. 2) Glass metallized with thin layers of silver. 3) Compression seal showing a glass window in a bronze bushing. 4) Housekeeper seal with thin (0.0005 in.) molybdenum foil sealed to glass of glass of quartz mercury are lamp. 5) Housekeeper seal between copper and glass.

10902

Dalton, R.H. (Corning Glass Works, Corning, N.Y.)
SEALING WITH SOLDER GLASS. Reprinted from Am. J. of Phys. 32, no. 6, 479-82, June 1964. Talk given at the Laboratory Workshop Conference on Inexpensive High Vacuum Techniques. Sponsored by the MIT Science Teaching Center and the Commission on College Physics. MIT Mar. 25-27, 1963

A discussion is given of the advantages and limitations of the techniques of sealing with solder glasses, of the characteristics which a glass must possess to be suitable for solder sealing, and of the properties of some of the available solder glasses.

10903

Degan, J.J. (Bell Labs., Merrimack Valley, Mass.)
FOCUS ON EFFICIENCY: COMPUTER GRAPHICS FOR HIC DESIGN. Bell Labs., Record 52, no. 9, 286-92, Oct. 1974

With fast-increasing customer demands for service, operating Telephone Companies need new and improved components for their transmission systems. To speed the development of such key system components as hybrid integrated circuits, Bell Labs'. engineers are using computer-supported graphics terminals and faster model-making facilities.

10904

PRIMER ON MICROPROCESSORS. PART I. Electronic Prod., pp. 25-32, Jan. 20, 1975

Not since the development of the transistor in 1948 has any product or technology offered such an exciting promise of things to come as the microprocessor. Applications span the entire realm of electronics and extend into new areas where existing technologies had never before penetrated. This article reviews microprocessor basics, such as software, the advantages and disadvantages of microprocessors, and what to look for when choosing a microprocessor.

10905

Hobson, L. (Burr-Brown Res. Corp., Tucson, Ariz.)
HIGH TEMPERATURE EPOXY/DOUBLE STACK EXPERIMENT. 11 pp., Dec. 4, 1974

Double stacked chips had the same test results as single chips, and therefore, double stacking is an acceptable process for a thin film resistor chips. The burn in portion of the testing is a worst case for the effect of power dissipation, therefore, the only variables undetermined, is chip size and passivations. Both of these are best measured by centrifuge. Future testing should only require evaluation of chip size and passivation.

10906

Kratz, J. (Buckbee-Mears Co., St. Paul, Minn.)
TO STAMP OR TO ETCH-HOW TO CHOOSE. Electronic Packaging and Production, 4 pp., Feb. 1972

A discussion of the processes and a formula for determination, whether to stamp or etch, depends on volume. Two basic processes are available to the manufacturer of lead frames and similar precision components: etching (photochemical machining) and precision metal stamping. Choosing between the two for a given requirement requires some basic knowledge of the capabilities and mechanics of both. The right choice can save precious time and a great deal of money for a manufacturer.

10907

Gage, B.P. (Boeing Co., Seattle, Wash.)
EMP HARDENING OF GFE. Rept. no. AFWL-TR-74-61, Rept. no. D224-10023-1, Final Rept. 121 pp., July 1973. AD 918 276L. F29601-72-C-0028

This report presents a preliminary methodology for the analysis and EMP hardening of Government Furnished Equipment (GFE). The EMP analysis and hardening techniques presented in the EMP Electronic Analysis and Design Handbooks were used as a basis for formulating this methodology. The proposed methodology considers design factors related to the unique problems associated with modifying existing equipment (e.g., cost and logistics.)

10908

Gage, B.P. (Boeing Co., Seattle, Wash.) EMP ELECTRONIC DESIGN HANDBOOK. Rept. no. AFWL-TR-74-58, Rept. no. D224-10019-1, Final Rept. 212 pp., Apr. 1973. AD 918 277L. F29601-72-C-0028

This handbook provides a state-of-the-art compilation of EMP hardening design information in a format of immediate use to electronic designers. Candidate hardening techniques are identified and their implementation is discussed. Pertinent design data are presented and detailed hardening examples are provided. In many cases the required design data were generated directly for this handbook. The appendix provides a general description of the test program.

10909

Vossen, J.L., Schnable, G.L. and Kern, W. (RCA Corp., David Sarnoff Res. Center, Princeton, N.J.) PROCESSES FOR MULTILEVEL METALLIZATION. J. of Vacuum Sci. & Technol. 11, no. 1, 60-9, Jan./Feb. 1974

Film deposition and etching techniques for producing multilevel metallized structures on complex devices are reviewed. Emphasis is placed on process procedures for controlled contouring of topographic features induced during pattern etching, techniques for ensuring coverage by deposited films of topography introduced into the substrate, and the dielectric deposition procedures that enhance breakdown strength and minimize pinholes. Broadly, the classes discussed are:

. Metallization techniques that reduce susceptibility to electromigration and hillock formation and that ensure step coverage.
. Dielectric deposition techniques that result in good step coverage, low stress, and low pinhole density.
. Photolithographic and etching techniques that can taper steps generated in the films and that do not form pinholes.

10911

Csaba[illegible]. (Slovak Tech. U., Dept. of Radiot[illegible]nol., Bratislava, Czechoslov.) and Frank, H. (Tech. U. Prague, Dept. of Solid State Eng., Prague, Czechoslov.) INFLUENCE OF SURFACE TREATMENT OF SILICON ON THE EFFECTIVE IMPURITY CHARGE DENSITY IN SURFACE STATES OF MOS STRUCTURES. Solid-State Electronics 16, no. 9, 985-9, Sept. 1973

The influence of various methods of mechanical, chemical-mechanical and chemical surface treatment of n-type (100) oriented silicon on the effective impurity charge density in surface states of MOS structures and their homogeneity for the given treatment was studied. Values of charge density, N_{ss} were evaluated from high-frequency C-V curves of MOS structures. It was found that the preoxidation surface treatment of silicon influences the effective surface charge density in a definite manner. The most suitable treatment found was a chemical etch in gaseous HCl following mechanical polishing. The homogeneity and value of N_{ss} depend on the thickness of the etched-off surface layer.

10912

Leuenberger, F. (Centre Electronique Horloger, S.A. Neuchatel, Switz.) VAPOUR-DEPOSITED SILICON DIOXIDE FOR DEVICE APPLICATIONS. Thin Solid Films 22, no. 3, 245-53, July 1974

Silicon dioxide layers deposited from the vapour phase at low temperatures are extensively applied in integrated circuit technology. Applications include doped oxide diffusion sources, protective layers and crossover insulators in multilevel metallization systems. This paper shows the feasibility of obtaining a SiO_2-Si interface whose electrical characteristics closely approach those of thermally grown SiO_2-Si sandwich structures. Interface state densities lying in the low 10^{10} cm^{-2} $_{e}V^{-1}$ range have been determined from quasi-static C(V) measurements. The results of excess noise measurements made on deposited gate oxide and thermally grown gate oxide MOSFETs are in reasonable agreement with the interface state density measurements.

10913

Bennett, A.G. (Bendix Corp., Tech. Commun., Kansas City, Mo.)
THE EFFECT OF RAPIDLY CHANGING VOLTAGES ON THICK-FILM RESISTORS. Rept. no. BDX 613-1085 (Rev.) Rept. no. EP4717600, Final Rept. 29 pp., May 1974. AT(29-1)-613 USAEC

Permanent resistance changes in thick-film film resistors are linked to dv/dt sensitivity by this study conducted to determine the mechanisms responsible for these undesirable effects. The resistor is viewed as a network of circuit elements, and an extension of previous theories is proposed to relate the effects of rapidly changing potentials to increased stress on the microscopic distributed capacitances and resistances that comprise thick-film structures and cause resistance reduction resulting from dielectric breakdown and particle fusion.

10914

McCaughan, D.V. and Kushner, R.A. (Bell Labs., Murray Hill, N.J.)
ION MIGRATION EFFECTS IN R.F. "SPUTTER CLEANING" OF DIELECTRIC FILMS. Thin Solid Films 22, no. 3, 359-63, July 1974

We have shown that r.f. backsputtering or "sputter cleaning" of dielectric films may cause: (1) the transfer of impurities from one sample to another or from the substrate table to previously clean samples; and (2) ion migration effects within SiO_2 films which are expected to cause gross degradation of "sputter cleaned" devices. Such degradation may not be annealable, since annealing does not cause the removal of mobile impurities, as has been shown previously. These results are in agreement with the previously presented theory of the ion migration process.

10915

Popova, L.I., Vitanov, P.K. and Antov, B.Z. (Central Inst. for Components, Bulgaria)
C-V AND I-V CHARACTERISTICS OF MIS STRUCTURES WITH PYROLYTIC SiO_2 AS DIELECTRIC. Thin Solid Films 23, no. 1, 15-22, Aug. 1974

The C-V and I-V characteristics of MIS capacitors with pyrolytically deposited SiO_2 as dielectric have been studied. Two features were found to be typical: a non-equilibrium lowering of the capacitance in the inversion mode, and a break in the original I-V characteristics. These effects appear after a given value of the negative voltage has been applied on the metal electrode. A qualitative treatment attributes the observed effects to the considerable conductance of the dielectric.

10916

Anderson, J.D. (Bendix Corp., Tech. Commun., Kansas City, Mo.)
READ-ONLY MEMORY IMPLEMENTATION STUDY. Rept. no. BDX 613-1053 (Rev.) Rept. no. PDO-6984754, Final Rept. 56 pp., Aug. 1974. AT(29-1)-613 USAEC

Electrically-alterable read-only memory (ROM) units have been incorporated into production test equipment. Production quantity costs of ROM's enable practical use of these large scale integrated (LSI) circuits in design of small-quantity equipment. One production testing is fully automated with six 4000-bit memories and twenty-two 256-bit memories as the control feature.

10917

Wiley, T.A. (Bendix Corp., Tech. Commun. Kansas City, Mo.)
EARLY PRODUCTION HISTORY ON HYBRID MICROCIRCUITS CONTAINING BEAM-LEAD SEMICONDUCTORS. Rept. no. BDX 613-1116 (Rev.), Rept. PDO 6984750, Topcial Rept. 28 pp., Aug. 1974. AT(29-1)-613 USAEC

Data from hybrid microcircuit prototype development and early coded electronic-switch production revealed that the beam-lead devices used in these hybrids are more reliable than the chip-and-wire active devices used in previous applications. Yields at the various processing levels were better than expected, and the overall microcircuit yield was more than 50 percent. Because of stringent quality requirements, this yield is considered acceptable, but is improving with cumulative production experience. Seven types of microcircuits for the coded switch are now being manufactured on a scheduled basis, and current problems are not sufficient to adversely affect production schedules.

10918

Smith, L.W. and Wilson, B.G. (Bendix Corp., Tech. Commun., Kansas City, Mo.)
AUTOMATIC TESTING AND HANDLING OF BEAM LEAD TRANSISTORS AND DIODES. Rept. no. BDX 613-1081, Technol. Spinoff Rept. 15 pp., Mar. 1974. AT(29-1)-613 USAEC

A Bendix designed system electrical tests all devices received in an as etched array, moves the good devices into an expanded array, and facilitates visual inspection. The system allows economical 100-percent testing and has greatly increased quality levels in next assemblies.

10919

Tapp, C.M. (Sandia Labs., Albuquerque, New Mex.) and Wiley, T.A. (Bendix Corp., Kansas City, Mo.)
A REVIEW OF HYBRID MICROELECTRONICS. Rept. no. SLA-73-1063, 59 pp., June 1974

The intent of this report is to survey Sandia and BKC experience with War Reserve (WR) hybrid microcircuits. General time scales for WR (stockpiled nuclear weapons) hybrid microcircuit development and use. The history of hybrid circuits will then be briefly reviewed. The presently evolving early production experience will be summarized. The technology advances now being developed and some future projections will then be discussed. Conclusions that can be drawn from the experience are also discussed.

19020

Knutson, R.E. (Sandia Labs., Hybrid Eng. Div., Albuquerque, New Mex.)
CERAMIC SUBSTRATES FOR HYBRID MICROCIRCUIT APPLICATIONS. Rept. no. SLA-73-0886, 82 pp., Sept. 1973. N74-19881

This report describes the various investigations undertaken and the test procedures developed to evaluate high density unglazed alumina substrates for use in thin film hybrid microcircuit applications. In addition to obtaining an increased understanding of substrate material, this project culminated in the publication of an official Sandia material specification. A fairly detailed explanation of certain aspects of the specification is also included.

10921

Stoner, C.L. (Sandia Labs., Mech. Design Div., Albuquerque, New Mex.)
PROTECTIVE CARRIER AND LOADING SYSTEM FOR BEAM LEAD SEMICONDUCTOR DEVICES. Rept. no. SLA-74-0052, 31 pp., Apr. 1974

The objective of this project was to develop a method for handling individual beam lead devices in production quantities for testing at high and low temperatures and to provide the capability for power burn-in without degrading the device. Prior methods for testing beam lead devices at high and low temperatures and burn-in under power was performed by removing the devices from the wafer array and bonding them to a circuitry. Only a small sample could be tested because once bonded, the devices could not be removed from the test circuitry.

10922

Holloway, P.H. and Long, R.L. (Sandia Labs., Supporting Technol. Div., Albuquerque, New Mex.)
EVALUATION OF PRE-BOND ETCHANTS IN HYBRID MICROCIRCUIT PROCESSING. Rept. no. SLA-73-1049, 66 pp., Nov. 1973

In order to remove a surface chromium oxide contaminant which interferes with thermocompression bonding, Sandia Labs. presently uses a pre-bond chemical etching step in its hybrid microcircuit (HMC) processing. To solve a production processing problem, five different etchants were tested to determine which most effectively increased the thermocompression bondability of HMC's. Two different potassium iodide plus iodine etches were shown to be marginal in restoring bondability. Limited data on ceric ammonium sulfate and sodium cyanide etchants indicated they could restore bondability. Extensive data demonstrated that a ceric ammonium nitrate (CAN) etchant restored the bondability of HMC's, did not change the surface topography, did not cause thin film deadhesion, and did not cause deleterious effects during accelerated aging tests. The incorporation of CAN as the pre-bond etchant in HMC processing was recommended.

10923

Hampy, R.E. and Wright. R.E. (Sandia Labs., Hybrid Eng. Div., Albuquerque, New Mex.)
PRELIMINARY PHOTOLITHOGRAPHIC PROCEDURES FOR HYBRID SUBSTRATES WITH CONDUCTIVE VIAS. Rept. no. SLA-73-0805, 26 pp., Sept. 1973

This memorandum describes several photolithographic procedures which were developed to provide conductive feedthrus or "vias" in hybrid microcircuits on 27 mil thick alumina substrates in order to provide an electrical connection(s) between the front and back metallized conductor layers. The vias are 25 mil diameter holes which have been punched in the alumina in the green state before firing. After puttering the tantalum nitride resistive layer on the front surface, chromium and gold are deposited on the front and back surfaces and in the holes by vacuum evaporation using a rotating planetary fixture. During the subsequent etching phases used to define the resistors and conductors on the top surface, the chromium-gold in the vias must be protected. Several photolithographic procedures have been developed to provide this protection and are described in the report. The most promising approach is based on laminating solid sheet photoresist on both surfaces.

10924

Lodi, R. (Sperry Res. Center, Sudbury, Mass.) and Dodson, W. (Sandia Labs., Albuquerque, New Mex.)
OPERATION AND RADIATION HARDNESS OF FULLY DECODED 16 x 16 MNOS - REPROM INTEGRATED CIRCUIT. Rept. no. SLA-73-7053, 12 pp.

This paper describes the operation and performance characteristics of a fully decoded radiation hardened 256-bit MNOS REPROM integrated circuit. Experimental data obtained after exposing the circuit to 10^6 rads total dose will be presented in conjunction with analysis which predicts the circuit behavior from the characteristics of the individual transistors used with the circuit.

10925

Bushmire, D.W. (Sandia Labs., Hybrid Eng. Div., Albuquerque, New Mex.)
DEVELOPMENT OF PRODUCTION DEFINITION AND ASSOCIATED PROBLEMS OF THE MC2305 HYBRID CIRCUITS. Rept. no. SLA-73-0806, June 1969-Dec. 1971, 24 pp., Sept. 1973

This report describes the Sandia procurement experience with the MC2305 thin film hybrid microcircuits. The MC2305 radar is a part of the MK3 arming, firing, and fusing system. These circuits use tantalum nitride as resistor material and aluminum as conductor material. The applique parts are chip-on-channel semiconductor devices and barium-titanate capacitors held down with epoxy. The interconnect system includes three-mil and one-mil aluminum wires with ultrasonic bonding. The discrete devices (capacitors, transistors and diodes) were procured from outside vendors by Collins Radio and assembled on the thin film substrate at Collins Radio. Specifications for the discrete devices and the completed hybrid circuit were originated at Sandia Labs.

10926

Sandia Labs., Matls. Analysis Div., Albuquerque, New Mex.
STUDIES OF Cr-Au THIN FILMS USED IN HYBRID MICROCIRCUITS. Rept. no. SLA-73-793, 32 pp., Sept. 1973. AT(29-1)-789

The capabilities of analytical techniques applied to the Cr-Au problem are described in terms of their applicability to the characterization of these and other films. The results and conclusions of this HMC system are then described in some detail.

10927

Bushmire, D.W. (Sandia Labs., Supporting Technol. Div., Albuquerque, New Mex.)
EFFECTS OF ELECTRICAL PROBING ON BEAM LEAD BONDING. Rept. no. SLA-73-943, 18 pp., Feb. 1974

This process evaluation was performed to determine the effect of electrical probing on beam lead bonding. Visual inspection of beam lead devices has shown that various amounts of physical damage to the gold plated beams occur during electrical probing. This report describes the results of beam lead bonding on devices that have received various amounts of physical damage on the beam due to electrical probing. The amount of device beam damage is related to the probe control rather than the number of times the devices are probed. It appears that 100% visual inspection is the most effective method of identifying "good" or "bad" beams after probing.

10928

Lemons, R.A. and Quate, C.F. (Stanford U., Microwave Lab., Standord, Calif.) INTEGRATED CIRCUITS AS VIEWED WITH AN ACOUSTIC MICROSCOPE. Appl. Phys. Letters 25, no. 5, 251-3, Sept.1, 1974

The images of a high-frequency bipolar transistor obtained with an acoustic microscope are compared with those of a differential interference optical microscope and a scanning electron microscope in order to illustrate that the acoustic microscope can be used in a reflection-type mode to obtain quality pictures of a surface containing integrated circuits.

10929

Learmer, L. and Smith, C.E. (Singer Co., Kearfott Div., Little Falls, N.J.) HIGHER LEVEL PACKAGING STUDY FOR AADC PROGRAM. Doc. no. Y254A064, Final Tech. Rept., Feb. 1972-Sept. 1974, 124 pp., Aug. 20, 1974. N00019-72-C-0270

An advanced prototype electronic packaging system, known as the "AADC Higher Level Package" has been designed and fabricated. The unit incorporates the features that are to be applied in the packaging of the All Applications Digital Computer (AADC). Characteristics of the Higher Level Package and its major elements such as the 146 pin zero insertion force, cam operated connector and the Basic Building Module (B^3M), which can retain a 3 inch diameter LSI wafer in a hermetic enclosure, are described.

10930

Anon.
AUTOMATED MASK ALIGNERS IN SEMICONDUCTOR MANUFACTURE. Circuits Mfg. 14, no. 5, 88-9, May 1974

In semiconductor device processes for integrated circuits and LSI, several successive photolithographic steps require accurate alignment of each mask on the silicon slice over the detail visible thereon from previous steps. Accuracy of masks and of the alignment operation has increased by over tenfold during the last decade. Using the best manual machings available at present, human operators meet these requirements with difficulty. Recently, newly available equipment performs the wafer-to mask alignment to better than one micron completely automatically. One such machine utilizes machine recognition targets put into the mask at the step-and-repeat level.

10931

Anon.
BREAKING CHARACTERISTICS OF LASER-SCRIBED WAFERS. Circuits Mfg. 14, no. 5 p. 76, May 1974

Wafer scribing already represents a major industrial application for lasers, and their importance to the electronics industry in this and other applications will continue to grow as manufacturing personnel develop more sophisticated techniques for using them. Two factors control scribing quality. 1) Bending stress applied to a scribed wafer causes local stress at the scribe line greater than that at points outside the kerf and the effects of the sharp notch. 2) For clean, reliable wafer cracking, stress enhancement must become so large that stress at the scribed line greatly exceeds the maximum yield strength of the material. But, simultaneously, stress at a point distant from the kerf must remain much less than the material's minimum yield strength.

10932

Anon.
BUYING CUSTOM LSI: A WELL-WRITTEN CONTRACT CAN KEEP YOU FROM GETTING BURNED. Circuits Mfg. 14, no. 8, 2 pp., Aug. 1974

Over the last few years, many commercial and industrial electronic system houses made major commitments to upgrade their product lines by using custom LSI circuits. In many cases commitments were not met, resulting in losses of millions of dollars. Understanding the typical problems in producing and procuring custom LSI integrated circuits can minimize such losses. A list of check points should be considered before deciding on an LSI vendor, such as: Design, Masks, Processing, Testing, Assembly and Final Test.

10933

Anon.
THIN FILMS AND SURFACE PREPARATION. Circuit Mfg. 14, no. 8, 2 pp., Aug. 1974

Hollow cathode cross-field sputtering provides the following benefits: 1) Surfaces may be irregular and the substrates may be thick. 2) Since the targets are not bonded to a holder users may exchange targets by single removal and replacement. Elimination of bonding permits almost 100% reclaiming of precious metals. 3) Anode gas bleed allows dc sputtering of reactive metals. 4) Process deposits material at high rates and produces coatings of good uniformity in thickness and resistivity and without gaseous inclusions. 5) Lower than conventional sputtering voltages make the process attractive for producing MOS and Schottky barrier devices, and any charge-couples devices very sensitive to soft X-ray radiation. 6) Substrate temperatures remain low, between 40-80°C. 7) Users of this type of equipment have reported 60-80% coverage of vertical walls. 8) Substrate rotation helps produce stress-free deposits. 9) Deposition efficiency equals approximately 22%.

10934

Anon.
FABRICATING MAGNETIC BUBBLE MEMORY OVERLAYS: SUBTRACTIVE ETCH FOLLOWS THREE METAL DEPOSITIONS. Circuits Mfg. 14, no. 8, p. 19, Aug. 1974

Making bubble memories economically requires an inexpensive method for fabricating bubble over lays. Such over lays must include all functions needed to generate, propagate, sense and annihilate magnetic bubble domains. IBM's overlay fabrication technique consists of three metal deposition steps followed by a subtractive etch. Evaporation of Ni-Fe onto a glass substrate in a dc in-plane magnetic field deposits a 200 A magnetoresistive film, the plating surface for subsequent electrodeposition steps. Portions of the film become sensors for the magnetic bubbles after the final etching.

10935

Anon.
CHECKING SEMICON CHIPS: TECHNIQUE ENDS THE NEED TO EYEBALL EACH AND EVERYONE Circuits Mfg. 14, no. 8, p. 16, Aug. 1974

Before capping, semiconductor chips generally undergo visual examination. Although this examination successfully screens out bulk surface defects, it is subject to human error and provides no means for discovering flaws not connected with surface irregularities. One alternative to visual inspection employs a laser to detect visible and invisible chip defects. When this laser scanning system photoexcites chips, individual fingerprint signals result. Each pulse of radiation from the laser photogenerated free electrons and holes in the chip. These carriers produce electrical signals at the terminals. Signals vary depending on the defects present.

10936

Anon.
ELECTRONIC MATERIALS PROCESSING IDEAS: FROM SUBSTRATES TO IC FABRICATION. Circuits Mfg. 14, no. 2, 58-9, Feb. 1974

The characteristics that different substrate materials offer the engineer (physical properties, adhesion mechanisms, dielectric constant and varieties of surface defects) are summarized. Different substrate materials currently used to produce thin film circuits are all a compromise of many different factors which must be considered in selecting the best substrate material. In general, the as-fired substrate seems the best compromise and is finding ever-increasing application. The advantages and disadvantages of the devices are described:

- PMOS vs BIPOLAR
- NMOS vs PMOS
- CMOS vs NMOS
- SOS vs CMOS, NMOS, PMOS

10937

Anon.
ADVANCES IN SEMICONDUCTOR DEVICE FABRICATION. Circuits Mfg. 14, no. 2, 7 pp., Feb. 1974. 1973 IEEE Electron Devices Meeting. Washington, D.C., Dec. 3-5, 1973

This synopsis covers such diverse topics as ion implantation, dielectric-junction isolation, computer-aided design techniques, simultaneous fabrication of vertical transistors, and other fabrication technologies.

10938

Anon.
DISPLAYS, HYBRIDS AND MANUFACTURING TECHNOLOGY. Circuits Mfg. 14, no. 7, 5 pp., July 1974

An outline is given of the advantages of the different display technologies and also a description of trends visible in today's display market. Listed in this article are the following subjects of discussion:
1) Liquid crystal watch displays.
2) LED's for the future trends in LED technology
3) Standards for hybrid microcircuits
4) Manufacturing circuitry
5) Making LSI circuits with a thick film multilayer process
6) Simplifying hybrid fabrication
7) Fabricating reproducible thick film resistors
8) Hybrids - the tuning problem
9) Materials for better hybrids
Proponents of the different display techniques all maintain that their devices will make the breakthrough into mass use, with tremendous progress just around the proverbial corner. Only time will tell just which one will dominate.

10939

Small Precision Tools, San Rafael, Calif.
SEMICONDUCTOR BONDING HANDBOOK. 1974

An indepth discussion of bonding process and bonding tool parameters is presented. A detailed analysis of proper bonding techniques and common bonding faults is performed. The reliability aspects of various bonding techniques and materials is illustrated.

10940

Lin, H.C. and Chawla, A.S. (U. of Maryland, Dept. of Elec. Eng., College Park, Md.)
HIGH DENSITY MEMORY. Final Rept., Apr. 1972-Dec. 1973, 64 pp., 1973. AD 781 919. N00014-67-A-0239-0022

MNOS capacitors have been fabricated which involved the setting up of equipment for MNOS processing. Circuits for using such capacitors have been designed. The fabricated capacitors have been evaluated and their characteristics have been found promising for their use in the non-volatile memory. An MNOS capacitive memory structure has been designed. In particular a design of an 8 x 8 memory matrix has been completed. This design includes mask making for the various fabrication steps like diffusion epitaxy and aluminization. Fabrication of the MNOS 8 x 8 matrix memory is underway.

10941

Koike, S. and Kambara, G. (Matsushita Electronics Corp., Semiconductor Group, Res. Lab., Takatsuki, Osaka, Japan)
THE OPTICAL WRITING OF MNOS MEMORY WITH Au DEEP TRAPS. Solid-State Electronics 17, no. 9, 994-6, Sept. 1974

Recently, optical properties of nonvolatile semiconductor memories, using a principle of the photo-injection of carriers through deep traps in insulating layers, have generated much of the interest in applications to optical input pattern memories. In the case of the MNOS memory, it has been known that the deep traps distribute at the silicon dioxide-silicon nitride interface and play an important role in the operation mechanism. Unfortunately, their operation has been limited to the high energy wave length region such as ultraviolet light. However, the possibility of the optical operation of the MNOS memory in the low energy wave length region was reported recently. During the course of an investigation of the MNOS memory, we found a fact that in addition to above deep traps, another kind of deep traps present at the silicon-silicon dioxide interface as well as in the depletion region also affect the characteristics of the MNOS memory. By the use of Au-diffusion in order to introduce the deep traps in the regions, a new type of photosensitive MNOS memory operating in the visible and infrared light regions was obtained.

10942

Szekely, G.S. (System Evaluation Inc., Los Angeles, Calif.)
RELIABILITY ASSURANCE CRITERIA FOR FILM-HYBRID MICROCIRCUITS. pp. 395-400. 1973 Symposium on Reliability in Electronics. Budapest, Hung., Nov. 13-16, 1973

A brief overview is given of the particulars affecting reliability assurance for thick-film and for thin-film hybrid integrated circuits. Selected aspects are discussed, such as: specifications for hybrids, a three-tier specification system, pre-production checklist for custom hybrids, technological details and precautions for stability of laser-trimmed film resistors, evaluation of incoming batches of thick-film inks and pastes, internal visual inspection reject criteria for completed hybrid circuits, hallmarks of a desirable epoxy adhesive for attachment, and status of industrial professional standardization activities in the technical areas of hybrid microcircuits.

10943

Armstrong, W.E. and Tolliver, D.L. (Motorola Semiconductor Prod. Div., Phoenix, Ariz.)
A SCANNING ELECTRON MICROSCOPE INVESTIGATION OF GLASS FLOW IN MOS INTEGRATED CIRCUIT FABRICATION. J. of the Electrochem. Soc. 121, no. 2, 307-10, Feb. 1974

It has been shown that an increase in the concentration of phosphorous in a vapor-deposited oxide can change the viscosity-temperature characteristics of the film to cause "flow" at temperatures as low as 1000°C. In addition, this oxide flow can be further enhanced by annealing the glass in oxygen or steam ambients rather than in inert gases. Finally, the technique was shown to improve step profiles as it was applied to: (i) steps from poly silicon lying under the phospho-silicate glass film, (ii) thick oxide steps, and (iii) "contact window" openings.

10944

Herlir, M.A., Weiss, H.G. and McWhorter, A.L. (MIT. Lincoln Lab., Lexington, Mass.)
ADVANCED ELECTRONIC TECHNOLOGY.
Rept. no. ESD-TR-72-237, Quart. Tech. Summary, May 1-July 31, 1973, 18 pp., Aug. 15, 1973. AD 768 394
Rept. no. ESD-TR-73-262, Quart. Tech. Summary, Aug. 1-Oct. 31, 1973, 17 pp., Nov. 15, 1973. AD 774 451
Rept. no. ESD-TR-74-209, Quart. Tech. Summary, Feb. 1-Apr. 30, 1974, 17 pp., May 15, 1974. AD 781 380. F19628-73-C-0002

These reports review progress on Data Systems, Speech Understanding Systems, Seismic Discrimination, Educational Technology Program, Radar Measurements, FAA Interactive Graphics, and ATC Surveillance/Communication Analysis and Planning.

10945

Edwards, A.J. (U.S. Army Matl. Command, Harry Diamond Labs., Washington, D.C.)
THIN-FILM HYBRID MICROCIRCUITRY. PART I. BOXCAR CIRCUIT FOR A CURRENT HDL FUSE SYSTEM. Rept. no. HDL-TM-73-10, Tech. Mer., 22 pp., May 1973.
AD 768 091

A thin-film hybrid version of the boxcar circuit for a current HDL fuze system was developed. A single circuit was laid out and a computer program written to generate 4 identical circuit patterns using a computer-tape driven plotter. The resistor-conductor patterns were produced by standard photolithographic techniques, and discrete chip devices (diodes, capacitors, and transistors were attached with conducting epoxy cement. Connections to the chip devices and to lead-out pins were made by thermocompression wire bonding to complete the circuit fabrication. Preliminary electrical tests indicated acceptable insertion losses of approximately 0.6 dB and high-frequency roll-off points in the expected frequency range.

10946

Morris, H. (U.S. Navy, Nav. Ordnance Lab., Silver Spring, Md.)
PROPOSED HYBRID MICROCIRCUIT FLAT PACKAGE DESIGNS. Rept. no. NOLTR 73-76, 20 pp., Apr. 4, 1973. AD 761 153

This report describes a need for a new type of multi-lead flat package to house hybrid microcircuits for use in application with connectors developed under the U.S. Navy Standard Hardware Program. The problem is that several types of edge-connect or leadless packages compatible with similar types of connectors are being fabricated by the industry to house integrated circuits or large-scale integration devices, but there are none available to package hybrid microcircuits. In this report several designs of multilead hybrid microcircuit ceramic flat packages are described, and design models are presented.

10947

Schafft, H.A. (U.S. Dept. of Commerce, Natl. Bur. of Standards, Inst. for Appl. Technol., Electronic Technol. Div., Washington, D.C.)
SEMICONDUCTOR MEASUREMENT TECHNOLOGY: ARPA/NBS WORKSHOP II. HERMETICITY TESTING FOR INTEGRATED CIRCUITS. Rept. no. NBS-SP-400-9, Final Rept., 36 pp., Dec. 1974

The purpose of the workshop was to define more clearly some of the problems of hermeticity testing, to outline NBS efforts and plans in this area, and to encourage the coordination of efforts in hermeticity test development and standardization.

10948

Abshire, D.J. (U.S. Air Force, Wright-Patterson AFB, Air Force Inst. of Technol., Ohio)
DESIGN AND FABRICATION OF A VERSATILE TESTING SYSTEM FOR MNOS. Rept. no. GE/EE/74-22, AFIT Thesis, 93 pp., June 1974. AD 785 131

The versatile testing system for MNOS is a programmable generator that generated wavetrains necessary to measure writing characteristics, memory retention, and degradation information. It is capable of generating both positive and negative pulses of different amplitudes and widths. The generator also has the capability of increasing the widths of predetermined pulses after each wavetrain has been generated, and halting operation when a predetermined width has been reached. It functions as an independent unit; once programmed it is capable of generating the required wavetrains and measuring the threshold voltage of a test device without assistance from any external device.

10950

Coverley, G.P. and Behera, S.K. (Micro-Systems Internatl. Ltd., Ottawa, Ontario, Can.) and Colbourne, E.D. (Bowmar Can. Ltd., Ottawa, Ontario. Can.)
RELIABILITY OF MOS LSI CIRCUITS. Proceedings of the IEEE 62, no. 2, 244-59, Feb. 1974

MOS LSI circuits share many of the reliability problems associated with discrete semiconductors and medium-scale integrated circuits. However, because of the added complexity, larger chip size, and higher densities of MOS LSI circuits, different approaches are needed. A close working relationship between the designer, manufacturer, and user--the reliability triangle--is needed to generate the manufacturing controls, testing, methods, and reliability assessment procedures and to optimize the performance and reliability of the MOS LSI circuits. Using this approach, the MOS LSI circuit, having more functions per external connection, can provide a more reliable system than one of equal complexity, based on discrete devices or less complex integrated circuits. Specific areas of reliability such as pattern sensitivity, manufacturing controls, assembly, packaging, and electrical testing have also been discussed.

10951

Hinman, P.W. and Thoennes, W.P. (Rockwell Internatl., Anaheim, Calif.)
COMPUTER TECHNIQUES FOR ADVANCED INERTIAL SYSTEMS. Rept. no. AFAL-TR-74-237, Rept. no. C74-459/201, Final Rept., Apr. 1972-June 1974, 225 pp., Oct. 1974. F33615-72-C-1674

This document describes the requirements, design, fabrication and evaluation of a processor configured for a micronavigation (MICRON) system. The purpose of this advanced development effort was to develop the processing and input/output elements which fulfill the unique MICRON requirements consistent with the following goals: (1) low power, (2) small size, (3) high reliability, and (4) low cost. The fundamental technical advancements and new systems packaging concepts derived from the development must also be applicable to future avionics equipment designs.

10952

Buss, D.D. and Bailey, W.H. (Tex. Instr. Inc., Dallas, Tex.)
INVESTIGATION OF SEMICONDUCTOR CHARGE DEVICES. Part II. Rept. no. RADC-TR-73-259, Final Rept., 92 pp., Oct. 1973 AD 772 638. F30602-73-C-0027

This report details the design, fabrication, and testing of the breadboard model of a binary spread spectrum receiver. In determining how to implement the breadboard, both charge coupled devices (CCD's) and bucket brigade devices (BBD's) were evaluated. The later was selected because the design goals could be met using BBD's which are less expensive and easier to fabricate than CCD's. In determining what type of filter to construct, chirp was selected for two reasons: (1) Chirp has certain theoretical advantages over pn. (2) Chirp is more general than pn in the sense that weighting coefficients in a pn filter have unity magnitude, whereas chirp weighting coefficients are arbitrary.

10953

Opp, F., Colvin, W. and Allensworth, J. (Tex. Instr. Inc., Radar and Digital Systems Div., Dallas, Tex.)
RELIABLE ADVANCED SOLID-STATE RADAR. Rept. no. AFAL-TR-74-321, Rept. no. DM74-10-10, Final Rept., Aug. 15, 1969-Sept. 15, 1974, 326 pp., Jan. 15, 1974. F33615-70-C-1029

This report is a summary of the design, manufacture, and testing of a 1648-element, active, phased-array, multimode radar for airborne use. This test-bed provided actual application of three emerging technologies in microwave large integrated circuits, large/medium scale integration, and surface wave acoustical delay lines. In addition, this program supplied the opportunity for advancing the state-of-the-art in volume production of a high performance, reliable, microwave integrated circuit transceiver module. The Reliable Advanced Solid-State Radar (RASSR) was modeled after currently available radars in performance and modes of operation. A system description is given and special design considerations are outlined for the signal generator, receiver processor, computer, RF and DC distribution, mechanical and thermal aspects, maintainability, and reliability. The active antenna, transmit/receive module is described according to functional blocks with nominal performance requirements given. Various levels of automation of RF equipment in the manufacturing test facility is noted.

10954

Rockwell Internatl., Autonetcis Div., Anaheim, Calif.
RELIABILITY OF DEPOSITED GLASS. Rept. no. C74-281.10/201, R&D Monthly Status Rept., 7 pp., Dec. 1974. F30602-74-C-0160

This status report includes the results from the hermeticity tests which were completed on all the test samples. Glassivation layer breakdown voltages for three tested devices have been added to the characterization study and an update of tests performed per device is presented.

10955

Siekanowicz, W.W., Huang, H.C. and Paglione, R.W. (RCA Corp., RCA Labs., David Sarnoff Res. Center, Microwave Technol. Center, Princeton, N.J.)
ALUMINUM OXIDE PASSIVATION OF ELECTRON-BEAM-SEMICONDUCTOR SILICON DIODES. Interim Tech. Rept., 30 pp., Nov. 1, 1973. AD 772 101. N00014-73-C-0020. N00014-73-C-0111

DC and rf measurements have shown that beam-evaporated aluminum oxide constitutes a highly promising material for passivation of electron-beam-semiconductor targets. Aluminum-oxide-passivated targets are characterized by reverse breakdown voltages that range from 80% to essentially the full breakdown value and reverse leakage currents that are less than one micro-ampere. A life of 2600 hours was demonstrated on an aluminum-oxide-passivated target at a current gain of 2200, a beam voltage of 12 kilovolts, power and current densities of 41.5 watts and 0.82 amperes per sq. mm, respectively, on a 0.012-inch active diameter.

10956

Carnes, J.E., Cope, A.D., Rockett, L.R. et al. (RCA Labs., Princeton, N.J.)
EFFECTS OF RADIATION ON CHARGE-COUPLED DEVICES. Rept. no. AFCRL-TR-74-0276, Rept. no. PRRL-74-CR-35, Sci. Rept. no. 1, Sept. 25, 1973-Mar. 24, 1974, 56 pp., Aug. 1974. F19628-74-C-0080

The unique properties of charge-coupled devices (CCD's) make them very useful for several applications. These include imaging and memory applications as well as signal processing uses, such as analog delay lines, filters, correlators, etc. In some applications the devices may be exposed to high energy radiation which could affect CCD performance. The objective of this program is to investigate and improve the radiation tolerance of CCD's. To achieve this goal, we have studies the effects of radiation on surface channel CCD shift registers to establish both the nature of the radiation effects and of present day (unhardened) CCD technology.

10958

Loeb, W.E. and White, C.E. (Union Carbide Corp., Bound Brook, N.J.)
PARYLENE FOR CONFORMAL INSULATION. pp. 228-39. Proceedings of the Technical Program. 1968 National Electronic Packaging and Production Conference. Long Beach, Calif., Jan. 30, 31, 1968, Feb. 1, 1968, New York City, N.Y., June 4-6, 1968

A new polymer which is capable of being formed in extremely thin films, has been developed. "Parylene", the new material is deposited from the vapor phase by a process which in some respects resembles vacuum metallizing. Unlike vacuum metallization, however, which is conducted at pressures of 10^{-5} torr or below, the parylenes are formed at pressures around 0.1 torr, actually 50 tc 100 microns. The summarization of the physical, electrical, and thermal properties of the different parylenes are presented in this article.

10959

Simons, M. (Res. Triangle Inst., Res. Triangle Park, N.C.)
TRANSIENT SURFACE DAMAGE. Rept. no. 43U-812, Final Rept., Dec. 1, 1972-Dec. 31, 1973, 84 pp., Jan. 1974. AD 782 285. N00014-73-C-0236

This report describes the results of a study of transient surface damage phenomena in contemporary MOS and CMOS devices following pulsed radiation exposure. Measurements made on individual N- and P- channel transistor structures between 10^{-4} sec and 10^{3} sec after irradiation show that there are widespread variations in radiation sensitivity and space charge annealing behavior among samples prepared by different processes and by different manufacturers. Response data for devices fabricated on bulk silicon-on-sapphire (SOS) substrates and for various SiO_2 and Al_2O_3 gate insulators are compared and discussed. The effects of radiation-induced charge in the sapphire substrate of an SOS device are explored.

10960

Mok, T.D. and Salama, C.A.T. (U. of Toronto, Dept. of Elec. Eng., Ontarion, Can.)
A CHARGE-TRANSFER-DEVICE LOGIC CELL. Solid-state Electronics 17, no. 11, 1147-54, Nov. 1974

A logic scheme capable of performing AND-OR logic functions using charge-transfer devices is presented in this paper. Applications of the logic cell are discussed. A half-added, a 'flip-flop', a majority logic gate, an analog-to-digital and a digital-to-analog converter are obtained by extending or modifying the basic scheme. An integrated MOS BBD realization of the AND-OR logic cell is described in detail. Experimental results are presented and shown to be in agreement with theoretical calculations

10961

Flassayer, C., Morenza, J.L., Martinez, A. et al. (Laborstoires d'Automatique et d'Analyse des Systems du C.N.R.S., France)
SWITCHING PHENOMENA AND MEMORY EFFECTS IN N-TYPE METAL SILICON SCHOTTKY DIODES. Third European Solid State Device Research Conference. Munich, Germany, Sept. 18-21, 1973. N74 17939

This paper will describe multistate memory phenomena observed on silicon Schottky contacts. This type of phenomena has already been observed on a large variety of heterojunctions, essentially made from compound semiconductors. More recently several investigators, have reported bistable behavior on silicon devices. These offer, of course, the important potential advantages to be more compatible with integrated circuits.

10963

Youngberg, D.A. and Lenhardt, B.W. (Bendix Corp., Kansas City, Mo.)
CHARACTERIZATION OF THERMOCOMPRESSION BONDING PARAMETERS FOR BEAM-LEAD BONDING. Rept. no. BDX 613-1175 USAEC.

Thermocompression (TC) Bonding is a technique used to weld two similar materials by application of heat and pressure for a specific time. To obtain reliable, consistent beam-lead attachment by TC bonding, each bonding parameter value must be known and controlled. TC bonding schedules are developed to determine parameter boundary values that depend on the fundamental physics of the bonding process. This necessitates thorough TC bonder characterization (definitions of limits). This paper discusses the practical considerations of beam-lead wobble-tool bonding and describes the techniques used to characterize bonding tool temperature, work-stage temperature, bond time or wobble speed, and bond force.

10964

Onyshkevych, L.S., Shahbender, R., Tomkiel, S. et. al. (RCA Labs., Princeton, N.J.)
DESIGN,CONSTRUCTION, AND TESTING OF A MAGNETIC BUBBLE MEMORY CHIP. RCA Rev. 35, no. 2, 216-33, June 1974

A 34-bit cylindrical domain (bubble)memory chip with complete functions for read, write, erase and store operations was designed, fabricated and tested. Description of the design and fabrication steps and experimental test data are presented. The ultimate viability of the bubble memory concept is still to be established and will in part be determined by progress achieved with competing approaches.

10967

Lindberg, F.A. (Westinghouse Defense and Electronic Systems Center, Systems Dev. Div., Baltimore, Md.)
HARDENED HYBRID SEMICONDUCTOR PACKAGES. Rept. no. HDL-TR-216-1, Rept. no. 74-0303A, Final Rept., June-Dec. 1973, 81 pp., May 1974. AD 783 432.
DAAG39-73-C-0216

The overall objective of the program was to develop a hardened hybrid packaging technique. The package and interconnections rather than the integrated circuit chips were the object of interest as far as failure due to radiation was concerned. A constraint was placed on this program to develop a process which was adaptable to mass production with high yields.

10969

Goldenberg, H.R. (Polytechnic Inst. of N.Y., Brooklyn, N.Y.)
INTEGRATED CIRCUIT RELIABILITY PREDICTION AND COMPLEXITY MODELS. Rept. no. PINY EE/EP-74-004, Rept. no. EER 103, Sci. Rept.. 119 pp., June 1973. AD 781 330.
N74-32707. N00014-67-A-0438-0013

A method for calculating the average hazard rate for a catastrophic failure test using the test duration, the number of failures, and the sample population, the failure rate can be approximated by the number of failures divided by the product of the sample population and the test duration. An equivalency criterion is developed that allows a transformation between hazard model shapes. The model shapes examined in detail are the constant, the Weibull, and the piecewise linear shapes. It is shown that significant errors in reliability can result from assuming a constant hazard. The principal failures modes of digital integrated circuits are examined, and they are related to the complexity of the circuit by qualitative arguments.

10970

Vaccaro, J. (U.S. Air Force, Griffiss AFB, RADC, Rome, N.Y.)
SEMICONDUCTOR RELIABILITY WITHIN THE U.S. DEPARTMENT OF DEFENSE. Proceedings of the IEEE 61, no. 2, 169-84, Feb. 1974

This paper describes the standardization and specification approach used by the U.S. Department of Defense to procure reliable semiconductor devices. A brief discussion of the background and rationale leading up to the present approach, and some of the experience upon which it was based, is presented. Related reliability studies and other activities necessary to assure effective implementation of this approach are summarized. The emphasis in the discussion of these studies is on identification of failure modes and mechanisms and the use of this information in device specification, qualification, reliability testing, and reliability prediction. Major consideration is given to microelectronic-device reliability problems.

10971

Reynolds, F.H. (Post Office Telecommun. Hdqtrs., Res. Dept. London, Engl.)
THERMALLY ACCELERATED AGING OF SEMICONDUCTOR COMPONENTS. Proceedings of the IEEE 62, no. 2, 212-22, Feb. 1974

The rising interest in the use of elevated temperatures to accelerate the life of semiconductor components warrants a review of the mathematical basis of the technique. Starting from the four reliability probability functions, the log-normal density function is featured showing how the temperature dependence of the associated cumulative failure function leads to a prediction of the component median life under service conditions through the construction of Arrhenius lines. Both steady and incrementally raised temperatures can be employed to gather test data, the latter, the step-stress method-involving a correction procedure. The analysis is illustrated by its application to test results from bipolar and MOS transistors.

10972

Anon.
PROCEEDINGS OF THE TECHNICAL PROGRAM. 1974 NATIONAL ELECTRONIC PACKAGING AND PRODUCTION CONFERENCE. 248 pp., Anaheim, Calif., Feb. 26-28, 1974, New York, N.Y. June 18-20, 1974

Sessions:
- I Selected Special Processing Information Concerned with Printed Wiring Manufacturing Technology
- II Effective Methods of Selecting Automated Digital Test Equipment
- III Relating Reliability to Process Control
- IV Selection Criteria for Automated Analog Test Equipment
- V Soldering-Processes and Mechanization
- VI Automation Techniques for Printed Circuit Production
- VII Coil Winding Symposium

CONNECTOR SYMPOSIUM

Sessions:
- I Aerospace Connections
- II Printed Wiring Boards Interconnecting Techniques
- III New Concepts in Interconnection Techniques

10973

Alonso, R.L. (Adar Assoc., Inc., Cambridge, Mass.)
TESTING RAMS FOR THE USER--DEVICES, BOARDS AND SYSTEMS. pp. 38-44. Proceedings of the Technical Program. 1974 National Electronic Packaging and Production Conference. 248 pp., Anaheim, Calif., Feb. 26-28, 1974, New York, N.Y. June 18-20, 1974

Semiconductor RAM devices are rapidly becoming a major factor in the electronic industry, and most new designs use semiconductor RAMS, rather than core. Testing RAMS focused for a long time on testing devices, rather than on boards or systems. A second phase, now quite visible in early 1974, is the shift from testing devices to testing boards. One might suppose that exhaustive device testing might eliminate or greatly reduce the need for board testing, but this turns out not to be so for several reasons. First, board assembly always implies potential physical damage to components, or solder splashes, bent pins, wrong component insertions. Second, and more important in the case of RAMS, the board's electrical environment is often far from a nominal design environment. What this means for testing is that it is necessary to test the combination of device-in-board to guarantee performance.

10974

Anon.
HOW MUCH WILL SOS HELP? Electronics 48, no. 2, 66-7, Jan. 23, 1975

Time is running out on the chances of silicon on sapphire to become the next high-volume technology for digital circuits. Once considered the thin-film technique that would supplant bulk silicon, SOS may have to be content in a niche reserved for special applications such as military systems and in-house process control.

10975

Anon.
HYBRID BONDING AND INTERCONNECTIONS. Circuits Mfg. 14, no. 2, 8 pp., Dec. 1974

When exposed to elevated temperatures, during burn-in for example, aluminum to gold ultrasonic bonds undergo a degradation in strength. After experiencing some problems with low strength bonds on completed hybrid devices, a testing program was set up to provide suitable degradation data on aluminum to gold ultrasonic bonds. Other hybrid bonding techniques and bond failures, including those resulting from abrasive trim overspray, are also presented and analyzed.

10976

Hayashi, I.
GaAs LASERS DIODES WILL BE READY FOR OPTICAL COMMUNICATION IN THE NEAR FUTURE. NEC Res. & Dev., no. 33, pp. 1-14 Apr. 1974

The recent breakthrough in the operational life of GaAs heterostructure lasers should bring practical applications of these devices in the near future. Lasers with a stripe geometry have been operated in cw at diode currents near 100 milliamperes and have given coherent light outputs of 10 milliwatts in single mode. A combination of this GaAs laser with the low loss glass fiber, SELFOC, has proven to be an attractive optical communication system. A new package combining GaAs lasers will replace the ordinary gas or solid lasers in a variety of applications. They will also open up new fields of application because of their compactness, ease of operation and low prices.

10977

Nagao, H. and Katayama, S.
SILICON IMPATT DIODE DEVICE INCORPORATING A DIAMOND HEAT SINK. NEC Res. & Dev., no. 35 pp. 67-76, Oct. 1974

High power silicon IMPATT diodes with a diamond heat sink have been developed for use in 6 GHz through 22 GHz. Power outputs of these diodes are 2.2 watts (7 GHz band) 1.8 watts (10 GHz band), 1.2 watts (15 GHz band) and 0.8 watts (20 GHzband). When the operating junction temperature is kept below 180°C, the failure rate of these diodes is expected to be less than 1,000 FIT. Device design, construction, fabrication methods, thermal and oscillation characteristics and reliability of the IMPATT diode will be outlined.

10978

Nakamura, K. and Kamoshida, M.
ELECTRICAL CHARACTERISTICS OF ION-IMPLANTED p-CHANNEL MOS TRANSISTORS. NEC Res. & Dev., no. 33, pp. 29-37, Apr. 1974
J. of Appl. Phys. 45, no. 1, 334-40, 1974

In this report, acceleration-energy, gate-oxide-thickness, and implantation-dose dependences of the threshold voltages of ion-implanted p-channel MOS transistors will be compared with the values obtained by using Swanson and Meindl's step-function-approximation. Other device characteristics, such as "gain" terms and breakdown voltages, will be discussed. The ion-implanted device stability investigated by BT treatments will be described. Anneal temperature dependence of the device stability will also be shown. Finally, static transfer characteristics of the p-channel enhancement-depletion inverter will be indicated, together with the calculated results obtained using the theory presented.

10979

Okabayashi, H. and Shinoda, D.
RANGE AND STANDARD DEVIATION OF ION-IMPLANTED PHOSPHORUS AND BORON IN SILICON. NEC Res. & Dev., no. 35, pp. 10-4, Oct. 1974

The projected range, R_p, and the projected standard deviation, ΔR_p, of 50-260 keV ^{31}P ions implanted in silicon have been measured by the C-V technique. The measured R_p values satisfy the experimental relation, R_p=1.1μm/MeV, reported for higher energy implantations. The measured ΔR_p values at lower energies are larger than the theoretical predictions. The difference shows a tendency to decrease as the ion energy increases and becomes zero at between 200 and 300 keV. The lateral standard deviation, ΔY, can also be measured by the C-V technique in combination with the oblique implantation technique. The measured ΔY values for both ^{31}P and ^{11}B at ion energies studied here are in good agreement with the theoretical predictions.

10980

Raytheon Co., Equip. Div., Equip. Dev. Labs., Wayland Lab., Wayland, Mass.
RELIABILITY FAILURE RATE/MODE HANDBOOK SECTION 3.1. INTEGRATED CIRCUIT FAILURE RATES. Tech. Std. no. 2987, Partial Issue, 82 pp., Aug. 1971

This document includes a set of tables giving the experienced field failure rates, of integrated circuits, a prediction procedure for hybrid microcircuits and a set of graphs giving the failure rates of IC's as a function of temperature obtained primarily from laboratory tests of IC's at elevated temperatures. The basic source for this handbook is the Reliability Analysis Center of RADC operated by the IIT Research Institute.

10981

Williams, R., Goedertier, P.V. and Knox, J.D. (RCA Labs., Phys. Electronics Res. Lab., Princeton, N.J.)
LASER SCANNING AS A TOOL FOR TESTING INTEGRATED CIRCUITS. RCA Eng. 20, no. 1, 76-8, June/July 1974

Laser scanning can be used to test integrated circuits for defects. Each functioning element is probed by sequentially scanning the entire circuit with the focused spot from a laser beam. The method is described and some results are shown for a simple circuit.

10982

Rodgers, III, R.L. (RCA Labs., Electro-Optic Prod., CCD Mfg. and Eng., Lancaster, Penn.)
CHARGE-COUPLED IMAGER FOR 525-LINE TELEVISION. RCA Engr. 20, no. 1, 79-82 June/July 1974

The operation and performance parameters are described for a CCD image sensor having 512x320 elements (163,840 individual storage sites). The device is designed and fabricated for use in the standard 525-line television system. This solid-state imager is capable of performance superior to that of camera tubes with regard to signal-to-noise ration, freedom from lag, and absence of microphonics. Additional features incude its small size, light weight, low power, and precision image characteristics.

10983

Anon.
HOW MANY BONDS WILL ULTRASONIC WEDGES MAKE? Circuits Mfg. 14, no. 9, 82-4, Sept. 1974

Results from a lengthy test program performed by a major manufacturer of MOS devices were reported. Tests in the program sought the following objectives:

- To record the number of bonds each wedge produced,
- To determine failure modes and reasons for damage by photographing wedges that show different stages of wear,
- To develop preventative and wedge care techniques, and
- To fix conclusively the economics of wedge use versus overall circuit cost.

10984

Anon.
FLIP CHIPS ARE JUMPING OVER BEAM LEADS. Circuits Mfg. 14, no. 9, 80-1, Sept. 1974

Manufacturers can easily automate flip chip hybrid circuit assembly. The absence of projecting, entangling leads on the flip chips permits the first step in automatic assembly: vibratory bowl feeding. Symmetrical geometry, straight sides and solder bumps allow the transfer mechanism to grasp each chip simply with the correct side up. Proper orientation may come from interpreting a symbol on the plain side of the chip or an electrical reading of the circuit side of the chip. Smooth functioning of these three operations puts a manufacturer well on the way to high yield rates.

10985

Etzbach, A.L.
CONFORMAL COATINGS: MATERIALS AND TRENDS. Electronic Packaging and Production 14, no. 8, 5 pp., Aug. 1974

Properties of conformal coating materials used on PC boards and components are continually changing to meet user demands. Nationwide trends toward more pollution control, greater concern for employee safety and increasing inflation have been a big factor in the formulation of materials which are more flame-resistant, less toxic and more easily repairable. Since there is no perfect conformal coating a general comparison of advantages and limitations for the seven listed materials will be helpful. These material types can be used for commercial or military applications, although new fluorocarbons have not yet been submitted for military approval.

10986

Clelford, A.P. and Payne, J.R. (Microsystems Internatl. Ltd., Ottawa, Can.)
PACKAGE DEVELOPMENT FOR A LARGE MULTICHIP ARRAY. Electronic Packaging and Production 14, no. 9, pp., Sept. 1974

A multiplicity of memory circuits can be packaged on PC's by using either plastic or hermetic DIP's. An alternative is to use the hybrid approach in the form of a multi-chip array. The most efficient assembly of an MCA package can be achieved through the use of beam-lead or flip-chip devices. The beam-lead approach was taken since it is most compatible for thermocompression bonding onto thin-film gold metallization, which was used for bonding layer. More importantly, it gave excellent die-replacement characteristics.

10987

Belland, R. (Tex. Instr., Dallas, Tex.)
LASER SCRIBING AND DRILLING OF CERAMIC SUBSTRATES. Electronic Packaging and Production 15, no. 1, 56-8, Jan. 1975

Three techniques used for substrate separation are: prescoring, sawing, and laser scribing. The latter has proved to be an effective tool when care is taken to minimize the degrading properties of slag. The high-powered YAG and CO_2 lasers have evolved from research instruments to useful engineering and manufacturing tools. There are both advantages and limitations in using YAG and CO_2 lasers as applied to ceramic scribing and hole drilling, and various problems are encountered. Basic guidelines for minimizing or eliminating these problems are discussed.

10988

Anon.
IS PHOTORESIST BAKING GOING HARD AND SOFT WITH INFRARED? Circuits Mfg. 14, no. 11 7 pp., Nov. 1974

Some semiconductor device manufacturers are softbaking with infrared (IR) as an energy source. A few have gone to IR hardbaking. Three companies were interviewed to find out more about this trend. All three point fingers at photoresist manufacturers for not investigating IR baking thoroughly. Consequently, they say, recommendations by resist suppliers often lead to processing problems that prevent more widespread adoption of IR baking by the industry.

10989

Anon.
TESTING SEMICONDUCTORS: BATTLING AN ECONOMICS OCTOPUS: WHAT PART DO YOU ATTACK FIRST? Circuits Mfg. 14, no. 11 6 pp., Nov. 1974

Whether you're manufacturer or a user of LSI and memory devices, testing is synonymous with reliability. On the other hand, the level of testing you choose to perform reflects directly upon your profit/loss column. Too much testing leads to prohibitive costs; too little to unacceptable reject rates. Although a single best solution to the testing dilemma seems unlikely, these papers, may help show you a way toward more effective, economical testing.

10990

Anon.
PLASMA ETCHING: WHAT IT IS, WHAT IT DOES AND WHAT IT DOESN'T DO FOR IC MANUFACTURERS. Circuits Mfg. 14, no. 10, 4 pp., Oct. 1974

In comparison to wet chemicals, plasma etching may offer semiconductor manufacturers a dream technique. Whereas, every wet etching process requires rinsing and drying after each operation, plasma etching does not. Wet etching often requires a glass coating between the nitride layer and the photo resist to prevent liftoff; but plasma etching does not. In fact, according to some reports, photoresist does not lift during plasma etching. The process also avoids the hassles of getting rid of spent reagents or toxic fumes. On thin films, even when parts remain in the plasma etching chamber 4 times longer than necessary, less than 0.25 micron undercut occurs. Experimentally, plasma etching can produce mask apertures as small as 0.1 micron; and it routinely can give 1 micron results, depending on photoresist. But plasma techniques currently available in some marketed equipment cannot do certain crucial jobs required in the industry for example, etching aluminum and gold; or etching SiO_2 and stopping at the silicon underlayer. In addition, uniformity of etch still poses problems for some uses and some makes of equipment. This report describes the mechanisms at work when plasma etches, and delineates some of its advantages and disadvantages as a production technique.

10991

Loranger, J.A. Jr. (Loranger Mfg. Corp. Warren, Pa.)
THE CASE FOR COMPONENT BURN-IN: THE GAIN IS WELL WORTH THE PRICE. Electronics 48, no. 2, 73-8, Jan. 23, 1975

Besides significantly increasing systems reliability, component burn-in can give substantial cost savings to the systems builder, as it greatly reduces the need for reworking and field repair. With the present state of device technology, it is considered unwise to eliminate burn-in.

10992

Figuli, E.S. (Western Elec., Allentown, Penn.)
VELOCITY GOLD PLATING OF IC's. Electronic Packaging and Production 14, no. 5, 6 pp., May 1974

Rapid replacement of depleted gold ions at the plating surface results in higher plating efficiency. Most defects in plating are photoresist-related. Improper handling does result in many defects, but experience has indicated that the majority of them occur because the photoresist does not adhere properly to the surface of the wafer. The capability for producing relatively defect-free gold deposits and the corresponding higher chipper wafer yields as compared with the conventional method. No changes are made in the manufacturing process, in the velocity method except with power supply. Beyond that, no special component or equipment normally used in gold-plating facilities, are employed.

10993

Himmel, R.P. (Hughes Aircraft Co., Culver City, Calif.)
THE EFFECT OF STATIC ELECTRICITY ON THICK FILM RESISTORS. Insulation/Circuits 18, no. 10, 41-4 pp., Sept. 1972

While thick film resistive materials have been improved considerably in recent years, many still experience a severe and permanent change in resistivity when exposed to static electricity. This becomes a problem when safeguards to prevent static electricity are not taken during the manufacture of hybrid circuits. Some of the latest generation of commercially available thick film materials have been evaluated for relative sensitivity to static voltages. The results of this study indicate that the presence of metal and metal oxide aggregate particles in the resistive material causes the observed behavior.

10994

King, J. (Hybrid Systems Corp., Burlington, Mass.)
THICK OR THIN-FILM RESISTORS? FOR HIGH POWER AND RESISTANCE AT LOW COST, THICK FILMS ARE BEST, BUT WHEN HIGH PRECISION AND TRACKING ARE IMPORTANT, USE THIN FILMS. Electronic Design 22, no. 17, 92-5, Aug. 16, 1974.

In hybrid microcircuits, the choice narrows to either thick or thin-film resistors. The best choice is dictated by circuit requirements; there is no clear advantage of one technology over the other in all cases. Thin-film resistors are used where high precision, stability and low noise are required. But thick-film resistors have better power handling capability and lower cost. Of all circuit components, resistors are the most widely used, especially in microcircuit packages. To a large extent, this is because thick and thin-film resistors can be made inexpensively and in high density. Thus circuits like digital-to-analog converters, which are highly resistor-dependent, are a particular favorite for microcircuit hybrid packaging.

10995

Nesselroth, M. (Motorola, Inc., Fort Lauderdale, Fla.)
LASER TRIMMING: MANUAL OR COMPUTER-CONTROLLED? Electronic Packaging and Production 14, no. 9, 56-9, Sept. 1974

Laser systems are not available to satisfy a variety of trimming requirements. Presented here are several of the more important technical criteria which must be considered by a buyer in his selection of such a system. Originally, CO_2 systems were commonly used for resistor trimming, but they have since been superseded by tungsten-pumped and, more recently, krypton-pumped YAG lasers. A careful selection of a laser trim system based on the many factors discussed here should provide the user with a capability for quickly and efficiently trimming thick-or thin-film resistors.

10996

Kennedy, T.N. (IBM Corp., General Prod. Div., San Jose, Calif.)
EVALUATING RF SPUTTERED Al_2O_3 FOR MICROCIRCUIT FABRICATION. Electronic Packaging and Production 14, no. 12, 5 pp., Dec. 1974

The properties of RF sputtered Al_2O_3 films have been shown to be dependent of the input power, substrate bias, substrate temperature and sputtering pressure. Deposition rate increased linearly with power, and, at 6 W/cm^2, a rate of 550 Å/min was obtained. The quality of the films as determined by etch rate and optical density is related to the entrapped argon in the films; however, residual tensile stresses, undesirable in thin amorphous films, were observed in films deposited under conditions in which there was insufficient resputtering, i.e., at low substrate bias. In general, good quality, passivating Al_2O_3 films can be obtained by sputter deposition at high negative substrate bias (-100 V), moderate sputtering pressures (5 to 20 x 10^{-2} torr) and moderate substrate holder temperatures (150°C)

10997

Novak, W.T. (Cobilt, Sunnyvale, Calif.)
WAFER PRINTING FOR HIGHER YIELDS. Electronic Packaging and Production 14, no. 9, 4 pp., Sept. 1974

Semiconductor processing requires photolithgraphic steps to define specific patterns on the wafer's surface. This discussion evaluates the three printing methods and indicates how to optimize each method in order to achieve maximum yields.

10998

Zaks, D.I. and Naumov, N.M.
THERMAL INTERACTION IN INTEGRATED CIRCUITS. Izv. Vuzov SSSR-Radioelektronika XIV, no. 11, 1304-11, 1971. Translator: Leo Kanner Assoc., Redwood City, Calif. AD 785 985

Interactions take place in integrated circuits between the thermal and electrical fields (thermal interaction). This phenomenon, frequently degrading the operation of semiconductor instruments, can be used for creation of low frequency range integrated circuits. Several examples of such circuits and models of them are examined.

10999

Goryunov, N.N.
PROPERTIES OF TRANSISTORS DURING CONTINUOUS OPERATION AND STORAGE. Biblioteka po Radioelektronike. Svoystva Poluprovodnikovykh Priborov pri Dlitel'noy Rabote i Khranenii, Nr. 23, pp. 1-103, 1970.
Rept. no. FTD-MT-24-235-74, 133 pp., Jan. 17, 1974. Transl. by USAF, Foreign Technol. Div., Wright-Patterson AFB, Ohio. AD 773 880

This is a discussion about the properties of semiconductor diodes and transistors during their continuous operation and storage. Descriptions are given of basic reasons for the failures of instruments connected with phenomena on the surface of crystals, the breakdown of junctions, and the description of contacts. Mathematical models of the processes of failures are given. Technical specifications are stated for the quality and reliability of instruments, the methods of checking them, and test evaluation. Information is given about accelerated tests and indestructible quality control. The experimental dependences of the failure rate and change in parameter values of instruments on time and load are given. Recommendations are given regarding the design of reliable equipment on diodes and transistors.

11000

Reynolds, F.H., Lawson, R.W. and Mellor, P.J.T. (Brit. Post Office Telecommun. Hdqtrs., London, Engl.)
SPECIFICATIONS FOR INTEGRATED CIRCUITS IN TELECOMMUNICATIONS EQUIPMENT. Proceedings fo the IEEE 62, no. 2, 223-30, Feb. 1974

The demand for reliable semiconductor components in telecommunications system has stimulted the preparation of two specification schemes, one for bipolar digital integrated circuits of the widely used standard-scale type and the other for MOS custom components representing large-scale integration. While sharing many reliability requirements with other applications, the telecommunications field is distinguished by the need for a long service life, often of several decades. Both schemes accordingly involve accelerated tests, particularly those employing elevated ambient temperatures. Other requirements are also common, as for encapsulation, but the main approaches differ. For bipolar circuits, the traditional component sampling procedure is adopted, details being given of the basis and background of some of the more important clauses. The MOS specification is based on design and process control, of which only the latter is presently developed featuring the use of a specially designed test component.

11001

Anon.
Microelectronics and Reliability 13, no. 1, 1-60, Feb. 1974
Microelectronics and Reliability 13, no. 2, 61-150, Apr. 1974
Microelectronics and Reliability 13, no. 3, 151-232, June 1974
Microelectronics and Reliability 13, no. 4, 233-308, Aug. 1974
Microelectronics and Reliability 13, no. 5, 309-432, Oct. 1974
Microelectronics and Reliability 13, no. 6, 433-550, Dec. 1974

11002

Sinnadurai, F.N. (Brit. Post Office Res. Centre, Engl.)
THE ACCELERATED AGEING OF PLASTIC ENCAPSULATED SEMICONDUCTOR DEVICES IN ENVIRONMENTS CONTAINING A HIGH VAPOUR PRESSURE OF WATER. Microelectronics and Reliability 13, no. 1, 23-7, Feb. 1974

Early indications that water vapour accelerates the degradation of plastic encapsulated semiconductor devices have been pursued further with tests at high, unsaturated vapour-pressures. Equipment has been developed to apply unsaturated water vapour at pressures greater than one atmosphere to the devices and the results have shown a well ordered relationship between vapour pressure and time to failure, which may be extrapolated to the environmental conditions pertaining to use. The validity of an accelerated test using the the vapour pressure of water is supported by experimental observations and provides the basis for a simple, short-term test for assessing the reliability of plastic encapsulated semiconductor devices intended for long-life applications.

11003

Bredenkamp, G.L. (Natl. Elec. Eng. Res. Inst., Council for Sci. and Ind. Res., Solid State Electronics Div., Pretoria, South Africa)
DESIGN OF PRECISION THIN FILM RESISTIVE NETWORKS. Microelectronics and Reliability 13, no. 1, 49-50, Feb. 1974

Untrimmed resistor networks having relative tolerances better than + 0.05 per cent can be designed by eliminating the effect of both the resistivity distribution across the substrate and also that of undercutting during etching. The design rules for achieving this are set out.

11004

Kemeny, A.P. (Ind. Res. Inst. for Electronics "HIKI", Budapest, Hung.)
LIFE TESTS OF SSI INTEGRATED CIRCUITS. Microelectronics and Reliability 13, no. 2, 119-42, Apr. 1974

Some results as well as a new and simple method digitial IC life testing are dealt with here referring to the beginning of a large-scale test programme which started years ago. As the first step, bipolar, SSI digital ICs of the TTL, DTL and RTL series have been conducted comprising about 60 million device-hrs, life-tested by various long-run stress methods as temperature storage d.c.-and switching-service operational tests to gain a fair picture on main failure mechanisms, the nature and shift tendencies of parameter distributions as well as on the activation energy of degradation process--besides the estimation of characteristic failure rates in various stress forms--to facilitate the use of accelerated methods and to rendering possible the optimal choice among testing methods for future reliability assessment work. It has been shown that temperature activation energies of approx. 1.0 eV--essentially the same as at discrete planar transistors--were resulted if "side" effects of experiments are carefully avoided.

11005

Prasad, P.S.K. (Bharat Electronics Ltd., Bangalore, India)
RELIABILITY PREDICTION AND GROWTH STUDIES -- HOW ACCURATE AND USEFUL? Microelectronics and Reliability 13, no. 3, 195-202, June 1974

In a reliability programme, predictions are made at various stages. The usual prediction techniques up to the early design stage are similar equipment technique, similar complexity technique, prediction by function and prediction by stress factors and component population. At a fairly advanced stage of the design, however, more sophisticated techniques have been attempted, such as degradation analysis, parameter variation method, worst case method and Monte-carlo method.

11006

Li, S.P. (JPL, Calif. Inst. of Technol., Pasadena, Calif.)
A MEASUREMENT TECHNIQUE OF TIME-DEPENDENT DIELECTRIC BREAKDOWN IN MOS CAPACITORS. Microelectronics and Reliability 13, no. 3, 209-14, June 1974. NAS 7-100

The statistical nature of time-dependent dielectric breakdown characteristics in MOS capacitors was evidenced by testing large numbers of capacitors fabricated on single wafers. A multi-point probe and automatic electronic visual display technique are introduced that will yield statistical results which are necessary for the investigation of temperature, electric field, thermal annealing, and radiation effects in the breakdown characteristics, and an interpretation of the physical mechanisms involved. It is shown that capacitors of area greater than 2×10^{-3} cm^2 may yield worst-case results, and that a multi-point probe of capacitors of smaller sizes can be used to obtain a profile of non-uniformities in the SiO_2 films.

11007

Braun, L. (TRW Systems Group, Redondo Beach, Calif.)
ELECTROMIGRATION TEST ING--A CURRENT PROBLEM. Microelectronics and Reliability 13, no. 3, 215-28, June 1974

Electromigration is arousing growing interest and concern as a potential failure mechanism in integrated circuit metallization, particularly from users and designers of LSI and other small-geometry devices, in which current densities of $10^5 - 10^6$ A/cm^2 are becoming increasingly common. This paper examines the various problems associated with conducting and evaluating electromigration tests in order to obtain valid lifetime information about actual devices. The literature is reviewed to indicate the extent and relevancy of the available data, as well as the numerous contradictions and uncertainties that exist. The problems that arise with test procedures, measurements, and the evaluation and application of test data are examined and means for surmounting such problems are suggested.

11008

Taketa, Y. and Haradome, M. (Nihon U. at Narashino, Phys. Sci. Labs., Japan)
STABILITY AND DETERIORATION MECHANISM OF THICK FILM RESISTORS. Microelectronics and Reliability 13, no. 4, 281-9, Aug. 1974

Life test stability and failure mechanism of RuO_2-based thick film resistors at elevated temperature and high humidity have been examined. It is found that the change of resistance under high humidity conditions is caused mainly by reaction of $RuO_2 + xH_2O$ $RuO_2{:}xH_2O$, and that the resistance value of RuO_2:Ag:Glass in the high temperature conditions mainly due to oxidation of Ag, and that initial drift and internal strain in the resistors tend to be influenced by the firing conditions. In the case of the resistors having conductive component of solid solution of RuO_2 and other metals (exp. $Bi_2Ru_2O_7$). the resistors have little resistance drift and are stable.

11009

Doyle, N. (Fairchild Semiconductor, Inc., Mountain View, Calif.)
LIC TECHNOLOGY. Microelectronics and Reliability 13, no. 5, 315-24, Oct. 1974

The first monolithic integrated circuit, constructed in 1961, was an RTL flip-flop. Three years later the first linear IC followed. Like the flip-flop, this was also a basic building-block--an operational amplifier. Since that time the growth of digital ICs into MSI and LSI systems has been paralleled by the evolution of complex linear subsystems. The typical linear IC of the 1970s is no longer a simple analog gain block but rather a complex device performing a number of precise functions. This seminar will review the present status of linear IC technology and discuss future trends.

11010

Doyle, N. (Fairchild Semiconductor, Inc., Mountain View, Calif.)
IC VOLTAGE REGULATORS. Microelectronics and Reliability 13, no. 5, 325-38, Oct. 1974

The power supply is the one design area common to all systems and, at the same time, that portion of the system most likely to be neglected in design effort or foreshortened on design time due to continual changes in the system power requirements. The purpose of this paper is to familiarize the designer with the Fairchild range of monolithic voltage regulators and to show some of the more popular applications of these devices.

11011

Alfke, P. (Fairchild Semiconductor, Inc., Mountain View, Calif.)
BIPOLAR MEMORIES. Microelectronics and Reliability 13, no. 5, 339-43, Oct. 1974

Bipolar Read-Write Memories (RAMS) are very complex and sophisticated devices using the latest advances in semiconductor technology to achieve high speed and high packing density. They are more expensive and consume more power than MOS circuits of comparable complexity, but they are significantly faster and are much easier to understand and to use. Bipolar RAMs use the same supply voltages as the associated logic (+5 V for TTL, -5·2 V for ECL) and their inputs and outputs are level compatible with the logic, no special interface elements are required.

11012

Alfke, P. (Fairchild Semiconductor, Inc., Mountain View, Calif.)
CHARGE COUPLED DEVICE APPLICATIONS. Microelectronics and Reliability 13, no. 5, 345-7, Oct. 1974

A summarized presentation of Fairchild's line of charge-coupled devices: their geometries, applications and future trends.

11013

Avery, L.R. (RCA Solid State-Europe, Sunbury-on-Thames, Middlesex, Engl.)
MIXED-DISCIPLINE MONOLITHIC INTEGRATED CIRCUITS--BIPOLAR, MOS AND COS/MOS TECHNOLOGIES AND FUTURE TRENDS. Microelectronics and Reliability 13, no. 5, 349-61, Oct. 1974

This paper describes the basic bipolar integrated-circuit process, its advantages and its limitations. The benefits of close matching and temperature tracking are discussed. The current mirror concept is developed and its various forms and its value in circuit design are discussed, culminating in the operational transconductance amplifier (OTA). The paper then deals with the shortcomings of p-n-p lateral transistors and their replacement by p-MOS devices to achieve wideband performance in operational amplifiers. MOS-input operational amplifiers, together with techniques for reducing offset voltage and offset-voltage drift, are mentioned. The special requirements of COS/MOS processing for linear-mode devices are also examined. The possibility of circuits with zero popcorn noise and ultra high input impedance, and the combination of linear and digital functions on a single chip, are also discussed. COS/MOS-bipolar interface circuits are analyzed, followed by future trends in design, including dielectric, air isolation and beam-lead technology.

11014

Bishop, A. and Jones, P. (RCA Ltd., Sunbury-on-Thames, Middlesex, Engl.)
C-MOS--A STATUS REPORT. Microelectronics and Reliability 13, no. 5, 363-72, Oct. 1974

C-MOS has the high packing density of MOS combined with logic speeds approaching that of TTL. The general characteristics of C-MOS have been fully described, and as a contrast this paper examines two specific aspects of C-MOS. Firstly on the processing side a comparison is made of today's approaches. Secondly, a comparison between C-MOS and TTL is illustrated by a typical equipment design.

11015

Payne, A.J. (IIT Semiconductors, Foots Cray, Sidcup, Kent, Engl.)
LINEAR AND INTERFACE CIRCUITS
Microelectronics and Reliability 13, no. 5, 373-8, Oct. 1974

The scope of linear and interface circuits covers such a vast field that this paper will be limited to brief descriptions of some recent IIT Semiconductors developments in the field of custom design and the 7100 series of standard devices. These devices encompass TTL, MOS and Bipolar technology and therefore provide a broad technology view across a limited number of products. Briefly, the circuits are divided into three groups:

(a) Input interface circuits.
(b) Output interface circuits.
(c) Miscellaneous peripheral circuits.

11016

Penney, J.D. (ITT Semiconductors, Foots Cray, Sidcup, Kent, Engl.)
MOS AND BIPOLAR ICS IN CONSUMER APPLICATIONS. Microelectronics and Reliability 13, no. 5, 379-86, Oct. 1974

This paper considers the application of Bipolar and MOS technologies to a number of consumer areas. It discusses the relevant advantages of MOS and Bipolar technology; a wide range of actual devices are included, and brief details of the operating performance.

11017

Uebe, F. (Motorola Semiconductor Prod. Div., Geneva, Switz.)
N-CHANNEL MOS MEMORIES--NEW POSSIBILITIES FOR MICROPROCESSOR MEMORY DESIGN. Microelectronics and Reliability 13, no. 5, 387-400, Oct. 1974

The new generation of microprocessors has considerably reduced the hardware size of the central units and the dimensions of their power supplies. Chip-sized CPUs have created new areas of applications, especially where small size and light weight are demanded. The memory portion of such a data processing system, however, remained unchanged.

11018

Naylor, R. (Internatl. Computers Ltd., Microsystems Sector, Res. & Advanced Dev. Centre, Manchester, Engl.)
DIGITAL IC APPLICATIONS--HYBRID INTERCONNECTION OF DIGITAL CIRCUITS.
Microelectronics and Reliability 13, no. 5, 411-2, Oct. 1974

Significant advances in the operating speed and complexity of silicon integrated circuits that can be fabricated on a silison chip have been made in recent years. In order to be able to take maximum advantage of these improvements, it is necessary to mount the circuits closer together and the use of hybrid technologies enables this to be achieved, whether the circuits are in an LSI or conventional form.

11019

Kendall, J.T. (Natl. Cash Register Co., Dayton, Ohio)
RECENT PROGRESS IN MNOS MEMORY TECHNOLOGY.
Microelectronics and Reliability 13, no. 5, 413-5, Oct. 1974

Since the publication of the first papers, a considerable amount of development work has been carried out in an effort to build a practical memory using the variable-threshold MNOS transistor. Some major processing difficulties have had to be overcome and some novel circuits have been developed.

11020

Chapple, I.K. (Plessey Co. Ltd., Plessey Memories, Towcester, Northants, Engl.)
THE APPLICATION OF MOS MEMORIES TO REPLACE CORE STORAGE IN LARGE COMPUTERS.
Microelectronics and Reliability 13, no. 5, p. 415, Oct. 1974

If plans for dynamic MOS RAMs are fulfilled, a phasing out of core storage in computer main frames is inevitable except where non-volatility is essential to a user. Every delay in production of semiconductors and cost reduction in core will extend the lifetime of entrenched core technology.

11021

Debenham, M.J. (Standard Telecommun. and Cables Ltd., London, Engl.)
MOS IN TELECOMMUNICATIONS.
Microelectronics and Reliability 13, no. 5, p. 417, Oct. 1974

At present, therefore, there is a discrete semiconductor use in telephone exchanges. MOS entered the telecomms area firstly through subassemblies within the telephone exchange. This phased introduction has maximised field experience with MOS and generated confidence in the ability of MOS to outperform a mechanical counterpart in reliability, size and power consumption.

11022

Shenton, G. (AMI Micro-systems Ltd., Swindon, Wiltshire, Engl.)
A SYSTEMS APPROACH TO THE DESIGN OF MOS MEMORY COMPONENTS.
Microelectronics and Reliability 13, no. 5, 419-24, Oct. 1974

The newer MOS technologies have produced a diverse set of memory chips offering the memory designer the possibility to select a more optimum component for his particular application. All designs have aimed at making the chips more compatible with the processor and bus oriented systems. A spin-off of such intense memory chip development is that the MOS memory is now available as a cheap system component which can readily be incorporated in many areas of logic design in which memory as such would not previously have been considered. The prudent designer must be careful to choose devices which have not only the requisite performance, but substantial and reliable sourcing.

11023

Yadav, R.P.S. (M.M. Postgraduate Coll., Modinager (U.P.), India)
COMPONENT RELIABILITY UNDER ENVIRONMENTAL STRESS.
Microelectronics and Reliability 13, no. 6,473-5, Dec. 1974.

In this paper, the author has developed a mathematical model for the evaluation of components' reliability under the assumption that the component possesses a non-constant (variable) failure rate of the form $(m/k)t^{m-1}$, which means that the failure density function follows Weibull pattern (distribution). The stress, under which component operates, has been assumed to be Maxwellian. In the end, cases when Weibull distribution reduces to exponential and Rayleigh distributions, have also been discussed.

11024

Pease, R.L. and Galloway, K.F. (U.S. Navy, Nav. Ammunition Depot, FLSD, Strategic Systems and Components Div., Sci. Analysis Branch, Crane, Ind.)
DEGRADATION OF BIPOLAR TRANSISTOR ELECTRICAL PARAMETERS DURING SEM EVALUATION. Microelectronics and Reliability 13, no. 6, 549-50, Dec. 1974

The scanning electron microscope (SEM) has become a valuable tool in the study of semiconductor devices for inspection of metallization and passivation integrity as well as failure analysis. Such an evaluation is nondestructive to the bulk properties of the device materials since the electron energy is generally below the threshold for producing displacement effects or chemical changes. However, the electrons deposit energy in the materials through ionization processes. The effects of ionization radiation on bipolar transistors has been studied in some detail. The permanent effects result in increased leakage currents and decreased gain and are realized through charge trapped in the various oxides and states which can exchange charge with the semiconductor material at oxide-semiconductor interfaces. This note illustrates the relative amount of parameter degradation which can be expected during typical SEM cans.

11025

IEEE
Proceedings 1974 Annual Reliability and Maintainability Symposium. Sponsored by the IEEE Reliability Group, AIAA, AIIE Quality Control and Reliability, Eng. Div., ASME, ASQC Reliability Div., IES and ASM. Los Angeles, Calif. 579 pp., Jan. 29-31, 1974. IEEE Cat. No. 74CH0820-IRQC

Sessions:
- 1A R & M - The Buyer/Seller Interface
- 1B Maintainability Technology Development
- 1C Consumer Products
- 1D Tutorial I
- 2A Integration of R & M into the Design Process
- 2B Test Effectiveness
- 2C Product Liability
- 2D Tutorial II-Mathematics
- 3A Status of MIL-HDBK-217B
- 3B Care Workshop
- 4A Life Cycle Cost Analysis
- 4B Reliability of Materials
- 4C Safety
- 4D Tutorial III-Test Modeling
- 5A Advisory Board Panel
- 5B Transportation
- 6A Paper Fair
- 6B Human Performance Reliability Modeling
- 6C Reduced Support Cost-A Design Objective
- 7A Device Reliability
- 7B Math Modeling
- 7C Pot Pourri
- 7D Tutorial IV-Maintainability
- 8A Realistic Prediction Techniques
- 8B Mechanical Reliability

11026

Foster, J.W. (Tex. A&M U., Texarkana, Tex.) and Craddock, W.T. (U.S. Army Mobility Equip. Res. and Dev. Center, Fort Belvoir, Va.)
ESTIMATING LIFE PARAMETERS FORM BURN-IN DATA. pp. 206-9. Proceedings 1974 Annual Reliability and Maintainability Symposium. Sponsored by the IEEE Reliability Group, AIAA, AIIE Quality Control and Reliability Eng. Div., ASME ASQC Reliability Div., IES and ASM. Los Angeles, Calif. 579 pp., Jan. 29-31, 1974. IEEE Cat. no. 74CH0820-IRQC

This paper begins with a pertinent literature review which specifies areas of the general background theory. Secondly, the model is presented and a time to failure probability density function along with a reliability function are derived. Next the parameters are estimated using the maximum likelihood principle for both time terminated and failure terminated testing. The equations which evolved require numerical techniques for solution. Finally, a Monte Carlo simulation is performed to study the behavior of the estimates. Histograms of the estimators are presented.

11027

Reich, B. and Hakim, E.B. (U.S. Army Electronics Technol. and Devices Lab., (ECOM) Semiconductor Devices and Electronics Tech. Area, Fort Monmouth, N.J.)
CAN PLASTIC SEMICONDUCTOR DEVICES AND MICROCIRCUITS BE USED IN MILITARY EQUIPMENT? pp. 396-402. Proceedings 1974 Annual Reliability and Maintainability Symposium. Sponsored by the IEEE Reliability Group, AIAA, AIIE Quality Control and Reliability, Eng. Div., ASME, ASQC Reliability Div., I IES and ASM. Los Angeles, Calif., 579 pp., Jan. 29-31, 1974. IEEE Cat. no. 74CH0820-IRQC

The majority of U.S. Manufactured semiconductor devices and integrated circuits are in plastic encapsulation; indications are that the current percentage of plastic encapsulated devices will continue to increase in the future. Currently, both MIL-S-19500 and MIL-M-38510, the general specifications for semiconductors and microcircuits, preclude their general use in military systems. The continually increasing percentage of produced plastic semiconductors and microcircuits and their lower prices have brought pressure upon the military to lift current restrictions on their general system applications. This paper addresses itself to whether or not this policy should be continued in 1974, based on results obtained over a six year period. Experience based on field results and observations, laboratory and controlled field testing is used as the basis for the current conclusion on plastic device usage in military equipment.

11029

Gertz, R.H. (Bell Telephone Labs., Holmdel, N.J.)
COMPONENT FAILURE RATES FROM FIELD STUDIES. pp. 409-12. Proceedings 1974 Annual Reliability and Maintainability Symposium. Sponsored by the IEEE Reliability Group, AIAA, AIIE Quality Control and Reliability, Eng. Div., ASME, ASQC Reliability Div., IES and ASM. Los Angeles, Calif., 579 pp., Jan. 29-31, 1974. IEEE Cat. no. 74CH0820-IRQC

An in-service reliability studies program was started several years ago covering many of the communications equipments in the Bell System. Data has been collected on more than 500 billion component operating hours and more than 3,000 component failures have been analyzed for 45 types of components. A failure rate "dictionary" has been compiled listing the estimated failure rates for these components when used in conservatively designed equipment operating in relatively low stress levels. These values are used to evaluate performance of existing equipment and to predict operating experience for newly designed equipment. A "black box" formula has been developed for reliability prediction which includes both the component failure rates and equipment removals for other than component reasons.

11030

Welker, E.L. and Lipow, M. (TRW Systems Group, Redondo Beach, Calif.)
ESTIMATING THE EXPONENTIAL FAILURE RATE FROM DATA WITH NO FAILURE EVENTS. Proceedings 1974 Annual Reliability and Maintainability Symposium. Sponsored by IEEE Reliability Group, AIAA Quality Control and Reliability, Eng. Div., ASME, ASQC Reliability Div., IES and ASM. Los Angeles, Calif., 579 pp., Jan. 29-31, 1974. IEEE Cat. no. 74CH)820-IRQC

This paper has considered alternatives to the method of maximum likelihood for estimating an unknown constant failure rate from data consisting of the number of failures, n, observed in T part hours of operation. The arguments which have been presented indicate that this estimator is numerically reasonable and that it is generated by rather logical methods. It is recognized that there is no single correct solution to this problem.

11031

Schwee, L.J., Irons, H.R., Anderson, W. E. et. al. (U.S. Navy, Nav. Surface Weapons Center, Silver Spring, Md.)
PROGRESS TOWARD THE CROSSTIE MEMORY II. Rept. no. NOLTR 74-176, 20 pp., Oct. 1, 1974

In the crosstie memory, information is stored in magnetic domain walls rather than domains and domain wall motion is not used in its operation. The basic building block of the crosstie memory is a magnetic shift register which depends on Bloch line motion rather than domain wall motion. The crosstie memory is intended for use as a block oriented random access memory (BORAM) or fast auxiliary memory (FAM). The advantages of the crosstie memory are speed, low power, high bit density, nonvolatility, a wide temperature range of operation, low cost and available technology. This report contains information on wall placement techniques, dynamic nucleation thresholds, propagation, microcircuitry, domain wall observation, and detection. Microcircuitry for shifting data has been developed and tested for 32-bit experimental shift registers. The information is observed using the magnetooptic Kerr effect. Detection is considered feasible using either magnetoresistance or guided wave optics.

11032

GE, Aerospace Electronic Systems Dept., Reliability & Quality Assurance, Matls. & Components
GENERAL ELECTRIC AEROSPACE ELECTRONIC SYSTEMS DEPARTMENT SEMICONDUCTOR PRESENTATION. 72 pp., Apr. 16, 1974

Overview of G.E. Utica, semiconductor quality and reliability practices and experiences. Includes highly summarized data on supplier quality, failure rate experience, failure modes and mechanisms, screening results, and advanced components experience.

11033

Taylor, S.A. (Martin Marietta Corp., Orlando, Fla.)
FAILURE MECHANISMS IN IRRADIATED PLASTIC INTEGRATED CIRCUITS. Rept. no. ECOM 0313-F, Rept. no. OR 12, 957, Final Rept., July 1-Dec. 31, 1973, 135 pp., Apr. 1974. AD 780 912. DAAB07-73-C-0313

This program was devised to evaluate the performance of plastic integrated circuits in various types of radiation environments. Two different test parts were employed. These parts were selected to be representative of broad semiconductor processing technologies. The bipolar process technology was represented by 741 operational amplifier. The complimentary metal-oxide silicon (CMOS) process was represented by the 4028 binary-to decimal decoder.

11034

Sato, S., Sato, A. and Okamoto, E. (Nippon Elec. Co., Ltd., Kawasaki, Japan)
AN SiO_2-Ta_2O_5 THIN FILM CAPACITOR. IEEE Trans. on Parts, Hybrids and Packaging PHP-9, no. 3, 161-6, Sept. 1973

A capacitor has been developed which is superior to previously reported duplex capacitors. The dielectric consists of anodic tantalum oxide overlaid with silicon dioxide deposited by RF sputtering. The capacitor remained stable with no failures occurring when aged under various conditions of voltage, temperature, and humidity. It can be processed in a manner compatible with the manufacturing process of the TM or TMM capacitor.

11035

Buckley, W.D. (Energy Conversion Devices Inc., Troy, Mich.)
A PROGRAM TO EXTEND THE OPERATING TEMPERATURE RANGE OF THE AMORPHOUS SEMICONDUCTOR MEMORY DEVICE. Final Tech. Rept., 140 pp. Nov. 16, 1973. AD 915 576L. N00163-73-C-0107

Major emphasis has been placed on the study of the high temperature storage characteristics of the high impedance state for different amorphous semiconductor compositions. Compositions have been investigated which can be stored at 125°C for extended periods. Progress has also been made in understanding the factors which determine the temperature coefficient of threshold voltage. A significant reduction in this coefficient was achieved for the compositions which exhibit improved high temperature storage characteristics.

11036

MacMillan, A.J., Romeo, D.E. and Sandor, J.E. (TRW Systems Group, Redondo Beach, Calif.)
LOW POWER HIGH DENSITY MOS ARRAYS FOR ARMY APPLICATION. Rept. no. ECOM-0215-2, Quart. Rept. no. 2, Sept. 15-Dec. 15, 1973, 59 pp., Jan. 1974. AD 918 658L. DAAB07-73-C-0215

This quarterly report details the accomplishments in a program to develop an optimized technology for the fabrication of relatively low speed, random logic, large scale digital integrated circuits. The optimized technology relates to circuits with minimum power dissipation and high packing density for use in systems operating at clock speeds of 1 MHz. The primary goal of the program is to develop a complementary MOS technology that permits the realization of circuits with significantly higher packing densities than standard cell complementary MOS devices while exhibiting a decrease in power consumption of some two orders of magnitude over presently available ration type P-MOS logic circuits. The accomplishments during the second quarter included fabrication and evaluation of test chips (Veep-2) analysis of the two approaches to obtaining an optimum packing density.

11037

Hurlston, R.E. MacKenna, E. and Weigand, R. (Fairchild Camera & Instr. Corp., Fairchild Res. and Dev. Palo Alto, Calif.)
PRODUCTION ENGINEERING MEASURE FOR DIGITAL ELECTRONIC FUZE TIME XM587E2.
Quart. Rept. no. 9, Dec. 1, 1971-Feb. 29, 1972, 28 pp., Sept. 1972
Quart. Rept. no. 10, Mar. 1-May 31, 1972, 33 pp., Dec. 1972
Quart. Rept. no. 11, June 1-Aug. 31, 1972, 31 pp., Aug. 1973
Final Rept. Nov. 21, 1969-Aug. 31, 1973, 137 pp., Sept. 1973. DAAB05-70-C-3114

A pilot line, capable of producing 5,000 MNOS programmable counters and 5,000 MOS scalers per week, was established. The MNOS programmable counter has non-volatile memory capability; the MOS scaler combines frequency division and logic functions and was designed using the Fairchild Micromosaic TM approach, both devices are LSI, and both are major components of the XM587E2 electronic time fuze. The reliability of the circuits was demonstrated by the successful completion of Group A and Group B high-reliability tests.

11038

Organic, V.J. and Shauer, H.A. (U.S. Army, ECOM, Technol. & Devices Lab., Fort Monmouth, N.J.)
STUDY OF TRANSIENT RADIATION EFFECTS ON A MONOLITHIC INTEGRATED CIRCUIT FERRITE PHASE SHIFTER DRIVER. Rept. no. ECOM-4069, Tech. Rept., 24 pp., Jan. 1973

A study has been performed to determine the permanent performance degradation due to transient radiation on a ferrite phase shifter driver circuit. The driver circuit contained two types of monolithic integrated circuits a large scale integration (LSI) P-channel metal-oxide-semiconductor (P-MOS) circuit to perform the steering logic and a bipolar circuit to perform the high current analog driver function. An analysis was made to predict possible failure modes, and irradiation tests were run on sample circuits. The subsequent test results showed satisfactory circuit performance, up to an irradiation level of approximately 10^3 n/cm^2 ($E \geq 10$keV) and gamma radiation of 3×10^4R.

11039

Dell'Oca, C., Drake, L.E., Marshall, R.W. et al. (Fairchild Camera & Instr. Corp., Fairchild Semiconductor, Mountain View, Calif.)
MANUFACTURING TECHNOLOGY ON RADIATION HARDENED MSI/LSI INTEGRATED CIRCUITS.
Rept. no. AFML-IR-500-1, Interim Tech. Rept. no. 1, May 16-Aug. 31, 1972, 72 pp., Sept. 1972. AD 908 294L.
Rept. no. AFML-IR-500-1, Interim Tech. Rept. no. 9, June 1-Aug. 31, 1974, 22 pp., Oct. 1974. F33615-72-C-1200

The objective of this project is to establish and demonstrate new manufacturing methods and techniques applicable to the production of radiation hardened bipolar integrated circuits with MSI/LSI complexity levels. The specific contract objectives are as follows:

. To determine the materials and processing technology necessary to manufacture radiation-hardened MSI/LSI integrated circuits with acceptable yields.
. To fabricate standard MSI/LSI circuits and accumulate yield data to support the cost effectiveness of the combined technology.
. To fabricate and deliver five different MSI circuits which will demonstrate the manufacturing capability.
. To implement a manufacturing design and fabrication facility for this technology which can be demonstrated to USAF personnel.

In the ninth quarter of this program, the fabrication of additional 97S09 and 97S12 wafers was completed, but no functional die were obtained. The status of the design and fabrication of the Counter/Shift Register Array and the Arithmetic Logic Unit are also discussed. Summaries of the objective electrical specifications for the five radiation hardened MSI circuits being developed are also discussed.

11040

Lindholm, F.A. et al. (U. of Fla., Eng. and Ind. Expt. Sta., Gainesville, Fla.)
A CENTER OF COMPETENCE IN SOLID STATE MATERIALS AND DEVICES.
Rept. no. AFCRL-68-0493, Sci. Rept. no. 2, 216 pp., Oct. 10, 1968. AD 678 170.
Rept. no. AFCRL-69-0147, Sci. Rept. no. 3, 281 pp., Apr. 10, 1969, AD 688 220.
Rept. no. AFCRL-69-0416, Sci. Rept. no. 4, 217 pp., Oct. 10, 1969. AD 700 077.
Rept. no. AFCRL-TR-73-0164, Final Rept. Sept. 1, 1967-Sept. 1,.1972, 208 pp., Oct. 10, 1972. AD 766 406. F19628-68-C-0058.

The general objective of this research program is to establish at the University of Florida a center of competence in solid-state materials and devices, with primary emphasis to be placed on materials and devices not used in the conventional silicon integrated-circuit technology. A five-year program sponsored by this contract has produced technical findings in several areas: characterization of semiconductor devices and integrated circuits; electronic ceramics; noise within solids and semiconductor devices; quantum and electronic properties of elemental and compound semiconductors; and magnetic films.

11041

Netherwood, P.H., Guntlow, V.T. and Dagnoli, D.F. (Sprague Elec. Co., North Adams, Mass.)
PEM FOR IMPROVEMENT OF PRODUCTION TECHNIQUES TO INCREASE THE RELIABILITY FOR CERAMIC ISOLATION CAPACITORS FOR INTEGRATED CIRCUITS. Rept. no. A120-31, Quart. Rept. no. 1, Jan. 28-Apr. 30, 1971, 18 pp., May 1971. AD 887 664.
Quart. Rept. no. 2, May 1-July 31, 1971, 45 pp., Aug. 1971. AD 889 247L.
Quart. Rept. no. 3, Aug. 1-Oct. 31, 1971, 26 pp., Nov. 1971. AD 890 913L.
Quart. Rept. no. 4, Nov. 1-Jan. 31, 1972, 20 pp., Feb. 1972. AD 893 906L.
Quart. Rept. no. 5, Feb. 1-Apr. 30, 1972, 22 pp., May 1972. AD 902 727L.
Quart. Rept. no. 6, May 1-July 31, 1972, 30 pp., Aug. 1972. AD 905 730L.
Quart. Rept. no. 7, Aug. 1-Oct. 31, 1972, 30 pp., Nov. 1972. AD 907 518.
Quart. Rept. no. 8, Nov. 1-Jan. 31, 1973, 20 pp., Feb. 1973. AD 908 861L.
Quart. Rept. no. 9, Feb. 1-Apr. 30, 1973, 30 pp., May 1973. AD 913 070L.
DAAB05-71-C-2619.

The object of this production engineering measure is the improvement of production techniques to increase the reliability for ceramic isolation capacitor for integrated circuit applications, to meet the requirements of electronic command technical requirement/SCS-391 dated 1970 June 5 at a 0.01% maximum allowable failure rate per 1000 hours when tested at twice the rated voltage and 125°C temperature with a 90% confidence level.

11042

Narasimhan, T.R., Brandt, H.G., Dagroli, D.P. et al. (Sprague Elec. Co., North Adams, Mass.)
PRODUCTION ENGINEERING MEASURE FOR HYBRID INTEGRATED CIRCUITS FOR FUZE APPLICATIONS. PART 1. INTEGRATED ARMING AND FIRING CIRCUIT. PART 2. PRECISION OSCILLATOR INTEGRATED CIRCUIT. Rept. no. A120-34, Quart. Rept. no. 1, June 26-Sept. 26, 1971, 56 pp., Oct. 1971.
Rept. no. A120-34, Quart. Rept. no. 2, Sept. 26-Dec. 26, 1971, 47 pp., Jan. 1972.
Rept. no. A120-34, Quart. Rept. no. 3, Dec. 26, 1971-Mar. 26, 1972, 63 pp., Apr. 1972.
Rept. no. A120-34, Quart. Rept. no. 4, Mar. 26-June 26, 1972, 55 pp., July 1972.
Rept. no. A120-34, Quart. Rept. no. 5, June 27-Sept. 26, 1972, 50 pp., Oct. 1972.
Rept. no. A120-34, Quart. Rept. no. 6, Sept. 27-Dec. 26, 1972, 39 pp., Jan. 1973.
Rept. no. A120-34, Quart. Rept. no. 7, Dec. 27, 1972-Mar. 26, 1973, 39 pp., Apr. 1973.
Rept. no. A120-34, Quart. Rept. no. 8, Mar. 27-June 26, 1973 39 pp., July 1973. AD 913 258L.
Rept. no. A120-34, Quart. Rept. no. 9, June 26- Sept. 26, 1973, 21 pp., Oct. 1973.
Rept. no. A120-34, Quart. Rept. no. 10, Sept. 27-Dec. 26, 1973, 40 pp., Jan. 1974.
Rept. no. A120-34, Quart. Rept. no. 11, Dec. 27, 1973-Mar. 26, 1974, 38 pp., Apr. 1974.
Rept. no. A120-34, Quart. Rept. no. 13, June 27-Sept. 26, 1974 38 pp., Oct. 1974. DAAB05-71-C-2642 .

The objective of this production engineering measure is to establish a production capability for hybrid integrated circuits for fuze applications. The integrated arming and firing circuit involves the fabrication of a thick film circuit substrate, and attachment of transistors and capacitor components, and packaging. The program includes actual fabrication of test samples, a production run and performance of electrical, mechanical, and environmental tests as required. Reports and other information procured under this requirement will be used for industrial mobilization and preparedness planning measures are required and, when necessary to assist in establishing additional sources.

11043

Oliver, C.B., Bower, D.F., Miller, J. et al. (Assoc. Semiconductor Mfrs. Ltd., Dev. Labs., Southampton, Gt. Britain)
A STUDY OF METAL CONTACTS TO SILICON.
Rept. no. RP6-70, Ann. Rept. no. 1, C.V.D. Res. Proj. RF6-59, 13 pp., Oct. 1970. AD 880 485.
Rept. no. RP6-59/73, Final Rept., C.V.D. Res. Proj. no. RP-59, 20 pp., Oct. 1973. AD 916 828. N/CP1715/67.

The contact resistance and reliability of metal-silicon contacts have been studied in order to improve the yield and reliability of integrated circuits. A mathematical model of a metal-silicon contact has been constructed using a transmission-line analogue. The model has been experimentally verified and may be used to predict the electrical resistance and maximum current density in a contact. The electrical contact resistance of several metalization systems to silicon has been measured as a function of dopant concentration and type. The systems studied include aluminum, titanium, molybdenum, tungsten, chromium, platinum silicide and paliadium silicide. The reliability of metal-silicon contacts has been tested by thermal or electrical stressing for up to 2000 hours. Visual and electrical examination of stressed devices has shown that the metal-silicon contact is unlikely to degrade before the metallization under normal operating conditions.

11044

U.S. Air Force, Wright-Patterson AFB, Ohio.
MICROELECTRONICS. SERIES 1-0 GENERAL.
AFSC Design Handbook no. DH1-8, Third Edn. Nov. 10, 1973.

This series is carefully structured to ensure efficient use and to prevent redundant coverage of technical areas. As technical knowledge is generated, acquired, and reduced to design data, it is presented in the handbook structure where it can be readily found and applied by those who need it. A description of the various handbooks is in AFSC DH 1-1, General Index and Reference.

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