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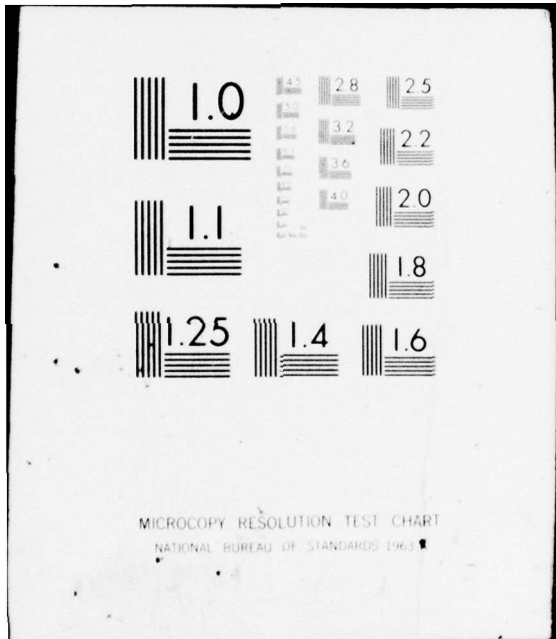
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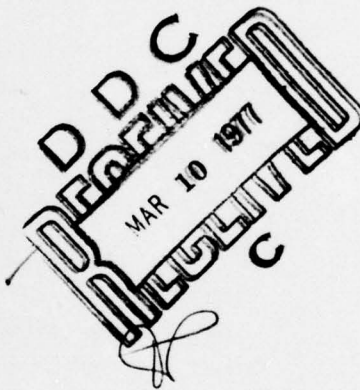
RESEARCH AND DEVELOPMENT TECHNICAL REPORT  
REPORT ECOM-74-0272-9

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ENVIRONMENT AND RADAR OPERATION SIMULATOR

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December 1976

Ninth Quarterly Report for Period 1 July 1976 through  
30 September 1976

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Prepared for

**ECOM**

US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

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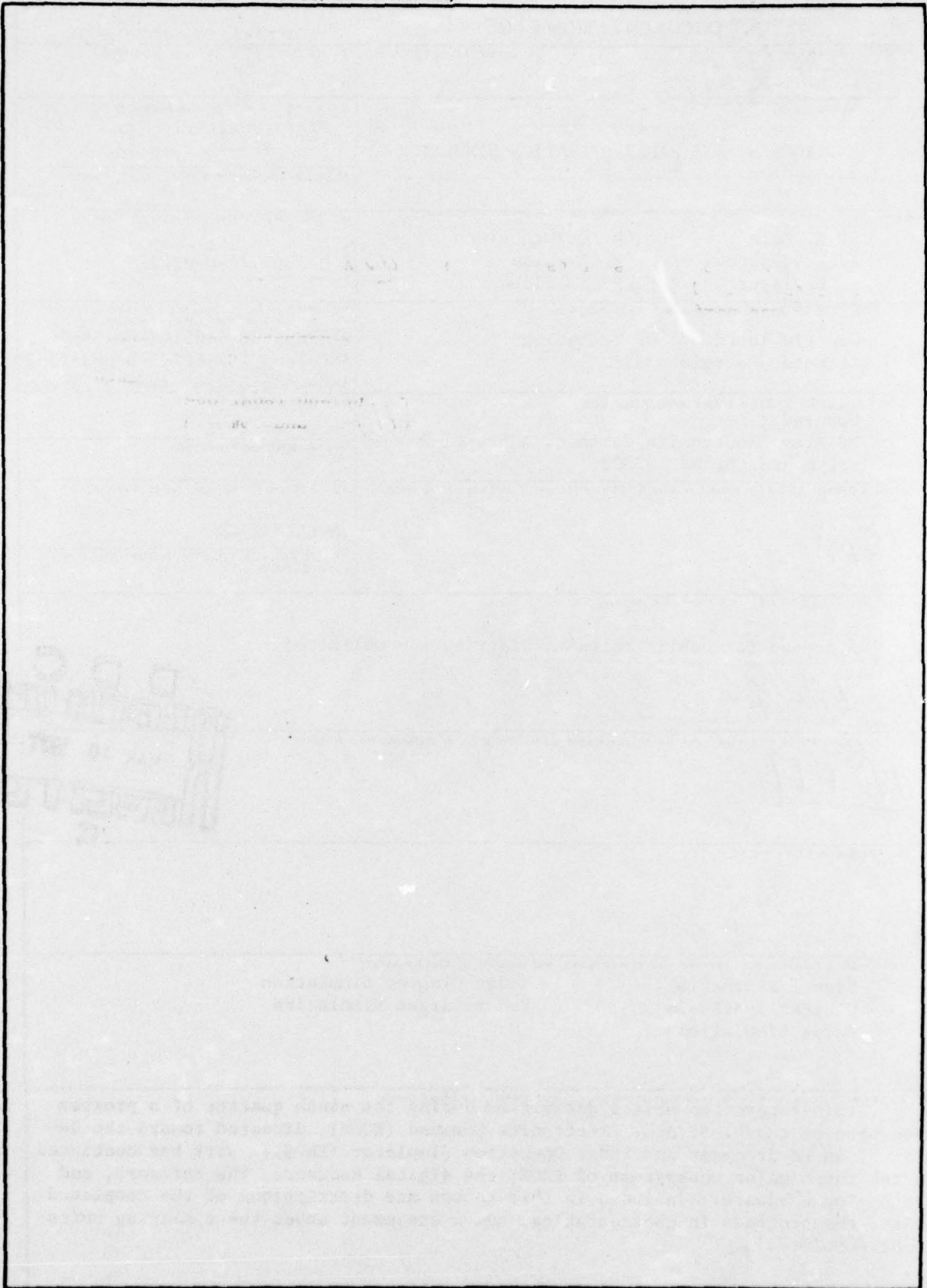
REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM	
1. REPORT NUMBER <b>18</b> ECOM 74-0272-9	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER <b>9</b>	
6. TITLE (and Subtitle) ENVIRONMENT AND RADAR OPERATION SIMULATOR.		5. TYPE OF REPORT & PERIOD COVERED Ninth Quarterly rept. no. 9 1 Jul - 30 Sep 76	
10. AUTHOR(S) S. N. Cole, R. C. Michelson A. R. Clayton, B. S. Rice E. R. Flynt, E. S. Sjoberg		8. CONTRACT OR GRANT NUMBER(S) <b>15</b> DAAB07-74-C-0272	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Georgia Institute of Technology Atlanta, Georgia 30332		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS DA Proj C8-3-05107-05-C8-CA AMC Proj 1S7-62703-D-H93-P1-06 AMC Code 672703-12-H93-PI-06	
11. CONTROLLING OFFICE NAME AND ADDRESS Commander US Army Electronics Command, AMSEL-CT-R Ft. Monmouth, NJ 07703		14. REPORT DATE December 1976	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) <b>12</b> 15 p.		15. SECURITY CLASS. (of this report) UNCLASSIFIED	
15a. DECLASSIFICATION/DOWNGRADING SCHEDULE			
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited <b>16</b> 1S762703DH93			
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) <b>17</b> P1			
18. SUPPLEMENTARY NOTES			
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Signal Synthesis                      Radar Clutter Simulation Clutter Synthesis                      Radar Target Simulation Radar Simulation			
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report summarizes activities during the ninth quarter of a program sponsored by the U. S. Army Electronics Command (ECOM), directed toward the design of an Environment and Radar Operation Simulator (EROS). Work has continued on the three major subsystems of EROS; the digital hardware, the software, and the analog hardware. Included in this report are descriptions of the completed units, the progress in documentation, and a statement about the remaining units to be completed.			

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PREFACE

This report was prepared at the Georgia Tech Engineering Experiment Station under Contract No. DAAB07-74-C-0272. The work covered by this report was performed in the Applied Engineering Laboratory under the supervision of Dr. H. A. Ecker and Mr. J. L. Eaves, Director of the Applied Engineering Laboratory and Chief of the Radar Technology Division, respectively. The progress reported herein was performed during the ninth quarter of a program to develop an environment and radar operation simulator (EROS) to be used in testing radar receivers and components.

This project is being monitored by Mr. Otto E. Rittenbach of the U. S. Army Electronics Command, and his helpful suggestions are acknowledged.

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## 1. INTRODUCTION

This report covers work performed during the period 1 July 1976 through 30 September 1976, the ninth quarter of a 30-month program to design and build an Environment and Radar Operation Simulator (EROS). The effort during this quarter has been devoted entirely to continuing the implementation of EROS hardware and software.

A large part of EROS hardware and software is completed through unit development and debug. Sections 2, 3, and 4 describe the current status of the digital hardware, software, and analog hardware respectively.

## 2. DIGITAL HARDWARE

### 2. Introduction

EROS digital hardware creates the synthetic clutter radar return, merges this with the recorded target radar return, and delivers the sampled envelope of the radar return at video to the analog hardware. Each sample sent to the analog hardware represents the amplitude and phase of the backscatter from a 15-meter range ring. The EROS digital hardware is subdivided functionally and physically into two major subsystems called the "clutter processor" and the "target processor". The clutter processor occupies one of the two cabinets that house the EROS hardware. It generates the sampled clutter backscatter for 544 cells at Doppler frequencies and attenuates these samples by antenna-pattern weights taking into account the azimuth direction of the radar's antenna beam. The target processor shares the other EROS hardware cabinet with the computer interface and with part of the analog hardware. The target processor supports the real-time computer software in providing a buffer for a large number of target samples and in performing antenna pattern weighting. It also combines the target and clutter signals and delivers the composite to the analog hardware at the video frequency.

### 2.1 Clutter Processor

The clutter processor cabinet contains three drawers. The in-phase and quadrature components of the digital filters occupy one drawer each. The third drawer contains the timing and control, the random-number generator, the control panel (for debug and maintenance), and the antenna-pattern weighting.

The two digital-filter drawers are identical, and one of these has been built. Its testing promises to be straightforward, since it consists entirely of standard modules, which have already been tested. Testing of the control drawer is still in progress, and many of the functions are working. The only function that remains to be verified is the antenna-pattern weighting. The ribbon cables that interconnect the three clutter processor drawers and that communicate with the other cabinet have been built and tested.

### 2.2 Target Processor

The target processor occupies the space of two drawers. The majority of the hardware is contained in one drawer which performs the following functions:

- ° provide a buffer for asynchronous target samples from the computer;
- ° target backscatter antenna-pattern weighting;
- ° target backscatter azimuth integration;
- ° combine target and clutter backscatter;
- ° interface with the analog hardware at the video frequency (sample rate of 10 MHz).

A microprogram stored in programmable read-only memory has been developed to implement several of the above functions. The control panel, which displays the state of the microprogram and which permits operator intervention (for debug and maintenance) occupies the space of a second drawer.

All of the hardware has been built except the interface to the analog hardware, which has been designed and is currently being fabricated. The testing efforts are currently being devoted to the microprogram control. It is planned that the testing of the target processor functions listed above will be supported by the real-time software after it has been debugged.

The target processor documentation completed thus far consists of the majority of the drawings. All of the schematics are complete except for the video interface to the analog hardware, and many of the assembly drawings are complete. The text describing the theory and operation of the target processor remains to be written.

### 3. SOFTWARE

#### 3. Introduction

EROS software is employed to create and update scenario information and to supply control data during real-time simulation. The large files of data associated with EROS have imposed constraints on software development:

- Many of the files do not fit into core storage, which makes it necessary to use disk sorting and multiple passes through the same data.
- The graphic display unit is incorporated into file maintenance to make it easier for the EROS user to verify that the scenario data are correct.
- Disk input during real-time simulation is a potential bottleneck.

Many of these problems have been overcome, and a majority of the EROS software is complete.

#### 3.1 Scenario Preparation Software

In the Eighth EROS Quarterly Report the following scenario preparation programs were accounted as complete: Spectral Clutter Library Maintenance, Complete Clutter Library Maintenance, Range Dependent Reference Data, and Target Recording. During the past quarter additional programs have been completed. These are described in the following paragraphs.

##### Antenna Pattern Reference Data

Each simulation run uses a table of 4096 antenna pattern weights (stored in the computer's core memory) for attenuating target return and a table of 68 antenna pattern weights (stored in a random-access memory in the digital hardware) for attenuating clutter return. Both tables may be derived either from an abbreviated input file of 13 antenna-pattern points or from a more detailed file of 4096 antenna-pattern points. The target antenna weight table is identical to the 4096-point antenna pattern. The clutter antenna weights are derived from the antenna pattern using Equation (20) in Section 3.3 of the Sixth EROS Quarterly Report. The program to edit user-supplied antenna pattern data and to prepare these reference tables is working.

### Clutter Scenario Editor

Each clutter scenario is subdivided into 8192 clutter cells, and a complete clutter scenario definition consists of specifying a type of clutter and an amplification factor for each of these cells. (The amplification factor is used to include position-dependent modifications of clutter-cell radar cross section due to variations in cell area, masking, incidence angle, etc.) The clutter scenario editor reduces the effort required for clutter scenario definition and improves its accuracy by providing the following facilities:

- graphic CRT display of cell contents with instantaneous response to any update;
- use of the light pen to specify cell-content changes;
- file manipulation facilities to provide backup copies and to permit new scenarios to be created as modifications to old scenarios; and,
- the option to produce a paper copy of selectable portions of the scenario.

The clutter scenario editor is working, and its user's manual is up to date.

### Clutter Scenario Compilation

The transformation of a clutter scenario into a real-time format involves obtaining the filter and radar-cross-section parameters from the reference files, applying the array amplification factors, and reorganizing the data to optimize disk access for real-time operation. Sorting is used twice to facilitate the above data handling. This program is working.

The programs that remain to be written are the target scenario editor, target scenario compilation, audio playback of target recordings, and support for EROS calibration. Software documentation is written for all of the programs that are working and for the target scenario editor.

### 3.2 Real-time Software

In the Eighth EROS Quarterly Report the Real-time Executive and the Real-time Target Processor were accounted as complete. During the past quarter the Real-time Clutter Processor and part of the Simulation Initialization Program have been completed as well. These programs have been integrated together using scaffolding programs to generate test scenario data and to trace (with selectable detail) the outputs produced by the real-time software. Because of the large volume of clutter data and the requirement to respond to antenna scan direction reversals at unpredictable times, the Real-time Clutter Processor has had to overcome a challenging disk data access problem.

The remaining real-time software to be developed is the completion of testing the integrated real-time system and the completion of simulation initialization. Documentation of the real-time software also remains to be written.

#### 4. ANALOG HARDWARE

EROS analog hardware combines the synthetic radar backscatter components into appropriate form for insertion into the subject radar. It also obtains signals from the radar in order to synchronize EROS with it. The following major components of the analog hardware are complete.

##### A/D Converter Unit

This module converts various signals from the radar under test into appropriate form for use by EROS. Its two 12-bit A/D converters digitize the radar's antenna azimuth and range-gate position during simulation. During scenario preparation these two converters are also used to digitize the in-phase and quadrature components of a recorded target signal. Incorporated in this unit are filters, amplifiers, calibration circuits, and electronic switches for selecting between simulation and scenario preparation.

##### Synchronizer

The synchronizer unit processes information from the pulse repetition frequency (PRF) trigger of the radar or from an internal crystal oscillator in order to synchronize EROS. It generates clock pulses at rates of approximately 10 MHz, 37.5 kHz, and 4.167 kHz. The clocks are integer multiples and submultiples of the radar's 37.5 kHz trigger when EROS is connected to the radar. During scenario preparation when EROS is collecting recorded target data, these clocks are internally crystal controlled.

##### Radar Interface Module

The primary purpose of the radar interface module is to provide the various interconnection options between EROS and the radar under test. It is housed in a box separate from the EROS rack mounted hardware and is connected via a 10-foot cable. It contains a patch panel for interconnection of radar and simulation circuits, a regulated power supply for the radar, a post-audio filter amplifier, and comparators for converting various radar status signals (e.g. automatic alarm) to digital logic levels.

Two modules of the analog hardware have not been completed. Their status is described below.

### Range Gate Unit

This module provides switching logic for control of the various operating modes and generates strobe and reset signals for the latches associated with the D/A converters. It actuates the latches sequentially for all range rings in the video modes, and gates a single selectable range ring in the Doppler mode. A breadboard model of this unit has been completely tested, and the final model is presently being wired.

### Analog Signal Processor

This module contains the D/A converters, analog range-weight multipliers, range integrators, noise generators, and filtering and matching circuits. Its major functions have been separately breadboarded and tested. Layout for construction of the final model of this unit has been started.

Documentation of the analog hardware thus far consists of freehand circuit diagrams of the various modules. Finished diagrams and a description of the analog hardware for the operator's guide remain to be prepared.



## 5. NEXT QUARTER PLANS

During the next quarter EROS implementation and checkout is scheduled for completion. The unit assembly and system integration will be performed, and the user's manual will be completed. The final report will be drafted at the end of next quarter.

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US ARMY ELECTRONICS COMMAND  
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TITLE OF REPORT: Environment and Radar Operation Simulator (EROS)  
CONTRACT NUMBER: DAAB-74-C-0272  
CONTRACTOR: Georgia Institute of Technology

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