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TRANSMISSION OF ANALOG SIGNALS USING BURST TECHNIQUES.(U)
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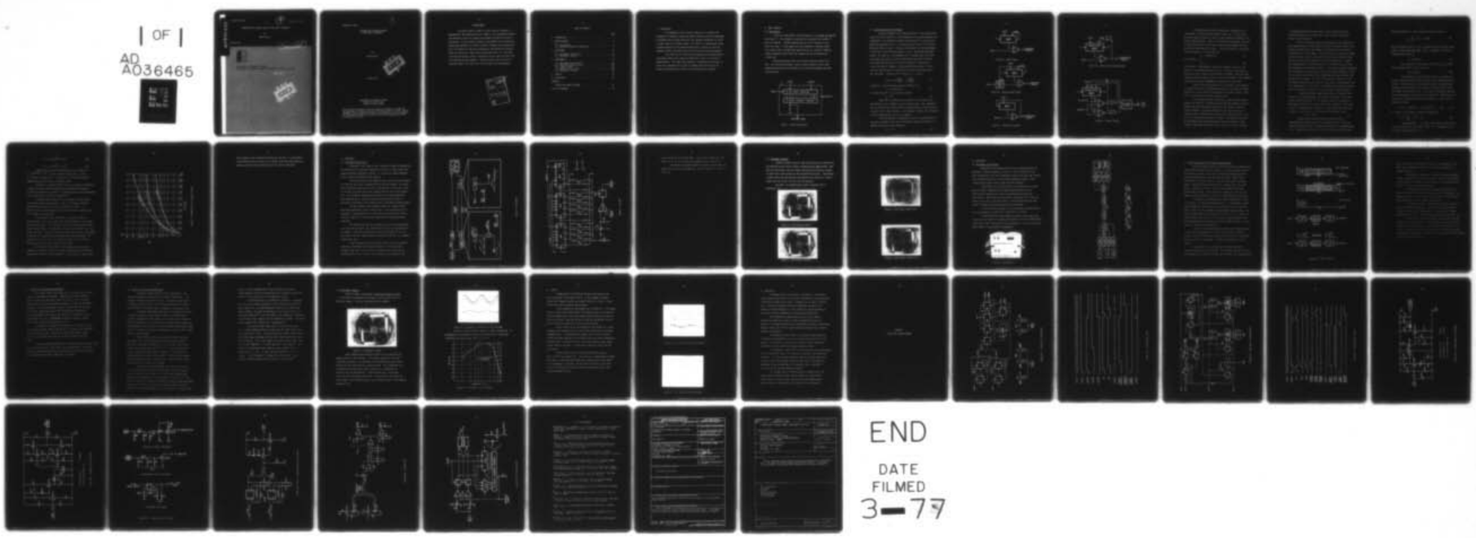

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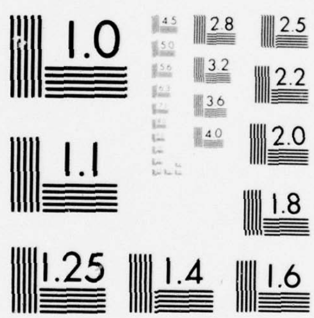

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TRANSMISSION OF ANALOG SIGNALS USING BURST TECHNIQUES

by

MARTIN WOLFF

January 1977

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

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This work was supported in part by Contract No. N00014-75-C-0982 and the Department of Computer Science at the University of Illinois, Urbana-Champaign, and was submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering, at the University of Illinois.

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1. INTRODUCTION

The fundamental idea of burst processing is to combine the advantages of stochastic processing (utter simplicity) with the advantages of weighted binary (higher precision with reasonable bandwidth) to obtain a system lying in the middle ground. The result is a system which allows continous processing of non-synchronized signals yielding low precision immediate results and higher precision final results through averaging.[1]

The simplicity of circuitry and minimization of synchronization requirements makes burst processing potentially useful in the area of communications. This paper then proposes to investigate various ways in which burst techniques can be used in communications and to give the design considerations and results of three demonstration systems.

2. BURST ENCODING

2.0 Burst Basics

A basic building block in burst processing is the Block Sum Register (see Figure 1). The voltage sum represents an average of the contents of the shift register. The BSR therefore can act as an integrator on the input bit stream. If each group on N bits represents a complete sample of an analog signal, the BSR does indeed function as a perfect integrator. Standard compacted bursts[2] have this property and can be decoded with a simple BSR.

Modifying the BSR allows various other encoding schemes to be used. With bidirectional BSRs, a form of delta modulation can be used. Companding becomes easily realizable in this case with weighted non-equal current sources.

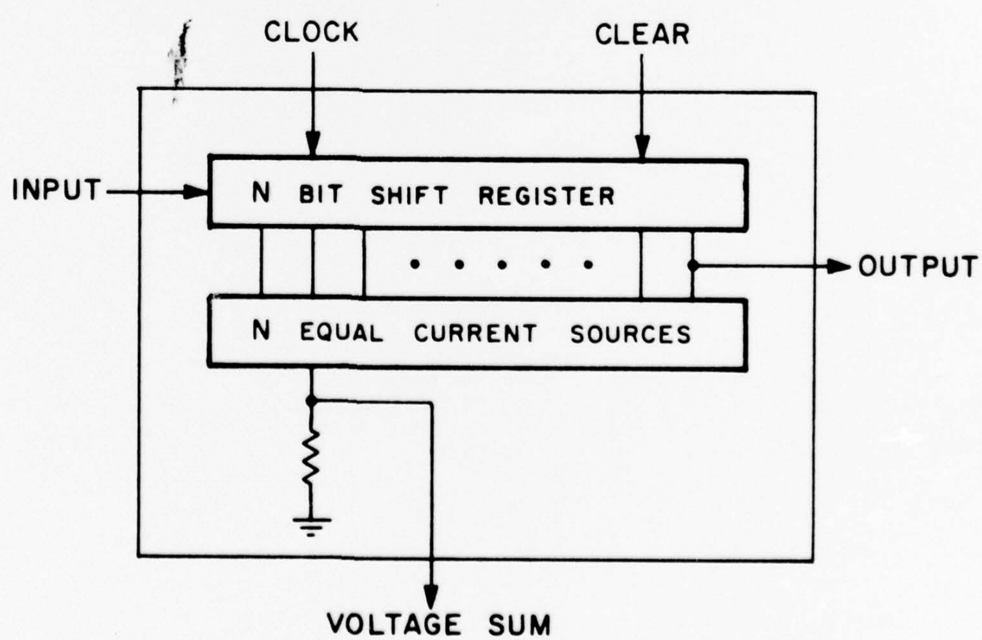


Figure 1. Block Sum Register

2.1 Encoding Using Burst Techniques

The burst encoder in the original proposal[1] is the ramp encoder (Figure 2a) which consists of a BSR connected as a stairstep generator and a comparator. The comparator compares the stairstep to an analog input generating compacted bursts, i.e. bursts where all ones or all zeros are contiguous within a sample. The basic ramp encoder has the disadvantage of requiring a relatively high sample bit rate. Because the stairstep samples the input at a time dependent on its voltage level, the input must change less than one level of quantization during one stairstep to prevent additional noise from being introduced.[3] Specifically, a 1Vpp sine wave of frequency f_c with maximum slope around $t = 0$ must vary less than one level of quantization $1/N$ (for N bit bursts and a 1 volt stairstep). Therefore for bit rate f_s ($t = \pm 1/2f_s$),

$$1/N > .5\left(\sin\frac{N2\pi f_c}{2f_s} - \sin\frac{-N2\pi f_c}{2f_s}\right) \qquad (1)$$

or where F_s is the normalized sampling frequency f_s/f_c

$$F_s > N\pi/\mathrm{ARCSIN}(1/N) \qquad (2)$$

For large values of $N \times F_s$ equation 2 becomes

$$F_s > N^2\pi \qquad (3)$$

Note that all transmissions discussed in this thesis (with the exception of 2e - BIBURST) are non return-to-zero. This implementation is different from transmissions in previous papers on Burst Processing which are all return-to-zero. Given external clocking, the non return-to-zero system would be used in real systems.

With the addition of sample/hold circuitry (Figure 2b) the bit rate can be reduced to the level of the Nyquist sampling criterion, i.e. samples at twice the signal frequency,

$$F_s > 2\,N \qquad (4)$$

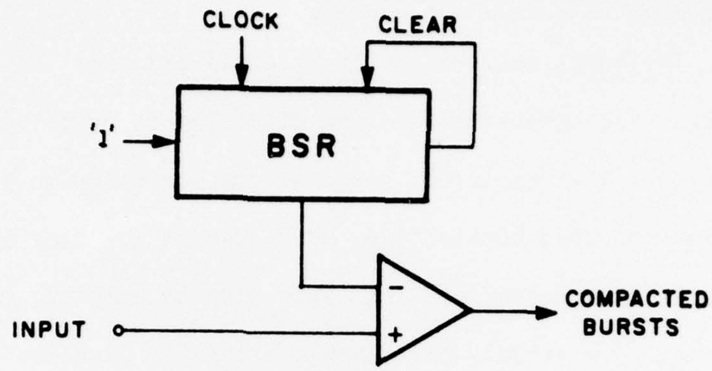


Figure 2a. Ramp Encoder

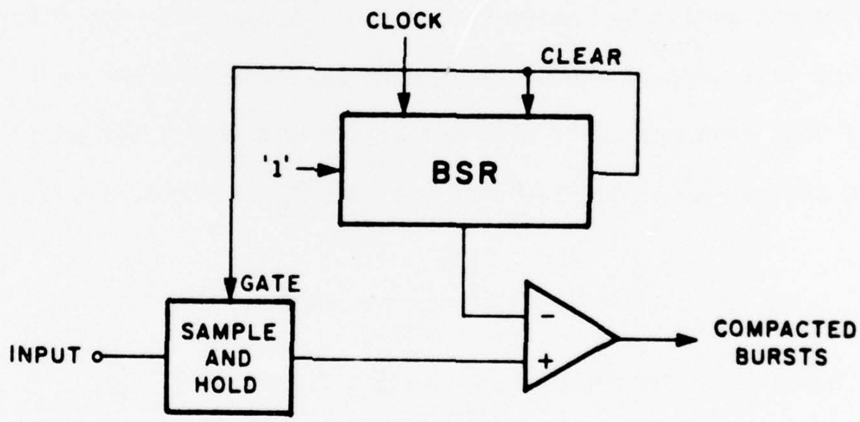


Figure 2b. Improved Ramp Encoder

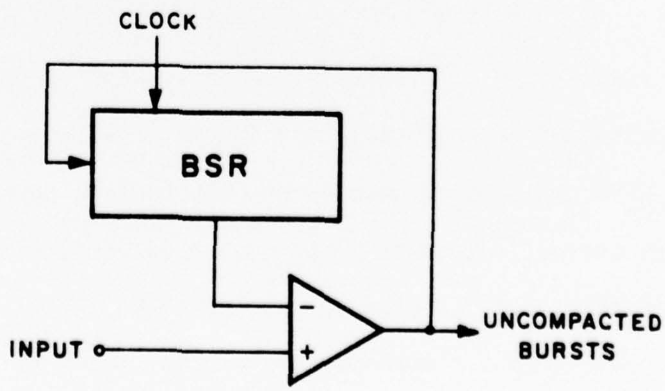


Figure 2c. Delta Block Encoder

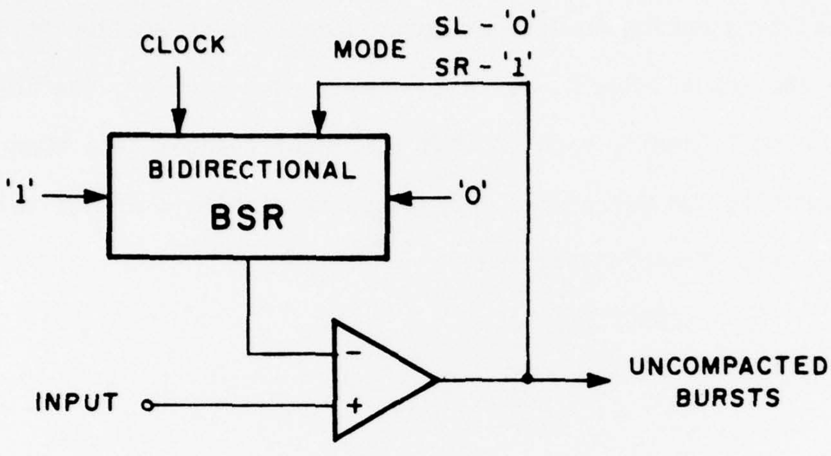


Figure 2d. Improved Delta Block Encoder

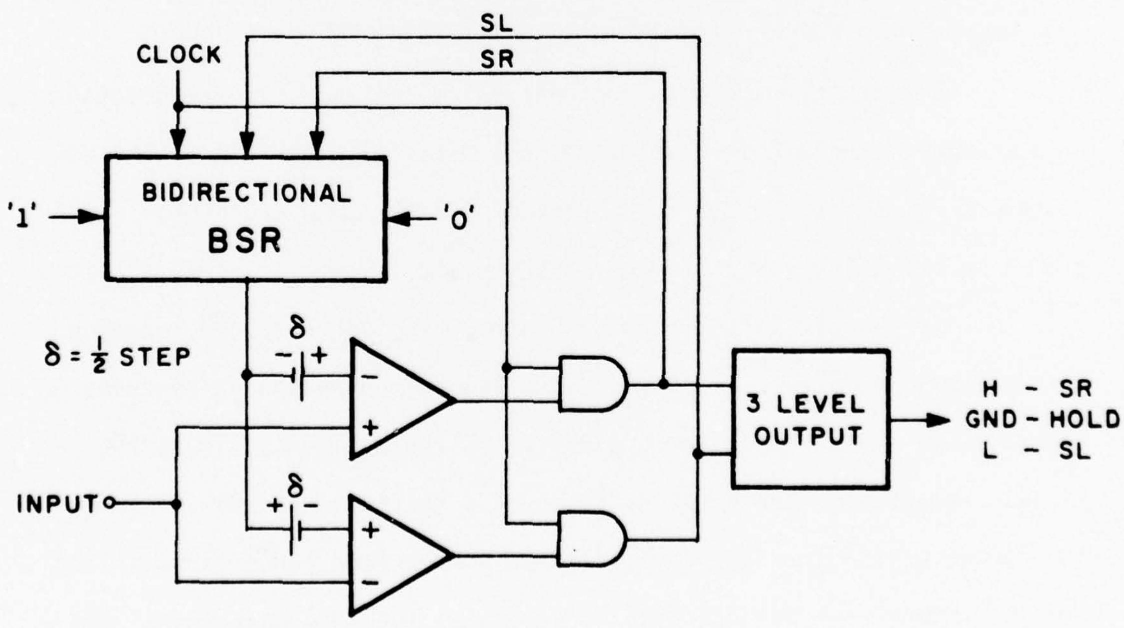


Figure 2e. Biburst Encoder

A different encoder using the same basic components as the ramp encoder is the delta block encoder[4] (Figure 2c). The BSR tracks the input signal by clocking in ones or zeros depending on whether it is below or above the input. Again, as in the basic ramp encoder, the burst bit rate must be sufficiently high so that the input changes less than one level of quantization per sample. Since a new sample is effectively taken with each bit, it would seem that

$$F_s > \pi/\mathrm{ARCSIN}(1/N) \tag{5}$$

or for large $N \times F_s$

$$F_s > \pi N \tag{6}$$

is sufficient. Unfortunately, the BSR only changes its value if the input bit is the opposite of the final bit. If the bit falling off is the same as the bit coming in the BSR does not change. Since the input signifies a desired change, this error must be eliminated. The tracking of the input must be made independent of the history of the signal.

Figure 2d using bidirectional shift registers is one solution. An increase of the BSR is guaranteed regardless of the state of the BSR (assuming of course the BSR is not already full of ones or zeros). Equation 5 is now valid for a single frequency input.

For a bandlimited input, obtaining a slope overload relation becomes more difficult. Extensive work has been done analyzing noise in conventional delta-modulation systems which the system in Figure 2d closely resembles. The major difference is that using a BSR as an integrator gives a maximum and a minimum output (and hence input if the BSR is to track the whole input) DC voltage. The theoretical analyses of conventional delta-mod have assumed no absolute maximum DC input voltage, instead they have dealt with an input of a certain rms power.

A straightforward method of determining a slope overload criterion for the BSR system will be given after a short review of some useful results in the literature.

Noise in delta-mod systems can be grouped into two categories; slope overload noise or noise caused by failure to track the input in the regions of maximum slope, and granular or quantization noise inherent in quantizing an analog signal. Since the input is not excursion voltage limited, any input slope is possible for a bandlimited signal and slope overload results must be expressed in terms of probabilities. O'Neal[5] and Protonotarious[6] have obtained results for slope overload noise with good agreement with experimental results. Using curves they have calculated, one can determine an optimal step size given a sampling frequency. Below this step size slope overload noise predominates and above the step size granular noise increases. For a RC limited gaussian input and $F_s = 64$ for example, the optimum step size for a $1V_{pp}$ input is approximately .047. This corresponds to a 21 bit BSR in a BSR system even though the calculations are not exactly correct for the DC maximum limited BSR system.

To totally eliminate slope overload noise, a frequently used criterion is to set the maximum slew rate of the encoder to four times the rms slope of the input.[7,8] For gaussian signals, the probability that slope overload error can occur under these conditions is less than 4×10^{-5}.[9] Expressing this relation for a $1V_{pp}$ system with step size $1/N$ and $F_s = f_s/f_c$ where f_c is the cutoff of the gaussian input,

$$F_s > 4\pi N/\sqrt{6} \tag{7}$$

Granular noise has been examined rigorously[5,7] but a crude method exists which gives quite accurate results.[10] The noise spectrum of granular noise is assumed to be white over a bandwidth equal to f_s. Given that noise error can vary from $-1/N$ to $+1/N$ at any time with equal probability, total average noise power is equal to

$$\frac{N}{2} \int_{-1/N}^{1/N} x^2 \, dx = 1/(3N^2). \tag{8}$$

The non-filterable portion of this (frequencies within the signal bandwidth) is clearly the total power x f_c/f_s. Therefore, for the non-filterable noise power N_g,

$$N_g = 1/(N^2 F_s{}^2 3) \tag{9}$$

Since the maximum signal power is 1/8 for this 1V_{pp} system, for the maximum signal to noise ratio S/N,

$$S/N = \frac{3}{8} (NF_s)^2 \tag{10}$$

A straightforward slope overload criterion is possible for the BSR integrator system because the input must be maximum amplitude limited. The maximum slope of a bandlimited input is dependent upon the maximum slope possible at the output of the bandlimiting filter with some finite amplitude input. In the case of cascaded RC sections, the maximum possible slope occurs with a step input. Specifically, for step size 1/N and normalized sampling frequency $F_s = f_s/f_c$ with $2\pi f_c$ being each RC pole,

$$1 - e^{-2\pi f_s} - 2\pi F_s e^{-2\pi F_s} - (2\pi F_s)^2 \frac{1}{2!} e^{-2\pi F_s} \ldots < \frac{1}{N} \tag{11}$$

or, where m is the number of identical cascaded RCs,

$$1 - e^{-2\pi F_s} \sum_{i=0}^{m} (2 F_s)^i / i! < \frac{1}{N} \tag{12}$$

A more meaningful F_s for higher order filters is the ratio of f_s to the -3dB point of the overall filter. For m cascaded RCs with an overall half power point of f_c',

$$(1 + (f_c'/f_c)^2)^{m/2} = 2^{1/2} \tag{13}$$

or

$$f_c' = f_c\,(e^{\ln(2)/m} - 1)^{1/2} \tag{14}$$

Equation 12 can be used substituting F_s' for F_s where $F_s' = F_s \times (e^{\ln(2)/m} - 1)^{1/2}$. Figure 3 shows the curves for m = 1 and m = 2 with F_s' instead of F_s. The value of N is the maximum possible where the only source of noise is granular noise.

Figure 2e is a modification of Figure 2d involving an additional transmission level yielding synchronization and bandwidth advantages. It shall be referred to as Biburst[11] - uncompacted bursts with bidirectional (plus, ground, minus) levels of transmission.

A Biburst system transmits a bit only when the input differs from the BSR value by more than half a step. The receiver therefore does notneed any clock at all unlike the previous systems. It derives its clock from the edge of the input pulses and if nothing comes in, it holds its current value.

The average bit rate requirement is obviously reduced for Biburst systems. For a $1V_{pp}$ signal with cutoff frequency f_c, the average absolute value slope is f_c. With step size 1/N, the system need transmit only N bits per cycle. A normal delta mod system would transmit $F_s = f_s/f_c$ samples per cycle. Therefore, a Biburst system uses only $N/F_s \times 100$ percent of the bits of a standard delta mod system under these conditions. For example, with $F_s = 64$ and N = 10 (satisfying Figure 3 first order RC), The Biburst bit rate is 15.6 percent of the maximum.

This savings figure refers to the average bit rate, not the bandwidth or maximum bit rate of a channel. Multiplexing multiple Biburst systems over a channel to take advantage of this savings is a possibility.

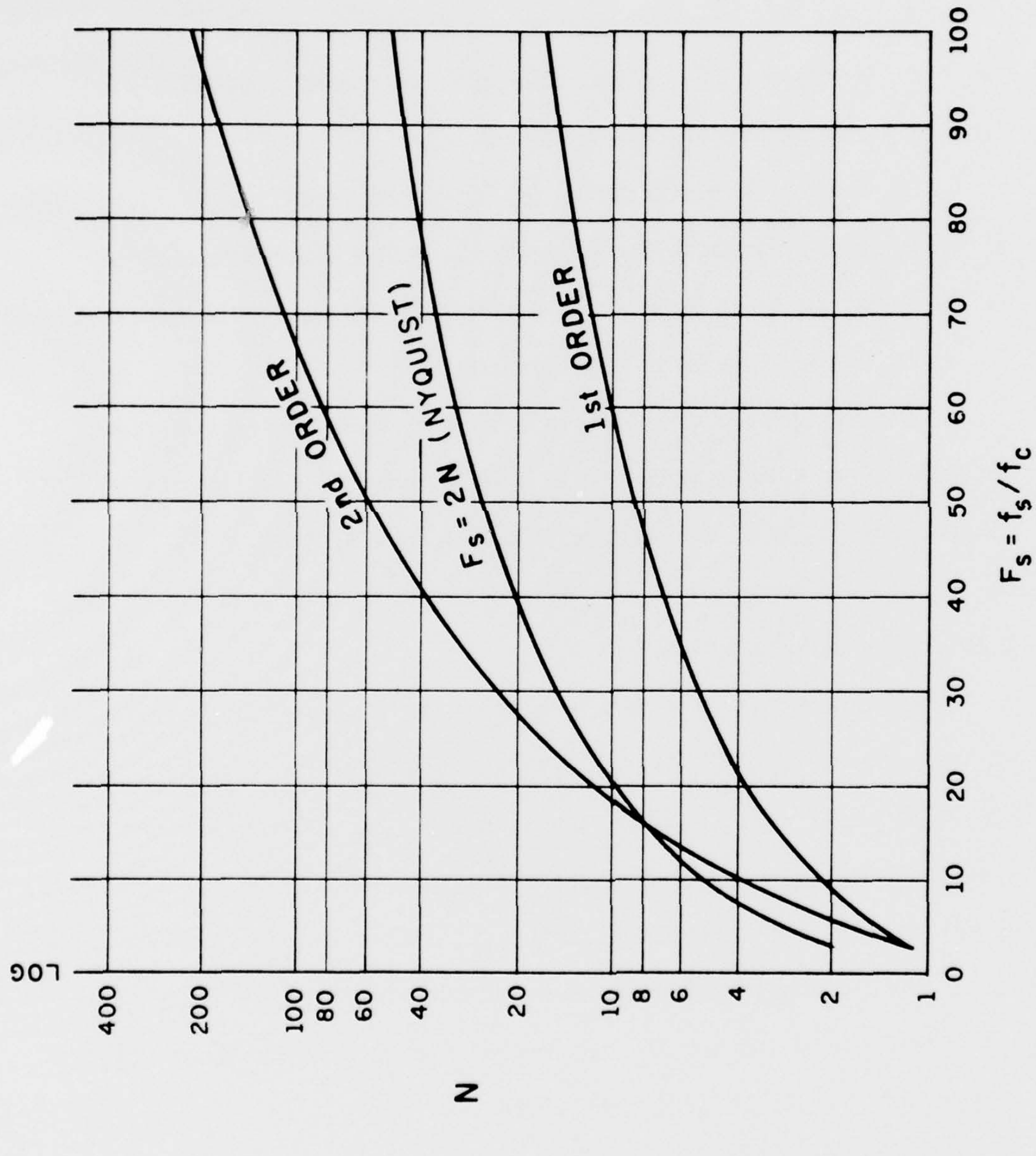


Figure 3. Maximum N for F_s with RC Filters

Martin Newman of the Information Engineering Laboratory is investigating multiplexing multiple stations over a channel using amplitude addressing - where a specific station transmits pulses of specific amplitudes.

3. BURSTCOMM I

3.0 Burstcomm I Description

Burstcomm I (see Figure 4) was a successful attempt to demonstrate the feasibility of using burst techniques to transmit a video signal with readily available integrated circuitry. It also gave a graphic demonstration of digital thresholding noise immunity.

The video portion of the composite video signal was burst encoded at a 50 M Bit rate using a nonsample/hold 10 bit ramp encoder. The bursts were transmitted along a twisted pair to the decoder--a 10 bit BSR. Noise in the form of periodic pulses was injected into one line of the twisted pair. This system was compared with straight co-ax video transmission with identical noise. The pulse height was adjusted to be equal in amplitude to the height of the video portion of the composite analog signal.

The sync portion of the composite signal was clipped off and transmitted separately from the video portion. This was necessary for a reasonable visual demonstration so that sync was kept through all levels of noise. When sync is lost, picture deterioration comparisons become impossible.

Not encoding the sync also allowed all 11 levels of quantization to be used for grey scale. ECL 10,000 series ICs were used throughout for two reasons: ease of use at 50 M Bits relative to Schottky T^2L and the fact that a very high speed comparator (10116 line receiver) is a standard 10,000 series chip.

A BSR was made with shift registers (10141) with high speed PNP transistors (MPS 3640) at each output (Figure 5). Since ECL output voltages range from -.9 to -1.8 volts and the buss sum voltage was set well below that (-5 to -4 volts), the transistors were operated in the

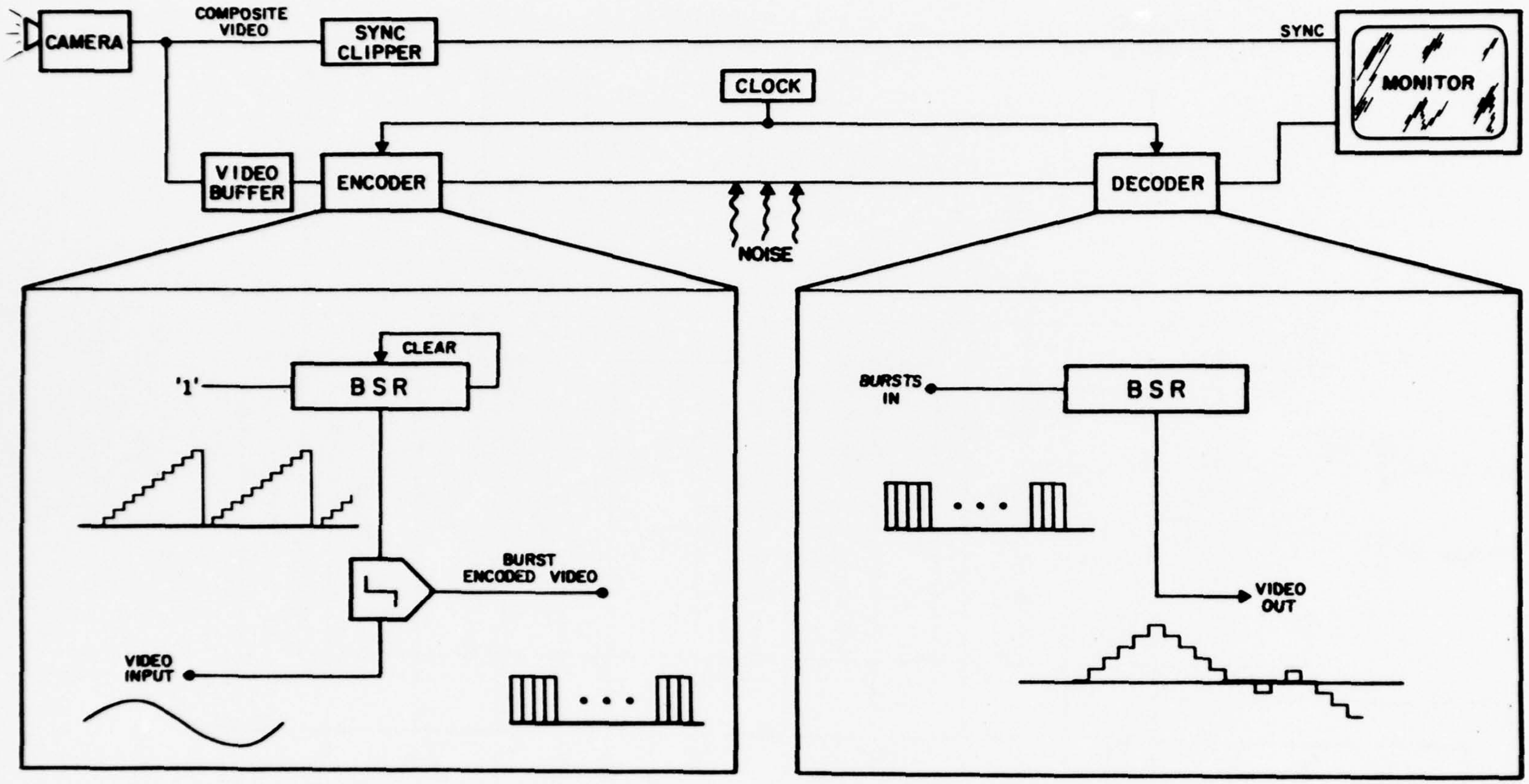


Figure 4. Burstcomm I

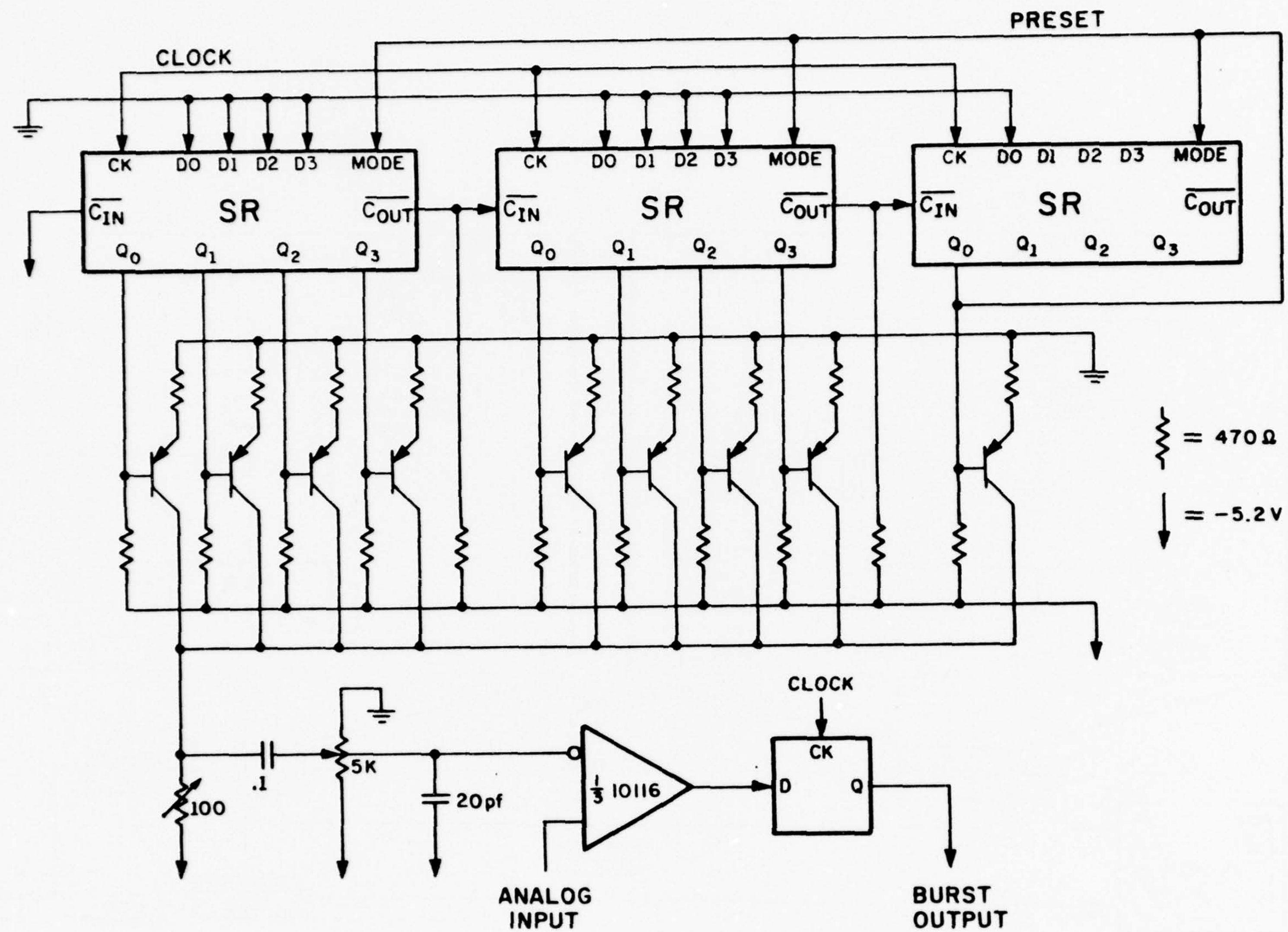


Figure 5. ECL BSR

active region only for maximum speed. The buss sum voltage was level shifted up to ~ 2v DC average to be compatible with a 10116 input.

The encoding and decoding BSRs were identical except that the encoder had 9 bits to the decoders 10. Each fit into a 2" x 1 1/2" x 3 1/4" box.

3.1 Burstcomm I Results

Figures 6 through 9 give an idea of what quality of transmission was attained and how clearly digital thresholding was demonstrated. Note that the ramp encoder used was without sample/hold and hence was subject to significant slope overload on the non-bandlimited signal. Nevertheless, a usable result was obtained with the superior noise immunity of digital signals and the simpler circuitry of burst encoding.

Burstcomm I was demonstrated to ONR in November 1975 in Washington, D.C.

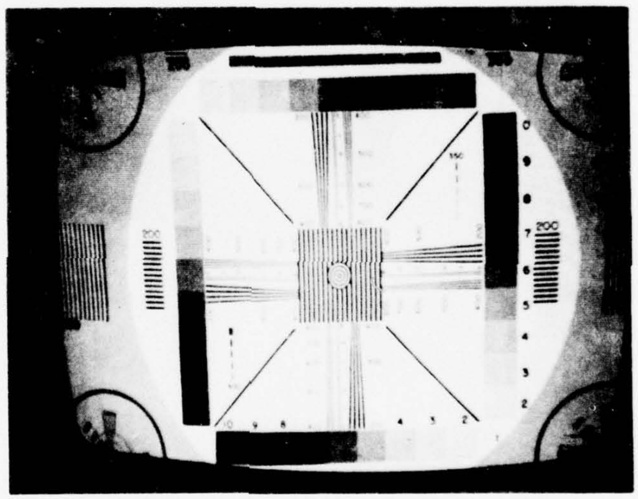


Figure 6. Co-Ax Video, No Noise

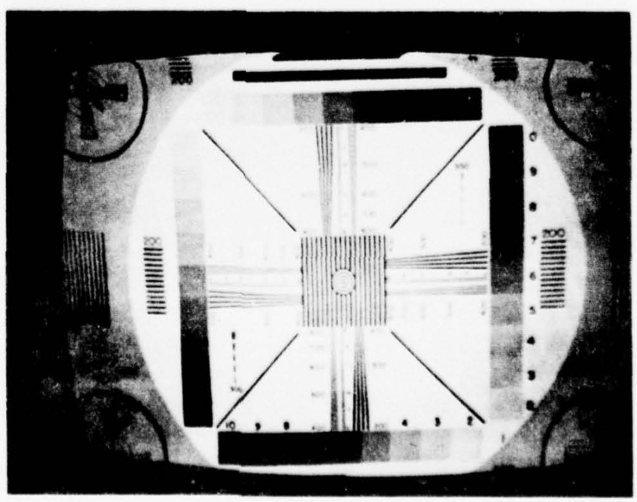


Figure 7. Burst Video, No Noise

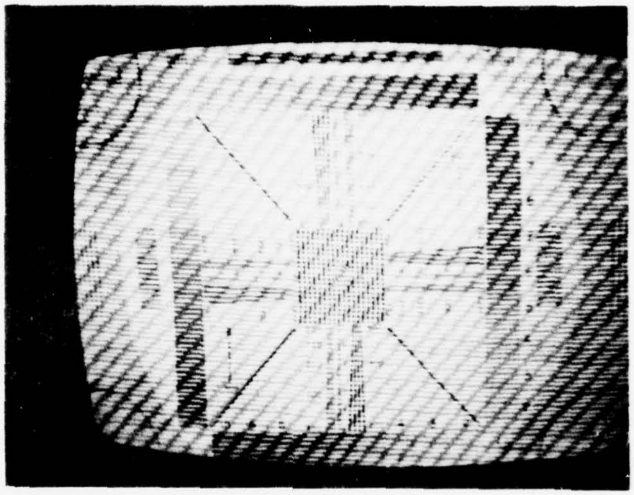


Figure 8. Co-Ax Video, Severe Noise

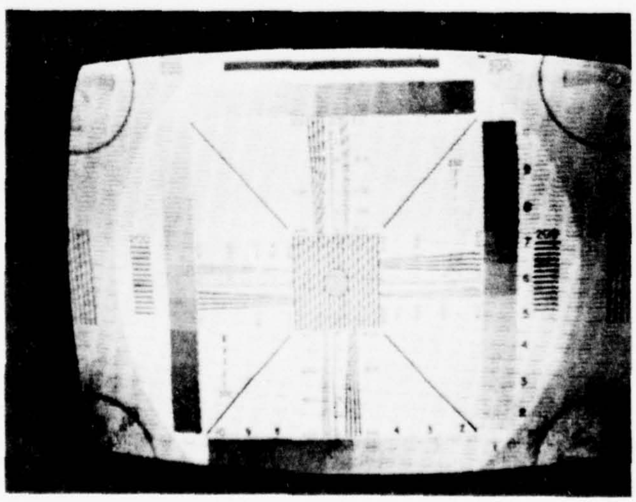


Figure 9. Burst Video, Severe Noise

4. BURSTCOMM II

4.0 Burstcomm II Description

Burstcomm II was designed and built as an improved version of Burstcomm I using the same basic circuitry. With the addition of one extra transmission level, sync information as well as an audio and a sensor line are added (Figure 11). The resulting multiplexed signal is transmitted along an optical fiber to gain total EMI immunity.

Specifically, positive going pulses are transmitted for video, audio and sensor information while negative going pulses indicate horizontal and vertical sync as well as the beginning of audio and sensor bursts. Audio bursts are sent every H sync pulse (15.75 KHz) and sensor bursts every V sync pulse (60 Hz). During these times the video signal is blacked out anyway and need not be transmitted.

Circuit and timing diagrams of the multiplexer and demultiplexer are in the appendix as Figures AD-1 through AD-4, pp. 32-35.

The multiplexer and demultiplexer are housed in two boxes (see Figure 10) which contain all encoding and decoding circuitry including audio filter/amps, video filter/buffers and sync generators. They do not contain power supplies or the system clock generator.

Figure 10. Burstcomm II

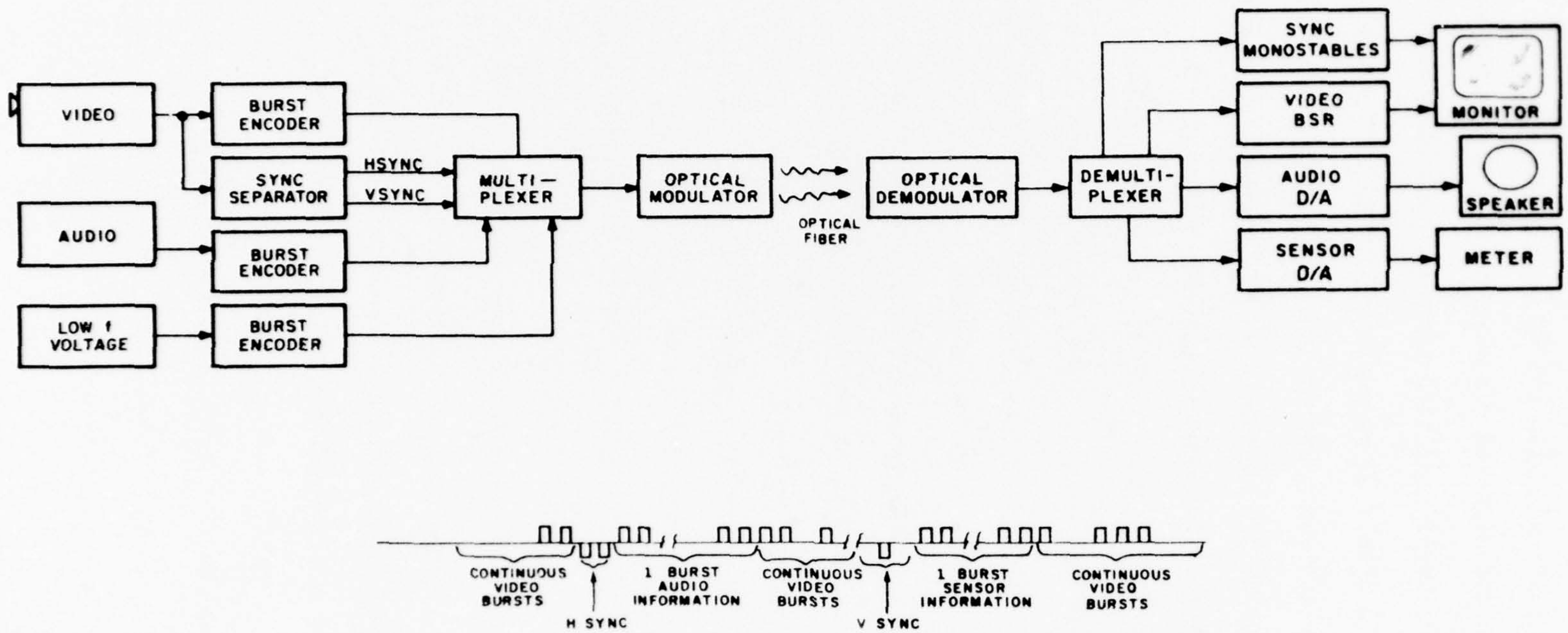


Figure 11. Burstcomm II

4.1 Audio and Sensor Circuits Design Considerations

Due to the high--50 M Bit--bit rate, the audio and sensor bursts can be treated as sample and hold samples. No slope overload can occur in the 200 ns (10 bits x 20 ns per bit) needed to generate each burst with the bandlimited audio and the nearly DC sensor. Specifically, from Figure 3 for 10 bit bursts, $F_S > 60$ for first order RC filtered inputs. Since the filter used (see AD-5) is greater than first order and $F_S = 50\text{ MHz}/(10 \times 3.2\text{KHz}) = 1563$, the audio samples are clearly without slope overload. Since the audio is sampled at 15.75 KHz, the Nyquist criterion dictates a cutoff of 7.87 KHz before aliasing occurs.

To transmit a voice grade audio signal a bandwidth of 3.2 KHz is sufficient. To reduce quantization error it is desireable to encode higher frequencies as well as providing that they can be filtered out and that they will not be folded into the desired frequency range. The cutoff frequency then for the encoder filter is 15.75 - 3.2 = 12.55 KHz. Aliasing which occurs from 3.2 KHz to 12.55 KHz does not matter since those frequencies will be filtered out at the decoder end with a 3.2 KHz low pass. Figure 12 illustrates this.

Since real filters do not have the abrupt cutoff characteristics of ideal ones and components for filters come in certain convenient values, the actual filters constructed were a 5.5 KHz LPF in the encoder and a 3.2 KHz LPF in the decoder. Figures AD-5 and AD-6, pp. 36-37, circuits.

The encoder LPF is acutally one-third order constant-k π section cascaded with two RC sections. The "faithless constant-k"[12] was used because of its simplicity and the fact that the filter characteristics

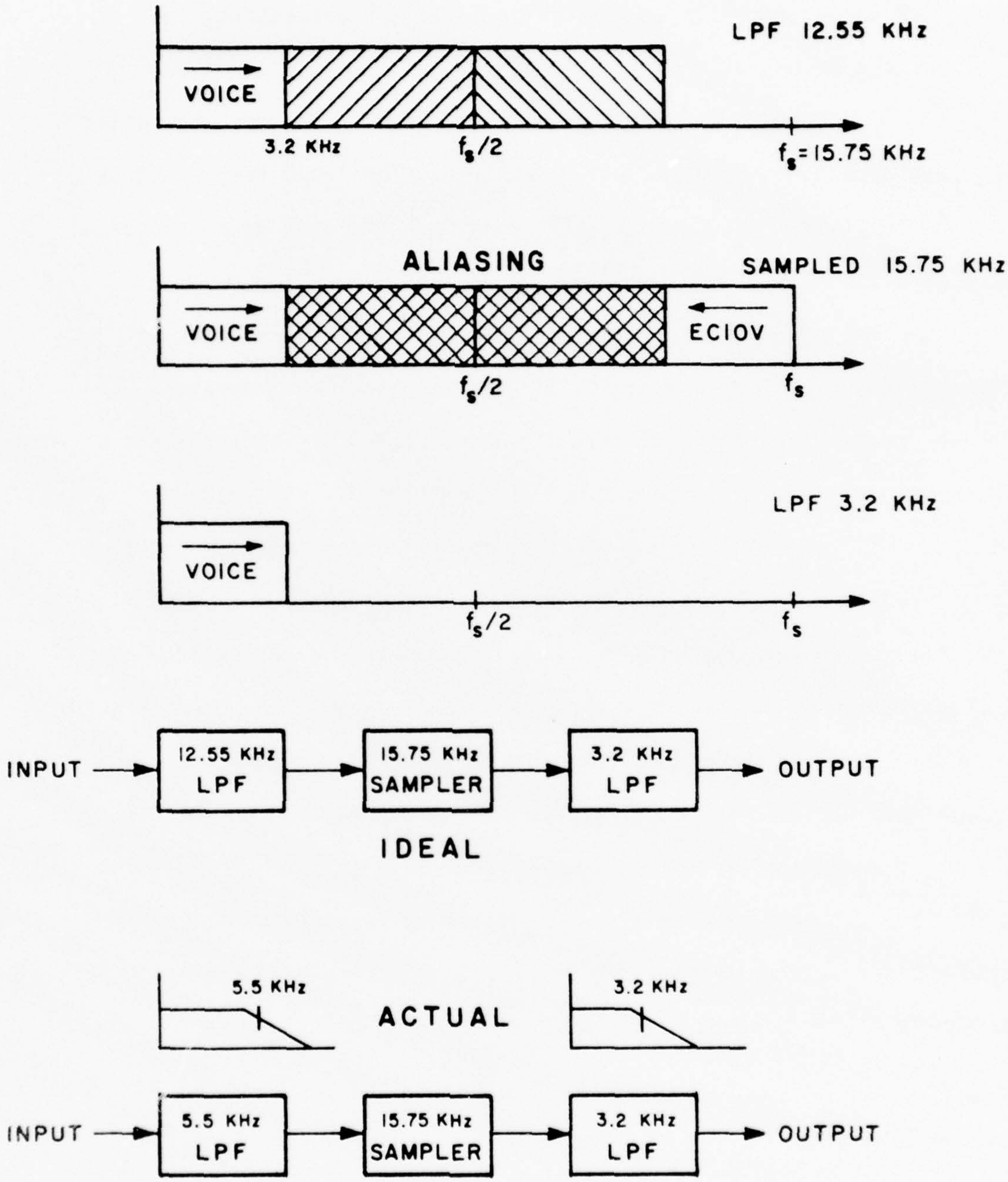


Figure 12. Audio Filtering

were not critical. With the two RCs, ripple in the passband is less than 1 dB and attenuation at the critical 12.55 KHz frequency is greater than 20 dB.

The decoder LPF consists of a 3.2 KHz third order constant-k low pass cascaded with a low Q 7.9 KHz trap. The low Q trap flattens out the constant-k response as well as making sure that granular noise at $f_s/2$ = 7.9 KHz is down more than 20 dB.

The encoder circuit is also a pre-amp which amplifies an input from a high Z microphone to $1V_{pp}$ levels for the comparator. The decoder includes an audio amp which runs off of 5.2 V and provides a $3V_{pp}$ output across an 8 ohm speaker (1/4 watt RMS).

The decoder consists of a counter/D-A converter instead of a BSR to reduce the package count. Due to the fact the audio bursts arrive as separate burst samples there is no need for the "window" characteristic of a BSR. The sensor decoder is also a counter/D-A pair.

The D-As consist of PNP transistors wired up just like a BSR except that the emitter resistors are weighted according to the binary weight of each counter output. Due to the range of currents (8:1 for a four bit counter) the resistor values had to be adjusted for varying base emitter voltage drops. The final D-A is accurate to within 10 percent of the least significant bit.

4.2 Video Circuits Design Considerations

The video circuitry (see Figure AD-7, p. 38) consists of filter-buffers at the encoder and decoder. Again the third order constant-k filter is used, this time with a cutoff of 2.4 MHz. This is near the upper frequency possible with effective samples at 5 MHz from the Nyquist criterion. At this point however, there is significant slope overload error of the time/voltage type of the non-sample/hold ramp encoder. Future improvements could include the addition of sample/hold circuitry to eliminate this error. Nevertheless, Burstcomm I showed a useable visual result is possible even with this error.

The encoder is adjusted to not encode any of the sync portion of the composite video signal since the sync is already being transmitted as negative going pulses. Specifically, two 50 MBit negative going pulses in a row signify HSync and one followed by nothing signifies VSync.

Sync circuitry (also Figure AD-7) included two Schmidt trigger inputs to get clean pulses at ECL logic levels and two monostables at the output. As soon as incoming negative pulses are decoded into vertical or horizontal sync information, the correct monostable is triggered.

4.3 Optical Link Design Considerations

To achieve picture quality similar to Burstcomm I, the optical link needs to transmit bits at a rate of 50 Mbits/sec. This dictates a minimum pulse period of 20 ns. In addition, three levels of intensity have to be sent. The following discussion will refer to Figure AD-8 on p. 40 which contains a schematic of the optical link.

Bifurcated Dolan-Jenner E624 glass fiber bundles are used for a number of reasons; a large diameter (.044") at the transmitting end with consequent efficient coupling in of light, ease of mounting, two LEDs transmitting to one receiver for more total optical power, and most importantly--the fact that a few surplus E624s were floating around the lab. A figure of 45 percent transmittance is given for the 2' fiber bundle at around 650 nm.

Dialco 521-9195 red LEDs were chosen for their relatively high power (for a visible LED), narrow beam (half power into half angle 35o), fast speed of response (1 ns rise and fall time in spec. sheet), and low capacitance (20 pF at V = 0). They are driven with current sources to maximize speed of response. An MPS 3640 PNP is used as each current source at the output of an ECL gate and provides a current swing of 10-40 ma through the LED. Measured optical power output varies from roughly 9 to 31 μwatts.

The receiving end presented many more design difficulties. An initial design using cascaded cascode stages proved too unstable and also lacked sufficient speed. The final simple photodiode-amp combination was derived from a circuit used by a group at GE.[13] The amplifier consists of multiple 1/3 10116 line receivers operating between ground and -5.2V with 10K resistors for negative feedback stability. Only two of the three comparators on the first stage IC are used as the use of all three cascaded leads to high frequency oscillations. The amp operates from DC to around 80 MHz with a measured rise and fall time of 6 ns and a gain of 4.7 volts/μamp small signal.

The photodiode used is an HP4207 PIN photodiode. Advantages of a PIN over an avalance photodiode include decreased sensitivity to power supply noise, increased temperature stability, and lower power supply voltages. The major disadvantage is less output current for a given light intensity.[14] Since Burstcomm II was intended as a demonstration with short fiber lengths, the PIN photodiode was chosen. Calculated current responsivity at 640 nm was 3 μamp/mwatt/cm^2.

Total optical power output swing of the LED is 22 μwatts. For .1" spacing between emitter and fiber and .022" fiber radius, the solid half angle is 12.5°. Using the Dialco spec. sheet, roughly 15 percent of the output power goes into the fiber (ignoring coupling losses from reflection). Flux at the output of the fiber (radius .0625") then is $22 \times .15/((.0625/2)^2 \times \pi \times 2.54^2)$ μwatt/cm^2 = .167 mwatt/cm^2. The output of the photodiode (again ignoring losses between fiber and photodiode) is $3 \times .167 = .5$ μamp. The amp output then is $4.7 \times .5 =$ $2.35V_{pp}$. Since the output is clipped at ECL logic levels ($.9V_{pp}$) these calculations indicate that the optical link should work.

4.4 Burstcomm II Results

Figure 13 shows a test pattern transmitted through Burstcomm II. The effects of quantization are clearly visible but the result is definitely useable. Sync was transmitted with no problems.

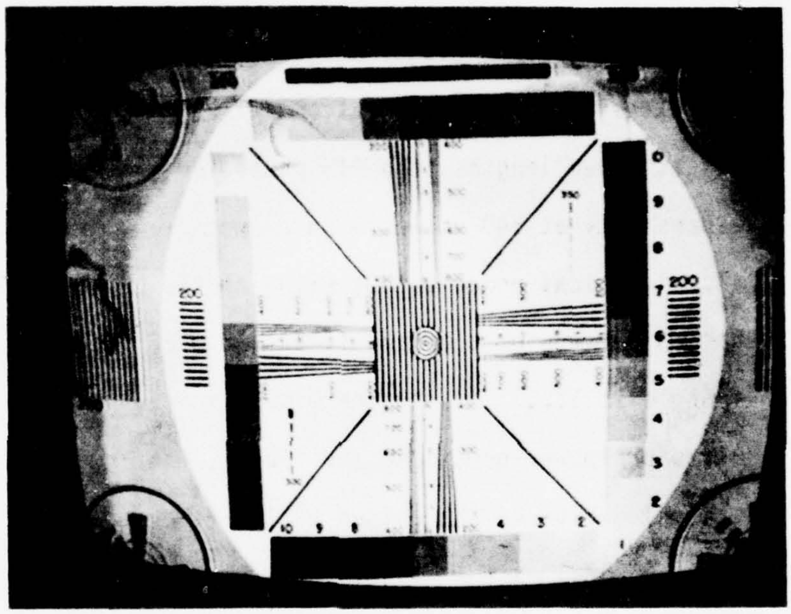


Figure 13. Burstcomm II Video

Audio presented some problems initially with the sensitive mic preamp picking up radio stations. An RF bypass capacitor on the input eliminated the problem. The amplifier on the demultiplexer causes interference with the video when set to maximum volume. This problem would be eliminated by increased power supply filtering or by separating the amplifier from the demultiplexer. Figure 14 shows what a transmitted 1 KHz sine wave (unfiltered) looks like. The top trace is the input, the middle trace is the unfiltered output, and the bottom trace is the difference between the two.

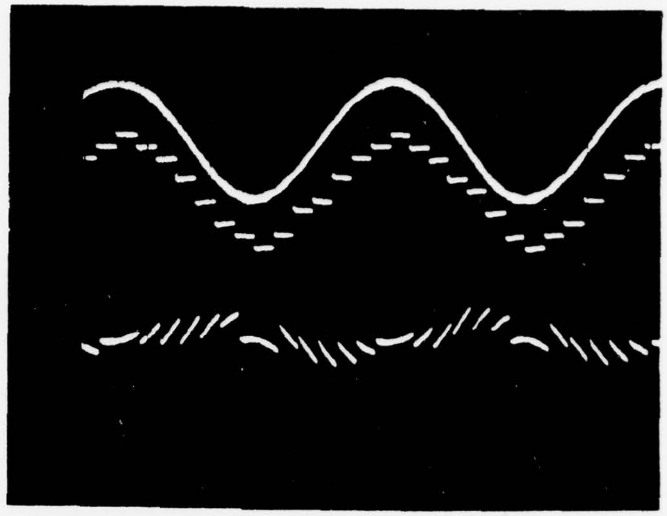


Figure 14. Burstcomm II Transmission 1 KHz Sine Wave

The overall audio frequency response is shown in Figure 15. It corresponds well with what was predicted from the design. The actual -3 dB points are approximately 400 Hz and 3 KHz.

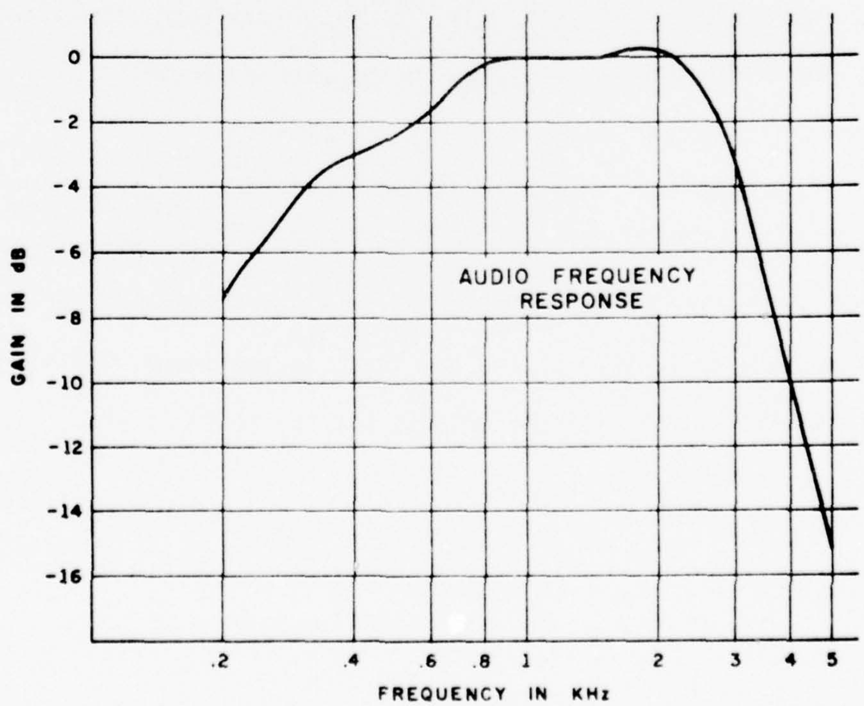


Figure 15. Burstcomm II Audio Response

5. BIBURST

A demonstration of the Biburst encoder (see Figure 2e) was built and tested in the summer of 1975. It was designed to encode/decode audio frequency signals and transmit them with 3 levels of transmission (positive and negative going pulses).

Circuit diagrams for the encoder are in Figure AD-9. The decoder consists simply of the bidirectional shift register with a clock derived from the delayed edge of the input pulses and mode controlled by polarity of the input pulse. Note that to have no clock on the decoder, the bits must of course be transmitted in return to zero notation.

Visual results (on an oscilloscope for the encoding of a single frequency) were quite positive for non-filtered output due to the nature of Biburst error. The encoded signal appears only to lag an input by a phase difference dependent on the slope of the input unlike conventional delta-mod which, in regions well away from slope overload, jumps around on both sides of the input. Filtered errors should be similar for the two systems.

Figures 16 and 17 give an idea of what Biburst encoding looks like for two values of F_s. Even for low F_s, degradation of encoder performance is controlled and gradual and a useable result (even though it is attenuated) is achieved. The top trace is the input, the middle trace is the Biburst non-filtered output, and the bottom trace is the difference between the two.

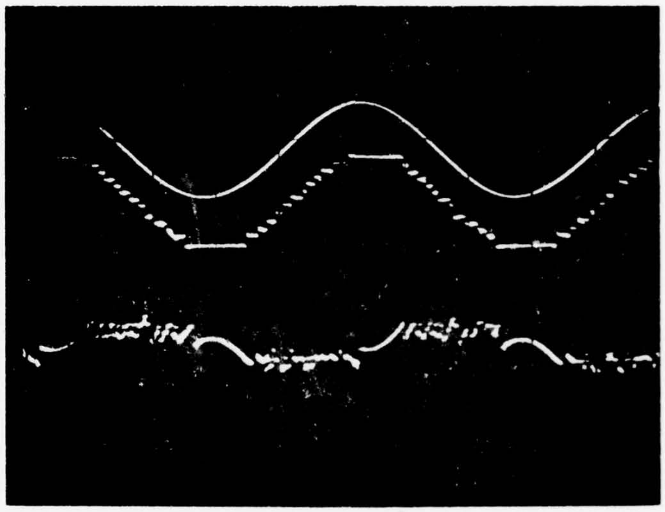


Figure 16. F_x = 100 Noise Amplitude Doubled

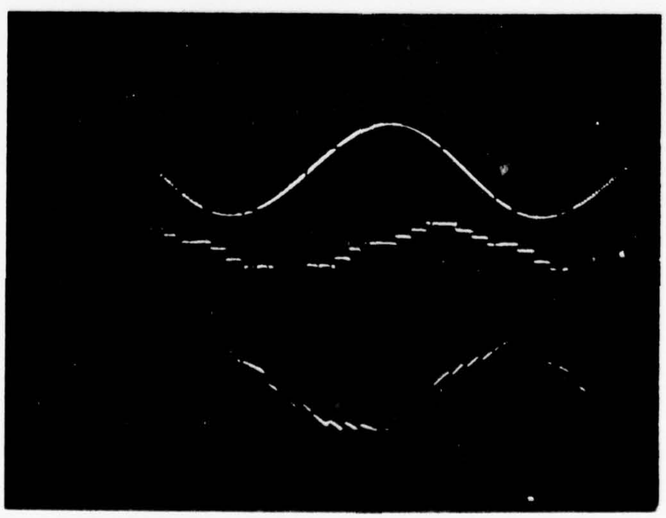


Figure 17. F_s = 20 Noise Amplitude Normal

6. CONCLUSIONS

The demonstrations of Burstcomm I, Burstcomm II, and Biburst clearly show the possibility of using burst techniques in the transmission of digitally encoded analog signals. Depending on the specific application, a version of encoding using burst techniques may prove to be otpimal by taking advantage of circuit simplicity, minimal synchronization, easy intrinsic companding, or multiplexing possibilities.

Ramp encoding with sample/hold circuitry on the input is generally the best burst system in terms of bandwidth and could be optimal if the added complexity of the sample/hold circuitry is permissible. Against standard PCM it offers synchronization advantages versus higher bandwidth requirements.

The absolute simplest system is the original ramp encoder but it requires high bandwidth if its form of slope overload error is to be avoided. If bandwidth is sufficient or the error can be tolerated to some extent, it does provide the cheapest encoding method.

If companding is useful (due to amplitude distribution characteristics of a particular input), a bidirectional delta-mod like system could be optimal. It offers minimum sample bit rates for certain inputs (see Figure 3), those with strongly limited maximum slopes. The major disadvantage is that bidirectional shift registers versus sample/hold circuitry for the s/h ramp encoder are needed.

For ultimate lack of synchronization (no decoder clock) and reduced average sample bit rate, Biburst stands out. Multiplexing possibilities, no sync, and easy companding must be weighed against multiple levels of transmission and increased circuit complexity.

APPENDIX

CIRCUIT AND TIMING DIAGRAMS

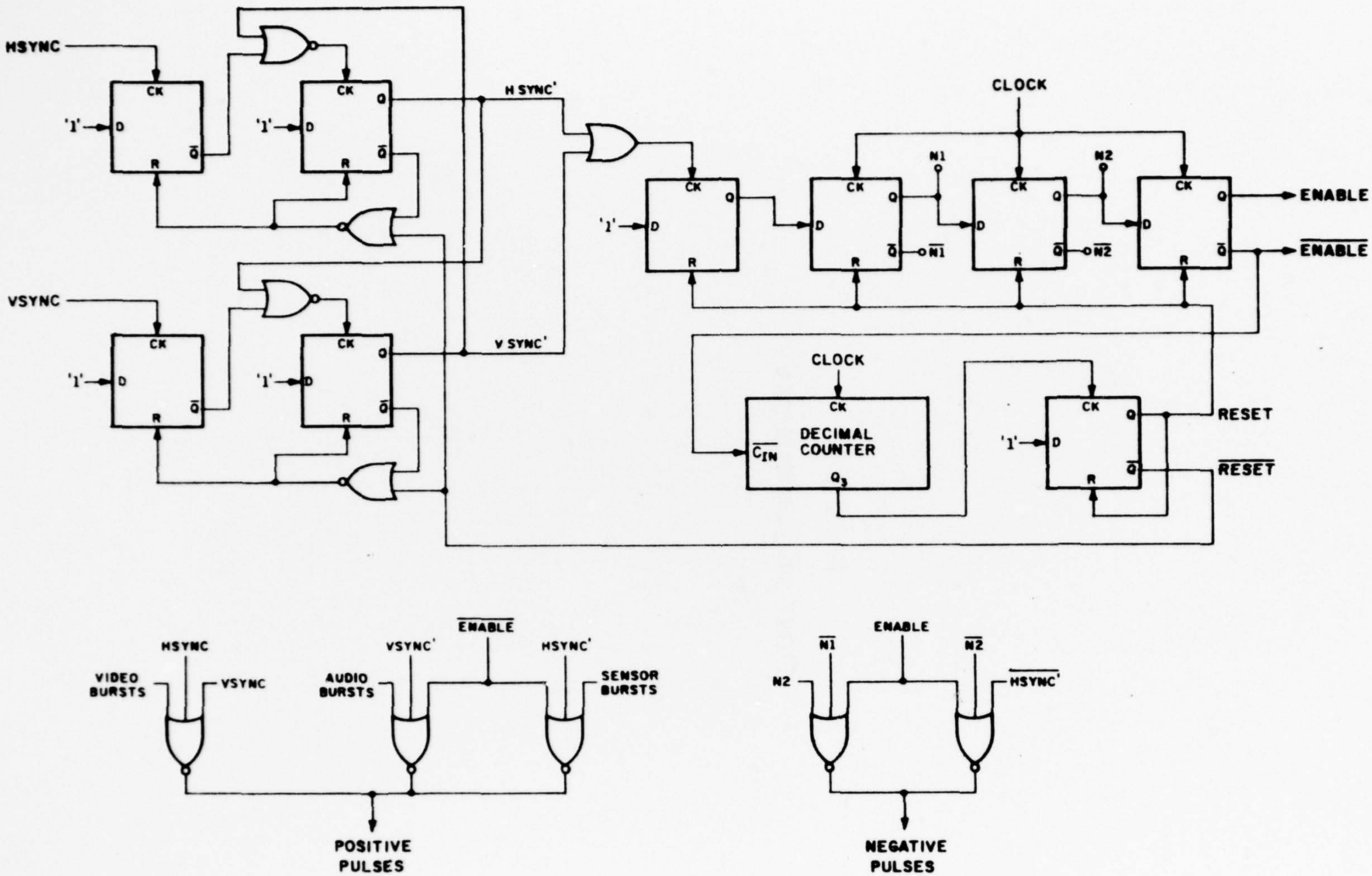


Figure AD-1. Burstcomm II Multiplexer

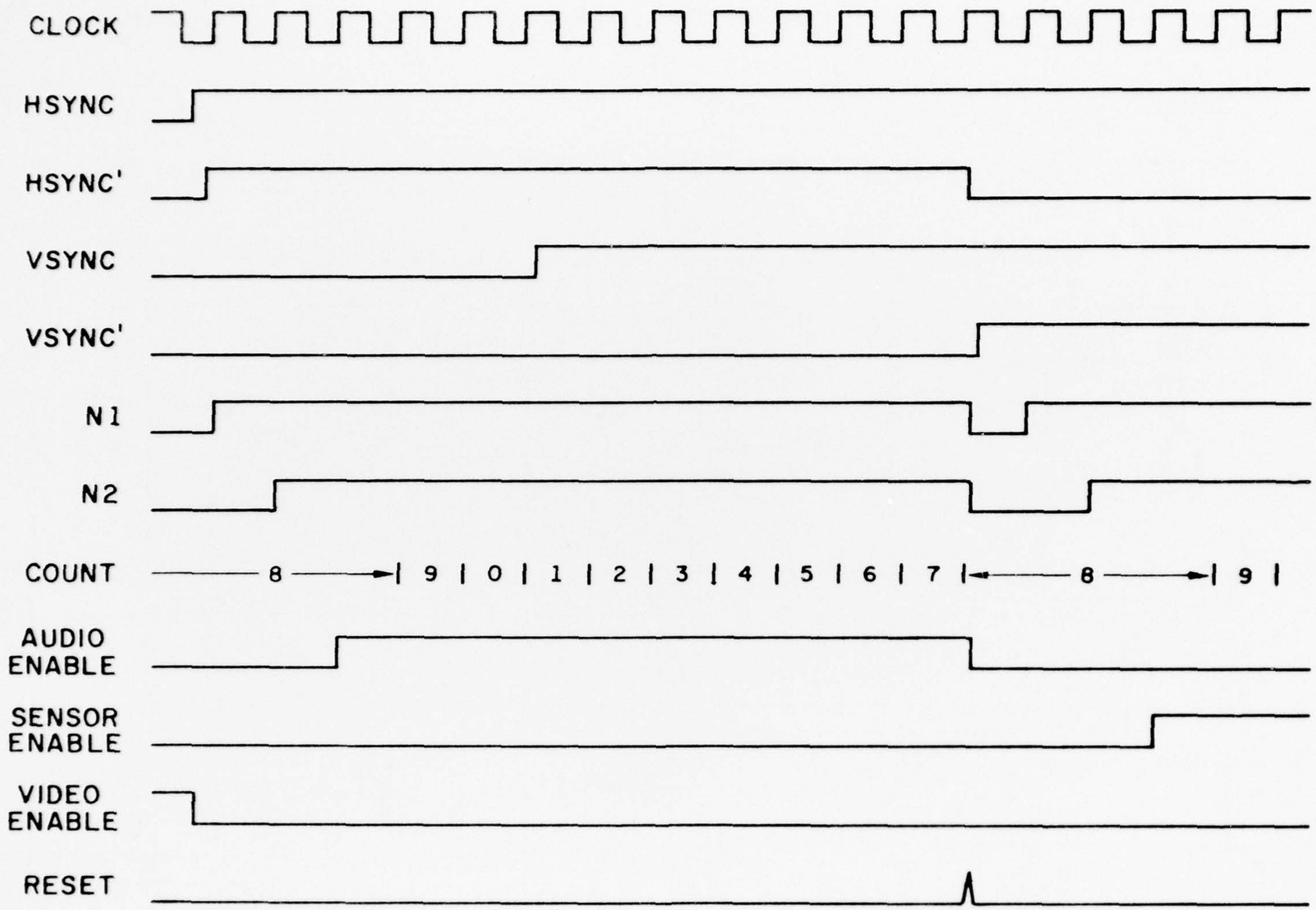


Figure AD-2. Multiplexer Timing

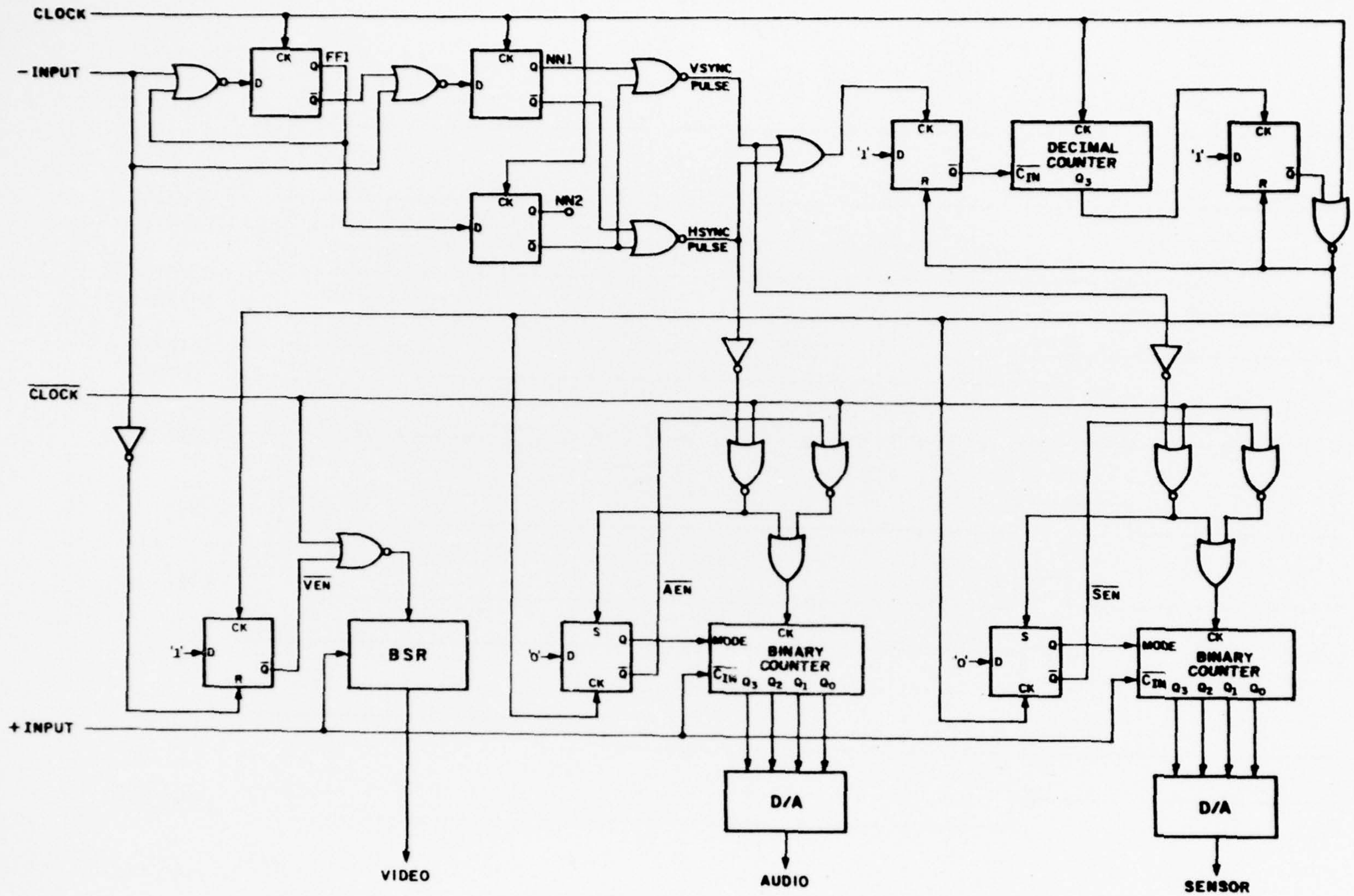


Figure AD-3. Burstcomm II Demultiplexer

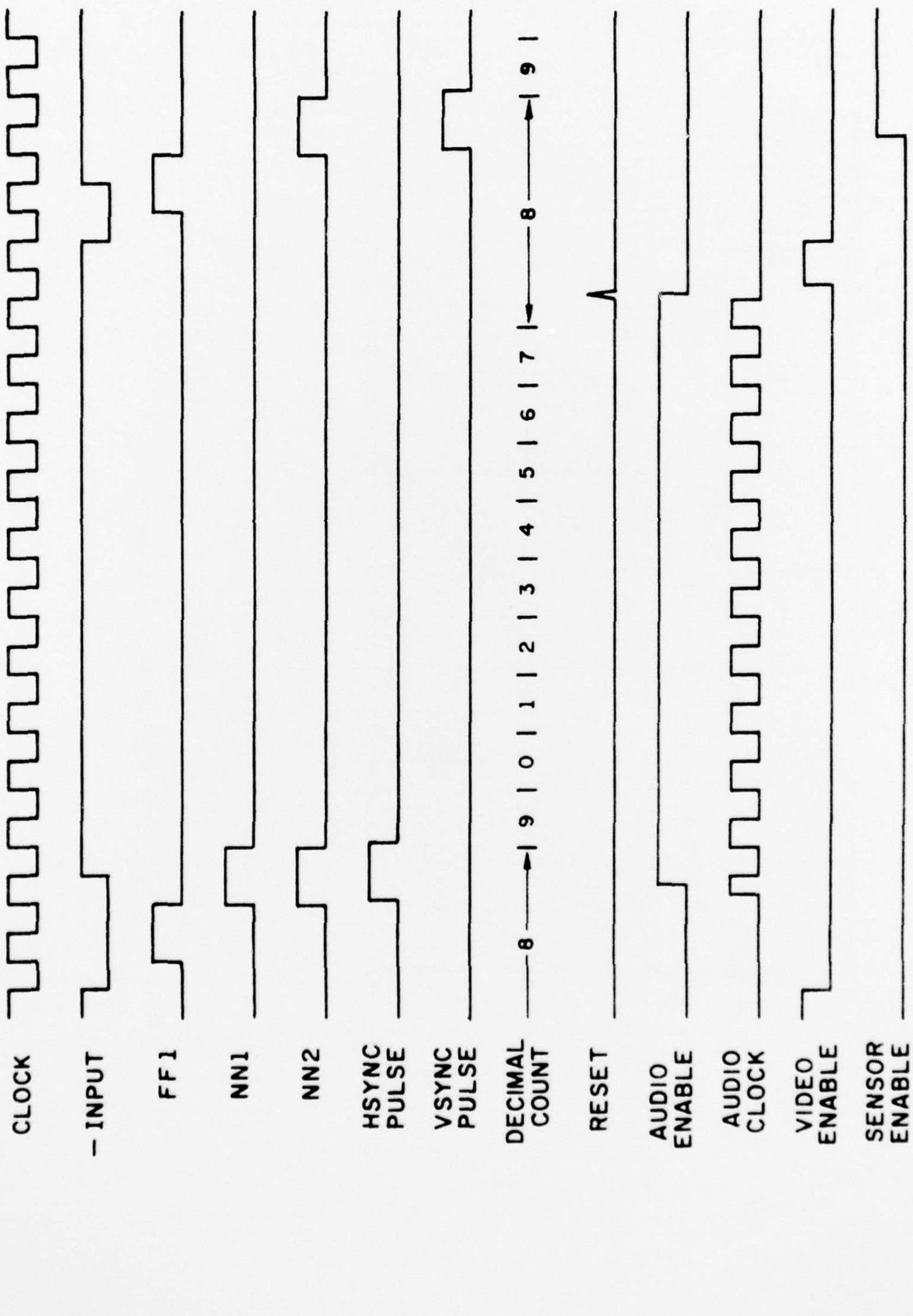
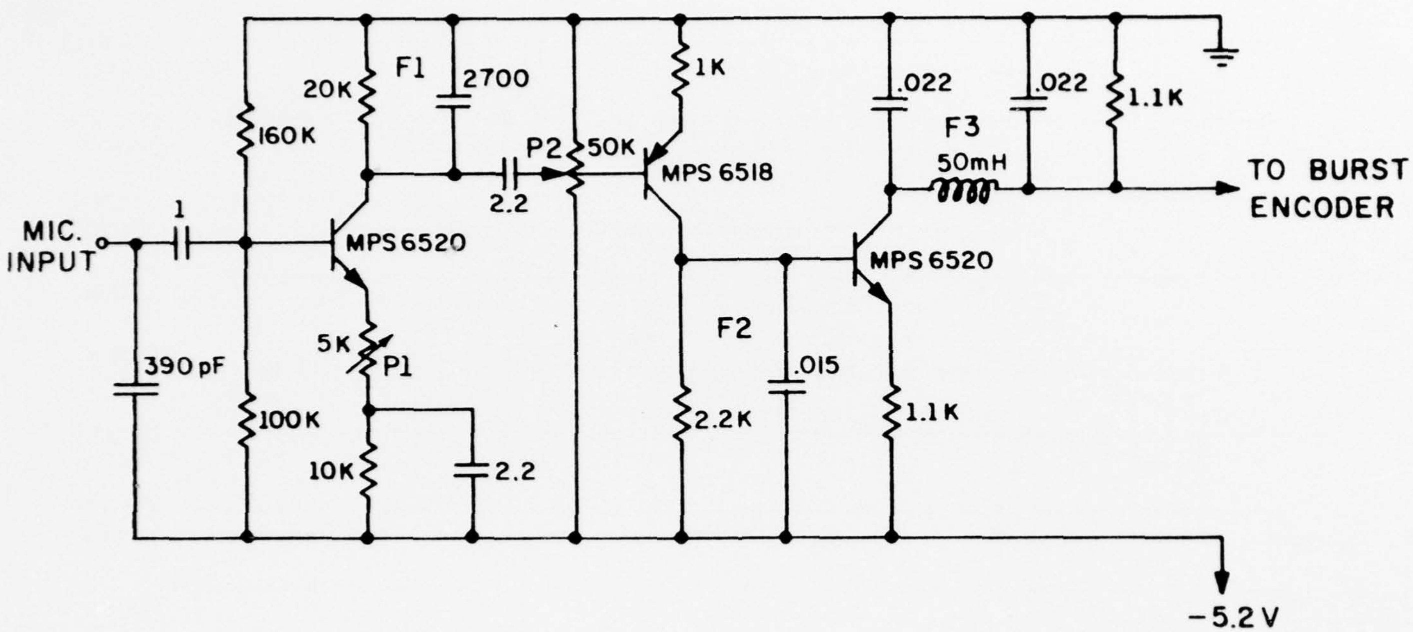


Figure AD-4. Demultiplexer Timing

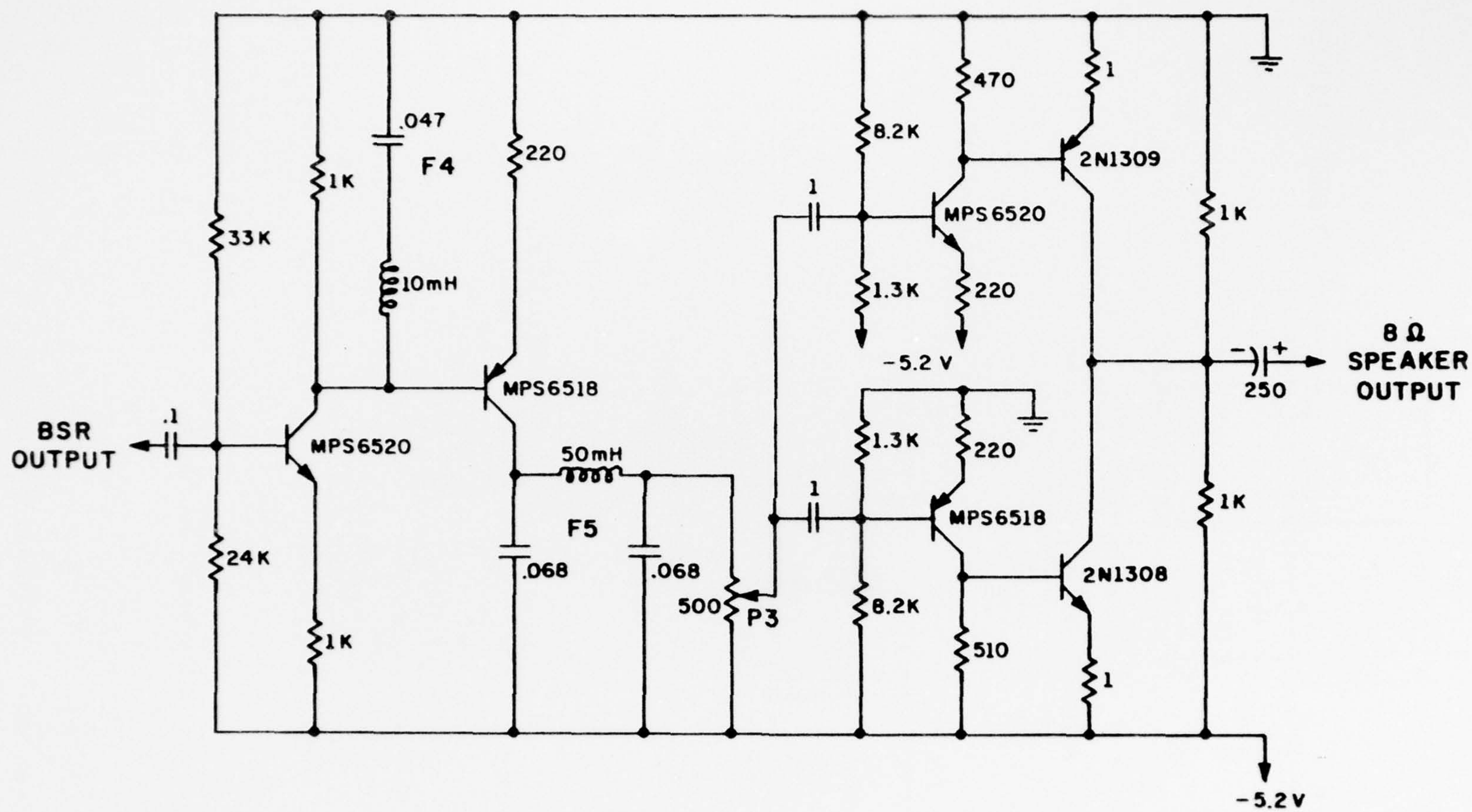


F1-5.9 KHz RC LPF   P1-Gain

F2-4.8 KHz RC LPF   P2-Level

F3-5.5 KHz 3d Order LPF

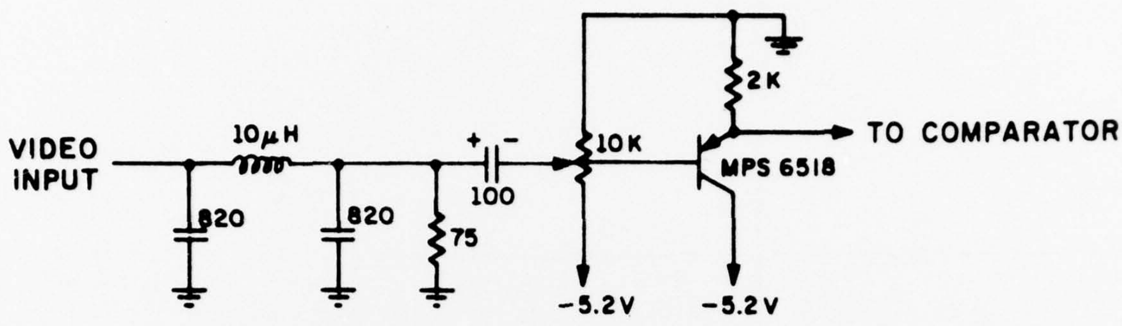
Figure AD-5. Encoder Audio Filter/Preamp



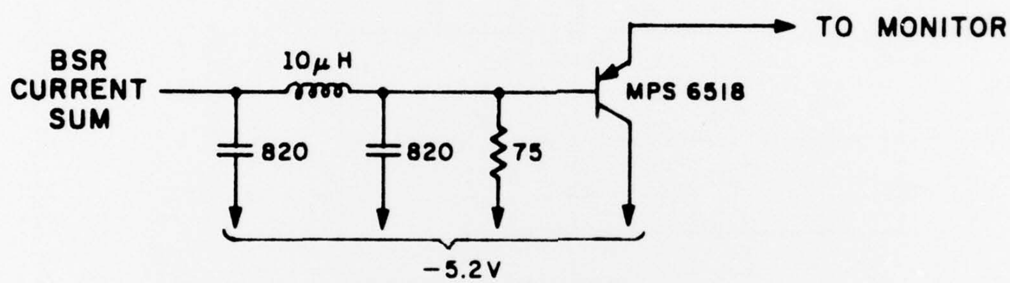
F4-7.9 KHz Trap P3-Volume

F5-3.2 KHz 3'd Order LPF

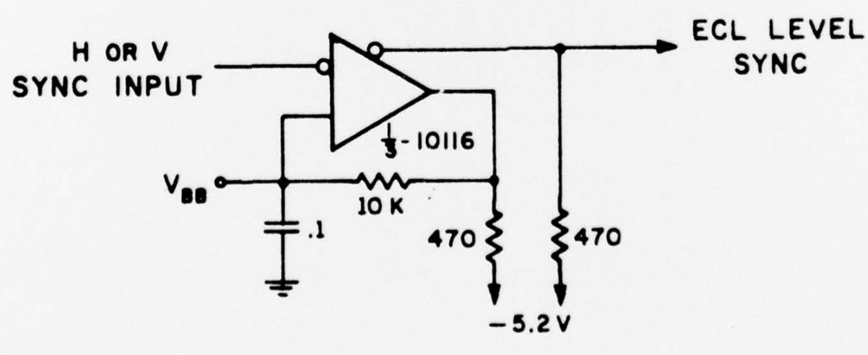
Fgiure AD-6. Decoder Audio Filter/Amp



Multiplexer Video Filter/Buffer



Demultiplexer Video Filter/Buffer



Multiplexer Sync Shaper

Figure AD-7. Video and Sync Circuitry

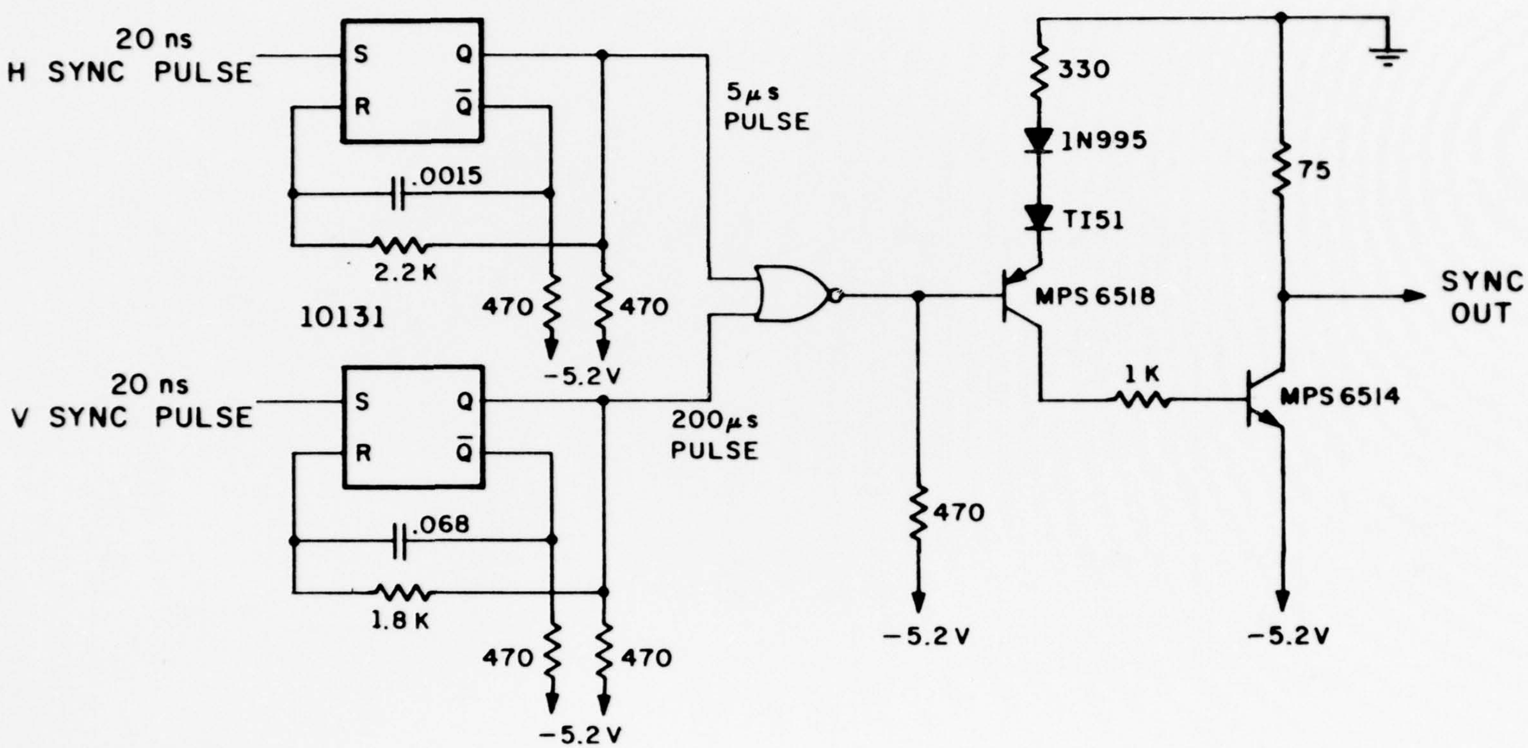


Figure AD-7 (cont.). Demultiplexer Sync Circuitry

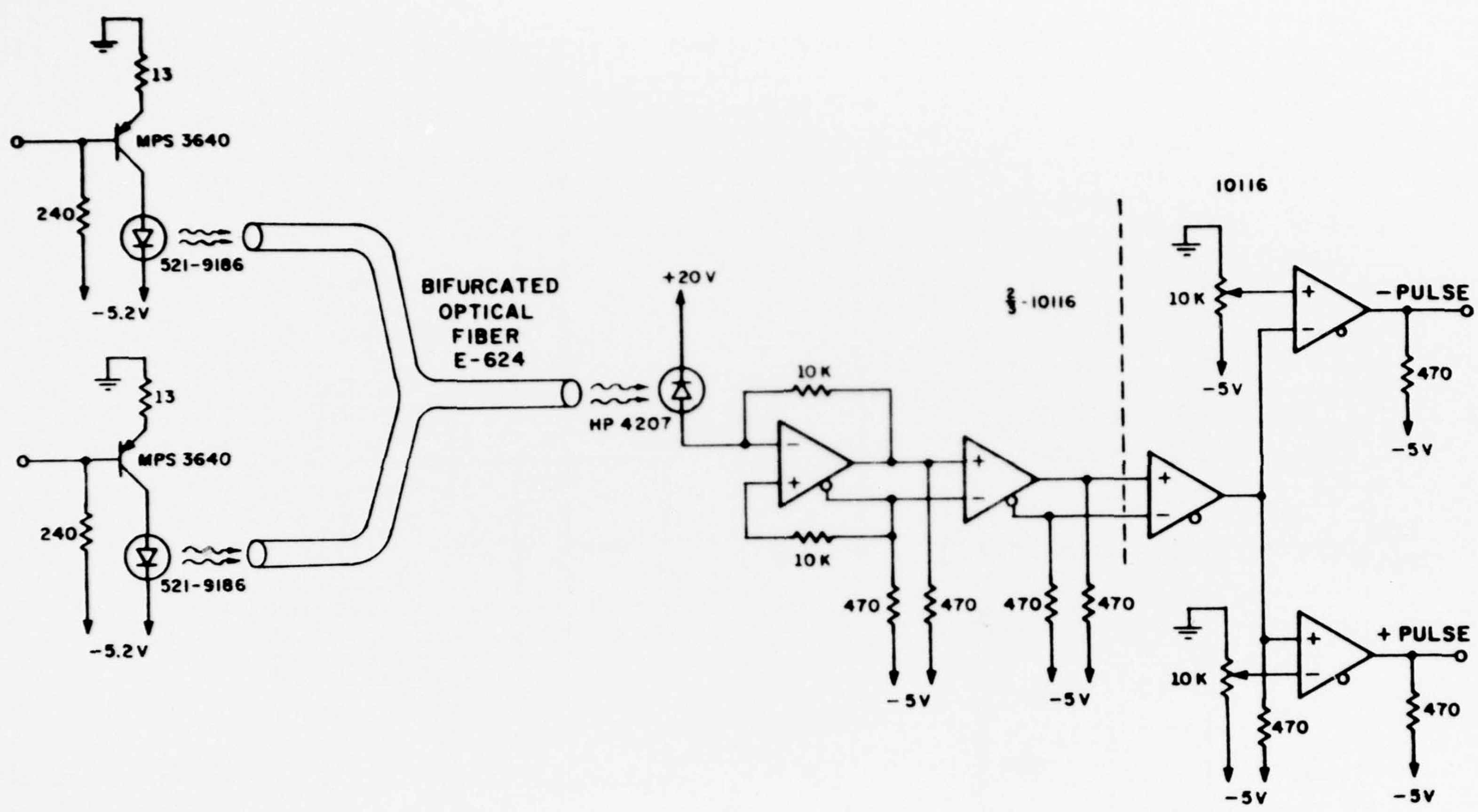


Figure AD-8. Optical Link

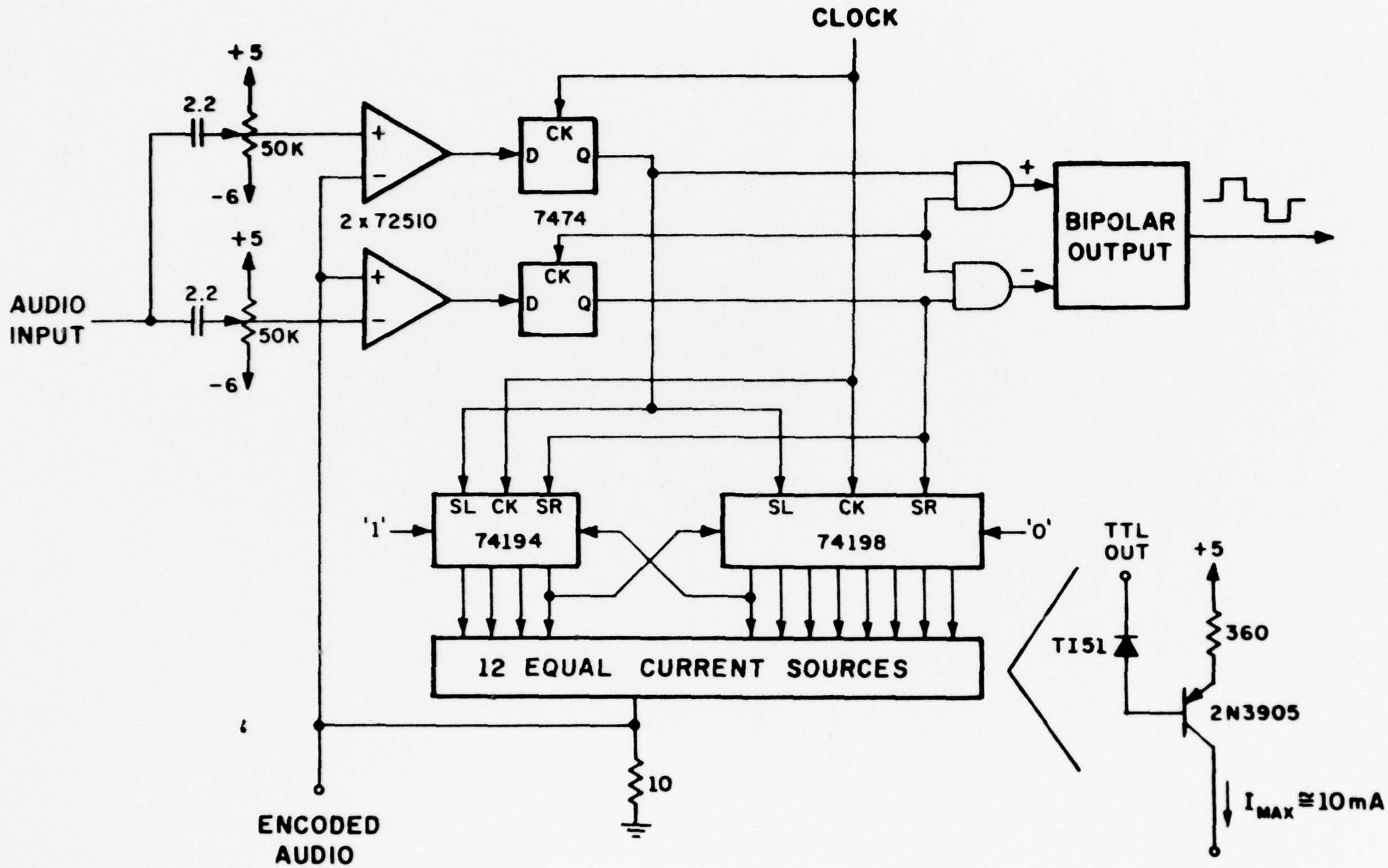


Figure AD-9. Biburst Encoder

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