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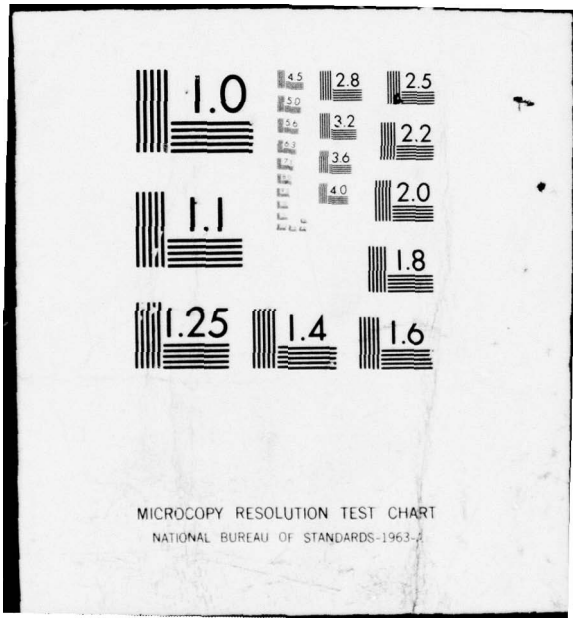
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ENHANCEMENT MODE TRANSFERRED-ELECTRON LOGIC DEVICES (TELDs)

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RCA Laboratories
Princeton, New Jersey [illegible]

December [illegible]

FINAL REPORT

For the period 1 December [illegible] to 30 November [illegible]

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This report describes the results of the quasi-enhancement mode transferred-electron logic program which was intended to develop GaAs devices suitable for this mode of operation and evaluate them in pulse amplifier circuits.

Epitaxial GaAs wafers were grown by vapor hydride synthesis. Electrolytic etching of the wafers was used to obtain uniform nd product across the wafers. Quasi-enhancement mode devices were fabricated and

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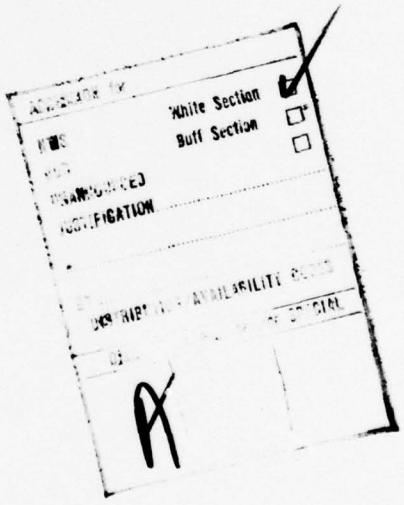
dc, rf, and switching parameters were characterized. Current drop of the order of 10-15% was measured. Trigger sensitivity of these devices was 1.5-2.5 V. The quality of the epi-layer substrate has to be further improved so that lower nd product can be used; this will improve the trigger sensitivity and reduce device dissipation. A TELD-FET circuit evaluated as a pulse amplifier was found to provide voltage gain with good trigger sensitivity and high-frequency response. This configuration combines the advantages of FETs (good trigger sensitivity) and TELDs (threshold and neuristor) and is potentially very useful for ultrahigh-speed logic. Voltage gains of up to 4 were realized for about 100-ps pulse width (half-height) operation.

PREFACE

This Final Report describes research done at the Microwave Technology Center of RCA Laboratories, at Princeton, New Jersey, under Contract No. N00014-76-C-0464 during the period 1 December 1975 to 30 November 1976. F. Sterzer is the Center's Director; S. Y. Narayan was the Project Supervisor, and L. C. Upadhyayula the Project Scientist. Others who participated in the research are R. E. Smith and J. F. Wilhelm.



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SECTION I

INTRODUCTION

The objectives of this research program are (i) to develop quasi-enhancement mode transferred-electron logic devices (TELDs) and (ii) to evaluate these devices as pulse amplifiers.

The device technology developed under a concurrent ONR program (N00014-75-C-0100) was used to fabricate the devices. Electrolytic etching under photostimulation was used for optimizing nd product across the wafer. Buffer layers were used to improve the epitaxial material quality. Many wafers were processed, and the devices showed 10-15% current drop with 1.5- to 2.5-V trigger sensitivity. Pulse amplifiers were evaluated with chip load resistors. To improve the amplifier performance a TELD-FET combination was evaluated. This circuit showed good trigger sensitivity with voltage gain and capability to process narrow pulses of 150-ps width.

Preliminary computer simulation results on quasi-enhancement mode TELDs are in agreement with the phenomenological theory developed. More extensive simulations will be necessary to obtain optimum device parameters compatible with the input and output pulse requirements such as amplitude, rise time, and device delay.

The effort in all these areas will be discussed in detail in the following pages.

SECTION II

DESIGN OF QUASI-ENHANCEMENT MODE TELDs

A. INTRODUCTION

The transferred-electron effect in GaAs has been used to develop high-speed threshold logic devices. The depletion mode operation of these devices has been studied extensively by several researchers [1,2,3,4]. One of the major problems in the operation of depletion mode devices is the dc dissipation, which is of the order of several hundred milliwatts per device to realize small-device delay of 20-50 ps. The quasi-enhancement mode operation of these devices proposed by Upadhyayula [5] makes it possible to reduce the device dissipation substantially and yet maintain small delay-dissipation product. In the following pages we will discuss the theory of quasi-enhancement mode TELDs and deduce the material parameters and device geometry.

B. THEORY OF QUASI-ENHANCEMENT MODE TELD

A schematic of a three-terminal planar logic device is shown in Fig. 1. The biasing arrangements for depletion and quasi-enhancement mode operation are shown in Figs. 1(a) and 1(b), respectively. In the quasi-enhancement

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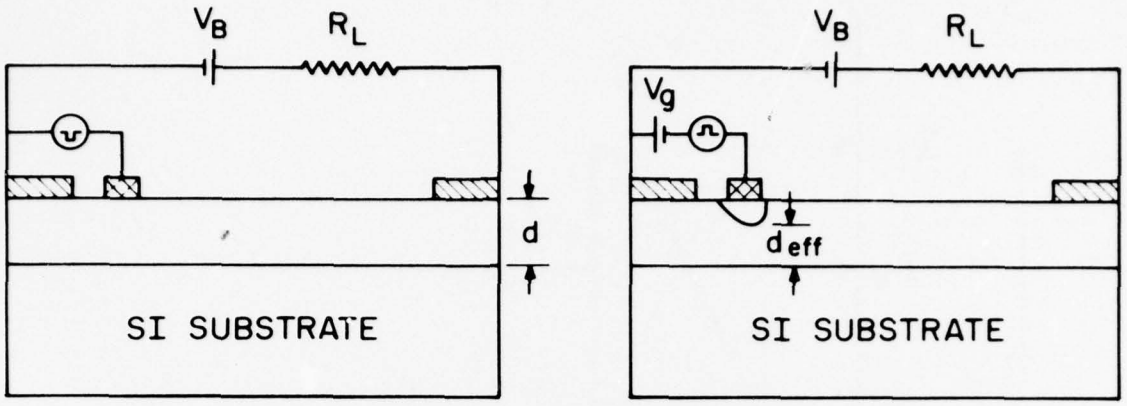
1. T. Sugeta et al., "Characteristics and Applications of a Schottky-Barrier-Gate Gunn-Effect Digital Device," IEEE Trans. Electron Devices ED-21, 504 (1974).
2. K. Mause et al., "Circuit Integration with Gate Controlled Gunn Devices," *Proc. 4th Intern. Symp. on GaAs and Related Compounds*, Boulder, Colo., September 1972, pp. 275-285.
3. S. Yanagisawa, O. Wada, and H. Takanashi, "Gigabit Rate Gunn-Effect Shift Register," Technical Digest, Intern. Electron Device Meeting, Washington, DC, 1975, p. 317.
4. L. C. Upadhyayula et al., "Transferred Electron Logic Devices (TELDs) for Gigabit Rate Signal Processing," IEEE Trans. Microwave Theory and Techniques MTT-24(12), 920 (Dec. 1976).
5. L. C. Upadhyayula, "Quasi-Enhancement Mode Operation of Transferred Electron Logic Devices (TELDs)", Electronics Letters 12(10), 262 (13 May 1976).



(a) (b)

Figure 1. Schematic of (a) a depletion mode TELD; (b) a quasi-enhancement mode TELD.

mode the device is biased well above the threshold field. The channel under the gate region is depleted by a suitable bias, so that the nd_{eff} is below that required for domain formation [Fig. 1(b)]. In this situation the traveling high field domains do not form, but the electric field in the conducting channel is well above the domain-sustaining field. Therefore, if a positive signal is applied to the gate, the depletion region decreases and the nd product exceeds the nd_{crit} required for the domain formation. High field domains are nucleated under the gate; these travel to the anode and get absorbed. The I-V characteristic of a typical device is shown in Fig. 2, and the device operation is explained with reference to this.

The operating point in the quiescent state is denoted by $V_q I_q$, where V_q is greater than the threshold voltage (V_{th}). A positive (instead of negative) signal when applied to the control gate decreases the depletion region; domains can therefore be nucleated when the input signal reaches an appropriate level. The device current increases from I_q to I_v in the presence of an input (positive) signal. The designation "quasi-enhancement mode" is derived from this phenomenon: that there is a current increase in the presence of an input signal and that the quiescent current (I_q) is not quite zero. The dc dissipation in this mode of operation is $V_q I_q$ which is far less than that for depletion mode operation. Furthermore, the operating point in the quiescent state lies on the

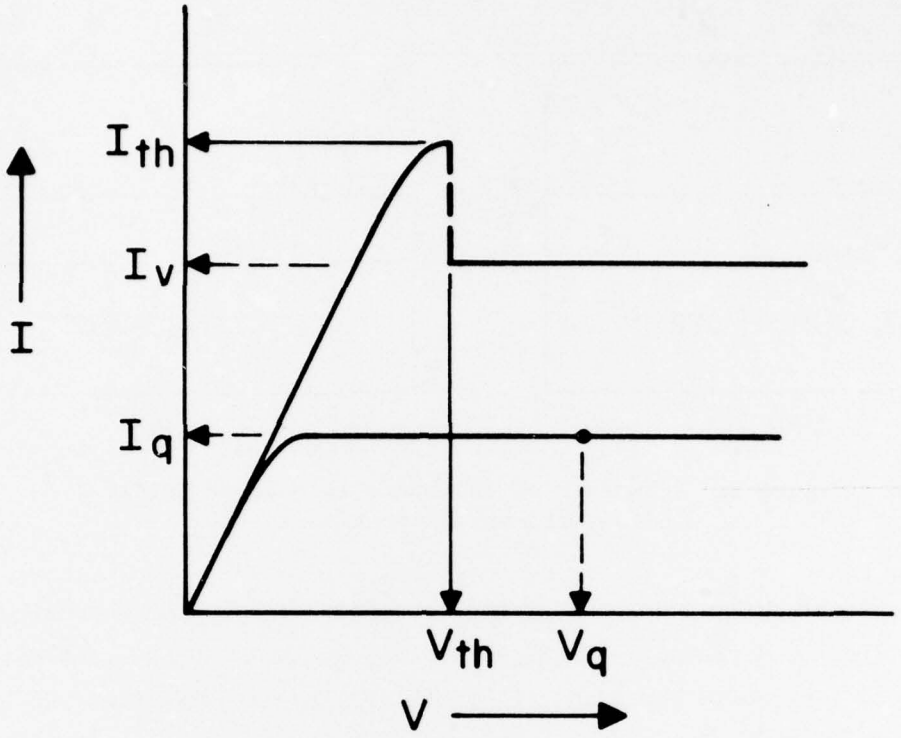


Figure 2. I-V characteristic of a TELD.

saturated portion of the I-V characteristic. Hence, small changes in the bias supply voltage do not change the operating point. In contrast to this, the depletion mode device is biased at 0.9-0.95 V_{th} and any fluctuations in the bias supply or noise voltages can cause spurious device triggering.

C. DEVICE DESIGN

1. Doping Density and Channel Thickness Considerations

The doping density, channel thickness, and device geometry should be optimized to obtain good device performance.

Mause et al. [6] have shown that for domain formation in planar Gunn devices the criteria are

$$nd_{crit} > 1.0 \times 10^{12} \text{ cm}^{-2}$$

and

$$n\ell_{crit} > 1.0 \times 10^{13} \text{ cm}^{-2}$$

They also showed that the current drop-back, when the device thresholds, increases with an increase of nd and $n\ell$ above their critical values. An nd value of 2-4 x 10^{12} cm^{-2} is generally used to achieve 15-20% current drop-back. The device characteristics therefore strongly depend upon the material parameters such as doping density and channel thickness. In the quasi-enhancement mode operation, a negative voltage is applied to the gate to maintain the effective nd product below the critical value. The voltage required to maintain $nd_{eff} < nd_{crit}$ depends on the actual doping density (n) and channel thickness (d) or the pinch-off voltage ($\phi_p \simeq ned^2/2\varepsilon$). For the same nd-product material, the lower the n the higher the pinch-off voltage and also the higher the trigger voltage required. A recent trigger sensitivity study [7] showed that for higher channel pinch-off voltage, the gate sensitivity was poorer. Also, when these devices are used in logic circuits, they must produce an output voltage that is at least equal to the trigger voltage required to provide fan-out. The selection of material parameters (n,d) therefore plays an important role in the case of quasi-enhancement mode TELDs. Two examples are given below to show how one can achieve a trigger sensitivity of 0.5-1.0 V. It should be noted that the thermal energy at room temperature corresponds to 0.025 V and that, for good stability, the trigger sensitivity should be at least ten times this value. For an ECL (emitter-coupled logic) device the

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6. K. Mause, A. Schlachetzki, E. Hesse, and H. Salow, "Monolithic Integration of Gallium Arsenide-Gunn Devices for Digital Circuits," *Proc. Fourth Biennial Cornell Electrical Engineering Conf. on Microwave Devices, Circuits and Applications*, Vol. 4, 1973, p. 211.
7. L. C. Upadhyayula, "Trigger Sensitivity of Transferred Electron Logic Devices," IEEE Trans. Electron Devices ED-23, 1049-1052 (Sept. 1976).

difference between the high and low logic levels is about 0.8 V. Due to these considerations, we selected the trigger sensitivity goal to be between 0.5 and 1.0 V.

Let us consider a device with 4×10^{16} cm^{-3} doping density and 0.45 μm channel thickness. The nd product for this device is 1.8×10^{12} cm^{-2} and, according to Mause et al. [6], a 20% current drop is possible in such a device. The pinch-off voltage is 5.9 V. When d_{eff} is 0.25 μm, nd_{eff} becomes 10^{12} cm^{-2}, and domains can be suppressed. To achieve this d_{eff}, a 0.2-μm region under the gate channel has to be depleted. The voltage required to do this is given by

$$V_1 = \frac{e\, n\, d_1^2}{2\varepsilon} = 1.16 \text{ V}$$

where d_1 is the depletion thickness (= 0.2 μm). If the depletion region is decreased to 0.1 μm by an external signal (ΔV_g) at the gate, then the $nd_{eff} \simeq$ 1.4×10^{12} cm^{-2} and domains can be nucleated. The reverse bias on the gate to achieve this is given by

$$V_2 = \frac{e\, n\, d_2^2}{2\varepsilon} = 0.29 \text{ V}$$

(where d_2 = 0.1 μm). The trigger signal ΔV_g, applied at the gate, is given by

$$\Delta V_g = V_1 - V_2 = 0.87 \text{ V}$$

Similarly, for a device with 6×10^{16} cm^{-3} doping, 0.4-μm channel thickness, and nd = 2.4×10^{12} cm^{-2} we can show that

$$V_1 = 0.98 \text{ V}; \quad nd_{1eff} = 0.9 \times 10^{12} \text{ cm}^{-2}$$

$$V_2 = 0.39 \text{ V}; \quad nd_{2eff} = 1.5 \times 10^{12} \text{ cm}^{-2}$$

and $$\Delta V_g = 0.59 \text{ V}$$

A TELD with 4-6 x 10^{16} cm^{-3} doping, 0.3- to 0.45-μm channel thickness, and nd in the 1.8-2.4 x 10^{12} cm^{-2} range can therefore be operated in the quasi-enhancement mode with a trigger sensitivity of 0.59-0.87 V - a very promising result, indeed. As $n\ell \gtrsim 10$ nd is chosen for TELDs, the cathode-anode spacing for such a device should be between 5 and 10 μm. In order to achieve the trigger sensitivity desired, both n and d have been tailored within the limits specified above.

Even though attempts are being made to improve the uniformity of the doping density and channel thickness, a 20-25% variation in each of these parameters is present in the epitaxial wafers grown. Recently, we have been using an electrolytic etching technique described by Rode et al. [8]. This etching technique is self-limiting and tailors a layer initially nonuniform (in thickness and doping density) to one with a constant nd product across the entire wafer. It removes the uncertainty for the doping density and the channel thickness and provides an nd value between 2.4 x 10^{12} and 4 x 10^{12} cm^{-2}. This technique has improved the device yield and current drop-back considerably. Therefore, this process is routinely used by us in fabricating TELDs. This, however, is not an optimum situation if we want to operate these TELDs in the quasi-enhancement mode. Electrolytic etching under photostimulation has to be used; this further reduces the active channel thickness by about 0.2 μm and results in an nd value of 1.6-2.8 x 10^{12} cm^{-2}.

2. Device Geometry

Under quiescent biasing conditions the TELD remains in a nonoscillatory state. For small input signals, the device transfer characteristics are similar to those of a field effect transistor (FET). For large input signals, the device thresholds and domain formation occurs. Recent studies [7] on TELDs showed that the device gain (G_v) is given by

$$G_v = g_m R_L + \Delta I R_L / \Delta V_g$$

---

8. D. L. Rode, B. Schwartz, and J. V. Dilorenzo, "Electrolytic Etching and Electron Mobility of GaAs for FETs," Solid State Electronics 17, 1119 (Nov. 1974).

where g_m = low field transconductance

R_L = load resistance

ΔI = current drop-back

and ΔV_g = input trigger voltage

The upper limit on R_L is set by the external-circuit charging time constants as discussed by Mause et al. [6]. Therefore, a g_m of the order of 5-10 $m\Omega^{-1}$ is required to obtain device gain in addition to good current drop (ΔI). The low field transconductance, g_m, is directly proportional to the ratio of gate width to gate length (W/ℓ_g). This ratio is about 100 for FETs. We would like to use a value of 50-100 for this ratio. Since the device dissipation increases in direction proportion to W, an optimum value for W/ℓ_g has to be determined.

Conventional photolithographic techniques limit the smallest value for ℓ_g to about 2.0 μm. A device width between 100 and 200 μm will be used. Since the doping density is in the 4-6 x 10^{16} range, cathode-anode spacing of 10-12 μm will be chosen.

In the depletion mode of operation such a device alone will dissipate 130-260 mW power; in the quasi-enhancement mode the dc dissipation is about 98-196 mW. *As discussed in Section V, when an external load resistor is included the total dissipation in the quasi-enhancement mode is 50% of that for the normal mode operation.* The output voltage will be about 1.0 V; a voltage gain of 1.2-1.5 is therefore expected.

SECTION III

MATERIAL GROWTH AND EVALUATION

1. Material Growth

a. *Improved Electrical Properties.* - The objective of the materials portion of this program is to improve the electrical properties and uniformity of thin GaAs epitaxial layers grown on semi-insulating (SI) substrates.

Epitaxial GaAs is grown by RCA vapor-hydride synthesis. The details of this growth process are well documented in the literature [9].

b. *Uniformity of Doping Density and Thickness.* - In addition to other variables, the uniformity of the temperature in the reaction and deposition zones will affect the uniformity of the doping density and thickness of the epi-layers. One of our reactors was modified to use heat-pipe furnaces for the Ga, reaction, and deposition zones. The heat pipes provide flat temperature profiles with an abrupt transition between zones.

c. *Buffer Layers.* - High-resistivity or undoped epitaxial layers were used as buffer layers. H_2O-doped and Cr-doped high-resistivity layers were grown in reactor #1. Air Force Avionics Laboratory (AFAL) evaluated these H_2O-doped layers and found that the layers are p type with a resistivity of 7-8 x 10^4 Ω-cm. Photoluminescence studies indicated that the epi-layer quality is good. Cr-doped epi-layers were also evaluated by AFAL/DHR; it was found that the resistivity of these layers is of the order of 10^8 Ω-cm.

A boron nitride liner was used in the reaction zone part of the reactor to minimize the chance of any Si getting into the grown layers. The background carrier concentration in the wafers grown in this reactor corresponds to breakdown voltage in excess of 1000 V. The layers were p type with a hole concentration of 4 x 10^{12} cm^{-3} and mobility of 180 $cm^2/V\text{-}s$. When layers were backdoped to an excess carrier concentration of 2-3 x 10^{15} cm^{-3}, the liquid-nitrogen mobility was about 40,000-50,000 $cm^2/V\text{-}s$.

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9. J. J. Tietjen et al., "Vapor-Phase Growth of Several III-V Compound Semiconductors," Solid State Technology 10, 42 (1972).

d. *Specific Material Requirements.* - In Section II.C it was shown that the epitaxial GaAs wafers with a doping density of 4-6 x 10^{16} cm^{-3} and a thickness of 0.3-0.45 μm are required to meet the goals of the program. Since the wafers are subjected to electrolytic etching before device fabrication, it was necessary to grow the epi-layers much thicker. Several wafers were grown with doping density in the 1-6 x 10^{16} cm^{-3} range and thickness in the 1- to 3-μm range.

2. Material Evaluation

a. *Introduction.* - A knowledge of the material parameters such as the doping density (n), thickness (d), electron mobility (μ), and presence or absence of trapping centers is very important to anyone wishing to understand and improve device performance. Electron mobilities were obtained from van der Pauw measurements [10] on the actual device wafers. Van der Pauw measurements were made at both room and liquid-nitrogen temperatures on as-grown or electrolytically etched wafers. Capacitance-voltage (C-V) measurements were used to provide doping profiles, to calculate nd-product values, and to detect the presence of trapping centers.

b. *Van der Pauw Measurements.* - Mause et al. [6] have shown that electron mobility decreases as n-layer thickness is decreased, unless a buffer layer is introduced to eliminate the epi-substrate interface effects. For this reason, van der Pauw measurements [10] were made on the actual device wafers. The entire wafer or a 0.5 cm x 0.5 cm cleaved specimen with fused indium contacts on each corner was used for the measurements. The measurements were made at room temperature and liquid-nitrogen temperature. These measurements were repeated on some of the wafers both after electrolytic etching and after electrolytic etching with photostimulation. Table 1 shows van der Pauw data on some of our recent wafers. The liquid-nitrogen mobilities are consistently low and correspond to a compensation ratio $(N_D + N_A)/(N_D - N_A)$ of 2-5, even though the epi-layer thickness is 1.5 μm or more. Wafers B-339 and B-340 were etched electrolytically under photostimulation; the final thicknesses of

10. L. J. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effects on Discs of Arbitrary Shape," Phillips Res. Repts. 13, 1 (1958).

TABLE 1. VAN DER PAUW DATA FOR DEVICE WAFERS

Wafer	Growth Parameters		As-Grown Wafer				After Electrolytic Etching				After Electrolytic Etching with Photostimulation			
			300K		77K		300K		77K		300K		77K	
	N	d	n	μ	n	μ	n	μ	n	μ	n	μ	n	μ
#	($x10^{16} cm^{-3}$)	(μm)	($x10^{16}$ cm^{-3})	(cm^2/V-s)	($x10^{16}$ cm^{-3})	(cm^2/V-s)	($x10^{16}$ cm^{-3})	(cm^2/V-s)	($x10^{16}$ cm^{-3})	(cm^2/V-s)	($x10^{16}$ cm^{-3})	(cm^2/V-s)	($x10^{16}$ cm^{-3})	(cm^2/V-s)
B-240	1.2	5	2.4	5,460	2.0	12,760								
2438	1.5	3	5.0	3,530	4.1	8,220								
2568-A	1.5	2.5	1.2	7,230	1.1	16,390	1.6	7,230	1.52	16,390				
2568-B	1.5	2.5	1.0	6,510	0.96	17,100	0.76	6,200	0.71	18,000	0.51	5,880	0.51	16,760
B-268 (3-μ buffer)	2.0	3.0	2.8	5,480	2.25	13,100	2.4	4,500	1.8	13,000				
B-269	1 to 2	3.0	3.4	5,300	2.66	7,910								
B-270			2.27	5,610	1.8	13,000	2.2	5,100	2.0	11,800				
B-339*		1.0	6.4	3,900	5.2	5,700	-	-	-	-	-	-	-	-
B-340*		1.0	4.4	4,000	3.9	5,500	-	-	-	-	-	-	-	-
B-405	2.0	3.0	1.7	5,600	1.3	15,000	1.9	4,800	1.6	11,000				
B-412	2.0	3.0	2.2	5,700	1.8	14,000	2.2	5,600	1.8	15,000				

*B-339 and B-340 were etched electrolytically under photostimulation; estimated final thicknesses are 0.6 and 0.45 μm, respectively. No van der Pauw measurements were possible.

NOTE: Wafers #B-268 to B-412 were grown after heat pipes had been installed.

the epi-layers were 0.6 and 0.45 μm, respectively. The very high resistance of the layers made Hall measurements impossible. This result, along with other device data (such as light sensitivity and small current drops), indicates that the electrical quality of the epi-layer close to the epi-substrate interface is poor.

c. *Doping Profiles*. - Doping profiles were measured on the actual device wafers by means of an analog system. Schottky barriers of 0.25- or 0.125-cm-diameter aluminum or chrome-gold were used in these measurements. Figure 3 shows typical doping profiles on wafers used in the fabrication of quasi-enhancement mode TELDs. The doping density is fairly uniform. In most of the cases the doping density obtained from these profiles is higher than that obtained from van der Pauw data. The doping density is 4-6 x 10^{16} cm^{-3}.

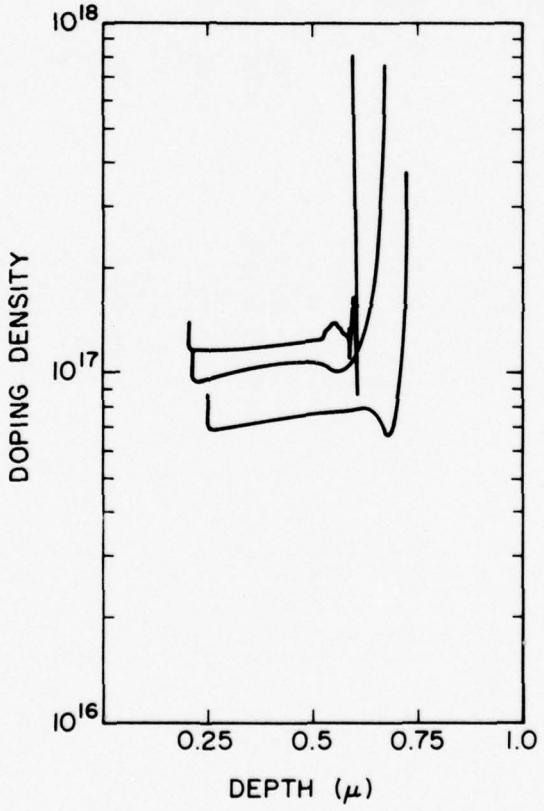

Figure 3. Typical doping profiles of TELD wafers.

d. *nd Product*. - The Schottky-barrier capacitance was measured on a Boonton capacitance bridge as a function of the junction reverse-bias voltage. Fig. 4 shows the typical plot of the C-V data. The nd product was calculated from the C-V plot by use of the relation

$$nd = \frac{\int CdV}{Ae} = \frac{\text{area under the C-V curve}}{Ae}$$

where A is the area of the Schottky diode and e is the electronic charge. The nd product was in the range of 2.5-3.5 x 10^{12} cm^{-2} for most of the wafers used in this program.

e. *Trap Measurements*. - Heeks [11] has clearly pointed out the deleterious effects of the presence of trapping centers on the performance of transferred-electron logic devices. Teszner and Boccon-Gibot [12] discussed the influence of electron trapping on domain dynamics in epitaxial Gunn devices. Essentially, the presence of traps decreases the percentage current drop one can obtain in a TELD and increases the threshold voltage. A knowledge of trap density and energy level may therefore help identify the impurity species and eliminate them from the growth system. Transient capacitance measurements [13,14] to determine these parameters were made on Schottky barriers formed on wafer #2568-B. These data indicated (i) a trap density of the order of 10^{16} cm^{-3}, (ii) a trap energy of about 0.8 eV, and (iii) trapping centers located at the epi-substrate interface. The rest of the n layer was free from traps. This observation agrees with the low mobilities and small current drops generally obtained. To understand this problem fully, further investigations have to be carried out.

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11. J. S. Heeks, "Some Properties of the Moving High Field Domains in Gunn-Effect Devices," IEEE Trans. Electron Devices ED-13, 68 (1966).
12. J. L. Teszner and B. Boccon-Gibot, "Influence of Electron Trapping on Domain Dynamics in Epitaxial Gunn Diodes," J. Appl. Phys. 44, 2765 (1973).
13. D. V. Lang, "Deep Level Transient Spectroscopy: A New Method to Characterize Traps in Semiconductors," J. Appl. Phys. 45(7), 3023-3032 (1974).
14. M. D. Miller and D. R. Patterson, "Transient Capacitance Deep-Level-Spectrometry Instrumentation," Tech. Rept. PRRL-76-TR-129, RCA Laboratories, Princeton, N.J.

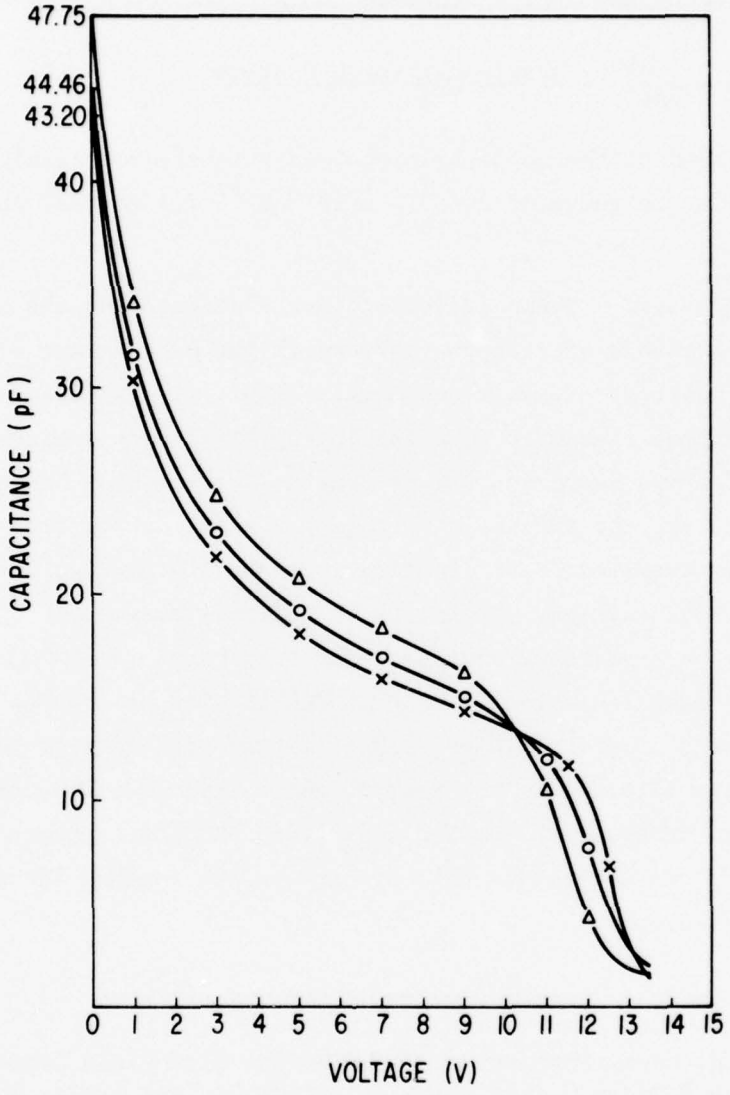


Figure 4. Schottky-barrier capacitance of typical test diode as a function of reverse-bias voltage.

SECTION IV

DEVICE TECHNOLOGY

A. INTRODUCTION

Electrolytic etching was used to obtain uniform nd product across the wafer so that the threshold current and current drop on all the devices fabricated on any particular wafer would not differ by more than 5-10%. Standard photolithographic techniques were then used to fabricate TELDs with a 12- or 35-μm channel.

B. ELECTROLYTIC ETCHING

Electrolytic etching is a self-limiting process; the etching stops when the active-layer thickness corresponds to the maximum depletion-layer thickness for the particular doping density. Rode et al. [8] studied the electrolytic etching and electron mobility of GaAs and concluded that essentially the bulk mobility can be maintained in layers as thin as 0.2 μm. During this electrolytic etching process, if the wafer is illuminated by a light source, excess carriers can be generated in the wafer. The sample behaves as if it were more heavily doped or had a thicker channel than it actually has, so that more material can be removed by anodic oxidation and etching.

We used a mixture of hydrogen peroxide and phosphoric acid with a pH of 1.95-2.0 as the electrolyte. Anodic oxidation was carried out at a bias voltage of 50-100 V. The oxide was etched in 50% NH_4OH. Oxidation and etching steps were repeated until no further oxide formed in any part of the sample. At this point, the sample was illuminated with a microscope light and the electrolytic etching was carried out to the limit.

Van der Pauw and C-V data on the electrolytically etched wafers are presented in Section III. The variation in nd product across the wafers was within 10%, but the electrical quality was marginal.

C. DEVICE FABRICATION

The fabrication schedule for quasi-enhancement mode TELDs is shown in Fig. 5 and summarized below.

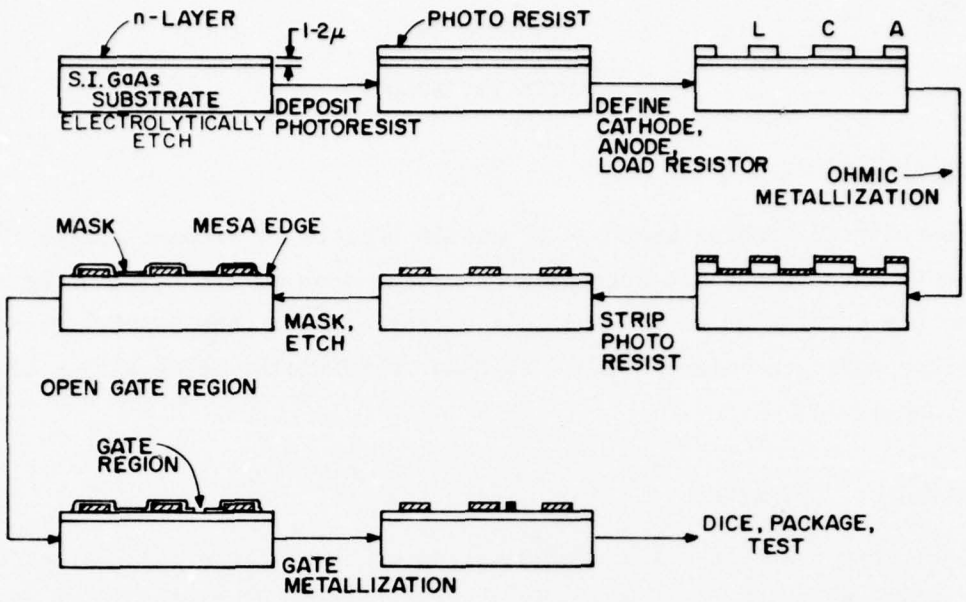


Figure 5. Process steps in the fabrication of quasi-enhancement mode TELD mesa devices.

(a) The wafer is electrolytically etched until a uniform nd product is obtained across the wafer.

(b) A wafer of n-GaAs grown on a (100)-oriented semi-insulating GaAs substrate is cleaned in organic solvents. The $\{0\bar{1}1\}$ and {011} crystallographic planes are determined.

(c) The wafer is thoroughly cleaned in organic solvents. The device structure is oriented along the {011} direction, and the areas where the cathode, anode, and load resistor contacts have to be defined are opened to expose the GaAs surface by a conventional photolithographic process.

(d) The ohmic contact metallization, AuGe/Ni/Au, is evaporated over the wafer. The resist is stripped off; this removes the metallization everywhere except from the cathode, anode, and load resistor contacts. The ohmic contacts are sintered at 380-400°C in a hydrogen atmosphere.

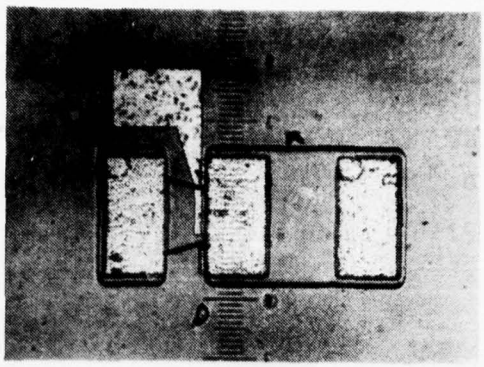
(e) The anode, cathode, and active regions are masked, and devices are isolated by etching down to the semi-insulating GaAs substrate. An anisotropic etch such as ($8H_2O_2:1H_2SO_4:1H_2O$) is used for etching. *This is an important step in the device fabrication since it results in a gradually tapered device edge contour and facilitates continuous gate metallization across the mesa edge.*

(f) The gate areas are opened by the use of photoresist.

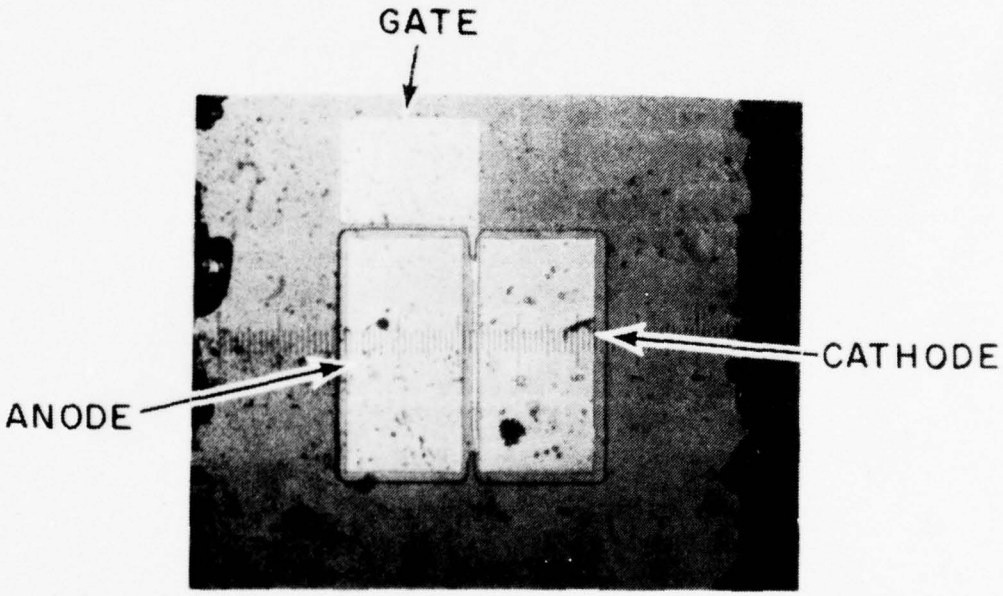
(g) The gate metallization is evaporated on. We have used Cr-Au for most of our wafers. The photoresist is stripped off, leaving the gate metallization on.

(h) The wafer is then diced, and devices are mounted on carriers.

During the early part of the program we fabricated devices with ℓ_{ca} = 35 μm, ℓ_g = 5 μm, W = 50 μm, and ℓ_{cg} = 1-2 μm. After having carried out the trigger sensitivity study discussed in Section II, we have been fabricating devices with ℓ_{ca} = 12 μm, ℓ_g = 2 μm, and W = 120-150 μm. The 35-μm devices have integral cathode load resistors; the 12-μm devices do not. The fabricated devices are shown in Fig. 6. Low- and high-frequency characteristics are discussed in Section V.



(a)



(b)

Figure 6. Photomicrographs of fabricated multilevel mesa devices: (a) 35-μm device and (b) 12-μm device.

SECTION V

DEVICE EVALUATION

A. INTRODUCTION

The low-frequency transfer characteristics and the high-frequency switching characteristics of the fabricated TELDs have been studied. The percentage current drop ($\Delta I/I_{th}$), the trigger sensitivity (ΔV_g), the propagation delay (τ_d), and the voltage gain (G_v) were measured. A TELD-FET combination circuit was also evaluated. The preliminary results indicate this circuit to be more promising than the TELD-resistor combination.

B. LOW-FREQUENCY TRANSFER CHARACTERISTICS

The transfer characteristics of the devices were measured on a curve tracer. The gate off-set voltage was used to bias the device in the quasi-enhancement mode; positive step voltage was used for gate triggering. Figure 7 shows typical transfer characteristics of a TELD. The threshold current and current increase for this device are 14 and 4.0 mA, respectively. The minimum trigger voltage required is 2.0 V. Because of the epi-substrate interface problems, the wafer was not etched electrolytically under photostimulation. The higher nd product and small current drop-back are responsible for the poor trigger sensitivity. The current drop for this device is 11%.

C. PULSE AMPLIFIER

Two types of pulse amplifiers were designed with the quasi-enhancement mode TELDs, and their performance was studied. In one class of pulse amplifiers, chip resistors were used to develop the output voltage; in the other class of pulse amplifiers a field effect transistor was used as a trigger element. The performance of these circuits is described below.

1. TELD with Chip Load Resistor

Figure 8 shows a TELD pulse amplifier circuit with a chip load resistor. The value of the chip resistor is approximately equal to that of the low field

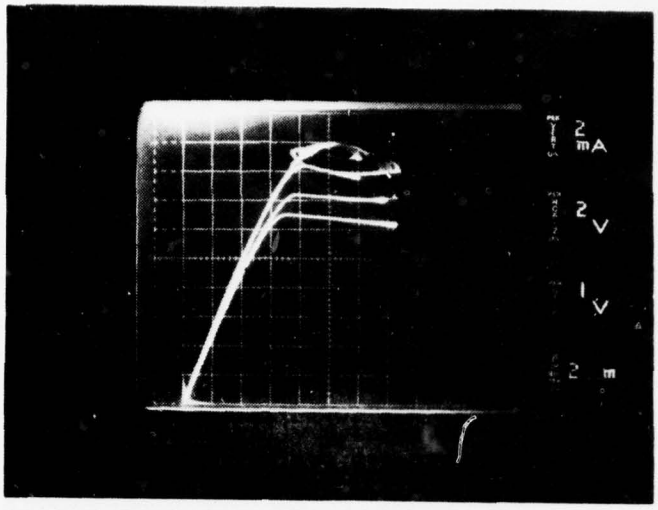


Figure 7. Transfer characteristics of quasi-enhancement mode TELD (gate off-set voltage = 1.3 V).

device resistance (i.e., 300-500 Ω for 35-μm devices and 50-100 Ω for 12-μm devices). A dc bias was applied across the device-load resistor combination. A negative bias was applied to the gate until the oscillations were completely stopped. A positive signal was applied to the gate, and the pulse output developed across a 50-Ω sampling resistor was measured on a sampling scope. Figure 9 shows the output current waveforms. The output waveform when the device was operated in the depletion mode is also included here. In both enhancement and depletion modes, near-transit-time oscillations are present. The dc dissipation is 166 mW in the depletion mode and 135 mW in the enhancement mode, resulting in a saving of 19%.

2. TELD-FET Combination

a. *Principle of Operation.* - Mause et al. [6] suggested that a FET could be used as load with a TELD, but in the common drain configuration the voltage gain is only 0.5. Hashizume and Kataoka [15] used a TELD-FET combination,

15. N. Hashizume and S. Kataoka, "Integration of GaAs MESFETs and Gunn Elements in a 4-Bit Gate Device," Electronics Letters 12(15), 370-372 (22 July 1976).

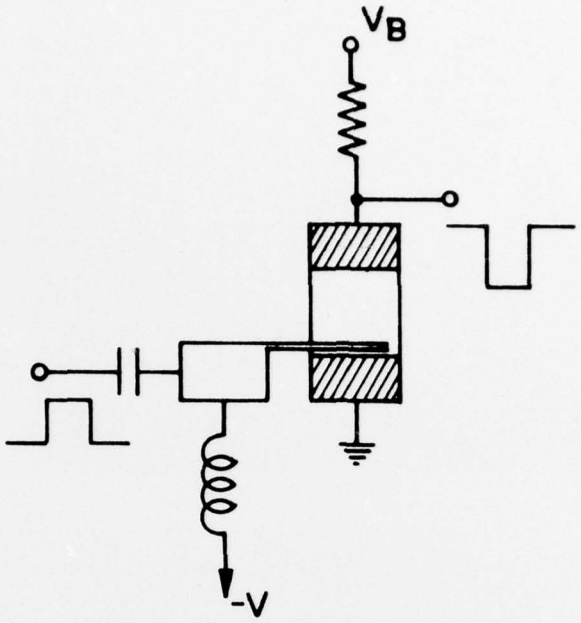
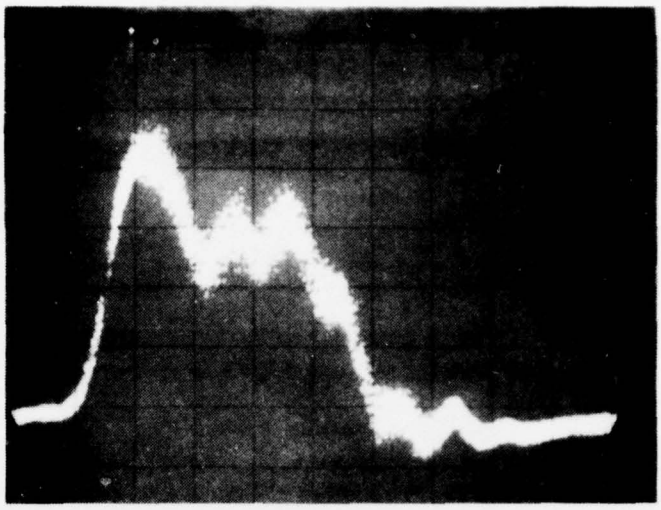


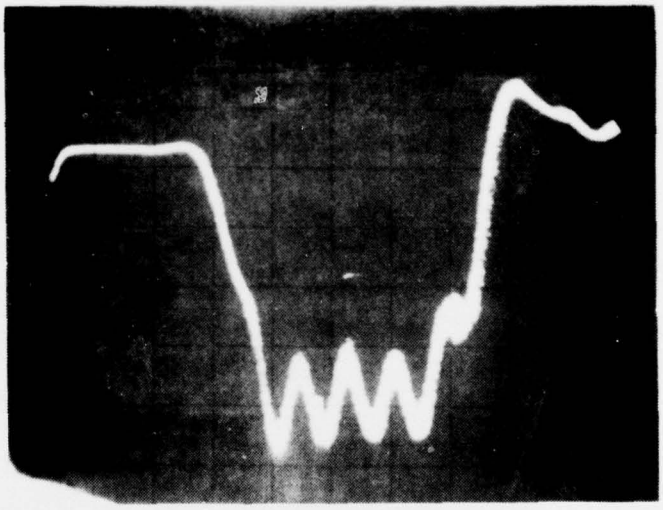
Figure 8. TELD pulse amplifiers with chip load resistor.

but the trigger input was to the TELD. The amplitudes of the signal levels are so high that they do not appear to be compatible with high-speed circuits; in fact, the circuits worked poorly in regard to high-frequency performance. Compared to a TELD, a FET has a much larger transconductance even for the same gate width-to-length ratio. We therefore studied a few pulse amplifier circuits with FET as the trigger element and TELD as a nonlinear element. Figure 10 shows one such pulse amplifier with the TELD in the drain side of the FET. Figure 11 shows the I-V characteristics of the FET for different gate voltages. For our discussion, the TELD characteristics are shown superimposed on the FET characteristics. The devices (FET and TELD) were chosen so that the drain current of the FET for zero gate-source voltage was higher than that of the peak (threshold) current for the TELD. A load line is drawn with a slope equal to the inverse of the low field resistance of the TELD. The operating voltage for the TELD-FET combination was chosen so that when the circuit is triggered the voltage available for TELD would exceed the



(a)

Vertical: 0.4 mA/div.
Horizontal: 200 ps/div.



(b)

Vertical: 1.0 mA/div.
Horizontal: 200 ps/div.

Figure 9. Performance of (a) quasi-enhancement mode and (b) depletion mode TELDs.

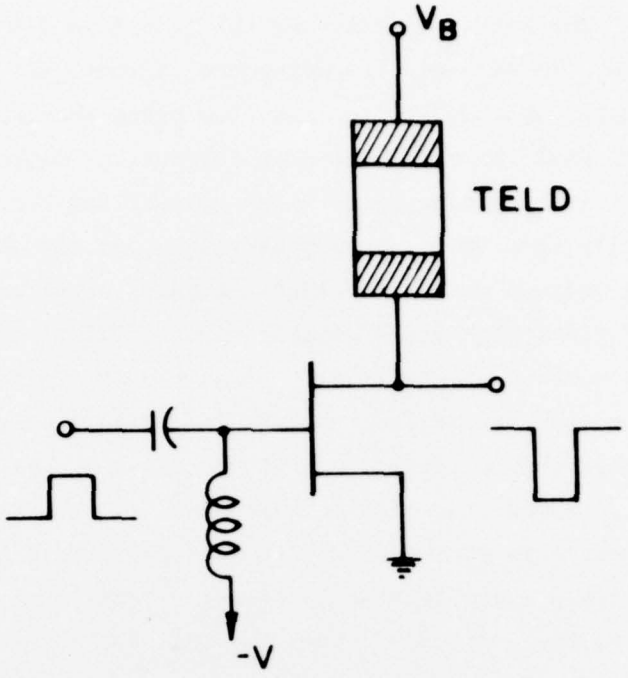


Figure 10. TELD-FET pulse amplifier with TELD as nonlinear load.

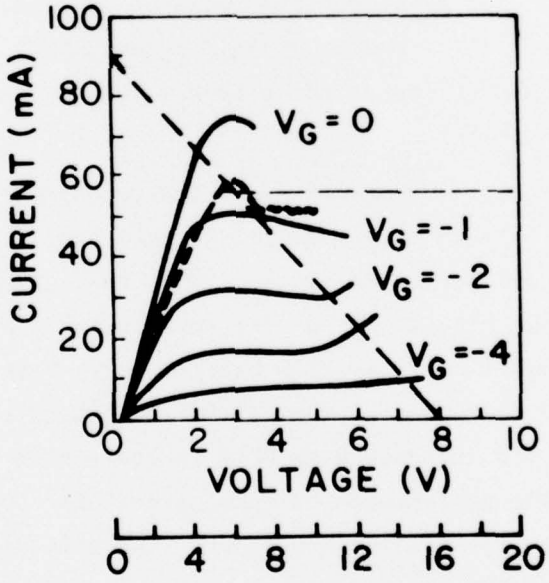
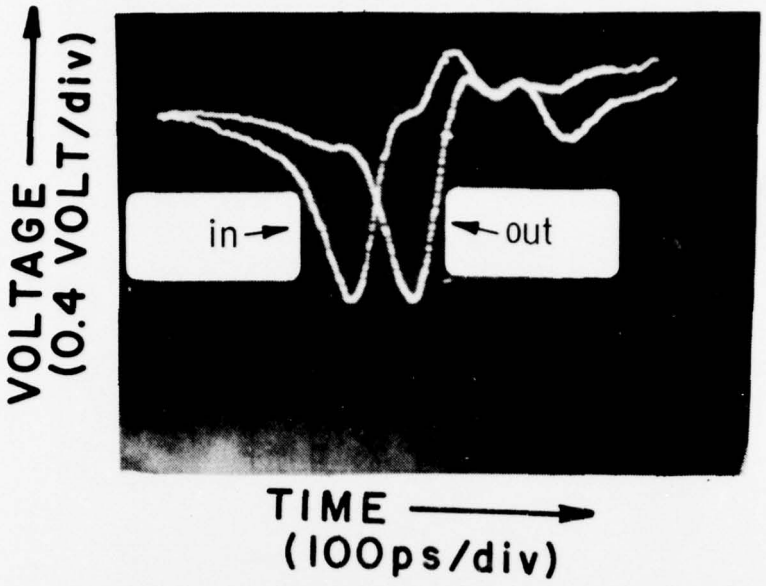


Figure 11. I-V characteristic of a FET with TELD characteristic superimposed. (The lower voltage scale (0-20) applies to the TELD; the current scale is the same for both devices.)

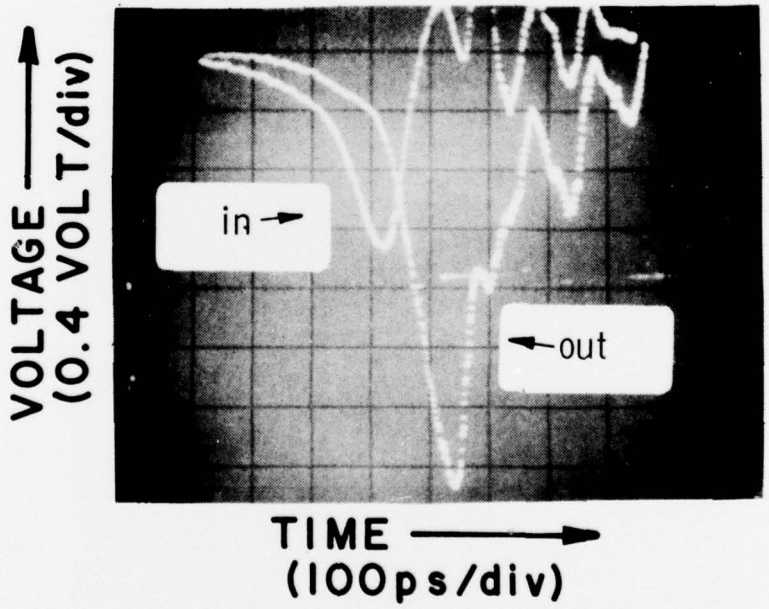
threshold value. The operating bias and the load line fix the quiescent biasing condition. To maintain the quiescent current, FET gate was returned to a negative supply voltage. Also, the bias point was selected so that the quiescent current would be below the peak current and above the valley current for TELD. A positive input applied to the gate of FET increases the drain current momentarily to a value above peak current of the TELD. The load line is such that the voltage across the TELD increases above the threshold value. Under these conditions high field domains form in TELD, and the current drops. Since the valley current of the TELD is lower than the quiescent current, the operating point on the FET shifts into the linear part of the I-V curve. A substantial voltage change thus occurs at the drain of the FET, and a negative output pulse is produced with high voltage gain. The TELD-FET combination described above works as an invertor. In many applications the circuits have to be cascaded, i.e., the output of the first circuit must be capable of triggering the following circuit. This requires the output of the pulse amplifier to be of the same polarity as the input trigger pulse. In order to achieve this the TELD has to be incorporated in the source side of the FET. This configuration will be similar to the common drain configuration discussed by Mause et al. [6]. When a linear load resistor is used, it is not possible to obtain voltage gain in the common drain configuration. The TELD, however, is a nonlinear load, and it can be shown that a voltage gain of up to 2.0 is possible.

b. *Experimental Results*. - Figure 12 shows the performance of a TELD-FET invertor circuit. Pulses as narrow as 150 ps have been processed through this circuit. The pulse amplifier has a gain of 2-4. Figure 13 shows the performance of the same circuit for a wide input pulse. Near-transit-time oscillations characteristic of the TELD are present. These observations confirm the principle of operation of the circuit discussed earlier.

Another circuit was designed with TELD in the source side of the FET (source follower). The performance of this circuit is shown in Fig. 14. The output polarity is the same as the input. The voltage gain of this circuit is unity.

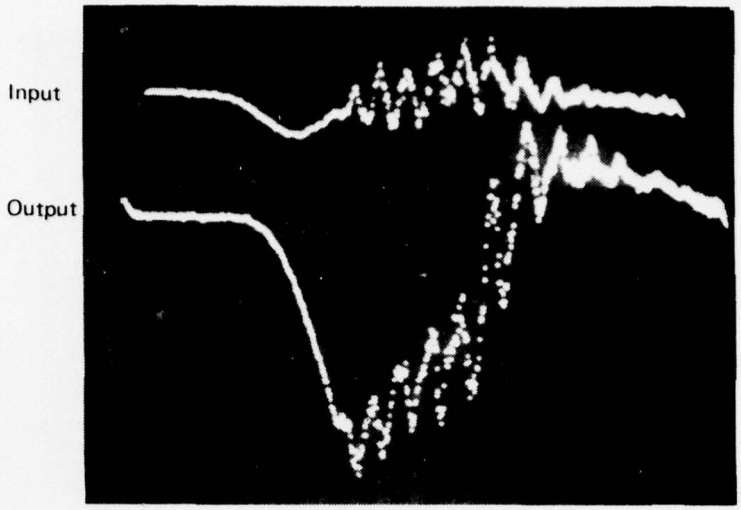


(a)



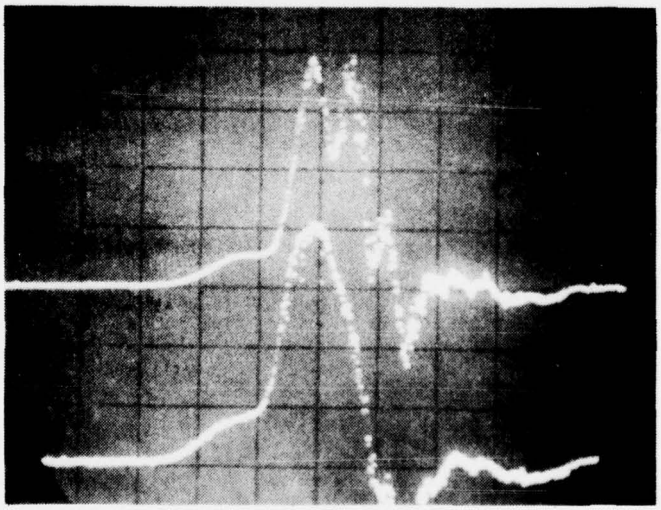
(b)

Figure 12. Performance of TELD-FET invertor when TELD is (a) in the linear part of I-V and (b) in the nonlinear part of I-V.



Horizontal Scale: 200 ps/div.
(input pulse is inverted for display).
Vertical Scale: 0.4 V/div.

Figure 13. Response of a TELD-FET circuit to a wide input pulse.



Horizontal Scale: 200 ps/div.
Vertical Scale: 0.2 V/div.

Figure 14. TELD-FET source follower performance.

SECTION VI

CONCLUSIONS

Thin epitaxial GaAs layers were grown on semi-insulating substrate by means of RCA's vapor hydride synthesis. Oxygen- and chrome-doped semi-insulating buffer layers and high-resistivity undoped buffer layers were grown to improve the quality of the epi-layers. Further improvements are required in this area. Electrolytic etching with or without photostimulation was used to obtain uniform nd product across the wafer. Devices with 35-μm and 12-μm cathode-anode spacing were fabricated and evaluated. The devices did show the quasi-enhancement mode operation. Further optimization of material and device parameters is required to improve the device performance. TELD-FET combination was used in a new mode of operation; this combination appears to be superior to circuits in which only TELDs or FETs were used. Preliminary data on computer simulation agree with the theoretical and experimental results. For a better understanding of the practical applications of TELD-FET combinations, simulations for devices with higher doping density and higher nd product have to be carried out.

APPENDIX*

A computer program was developed under a concurrently sponsored ONR contract, No. N00014-76-C-0465, for simulating the performance of TELDs.

Figure A-1 shows a flow chart for the program used to simulate the three-terminal of planar TELD. The initialization is done arbitrarily or from a file containing a known operating condition (values of N and V). The current flow at each electrode is available for any time step. Steady-state results were obtained from the dynamic program by executing until all transients died out.

Some nonphysical effects were sometimes found to occur due to the truncation of the length of the ohmic contact in the model. Most of these effects were eliminated by an increase in donor density in the regions under the contacts. This is justified by the fact that the contacts are always much bigger than the active device, so that less field should occur beneath them.

This program was used to obtain preliminary data on the quasi-enhancement mode operation of TELDs. The parameters used for simulation are: $N_D = 5 \times 10^{15}\ cm^{-3}$, D = 2 μm, $\ell_{ca} \simeq 13$ μm, $\ell_g = 2$ μm, $V_B = 6$ V, and $V_g = -4$ V. Figure A-2 shows the surface potential as a function of the distance from the gate to the anode. In the quiescent state there is a high field under the gate, but the effective nd product there is below the critical value; the electric field outside the gate is far below the threshold field. Therefore, no accumulation layers or domains formed in the quiescent state. When the gate bias is charged from -4 to 0 V (by application of a 4-V positive pulse), high field domains form, which then travel to the anode in about 60 ps. Figures A-2 and A-3 show the cathode and anode current changes, respectively, when the 4-V positive pulse was applied to the gate. The current changes from a steady-state value of 126 μA/μm gate width to one of 193-μA/μm gate width, i.e., 53%. Transients due to the displacement current can be seen in the first 5-10 ps after switching. In another simulation we found that -2.0 V on the gate with the same device parameters was able to provide the steady state, and therefore required only 2 V for triggering. But the percentage current change was smaller.

*This work was carried out by Walter R. Curtice under OONR contract No. N00014-76-C-0465.

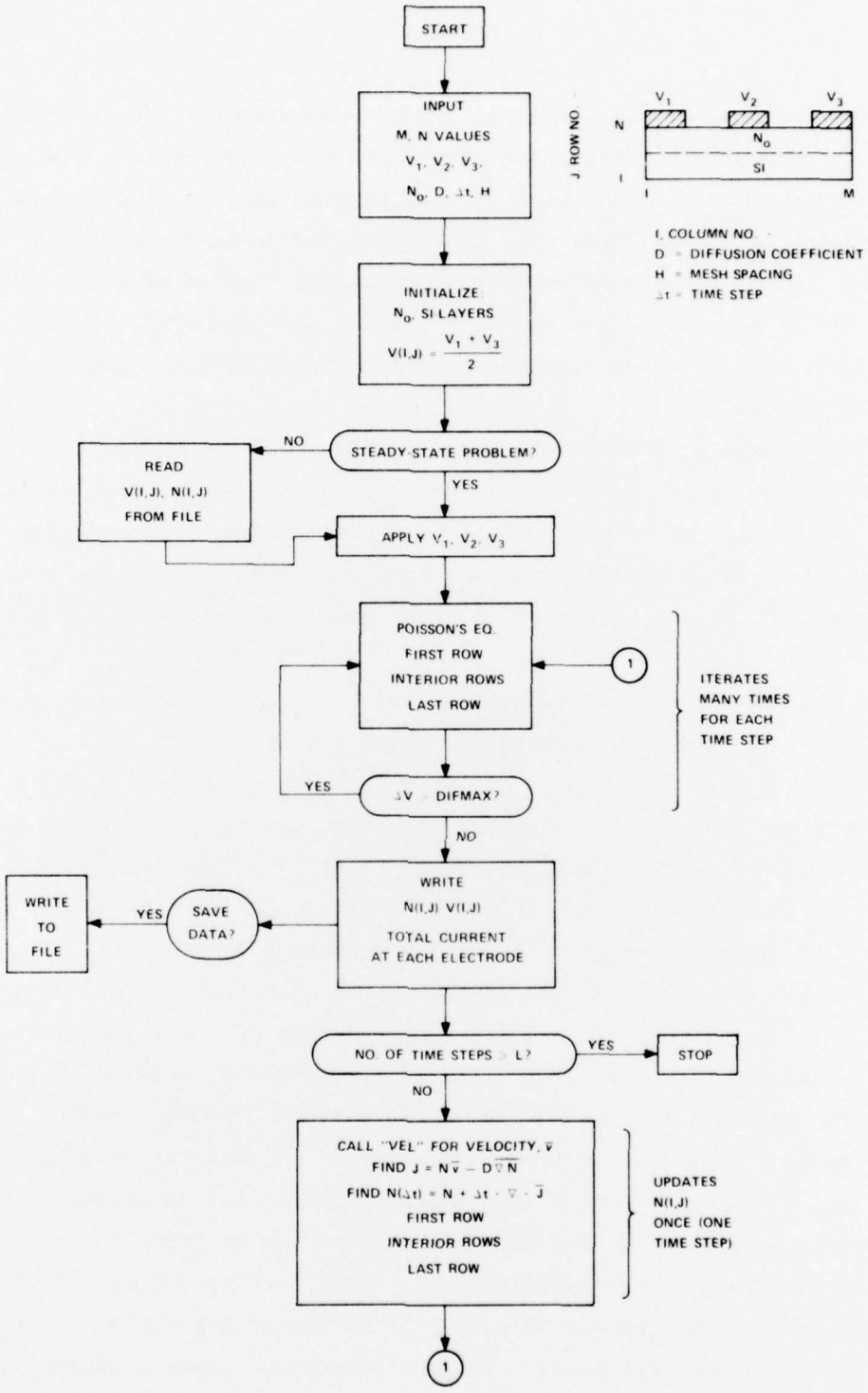


Figure A-1. Flow chart for computer simulation of TELDs.

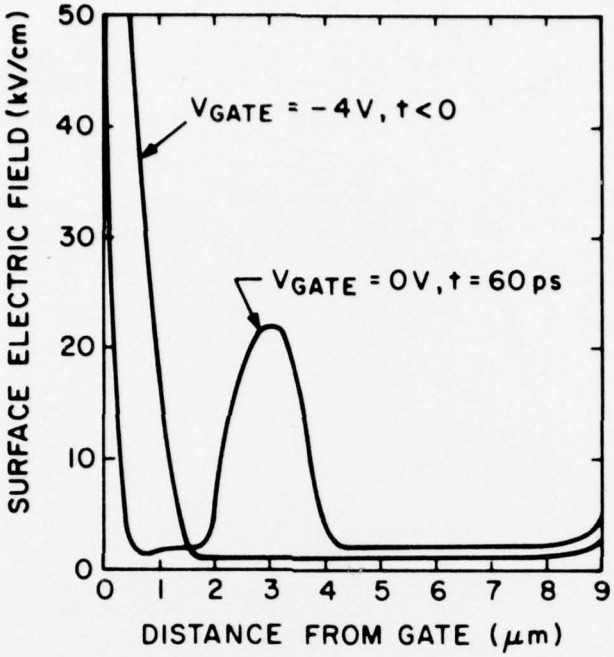


Figure A-2. Surface electric fields vs distance from gate with gate voltage as a parameter.

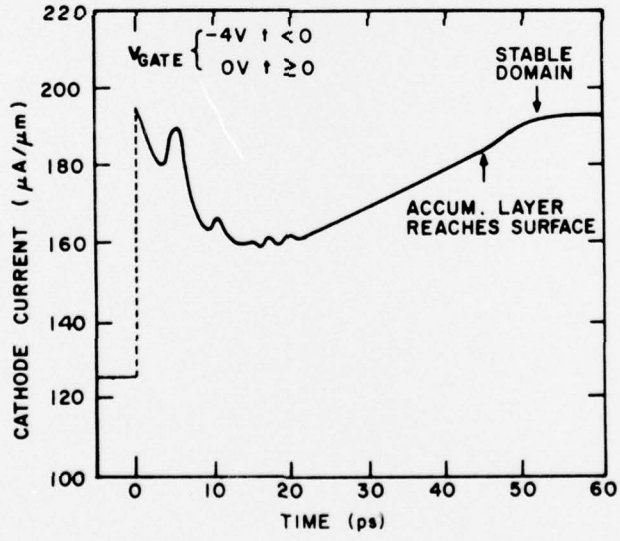


Figure A-3. Cathode current as a function of time in quasi-enhancement mode TELD.

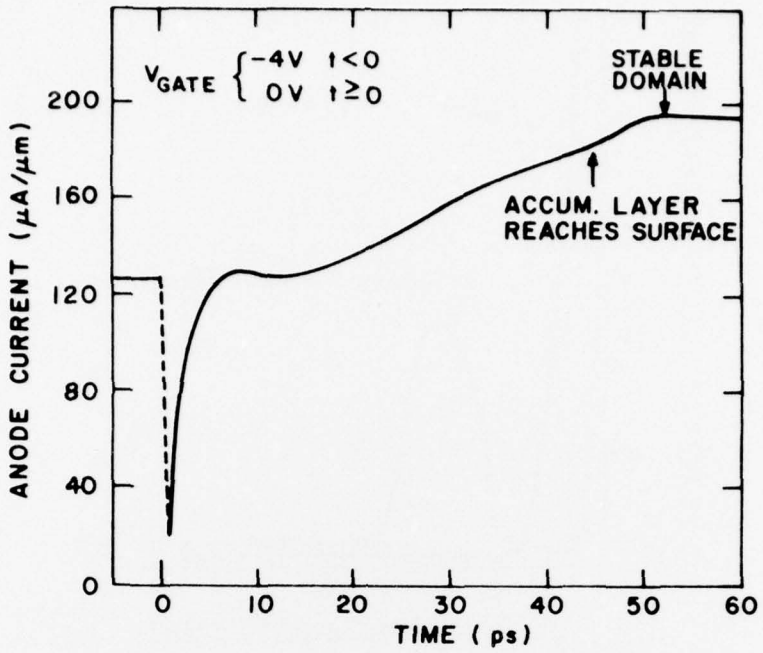


Figure A-4. Anode current as a function of time in quasi-enhancement mode TELD.

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