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TRADE-OFF INVESTIGATIONS AND DETAILED DESIGN OF POWER INVERTERS--ETC(U)
JAN 77 W G LAWRENCE DAAG53-76-C-0077
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

An investigation to determine the optimum design for a modular family of power inverters has been completed. The inverters are to provide 60 Hz or 400 Hz (selectable) sine wave outputs at 120V/240V, single phase/3-phase when supplied from a 30-60 Vdc source. Included in the family are inverters of from 1.5 to 10 kW. Optimization is done with regard to cost, size, weight, efficiency, reliability, availability and maintainability. Various options were examined during Phase I. Phase II: detailed study of options.

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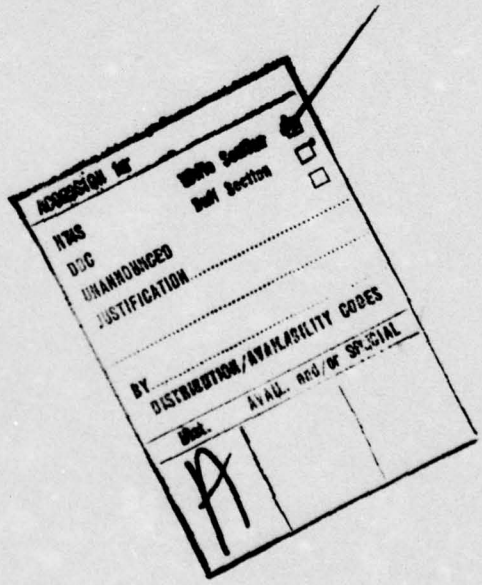
## PREFACE

The work reported herein was performed by DECC (Delta Electronic Control Corporation) under contract to the United States Army Mobility Equipment Research and Development Center (contract DAAG53-76-C-0077). The Contracting Officer's Representative was Dietrich J. Roesler at Fort Belvoir, Virginia.



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## 1.0 INTRODUCTION

1.1 SCOPE. This report describes an investigation of design trade-offs leading to the design of a family of low cost, light-weight power inverters providing single-phase or three-phase ac power when supplied from batteries, fuel cells or other sources of 30-60 volts dc.

The investigation was performed by Delta Electronic Control Corporation (DECC) of Irvine, California for the U.S. Army Mobility Equipment Research and Development Center (MERDC).

The report includes a discussion of the comparisons and trade-offs performed and a recommended design based on the study. Although no hardware was produced to verify the design, results of tests performed by DECC on similar equipment have been utilized.

1.2 OBJECTIVES. The objective of this study was to investigate design trade-offs and to determine the optimum inverter design within the scope of the program with particular regard to

1. Low production cost
2. Minimum size and weight
3. Maximum efficiency
4. Maximum reliability, availability, and maintainability

Specific design objectives for the inverters are detailed in Tables 1-1, 1-2, and 1-3.

## OBJECTIVES

| DESCRIPTION | DATA |
|---|---|
| Power | See Table 2 |
| Freq In/Freq Out | DC/60 or 400 Hz |
| Voltage In/ Voltage Out | 30-60 DC see Table 2 |
| Power Factor | .8 |
| Phases | see Table 2 |
| Frequency Regulation | ± .5% short term ± 1% long term |
| Voltage Regulation | 2% |
| Single Harmonic/ Total Harmonic | 2% / 5% * |
| Deviation Factor | 5% * |
| Efficiency | 85% |
| Cooling | Forced convection |
| Transient Overload | 120% for 10 sec. @ $V_{in}$ = 40 V |

| DESCRIPTION | DATA |
|---|---|
| Paralleling | Any number |
| Protection | Reverse polarity, overload, short circuit, high or low input voltage |
| Noise | at 10 ft: 68 db max. |
| EMI | MIL-STD-461 |
| MTBF | 5000 hrs. min. |
| Temperature Range | Operation: -65°F to +125°F |
| | Storage: -65°F to +155°F |
| Altitude | Sea level to 8000 ft. |
| Humidity | 5 to 95% |
| Housing | Weatherproof |
| Volume | See Table 3 |
| Weight | See Table 3 |

TABLE 1-1

* Add 1% for single phase

## TABLE 1-2

### Voltage Connection

| kW Rating | Single Phase | | | Three Phase |
|---|---|---|---|---|
| kW | 120 V 2 wire | 240 V 2 wire | 120/240 V 3 wire | 120/208 V 4 wire |
| 1.5 | X | X | | |
| 3 | X | X | X | X |
| 5 | X | X | X | X |
| 10 | X | | X | X |

## TABLE 1-3

### Weight and Volume of Inverters

| Power kW | Max. Weight lbs | Desired Weight lbs | Max. Volume $in^3$ | Desired Vol. $in^3$ |
|---|---|---|---|---|
| 1.5 | 55 | 30 | 1400 | 900 |
| 3 | 80 | 60 | 2500 | 1750 |
| 5 | 130 | 90 | 3500 | 3250 |
| 10 | 250 | 180 | 6500 | 6000 |

## 2.0 DISCUSSION

### 2.1 TRADE-OFF STUDY.

2.1.1 General Considerations. The guidelines for this investigation limit the inverter design to the general form shown in Figure 2-1. Individual block functions and design trade-offs are discussed below.

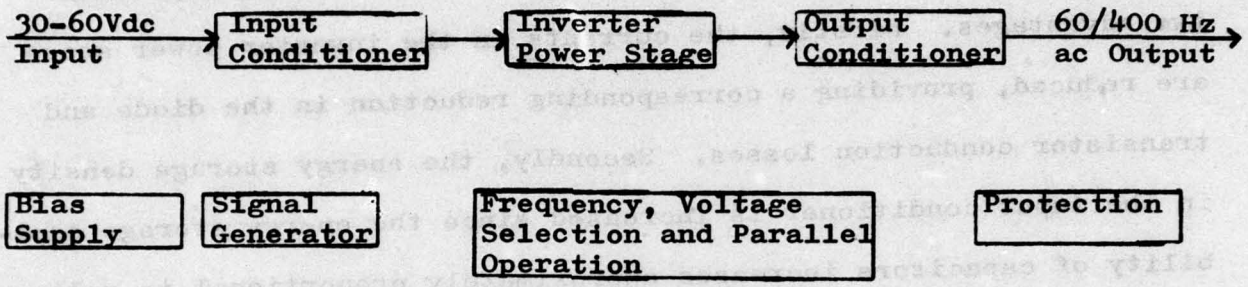



Figure 2-1. Functional Diagram

2.1.2 Input Conditioner. The input conditioner may perform the following functions:

1. Reduction of conducted electromagnetic interference (EMI)
2. Energy storage
3. Voltage transformation
4. Voltage regulation and isolation
5. Input protection

2.1.2.1 EMI Reduction. Some filtering will generally be required in the input line to minimize conducted EMI to the level specified in MIL-STD-461.

2.1.2.2 Energy Storage. The input current to the inverter power stage may contain an ac component (at a frequency of twice the inverter frequency). As a result, an ac voltage will develop across the source impedance and will tend to modulate the inverter output,

generating unwanted harmonic components. The input conditioner will generally include a large capacitance to bypass the ac current.

2.1.2.3 Voltage Transformation. For a given level of power, the current is inversely proportional to the voltage. Therefore, the current requirements from the input conditioner can be minimized by using the highest practical voltage. Higher voltages provide two advantages. Firstly, the currents in the inverter power stage are reduced, providing a corresponding reduction in the diode and transistor conduction losses. Secondly, the energy storage density in the input conditioner is increased since the energy storage capability of capacitors increases approximately proportional to voltage. Thus, to minimize both output losses and capacitor volume, the input conditioner section would provide the inverter power stage with the highest practical voltage. A voltage transformation to 200 Vdc is attractive because it conveniently provides the desired output voltages without further transformation in the output conditioner, and simultaneously avoids the use of components with unduly high ratings and poor availability. The use of 200 Vdc reduces the volume of the energy storage capacitors to 15% of the volume required without transformation. This advantage is partially offset by the needed addition of the voltage converter circuitry. Nonetheless, there appears to be a net advantage to voltage transformation especially if the converter includes a voltage regulator.

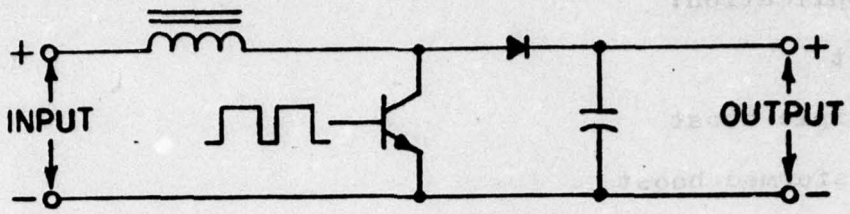
The following dc-dc converter types were evaluated for use in this application:

1. Boost
2. Multiple boost
3. Transformed boost
4. Transformer coupled boost
5. Pulse-width modulated inverter
6. Series regulator plus inverter
7. Boost plus inverter

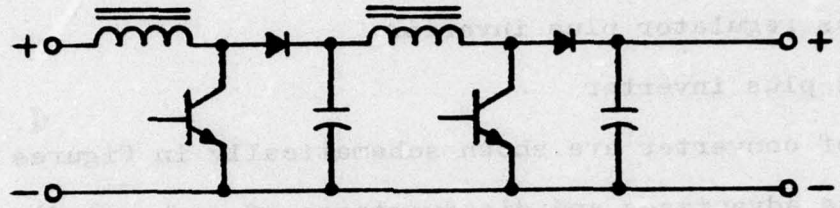
The types of converter are shown schematically in Figures 2-2a and 2-2b and the advantages and disadvantages of each are discussed below.

2.1.2.3.1 Boost Converter. The boost converter is the simplest means of transforming a low, unregulated dc voltage to a much higher regulated dc voltage. Only one transistor (or group of parallel transistors) is required, minimizing cost. Only one diode is required in the output circuit and thus the efficiency is high. EMI and switching control problems are minimal. Large ratios of output-to-input voltage unfortunately require switching transistors to have very short "off" times which produces transistor control problems. The boost converter also does not provide the input-output isolation which may be necessary.

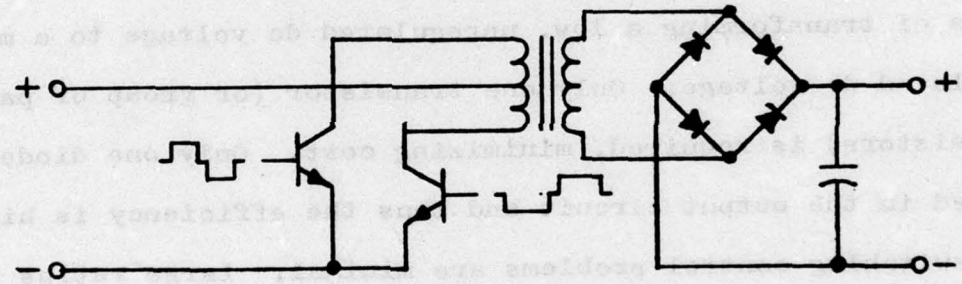
2.1.2.3.2 Multiple Boost. Using two or more seriesed boost regulators makes higher output-to-input voltage ratios more feasible, but adds complexity and cost and still provides no isolation.



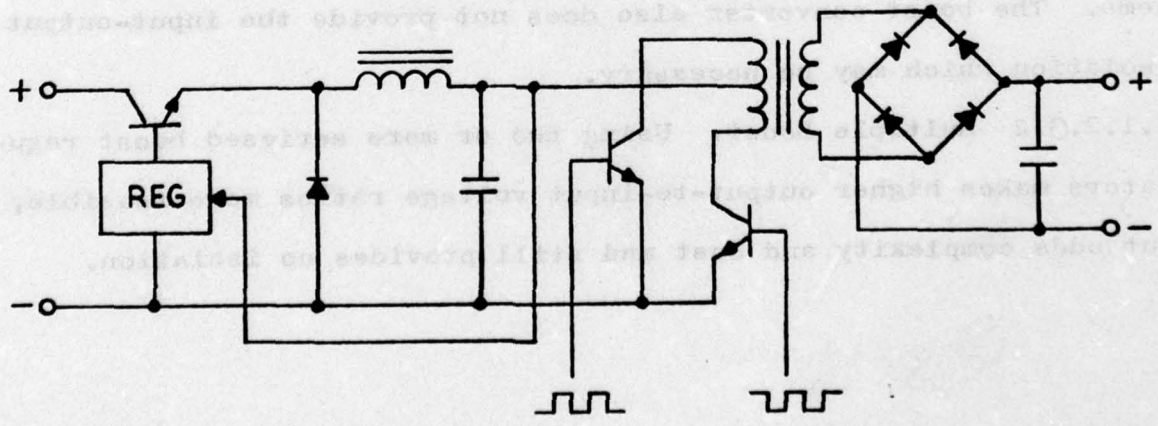

BOOST



MULTIPLE BOOST

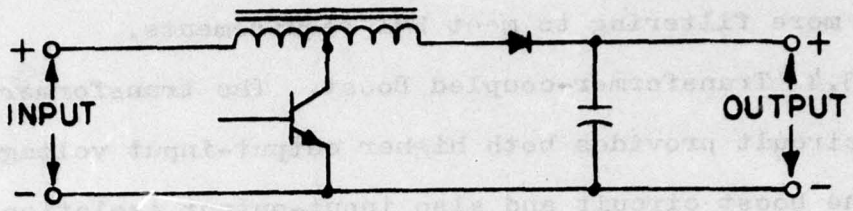


PULSE WIDTH MODULATED

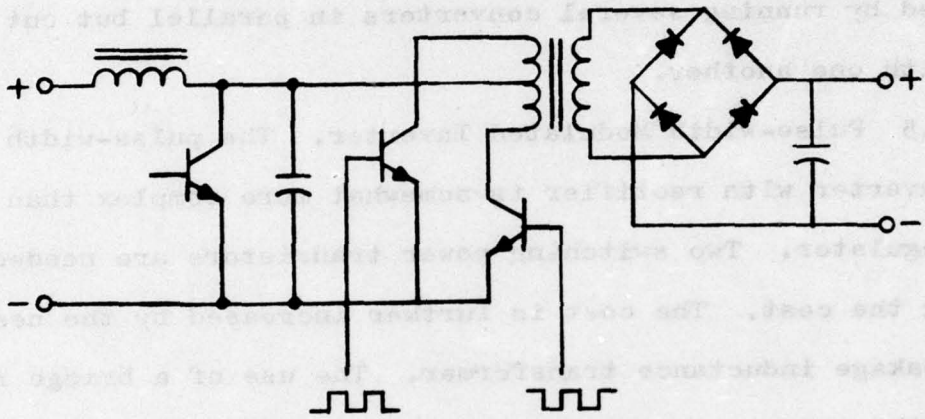



SERIES REGULATOR PLUS INVERTER

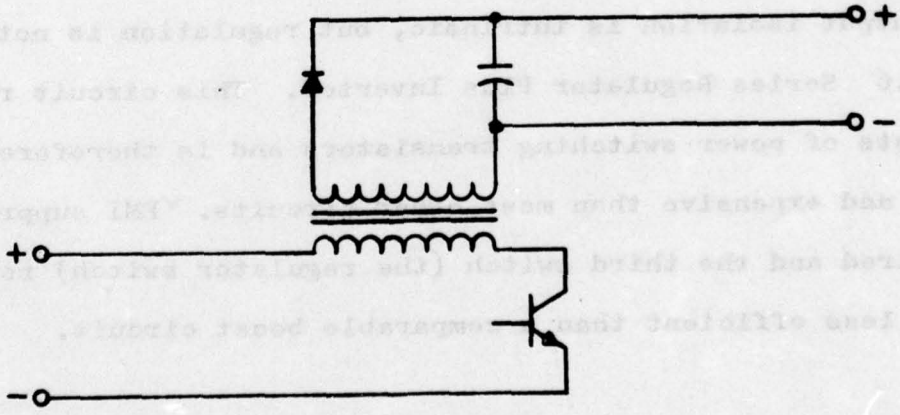
FIG 2-2, DC-DC CONVERTER




TRANSFORMED BOOST




BOOST PLUS INVERTER




BOOST, TRANSFORMER COUPLED

FIG 2-2, DC-DC CONVERTER

2.1.2.3.3 Transformed Boost. The transformed boost circuit can provide higher output-input voltage ratios than the boost circuit, but the input current is no longer ideally dc. Therefore, it requires more filtering to meet EMI requirements.

2.1.2.3.4 Transformer-coupled Boost. The transformer coupled boost circuit provides both higher output-input voltage ratios than the boost circuit and also input-output isolation. Again, only one switching transistor (or parallel group) is required and only one diode in the load circuit, although there are transformer losses. EMI filtering is still a problem, but the problem can be minimized by running several converters in parallel but out of phase with one another.

2.1.2.3.5 Pulse-width Modulated Inverter. The pulse-width modulated inverter with rectifier is somewhat more complex than the boost regulator. Two switching power transistors are needed, increasing the cost. The cost is further increased by the need for a low leakage inductance transformer. The use of a bridge rectifier in the output necessarily reduces the efficiency, generally to less than that of a comparable boost regulator. Transient suppression presents a problem as in the transformer coupled boost. Input-output isolation is intrinsic, but regulation is not.

2.1.2.3.6 Series Regulator Plus Inverter. This circuit requires three sets of power switching transistors and is therefore more complex and expensive than most other circuits. EMI suppression is required and the third switch (the regulator switch) renders the circuit less efficient than a comparable boost circuit.

2.1.2.3.7 Boost Plus Inverter. The advantages of the boost-plus-inverter circuit are that EMI filtering and input-output isolation are intrinsic. Also since the square-wave inverter provides most of the voltage boost, the narrow "off" times are not required in the boost circuit. Transient suppression remains a problem. A bridge circuit for the inverter would improve this, but at the cost of adding two additional sets of switching transistors to an already complex, inefficient and expensive converter.

2.1.2.3.8 Recommendation. Table 2-1 summarizes the advantages and disadvantages of the various circuits. For the present application, the transformer-coupled boost circuit would appear to offer a reasonable compromise. Although there are transformer losses, the circuit provides input-output isolation, eliminating the need for an isolation transformer of comparable loss in the output conditioner. Transient suppression is possible by means of recovery circuits or by using the energy for useful work such as powering the bias supply. EMI suppression is necessary, but the problem can be minimized by running several converters in parallel and out of phase with one another. This requires no increase in the number of power transistors, minimizing the cost difference.

2.1.2.4 Voltage Regulation and Isolation. Voltage regulation in the input conditioner is a necessity for many types of inverter power stage. Input-output isolation is necessary at some point in the inverter, and would generally be included in either the input conditioner or the output conditioner.

TABLE 2-1. DC/DC CONVERTER

| CHARACTERISTIC TYPE | BOOST | PULSE-WIDTH MODULATED | SERIES REG. & INVERTER | TRANSFORMED BOOST | BOOST & INVERTER | TRANSFORMER COUPLED BOOST |
|---|---|---|---|---|---|---|
| Number of switches carrying peak current | 1 | 2 | 3 | 1 | 3 | 1 |
| Complexity | Least complex | Moderate | Most complex | Nearly least complex | Most complex | Moderate |
| Input EMI Filtering | Intrinsic | Must add | Intrinsic | Must add | Intrinsic | Must add |
| Input/Ouput Isolation | No | Yes | Yes | No | Yes | Yes |
| Weight | Lightest | Moderate | Heaviest | Light | Heavy | Light |
| Cost | Least | Between moderate & most expensive | One of most expensive | Moderate | One of most expensive | Moderate |
| Switching Transient Control | Easiest to suppress | Difficult to suppress. Requires low leakage inductance transformer & dissipative suppression networks | Same as pulse-width modulated type | Easy to suppress | Same as pulse-width modulated type | Easy to suppress |
| Efficiency | High. One transistor drop in input circuitry | Fairly high. Less than with boost circuit because of secondary bridge & transient suppression losses | Poor. Two transistors in series conduct input current | High. One transistor conducts input current | Fairly high. Only one transistor conducts input current, others much less | High. One transistor conducts input current |

2.1.2.5 Input Protection. The input conditioner may also include several input protection circuits to protect against excessive input voltage, excessive input current, improper input polarity, or other improper condition.

2.1.3 Inverter Power Stage. The inverter power stage performs the basic function of the inverter by changing the input dc into the required output. The following is a list of the common forms:

1. Class-B linear power amplifier
2. Square-wave inverter plus filter
3. Quasi-square-wave inverter plus filter
4. Additive combination of rectangular waveforms plus filter
5. Pulse-duration modulated rectangular waveform plus filter

2.1.3.1 Class B Linear Power Amplifier. This form of power stage may be eliminated immediately from consideration on the basis of efficiency. The entire inverter is to have a total efficiency of 85%, and even an ideal Class-B amplifier has a maximum efficiency of 78.5%.

2.1.3.2 Square-Wave Inverter Plus Filter. The square wave inverter is the simplest type in principle, but unfortunately has several offsetting disadvantages. The square wave is identical to the output signal in frequency. The filters required must remove all frequencies above the fundamental and therefore are physically large and generally heavy because of the low frequencies involved. Because the output is dependent on the voltage supplied to the power stage, the input conditioner must supply a closely regulated voltage to the stage.

2.1.3.3 Quasi-square-wave Inverter Plus Filter. The quasi-square-wave inverter is similar to the square-wave inverter except that pulse-width modulation may be used to control the output amplitude. Alternately, a fixed duty cycle could be imposed to minimize the third harmonic in the output and reduce filter requirements.

2.1.3.4 Additive Combination of Rectangular Waveforms Plus Filter. The filter requirements of the previous inverter power stage form may be further reduced by combining rectangular outputs from several inverters to a stepped waveform approximating a sine wave. While decreasing the filter demands, this form is complex and separate filters are still required for each required output frequency.

2.1.3.5 Pulse-duration Modulated (PDM) Rectangular Waveform Plus Filter. The filter requirements of the above forms are greatly reduced by generating a high-frequency rectangular waveform which is pulse-duration modulated to synthesize the output sine wave while simultaneously controlling the amplitude and frequency of the output. The filter need only remove the high-frequency switching frequency from the output signal. Filter design is, therefore, relatively independent of the output frequency and the same filter may be used for the 60 Hz and 400 Hz outputs and for any other reasonable frequency desired. An additional advantage is that the filter impedance is lower at the output frequencies, reducing the phase shift across the filter and minimizing problems of parallel operation and operation with unbalanced loads. These advantages appear to outweigh the slight increase in complexity of this form over most other forms of inverter power stage.

2.1.3.6 Switches for PDM Inverter Power Stage. In the PDM power stage, rectangular PDM signals are applied to power switches by signal-generating circuitry. The power switches may be connected in either push-pull or bridge configuration, and within the guidelines for this study, may be either transistors or SCR's (silicon controlled rectifiers). Push-pull circuits have only one switching element at a time in series with the load, minimizing losses, but require an output transformer, which adds weight and further losses. Furthermore, each switch element must be capable of withstanding twice the conditioner output voltage. A bridge circuit, on the other hand, places two switching elements in series with the load, adding switching losses. An output transformer is not necessarily needed, however, if input-output isolation has been provided elsewhere in the inverter, and the bridge avoids the energy recovery problems generally associated with the leakage inductance in push-pull circuits.

2.1.3.7 Transistors vs SCR's. At power levels above 50kW, SCR's begin to have an advantage over transistors. For a given high voltage, SCR's have a much greater current carrying capability than transistors. The overall cost of a single, large SCR including commutation circuitry does not appear to be significantly less than that of an equivalent number of transistors in parallel. At lower power levels, in particular, transistors generally appear more attractive than SCR's because of the following disadvantages of SCR's:

1. Limited maximum switching frequency
2. High conduction losses

3. Difficult to protect if load is shorted

4. Susceptible to spurious switching from transients

From the standpoint of maintainability, there is a distinct advantage if the whole family of inverters can be constructed from a single type of power switch module. One attractive method of doing this would be to use transistors for all inverters. Transistors may be paralleled to provide the necessary load capability. An advantage of this method is that it provides an opportunity to improve reliability at minimum extra cost if redundant transistors are then added allowing the production of full rated power even if one transistor fails. Using several transistors distributed in space also helps thermally. Spreading the heat source out makes natural convection cooling feasible. Normally, high-power SCR's must be cooled by forced air or liquid-cooled heat sinks.

2.1.3.8 Recommendation. From the standpoints of size, weight, efficiency, reliability, and maintainability, the most satisfactory form of inverter power stage appears to be a bridge configuration using transistors as switches controlled by a pulse-duration modulated signal of high frequency. This form is also appealing from the cost standpoint. In general, those forms which are less complex in their control require more expensive filtering. Figure 2-3 shows the recommended inverter power stage form.

2.1.4 Output Conditioner. The output from the inverter must be selectable so as to provide the required voltages. In addition, the output conditioner may include output filtering and input-output isolation if it is not included elsewhere in the inverter.

Voltage selection and isolation can both be accomplished easily by the use of an output transformer. Transformer secondaries could be rewired in series or parallel to provide the desired output voltages. The disadvantage of this form of output conditioner is that the transformers required are large and heavy, especially if a 50 Hz output were required at some future time. The output transformer may be eliminated if input-output isolation is provided elsewhere in the inverter. Transformer isolation in the output conditioner also inevitably creates some audio noise, whereas an isolation transformer in the input conditioner would operate above the audible range. On the other hand, transformer output eliminates any dc component in the output signal. Such a dc component tends to act as a brake which would reduce the efficiency of induction motor loads. If the output transformer is eliminated, the inverter will require a design which will minimize the dc output component, e.g., by feedback.

Without the output transformer to provide output voltage selection, the selection must be performed in another manner. Proper connection and reconnection of stages shown in Figure 2-3 can provide the appropriate outputs. The 3 kVA and 5 kVA inverters require 4 different connection combinations. Figure 2-4 shows how six of the stages shown in Figure 2-3 (or paralleled sets of stages) can be reconnected to provide all of the required outputs.

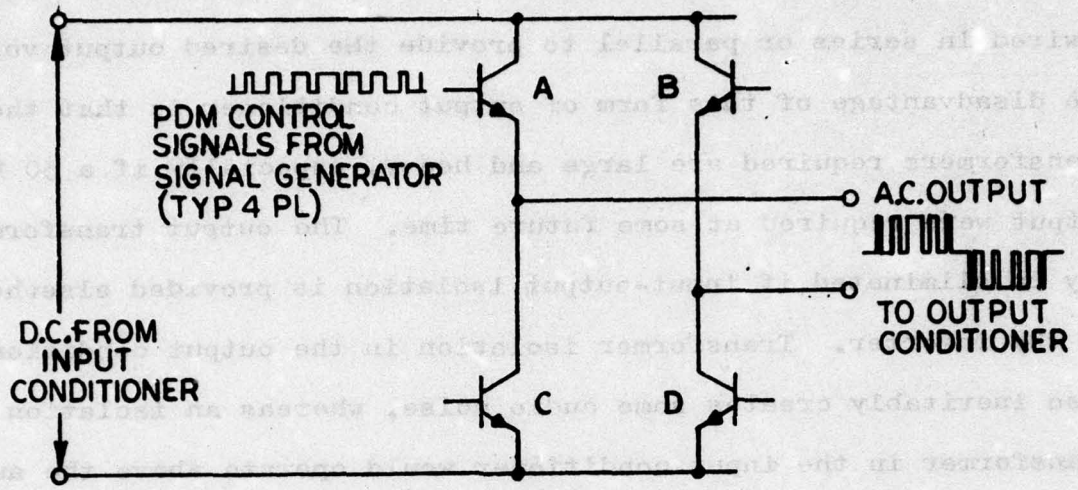



Figure 2-3. Inverter Power Stage Form

2.1.5 Bias Supply. The dc bias supply provides the bias voltages for all of the circuitry. To provide a variety of bias voltages, the bias supply will generally consist of dc-ac inverter which may operate from the input voltage directly or from a boosted dc voltage. It will include a transformer to provide the different voltages, and appropriate rectifiers.

2.1.6 Signal Generator. The inverter power stage acts as a power amplifier for signals developed at lower levels in the signal generator. Each inverter requires generation of single phase and/or three phase outputs of closely controlled frequency and amplitude. Alternative sine wave sources include sine-wave oscillators, square-wave generators with filters, quasi-square-wave generators with filters, and digital-to-analog converters.

2.1.6.1 Sine-wave Oscillator. The sine-wave oscillator has two distinct disadvantages; two sets of frequency-determining elements are required for the two frequency outputs, and for three-phase generation the three oscillators must be kept precisely 120° apart in their phasing.

2.1.6.2 Square-wave Generators with Filters. A square-wave source is simple to produce, but filtering becomes a problem along with the need to maintain proper phasing with changes in component values.

2.1.6.3 Quasi-square-wave Generators with Filters. A quasi-square wave reduces the filtering demands, but a three-level logic signal is required which is not readily available from standard logic elements.

2.1.6.4 Digital-to-analog Converter. While seeming more complicated at first glance, this method of signal production has distinct advantages over the other forms. Each of the three separate phases may be derived from a common counter and control network driven by a single crystal-controlled oscillator. The number of steps provided in the converter for synthesizing the sine-wave may be chosen to provide low distortion, and minimum filtering and phase shift. By suitable selection of the oscillator frequency, a single crystal oscillator can be used to provide 50, 60 or 400 Hz outputs just by changing the countdown between the oscillator and the digital-to-analog converter. Figure 2-5 shows the major components of the sine-wave synthesizing circuitry. The crystal controlled oscillator feeds a frequency controlled signal to the divider through control circuitry. This control circuitry may

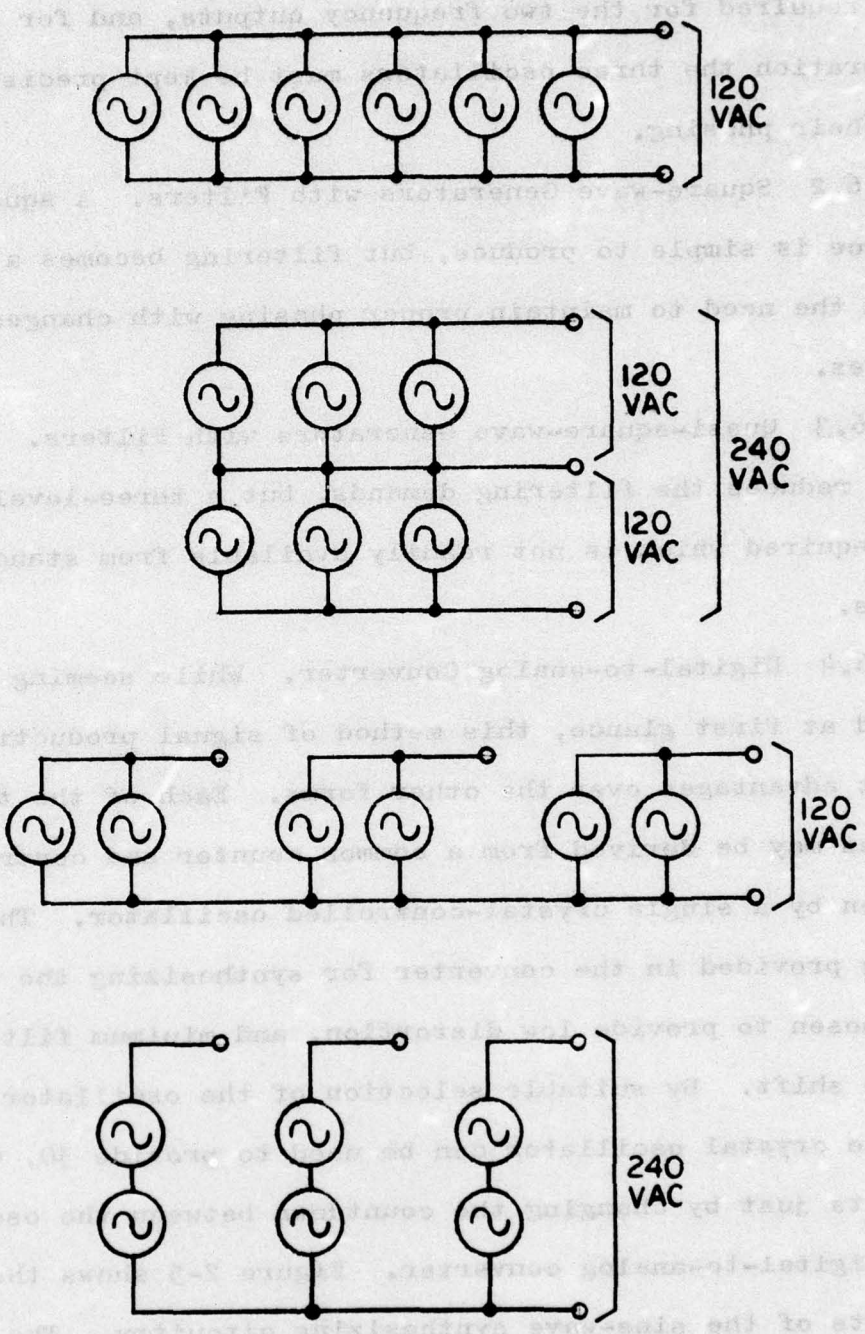



FIG 2-4, OUTPUT STAGE INTERCONNECTIONS

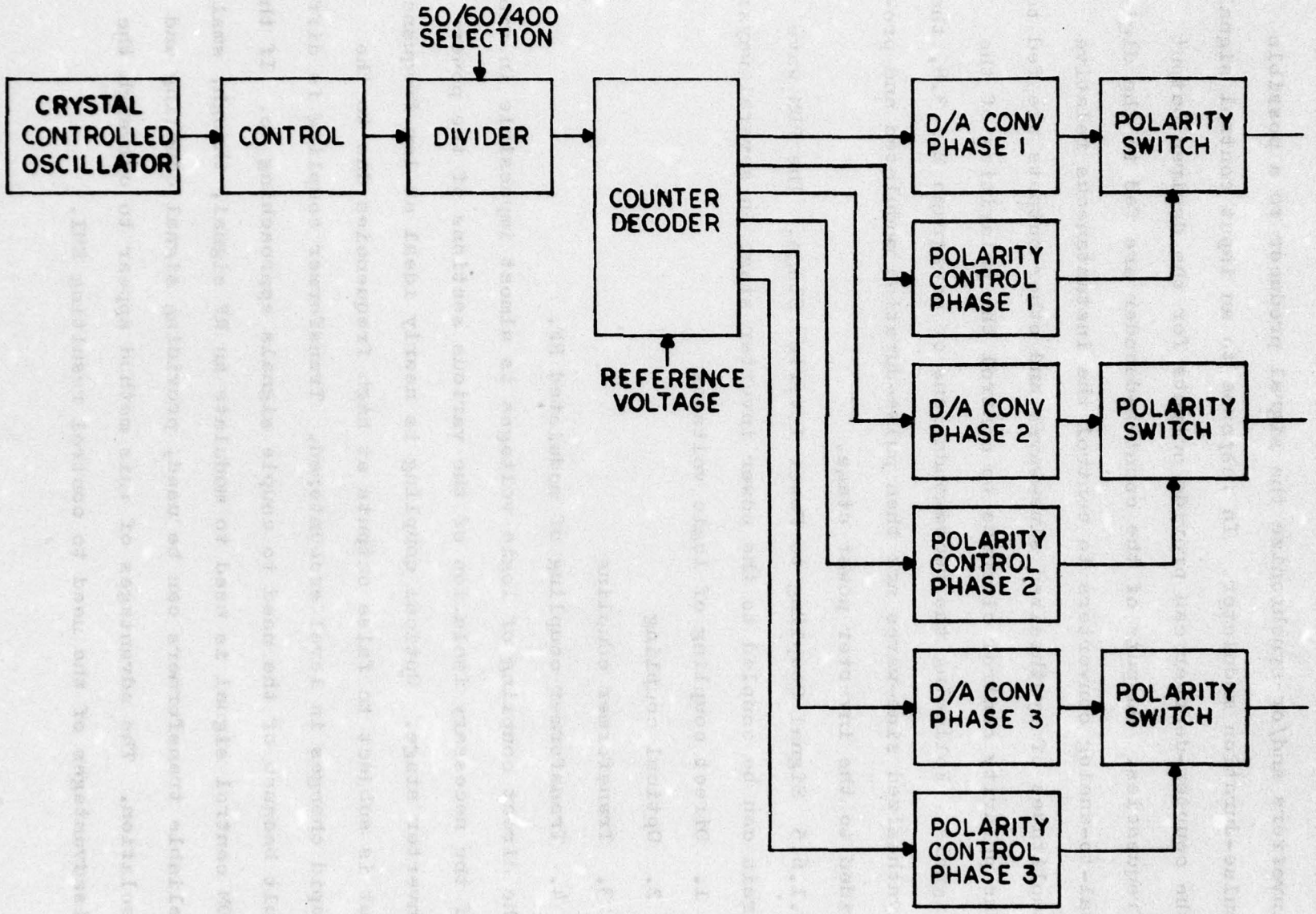



FIG 2-5, SINE WAVE SYNTHESIZING CIRCUIT

include synchronizing circuitry to synchronize interconnected inverters and/or synchronize the signal producer to a possible pulse-duration modulator. In response to an input control signal the counter-decoder can provide outputs for the desired output frequencies. Outputs of the counter-decoder are fed to the digital-to-analog converters to control the instantaneous relative amplitudes of synthesized sine-waves and other outputs are fed to the polarity control circuits to control the polarities of the signals. Following the recommendations of paragraph 2.1.3.8, the synthesized sine-waves are then pulse-duration modulated and provided to the inverter power stage.

2.1.6.5 Signal Coupling to Power Inverter Stage. The PDM wave train can be coupled to the power inverter stage in several ways:

1. Direct coupling of logic voltages
2. Optical coupling
3. Transformer coupling
4. Transformer coupling of modulated RF.

The direct coupling of logic voltages is almost impossible in view of the necessary isolation of the various sections of the power inverter stage. Optical coupling is nearly ideal at low frequencies, but is subject to false outputs at high frequencies due to the rapid changes in level encountered. Transformer coupling is difficult because of the need to couple signals approaching dc. If the PDM control signal is used to modulate an RF signal, though, small reliable transformers can be used, providing signal coupling and isolation. The advantages of this method appear to outweigh the disadvantages of the need to control resulting EMI.

2.1.7. Frequency and Voltage Selection and Parallel Operation. With the signal generator discussed in paragraph 2.1.6.4, output frequency is selected by supplying the appropriate control signal to the divider as shown in Figure 2-5. Output voltage selection is performed by proper interconnection of inverter power stage sections as discussed in paragraph 2.1.4.

In order to allow inverters to be paralled, the inverters must run at the same frequency and in phase. Additional control circuitry is therefore required to insure that the proper relationships are maintained during operation and to prevent units which are not in phase from being paralleled. Additionally, some method must be provided to insure equal load sharing among the paralleled inverters.

The frequency requirement can be realized by supplying a synchronizing signal between units which establishes the overall frequency and waveform of the output. A second synchronizing pulse might be supplied whenever the reference phase goes through zero degrees or some other point. For convenience one inverter may automatically act as "master" to which all other units are slaved. One method is to synchronize each unit's phase to that of the unit which provides the first synchronizing pulse to a common synchronizing line.

Load sharing between parallel inverters may be insured by external balance transformers or current monitors which control the output of each unit to assure proper load sharing. Interconnections between load-sharing units may be minimized if each unit incorporates circuitry which adjusts the output voltage downward slightly as the current increases. Proper design would cause load sharing while keeping the output voltage within specification.

2.1.8 Protection Circuitry. In addition to the frequency, amplitude, and paralleling control circuitry, the inverters will generally need further control and protection circuitry to perform the following functions:

1. System start-up and shut down control
2. Fault protection

2.1.8.1 Start-up and Shut Down. Stresses during start-up can be minimized by controlling the sequence of events as the unit begins to operate. For example, initially the input filter capacitors appear as a short across the input power source resulting in a large inrush current. This inrush can be limited by a series impedance which is later shunted by a short circuit to prevent power dissipation. Actual inverter operation may be prevented during initial charging. Shut-down protection might include circuitry to remove the loading prior to input power removal, and provision for discharge of capacitors.

2.1.8.2 Fault Protection. The specification of this study require design provision for protection against input polarity reversal, high or low input voltage, overload or short circuit output, and excessive temperature.

2.1.9 Trade-off Summary. Figure 2-6 and Table 2-2 summarize the advantages and disadvantages of the various inverter designs considered. Based upon the trade-offs depicted, considering cost, size and weight, efficiency, signal quality (distortion) and reliability, maintainability, and availability, the configuration in Figure 2-7 is recommended.

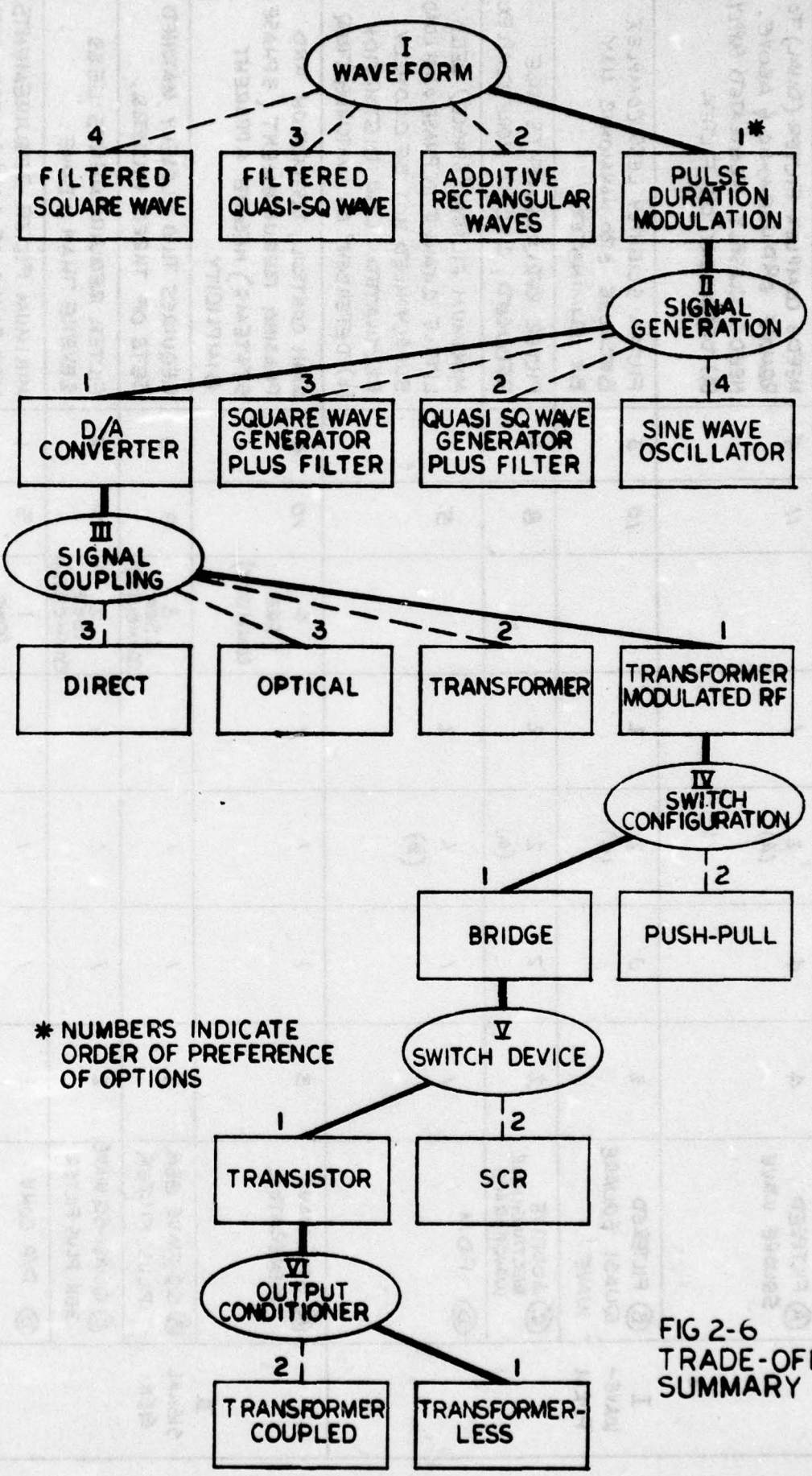



FIG 2-6
TRADE-OFF
SUMMARY

| | | CRITERIA (NUMBERS INDICATE ORDER OF PREF) | | | | | | ORDER OF PREF | |
|---|---|---|---|---|---|---|---|---|---|
| FEATURE | OPTION | COST | SIZE/WT | EFFICIENCY | RELIAB. | OTHER | TOTAL* | | COMMENTS |
| I WAVE-FORM | (A) FILTERED SQUARE WAVE | 4 | 4 | 2 (a) | 1 | | 11 | 4 | NEEDS COMPLEX FILTER (DUAL) TO REMOVE 3RD HARMONIC & ABOVE. NEEDS CLOSELY REGULATED SUPPLY. (a) DEPENDENT ON FILTER |
| | (B) FILTERED QUASI SQUARE WAVE | 3 | 3 | 2 (a) | 2 | | 10 | 3 | FILTER SLIGHTLY LESS COMPLEX BECAUSE 3RD HARMONIC MAY BE ELIMINATED. |
| | (C) ADDITIVE RECTANGULAR WAVEFORMS | 2 | 2 | 2 (a) | 2 | | 8 | 2 | FILTER REQUIREMENTS ARE REDUCED, CIRCUIT MORE COMPLEX. |
| | (D) PDM | 1 | 1 | 1 (b) | 2 | | 5 | 1 | MINIMUM FILTER (SINGLE) REQD. LITTLE CHANGE IN PHASE WITH LOAD SUPPLY NEED NOT BE CLOSELY REGULATED. LOW DISTORTION (b) DEPENDENT ON SWITCHING FREQ |
| II SIGNAL GEN | (A) SINE WAVE GENERATOR | 5 | 1 | 1 | 1 | 4 (SEE COMMENTS) | 10 | 4 | GAIN CONTROL, DISTORTION AND PHASING REQUIREMENT (3 PHASE SYSTEMS) NEGATE APPARENT SIMPLICITY. |
| | (B) SQ WAVE GEN PLUS FILTER | 3 | 1 | 1 | 1 | 3 (SEE COMMENTS) | 9 | 3 | REQUIRES TWO CLOSELY MATCHED SETS OF THREE FILTERS. |
| | (C) QUASI-SQ WAVE GEN PLUS FILTER | 2 | 1 | 1 | 1 | 2 (SEE COMMENTS) | 7 | 2 | FILTER REQUIREMENTS LESS SEVERE THAN ABOVE. |
| | (D) D/A CONV | 1 | 1 | 1 | 1 | 1 (SEE COMMENTS) | 5 | 1 | MINIMUM FILTER REQUIREMENTS. WIDE RANGE OF GAIN CONTROL WITH LOW DISTORTION. |

* SMALLEST TOTAL PREFERRED

TABLE 2-2, TRADE-OFF SUMMARY

| FEATURE | OPTION | CRITERIA (NUMBERS INDICATE ORDER OF PREF) COST | SIZE/WT | EFFICIENCY | RELIAB. | OTHER | TOTAL* | ORDER OF PREF | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|
| III SIGNAL COUPLING | (A) DIRECT COUPLING | 1 | 1 | 3 | 1 | 4 (SEE COMMENTS) | 10 | 3 | NOT PRACTICAL FOR USE WITH TRANSFORMERLESS OUTPUT CONDITIONER |
| | (B) OPTICAL COUPLING | 2 | 1 | 2 | 2 | 3 (SEE COMMENTS) | 10 | 3 | AVAILABLE COUPLERS APPEAR INADEQUATE AND/OR EXPENSIVE FOR APPLICATION |
| | (C) TRANSFORMER COUPLING | 1 | 2 | 1 | 3 | 2 (SEE COMMENTS) | 9 | 2 | TRANSFORMER REQUIRED TO COUPLE LOW FREQUENCY COMPONENTS |
| | (D) TRANSFORMER COUPLED / MODULATED RF | 1 | 1 | 1 | 1 | 1 (SEE COMMENTS) | 5 | 1 | REQUIRES CARE TO PREVENT EMI |
| IV SWITCH CONFIG | (A) PUSH-PULL | 1 (SEE COMMENTS) | 1 (SEE COMMENTS) | 1 | 1 (SEE COMMENTS) | 2 | 6 | 2 | NEED FOR OUTPUT TRANSFORMER NEGATES INDICATED ADVANTAGE |
| | (B) BRIDGE | 2 | 2 | 1 | 2 | 1 (SEE COMMENTS) | 8 | 1 | PERMITS HIGHER VOLTAGE OPERATION OFFSETTING LOSSES OF ADDED SWITCHES. SIMPLIFIES ENERGY RECOVERY. NO OUTPUT TRANSFORMER REQUIRED. |
| V SWITCH DEVICE | (A) SCR | 1 | 1 | 2 | 2 | 2 | 8 | 2 | |
| | (B) TRANSISTOR | 1 | 1 | 1 | 1 | 1 | 5 | 1 | PARALLEL TRANSISTOR ARRAYS GIVE EVEN BETTER RELIABILITY IF REDUNDANT TRANSISTORS ADDED |
| VI OUTPUT COND-ITIONER | (A) TRANSFORMER | 2 | 2 | 2 | 2 | | 8 | 2 | |
| | (B) TRANSFORMER-LESS | 1 | 1 | 1 | 1 | | 4 | 1 | |

TABLE 2-2, TRADE-OFF SUMMARY (CONT'D)

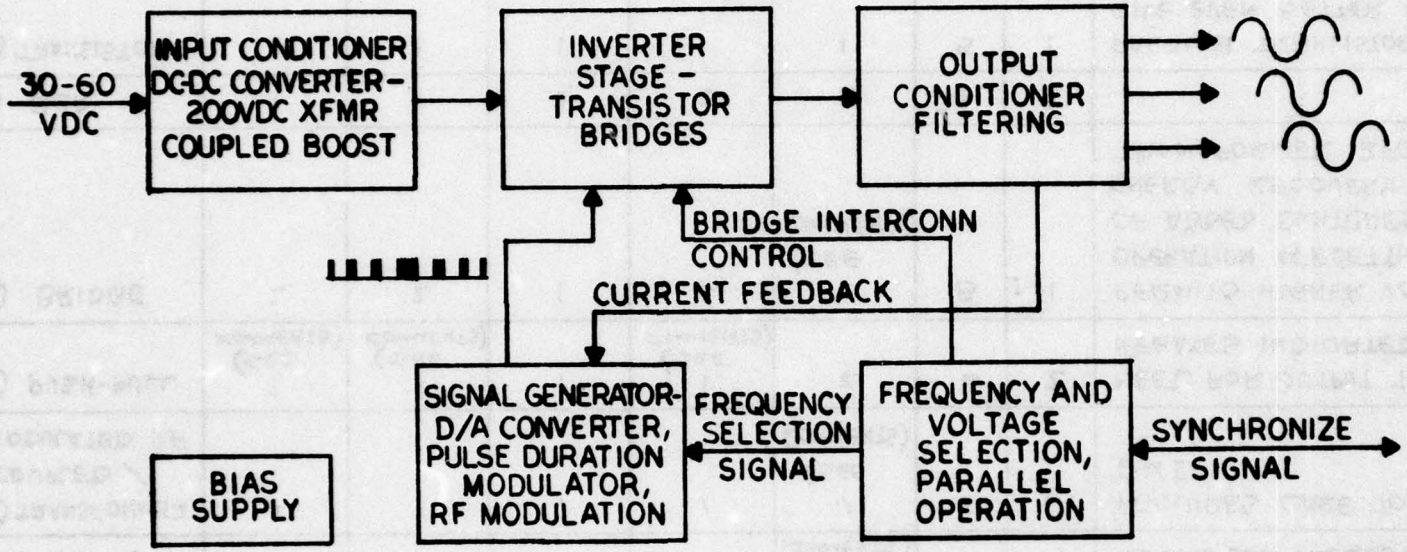



FIG 2-7, SIMPLIFIED BLOCK DIAGRAM

## 2.2 DETAIL DESIGN.

**2.2.1 Assumptions.** The detailed design presented here is based upon the design recommendations resulting from the initial trade-off study described in Section 2.1. Figure 2-7 presents a simplified block diagram of the recommended design. The detailed design of an inverter of this type is discussed below. The circuits shown are generally applicable to any of the family of inverters. The number of bridge stages per sector will be dependent upon the power requirements, and the 1.5 kW unit will not need the three-phase capability.

**2.2.2 Input Conditioner.** The input circuit has three primary functional circuits and can be envisioned as in Figure 2-8.

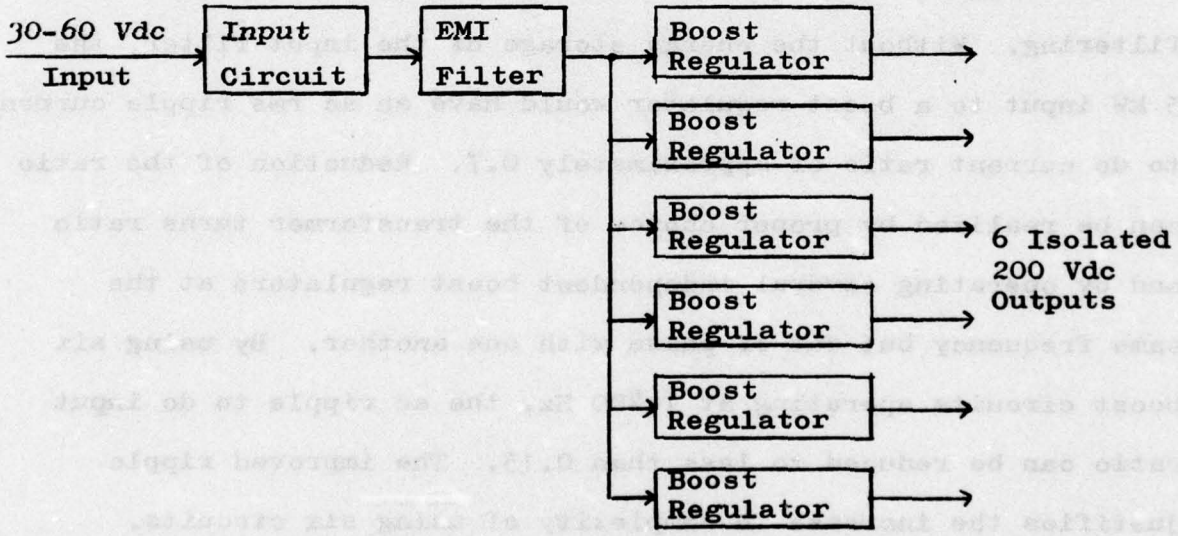



Figure 2-8. Input Circuit Functional Drawing

2.2.2.1 Input Circuit. The input circuit, shown in Figure 2-9 provides most of the input protection circuitry. CB1 is the main circuit breaker for the inverter and provides over-current protection for the inverter. Since CB1 is essentially a slow device, however, other forms of protection are incorporated elsewhere in the inverter. CB1 in connection with CR1 also provides protection against reverse input polarity. CB1 in conjunction with Q1 provides protection against excessive input voltage as determined by R1, R2, C2, and CR2.

Inrush current to filter capacitors C3 and C4 is limited at turn-on by R4. As the capacitors charge, the voltage across R4 approaches zero allowing Q2 to turn on and operate relay K1 thereby shorting out the dissipative R4. R8 provides a signal to permit operation of the signal generator (paragraph 2.2.8).

2.2.2.2 EMI Filter. C1, C3, C4, L1 and L2 provide conducted EMI filtering. Without the energy storage of the input filter, the 5 kW input to a boost regulator would have an ac rms ripple current to dc current ratio of approximately 0.7. Reduction of the ratio can be realized by proper choice of the transformer turns ratio and by operating several independent boost regulators at the same frequency but out of phase with one another. By using six boost circuits operating at 14400 Hz, the ac ripple to dc input ratio can be reduced to less than 0.15. The improved ripple justifies the increase in complexity of using six circuits.

2.2.2.3 Boost Regulator. Figure 2-10 is a simplified schematic

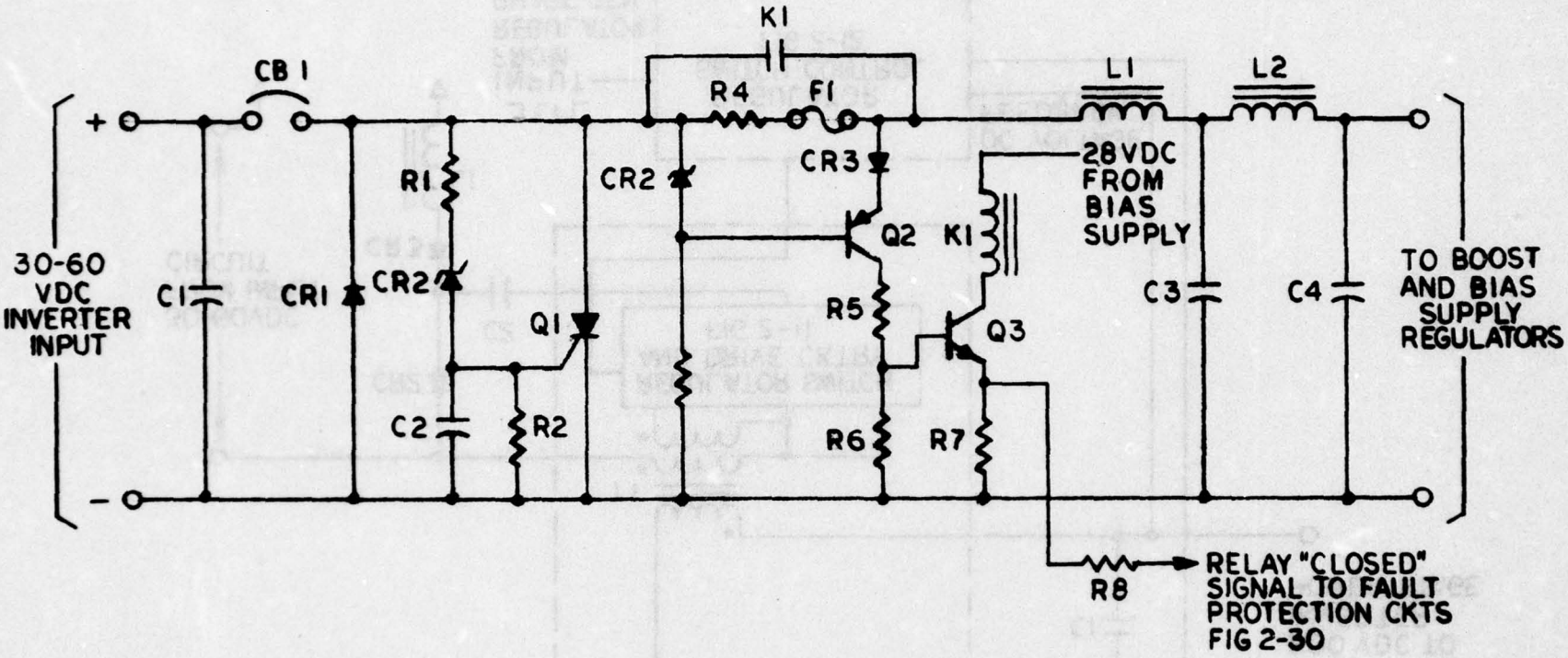



FIG 2-9, INPUT CIRCUIT

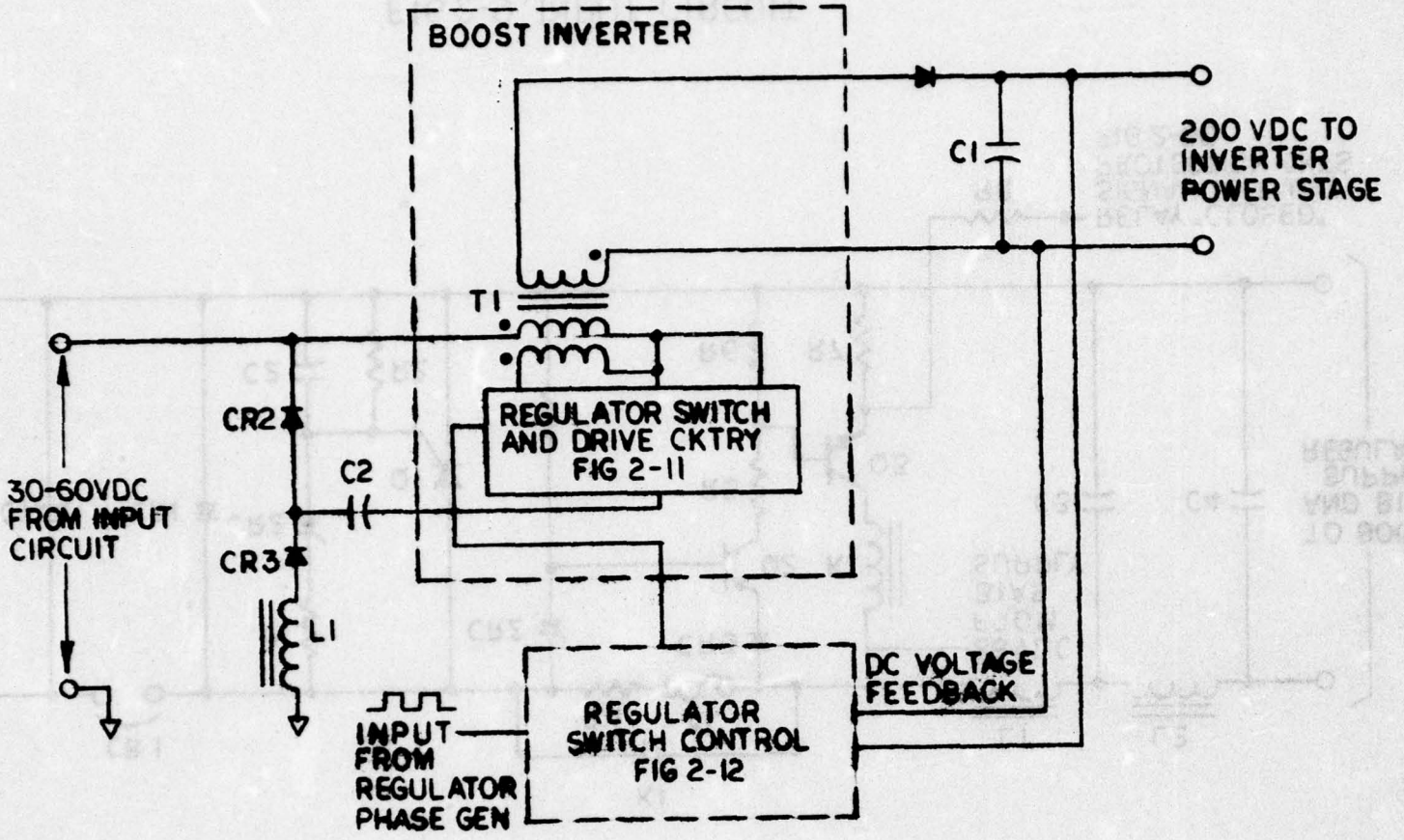



FIG 2-10, BOOST REGULATOR

of one transformer-coupled boost regulator. $T_1$ is the regulator transformer, $CR_1$ is the output dc rectifier, and $C_1$ is an output filter capacitor. The regulator switch and drive circuits are shown in Figure 2-11.

CR2, CR3, $L_1$ and C2 provide energy recovery. They protect the switch by returning to the storage portion of the input circuit that energy which is stored in the transformer leakage inductance at the moment the switch is turned off. Alternatively the energy might have been dissipated by a resistive network with consequent decrease in overall efficiency. Without some form of protection, however, the energy could destroy the switch.

2.2.2.3.1 Regulator Switch and Drive Circuitry. The switch actually consists of fifteen parallel transistors and associated drive circuitry. Figure 2-11 is a schematic drawing of the circuitry. Under overload conditions, each switch (15 parallel transistors) is required to conduct nearly 75 amps and thus requires a peak base drive current of 7.5 amps. The circuitry shown provides the necessary drive and two forms of overcurrent protection are also provided.

During normal operation, the current supplied by the regulator switch control (see section 2.2.2.3.2) turns on transistor $Q_1$. $Q_1$ in turn causes Q2, Q4, and Q5 to conduct. Q5 supplies the base current to the switching transistors. The circuit is arranged, however, so that Q2 is able to conduct for a limited period unless the output switch transistors are driven nearly to saturation. Normally these transistors are quickly driven to saturation and diode $CR_{14}$ then causes Q3 to conduct. With Q3 conducting, Q2

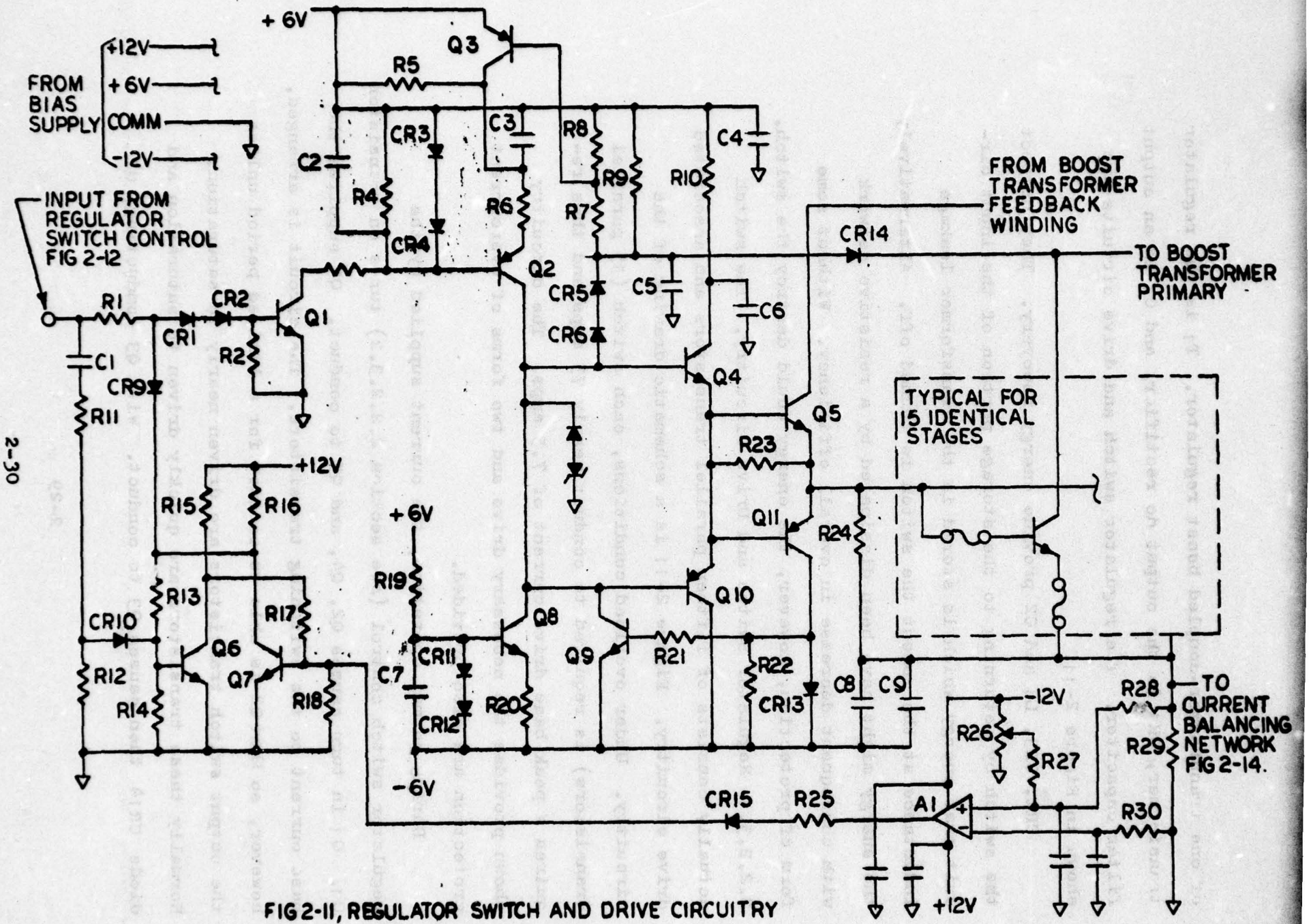



FIG 2-11, REGULATOR SWITCH AND DRIVE CIRCUITRY

may conduct indefinitely and the circuit will function normally; however, should the switch transistors fail to reach saturation soon enough, C3 will charge and Q2 then turns off. Thus, the time required for C3 to charge imposes an upper limit on the length of time during which the switching transistors may conduct without reaching saturation, thereby protecting the transistors from continuous operation in a high dissipation state. With Q2 off, Q8 conducts sufficiently to turn on Q10 and Q11 thereby reverse biasing the base circuit of the switch transistors. Q9 is provided to aid in pulling down the base circuit when large reverse currents flow by making the circuit regenerative. When Q11 conducts, a voltage is developed across CR13 and R22 which tends to turn on Q9. Q9, in turn, increases the conduction through Q10 causing Q11 to turn on even harder.

Q6 and Q7 form a flip-flop which is reset at the start of each input current pulse from the logic circuit. If an overcurrent condition exists the voltage developed across shunt resistor R29 by the load current will be sufficient to overcome the bias voltage applied to the input of comparator A1 by R26 and R27. The comparator output then swings positive and the flip-flop is triggered to the set condition. All of the input current pulse then flows though transistor Q7 and Q2 is turned off. The switch transistors then turn off until the next cycle at which time the process repeats. Normal operation will resume if the overcurrent condition has been corrected.

2.2.2.3.2 Regulator Switch Control. The switch control circuitry

is shown in Figure 2-12. The primary inputs to this circuit are

1. A 14,400 Hz square wave from circuitry which controls the relative phases of the boost regulators.
2. A dc signal from current balance circuitry.
3. A dc voltage feed back from the regulator output.

The output from the circuit is a train of pulse-width modulated current pulses which control the regulator switch.

Resistor R1, capacitor C2 and operational amplifier A1 form an integrator circuit used to transform the squarewave input signal applied to capacitor C1 into the triangular wave form required by the modulator circuit, comparator amplifier A2. Capacitor C1 blocks the dc component of the square wave, and resistor R2 serves to stabilize the output wave form about a zero volt (dc) reference point.

The dc output voltage from the regulator is fed back to the series string consisting of R7, CR1 and U1 . U1 is an optical coupler providing an output current from the coupler which is proportional to the input current while simultaneously maintaining the electrical isolation of the input and output circuits. The input current to the coupler is a function of the output voltage, the zener voltage of CR1 and R7. By making the zener voltage nearly equal to the regulated output voltage, R7 may be made small. A relatively large change in coupler current then results from a small change in the regulated output voltage.

The output current from the coupler is applied to error

amplifier A3. The output of A3 is applied to the inverting input of comparator A2. The comparator output swings negative whenever the output of A3 is more positive than the instantaneous value of the triangular waveform from A1. Under these conditions, Q1 is turned on, and a current pulse is supplied to the switch driver until the triangular waveform again exceeds the output of A3. The more negative is the output of A3, the shorter will be the current pulse produced by Q1. This is the required action for control since the output of A3 goes more negative in response to a high DC voltage at the regulator output terminals, and shortening the current pulse tends to reduce the output voltage. The opposite is also true; a low output voltage tends to result in the generation of a longer current pulse. Zener diode CR2, together with resistors R12, R13, and R14 provide a current at the input of A3 to off-set the coupler output current as required to adjust the regulator output voltage to the desired value of 200 volts. In addition to the above, A3 is also supplied with a current through R9 which flows in response to the voltage developed at the output of the current balance network (2-14). This additional current serves to increase or decrease the output voltage as required to achieve a balanced condition in which the load current is equally shared among two or more regulators.

The reference square wave is also applied to amplifier Q2. The output of Q2 is differentiated by C16 and R17 to form a narrow pulse used to turnoff Q3 at the peak of each cycle of the triangle generated by A1. When Q3 is turned off, the output of

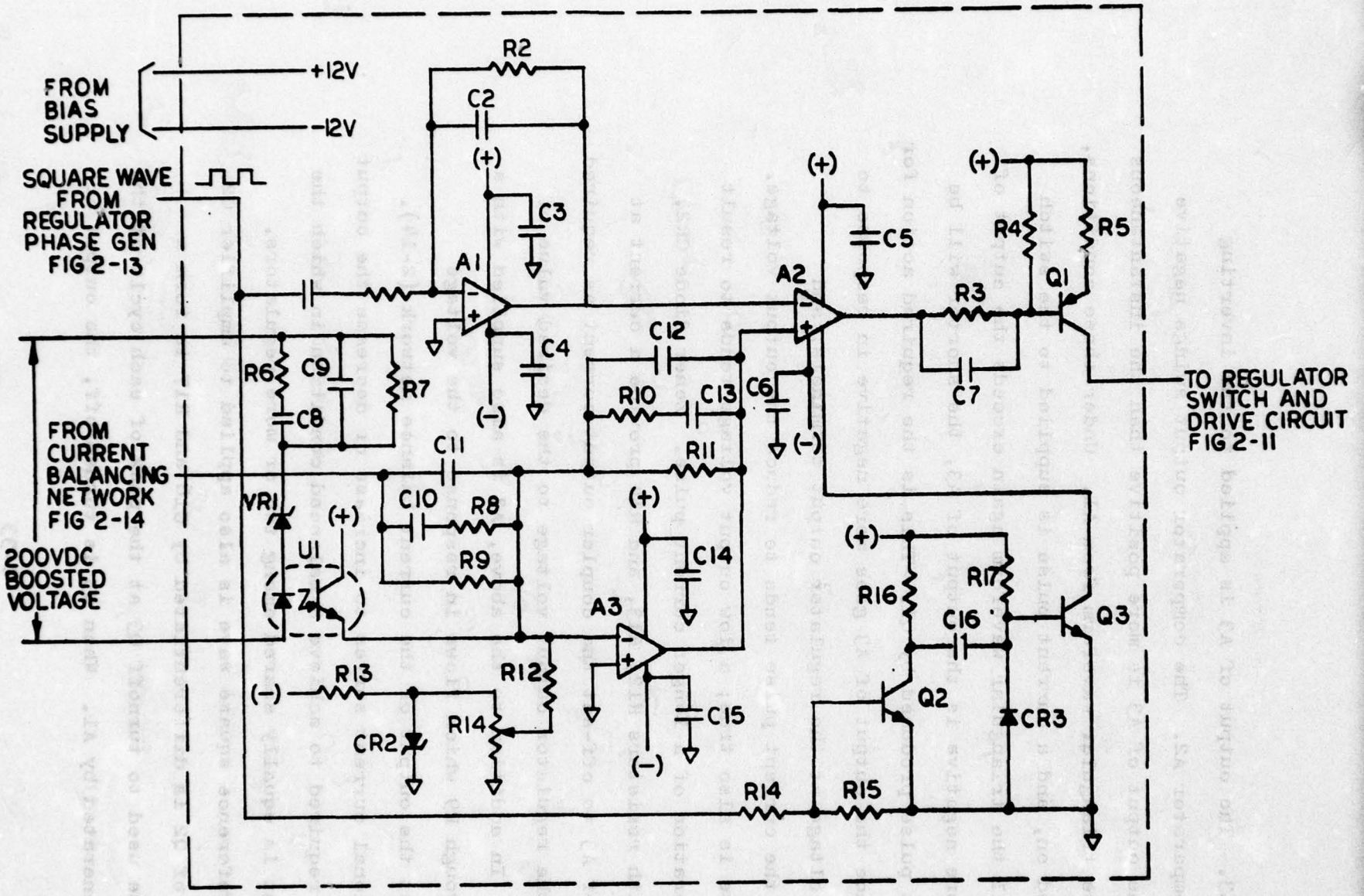


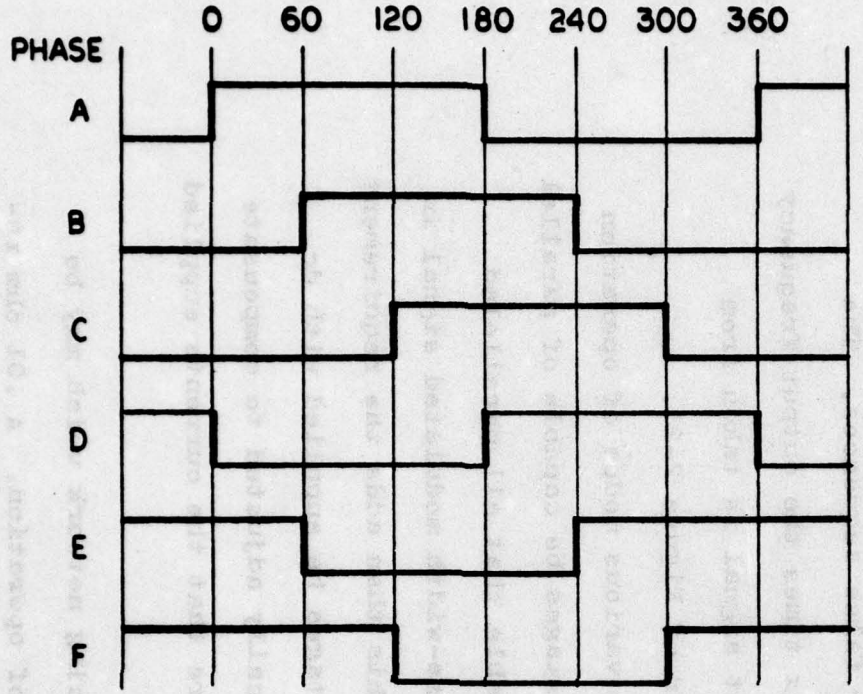

FIG 2-12, REGULATOR SWITCH CONTROL

A2 is forced high to interupt the output current pulse which could otherwise flow continuously during severe undervoltage conditions. This periodic interuption is essential if saturation of the transformer is to be avoided.

2.2.2.3.3 Regulator Phase Generator. The six phase square wave generator required by the boost regulator circuit is shown in Figure 2-13. The circuit consists of three D-type flip-flops interconnected to form a Johnson counter. Two NOR gates are included to clear the counter of any false sequences. The input frequency to the counter is six times the output frequency of 14,400 Hz: 86,400 Hz. The input signal is taken from counter U-1 of the oscillator/divider of Figure 2-21.

2.2.2.3.4 Output Load Sharing. The various modes of operation of the unit require that the output stages be capable of parallel operation. In so doing, it is desirable that all paralleled stages be supplied with the same pulse-width modulated signal in generating the sine wave, however, this then adds the requirement that each of the paralleled output stages be supplied with dc input voltages which may be automatically adjusted to compensate for minor circuit difference to insure that the currents supplied to the output stages are equal.

Figure 2-14 is a current balancing network which may be connected as required for each mode of operation. A .01 ohm resistor is placed in series with each of the boost regulator switching stages. The current through the resistor results in a small, pulsed voltage which is amplified and filtered by amplifier A1. The output of A1 is a positive dc voltage



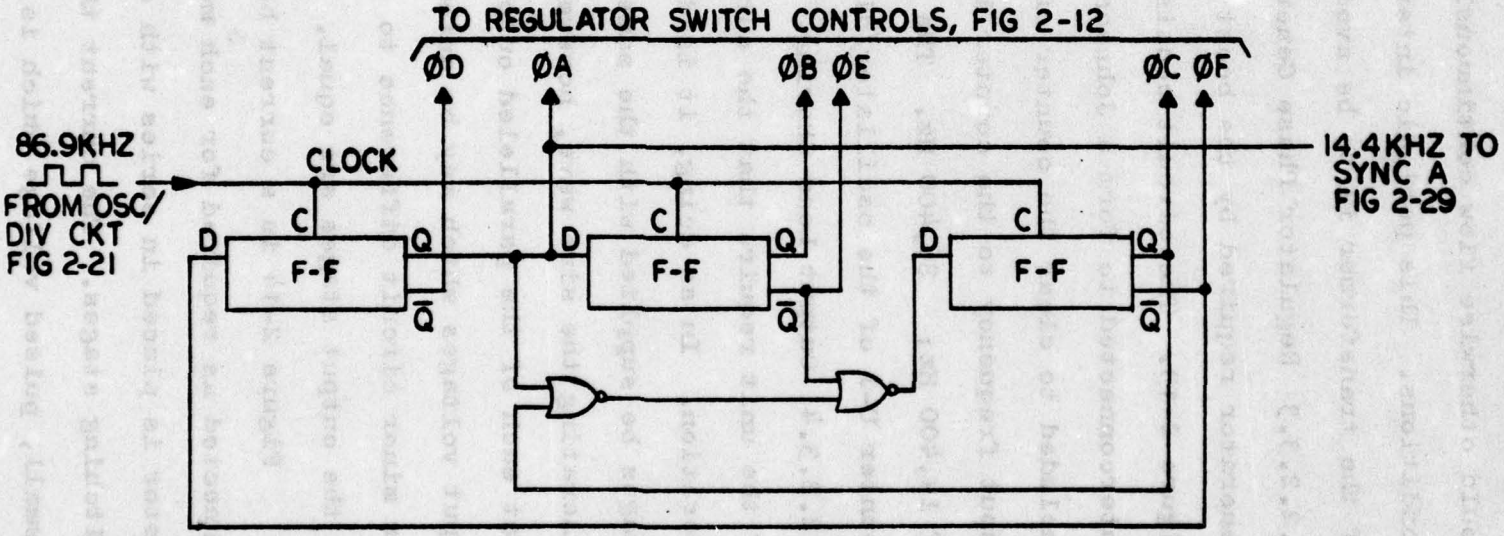




FIG 2-13, REGULATOR PHASE GENERATOR

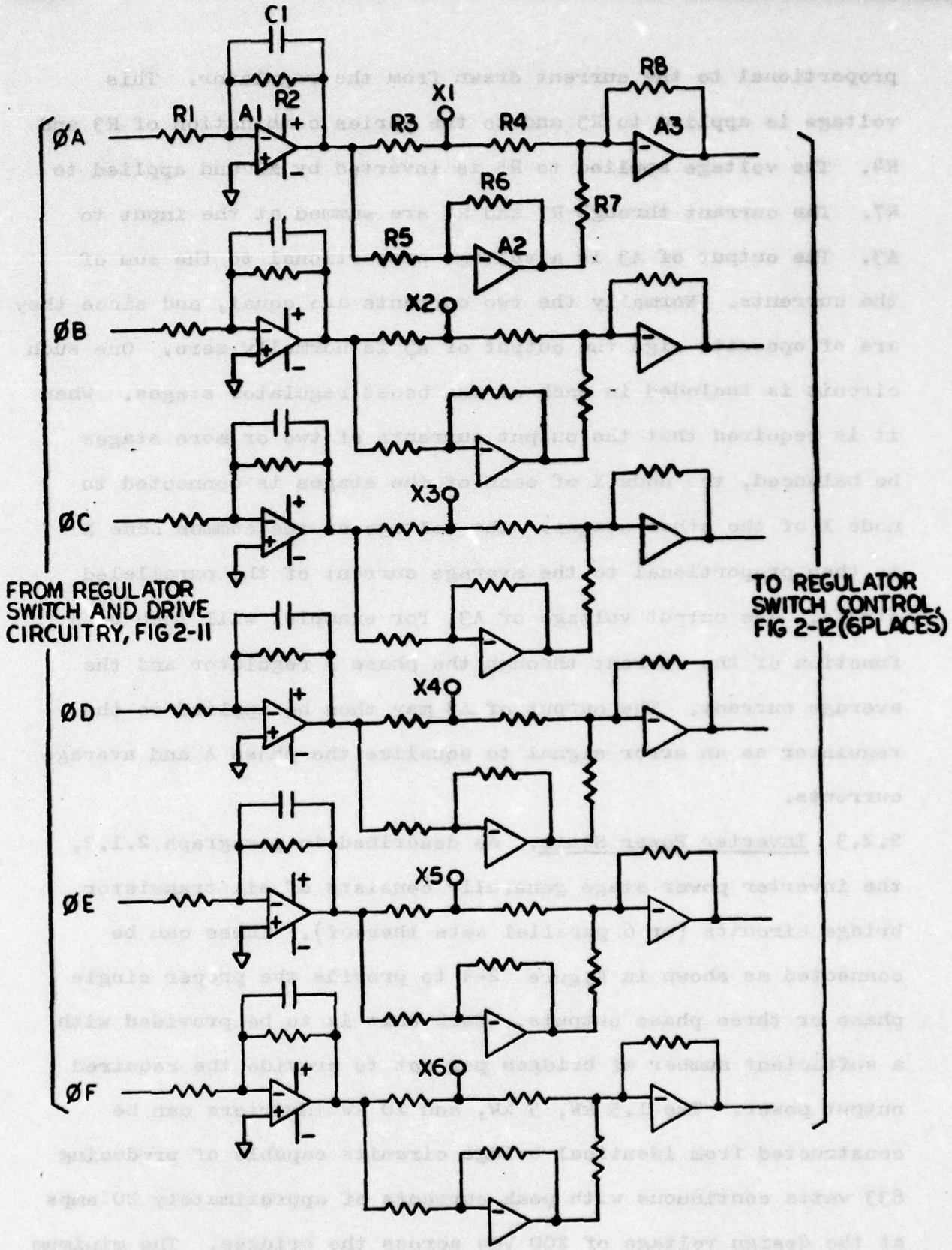



FIG 2-14, CURRENT BALANCING NETWORK

proportional to the current drawn from the regulator. This voltage is applied to R5 and to the series combination of R3 and R4. The voltage applied to R5 is inverted by A2 and applied to R7. The current through R7 and R4 are summed at the input to A3. The output of A3 is a voltage proportional to the sum of the currents. Normally the two currents are equal, and since they are of opposite sign the output of A3 is normally zero. One such circuit is included in each of the boost regulator stages. When it is required that the output currents of two or more stages be balanced, the node X of each of the stages is connected to node X of the other stages. The voltage at the common node X is then proportional to the average current of the paralleled stages. The output voltage of A3, for example, will then be a function of the current through the phase A regulator and the average current. The output of A3 may then be applied to the regulator as an error signal to equalize the phase A and average currents.

2.2.3 Inverter Power Stage. As described in paragraph 2.1.3, the inverter power stage generally consists of six transistor bridge circuits (or 6 parallel sets thereof). These can be connected as shown in Figure 2-4 to provide the proper single phase or three phase outputs. Each unit is to be provided with a sufficient number of bridges per set to provide the required output power. The 1.5 kW, 5 kW, and 10 kW inverters can be constructed from identical bridge circuits capable of producing 833 watts continuous with peak currents of approximately 20 amps at the design voltage of 200 Vdc across the bridges. The minimum

supply voltage to an ideal bridge would be 120 Vdc x 1.414 = 169.7. If the bridge is 95% efficient the requirement increases to 169.7/.95 or 178.6. Thus the 200 Vdc design voltage is adequate.

Figure 2-15 shows a single bridge circuit and Figure 2-16 shows the associated drive circuitry. Each output stage sub-section consists of four groups of high-power switching transistors arranged in a bridge configuration. Each group consists of four power transistors for a total of 16 power transistors per output sub-section. Fuses are provided in the base and emitter lead of each transistor for protection and to remove faulty transistors from the circuit automatically. The slight resistance of the fuses also tends to equalize the current among the transistors.

Each group of power transistors is driven by an independent drive circuit shown in Figure 2-16. The circuit performs two important functions in addition to turning the switch on and off. The circuit also introduces the delay necessary to prevent simultaneous conduction of pairs switches which could short the supply voltage, and the circuit also provides short circuit protection of the power transistors.

Modulated square wave signals from the signal generator via the signal coupling circuit of Figure 2-27 are alternately applied to transformers T1 and T2 to turn the output switch on and off as required. Application of the control signal to T1 results in a positive voltage at the emitter of Q1. This voltage also reverse biases the emitter of Q2 by an amount determined by R1 and

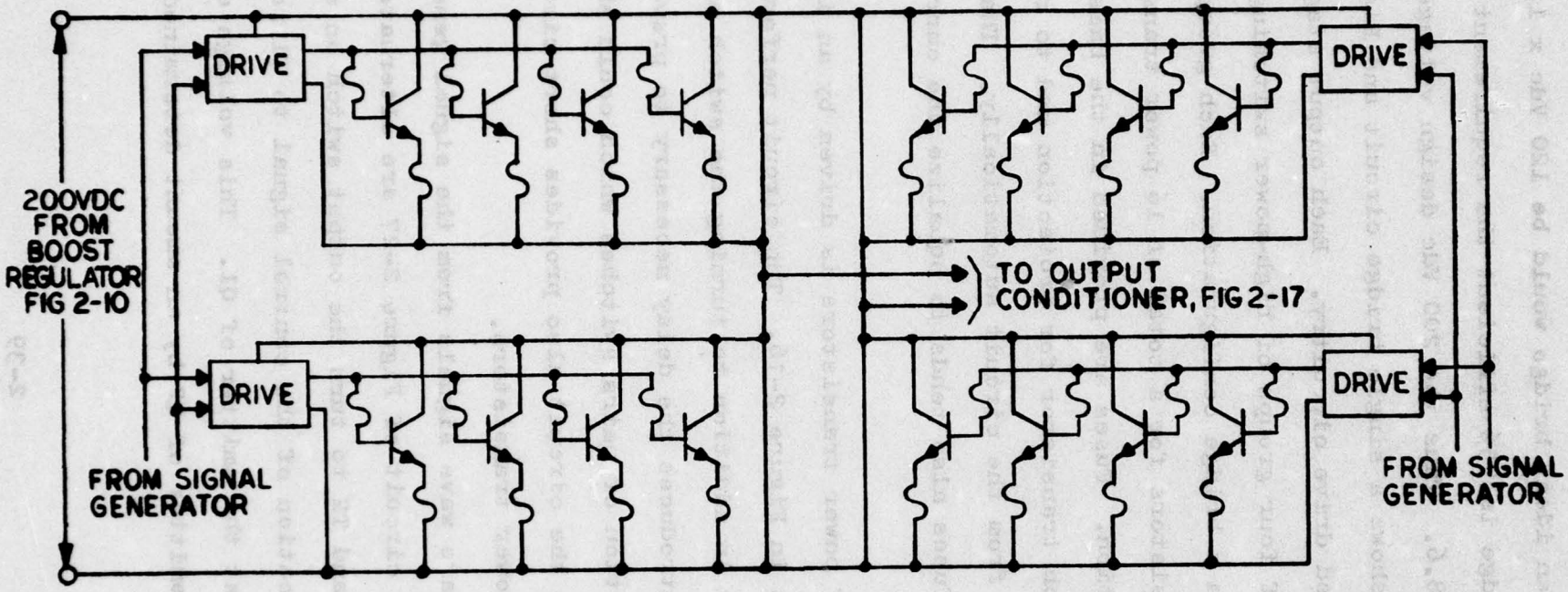



FIG 2-15, INVERTER POWER STAGE

R3 while simultaneously charging C2 through R4. When the voltage on C2 is sufficient to overcome the voltage on R3, Q2 conducts and turns on Q1. Q1 drives amplifier Q4 through diode CR6. Q4, in turn, drives the output switch transistors. The delay introduced by the charging of C2 prevents simultaneous conduction of upper and lower legs of the bridge which are directly connected in series across the power supply.

Diode CR5 is added into the circuit to prevent saturation of the output switching transistors by diverting a part of the drive current to Q4 once the collector voltage of the output switches drops to the desired level. In the event that the switch transistors are severely overloaded, the collector voltage of the switch transistors will remain at some relatively high value. C3 will then charge through R5 and cause Q3 to turn on after a predetermined interval. Q3 in turn shuts off Q2, Q1 and Q4, thereby removing the drive current from the power transistors.

In normal operation, the power transistors are turned off by applying the squarewave signal to transformer T2 and removing it from transformer T1. When the signal is applied to T2, the emitter of Q5 goes negative causing Q5 to turn on. When Q5 turns on, the bases of both Q4 and the power transistors are reverse biased, thereby rapidily switching off the output transistors.

2.2.4 Output Conditioner. The output conditioner consists of a filter for each bridge circuit to remove unwanted components

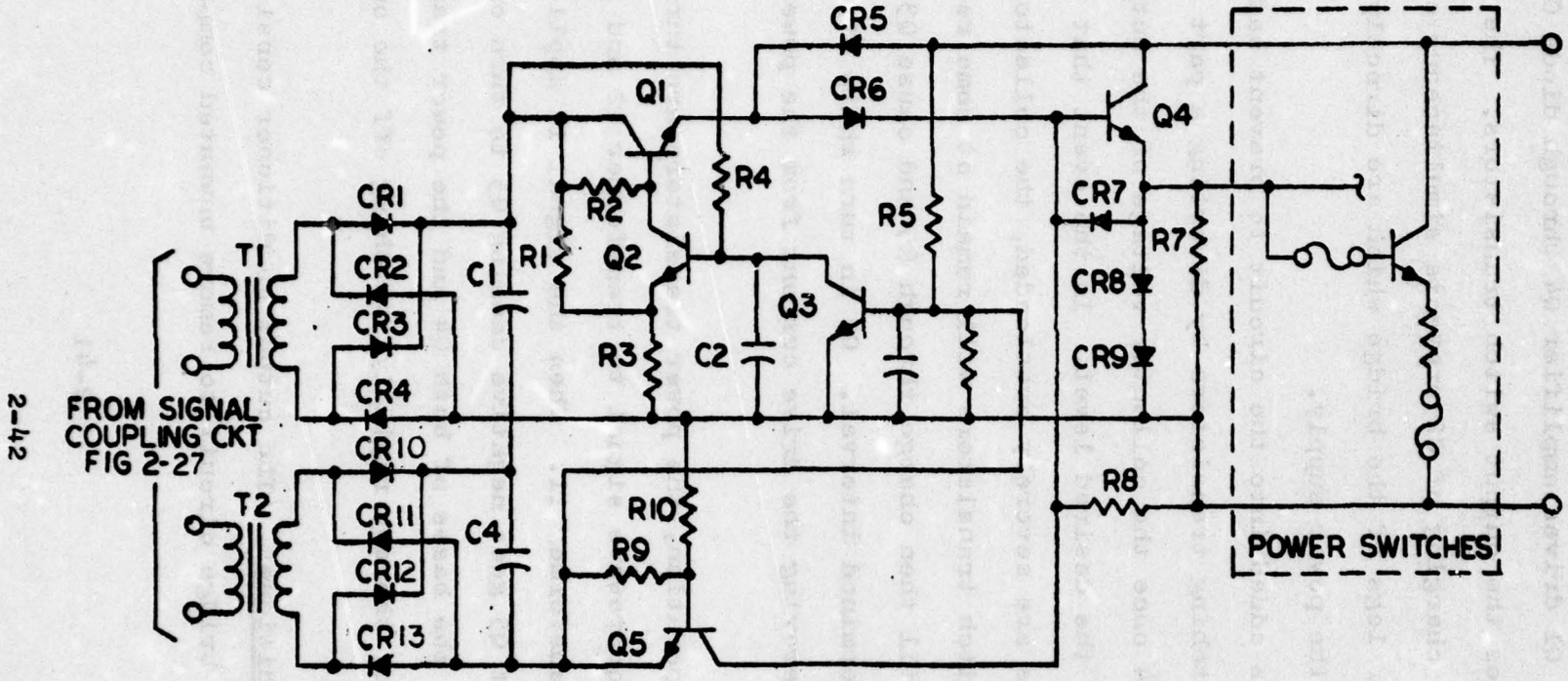



FIG 2-16, INVERTER POWER STAGE DRIVE

of the switching frequency from the output signal. It is designed to provide minimum attenuation and phase shift of the output frequency. The filter design is shown in Figure 2-17. The relatively simple design of the filter is made possible by the high switching frequency employed in the output stages. Transients caused by load application or removal are minimal since very little inductance is required in the filter.

2.2.5 Bias Supply. The various internal operating voltages needed by the unit are provided by including a separate regulator and bias supply for this purpose. The regulator-bias supply is capable of providing an output of approximately 350 watts and may therefore be used as part of any inverter in the family. The supply consists primarily of a boost-type converter, an inverter, and an output transformer tapped to provide (often isolated) voltages.

2.2.5.1 Bias Supply Boost Converter. The regulator is a boost type dc-dc converter. A schematic diagram is shown in Figure 2-18, 2-19. The maximum input current to the regulator is 13 amperes at 30 volts. The output of the regulator is 133 volts. This voltage is selected to permit the ready development of a square wave having a peak amplitude of 133 volts. The fundamental frequency of the square wave then has a peak amplitude equal to $133 \times 4/\pi = 169$ volts. The rms value of the fundamental is then 120 volts.

In Figure 2-18 Q1, Q2, and CR-1 form a combined input voltage detector and low voltage regulator. If the input voltage is applied to the unit slowly, rather than abruptly,

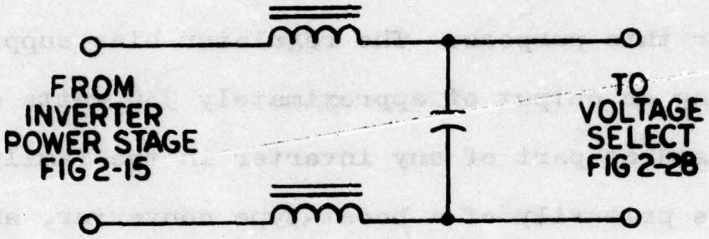



FIG 2-17, OUTPUT CONDITIONER

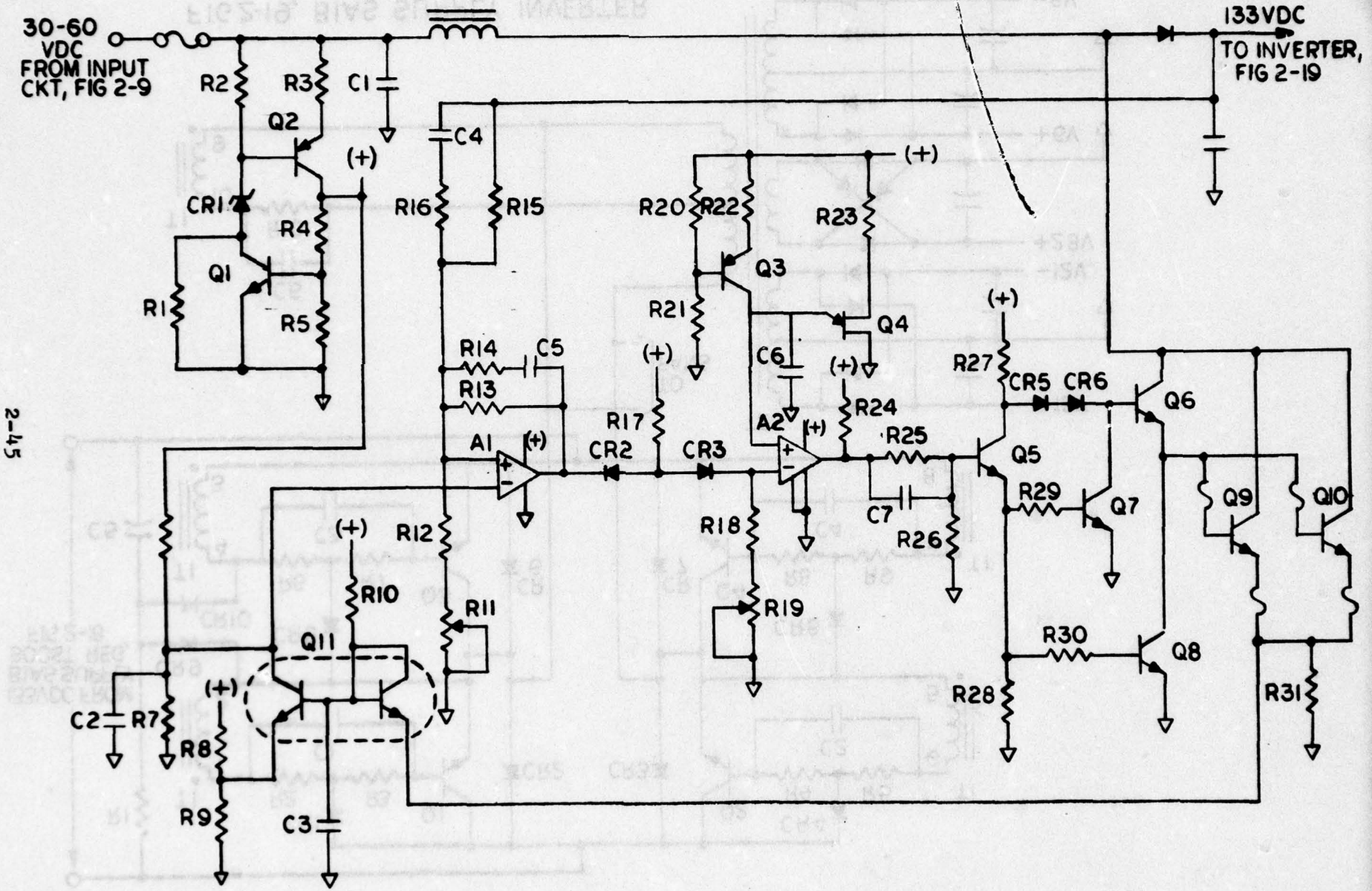



FIG 2-18, BIAS SUPPLY BOOST REGULATOR

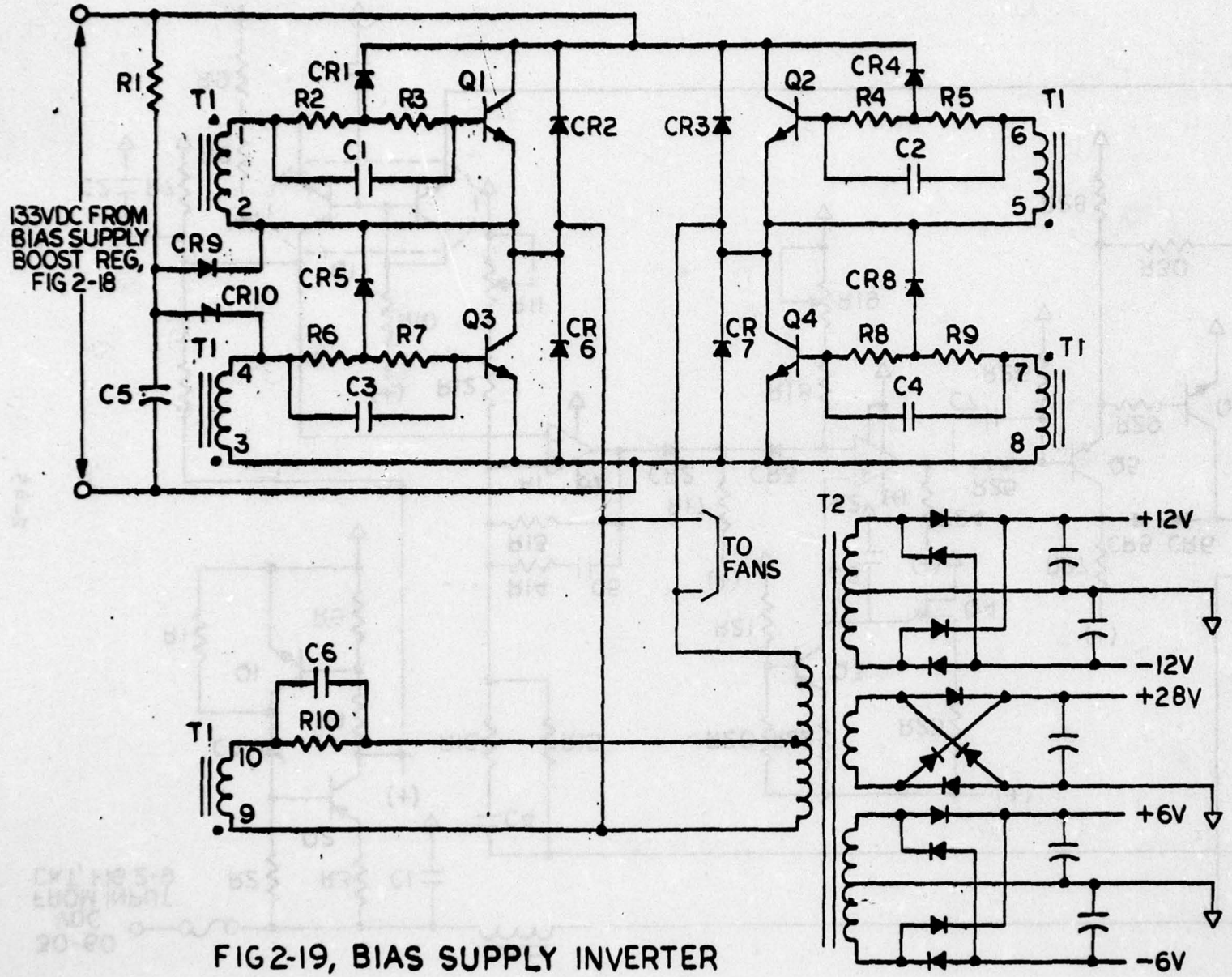



FIG 2-19, BIAS SUPPLY INVERTER

large input currents may be taken by the regulator until the normal operating voltage is reached and the circuit begins to operate normally. To preclude this situation, CR1 is included to prevent the inverter from turning on until the input voltage exceeds the zener voltage of CR1. When CR1 conducts, transistor Q2 turns on causing Q1 to conduct also. The anode of the zener diode is then essentially at zero volts. The base of Q2 is therefore above zero by an amount equal to the zener voltage. Sufficient base current is drawn from Q2 to insure saturation of Q2. The collector of Q2 is then very nearly at the same voltage as the zener diode cathode. The collector of Q2 therefore acts as a source of regulated voltage to the remainder of the control circuitry in the bias supply regulator.

The waveform at the emitter of unijunction transistor oscillator Q4 is a sawtooth waveform of approximately 20 kHz. Q3 is connected so as to supply a constant current to capacitor C6 and improve the linearity of the sawtooth waveform. The sawtooth signal is applied to comparator amplifier A2 and is used to determine the pulse width of the switching signal applied to parallel switching transistors Q9 and Q10.

The output of the regulator is applied to error amplifier A1, through resistor R15. R11 provides a means of adjusting the output voltage. The output of the error amplifier is applied to the comparator input by means of diodes CR2 and CR3, together with resistors R17, R18, and R19. This network limits the positive peak excursion of the voltage applied to A2 and

is necessary to establish a minimum value of $t_{off}$.

The output of A2 drives transistor Q5. When off, the collector circuit of Q5 turns on transistors Q6, Q9, and Q10. Q9 and Q10 are a parallel pair and form the regulator switch. Transistors Q7 and Q8 turn on out of phase with Q6, Q9, and Q10 and serve to speed up the turn-off portion of the switching cycle.

R31 is a current shunt in the regulator output. If the voltage across R31 exceeds the voltage on R9, then transistor Q11-B tends to turn off and Q11-A turns on. When Q11-A conducts, the reference voltage to error amplifier A1 is reduced. The output voltage from the regulator then falls in proportion to the reduction in the reference voltage and thereby limits the current supplied by the regulator.

2.2.5.2 Bias Supply Inverter. The schematic diagram for the bias supply inverter is shown in Figure 2-19. The 133 Vdc output of the regulator provides the power for the oscillator. Transistor Q1 through Q4 are connected to form a bridge oscillator circuit. The circuit is initially started by charging capacitor C5 through resistor R1. When the voltage on C5 exceeds the breakdown voltage of diode CR10, a current pulse is supplied to the base of Q3 and, by the transformer action of T1, to the base of Q2. The current is sufficient to cause Q2 and Q3 to conduct momentarily. Transformers T1 and T2 are connected so that the conduction is reinforced by feedback voltages developed at terminals 9 and 10 of T1. Transistors Q2 and Q3 then turn on

until transformer T1 saturates. At that time, the current input to T1 from T2 is limited by R10. Q2 and Q3 turn off when T1 saturates, and T2 reverses its voltage taking the transformer out of saturation and turning Q1 and Q4 on. However, in time the transformer again starts into saturation and the cycle repeats.

The frequency of the resulting oscillation is determined primarily by tranformer T1.

Transformer T2 isolates the various outputs and produces the required voltages.

2.2.6 Signal Generator. The signal generator circuitry below is discussed in terms of functional subcircuits. Each subcircuit might be built from discrete components or combined in a single hybrid circuit module. A block diagram of how these individual circuits would be combined is shown in Figure 2-20.

2.2.6.1 Oscillator/Divider. This circuit contains the crystal controlled oscillator, dividers, and the control of the inverter output frequency. It provides control signals to three analog-to-digital converters and polarity information for each phase.

Figure 2-21 is the schematic diagram of the oscillator/divider circuit. U1 is a single integrated circuit providing most of the components of the clock and divider functions. The crystal and three passive components are external to the I.C., however. The 1,382.4 kHz output is supplied to the auxiliary function subcircuit (Figure 2-26C). The 86.4 kHz output is taken

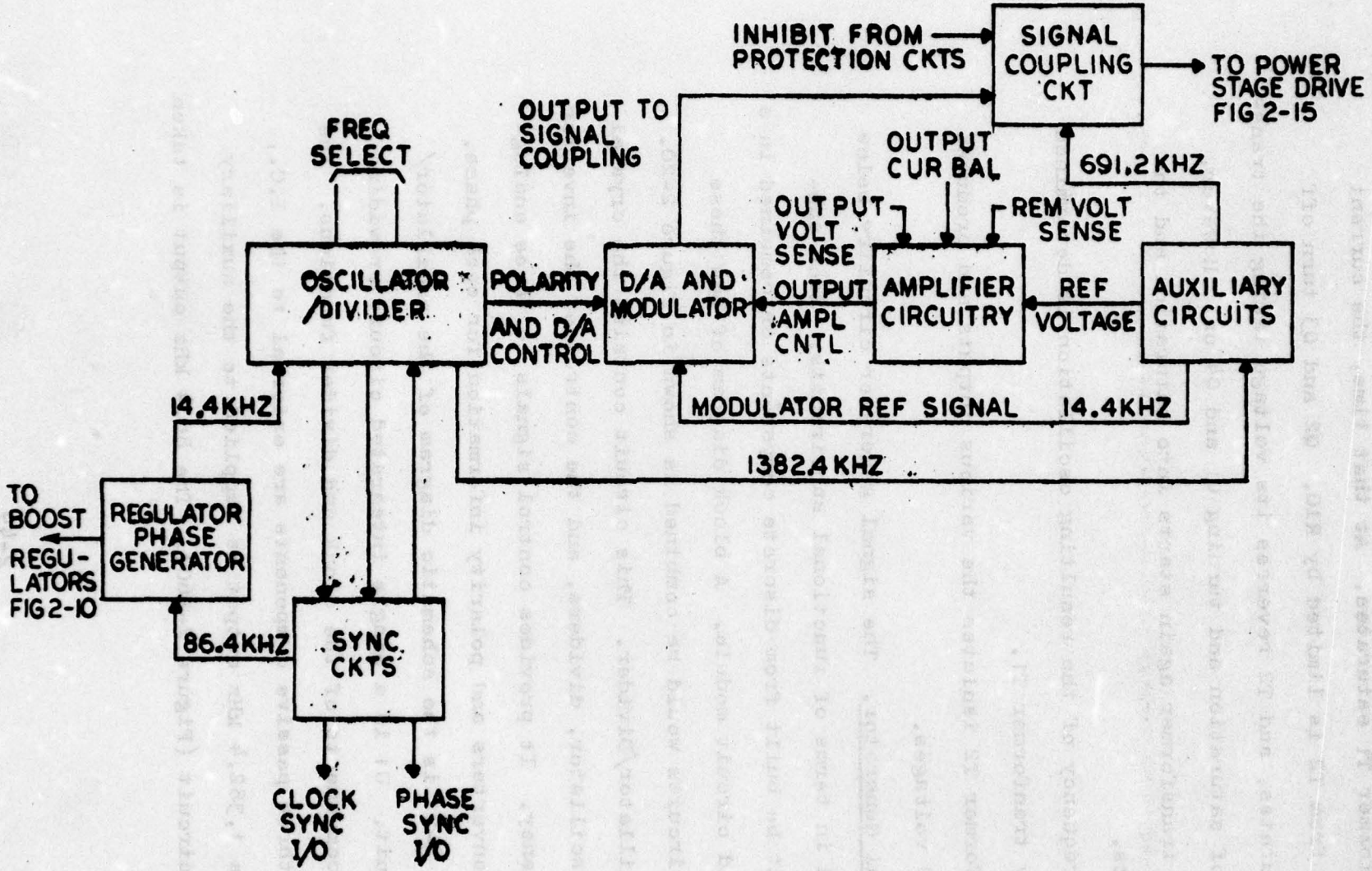



FIG 2-20, SIGNAL GENERATOR

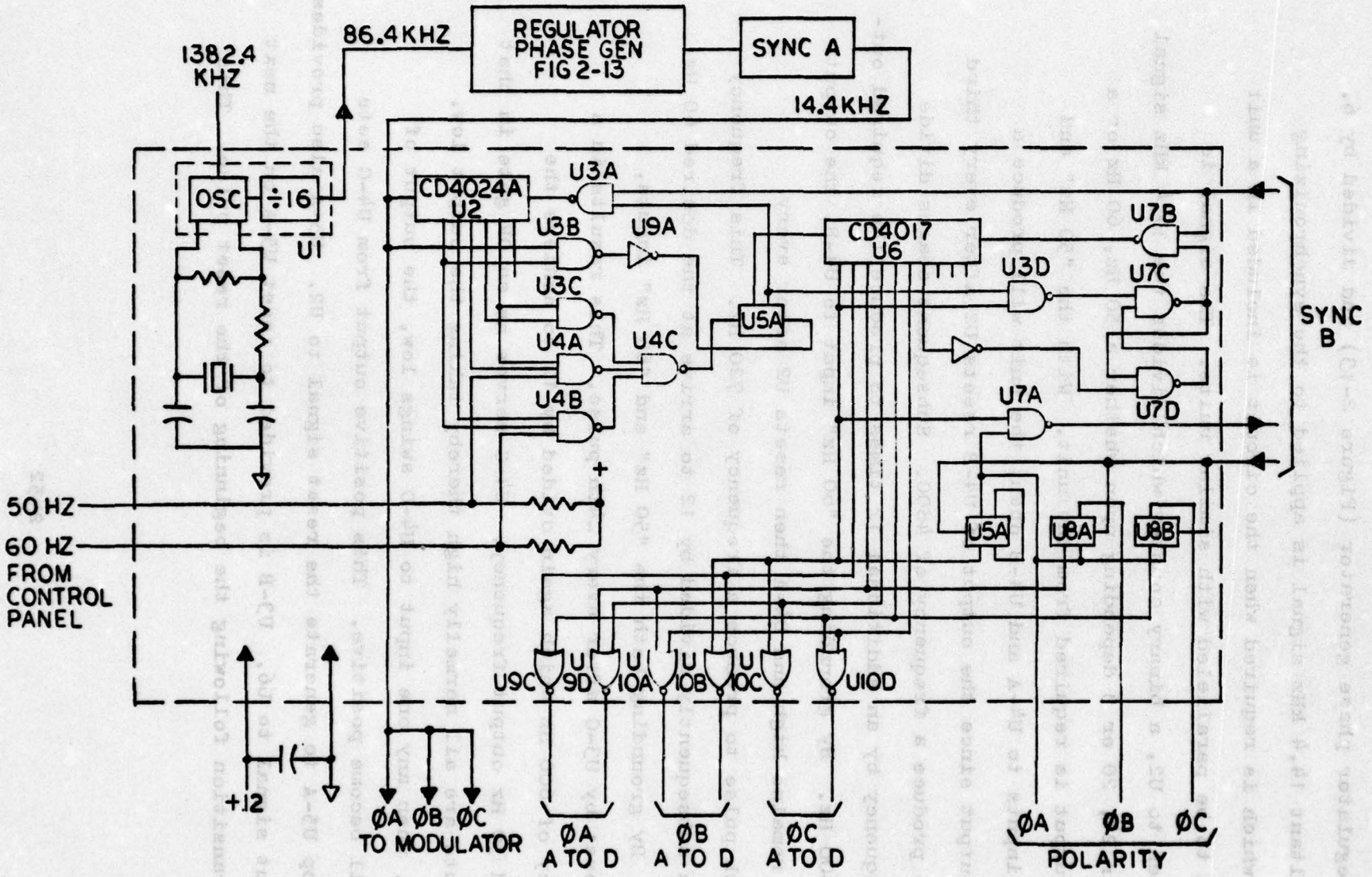



FIG 2-21, OSCILLATOR/DIVIDER

to the regulator phase generator (Figure 2-13) and divided by 6. The resultant 14.4 kHz signal is applied to the synchronizing circuit which is required when the circuit is included in a unit intended to be paralleled with similar units. The signal is then taken to U2, a binary counter which divides the 14.4 kHz signal by either 24, 20 or 3 depending upon whether a 50 Hz, 60 Hz or a 400 Hz output is required from the unit. With the "50 Hz" and "60 Hz" inputs to U4-A and U4-B open, the unit will produce a 400 Hz output since the output of U4-B resets U2 after every third pulse to produce a frequency of 4800. Subsequent stages divide this frequency by an additional 12 times to produce the required output of 400 Hz. By grounding the "60 Hz" input to U4-B, the output of U4-B remains high and U4-A then resets U2 after every twentieth pulse to produce a frequency of 720 Hz. This frequency is again subsequently divided by 12 to arrive at the desired 60 Hz output. By grounding both the "50 Hz" and "60 Hz" inputs, U2 is reset by U3-C after every 24th pulse. This results in a frequency of 600 Hz which again dvided by 12 to achieve the required 50 Hz output frequency. U4-C serves as an OR gate in that the inputs are all normally high thereby taking the output low. However, when any one input to U4-C swings low, the output of U4-C will become positive. This positive output from U4-C sets flip-flop U5-A to generate the reset signal to U2. U5-A also provides the input signal to U6. U3-B is provided to reset U5-A on the next clock transition following the beginning of the reset pulse. This

insures that the reset pulse is of pre-determined width and that there are no race problems in the circuit. U6 is an integrated circuit containing a counter and a decoder which operate to cause each of the outputs to go positive in turn while the others remain low. The I.C. normally provides a sequence of ten output pulses; however, a reset circuit consisting of U3-D, U7-B, U7-C and U7-D limits the sequence to six pulses. The six pulses are combined by NOR gates U9-C, U9-D, U10-A, U10-B, U10-C and U10-D to implement the signals required to drive the D-A converter. Flip-flops U5-B, U8-A and U8-B are interconnected with each other and with the outputs of U6 to determine the polarity of the output sine wave.

2.2.6.2 D/A and Modulator. The D/A and Modulator subcircuit together with the amplifier subcircuit serve the function of combining all the control, feedback and reference voltages needed to develop the switching signals required by the output stages. Separate pairs of circuits are required for each output phase.

The digital-to-analog converter of Figure 2-22 supplies a current to the input of amplifier A4 which is a stepped approximation of the magnitude of a sine wave function as shown in Figure 2-24a. The amplitudes of the current steps are determined by the summing amplifier (A3, Figure 2-23) and resistors R1, R2, and R3. Q3 and Q4 normally shunt the current flowing through R2 and R3, respectively, to ground. However, Q3 and Q4 are each periodically turned off by the logic signals from the

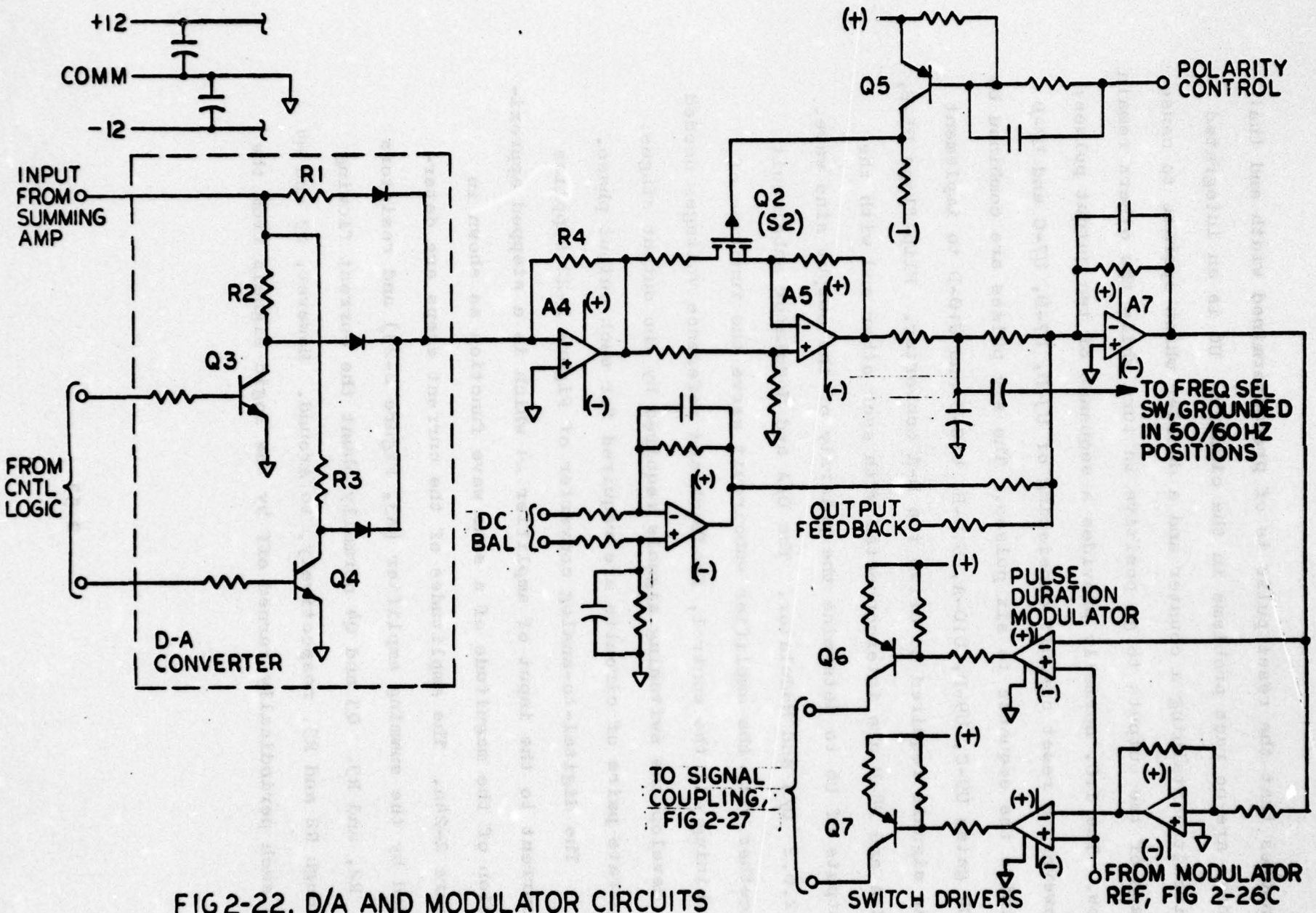



FIG 2-22, D/A AND MODULATOR CIRCUITS (ONE/PHASE)

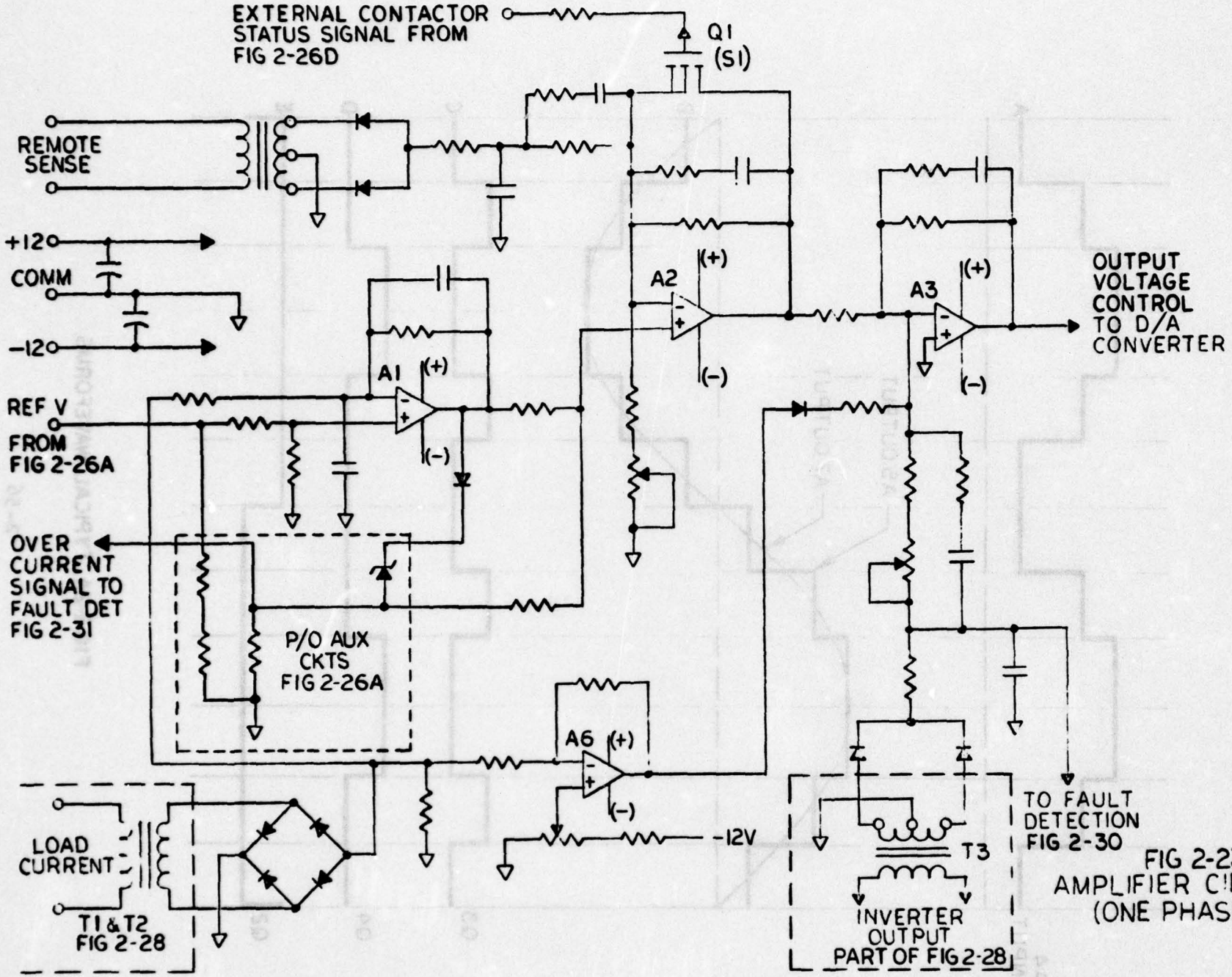



FIG 2-23
AMPLIFIER CIRCUITS
(ONE PHASE)

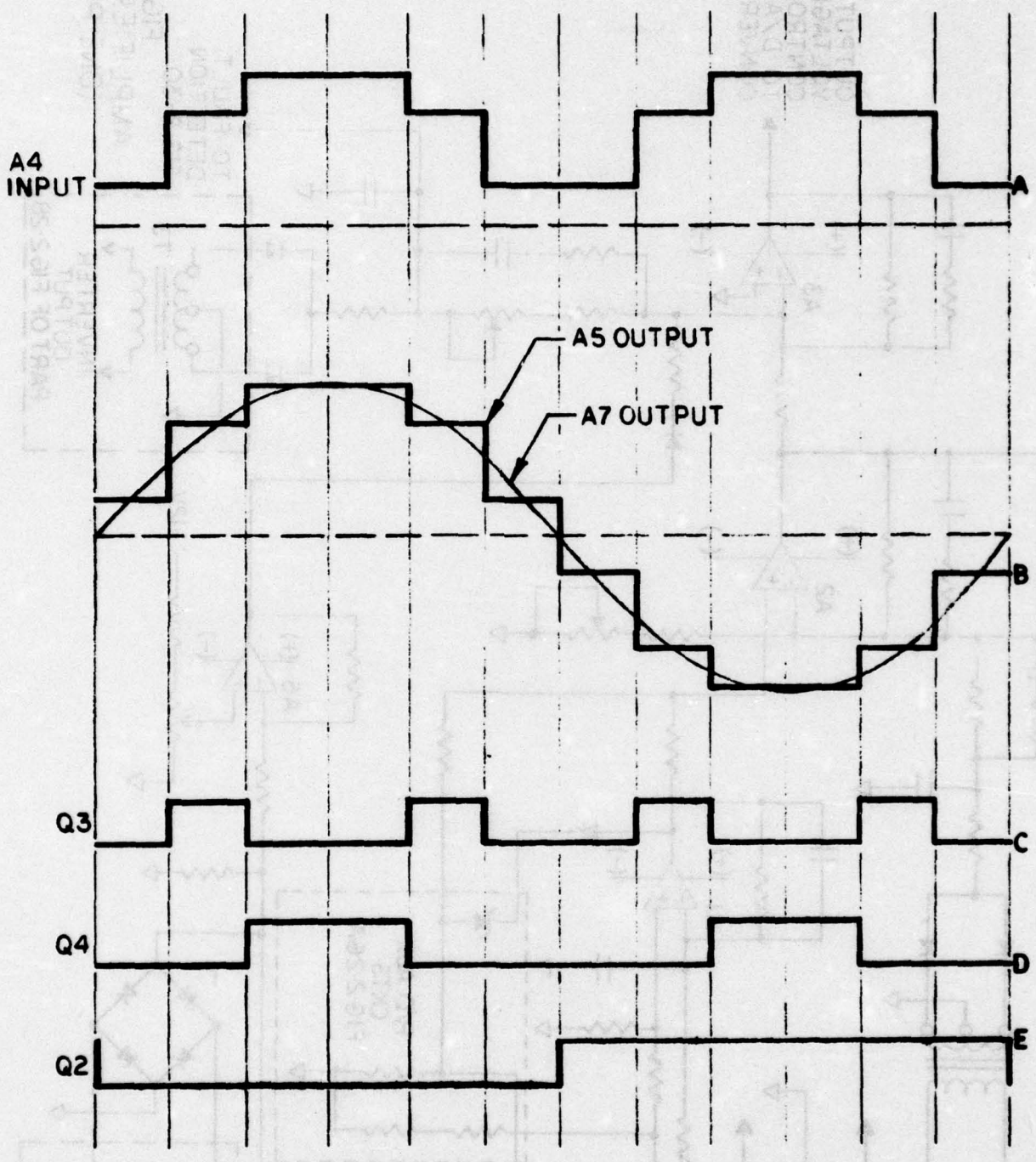



FIG 2-24, TYPICAL WAVEFORMS

oscillator/divider subcircuit thereby allowing the current to flow into the input terminal of A4. Figure 2-24c and 2-24d indicate the relative timing of these currents. The current through R1 flows continuously. The output of A4 is a negative voltage equal to the product of the input current and the resistance of R4, the feedback resistor.

The positive and negative portions of the sine wave are obtained by periodically switching the gain of A5 from +1 to -1 by means of Q2. The timing for the control signal to Q2 is shown in Figure 2-24e. Figure 2-24b illustrates the resulting un-filtered and filtered outputs of A5 and A7 respectively. Amplifier A8 receives a voltage input from the output of the unit. A8 acts as a low pass filter to remove the ac component of the signal. Any residual dc is then applied as negative feedback to A7 to reduce the dc component of the output.

A9 and A10 are comparator amplifiers which form the pulse modulator. A11 simply inverts the signal applied to A10. A triangular waveform is developed by the auxiliary circuit group (Figure 2-20) which is applied to both A9 and A10. The resulting wave forms are shown in Figure 2-25 (see Figure 2-3 for significance of switch designations). Q6 and Q7 are current amplifiers which drive the output switches via the signal coupling circuit of section 2.2.6.4.

2.2.6.3 Amplifier Circuits. The amplifier circuitry is shown in Figure 2-23. The inputs to amplifier A1 consist of the system reference voltage and a dc voltage which is proportional to the

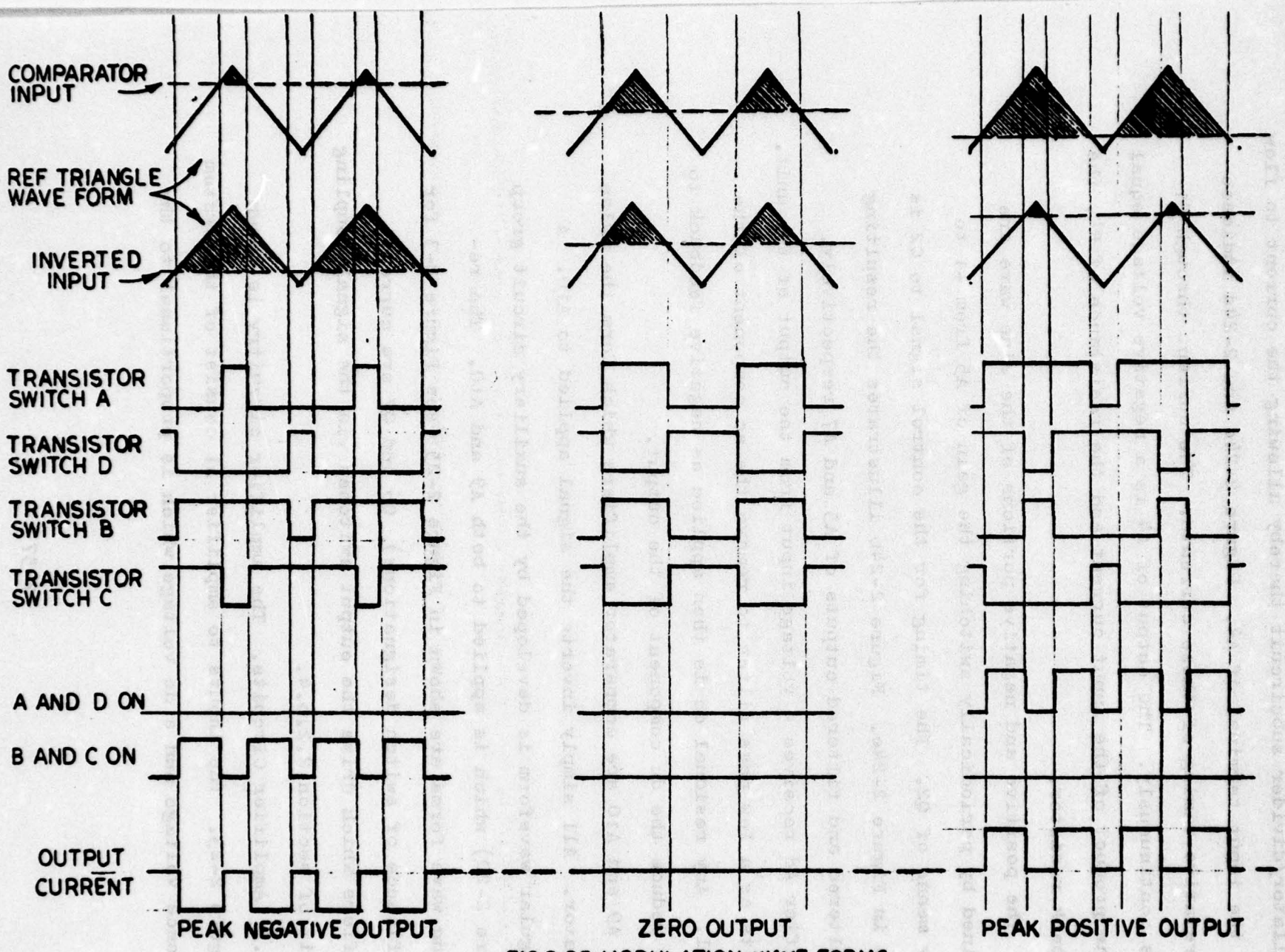



FIG 2-25 MODULATION WAVE FORMS

output current. With no load current, the output of A1 is a negative voltage determined entirely by the reference voltage. As the load current is increased, the output of A1 moves nearer to zero volts, thereby altering the reference applied to A2. This reduces the inverter output voltage in a controlled manner and serves to establish and output impedance which allows direct paralleling of units. When the load current exceeds 150% of the rated output, the zener diode conducts and reduces the output voltage to zero at a load current of 200 % of nominal.

The inputs to amplifier A2 are a dc voltage proportional to the load voltage at the selected point of regulation and the system reference as modified by A1. Typically, the regulation point is on a load bus which may initially be isolated from the inverter output by an open contactor. Therefore, switch S1 (a field effect transistor) is included to limit the inverter output voltage in the event that the contactor is open. S1 may be controlled by an auxiliary switch which is part of the contactor in such installations.

Amplifier A3 sums three signals. These are: 1) the output of A2 which serves as a reference for A , 2) a dc feedback voltage proportional to the inverter output and 3) a voltage proportional to the amount by which the instantaneous peak output current exceeds a pre-set limit. The first two signals establish the normal inverter output voltage. The third signal serves primarily to protect the output stage from large, peak overcurrents such as those created by a capacitor-input rectifier and filter.

2.2.6.4 Auxiliary Circuitry. The auxiliary circuitry of Figure 2-26 contains four functions not otherwise placed conveniently.

Reference diode CR1 (2-26A) provides the reference voltage for the entire system. Amplifier A1 and resistors R2 and R3 increase the current capability of the reference source while also providing a means of precisely adjusting the voltage from the circuit. C1 is included so that the output of A1 requires a finite time to reach the normal output level. This delay permits the inverter circuits to build up the output voltage in a controlled, rather than abrupt, manner. R4, R5 and CR2 determine the point at which the current limiting and over-current protection circuits begin to function.

U1 (2-26B) is a flip-flop used to divide the 1382.4 kHz oscillator frequency to 691.2 kHz for use in the sine wave generator output signal coupling circuits. The flip-flop insures that the output waveform is symmetrical. Q1 is merely a current amplifier to provide the necessary drive to the interface circuit.

A2, R9 and C4 (2-26C) form an integrator which converts the 14.4 kHz square wave from counter U2 oscillator/divider subgroup into the triangular waveform required by the pulse width modulator. C3 and R10 block the dc component of the input waveform and stabilize the output operating point at zero volts reference.

The transistor circuit of Figure 2-26D provides an interface between the auxiliary contacts of the external output con-

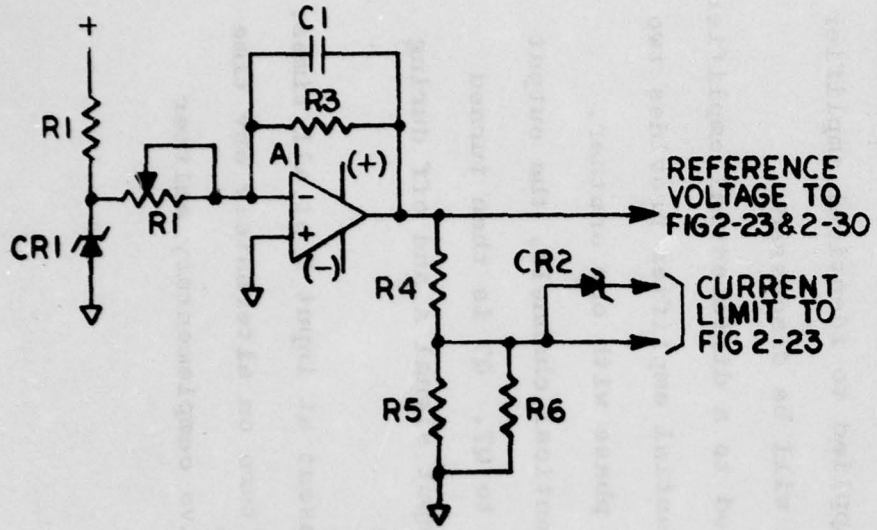



FIG 2-26A

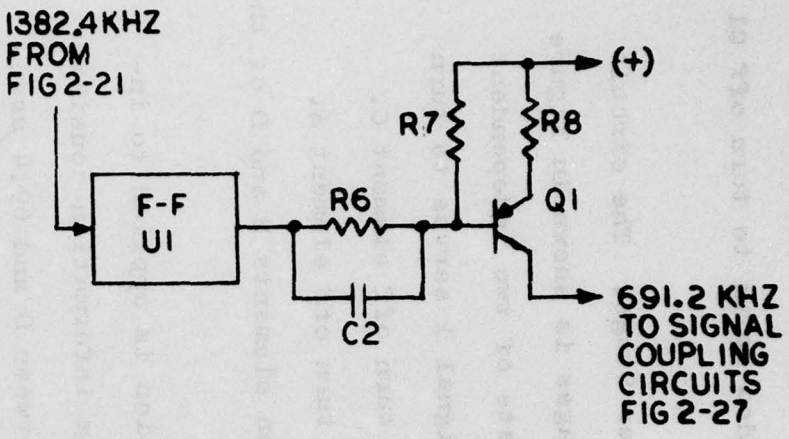



FIG 2-26B



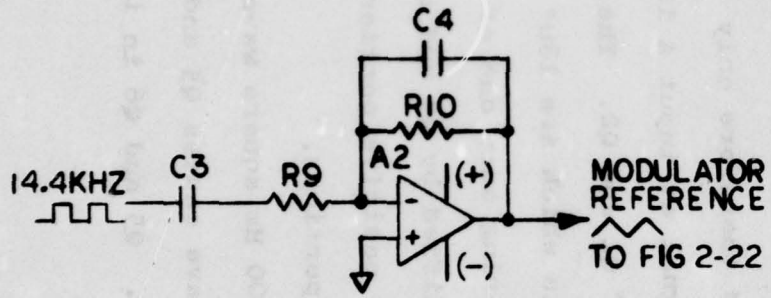



FIG 2-26C

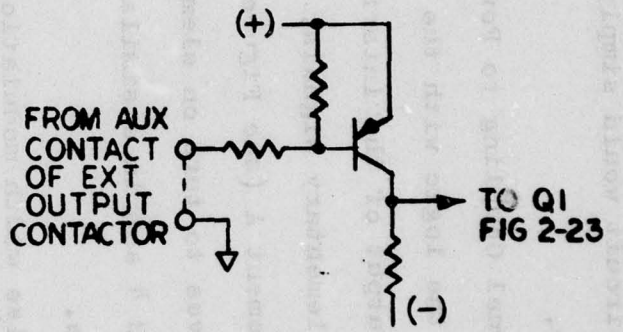



FIG 2-26D

AUXILIARY CIRCUITRY

tactor (if used) and Q1 of Figure 2-23. Alternately, the input to the circuit would simply be grounded so as to turn off Q1 at all times.

2.2.6.5 Signal Coupling to Power Inverter Stage. The circuit interfacing the logic with the output stages is shown in Figure 2-27. The output of the interface consists of two independent sets of complementary signals. Output signal 1 serves to turn on bridge element A (see Figure 2-3) and turn off element C. Output 2 serves to turn on element C and turn off element A. Outputs 3 and 4 act in a similar manner on elements B and D of the output bridge.

The pulse width modulation information is applied to inputs A & B of the interface circuit. This information consists of a series of pulses varying in width between 0 and 69.4 μsec. at a 14.4 kHz rate. Each input is applied to identical amplifier circuits, and therefore only input A will be discussed.

The signal at input A is applied to a differential amplifier consisting of Q1 and Q2. The differential amplifier provides two output signals which are 180° out of phase with one another. Again considering only one of two identical channels, the output of Q1 is amplified by Q4 and applied to Q7. Q7 is then turned on during the positive portions of input signal A and off during the negative portions.

A 691,200 Hz square wave is present at input D at all times. This square wave causes Q5 and Q6 to turn on alternately any time that Q7 is on. Q5 and Q6 in turn drive complementary emitter

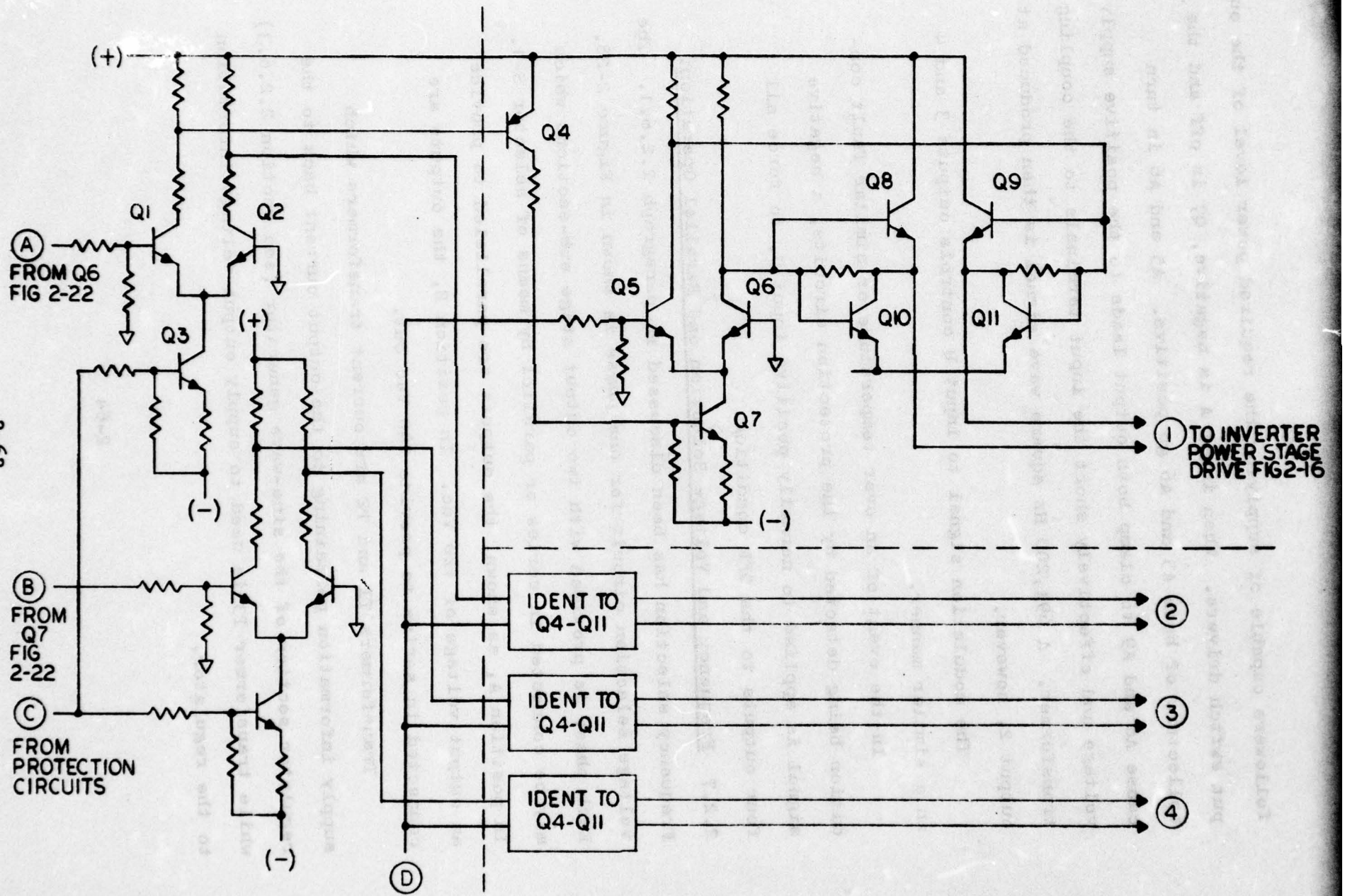



FIG 2-27, SIGNAL COUPLING

followers capable of supplying the required power level of the output switch drivers. When input A is negative, Q7 is off and the collectors of both A5 and A6 go positive. A5 and A6 in turn cause A8 and A9 to clamp both output leads to the positive supply voltage and effectively short the input terminals to the coupling transformer. A 691,200 Hz square wave signal is then produced at output 2, however.

The modulation signal to input B controls outputs 3 and 4 in a similar manner.

In the event of an over temperature or similar fault condition being detected by the protection circuits, a negative signal is applied to normally positive input C, to force all four outputs to the OFF condition.

2.2.7 Frequency and Voltage Selection and Parallel Operation. Frequency selection has been discussed in paragraph 2.2.6.1. The voltage selection circuit for one phase is shown in Figure 2-28. Each phase is provided with two output stage sub-sections which may be connected in series or parallel by means of selector S-1. In position A, as shown, the outputs are paralleled to provide an output voltage of 120 Vac. In position B, the outputs are connected in series to provide 240 Vac out.

Transformers T1 and T2 are current transformers which supply information pertaining to the output current back to the regulator section of the sine-wave generator (see section 2.2.6.3) while transformer T3 is used to supply output voltage information to the regulator.

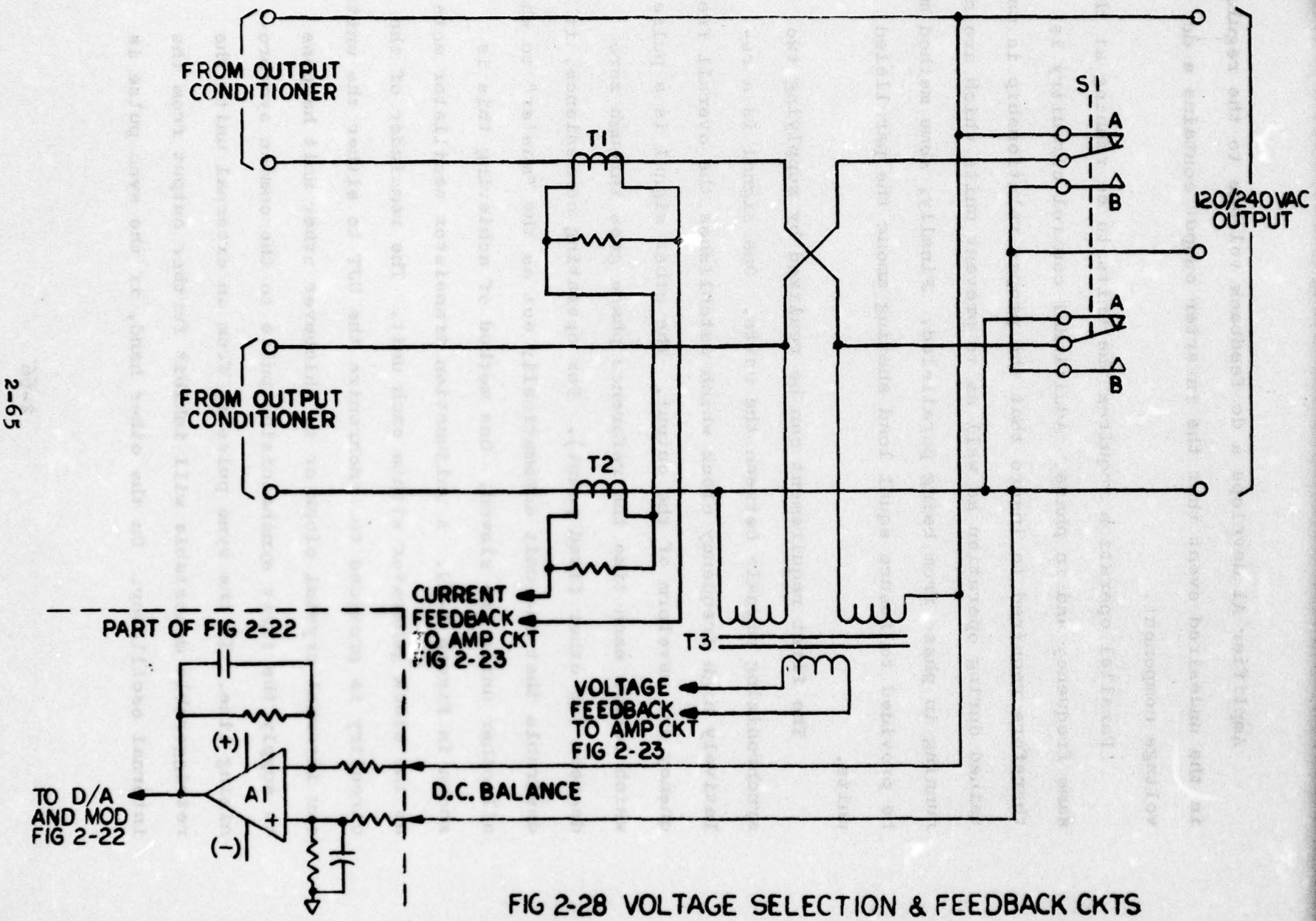



FIG 2-28 VOLTAGE SELECTION & FEEDBACK CKTS

Amplifier A1 develops a dc feedback voltage to the regulator in the undesired event that the inverter output contains a dc voltage component.

Parallel operation requires the units to be running at the same frequency and in phase. Additional control circuitry is therefore required to insure that the proper relationship is maintained during operation as well as to prevent units which are not running in phase from being paralleled. Finally, some method must be provided to insure equal load sharing among the paralleled units.

The first requirement can be realized by supplying two synchronizing signals between the units. One signal is a relatively high frequency clock which establishes the overall frequency and waveform of the output. The other signal is a pulse which occurs each time the reference phase goes through zero degrees (or other fixed point). For operating convenience, it is desirable that one unit automatically act as the "master" to which all other units are slaved. One method of achieving this is shown in Figure 2-29. A unijunction transistor oscillator acts as the clock generator within each unit. The remainder of the circuitry is provided to synchronize the UJT to either the unit's own internal crystal clock or to whichever other unit happens to supply the first synchronizing pulse to the common synchronizing line. If the sync pulse is from an external unit, the retriggerable monostable will inhibit further output from the internal oscillator. On the other hand, if the sync pulse is

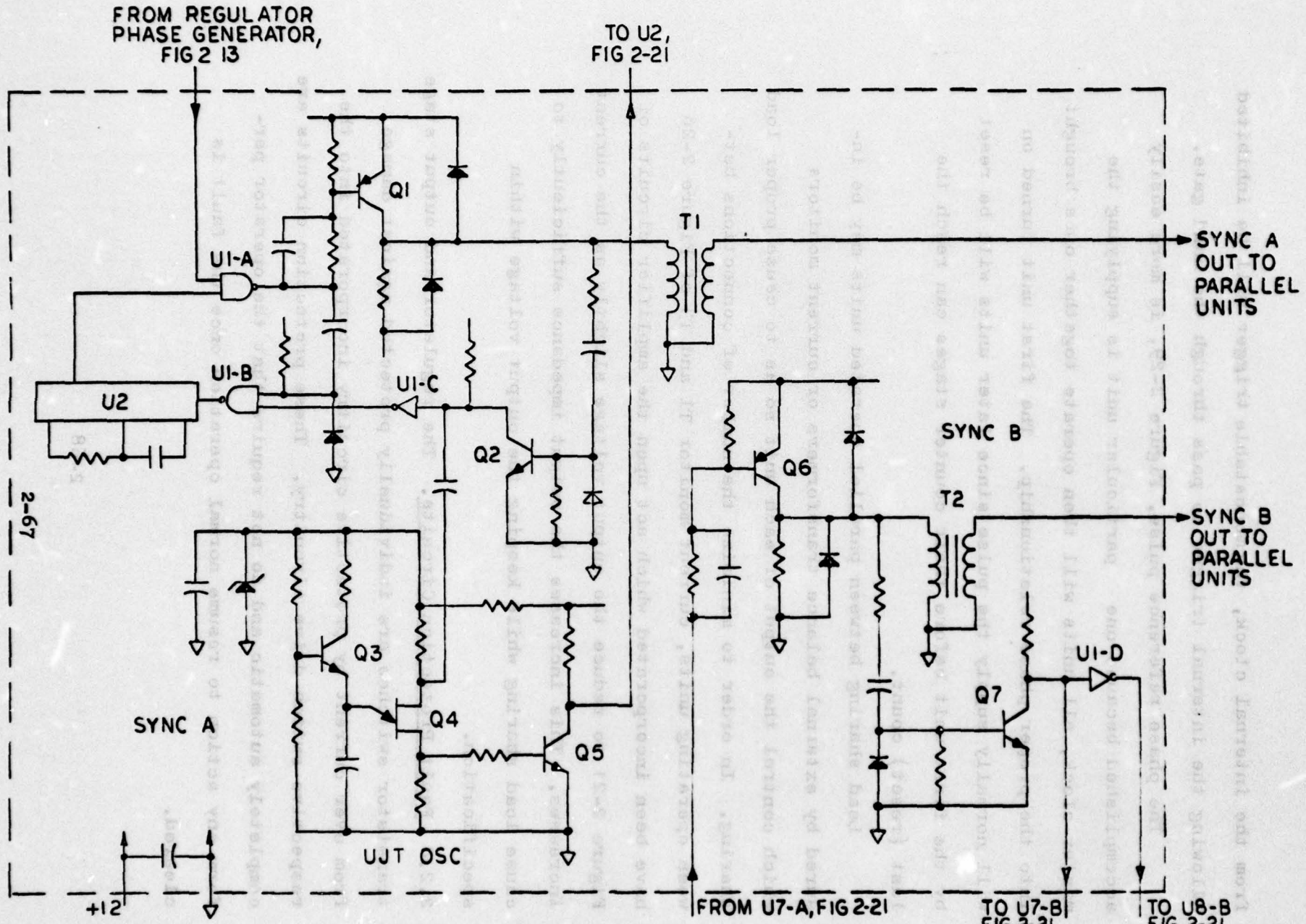



FIG 2-29, SYNCHRONIZATION CIRCUITRY

from the internal clock, the monostable trigger will be inhibited allowing the internal trigger to pass through the nand gate.

The phase reference pulse, Figure 2-29, is more easily accomplished because one particular unit is supplying the master clock, all units will then operate together once brought into the proper phase relationship. The first unit turned on will normally supply the pulse since later units will be reset by the first unit before their counter stages can reach the last (reset) count.

Load sharing between parallel operated units may be insured by external balance transformers or current monitors which control the output of each unit so as to cause proper load sharing. In order to minimize the number of connections between operating units, current monitor T1 and T3 of Figure 2-26 have been incorporated which act upon the amplifier circuits of Figure 2-21 to reduce the output voltage slightly as the current increases. This increases the output impedance sufficiently to cause load sharing while keeping the output voltage within specification.

2.2.8 Fault Protection Circuits. The regulator and output stage transistor switches are individually protected against damage from over current by protective circuitry incorporated into the respective switch drive circuitry. These protection circuits are completely automatic and do not require that the operator perform any action to resume normal operation once the fault is cleared.

The overall unit however, is protected by circuitry, Figure 2-30, which does require that the operator manually reset the control circuitry once specific faults occur. These faults include undervoltage or overvoltage on either the input dc voltage or any of the three ac output phases, overcurrent on any output, or an overtemperature condition within the unit. The effect of any of the fault conditions is to turn off the gate drive signal to the output switches, operates a "fault" signal relay, and de-energize a "run" signal relay. The relays are provided for the control of associated equipment, tripping circuit breakers etc as may be required in the operation of the unit. In addition, overcurrent and overtemperature indicator lamps are provided. The "fault" and "run" relays are controlled by a set/reset flip-flop consisting of nand gates U2-C and U2-D. The "run" relay is controlled additionally by signals applied to nand gate U2-B which delay the operation of the relay until after the inverter output has had time to reach the normal operation level and synchronizes with any parallel units. During initial turn-on, the flip-flop is reset by capacitor C2 which holds the reset input in the zero state for a brief period until charged through resistor R25. The output of U2-D is normally high and fault signal relay K1 is therefore de-energized. Both inputs to U2-C are normally positive and the flip-flop is in a stable state. Once a fault occurs, however, the output of U1-B goes negative which sets the flip-flop to the other state with the output of U2-D being low. This turns on Q3 and

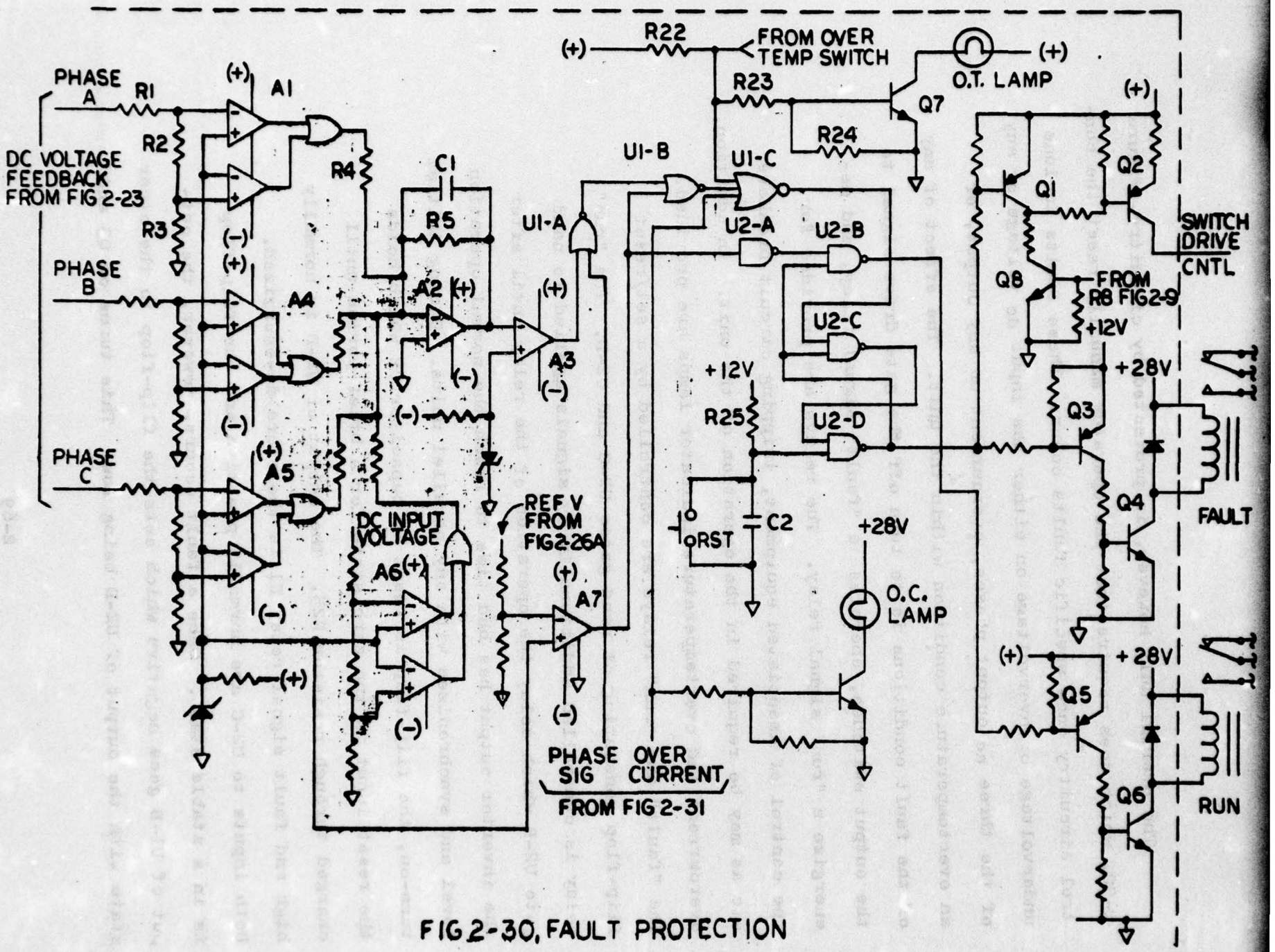



FIG 2-30, FAULT PROTECTION

energizes the fault signal relay. At the same time, Q1 turns on to turn off the gate drive amplifier Q2. With Q2 off, all output from the inverter is immediately inhibited. The flip-flop may be manually reset by means of a push button switch. The sine-wave generator section (see paragraph 2.2.6) contains transformers, rectifiers and filters which provide dc voltages which are proportional to the ac output voltage for each phase. These voltages are also applied to the individual phase inputs of the fault detection circuit. The schematic for this circuit is shown in Figure 2-30. The phase A input is applied to two inputs of dual comparator A1. In addition, a positive reference voltage is applied to the other two inputs of A1. The connections are arranged such that if the input voltage is either higher or lower than the specified limits, the output of A1 will swing positive.

R4, C1 and A1 act as an integrator circuit to determine the allowed period of out of tolerance operation. The output of A1 is a negative-going ramp generated in response to the sudden positive step which occurs at the output of A1 in the event of either a undervoltage or overvoltage condition.

The output of A2 is applied to one input of comparator A3. A negative reference voltage is applied to the other input. When the output of A2 becomes more negative than the reference, the output of A3 goes positive; however, the output of A3 is normally zero volts. The phase B and phase C circuits function in the same manner, as also does the input voltage detector

(circuits A4, A5 and A6 respectively). The output of A3 is applied to one input of NOR gate U1-A. The other input comes from the phase comparison circuit to be described later. Normally, both inputs to U1-A are low and therefore the output is high. However, during start-up one or both of these signals will go high forcing the output of U1-A low. To prevent this momentary condition from shutting down the inverter, U1-B is included in the circuit. In addition to the signal from U1-A, U1-B also gets an input from comparator A7.

The sine-wave generator reference voltage (Figure 2-26A) is applied to comparator A7. Upon initial turn on of the unit, this voltage does not immediately reach its final value . This delay is introduced to control the rate at which the output voltage from the inverter builds up to the operating voltage. By applying the reference voltage to A7, the output of A7 may be used to inhibit the action of the undervoltage detection and phase comparison circuits during the turn-on sequence. During turn-on, the output of A7 is a positive voltage applied to one input of NOR gate U1-B, thereby holding the output of U1-B low regardless of the other input. In addition, the output of A7 is inverted by U2-A and applied to one input of NAND gate U2-B. The output of U2-B is thereby forced to the high state de-energizing the "run" relay, until the reference supply voltage reaches the value required to swing the output of A7 negative. The phase comparator circuit of Figure 2-31A compares the phase of one leg of inverter output to the phase of the load bus to which

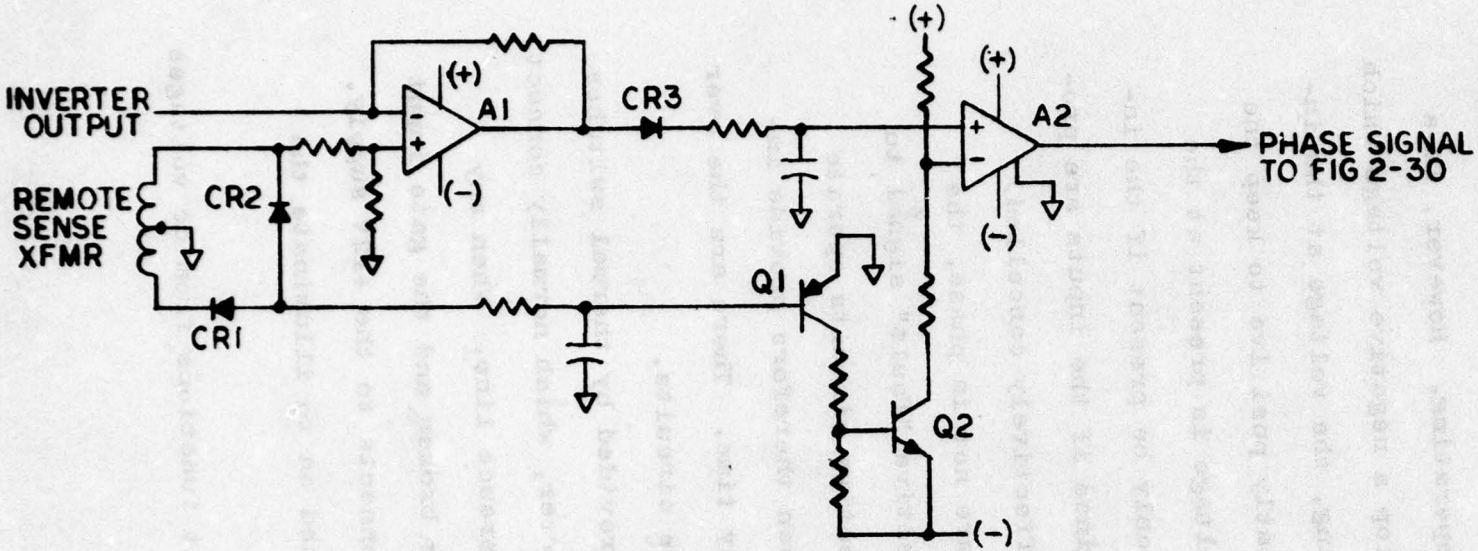



FIG 2-31A, PHASE COMPARATOR CKT

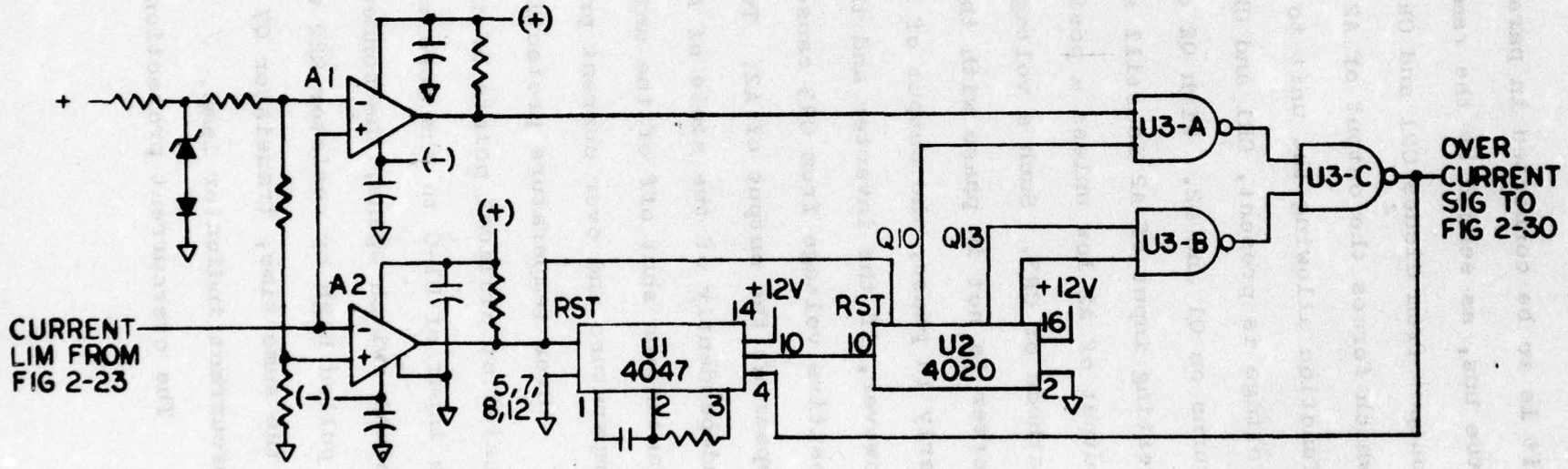



FIG 2-31B, OVER CURRENT TIME LIMITER

it is to be connected in parallel. If no voltage is present on the bus, as sensed by the remote sense transformer, there is no output from diodes CR1 and CR7; therefore, both Q1 and Q2 are off which forces the output of A2 low. This inhibits the comparison function allowing the unit to start operating. However, if a voltage is present, CR1 and CR2 develop a negative voltage which turns on Q1 and Q2. With Q2 conducting, the voltage at the inverting input of A2 is still sufficiently positive to keep the output of A2 low unless a positive voltage is present at the cathode of CR3. Such a voltage will only be present if the inverter is not in phase with the bus since if the inputs are properly in phase, the output of A1 is effectively cancelled. However, if the inverter and the bus are not in phase, the positive voltage from CR3 causes a positive "fault" signal to appear at the output of A2. Two protective circuits operate independently of the state of A7 and can therefore provide instantaneous shut off of the unit at any time. There are the over temperature and over current protective circuits.

Over temperature protection is provided by thermal switches located at critical points of the inverter, which normally connect the input of U1-C to the zero volt reference line. When any thermal switch opens, the connection is broken and the gate input is pulled high by resistor R22 which connects to the +12V supply. At the same time, transistor Q7 is turned on to illuminate the overcurrent indicator lamp.

The overcurrent protection circuit functions from dc voltages

developed in the sine-wave generator regulator circuit as described in section 2.2.6.3. At normal operating currents, the voltages are nearly constant although there is a slight linear change with changing output current. However, once the output current increases beyond a threshold level, the control voltage supplied to the protection circuit varies much more rapidly with increasing current than in the normal operating range. The schematic diagram for the remainder of the overcurrent protection circuit is shown in Figure 2-31B. The control voltage is supplied to comparator amplifiers A1 and A2. An overcurrent of 150% will cause the output of A2 to go to zero volts from the normally high voltage of the output. This removes the reset signal from astable-multivibrator U1 and allows the circuit to oscillate. The output of U1 is counted down by counter U2. The appropriate outputs of U2 are decoded by U3-B so that if the overcurrent condition persists for 120 seconds, the output of U3-B goes negative and a positive going fault signal results at the output of U3-C. This fault signal is applied to the input of U1-B, Figure 2-30, to shut down the gate drive current to the output switching transitors.

If the overcurrent exceeds 200% of full load, then the output of A1 goes positive. Since U1 is already oscillating by virtue of the lesser over current required to activate A2 counter U2 will operate as before. However, the connections are such that only 10 seconds are required for the counter output together with the positive voltage from A1 to cause the output of

U3-A to go negative, thereby forcing the output of U3-C to go high as before.

The effect of the above is to allow the unit to run for 120 seconds at a moderate overcurrent level, yet shut the unit down quickly in the event of a more serious fault.

Fault isolation in the inverter control is to be accomplished using only a VOM. In general, this may be accomplished using ordinary test points to monitor critical voltages (with voltage dividers and/or isolation resistors where required). Over-temperature and over-current indicators are also provided. If required, frequency and phasing could be checked with sufficient accuracy by monitoring dc voltages proportional to the duty cycles of a monostable multivibrator and a flip-flop, respectively, which could be incorporated into the protective circuitry. Typically, however, any failure in the frequency or phasing circuits will result in the complete loss of at least one phase; therefore, precise internal monitor circuits are not necessary or recommended.

2.3 MECHANICAL AND THERMAL DESIGN. For the sake of simplicity and maintainability, the same packaging approach is recommended for each inverter in the family. The primary differences will be in the number of transistor bridges in the power inverter stage required to produce the necessary power. The following discussion pertains particularly to the 5 kW inverter, but the extension to higher power units is reasonably obvious.

2.3.1 Mechanical Design. Figure 2-32 shows a layout of the recommended inverter. It will be observed that the volume is 3480 cubic inches, which is under the maximum volume of 3500 cubic inches. With the experience gained in contract No. DAAK04-74-C-0388, it appears that this volume is easily attainable with proper attention to detail design. It will be noted that output stages form interior supports for the housing, thus making a very rugged assembly. It will also be noted that all electronic components are enclosed in a watertight enclosure, thus assuring long life under severe humidity, salt spray, or dust conditions. The weight is evenly distributed throughout the assembly for easy handling by operating personnel. The front panel controls, connectors, and pilot lights are protected from damage by a flange extending completely around the front panel.

2.3.2 Cooling. In the design shown in Figure 2-32, a fan sucks air through the sides of the unit, with all the heat producing elements in the package conducting heat to the sides. This design lends itself well to cooling with the fan shown, or with a variety

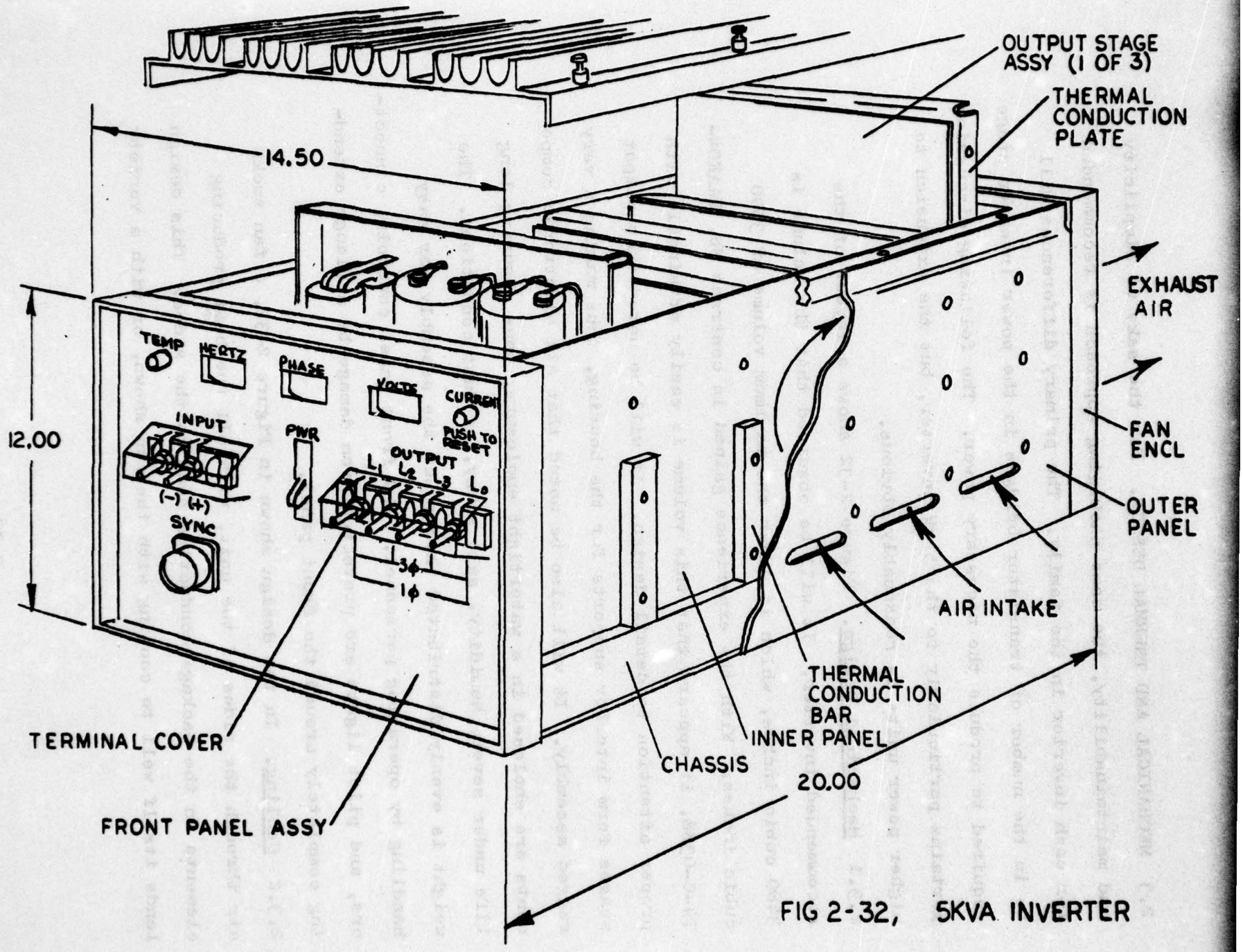



FIG 2-32, 5KVA INVERTER

of arrangements with the cooling air from some other source. One possible source of air would be the blowers of a fuel cell supplying dc to the inverter. DECC has experimented with a double wall construction which effectively triples the surface area available for convective cooling. This has been verified experimentally. With the expected temperature rise, however, approximately half of the cooling is accomplished by convection and half by radiation. It is assumed that the thermal drop between the inner and outer wall is very small, which indeed has proven to be true in the models of this type of cooling. Thus, the cooling from radiation would remain the same with or without the double wall construction. The convective cooling from the sides is increased by a factor of 3. Thus, the total cooling available from the sides of the unit is increased by a factor of about 2. Since the cooling from the top, front and back is not affected, it is anticipated that improvement in cooling is of the order of 50% overall, which is still very significant. A field option could allow for operation without a fan, as shown in Figure 2-33. It may be necessary to derate the unit either in maximum temperature or maximum power, if this option is used.

2.3.3 Construction Costs. The assembly as shown is easily fabricated from sheet metal and should be very economical to produce in quantity. No special tools, expensive dies or jigs are required for production and the design is believed to be a straight-forward easy production concept.

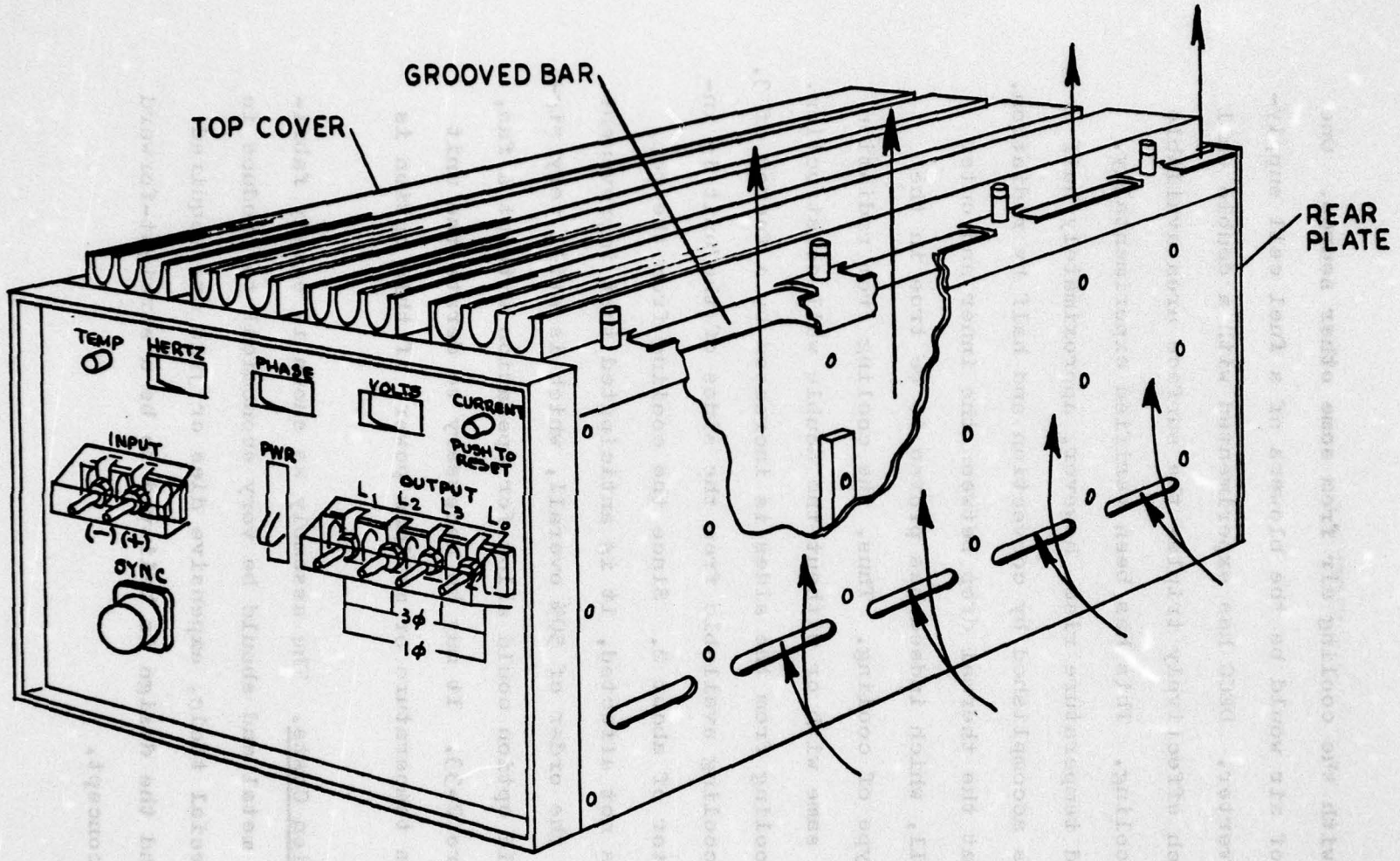



FIG 2-33, 5KVA INVERTER
SPECIAL PARTS FOR CONVECTION COOLING ARE NOTED

2.3.4 Electromagnetic Interference. The design of Figures 2-32, 2-33 minimizes EMI generation. The "transformerless" approach offers some advantages and some disadvantages, as far as EMI is concerned. In previous work of this nature, it was found that low frequency transformers are very difficult to shield to prevent radiation at low frequencies because of the great skin thickness at low frequencies. In the proposed inverter all the internal frequencies will be high enough so that radiation should not be a problem through a housing of reasonable thickness.

Conducted interference is somewhat more difficult because of the large filters required. Proper EMI construction techniques minimize the conducted interference caused by poor wiring layout. In this design the input and output are isolated from all the switching circuits by the barrier shown in Figure 2-32 on which the capacitors and inductor are shown mounted. EMI filters attach directly to each input and output lead.

No problems should be encountered with susceptibility of this unit to conducted or radiated noise because of excellent shielding and because of the EMI filters on each lead.

2.3.5 Audible Noise. The utilization of a high frequency inverter for the boost circuit and "transformerless" output causes the noise from high current leads, transformers, inductors and so forth to be above the audible frequency range. The principal source of noise within the audible frequency range specified is the fan. It is anticipated that this fan can be made reasonably quiet. In any case, the fan can be turned off by utilizing the field option of convection cooling.

## 3.0 RESULTS

3.1 TRADE-OFF STUDY. The preliminary trade-off study evaluated many forms of inverter which might be suitable for the intended use and which might meet the design requirements. Designs were evaluated with respect to the objectives of low production cost, minimum size and weight, maximum efficiency, and maximum reliability, availability, and maintainability. The trade-off study resulted in a recommended general form for the family of inverters.

3.2 DETAIL DESIGN. Although no hardware was built, a detailed mechanical and electrical design was developed for the family of inverters.

3.3 PROJECTED CHARACTERISTICS. As a result of the detailed design and previous experience in the production of inverters, various characteristics of the inverters can be projected.

3.3.1 Frequency Regulation. Because the output frequency is controlled by a crystal oscillator, the frequency regulation is expected to be in order of magnitude better than the required .5% short term and 1% long term.

3.3.2 Voltage Regulation. To permit direct paralleling of units, the voltage regulation is carefully controlled to provide a 2% V maximum drop at full load as allowed by the specification.

3.3.3 Distortion. The maximum single frequency distortion component is expected to be approximately 1% or half of the allowed limit. Total harmonic distortion is expected to be well under the 5% allowable distortion.

3.3.4 Efficiency. It appears that the specificed efficiency of 85% is a realizable goal. Table 3-1 lists the estimated loss

breakdown for the 5kW unit.

3.3.5 Cost. Cost is minimized by the use of common components for all the inverters in the family. The control logic and bias supplies would be identical for all units. The higher power units would employ parallel sets of the same transistor switching assemblies as would be used in the low power units. The magnetic elements and some elements of the input circuit would be the only items individually sized for each inverter. Cost is further minimized by the elimination of all large, expensive low frequency transformers and inductors from the design. Use of the boost inverter appears to be the most economical method of meeting the severe energy storage requirements presented by single phase operation of the larger machines. In addition, the entire system may be fabricated from readily available, proven components.

3.3.6 Reliability and Maintainability. DECC has designed and built a 1.5 kW inverter using much of the circuitry recommended here. The resulting design underwent a part stress analysis prediction according to MIL-HDBK-217B. The calculated MTBF for the inverter using standard commercial components was 3700 hours, and using high reliability parts was 16000 hours. Two inverters using the commercial components have been operating in the field. One of them has logged a total of 4000 hours without failure and the other has logged 2500 hours without failure. Parts count analysis of the proposed designs predicts comparable MTBF's for the 3, 4, and 10 kW units.

TABLE 3-1

Summary of Losses, 5kW Unit

| | | Watts |
|---|---|---|
| **Input filter** | | |
| Inductor | | 8 |
| Inductor | | 8 |
| | | 16 |
| **Bias Supply Boost Regulator** | | |
| Drive | | 2.2 |
| Switching transistors | | 24.7 |
| Inductor | | 3.1 |
| | | 30 |
| **Bias Supply Inverter** | | |
| Switching Transistors | 25.25 x 6 | 151.5 |
| Transformer | 26.7 x 6 | 160.2 |
| Energy recovery system | 7.45 x 6 | 44.7 |
| Rectifier | 3.6 x 6 | 21.6 |
| Drive | 13.3 x 6 | 80 |
| | | 458.0 |
| **Output Switch** | | |
| Switching transistors | 27.1 x 6 | 162.6 |
| Filter | 5.4 x 6 | 32.4 |
| Drive | 4.8 x 6 | 28.8 |
| | | 223.8 |
| Misc. Logic | | 50.0 |
| Relays | | 20.0 |
| Fans | 15 x 2 | 30.0 |
| | | 867.8 |

$$\text{Efficiency} = \frac{5000}{5000 + 867.8} \times 100\% = 85.2\%$$

The use of modular construction as shown in the design provides a major aid in maintainability. The whole family of inverters can be repaired from a relatively small stock of common assemblies.

3.3.7 Weight and Size. Because of the modular nature of the design, the weight and volume of the various units will tend to vary directly in proportion to the rated output power. However, the common circuitry such as the bias supply and signal generator circuits add a fixed volume and weight to the variable quantities.

In general, the specified maximum weight and volume limitations are consistant with equipment previously developed at DECC although it would appear that the weight limit for the 3 kW unit should be increased by 5 to 10 pounds. The target values for weight and volume are not consistant with the design goals of convection cooling and low cost, however. Convection cooling requires the largest possible surface area together with an internal structure of adequate thermal conductivity leading to the surface of the unit. The first priority for the family of units is low cost, and little, if any, savings could be effected by reducing the volume to the target values. Furthermore, such items as the bias supply and signal coupling circuits would have to be sized for each inverter in the family rather than having common parts which could be installed in any of the inverters. This would obviously increase the number and cost of the spare parts required.

Reduction of weight in the unit would require the use of smaller transformers, fewer switching transistors, for example. These changes would all have an adverse effect upon efficiency and reliability, and therefore, are not recommended even though efficiency and reliability are less important goals than weight in the listing of priorities.

3.3.8 Effects of Higher or Lower Supply Voltages. The effects of utilizing nominal supply voltages significantly higher or lower than the specified range of 30 - 60 volts were not investigated in detail. However, it is apparent that increasing the supply voltage leads to more efficient operation by reducing the input current and consequent conduction losses, for a given output power. Extremely high voltages are undesirable in view of the difficulty of obtaining adequately rated components. Supply voltages in the 200 Vdc to 300 Vdc range are practical, however, and would eliminate the need for any bonus of voltage boost within the unit. Efficiencies greater than 90% might then be anticipated and costs would be reduced significantly. Low voltages would, of course, produce the opposite effect.

## 4.0 CONCLUSIONS

It appears possible to meet the specification requirements with the proposed design at a lower cost than would be possible with the other alternatives which were investigated.

The discussion has considered the design of the 5 kW inverter in considerable details. With the possible exception of the 3 kW unit, all other units in the family could be assembled from appropriate combinations of sub-assemblies from the 5 kW unit. Thus, the 10 kW unit would use paralleled switching circuits to meet the added current requirements of the boost regulator and output switches. The 1.5 kW unit would simply be one phase of the 5 kW unit (actually 1.67 kW). Separately sized magnetic components are recommended for each unit, however.

The 3 kW unit does not conveniently fit into the modular series with the other units unless the entire series is constructed from very small modules. There are at least four possible alternatives to the smaller modules. These include:

1) Delete the requirement for a 3 kW unit.
2) Develope a group of smaller modules specifically for the 3 kW unit.
3) Use half of the "standard" modules to construct a 2.5 kW unit. Note that a transformer would be required at the output, however, to provide the required voltage selection. See figure 4-1A.
4) Four standard modules could be used to provide 3.3 kW at either 120 or 240 volts output (single phase). Three modules would then be used to provide 3.3 kW 120

volts, three phase. See Figure 4-1B. The extra module could be used to provide an addition 833.3 W of single phase 120 volt power.

Of the above, option 4 appears to have the most merit.

The critical areas are the efficiency of the boost regulator (which contributes over half of the total losses) and the thermal design of the unit. While heavier and larger forms of packaging might permit the unit to operate without any forced air cooling, in the interest of overall economy the inclusion of one or more small fans is recommended.

While no hardware was built as part of this study to prove the design, experience gained at DECC in the development and manufacture of related products leads to the belief that the predicted results are realizable.

AD-A036 027 DELTA ELECTRONIC CONTROL CORP IRVINE CALIF F/G 10/2
TRADE-OFF INVESTIGATIONS AND DETAILED DESIGN OF POWER INVERTERS--ETC(U)
JAN 77 W G LAWRENCE DAAG53-76-C-0077
UNCLASSIFIED DECC-61131-002 NL

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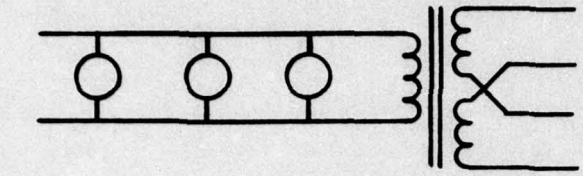
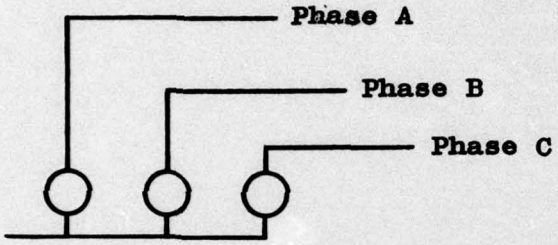


2.5 kW

120/240 V

single phase




120 V

3 phase

A

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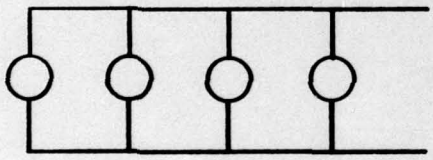
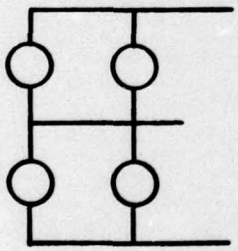


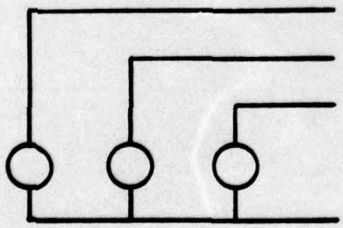
120 V, single phase

3.3 kW



240 V, single phase

3.3 kW



120 V, 3 phase

2.5 kW

B

Figure 4-1. 3 kW Inverter