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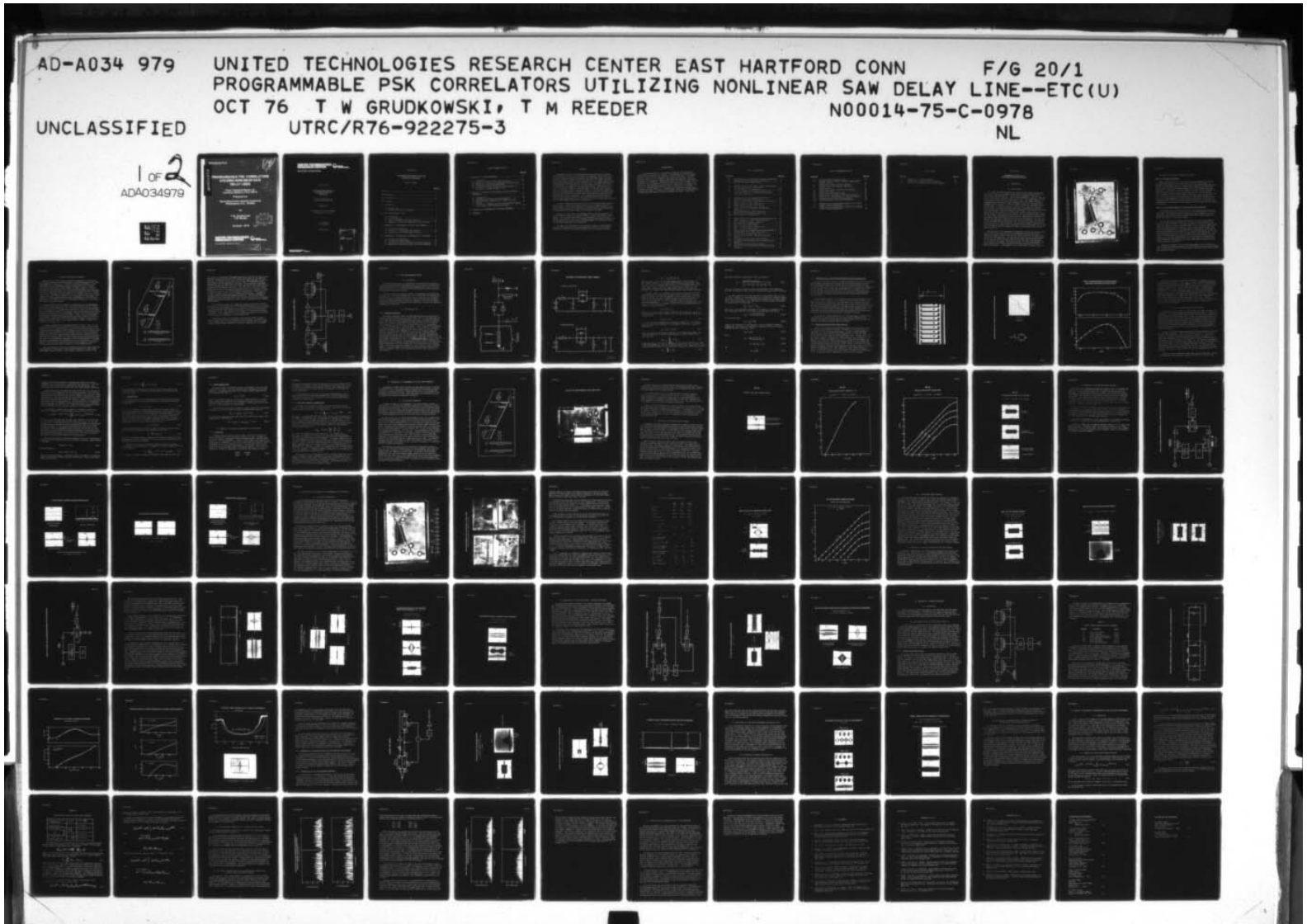

R76-922275-3

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Final Technical Report on
Contract N00014-75-C-0978

Prepared for

Naval Electronics System Command
Washington, D.C. 20360

by

T.W. Grudkowski
T.M. Reeder

October 1976

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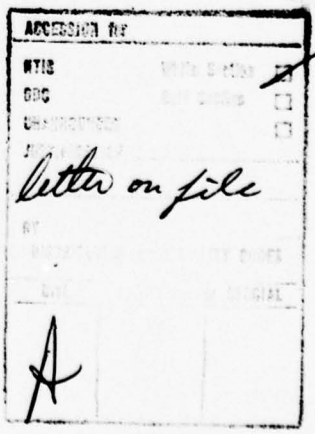

Programmable PSK Correlators Utilizing Nonlinear SAW Delay Lines

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ABSTRACT

This report describes an experimental and theoretical study of nonlinear tapped delay lines for use in electronically programmable, long code Phase Shift Key (PSK) signal correlation and encoding. The programmable delay line device studied here, which is called the PSK Diode Correlator, is a hybrid, Integrated Circuit device which utilizes a Surface Acoustic Wave (SAW) tapped delay line and an attached microelectronic diode and resistor array. PSK Signal processing is accomplished at the P diode-taps of the signal processing region of the device by a low power, wide bandwidth, nonlinear mixing process. PSK input and cw reference voltages are applied to the two delay line inputs at center frequency f_1 and f_2 respectively and the correlation output at the difference frequency is received at a common electrode summing the nonlinear outputs of the P diode taps. Rapid PSK code programming of the correlator taps is achieved by applying equal amplitude, positive or negative bias to the antiparallel diode pair located at each delay line tapping transducer. Each correlator module has an associated cascade delay channel fabricated on the same SAW substrate to allow interconnection with identical modules for long code PSK processing.

The design, fabrication and testing of 64 and 128 tap devices are described which utilize lithium niobate delay lines and silicon on sapphire diode and resistor arrays. These devices operate with signal and output frequencies near 70 and 30 MHz respectively and have delay line tap spacing chosen for processing PSK sequences with chip rates equal to, or a multiple of 9.8 MHz.

Operation of these devices as programmable PSK encoders and correlators is demonstrated with experimental results compared to theoretical behavior. Application to long code PSK signal processing is evaluated by testing a 2 module cascade. The detailed design of the broadband cascade delay channel is described. Systems applications including high speed reprogramability, interference rejection and error compensation are demonstrated.

The effect of system errors on the correlation response of a multi-module long code PSK cascade processor is analyzed, and the effect of finite module bandwidth is discussed in a simulated 8 module, 1024 chip cascade correlator.

ACKNOWLEDGMENTS

The authors are pleased to acknowledge the many contributions made by others during the course of the program. The successful construction and performance of the 64 and 128 tap correlators is due in large part to the microelectronic expertise of E. Branciforte who fabricated the devices. Careful processing of the silicon on sapphire diode arrays and diagnostic devices was performed by B. Bujnarowski. Detailed measurements of the device parameters were carried out with the competent assistance of W. Sheades and D. Kleeberg. The authors have also appreciated and have benefitted from discussions with D. Webb of the U. S. Naval Research Laboratories and L. Sumney of the U. S. Naval Electronics Systems Command. A. J. DeMaria and M. Gilden have provided their enthusiasm and support. Thanks are also sincerely expressed to the Illustrations and Word Processing Groups for help in assembling this report in final form.

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1.0 INTRODUCTION

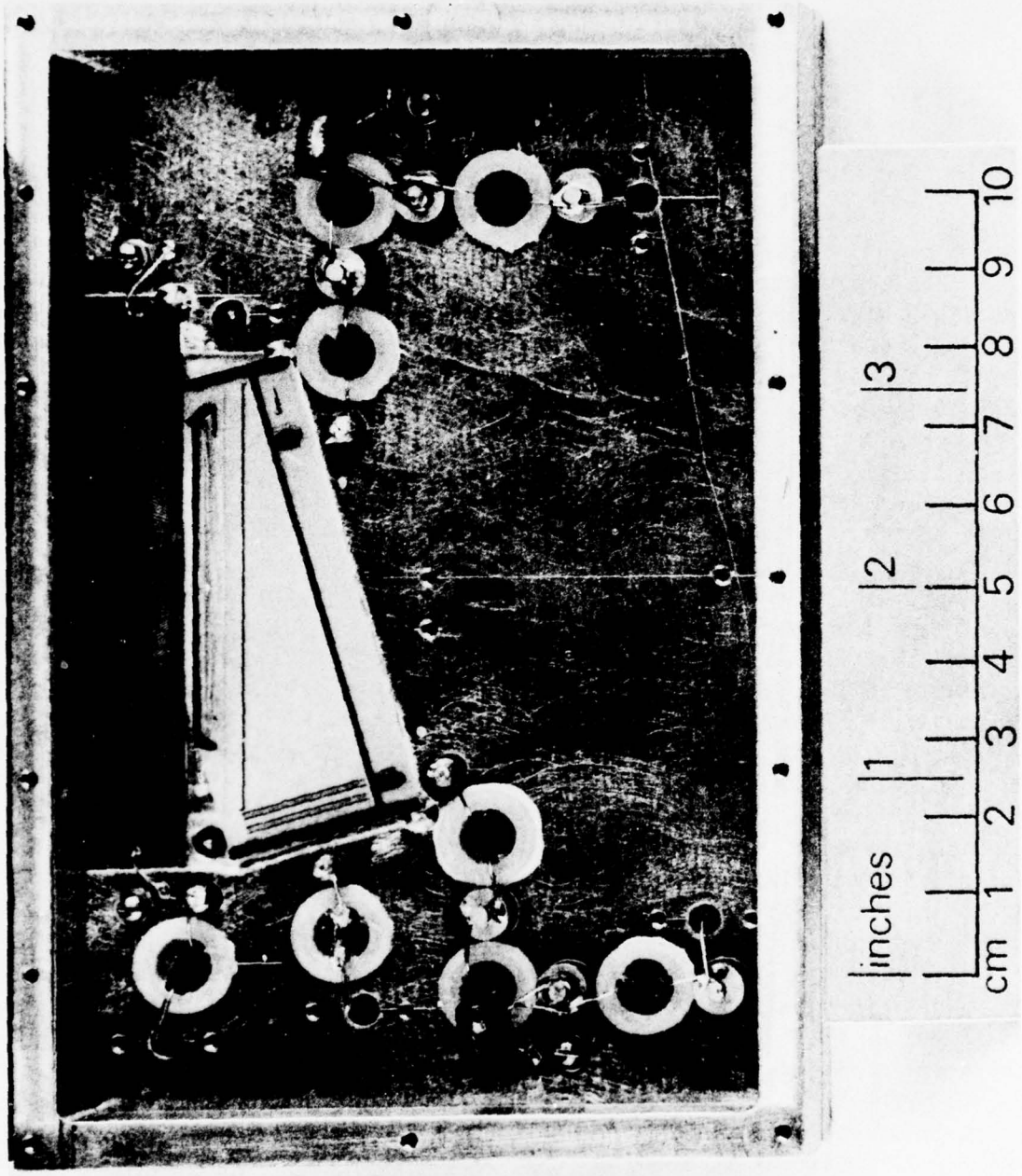
1.1 Program Scope

This report describes an exploratory research and development program which was directed toward the development of the UTRC PSK Diode-Correlator device in a form suitable for high chip rate, electronically programmable, long code PSK signal correlation and encoding. The PSK Diode-Correlator is a hybrid, integrated circuit device which utilizes a Surface Acoustic Wave (SAW) tapped delay line and an attached microelectronic diode and resistor array. PSK signal processing is accomplished by converting the input IF frequency signal (f_1) into a SAW which propagates across the delay line surface toward a series of P, equispaced acousto-electric taps. A second cw wave (f_2) is also excited on the delay line surface which provides a cw reference signal at each tap. RF voltages at frequencies f_1 and f_2 excited at each tap are applied to antiparallel diode-pairs which perform as miniature product mixers with desired product output at $f_3 = f_2 \pm f_1$. The phase polarity of mixer output is selected by choice of diode-pair DC bias current applied through an isolation resistor network. By fabricating the diode and resistor array in silicon-on-sapphire, a microelectronic mixer array is created with exceptionally good tap to tap isolation, efficient mixer operation to at least 500 MHz, and very low power dissipation per tap, typically microwatts. The simplicity of this new tapped delay line processor (Ref. 1), offers the possibility of very high chip rates to 100 MHz and beyond. The electronic flexibility provided by the use of a reference cw input allows a new range of system flexibility in that temperature and doppler frequency perturbations can be electronically offset by feedback control of f_2.

The major goal of the program was to demonstrate that the PSK Diode-Correlator could be built in the form of the 128 chip programmable modules which can be operated in cascade to provide long code PSK signal correlation and encoding with useful system specifications. This goal was satisfied with the successful demonstration of a two module 256 chip cascade having nearly theoretical performance. The two 128 chip PSK Diode-Correlator modules were delivered to NRL personnel at the close of the program. Each module consists of a 128 tap programmable PSK signal processor and a parallel cascade delay channel fabricated on the same delay line substrate. A photograph of one of these modules is shown in Fig. 1-1.

FIG. 1-1

PHOTOGRAPH OF ONE OF TWO 128 TAP PSK DIODE CORRELATOR MODULES DELIVERED UNDER THIS PROGRAM



The scope of this program encompassed two phases:

Phase I: PSK Module Development

Phase I addressed the basic design, construction and operation of the PSK Diode-Correlator module for use in PSK signal correlation and encoding. An equivalent circuit approach was utilized to relate important PSK signal parameters such as input frequency, chip rate, insertion loss, spurious signal level, and dynamic range to the Diode-Correlator delay line and semiconductor diode array parameters. The choice of delay line substrate materials and tap configuration was assessed with the goal of minimizing module insertion loss and spurious signal interference while maximizing module bandwidth. A novel tilted interaction region design on a lithium niobate substrate was adopted which satisfied this goal. A 64 tap prototype PSK Diode-Correlator was fabricated and experimentally evaluated as a programmable PSK signal encoder and correlator. The design of a broadband cascade delay channel allowing minimum signal distortion when cascading several modules for long PSK code processing was also established and experimentally characterized.

Phase II: A Multi-Mode Approach to Long Code PSK Signal Processing

In this phase, two deliverable 128 tap PSK Diode-Correlators were designed and fabricated to demonstrate the principles of the modular approach to long code processing. Minor modifications of the prototype design of Phase I were incorporated with the goal of obtaining a module which could be readily cascaded to process PSK codes of length 1024 or larger.

The two 128 tap PSK Diode-Correlator modules were experimentally operated as a two (2) module cascade subsystem for the correlation and encoding of PSK signals with up to 256 chips. The separate modules of the cascade subsystems were tested and evaluated in several different ways. First, the salient characteristics of the separate modules; bandwidth, insertion loss, spurious signal level, dynamic range were measured. In a second series of experiments, the two modules were set up to perform as a matched pair, 128 chip PSK communication system. One module was used as the encoder while the other served as the correlator. Correlation and encoding characteristics were measured for several different 128 chip codes. In a third series of experiments, the two modules were assembled with a cascade signal frequency amplifier and output signal summer to form a 256 chip cascade susbystem. The characteristics of the subsystem were measured for both signal encoding and correlation.

Theoretical analysis of the ideal module performance and of the effects of system errors when cascading modules for long PSK code processing were also carried out. In particular, the effect of finite module bandwidth on long code correlation performance was assessed.

1.2 Background And Method of Approach

Phase shift key (PSK) modulated waveforms find application in secure and multisubscriber communication systems because of their high matched filter detection probability in the presence of hostile interference and because of the large number of nearly orthogonal sequences available (Refs.2-5). Surface wave matched filters offer a highly competitive approach relative to digital filters particularly where high chip rates, low power consumption, and low cost are significant factors (Refs. 6-15). SAW matched filters have also an important advantage of asynchronous detection capability and therefore reduction in system lock up time. Programmable SAW matched filters are highly desirable for increased system security, and several embodiments are undergoing active development. The capability of code programming and electronic reprogramming in the field after fabrication of the basic unit offers the considerable advantage of cost reduction and multiple system applications.

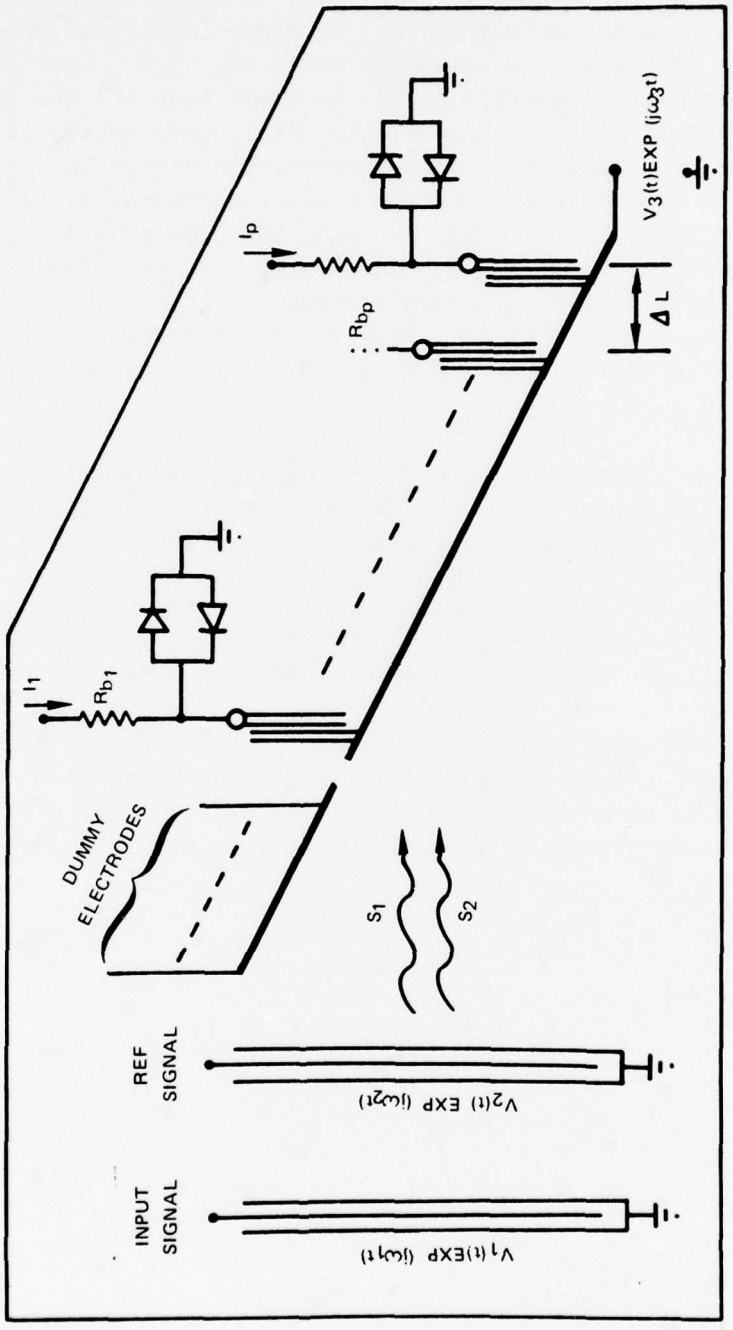
Here, we describe a unique approach to the realization of the programmable SAW PSK matched filter which utilizes the nonlinear interaction between surface waves within a diode tapped delay line. This device differs from other programmable SAW correlators in its simple hybrid construction, requiring only two diodes per tap, low power consumption, large dynamic range and high tap to tap uniformity. In addition, the device is directly ammenable to large time bandwidth PSK signal processing and cascading of individual modules to form a long code programmable matched filter. The nonlinear approach offers additional system flexibility via the electronic adjustability of the device reference frequency allowing direct compensation for phase errors such as Doppler shift or changes in ambient temperature of the delay line.

A schematic diagram of the PSK Diode-Correlator is shown in Fig. 1-2. In common with previously described Diode-Convolver devices (Refs. 16-21), the PSK Diode-Correlator is a hybrid combination of a piezoelectric tapped delay line and an attached silicon-on-sapphire (SOS) integrated circuit diode and resistor array. However, the geometry differs here from previous devices in that two diodes are connected to each tap and the two acoustic waves utilized in signal processing equations both enter the tapped interaction region from the same end of the delay line. This is a consequence of the tilted interaction region geometry which has been found to offer significant advantages of low intertap relfections, low propagation loss and excellent tap uniformity relative to the equivalent in-line tap geometry. The SOS diode and resistor array is located adjacent to the delay line taps and provides an acoustic termination to the propagating waves.

The device operation relies on the nonlinear mixing between input signal and reference waves at frequencies f_1 and f_2 respectively within a bi-phase coded diode tapped interaction region. Phase coding is provided by control of a μW

FIG. 1–2

PROGRAMMABLE PSK DIODE CORRELATOR CONFIGURATION



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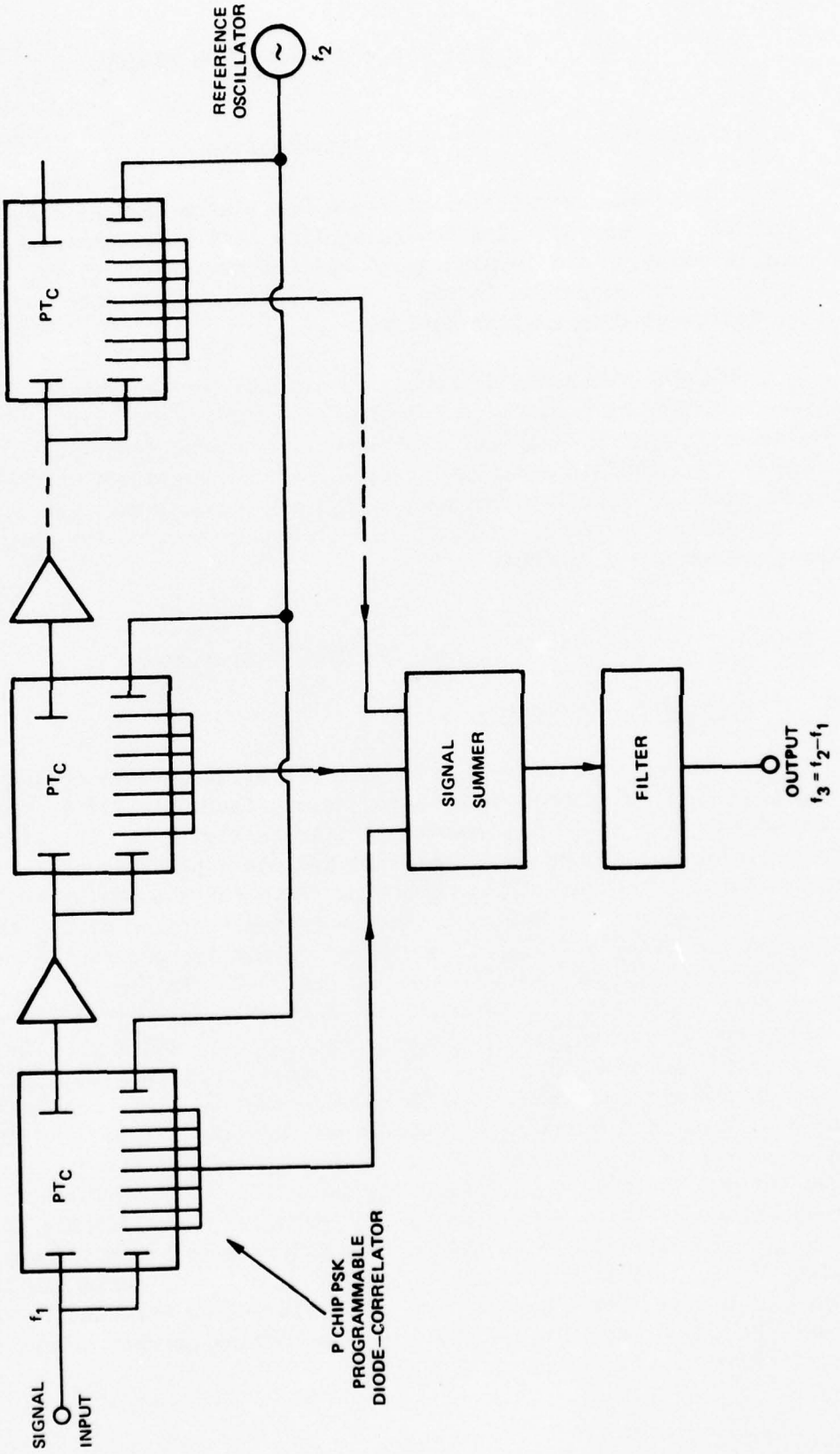
level current to antiparallel diode-pairs connected to each tap; the phase of the nonlinear tap output is altered by 180 degrees upon reversal of the diode bias polarity. The matched filter bi-phase code is thus simply programmed by means of the bias polarity sequence applied to the diode taps, with programming speed of approximately 100 nsec experimentally measured. True correlation is performed between the programmed phase code of the diode taps and the input signal code with preservation of correlation time scale. Since correlation is obtained through a product mixing process, the desired correlation output is received with carrier frequency $f_3 = f_2 \pm f_1$. The basic correlation module may be incorporated within a cascade, as shown in Fig. 1-3, for long PSK code processing. This approach utilizes a parallel delay channel associated with each processor composed of a broadband delay line and loss compensating amplifier. This parallel channel approach has been recently shown (Ref. 22) to be practical for delay line cascades approaching millisecond length with minimum effects of bandlimiting for broadband channel design.

In the following report, the fundamental operation and design of the PSK Diode-Correlator is developed and the fabrication and performance of two 128 tap, 9.8 MHz chip rate programmable devices are described. These devices are operated as programmable PSK signal encoders and correlators and also as a matched pair transmission system. The operation of a two module, 256 chip cascade correlator is reported. System characteristics of high speed programmability, interference rejection and error compensation are also demonstrated.

Theoretical analysis of the cascade circuit and the effects of system errors on long code correlation waveforms is also developed. This analysis is found to predict accurate signal processing of 1024 chip PSK codes by a cascade of eight 128 chip modules identical to the modules developed for this program.

FIG. 1-3

PSK DIODE-CORRELATOR CASCADE CIRCUIT



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2.0 PSK DIODE-CORRELATOR DESIGN

2.1 Introduction

The basic characteristics of Diode-Correlator devices have been developed in earlier programs directed toward applications in electronically variable chirp signal correlation and in high speed Fourier transforms (Refs. 16-21). Here we shall focus our attention to the special features that make the PSK Diode-Correlator different from earlier devices.

A tutorial theory is developed to explain the programmable phase-amplitude characteristics of a single PSK diode-tap. This theory provides an adequate model for calculating the bi-linear coefficient, two port insertion loss, and dynamic range of the complete correlator. The design criteria and trade-offs available in practical PSK Diode-Correlator design are summarized. The electronic adjustability of the device is highlighted; design conditions for doppler and temperature compensation are described.

2.2 The PSK Diode Tap

2.2.1 Fundamental Operation

The salient difference between the PSK Diode-Correlator and earlier diode-coupled, nonlinear tapped delay line devices (Refs. 16-21) is that two diodes are used at each tap as is shown schematically in Fig. 2-1. The simple antiparallel diode connection allows both amplitude and phase polarity of diode-tap nonlinear output to be chosen by simply adjusting the magnitude and sign of the applied dc bias current, I_{bp}. The fact that reversing the sign of I_{bp} simultaneously reverses the phase polarity of nonlinear output is more easily seen by considering the simplified circuit models shown in Fig. 2-2. In Fig. 2-2a, the interdigital delay line transducer-tap is represented by voltage sources V_{g1} anf V_{g2} corresponding to tap excitation at frequencies f_1 and f_2 and a frequency dependent transducer impedance, Z_g. The other P-1 diode taps have shunt admittance Y_{P-1} which is shown in parallel with the output load R_L. Diagnostic experiments on the nonlinear mixing efficiency of the antiparallel diode pair have shown that the major source of nonlinearity is due to the forward biased diode. Thus, if positive bias current is applied in Fig. 2-2a, the circuit may be further simplified, as shown in Fig. 2-2b, to represent the antiparallel diode circuit as a forward biased diode, a capacitance due to the circuit and reverse biased diode, and a current source at the sum or difference frequency $f_3 = f_2 \pm f_1$ which is due to nonlinear mixing. As has been clearly shown in earlier diode correlators having a single diode per tap (Refs. 17-19), the nonlinear mixing current source is given to first order by

FIG. 2-1

SCHEMATIC VIEW OF THE p^{th} TAP IN THE PSK DIODE-CORRELATOR

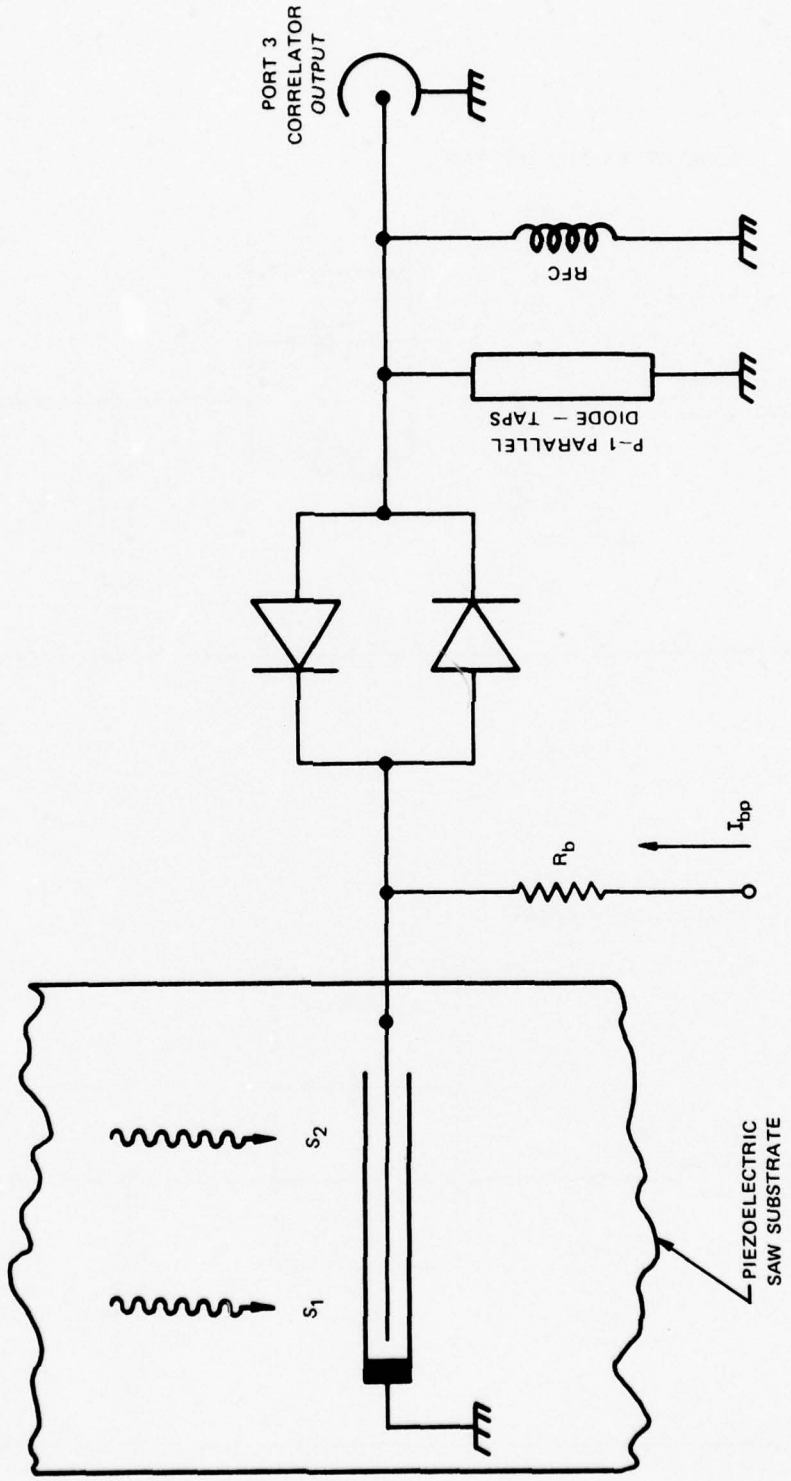

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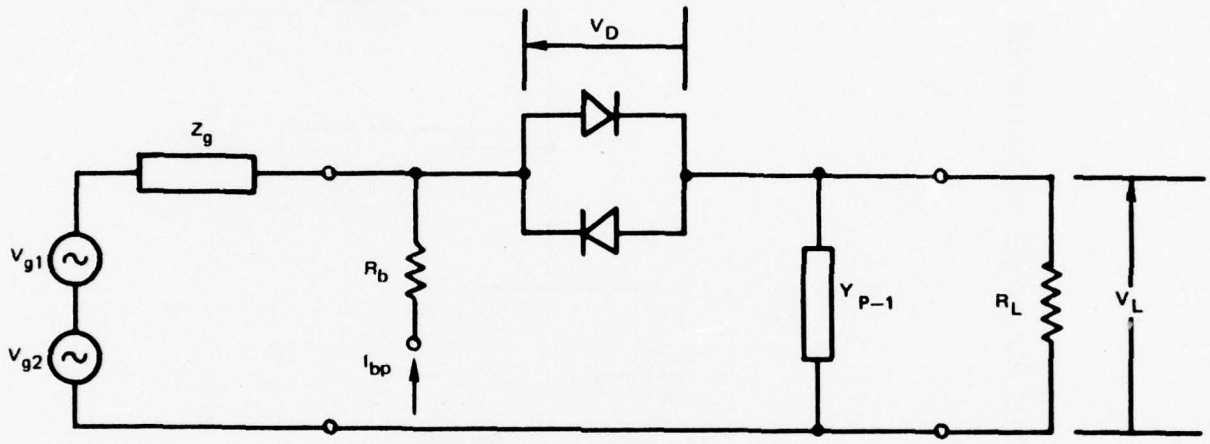
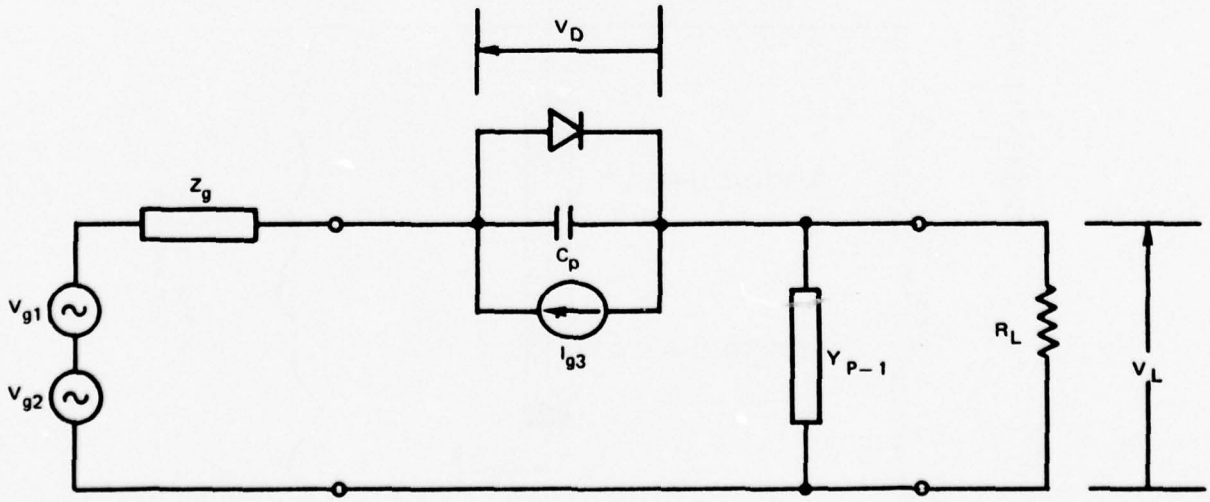
FIG. 2-2

PSK DIODE-TAP EQUIVALENT CIRCUIT MODELS

a) CIRCUIT AT THE p^{th} TAP



b) SIMPLIFIED CIRCUIT



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$$I_{g3} = - (I_{bp}/2V_q^2)\, V_{D1}\, V_{D2} \qquad (2\text{-}1)$$

where V_{D1} and V_{D2} are the ac voltages appearing across the diode pair at f_1 and f_2 and $V_q = n\,kT/q$ is the effective diode junction thermal voltage. Note that the sign of the nonlinear current source is directly proportional to bias current I_{bp}. Thus, if the sign of I_{bp} is reversed, the sign of I_{g3} is also reversed and the phase polarity of mixer output coupled to Port 3 is also reversed. This verifies the simple PSK bias current control described earlier.

The basic quantity to be computed in the theoretical analysis of the PSK Diode-Correlator is the amplitude and phase of Port 3 output due to nonlinear mixing at the pth tap. Once this quantity is known, the operation of a P tap correlator can be described by summing the Port 3 contributions from all P taps. Let us assume that the desired nonlinear output is centered at the difference frequency, $f_3 = f_2 - f_1$. Analysis on earlier Diode-Correlator devices (Refs. 16-19) has shown that the Port 3 output due to the pth diode-tap can be expressed in phasor notation by

$$V_{3P} = H_p\, V_{g1}^{*}\, V_{g2} \qquad (2\text{-}2)$$

where H_p is the Port 3 mixer transfer coefficient for the pth tap. H_p can be derived from Eq. (2-1) with the help of Fig. 2-2b and a few circuit definitions. We shall define

$$Z_{Pi} = Z_{gi} + Z_{bi} \qquad (2\text{-}3)$$

as the pth tap series impedance when evaluated at frequency f_i. The impedance Z_{bi} is the total series impedance of the antiparallel diode pair. Z_{bi} is well represented by

$$Z_{bi} = [g_b + j\,\omega_i\, C_D]^{-1} \qquad (2\text{-}4)$$

where $g_b = I_{bp}/V_q$ is the dynamic conductance of the forward biased diode. The shunt admittance due the other P-1 diode-tap will, in general, have a series representation,

$$Y_{(P-1)i} = \sum_{\substack{n=1 \\ n\neq p}}^{P} (1/Z_{ni}) \qquad (2\text{-}5)$$

because Z_{bi} and Z_{pi} vary with bias current. It will also be convenient to define a tap load impedance Z_{Li} which is the parallel combination of $Y_{(P-1)i}$ and $G_L = 1/R_L$. Further, we shall define the total shunt admittance Y_{Pi} due to all P diode taps as

$$Y_{Pi} = \sum_{n=1}^{P} (1/Z_{ni}) \qquad (2\text{-}6)$$

With these definitions, one may show that H_p is given by

$$H_p = \frac{(I_{bp}/2V_q^2)\, Z_{b1}\, Z_{b2}\, Z_{b3}}{(Z_{p1} + Z_{L1})\,(Z_{p2} + Z_{L2})\, Z_{p3}\,(Y_{p3} + G_L)} \tag{2-7}$$

Thus, H_p is completely defined in terms of the diode-tap circuit parameters. Note that all quantities which vary with diode-tap bias I_{bp} are given a subscript p.

For later comparison with diode-tap acoustic driving power levels, it will be useful to express the voltage generators V_{gi} in terms of the available acoustic power that they represent. Since interdigital transducer-taps are bidirectional and we assume peak voltages in all equations, the relation between tap generator voltage and acoustic driving power is

$$P_{ai} = |V_{gi}|^2 / 4 R_{ai} \tag{2-8}$$

where R_{ai} is the tap radiation resistance at frequency f_i. Consequently, the Port 3 nonlinear output due to excitation at the pth tap can be written,

$$V_{3P} = 4 H_p \sqrt{R_{a1} R_{a2} P_{a1} P_{a2}} \tag{2-9a}$$

and the output power

$$P_3 = |V_{3p}|^2 / 2R_L \tag{2-9b}$$

Finally, for convenience in later analysis, it will be helpful to define a relative tap output coefficient g_p which is normalized to unity at a specific value of tap bias current, I_{bo}. Thus,

$$V_{3p} = A_o\, g_p \tag{2-10}$$

where

$$A_o = 4 \sqrt{R_{a1} R_{a2} P_{a1} P_{a2}}\, H_o, \tag{2-11}$$

$$H_o = H_p\,(I_{bp} = I_{bo}) \tag{2-12}$$

and

$$g_p = H_p / H_o \tag{2-13}$$

2.2.2 Characteristics of SOS Diode Arrays for PSK Delay Line Applications

The active switching elements of the PSK Diode-Correlator utilize an integrated circuit array of antiparallel diode pairs and their associated bias resistors. Silicon-On-Sapphire (SOS) has been chosen for the substrate material in order to provide high diode isolation and to simplify the thin film resistor fabrication. The two inch SOS starting wafers are characterized by a one micron thick n type silicon film with carrier concentration of 10^{16} cm^{-3} and 3 ohm-cm resistivity. The detailed fabrication process for these and similar arrays developed earlier for electronically variable radar applications have been previously reported (Refs. 19-20).

A photograph of a portion of the completed diode and resistor array is shown in Fig. 2-3. The n^+ cathodes of the diodes in the upper row are connected to a common aluminum electrode, as are the p-type anodes of the diodes in the lower row. By electrically shorting the upper and lower common electrodes togerther, the antiparallel diode array is obtained with centrally located p-type bias resistors. For the 128 tap devices considered here, the .010" element spacing requires a 1.3" array length possessing highly uniform diode and resistor characteristics. This requirement has been satisfied with measured diode characteristics uniform to $\pm$ 1/2 percent and typical bias resistors R_b = 3000 ohms $\pm$ 6 percent.

The dc current voltage characteristic of a PSK diode pair, as observed from the bias port, are given in Fig. 2-4. Note the excellent symmetry of these characteristics about the voltage origin. Highly symmetric characteristics are important for achieving balanced carrier PSK output.

2.2.3 Experimental Tap Nonlinear Characteristics

From Eq. 2.1, the phase of the nonlinear output from a single tap is theoretically switched by 180° by reversing the polarity of the dc bias current, I_{bo}, applied to the antiparallel diode pair. The phase reversal accuracy of a single tap test circuit was determined quantitatively by using an HP 8405A vector voltmeter and a coherent cw phase reference signal. The tap circuit consisted of a single SOS diode pair with input signals at f_1 = 70 MHz and f_2 = 100 MHz coupled through 1 pf capacitors to simulate acoustic wave excitation. The phase of the difference frequency output at f_3 = 30 MHz was then compared with a coherent phase reference. The resulting change in phase of the tap output when the bias polarity was switched is shown in Fig. 2.5a as a function of the magnitude of the normalized dc bias current $|I_{bp}/I_{bo}|$, where I_{bo} = .04 ma is the bias required for maximum nonlinear output amplitude at input power levels of P_1 = 0 dBm and P_2 = 20 dBm applied to the input capacitors. Phase reversal accuracy is seen to be within 0.5 degrees over the two decade bias range of $.025 \leq |I_{bp}/I_{bo}| \leq 2.5$. A switching speed of approximately 100 nsec was also measured.

FIG. 2-3

SOS DIODE ARRAY FOR PSK APPLICATION

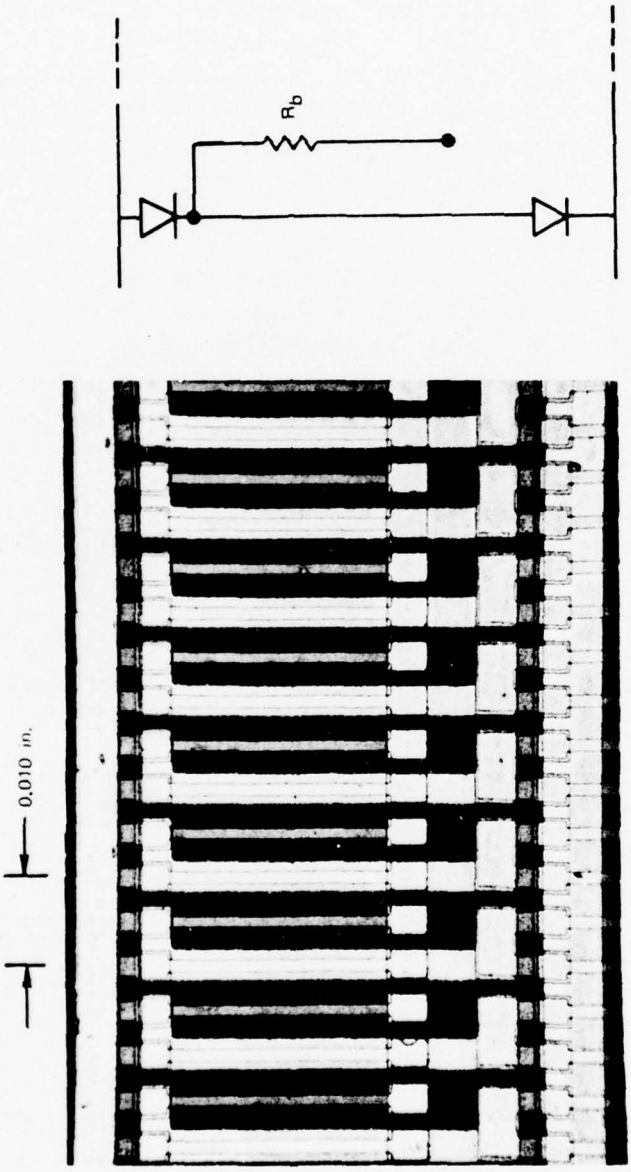


FIG. 2–4

SOS PSK DIODE–PAIR CURRENT–VOLTAGE CHARACTERISTICS

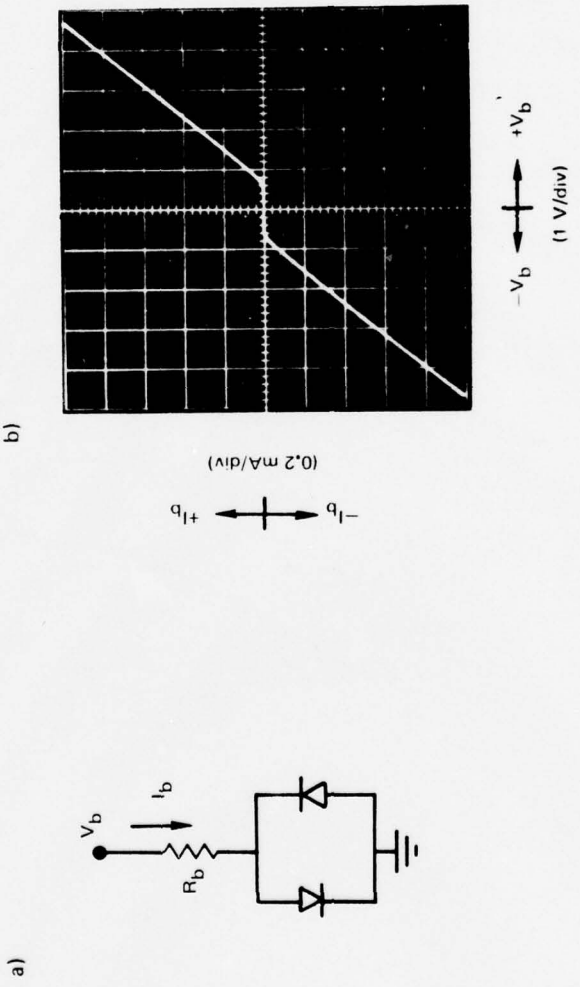
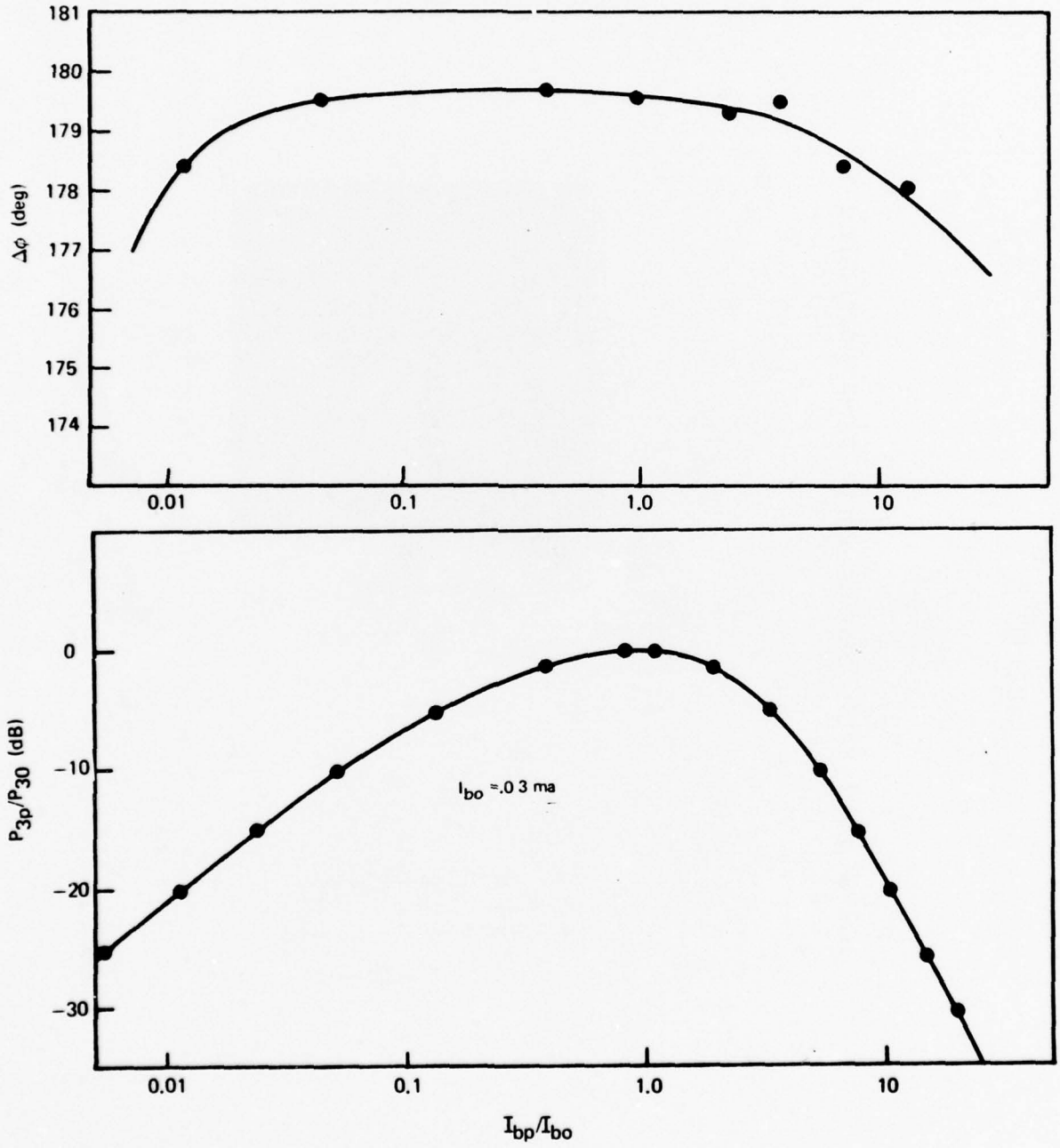


FIG. 2-5

SINGLE TAP MEASUREMENTS OF PHASE REVERSAL AND POWER DEPENDENCE ON BIAS CURRENT



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In the present application only phase programming is required so that all taps are biased at the same dc level $|I_{bp}| = |I_{bo}|$. Tap amplitude programming is also possible by varying the bias amplitude. From Eq. 2-1, a linear relationship between nonlinear output current and dc bias current is predicted at small dc bias. At larger bias, it can be shown (Ref. 19) that the output current is proportional to the inverse square of the dc bias current. The experimental dependence of the relative output power P_{3p}/P_{30} on normalized bias current, $|I_{bp}/I_{bo}|$, for a single dual diode SOS delay line tap is shown in Fig. 2.5b where P_{30} corresponds to the maximum power generated at $I_{bp} = I_{bo}$. These measurements were performed using a dummy tap on one of the two 128 tap PSK Diode Correlators, M-229, with electrical input powers of $P_1 = P_2 = 10$ dBm and $I_{bo} = .03$ ma. The predicted output dependence on bias current is closely followed in both high and low bias ranges with a single tap output dynamic range of greater than 30 dB observed.

2.3 Device Configuration and Design Parameters

As shown in Fig. 1.2, both signal and reference input waves are launched at the same side of the diode tapped, nonlinear interaction region. A slanted tap configuration (Ref. 23) was adapted which differs from the in-line tap geometries used in previous Diode-Correlators (Refs. 16-20). The prior in-line tap design suffered from excessively high intertap reflection and wave propagation losses because of the large number of electrodes in the acoustic wave path. Even with reflection cancelling eight wavelength fill-in electrodes located between taps (Ref. 24) the in-line geometry on $LiNbO_3$ resulted in losses as high as 0.15 to 0.20 dB per tap for wave frequencies near 100 MHz. Losses of this magnitude result in severe nonuniformity of the interaction and are unacceptable for the present application.

With the slanted configuration, propagation losses and spurious reflections are significantly reduced. Each tap is successively offset in the transverse direction by an amount $\Delta W_t = .004"$ so that the tap width, $W_t = .087"$, is a fraction of the input transducer beam width, $W_0 = 0.61"$. The portion of the input beam intercepting a given tap thus propagates through a reduced number, m, of equivalent in-line taps where $m = W_t/2\Delta W_t = 11$. The reduction in propagation losses is countered by increased input transducer losses since the taps now intercept only a fraction of the input acoustic beam width. However, the overall correlation insertion loss is still reduced relative to an equivalent in-line geometry since the total power division loss for both input and reference waves, given by 20 LOG $W_t/W_0 = 17$ dB, is lower than the in-line propagation losses for 128 taps.

The active taps are preceeded by physically identical dummy taps to provide essentially equal wave propagation characteristics prior to any active tap.

Intertap reflections are minimized by choosing input signal and reference frequencies, f_1 = 71.1 MHz and f_2 = 100.5 MHz and tap spacing, ΔL = .014" such that ΔL is an odd multiple quarter wavelength at both frequencies. Split finger tap electrodes are also utilized to further reduce intertap reflections.

Eighth wavelength fill-in dummy electrodes between taps (Ref. 24) were not used and are in fact undesirable for the slanted tap geometry. Their inclusion would result in severe wavefront tilt at a tap because of the variation in delay at points along a tap width resulting from the linearly decreasing prior metallization pattern. Tap efficiency would be reduced since the wavefront and interdigital tap electrodes would be no longer parallel. However, for the tap design adopted here, with a low metallization to free surface ratio in the propagation path between taps, the wavefront tilt and resulting overall loss in efficiency, has been computed to be less than 3 dB. This loss could be recovered in future work by fabricating the tap electrodes parallel to tilted wavefront.

The difference frequency output voltage at the summing electrode can be written as the summation of the individual tap outputs from Eq. 2-10, as

$$V_3(t)e^{j\omega_3 t} = e^{j(\omega_2 - \omega_1)t} A_o \sum_{p=1}^{P} g_p S(t-t_{01}-t_p)e^{-j(\omega_2-\omega_1)t_p} \qquad (2\text{-}14)$$

where t_{01} is the time delay from the signal input transducer to the first tap, $t_p = (p - 1)\Delta T$ is the delay from the first to the pth tap, $\omega_i = 2\pi f_i$, and $S^p = V_{g1}/|V_{g1}|$. In writing Eq. (2-14), we have assumed equal excitation at each tap resulting from the equal reflection and propagation losses of the slanted electrode geometry. It is this condition which allows undistorted, uniform interaction between the copropagating waves which does not hold for the inline tap geometry. We have neglected the position dependence of free surface attenuation and diffraction losses. For frequencies ≤ 100 MHz, and for wide aperture input transducers considered, these losses contribute less than 0.1 dB/cm on $LiNbO_3$ (Ref. 25) which can be compensated by tap apodization.

The exponential phase term within the summation of Eq. 2-14 is eliminated by requiring that the nonlinear output from all taps add coherently. Phase coherence is met when

$$(\omega_2-\omega_1)t_p = 2\pi n_o \qquad (2\text{-}15)$$

which corresponds to

$$f_2-f_1 = n/\Delta T = n R_c = f_3 \qquad (2\text{-}16)$$

where n_o and n are integers, $n = n_o/(P-1)$ is equal to the number of rf cycles per chip at the difference frequency and R_c is the chip rate. With Eq. 2-15 satisfied, Eq. 2-14 becomes

$$V_3(t) = A_o \sum_{P=1}^{P} g_P \, S(t-t_{01}-t_p) \qquad (2\text{-}17)$$

which represents the correlation between the input signal code and the tap sequence. Because the tap weights are fixed in space, the correlation time scale is preserved.

2.3.1 Insertion Loss

The insertion loss for the Diode-Correlator is a function of the bilinear relationship between the input and reference signal input powers and the port 3 output power,

$$P_3 = F_T \, P_1 \, P_2, \qquad (2\text{-}18)$$

where F_T is a terminal bilinearity coefficient which is a function of both delay line and diode parameters. Maximum output power (and therefore minimum insertion loss between ports 1 and 3) is obtained when the cw reference power is increased to the point where the diodes begin to saturate. The latter condition occurs when the diode ac current becomes equal to the dc bias current. F_T may be defined in terms of the input transducer conversion efficiencies, H_1 and H_2, the acoustic beam splitting and transmission efficiency for the slanted electrode geometry, H_S, and the internal bilinear coefficient, F_I:

$$F_T = H_1 \, H_2 \, H_S^2 \, F_I \qquad (2\text{-}19)$$

For input transducer and tap widths of W_o and W_t respectively, and for transmission through m equivalent in-line taps prior to detection,

$$H_S = \frac{W_t}{W_o} \, (m \, T_p) \, K_T \qquad (2\text{-}20)$$

where T_p is the average acoustic transmission efficiency per tap and the factor K_T represents the effect of wavefront tilt on the conversion efficiency of a tap resulting from the slanted geometry.

From Eqs. 2-9 to 2-13, the internal bilinear coefficient, F_I, defined as the ratio of the output power to the product of the acoustic powers driving the taps, is given by

$$F_I = \frac{P_3}{P_{a1} P_{a2}} = 8 \, P^2 \, | \, H_o \, |^2 \, R_{a1} \, R_{a2} / R_L \qquad (2\text{-}21)$$

at the point of complete overlap and for coherent signal addition from P taps.

2.3.2 Output Dynamic Range

The dynamic range of the Diode-Correlator is determined on the lower limit by noise output at port 3 from the diode array and at the upper limit by diode saturation. The maximum noise output from a single, forward biased diode was found by Watson (Ref. 26) to be

$$P_n = 1.5\ kTB \tag{2-22}$$

where k is Boltzman's constant, T is the Kelvin temperature and B is the bandwidth. Maximum noise output will be obtained when the port 3 output circuit is impedance matched, in which case the noise power delivered to port 3 will be the same as the noise output due to a single diode.

Diode saturation occurs when the diode ac current equals the dc bias current. From Eqs. 2-2 to 2-8, this occurs at acoustic saturation power levels of

$$P_{asi} = | I_{bo}(Z_{gi} + Z_{Li}) |^2 / 4\ R_{ai} \tag{2-23}$$

The ratio of the saturation output power level to the noise level, equal to the dynamic range is then found as

$$D.R. = P_{3s}/P_n = F_I\ P_{as1}\ P_{as2} / 1.5\ kTB \tag{2-24}$$

2.4 Capability For Electronic Compensation of System Errors

2.4.1 Introduction

The phase coherence condition, given by Eqs. 2-15 and 2-16, resulting in coherent addition of the nonlinear output signals at all taps, is perhaps the single most important requirement for achieving maximum peak to sidelobe performance of the PSK Diode Correlator. This is, in fact, true for any linear or nonlinear delay line correlator. Slight chip to chip deviations from phase coherence add cummulatively along the delay line, and in the worst case result in total cancellation of the correlation peak response. The severity of the effect is greatest for PSK signals having high time bandwidth products, since it has been shown (Ref. 27) that the degradation of correlation peak response varies as

$$\frac{V_3(\Delta\varphi)}{V_{3max}} = \frac{\sin(\pi\Delta\varphi)}{\pi\Delta\varphi} \tag{2-25}$$

where $\Delta\varphi$ is the accumulated phase error along the length of the device, equal to the product of the number of chips, P, the number of rf cycles per chip, n, and the fractional phase error between successive chips. Phase errors may result from a number of sources including errors in the signal or in the delay line intertap time delay.

In the following, we shown that the nonlinear mixing process of the PSK Diode Correlator offers an electronic adaptability not directly available in linear delay line devices, for restoration of the correlation peak response in the presence of phase errors.

2.4.2 Doppler and Temperature Compensation

When phase errors are present between the received PSK signal and the correlator taps, such that Eqs. 2-15 and 2-16 are not satisfied, the difference frequency output voltage of Eq. 2-14 takes the form

$$V_3(t) = A_o \sum_{p=1}^{P} g_p \, S(t-t_{01}-t_p) \, e^{-j\Delta\varphi_p} \qquad (2\text{-}26)$$

Where $\Delta\varphi_p$ in the accumulated phase error at the pth tap. This error may result, for example, from departure, $\Delta\omega_1$, from optimum signal frequency due to Doppler shift. The correlator intertap time delay, $\Delta T' = \Delta T + \delta T$, may also be in error due to thermally or mechanically caused variation in the wave velocity or by fabrication errors which add linearly along the delay line. The resulting phase error at the pth tap of the Diode Correlator is related to these variables, assuming small deviations, by

$$\Delta\varphi_p = n\,(P-1)2\pi \left(\frac{\delta\omega_2}{\omega_3} - \frac{\delta\omega_1}{\omega_3} + \frac{\delta T}{\Delta T} \right) \qquad (2\text{-}27)$$

The difference frequency output now occurs at $\omega_3' = \omega_3 + \delta\omega_3$ where $\delta\omega_3 = \delta\omega_2 - \delta\omega_1$. The possibility for offset of the correlator reference frequency has also been included and offers a unique method for directly compensating for the system phase errors within the basic module. For example, Doppler shift of the received signal is directly cancelled by an equal offset of the cw reference frequency. Ambient temperature variations may also be compensated, by adjusting $\delta\omega_2/\omega_3 = -\alpha_T \delta T$ where α_T is the thermal coefficient of time delay and δT is the temperature shift (Ref. 28). In addition to compensation for undesirable system deviations, the electronic adjustability also permits detection of signals having intentional variations in frequency allowing the possibility of increased system security or additional system subscribers.

The sensitivity of the PSK Diode-Correlator to the Time Delay errors such as caused by changes in ambient temperature is in itself reduced relative to the equivalent linear SAW correlator. This follows directly from Eq. 2-27 since, n, the number of rf cycles per chip at the difference frequency is less than N, the number of cycles per chip at the signal frequency. This reduction is given by the ratio of rf cycles per chip n/N, equal to ω_3/ω_1.

3.0 EVALUATION OF A PROGRAMMABLE 64 TAP PSK DIODE CORRELATOR

A prototype 64 tap PSK Diode Correlator was fabricated and tested to evaluate the characteristics of the slanted tapped interaction region geometry, described in Section 2.3, and to demonstrate the basic capabilities of the nonlinear PSK encoding and correlation technique. Based upon these tests, modifications to the prototype design were then included, where appropriate, in the design of the two 128 tap PSK Diode Correlators described in Section 4.

3.1 64 Tap Device Parameters

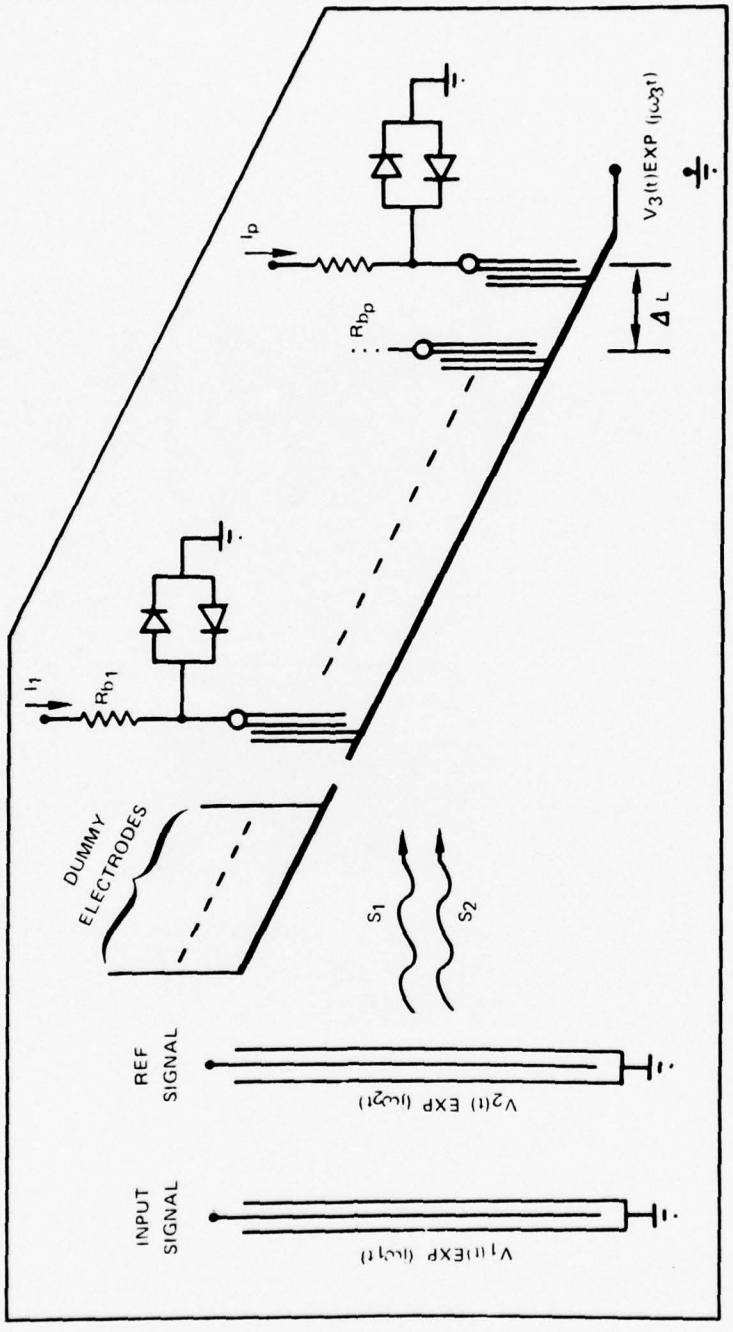
A schematic diagram of the programmable 64 tap PSK prototype correlator is shown in Fig. 3-1. The input and reference signal waves at frequencies f_1 and f_2, respectively, are launched at the same end of the delay line and propagate toward the tapped interaction region. When both signals pass beneath a tap, a nonlinear signal at $f_3 = f_2 \pm f_1$ is generated by means of forward biased diode nonlinearity. The nonlinear signals produced at successive taps may be selected in phase or 180° out of phase depending on the sign of the DC bias current driving the diodes.

As shown in Fig. 3-1, a slanted tap configuration (Ref. 23) is adopted which differs from other geometries used in previous Diode-correlators (Refs. 16 to 21). Each .087 inch aperture tap is offset in the direction of the delay line width as well as in the wave propagation direction, and overlaps a fraction of the input waves. The active taps are preceded by physically identical dummy electrodes to provide essentially equal attenuation at any tap along the array. The taps consist of N = 1 transducers having split $\lambda/8$ electrodes (Ref. 24) with center frequency of 85 MHz and tap spacing ΔL = .014 inch. For Y cut Z propagating lithium niobate, this corresponds to a chip rate R_c = 9.81 MHz. Intertap reflections are minimized by choosing f_1 = 71.1 MHz and f_2 = 100.5 MHz such that ΔL is an odd multiple quarter wavelength at both frequencies. This interaction region design offers advantages of low propagation loss and spurious reflection level by reducing the number of taps effectively seen by a single portion of the beam. The difference frequency nonlinear output signal is taken at the common bus electrode. Tap to tap phase coherence is satisfied with f_3 = 29.4 MHz = n R_c where n = 3 cycles per chip at the difference frequency.

The prototype 64 tap PSK correlator fabricated as described is shown in Fig. 3-2. Note that the integrated circuit silicon-on-sapphire (SOS) diode and resistor array is located in close proximity to the slanted tap electrodes to minimize bond wire length and tap cross talk. As the SOS is now an acoustic termination, both input and reference signal transducers must be located at a common end of the delay line. These transducers are series tuned and are composed of N_1 = 2.5 and N_2 = 6 interdigital period of split $\lambda/8$ electrodes respectively with an acoustic beam width of 0.36 inch. An additional input transducer has been included for diagnostic purposes.

FIG. 3-1

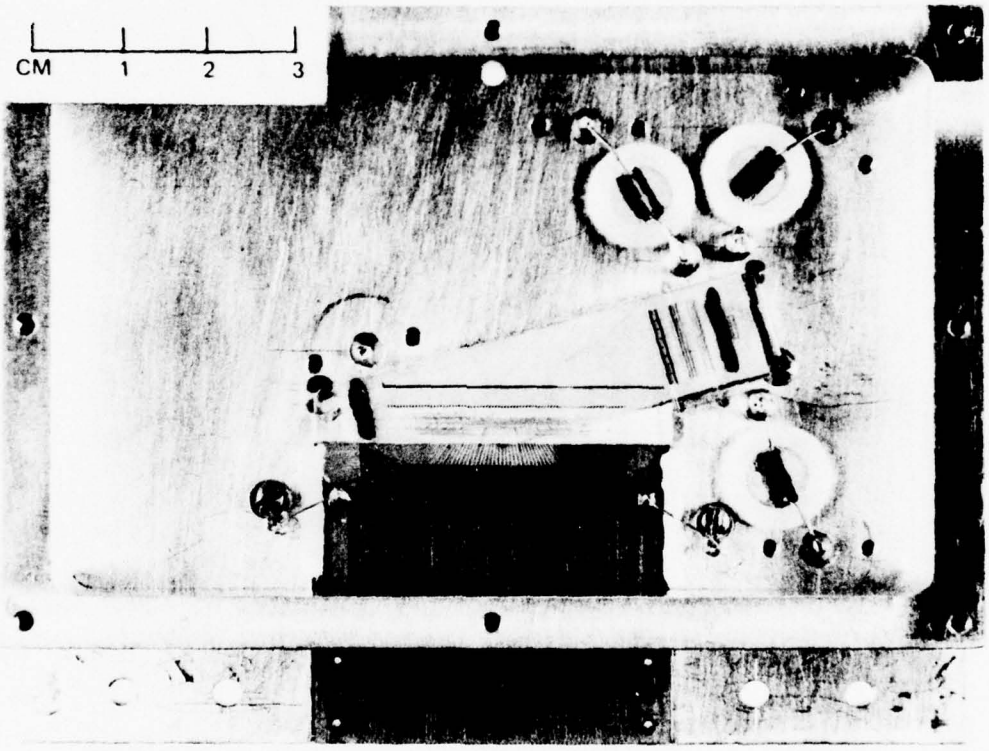
PROGRAMMABLE PSK DIODE CORRELATOR CONFIGURATION



76 10 10-1

FIG. 3-2

UTRC 64 TAP PROGRAMMABLE PSK CORRELATOR



As shown in Fig. 3-2, a compact, special purpose printed circuit board connector was developed to provide dc bias to the individual diode taps. Matching connectors, hard wired with the desired positive and negative bias codes, allow quick programming of the tap phase sequence.

The nonlinear output at f_3 = 29.4 MHz from the 64 tap device operating at f_1 = 71.1 MHz and f_2 = 100.6 MHz is seen in Fig. 3-3. The triangular output waveform is the correlation between the 6.4 us input signal and the tap weight coefficients for equal bias current applied to each tap. High spurious signal suppression is observed in the lower trace of Fig. 3-3 in which the output is attenuated by 60 dB to equal the spurious signal level.

Figures 3-4 and 3-5 demonstrate the device efficiency and linearity between output and input electrical power levels when operated with tap bias I_{bp} = 0.017 ma for maximum efficiency. A maximum output power of P_3 = -16 dBm for $P_1 = P_2$ = 24 dBm is obtained. From Fig. 3-4, deviation from linearity, which represents the onset of saturation, occurs at $P_1 = P_2$ = 10 dBm. A minimum two port insertion loss of 35 dB is observed from Fig. 3-5 for P_2 = 24 dBm with an output signal dynamic range exceeding 60 dB.

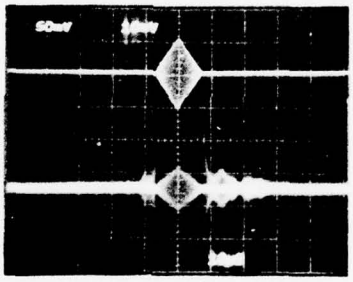
3.2 Operation as a 64 Chip PSK Signal Encoder

Programmable PSK signal encoding is accomplished by applying positive and negative bias current along the tapped diode array for the desired phase coded sequence. The tap phase is then scanned using a long reference signal and a short input signal, equal in width to the chip length. The performance of the 64 tap prototype module as a PSK signal encoder is shown in Fig. 3-6 for input and reference signal power levels of 24 dBm. In the upper photograph, all chips are programmed for constant phase, while in the middle photograph the taps are programmed in a pseudo-random bi-phase sequence. All but one of the 64 taps are found to function with tap #43's inactivity most likely caused by a poor wire bond.

Small variation in amplitude between chips was observed. However, this variation was greatly reduced from that found for previous Diode-Correlators of similar tap count, but having a linear tap configuration. The improved amplitude uniformity results from reduced propagation loss and reflections provided by the slanted electrode design. Further improvement in tap characteristics were incorporated in the 128 tap correlator design as discussed in Section 4. True phase reversal between chips is seen in the lower photograph of Fig. 3-6 by comparing a portion of the 64 chip PN sequence with a cw phase reference. The observed output power level of the encoded signal is reduced from the correlation output level of Figs. 3-3 and 3-4 by the ratio $(1/P)^2$ or 20 log 1/64 = -37 dB. The encoded output level is therefore -53 dBm.

PSK-64

CONVOLUTION AND DYNAMIC RANGE



CONVOLUTION OUTPUT FOR RECTANGULAR INPUTS

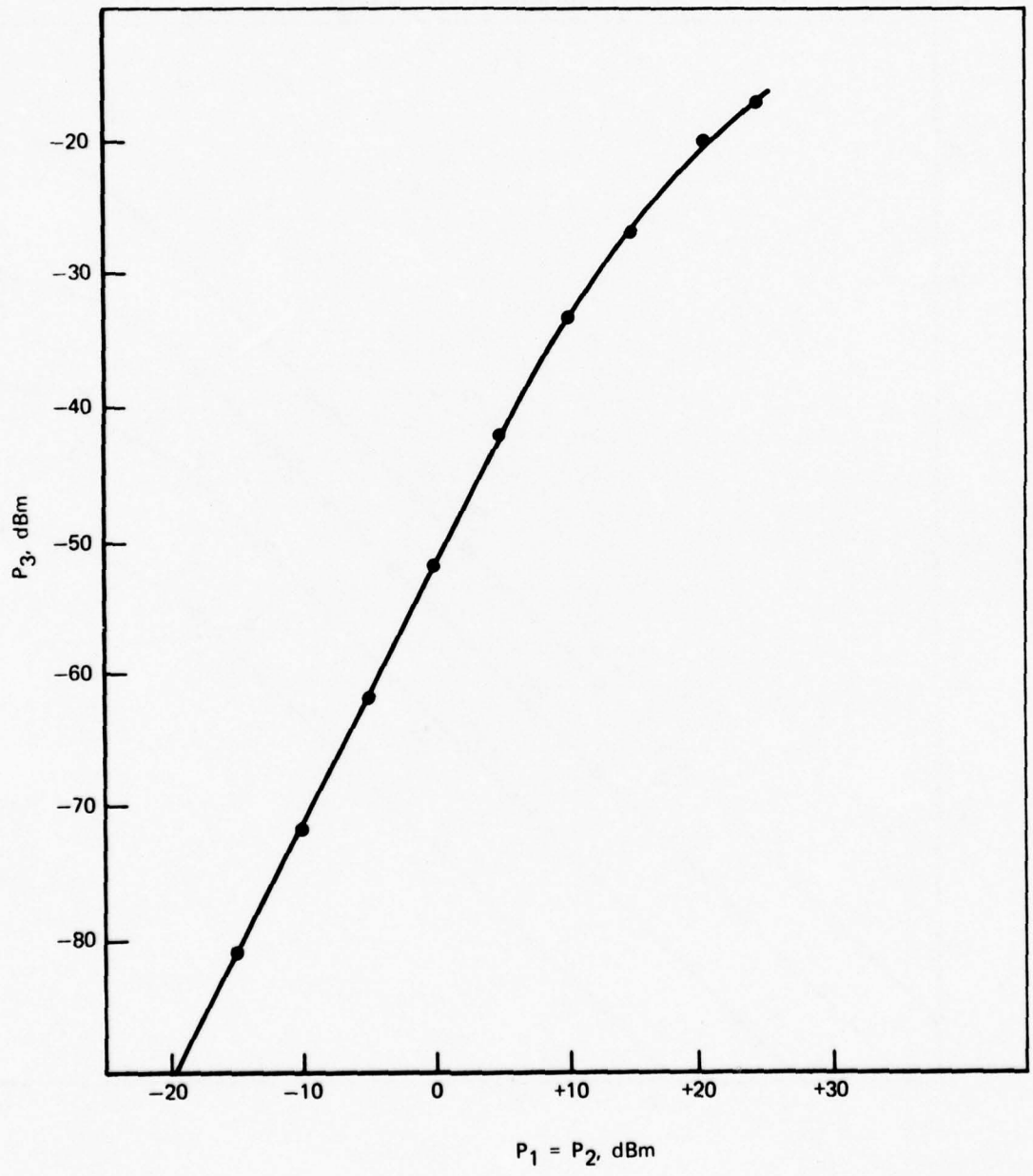
DOUBLE EXPOSURE SHOWING 60 dB DYNAMIC RANGE

FIG. 3–4

PSK–64

CONVOLUTION OUTPUT VERSUS $P_1 = P_2$

I_{bp} = 0.017 mA, f_1 = 71.1 MHz, f_2 = 100.6 MHz

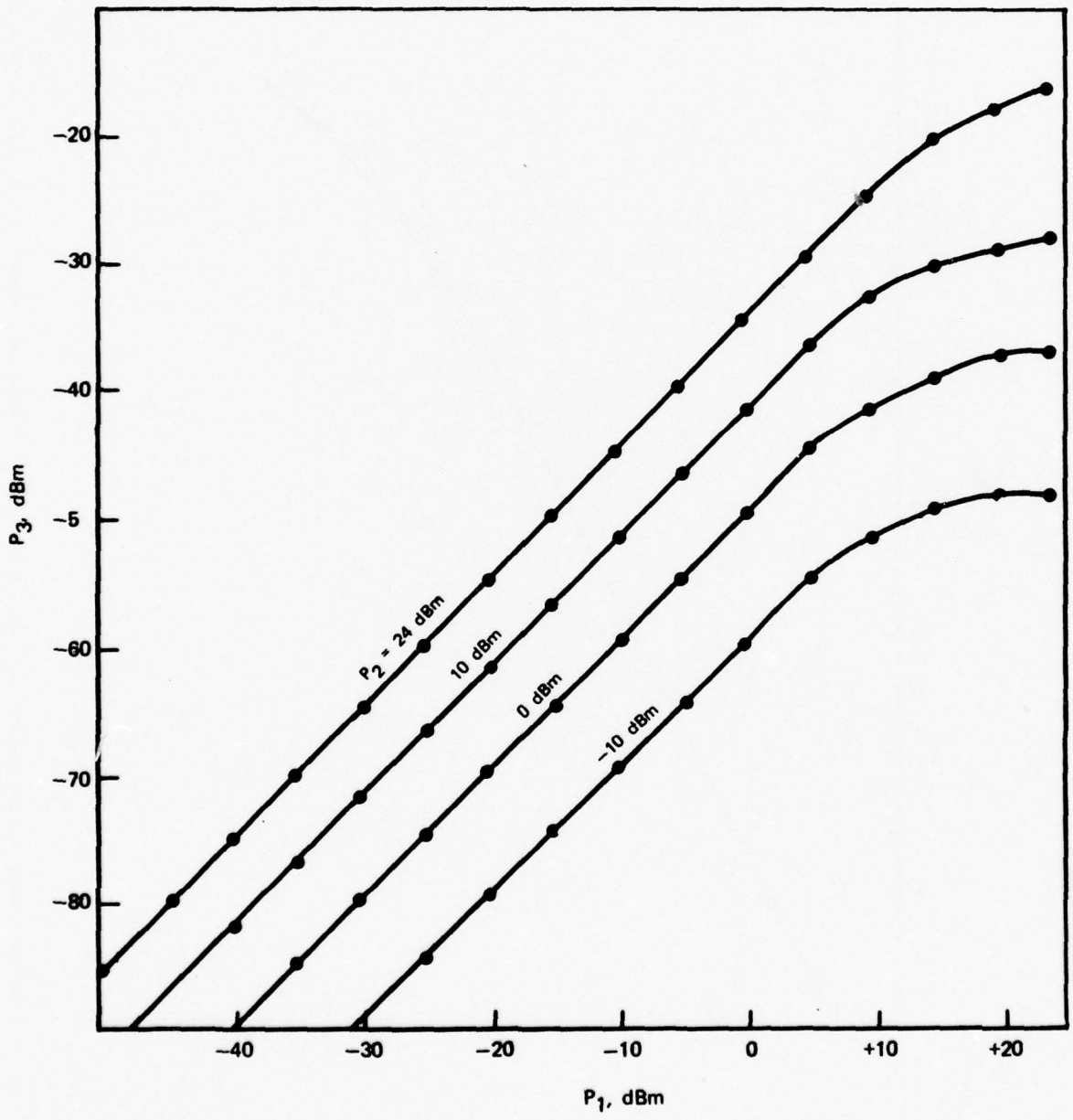


R10–165–10

PSK–64

CONVOLUTION OUTPUT VERSUS INPUT

I_{bp} = 0.017 mA, f_1 = 71.1 MHz, f_2 = 100.6 MHz

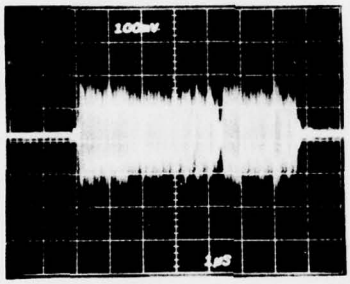


R10–165–1

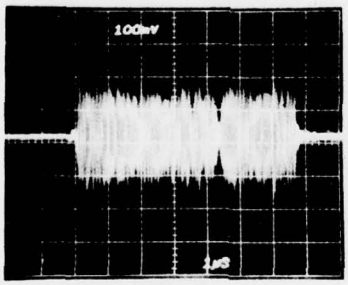
PSK–64

ENCODED WAVEFORMS AT f_3 = 29.5 MHz

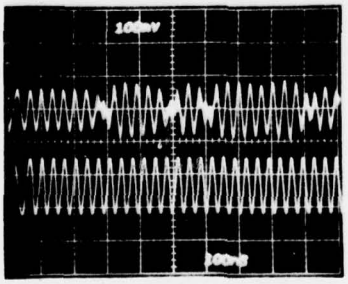
f_1 = 71.1 MHz, f_2 = 100.6 MHz, $P_1 = P_2$ = +24 dBm



ALL TAPS
EQUAL PHASE



TAPS BIASED IN
BI–PHASE PN SEQUENCE



PORTION OF ENCODED
BI–PHASE SEQUENCE

cw PHASE REFERENCE

3.3 Operation as a 64 Chip PSK Signal Correlator

Correlation of an externally generated PSK sequence with the programmed tap sequence of the PSK Diode-Correlator has been evaluated using the circuit of Fig. 3-7. The external PSK sequence of bit length T and is generated using a programmable Hewlett Packard 8016A pulse generator with chip rate adjusted equal to R_c of the Diode Correlator. Since the pulse generator provided a continuous, repetitive 64 chip sequence, the reference signal at f_2 was pulsed on and off for equal times, T, and timed to spatially overlap the signal wave propagation along the interaction region. The correlation output at f_3 produced over time 2T by this technique is of course identical to that produced using a cw reference signal and a single nonrepetitive input bit.

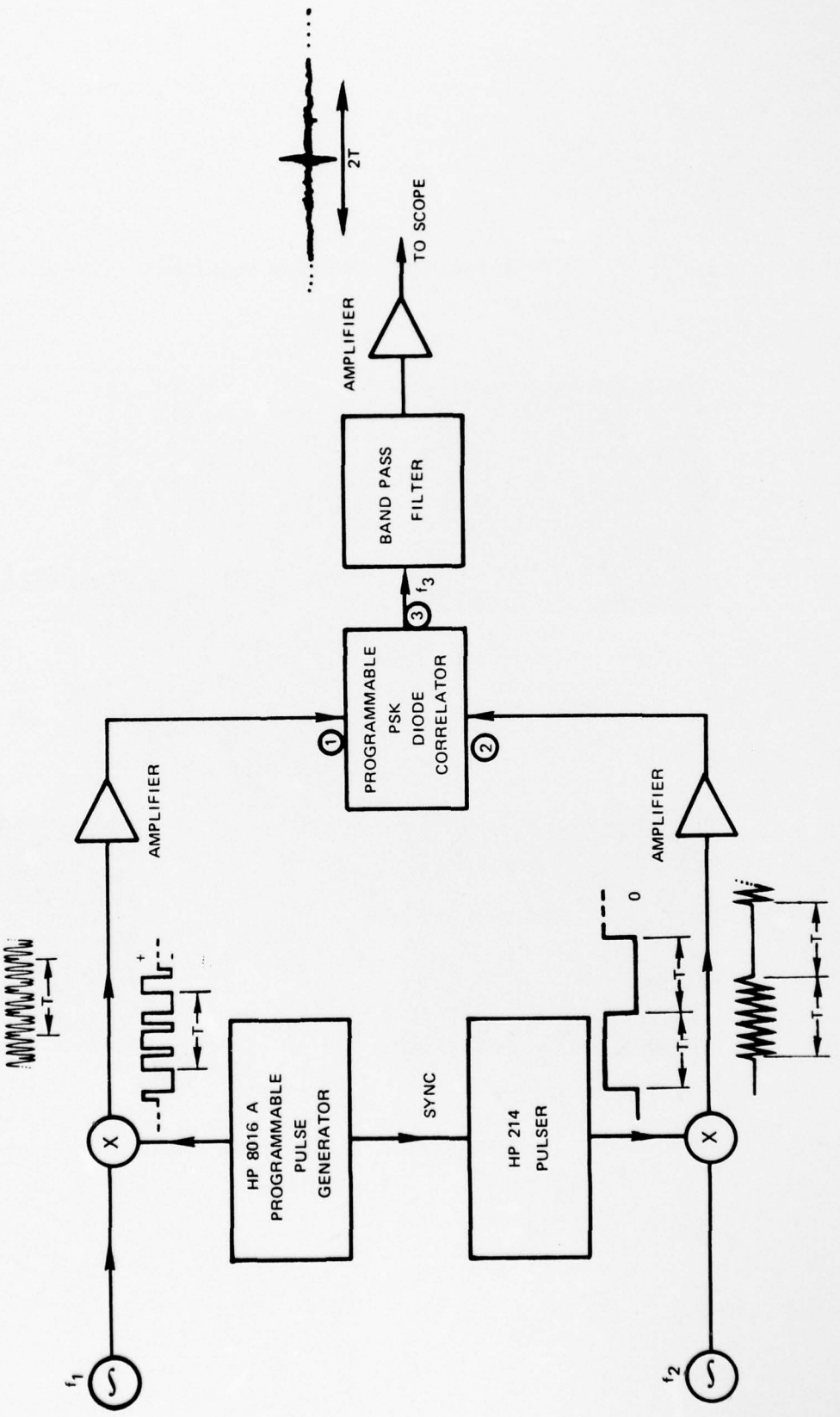
Figure 3-8 shows the correlation results for a 64 chip pseudo-random sequence of bit length T = 6.54 μsec and chip rate of 9.81 MHz. The correlation output of the 64 tap module programmed with the matching code is seen to closely resemble the theoretical output calculated for this PN sequence both in sidelobe structure and peak to sidelobe ratio of 14 dB. Note also the clean spectral response and true nulls observed in the expanded output waveform.

The noise like appearance of the PN input sequence to an unmatched correlator is shown in Fig. 3-9 with all the taps programmed with constant phase.

Figure 3-10 demonstrates the matched correlator response to a 13 chip bi-phase Barker code input. The input chip rate of 1.96 MHz corresponds to an overlap within the device of 5 taps per chip. The 20 dB peak to sidelobe ratio compares well with the 22.8 dB ratio expected for this sequence, however, some distortion in sidelobe structure is apparent.

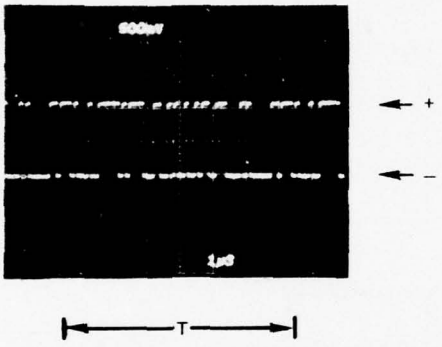
FIG. 3-7

CIRCUIT DIAGRAM FOR PROGRAMMABLE PSK CORRELATION EXPERIMENTS

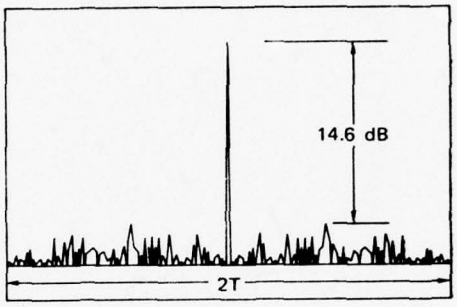


R10-165-5

64 CHIP PSEUDO–RANDOM SEQUENCE CORRELATION

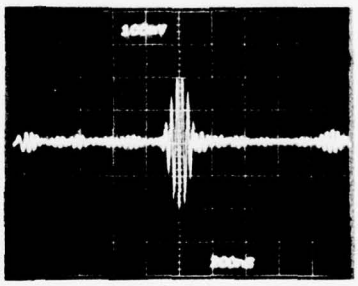


INPUT PN CODE
9.8 MHz CHIP RATE



THEORETICAL CORRELATION

PEAK/SIDELOBE
RESPONSE

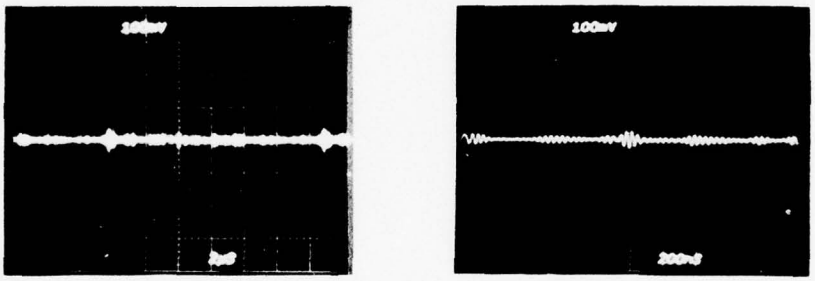


DEVICE OUTPUT WITH TAPS MATCHING INPUT PN CODE

$P_1 = -10$ dBm, $P_2 = +15$ dBm

FIG. 3–9

64 CHIP PSEUDO–RANDOM SEQUENCE INPUT

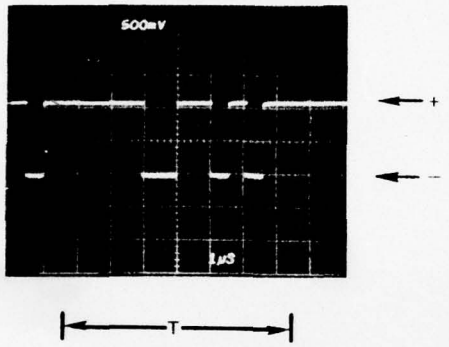


DEVICE OUTPUT WITH ALL TAPS AT SAME PHASE

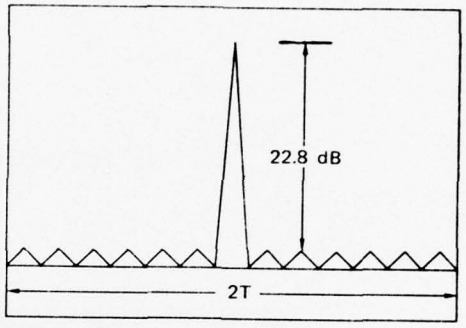
P_1 = –10 dBm, P_2 = +15 dBm

FIG. 3–10

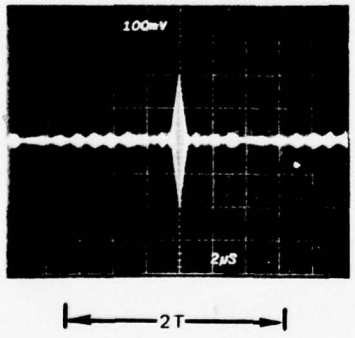
BARKER CODE CORRELATION



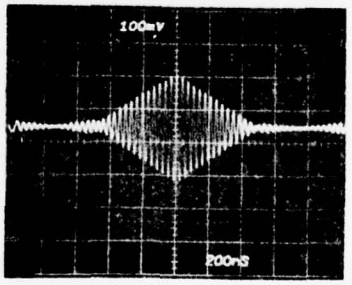
INPUT 13 CHIP BARKER CODE
1.96 MHz CHIP RATE



THEORETICAL CORRELATION
OUTPUT



20 dB
PEAK/ SIDELOBE
RESPONSE



DEVICE OUTPUT WITH TAPS MATCHING INPUT CODE

P_1 = –10 dBm, P_2 = +15 dBm

4.0 EVALUATION OF A MATCHED PAIR OF PROGRAMMABLE 128 TAP MODULES

4.1 128 Tap Device Parameters

Two 128 tap modules were fabricated and delivered under the program. Photographs of these modules are shown in Figs. 4-1 and 4-2. The 2.5 x 1 x .040 inch yz lithium niobate delay line of each module was mounted within an oversize aluminum chassis using a compliant silicon adhesive. Both the signal processor and cascade delay channel are fabricated on the same substrate for two major reasons. First, substrate misorientation and mask alignment errors, if present, are the same for both acoustic paths so that the relative time delay between channels is preserved. In addition, thermal variations in the propagation velocity and delay line lengths are precisely equal for both paths provided that thermal gradients along the substrate are absent. The two sections were physically isolated from each other by applying acoustic dampening tape between acoustic channels. The cascade delay channel transducers were tuned using broadband networks to minimize bandlimiting when cascading modules for long PSK code processing. Characteristics of the delay channel design are discussed in Section 5.2.

The 128 tap correlator design is similar to that of the 64 tap prototype device described in Section 3.1. Signal and reference input transducers comprising ports 1 and 2 respectively were series tuned at frequencies f_1 = 71.1 MHz and f_2 = 100.5 MHz respectively. Both have a split $\lambda/8$ electrode design with N_1 = 2.5 and N_2 = 6 interdigital periods and a 0.63 inch acoustic aperture. The delay line tap transducers are operated untuned, with a center frequency of 85 MHz and have N = 1/2 interdigital periods consisting of 4 split ($\lambda/8$) electrodes. This modification from the prototype 64 tap correlator design which had N = 1 split electrode taps, followed from experiments involving 4 additional diagnostic devices. These devices were identical except for the number of eight wavelength electrodes per tap. Tap designs of N = 1 and 1/2 interdigital periods with and without the addition of fill in, intertap electrodes were investigated. Diagnostic experiments clearly demonstrated the superiority of the N = 1/2 design chosen without fill in electrodes for reduced wave attenuation, wavefront phase distortion and intertap reflections.

The taps were spaced by ΔL = .014 inch corresponding to a chip rate of R_c = 9.81 MHz. This spacing was chosen equal to an odd number of quarter wavelengths at the signal and reference frequencies so that acoustic reflections would cancel. The tilted electrode configuration of Fig. 1-2 was employed with transverse tap to tap offset of .004 inch. With a tap aperture of .087 inch, a given tap will experience decreasing reflections from 22 following taps, or only, 11 on the average. Wave propagation loss is also reduced relative to an equivalent in-line tap geometry. The active tapped interaction region is preceded by 24 dummy taps so that wave propagation characteristics prior to each active tap would be identical. The difference frequency output at $f_3 = f_2 - f_1$ = 29.4 MHz is taken at the common bus electrode comprising port 3. Tap to tap phase coherence is satisfied with $f_3 = n\ R_c$ corresponding to n = 3 cycles per chip at the difference frequency.

FIG. 4-1

CLOSE UP VIEW OF 128 TAP PSK DIODE CORRELATOR MODULE M230

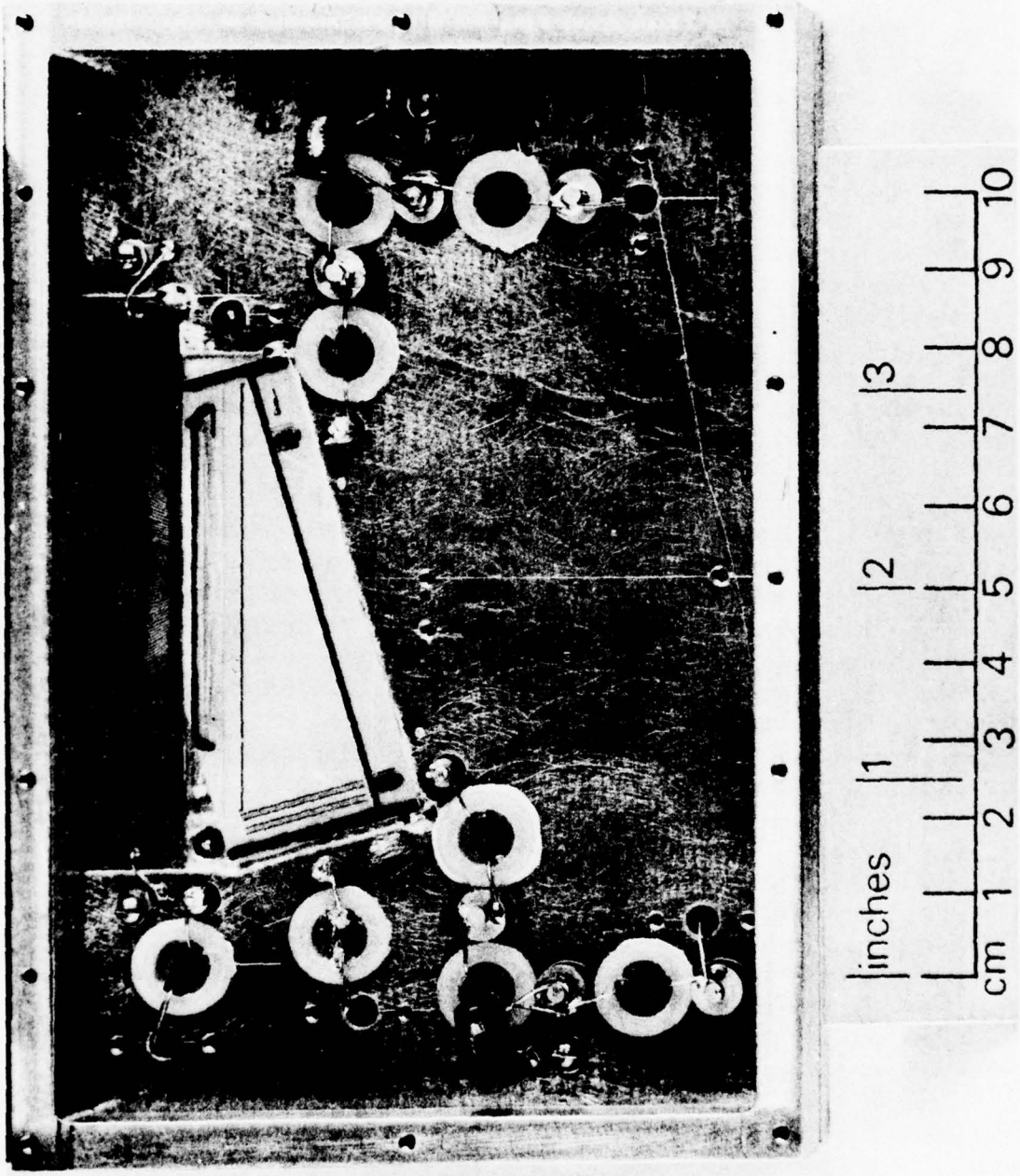
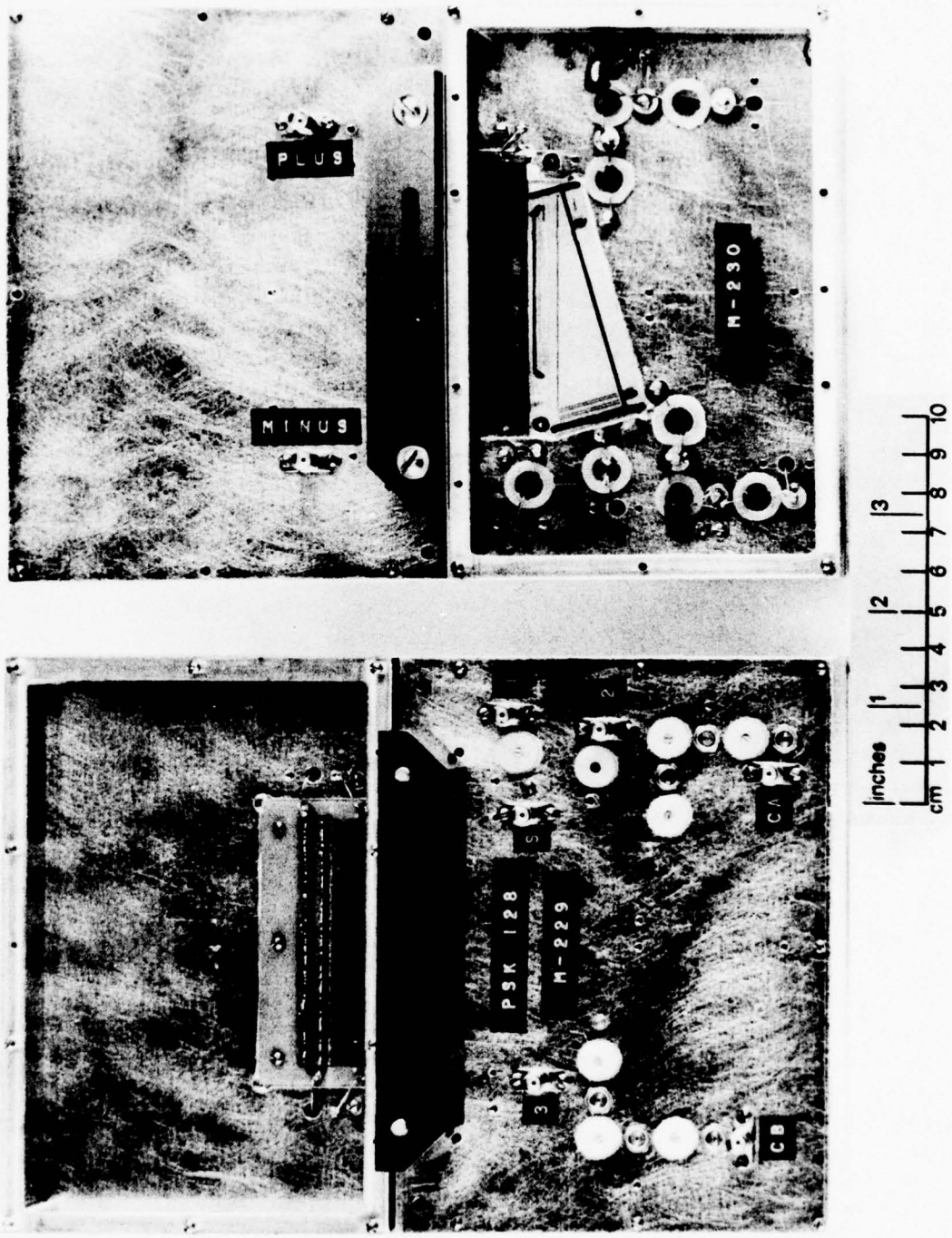


FIG. 4-2

UTRC PROGRAMMABLE 128 TAP PSK DIODE-CORRELATORS

M229 AND M230 WITH CODED BIAS CONNECTORS ATTACHED



Nonlinear mixing of the signal and reference waves occurs within the silicon on sapphire diode array mounted on the delay line adjacent to the tap electrodes. Each nonlinear tap is phase coded by means of the polarity of diode bias current applied through its bias resistor R_{bp} = 3000 ohms.

The SOS diode array elements of the correlator were ultrasonically wire bonded to the adjacent delay line taps using .001 inch aluminum wire. The associated SOS bias resistor array was bonded to the multi-conductor printed circuit board shown in the upper portion of Fig. 4-1. A coded connector was developed to mate with this printed circuit board to provide positive or negative bias to the diode array in the desired sequence. Several connectors were hard wired with different codes to allow quick tap reprogramming.

These connectors are shown attached to the two 128 tap modules in Fig. 4-2. No attempt was made to minimize the overall package dimensions, chosen here for ease of fabrication and handling in the laboratory environment.

The nonlinear characteristics of these devices were measured first by using a pulsed, constant phase 13 μsec input signal, a cw reference signal and equal bias, I_{bp} = 0.02 mA, applied to all diode taps. The triangular correlation between the input and tap cw codes is shown in Fig. 4-3a for device M230. The difference frequency output shown is filtered prior to detection to eliminate undesirable input frequency components. Spurious triple transit suppression of 50 dB is shown in the double exposure of Fig. 4-3b. Direct electromagnetic feedthrough suppression is > 60 dB.

Correlator insertion loss and dynamic range information are shown in Fig. 4-4 where the output power, P_3, is plotted versus input signal power, P_1, for several reference input power levels. Diode tap bias of I_{bp} = 0.02 mA is chosen for maximum nonlinear output under nonsaturating small signal conditions. The bilinear relationship given by Eq. (2-21) is seen to be well satisfied up to the onset of diode saturation output powers. For P_2 = 24 dBm, saturation onset is observed at P_3 = -23 dBm and the maximum saturated output level of P_3 = -18 dBm is found. Correlator insertion loss of 40 dB is found at P_2 = 24 dBm and P_1 levels less than 15 dBm.

Table I summarizes the comparison of experimentally measured correlator parameters for M229 and M230 with theoretical parameter values calculated from the theory described in Section 2.3. The theory accurately models the small signal device performance over the wide tap bias range from 10^{-5} to 1 ma. By assuming that large signal saturation begins when the diode dc bias equals the fundamental f_1, f_2 driving currents, saturation level correlator input and output power levels are estimated which appear to be within 3 dB of actual device performance. Perhaps most outstanding is the 75 dB output noise to saturation level dynamic range.

TABLE I

COMPARISON OF CORRELATOR PARAMETERS

	M229	M230	Theory
f_1(MHz)	71.1	71.1	71.1
f_2(MHz)	100.5	100.5	100.5
f_3(MHz)	29.4	29.4	29.4
v_a(mils/μsec)	137.30	137.31	137.3
Port 1 C.L. (dB)			7.3
B.W. (MHz)			25
VSWR	1.7	1.6	
Port 2 C.L. (dB)			7.6
VSWR	1.9	1.7	
Total Beam Division Loss, H_s^2 (dB)			20
Tap Piezo. Coef. (K^2)			.035
Internal Bilinearity Coef. $F_{I\ opt}$(dBm)	-22	-25	-26
External Bilinearity Coef. $F_{E\ opt}$(dBm)	-57	-60	-60
$P_{3\ SAT}$(dBm)	-24	-26	-27
$P_{1S} = P_{2S}$(dBm)	17	19	19
Dynamic Range (dB)	79	77	75

M230: 128 CHIP CW SEQUENCE CORRELATION

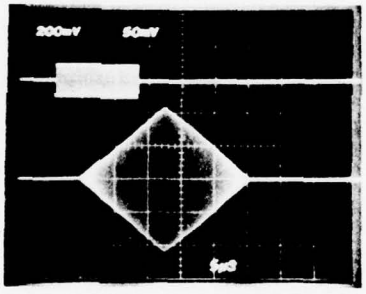
(f_1 = 71.1 MHz, f_2 = 100.5 MHz, f_3 = 29.4 MHz

$P_1 = P_2$ = 24 dBm)

(a)

f_1 INPUT

f_3 OUTPUT



(b)

50 dB DOUBLE EXPOSURE

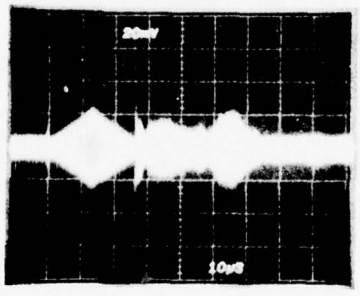
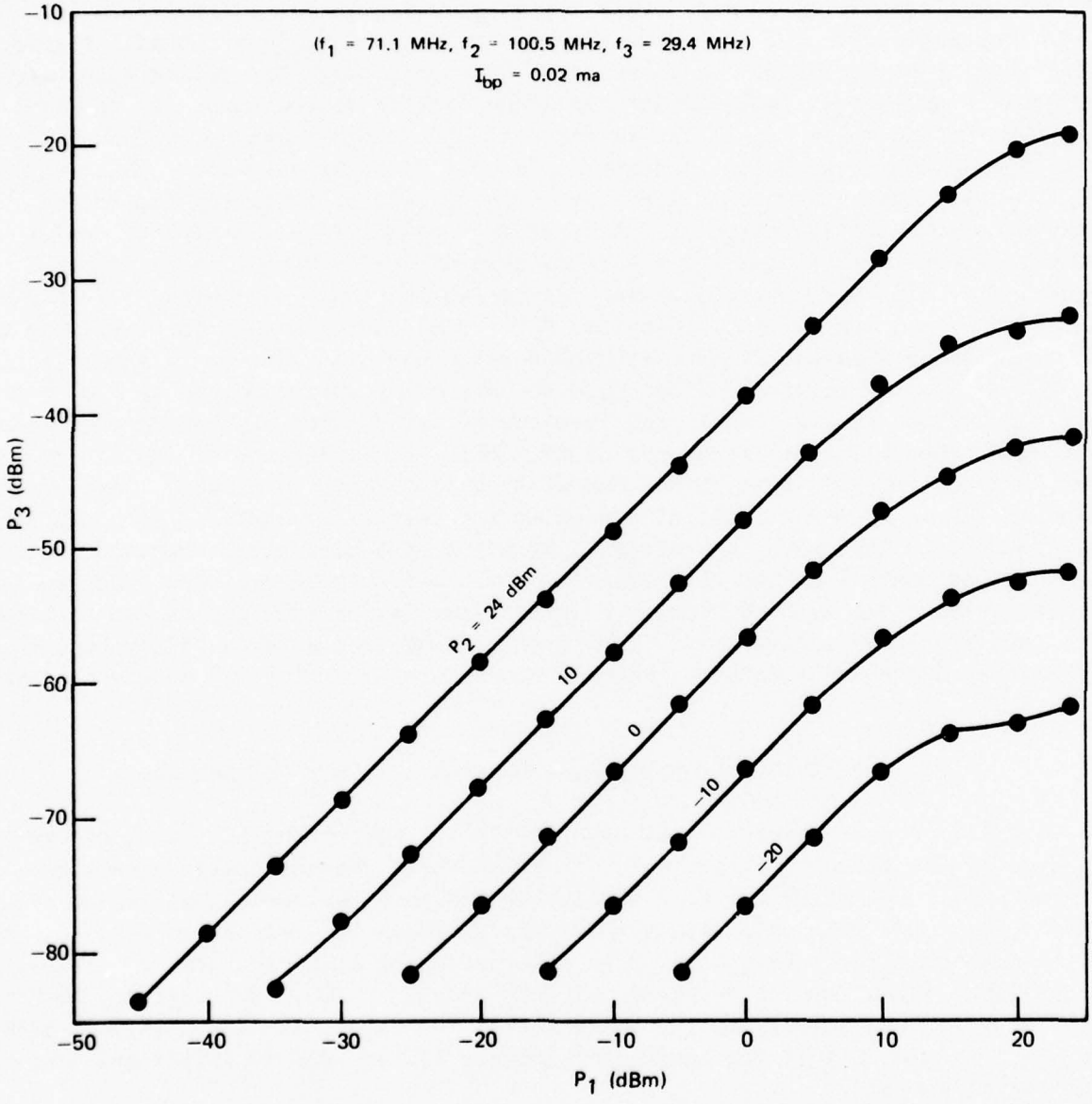


FIG. 4-4

128 TAP PSK DIODE CORRELATOR M229

POWER OUTPUT VERSUS POWER INPUT



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4.2 128 Chip PSK Signal Encoding

An encoded PSK signal and readout of the diode tap uniformity is obtained by applying a short rf burst ($\tau \ll \Delta T$) to Port 1 and a cw reference signal to Port 2. Photographs of the impulse response for M230 are shown in Fig. 4-5 for two tap bias codes. Input power levels and frequencies are $P_1 = P_2 = 24$ dBm, $f_1 = 71.1$ MHz and $f_2 = 100.5$ MHz. The -20 dBm output power level is 42 dB lower than the output with all taps coherently summed. This compares well with the 20 Log(1/128) dB = -41 dB loss expected. All taps were biased equally with $|I_{bp}| = .04$ mA. Figure 4-5(a) shows the tap readout at f_3=29.4 MHz for equal phase tap coding resulting from equal bias current polarity and amplitude applied to the taps. It is significant to note that while tap to tap random amplitude nonuniformities within $\pm$ 1.5 dB are observed, the overall tap sequence has a near constant envelope. This results from the near equal propagation loss for the waves intercepting any tap in the tilted electrode configuration as discussed in Section 2-3. All taps of device M230 were found to function, while several taps of device M229 were defective because of bonding difficulties during device fabrication. An encoded 127 chip PSK sequence is shown in Fig. 4-5(b) for M230 where the diode taps are biased in a 127 chip biphase M-sequence. An expanded portion of this sequence is shown in Fig. 4-6(a) showing reversal of the chip to chip phase when compared to a cw reference. Also shown in Fig. 4-6 is the spectrum of the encoded biphase encoded signal centered at the difference frequency of 29.4 MHz. The sidelobes of the sin x/x spectrum are suppressed by a 15 MHz bandwidth output bandpass filter. Good carrier balance is shown by the absence of a peak at the carrier frequency. Although the code sequence in this case is programmed by means of a hard wired connector board, computer code control of tap bias polarity would allow submicrosecond code programming rates. The encoded signals obtained from device M229 for cw and biphase coded taps are shown in Fig. 4-7. The three missing taps were caused by bonding difficulties during fabrication. Random nonuniformities of $\leq$ 1.5 dB are observed.

4.3 Correlation of Actively Generated 128 Chip PSK Sequences

Correlation characteristics of several actively generated PSK sequences were tested using the circuit of Fig. 4-8. An HP 8016A programmable pulse generator and doubly balanced mixer was used to biphase modulate the signal carrier at frequency f_1=71.1 MHz with chip rate R_c=9.81 MHz matching the device tap spacing. The desired modulated burst length was then selected using a HP 214 pulse generator. The amplified signal and cw reference at frequency f_2 = 100.5 MHz were applied to Ports 1 and 2, respectively of the correlator. The output at f_3 = 29.4 MHz, after transmission through a 15 MHz bandwidth bandpass filter, was amplified and displayed on an oscilloscope.

FIG. 4-5

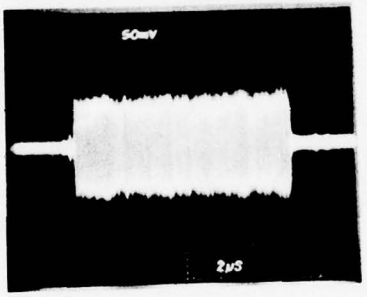
M230: 127 CHIP ENCODED SIGNALS

f_1 = 71.1 MHz, f_2 = 100.5 MHz, f_3 = 29.4 MHz

$P_1 = P_2$ = 24 dBm, I_{bp} = 0.04 ma

τ_1 = 100 nsec, τ_2 = cw

(a) CONSTANT PHASE TAPS



(b) M-SEQUENCE TAPS

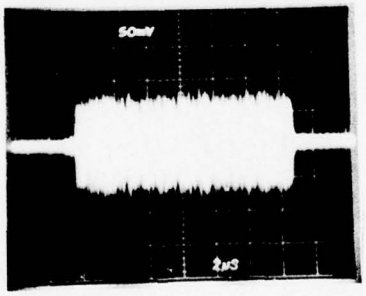
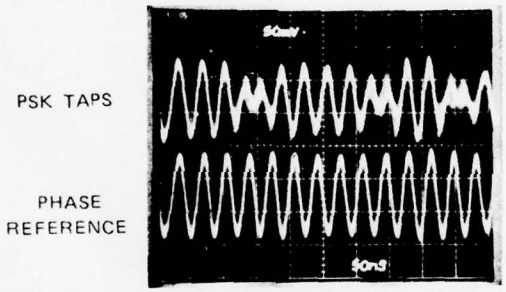


FIG. 4–6

M230:127 CHIP M–SEQUENCE ENCODED SIGNAL

($P_1 = P_2 = 24$ dBm, $f_1 = 71.1$ MHz, $f_2 = 100.5$ MHz, $f_3 = 29.4$ MHz)



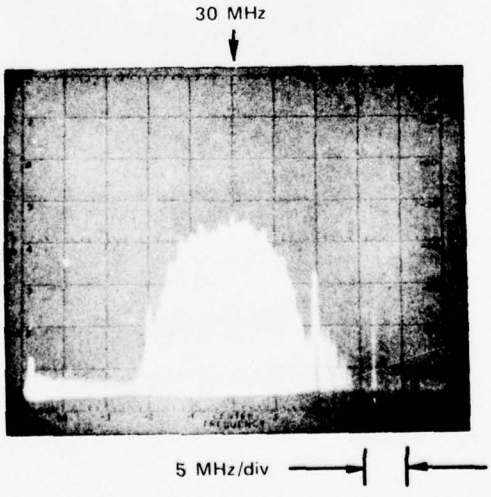


FIG. 4-7

M229: 127 CHIP ENCODED SIGNALS

f_1 = 71.1 MHz, f_2 = 100.5 MHz, f_3 = 29.4 MHz

$P_1 = P_2$ = 24 dBm, I_{b_p} = 0.04 ma

τ_1 = 100 nsec, τ_2 = cw

(a) CONSTANT PHASE TAPS

(b) M-SEQUENCE TAPS

CIRCUIT DIAGRAM FOR PROGRAMMABLE CORRELATION EXPERIMENTS

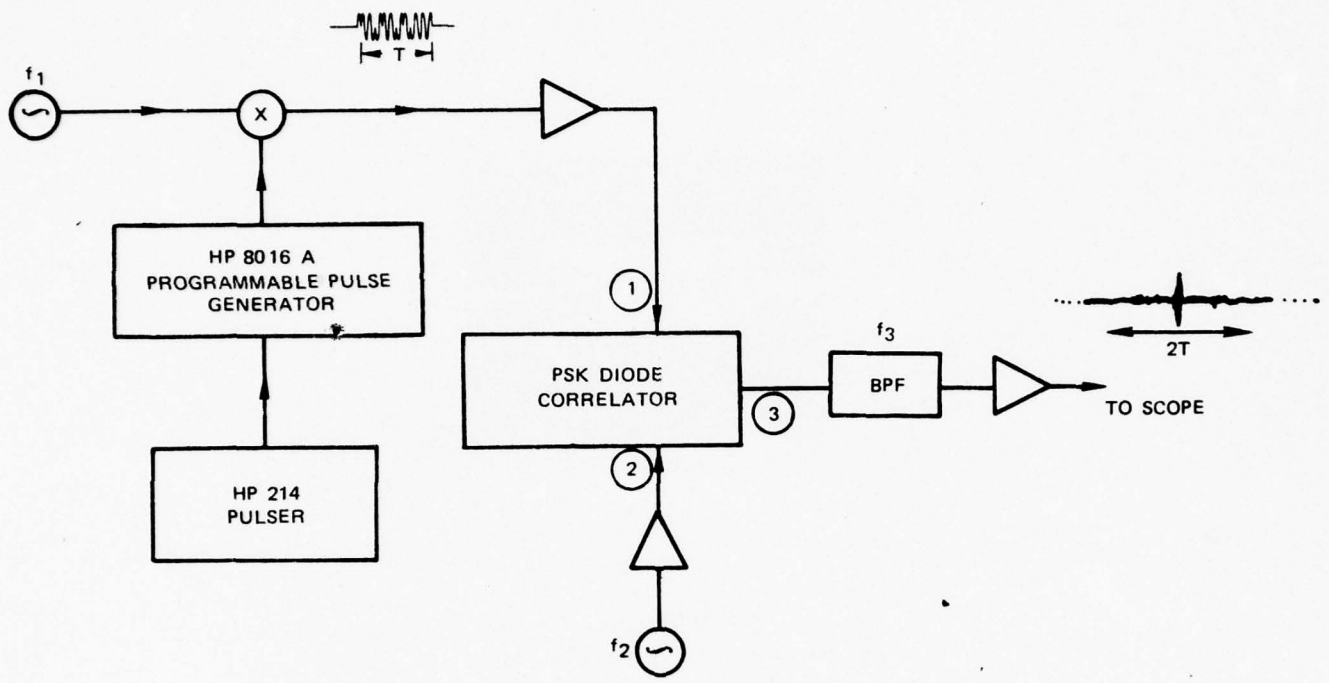


FIG. 4-8

76-10-10-2

Matched filter correlation of a 127 chip biphase M-sequence burst is shown in Fig. 4-4. The M-sequence chosen corresponds to that derived from a seven state shift register generator having feedback taps 6 and 7 with modulo 2 addition (Ref. 5). The experimental peak to sidelobe ratio of 21 dB is within 2 dB of the predicted 23 dB response for this sequence. The display of Fig. 4-9(b) was photographed in a single exposure by overlaying a strip of Kodak Wratten gelatin Filter #99 over the baseline so that both the narrow peak and intense sidelobe structure would be visible. The 200 nsec central correlation peak is shown in the expanded photo of Fig. 4-9(c).

Matched filter correlation of a different 127 chip M-sequence having equivalent shift register feedback taps 1 and 7, is shown in Fig. 4-10. The experimental 20.2 dB peak to sidelobe ratio is within 1 dB of the theoretical 21.2 dB. Also shown is the cross correlation waveform between an input cw sequence and the M-sequence tap code. The central null of 34 dB relative to the matched filter correlation peak, is a measure of the ultimate peak to sidelobe ratio achievable with the present device. This is to be compared with the theoretical 42 dB null. The cross correlation between this sequence (feedback taps 1, 7) and the previous M-sequence (feedback taps 6, 7) is shown in Fig. 4-10(c).

Thirteen bit Barker code autocorrelation results are given in Fig. 4-11. In this case, each bit corresponds to 10 correlator taps except for the 13^{th} bit, which is composed of 8 taps. The waveform generated very closely approximates the exact response with 6 nearly equal sidelobes on each side of the peak. The peak to sidelobe ratio of 21.5 dB compares well with the 22.3 dB theoretical response.

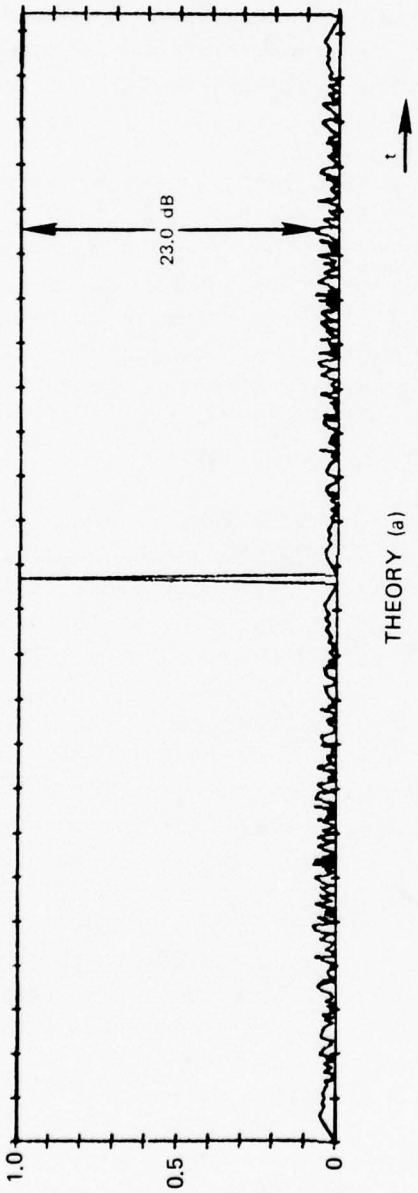
The M-sequence burst correlation waveforms described in general have peak to sidelobe ratio of approximately 20 log $1/\sqrt{N}$ where N is the sequence length. However, when repetitively correlated in a cyclic sequence, portions of all chips of the code overlap all taps at a given instant, such that the expected peak to sidelobes ratio then becomes 20 log $1/N$, with constant sidelobe level between correlation peaks. Experimentally, cyclic correlation response was tested by actively generating a 254 chip code composed of a repetition of 2(127) chip M-sequences, and correlating this code with the same 127 chip code programmed within the correlator as shown in Fig. 4-12(a). Prior to complete code overlap, the equivalent burst sidelobe pattern results. However, between correlation peaks, a nearly constant 30 dB sidelobe level is obtained as shown in the double exposure of Fig. 4-12(b). This sidelobe level for a 127 chip cyclic M-sequence compares favorably with that achieved in fixed coded linear correlators (Ref. 30). The discrepancy between the experimental and theoretical levels can be attributed to random phase and amplitude errors, band limitation and spurious contribution including acoustoelectric coupling between taps.

FIG. 4.9

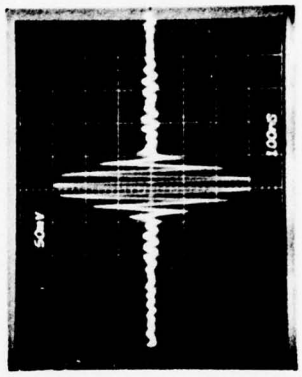
AUTOCORRELATION OF 127 M(6,7) BURST SEQUENCE

ACTIVE CODE GENERATION

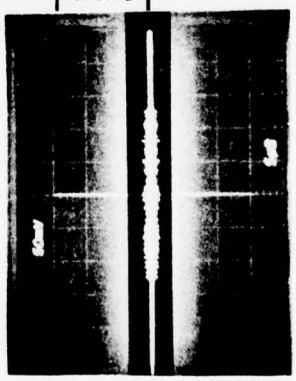
(DEVICE M230 $P_1 = P_2 = 24$ dBm)



THEORY (a)



(c)



(b)

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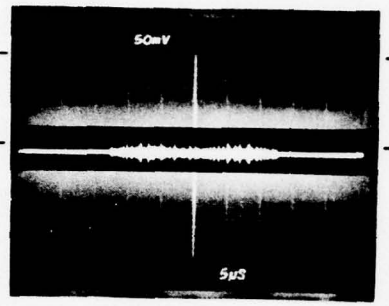
127 CHIP (1,7) M-SEQUENCE BURST CODE

ACTIVE CODE GENERATION
(DEVICE M230, $P_1 = P_2 = 24$ dBm)

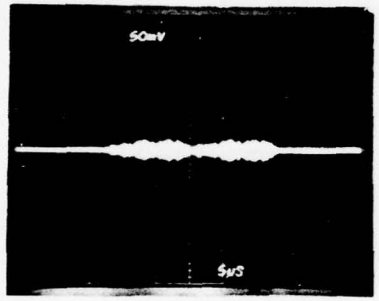
THEORY 21.2 dB



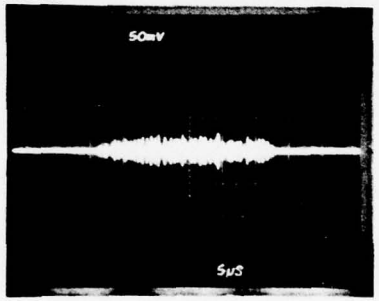
20.2 dB EXPERIMENT

AUTOCORRELATION

34 dB
CENTRAL NULL



CW INPUT CODE



(1,7) ⟶ (6,7)

15 dB
SIDELOBES

CROSS CORRELATION

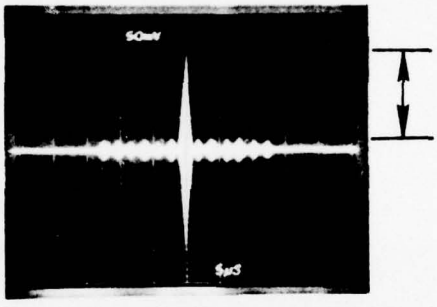
FIG. 4-10

FIG. 4–11

AUTOCORRELATION OF 13 BIT (128 CHIP) BARKER CODE SEQUENCE +++++––+–+–+

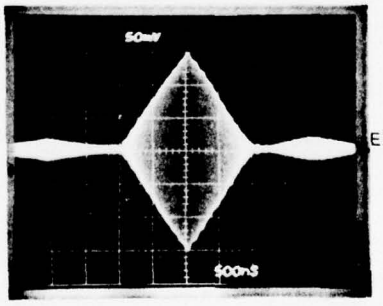
ACTIVE CODE GENERATION

(DEVICE M230, $P_1 = P_2 = 24$ dBm)

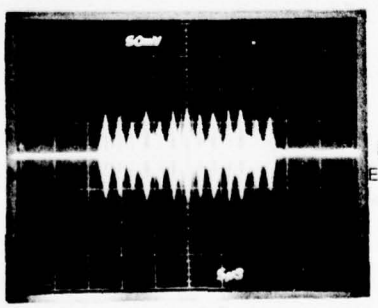


22.3 dB
THEORY

21.5 dB
EXPERIMENT



EXPANDED
PEAK

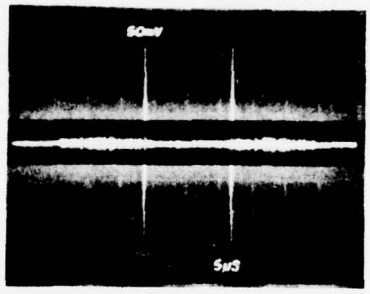


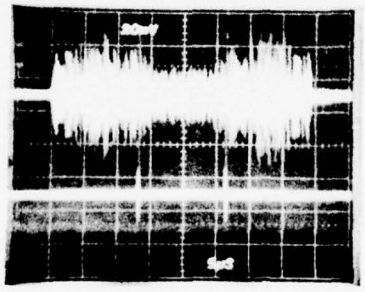
21 dB
DOUBLE
EXPOSURE

AUTOCORRELATION OF 127 M(6,7) CYCLIC SEQUENCE

ACTIVE CODE GENERATION

(DEVICE M230 $P_1 = P_2 = 24$ dBm)





30 dB
DOUBLE
EXPOSURE

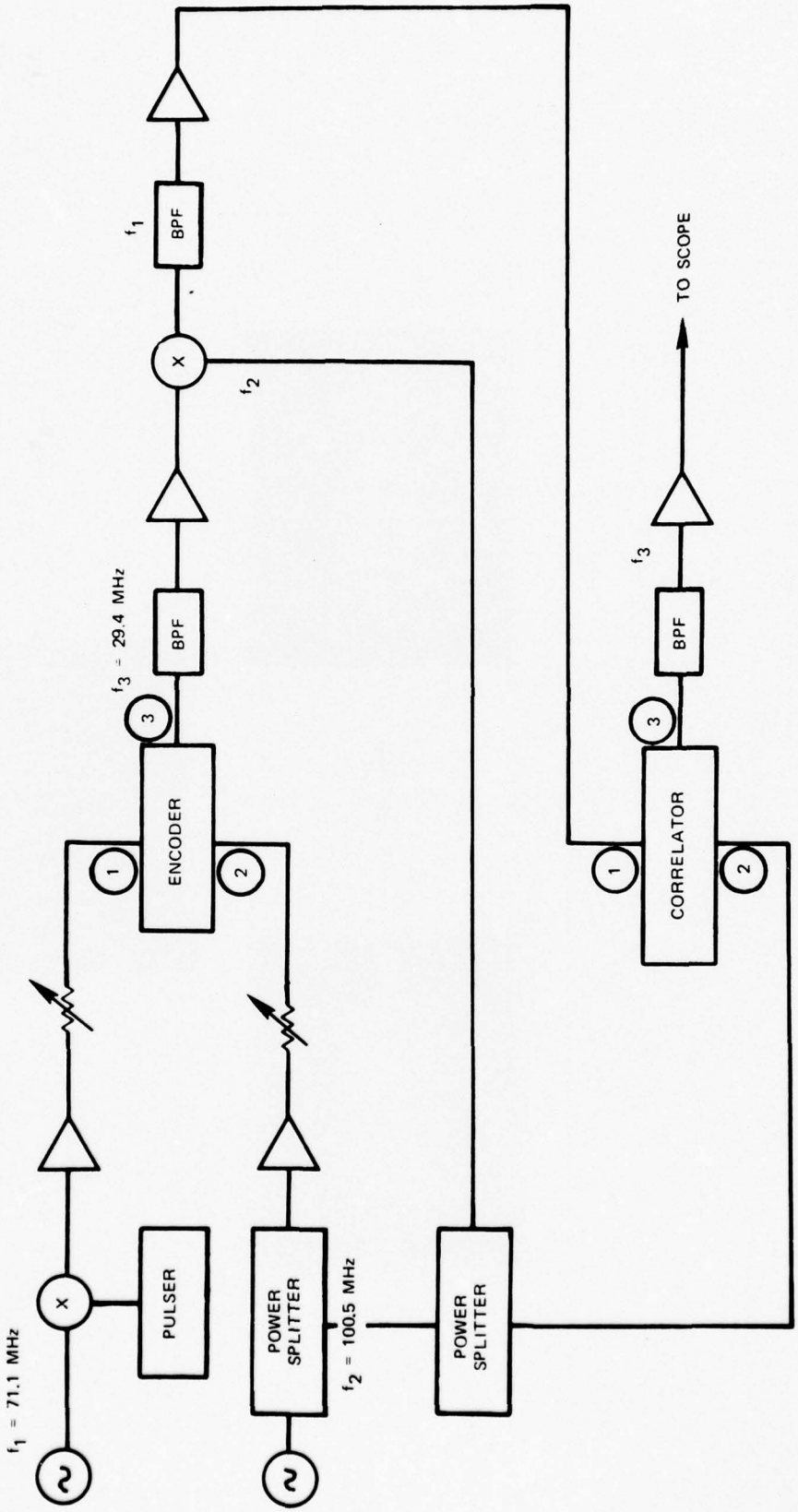
4.4 Matched Pair 128 Chip PSK Encoder - Correlator Experiment

The input signal generated actively in the previous experiments is replaced by a nonlinearly generated signal obtained using another PSK Diode Correlator module M230. With reference to Fig. 4-13, an encoded signal is obtained at f_3 = 29.4 MHz as described in Section 4.2. After amplification, mixing with the encoder reference frequency, f_2 = 100.5 MHz, and transmission through a 15 MHz bandwidth band pass filter, the encoded signal is translated to f_1 = 71.1 MHz and is fed to the second PSK correlator M229. The cw correlator reference is derived from the same f_2 source used to encode the signal waveform. The correlation output, after filtering and amplification is displayed on an oscilloscope. Both the encoder and correlator codes may be arbitrarily programmed in the desired PSK sequences. The biphase signal produced by the encoder at the difference frequency f_3, and after mixing to the input frequency f_1 are displayed in Fig. 4-14. Note that at f_1 and f_3 each chip contains 7 and 3 rf cycles respectively. Phase reversal between chips at the input carrier frequency f_1 is shown in Fig. 4-14(b).

The matched filter response for both encoder and correlator programmed with a 127 chip M-sequence code (feedback taps 6,7) is shown in Fig. 4-15(a). An expanded view of the correlation peak is given in Fig. 4-15(b). The M-sequence autocorrelation function closely follows that shown in Fig. 4.9 obtained with an actively generated signal input. In both cases the peak to sidelobe response is 21 dB. The matched filter triangular response for both encoder and correlator taps programmed with a constant phase is given in Fig. 4-15(c). These results demonstrate that the matched pair PSK diode correlator 128 chip transmission system performs in a comparable manner to an equivalent system utilizing active code generation.

FIG. 4-13

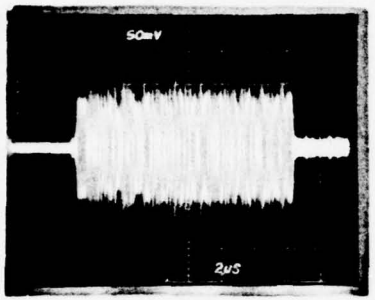
128 TAP PSK DIODE-CORRELATOR PAIR ENCODING-CORRELATION EXPERIMENT



76-09-229-10

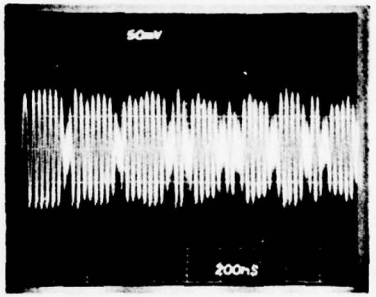
127 CHIP PSK M-SEQUENCE ENCODED WAVEFORMS

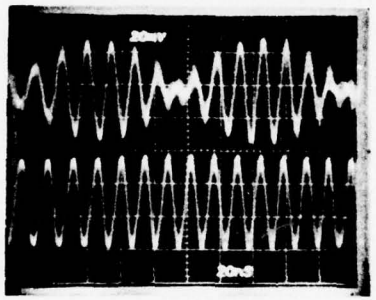
($P_1 = P_2 = 24$ dBm)



(a)

$f_3 = 29.4$ MHz





•••+-•••

•••--•••

$f_1 = 71.1$ MHz

(b)

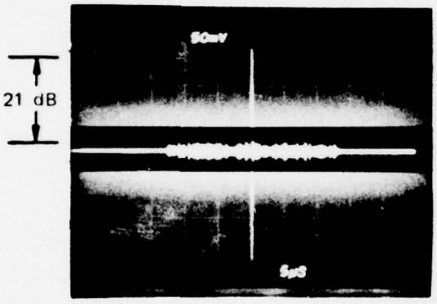
FIG. 4-14

FIG. 4–15

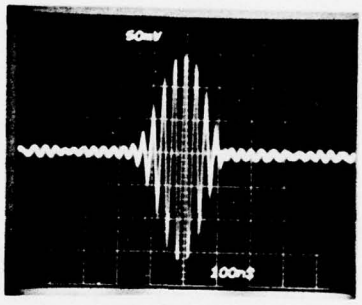
128 TAP PSK DIODE CORRELATOR PAIR ENCODING–CORRELATION EXPERIMENT

AUTO CORRELATION WAVEFORMS

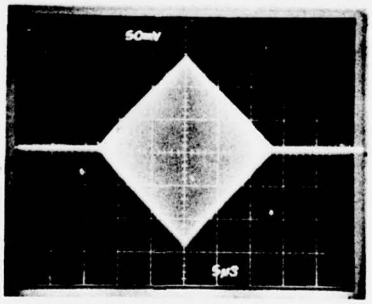
(f_1 = 71.1 MHz, f_2 = 100.5 MHz, f_3 = 29.4 MHz)



127 CHIP M–SEQUENCE
(6,7 FEEDBACK TAPS)



EXPANDED VIEW OF M–SEQUENCE
CORRELATION PEAK



CONSTANT PHASE TAPS

5.0 EVALUATION OF SYSTEMS APPLICATIONS

5.1 Introduction

In this section we consider applications of the PSK Diode Correlator module within the systems environment. Such applications include cascading discrete P chip modules as building blocks of a long code PSK correlator, demonstration of its high speed code programmability and jam resistance for secure and multisubscriber systems and compensation for frequency offset of a received PSK signal.

5.2 Application to Long Code PSK Signal Processing

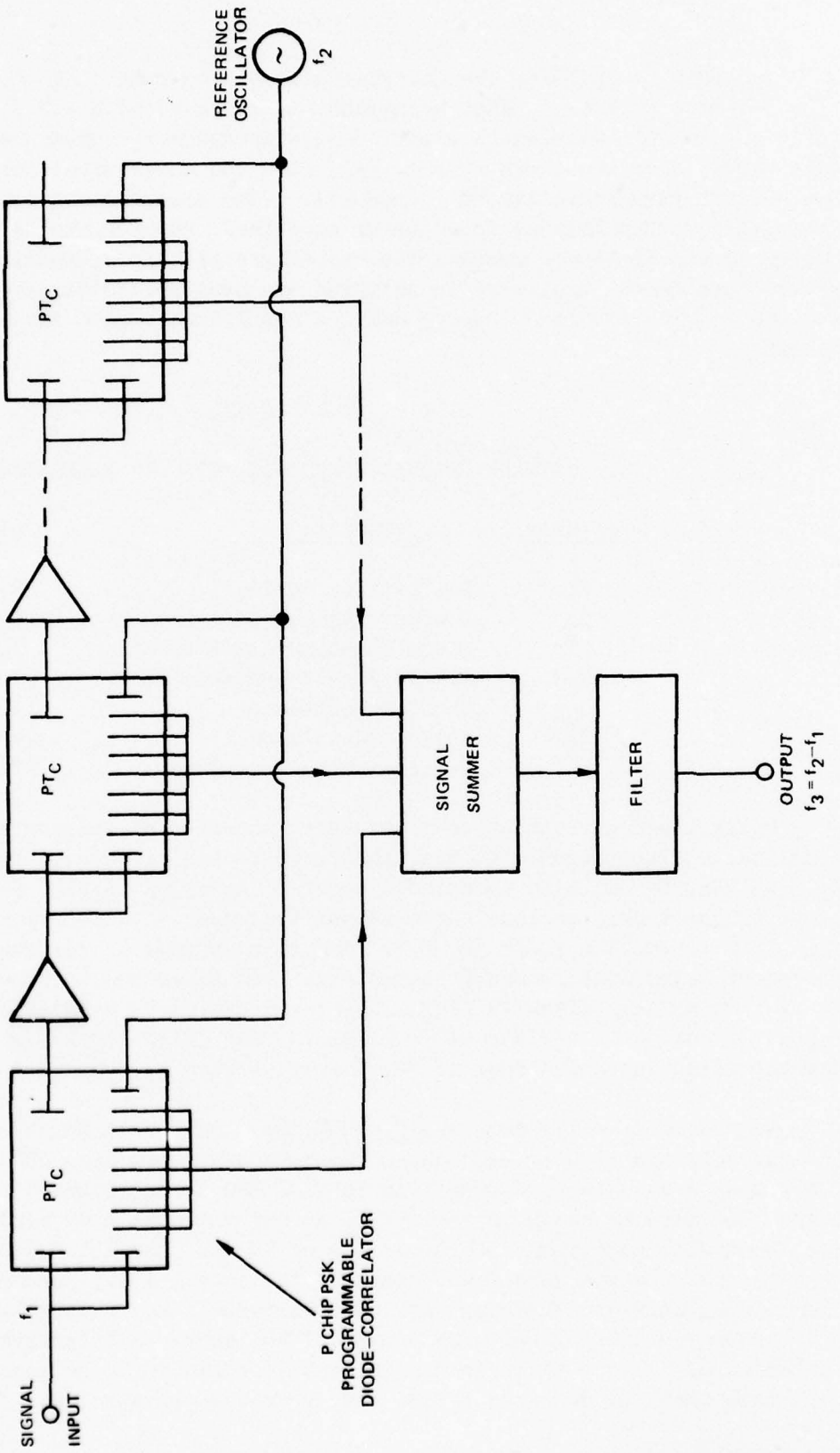
As shown in Fig. 5-1, individual PSK Diode Correlator modules may be cascaded to form a long code processor, by successively delaying the input sequence through a separate parallel cascade delay channel associated with each module. This approach has been recently utilized successfully with fixed code ST quartz delay lines for a seven delay line, 350 μsec cascade (Ref. 22). The excellent results achieved there predict that even greater cascade lengths may be employed without severe signal to noise degradation resulting from band limiting within the cascade delay channel transducers. One would expect a similar performance when cascading lithium niobate PSK Diode Correlator modules however, with the additional advantages of complete tap code programmability and phase error compensation by means of electronic adjustability of the reference frequency offset. The experimental performance of a two module cascade for correlation of 250 chip sequence is described here. These results suggest that extension to PSK correlation of codes with length up to 1024 and longer can be achieved by cascading 8 or more of the modules described here.

5.2.1 Cascade Delay Channel Design

The cascade delay channel must be sufficiently broadband to allow accurate signal transmission and low bandlimiting for the required number of cascaded modules. To achieve a cascade delay circuit 3 dB bandwidth equal to the chip rate, R_c, with Q modules, requires that each cascade delay channel has a (3/Q) dB bandwidth equal to R_c. For a 1024 chip code, with 128 chips per cascade and R_c = 10 MHz, eight modules are required, each having a 0.375 dB bandwidth of 10 MHz. Our approach toward meeting this goal is based upon the broadband impedance inverter transducer tuning circuit shown in Fig. 5-2. This circuit has been demonstrated to provide almost maximally flat transducer response with relatively low insertion loss and high triple transit suppression (Ref. 29). The low pass PI-section shown approximates a uniform transmission line having impedance Z_I and quarter wavelength frequency f_I. The corresponding network elements L_P and C_P are chosen to optimize the delay line insertion loss and bandwidth using computer aided design.

FIG. 5-1

PSK DIODE-CORRELATOR CASCADE CIRCUIT



N12-163-9

In order to optimize the inverter design, the remaining circuit components of Fig. 5-2 must be known. Each transducer is composed of N = 2.5 interdigital periods of eighth-wavelength electrodes. Impedance measurements of the series tuned transducer are shown in Fig. 5-3, with the theoretical curves computed using the circuit parameters listed in Table II. The electromechanical coupling coefficient, $K^2 = .035$ is that found by Bristol (Ref. 24) for eighth wavelength electrodes on y-z lithium niobate. The transducer electrode capacitance, C_N, and shunt capacitance, C_{SH}, were found using the measured total capacitance $C_T = C_N + C_{SH}$ and varying the ratio C_N/C_{SH} until a sufficiently good fit to the data was obtained.

TABLE II

CASCADE CHANNEL TRANSDUCER CIRCUIT PARAMETERS

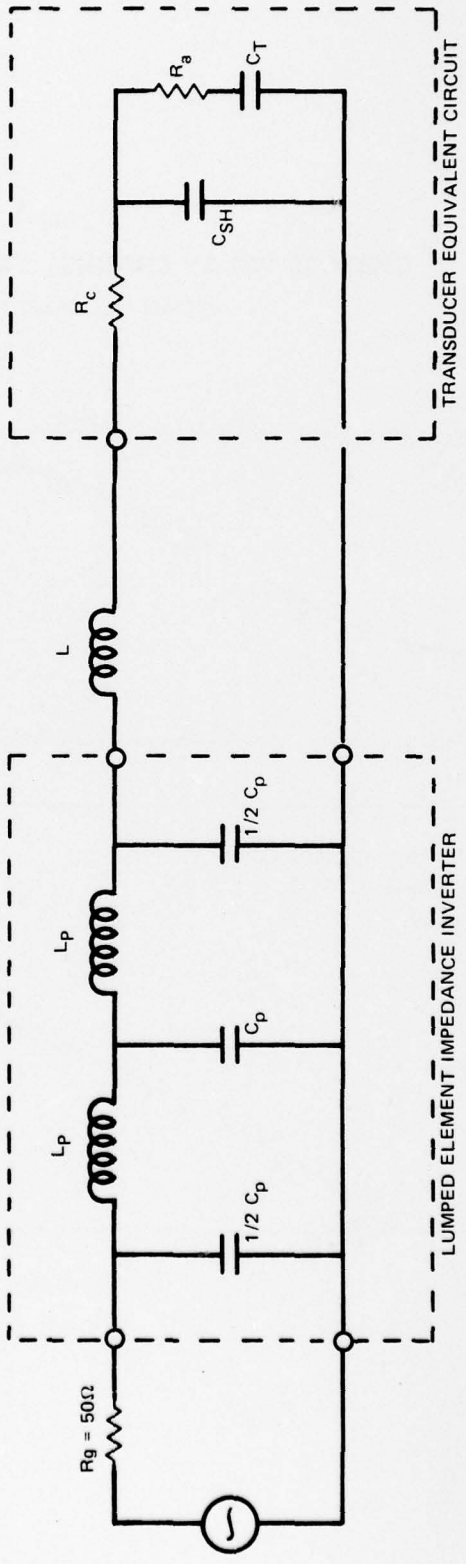
Variable	Definition	Value
N	No. of I.D. Periods	2.5
f_o	Center Frequency	71.5 MHz
K^2	Piezo Coupling Coefficient	3.5%
C_T	Active Electrode Capacitance	5.0 Pf.
C_{SH}	Shunt Capacitance	1.0 Pf.
R_C	Series Resistance	24 Ω
L	Series Tuning Inductance	826 nH

Using these circuit values, optimized inverter parameters were determined. A maximally flat response at the transducer center frequency, f_o, was found for $f_I = 68$ MHz, essentially independent of Z_I. As shown in Fig. 5-4(a), a nonzero slope of the insertion loss curve versus frequency is possible at other values of f_I. This controlled slope could be used to advantage in compensating for frequency dependent delay line losses if necessary. The insertion loss and 3 dB bandwidth at $f_I = 68$ MHz are given in Figs. 5-4(b) and 5-4(c) as a function of inverter impedance. A maximum bandwidth of 32.6 MHz is calculated for $Z_I = 170$ ohms with a corresponding insertion loss of 20 dB at $f_o = 71.5$ MHz.

Values of $Z_I = 132$ ohms and $f_I = 68$ MHz were chosen for the experimental inverter circuit with corresponding network components $L_P = 220$ nH and $C_p = 15$ pF. The computed and measured insertion loss of the inverter tuned cascade delay channel of M230 is shown in Fig. 5-5. An experimental 3 dB bandwidth of 20 MHz was found with a minimum insertion loss of 18 dB. The 7.1 MHz periodic nonuniformities in the bandpass were found only for the actual 13.05 μsec cascade delay channels of M229 and M230 and were not observed in an identical but shorter 6.42 μsec prototype delay line. The source of the spurious interference is thus not connected with the transducer design, but is believed to be caused by a spurious bulk mode which is detected by the larger transducer spacing. This mode could

FIG. 5–2

BROADBAND TRANSDUCER CIRCUIT INCLUDING A LUMPED ELEMENT IMPEDANCE INVERTER



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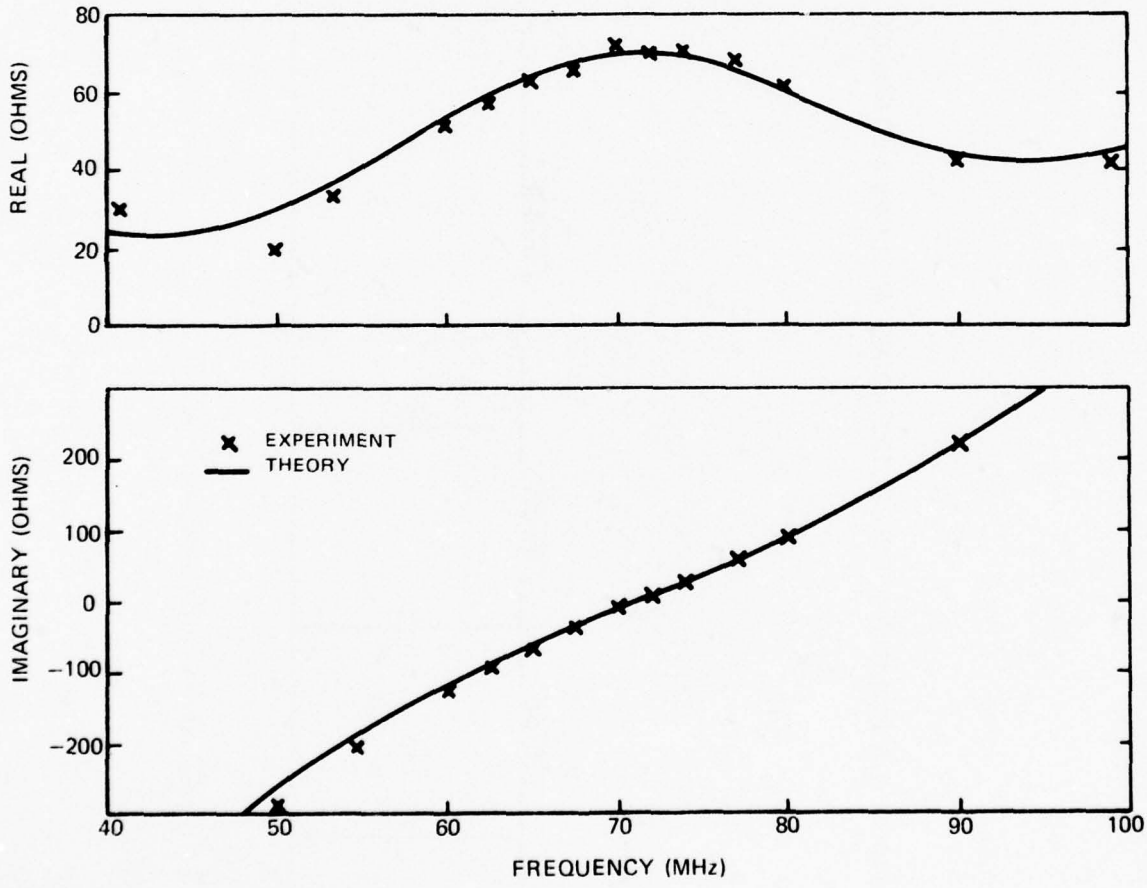
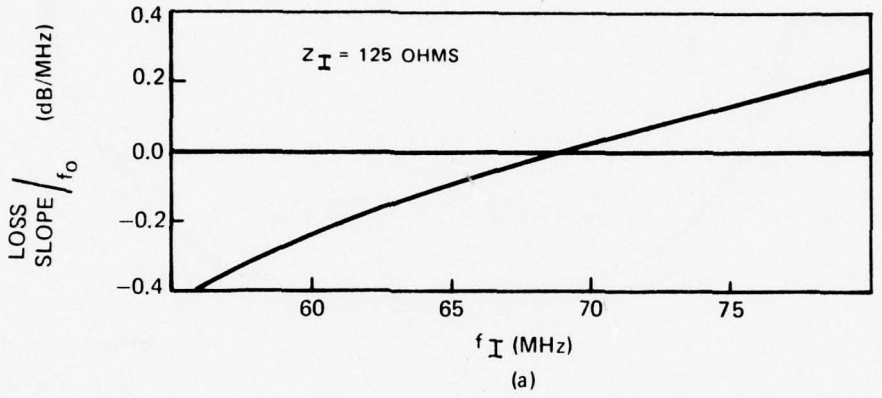
CASCADE DELAY CHANNEL TRANSDUCER IMPEDANCE

SERIES INDUCTIVE TUNING

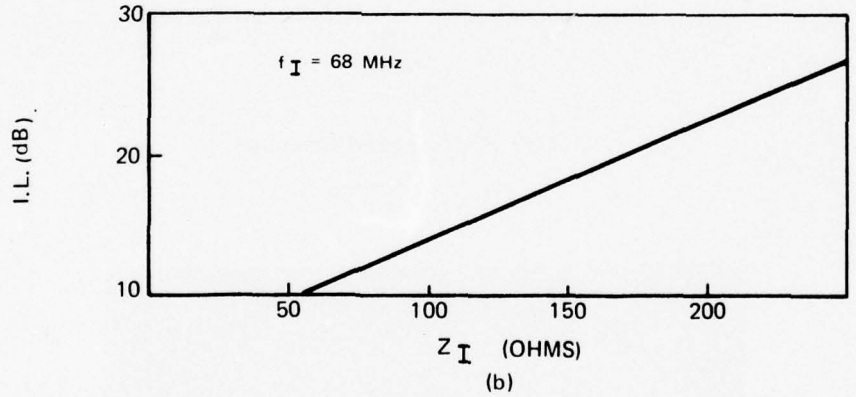


76–04–297–4

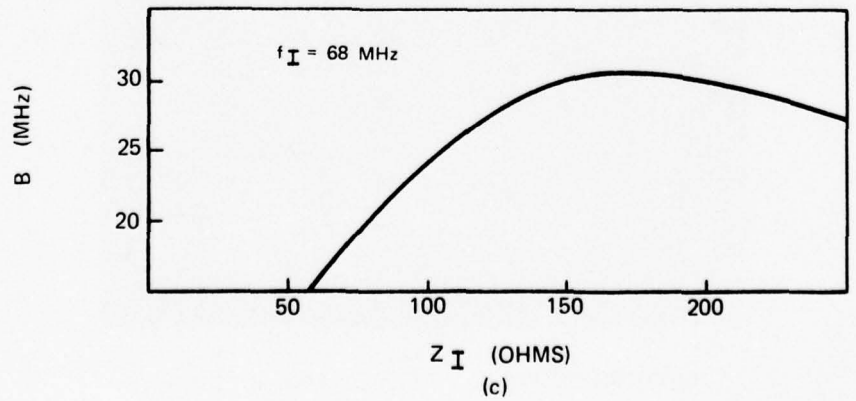
COMPUTED INVERTER–TUNED CASCADE DELAY CHANNEL CHARACTERISTICS



(a)



(b)

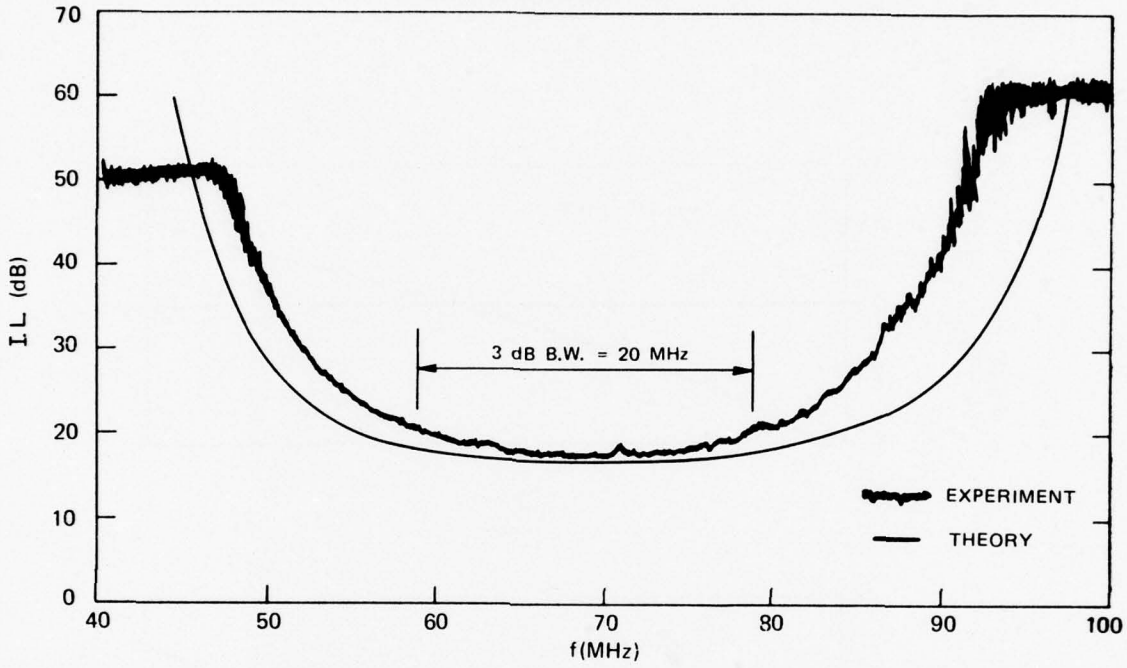


(c)

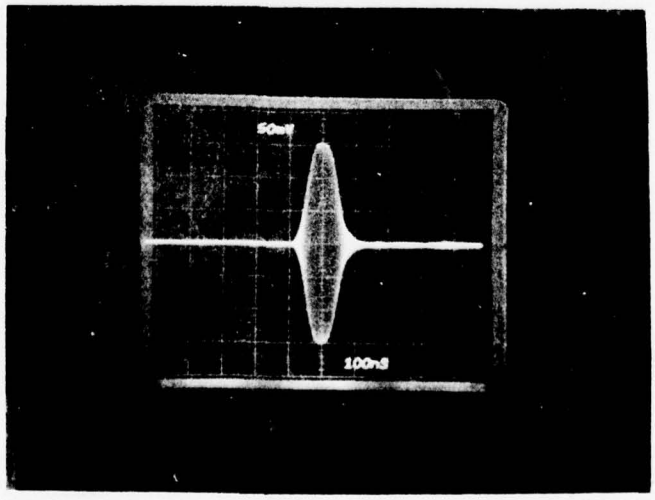
76–04–297–7

INVERTER–TUNED CASCADE DELAY CHANNEL PERFORMANCE

DEVICE M230



a) TWO PORT INSERTION LOSS



b) PULSE RESPONSE f_1 = 71 MHz, τ = 100 nsec

be eliminated in future work by beveling the reverse side of the delay line. The .375 dB bandwidth of approximately 10 MHz (equal to the PSK chip rate) was obtainedwith the prototype delay line, making the channel design appropriate for a 1024 chip sequence delay. A 3 dB bandwidth of 24 MHz was also achieved. The measured triple transit suppression of 40 dB at 70 MHz compares well with the computed 39 dB value. The delay channel response of device M230 at 71 MHz for a 100 nsec pulse is shown in Fig. 5-5(b).

The test circuit used for evaluating the performance of a cascade connection of two 128 tap correlator modules is shown in Fig. 5-6. The cascade delay channel is situated on the same substrate as the 128 tap correlator so that fabrication errors and thermal changes in propagation delay would be identical for both acoustic paths.

The delay channel length was 15 nsec less than the 128 chip code length to account for group delay in the transducer tuning circuits and cascade amplifier. Slight adjustments to the delay channel length were made using lengths of cable. Experimentally, the input signal at f_1 = 71.1 MHz is split between the first module input Port 1 and the cascade channel, with a cw reference frequency at f_2 = 100.5 MHz applied equally to both modules. The output at f_3 = 29.4 MHz were then summed, filtered, amplified and displayed on the oscilloscope. Differences in module insertion loss were compensated by adjusting the cascade channel circuit gain for equilization of the nonlinear output from both modules.

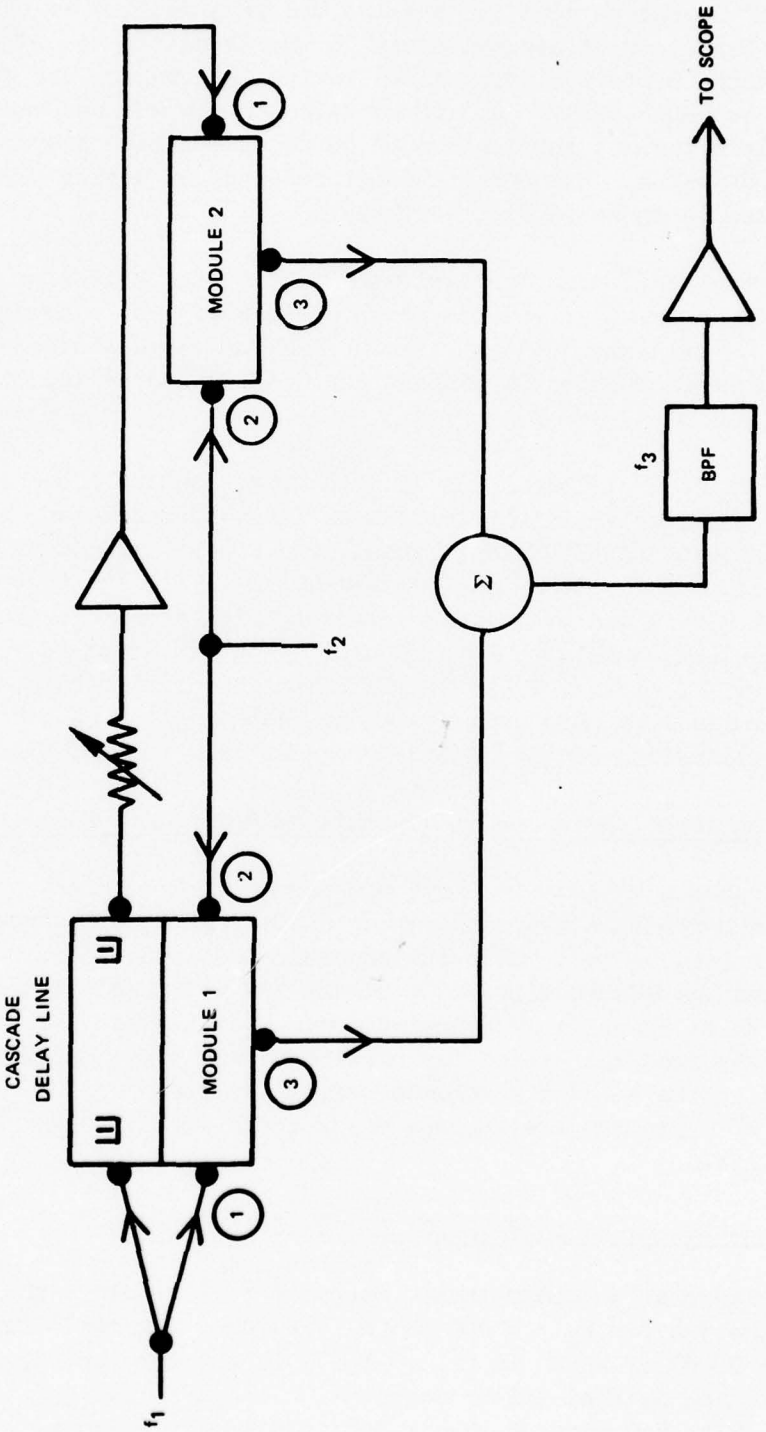
5.2.2 Evaluation of A Two Module Cascade As A 256 Chip PSK Signal Encoder

The encoded waveforms for taps programmed with constant phase and for a 255 chip biphase M-sequence with equivalent shift register feedback taps (4, 5, 6, 8) are shown in Fig. 5-7(a). With the exception of three mechanically faulty taps in the second cascade module, M229, random tap amplitude variations are approximately $\pm$ 1.5 dB with an essentially constant overall envelope. The lack of wave attenuation effects result from the tilted tap electrode geometry. Good carrier suppression is observed in the encoded M-sequence signal spectrum or Fig. 5-7(b). Sidelobes of the sin x/x spectrum are suppressed by means of the 15 MHz bandwidth output bandpass filter.

5.2.3 Evaluation as a 256 Chip PSK Signal Correlator

The triangular autocorrelation output for a 26 μsec input cw phase code is shown in Fig. 5-8 for P_1 = 5 dBm and P_2 = 24 dBm. Spurious suppression for the cascade was 50 dB as shown in Fig. 5-8(c), is the same as found for each module separately. The matched filter correlation response for a 255 chip M-sequence is shown in Fig. 5-9 along with the computed ideal response. Except for the first trailing sidelobe level of 20.5 dB, all sidelobes are down by 22 dB or more as compared to the computed 23 dB for this sequence. The higher trailing sidelobe level

FIG. 5-6



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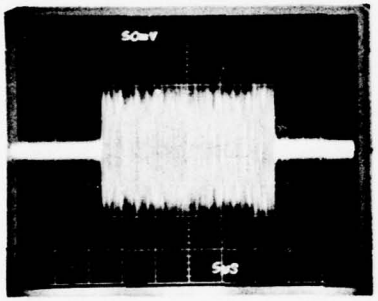
CASCADE CIRCUIT PSK ENCODED SIGNAL

255 CHIP M-SEQUENCE (4,5,6,8)

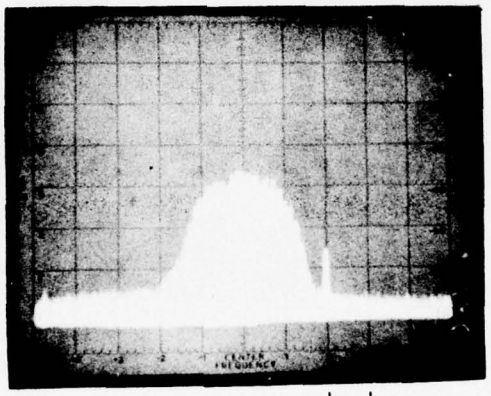
(f_1 = 71.1 MHz, f_2 = 100.5 MHz, $P_1 = P_2$ = 24 dBm)

f_3 = 29.4 MHz



(a)

30 MHz



FILTERED SPECTRUM

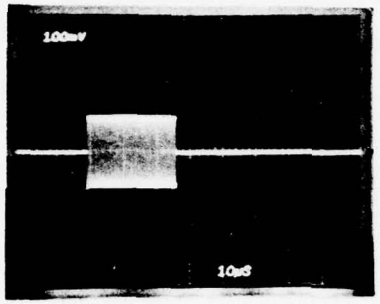
5 MHz/div

(b)

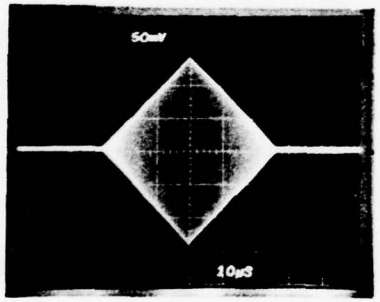
FIG. 5-7

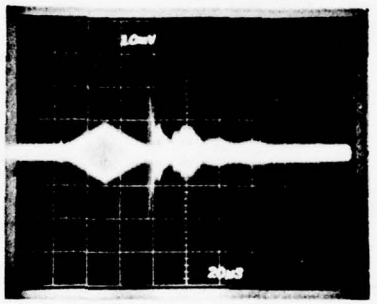
CASCADE CIRCUIT CORRELATION OF 256 CHIP CW SEQUENCE

(f_1 = 71 MHz, P_1 = 5 dBm, f_2 = 100 MHz, P_2 = 24 dBm)



INPUT SIGNAL





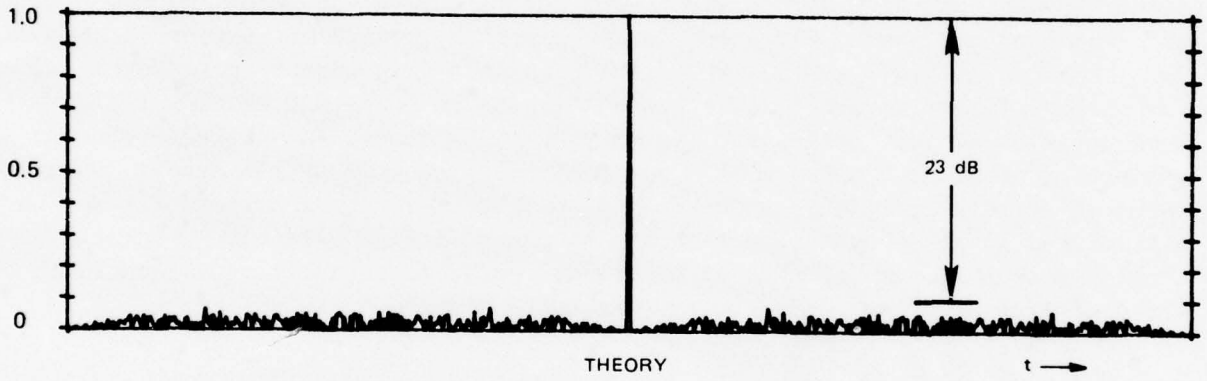
50 dB
DOUBLE
EXPOSURE

CORRELATION OUTPUT

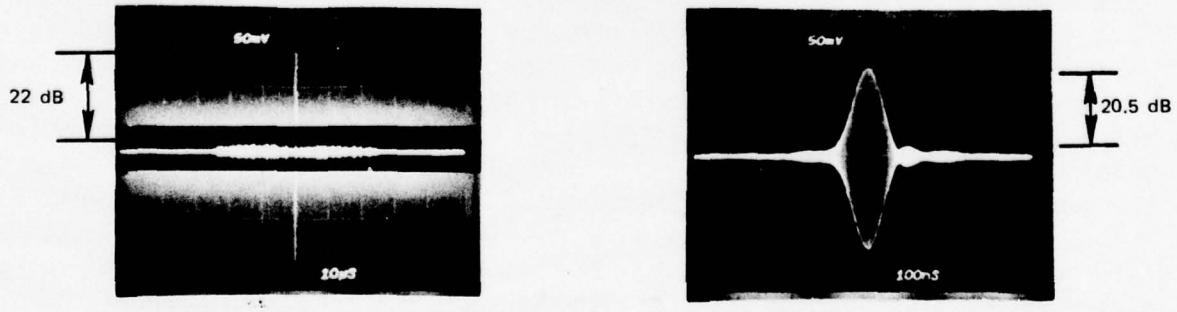
FIG. 5-8

CASCADE CIRCUIT AUTOCORRELATION OF 225 CHIP M-SEQUENCE

(f_1 = 71.1 MHz, P_1 = 5 dBm, f_2 = 100.5 MHz, P_2 = 24 dBm)



THEORY



EXPERIMENT

may result from power division and re-excitation within the tap output circuits so that a replica of the peak, one chip duration later, occurs when the regenerated signal wave at the adjacent taps are again received and summed at each original tap. By increasing the tap electrical or acoustic isolation this spurious response could be significantly reduced.

5.3 Application as a High Speed Programmable PSK Matched Filter

Rapid reprogramming capability of a single correlator, allowing matched filter correlation for arbitrary biphase codes at the fundamental or a submultiple chip rate, offers considerable advantage for cost-reduction in a multisubscriber, secure communication system. Experimental demonstration of electronic switching capability of the PSK diode calculator tap code is shown in Fig. 5-10 for burst signal inputs. In Fig. 5-10(a), both the correlator tap sequence and the signal code are constant phase, resulting in the periodic triangular autocorrelation waveforms shown. In Fig. 5-10(b), the diode taps have been periodically reprogrammed for matched filter correlation between alternate cw phase and biphase 127 chip M-sequence coded input signals. Tap reprogramming occurs immediately prior to processing of a coded burst with a tap switching speed of approximately 100 nsec. When the correlator code is programmed as a fixed M-sequence matched filter, the alternating cw code bursts are rejected as shown in Fig. 5-10(c). Terminals of a multiscriber system may thus be programmed or electronically reprogrammed in the field after producting of the basic correlator module.

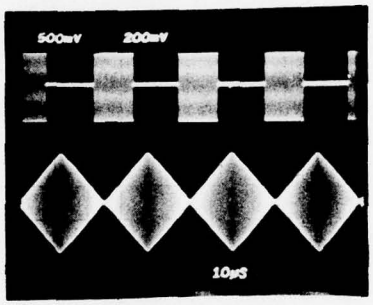
5.4 Interference Rejection Characteristics

Spread spectrum signals have high matched filter detection probability in the presence of interference for code sequences having low cross correlation response to the signal interference. cw interference within the main signal spectrum is considered to be a more hostile environment than spread spectrum interference because of the larger power density located within the system passband (Ref. 5). The matched filter performance of the PSK Diode correlator with cw jammer interference added to the desired 127 chip M-sequence signal input is shown in Fig. 5-11. Both the jammer input to signal power ratio varies from -10 to +23 dB with signal power P_1 = 5 dBM and reference power P_2 = 24 dBm, the output signal to noise ratio is seen to decrease from 17 to 4.5 dB. Even at a 30 dB interference/signal ratio signal correlation peak is still discernable with a 2 dB signal to noise level. These results are found to be slightly dependent on the location of the interference within the signal spectrum and correspond to near worst case values. In addition, the amount of interference rejection in any spread spectrum system depends in general on the system parameters including signal sequence, length and chip rate. Dependence on the total input power level near saturation levels at the diode

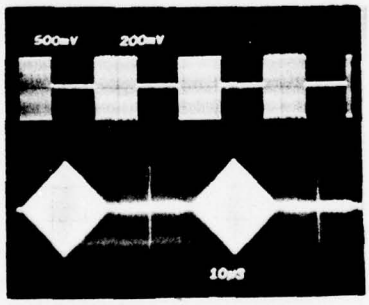
ELECTRONIC SWITCHING OF PSK TAP PROGRAMMING

(I_{b_T} = 4 ma)

INPUT: cw / cw
TAPS: cw / cw



INPUT: cw /M
TAPS: cw /M



INPUT: cw /M
TAPS: M/M

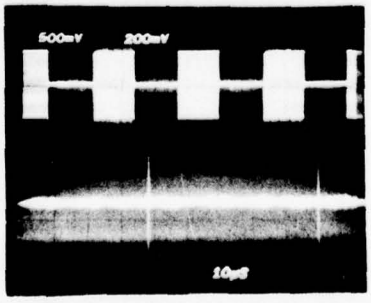
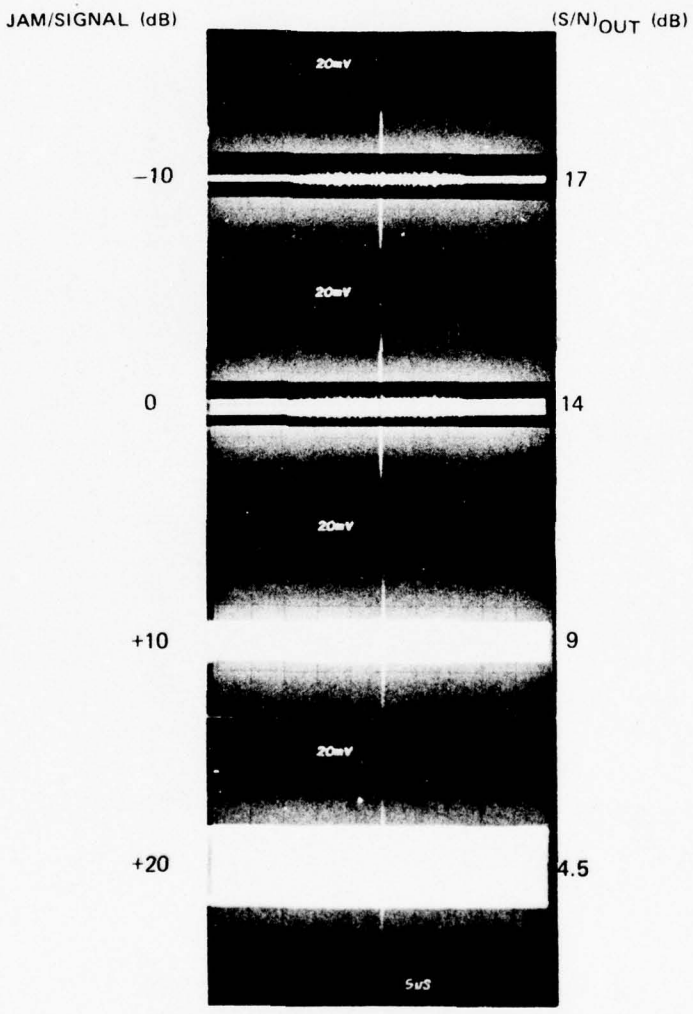


FIG. 5-11

SIGNAL CORRELATION IN PRESENCE OF INTERFERENCE

(127 CHIP M-SEQUENCE SIGNAL, cw JAM)

($f_{JAM} = f_{SIGNAL}$ = 71.1 MHz, P_1 = 5 dBm, P_2 = 24 dBm)



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taps is also expected; however from Fig. 4-4 this is minimal for interference levels less than 10 dBm. In contrast, interference rejection of a competitive digital correlator system has been found to optimize at a fixed total input power level of -12 dBm with rapid degradation at lower levels due to internal clock noise contributions (Ref. 15).

5.5 Restoration of Correlation Peak to Sidelobe Response in the Presence of Signal Frequency Offset

As discussed in Section 2.4, deviation from the optimum input frequency results in a reduction in correlation peak to sidelobe response by an amount equal to $\sin \pi\Delta\varepsilon_D/\pi\Delta\varepsilon_D$ where $\Delta\varepsilon_D$ is the total phase error given by Eq. 2-27. For an input signal frequency f_1 = 71 MHz and a chip rate R_c = 9.8 MHz, a 3 dB decrease in peak to sidelobe response is expected for a linear delay line correlator with $\Delta f_1 = \pm 35$ kHz (Ref. 27).

This also holds for the nonlinear correlator with fixed reference frequency f_2. Experimentally a range of $\Delta f = \pm$ 37 kHz was measured for a 3 dB output peak to sidelobe degradation for a 127 chip M-sequence correlation. However, when both f_1 and f_2 were varied by equal amounts, the peak to sidelobe level was restored even for much larger frequency excursions. In fact, not until $\Delta f_1 = \Delta f_2 = \pm$ 3 MHz was the restored peak to sidelobe ratio degraded by 3 dB relative to that obtained at frequencies of f_1 = 71.1 MHz and f_2 = 100.5 MHz. This range most likely is limited by increased wave reflections and bandwidth restriction away from the design frequencies. Because of this large range observed, the PSK Diode Correlator may be adjusted to accurately process PSK codes over a wide input carrier frequency range allowing subscribers tuned to the various carrier frequencies in addition to compensating for input signal Doppler shift. Additional security could also be achieved by adopting a fast frequency hop code composed of Q successive bits, each of different signal carrier frequency, and each bit composed of a varying P chip PSK sequence. The matched correlator would be composed of a cascade of Q, PSK Diode Correlators, each having a different reference frequency and code programming which could be continuously updated.

6.0 ANALYSIS OF THE EFFECT OF SYSTEM ERRORS ON LONG CODE CASCADE PERFORMANCE

6.1 Introduction

In this section we will summarize the important parameters affecting PSK signal encoding and correlation characteristics of the PSK Diode-Correlator cascade circuit. The cascade circuit, shown schematically in Fig. 1-3, is composed of Q cascaded modules, each having a P diode-taped signal processing path in parallel with a cascade delay channel. The signal wave at ω_1 is coherently delayed between modules and mixed with a continuous reference wave at frequency ω_2 at each diode tap. The nonlinear tap output signals at $\omega_3 = \omega_2 - \omega_1$, have their relative phase controlled by the polarity of the bias currents driving the diode taps. In both the encoding and correlation modes, the PSK code may be rapidly altered by reprogramming the tap bias sequence.

The formalism for predicting the effects of the major error contributions on the output waveform is developed in terms of those factors directly relating to the PSK Diode Correlator cascade circuit. This formalism is applied to the experimental 2 module 256 chip cascade demonstrated as described in Section 5.2. The observed autocorrelation response is compared to the response predicted by the analysis using estimates of the system error contributions. The effects of bandlimiting of a multi-module cascade are discussed. In particular, the waveform degradation of an 8 module, 1024 chip cascade processor due to finite module bandwidth is considered.

6.2 Formalism for Predicting Waveform Degradation

The ideal response of a single P tap Diode Correlator module has been discussed in Section 2.2 and is given by Eq. 2-14. By cascading Q of these modules in series, a code of length PQ may be processed. The output voltage of the qth module may be written

$$V_{3q}(t)e^{j\omega_3 t} = e^{j(\omega_2-\omega_1)t} A_q \sum_{p=1}^{P} S(t-t_{01}-t_p)e^{-j(\omega_2-\omega_1)t_p} \qquad (6.1)$$

Here, A_q is the effective nonlinear coefficient, $g_{p,q}$ is the tap code (± 1), t_{01} is the time delay to the first tap, $t_p = (p-1)\Delta T$ is the time delay from the first to the p^{th} tap, ΔT is the intertap delay, equal to the reciprocal of the chip rate, R_C, and $S(t-t_{01}-t_p)$ is the input signal. By design, the input and reference frequencies satisfy the relation

$$\omega_2 - \omega_1 = \omega_3 = nR_C, \; n = 1, 2, 3, \ldots, \qquad (6.2)$$

and the exponential term within the summation of Eq. (6.1) is identically unity.

In the presence of system or fabrication errors, the degraded module output has the general form

$$V_{3_q}(t)e^{j\omega'_3 t} = e^{j\omega'_3 t} \sum_{p=1}^{P} A_{p,q}\, g_{p,q}\, X_{p,q}(\tau')\, S(t-t_{01}-t_p)\, e^{-j\Delta\varphi_{p,q}} \qquad (6.3)$$

where subscripts p, q identify variables pertaining to the p^{th} tap of the q^{th} module. Each tap may now have a variable amplitude $A_{p,q}$ and phase error, $\Delta\varphi_{p,q}$. The output frequency, ω_3', differs from the design frequency given by Eq. (6.2) by an amount $\Delta\omega_3$.

The chip ambiguity function (Refs. 28, 32), $X_{p,q}(\tau')$ where $0 < \tau' < \Delta T$, results from the convolution between the input transducer and the p^{th} tap of the q^{th} cascade module. Its maximum value, $X_{p,q}(0)$, occurs when a signal chip is centered at that tap at $\tau' = 0$. For infinite system bandwidth and with other errors negligible each signal chip has a rectangular envelope and contributes an equal + or - unit to the summation with $X_{p,q}(0)$ equal to unity. For finite system bandwidth, the envelope of each signal chip is no longer rectangular, but has a rise and fall time associated with the system bandwidth after transmission through (q-1) cascade delay channels and an input signal transducer. The chip envelope is also dependent on the input code sequence as a result of neighboring chip interference, with maximum contribution to $X_{p,q}(0)$ for equally coded neighboring chips and minimum contribution for unlike neighbors. Computation of the bandwidth related correlation degradation may thus be made from knowledge of the chips envelope at each tap of the cascade and by accounting for the chip to chip interference. The chip rise time can be obtained by either taking the inverse Fourier transform of the system frequency response prior to the p^{th} tap of the q^{th} module, or experimentally through direct measurement. The latter method is used here by recirculating a pulse through a single cascade delay channel and broadband amplifier loop and measuring the pulse rise time after each circulation. The effect of neighboring chip interference is estimated by assuming a constant, trapezoidal or triangular chip envelope depending on the equality of the neighboring chip codes and the ratio $\gamma(q)$ of rise time $\tau_R(q)$ to chip duration $\Delta T = 1/R_C$,

$$\gamma(q) = \frac{\tau_R(q)}{\Delta T} \qquad (6.4)$$

This analysis leads to the rise time and code dependent weighting $X_{p,q}(0)$ of each chip's contribution to Eq. (6.3), given in Table 3. In the table, $S_{p,q}$ represents the signal code at the p^{th} tap of the q^{th} module.

TABLE III

Chip Weighting Produced by Finite System Bandwidth

Neighboring Chip Code Relationship	$X_{p,q}(0)$	$\gamma(q) = \frac{\tau_R(q)}{\Delta T}$
$S_{p-1,q}=S_{p,q}=S_{p+1,q}$	1	$0 \le \gamma(q) \le 1$
$S_{p-1,q}=S_{p,q}\neq S_{p+1,q}$ or $S_{p-1,q}\neq S_{p,q}=S_{p+1,q}$	$\frac{1}{4\gamma(q)}$	$.5 \le \gamma(q) \le 1$
	$1 - \gamma(q)$	$0 \le \gamma(q) \le .5$
$S_{p-1,q}\neq S_{p,q}\neq S_{p+1,q}$	$1 - \frac{\gamma(q)}{2}$	$0 \le \gamma(q) \le 1$

The phase error, $\Delta\omega_{p,q}$, is defined here as the sum of the accumulated errors of prior cascade modules, $\Delta\omega_q{}^K$, and a term $\Delta\omega^V{}_{p,q}$ which varies with tap number. To first order, the varying phase error is given by

$$\Delta\varphi^V{}_{p,q} = n(p-1)\, 2\pi\left(\frac{\Delta\omega_3}{\omega_3} + \frac{\delta T}{\Delta T}\Big|_q\right) + \Delta\varphi^R \qquad (6.5)$$

where n is given by Eq. (6.2), δT is the intertap time delay error resulting from temperature, crystal orientation, or other errors, and $\Delta\varphi^R$ is a random component. The constant phase error term, $\Delta\varphi^K{}_q$, is then

$$\Delta\varphi^K{}_q = \sum_{q'=1}^{q-1} (\Delta\varphi^K{}_{q'} + \Delta\varphi^V{}_{p,q'}) \qquad (6.6)$$

Examination of Eqs. (6-5) and (6-6) reveal several error compensating techniques. First, since $\Delta\omega_3 = \Delta\omega_2 - \Delta\omega_1$ is the difference between reference and signal frequency errors, Doppler shift of a received signal may be offset by an equal shift of the reference frequency. A reference frequency offset may also be applied for time delay error compensation provided that the errors, $\delta T/\Delta T|_q$, are constant for all modules. The accumulated phase error, $\Delta\varphi^K{}_q$, may be independently cancelled by a compensating phase shift inserted between cascades. These compensating techniques may be of particular importance to long code PSK processing where accumulated phase errors seriously degrade the correlator performance.

If Eq. (6-1) is extended to encoded signal of total length PQ, the resulting signal, with errors included, becomes

$$\cdots A^E{}_{p,q}\, e^{E}{}_{p,q}\, X^E{}_{p,q}(\tau')\, e^{-j\Delta\varphi^E{}_{p,q}}\, \delta(t-t_{p,q}) \qquad (6.7)$$

where $t_{p,q} = [(q-1)P + (p-1)]\Delta T$. This encoded signal may be heterodyned back to the original signal frequency, $\omega_1{}^E$.

It will be convenient to use a single subscript, k, in describing the correlator cascade output, such that $k = (q-1)P + p$. The correlation output may be separated into two summations which describe the output before and after the desired correlation peak. For $0 \leq t \leq PQ(\Delta T)$, the output is given by

$$V_3{}^C(t)e^{j\omega_3{}^C t} = e^{j\omega_3{}^C t} \sum_{k=1}^{K} W_k(\tau')\, g^C{}_k\, g^E{}_{QP-k+K}\, e^{-j\Delta\varphi^T{}_k} \tag{6-8}$$

where

$$K = 1 \text{ to } PQ$$
$$W_k(\tau') = A^C{}_k\, A^E{}_{K-k+1}\, X^C{}_k(\tau')\, X^E{}_{K-k+1}(\tau') \tag{6-9}$$

and

$$\Delta\varphi^T{}_k = \Delta\varphi^C{}_k + \Delta\varphi^E{}_{K-k+1} \tag{6-10}$$

Following the correlation peak, for $PQ(\Delta T) \leq t \leq (2PQ-1)\Delta T$, we find

$$V_3{}^C(t)e^{j\omega_3{}^C t} = e^{j\omega_3{}^C t} \sum_{k=1}^{PQ-K} W_k(\tau')\, g^C{}_{k+K}\, g^E{}_k\, e^{-j\Delta\varphi^T{}_k} \tag{6-11}$$

where

$$K = 1 \text{ to } PQ-1$$
$$W_k(\tau') = A^C{}_{k+K}\, A^E{}_{PQ-k+1}\, X^C{}_{k+K}(\tau')\, X^E{}_{PQ-k+1} \tag{6-12}$$

and

$$\Delta\varphi^T{}_k = \Delta\varphi^C{}_{k+K} + \Delta\varphi^E{}_{p-k+1} \tag{6-13}$$

This formalism may be applied in general to any PSK sequence to be processed, whether generated actively or by a matched cascade Diode- Correlator circuit and is amendable to direct simulation by digital computer. The degree of waveform degradation is also a function of the particular PSK code (Ref. 28) in addition to the processor parameters considered above.

6.3 Theory-Experiment Comparison for a 2 Module, 256 Chip Cascade

The formalism developed in Section 6.2 is applied to the experimental 2 module 256 chip cascade described in Section 5.2.

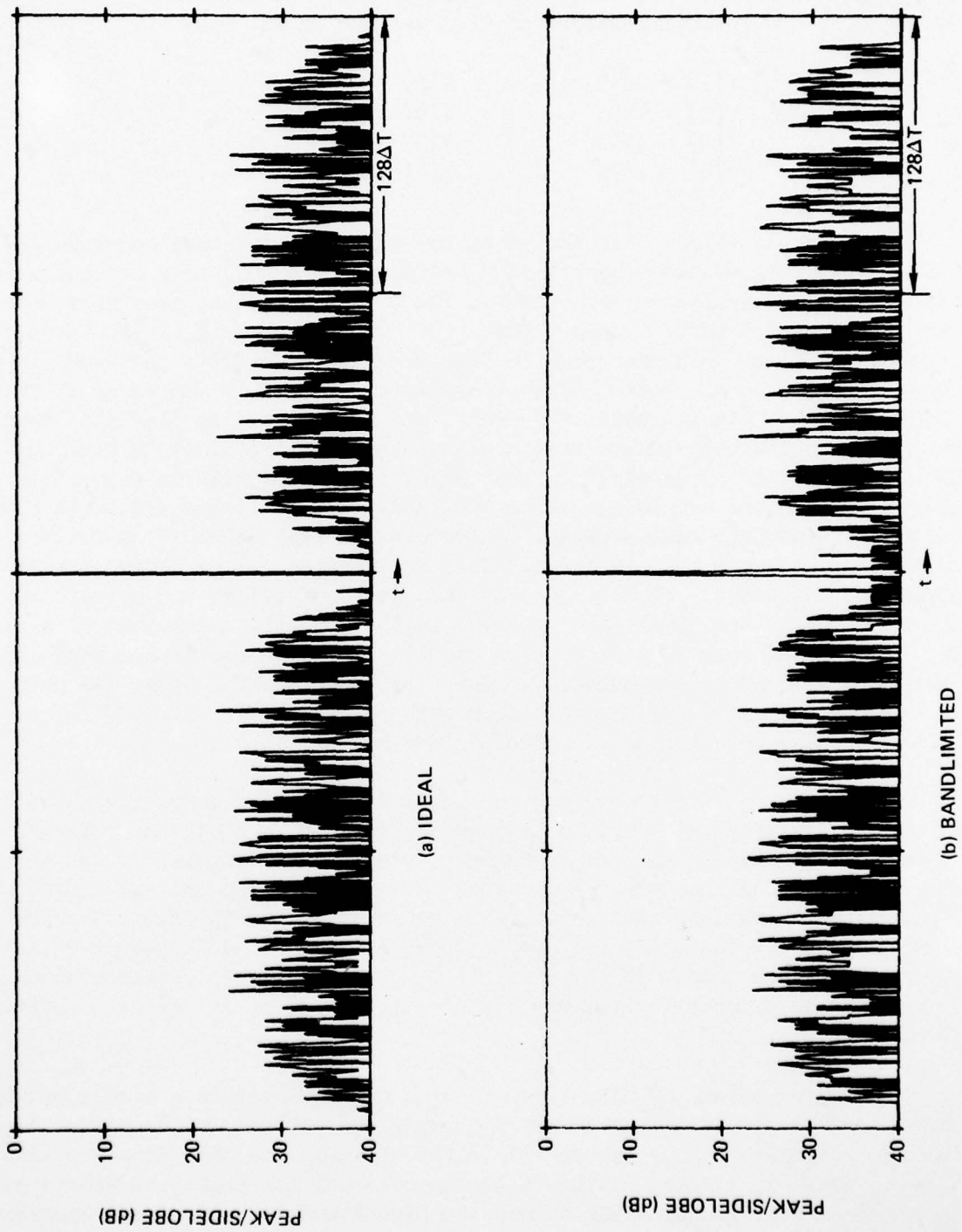
In the experiment, only random tap amplitude variations of $\pm$ 1.5 dB and chip rise time for each module (corresponding to $\gamma(q)$ from Eq. 6.4 of $\gamma(1) = .285$ and $\gamma(2) = .493$) were directly measured. Neglecting other system errors, the computed autocorrelation waveform for the same 255 chip M-sequence used in the experiments described in Section 5.2 is shown in Fig. 6-1(b) and compared with the ideal response of Fig. 6-1(a). The degraded peak to sidelobe response of 22 dB computed for the 64th sidelobe is in agreement with the experimental results of Fig. 5-9.

Unlike the ideal waveform, the first near-in sidelobes before and after the correlation peak have the same phase as the correlation peak and are 20 dB down. This results in the apparent widening of the peak since the first null in the response does not occur until the phase reversal between the 1^{st} and 2^{nd} sidelobes. The experimental near-in sidelobe response of 20.5 shown in Fig. 5-9 is in essential agreement with the prediction, however, intertap regeneration effects may also contribute to these 1^{st} trailing sidelobes. A reduction in the correlation peak by 1.8 dB is also predicted. The major contribution to the waveform degradation in this case was caused by bandlimiting. The 1.5 dB random amplitude variation contributed less than .1 dB degradation. Random phase errors of $\pm$ 1 degree were also considered with negligable waveform degradation.

6.4 The Effects of Bandlimiting on the Autocorrelation Response of an 8 Module, 1024 Chip Cascade Correlator

The effect of finite module bandwidth is considered when eight correlator modules, identical to the 128 tap devices constructed here, are cascaded to form a 1024 chip programmable correlator. From the results obtained in the 256 chip correlation response discussed in Section 6.3, as well as the work of others (Refs. 30, 33), bandlimiting must be considered in accurately predicting the cascade correlator response. However, its consequences are not severe for broadband delay channel design. As discussed in Section 6.2, the effect of bandlimiting was

FIG. 6.1



76–10–130–2

found by measuring the rise time of a pulse after each recirculation around a cascade delay channel and broadband compensating amplifier loop. These measurements resulted in the following values of $\gamma(q)$ defined in Eq. 6.4:

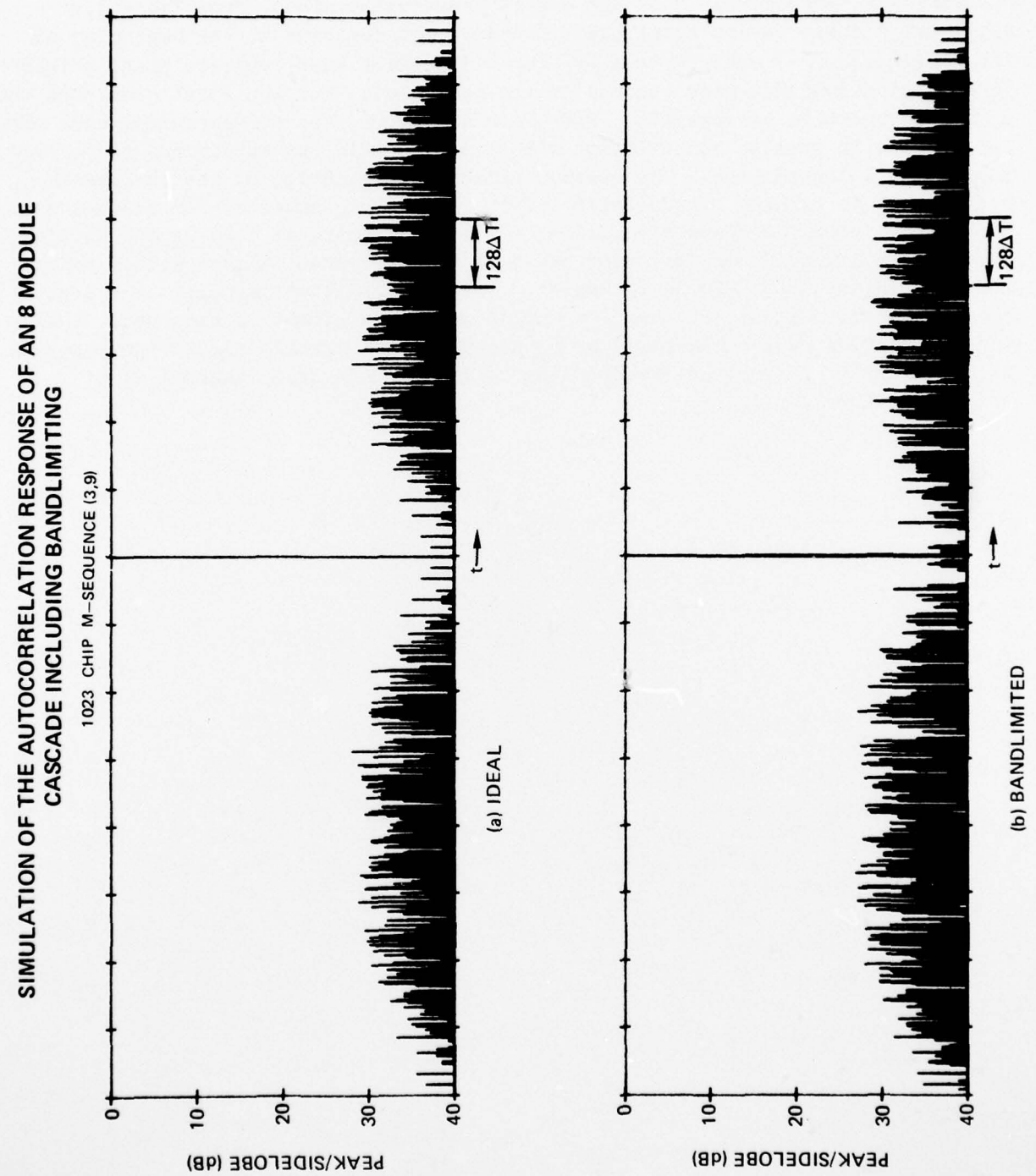
$\gamma(1) = .245$	$\gamma(5) = .7$
$\gamma(2) = .493$	$\gamma(6) = .737$
$\gamma(3) = .590$	$\gamma(7) = .786$
$\gamma(4) = .675$	$\gamma(8) = .798$

Using these values, and including the effect of the code sequence given in Table 3, the degraded autocorrelation response for a 1023 chip M-sequence was computed. The sequence used was computed for a shift register generator having feedback taps 3 and 9 added modulo 2 (Ref. 5). The computed ideal and bandlimited responses respectively are shown in Fig. 6-2 for an actively generated input sequence. The ideal peak to sidelobe ratio of 28.5 dB is decreased to 26.8 dB by bandlimiting. This degradation appears only in the leading sidelobe structure which has a generally larger envelope than the trailing sidelobe structure. This is understandable by considering that prior to the correlation peak, the individual chip contributions are larger since the bandlimiting effects are smaller than at, or following, complete code overlap. A correlation peak degradation relative to the ideal response of 3.1 dB is found. This degradation may be compensated for by adjusting the cascade channel gain at each stage of offset the average loss in that stage caused by bandlimiting. As found in the 255 chip simulation of Section 6.3, the correlation peak is widened as a result of equal phase of the peak and first leading and trailing sidelobes. At the first sidelobe position, the pulse width corresponds to a 13.7 dB decrease from peak response. The first nulls in the response occur at phase reversal between the 1^{st} and 2^{nd} sidelobes.

It is instructive to explore the cause of the above autocorrelation degradation, particularly the source of the apparent widening of the correlation peak and the change in phase of the first sidelobe. The simulation carried out above was for one specific 1023 chip burst M-sequence having a specific initial condition of the 10 stage shift register generator, namely (1000000000). The first 9 chips of the code produced by the shift register have equal phase, and the first 9 taps of the first correlator module of the simulation were programmed in that sequence. The remaining tap programming corresponded to the subsequently generated portion of the code.

The major effect of long runs of the same phase within a single module is found for the first leading or trailing sidelobe closest to the correlation peak. For these sidelobes, the tap code is offset by only one chip from the signal code. Within the first module, having long runs of equal tap phase, an excess correlation sum +25 is found, while within the eighth module, only a +3 excess is produced. In the ideal case, all taps contribute equally and the overall excess sum

FIG. 6.2


SIMULATION OF THE AUTOCORRELATION RESPONSE OF AN 8 MODULE CASCADE INCLUDING BANDLIMITING
1023 CHIP M–SEQUENCE (3,9)
PEAK/SIDELOBE (dB)
0
10
20
30
40
128ΔT
t
(a) IDEAL
(b) BANDLIMITED
76–10–130–1

of -1 is found, reversed in sign relative to the correlation peak. However, with bandlimiting, each module does not contribute equally since, from Table 3, neighboring chips having equal phase (a condition dominant at the beginning of the burst sequence) contribute a greater + increment than opposite phase neighbors (a condition dominant near the end of the sequence). For the first sidelobes then, an excess positive sum results. For other sidelobes, the corresponding code offset results in greater cancellation within each module separately and therefore less overall degradation. The overall effect is a widening of the correlation peak, which is perhaps the dominant effect intuitively expected for reduced system bandwidth. From the above discussion, the peak widening is code dependent with less broadening produced for codes having a greater phase balance within each module. In addition, the shift register initial condition may also be a contributing factor; however, further investigation of its effect is required. While the correlation peak broadening may be acceptable in certain system applications, its elimination by further broadbanding of the cascade delay channel is of primary interest.

7.0 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE DEVELOPMENT

Accurate, programmable PSK signal processing has been demonstrated using the two 128 tap PSK Diode Correlators developed under this program. Autocorrelation of burst bi-phase maximal length sequences having peak to sidelobe levels of 21 dB have been achieved, with 30 dB sidelobe suppression observed for the cyclic sequence autocorrelation response. When used as a PSK signal encoder, good phase balance and carrier suppression has been shown. As a result, the autocorrelation response using a PSK Diode Correlator Encoder pair was essentially undistinguishable from that achieved using an actively generated signal. Tap programming speed near 100 nsec has been measured. The low power dissipation within the taps ($\sim$ 6 μw/tap) is a particularly attractive property when small size and weight are important requirements. Even when the reference frequency generator is included, a total 128 chip, 10 MHz correlator power consumption of a few watts results which is considerably lower than that required with a digital approach (Ref. 15). The present chip rate of 9.8 MHz may be straightforwardly extended to rates approaching 100 MHz without significant increase in power consumption or device complexity.

Utilization of the nonlinear approach has been shown to provide an additional degree of flexibility to a PSK receiver through the capability for compensation of signal frequency offset or phase errors by electronic adjustment of the cw reference frequency. This capability allows restoration of the autocorrelation peak to sidelobe response which would otherwise be seriously degraded by Doppler shift or changes in the ambient temperature of the delay line. Input frequency shift of $\pm$3 MHz has been compensated by equal offset of the reference frequency with 3 dB degradation in the peak to sidelobe ratio. A reduced degradation due to changes in ambient temperature of the delay line is also predicted.

A cascade approach to long code PSK processing has been studied and demonstrated for a two module cascade circuit. The experimental results, together with simulation by digital computer, predict accurate signal processing of 1024 chip sequence using a cascade of 8 modules, identical to those tested here. The chief degradation is a predicted broadening of the correlation peak caused by bandlimiting within the cascade delay channel. Improvements in the correlator tap structure and broadband delay channel would further enhance the device performance by reducing the spurious level and bandlimiting effects.

While an 8 module 1024 chip cascade is feasible, cascades of many more modules are impractical because of increased power consumption, cost and complexity. An alternative technique is particularly attractive when correlating such very long sequences. This technique utilizes a single module and recirculating delay channel (Ref. 33) identical to those developed here. While the complete asynchronous operation available for the cascade approach is forfeited, a considerable reduction in system lock up time is still retained relative to an equivalent digital system.

In addition to phase programmability of the diode taps, control of the tap amplitude is also available by varying the magnitude of the dc current biasing the diodes. Amplitude control over a 30 dB dynamic range has been demonstrated in the single tap experiment described in Section 2.2. With both bi-phase and amplitude weighted taps, the device takes the form of a generalized transversal filter having equal tap weights and real coefficients. Programmable bandpass and notch filters having variable bandwidth may be synthesized with the center frequency controlled by the reference frequency offset. Complex tap weights may also be obtained using a pair of programmable frequency filters combined in phase quadrature. Such a device would be capable of correlating arbitrary nondispersive or dispersive waveforms such as PSK, Chirp Z or frequency hop signals and would represent a new state of the art in SAW device technology.

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This report describes an experimental and theoretical study of nonlinear tapped delay lines for use in electronically programmable, long code Phase Shift Key (PsK) signal correlation and encoding. The programmable delay line device studied here, which is called the PSK Diode Correlator, is a hybrid, Integrated Circuit device which utilizes a Surface Acoustic Wave (SAW) tapped delay line and an attached microelectronic diode and

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resistor array. PSK signal processing is accomplished at the P diode-taps of the signal processing region of the device by a low power, wide bandwidth, nonlinear mixing process. PSK input and cw reference voltages are applied to the delay line inputs at center frequency f_1 and f_2 respectively and the correlation output at the difference frequency is received at a common electrode summing the nonlinear outputs of the P diode taps. Rapid PSK code programming of the correlator taps is achieved by applying equal amplitude, positive or negative bias to the antiparallel diode pair located at each delay line tapping transducer. Each correlator module has an associated cascade delay channel fabricated on the same SAW substrate to allow interconnection with identical modules for long code PSK processing.

The design, fabrication and testing of 64 and 128 tap devices are described which utilize lithium niobate delay lines and silicon on sapphire diode and resistor arrays. These devices operate with signal and output frequencies near 70 and 30 MHz respectively and have delay line tap spacing chosen for processing PSK sequences with chip rates equal to, or a multiple of 9.8 MHz.

Operation of these devices as programmable PSK encoders and correlators is demonstrated with experimental results compared to theoretical behavior. Application to long code PSK signal processing is evaluated by testing a 2 module cascade. The detailed design of the broadband cascade delay channel is described. Systems applications including high speed reprogrammability, interference rejection and error compensation are demonstrated.

The effect of system errors on the correlation response of a multi-module long code PSK cascade processor is analyzed, and the effect of finite module bandwidth is discussed in a simulated 8 module, 1024 chip cascade correlator.