AFAL-TR-76-64

DIGITAL INSTRUMENTATION OF F-106 AIRCRAFT

REFERENCE SYSTEMS BRANCH
RECONNAISSANCE AND WEAPON DELIVERY DIVISION

MAY 1976

TECHNICAL REPORT AFAL-TR-76-64
FINAL REPORT FOR PERIOD 28 AUGUST 1975 - 15 JANUARY 1976

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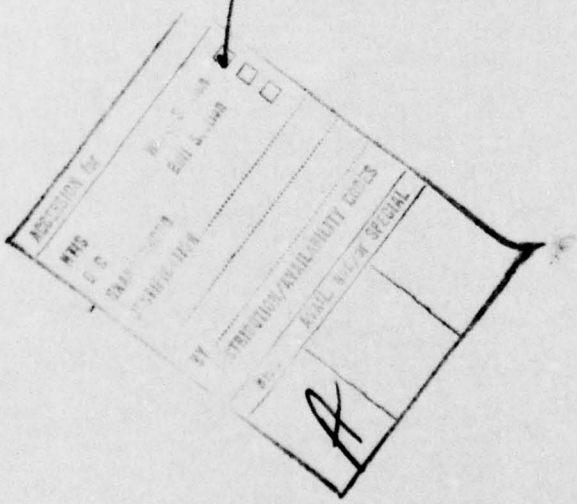

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1. REPORT NUMBER: AFAL-TR-76-64	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): DIGITAL INSTRUMENTATION OF F-106 AIRCRAFT.	5. TYPE OF REPORT & PERIOD COVERED: Final Report, 28 Aug 75 - 15 Jan 76
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Frederick Cruger, Captain, USAF Sammie L. Diles, Staff Sergeant, USAF	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Reference Systems Branch (RWA) Air Force Avionics Laboratory Wright-Patterson AFB, Ohio 45433	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 6095 95 03
11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Avionics Laboratory Wright-Patterson AFB, Ohio 45433	12. REPORT DATE: May 76 13. NUMBER OF PAGES: 63
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): 6095 95	15. SECURITY CLASS. (of this report): Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

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17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Digital Instrumentation
Avionics Computer Interface
F-106 Aircraft
HCM-204 (IRAM Computer)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This final report describes computer hardware and software provided by the Air Force Avionics Laboratory (AFAL) in support of the AFAL Comparative Gunsight Study. Two hardware interfaces and one special purpose fire-control-system computer program permitted transmission of digital data from the HCM-204 computer in F-106 aircraft to other on-board recording and computing systems. The all-digital instrumentation provided permanent record of the inputs and

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outputs of operating system software being tested. This system eliminates conversion and scaling errors generated in analog instrumentation.

FOREWORD

This final technical report was prepared in the Air Force Avionics Laboratory, Reconnaissance and Weapon Delivery Division, Reference Systems Branch, (AFAL/RWA-4), Wright-Patterson AFB, Ohio. The work was accomplished under Project Number 6095 "Inertial Reference and Guidance Technology," Task Number 609505 "Reference System Software Development" and Work Unit 60950503 "Gunsight Computer Interface." The effort was conducted during the time period 28 August 1975 through 15 January 1976. The principal investigators for the Air Force Avionics Laboratory were Captain Frederick Cruger and Staff Sergeant Sammie L. Jiles.

This report was submitted by the authors in March 1976.

Thanks are extended to 475th Test Squadron (Operational) personnel and to field engineering representatives of Honeywell, Inc. and Hughes Aircraft Corp. for their assistance in determining the operational instrumentation requirements.

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SECTION I

INTRODUCTION

1. PURPOSE

Work Unit 60950503 was initiated to support the Air Force Avionics Laboratory (AFAL) Comparative Gunsight Study conducted at Tyndall AFB, Fla. Under this work unit, the Reference Systems Branch (AFAL/RWA-4) provided computer hardware and software to enhance the performance of the F-106 aircraft instrumentation systems. Although the flight test is still under way, RWA-4 has fulfilled its obligations. This report describes the computer interface hardware and software and formally terminates Work Unit 60950503.

2. BACKGROUND

To perform accurately, the computing gunsights required certain information from the avionics systems. In the initial phases of the test, this information was available as a collection of analog signals that had been appropriately scaled by the aircraft instrumentation system. These signals were multiplexed and recorded on an analog recorder for post-flight analysis. A separate multiplexer and analog-to-digital converter (A/D) converted these signals into useable data for the gunsight digital computer (Figure 1).

The analog instrumentation tapes were sent to Eglin AFB, digitized, tabulated, and delivered to AFAL analysts at WPAFB. Unfortunately, much of this information did not correlate with known flight test results.

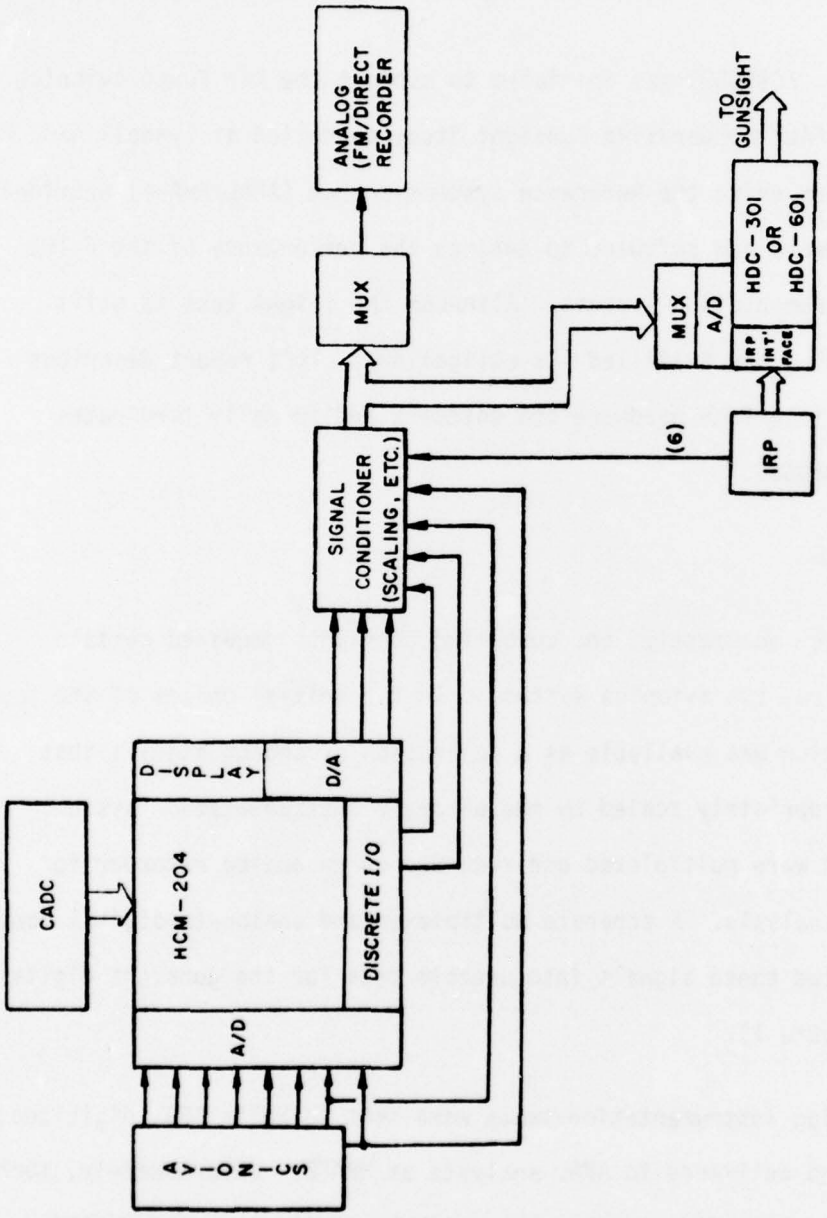

Figure 1. F-106 Hybrid Instrumentation System

Inaccuracies were attributed to the many A/D, D/A, and scaling conversions required for the hybrid (analog/digital) instrumentation and computing system. AFAL/RWA-4 provided two computer interfaces and one special purpose fire control system (FCS) computer program to permit all-digital instrumentation.

3. HARDWARE DESIGN PHILOSOPHY

All hardware was built from readily available integrated circuits (IC's) so that failures might be easily repaired. All IC's were mounted in sockets for ease of replacement; this incurred an increase in parts cost, but permitted maintenance and design alterations which otherwise would have been impossible. The computer interfaces were wire-wrapped, rather than soldered, to facilitate corrections and modifications during and after checkout. All wiring was performed by AFAL/RWA-4 at WPAFB. The completed interfaces were delivered to Tyndall AFB with schematic drawings and wire lists for input/output (I/O) connections.

4. SOFTWARE DESIGN PHILOSOPHY

The HCM-204 FCS Computer in the F-106 test aircraft required a special instrumentation computer program to transmit digital information to the gunsight computer and the instrumentation system. AFAL/RWA-4 provided a program that could be readily modified. The number and types of data words transmitted by the HCM-204 could be altered simply by changing a list of I/O parameters within the program; no changes to the actual program structure were necessary. This facilitated field changes as instrumentation requirements changed and allowed the same instrumentation

program to be used on other F-106 test aircraft with different instrumentation requirements. Also provided was an assembly language program and computer facilities at Tyndall were used to obtain a punched paper tape which could be loaded on the HCM-204. Instructions for modifying the program were given to engineering personnel at Tyndall AFB.

SECTION II

THEORY OF OPERATION

1. HCM-204 OUTPUT INTERFACE

The HCM-204 was an integral part of the F-106 FCS but had no requirement to transmit conventional parallel digital data to other devices. It did, however, have a limited number of one, two, and four bit I/O space +28vdc discretes and an 18-bit display register which was under software control. This was the only accessible output of parallel digital words.

AFAL/RWA-4 provided the circuitry shown in block diagram form in Figure 2. Optical isolators were used to convert the +28vdc display light outputs to 5vdc signals compatible with standard transistor-transistor logic (TTL) circuitry. Differential line drivers were used to transmit the information from the FCS computer (in the nose of the aircraft) to the instrumentation system (in the weapons bay). Differential line receivers converted the information back to single-ended TTL signals; these signals were used as parallel inputs to the computer interfaces.

The 11 least significant bits (LSB) were also connected to inputs of a 16 channel multiplexer (parallel-to-serial converter, or "mux"). The other five mux inputs were hard-wired to a specific inputs sequence. Using a 16KHz clock to count through the 16 inputs, a serial data train was obtained; 11 data bits were followed by five synchronization (sync) bits. Each time the mux began the sync pattern, a +28vdc discrete was sent to the HCM-204. Upon receiving this signal, the

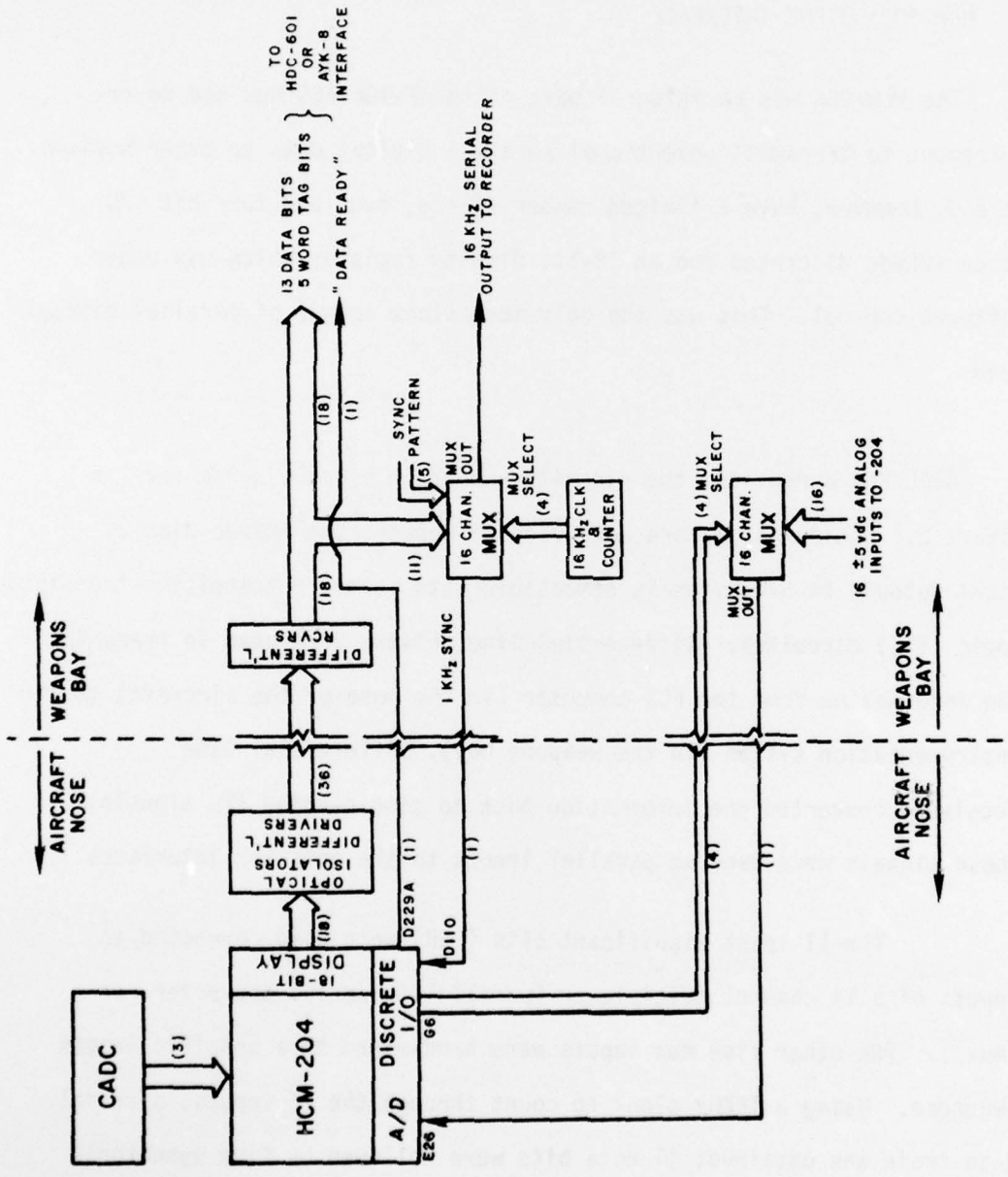

Figure 2. HCM-204 Output Interface

special FCS computer program caused a new data word to be sent to the display register. When the mux completed the sync pattern, it again sent 11 bits serially to the recorder and again followed them with a sync pattern. The mux generated a continuous 16KHz serial output; each set of data bits represented a new data word from the HCM-204. The word transfer rate from the HCM-204 to the instrumentation system was thereby fixed at 1KHz.

A feature was included in the interface which permitted HCM-204 digitization of analog signals normally not connected to the HCM-204 A/D inputs. A second 16-channel analog mux was built; it selected inputs as designated by a four-bit discrete output from the HCM-204 and transmitted them to an unused A/D input (E26). They then could be digitized and sent to the display register.

AFAL/RWA-4 designed, built, and tested the HCM-204 output interface shown in Figure 2. Field checkout and installation in the aircraft was performed by the 475th Test Squadron at Tyndall AFB.

2. HCM-204 INSTRUMENTATION PROGRAM

AFAL/RWA-4 provided one special purpose computer program to enable the HCM-204 to transfer parallel digital data to the instrumentation system through the display register. A flow diagram is shown in Figure 3. The actual assembly language listing is included in Appendices A and B. The code was not designed to minimize core requirements; it was written in a form that allowed straightforward modification.

The program read specified data from the A/D inputs and from the Central Air Data Computer (CADC). These data were presented as 12-bit data words, each with a unique five-bit tag, to the 18-bit display register. Each word was held in the display for one millisecond, since the cyclic select/read/display process was synchronized by a 1KHz signal from the HCM-204 output interface.

The punched paper tape was designed to be loaded as a "change tape" on the HCM-204. It made two basic changes to the normal FCS program: 1) it loaded the instrumentation program into a normally unused memory drum block (Block 2 of Channel 16_8), and, 2) it altered the program executive (Channel 0) to force entry into the instrumentation program when "Homing Point T" was selected in the cockpit.

The addition to Channel 0 caused a four-bit discrete input (G83) to the HCM-204 to be read. If G83 = 1011 (13_8), Block 2 of Channel 16_8 was read from the drum and control transferred to the instrumentation program. If G83 $\neq 13_8$ (i.e., Homing Point T not selected), normal program operation was resumed.

The entire instrumentation program was included in the addition to Channel 16_8; program operation is best described by the flow diagram in Figure 3. Each time the sync pulse (D110) from the output interface hardware went "high" (i.e., +28v, logical "1"), the program sent a new data word to the display register and set an output discrete (D229A) "high", indicating a valid output ("data ready" in Figure 2). A new input was then selected, any necessary A/D conversion performed, and the program would wait for the sync pulse to go "low." When D110 went

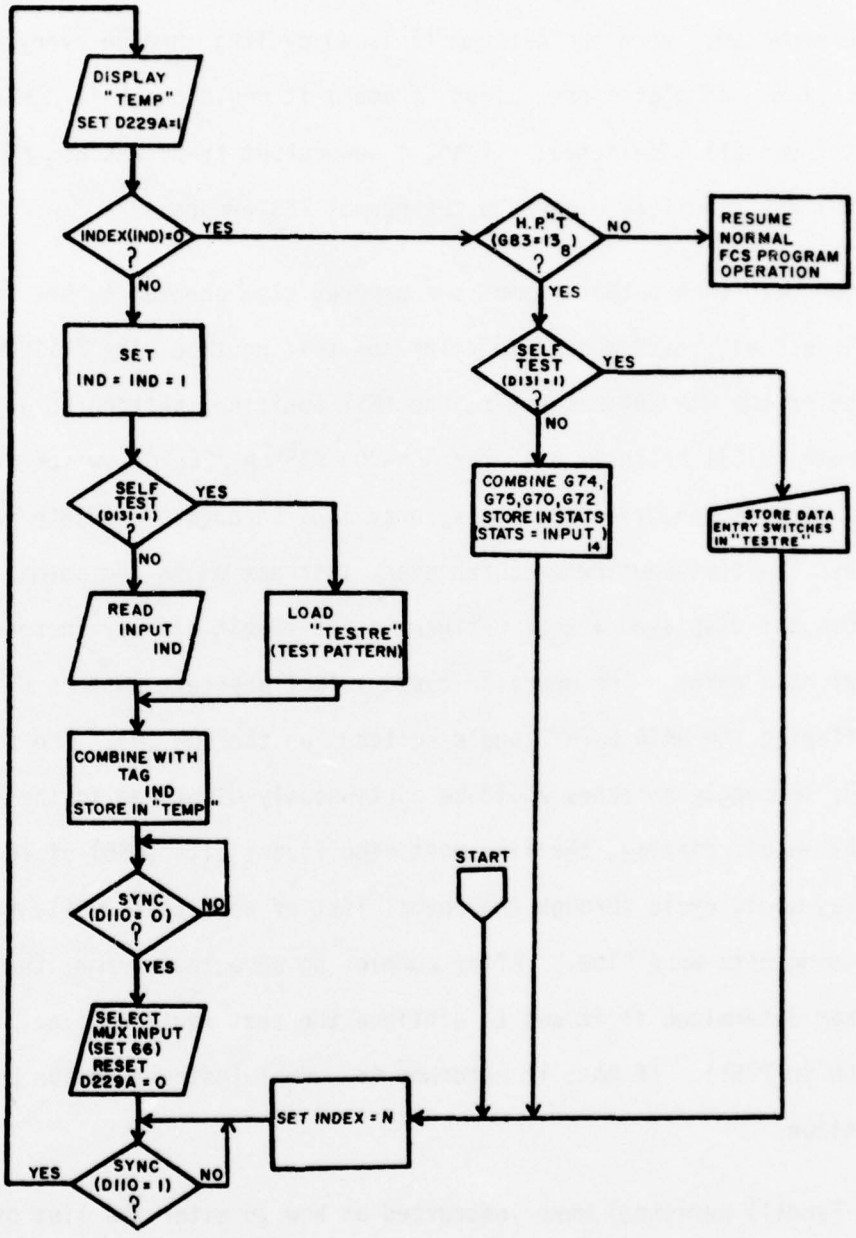

Figure 3. HCM-204 Instrumentation Program Flow Chart

"low", D229A was reset. When D110 again went "high", the new data word was sent to the display, D229A was again set "high", and the entire cycle repeated. When the program finished cycling through every data word, (i.e., completed one output "frame") it would check if Homing Point T was still selected. If so, a new output frame was begun. If not, control was transferred back to the normal FCS program.

Between each output frame, the program also checked to see if it was in a "self test" mode. To enter the test routine, the TEST/NORM switch on the HCM-204 was set to the TEST position, setting an input discrete (D131) "high." With the HCM-204 DISPLAY SELECT switch in the SWITCHES position, the program began cycling through a complete output frame. The test routine executed every instruction in the normal program but displayed a test pattern in the 18-bit display instead of the normal data words. The operator could select any test pattern simply by positioning the DATA ENTRY toggle switches on the HCM-204. The positions of the 10 toggle switches would be continuously displayed in the 10 LSB's of the 18-bit display, the five most significant bits (MSB) of the display would cycle through the normal list of word tags, while the three remaining bits were "low." After completing an output frame, the program determined if it was to continue the test routine (i.e., TEST/NORM switch in TEST). If not, it returned to normal instrumentation program operation.

Tyndall personnel were instructed on how to alter the list of data sent to the computer interfaces through the display. To add a new data word, they must: 1) add the corresponding input instruction to the program list called "TABLE OF INPUT INSTRUCTIONS"; 2) indicate to which

input (if any) of the 16 channel mux the analog data is connected, by making the appropriate entry in the "TABLE OF E26 INPUT MUX SELECT CODES", and; 3) add one to the value of N, under "TEMPORARY STORAGE LOCATIONS". They must remember that each entry in the "TABLE OF INPUT INSTRUCTIONS" is associated with the corresponding entires in the "TABLE OF ... MUX SELECT CODES" and the "TABLE OF OUTPUT WORD TAGS". In the AFAL/RWA-4 program, the maximum number of output words per frame (N) is 27_8; any larger N would cause the three tables to overlap in memory. The tables could be spread out to permit longer lists.

3. HDC-601 DMA INTERFACE

In one of the Tyndall F-106 test aircraft the output of the HCM-204 was sent to the direct-memory-access (DMA) input of a Honeywell HDC-601 minicomputer in the weapons bay. Figure 4 shows a block diagram of the HDC-601 DMA interface built by AFAL/RWA-4. The circuitry permitted 1) HCM-204 outputs to be loaded into the HDC-601 memory (i.e., a DMA "Write") and, 2) HCD-601 memory contents to be sent to a digital magnetic tape recorder (i.e., a DMA "Read").

a. DMA Write

The 13 data bits from the differential line receivers were connected directly to the DMA data input lines ("DATA1-DATA13"). The five word tag bits were connected to tri-state gates whose outputs were connected to the five LSB of the DMA memory address lines. When the HCM-204 set D229A "high", a DMA Write Request ("WRITE" in Figure 4) was sent to the HDC-601. WRITE also enabled the tri-state gates, so

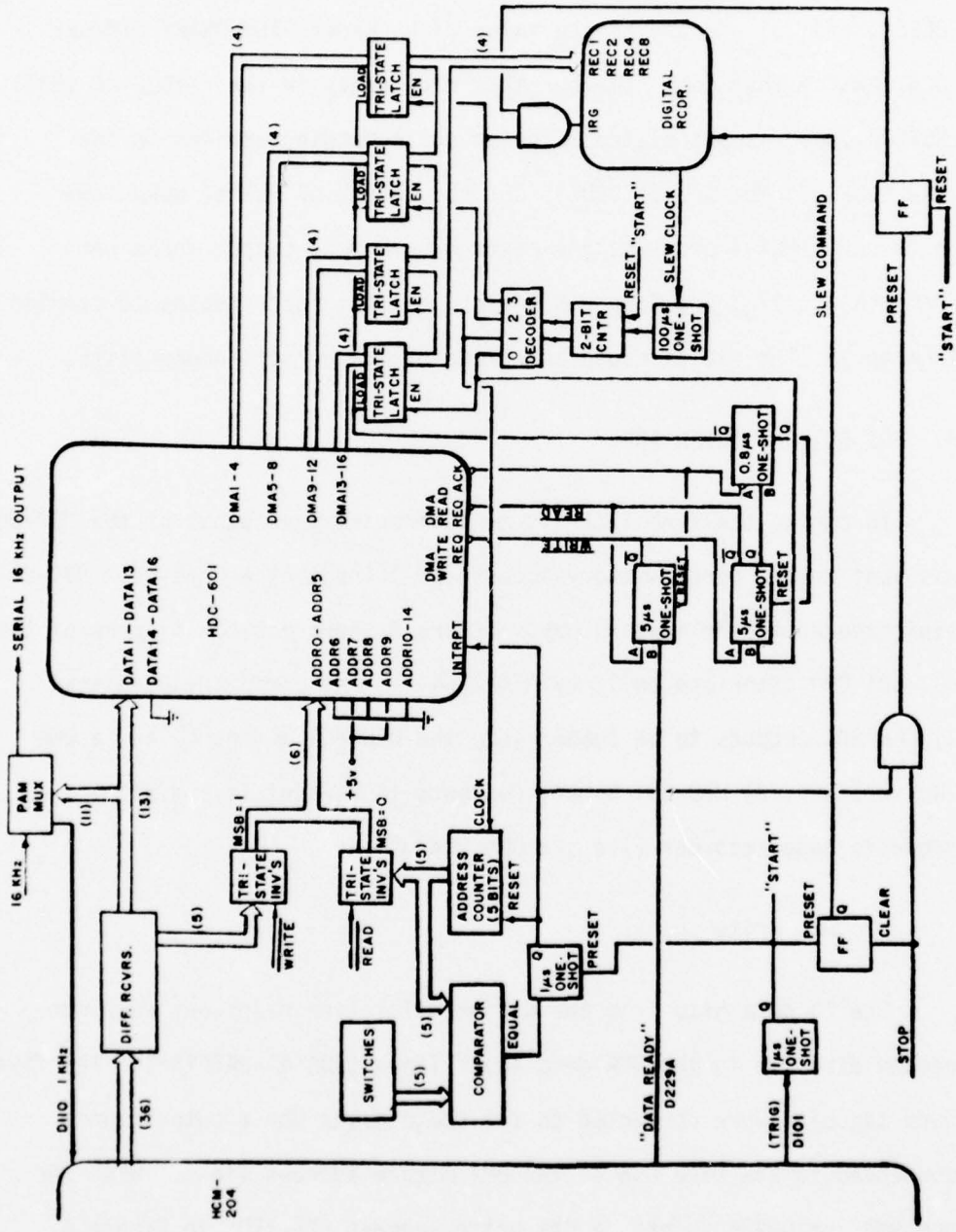

Figure 4. HDC-601 DMA I/O Interface

the word tag bits controlled the memory address being loaded; since each 18-bit data word from the HCM-204 contained a unique 5-bit word tag, each variable (attitude, radar range, airspeed, etc.) was effectively assigned a particular HDC-601 memory location. Operating software in the HDC-601 merely had to read these predetermined locations to obtain the latest values of the corresponding variables.

b. DMA Read

The digital tape recorder recorded 16-bit words from the HDC-601 as four 4-bit bytes. The recorder generated 2 KHz "SLEW CLOCK" pulses; each pulse represented a "request" from the recorder for the next four bits to be recorded. The SLEW CLOCK was the input to a 2-bit counter/decoder combination, which in turn controlled a 16-line-to-4-line multiplexer. As shown in Figure 4, "0" from the decoder generated a 0.5μs "DMA READ REQUEST". When the HDC-601 acknowledged the request, the interface delayed 0.8μs and then loaded the four tri-state latches with the DMA output ("DMA 1" through "DMA 16"). The contents of each latch were transmitted to the recorder as each succeeding "SLEW CLOCK" pulse caused the decoder to increment. Every fourth pulse, another DMA READ REQUEST was generated and another 16-bit word from the HDC-601 memory was loaded into the latches.

To determine which memory word was to be read from memory, the HDC-601 examined the 16 address lines. During a "DMA WRITE" the HCM-204 controlled the address lines, but during a "DMA READ" the address lines were controlled by the five-bit "address counter" in Figure 4. This counter was incremented every fourth "SLEW CLOCK" pulse. Successive "DMA READ REQUESTS" thereby resulted in words from successive memory locations

being sent to the recorder. Using the "SWITCHES" in Figure 4, the system user selected how many different words (up to 31) were to be sent to the recorder. When this number had been sent, an interrupt ("INTRPT") was sent to the HDC-601 to request that the values of the words be updated before the next output frame was begun. As long as the interface received "SLEW CLOCK" pulses, the HDC-601 continued to cycle through the block of memory assigned to data being recorded. When the interface received a "STOP" command, the current output frame was completed. However, as the last byte of the last word was recorded, an inter-record gap (IRG) command was sent to the recorder; this generated an IBM-compatible IRG, stopped "SLEW CLOCK" pulses, and halted the tape transport. A "START" command was necessary to again begin recording data from the HDC-601.

c. Control

The DMA interface was built so that a single TTL "START/STOP" signal could be used, or a "START" could be generated from the trigger on the aircrew hand control (D101) and a "STOP" generated by the HDC-601. The circuit implementation also prevented simultaneous "DMA WRITE" and "DMA READ" requests since the address lines were common to both. Detailed schematics were delivered to Tyndall so that modifications could be made if operational requirements were changed. The schematics are also included in Appendix C.

4. AYK-8 INPUT INTERFACE

Because operational aircraft generally did not have computers with the DMA capability of an HDC-601, the AFAL Comparative Gunsight study

also required a means of transmitting data from the HCM-204 to a relatively simple computer, such as an AN/AYK-8. AFAL/RWA-4 provided the interface shown in block diagram form in Figure 5.

a. Memory

Since neither the HCM-204 nor the AYK-8 have an interrupt capability, the interface had to provide for asynchronous reception and transmission of data. The interface was essentially a buffer memory; the HCM-204 entered data whenever it was ready and the AYK-8 could read data from the memory when required. The interface used the 18-bit words from the HCM-204 output interface; the 12 LSB's were treated as data while the five MSB's (word tag" determined into which interface memory location the data were loaded. Since the HCM-204 instrumentation program assigned a consistent, but unique, word tag to each variable, the AYK-8 programmer had a priori knowledge of the interface memory location of each variable. To provide operational flexibility, the interface had two input modes and two output modes under which data could be written into or read from the memory.

b. Input Control

The "MODEH" signal in Figure 5 determined under which mode the HCM-204 could enter data into the interface memory. With "MODEH=1", the input holding register was loaded when "REQH=1", and the 12 data bits were loaded into the memory. In this mode, the "DATA READY" signal of Figure 2 was connected to "REQH". If, however, the discrete signals for MODEH and REQH were not available, "MODEH" could be grounded (i.e. MODEH=0), REQH connected to 5vdc (REQH=1), and the interface

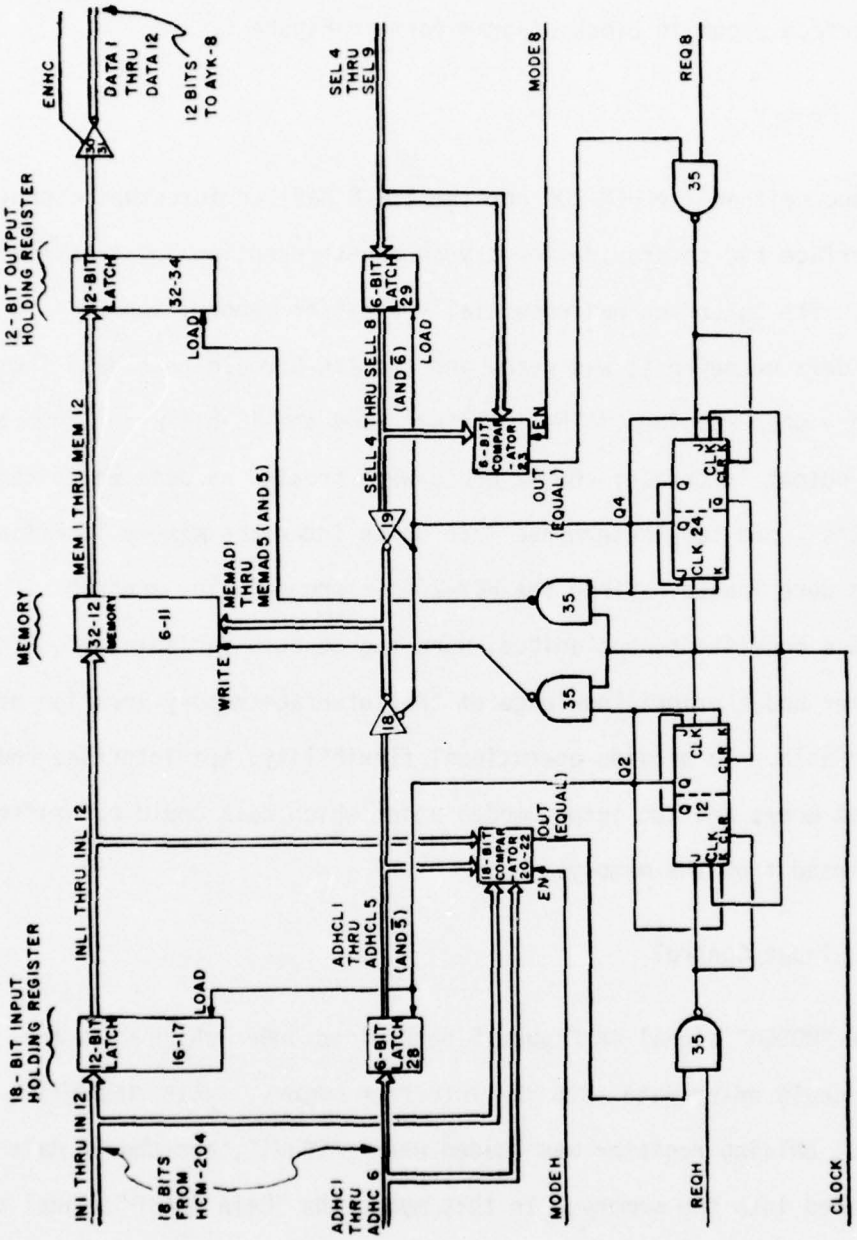

Figure 5. HCM-204/AYK-8 Interface

memory loaded data whenever one or more bits of the 18-bit input changed. This was done by comparing the input lines to the input holding register contents. When they were different, the interface loaded the new word into the holding register and into the designated memory location. The synchronous flip-flops in Figure 5 prevented line transients from causing erroneous entries in the memory.

c. Output Control

The "MODE8" signal in Figure 5 determined under which mode the AYK-8 could read data from the interface memory. Its operation was analogous to that of "MODEH". With "MODE8=1" the output holding register was loaded when "REQ8=1", the 12 data bits being read from the location selected by a six-bit AYK-8 output (SEL4 through SEL9). If, however, the discrete signals for "MODE8" and "REQ8" were not available, they could be preset to 0 and 1, respectively, and the output holding register was loaded whenever one or more bits of the six-bit "select" from the AYK-8 changed.

d. Strapdown IRP Interface

The AYK-8 was also required to monitor the outputs of a H-478 strapdown inertial reference package (IRP). Three channels of velocity information (ΔV_x, ΔV_y, ΔV_z) and three channels of angular attitude information ($\Delta\theta_x$, $\Delta\theta_y$, $\Delta\theta_z$) were generated by the IRP. The numeric data was gathered by counting pulses over a time interval; each pulse represented an incremental change in velocity (ΔV) or attitude ($\Delta\theta$). The interface included six counters each driven by one of the data inputs. When the AYK-8 read one of the channels, the value of the counter was

loaded into an output holding register and the counter was reset to zero. The counter accumulated pulses until the AYK-8 again caused its contents to be loaded into the output register and then zeroed.

The pulse outputs and master clock were received by differential line receivers, as shown in Figure 6. The outputs of the tri-state output holding registers were connected to the same AYK-8 input lines as the HCM-204/AYK-8 interface. When "SEL1-SEL3=0", "ENHC" enabled the tri-state inverters in Figure 5, so "SEL4-SEL9" selected words from the interface memory. When "SEL1-SEL3≠0", "SEL1-SEL3" selected which channel of inertial data was sent to the AYK-8 by generating the proper enable signals (outputs of the decoder in Figure 6). The AYK-8 therefore required nine select lines to read inputs from both the IRP and the HCM-204.

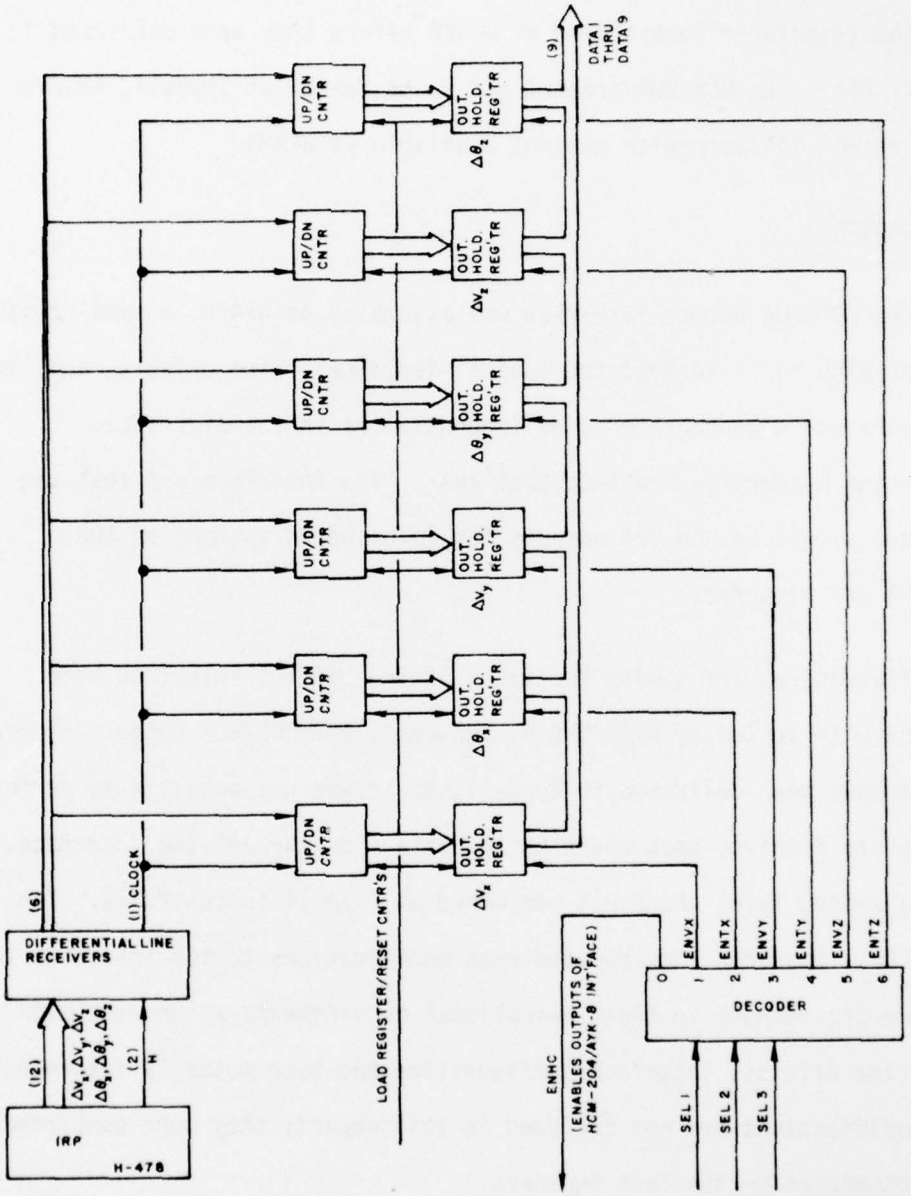

Figure 6. Strapdown IRP Interface

SECTION III

RESULTS AND CONCLUSIONS

The interfaces were tested at WPAFB before they were delivered to Tyndall AFB. The HCM-204 program had to be tested at Tyndall, however, since an HCM-204 assembler was not available at WPAFB.

1. HARDWARE

The HCM-204 output interface was assembled at WPAFB; a small test set was also built so that the optical isolators, line drivers, and line receivers could be operated simultaneously (as in the aircraft), permitting a complete front-to-back test. The interface and test set provided simulated HCM-204 outputs for later bench testing of the HDC-601 DMA interface.

The control and timing functions of the HDC-601 interface were successfully tested by AFAL/RWA-4. However, the HCM-204 output interface had already been delivered to Tyndall, so it was not possible to perform a complete front-to-back check on the data flow through the interface. Such a system level check was performed at Tyndall successfully. The 475th Test Squadron incorporated some modifications to the interface to accommodate changes in their operational requirements which were made after the original interface configuration had been mutually determined. The modifications are not included in this report; they were completed and documented by the Test Squadron.

The AYK-8 input interface was tested on the AFAL Mobile Evaluation Laboratory (MEL). The MEL PDP-11/40 minicomputer simulated HCM-204

outputs and AYK-8 inputs. The interface received, stored, and transmitted data as designed. The IRP interface was tested by connecting its inputs to the strapdown IRP, and monitoring the six up/down channels with a laboratory counter. The commercial counter was used because sufficient counter and output register IC's were not available. Test results indicated that the interface performed as designed.

The hardware interfaces allow transfer of data from the aircraft avionics computer to several digital instrumentation/data processing systems. They eliminate the necessity for the A/D and D/A conversions of a hybrid system. Digital recording also eliminates the errors attributed to analog recording and reproducing. Computerized tabulation of the instrumentation data is also facilitated. Perhaps the largest payoff, however, is that the digital instrumentation provides a permanent record of the precise inputs and outputs of the operating software in the gun-sight computer.

2. SOFTWARE

The HCM-204 instrumentation program was tested on the maintenance mock-up at Tyndall. A 1KHz synchronization pulse was connected and the mock-up HCM-204 transferred data to the display successfully. The self-test routine was checked and verified. The memory drum of the aircraft was loaded with the instrumentation program and tested successfully in the mock-up computer. Testing on the aircraft will be completed by Test Squadron personnel.

The RWA-4 instrumentation program occupies 100% of the HCM-204 duty cycle, so normal FCS computations are not performed when the special

program is operating. For the Comparative Gunsight Study, this is of no consequence, since the HCM-204 serves no useful purpose during gun operation. If, however, the HCM-204 is required to perform some of its normal functions and digital instrumentation is still desired, an extensive effort would be required to interlace instrumentation and avionics software. In fact, such an integration may not be practicable, or even possible.

3. CONCLUSION

The hardware and software provided will fulfill the requirements of the AFAL flight tests being conducted at Tyndall. Both hardware and software may be easily modified to accommodate changes in operational requirements. In particular, the HCM-204 instrumentation program and output interface allow digital data transmission for a virtually unlimited number of flight test applications.

APPENDIX A

ASSEMBLY LANGUAGE LISTING

This appendix includes the entire assembly language program developed by AFAL/RWA-4. The listing was obtained from the IBM cards used to create the actual program tape. Comment cards were included to denote program flow.

The discrete HCM-204 inputs used for program control are listed under "DIGITAL INPUTS AND OUTPUTS USED FOR PROGRAM CONTROL". The significance of the status word bit configuration is described under "STATUS WORD CONFIGURATION".

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**
**
**
**      COMPATIBLE WITH THE -29 TAPE IN A/C 778
**      LOSCG INSTRUMENTATION TEST ROUTINE
**      ACTUATED BY SELECTING HOMING POINT T
**      CAPT FREDERICK CRUGER  AIR FORCE AVIONICS LABORATORY
**      19 NOV 75
**
**      PROGRAM ENTRY SEQUENCE IN CHANNEL 0
**
**      CHANNEL 0 SECTOR 675
**
        ORG 675
        TRA AUTOL       TRANSFERS TO AUTO-LOCK ROUTINE
**
**      CHANNEL 0 SECTOR 745
**
        ORG 745
AUTOL   CLA 3140        LOADS H SUB I
        SAU /A66
        LXI 0014
        FXB 001,2
        RDI /G83        READS D175-D178
        SUB CONST       TESTS FOR /G83 = 13
        INZ OUT
CHUMOD  RDB 0,5,10
        TRA 00
OUT     CLA 3441        PREPARES TO RESUME NORMAL MA-1 PROGRAM OPERATION
        TRA 676
CONST       0013
**
**
**      CHANNEL 10 SECTOR 400
**
        ORG 0
START   LXA M           LOADS INDEX WITH NUMBER OF WORDS IN INPUTS TABLE
        SML
        TRA LOOP        ENTERS LOOP TO WAIT FOR FIRST SYNC PULSE INPUT
DISP    DRL TEMP        TRANSFERS NEW OUTPUT WORD TO DISPLAY REGISTER
        CLA DMARE       LOADS DMA REQUEST
        WDU /G5         SETS DMA REQUEST
        TIX READ        GOES TO READ A NEW WORD IF INDEX IS NOT ZERO
        TRA RESTRT      GOES TO RESTRT WHEN OUTPUT FRAME COMPLETE (INDEX=0)
READ    NOP             THIS INSTRUCTION INSERTED FOR EACH DIFFERENT WORD
READ1   NOP
READ2   NOP
READ3   ANA BLANK       BLANKS 7 MSB OF DATA WORD
        ADD TAG         TAGS THE DATA WORD FOR OUTPUT TO 601
        STO TEMP
HOLD    RDI /G71        READS SYNC PULSE INPUT
        ANA BLANK
        TNZ HOLD        IF SYNC PULSE = 0, PROGRAM CONTINUES TO LOOP
        CLA ZERO        LOADS 0
        WDU /G5         CLEARS DMA REQUEST
LOOP    CLA*MUX         SELECTS ANALOG MUX INPUT TO F26
        WDU /G6         SENDS SELECT CODE TO ANALOG MUX
INPIN   CLA*INPUTS
        STO READ        INSERTS NEW INPUT INSTRUCTION IN READ
        CLA*TAGS        SELECTS WORD TAG FOR NEXT DATA WORD
        STO TAG
CHAN    RDI /G71
        ANA BLANK       BLANKS ALL EXCEPT SYNC BIT INPUT
        TN2 DISP        GOES TO DISPLAY STEPS WHEN SYNC BIT = 1
        TRA CHAN        READS SYNC BIT INPUT AGAIN IF IT  = 0
```

```
**
**      CHECK HOMING POINT SELECT TO SEE IF SPECIAL PROGRAM IS TO CONTINUE
**
        ORG 40
RESTRT  LAI 0014          READS D116
        TXB 0011,2        CHECKS TO SEE IF D116 = 0
        RDI /G83          READS D175-D178
        SUB CONST1        CHECKS TO SEE IF D175-D178 = 13
        TNZ 0011
        TRA TEST          GOES TO CHECK TEST/NORM SWITCH
OUT1    ISK /SRORU        PREPARES TO RESUME NORMAL MA-1 PROGRAM OPERATION
        RUB 0,0,1         READS CHANNEL 0 BACK IN (D116 = 0)
        TRA 00
**
**      PROGRAM ROUTINE TO CHECK TEST/NORM SWITCH
**
        ORG 60
TEST    LAI /G76
        TXB TEST1,0
        CLA NORMIN
        STO INPIN         INSERTS NORMAL DATA INPUT INSTRUCTION
        TRA STATUS        GOES TO CHECK STATUS WORD
TEST1   CLA TESTIN        SELECTS TEST PROGRAM (DIGIN) ENTRY INSTRUCTION
        STO INPIN         INSERTS TEST PROGRAM (DIGIN) ENTRY INSTRUCTION
        TRA START         STARTS NEW OUTPUT FRAME
**
**      PROGRAM ROUTINE TO GENERATE TEST INPUTS USING 140 UNIT SWITCHES
**
        ORG 100
DIGIN   TRA 00
        RDI /G86
        ALS 6
        STO INTEMP
        RDI /G84          READS D180-183
        ANA THREE         BLANKS ALL BUT D182-D183
        ALS 0004
        ADD INTEMP        COMBINES D165-D168 WITH D182-D183
        STO INTEMP
        RDI /G87          READS D170-D173
        ADD INTEMP        ACCUMULATOR NOW HAS SWITCH INPUTS IN 10 LSB
        STO INTEMP
        CLA TESTRE        PUTS TEST DATA INPUT INSTRUCTION IN ACCUMULATOR
        TRA DIGIN         RETURNS TO THE MAIN PROGRAM
**
**      PROGRAM ROUTINE TO FORM STATUS WORD
**
        ORG 120
STATUS  RDI /G74          READS /G74
        ALS 4
        STO STATS
        RDI 0012          READS /G75
        ADD STATS         COMBINES /G74, /G75 INTO BITS 8 - 1
        ALS 1
        STO STATS
        RDI 0005          READS /G70
        ARS 3             LEAVES D101 (TRIGGER 2) IN BIT 1
        ADD STATS         COMBINES /G74, /G75, D101 INTO BITS 9 - 1
        ALS 1
        STO STATS
        RDI 0007          READS /G72
        ARS 3             LEAVES D103 (1R TRACK) IN BIT 1
        ADD STATS         COMBINES /G74, /G75, D101, D103 INTO BITS 10 - 1
        STO STATS         STORES COMPLETE STATUS WORD IN STATS
        TRA START
```

```
**      STATUS WORD CONFIGURATION
**
**      BIT 10  D105  NOT SEARCH
**      BIT  9  D113  RTUF
**      BIT  8  D121  DHOT
**      BIT  7  D129  ATUT
**      BIT  6  D106  VIS IDENT
**      BIT  5  D114  MAN PUR
**      BIT  4  D122  AHM
**      BIT  3  D130  SPECIAL WEAPON
**      BIT  2  D101  TRIGGER 2
**      BIT  1  D109  IR TRACK
**
**
**      TABLE OF INPUT INSTRUCTIONS
**
        ORG 150
INPUTS  NOP
        RAI /A9         ANGLE OF ATTACK
        RDG /0373       MACH
        RDG 0057        ALTITUDE
        RDI /0353       RADAR RANGE
        RAI /E17A       SIN ELEVATION
        RAI /E18A       SIN AZIMUTH
        RAI /E19        SIN PITCH
        RAI /E21        SIN ROLL
        RAI 0041        READS /E15N  DEL D
        RAI 0042        READS /E16N  DEL E
        RAI /A10        IMPACT TEMPERATURE
        RAI 0055        READS /E26  IR AZ RATE
        RAI 0055        READS /E2o  IR EL RATE
        CLA STATS       STATUS WORD
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
        CLA INPUTS      ZERO (SPARE)
**
**      TABLE OF E2o INPUT MUX SELECT CODES
**
        ORG 200
MUX     NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
            020000      E2o INPUT MUX CHANNEL 1
            000000      E26 INPUT MUX CHANNEL 0
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
```

```
**
**      TABLE OF OUTPUT WORD TAGS
**
        ORG 230
TAGS    NOP
            000000
            020000
            040000
            060000
            100000
            120000
            140000
            160000
            200000
            220000
            240000
            260000
            300000
            320000
            340000
            360000
            400000
            420000
            440000
            460000
            500000
            520000
            540000
**
**      TEMPORARY STORAGE LOCATIONS
**
        ORG 260
INTEMP  NOP
N           0017        NUMBER OF OUTPUT WORDS PER FRAME
STATS   NOP
TAG     NOP
TEMP    NOP
CONST1      0013
BLNK        017777      BLANKS 5 MSB OF DATA WORD
BLANK       0000
THREE       0003
DMARE       200000
ZERO        0000
NORMIN  CLA*INPUTS
TESTIN  ISK DIGIN
TESTRE  CLA INTEMP
**
**
**      DIGITAL INPUTS AND OUTPUTS USED FOR PROGRAM CONTROL
**
**      PROGRAM ENTRY           D116, D175-D178 = 01011   HOMING POINT T
**      TEST ENTRY              D131        BIT 1 OF /G76
**      DMA REQUEST             D229A       BIT 4 OF /G5
**      MUX SELECT (E26) MSB    D229N       BIT 4 OF /G6
**      MUX SELECT (E26)        D228N       BIT 3 OF /G6
**      MUX SELECT (E26)        D227N       BIT 2 OF /G6
**      MUX SELECT (E26) LSB    D226N       BIT 1 OF /G6
**      SYNC INPUT (1 KHZ)      D110        BIT 3 OF /G71
**
$
$
```

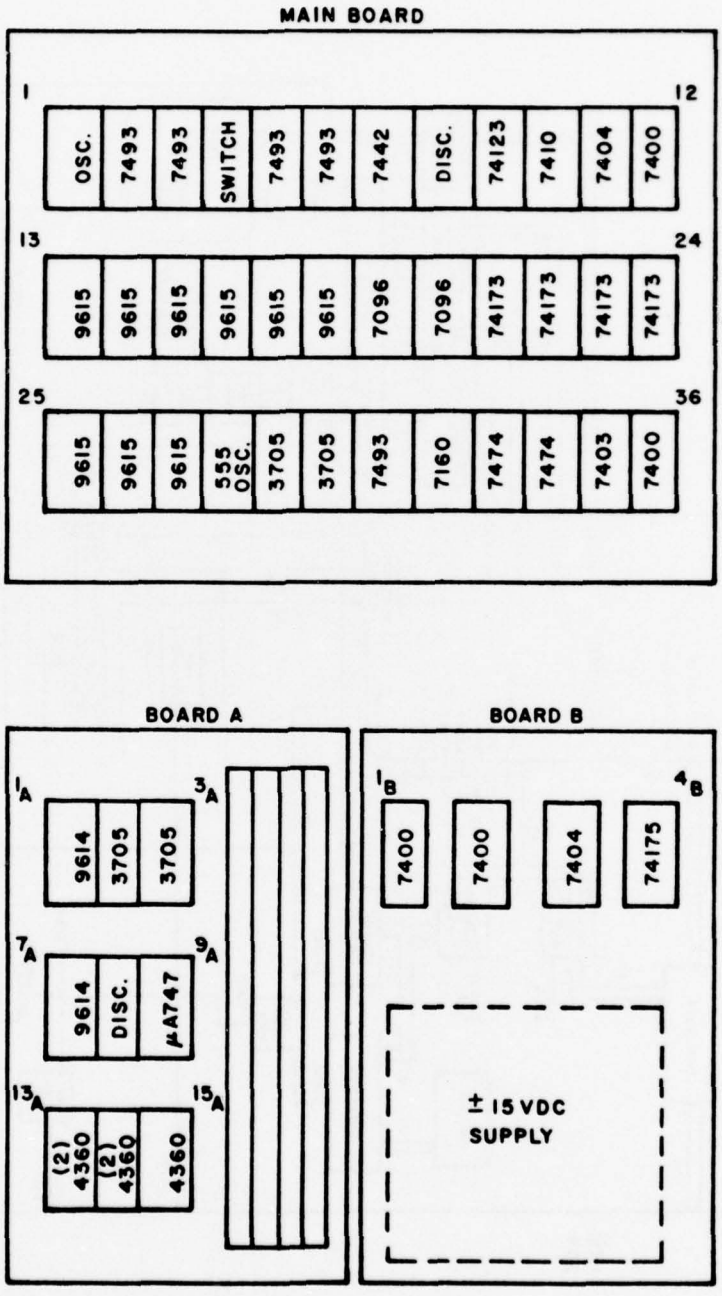
APPENDIX B

HDC-601 DMA I/O SCHEMATICS

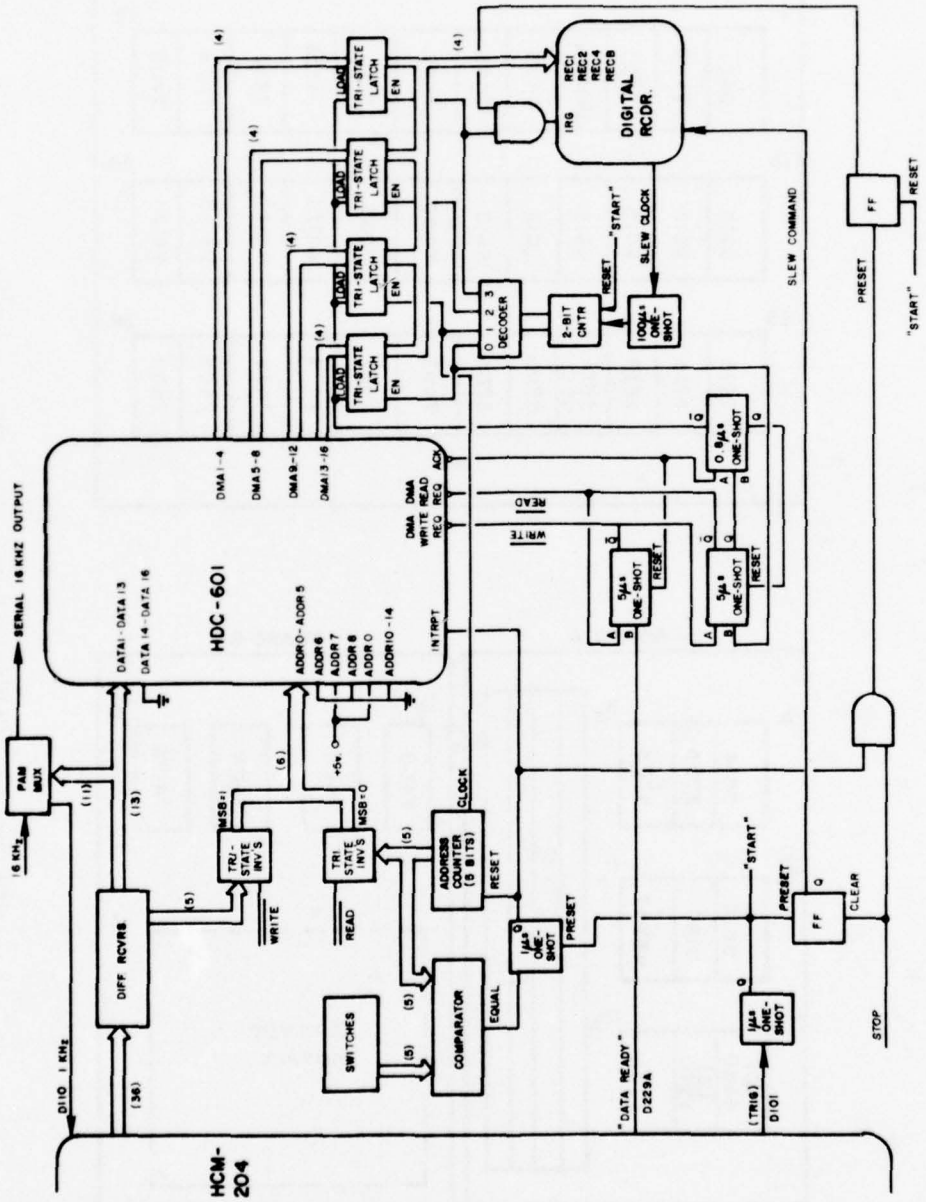
This appendix includes all the schematics delivered with the hardware to engineering personnel at Tyndall AFB. The HCM-204 output interface is not included; the input to this DMA interface is the 18 TTL outputs of the HCM-204 output interface.

This appendix shows the interface as delivered to Tyndall. Changes in operational requirements necessitated certain modifications which were completed and documentated by Tyndall personnel.

The schematics were drawn so that they may be placed adjacent to one another to form a single complete schematic.



HCM-204/HDC-601/Digital Mag. Tape DMA Interface


HDC-601
DIGITAL RCDR.
REC1
REC2
REC4
REC8
IRQ
TRI-STATE LATCH
LOAD
EN
2-BIT CNTR
0 1 2 3 DECODER
RESET
"START"
SLEW CLOCK
100μs ONE-SHOT
SLEW COMMAND
FF
PRESET
CLEAR
RESET
DMA1-4
DMA5-8
DMA9-12
DMA13-16
DMA WRITE REQ
DMA READ REQ
ACK
READ
WRITE
INTRPT
DATA1-DATA13
DATA14-DATA16
ADDR0-ADDR5
ADDR6
ADDR7
ADDR8
ADDR9
ADDR10-14
+5v
0
0.8μs ONE-SHOT
5μs ONE-SHOT
SERIAL 16 KHZ OUTPUT
PAM MUX
16 KHz
DIFF RCVRS
DI10 1 KHz
(36)
(11)
(13)
(6)
(5)
MSB+1
MSB-0
TRI-STATE INV'S
WRITE
READ
ADDRESS COUNTER (5 BITS)
CLOCK
RESET
PRESET
1μs ONE-SHOT
SWITCHES
COMPARATOR
EQUAL
"DATA READY"
D229A
(TRIG)
D101
STOP
HCM-204

J29

BIT1 THRU BIT18 (BIT1 THRU BIT18)	Data from HCM-204
D229A	Discrete indicates "new data ready"
D22GN THRU D229N	4 bit code to select E2G input mux. channel
D101	Discrete indicates "Trigger 2"

J30

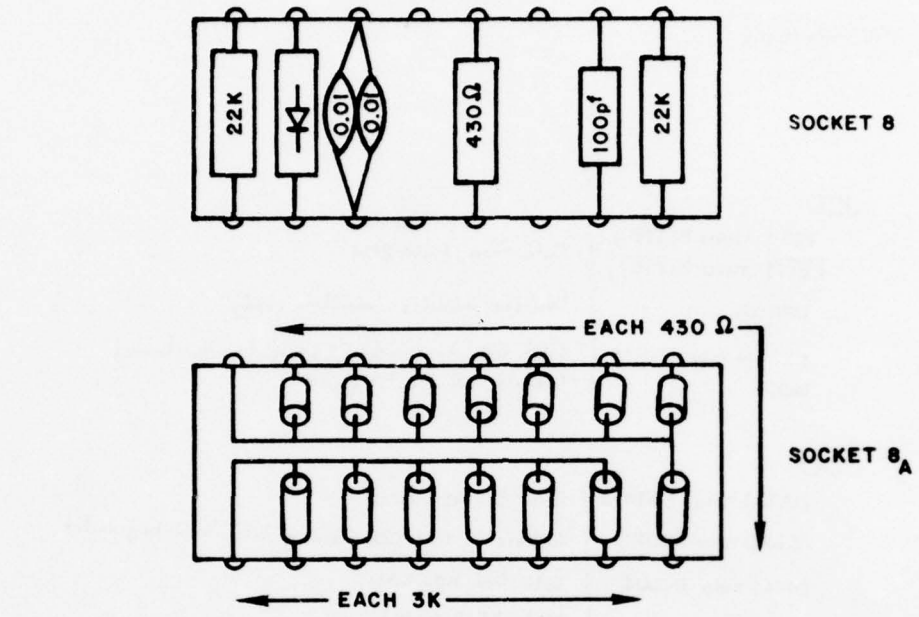
DATA1 THRU DATA13	Data to HDC-601
ADDR0 THRU ADDR9	Address to HDC-601 - remaining bits should be grounded
DMA1 THRU DMA16	Data from HDC-601
READ	DMA READ request
WRITE	DMA WRITE request
INTRPT	INTERRUPT - indicates "frame complete - refresh info. words"
ACK	DMA Acknowledge

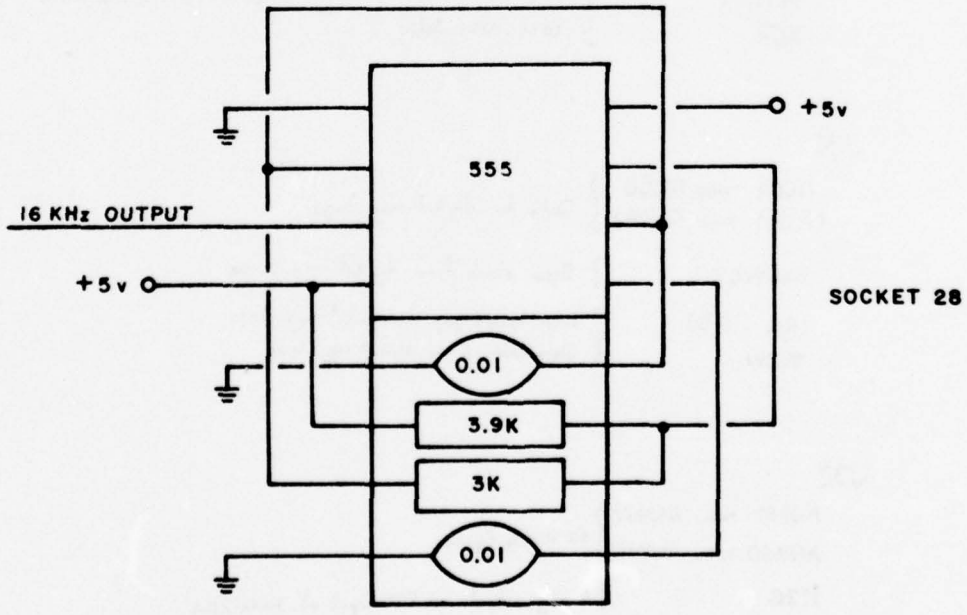
J31

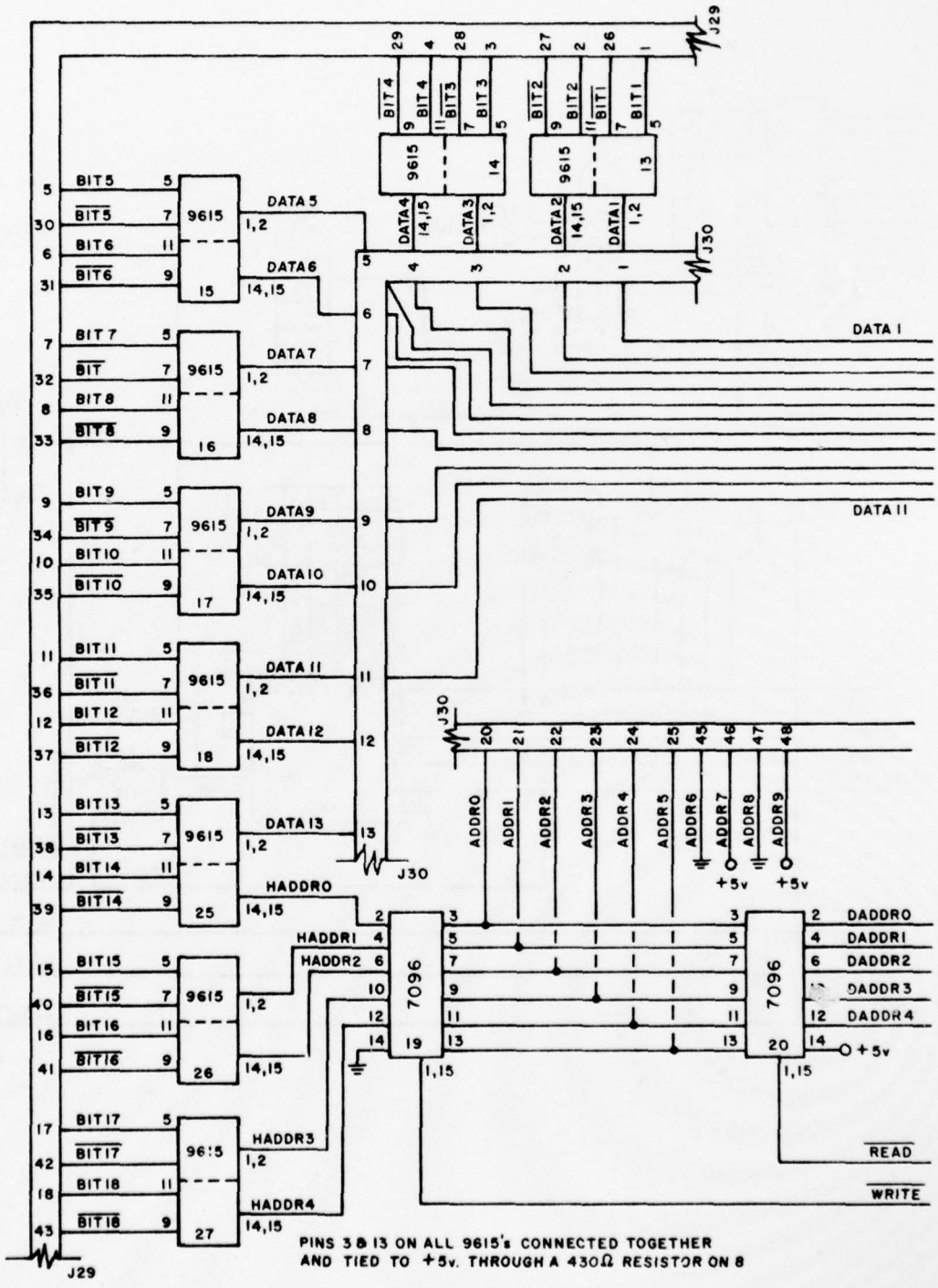
REC1 THRU REC8 (REC1 THRU REC8)	Data to digital mag. tape
SLEWCK	Slew clock from digital mag. tape
IRG (IRG)	Inter-record-gap to digital mag. tape
SLEW	Slew command to digital mag. tape

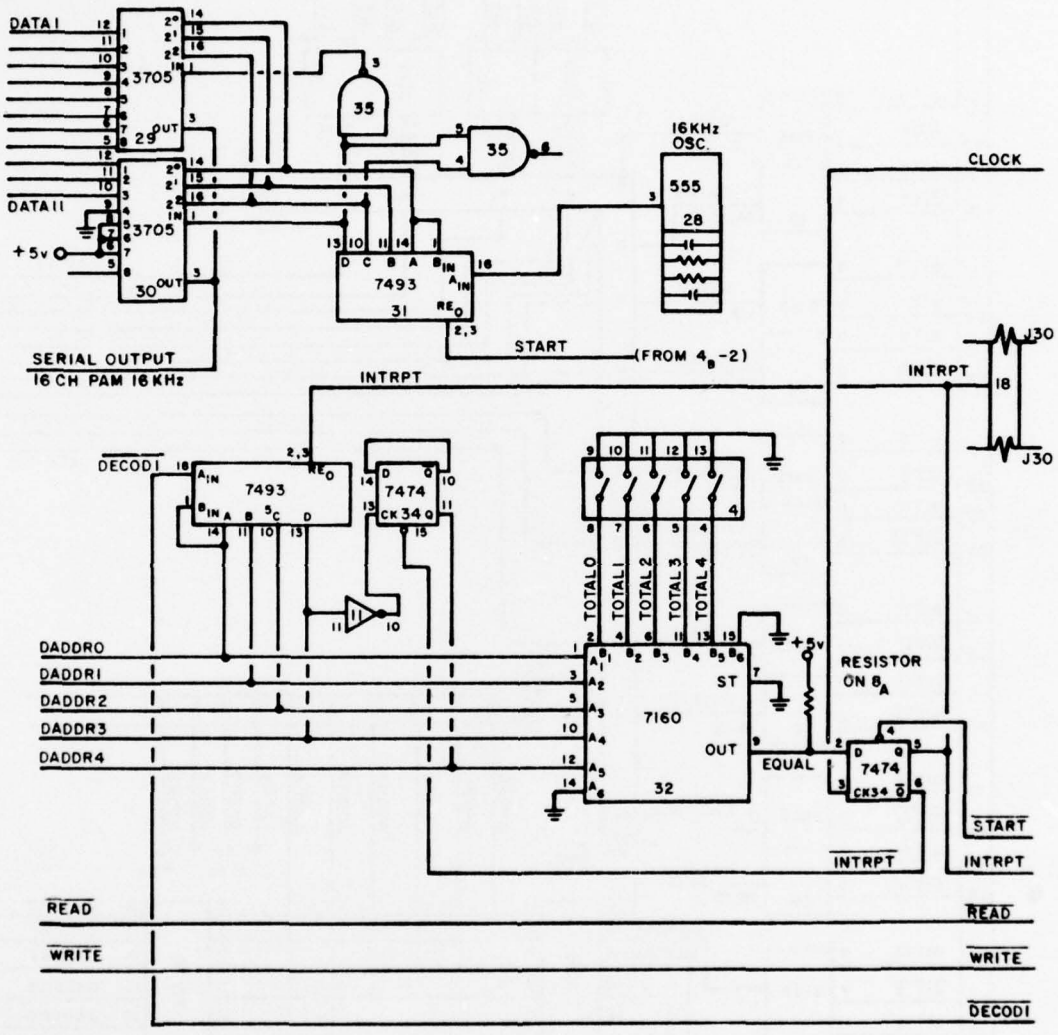
J32

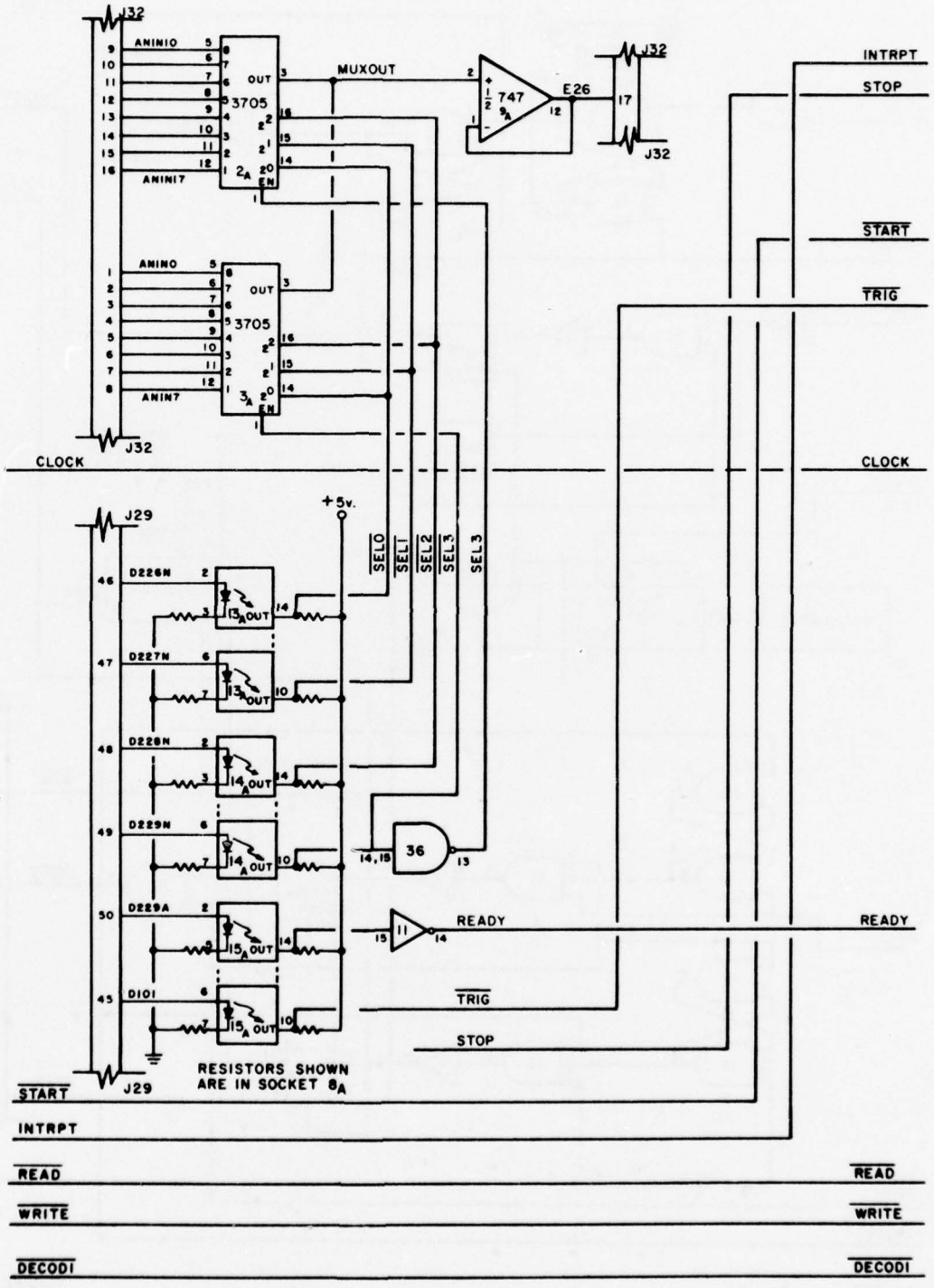
AN1N0 THRU AN1N7 AN1N10 THRU AN1N17	16 Analog inputs
E2G	Analog output to E2G input of HCM-204
D110	1 KHz synchronizing input to HCM-204

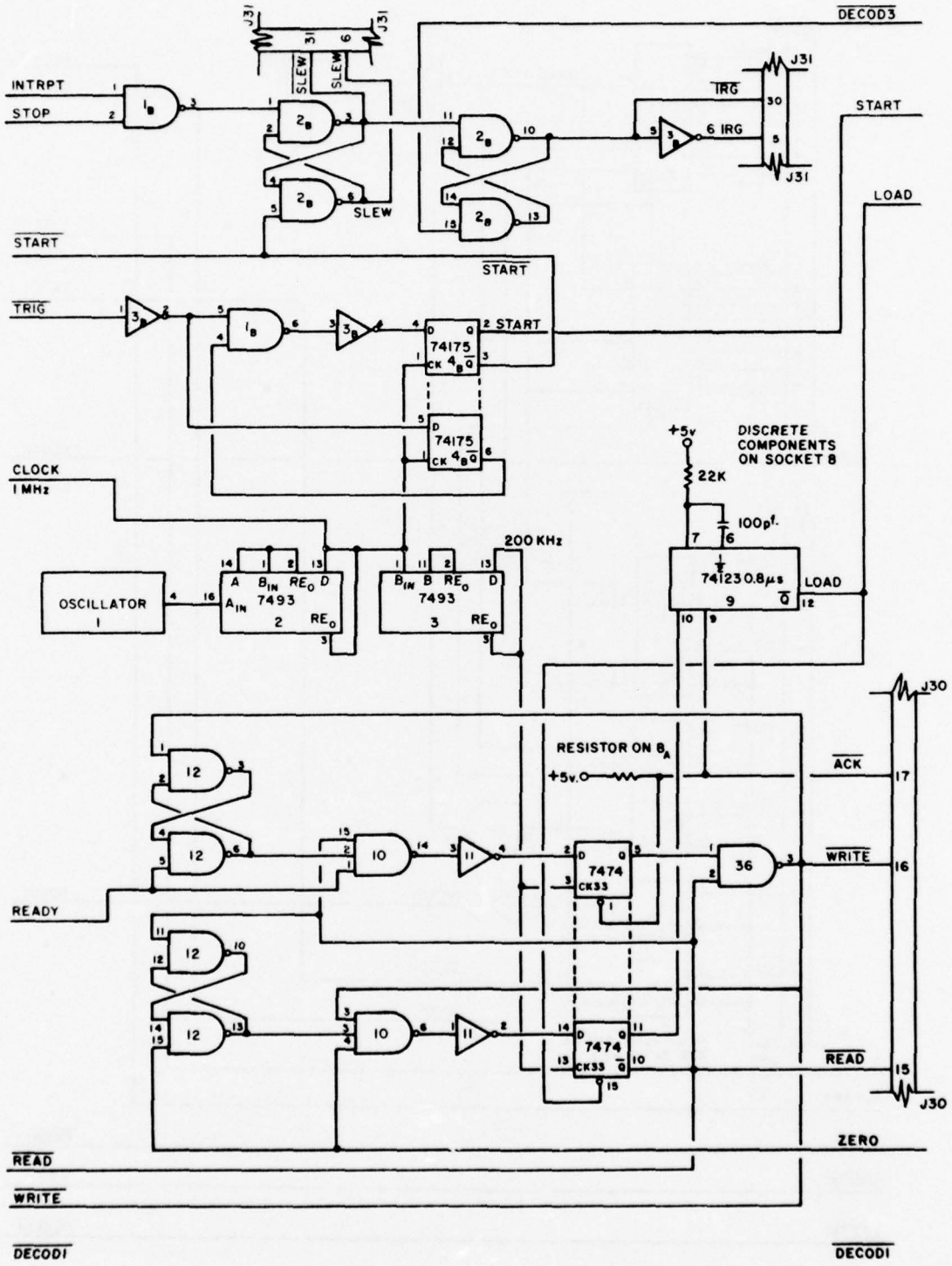

22K
0.01
0.01
430Ω
100pf
22K
SOCKET 8
EACH 430 Ω
SOCKET 8A
EACH 3K

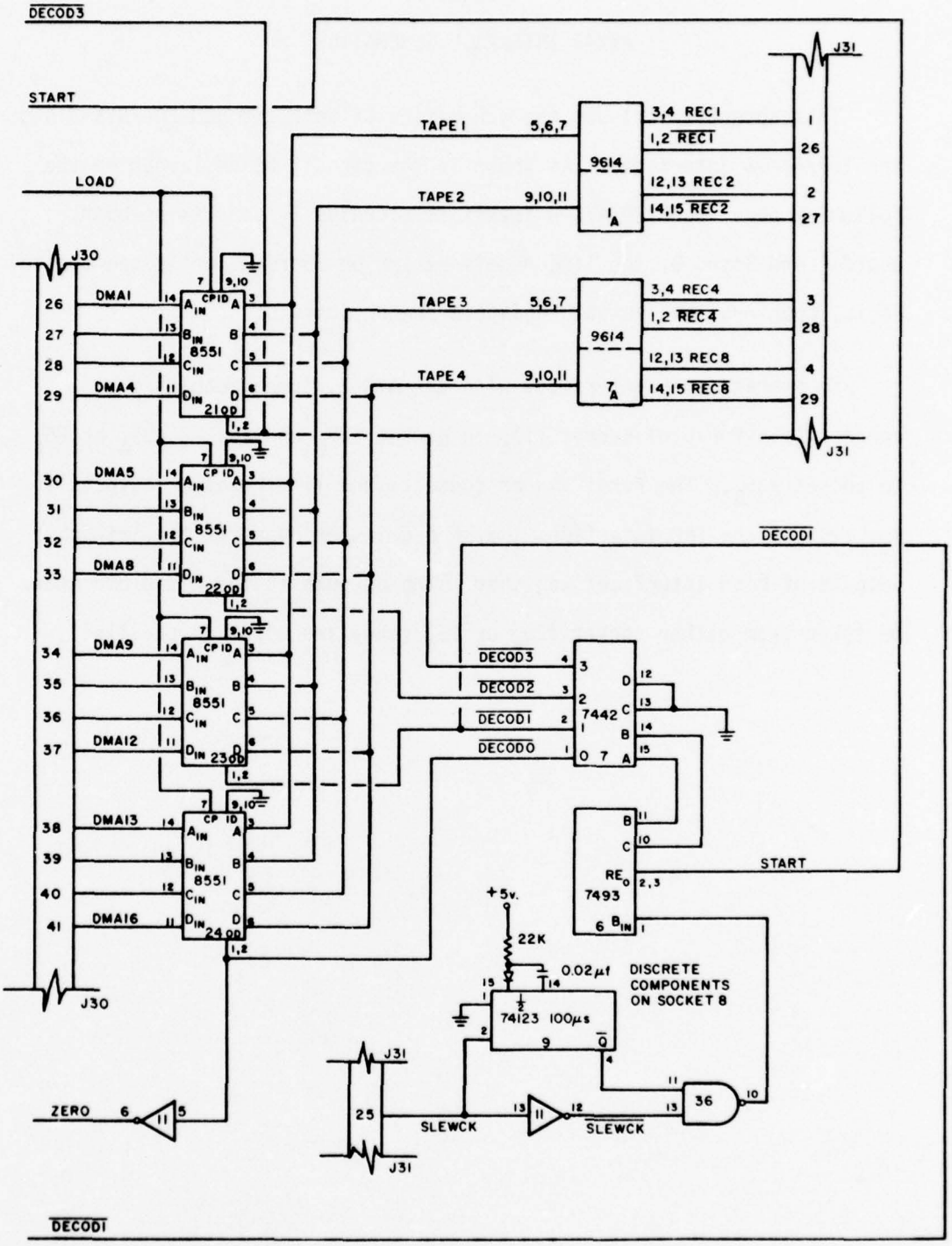

+5v
555
16 KHz OUTPUT
+5v
SOCKET 28
0.01
3.9K
3K
0.01


J29
J30
9615
7096
BIT 4
BIT 3
BIT 2
BIT 1
DATA 4
DATA 3
DATA 2
DATA 1
DATA I
DATA II
ADDR0
ADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
ADDR7
ADDR8
ADDR9
+5v
HADDR0
HADDR1
HADDR2
HADDR3
HADDR4
DADDR0
DADDR1
DADDR2
DADDR3
DADDR4
READ
WRITE
PINS 3 & 13 ON ALL 9615's CONNECTED TOGETHER
AND TIED TO +5v. THROUGH A 430Ω RESISTOR ON 8


DATA I
DATA II
+5v
3705
29
30
35
35
16KHz
OSC.
555
28
7493
31
CLOCK
START
(FROM 4B-2)
SERIAL OUTPUT
16 CH PAM 16 KHz
INTRPT
INTRPT
J30
18
J30
DECOD I
7493
7474
7474
TOTAL 0
TOTAL 1
TOTAL 2
TOTAL 3
TOTAL 4
DADDR0
DADDR1
DADDR2
DADDR3
DADDR4
7160
ST
OUT
32
EQUAL
+5v
RESISTOR
ON 8A
START
INTRPT
INTRPT
READ
WRITE
READ
WRITE
DECOD I


J32
ANINIO
ANINI7
ANINO
ANIN7
3705
MUXOUT
747
E26
INTRPT
STOP
START
TRIG
CLOCK
J29
+5v.
SEL0
SEL1
SEL2
SEL3
SEL3
D226N
D227N
D228N
D229N
D229A
D101
36
READY
RESISTORS SHOWN
ARE IN SOCKET 8A
START
INTRPT
READ
WRITE
DECODI


J31
SLEW
DECOD3
INTRPT
STOP
IRG
6 IRG
START
LOAD
SLEW
START
TRIG
74175
CLOCK
1 MHz
200 KHz
+5v
DISCRETE
COMPONENTS
ON SOCKET 8
22K
100pf.
OSCILLATOR
7493
74123 0.8μs
RESISTOR ON B_A
ACK
WRITE
READY
7474
36
J30
READ
ZERO
DECOD1

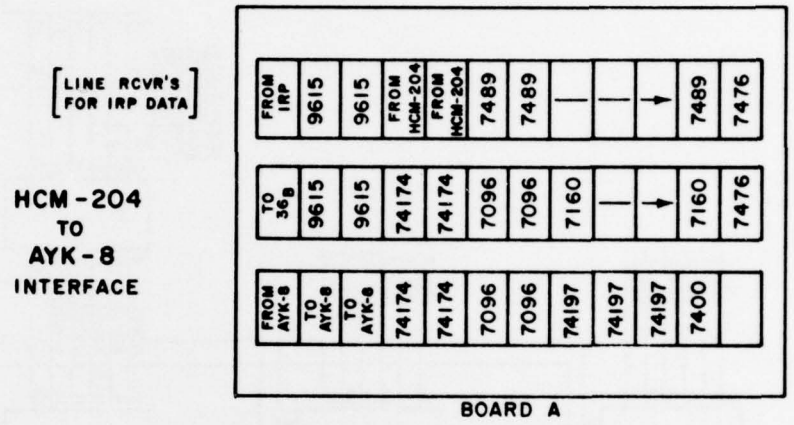

DECOD3
START
LOAD
J30
J31
TAPE 1
TAPE 2
TAPE 3
TAPE 4
5,6,7
9,10,11
9614
3,4 REC 1
1,2 REC 1
12,13 REC 2
14,15 REC 2
3,4 REC 4
1,2 REC 4
12,13 REC 8
14,15 REC 8
DMA1
DMA4
DMA5
DMA8
DMA9
DMA12
DMA13
DMA16
8551
2100
2200
2300
2400
DECOD1
DECOD2
DECOD0
7442
7493
+5v.
22K
0.02 μf
74123 100μs
DISCRETE COMPONENTS ON SOCKET 8
ZERO
SLEWCK
36
DECOD1

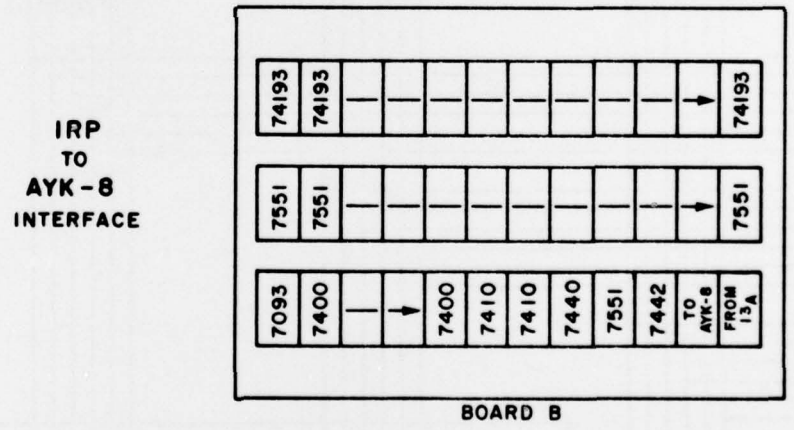
APPENDIX C

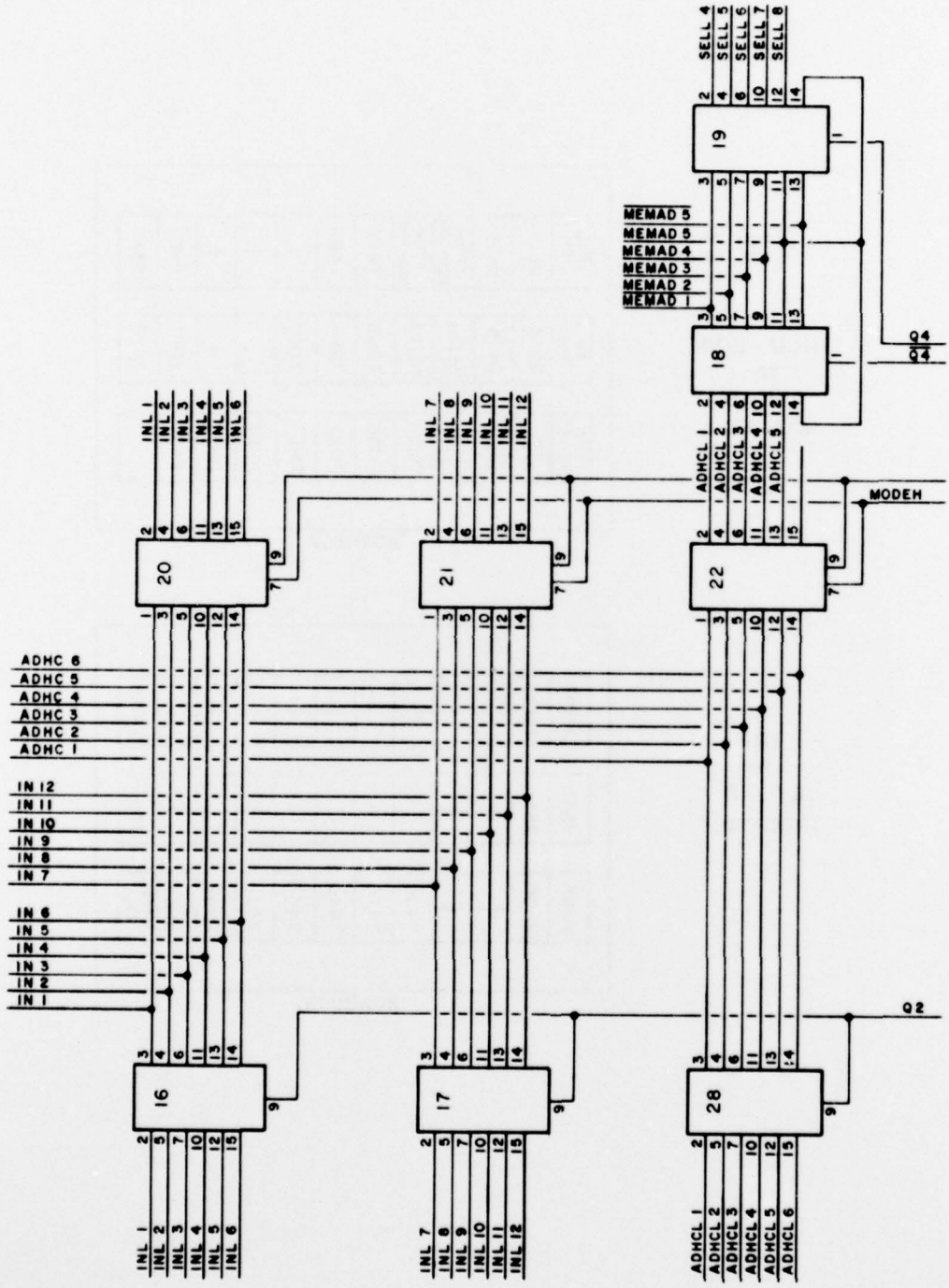
AYK-8 INTERFACE SCHEMATICS

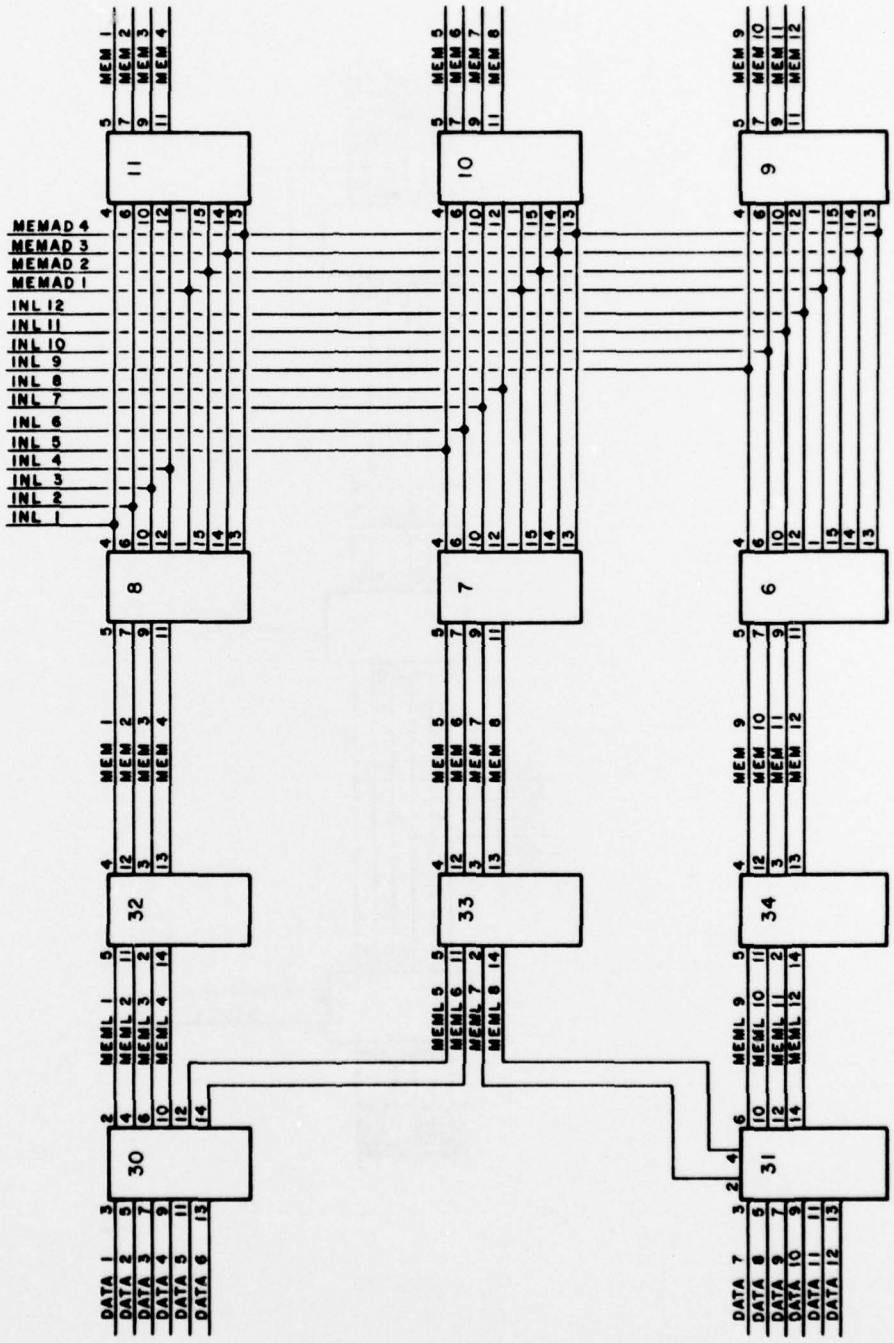
This appendix includes the schematics of both the HCM-204/AYK-8 and the IRP/AYK-8 interfaces. As shown in the circuit board layout on the following page, the IRP/AYK-8 interface occupies IC sockets on both Board A and Board B; the line receivers are on Board A, while the control logic, counters, and output registers are on Board B.

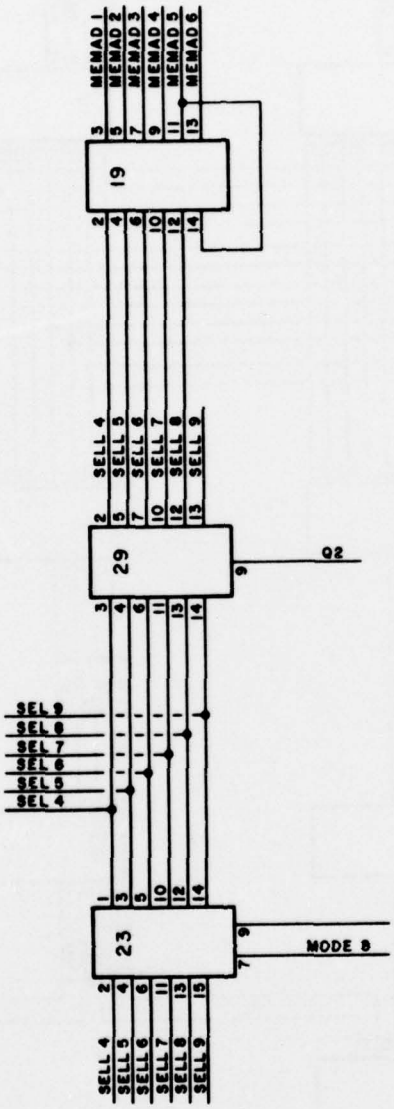
To operate both interfaces with the AYK-8, jumper cables must connect (pin-for-pin) socket $\#13_A$ to socket $\#36_B$ and socket $\#25_A$ or 26_A to socket $\#35_B$. The first jumper connects the line receiver outputs to the rest of the IRP interface; the second jumper connects the tri-state outputs of both interfaces together. The outputs to the AYK-8 can then be taken from either socket $\#25_A$ or 26_A (they are wired in parallel).

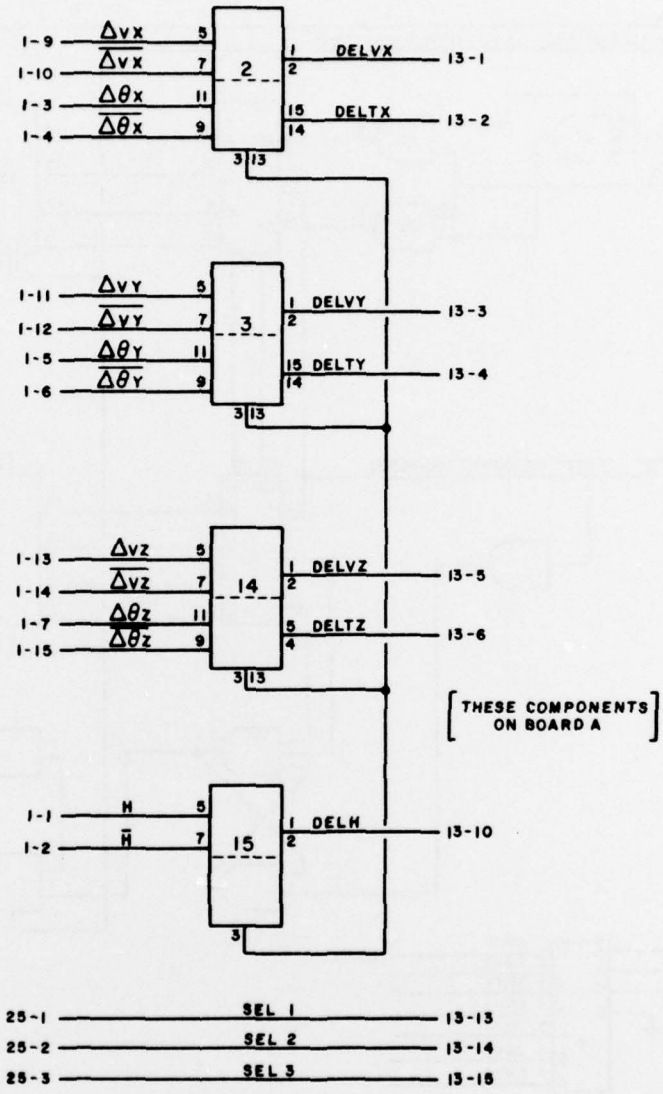

LINE RCVR'S FOR IRP DATA
HCM-204 TO AYK-8 INTERFACE
FROM IRP 9615 9615 FROM HCM-204 FROM HCM-204 7489 7489 — — → 7489 7476
TO 36B 9615 9615 74174 74174 7096 7096 7160 — → 7160 7476
FROM AYK-8 TO AYK-8 TO AYK-8 74174 74174 7096 7096 74197 74197 74197 7400
BOARD A

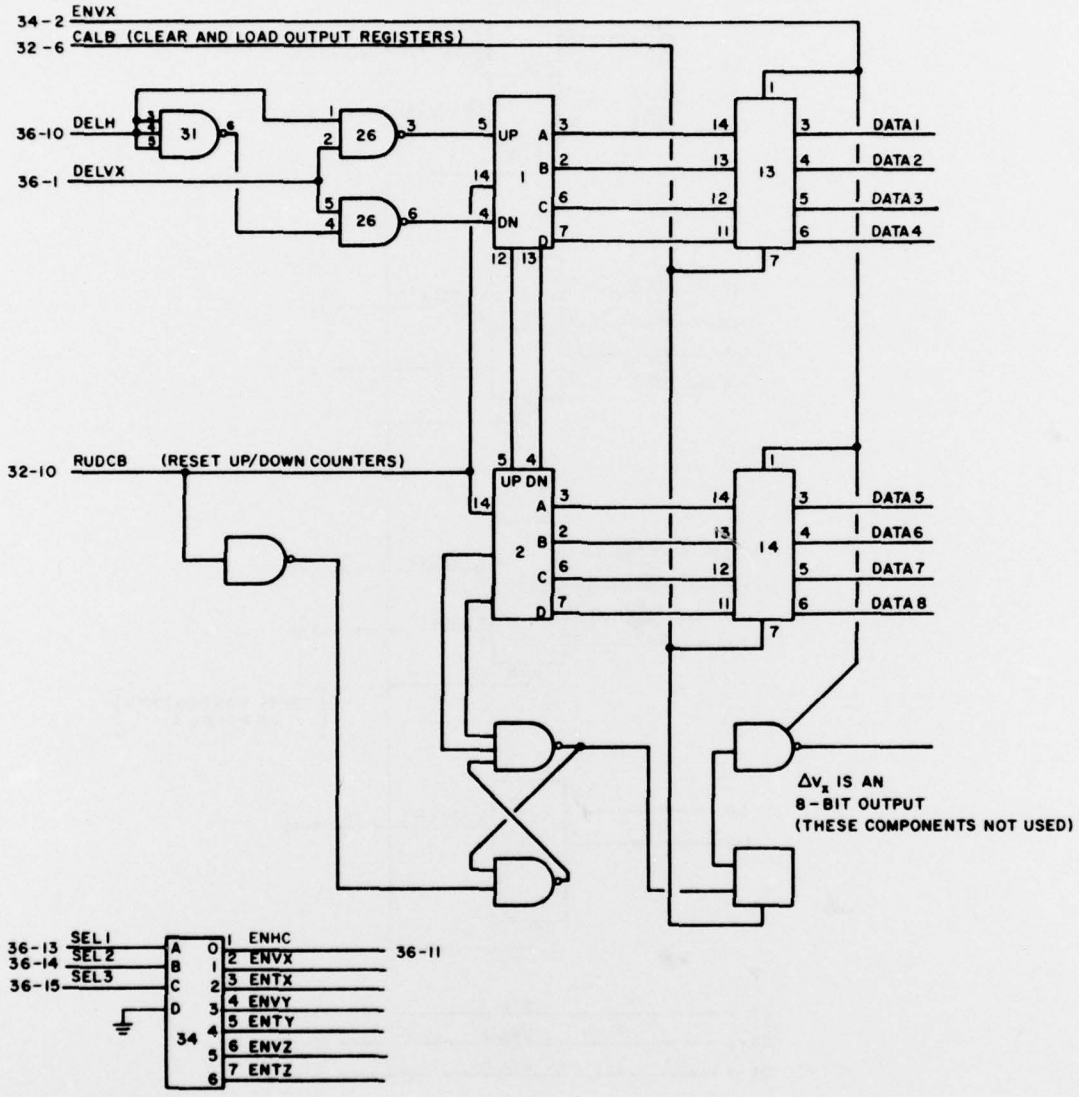

IRP TO AYK-8 INTERFACE
74193 74193 — — — — — — — — → 74193
7551 7551 — — — — — — — — → 7551
7093 7400 — → 7400 7410 7410 7440 7551 7442 TO AYK-8 FROM 13A
BOARD B

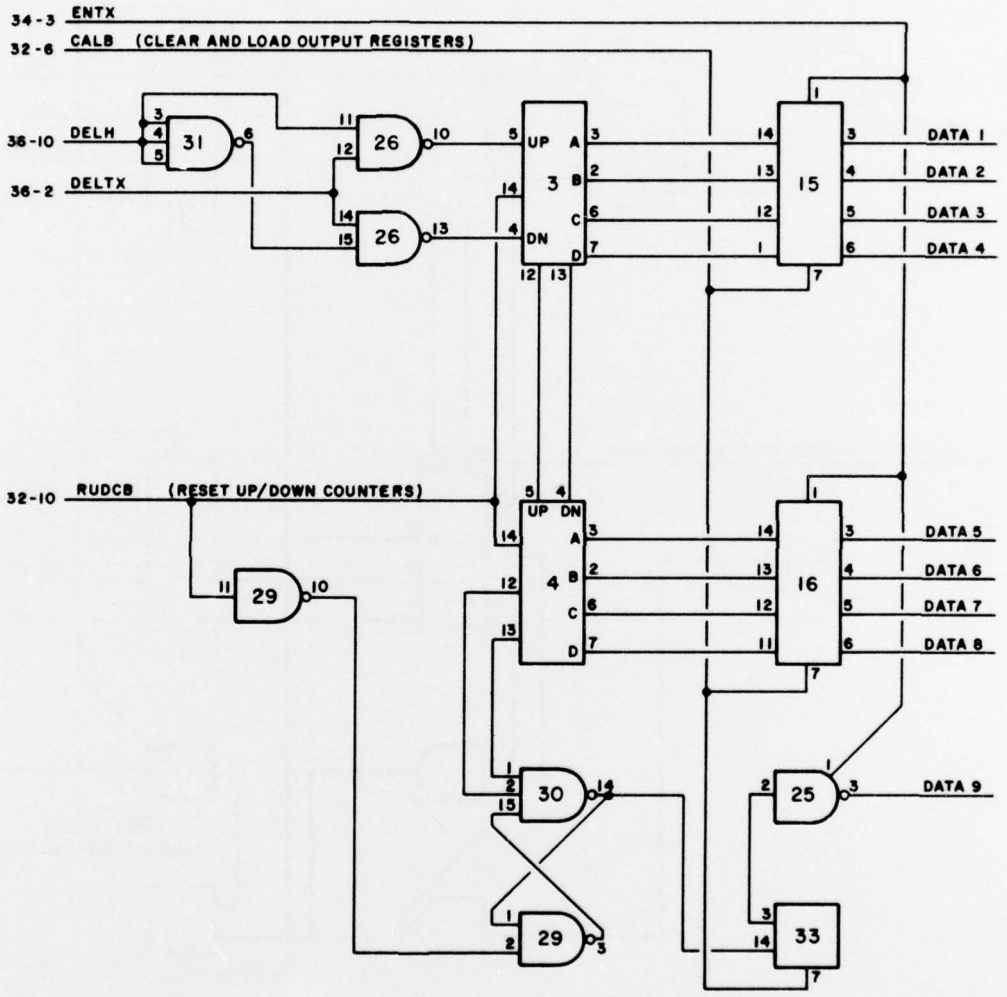

SELL 4
SELL 5
SELL 6
SELL 7
SELL 8
19
MEMAD 5
MEMAD 5
MEMAD 4
MEMAD 3
MEMAD 2
MEMAD 1
18
Q4
Q4
INL 1
INL 2
INL 3
INL 4
INL 5
INL 6
INL 7
INL 8
INL 9
INL 10
INL 11
INL 12
ADHCL 1
ADHCL 2
ADHCL 3
ADHCL 4
ADHCL 5
MODEM
20
21
22
ADHC 6
ADHC 5
ADHC 4
ADHC 3
ADHC 2
ADHC 1
IN 12
IN 11
IN 10
IN 9
IN 8
IN 7
IN 6
IN 5
IN 4
IN 3
IN 2
IN 1
Q2
16
17
28
ADHCL 6

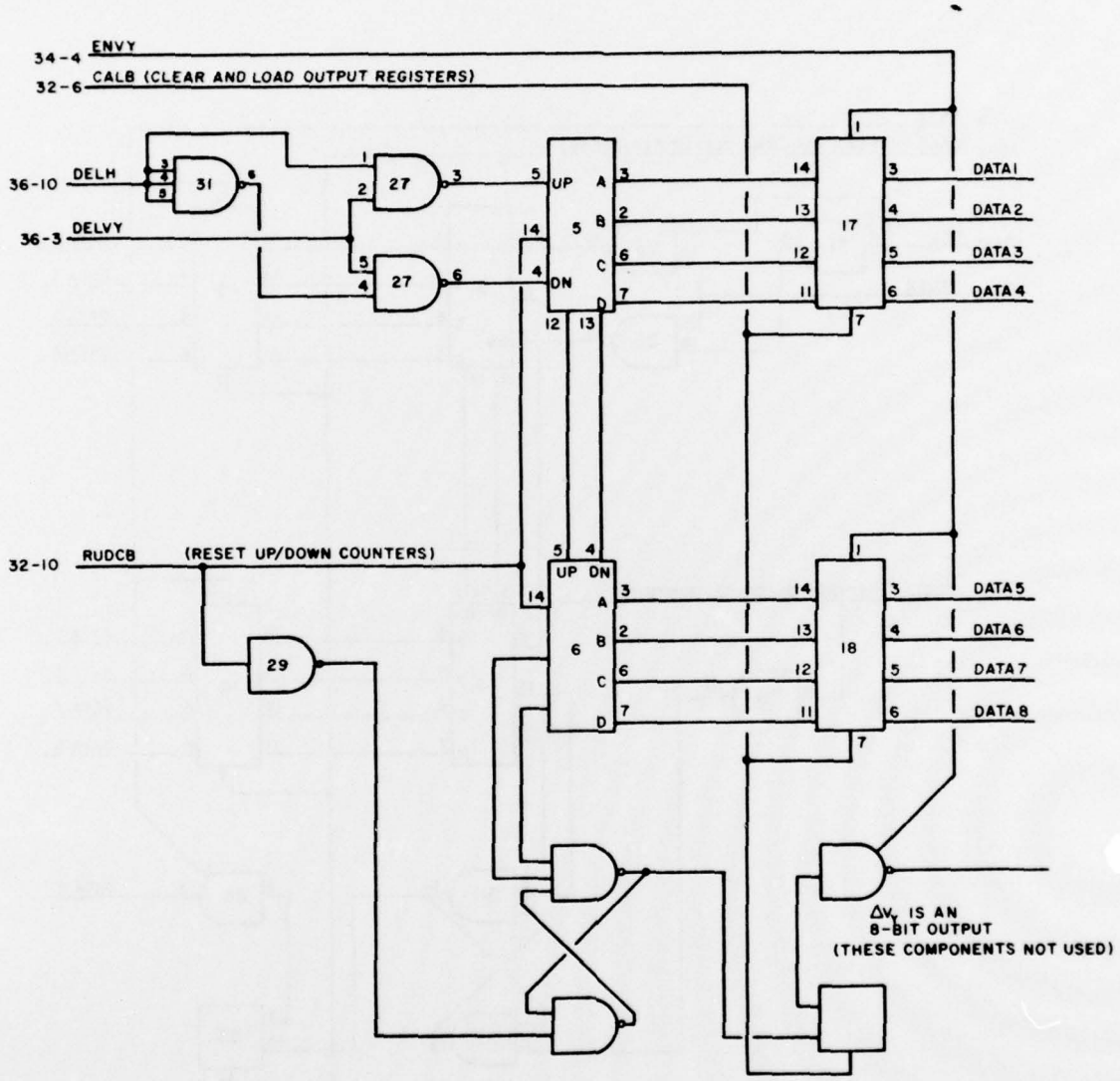

MEMAD 4
MEMAD 3
MEMAD 2
MEMAD 1
INL 12
INL 11
INL 10
INL 9
INL 8
INL 7
INL 6
INL 5
INL 4
INL 3
INL 2
INL 1
11
10
9
8
7
6
32
33
34
30
31
MEM 1
MEM 2
MEM 3
MEM 4
MEM 5
MEM 6
MEM 7
MEM 8
MEM 9
MEM 10
MEM 11
MEM 12
MEML 1
MEML 2
MEML 3
MEML 4
MEML 5
MEML 6
MEML 7
MEML 8
MEML 9
MEML 10
MEML 11
MEML 12
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12

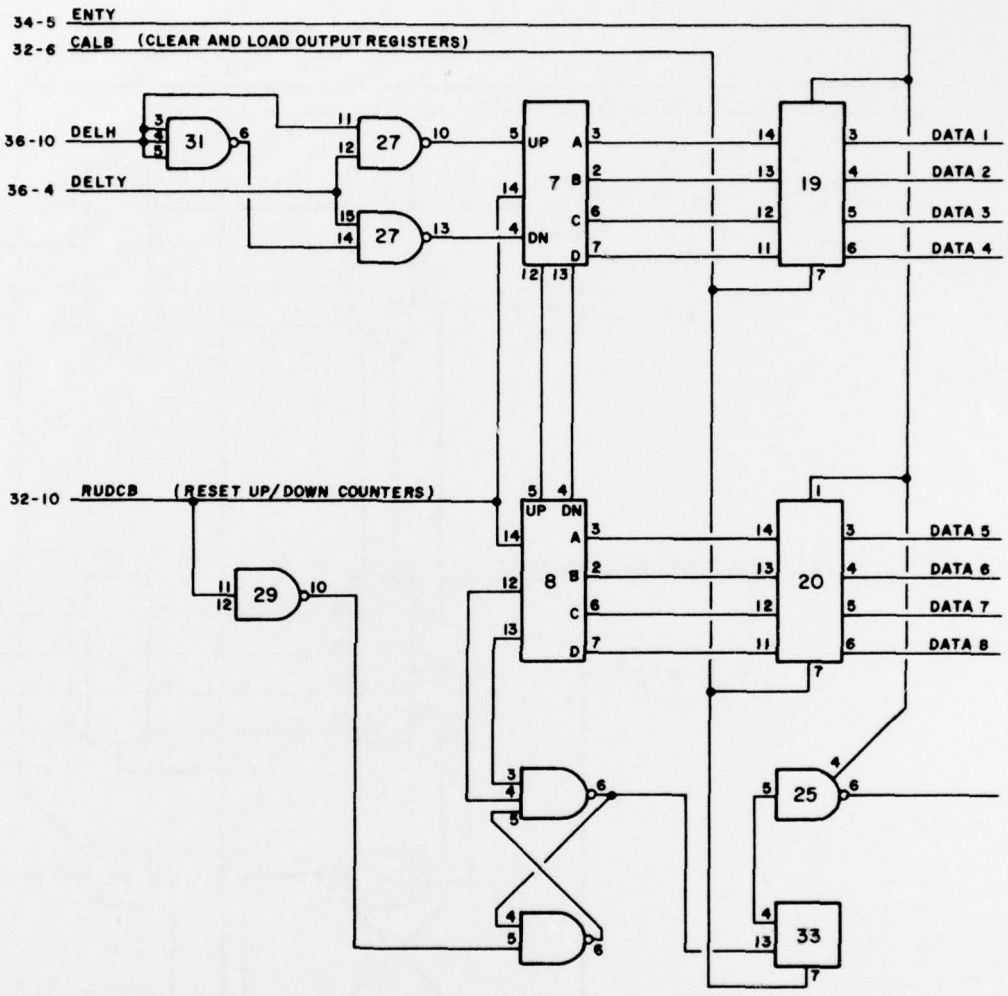

MEMAD 1
MEMAD 2
MEMAD 3
MEMAD 4
MEMAD 5
MEMAD 6
19
SELL 4
SELL 5
SELL 6
SELL 7
SELL 8
SELL 9
29
Q2
SEL 9
SEL 8
SEL 7
SEL 6
SEL 5
SEL 4
23
MODE 8
SELL 4
SELL 5
SELL 6
SELL 7
SELL 8
SELL 9

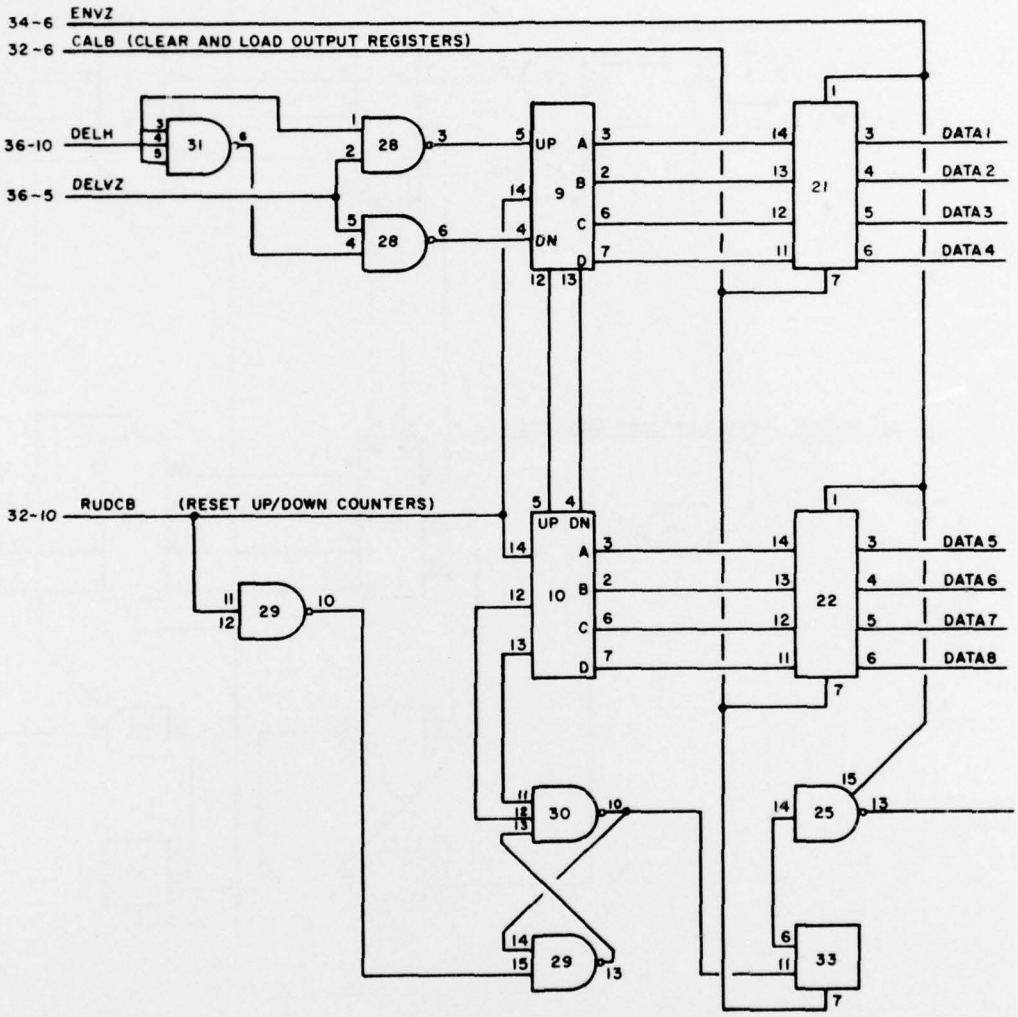

1-9
ΔVX
1-10
ΔVX
1-3
Δθx
1-4
Δθx
2
DELVX
13-1
DELTX
13-2
1-11
ΔVY
1-12
ΔVY
1-5
Δθy
1-6
Δθy
3
DELVY
13-3
DELTY
13-4
1-13
ΔVz
1-14
ΔVz
1-7
Δθz
1-15
Δθz
14
DELVZ
13-5
DELTZ
13-6
THESE COMPONENTS ON BOARD A
1-1
H
1-2
H
15
DELH
13-10
25-1
SEL 1
13-13
25-2
SEL 2
13-14
25-3
SEL 3
13-15

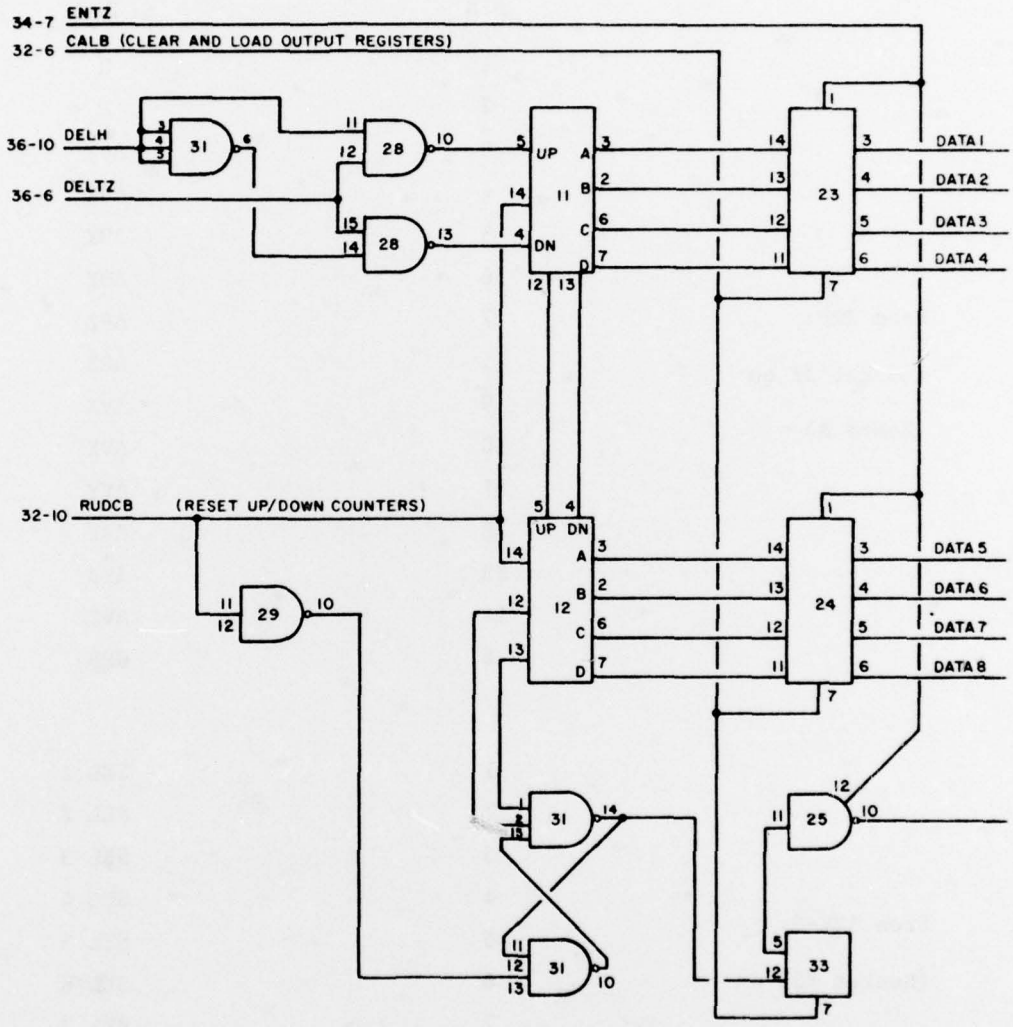

34-2 ENVX
32-6 CALB (CLEAR AND LOAD OUTPUT REGISTERS)
36-10 DELH
36-1 DELVX
31
26
26
UP
DN
1
13
DATA 1
DATA 2
DATA 3
DATA 4
32-10 RUDCB (RESET UP/DOWN COUNTERS)
UP DN
2
14
DATA 5
DATA 6
DATA 7
DATA 8
ΔVx IS AN
8-BIT OUTPUT
(THESE COMPONENTS NOT USED)
36-13 SEL 1
36-14 SEL 2
36-15 SEL 3
34
1 ENHC
2 ENVX
3 ENTX
4 ENVY
5 ENTY
6 ENVZ
7 ENTZ
36-11


34-3 ENTX
32-6 CALB (CLEAR AND LOAD OUTPUT REGISTERS)
36-10 DELH
36-2 DELTX
31
26
26
UP
DN
3
15
DATA 1
DATA 2
DATA 3
DATA 4
32-10 RUDCB (RESET UP/DOWN COUNTERS)
29
UP DN
4
16
DATA 5
DATA 6
DATA 7
DATA 8
30
29
25
DATA 9
33


34-4 ENVY
32-6 CALB (CLEAR AND LOAD OUTPUT REGISTERS)
36-10 DELH
36-3 DELVY
31
27
27
UP
DN
5
A
B
C
D
17
DATA1
DATA2
DATA3
DATA4
32-10 RUDCB (RESET UP/DOWN COUNTERS)
29
UP DN
6
18
DATA5
DATA6
DATA7
DATA8
ΔVt IS AN
8-BIT OUTPUT
(THESE COMPONENTS NOT USED)


34-5 ENTY
32-6 CALB (CLEAR AND LOAD OUTPUT REGISTERS)
36-10 DELH
36-4 DELTY
31
27
27
7
UP
DN
A
B
C
D
19
DATA 1
DATA 2
DATA 3
DATA 4
32-10 RUDCB (RESET UP/DOWN COUNTERS)
29
8
UP DN
20
DATA 5
DATA 6
DATA 7
DATA 8
25
33


34-6 ENVZ
32-6 CALB (CLEAR AND LOAD OUTPUT REGISTERS)
36-10 DELH
36-5 DELVZ
31
28
28
9
UP
DN
A
B
C
D
21
DATA 1
DATA 2
DATA 3
DATA 4
32-10 RUDCB (RESET UP/DOWN COUNTERS)
29
10
UP DN
22
DATA 5
DATA 6
DATA 7
DATA 8
30
25
29
33


34-7 ENTZ
32-6 CALB (CLEAR AND LOAD OUTPUT REGISTERS)
36-10 DELH
36-6 DELTZ
31
28
28
UP
DN
23
DATA 1
DATA 2
DATA 3
DATA 4
32-10 RUDCB (RESET UP/DOWN COUNTERS)
29
UP DN
12
24
DATA 5
DATA 6
DATA 7
DATA 8
31
31
25
33

AYK-8 INTERFACE INPUT/OUTPUT CONNECTORS

	PIN	SIGNAL
From IRP: (Socket #1 on Board A)	1	H
	2	H
	3	ΔθX
	4	ΔθX
	5	ΔθY
	6	ΔθY
	7	ΔθZ
	15	ΔθZ
	9	ΔVX
	10	ΔVX
	11	ΔVY
	12	ΔVY
	13	ΔVZ
	14	ΔVZ
	8	GND
From AYK-8: (Socket #25 on Board A)	1	SEL 1
	2	SEL 2
	3	SEL 3
	4	SEL 4
	5	SEL 5
	6	SEL 6
	7	SEL 7
	9	SEL 8
	10	SEL 9
	14	MODE 8

From HCM-204: (Socket #4 on Board A)	1	IN1
	2	IN 2
	3	IN 3
	4	IN 4
	5	IN 5
	6	IN 6
	7	IN 7
	9	IN 8
	10	IN 9
	11	IN 10
	12	IN 11
	13	IN 12
From HCM-204: (Socket #5 on Board A)	1	ADHC 1
	2	ADHC 2
	3	ADHC 3
	4	ADHC 4
	5	ADHC 5
	6	ADHC 6
	9	REQ H
	10	MODE H
Board A to Board B: (Socket #13 on Board A Socket #36 on Board B)	1	DELVX
	2	DELTX
	3	DELVY
	4	DELTY
	5	DELVZ
	6	DELTZ
	7	RUDC
	9	CAL
	10	DELH
	11	ENHC
	12	
	13	SEL 1
	14	SEL 2
	15	SEL 3

	1	DATA 1
	2	DATA 2
To AYK-8:	3	DATA 3
(Socket #26, 27 on Board A	4	DATA 4
	5	DATA 5
Socket #35 on Board B)	6	DATA 6
	7	DATA 7
	9	DATA 8
	10	DATA 9
	11	DATA 10
	12	DATA 11
	13	DATA 12

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