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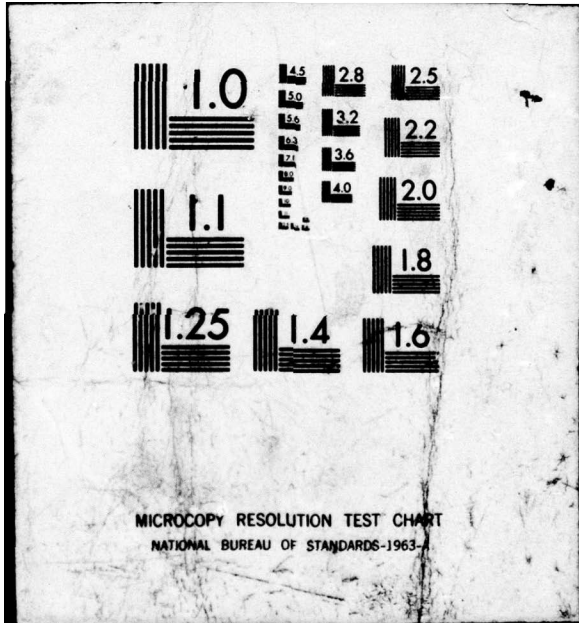
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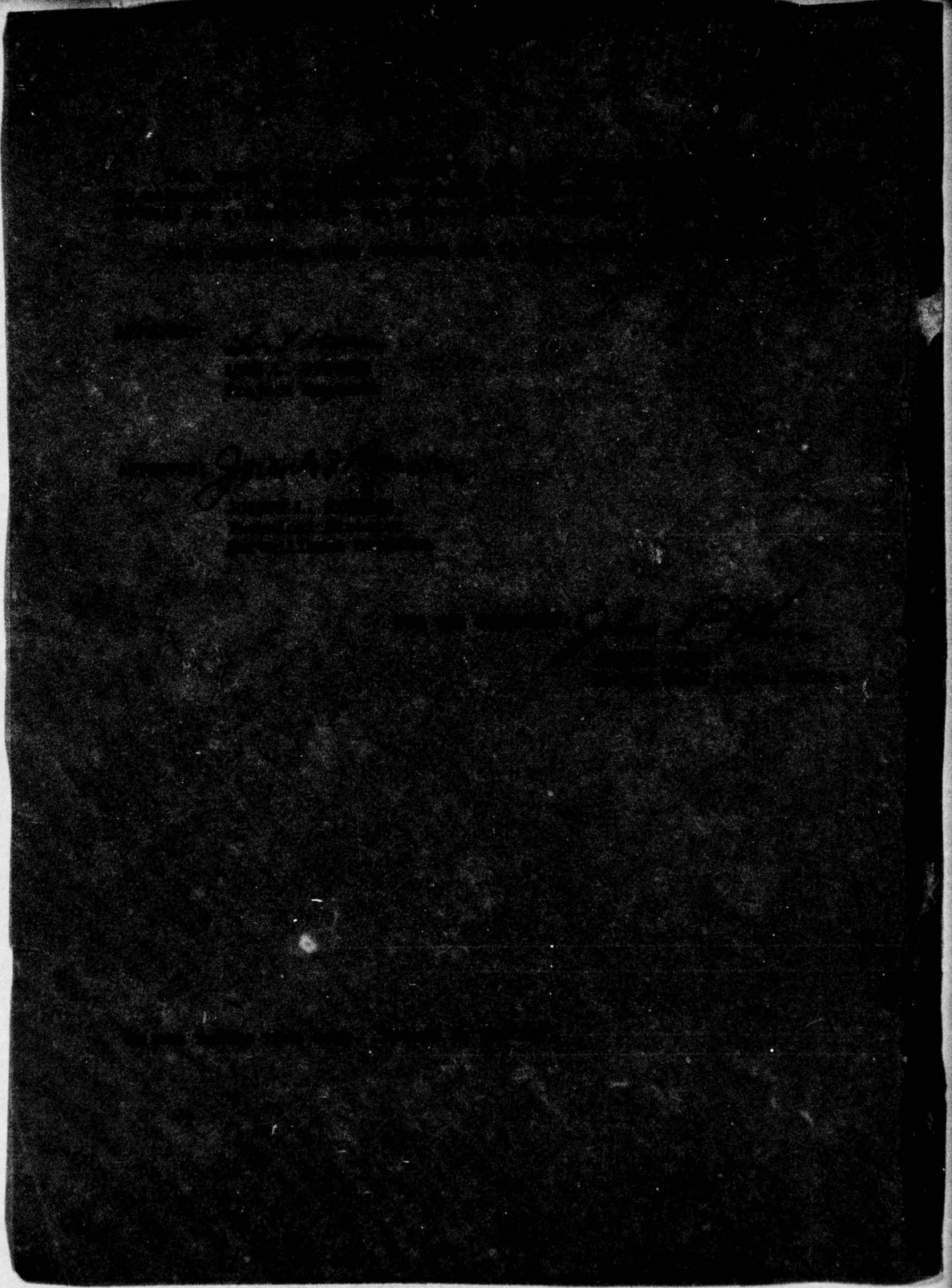
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This is the Final Technical Report on subject contract whose objectives are to investigate theoretically and experimentally new solid-state phenomena and techniques having application to microwave generation, amplification and control.			
Tasks under this program are: Properties of IMPATT Diodes, Transverse Effects in IMPATT Devices, Pulsed IMPATT Diodes, Field-Effect Transistors, Experimental			

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Field-Effect Transistor Investigations, IMPATT Diode Amplifiers, Controlled
Avalanche Transit Time (CATT) Devices.

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ABSTRACT

The previously published results of the two-dimensional finite-element simulation of the microwave GaAs MESFET are summarized. The potential accuracy of the Hermite cubic finite-element approximation in two-dimensional modeling of the MESFET can only be achieved by improving the accuracy with which singular points are modeled. It is shown how local mesh refinement can be carried out which preserves the exact conservation of current property of the finite-element method. Sparse tableau formulation of the equations is discussed.

A submicron-gate vertical junction field-effect transistor design has been proposed which can be fabricated using conventional photolithographic techniques. The fabrication procedure utilizes an anisotropic etch into epitaxial pn^+ Si to define the source followed by a phosphorus diffusion to open a conducting channel. Devices have been fabricated and results are presented. A numerical simulation of the proposed JFETs dc operation has been carried out. Results of this analysis are presented.

One principal objective of the FET program was to design an X-band GaAs Schottky-barrier FET. An optimization computer program to aid in the design of a special class of microwave circuits including the above case has been developed. Results of the design and analysis are presented and discussed.

The behavior of IMPATT oscillators under pulsed operating conditions has been studied. A simple thermal model for the pulsed IMPATT oscillator has been found. Using the model, a bias current compensation circuit to limit the frequency shift during pulsed operation was built and tested. Results indicated that the total frequency shift during the pulse interval can be reduced by a factor of 10. Experimental results are also discussed for a variety of X-band IMPATT oscillator operating conditions.

During this period, analytical expressions have been developed such that when numerical methods are utilized, they will provide information on the avalanche multiplication factor, avalanche delay, electron- and hole-current densities in the avalanche subregion and the small-signal impedances of a CATT oscillator. An extremely simple study was carried out for the emitter-coupled oscillator. Conditions for optimum extractable power and load requirements for the emitter-coupled CATT oscillator have been obtained.

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R. J. Trew, G. I. Haddad and N. A. Masnari, "Harmonic Tuning Effects of TRAPATT Oscillators," Presented at the 1975 Int. Microwave Symposium, Palo Alto, CA, May 1975.

J. J. Barnes and R. J. Lomax, "Two-Dimensional Simulation of Semiconductor Devices Using Finite Element Methods," Presented at the 79th Summer Meeting of the American Math. Society, Western Michigan University, Kalamazoo, MI, August 1975.

J. R. East and N. A. Masnari, "Frequency Drift Behavior of Pulsed IMPATT Diodes," To be presented at the 1976 Government Microcircuit Applications Conf., Lake Buena Vista, FL, November 1976.

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E. H. Sigman, "Determination of Current vs. Electric Field Characteristics in Multivalley Semiconductors," Tech. Report No. TR-73-401, January 1974. AD#776806/2GI.

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J. J. Barnes, R. J. Lomax and G. I. Haddad, "Finite Element Simulation of GaAs MESFETs With Lateral Doping Profiles and Submicron Gates," Electron Devices (submitted for publication).

J. J. Barnes and R. J. Lomax, "Finite-Element Methods in Semiconductor Device Simulation," Proc. IEEE (submitted for publication).

EVALUATION

This effort conducted both theoretical and experimental investigations of solid-state microwave generation devices. These devices (IMPATT Diodes, Field-Effect Transistors, and Controlled Avalanche Transit Time Devices) were investigated in an attempt to improve power output, frequency stability, and efficiency as required by TPO 5. The models developed under this program will aid in the design of these devices for use in future radar and communications equipments.

Leon L. Stevens

LEON L. STEVENS
Project Engineer

MICROWAVE SOLID-STATE DEVICE AND CIRCUIT STUDIES

1. General Introduction. (N. A. Masnari)

The research under this program is concerned with the investigation of various phenomena and techniques for the generation, amplification, detection and control of electromagnetic energy at microwave frequencies. The work is mainly oriented toward an investigation of the basic properties, capabilities and potential of various devices. Studies during the program have included:

1. Avalanche transit-time devices including IMPATT, TRAPATT and CATT devices.
2. Transferred-electron devices.
3. Microwave field-effect transistors.
4. Microwave circuits.
5. Transient operation of microwave devices.

The research carried out during the past three years has resulted in numerous Ph.D. dissertations, technical journal articles and paper presentations. The publications are listed in the preliminary pages of this final report. The activities which were carried out during the final stages of this contract are reported in detail below. Complete discussions of earlier investigations can be found in the above-listed technical reports.

2. Field-Effect Transistors

R. J. Lomax

2.1 Introduction. The purpose of this study is to investigate the performance limitation of the GaAs MESFET and to determine methods to improve the present performance of these devices. As both a low noise and power microwave amplifier the GaAs MESFET has proven to be better than the state-of-the-art bipolar-junction transistors and insulated-gate field-effect transistors. In order to obtain improvement in microwave performance it seems necessary to resort to submicron gate-length geometries; however, this reduction in geometry leads to device operation in the region where the classical one-dimensional gradual-channel approximation is expected to be invalid. By using a full two-dimensional device simulation the operation of the MESFET has been obtained subject to the limitations of the device processing parameters used in the simulation and the validity of the form of the transport equation model.

2.2 Previously Reported Work. By using the simulation it is possible to examine the electric field, electron concentration and voltage distribution throughout the device and thereby propose changes in the processing steps that could result in improvement in the microwave performance of the MESFET. It was shown that the drain current may be increased by placing a lower doped region between the gate and the drain of the MESFET where the highest field exists, since drift velocity saturation degrades the device performance. Simulations of MESFET structures with different channel doping concentrations, graded doping profiles and

aspect ratios were performed. Furthermore the 0.4- μm gate length GaAs MESFET was shown to exhibit a negative-resistance region in the drain current characteristic.

Use of the simulation to predict the large-signal response of the MESFET to an applied negative gate pulse has shown that the transit-time limitation is applicable for some structures where high field effects are dominant and the effective gate length may be larger than the metallurgical gate length.

Application of the finite-element method to the two-dimensional simulation of the semiconductor device equations is new with these results being some of the first reported. Accordingly, the equation formulation and extension to the Hermite bicubic shape function were described in detail as well as the associated choices for the time evolution scheme to be employed.

This aspect of the work has been described in detail in a previously published Technical Report.¹

Subsequent to the publication of the above mentioned report, further work has been carried out in refining the numerical technique.² In the last Interim Technical Report 9/10 the conservation properties of the finite element method were discussed. It was shown that by using the the appropriate expressions for computation of the current densities, it is possible to obtain exact current conservation

1. Barnes, J. J., "A Two-Dimensional Simulation of MESFETs," Technical Report No. RADC-TR-76-153, Rome Air Development Center, Air Force Systems Command, Griffiss Air Force Base, NY 13441, May 1976. AD#A026413.
2. Barnes, J. J. and Lomax, R. J., "Finite-Element Methods in Semiconductor Device Simulation," submitted for publication.

at the device terminals, thereby permitting unambiguous evaluation of terminal characteristics. In addition, it is generally accepted that numerical methods which reproduce conservation properties of the physical system are less amenable to numerical problems such as instability.

2.3 Bicubic Hermite Model. Previous reports have given a number of results based on a finite-element approximation having linear approximating functions. Because of the known limitations of accuracy of the linear approximation and also because of its lack of interelement current continuity, recent work has been on the development of a higher order approximation (Hermite bicubic). The rest of this report gives preliminary results from this model and then a procedure is discussed to deal with the singularities which are present in this problem at the edges of the contacts. This procedure, mesh refinement, is also usable to improve accuracy in regions of the device where large changes in solution parameters occur over small distances.

Previous reports have described the basic bicubic-Hermite finite-element technique. Results have been obtained this quarter for a GaAs MESFET with epitaxial doping $5 \times 10^{15} \text{ cm}^{-3}$ to a depth of $0.6 \text{ }\mu\text{m}$ changing to a substrate doping of 10^{13} cm^{-3} between 0.6 and $0.8 \text{ }\mu\text{m}$ which then extends to $1.0 \text{ }\mu\text{m}$. The applied gate voltage was $V_{GS} = 0 \text{ V}$ and the drain voltage was 0.5 V . A built-in voltage of -0.8 V was assumed at the gate. A drain current of 160 mA/cm was obtained. In this calculation a uniform square mesh of 10×5 elements was used. Results are given in Figs. 2.1 through 2.3. Figure 2.1 and 2.2 show the electron density on logarithmic and linear plots, respectively, while Fig. 2.3 shows the potential

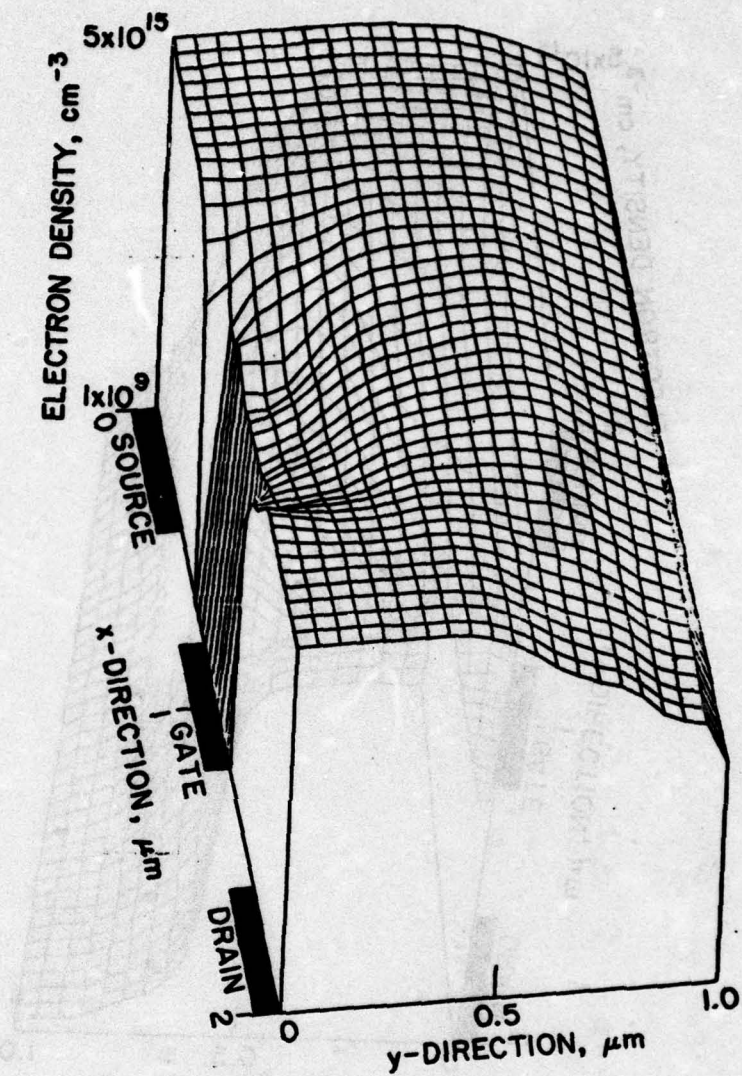


FIG. 2.1 LOGARITHMIC PLOT OF ELECTRON DENSITY DISTRIBUTION FOR GaAs MESFET.

$$V_{GS} = 0 \text{ V}, V_{DS} = 0.5 \text{ V}, N_D = 5 \times 10^{15} \text{ cm}^{-3}.$$

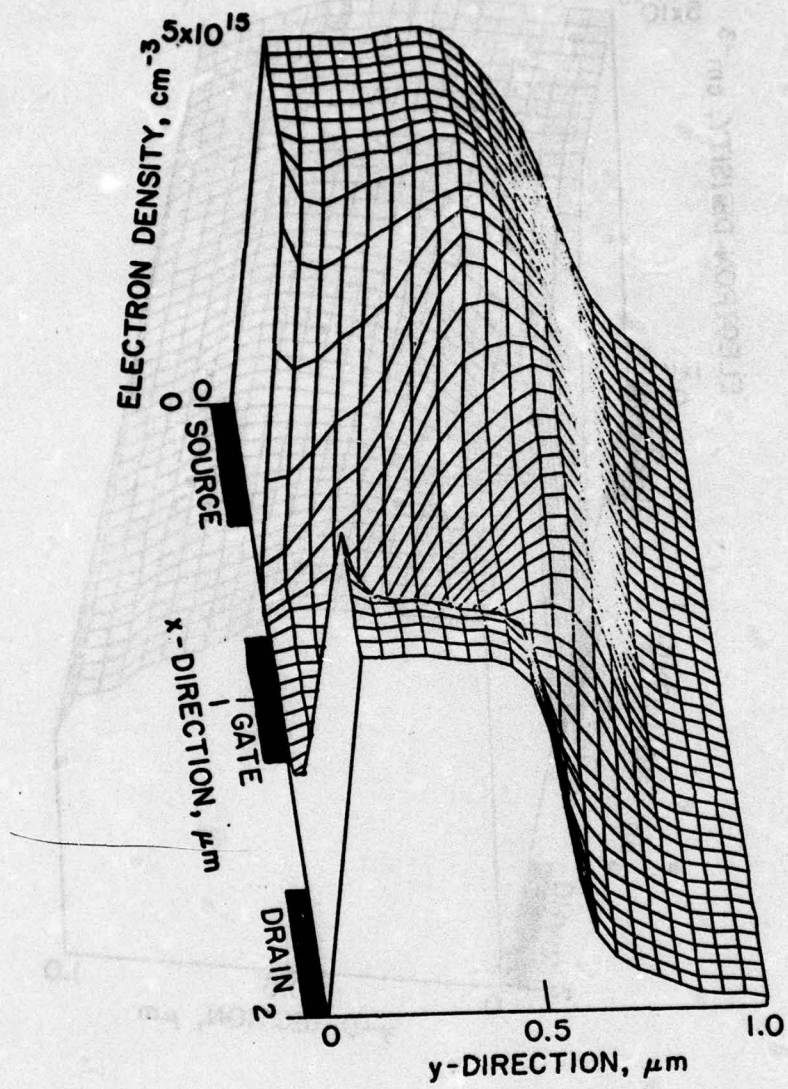


FIG. 2.2 LINEAR PLOT OF ELECTRON DENSITY DISTRIBUTION FOR GaAs MESFET.

$$V_{GS} = 0 \text{ V}, V_{DS} = 0.5 \text{ V}, N_D = 5 \times 10^{15} \text{ cm}^{-3}.$$

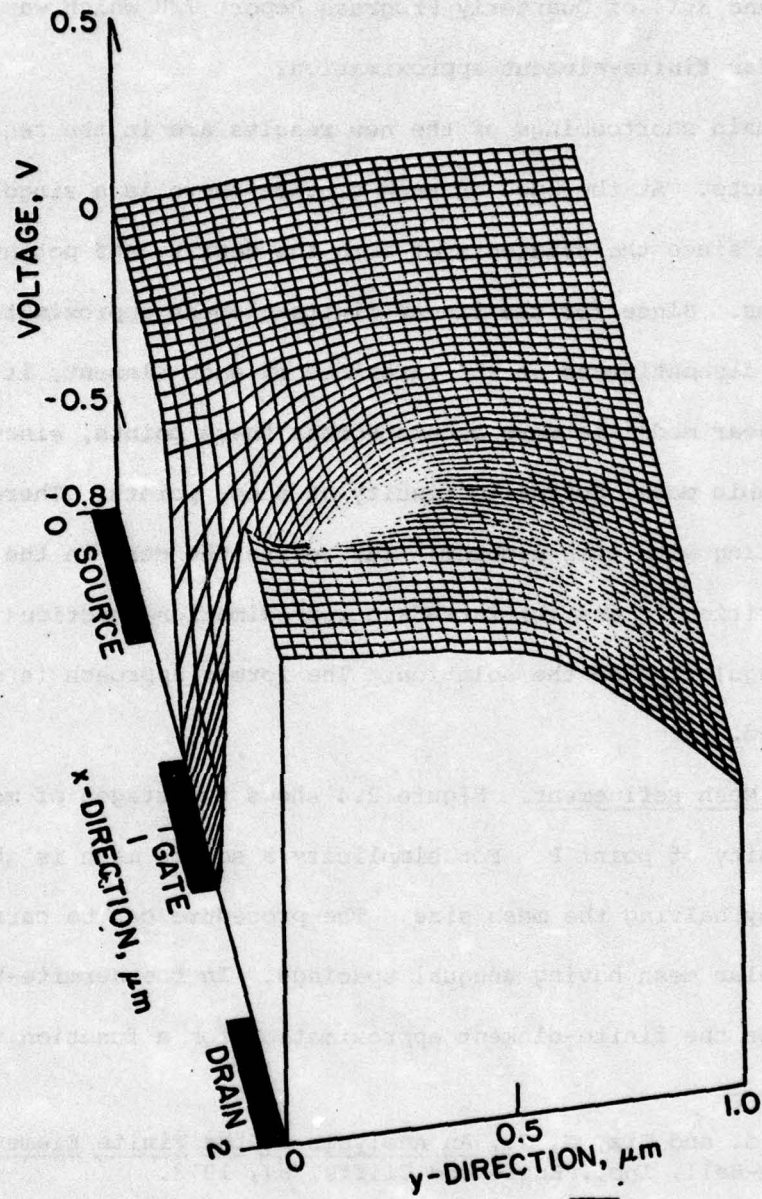


FIG. 2.3 POTENTIAL DISTRIBUTION FOR GaAs MESFET. $V_{GS} = 0$ V, $V_{DS} = 0.5$ V,
 $N_D = 5 \times 10^{15}$ cm⁻³.

distribution. This is a similar but not identical case to that shown in Figs. 3.13 and 3.14 of Quarterly Progress Report 7/8 which was computed using a linear finite-element approximation.

The main shortcomings of the new results are in the regions close to the contacts. At the edge of each contact there is a singularity of the solution since the gradients of both the density and potential are discontinuous. Since for the linear finite-element approximation the gradient is discontinuous at the interface of each element, it is possible that the linear model is more accurate near these points, since the Hermite-bicubic model forces continuity at these points. There are two ways of dealing with this problem:³ (a) refine the mesh in the vicinity of the singularities^{4,5} and (b) introduce approximation functions which possess the same singularity as the solution. The former approach is currently being studied.

2.4 Mesh Refinement. Figure 2.4 shows two stages of mesh refinement in the vicinity of point P. For simplicity a square mesh is shown with refinement by halving the mesh size. The procedure can be carried through for rectangular mesh having unequal spacings. In the Hermite-bicubic approximation the finite-element approximation for a function $u(x,y)$ is

3. Strang, G. and Fix, G. J., An Analysis of the Finite Element Method, Prentice-Hall, Inc., Englewood Cliffs, NJ, 1973.
4. Somerville, I. J., "A Technique for Mesh Grading Applied to Conforming Plate Bending Finite Elements," Int. J. Num. Meth. Engrg., vol. 7, pp. 310-312, 1973.
5. Cary, G. F., "A Mesh-Refinement Scheme for Finite Element Compositions," Comp. Meth. Appl. Mech. Engrg., vol. 7, No. 1, pp. 93-105, January 1976.

expressed in terms of the values of u , u_x , u_y , u_{xy} evaluated at the nodes, where the subscript signifies the partial derivative. At the interface of the original mesh and the refined mesh there will be points which belong to the refined elements but not the coarse mesh. These are labeled D1 and D2 in Fig. 2.4 and will be called "dummy" nodes. The values of u , u_x , u_y , u_{xy} at these nodes can be determined from the finite-element approximation for the adjacent unrefined element. In fact only the nodal values at each end of the corresponding element side are involved. The values of u , u_x , u_y , u_{xy} at all regular nodes can be grouped together into a vector \underline{u}_r . The dummy nodal values arising from the first refinement to one-half the original mesh size (D1 in Fig. 2.4) will be denoted \underline{u}_{d1} . The dummy nodes D2 from the second refinement will be denoted \underline{u}_{d2} and so on. At each level of refinement, the new dummy nodal values can be expressed in terms of all the previously defined values, regular and dummy. This can be written in matrix notation as

$$\begin{aligned}
 \underline{u}_{d1} &= \underline{S}_{10} \underline{u}_r , \\
 \underline{u}_{d2} &= \underline{S}_{21} \underline{u}_{d1} + \underline{S}_{20} \underline{u}_r , \\
 \underline{u}_{d3} &= \underline{S}_{32} \underline{u}_{d2} + \underline{S}_{31} \underline{u}_{d1} + \underline{S}_{30} \underline{u}_r .
 \end{aligned}
 \tag{2.1}$$

(Note: In this section, many of the matrices appearing are not square. Their dimensions may be inferred from the conformability properties.) The S-matrices are very sparse since only two nonzero u-coefficients appear in each right-hand term. From Eq. 2.1 the dummy terms can be eliminated successively to yield

$$\underline{u}_d = \underline{T} \underline{u}_r, \quad (2.2)$$

where

$$\underline{u}_d^t = (u_{d1}^t, u_{d2}^t, \dots, u_{dm}^t) \quad (2.3)$$

for m stages of refinement. It can be shown that formally

$$\begin{bmatrix} \underline{I} \\ \underline{T} \end{bmatrix} = \begin{bmatrix} \underline{I} \\ \underline{S}_m \end{bmatrix} \begin{bmatrix} \underline{I} \\ \underline{S}_{m-1} \end{bmatrix} \dots \begin{bmatrix} \underline{I} \\ \underline{S}_1 \end{bmatrix}, \quad (2.4)$$

where \underline{I} is the identity matrix and $\underline{S}_m = (S_{m,m-1}, S_{m,m-2}, \dots, S_{m0})$. Computationally it is more efficient to evaluate \underline{T} recursively, e.g., when m equals 3,

$$\underline{T} = \begin{bmatrix} \underline{S}_{10} \\ \underline{S}_{21} \underline{S}_{10} + \underline{S}_{20} \\ \underline{S}_{32} (\underline{S}_{21} \underline{S}_{10} + \underline{S}_{20}) + \underline{S}_{31} \underline{S}_{10} + \underline{S}_{30} \end{bmatrix}. \quad (2.5)$$

2.5 Modified Finite-Element Equations. The Ritz formulation of the finite-element method involves the minimization of a generalized energy expression. In a typical case such as Poisson's equation the energy functional will have the form

$$E \equiv \frac{1}{2} \underline{u}^t \underline{K} \underline{u} - \underline{f}^t \underline{u}, \quad (2.6)$$

where \underline{k} is the stiffness matrix and \underline{f} is the load vector (see previous reports for terminology). If \underline{K} is computed in the normal manner by adding contributions from all elements it is necessary to recall that because of Eq. 2.2, all components of \underline{u} are not independent, i.e., this is a constrained minimization problem. The minimization can be carried out by

the standard method of undetermined Lagrangian multipliers, but when \underline{T} is known, direct substitution is simplest formally. (Numerically, fewer equations result at the expense of greater bandwidth of the matrix.)

Thus

$$\underline{E} \equiv \frac{1}{2} \underline{u}_r^t \underline{E}^t \underline{K} \underline{E} \underline{u}_r - \underline{f}^t \underline{E} \underline{u}_r, \quad (2.7)$$

where

$$\underline{E} = \begin{bmatrix} \underline{I} \\ \underline{T} \end{bmatrix}. \quad (2.8)$$

The resulting linear equations are

$$\underline{E}^t \underline{K} \underline{E} \underline{u}_r = \underline{E}^t \underline{f}. \quad (2.9)$$

As discussed in earlier reports, the Ritz formulation cannot be used for the charge continuity equation, and instead the Galerkin method is being used. The Galerkin equations resulting from the standard procedure, treating dummy nodes on the same footing as regular nodes, will be (for the same problem as above)

$$\underline{K} \underline{u} = \underline{f}. \quad (2.10)$$

Because the constraint Eq. 2.2 must still be valid, Eq. 2.10 is an overdetermined set:

$$\underline{K} \underline{E} \underline{u}_r = \underline{f}. \quad (2.11)$$

To make the solution determinate an obvious possibility is to drop those equations corresponding to the dummy nodes. However, it can be shown that this destroys the conservation properties discussed in the previous report.

If Eq. 2.11 is premultiplied by E^t then Eq. 2.9 will result. This corresponds to reducing the number of equations by deleting those arising from the dummy nodes, but adding linear multiples of them to equations arising from adjacent regular nodes. It can be shown that the resulting Eq. 2.9 still retains the conservation property.⁶

2.6 Alternative Sparse Tableau Approach. An alternative approach which has been suggested by Hachtel⁷ is to defer elimination of the dummy variables. This results in a larger set of equations and unknowns but a much sparser matrix. If an optimum ordering algorithm is applied to this set it should give a solution time at least as good as when partial elimination is carried out previously, and in general better. Because optimization algorithms tend only to optimize each stage of elimination rather than optimize globally, the improvement is not necessarily obtained however. Nevertheless, because of the simplicity of equation formulation this approach is attractive.

Equation 2.1 may be rewritten as

$$\underline{Lu}_d = \underline{Su}_r \quad , \quad (2.12)$$

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6. Lomax, R. J., "Conservation Properties of the Finite-Element Method and Their Application to Semiconductor Device Modeling," submitted for publication.
 7. Hachtel, G., "The Sparse Tableau Approach to Finite-Element Assembly," Sparse Matrix Computations, Bunch, J. R. and Rose, D. J. (Ed.), Academic Press, Inc., New York, pp. 349-363, 1976.

where

$$\underline{L} = \begin{bmatrix} \underline{I} & & & & & \\ -\underline{S}_{21} & \underline{I} & & & & \\ -\underline{S}_{31} & -\underline{S}_{32} & \underline{I} & & & \\ \vdots & \vdots & \vdots & \ddots & & \\ -\underline{S}_{m1} & -\underline{S}_{m2} & \dots & -\underline{S}_{m,m-1} & \underline{I} & \end{bmatrix}, \quad \underline{S} = \begin{bmatrix} \underline{S}_{10} \\ \underline{S}_{20} \\ \underline{S}_{30} \\ \vdots \\ \underline{S}_{m0} \end{bmatrix}. \quad (2.13)$$

Note that \underline{L} is lower triangular. In addition the matrix \underline{K} is written in block form

$$\underline{K} = \begin{bmatrix} \underline{K}_{rr} & \underline{K}_{rd} \\ \underline{K}_{dr} & \underline{K}_{dd} \end{bmatrix}. \quad (2.14)$$

Then a set of equations equivalent to Eq. 2.9 and incorporating Eq. 2.1 is

$$\begin{bmatrix} \underline{K}_{rr} & \underline{K}_{rd} & -\underline{S}^t \\ \underline{K}_{dr} & \underline{K}_{dd} & \underline{L}^t \\ -\underline{S} & \underline{L} & \underline{O} \end{bmatrix} \begin{bmatrix} \underline{u}_r \\ \underline{u}_d \\ \underline{\Lambda} \end{bmatrix} = \begin{bmatrix} \underline{f}_r \\ \underline{f}_d \\ \underline{O} \end{bmatrix}, \quad (2.15)$$

where $\underline{\Lambda}$ represents an "undetermined multiplier" in the Langrangian sense.

To avoid pivoting due to the zeros in the bottom left of the matrix of Eq. 2.15, the set can be reordered as

$$\begin{bmatrix} \underline{L} & \underline{O} & \underline{S} \\ \underline{K}_{dd} & \underline{L}^t & \underline{K}_{dr} \\ \underline{K}_{rd} & -\underline{S}^t & \underline{K}_{rr} \end{bmatrix} \begin{bmatrix} \underline{u}_d \\ \underline{\Lambda} \\ \underline{u}_r \end{bmatrix} = \begin{bmatrix} \underline{O} \\ \underline{f}_d \\ \underline{f}_r \end{bmatrix}. \quad (2.16)$$

Gaussian elimination in the order suggested by Eq. 2.16 leads back immediately to Eqs. 2.2 and 2.9, however, as suggested by Hachtel, an ordering algorithm may find a more efficient order of elimination.

2.7 Conclusions. Detailed discussion of the conclusions of the MESFET study are given in Reference 1. In summary, two important effects merit attention with regard to improvements in device structure. The use of a lower doping in the high field region can increase I_D and g_m by reducing the saturated drift velocity degradation which occurs for electric fields much larger than needed to produce velocity saturation. As the gate length of experimental devices shrinks it is possible for the negative-resistance region in the device I_D vs. V_{DS} characteristics to be sufficient to cause the MESFET amplifier to oscillate, thus destroying the advantage over the Si MESFET gained by using the higher mobility GaAs material. Changes of geometry and doping in order to eliminate this effect can be simulated prior to device fabrication.

This study was unique in that it produced the first reported results of the application of the finite-element method to the solution of the time-dependent two-dimensional semiconductor device equations. Although Reiser has studied the Si MESFET,⁸ this was the first reported full two-dimensional simulation of the GaAs MESFET.⁹ The transient simulation was one of the few time-dependent two-dimensional simulations so far performed, and the transit-time limitation of performance was found in the structure

8. Reiser, M., "A Two-Dimensional Numerical FET Model for DC, AC and Large Signal Analysis," IEEE Trans. on Electron Devices, vol. ED-20, No. 1, pp. 35-45, January 1973.

9. Barnes, J. J. and Lomax, R. J., "Two-Dimensional Finite-Element Simulation of Semiconductor Devices," Electronics Letters, vol. 10, No. 16, pp. 341-343, August 1974.

under consideration.¹⁰ The results for the compensated doping in the high field region represent the only two-dimensional study of this feature thus far reported.¹¹

The simulation methods developed here may be used to study the MESFET in conjunction with an experimental investigation, or they may be used to study other semiconductor devices. The methods used for results obtained so far¹ are being refined² and improved⁷ to reduce the amount of computation time required and/or increase their accuracy. As improvements are made the possibility is opened up for more accurate and extensive large-signal simulation for a number of structures.

3. Investigations of FET Structures

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3.1 Introduction. Although the FET is inherently simpler in its principles of operation than the bipolar junction transistor (BJT), it was not until recently that the FET began to supplant the BJT in many applications. The advantages of the FET over its bipolar counterpart are numerous:

1. The FET is inherently less noisy than the BJT because it is not subject to the shot and recombination noise mechanisms which characterize

10. Barnes, J. J. and Lomax, R. J., "Transient Two-Dimensional Simulation of a Submicrometer Gate-Length M.E.S.F.E.T.," Electronics Letters, vol. 11, No. 21, pp. 519-521, October 1975.

11. Barnes, J. J. and Lomax, R. J., "Finite-Element Simulation of GaAs MESFETs with Compensated Doping Profiles and Submicron Gates," IEEE Trans. on Electron Devices, vol. ED-23, No. 9, September 1976.

BJT operation. Above 4 GHz, FETs are being routinely reported^{1,2} with lower noise figures than BJTs over comparable bandwidths.

2. Because the FET is a majority carrier device, fabrication materials can be chosen without regard to their minority carrier lifetime and transport properties.

3. The fabrication of FETs generally requires fewer high energy steps (e.g., impurity diffusion, ion implantation), resulting in potentially higher reliability and yield, as well as allowing more ingenuity in device design. This, combined with 2, allows the FET designer to utilize many promising new materials (GaAs, GaAlAs, InP, etc.) while sidestepping the potential problems associated with a new materials technology.

4. The large variety of FET structures available (e.g., junction, insulated-gate and Schottky-barrier-gate) allows the selection of the device most suitable to a given application as well as allowing greater potential for future development.

5. In general, greater packing density can be achieved using FETs over BJTs because fewer fabrication steps are required and because device isolation can usually be accomplished without the need for a separate diffusion.

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1. Turner, J. and Arnold, S., "Schottky-Barrier FETs--Next Low-Noise Designs," Microwaves, vol. 11, No. 4, pp. 44-49, April 1972.
 2. Liechti, C. A., "Microwave Field-Effect Transistors--1976," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-24, No. 6, pp. 279-300, June 1976.

For these and other reasons, the field-effect transistor has recently made significant advances in many fields such as computer memory and microprocessor development, microwave power generation and amplification and communications. All signs point to continued rapid growth in these and other fields in the years ahead.

3.2 Principles of Operation. A schematic diagram of a two-sided, symmetric, junction field-effect transistor with appropriately defined dimensional symbols is shown in Fig. 3.1. A depletion region exists at each of the p^+-n junctions. The width of the depletion region at any point is determined by the voltage between the gate terminal and the adjacent channel region. Thus by varying the gate voltage, the channel conductance can be modulated over a large range. As current flows in the channel, the ohmic voltage drop from source to drain will cause the shape of the depletion region to become distorted as shown in Fig. 3.2 with the drain biased positive relative to the source. Eventually the voltage at the drain will be sufficient to "pinch off" the channel, thus causing the current to saturate. Pinch-off will occur at different values of drain voltage and saturation current depending on the voltage at the gate (Fig. 3.3). If the FET is operated under reverse-gate-bias conditions, then the gate impedance will be very large and power gain can result.

In order to find a mathematical expression for the FET terminal currents and voltages, the following assumptions will be made:

1. No current flows across the reverse-biased p^+-n junction.
2. The length-to-width ratio L/a is much greater than unity.
3. The doping in the gate is sufficiently high that the depletion region lies entirely in the n-region.

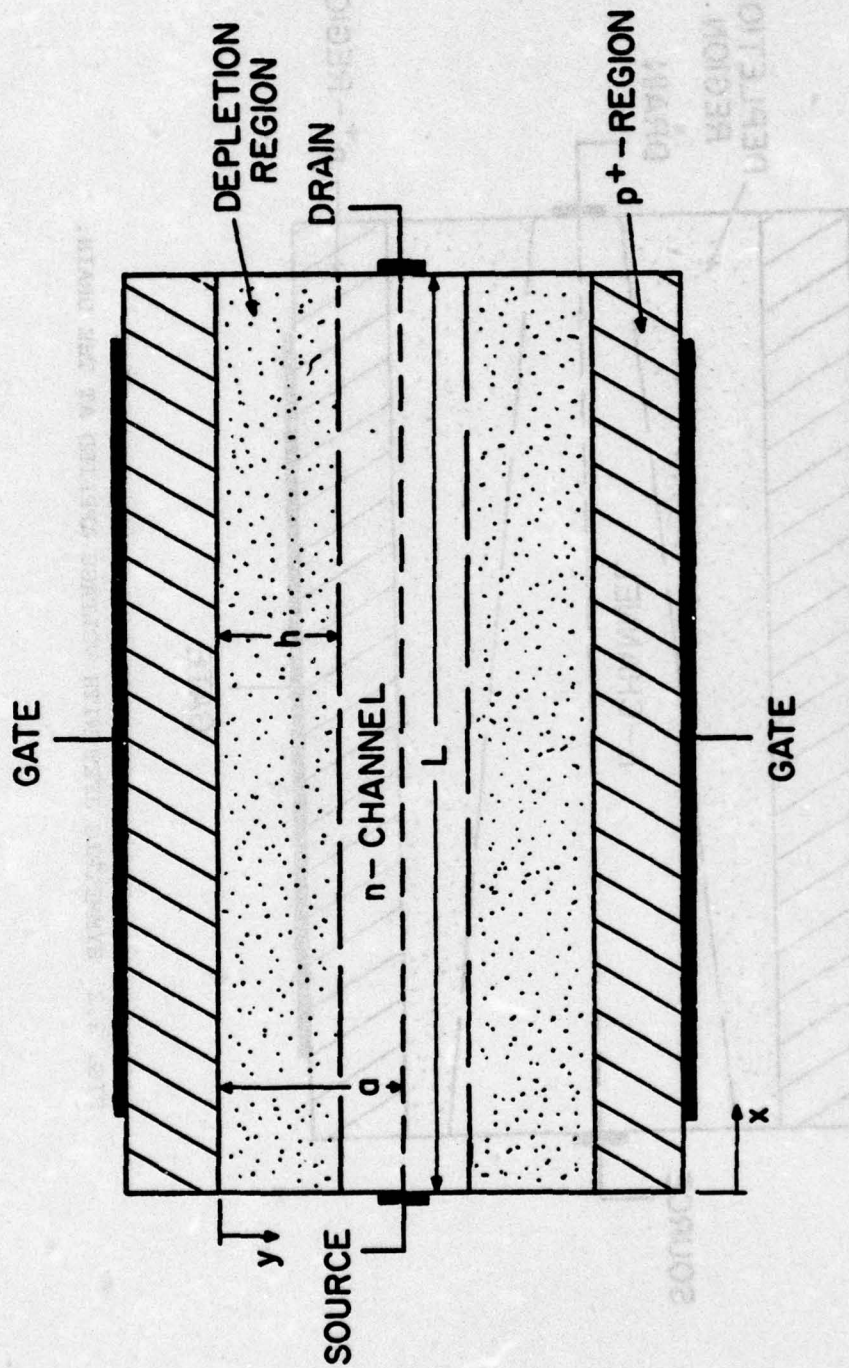


FIG. 3.1 SYMMETRIC JFET WITH NO VOLTAGE APPLIED AT THE DRAIN.

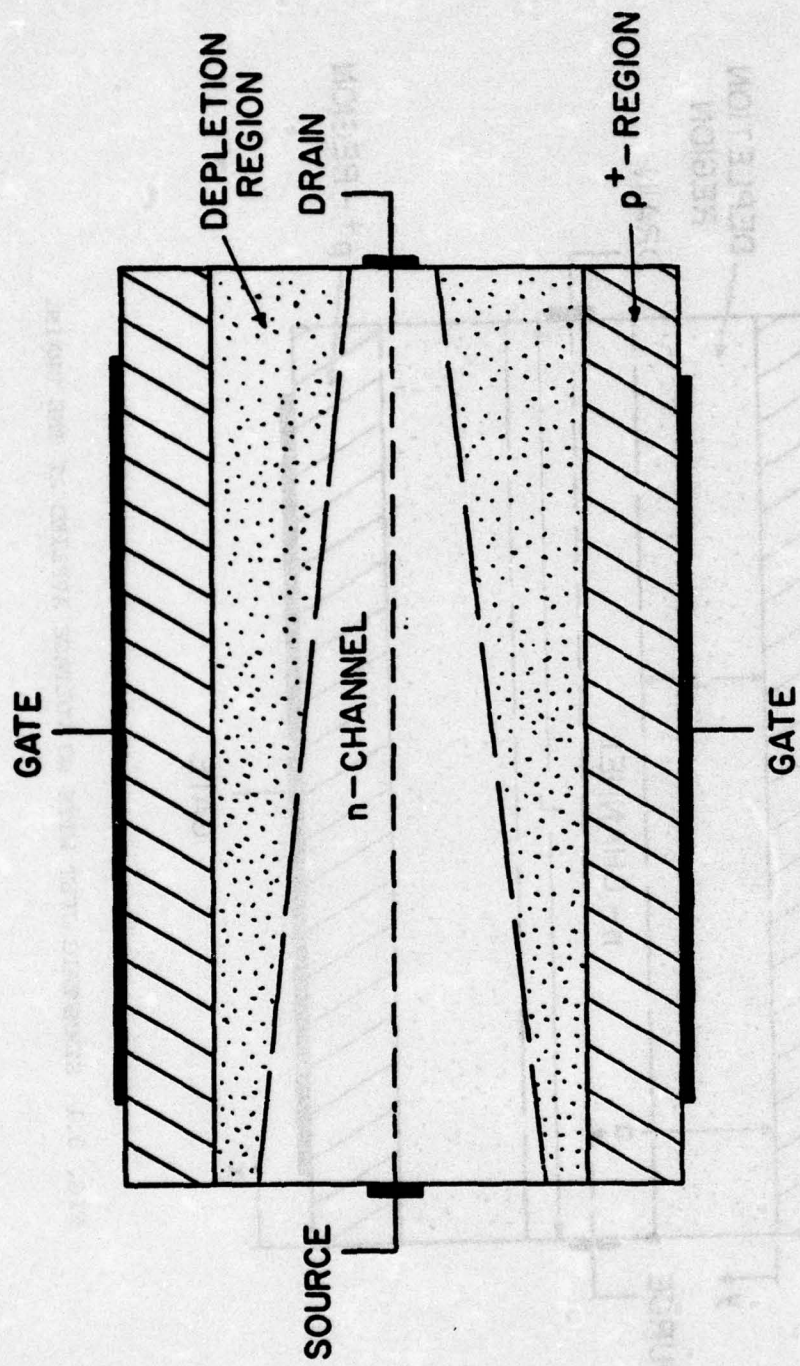


FIG. 3.2 SYMMETRIC JFET WITH VOLTAGE APPLIED AT THE DRAIN.

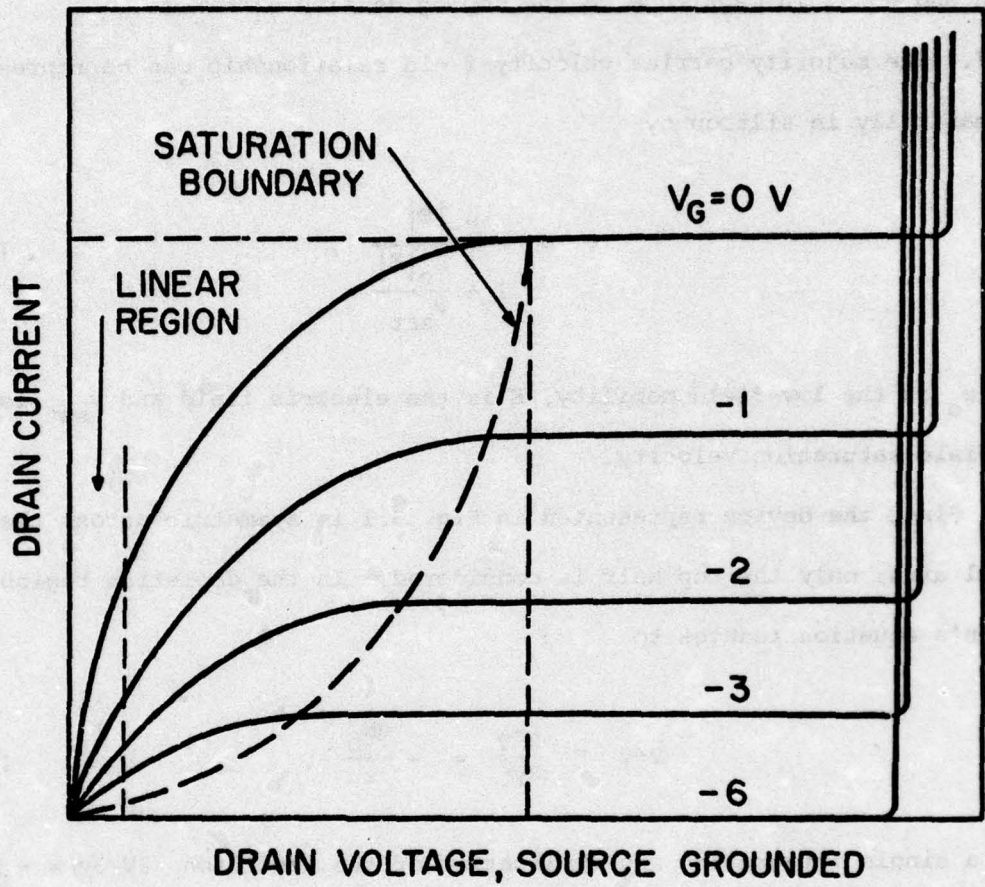


FIG. 3.3 OUTPUT CHARACTERISTICS OF COMMON-SOURCE FET (n-CHANNEL).

4. Minority carrier current is negligible everywhere.
5. Diffusion current is negligible everywhere.
6. The concentration of majority carriers is zero in the depletion region and equal in magnitude to the doping density elsewhere.
7. The majority carrier velocity-field relationship can be represented mathematically in silicon by

$$v = \frac{\mu_o |E|}{1 + \frac{\mu_o |E|}{v_{sat}}} \quad (3.1)$$

where μ_o is the low-field mobility, E is the electric field and v_{sat} is the high-field saturation velocity.

Since the device represented in Fig. 3.1 is symmetric across the channel axis, only the top half is considered. In the depletion region, Poisson's equation reduces to

$$\nabla^2 V = \frac{\partial^2 V}{\partial y^2} = - \frac{qN_D}{\epsilon} \quad (3.2)$$

After a single integration and application of the condition $\partial V / \partial y = - E_y = 0$ at the depletion edge, it is found that

$$\frac{\partial V}{\partial y} = - \frac{qN_D}{\epsilon} (y - h) \quad (3.3)$$

An additional integration and application of the voltage boundary condition at the junction results in

$$V = - \frac{qN_D}{\epsilon} \left(\frac{y^2}{2} - hy \right) + V_G - V_{bi} \quad (3.4)$$

where V_{bi} is the built-in junction potential. Then, on the channel boundary,

$$V(y = h) = \frac{qN_D h^2}{2\epsilon} + V_G - V_{bi} \quad (3.5)$$

From this expression, the values of the depletion width at the source and drain can be determined:

$$h_s = \left(\frac{2\epsilon}{qN_D} \right)^{1/2} (-V_G + V_{bi})^{1/2} = a \left(\frac{-V_G + V_{bi}}{V_p} \right)^{1/2} \quad (3.6)$$

and

$$h_D = \left(\frac{2\epsilon}{qN_D} \right)^{1/2} (V_D - V_G + V_{bi})^{1/2} = a \left(\frac{V_D - V_G + V_{bi}}{V_p} \right)^{1/2}, \quad (3.7)$$

where $V_p = qN_D a^2 / 2\epsilon$ is the total voltage required to deplete the entire channel and the source is taken to be at ground potential.

Ohm's law in the channel can be written as

$$E = \frac{J_n}{\sigma} \quad (3.8)$$

At any point in the channel the current density J_n is given by

$$J_n = - \frac{I_D}{2(a - h)Z} \quad (3.9)$$

and the channel conductivity can be written as

$$\sigma = qN_D \mu = \frac{qN_D \mu_o}{1 + \frac{\mu_o |E|}{v_{sat}}} \quad (3.10)$$

Thus,

$$E_x = -\frac{\partial V}{\partial x} = \frac{-I_D \left(1 + \frac{\mu_o}{v_{sat}} \frac{\partial V}{\partial x} \right)}{2qN_D \mu_o (a - h) Z} \quad (3.11)$$

or

$$I_D = 2qN_D \mu_o (a - h) Z \frac{\partial V}{\partial x} - \frac{I_D \mu_o}{v_{sat}} \frac{\partial V}{\partial x} \quad (3.12)$$

Integration from source to drain gives

$$I_D L = \int_0^L \left[2qN_D \mu_o (a - h) Z - \frac{I_D \mu_o}{v_{sat}} \right] \frac{\partial V}{\partial x} dx \quad (3.13)$$

Both h and $\partial V/\partial x$ are unknown functions of position along the channel.

However, if a change of variable is made from x to h , the integration can be carried out, i.e., since h is an explicit function of x , Eq. 3.13 can be written as

$$I_D L = \int_{h_S}^{h_D} \left[2qN_D \mu_o (a - h) Z - \frac{I_D \mu_o}{v_{sat}} \right] \frac{\partial V}{\partial h} dh$$

and substitution of Eq. 3.5 for $V(h)$ results in

$$I_D L = \frac{2q^2 N_D \mu_o Z}{\epsilon} \left[\frac{a}{2} (h_D^2 - h_S^2) - \frac{1}{3} (h_D^3 - h_S^3) \right] - \frac{I_D q N_D \mu_o}{2\epsilon v_{sat}} (h_D^2 - h_S^2) \quad (3.14)$$

Rearrangement and substitution of Eqs. 3.6 and 3.7 results in

$$I_D = \frac{2qN_D \mu_o Z a v_p}{L \left(1 + \frac{\mu_o v_D}{v_{sat}} L \right)} \left\{ \frac{v_D}{v_p} - \frac{2}{3} \left[\left(\frac{v_D - v_G + v_{bi}}{v_p} \right)^{3/2} - \left(\frac{-v_G + v_{bi}}{v_p} \right)^{3/2} \right] \right\} \quad (3.15)$$

3.2.1 Long-Channel Case. Equation 3.15 for the drain current as a function of terminal voltages is identical to the expression derived by Shockley³ with the exception of the term $[1 + (\mu_o v_D)/v_{sat} L]$ in the denominator of the coefficient. This term is a measure of "hot" electron effects in the channel, i.e., the extent to which electron velocities are saturated. If $\mu_o v_D/v_{sat} L \ll 1$, then the "hot" term can be neglected over the entire voltage range of operation of the device. Equation 3.15 for the "long-channel case" simplifies to

$$I_D = \frac{2qN_D \mu_o Z a v_p}{L} \left\{ \frac{v_D}{v_p} - \frac{2}{3} \left[\left(\frac{v_D - v_G + v_{bi}}{v_p} \right)^{3/2} - \left(\frac{-v_G + v_{bi}}{v_p} \right)^{3/2} \right] \right\} \quad (3.16)$$

This expression is plotted in Fig. 3.3 for several values of gate voltage.

From Eq. 3.16 the unsaturated transconductance g_m can be found:

$$g_m \triangleq \left. \frac{\partial I_D}{\partial v_G} \right|_{v_D = \text{constant}} = \frac{2qN_D \mu_o Z a}{L} \left[\left(\frac{v_D - v_G + v_{bi}}{v_p} \right)^{1/2} - \left(\frac{-v_G + v_{bi}}{v_p} \right)^{1/2} \right] \quad (3.17)$$

Likewise the unsaturated drain conductance g_d is found to be

- Shockley, W., "A Unipolar Field-Effect Transistor," Proc. IRE, vol. 40, No. 11, pp. 1365-1376, November 1952.

$$g_d \triangleq \left. \frac{\partial I_D}{\partial V_D} \right|_{V_G = \text{constant}}$$

$$= \frac{2qN_D \mu_o Z a}{L} \left[1 - \left(\frac{V_D - V_G + V_{bi}}{V_P} \right)^{1/2} \right] \quad (3.18)$$

In the linear region ($V_D \rightarrow 0$, Fig. 3.3), the drain conductance becomes

$$g_{do} = \frac{2qN_D \mu_o Z a}{L} \left[1 - \left(\frac{-V_G + V_{bi}}{V_P} \right)^{1/2} \right] \quad (3.19)$$

It is clear from Eq. 3.19 that the FET, unlike the BJT, can be operated as a voltage-controlled resistor since the output conductance is strongly dependent on gate voltage but independent of drain voltage in the linear region.

As the drain voltage increases, it will eventually become large enough to cause the depletion region to pinch off the conducting channel at the drain (Fig. 3.2). This condition will occur whenever

$$V_D - V_G + V_{bi} = V_P \quad (3.20)$$

This expression defines the saturation boundary for the FET and is shown as a dashed line in Fig. 3.3. When the saturation condition is substituted into Eq. 3.18, it is seen that the drain conductance becomes zero at that point, causing the current I_D to saturate.

It has been assumed in this analysis that a one-dimensional solution to Poisson's equation is valid in the depletion region. For values of drain voltage beyond pinchoff, this assumption can no longer be made near the drain. Several generalizations can be made however regarding operation of

the "long-channel" FET beyond pinchoff. The tendency for the pinched off channel to decrease the current is counteracted both by the effect of the large field in the channel beyond the pinchoff point as well as by the addition of a significant amount of diffusion current into the drain. As the drain voltage increases further, the pinchoff point will occur nearer the source, reducing the effective channel length and causing an increase in the drain current. This results in a slight upward tilt of the curves in Fig. 3.3 in saturation. When the drain voltage is large enough to break down the gate junction, very large currents will flow.

If it is assumed that the saturated current is nearly constant for a given gate voltage and equal to its value at pinchoff, then an analytical expression for both current and transconductance in saturation can be found. When Eq. 3.20 is substituted into Eq. 3.16 and is differentiated, it is found that

$$I_{Dsat} = \frac{2qN_D \mu_o Z a V_p}{L} \left\{ 1 - \frac{-V_G + V_{bi}}{V_p} - \frac{2}{3} \left[1 - \left(\frac{-V_G + V_{bi}}{V_p} \right)^{3/2} \right] \right\} \quad (3.21)$$

and

$$g_{msat} = \frac{2qN_D \mu_o Z a}{L} \left[1 - \left(\frac{-V_G + V_{bi}}{V_p} \right)^{1/2} \right] \quad (3.22)$$

3.2.2 Short-Channel Case. Whenever the channel is sufficiently short that $\mu_o V_p / v_{sat} L$ is not small compared with unity, Eq. 3.15 cannot be simplified. For this case, the electrons will reach their scattering-limited velocity v_{sat} before reaching the drain. The result of retaining the "hot" electron term in Eq. 3.15 is to decrease the value of drain

voltage as saturation sets in because of the additional current-limiting mechanism. This will cause both I_{Dsat} and g_{msat} to decrease below the values predicted by Eqs. 3.21 and 3.22, respectively, resulting in a falloff both in gain and available power.

In saturation the same mechanisms are operating as in the long-channel case to maintain a nearly constant drain current. However, the hot-electron effect complicates the voltage and electron distributions considerably. Since current saturation occurs before the drain voltage is sufficient to pinch off the channel, a finite channel width will remain open at the drain (Fig. 3.4). The injection of saturated carriers into this high-field region will cause an accumulation of electrons to build up in this narrow channel (Fig. 3.4) with a compensating depleted region being formed immediately beyond the drain edge of the gate where the field begins to decrease. Drain voltage in excess of the saturating voltage will be accounted for across this stationary dipole layer rather than in the movement of the pinchoff point toward the source.^{4,5}

3.2.3 Ac Small-Signal Considerations. A small-signal model of the common-source FET in saturation is shown in Fig. 3.5a. The active channel consisting of a distributed gate capacitance and channel conductance is modeled as the lumped series elements r_c and C_{gs} . The current generator

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4. Lehovec, K. and Miller, R., "Field Distribution in Junction Field-Effect Transistors at Large Drain Voltages," IEEE Trans. on Electron Devices, vol. ED-22, No. 5, pp. 273-281, May 1975.
 5. Kennedy, D. and O'Brien, R., "Computer-Aided Two Dimensional Analysis of the Junction Field-Effect Transistor," IBM J. Res. and Develop., vol. 14, No. 2, pp. 95-116, March 1970.

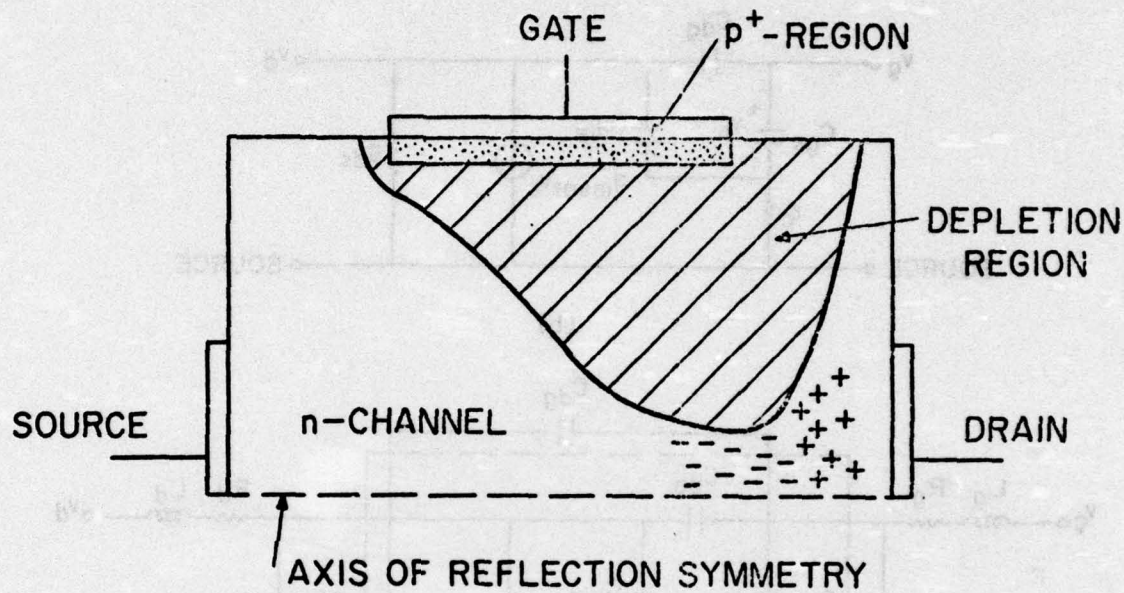


FIG. 3.4 SHORT CHANNEL JFET IN SATURATION.

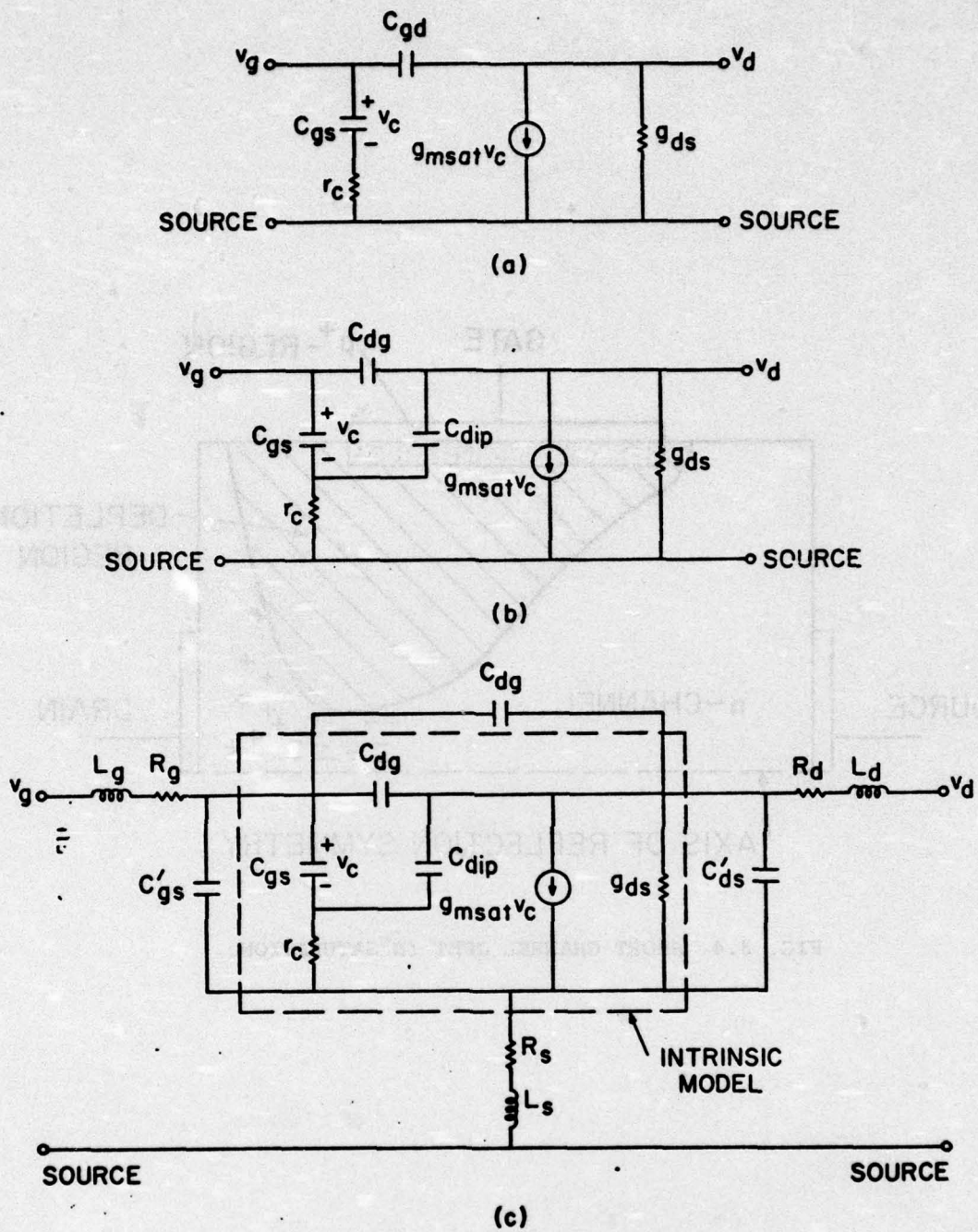


FIG. 3.5 CIRCUIT MODELS FOR JFET: (a) INTRINSIC LONG-CHANNEL JFET, (b) INTRINSIC SHORT-CHANNEL JFET, (c) EXTRINSIC JFET.

in the output is shown as the product of the transconductance g_{msat} and the voltage V_c across the capacitance C_{gs} . At low frequencies the capacitance will dominate the input admittance and thus the entire input signal V_g will be amplified in the output. However at higher frequencies, current will be drawn in the input circuit causing a voltage loss across r_c . The FET will therefore have an upper frequency limit beyond which no useful gain can result. Capacitance C_{gs} must be kept small in order to allow the cutoff frequency to be as high as possible.

Capacitance C_{gd} between gate and drain is degenerative feedback which degrades gain at high frequencies. The FET must therefore be designed to minimize this capacitance in order to operate at high frequencies. The output conductance g_{ds} includes the effect of the nonzero slope of the output characteristic in saturation although this conductance is usually small and can be neglected.

A simple two-port analysis of the intrinsic long-channel FET (Fig. 3.5a) results in the following expressions for the small-signal admittance parameters:

$$y_{11} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} r_c} + j\omega C_{gd} \quad (3.23)$$

$$y_{12} = -j\omega C_{gd} \quad (3.24)$$

$$y_{21} = \frac{g_{msat}}{1 + j\omega C_{gs} r_c} - j\omega C_{gd} \quad (3.25)$$

and

$$y_{22} = g_{ds} + j\omega C_{gd} \quad (3.26)$$

If the feedback capacitance C_{gd} is neglected, the current gain can be written as

$$h_{21} = \frac{y_{21}}{y_{11}} = \frac{g_{msat}}{j\omega C_{gs}} \quad (3.27)$$

Defining the cutoff frequency f_c as the frequency at which the current gain falls to unity, it is found that

$$f_c = \frac{g_{msat}}{2\pi C_{gs}} \quad (3.28)$$

An expression for C_{gs} can be written by recalling the expression for the depletion capacitance of a reverse-biased abrupt $p^+ - n$ junction,

$$C_{gs} = \left(\frac{qN_D \epsilon}{2V} \right)^{1/2} \times \text{junction area} \quad (3.29)$$

where V is the total bias across the junction (positive for reverse bias). Since the voltage across the gate capacitance varies from its smallest value at the source to V_p or more at the drain, it can be approximated by

$$\bar{V} = \frac{V_p}{2} \quad (3.30)$$

The area of the gate is simply LZ . It can be found that by substituting Eqs. 3.29 and 3.30 into 3.28,

$$f_c = \frac{\sqrt{2}}{\pi} \frac{\mu_o V_p}{L^2} \quad (3.31)$$

It is clear from Eq. 3.31 that the cutoff frequency of the intrinsic FET can be increased by (1) using materials with high majority carrier

mobility (such as GaAs which exhibits a low-field electron mobility of $5000 \text{ cm}^2/\text{V-s}$ compared with $1000 \text{ cm}^2/\text{V-s}$ in Si, (2) decreasing the channel length L , and (3) designing the device with as high a value of V_p as possible.

When the channel length L becomes small enough that hot-electron effects are significant, this analysis must be altered in several ways. First the small-signal model must be altered to include the capacitance of the dipole layer at the drain (Fig. 3.5b). In addition, it can be shown⁶ that the cutoff frequency will no longer increase as $\mu_o V_p/L^2$ but rather as v_{sat}/L . This is because in the low-field case, the average carrier velocity is proportional to the average channel field which varies as $1/L$. When the velocity becomes saturated, this dependence disappears. Thus f_c can be increased by decreasing the channel length L , although not as rapidly as for the long-channel case. The low-field mobility is not as important as the saturated drift velocity. This still makes GaAs a good candidate for FET fabrication since electron drift velocity in GaAs passes through a peak at $2 \times 10^7 \text{ cm/s}$ which is twice the value of v_{sat} for electrons in silicon (Fig. 3.6).

Parasitic impedances must also be added to the intrinsic device model as shown in Fig. 3.5c. R_s and R_d represent the effects of both contact resistances and the resistances of the unmodulated channel at the source and drain, respectively. R_g is the sum of the contact resistance and the bulk resistance of the gate. If extrinsic capacitances exist between

6. Hower, P. and Bechtel, G., "Current Saturation and Small-Signal Characteristics of GaAs Field-Effect Transistors," IEEE Trans. on Electron Devices, vol. ED-20, No. 3, pp. 213-220, March 1973.

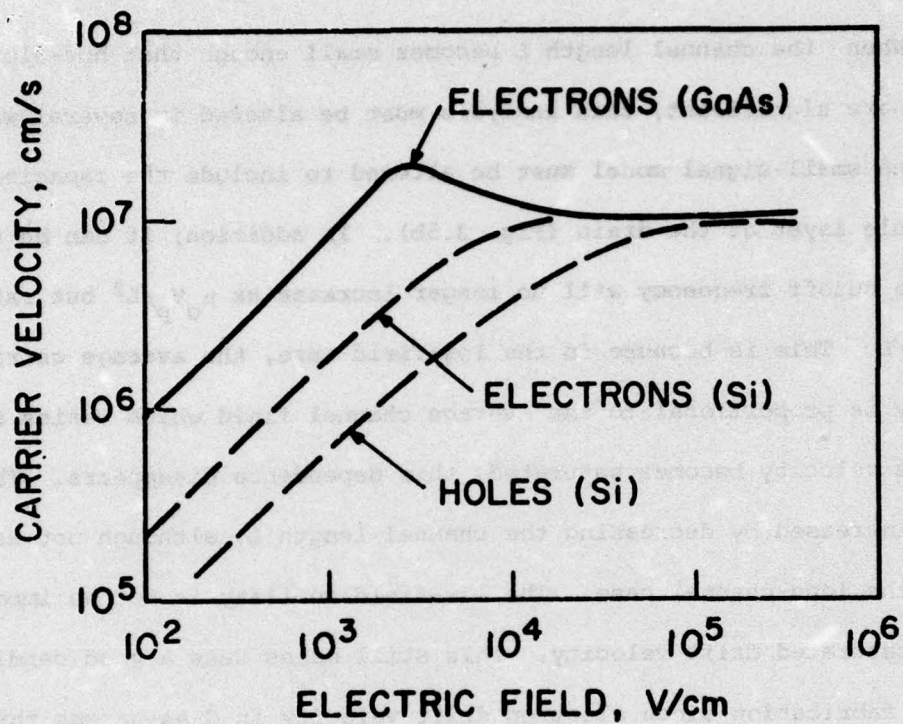


FIG. 3.6 VELOCITY VS. ELECTRIC FIELD CURVES FOR CARRIERS IN SILICON AND GALLIUM ARSENIDE.

terminals, they too must be added to the intrinsic model. L_s , L_g and L_d represent the inductances of leads and packages. In order to optimize the performance of the FET, all extrinsic impedances must be made negligible.

Much of the recent effort in FET development has centered on increasing the frequency response of the device. The principal limiting factor on the high-frequency operation of a well-designed FET is the transit time of majority carriers through the channel.⁷ One way to decrease the transit time is to maximize the majority carrier mobility and saturated drift velocity, for example, by selecting a semiconductor material which exhibits a very high intrinsic mobility and v_{sat} , and by limiting those factors which tend to degrade the carrier mobility such as surface and bulk recombination centers and high doping densities. The carrier transit time is also strongly dependent on the channel length L , varying as L^2 for the long-channel case and as L when carrier velocities are saturated over some part of the channel.⁶ The limiting frequency can thus be increased by making the FET gate length as short as possible. As improvements in lithographic techniques and material preparation have been made, submicron channel FETs in high-mobility materials have been reported⁸⁻¹¹ with power gain in X-band and above.

7. Dacey, G. C. and Ross, I. M., "The Field Effect Transistor," Bell Syst. Tech. J., vol. 34, No. 6, pp. 1149-1189, November 1955.
8. Turner, J. A., Waller, A. J., Bennett, R. and Parker, D., "An Electron Beam Fabricated GaAs Microwave Field Effect Transistor," 1970 Symp. GaAs and Related Compounds (Inst. Phys., Conf. Series No. 9), London, pp. 234-239, 1971.
9. Ozdemir, F., Ladd, G. O., Wolf, E. D., Perkins, W. E., Hirsch, N. and Cleary, F. W., "Electron Beam Fabrication 0.5 μ m Gate GaAs Schottky-Barrier Field-Effect Transistor," Tech. Digest 1974 Int. Electron Devices Meeting (Suppl.), Washington DC, p. 5, December 1974.

3.3 Proposed Microwave Junction FET. A new vertical JFET structure is proposed which is expected to achieve useful power gain in X-band. A cross-sectional diagram of the proposed JFET is shown in Fig. 3.7. This device is expected to have the following advantages over previously proposed microwave FET structures:

1. A submicron channel will be fabricated utilizing standard photolithographic techniques without requiring excessively small mask dimensions.
2. Electron mobility in the channel will be high due to the low doping levels used.
3. Parasitic source resistance will be greatly reduced.
4. Power dissipation will be greatly increased due to the proximity of the source contact to the active channel region.

The steps required to fabricate this device are shown schematically in Fig. 3.8. The starting material is epitaxial <100> p-type silicon on an n^+ -substrate. After windows are opened in the initial oxide layer an anisotropic etch is performed which serves to isolate each device from its neighbors. A fresh oxide is then grown to passivate the mesa and to mask subsequent steps. Next an anisotropic-source definition etch is carried out through carefully aligned windows. The dimensions of the source windows

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10. Baechtold, W., Daetwyler, K., Forster, T., Mohr, T. O., Walter, W. and Wolf, P., "Si and GaAs 0.5 μm -Gate Schottky-Barrier Field-Effect Transistors," Electronic Letters, vol. 9, No. 10, pp. 232-234, May 1973.
 11. Baudet, P., Binet, M. and Boccon-Gibod, D., "Submicrometer Self-Aligned GaAs MESFET," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-24, No. 6, pp. 372-376, June 1976.

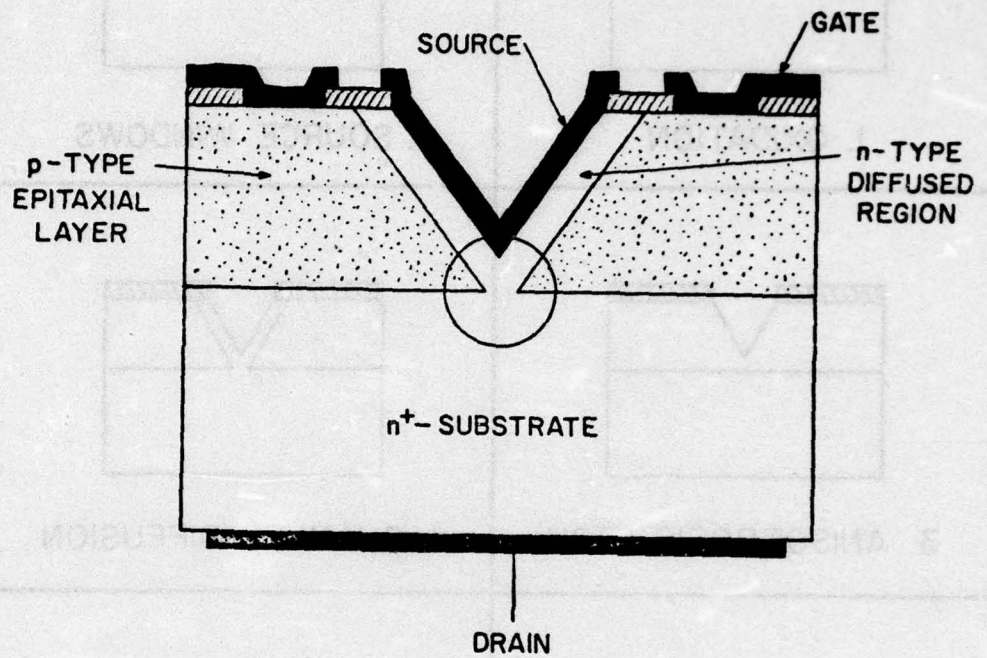


FIG. 3.7 PROPOSED VERTICAL JUNCTION FIELD-EFFECT TRANSISTOR.

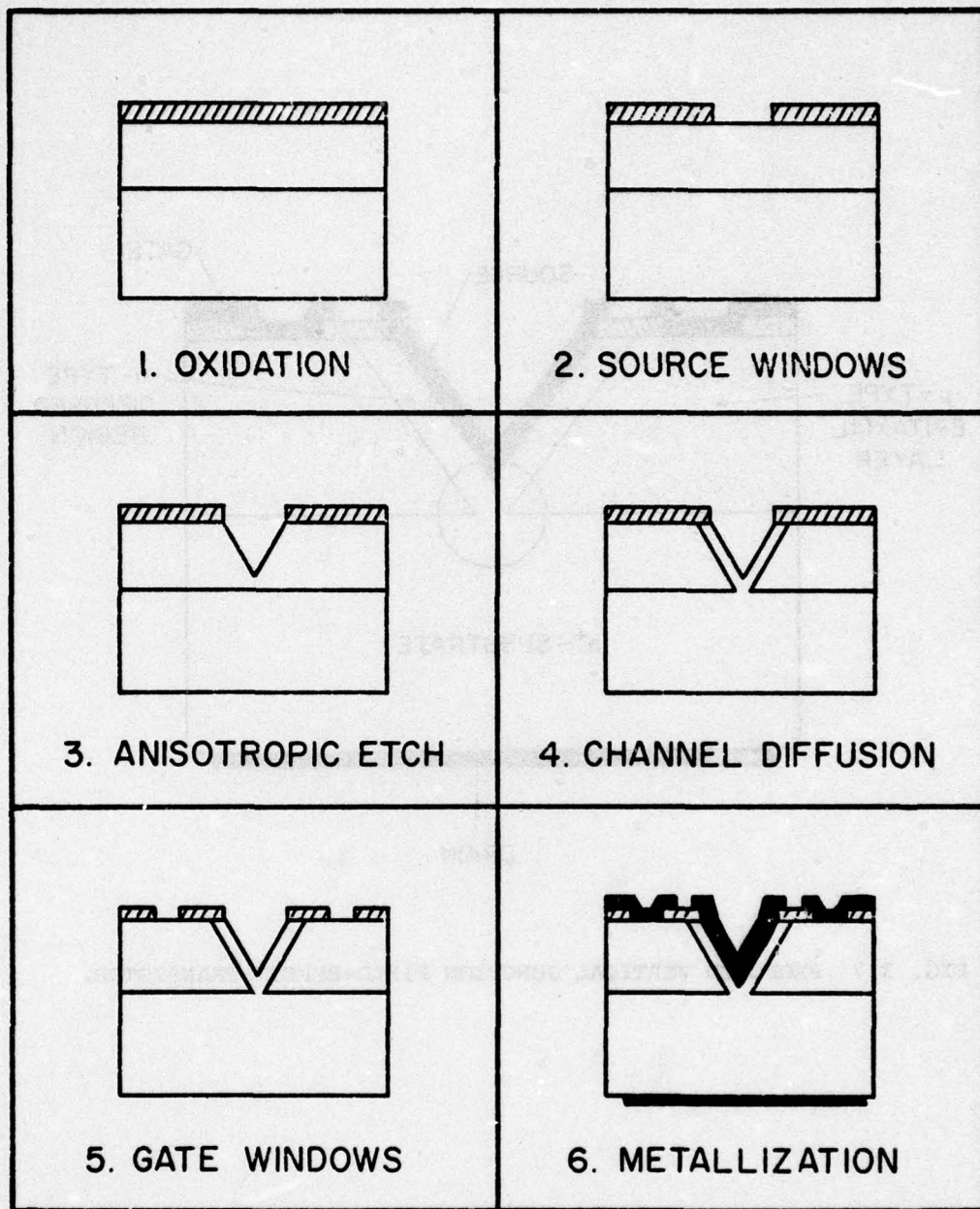


FIG. 3.8 FABRICATION SEQUENCE FOR VERTICAL JFET.

are controlled to yield a V-groove terminating a specified distance from the substrate. A phosphorus diffusion is then performed until the junction depth is sufficient to open an n-type channel with the desired channel height. Care is taken to achieve this diffusion with as low a final surface concentration as possible to assure high electron mobility in the channel. When gate windows are opened and the final metal pattern is defined, the vertical JFET is complete.

In order to achieve higher frequency operation, this device can be fabricated in GaAs with several procedural modifications. Oxidation steps must be replaced by the deposition of an appropriate insulating film. In addition the diffusion may be replaced by an ion-implantation step since high temperature diffusions are very difficult to accomplish in GaAs.

There are several factors which tend to limit the operating capabilities of this device. Considerable parasitic source-to-gate and drain-to-gate capacitances exist as well as a parasitic gate resistance. These must all be minimized to ensure operation at microwave frequencies. Source and drain parasitic resistances are not expected to be significant.

Since the channel length-to-width ratio is not large for the proposed JFET, the traditional, one-dimensional analysis³ cannot be used. A two-dimensional computer analysis utilizing a finite-element numerical simulation¹² has instead been employed to determine the expected terminal characteristics of the vertical FET. From this analysis, values of the transconductance at various bias voltages can be determined. A small-signal

12. Lomax, R. J., "Final Report on Transverse Effects in Avalanche Transit-Time Devices," NSF Grant No. GK-37581, Electron Physics Laboratory, The University of Michigan, Ann Arbor, August 1975.

model is then proposed to include the effects of parasitic circuit elements. This model is used to predict gain vs. frequency curves and f_c for the fabricated JFET which will be compared with experimentally obtained values.

3.4 Numerical Analysis of the Vertical JFET Structure. A two-dimensional numerical simulation of the vertical JFET structure has been performed for various bias conditions in order to better understand the principles of its operation. The simulation program¹² utilizes the finite-element method for analyzing time-dependent partial differential equations with boundary and initial conditions. The particular equations to be solved for the JFET structure are Poisson's equation,

$$\nabla^2 v = \frac{q}{\epsilon} (n - p - N_D + N_A) \quad (3.32)$$

and the continuity equations for electrons and holes, respectively,

$$\frac{\partial n}{\partial t} = \nabla \cdot (\underline{J}_n / q) + G_n - R_n \quad (3.33)$$

and

$$\frac{\partial p}{\partial t} = -\nabla \cdot (\underline{J}_p / q) + G_p - R_p, \quad (3.34)$$

where

$$\underline{J}_n / q = -n \underline{v}_n + D_n \nabla n, \quad (3.35)$$

$$\underline{J}_p / q = p \underline{v}_p - D_p \nabla p \quad (3.36)$$

and all other symbols take on their customary meanings. Equations 3.32 through 3.34 can be simplified by assuming that (1) minority carriers can be neglected everywhere and (2) generation and recombination can be neglected for the majority carriers everywhere in the device. Under these assumptions Equations 3.32 through 3.34 can be written separately on each side of the junction as

$$\nabla^2 v = \frac{q}{\epsilon} (n - N_D) \quad (3.37)$$

and

$$\frac{\partial n}{\partial t} = \nabla \cdot (\underline{J}_n / q) \quad (3.38)$$

on the n-side, and

$$\nabla^2 v = - \frac{q}{\epsilon} (p - N_A) \quad (3.39)$$

and

$$\frac{\partial p}{\partial t} = - \nabla \cdot (\underline{J}_p / q) \quad (3.40)$$

on the p-side.

The finite-element representation of the semiconductor equations has been used to obtain the desired solutions. A complete discussion of this method is contained in the text of Strang and Fix.¹³ The basic technique is to use a FORTRAN computer program to formulate Poisson's equation and the majority carrier continuity equation in terms of their finite-element representations and then to solve alternately for the voltage and carrier concentration approximating functions over a specified number of time steps. The element shape functions chosen for this analysis are simply linear functions containing constants which are independent of time and position. A complete description of the finite-element method as applied to the vertical JFET structure is contained in the technical report which is presently in preparation. The report contains information pertaining to

13. Strang, G. and Fix, G. J., An Analysis of the Finite-Element Method, Prentice-Hall, Inc., Englewood Cliffs, NJ, 1973.

the conservation properties as applied to the terminal currents as well as stability considerations.

3.5 Two-Dimensional Vertical JFET Model. In order to use the finite-element numerical technique described above to analyze the proposed FET structure, a two-dimensional model of the interior of the device must be constructed with an appropriate grid overlay. The model chosen for this analysis is shown in Fig. 3.9. Because of the symmetry of the device, only half of the structure must be considered. Compensation for the reflection symmetry can then be taken into account where necessary. A regular grid overlay consisting of isosceles triangles with height $0.092 \mu\text{m}$ and base $0.13 \mu\text{m}$ was superimposed over the model. The angle at the base of each triangular element is 54.76 degrees compared with 54.74 degrees for the angle between a $\langle 111 \rangle$ plane and its adjacent $\{110\}$ vector in the Si face-centered cubic lattice. The doping distribution is shown in Fig. 3.10. A donor concentration of $N_D = 5 \times 10^{15} \text{ cm}^{-3}$ was assumed for the n-type channel. This was increased to $N_D = 1 \times 10^{16} \text{ cm}^{-3}$ in the n^+ -drain and near the source to simulate ohmic contact regions. Similarly in the p-type gate, the acceptor concentration was chosen as $N_A = 5 \times 10^{15} \text{ cm}^{-3}$ with an increase to $N_A = 1 \times 10^{16} \text{ cm}^{-3}$ near the gate contact.

Dirichlet boundary conditions were assumed for all conducting boundaries (designated with heavy black borders in Fig. 3.9); i.e., for Poisson's equation,

$$V = \begin{cases} 0 & \text{at all source nodes,} \\ V_G & \text{at all gate nodes,} \\ V_D & \text{at all drain nodes,} \end{cases} \quad (3.41)$$

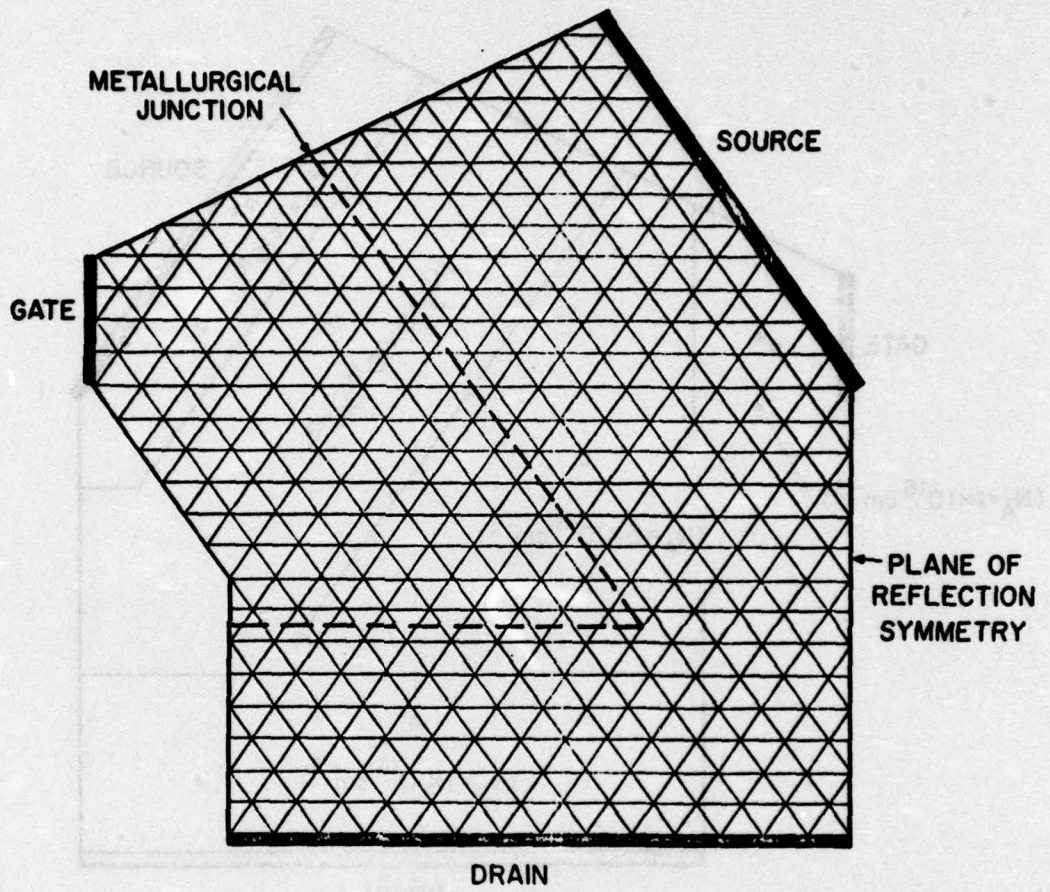


FIG. 3.9 TWO-DIMENSIONAL MODEL OF VERTICAL JFET FOR NUMERICAL ANALYSIS.

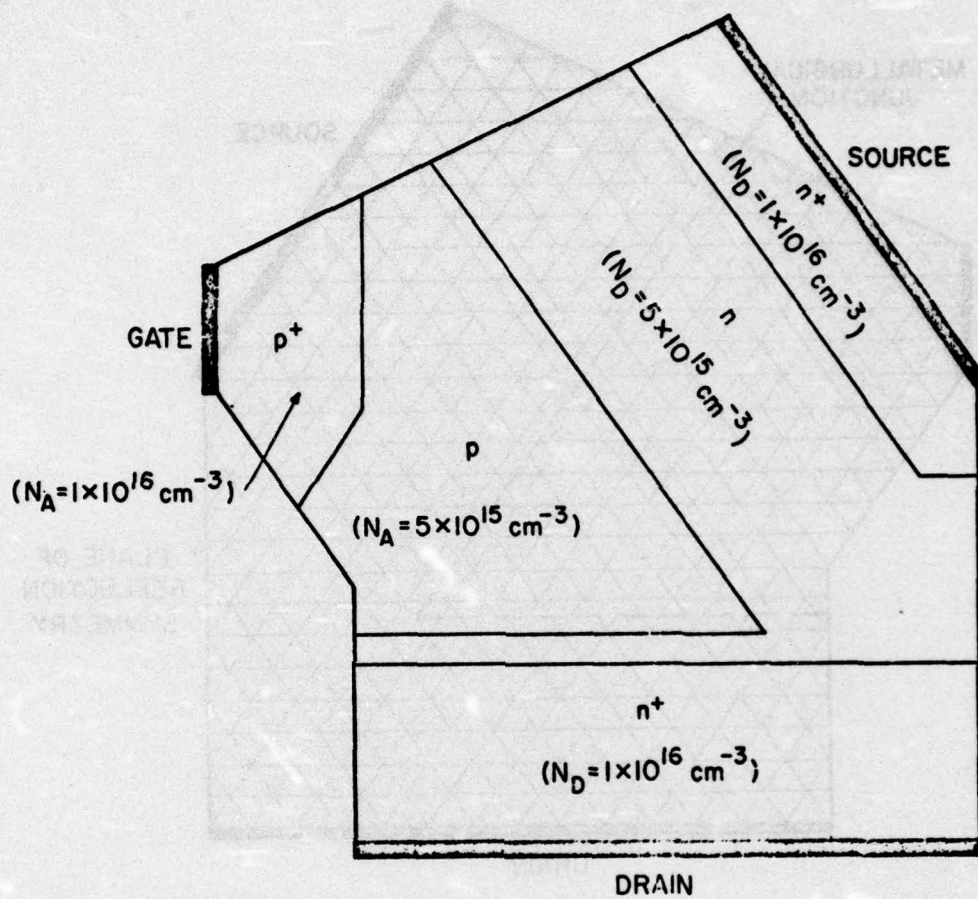


FIG. 3.10 DOPING DISTRIBUTION IN TWO-DIMENSIONAL JFET MODEL FOR NUMERICAL ANALYSIS.

and for the continuity equations,

$$n = 1 \times 10^{16} \text{ cm}^{-3} \quad (3.42)$$

at all source and drain nodes, and

$$p = 1 \times 10^{16} \text{ cm}^{-3} \quad (3.43)$$

at all gate nodes. At all other boundary nodes, Neumann conditions were assumed so that for Poisson's equation,

$$\nabla V = 0 \quad (3.44)$$

at all nonconducting boundary nodes, and for the continuity equations,

$$\nabla n = 0 \quad (3.45)$$

at all n-type nonconducting boundary nodes, and

$$\nabla p = 0 \quad (3.46)$$

at all p-type nonconducting boundary nodes.

For the first program run (corresponding to a given value of V_G and V_D), the initial conditions on n and p at each node in the model were chosen as

$$n = N_D \quad (3.47)$$

and

$$p = N_A \quad (3.48)$$

For all successive runs, initial conditions on n and p were chosen as the final values from the previous run. Data were taken in a sequence which

minimized the change in V_D and/or V_G for successive runs in order to optimize the convergence rate of the program. Initial conditions on the voltage were not required since Poisson's equation was solved first for each run.

A velocity vs. electric field relationship of the form

$$v_n = - \frac{\mu_{no} E}{1 + \frac{\mu_{no} |E|}{v_{nsat}}} \quad (3.49)$$

was assumed for electrons and

$$v_p = \frac{\mu_{po} E}{1 + \frac{\mu_{po} |E|}{v_{psat}}} \quad (3.50)$$

for holes where $\mu_{no} = 1200 \text{ cm}^2/\text{V-s}$, $\mu_{po} = 400 \text{ cm}^2/\text{V-s}$, and $v_{nsat} = v_{psat} = 1 \times 10^7 \text{ cm/s}$. Electron and hole diffusion coefficients D_n and D_p were assumed to be independent of electric field with values of $31.1 \text{ cm}^2/\text{s}$ and $10.4 \text{ cm}^2/\text{s}$, respectively.

A time step of $\Delta t = 5 \times 10^{-13} \text{ s}$ was selected. This value satisfies both the dielectric relaxation time constraint,

$$\Delta t \leq \min \left(\frac{\epsilon}{q\mu_p F}, \frac{\epsilon}{q\mu_n n} \right) = 5.4 \times 10^{-13} \text{ s} ,$$

and the causality condition,

$$\Delta t \leq \frac{2(\Delta x)^2}{v_{nsat}(\Delta x) + 2D_n} = 1.1 \times 10^{-12} \text{ s} .$$

3.6 Results of the Analysis.

3.6.1 Dc Output Characteristics. The finite-element analysis program was run for several values of V_G and V_D with the source at ground potential. The voltage and majority carrier distributions for each case were allowed to evolve over many time steps until a steady-state solution was reached. Convergence was assumed when the maximum change in voltage at any node was less than 0.009 V per time step and the maximum change in carrier concentration at any node was less than $7.5 \times 10^{13} \text{ cm}^{-3}$ per time step. At each terminal (source, gate and drain), the values of drift, diffusion and displacement currents were then calculated from the voltage and carrier distributions. As a further check on convergence, the total gate current was calculated. For an ideal JFET with a reverse-biased gate, the dc gate current should never be more than the reverse saturation current for a Si pn junction. However, for the purposes of this analysis, it is required only that the gate current be negligible in comparison with typical values of drain current near saturation. In fact for the cases considered, the gate current was never more than 0.9 A/m or 0.7 percent of the maximum drain current observed.

Values of total drain current for several values of V_G and V_D are plotted in Fig. 3.11. Output conductance g_{ds} and transconductance g_m were calculated from the curves of Fig. 3.11 and are plotted in Fig. 3.12. The long-channel one-dimensional JFET model discussed in Section 3.2.1 predicts that for a given V_G , the value of transconductance in saturation, g_{msat} , will be equal to the output conductance at $V_D = 0$ (g_{do}). For the proposed vertical JFET, the transconductance is expected to be much less than g_{do} for the following reasons:

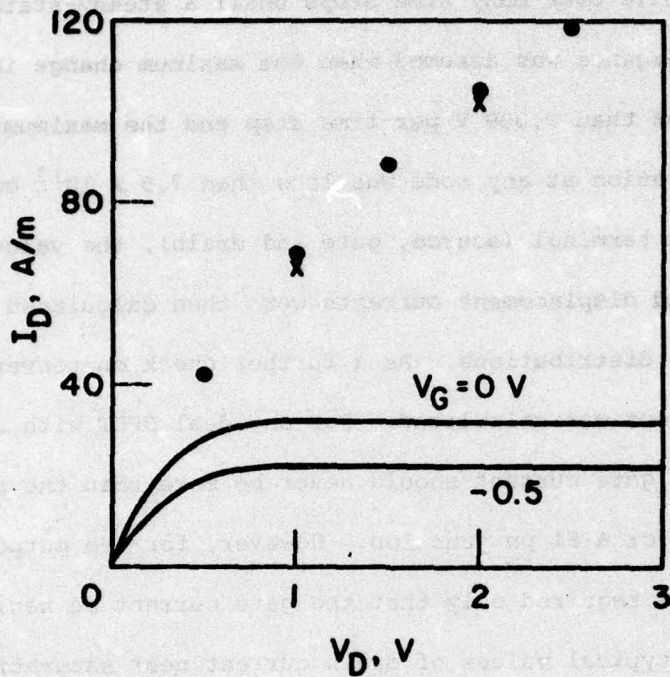


FIG. 3.11 OUTPUT CHARACTERISTICS OF VERTICAL JFET FROM NUMERICAL ANALYSIS

(• $V_G = 0$, × $V_G = -0.5$ V). SOLID LINES REPRESENT OUTPUT CHARACTERISTICS FROM EQ. 3.51).

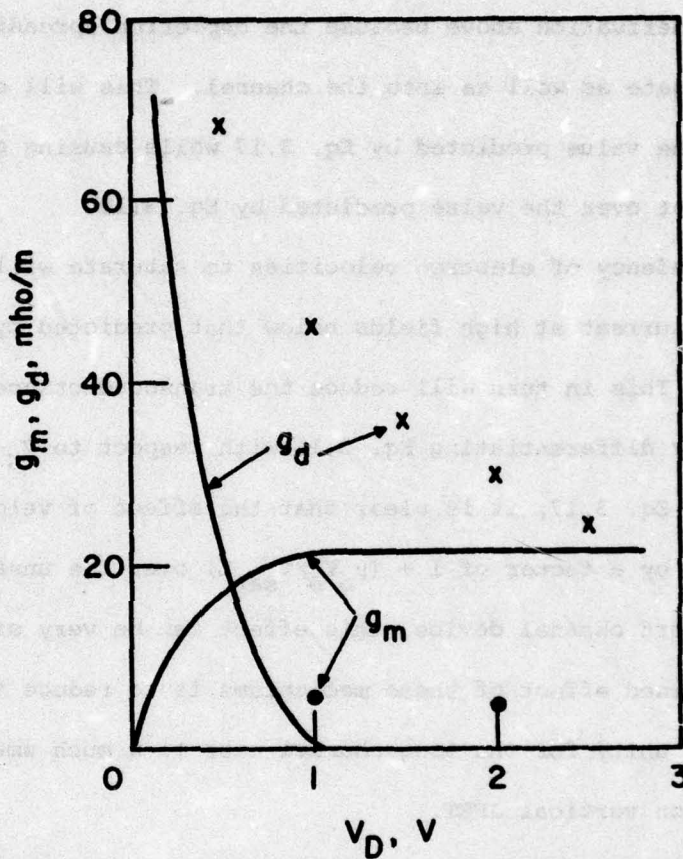


FIG. 3.12 TRANSCONDUCTANCE g_m AND DRAIN CONDUCTANCE g_d OF JFET FROM NUMERICAL ANALYSIS. (\cdot g_m AT $V_G = -0.25$ V, \times g_d AT $V_G = 0$). SOLID LINES REPRESENT g_m ($V_G = -0.25$ V) AND g_d ($V_G = 0$) DERIVED FROM EQ. 3.51.

1. The doping concentration in the gate is of the same order of magnitude as the doping concentration in the channel for the vertical JFET. A given change in gate voltage will affect the channel width of a pn junction FET significantly less than that of the p⁺n junction case assumed in the derivation above because the depletion spreading will occur into the gate as well as into the channel. This will cause g_m to decrease from the value predicted by Eq. 3.17 while causing g_{do} to increase somewhat over the value predicted by Eq. 3.19.

2. The tendency of electron velocities to saturate will reduce the value of drain current at high fields below that predicted by the long-channel model. This in turn will reduce the transconductance but will not affect g_{do} . By differentiating Eq. 3.15 with respect to V_G and comparing the result with Eq. 3.17, it is clear that the effect of velocity saturation is to reduce g_m by a factor of $1 + (\mu_o V_D / v_{sat} L)$ over the unsaturated case. For a short channel device, this effect can be very significant.

The combined effect of these mechanisms is to reduce the ratio of g_{msat}/g_{do} from unity for the long-channel case to a much smaller value for the submicron vertical JFET.

In order to evaluate the results of the numerical simulation it is necessary to make an approximate analysis of the JFET structure. By analogy with Eq. 3.15, it shall be assumed that the output characteristic takes the form

$$I_D = \frac{g_o V_p}{1 + \frac{\mu_o V_D}{v_{sat} L}} \left\{ \frac{V_D}{V_p} - \frac{2}{3} \left[\left(\frac{V_D - V_G + V_{bi}}{V_p} \right)^{3/2} - \left(\frac{-V_G + V_{bi}}{V_p} \right)^{3/2} \right] \right\} \quad (3.51)$$

where g_0 is the channel conductance with no depletion layer formed, V_p is the pinchoff voltage of an abrupt two-sided junction FET, and all other symbols take their usual meanings. Equation 3.51 is plotted in Fig. 3.11 for $V_G = 0$ and -0.5 V. It is clear that the values of I_D obtained from the numerical analysis are significantly greater in each case than those predicted by Eq. 3.51. A comparison of the transconductance derived from Eq. 3.51 with those values obtained from the numerical analysis (Fig. 3.15) shows that the output current is not as strongly affected by the gate voltage as Eq. 3.51 indicates. It is therefore necessary to examine more closely the electric fields and electron distributions within the FET structure and how they vary with changing terminal voltages in order to determine what transport mechanisms are operating in the FET that are not incorporated into Eq. 3.51.

3.6.2 Electron Concentration and Electric Field. Figures 3.13 and 3.14 represent electron and hole concentration contour plots for the vertical JFET structure with no bias on the gate and drain bias of 0.5 V and 2.0 V, respectively. Figure 3.15 is the same contour plot with $V_G = -0.5$ V and $V_D = 2.0$ V. Each contour represents equal values of electron or hole concentration as a percentage of the doping level at every point in the structure. From Figs. 3.13 to 3.15, it is clear that the electron concentration in the channel can be much greater than the donor concentration there, resulting in sizable accumulation regions. This is a violation of the assumption that the electron concentration in the undepleted areas of the channel is equal to the donor density. Since this assumption was fundamental to the derivation of Eq. 3.15 and thus of Eq. 3.51, these equations can no longer be expected to predict actual

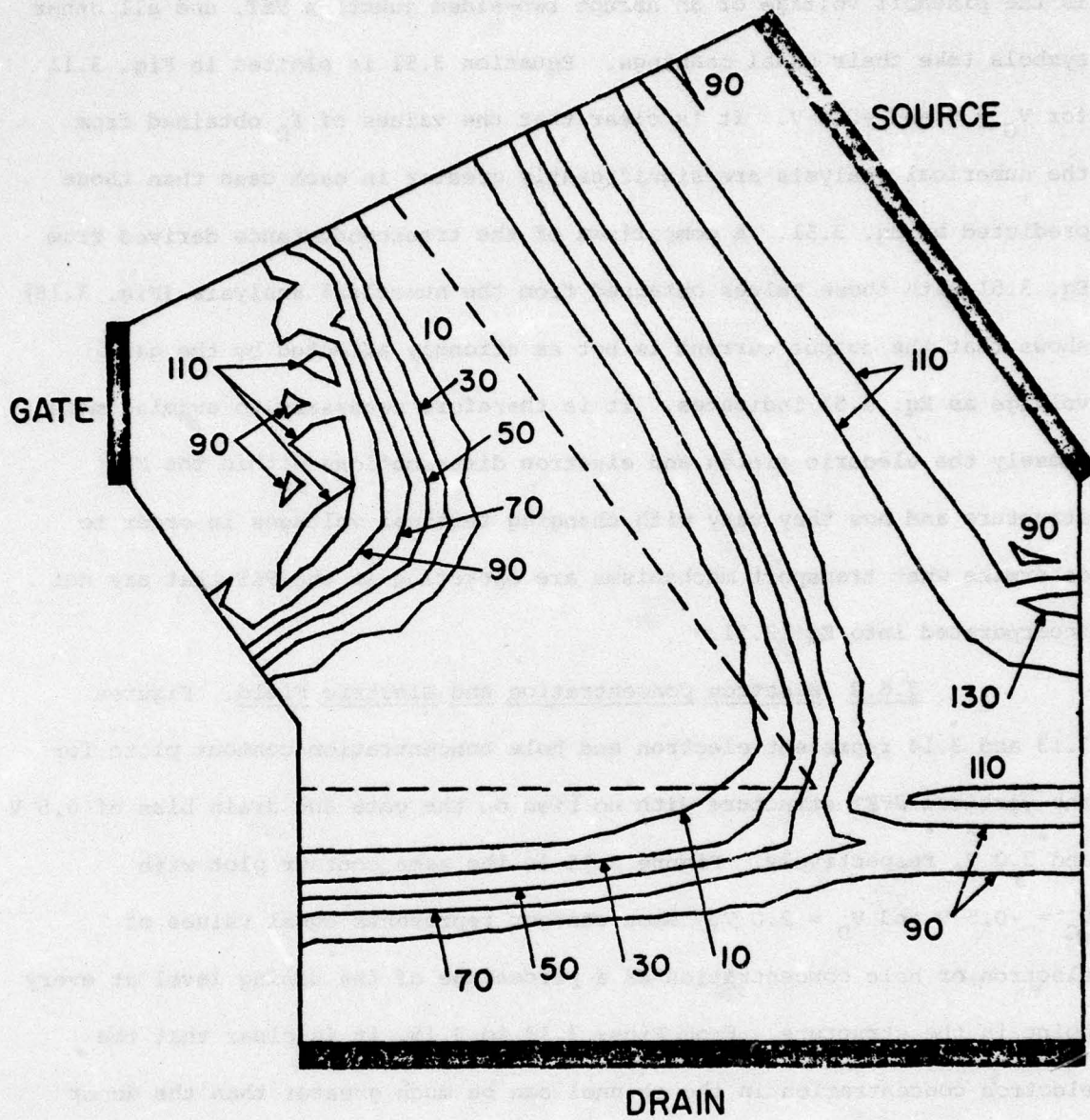


FIG. 3.13 CARRIER CONCENTRATION CONTOURS AS PERCENTAGE OF DOPING CONCENTRATION. ($V_G = 0$, $V_D = 0.5$ V)

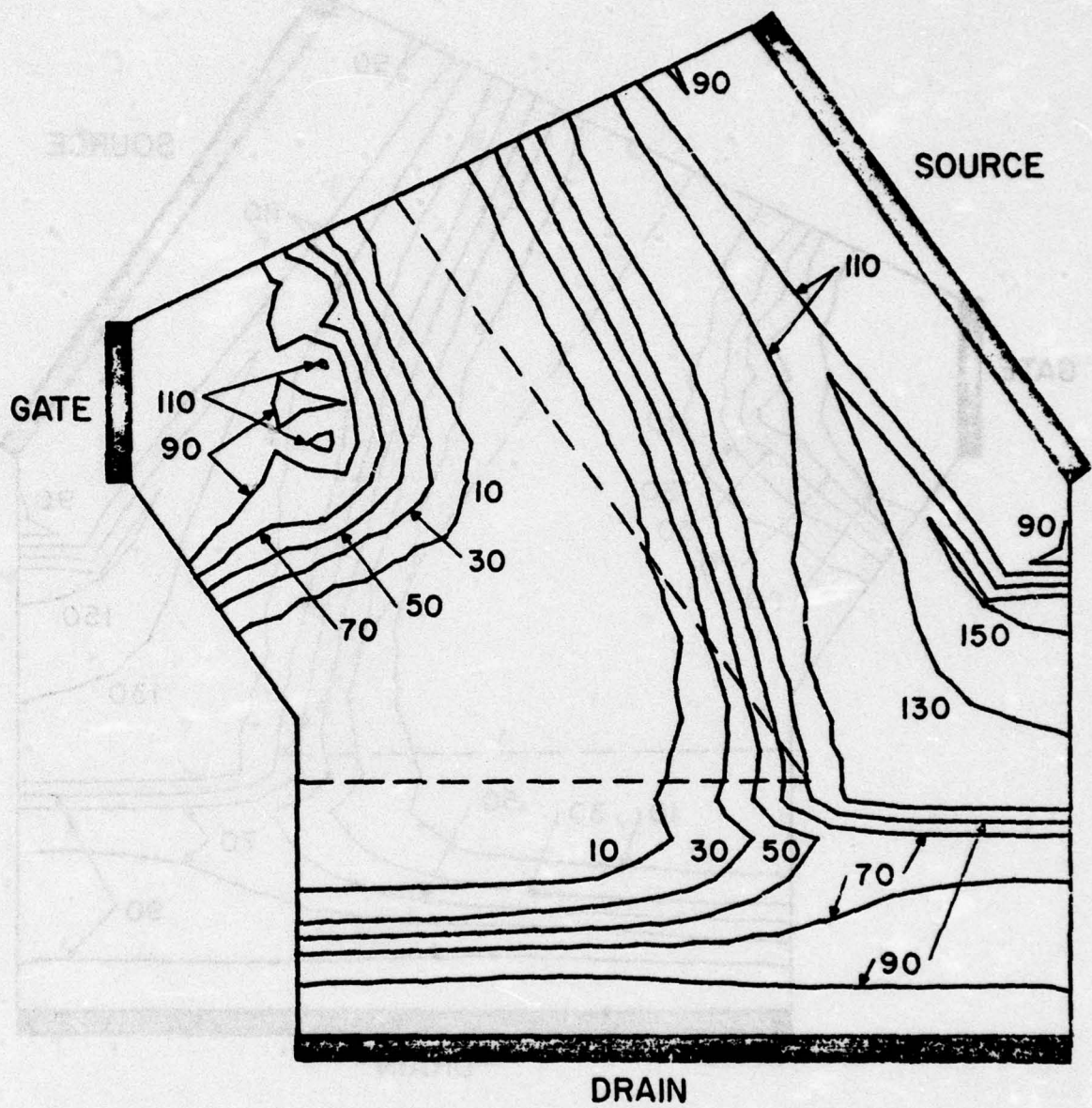


FIG. 3.14 CARRIER CONCENTRATION CONTOURS AS PERCENTAGE OF DOPING CONCENTRATION. ($V_G = 0$, $V_D = 2.0$ V)

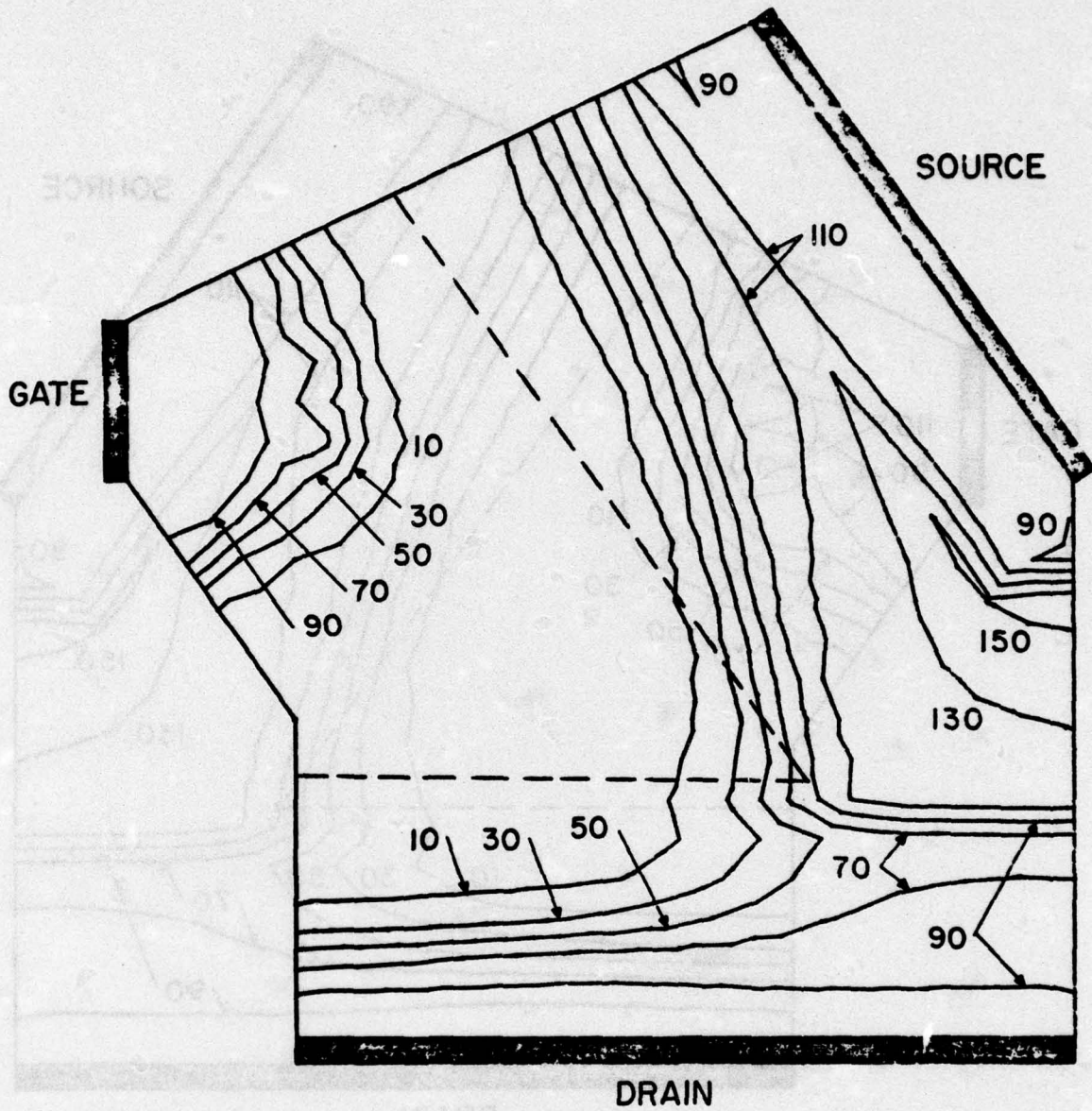


FIG. 3.15 CARRIER CONCENTRATION CONTOURS AS PERCENTAGE OF DOPING CONCENTRATION. ($V_G = -0.5$ V, $V_D = 2.0$ V)

device behavior with any degree of accuracy. The effect of accumulation in the channel on the drain current is twofold. First the higher concentration of electrons will increase the channel conductivity above the value assumed in Eq. 3.51, thus causing more current to flow for a given applied drain voltage. This is clearly evident from Fig. 3.11. In addition, the large concentration of electrons will oppose any tendency for the channel to become depleted with either increasing drain bias or (negative) gate bias. This will prevent the output current from becoming saturated at reasonable values of drain voltage. It will also keep the transconductance well below the values predicted by Eq. 3.51. Both of these effects are apparent from Figs. 3.11 and 3.12.

The origins of the accumulation regions in the channel can be traced to several sources. Under conditions of low drain bias (Fig. 3.13), the principal cause of accumulation in the channel is simply the proximity of the highly doped n^+ -regions representing the source and drain ohmic contacts at opposite ends of the channel (Fig. 3.10). The high concentration of electrons in these regions creates significant electron diffusion current into the channel at both the source and the drain. This causes slight accumulation regions to form as shown in Fig. 3.13. For larger values of drain voltage (Figs. 3.14 and 3.15) the electric field distributions in the channel can exacerbate the situation considerably.

Figures 3.16 and 3.17 are three-dimensional electric field profiles as a function of position in the JFET structure with no gate bias and $V_D = 0.5$ and 2.0 V, respectively. Figure 3.18 represents the electric field profile with $V_G = -0.5$ V and $V_D = 2.0$ V. It is clear that the

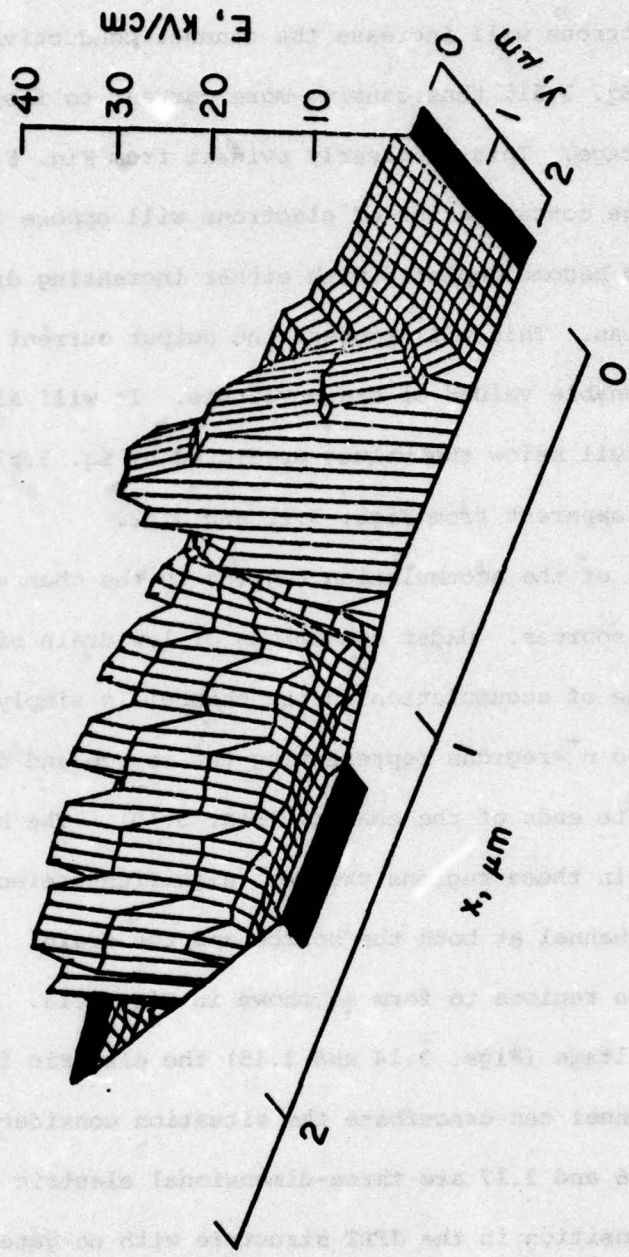


FIG. 3.16 ELECTRIC FIELD DISTRIBUTION FOR $V_D = 0.5$ V, $V_G = 0$.

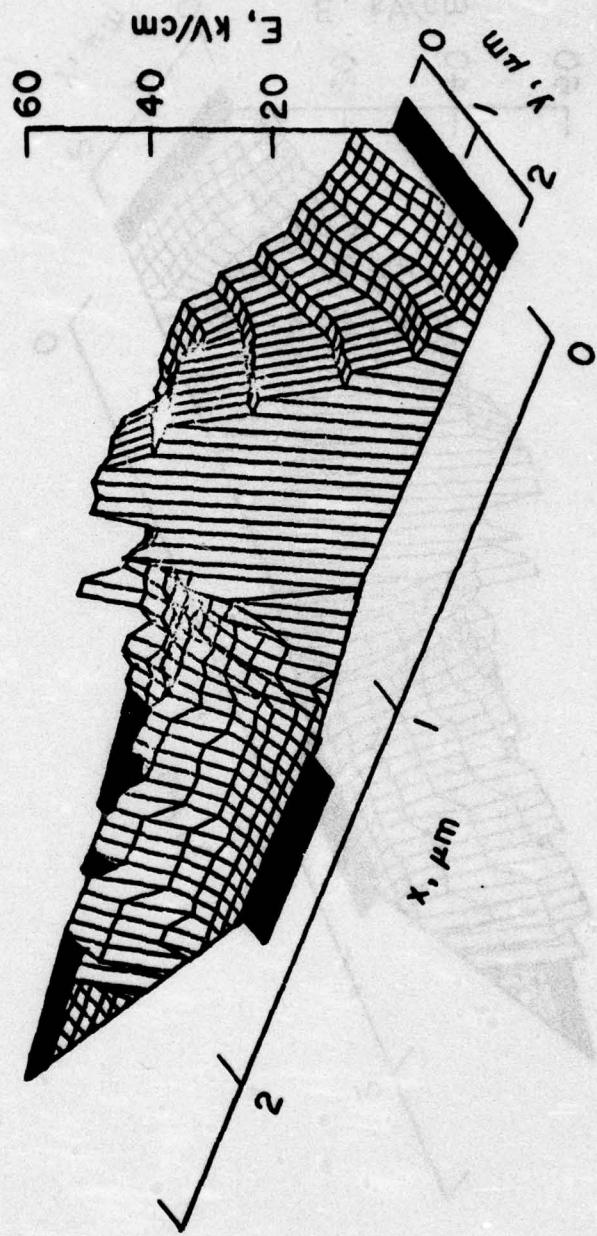


FIG. 3.17 ELECTRIC FIELD DISTRIBUTION FOR $V_D = 2.0 \text{ V}$, $V_G = 0$.

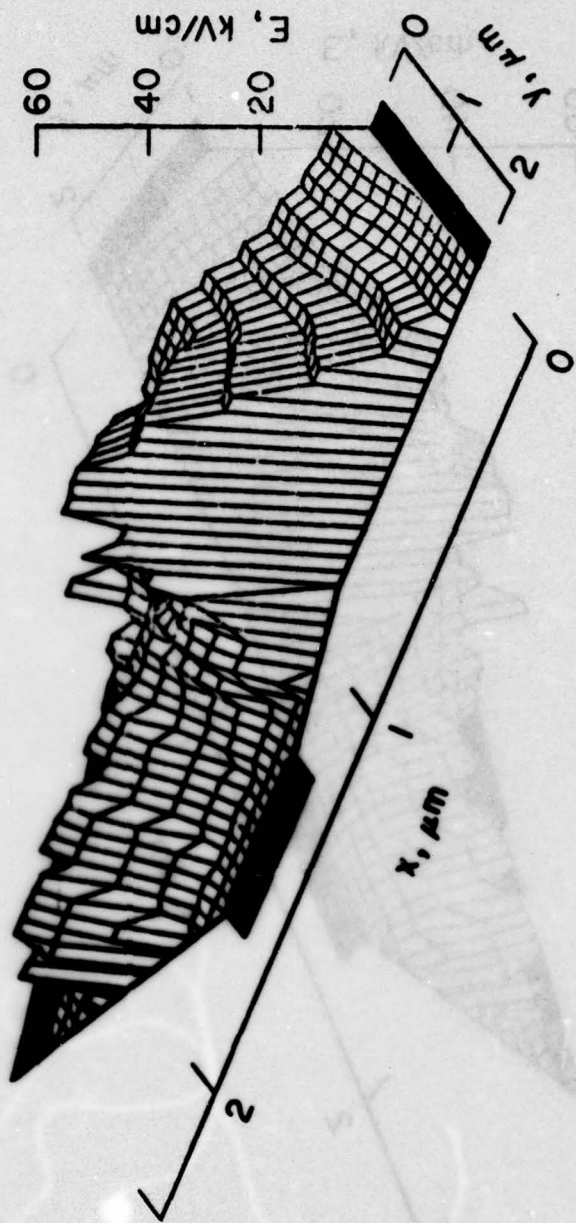


FIG. 3.18 ELECTRIC FIELD DISTRIBUTION FOR $V_D = 2.0$ V, $V_G = -0.5$ V.

magnitude of the electric field E is sufficiently large to cause the electrons to drift at their scattering-limited velocity. (This occurs for $E \geq 20$ kV/cm in Si.) This fact coupled with the narrowing of the channel from source to drain causes the electron concentration to build up near the center of the channel as indicated in Figs. 3.14 and 3.15.

The electric field attains a local maximum at the point of the V-shaped source contact (shown in Figs. 3.16 through 3.18) due to the very small radius of curvature there. This causes electrons which are injected into the channel at this point to reach their maximum velocity very rapidly and then to slow down as they pass out of this high-field region. An additional accumulation region is thus created near the source contact which can propagate into the channel as the electric field is increased.

All of the electric-field-related accumulation problems can be minimized by reducing the channel width a . This will allow the device to operate at lower bias voltages and thus decrease the average electric field in the channel. The accumulation effect will then be limited to diffusion from the ohmic contacts. This is not expected to significantly degrade the device performance.

The derivation of Eq. 3.15 (and thus of Eq. 3.51) was based on the assumption that pinchoff would occur at the drain end of the channel. Examination of Figs. 3.13 through 3.15 reveals that because of the two-dimensional nature of the electron distribution at the drain end of the channel where the p-type gate region contains a sharp corner, the channel attains its minimum width at a point nearer the source than expected. This affects not only the effective length of the channel,

but also the pinchoff voltage, since the depletion layer must be much wider in order to pinch off the channel anywhere other than the point of narrowest approach of the symmetric gate regions. This effect will also tend to increase the drain current above values predicted by Eq. 3.51 and must be included in any analysis of the operation of the vertical JFET.

3.7 Vertical JFET Fabrication Procedure.

3.7.1 Anisotropic Etching. The heart of the vertical JFET fabrication procedure is the anisotropic etching process. The etchant chosen for this part of the procedure is potassium hydroxide solution (1 gm KOH per ml water) heated to 80°C. It has been demonstrated¹⁴ that this etchant will etch exposed Si in the {100} directions at a rate of approximately 1 μm per min. In the {111} directions the etching rate is much slower and can effectively be considered negligible. Thus the KOH etchant will terminate its activity whenever the exposed Si region is bounded exclusively by <111> planes. In the particular case of a rectangular window of exposed <100> Si whose sides are parallel to {110} directions, the etchant will cut the V-groove pattern shown in cross section in Fig. 3.19. When this configuration is attained, the etch will terminate. The anisotropic etching process is used in this procedure both for isolation and for source definition. Because the depth of the groove is dependent only on the size of the window opening, the channel length of the JFET (defined as the distance from the bottom of the source groove to the n^+ -substrate) can be controlled to submicron dimensions simply by varying the width of the source window opening.

14. Stoller, A. I., "The Etching of Deep Vertical-Walled Patterns in Silicon," RCA Rev., vol. 31, No. 2, pp. 271-275, June 1970.

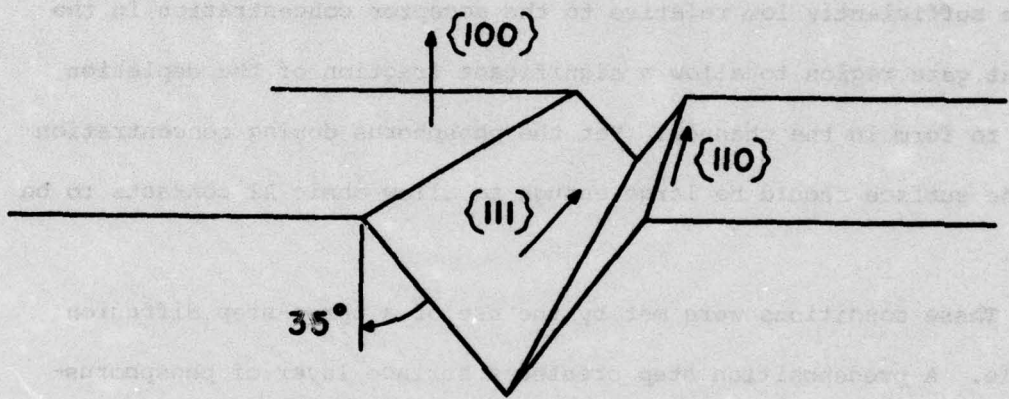


FIG. 3.19 ANISOTROPIC ETCH PATTERN IN $\langle 100 \rangle$ Si WHEN WINDOW OPENING IS PARALLEL TO $\{100\}$ DIRECTION.

3.7.2 Phosphorus Diffusion. Subsequent to the source definition etch, a phosphorus diffusion was done in order to create an n-type channel between the source groove and the n^+ -drain. The diffusion schedule was critical because of the following considerations.

1. The diffused pn junction must be deep enough to allow the channel to reach the n^+ -drain, yet it must not be so deep that the channel width at the drain end is greater than the channel length.

2. The donor density in the channel, particularly near the drain, must be sufficiently low relative to the acceptor concentration in the adjacent gate region to allow a significant fraction of the depletion region to form in the channel. Yet the phosphorus doping concentration near the surface should be large enough to allow ohmic Al contacts to be formed.

These conditions were met by the use of a three-step diffusion schedule. A predeposition step created a surface layer of phosphorus-doped Si with a low surface concentration. A long drive-in step then caused the phosphorus to diffuse into the Si until the desired junction depth was reached. Because the surface concentration of the resulting n-layer was much too low to make ohmic contact with Al, another phosphorus deposition step was carried out to create a thin surface layer of n^+ -Si. The final diffusion schedule was chosen to be:

1. Predeposition. A liquid-source phosphorus diffusion was done in N_2 ambient at $850^\circ C$ for 5 min.

2. Drive-in. The wafer was then baked in dry O_2 ambient at $1100^\circ C$ for 2 hours.

3. Ohmic contact deposition. Another liquid-source phosphorus diffusion was done in N_2 ambient at $1000^\circ C$ for 5 min.

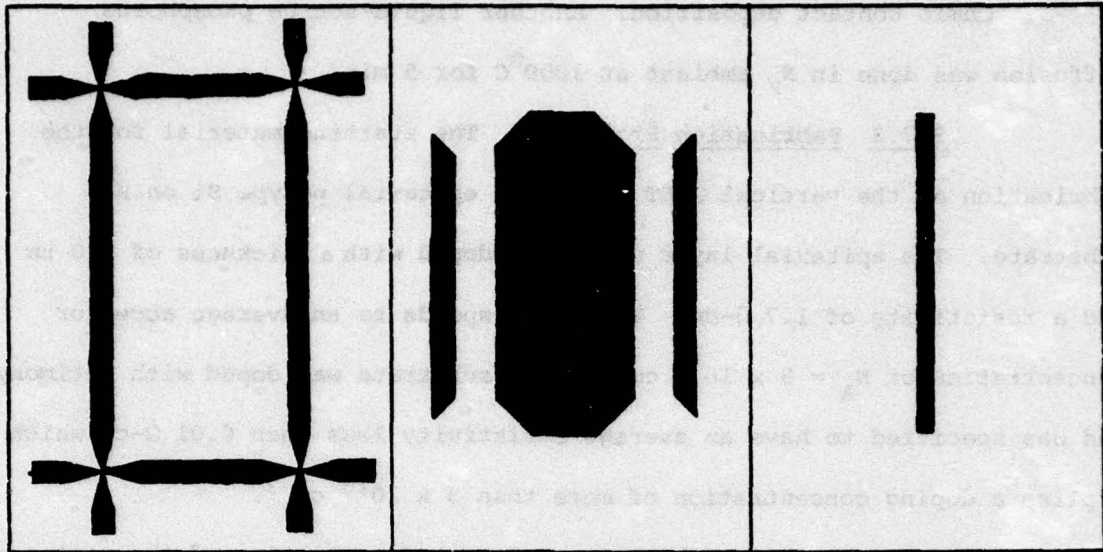
3.7.3 Fabrication Procedure. The starting material for the fabrication of the vertical JFET was $\langle 100 \rangle$ epitaxial p-type Si on n^+ -substrate. The epitaxial layer was boron-doped with a thickness of $5.0 \mu m$ and a resistivity of $1.7 \Omega\text{-cm}$. This corresponds to an average acceptor concentration of $N_A = 9 \times 10^{15} \text{ cm}^{-3}$. The substrate was doped with antimony and was specified to have an average resistivity less than $0.01 \Omega\text{-cm}$ which implies a doping concentration of more than $5 \times 10^{18} \text{ cm}^{-3}$.

A set of five photomasks were constructed consisting of the patterns shown in Fig. 3.20. Each pattern was repeated to make a series of five transistors with the linewidth of the source window openings varying from 4 to $6 \mu m$ in equal increments. This was done to allow the fabrication of source V-grooves varying in depth between 2.8 and $4.2 \mu m$ to compensate for any variation in epitaxial thickness. This five fold pattern was then step-and-repeated in both the x- and y-directions with center separation of 0.035 in to achieve the final array of patterns on each photomask.

The complete fabrication procedure was as follows:

1. Oxidation. The Si wafer was oxidized at $1050^\circ C$ for 5, 120 and 5 min in dry O_2 , steam and dry O_2 ambients, respectively, to yield an oxide thickness of $0.8 \mu m$. This oxide is used to mask the isolation etch.

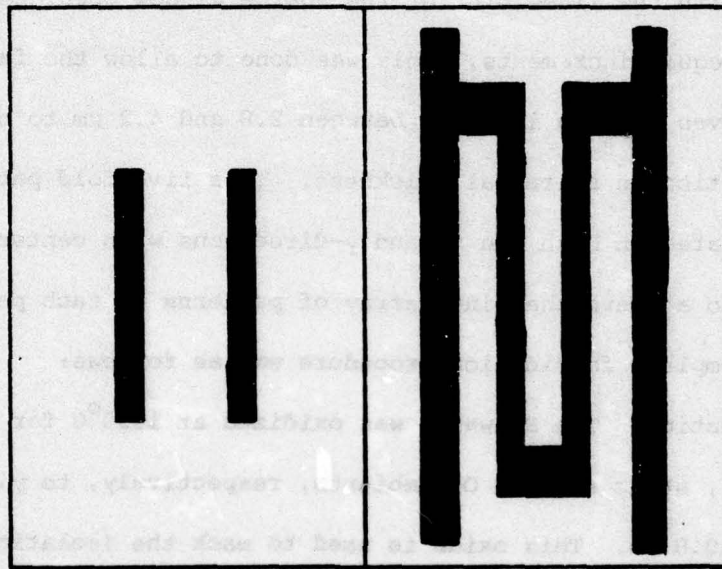
2. Photolithography. One part Kodak Thin Film Resist (KTFR) was mixed with one part KTFR Thinner and applied to the wafer which was then spun at 3000 rpm for 20 s. The photoresist was pre-baked at $60^\circ C$ for 15 min, exposed to ultraviolet light through photomask 1 for 4 s,



(a)

(b)

(c)



(d)

(e)

FIG. 3.20 PHOTOMASK PATTERNS FOR JFET FABRICATION WITH NEGATIVE PHOTORESIST.

(a) ISOLATION ETCH, (b) MESA WINDOWS, (c) SOURCE WINDOW, (d) GATE WINDOWS AND (e) METALLIZATION.

developed in KTRF Developer for 30 s, and post-baked at 120°C for 15 min.

3. Oxide etch. The oxide region exposed through the photoresist pattern was etched in buffered hydrofluoric acid (HF) for 7 min. The photoresist was then removed.

4. Isolation etch. The wafer was anisotropically etched in KOH solution at 80°C for 7 min. This causes the formation of isolated mesas of p-Si on a continuous substrate of n⁺-Si as shown in cross section in Fig. 3.21a. The oxide layer was then stripped.

5. Oxidation. A new oxide layer was grown according to the schedule in step 1.

6. Photolithography. Photomask 2 was used in the schedule described in step 2. This masking step is used to define an "active" window on the mesa surface while protecting the mesa edges from excessive loss during subsequent etching steps.

7. Oxide etch. The oxide layer was etched through the photoresist pattern and the photoresist was stripped as described in step 3.

8. Oxidation. Another oxide layer was grown according to the schedule in step 1.

9. Photolithography. One part KTRF was mixed with two parts KTRF Thinner and spun on the wafer at 4000 rpm for 20 s. The photoresist was pre-baked at 60°C for 15 min, exposed through photomask 3 for 4 s, developed in KTRF Developer for 30 s, and post-baked at 120°C for 15 min. This masking step opens the source windows.

10. Oxide etch. The oxide was etched and the photoresist was stripped as in step 3.

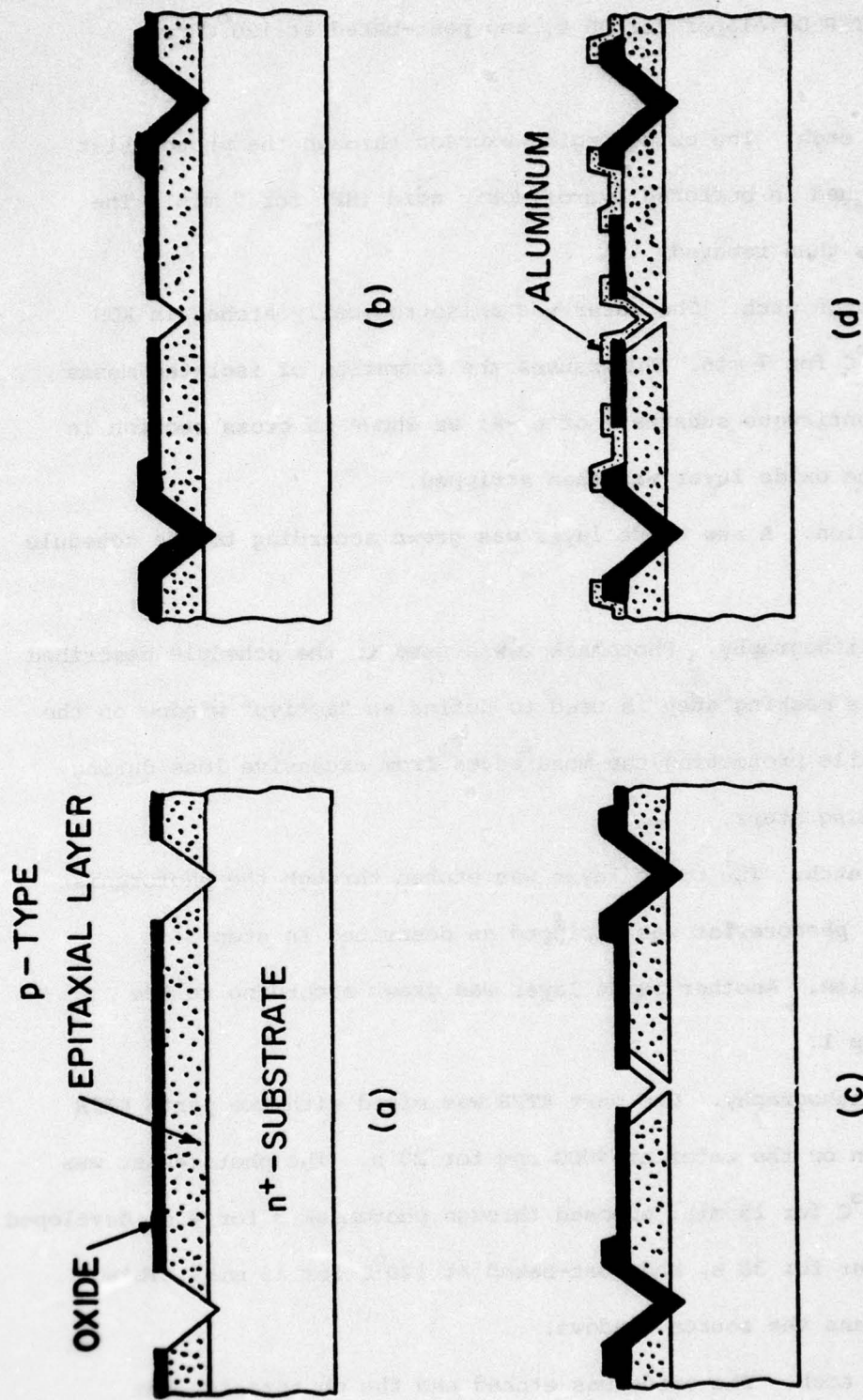


FIG. 3.21 SCHEMATIC CROSS SECTION OF VERTICAL JFET (a) AFTER ISOLATION ETCH, (b) AFTER SOURCE ETCH, (c) AFTER SOURCE DIFFUSION AND (d) AFTER METALLIZATION.

11. Source etch. The wafer was anisotropically etched in KOH solution at 80°C for 5 min. This creates the V-groove which will ultimately be the source terminal of the JFET (Fig. 3.21b).

12. Phosphorus diffusion. The phosphorus diffusion was carried out as described in Section 3.7.2. The diffusion is used to create the n-type channel of the FET as shown in cross section in Fig. 3.21c.

13. Photolithography. Photomask 4 was used in the schedule described in step 2. This is the masking step for the gate window formation.

14. Oxide etch. The oxide was etched and the photoresist was stripped as in step 3.

15. Metallization. Aluminum was evaporated over the entire wafer to a thickness of 0.4 μm .

16. Photolithography. Photomask 5 was used in the same schedule as in step 2.

17. Metal etch. The Al was etched through the photoresist pattern in one part H_3PO_4 : one part $\text{HC}_2\text{H}_3\text{O}_2$ at 60°C until the metal pattern was completely developed (Fig. 3.21d). The photoresist was then stripped.

18. Sintering. In some cases, it was necessary to sinter the JFETs in order to reduce the contact resistance between the Al and the Si. This was done in N_2 ambient at 525°C for 15 min.

3.8 Device Evaluation.

3.8.1 Physical Dimensions. A photomicrograph of five completed JFETs is shown in Fig. 3.22. The dimensions of each mesa surface were measured as 266 x 83 μm . Each source line was measured as 234 μm in length.

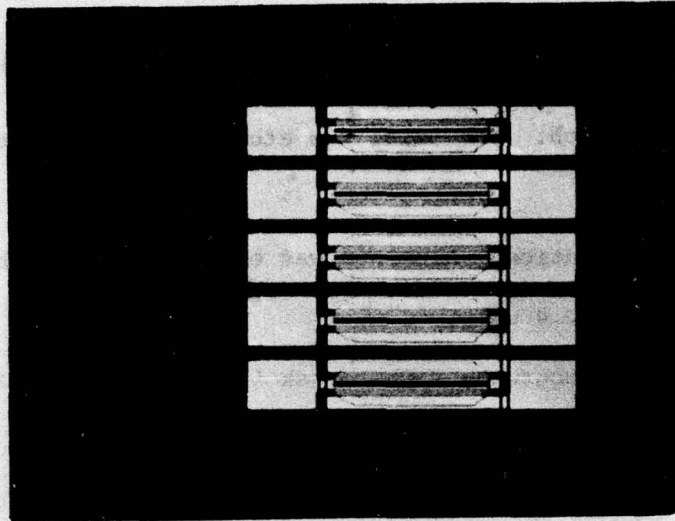


FIG. 3.22 TOP VIEW OF FIVE COMPLETED VERTICAL JFETS. SOURCE GROOVES VARY IN WIDTH FROM 4 μm FOR TOP TRANSISTOR TO 6 μm FOR BOTTOM TRANSISTOR.

An angle-lapped-and-stained cross section of four of the five devices is shown in Fig. 3.23. The depths of the etched source grooves were measured to be 4.1, 3.7, 3.4 and 2.8 μm from left to right in Fig. 3.23. (Note that the deepest groove has not etched to completion.) The width of the source windows which produced these grooves can be found by simply multiplying the groove depth by $\sqrt{2}$. For the above values, the source window openings are calculated as 5.8, 5.2, 4.8, and 4.0 μm , respectively. These values compare favorably with the measured mask window dimensions of 5.5, 5.0, 4.5 and 4.0 μm , thus indicating that the proposed structure can be fabricated with some degree of dimensional control and reproducibility. The channel lengths of the four devices (defined as the epitaxial thickness less the groove depth, assuming the subsequent diffusion reaches the substrate) were measured from Fig. 3.23 to be 0, 0.3, 0.6 and 1.2 μm , respectively. It should be pointed out here that the epitaxial thickness has been reduced from its original value of 5.0 μm to a value of 4.0 μm measured after completion of the devices. The loss is due to interdiffusion of boron and antimony dopant atoms at the pn^+ interface as well as to the loss of Si during oxidation steps.

3.8.2 Doping Profile. The doping profiles of the completed JFETs were inferred from measurements of sheet resistance and junction depths after each step of the diffusion schedule. Surface concentrations were estimated from the curves of Irvin¹⁵ and the final doping profiles were plotted assuming a complementary-error-function distribution after

15. Irvin, J. C., "Resistivity of Bulk Silicon and of Diffused Layers in Silicon," Bell System Tech. J., vol. 41, No. 2, pp. 387-410, March 1962.

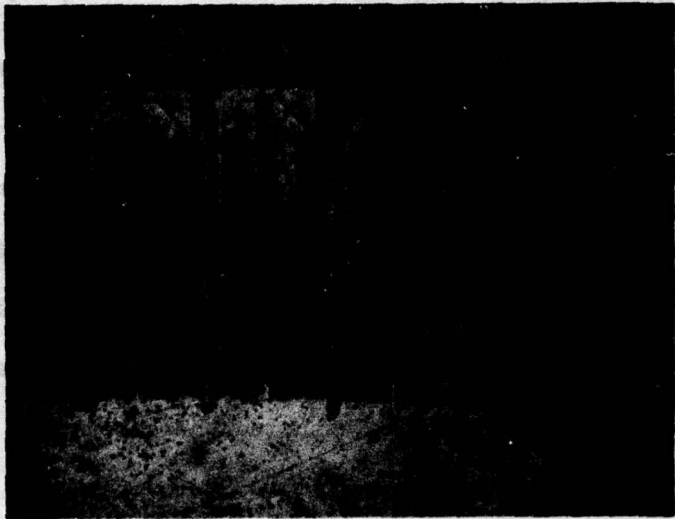


FIG. 3.23 CROSS SECTION OF FOUR TRANSISTORS AFTER ANGLE LAP AND STAIN.

SOURCE GROOVES VARY IN WIDTH FROM 5.5 μm FOR LEFT MOST

TRANSISTOR to 4 μm FOR RIGHT MOST TRANSISTOR.

each predeposition step and a Gaussian distribution after the drive-in step. The final doping profiles are shown in Fig. 3.24 for the phosphorus diffusion schedule described in Section 3.7.2 and in Fig. 3.25 for a similar schedule except that the predeposition was done at 900°C and the drive-in was done for 30 min. Figure 3.25 is included here to show that this diffusion schedule resulted in much too high a doping level in the channel compared with the p-type background concentration. The result of switching to the final diffusion schedule was to reduce the surface concentration from 1.2×10^{18} to $3 \times 10^{17} \text{ cm}^{-3}$ and to increase the junction depth from 0.4 to 0.65 μm .

The total phosphorus dose Q introduced into the wafer during the critical predeposition step can be calculated from the doping distribution after the drive-in as

$$Q = N_s \sqrt{\pi D_2 t_2} \quad , \quad (3.52)$$

where N_s is the surface concentration of phosphorus atoms after the drive-in step, D_2 is the phosphorus diffusion coefficient associated with the drive-in step, and t_2 is the total drive-in time. For the schedule of Fig. 3.24, Q is calculated as $9 \times 10^{12} \text{ cm}^{-2}$ and for Fig. 3.25 as $1.9 \times 10^{13} \text{ cm}^{-2}$.

A theoretical maximum Q can also be calculated¹⁶ assuming that the predeposition step results in a complementary-error-function distribution and a surface concentration equal to the solid-solubility

16. Warner, R. M. and Fordemwalt, J. N., eds., Integrated Circuits--Design Principles and Fabrication, McGraw-Hill Book Co., Inc., New York, 1965.

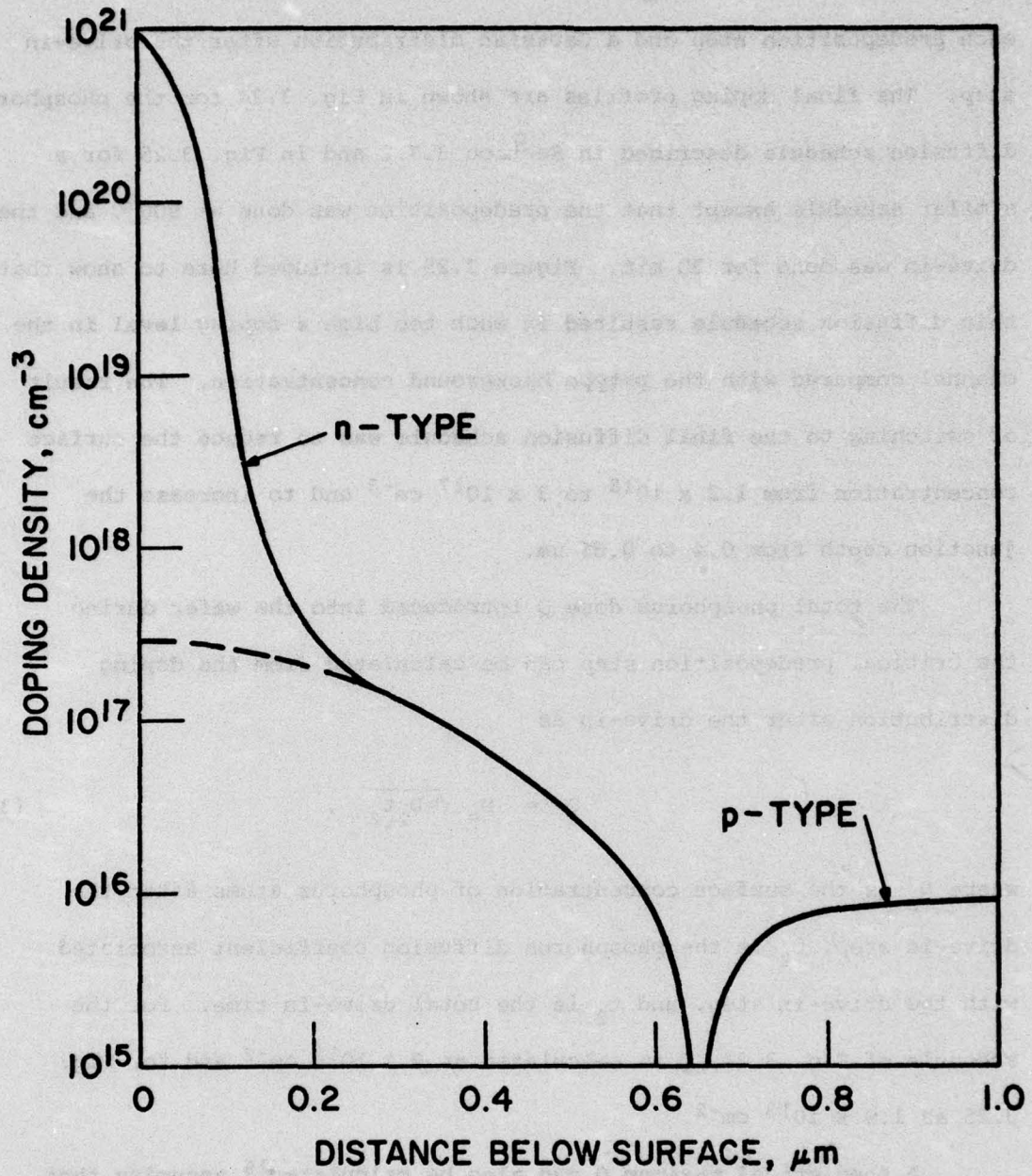


FIG. 3.24 DOPING PROFILE IN CHANNEL OF VERTICAL JFET. SEE TEXT FOR DIFFUSION SCHEDULE.

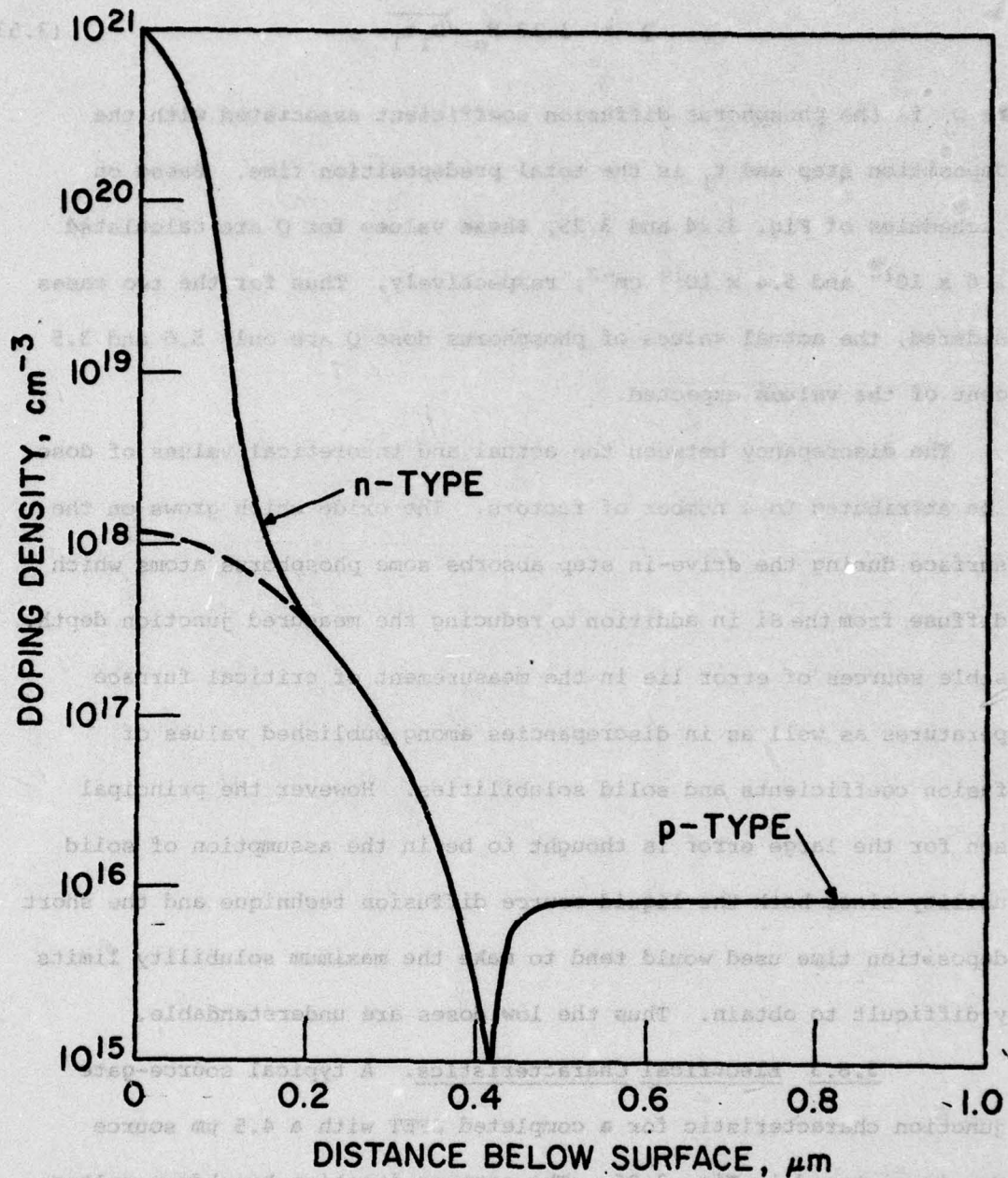


FIG. 3.25 DOPING PROFILE IN CHANNEL OF VERTICAL JFET. SEE TEXT FOR DIFFUSION SCHEDULE.

limit N for phosphorus in Si. This theoretical value is given by

$$Q = 1.13 N_0 \sqrt{D_1 t_1} , \quad (3.53)$$

where D_1 is the phosphorus diffusion coefficient associated with the predeposition step and t_1 is the total predeposition time. Based on the schedules of Fig. 3.24 and 3.25, these values for Q are calculated as 1.6×10^{14} and $5.4 \times 10^{14} \text{ cm}^{-2}$, respectively. Thus for the two cases considered, the actual values of phosphorus dose Q are only 5.6 and 3.5 percent of the values expected.

The discrepancy between the actual and theoretical values of dose can be attributed to a number of factors. The oxide which grows on the Si surface during the drive-in step absorbs some phosphorus atoms which outdiffuse from the Si in addition to reducing the measured junction depth. Possible sources of error lie in the measurement of critical furnace temperatures as well as in discrepancies among published values of diffusion coefficients and solid solubilities. However the principal reason for the large error is thought to be in the assumption of solid solubility since both the liquid-source diffusion technique and the short predeposition time used would tend to make the maximum solubility limits very difficult to obtain. Thus the low doses are understandable.

3.8.3 Electrical Characteristics. A typical source-gate pn junction characteristic for a completed JFET with a $4.5 \mu\text{m}$ source window is pictured in Fig. 3.26. The reverse junction breakdown voltage V_B is seen to be approximately 60 V with less than $5 \mu\text{A}$ of leakage current up to V_B . (This corresponds to a current density of less than

... that the... junction is a one-sided step junction...
... the measured voltage determined by the...
... is expected to be between 0.5 V... the agreement is considered

The output characteristics for I_D vs. V_{GS} for $V_{DS} = 0.5$ V are shown in Fig. 3.26. The device displays a linear relationship between I_D and V_{GS} in the region of operation shown. The channel length L is the channel length $L = 0.5$ cm and the channel width W is $W = 0.5$ cm. The channel length L is the channel length $L = 0.5$ cm and the channel width W is $W = 0.5$ cm.

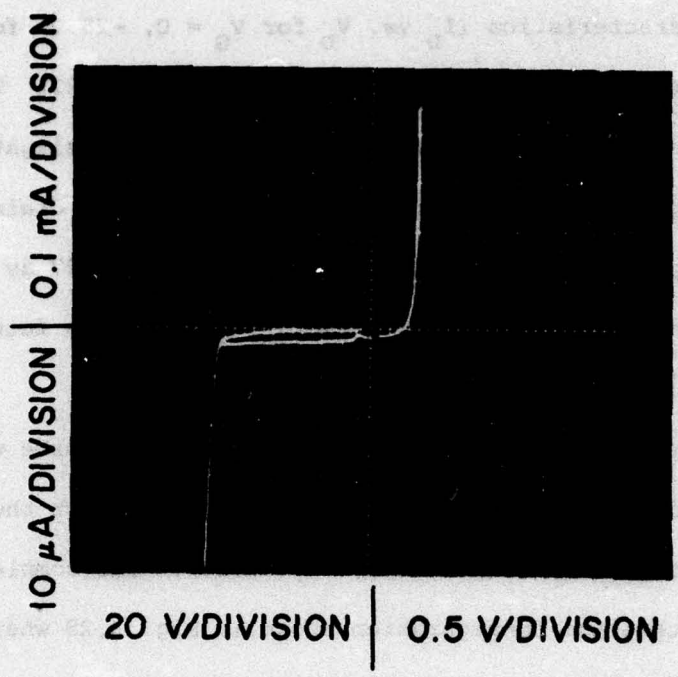


FIG. 3.26 SOURCE-GATE JUNCTION CHARACTERISTICS OF TYPICAL JFET.

0.47 A/cm².) Assuming that the junction is a one-sided step junction with the breakdown voltage determined by the lightly-doped p-side, V_B is expected¹⁷ to be between 60 and 65 V, so the agreement is considered good.

The output characteristics (I_D vs. V_D for $V_G = 0, -25$ V) for a typical JFET with a 4.5 μm source window is shown in Fig. 3.27. The device displays a tendency toward current saturation with a slight decrease in current as a large gate voltage is applied. The drain conductance in the linear region g_{do} is measured from Fig. 3.27 as $4.0 \times 10^{-3} \Omega^{-1}$. Transconductance at $V_D = 3$ V and $V_G = -12.5$ V is found to be $1.5 \times 10^{-4} \Omega^{-1}$.

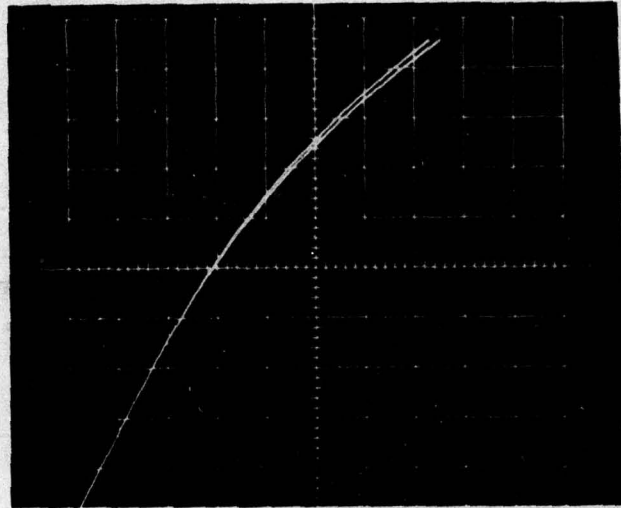
The channel length of a typical JFET with a 4.5 μm source window was found from Fig. 3.23 to be 0.6 μm . The junction depth for the subsequent diffusion was measured as 0.65 μm (Fig. 3.24). The completed JFET will therefore take the configuration shown in Fig. 3.28 where D is the diffusion depth (0.65 μm), L is the channel length (0.6 μm), and the channel half-width a can be found from the relation

$$a = \frac{D - L \sin 35.26^\circ}{\cos 35.26^\circ} = 0.37 \mu\text{m} \quad (3.54)$$

The drain conductance g_{do} can therefore be estimated as the conductance of a trapezoid of height L and base $2a$ (dashed line in Fig. 3.28) whose

17. Sze, S. M. and Gibbons, G., "Avalanche Breakdown Voltages of Abrupt and Linearly Graded p-n Junction in Ge, Si, GaAs, and GaP," Appl. Phys. Letters, vol. 8, No. 5, pp. 111-113, March 1966.

I_D , 20 mA/DIVISION



V_D , 0.5 V/DIVISION

FIG. 3.27 OUTPUT CHARACTERISTICS OF TYPICAL JFET. (V_G IS STEPPED IN 25 V INCREMENT.)

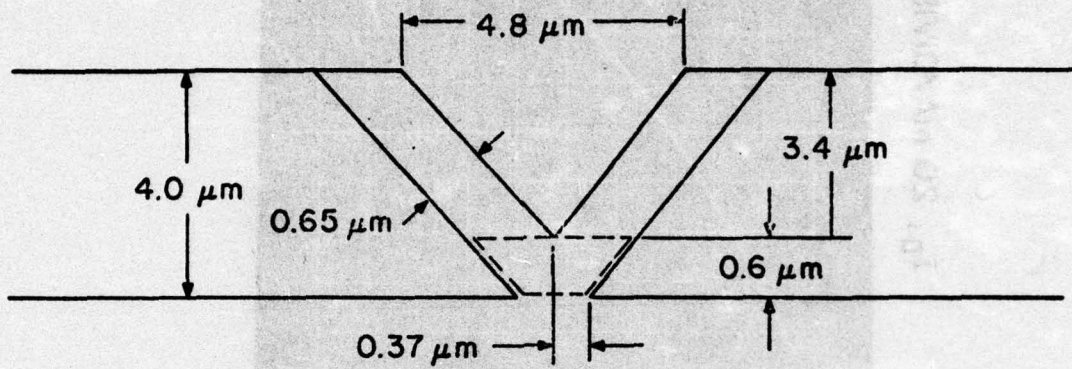


FIG. 3.28 SCHEMATIC CROSS SECTION OF COMPLETED 4.5 μm-SOURCE JFET SHOWING MEASURED DIMENSIONS.

doping can be approximated from Fig. 3.24 as

$$N_D = N_s \left(L - \frac{x}{D} \right), \quad (3.55)$$

where x is the vertical distance from the source. A value of $g_{do} = 0.42 \Omega^{-1}$ is obtained from this analysis for a structure with dimensions as given above. The large discrepancy between this value and the measured drain conductance can be attributed to the critical dependence of these calculations on the channel length L and the junction depth D which can be measured only by very inexact methods. In addition Eq. 3.54 does not take into account the curvature of the diffused junction near the drain end of the channel. This effect can reduce a considerably, especially when $D \approx L$.

As predicted by the finite-element numerical analysis of the vertical structure, the transconductance g_m is considerably smaller than the drain conductance g_{do} . It is not clear however to what extent this is due to the formation of an accumulation region in the channel or to the excessively high doping level in the channel in comparison with the background doping concentration (see Fig. 3.24), since both effects act to reduce the ratio of g_m/g_{do} .

3.9 Summary and Conclusions. A vertical junction field-effect transistor structure has been proposed which allows fabrication of a submicron gate length using conventional photolithographic techniques. The fabrication sequence for epitaxial $pn^+ <100> Si$ consisted of an anisotropic etch to define the source followed by a self-aligned phosphorus diffusion to create a conducting channel. Gate windows were then opened

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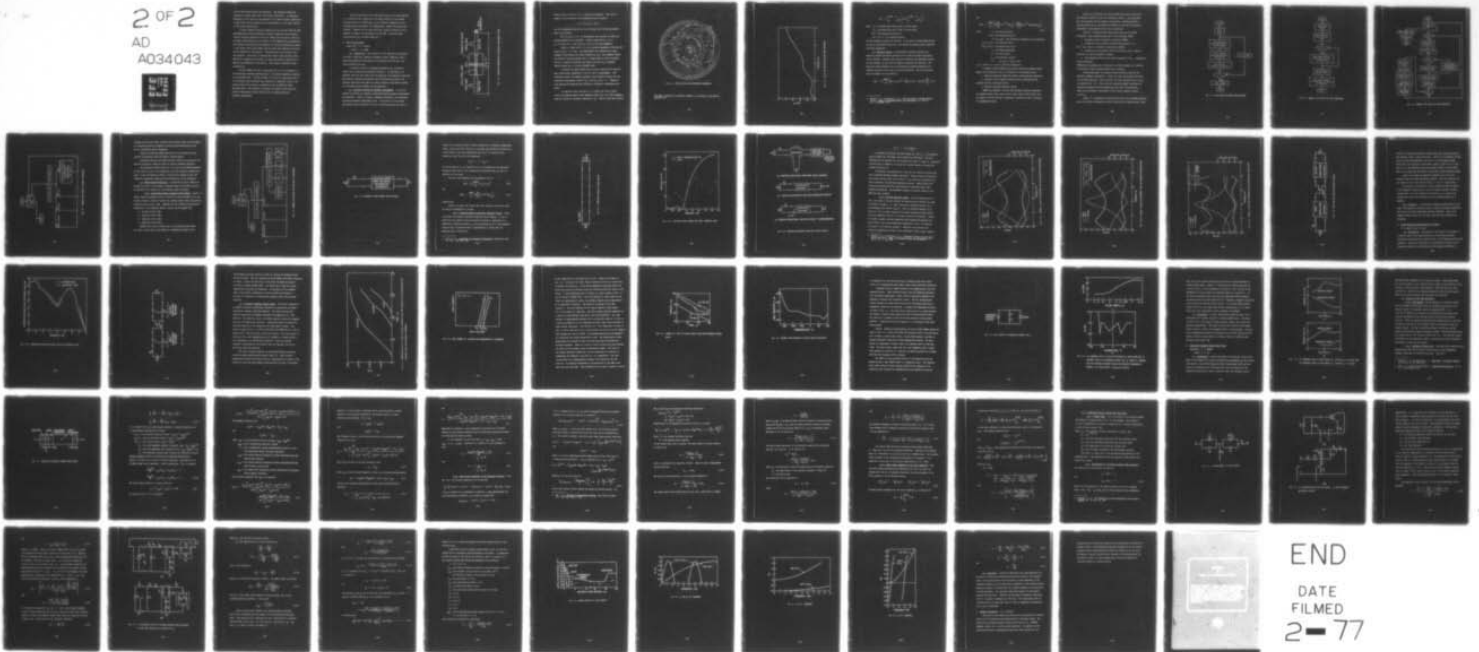
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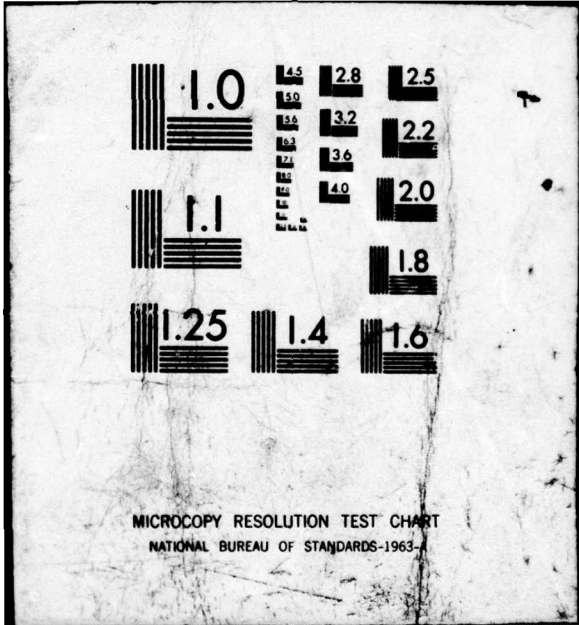
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and the final metal pattern was deposited. The completed JFETs were expected to exhibit power gain at microwave frequencies. An additional advantage of this structure was expected to be reduced channel temperature at high drain current densities due to the proximity of the source contact to the active device region.

A finite-element numerical simulation of the vertical JFET has been performed which solves consecutively Poisson's equation and the majority carrier continuity equation in both the channel and the gate to find the dc output characteristics of the device in the common-source configuration. This analysis has predicted the formation of electron accumulation regions in the channel which cause higher current levels than expected and hinder carrier depletion in the channel. Transconductance was therefore less than expected. The effect of reducing the channel width-to-length ratio should be to suppress the formation of these accumulation regions and to improve the performance of the device. This change is presently under consideration.

Vertical JFETs were made in epitaxial pn^+ <100> Si according to the fabrication schedule described above. The devices generally exhibited low transconductance. This was thought to be due to a high doping level in the channel which prevented the formation of a depletion layer on the channel side of the junction in addition to the accumulation effect described above. The inability to measure the channel width except by indirect means makes accurate analysis of the completed devices extremely complicated.

The full potential of this JFET design has not yet been explored. It is expected that a reduction of the donor density in the channel, obtained either by a modification of the diffusion schedule or by an ion-implantation technique, will considerably improve the device performance. Reversal of the source and drain contact locations is also expected to improve the performance of the JFET. These and other investigations are currently under way.

4. FET Circuit Studies

Supervisor: N. A. Masnari

Staff: G. Z. Qadah

4.1 Introduction. The objective of this phase of the program is to design a high-gain, wideband, microwave (X-band) amplifier using a GaAs Schottky-barrier FET together with properly selected input and output matching circuits.

In previous reports, the general procedures to be followed to achieve such a design were discussed in detail. In this report the progress since the last report will be presented, the completely developed multifunction optimization program will be discussed and some of the problems associated with amplifier design together with possible methods for overcoming these problems will be presented.

4.2 Transistor Scattering Parameter Measurements. In previous reports one method for transistor scattering matrix parameter measurements was described. Figure 4.1 shows a simplified diagram for the transistor scattering parameter measurement setup. The purpose of the proposed measurement method discussed in detail in previous reports was first to

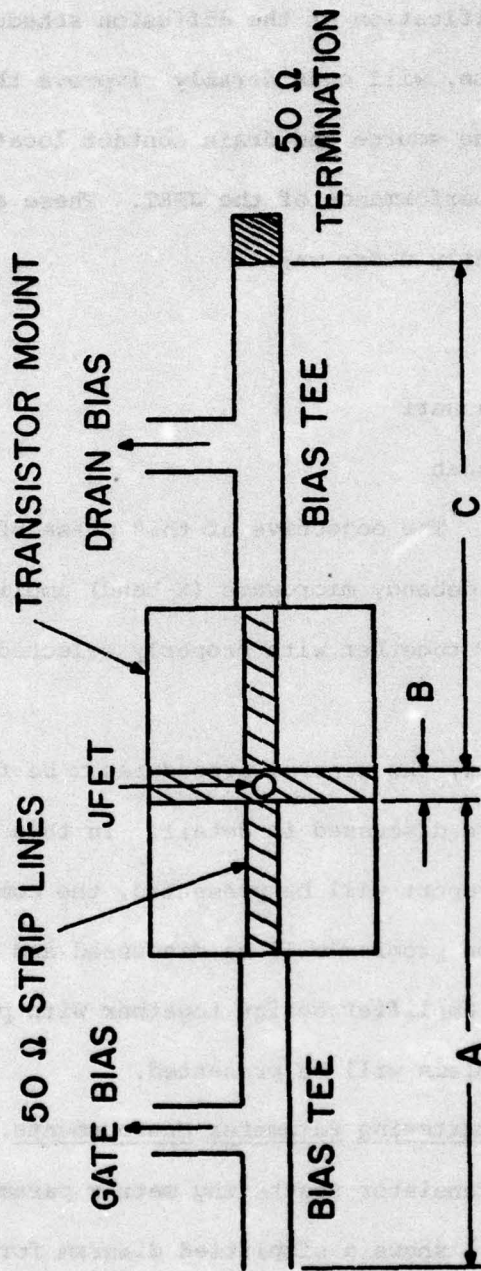


FIG. 4.1 SIMPLIFIED TRANSISTOR S-PARAMETER MEASUREMENT SETUP.

measure the A, C and (A + B + C) scattering parameters. Then using a computer routine based on the transmission matrix equation

$$B = A^{-1}(A + B + C)C^{-1} ,$$

the FET transmission matrix (B) can be obtained and the FET S-parameter matrix can be found.

[A], [C] and [A + B + C] measurements were carried out using the network analyser for an FMx-5073 n-channel JFET with $V_D = 2.8$ V, $I_D = 18.4$ mA, $V_G = -1.25$ V and $R_L = 270 \Omega$ as the load impedance.

Figure 4.2 shows the [A + B + C] scattering parameters over the frequency band of 2 to 4 GHz. The measurements were restricted to this frequency band because for higher frequencies $|S_{12}|$ (the feedback factor) was found to increase rapidly until it became equal to unity at X-band. Figure 4.3 clearly illustrates the manner in which $|S_{12}|$ increases rapidly within the 4 to 8 GHz frequency band.

In general the above method gave incorrect results due to measurement inaccuracies, especially in the [A] and [C] measurements. This inaccuracy caused the computer program to give incorrect results for the transistor S-parameters (such as $|S_{11}|$ and $|S_{12}|$ both > 1). Therefore this approach was modified and subjected to extensive investigation and study.

One approach being considered is to neglect the loss in parts A and C and replace them at each frequency within the 2 to 4 GHz frequency band by a length of lossless transmission line. Then by using the relation

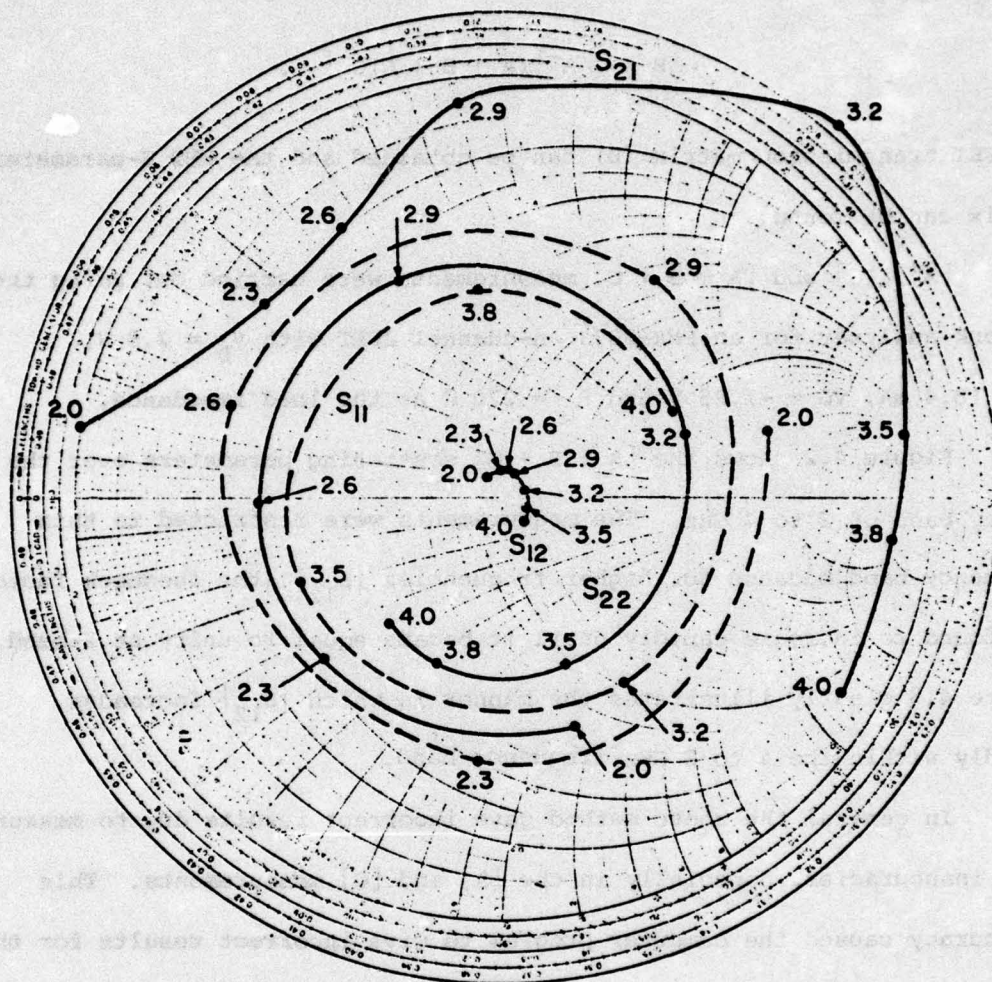


FIG. 4.2 JFET AND BIAS TEE SCATTERING PARAMETERS.

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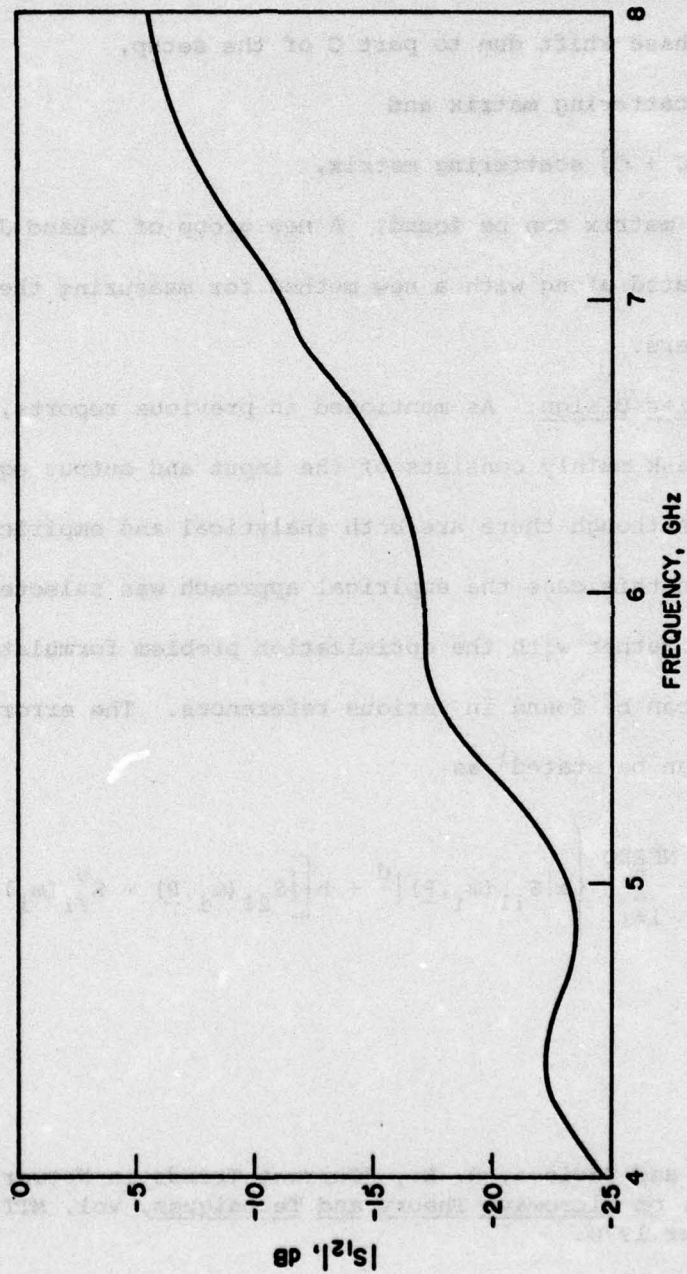


FIG. 4.3 $|S_{12}|$ FOR THE FET AND BIAS TEE STRUCTURE.

$$[S]^T = \begin{bmatrix} e^{-j\theta_1} & 0 \\ 0 & e^{-j\theta_2} \end{bmatrix} [S] \begin{bmatrix} e^{-j\theta_1} & 0 \\ 0 & e^{-j\theta_2} \end{bmatrix},$$

where θ_1 = the phase shift due to part A of the setup,

θ_2 = the phase shift due to part C of the setup,

$[S]^T$ = FET scattering matrix and

$[S]$ = $[A + B + C]$ scattering matrix,

the FET scattering matrix can be found. A new group of X-band JFET devices are being investigated along with a new method for measuring the transistor $[S]$ -matrix parameters.

4.3 Amplifier Design. As mentioned in previous reports, the amplifier design task mainly consists of the input and output equalizing circuit designs. Although there are both analytical and empirical methods for such designs in this case the empirical approach was selected. The empirical method together with the optimization problem formulation for computer solution can be found in various references. The error function and its gradient can be stated¹ as

$$E(\underline{P}) = \frac{1}{d} \sum_{i=1}^{NFREQ} \left\{ a |S_{11}(\omega_i, \underline{P})|^d + b \left[|S_{21}(\omega_i, \underline{P}) - S_{21}^v(\omega_i)|^d \right] \right\} \quad (4.1)$$

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1. Bandler, J. W. and Seviova, R. E., "Current Trends in Network Optimization," Trans. on Microwave Theory and Techniques, vol. MTT-18, No. 12, December 1970.

and

$$\nabla E(\underline{P}) = \sum_{i=1}^{NFREQ} \left\{ \operatorname{Re} \left[\frac{2R_g}{V_{g_i}} |\Gamma_i|^{d-2} \Gamma_i^* \nabla I_{g_i} \right] + \frac{8R_L R_g}{|V_{g_i}|^2} |T_i|^{d-2} T_i \operatorname{Re}(I_{L_i}^* \nabla I_{L_i}) \right\}, \quad (4.2)$$

where

E = the error function,

a, b, d = the weighting factors,

$\Gamma = S_{11}(\omega_i, \underline{P})$ = the reflection coefficient at the input port,

$|S_{21}(\omega_i, \underline{P})|^2$ = the transducer gain,

$|S_{21}^v(\omega_i, \underline{P})|^2$ = the desired flat gain,

\underline{P} = the design parameters,

I_L = the load current,

I_g = the generator current,

$T = S_{21}(\omega_i, \underline{P}) - S_{21}^v(\omega_i)$ and

$\omega_i \in \Omega$, where Ω is a set of specified frequencies.

A computer program FETCAD (field effect transistor computer aided design) was developed to aid in the design of the following cases:

1. Negative resistance amplifier design (reflection-type amplifier).
2. Microwave filter design (low-pass filter, band-pass filter, high-pass filter, band-stop filter).
3. Two-port microwave amplifier design.

FETCAD can optimize a circuit with arbitrary topology consisting of lossless series lines, open circuit stubs, short circuit stubs, and any number of active devices (transistors) specified by their scattering or transmission matrix.

Figure 4.4 illustrates the general FETCAD flow chart, which uses the subroutine INPUT for data and information readin, subroutine EVAL for error function and its gradient calculations, subroutine MIN for function minimization, and subroutine OUTPUT for printing the parameter optimization and parameter sensitivity calculations.

Figure 4.5 illustrates the general flow chart for the INPUT subroutine. This subroutine makes use of the following inputs:

1. Microwave circuit topological structure (INTEG1).
2. Information about parameter gradient calculations (i.e., $\partial/\partial l$, ∂/Z_0 , both or no gradient calculations) (INTEG2).
3. Information about program function selection (filter, negative resistance or two port amplifier design).
4. Load impedance and/or active device parameters ([S] or transmission matrix parameters).

FETCAD can be optimized for a load which is either constant or a function of frequency as well as being either real or complex.

As mentioned above, the adjoint network method is used for the parameter gradient calculations. Figure 4.6 shows the general flow chart for the EVAL subroutine which evaluates the error function (Eq. 4.1) and its gradient (Eq. 4.2). EVAL calls for subroutine ANALS to perform the original and adjoint network analysis and also calls for subroutine GRADC for the gradient calculations of the circuit terminal currents I_L and I_g .

Figure 4.7 illustrates the general flow chart for the ANALS subroutine which can analyze any amplifier circuit consisting of lossless series lines,

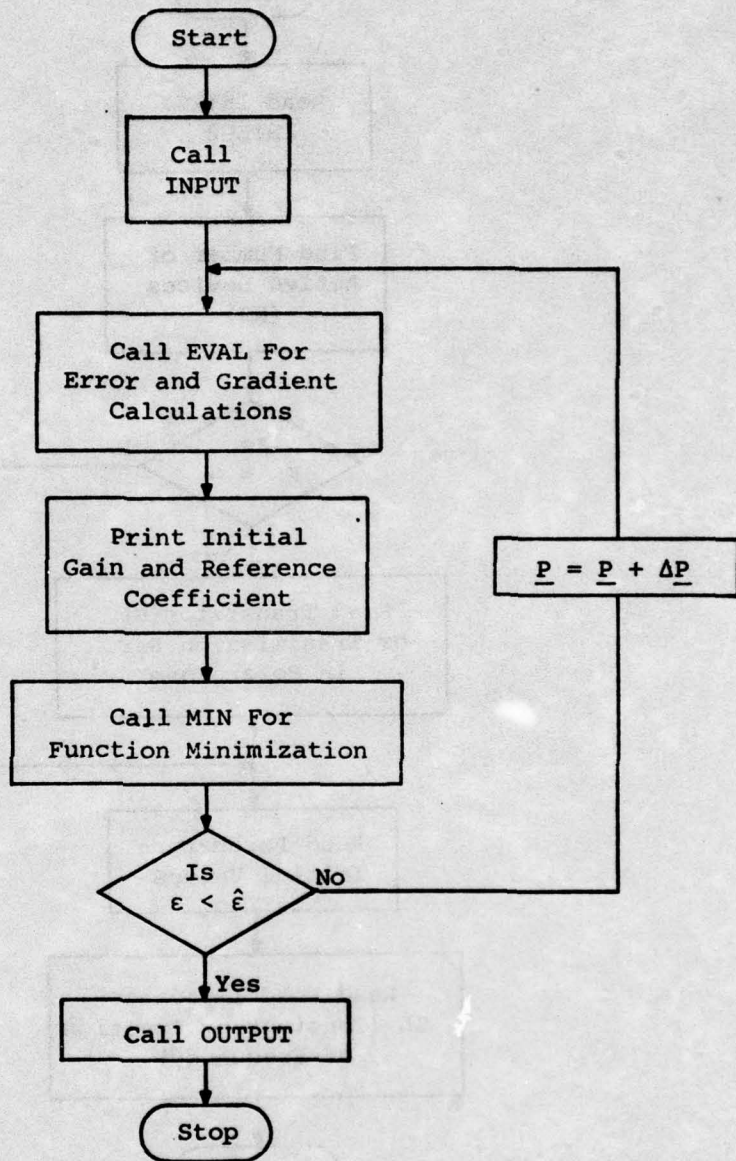


FIG. 4.4 FLOW CHART FOR FETCAD MAIN PROGRAM.

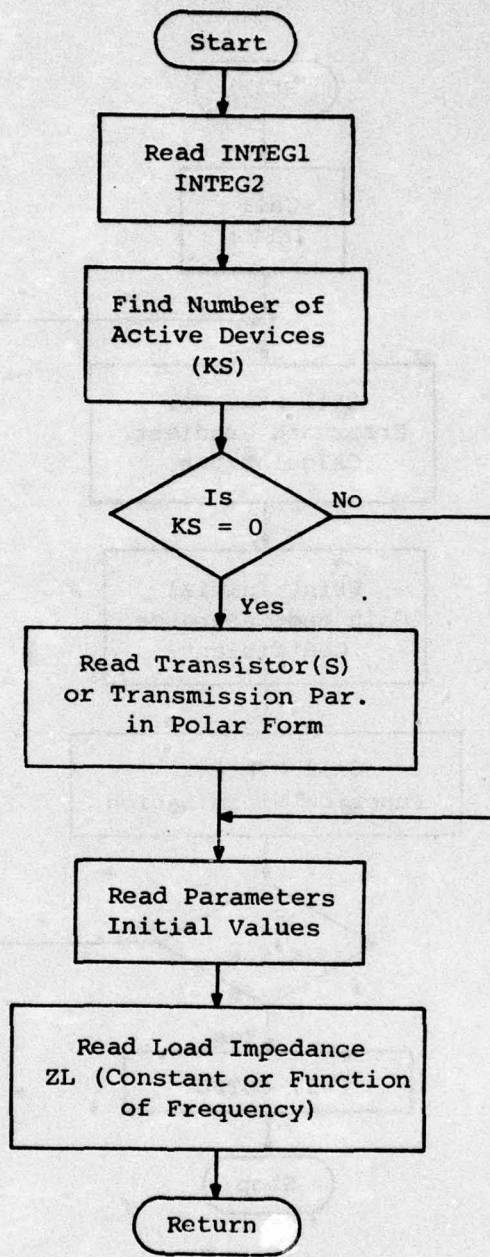


FIG. 4.5 GENERAL FLOW CHART FOR INPUT SUBROUTINE.

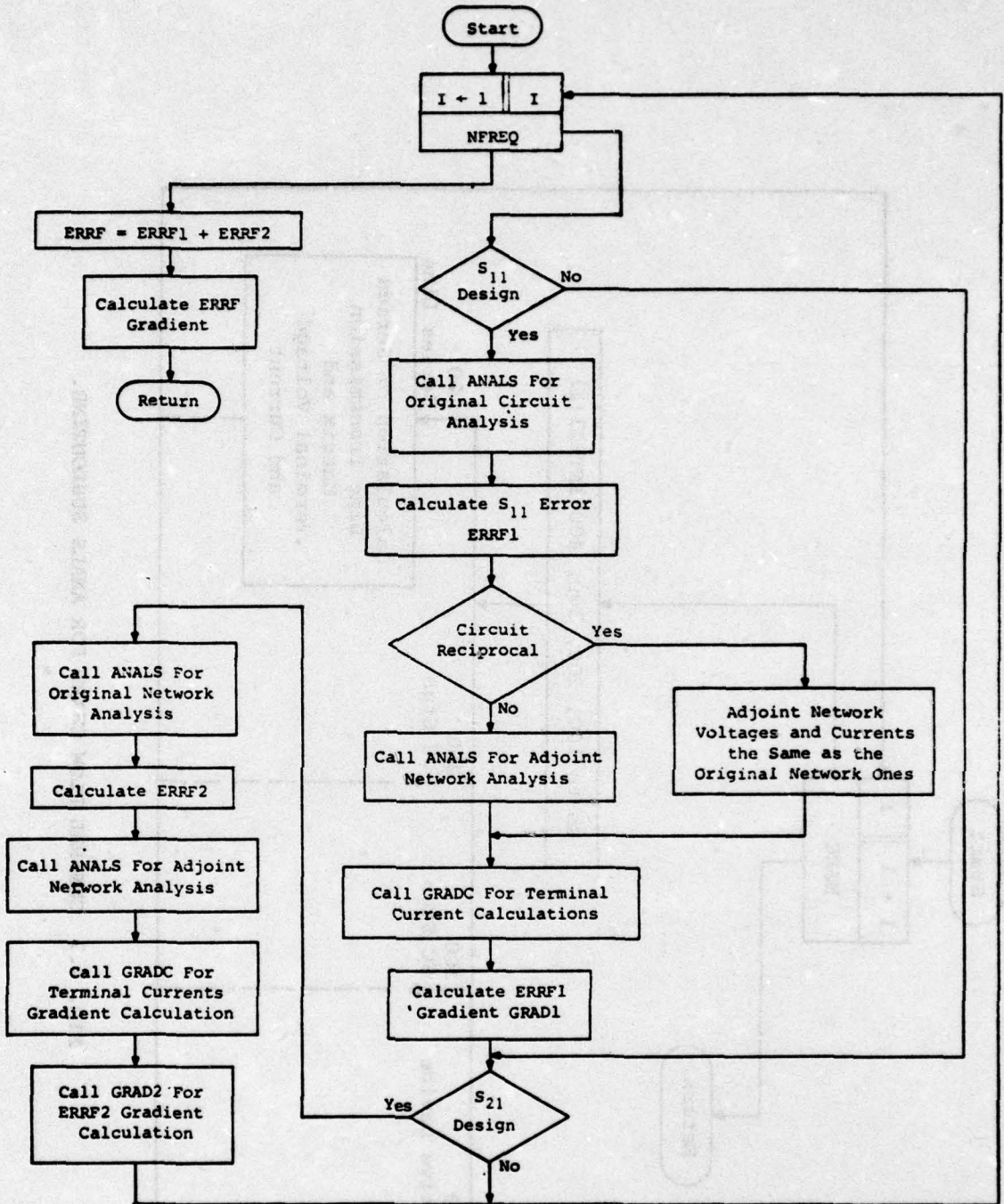


FIG. 4.6 GENERAL FLOW CHART FOR EVAL SUBROUTINE.

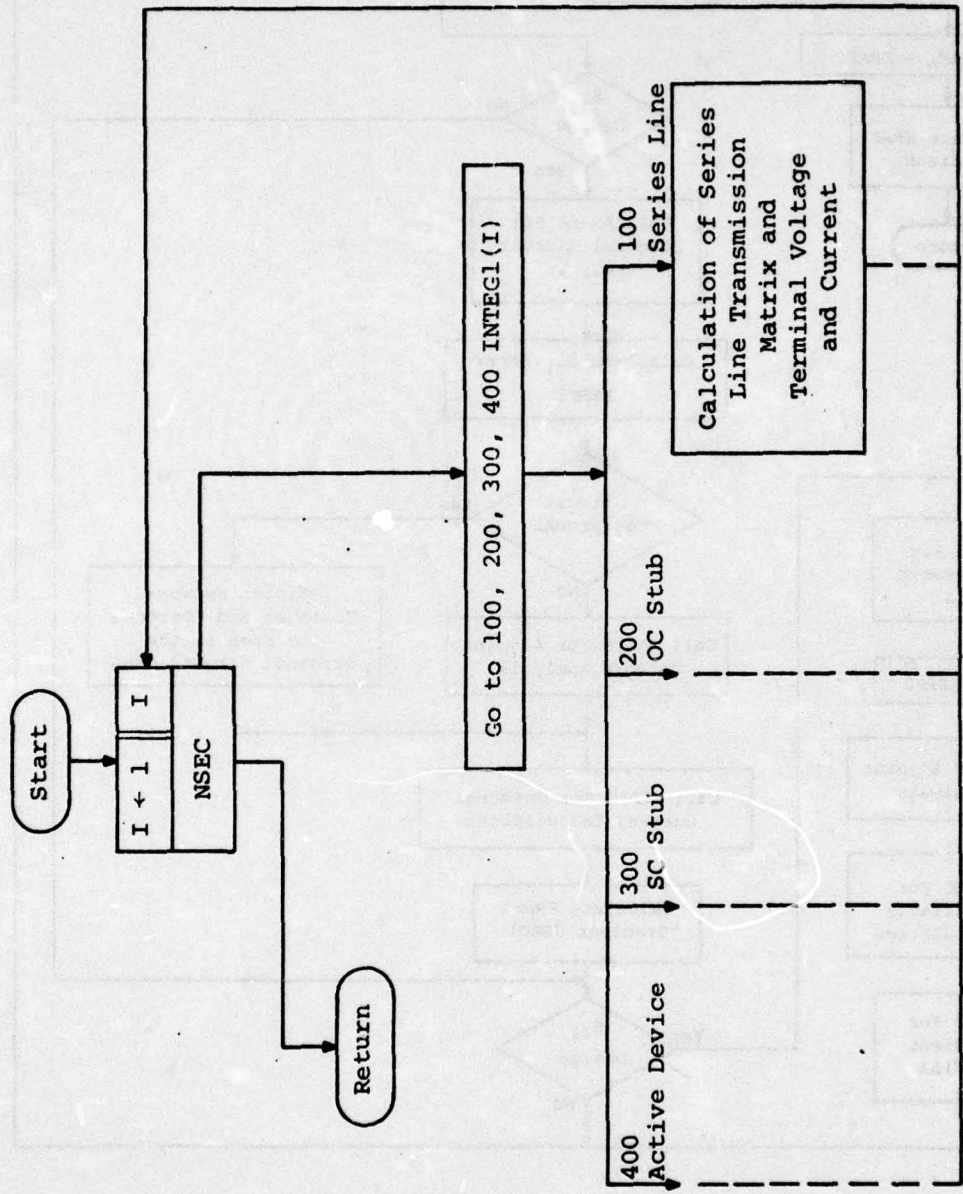


FIG. 4.7 GENERAL FLOW CHART FOR ANALS SUBROUTINE.

lossless open-circuit stubs, lossless short-circuit stubs, and any number of transistors and/or any number of active devices specified by their [S] or transmission matrix parameters.

Figure 4.8 shows the GRADC subroutine for the terminal current gradient calculations using the adjoint network method.

Subroutine MIN uses the Powell-Fletcher method for arriving at the function minimum by searching along the function gradient direction.

The subroutine OUTPUT prints out the initial and optimum parameters of the circuit as well as the gradients, gain and reflection coefficient. Also, it uses the subroutine EVAL to calculate the changes in gain and reflection coefficient resulting from perturbations of the parameters.

4.4 FETCAD Program Evaluation. As mentioned earlier, FETCAD can be used to assist in the design of different types of microwave circuits. An evaluation was carried out for different cases as follows:

4.4.1 Distributed Element Microwave Filter Design. Figure 4.9 shows a general microwave filter in which Z_G is real and equal to Z_L , and the box contains a selective network of lossless series lines, open-circuit stubs and short-circuit stubs. Depending on the location of the filter's selectivity in the frequency domain, filters can be divided into:

1. Low-pass filter (LPF).
2. Band-pass filter (BPF).
3. High-pass filter (HPF).
4. Band-stop Filter (BSF).

FETCAD can be used to design any of the cases mentioned above. As a test, it was used in the design of a Chebychev low-pass filter.

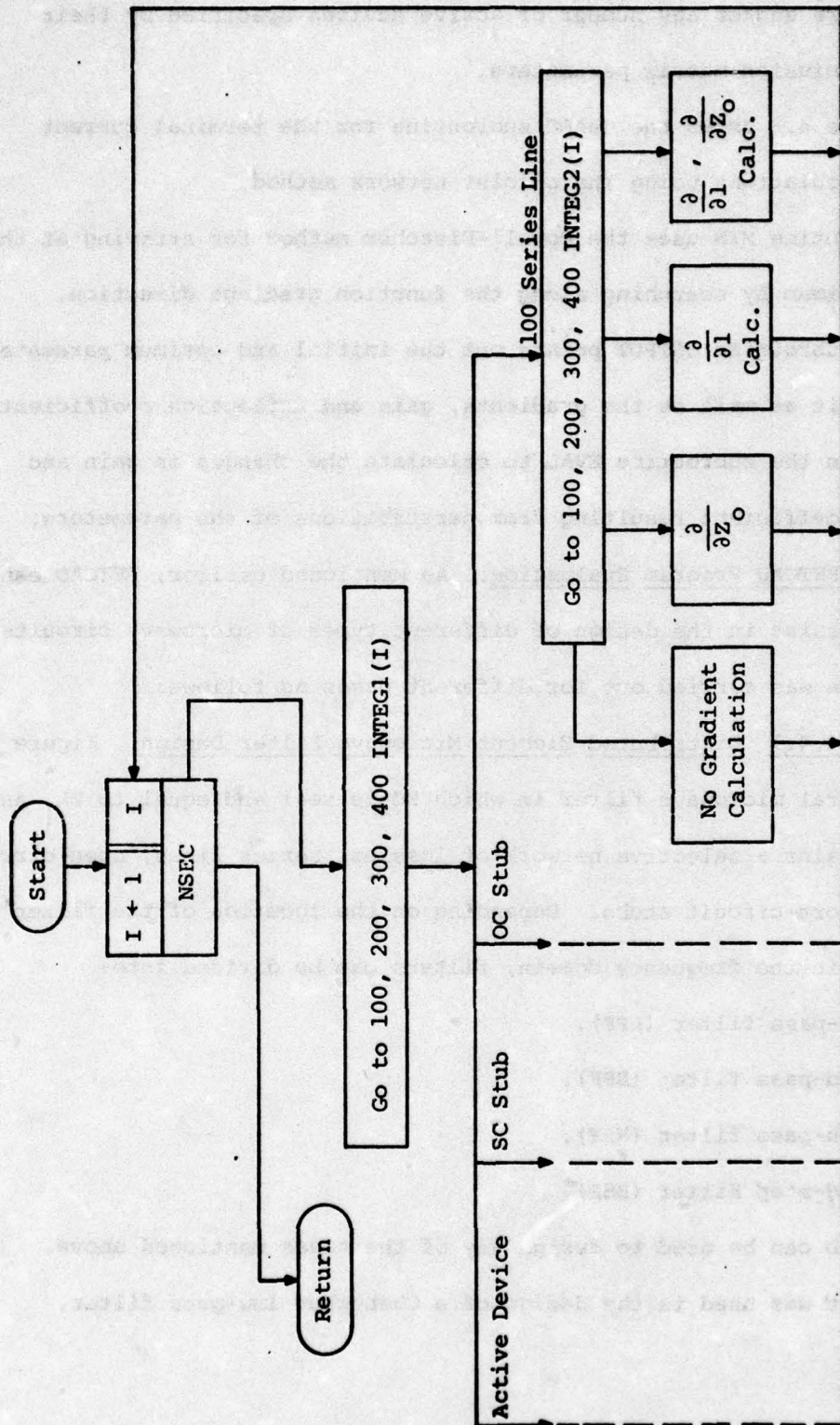


FIG. 4.8 GENERAL FLOW CHART FOR THE GRAD C SUBROUTINE.

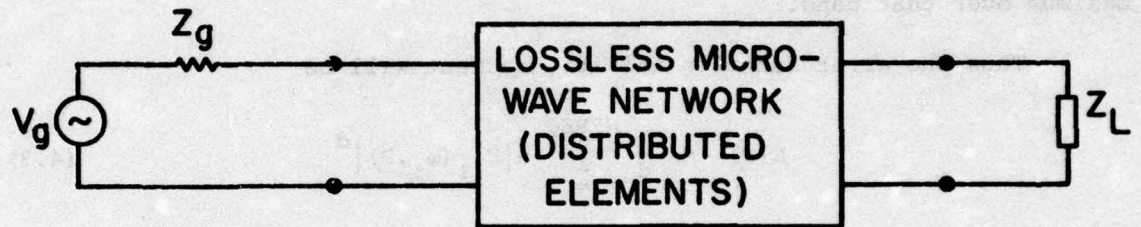


FIG. 4.9 MICROWAVE FILTER GENERAL BLOCK DIAGRAM.

Figure 4.10 illustrates such a filter consisting of 5 lossless transmission lines. Since the filter circuit is a lossless one and does not contain any active devices, then the transmission loss $|S_{21}|^2$ is related to the reflection loss $|S_{11}|^2$ by the expression

$$|S_{21}|^2 = 1 - |S_{11}|^2 .$$

For filter design, S_{11} is required only to be minimum over the specified frequency band; this in turn automatically guarantees that S_{21} will be maximum over that band.

Thus the error function and its gradient will be

$$E(\underline{P}) = \frac{1}{d} \sum_{i=1}^{NFREQ} a |S_{11}(\omega_i, \underline{P})|^d \quad (4.3)$$

and

$$\nabla E(\underline{P}) = \sum_{i=1}^{NFREQ} \operatorname{Re} \left[\frac{2R}{V} \frac{g}{g_i} |\Gamma_i|^{d-2} \Gamma_i^* \nabla I_{g_i} \right] , \quad (4.4)$$

respectively.

Figure 4.11 shows the initial and final insertion loss DB for such LPF having a bandwidth of 1.08 GHz.

4.4.2 Microwave Negative Resistance Amplifier Design. Figure 4.12a shows the negative resistance amplifier block diagram. It can be shown that the negative resistance amplifier design is equivalent to a reflection coefficient design S_{11} with Z_L^* replacing Z_L as a load impedance. Figure 4.12b,c illustrates such a transformation in which case the amplifier gain in DB will be

2. Collin, R. E., Foundation for Microwave Engineering, McGraw-Hill Book Co., Inc., New York, 1966.

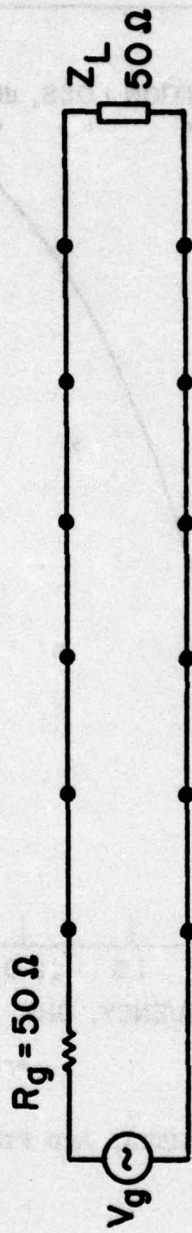


FIG. 4.10 CHEBYCHEV LOW-PASS FILTER DESIGN.

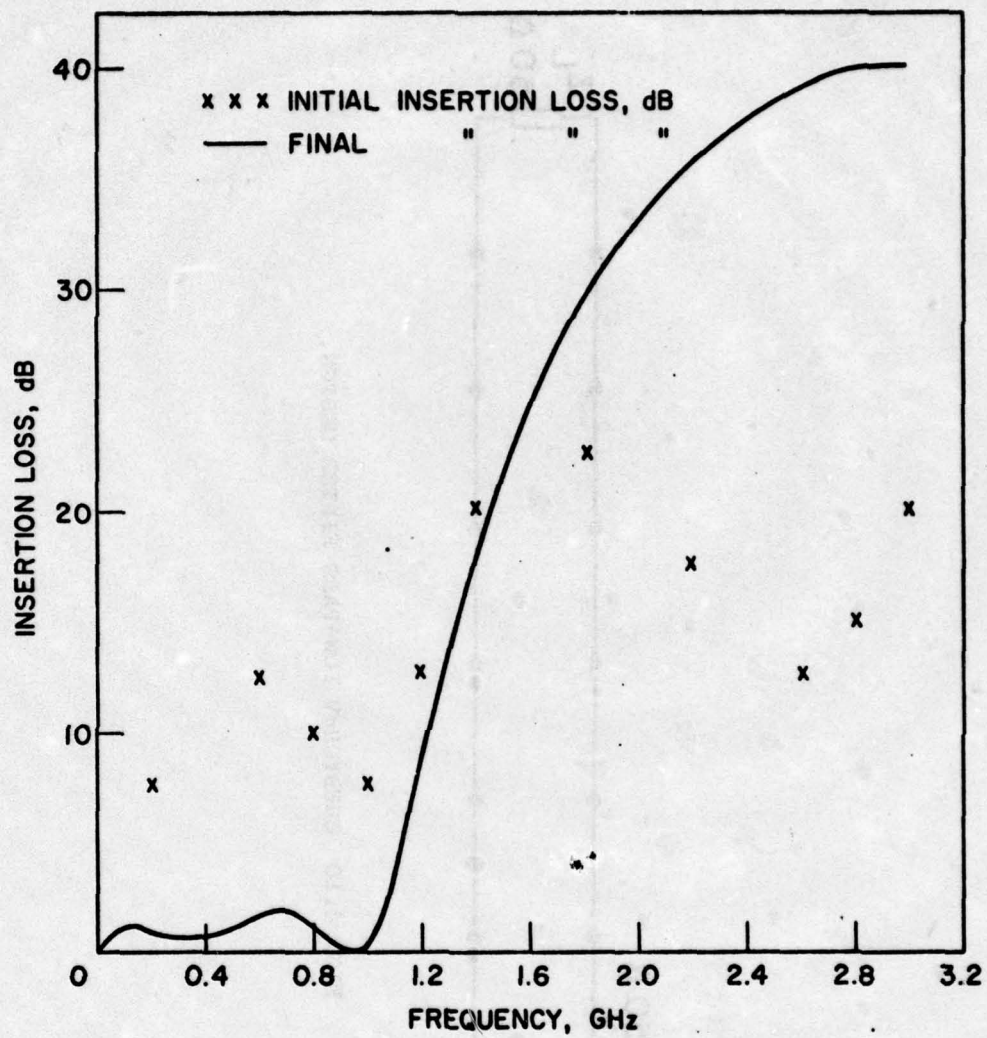
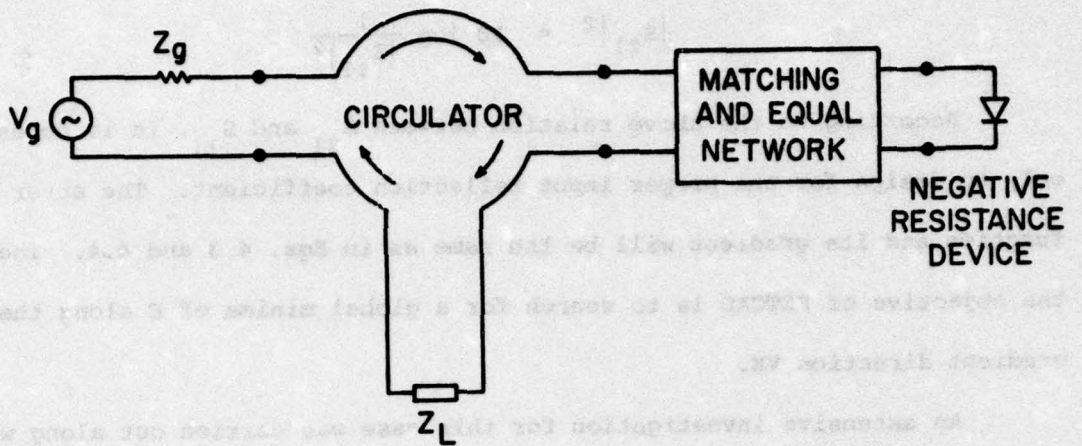
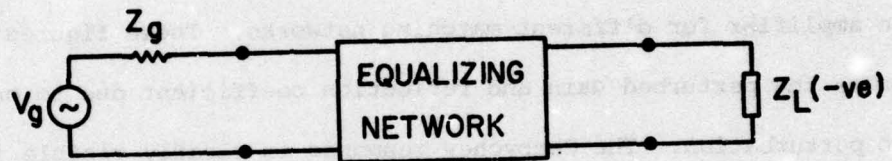


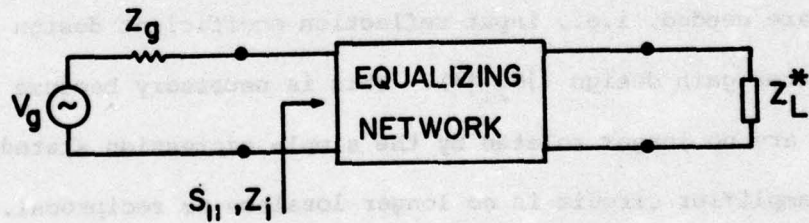
FIG. 4.11 LOW-PASS FILTER INITIAL AND FINAL INSERTION LOSS.



(a) NEGATIVE RESISTANCE AMPLIFIER BLOCK DIAGRAM



(b) NEGATIVE RESISTANCE AMPLIFIER EQUIVALENT CIRCUIT



(c) NEGATIVE RESISTANCE AMPLIFIER CIRCUIT TRANSFORMATION

FIG. 4.12 NEGATIVE RESISTANCE AMPLIFIER CIRCUIT DESIGN.

$$|S_{21}|^2 = 10 \log \frac{1}{|S_{11}|^2} .$$

According to the above relation between S_{21} and S_{11} , it is necessary only to design for the proper input reflection coefficient. The error function and its gradient will be the same as in Eqs. 4.3 and 4.4. Therefore the objective of FETCAD is to search for a global minima of E along the gradient direction ∇E .

An extensive investigation for this case was carried out along with using different matching network topologies. Figure 4.13a,b,c illustrates the initial and final gain in DB as well as the reflection coefficient for such an amplifier for different matching networks. These figures also illustrate the perturbed gain and reflection coefficient due to one element perturbation. The Chebychev response is clearly visible in the amplifier gain response.

4.4.3 Two-Port Amplifier Design. From the design point of view, this case is the most general and complicated one because two types of design are needed, i.e., input reflection coefficient design (S_{11}), and transducer gain design ($|S_{21}|^2$). This is necessary because $|S_{11}|^2$ and $|S_{21}|^2$ are no longer related by the simple expression stated earlier since the amplifier circuit is no longer lossless or reciprocal. Figure 4.14 shows a general two-port amplifier block diagram with JFET as the active device, and load and generator impedances of 50Ω . To evaluate this phase of the computer program, a transistor was selected with scattering parameters as found in the literature.³ Using a small computer

3. Neidert, R. E. and Willing, H. A., "Wide-Band Gallium Arsenide Power MESFET Amplifier," Trans. on Microwave Theory and Techniques, vol. MTT-24, No. 6, June 1976.

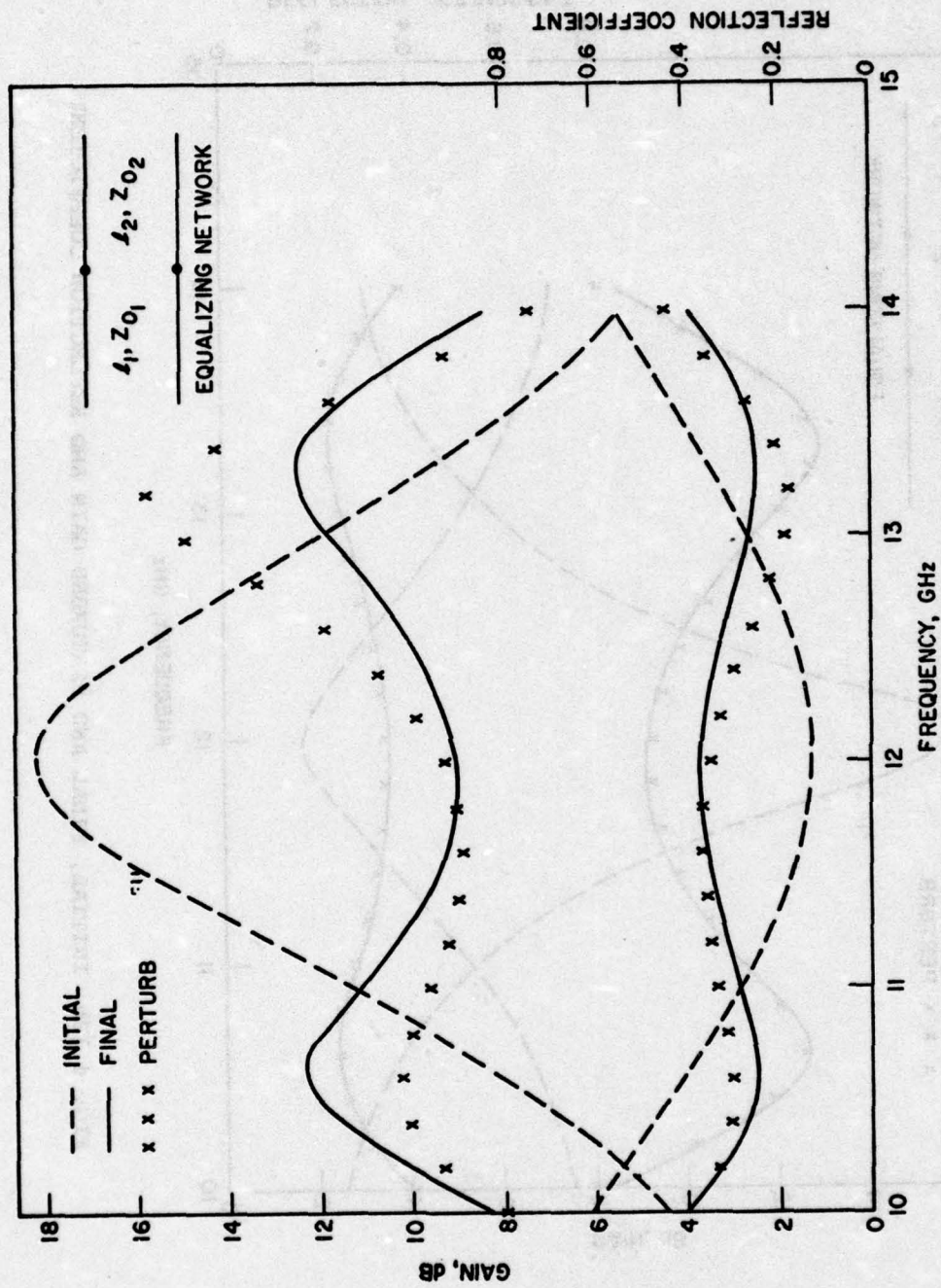


FIG. 4.13a INITIAL, FINAL AND PERTURBED GAIN AND REFLECTION COEFFICIENT.

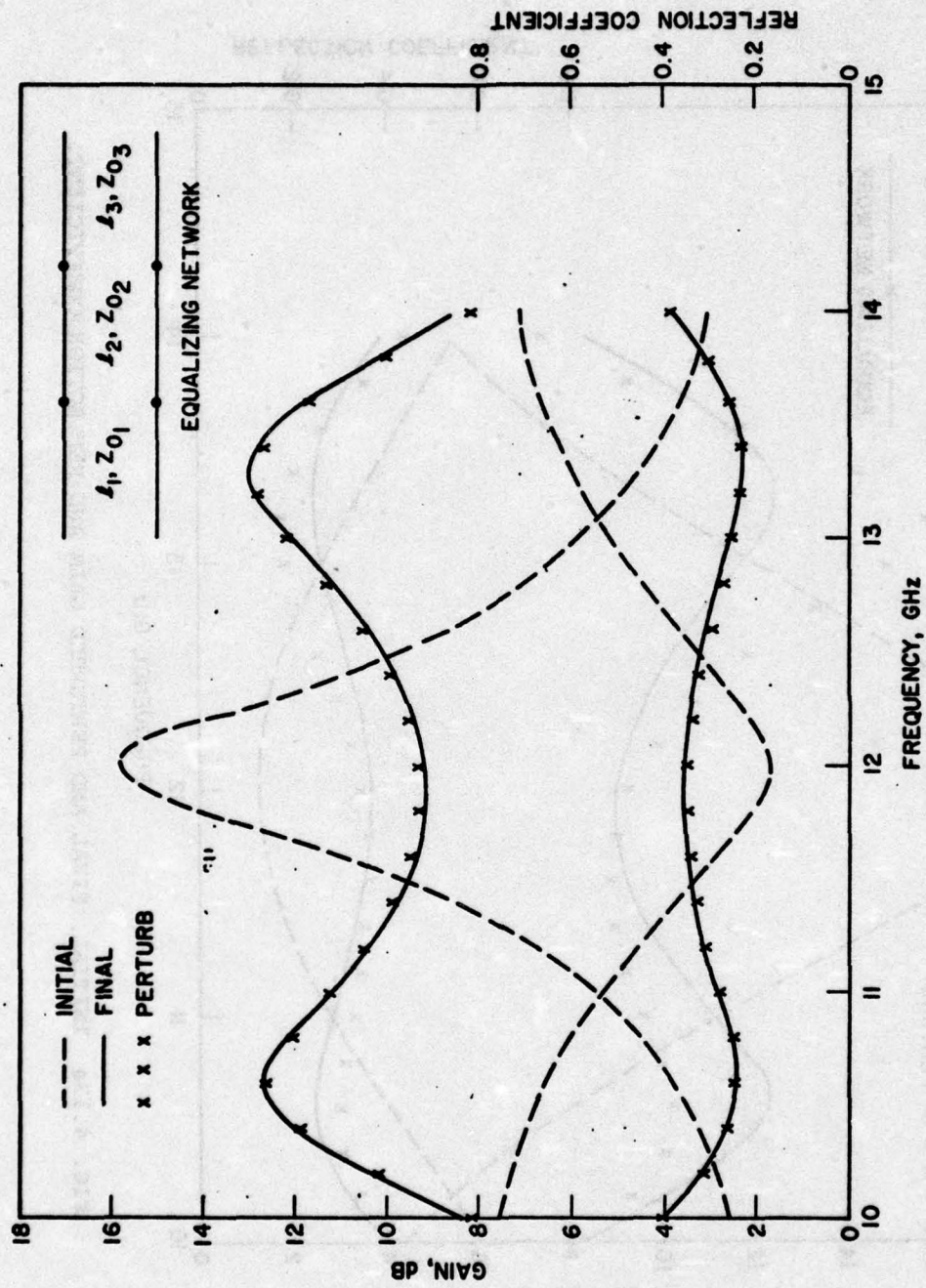


FIG. 4.13b INITIAL, FINAL AND PERTURBED GAIN AND REFLECTION COEFFICIENT.

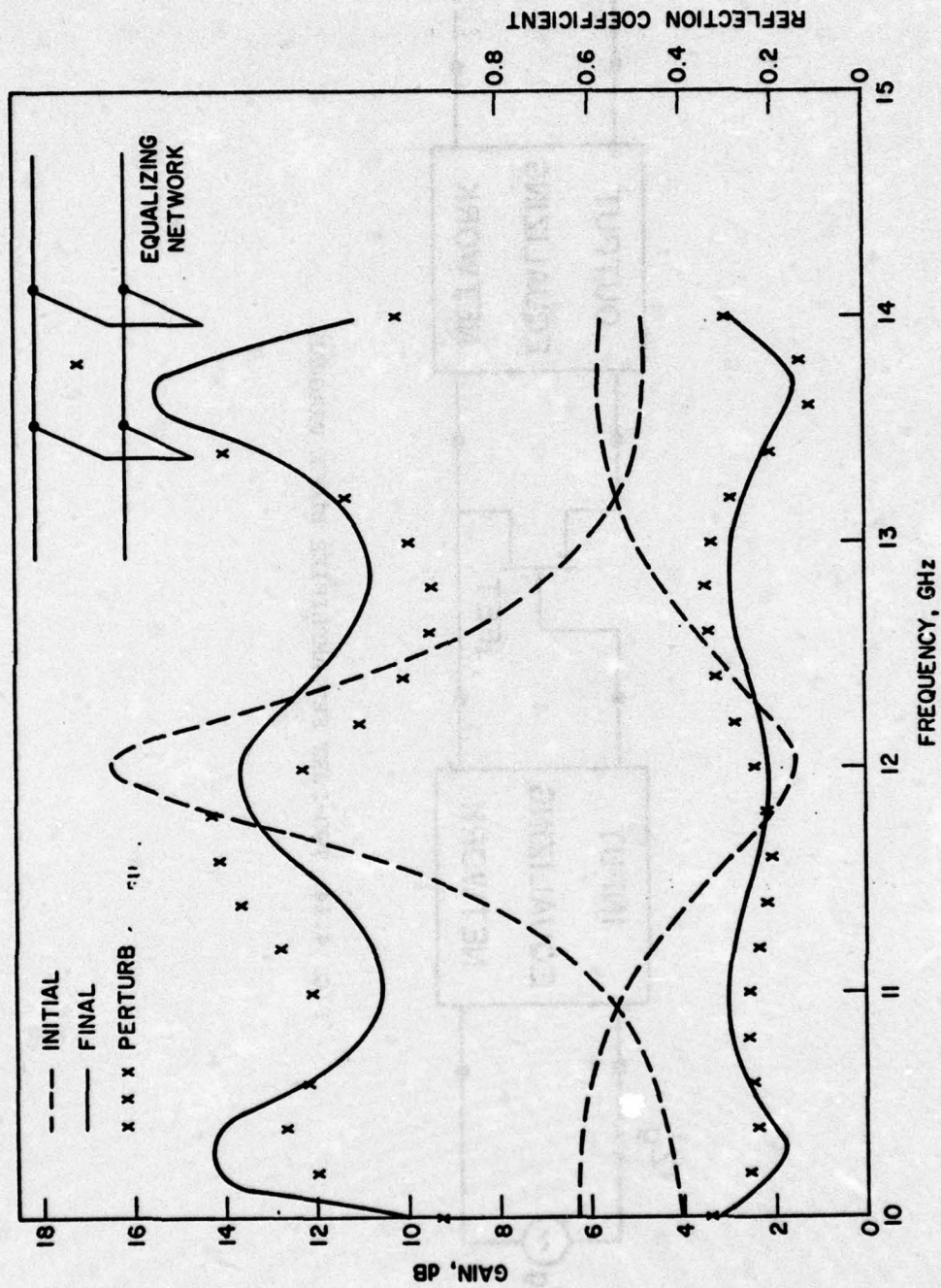


FIG. 4.13c INITIAL, FINAL AND PERTURBED GAIN AND REFLECTION COEFFICIENT.

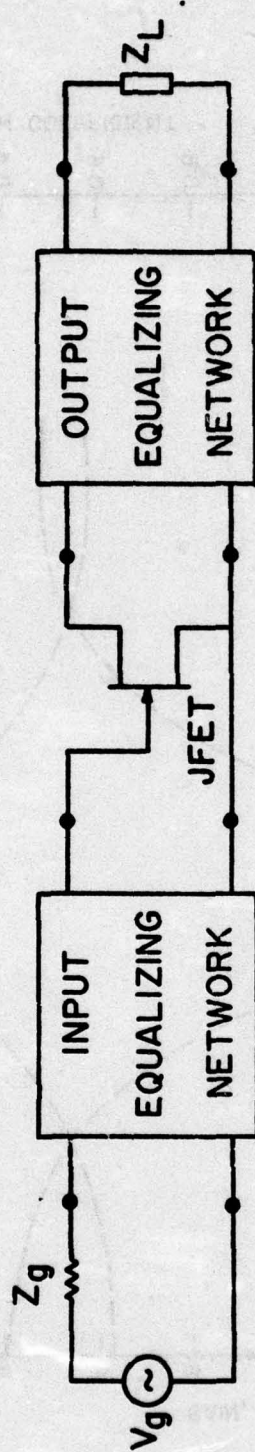


FIG. 4.14 TWO-PORT FET AMPLIFIER BLOCK DIAGRAM.

routine, the transistor maximum available gain MAG, unilateral gain UG and stability factor K were calculated. Figure 4.15 illustrates the MAG and the UG for the transistor over the 4 to 12 GHz frequency band. Notice that the transistor is absolutely stable in the 6.5 to 8.5 GHz and 11 to 12 GHz frequency bands but unstable outside of those bands. This is the reason why the MAG has values only in these frequency bands.

Figure 4.16 shows the transistor together with the initial proposed input and output equalizing networks. The error function and its gradient will be the same as in Eqs. 4.1 and 4.2, respectively.

An intensive investigation is being directed toward this phase of the computer program which is still not giving realistic results. In particular, the input reflection coefficient S_{11} is found to be greater than unity thus indicating that the optimized amplifier is unstable.

4.5 Conclusion. An optimization computer program which can be used in the design of microwave filters, negative resistance amplifiers, and two-port microwave amplifiers has been developed. Some of the computer design results for the above cases have been presented and discussed.

5. Pulsed Operating Characteristics of Devices

N. A. Masnari and J. R. East

5.1 Introduction. The purpose of this phase of the program is a general study of the pulsed operation of solid-state microwave oscillators with particular attention given to the frequency drift during operation. The goal of the study is to understand the limits on the frequency stability of oscillators and the necessary conditions on

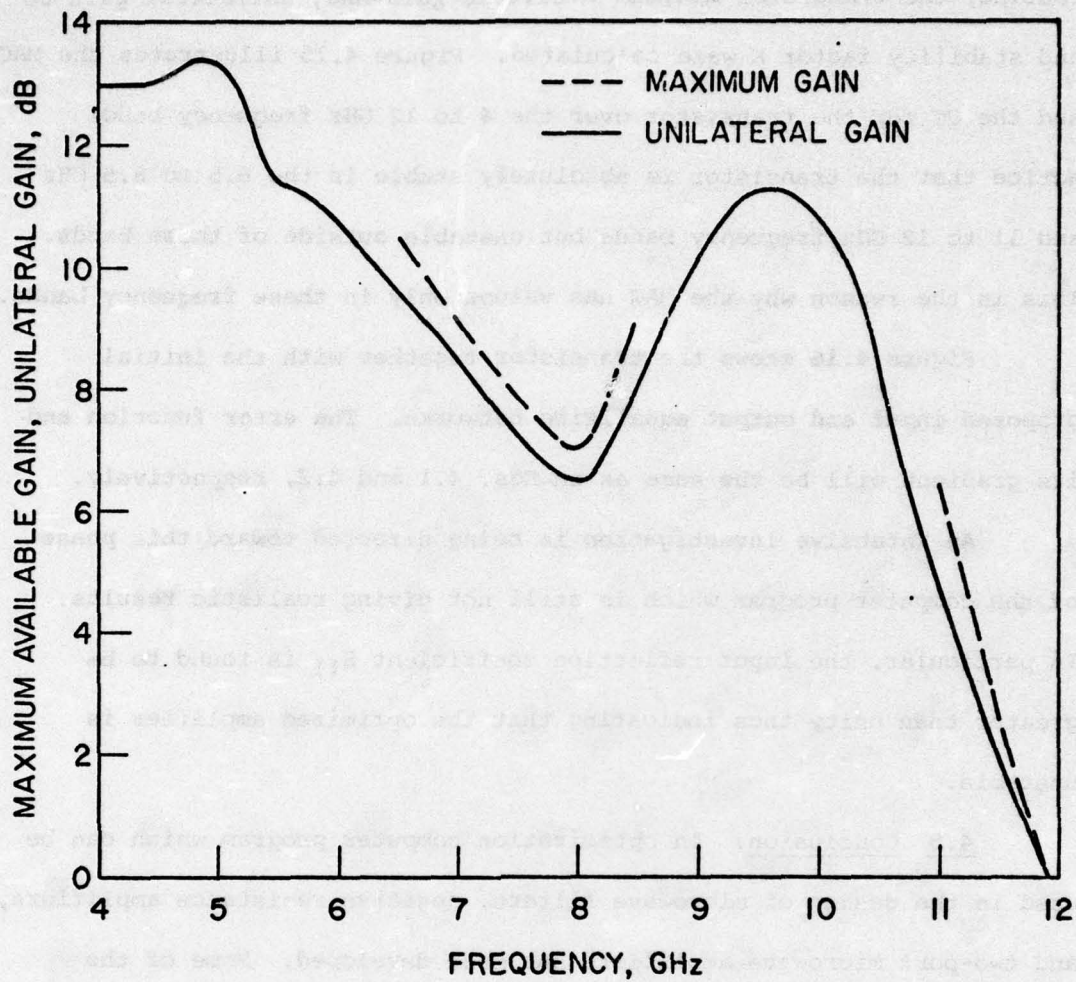


FIG. 4.15 TRANSISTOR MAXIMUM AVAILABLE GAIN AND UNILATERAL GAIN.

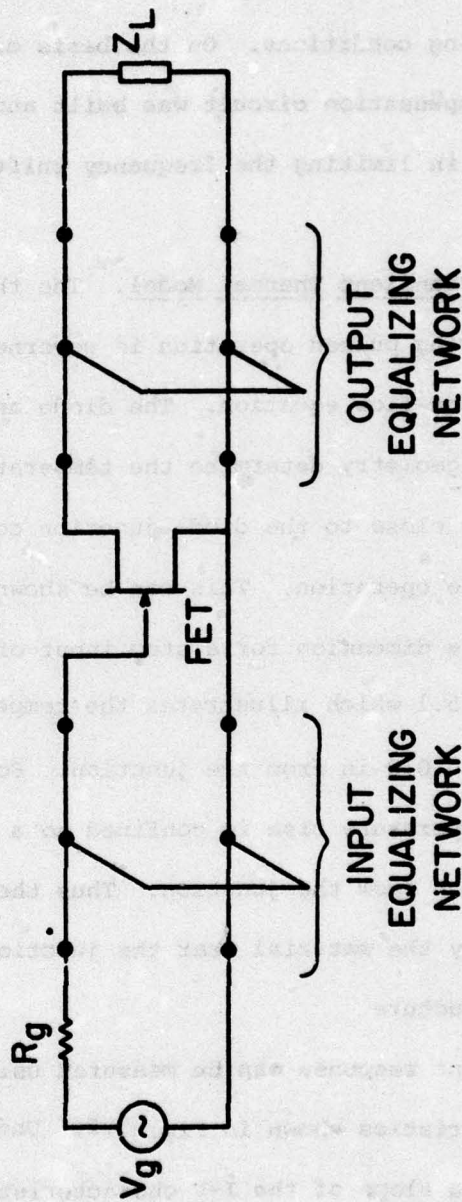


FIG. 4.16 FET AMPLIFIER INITIAL NETWORK.

the microwave and bias circuits to limit or control the frequency shift during the pulse. Work has centered on pulsed IMPATT oscillators operating at X-band. During the first part of the study the diode was characterized by a simple thermal model. The model can be used for various temperatures and operating conditions. On the basis of this thermal model a bias-current compensation circuit was built and tested to evaluate its capability in limiting the frequency shift during pulsed operation.

5.2 Oscillator Transient Thermal Model. The thermal response of an IMPATT oscillator during pulsed operation is governed by the three-dimensional transient heat-flow equation. The diode and heat-sink material properties and geometry determine the temperature vs. time behavior. The materials close to the diode junction control the temperature rise for short-pulse operation. This can be shown by solving the heat-flow equation in one dimension for a step input of power. The result is shown in Fig. 5.1 which illustrates the temperature vs. time at planes 0.001, 0.005 and 0.010 in from the junction. For pulse widths of less than 100 μ s the temperature rise is confined to a region within a few thousandths of an inch from the junction. Thus the transient response is determined by the material near the junction, and not by the cavity heat-sink structure.

The diode transient response can be measured using the reverse current-voltage characteristics shown in Fig. 5.2. Under constant temperature operation the slope of the I-V characteristic is equal to the inverse of the diode space-charge resistance plus the loss in the diode.

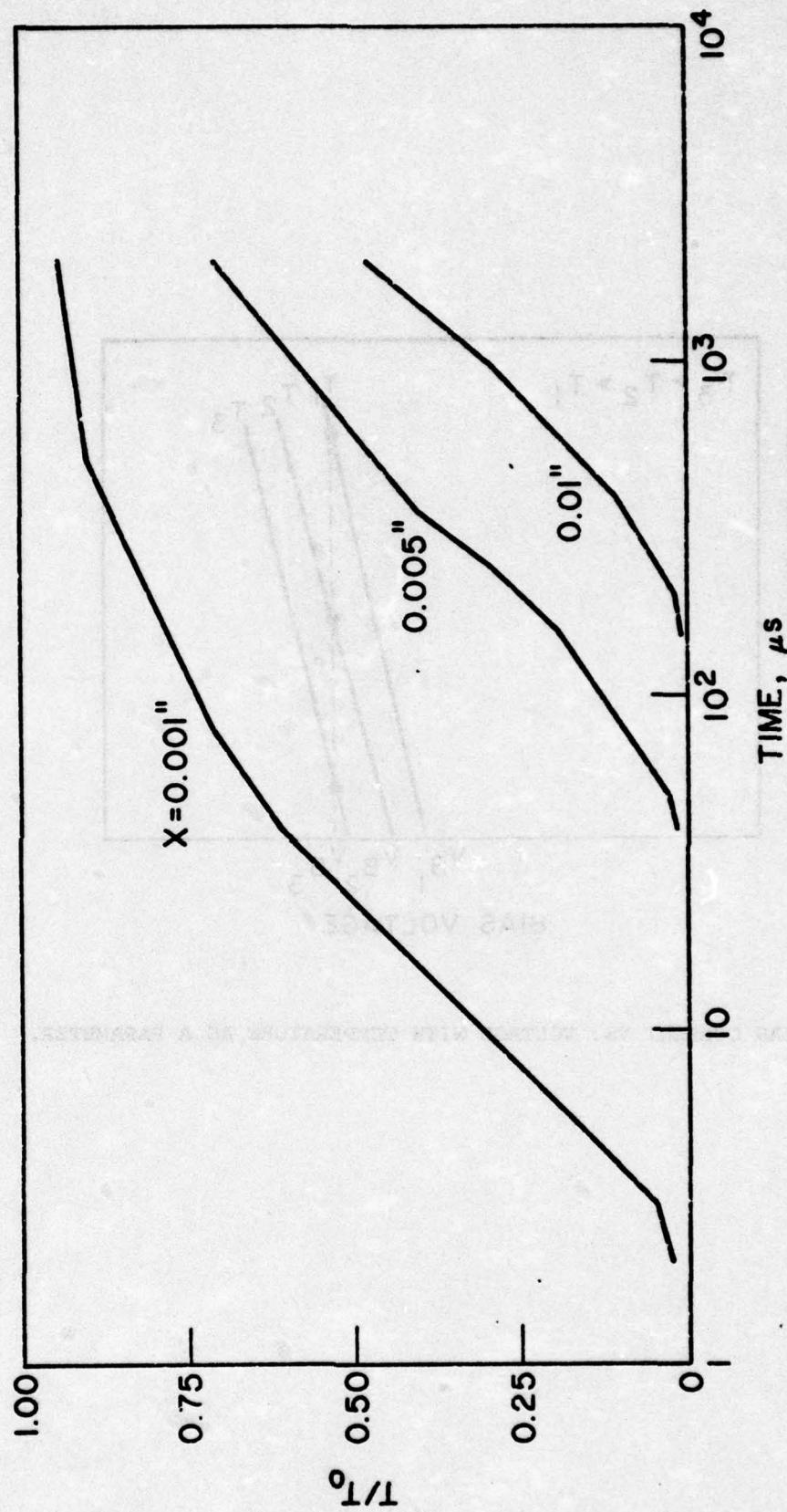


FIG. 5.1 TEMPERATURE RISE VS. TIME AT VARIOUS DISTANCES FROM THE JUNCTION FOR ONE-DIMENSIONAL STEP RESPONSE USING GOLD MATERIAL PARAMETERS.

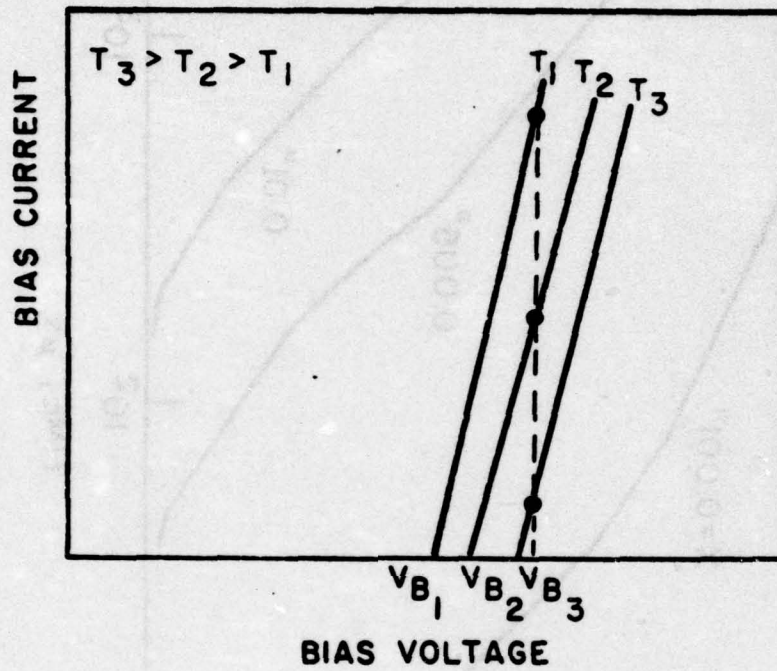


FIG. 5.2 BIAS CURRENT VS. VOLTAGE WITH TEMPERATURE AS A PARAMETER.

As the temperature is increased the I-V curve moves to the right in Fig. 5.2. To measure the diode thermal response the diode is biased with a constant voltage pulse. As the diode temperature increases during the pulse the current will decrease along the vertical dotted line shown in the figure. A semi-logarithmic plot of current vs. time is shown in Fig. 5.3 for an X-band Si IMPATT diode. Since the current vs. time curves in the figure are approximately linear, the thermal response can be approximated by an exponential variation. The slope of the curves is the time constant τ . The time constant can be found by making a least-square fit to the current vs. time data. The time constant has been measured for a variety of pulse widths, duty cycles and diode conditions. The time constant is approximately constant over a pulse-width range of 1 to 50 μ s, a duty-cycle range of 0.1 to 10 percent and over a two-to-one variation in diode thermal resistance. The variation of τ with temperature is shown in Fig. 5.4 which indicates that it varies between 32 and 20 μ s as the temperature changes from -146 to +100°C. This thermal behavior can be explained by considering the thermal properties of gold. The diodes used in these measurements are mounted on small gold heat-sink pads and bonded onto microwave packages. There is a 0.001 to 0.002 in thick gold layer between the diode and the package, which is gold-plated copper. The value of the thermal diffusion coefficient (D) was calculated as a function of temperature and compared to the plot of τ vs. temperature. The ratio τ/D was found to be approximately constant thus indicating that the value of τ is primarily determined by the properties of the small gold heat sink near the diode. This information can be used to design a circuit

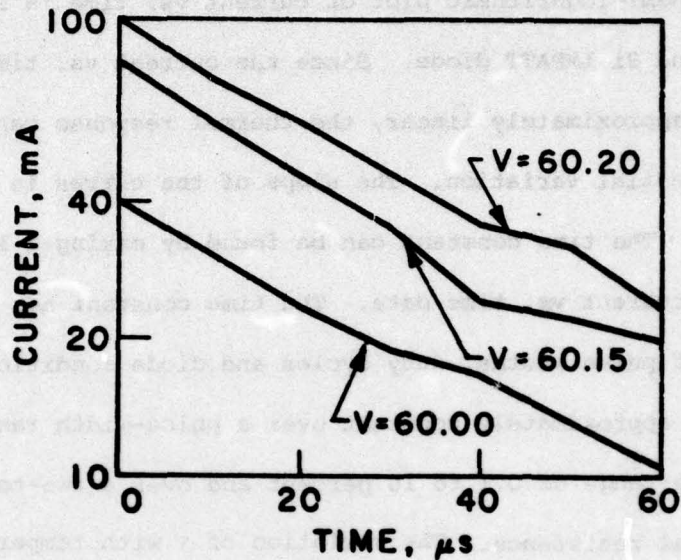


FIG. 5.3 CURRENT VS. TIME IN X-BAND IMPATT DIODE WITH CONSTANT VOLTAGE DRIVE.

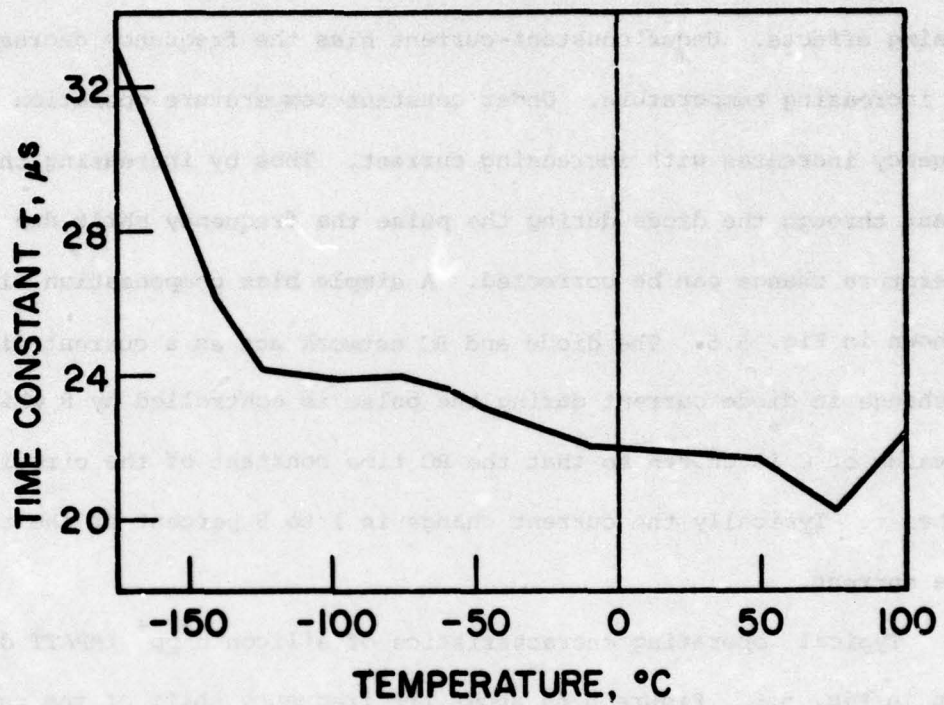


FIG. 5.4 THERMAL TIME CONSTANT OF PULSED IMPATT OSCILLATOR.

to compensate for the diode oscillation frequency shift which would occur in an uncompensated diode under normal pulsed operating conditions.

Frequency drift in IMPATT diodes can be compensated by using two opposing effects. Under constant-current bias the frequency decreases with increasing temperature. Under constant-temperature operation the frequency increases with increasing current. Thus by increasing the current through the diode during the pulse the frequency shift due to temperature change can be corrected. A simple bias compensation circuit is shown in Fig. 5.5. The diode and RC network act as a current divider. The change in diode current during the pulse is controlled by R while the value of C is chosen so that the RC time constant of the circuit matches τ . Typically the current change is 1 to 5 percent of the total diode current.

Typical operating characteristics of silicon n^+pp^+ IMPATT diodes are shown in Fig. 5.6. Figure 5.6a shows the frequency shift of the oscillator for a constant 1 percent duty cycle, a pulse width between 4 and 400 μ s, constant microwave tuning and a fixed compensation network. For short pulses the compensation network limits the frequency shift to less than 2 MHz. For pulse widths longer than 40 μ s the assumption that a single time constant is sufficient to describe the heating process is no longer valid and the frequency shift increases.

The effect of the microwave circuit on the frequency drift was measured using a GaAs IMPATT diode in a waveguide cavity. The frequency drift under constant current biasing conditions was compared to the frequency drift obtained for compensated bias and different cavity Q s.

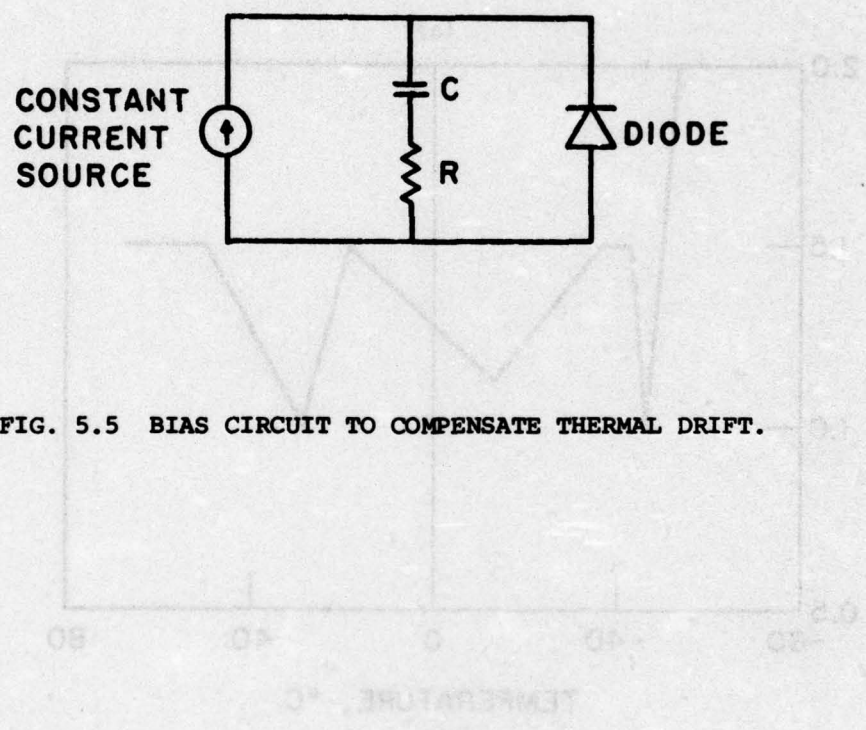
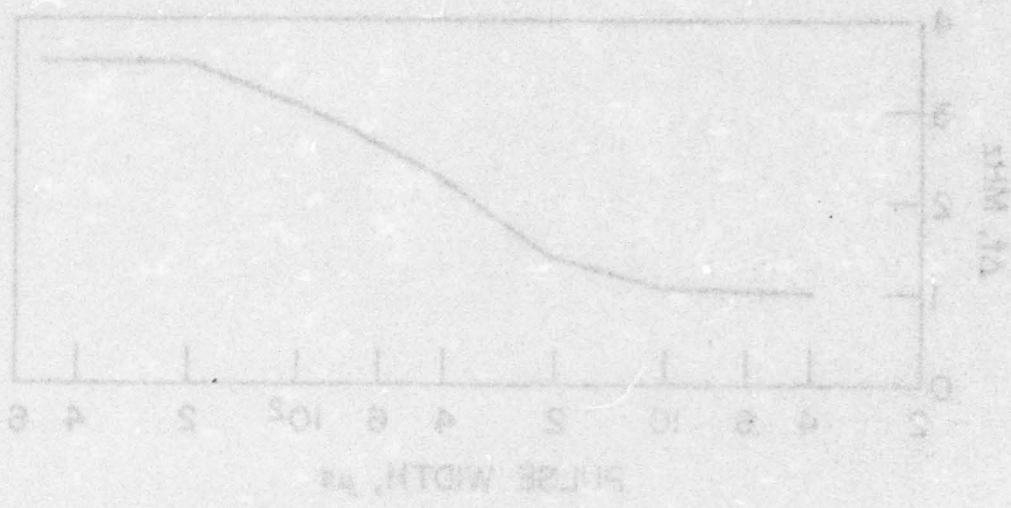


FIG. 5.5 BIAS CIRCUIT TO COMPENSATE THERMAL DRIFT.

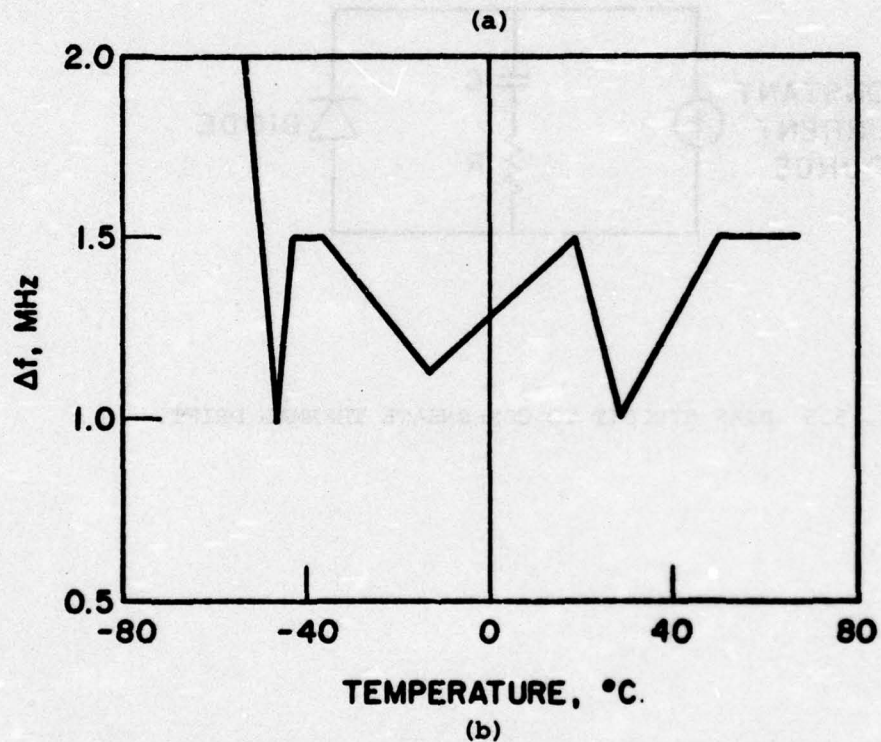
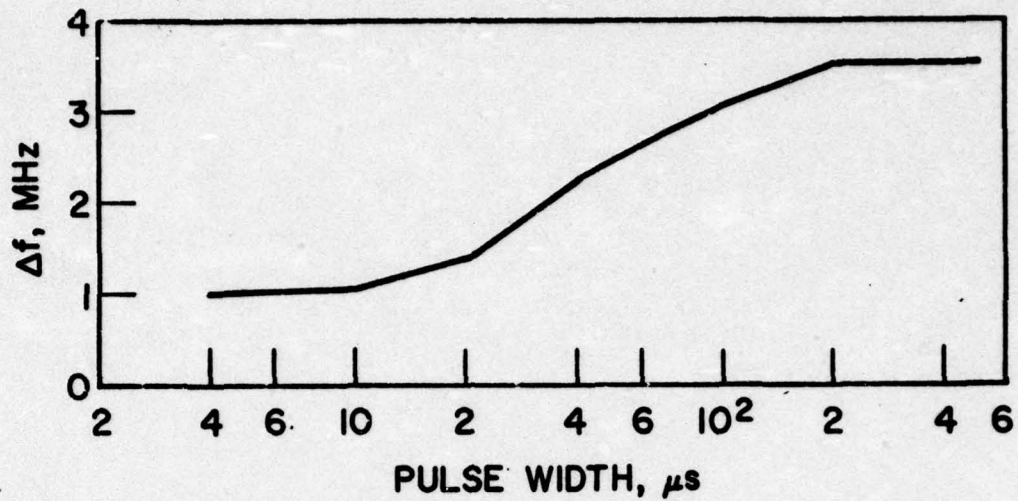


FIG. 5.6 (a) FREQUENCY SHIFT OF PULSE OSCILLATORS VS. PULSE WIDTH AND (b) FREQUENCY SHIFT OF COMPENSATED PULSED n^+pp^+ Si IMPATT VS. TEMPERATURE FOR CONSTANT MICROWAVE TUNING AND CONSTANT COMPENSATION NETWORK (5 μs PULSE WIDTH). (X-Band Oscillator)

The cavity Q was found by measuring the injection locking bandwidth vs. locking signal power. Figure 5.7 illustrates the results obtained for a circuit with $Q = 416$ as compared to one with $Q = 189$. The use of the compensation circuit reduces the frequency shift by a factor of 3. At the short pulse-width end of the data the compensated diode frequency increases because of pulse distortion due to frequency response limitations in the pulser and constant-current source. As the pulse width becomes longer than $50 \mu\text{s}$, the single time constant approximation is no longer valid and a more complicated current waveshape is necessary.

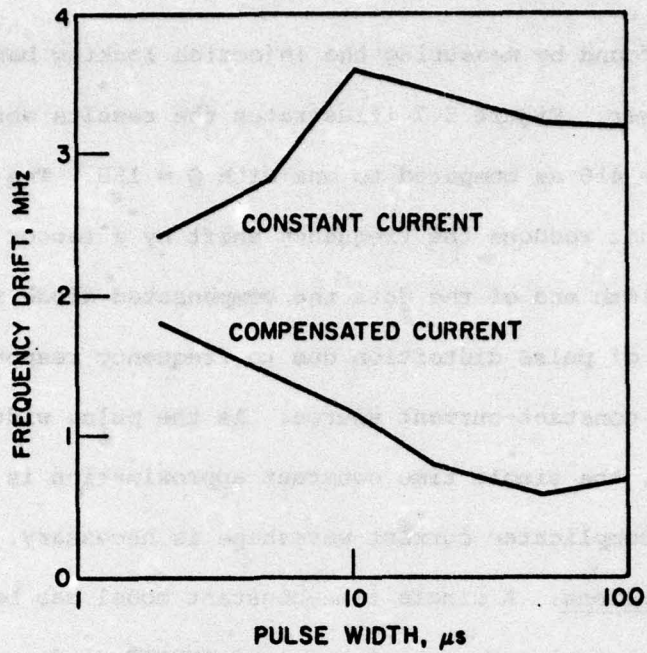
5.3 Conclusions. A single time-constant model has been used to characterize the thermal response of a pulsed IMPATT diode. This model is useful over a wide range of operating pulse widths, duty cycles and operating temperatures. The model has been used to build a bias compensation network to control the frequency shift of pulsed diodes. By using such a compensation network the frequency drift has been reduced significantly; for short pulse widths the frequency shift at X-band has been limited to less than 2 MHz.

6. Controlled Avalanche Transit-Time Triode

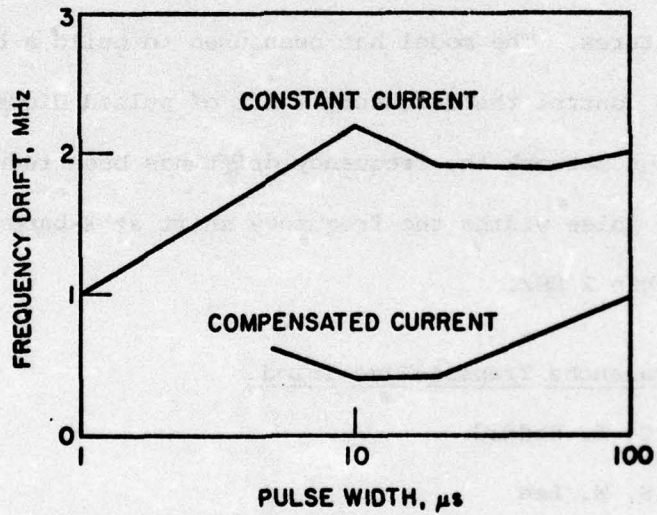
Supervisor: G. I. Haddad

Staff: S. W. Lee

6.1 Introduction. During this phase of the program, efforts were made to investigate the avalanche multiplication phenomenon and the transit-time effects in controlled avalanche transit-time triode (CATT) devices. Analytical expressions were developed which allow calculation of the avalanche multiplication factor, avalanche delay, RF avalanche current



(a)



(b)

FIG. 5.7 (a) FREQUENCY DRIFT OF GaAs IMPATT ($Q = 416$ AND $f_0 = 8.75$ GHz) AND
 (b) FREQUENCY DRIFT OF GaAs IMPATT ($Q = 189$ AND $f_0 = 8.77$ GHz).

and small-signal impedance of the collector region. These expressions will be very useful in the construction of a model for the CATT oscillator. A study on emitter-coupled three-terminal CATT oscillators was also carried out. Conditions for optimum extractable power and load requirement for the emitter-coupled CATT oscillator were obtained.

6.2 Analysis of the CATT Oscillator.

6.2.1 Introduction. In this analysis, it has been assumed that the emitter and the base regions of the CATT oscillator are very similar to that of the bipolar junction transistor (BJT). In a $n^+ - p^+ - n - i - n^+$ CATT device, electrons are injected from the emitter-base junction and diffuse across the base region into the base-collector junction. There are avalanche-generated holes feeding back into the base and emitter regions, but this feedback effect is neglected to keep the analysis simple. The basic differences between the CATT and the BJT devices arise from two physical processes, namely, avalanche multiplication and transit-time in the collector region (Fig. 6.1). The collector region is divided into two subregions, namely, the avalanche and drift subregions. The effects of each will be analyzed.

6.2.2 Avalanche Multiplication. The differential equations that appropriately describe the physics involved here are the fundamental transport equations for electrons and holes. They are^{1,2}

-
1. Bulucea, C. D. and Prisecarn, D. C., IEEE Trans. on Electron Devices, vol. ED-20, No. 8, August 1973.
 2. Moll, J. L. and Van Overstraeten, R., Solid-State Electronics, vol. 6, No. 3, March-April 1963.

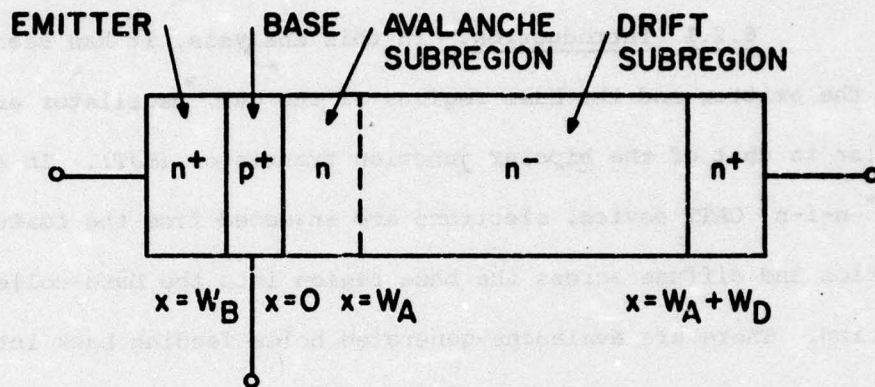


FIG. 6.1 CONTROLLED AVALANCHE TRANSIT-TIME TRIODE.

$$\frac{1}{v_s} \frac{\partial J_n}{\partial t} = - \frac{\partial J_n}{\partial x} + (J_p \beta_p + J_n \beta_n) ,$$

$$\frac{1}{v_s} \frac{\partial J_p}{\partial t} = \frac{\partial J_p}{\partial x} + (J_p \beta_p + J_n \beta_n) . \quad (6.1a)$$

It is assumed that under small-signal operation, the above quantities can be approximately represented as follows:

$$J_n(x,t) = \text{the electron particle current} = J_{no}(x) + \tilde{J}_{na}(x)e^{j\omega t} ,$$

$$J_p(x,t) = \text{the hole particle current} = J_{po}(x) + \tilde{J}_{pa}(x)e^{j\omega t} ,$$

$$E(x,t) = \text{the electric field} = E_o(x) + \tilde{E}_a e^{j\omega t} ,$$

$$\beta_n = \text{the field dependent electron ionization rate} = \beta_{no} + \beta'_{na} \tilde{E}_a e^{j\omega t} ,$$

$$\beta_p = \text{the field dependent hole ionization rate} = \beta_{po} + \beta'_{pa} \tilde{E}_a e^{j\omega t} \text{ and}$$

$$v_s = \text{the scattering limited drift velocity for electrons and holes.}$$

Another assumption used in calculating the avalanche multiplication factor M , is that M is a function of the dc bias only. The effect of the RF small signal can be neglected. Under dc conditions, Eq. 6.1a becomes

$$- \frac{\partial J_{no}(x)}{\partial x} + J_{po}(x)\beta_{po} + J_{no}(x)\beta_{no} = 0 ,$$

$$\frac{\partial J_{po}(x)}{\partial x} + J_{po}(x)\beta_{po} + J_{no}(x)\beta_{no} = 0 . \quad (6.1b)$$

The total current density is constant and thus,

$$J_o \stackrel{\Delta}{=} J_{po}(x) + J_{no}(x) = f(x) . \quad (6.2)$$

The solution of Eq. 6.1b is therefore:

$$J_{no}(x) = \frac{J_{dc} \int_0^x \beta_{po}(x') \exp \left\{ \int_0^{x'} [\beta_{po}(x'') - \beta_{no}(x'')] dx'' \right\} dx' + C_1}{\exp \left\{ \int_0^x [\beta_{po}(x') - \beta_{no}(x')] dx' \right\}}$$

The boundary conditions are

$$J_{no}(0) = J_{nsE} [\exp (qV_{EBO}/kT) - 1] \alpha_o + J_{nsc}$$

and

$$J_{po}(W_A) = J_{psc}$$

where $V_{EB} =$ the emitter-base junction voltage $= V_{EBO} + \bar{V}_{EB} e^{j\omega t}$,

$V_{EBO} =$ the dc emitter-base junction voltage,

$\alpha_o =$ the dc common-base current multiplication factor in a BJT with equivalent emitter and base structures,

$J_{nsE} =$ the reverse electron saturation current associated with the emitter-base junction,

$J_{nsc} =$ the reverse electron saturation current associated with the base-collector junction and

$J_{psc} =$ the reverse hole saturation current associated with applying these boundary conditions.

The following expression for $J_{no}(x)$ is obtained:

$$J_{no}(x) = \frac{J_{dc} \int_0^x \beta_{po}(x') \exp \left\{ \int_0^{x'} [\beta_{po}(x'') - \beta_{no}(x'')] dx'' \right\} dx'}{\exp \left\{ \int_0^x [\beta_{po}(x') - \beta_{no}(x')] dx' \right\}} + \frac{J_{nsE} [\exp (qV_{EBO}/kT) - 1] \alpha_o + J_{nsc}}{\exp \left\{ \int_0^x [\beta_{po}(x') - \beta_{no}(x')] dx' \right\}} \quad (6.3)$$

Equation 6.3 can be used to calculate the dc electron particle current density in the avalanche subregion if the electric field is a known function of the distance. At $x = W_A$,

$$J_o - J_{po}(W_A) = J_{no}(W_A)$$

and

$$J_{po}(W_A) = J_{psc}$$

The following relation can be derived from Eq. 6.3 by using the boundary condition at $x = W_A$:

$$J_o = \frac{J_{psc} \exp \int_0^{W_A} (\beta_{po} - \beta_{no}) dx' + \{J_{nse} [\exp (qV_{EBO}/kT) - 1] \alpha_o + J_{nsc}\}}{1 - \int_0^{W_A} \beta_{no}(x') \exp \left\{ \int_0^{x'} [\beta_{po}(x'') - \beta_{no}(x'')] dx'' \right\} dx'}$$

This can be written in the more convenient form

$$J_o = M J_{so} \quad (6.4)$$

where J_{so} is the dc current density if there is no avalanche multiplication,

$$J_{so} = J_{nse} [\exp (qV_{EBO}/kT) - 1] \alpha_o + J_{nsc} + J_{psc} \quad (6.5)$$

and M_n is the avalanche multiplication factor when initiated only by electrons:

$$M_n = \frac{1}{1 - \int_0^{W_A} \beta_{no} \exp \left\{ \int_0^{x'} [\beta_{po} - \beta_{no}] dx'' \right\} dx'} \quad (6.6)$$

and

$$M = \frac{J_n \left\{ J_{psc} \exp \left[\int_0^{W_A} (\beta_{po} - \beta_{no}) dx \right] + J_{nse} [\exp (qV_{EBO}/kT) - 1] \alpha_o + J_{nsc} \right\}}{J_{nse} [\exp (qV_{EBO}/kT) - 1] \alpha_o + J_{nsc} + J_{psc}} \quad (6.7)$$

Equations 6.4 through 6.7 can be employed to calculate the dc current density in the avalanche subregion and the avalanche multiplication factor M if the electric field is known.

It is worthwhile to note that when $\beta_{no} = \beta_{po}$, $J_{nsc} = 0$ and $J_{psc} = 0$, $J_o = J_{no}(W_A)$. Equations 6.4 through 6.7 can be combined to give

$$J_o = \frac{J_{nse} [\exp (qV_{EBO}/kT) - 1] \alpha_o}{1 - \int_0^{W_A} \beta_{no} dx} \quad (6.8)$$

and

$$M = \frac{1}{1 - \int_0^{W_A} \beta_{no} dx} \quad (6.9)$$

6.2.3 Small-Signal Impedance of the Avalanche Subregion. From Eq. 6.1a, the following expression can be derived:

$$\frac{1}{v_s} \frac{\partial}{\partial t} [J_p(x,t) + J_n(x,t)] = \frac{\partial}{\partial x} [J_p(x,t) - J_n(x,t)] + \frac{\partial}{\partial x} (\beta_p J_p + \beta_n J_n) .$$

If E_a is assumed to be independent of position, a good approximation for the punch-through condition, it can easily be shown that

$$J_{particle} = J_n(x,t) + J_p(x,t) \neq f(x) .$$

If it is assumed that $\beta = \beta_n = \beta_p$ and is integrated across the avalanche subregion, the following relation is obtained:³

$$\tau_A \frac{\partial}{\partial t} J_{\text{particle}}(t) = [J_p(x,t) - J_n(x,t)] \Big|_0^{W_A} + 2J_{\text{particle}} \int_0^W \beta dx, \quad (6.10)$$

where $\tau_A = W_A/v_s$. It has also been assumed that the scattering-limited drift velocities of electrons and holes are equal and are designated by v_s . The following boundary conditions apply under small-signal conditions,

$$J_n(0,t) = \left\{ J_{\text{nsE}} [\exp(qV_{\text{EBO}}/kT) - 1] \alpha_0 + J_{\text{nsc}} \right\} + \left[J_{\text{nsE}} \alpha \frac{\tilde{V}_{\text{EB}}}{kT} e^{qV_{\text{EBO}}/kT} e^{j\omega t} \right]$$

and

$$J_p(W_A,t) = J_{\text{psc}},$$

where α is the RF common-base current amplification factor when there is no avalanche multiplication. If J_s is defined as $J_s = J_{\text{so}} + \tilde{J}_s e^{j\omega t}$,

$$J_{\text{so}} + \tilde{J}_s e^{j\omega t} = \left\{ J_{\text{nsE}} [\exp(qV_{\text{EBO}}/kT) - 1] \alpha_0 + J_{\text{nsc}} + J_{\text{psc}} \right\} + \left[J_{\text{nsE}} \alpha \frac{\tilde{V}_{\text{EB}}}{kT} e^{qV_{\text{EBO}}/kT} e^{j\omega t} \right].$$

Equation 6.10 can be written as

$$\frac{\partial}{\partial t} J_{\text{particle}} = \frac{2J_{\text{particle}}}{\tau_A} \left(\int_0^{W_A} \beta dx - 1 \right) + \frac{2J_{\text{so}}}{\tau_A} + \frac{2\tilde{J}_s e^{j\omega t}}{\tau_A}. \quad (6.11)$$

The RF small-signal current density can easily be derived from Eq. 6.11.

3. Sze, S. M., Physics of Semiconductor Devices, John Wiley and Sons, Inc., New York, 1969, p. 218.

This is done by first making the following definitions:

$$J_{\text{particle}} = J_o + \tilde{J}_A e^{j\omega t},$$

$$J_o = J_{po}(x) + J_{no}(x) \neq f(x) \text{ and}$$

$$\tilde{J}_A = \tilde{J}_{pa}(x) + \tilde{J}_{na}(x) \neq f(x).$$

Substitution of the appropriate relations into Eq. 6.11 gives

$$\frac{\partial}{\partial t} (J_o + \tilde{J}_A e^{j\omega t}) = \frac{2}{\tau_A} (J_o + \tilde{J}_A) [(\bar{\beta} + \bar{\beta}' \tilde{E}_a e^{j\omega t}) W_A - 1] + \frac{2J_{so}}{\tau_A} + \frac{2\tilde{J}_s e^{j\omega t}}{\tau_A},$$

where $\bar{\beta}$ = the average ionization rate and

$\bar{\beta}'$ = the average value of $d\bar{\beta}/dE$.

If the second order term is ignored, the small-signal RF current density is found to be

$$\tilde{J}_A = \frac{\bar{\beta}' W_A \tilde{E}_a J_o + \tilde{J}_s}{(1 - \bar{\beta} W_A) + j \frac{W_A}{2}}, \quad (6.12)$$

where J_A represents the conduction current. There is also a displacement current given by

$$\tilde{J}_D = j\omega \epsilon E_a. \quad (6.13)$$

The total RF current density in the avalanche subregion is

$$\tilde{J}_T = \frac{\bar{\beta}' W_A \tilde{E}_a J_o + \tilde{J}_s}{(1 - \bar{\beta} W_A) + j \frac{W_A}{2}} + j\omega \epsilon \tilde{E}_a. \quad (6.14)$$

The common base-current amplification factor for a CATT device is simply

$$\alpha^* = \frac{\tilde{J}_{na}(W_A)}{\tilde{J}_{na}(-W_B)},$$

where $\tilde{J}_{na}(-W_B)$ is the emitter-base junction injected RF electron-current density and $\tilde{J}_{na}(W_A) = \tilde{J}_A$, since the base-collector junction is reverse biased and the RF hole current density at $x = W_A$ is essentially zero.

Therefore α^* can be written as

$$\alpha^* = \alpha \left[\frac{\bar{\beta}' W_A \tilde{E}_a (J_o / \tilde{J}_s) + 1}{1 - \bar{\beta} W_A + j(\omega \tau_A / 2)} \right]. \quad (6.15)$$

The small-signal admittance of the avalanche subregion can be deduced from Eq. 6.14 directly. It is found to be

$$\begin{aligned} Y_A &\triangleq A \tilde{J}_T / \tilde{V}_A \\ &= \frac{A[\bar{\beta}' J_o + (\tilde{J}_s / \tilde{E}_a W_A)]}{1 - \bar{\beta} W_A + (j\omega \tau_A / 2)} + j\omega C_A, \end{aligned}$$

where \tilde{V}_A = the amplitude of the RF voltage across the avalanche subregion,
 C_A = the capacitance of the avalanche subregion = $\epsilon A / W_A$ and
 A = the device area.

The admittance can be expressed as

$$Y_A = G_A + jB_A, \quad (6.16)$$

where

$$G_A = \frac{A[\bar{\beta}' J_o + (\tilde{J}_s / \tilde{E}_a W_A)](1 - \bar{\beta} W_A)}{(1 - \bar{\beta} W_A)^2 + [(\omega \tau_A)^2 / 4]}$$

and

$$B_A = \omega \left\{ C_A - \frac{\tau_A}{2} \frac{A[\bar{\beta}' J_0 + (\tilde{J}_s / \tilde{E}_a W_A)]}{(1 - \bar{\beta} W_A)^2 + [(\omega \tau_A)^2 / 4]} \right\} .$$

The resonant frequency is found by setting B_A equal to 0. If γ is the ratio between the RF conduction current and the total RF current, then γ can be expressed as

$$\gamma = \frac{\tilde{J}_A}{\tilde{J}_T} = \frac{1}{1 + j\omega \epsilon \tilde{E}_a [1 - \bar{\beta} W_A + (j\omega \tau_A / 2) / (\bar{\beta}' W_A \tilde{E}_a J_0 + \tilde{J}_s)]} . \quad (6.17)$$

For typical CATT oscillators operating under normal conditions $(1 - \bar{\beta} W_A)$ and $\omega \tau_A / 2$ are of comparable magnitude. Therefore the avalanche delay in a CATT device is less than that for an IMPATT diode. The avalanche delay increases as the avalanche multiplication is increased. It is important to note that α^* is directly proportional to $1/(1 - \bar{\beta} W_A)$.

6.2.4 Small-Signal Impedance of the Drift Subregion. When the small-signal expressions are substituted into Eq. 6.1a and it is assumed that there is no avalanche generation occurring anywhere in the drift subregion, the RF equations become

$$j \frac{\omega}{v_s} \tilde{J}_{na}(x) = - \frac{d}{dx} \tilde{J}_{na}(x) , \quad j \frac{\omega}{v_s} \tilde{J}_{pa}(x) = \frac{d}{dx} \tilde{J}_{pa}(x) . \quad (6.18)$$

The small-signal impedance for the drift subregion Z_D is defined as²

$$\tilde{Z}_D = \frac{1}{\tilde{J}_T} \int_{W_A}^{W_A + W_D} \tilde{E} dx . \quad (6.19)$$

By using the relation $\tilde{J}_T = \tilde{J}_P + \tilde{J}_n + j\omega\tilde{E}$, Eq. 6.19 can be written as

$$\tilde{Z}_D = \frac{W_D^2}{A\epsilon v_s} \left(\frac{1}{j\omega\tau_D} \right) + \frac{v_s}{\omega^2\epsilon A} \frac{1}{\tilde{J}_T} \tilde{J}_P(x,t) \begin{vmatrix} W_A+W_D \\ W_A \end{vmatrix} - \frac{v_s}{\omega^2\epsilon A} \frac{1}{\tilde{J}_T} \tilde{J}_n(x,t) \begin{vmatrix} W_A+W_D \\ W_A \end{vmatrix}.$$

In the drift subregion, as mentioned previously, $J_P(x,t)$ is essentially zero. The boundary conditions are

$$\tilde{J}_n(W_A, t) = \tilde{J}_A e^{j\omega t}$$

and

$$\tilde{J}_n(W_A+W_D, t) = \tilde{J}_A e^{j\omega(t-\tau_d)},$$

where $\tau_D = \frac{\Delta}{W_D/v_s}$. When appropriate substitutions are made, the expression obtained for \tilde{Z}_D is

$$\tilde{Z}_D = \frac{1}{\omega C_D} \left[\frac{2|\gamma|}{\theta_D} \sin \left(\frac{\theta_D}{2} - \theta_\gamma \right) \sin \frac{\theta_D}{2} \right] + j \frac{1}{\omega C_D} \left[\frac{2|\gamma|}{\theta_D} \cos \left(\frac{\theta_D}{2} - \theta_\gamma \right) \sin \frac{\theta_D}{2} - 1 \right] \quad (6.20)$$

where $\theta_D = \omega\tau_D$,

$$C_D = \epsilon A/W_D,$$

$$|\gamma| = \frac{1}{\left\{ \left[1 - \frac{\omega^2\epsilon\tilde{E}_a\tau_A}{2(\bar{\beta}'W_A\tilde{E}_aJ_o + \tilde{J}_s)} \right]^2 + \frac{[\omega\epsilon\tilde{E}_a(1-\bar{\beta}W_A)]^2}{[\bar{\beta}'W_A\tilde{E}_aJ_o + \tilde{J}_s]} \right\}^{1/2}}$$

and

$$\theta_\gamma = -\tan^{-1} \left[\frac{\omega\epsilon\tilde{E}_a(1-\bar{\beta}W_A)/(\bar{\beta}'W_A\tilde{E}_aJ_o + \tilde{J}_s)}{1 - \frac{\omega^2\epsilon\tilde{E}_a\tau_A}{2(\bar{\beta}'W_A\tilde{E}_aJ_o + \tilde{J}_s)}} \right].$$

6.3 A Simplified Emitter-Coupled CATT Oscillator.

6.3.1 A Simple Model. For the analysis of the emitter-coupled oscillators,⁴ the model shown in Fig. 6.2 was adopted. The collector region is represented by a parallel combination of a collector capacitance C_C and a current source $\alpha^{**}\tilde{i}_E$,

where $C_C = \text{the collector junction capacitance} = \epsilon A / (W_A + W_D)$,

$$\alpha^{**} = \alpha^* e^{-j\omega W_D / 2v_s},$$

$R_C = \text{the bulk resistance associated with the collector region,}$

$R_B = \text{the bulk resistance associated with the base region,}$

$C_E = \text{the capacitance of the emitter junction and}$

$\tilde{i}_E = \text{the RF current injected at the emitter-base junction.}$

The factor α^* takes care of the avalanche multiplication and the avalanche delay. The exponential term $\exp(j\omega W_D / 2v_s)$ takes care of the transit-time effect.

6.3.2 Optimization of the Emitter-Coupled CATT Oscillator.

The conditions for oscillation are given by

$$G_L + \text{Re}(Y) = 0$$

and

$$-B_L + \text{Im}(Y) = 0, \quad (6.21)$$

where Y is the admittance of the CATT oscillator at the 1-1' terminal shown in Fig. 6.3a. G_L and B_L are the load conductance and susceptance,

4. Toussaint, H. N., "Zur Bemessung de emittergekoppelten Oszillators," Frequenz, vol. 21, pp. 193, 1967.

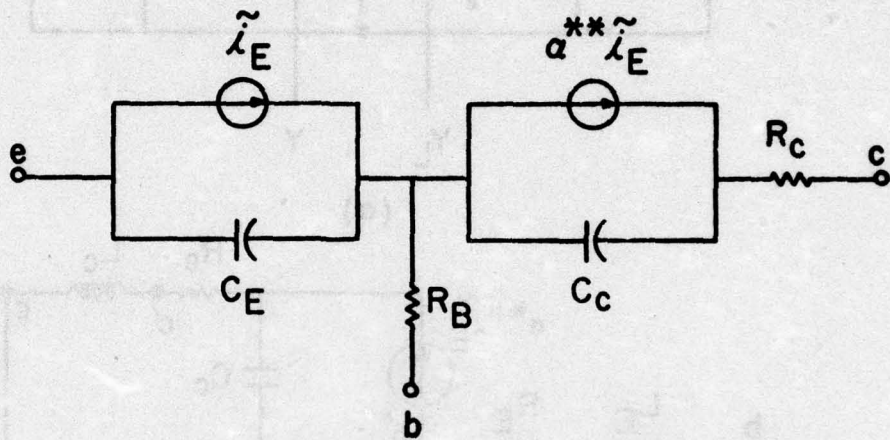


FIG. 6.2 A SIMPLE MODEL OF A CATT DEVICE.

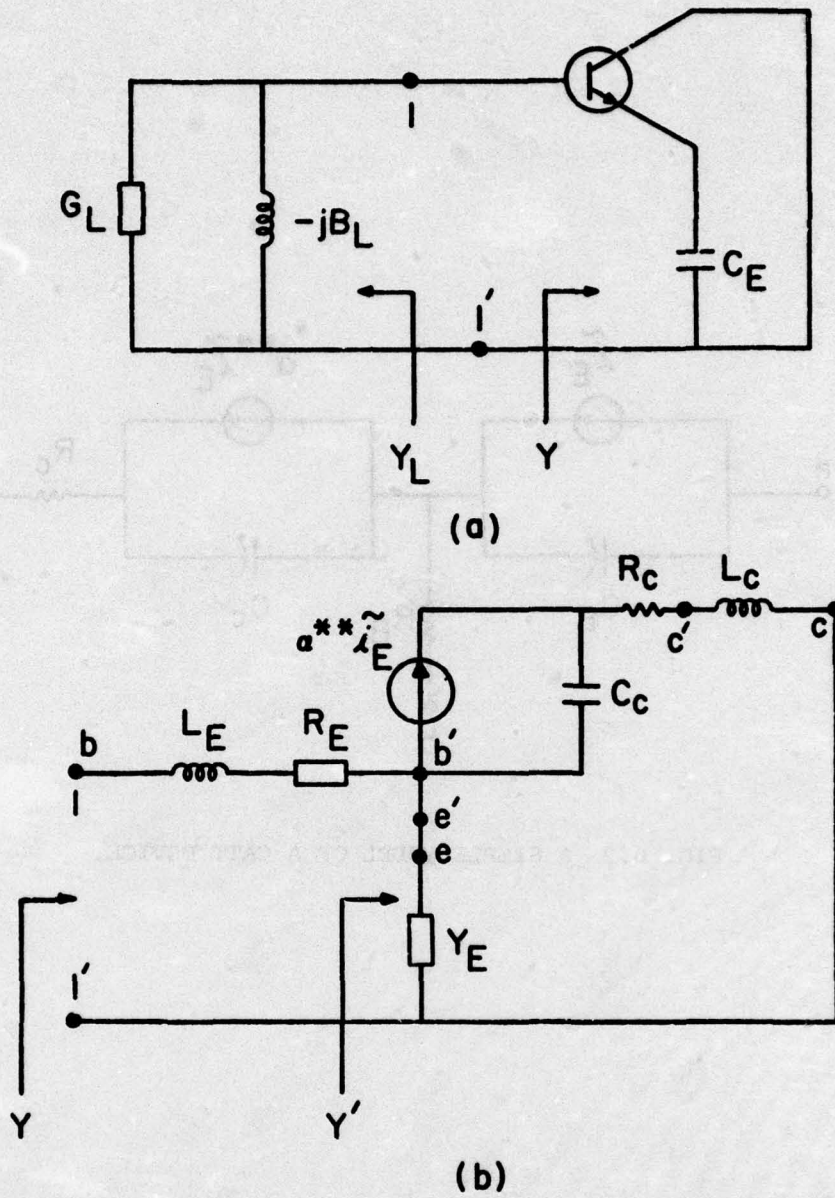


FIG. 6.3 (a) EMITTER-COUPLED CATT OSCILLATOR. (b) HIGH FREQUENCY EQUIVALENT CIRCUIT.

respectively. It is implied by the introduction of the admittance Y that a negative conductance exists between the collector and the inner base connection. In order to calculate Y , the high-frequency equivalent circuit shown in Fig. 6.3b is chosen. This equivalent circuit is simple enough to allow development of analytical expressions. The following additional symbols are used in the following analysis:

Y_E = the external admittance between the emitter and collector,

L_C = the collector lead inductance,

L_B = the base lead inductance and

Y_L = the load admittance.

The collector pn junction between the points b' and c' is represented by the collector capacitance C_C in parallel with the current source $\alpha^{**}\tilde{i}_E$ followed by a series resistance R_C . The emitter pn junction between points b' and c' is represented by a short circuit since it is assumed that the impedance of the emitter pn junction is much smaller than the external impedance $Z_E = 1/Y_E$. Neglecting the emitter impedance implies that no element of this circuit shown in Fig. 6.3b has strong operating point dependence. Thus the following analysis is not limited to small signals.

By elementary circuit analysis, the following expressions can be obtained:

$$Y' = \frac{\left[1 - \alpha^{**} - \left(\frac{\omega}{\omega_0} \right)^2 + j\omega C_C R_C \right] Y_E + j\omega C_C}{1 - \left(\frac{\omega}{\omega_0} \right)^2 + j\omega C_C R_C} \quad (6.22)$$

and

$$Y = \frac{1}{R_B + j\omega L_B + (1/Y')} \quad (6.23)$$

where $\omega_o = 1/\sqrt{L_C C_C}$. There are infinite combinations of Y_E and Y_L which would satisfy the oscillation condition as given by Eq. 6.21. However, there are optimum values of Y_E and Y_L where optimum power extraction can be achieved. This will be shown later. It is useful to redraw the circuit in Fig. 6.3 as shown in Fig. 6.4. The oscillator consists of an ideal amplifier which has feedback and is denoted by the complex current amplification factor $\alpha^{**} = \tilde{i}_2/\tilde{i}_1$. As a result of the feedback, the ideal amplifier can be replaced by the admittance $Y_N = -\tilde{i}_2/\tilde{V}_2 = -G_N - jB_N$. From the oscillation conditions, Y_B and Y_P can be expressed as

$$Y_B = - \left[\frac{Y_E \left(1 - \alpha^{**} - \frac{\omega^2}{\omega_o^2} + j\omega R_C C_C \right) + \frac{-\frac{\omega^2}{\omega_o^2} + j\omega R_C C_C}{R_C + j\omega L_C}}{1 + \frac{\omega^2}{\omega_o^2} + j\omega R_C C_C} \right] \quad (6.24)$$

and

$$Y_P = \frac{\alpha^{**} \left[1 - \frac{\omega^2}{\omega_o^2} + j\omega C_C R_C \right] Y_E}{1 + (R_C + j\omega L_C) (\alpha^{**} Y_E)} \quad (6.25)$$

In the case of oscillation, $Y_N + Y_P = 0$. Due to out-of-phase feedback, Y_N has a nonzero imaginary part and only a portion of the active collector current is usable for producing useful power while the other part results in power loss. This results in the following relations:

$$|\tilde{i}_2| = \sqrt{\tilde{i}_b^2 + \tilde{i}_w^2} \quad (6.26)$$

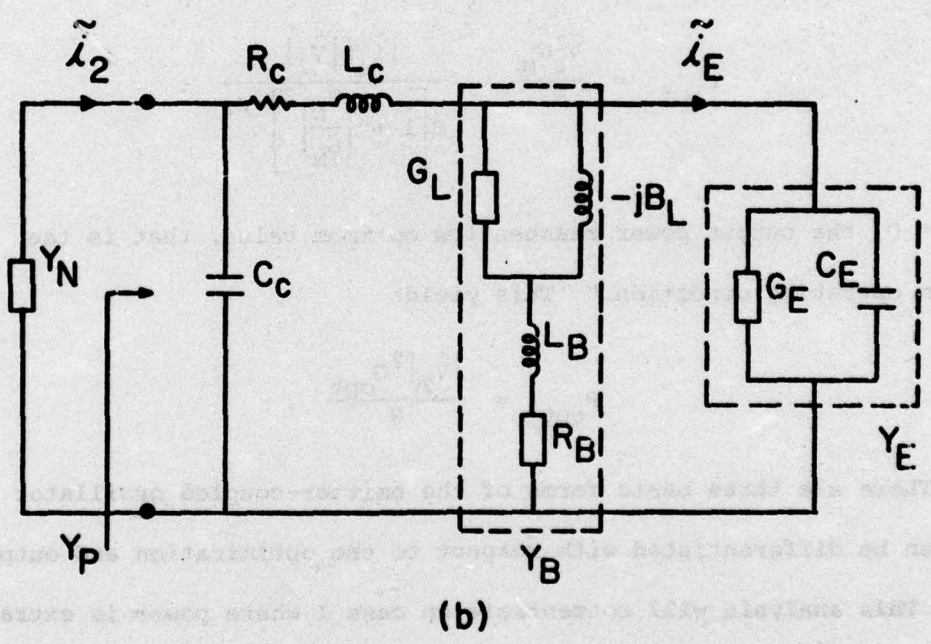
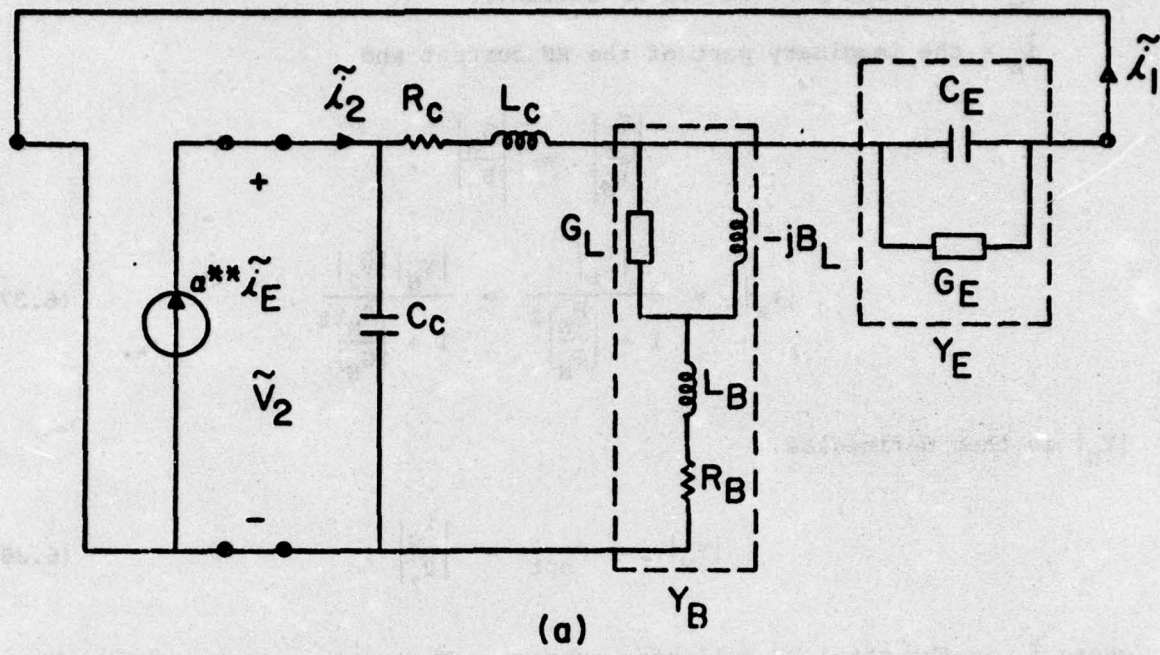


FIG. 6.4 (a) EQUIVALENT CIRCUIT OF EMITTER-COUPLED CATT OSCILLATOR.
 (b) THE IDEAL AMPLIFIER IS REPLACED BY Y_N .

where \tilde{i}_w = the real part of the RF current,

\tilde{i}_b = the imaginary part of the RF current and

$$\left| \frac{\tilde{i}_w}{\tilde{i}_b} \right| = \left| \frac{G_N}{B_N} \right| ,$$

$$|\tilde{i}_w| = \frac{|\tilde{i}_2|}{1 + \left(\frac{B_N}{G_N}\right)^2} = \frac{|y_N| |\tilde{v}_2|}{1 + \left(\frac{B_N}{G_N}\right)^2} . \quad (6.27)$$

$|y_N|$ is then defined as

$$|y_N| = G_{opt} = \left| \frac{i_c}{\tilde{v}_2} \right| , \quad (6.28)$$

where \tilde{i}_c is the total RF collector current. The power output is given by

$$P_{out} = \frac{\tilde{v}_2^2 G_N}{8} = \frac{|\tilde{i}_c| |\tilde{v}_2|}{8 \left[1 + \left(\frac{B_N}{G_N}\right)^2 \right]^{1/2}} . \quad (6.29)$$

For $\tilde{i}_b = 0$, the output power reaches its optimum value, that is the "optimum operating condition." This yields

$$P_{opt} = \frac{|\tilde{v}_2|^2 G_{opt}}{8} . \quad (6.30)$$

There are three basic forms of the emitter-coupled oscillator which can be differentiated with respect to the optimization and output power. This analysis will concentrate on case I where power is extracted from the base circuit only. For this case $Y_E = j\omega C_E$ and $Y_B = G_B - jB_B$. With $L_C = 0$, Eqs. 6.24 and 6.25 reduce to

$$Y_B = - \frac{j\omega C_E (1 - \alpha^{**} + j\omega R_C C_C) + j\omega C_C}{1 + j\omega R_C C_C} \quad (6.31)$$

and

$$Y_P = \frac{\alpha^{**}(1 + j\omega C_C R_C)j\omega C_E}{1 + \alpha^{**}R_C(j\omega C_E)} \quad (6.32)$$

By using Eqs. 6.32 and 6.28, the following is obtained for G_B and B_B :

$$G_B - jB_B = \frac{\omega^2 R_C C_C C_E + j\omega[(\alpha^{**} - 1)C_E - C_C]}{1 + j\omega R_C C_C} \quad (6.33)$$

If it is assumed that $\omega R_C C_C \ll 1$ and α^{**} is defined as $\alpha_1^{**} - j\alpha_2^{**}$, Eq.

6.33 reduces to

$$G_B \approx \omega C_E (\omega R_C C_C + \alpha_2^{**})$$

and

$$B_B \approx \omega[(1 - \alpha_1^{**})C_E + C_C] \quad (6.34)$$

The required G_B and B_B can be found once the appropriate C_E is known. In order to find the desired C_E , it is necessary to set

$$\begin{aligned} G_{opt} &= |Y_P| \\ &= \omega C_E \left| \frac{(\alpha_1^{**} + \omega C_C R_C \alpha_2^{**}) + j(\alpha_1^{**}\omega C_C R_C - \alpha_2^{**})}{(1 + \alpha_2^{**}R_C \omega C_E) + j(R_C \omega C_E \alpha_1^{**})} \right| \end{aligned}$$

It follows that

$$C_E^2 \left[\omega^2 (\alpha_1^{**2} + \alpha_2^{**2}) \left(R_C^2 - \frac{1}{G_{opt}^2} \right) \right] + C_E (2\omega \alpha_2^{**} R_C) + 1 = 0 \quad (6.36)$$

Equation 6.36 is a quadratic equation and can be easily solved to find the desired C_E .

A CATT device with the doping profile shown in Fig. 6.5 was considered and its equivalent circuit parameters calculated. A program was written and some of the results are plotted in Figs. 6.6 through 6.8.

The emitter-coupled CATT oscillator parameters are as follows:

$$A = 4.5 \times 10^{-4} \text{ cm ,}$$

$$D_{nB} = \text{the electron diffusion constant in the base region} = 13 \text{ cm}^2/\text{s},$$

$$\tau_{nB} = \text{the lifetime of the electron in the base} = 10^{-7} \text{ s},$$

$$= \text{the diffusion length of the electron} = 20 \text{ } \mu\text{m},$$

$$W_B = \text{the base width} = 0.5 \text{ } \mu\text{m},$$

$$W_A = \text{The avalanche zone width} = 5 \text{ } \mu\text{m},$$

$$W_D = \text{the drift zone width} = 18 \text{ } \mu\text{m},$$

$$v_s = \text{the scattering limited drift velocity} = 10^7 \text{ cm/s},$$

$$R_C = 0.5 \text{ } \Omega,$$

$$R_B = 0.37 \text{ } \Omega,$$

$$C_C = 0.021 \text{ } \Omega,$$

$$L_C = 0 \text{ nh},$$

$$L_B = 3 \text{ nh},$$

$$V_{CBO} = \text{the dc base-collector bias voltage, } 114 \text{ V, } M = 5; 132 \text{ V,}$$

$$M = 10 \text{ and } 148 \text{ V, } M = 20.$$

The following are defined for convenience:

$$R_1 = \frac{G_B}{G_{opt}} = \frac{\omega C_E (\omega R_C C_C + \alpha_2^*)}{G_{opt}}, \quad (6.37)$$

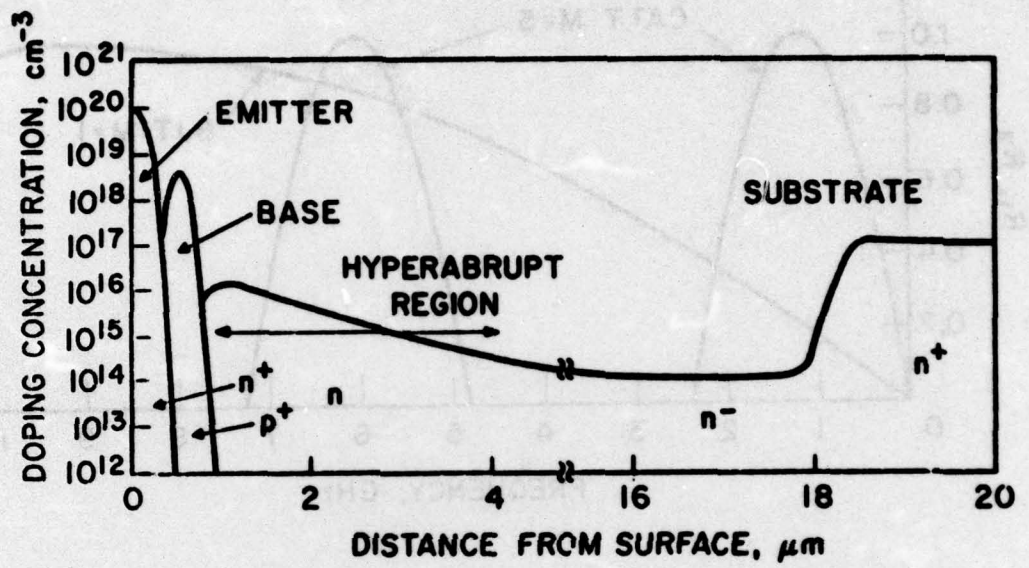


FIG. 6.5 DOPING PROFILE OF A CATT DEVICE.

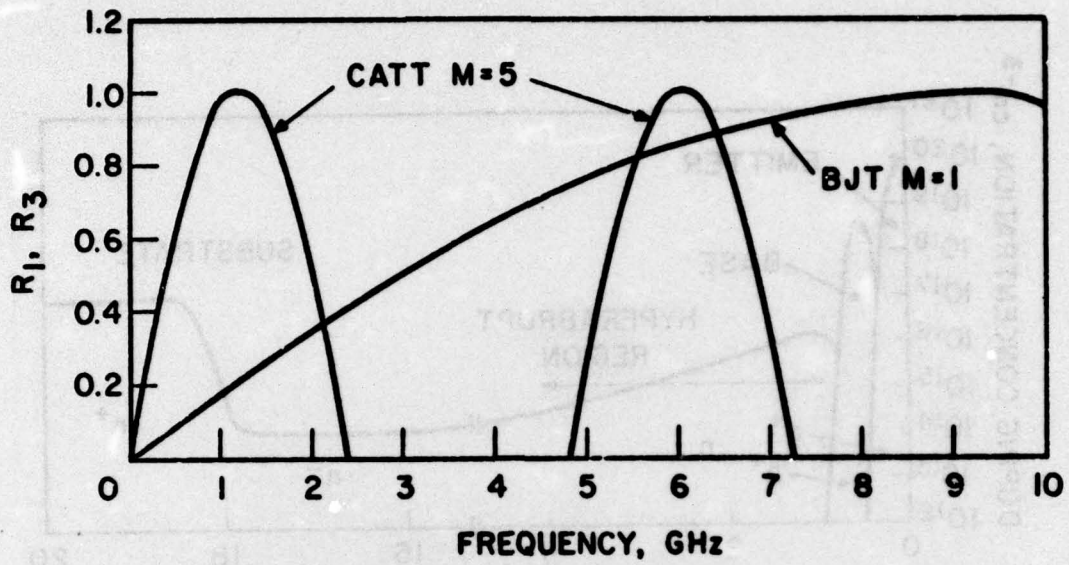


FIG. 6.6 R_1 AND R_3 VS. FREQUENCY.

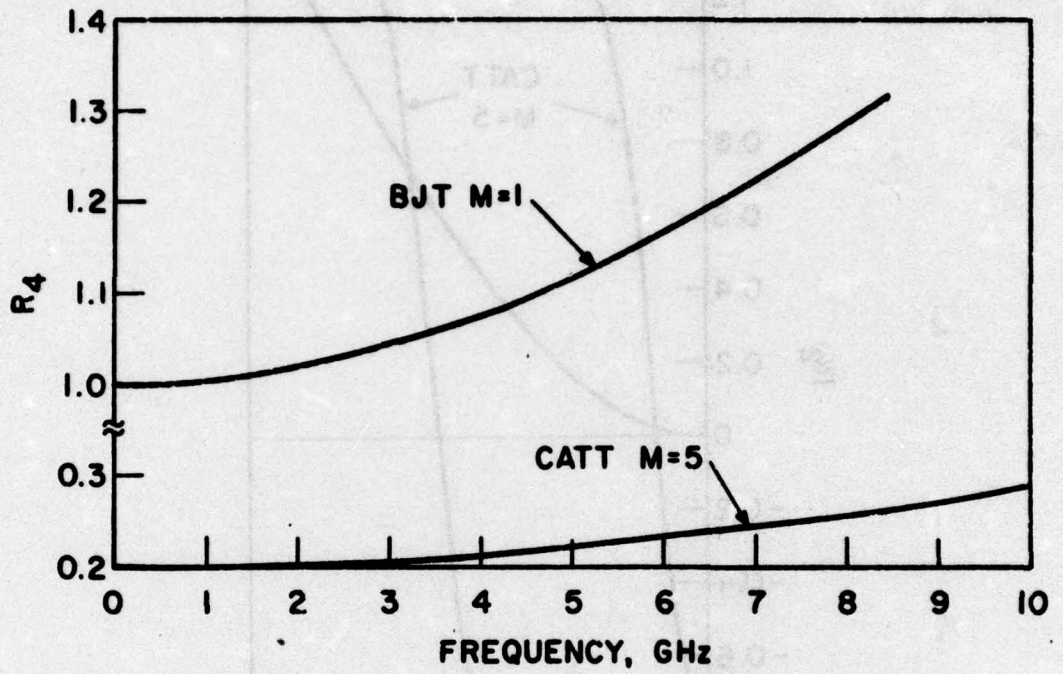


FIG. 6.7 R_4 VS. FREQUENCY.

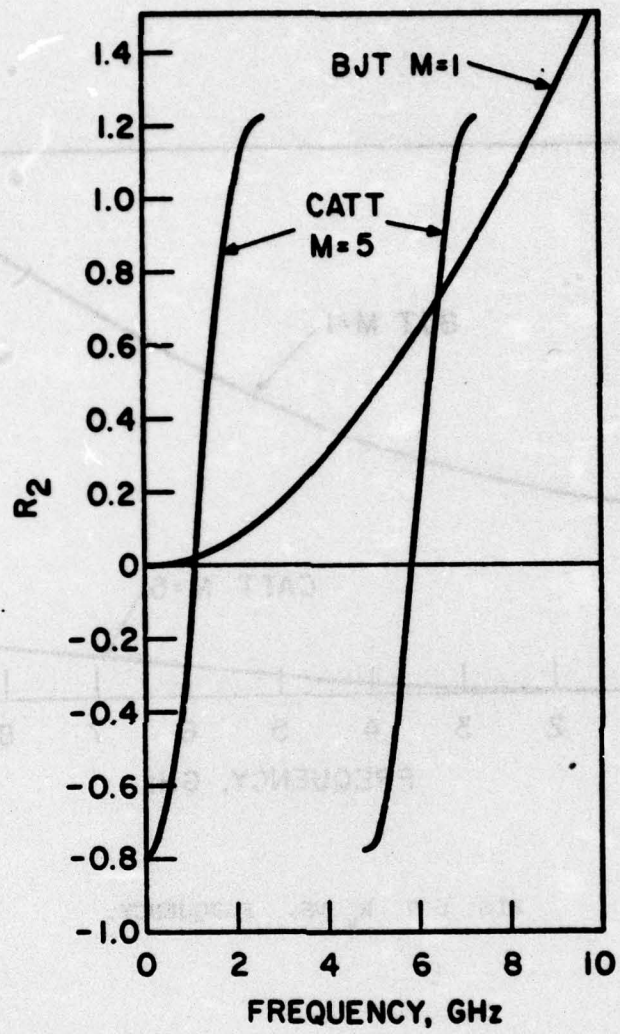


FIG. 6.8 R_2 VS. FREQUENCY.

$$R_2 = \frac{B'_B}{G_{opt}} = \frac{B_B - \omega C_C}{G_{opt}} = \frac{w(1 - \alpha_1^{**})C_E}{G_{opt}}, \quad (6.38)$$

$$R_3 = \frac{P_B}{P_{B_{opt}}} = \frac{G_B}{G_{opt}} = R_1 \quad (6.39)$$

and

$$R_4 = \frac{\omega C_E}{G_{opt}}. \quad (6.40)$$

6.4 Conclusion. Analytical expressions were developed which can be used to calculate the avalanche multiplication factor, the avalanche delay, the electron-carrier and hole-carrier current densities in the avalanche subregion and the small-signal impedance of the collector region. Numerical analysis is required and the computer program is in the process of being developed. The extremely simplified analysis of the emitter-coupled CATT oscillator indicates the existence of negative conductance $[Re(Y')]$ in bands of frequency 2.4 GHz wide. The output power level of the CATT device is higher than that of a BJT of comparable configuration by an order of magnitude.

7. General Conclusions. (N. A. Masnari)

The work on this program has involved the investigation of various devices for the generation and amplification of microwave energy. The devices have included avalanche transit-time devices (e.g., IMPATTs, TRAPATTs, CATTs, etc.) as well as FET structures. In addition to the detailed-theoretical investigations which have been carried out, the

program has also involved the fabrication and experimental evaluation of various devices. The achievements have been spelled out in the various progress reports issued quarterly during the lifetime of the contract. In addition, specific projects which resulted in PhD dissertations are described in detail in those dissertations; these also appeared as technical reports as itemized earlier.

