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MULTIPURPOSE DIGITAL MICROPROCESSOR EMULATOR.(U)

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TECHNICAL REPORT RG-76-62

**MULTIPURPOSE DIGITAL MICROPROCESSOR  
EMULATOR**

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11 May 1976

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## 1. Introduction and Background

This report describes an emulator designed and implemented to support the initial software development effort for a multipurpose digital microprocessor, and which also is to provide a vehicle for experimenting with hardware and software architectural changes proposed for the microprocessor. The initial test-bed application for the microprocessor is to be the guidance control computer in the T-6 missile. The flight control software will be developed utilizing this emulator.

The emulator is written in a variation of FORTRAN allowing the use of "structured" statements, including: IF...THEN...ELSE...; DO UNTIL (...)...; DO WHILE (...)...; and IF...THEN...OR IF...THEN...ELSE... This program is first run through a preprocessor which translates the statements into standard FORTRAN, providing the capability to run the emulator on any host computer which has a standard FORTRAN compiler available. The utilization of the emulator for the T-6 missile flight control software development is to be on the Missile Computer Software and Hardware Center's Raytheon R-520 and the MICOM CDC 6600 computers.

The design objectives of the emulator were to support the immediate software development effort for the T-6 missile application of the microprocessor, while retaining as much flexibility for proposed-change evaluation as possible. To support the software development effort, it was essential that the emulator perform exactly as though it were the microprocessor hardware executing microinstructions. Both considerations, fidelity of microinstruction execution and ease of change, supported the position that the emulator should be highly modular. Additional considerations which influenced the emulator design include: ease of set-up and operation; varying levels of detailed output available optionally to support different types of runs; and maximum portability to allow the emulator to run on other host computers. A single run control card was designed to define the desired characteristics of each run, and provides the mechanisms for specifying simulated memory preset values, output options, and run termination conditions (other than errors). For portability, the host-computer-dependent portions of the program were minimized and isolated for simplified conversion to other host computers.

The remainder of this report describes the specific requirements and the specific programming techniques used to meet the requirements, plus a description of some potential extensions to or generalizations from the current design. Since early applications software design and experimentation are often crucial during computer hardware definition and design, it is believed that the concepts provided here can provide an extremely useful tool in the continuing application of microprocessors to weapons control systems.

## 2. Microprocessor Hardware Organization

From the viewpoint of software, the microprocessor\* consists of a 16-bit (reconfigurable up or down in 4-bit increments) arithmetic logic unit (ALU) with a 16-word random access memory (scratchpad), a 32-operation instruction set, expandable to 58 operations by interpretation of a carry-control bit, and further expandable by a 3-bit instruction modifier (Figures 1 and 2). There are two associated memories: 1024 - 16-bit words of main memory; and 1024 - 48-bit words of control memory. Normal execution of a macroinstruction begins with the decoding of the main memory word pointed to by the first word in the scratchpad (software program counter - PC) into two 8-bit addresses. The leftmost eight bits are placed in the control memory address register (H-register), and the rightmost eight bits are placed in the main memory address register (C-register). Both the H- and C-registers are 10 bits in length: The C-register is wired such that this decoding operation causes the two high-order bits to be on, so that the references to main memory following the decode will be offset by 1400 octal. The top two bits of the H-register can be controlled from the execution of a microinstruction.

The 48-bit control memory words (microinstructions) are broken into 25 distinct fields (Table 1). Six of the fields are encoded, and the remaining 19 are considered as discrete control bits. Eighteen of these control bits are now functionally assigned, but additional control functions could be implemented if required by grouping some of the functions under additional encoded fields; i.e., where three bits are now three functions, three bits encoded could be used to control eight functions. Current encoded fields consist of: the 5-bit operation code, a 3-bit modifier code, two 4-bit operands (scratchpad addresses), a 10-bit next control word (H-register) field, and a 3-bit analog/digital (A/D) multiplexer address field.

Macroinstruction execution proceeds by decoding the control memory word pointed to by the H-register after a main-memory decode. The design of the hardware is such that some of the control functions specified by discrete bits are performed first. Then the operation code is executed, followed by the disposition of the result as directed by the instruction modifier, and the functions of the remaining discrete control bits are performed. One of the control bits is used to enable the loading of the H-register from the 10-bit next-H field. Thus, the microinstructions comprising a macrooperation are linked. The last microinstruction of a macrosequence will contain the address of a microinstruction which initiates the next decode of a main memory word through the PC, and then increments the PC by one. Therefore, the main memory control program will be sequential, unless modified by a reload of the PC.

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\*Monolithic memories 5701/6701 microprocessor.



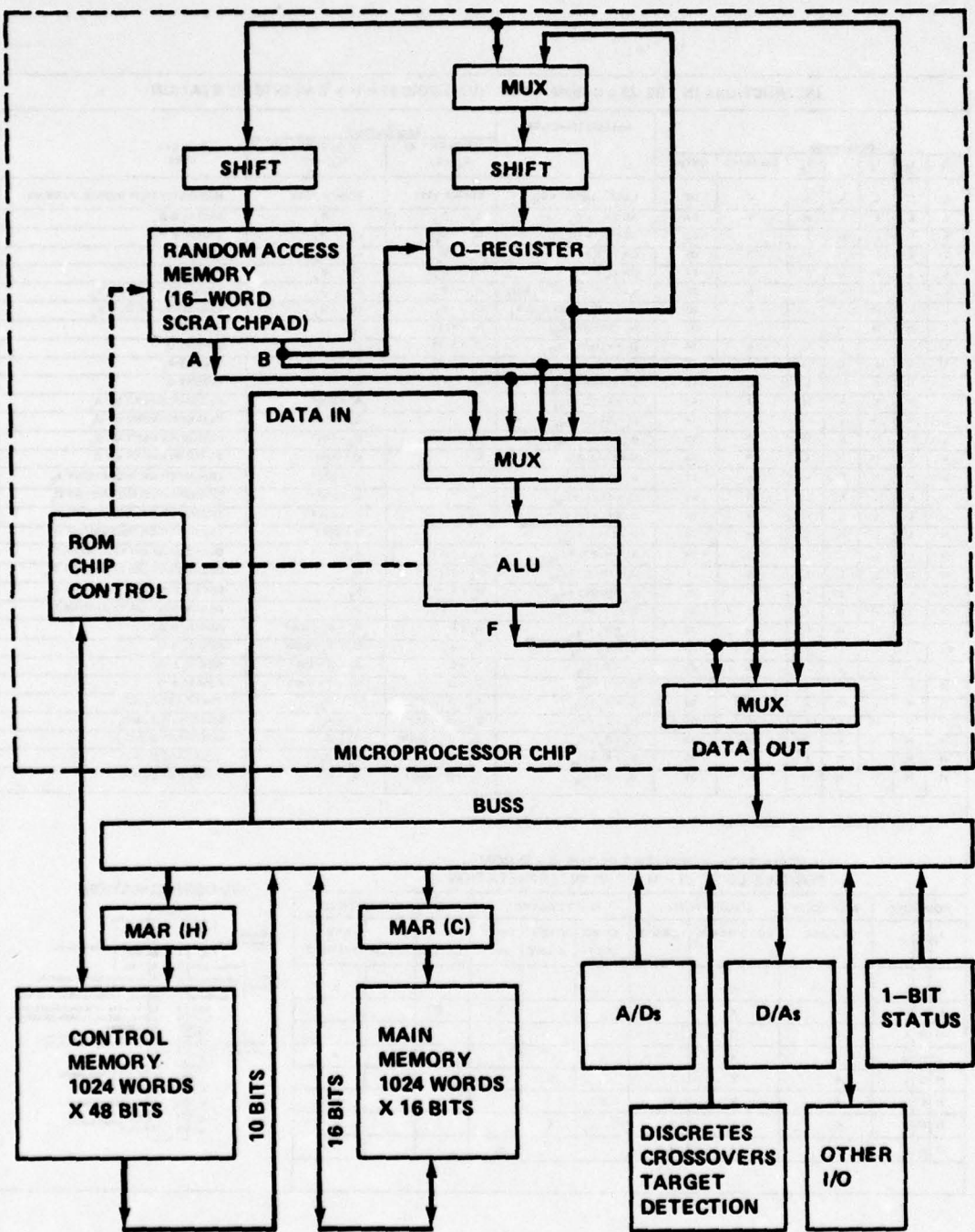


Figure 1. Multi-purpose digital microprocessor simplified block diagram.

INSTRUCTIONS IN THE 32 x 9 ROM - POSITIVE LOGIC (1 = H ≈ 3 V) INTERPRETATION										
ROM WORD					ALU INSTRUCTION		ALU OUTPUT			TYPICAL USES
I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	DECIMAL	OCTAL	NO CARRY IN (C <sub>N</sub> = L)	WITH CARRY IN (C <sub>N</sub> = H)		
L	L	L	L	L	0	00	LLLL + HHHH + C <sub>N</sub>	FORCE 1111	FORCE 0000	INITIALIZATION (FORCE 1's OR 0's)
L	L	L	L	H	1	01	AND A <sub>1</sub> & B <sub>1</sub>	A <sub>1</sub> B <sub>1</sub>	A <sub>1</sub> B <sub>1</sub>	AND A <sub>1</sub> & B <sub>1</sub>
L	L	L	H	L	2	02	AND D <sub>1</sub> & B <sub>1</sub>	D <sub>1</sub> B <sub>1</sub>	D <sub>1</sub> B <sub>1</sub>	AND D <sub>1</sub> & B <sub>1</sub>
L	L	L	H	H	3	03	OR A <sub>1</sub> & B <sub>1</sub>	A <sub>1</sub> B <sub>1</sub>	A <sub>1</sub> B <sub>1</sub>	OR A <sub>1</sub> & B <sub>1</sub>
L	L	H	L	L	4	04	OR D <sub>1</sub> & B <sub>1</sub>	D <sub>1</sub> B <sub>1</sub>	D <sub>1</sub> B <sub>1</sub>	OR D <sub>1</sub> & B <sub>1</sub>
L	L	H	L	H	5	05	EXCLUSIVE OR A <sub>1</sub> & B <sub>1</sub>	A <sub>1</sub> B <sub>1</sub>	A <sub>1</sub> B <sub>1</sub>	EXCLUSIVE OR A <sub>1</sub> & B <sub>1</sub>
L	L	H	H	L	6	06	EXCLUSIVE OR D <sub>1</sub> & B <sub>1</sub>	D <sub>1</sub> B <sub>1</sub>	D <sub>1</sub> B <sub>1</sub>	EXCLUSIVE OR D <sub>1</sub> & B <sub>1</sub>
L	L	H	H	H	7	07	A <sub>1</sub> + HHHH + C <sub>N</sub>	A <sub>1</sub> + 1111	A <sub>1</sub>	INVERT A <sub>1</sub>
L	H	L	L	L	8	10	D <sub>1</sub> + HHHH + C <sub>N</sub>	D <sub>1</sub> + 1111	D <sub>1</sub>	INVERT D <sub>1</sub>
L	H	L	L	H	9	11	B <sub>1</sub> + HHHH + C <sub>N</sub>	B <sub>1</sub> + 1111	B <sub>1</sub>	INVERT B <sub>1</sub>
L	H	L	H	L	10	12	Q + HHHH + C <sub>N</sub>	Q + 1111	Q	INVERT Q
L	H	L	H	H	11	13	A <sub>1</sub> + LLLL + C <sub>N</sub>	A <sub>1</sub>	A <sub>1</sub> + 0001	2's COMPLEMENT OF A <sub>1</sub>
L	H	H	L	L	12	14	D <sub>1</sub> + LLLL + C <sub>N</sub>	D <sub>1</sub>	D <sub>1</sub> + 0001	2's COMPLEMENT OF D <sub>1</sub>
L	H	H	L	H	13	15	B <sub>1</sub> + LLLL + C <sub>N</sub>	B <sub>1</sub>	B <sub>1</sub> + 0001	2's COMPLEMENT OF B <sub>1</sub>
L	H	H	H	L	14	16	Q + LLLL + C <sub>N</sub>	Q	Q + 0001	2's COMPLEMENT OF Q
L	H	H	H	H	15	17	A <sub>1</sub> + LLLL + C <sub>N</sub>	A <sub>1</sub>	A <sub>1</sub> + 0001	TRANSFER OR INCREMENT A <sub>1</sub>
H	L	L	L	L	16	20	D <sub>1</sub> + LLLL + C <sub>N</sub>	D <sub>1</sub>	D <sub>1</sub> + 0001	TRANSFER OR INCREMENT D <sub>1</sub>
H	L	L	L	H	17	21	B <sub>1</sub> + LLLL + C <sub>N</sub>	B <sub>1</sub>	B <sub>1</sub> + 0001	TRANSFER OR INCREMENT B <sub>1</sub>
H	L	L	H	L	18	22	Q + LLLL + C <sub>N</sub>	Q	Q + 0001	TRANSFER OR INCREMENT Q
H	L	L	H	H	19	23	A <sub>1</sub> + HHHH + C <sub>N</sub>	A <sub>1</sub> + 1111	A <sub>1</sub>	DECREMENT OR TRANSFER A <sub>1</sub>
H	H	L	L	L	20	24	D <sub>1</sub> + HHHH + C <sub>N</sub>	D <sub>1</sub> + 1111	D <sub>1</sub>	DECREMENT OR TRANSFER D <sub>1</sub>
H	H	L	L	H	21	25	B <sub>1</sub> + HHHH + C <sub>N</sub>	B <sub>1</sub> + 1111	B <sub>1</sub>	DECREMENT OR TRANSFER B <sub>1</sub>
H	L	H	H	L	22	26	Q + HHHH + C <sub>N</sub>	Q + 1111	Q	DECREMENT OR TRANSFER Q
H	L	H	H	H	23	27	A <sub>1</sub> + B <sub>1</sub> + C <sub>N</sub>	A <sub>1</sub> + B <sub>1</sub>	A <sub>1</sub> + B <sub>1</sub> + 0001	ADD A <sub>1</sub> & B <sub>1</sub>
H	H	L	L	L	24	30	D <sub>1</sub> + B <sub>1</sub> + C <sub>N</sub>	D <sub>1</sub> + B <sub>1</sub>	D <sub>1</sub> + B <sub>1</sub> + 0001	ADD D <sub>1</sub> & B <sub>1</sub>
H	H	L	L	H	25	31	A <sub>1</sub> + Q + C <sub>N</sub>	A <sub>1</sub> + Q	A <sub>1</sub> + Q + 0001	ADD A <sub>1</sub> & Q
H	H	L	H	L	26	32	D <sub>1</sub> + Q + C <sub>N</sub>	D <sub>1</sub> + Q	D <sub>1</sub> + Q + 0001	ADD D <sub>1</sub> & Q
H	H	L	H	H	27	33	A <sub>1</sub> + B <sub>1</sub> + C <sub>N</sub>	A <sub>1</sub> - B <sub>1</sub> - 0001	A <sub>1</sub> - B <sub>1</sub>	SUBTRACT A <sub>1</sub> & B <sub>1</sub>
H	H	H	L	L	28	34	B <sub>1</sub> + A <sub>1</sub> + C <sub>N</sub>	B <sub>1</sub> - A <sub>1</sub> - 0001	B <sub>1</sub> - A <sub>1</sub>	SUBTRACT B <sub>1</sub> & A <sub>1</sub>
H	H	H	L	H	29	35	D <sub>1</sub> + B <sub>1</sub> + C <sub>N</sub>	D <sub>1</sub> - B <sub>1</sub> - 0001	D <sub>1</sub> - B <sub>1</sub>	SUBTRACT D <sub>1</sub> & B <sub>1</sub>
H	H	H	H	L	30	36	B <sub>1</sub> + D <sub>1</sub> + C <sub>N</sub>	B <sub>1</sub> - D <sub>1</sub> - 0001	B <sub>1</sub> - D <sub>1</sub>	SUBTRACT B <sub>1</sub> & D <sub>1</sub>
H	H	H	H	H	31	37	D <sub>1</sub> + Q + C <sub>N</sub>	D <sub>1</sub> - Q - 0001	D <sub>1</sub> - Q	SUBTRACT D <sub>1</sub> & Q

A<sub>1</sub>: FIRST OPERAND; B<sub>1</sub>: SECOND OPERAND; D<sub>1</sub>: DATA IN; Q: 16-BIT Q REGISTER

INSTRUCTION MODIFIERS IN THE 8 x 8 ROM - POSITIVE LOGIC (1 = H ≈ 3 V) INTERPRETATION											
ROM WORD	ROM WORD	LOAD CONTROL	SHIFT CONTROL			DATA OUT CONTROL					
I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	DECIMAL	LOAD RAM B <sub>1</sub>	LOAD Q	SHIFT LEFT	SHIFT RIGHT	DON'T SHIFT	A LATCH	B LATCH	ALU OUTPUT F
L	L	L	0	X				X			X
L	L	H	1	X				X	X		
L	H	L	2	X				X		X	
L	H	H	3	X		X					X
H	L	L	4	X			X				X
H	L	H	5	X	X	X					X
H	H	L	6	X	X		X				X
H	H	H	7		X			X			X

**PIN CONFIGURATION**

Figure 2. Multipurpose microprocessor instruction set.

TABLE 1. MULTIPURPOSE MICROPROCESSOR INSTRUCTION FORMAT

Bit Positions			Field Length	Field Name/Control Function			
Field	Decimal	Octal					
1	0-4	0-4	5	Instruction Code			
2	5-7	5-7	3	Instruction modifier			
3	8-11	10-13	4	Operand A (scratchpad address)			
4	12-15	14-17	4	Operand B (scratchpad address)			
5	16-25	20-31	10	Next H address			
25	45-57	55-57	3	A/D multiplexor address			
Discrete Control Bits: (Action if Bit = 1)							
6	26	32	1	SR1 = 0			
7	27	33	1	SR2 = SR1			
8	28	34	1	H Reg = CM addr			
9	29	35	1	Main (C) = Buss			
10	30	36	1	Buss = Main (C)			
11	31	37	1	Buss = ALU data out			
12	32	40	1	Fetch enable			
13	33	41	1	Data in = Input discrettes or micad (KAD)			
14	34	42	1	SR1 = 1 if 4 data out = All 0's			
15	35	43	1	LSB of buss = SR1			
16	36	44	1	LSB of H = SR2			
17	37	45	1	Carry (CN) = 1			
18	38	46	1	Telemetry = Buss			
19	39	47	1	C = Buss			
20	40	50	1	Select D/A 1 and clock			
21	41	51	1	Select D/A 2 and clock			
22	42	52	1	Select D/A 3 and clock			
23	43	53	1	Clock A/D mux addr register			
24	44	54	1	Clock A/D conversion start (per bit)			
Control Memory							
Word Format:							
Bit:	0	5	8	12	16	26	45
Field Number	1	2	3	4	5	6 thru 24	25

### 3. Emulator Control Structure

The emulator, as now structured, consists of a main program and 25 subprograms which are used for initialization and run control; instruction and control-function simulation, diagnostic and statistical output, and the provision of machine-dependent (Raytheon 520) direct code support. It was also determined to be necessary to provide FORTRAN masking and shifting operations for bit access and manipulation. An exclusive OR function has also been added to the function library of the R-520. These direct code and FORTRAN extensions tend to reduce the portability of the system, but they were minimized and simplified so that the effort required to duplicate these capabilities on another host computer can be minimal.

All microprocessor memory, registers, and data paths are represented by FORTRAN COMMON variable names in order to minimize parameter passing in calling sequences. The organization of the R-520 computer is such that REAL FORTRAN variables are represented internally by 48 bits, and integers have 24-bit representation. Thus, a microprocessor control memory word is represented by a real variable name (CNTMEN), and all other microprocessor entities are represented by integer variables. The implicit variable-type identifiers of standard FORTRAN are used exclusively, while at the same time maintaining at least an abbreviation of the name of the elements, preceded where necessary by an integer-type letter (I through N). For example, the two 1-bit registers, SR1 and SR2, are identified in the emulation program as MSR1 and MSR2.

The main program reads the run control card (Table 2) and proceeds to step through all the run-initiation subprograms. These are described in detail later, but consist of initializing all simulated microprocessor memory, registers and data paths, and reading microinstructions and main memory sequence instructions and data values into the appropriate locations of simulated microprocessor memory (Table 3). Execution is then initiated by entering an outer loop (DO WHILE .NOT.FINIS(hed). AND..NOT.ERROR) in which a main memory access and decode is accomplished. An inner (macro) loop is then entered which is controlled by the contents of the H-field of the microinstructions. The emulator simulates the execution of all functions specified by the microinstructions, and falls out of the inner loop when a next-H = zero is encountered. At this point, the macrocount is incremented and the run termination conditions are examined to determine if the run should go on. If the run is to stop normally, the logical variable FINIS is set to .TRUE.; if a fatal error has been encountered, the logical variable ERROR will have been set to .TRUE. Either condition will cause the simulated run to stop, and a final statistical output routine will be called.

TABLE 2. MULTIPURPOSE MICROPROCESSOR RUN CONTROL CARD

Card Columns	Octal Value	Interpretation
1-4	1	Pre-clear control memory.
	2	Pre-set control memory, NO-OP, next H = here.
5-8	1	Pre-clear main memory
	2	Pre-set main memory, H = 0, C = here.
9-12	1	Minimum output during execution
	2	Extensive diagnostic output during execution.
13-16	0	No initialization output.
	1	Output simulated memory after load.
17-20	XXXX	Ten-bit initial value of PC. (i.e., starting address of main memory)
21-24	XXXX	Output control-interval time-octal (sec)
25-28	XXXX	Output control-microinstruction count.
29-32	XXXX	Output control-selected macroaddress.
33-36	Run	Termination criteria
	1	H-address stop
	2	C-address stop
	3	Simulated elapsed time
	4	Real elapsed time
	5	Macroinstruction count
37-40	XXXX	Octal termination value associated with above termination criteria.
41-44	1	Load memory cards are in contiguous octal representation
	2	Load control memory by 25 discrete octal fields

Note: Run control card can be expanded to accommodate more variable considerations - currently the card is read with a (20 04) format.

TABLE 3. MULTIPURPOSE MICROPROCESSOR MEMORY LOAD CARD

N-RUN (11) = 1: Card	
<u>Columns</u>	<u>Contents</u>
1	Key: 1 = main memory load 2 = control memory load 9 = load completed
9-12	Address: 4 octal digits
15-20	Main memory contents: 6 octal digits
21-36	Control memory contents: 16 octal digits
N-RUN (11) = 2:	
1	Key: 1 = Main memory load 2 = Control memory load 9 = Load completed
3-6	Address: 4 octal digits
8-10	Left 8 bits of main memory (octal)
11-13	Right 8 bits of main memory (octal)
15-33	Control memory instruction, by fields (octal)

Note: Memory load card could be extended to register loads or other size memory word loads by adding keys to columns 1 through 8, as desired.

#### 4. Emulator Routine Descriptions

This section describes in detail the actions performed by the individual subprograms of the microprocessor emulator. The sequence of the descriptions follows generally the order in which the routines are called, except that the more general purpose and widely used routines are described last. Flowcharts, listings, and detailed data element definitions are given on the appendices.

##### a. Subroutine INIT

This routine initializes all nonmemory elements of the simulated hardware to zero, except for scratchpad word one (PC), which is set to the value read from the run control card [NRUN(5)]. In addition, the emulator control variables FINIS and ERROR are set to .FALSE., and operation count and time accumulation variables are set to zero. This routine is called one time per emulator run.

b. Subroutine SETCM

This routine initializes all 1024 words of simulated control memory (CNTMEM), based on an initialization key read from the run control card (NRUN(1)). If the key is 1, all of memory is cleared to zero; if the key is 2, each word in memory is preset to a NO-OP in the op code field, and the H-field is set to point to its own address. With this setting, execution of a microprogram will hang in a one-word loop if it inadvertently gets outside the area where the microprogram under test is loaded. Any other value of the key on the run control card will cause an error message and will abort the run by setting ERROR to .TRUE. This routine is called once per emulator run.

c. Subroutine SETMN

This subroutine is the same as SETCM, except NRUN(2) is the applicable key, and presets main memory (MAINM) rather than control memory.

d. Subroutine LOADM

This subroutine reads data cards which contain the octal address and octal contents of all words of simulated control memory and main memory which are to be loaded for an emulation run. A key in column 1 is used to determine the type memory a given card applies to: key = 1 loads main memory, key = 2 loads control memory, and key = 9 signifies the load is completed; any other key causes an error message to be printed, and the flag ERROR is set to .TRUE. The load cards may contain the 16- or 48-bit contiguous octal value to be placed in memory, or may contain separate fields for each field of the macroinstructions and microinstruction, as preferred. This routine is called once per emulator run.

e. Subroutine DCODM

This subroutine is called to initiate the execution of a macroinstruction by accessing a word of main memory and decoding it. The main memory word accessed is the one whose address is currently in the Program Counter (PC - word one of the simulated scratchpad). Once the address is retrieved, the PC is incremented by one. Then the main memory word is broken into two 8-bit fields utilizing the subroutine GETMM. If an error flag is returned from GETMM, an error message is output and ERROR is set to .TRUE. Otherwise, the left-most 8 bits are incremented by 1400 octal and placed in the simulated H-register, and the right-most 8 bits are incremented by 1400 octal and placed in the simulated C-register. The original values of the two halves are stored in MINSTR and MOPND respectively. This subroutine is called once for each Macro executed.

f. Subroutine GETMM

This subroutine is generalized to extract any given field from a 16-bit simulated word located in a 24-bit R-520 word. It therefore has five parameters in its calling sequence: (1) the address of the word to be extracted from, (2) the starting bit, decimal 0 through 15, of the field to be extracted, (3) the number of bits to be extracted, (4) the address that the field, right adjusted and zero-filled, is to be stored in, and (5) an error flag which is set to zero when no error is encountered, or to an integer to identify the parameter which contained a recognizable error. This subroutine is normally called twice per macro, or once for each desired field extraction.

g. Subroutine DCODC

This subroutine is called to break down a 48-bit microinstruction into its constituent fields (currently 25) to facilitate interpretation and simulated execution of the specified operations and control functions. The selected 48-bit word is that pointed to by the index in the simulated H-register. The extraction of the fields is accomplished by calling GETCM, and the fields are placed in a 25-word vector in COMMON identified as MICRO(25). If an error flag is returned from GETCM, an error message is output and ERROR is set to .TRUE. The subroutine is called once for each microinstruction to be executed.

h. Subroutine GETCM

This subroutine is generalized to extract any given field from a 48-bit (60-bit in CDC version) real word, and return the result right-justified, zero-filled, in a 24-bit integer word. It is therefore currently limited to a 24-bit extraction, but the largest field currently required from a microinstruction is the 10-bit next-H field. The calling parameters are identical to those listed for GETMM, except that the starting bit may be any decimal number from 0 through 47. This subroutine is normally called 25 times per microinstruction, or once for each desired field extraction.

i. Subroutine EXECM

This subroutine manages the complex execution of a microinstruction. It first calls PRBIN for the application of those control functions which occur prior to instruction interpretation/execution. It then determines if the register SR2 is to cause the operation code to be modified, and does so if indicated. It then determines which of seven functional areas of execution that the operation code falls in, and then calls the appropriate routine to execute that operation. If the operation code is outside the allowed range (0 - 31 decimal), then an emulator error has occurred, a message is output, and ERROR is set to .TRUE. Otherwise, the subroutine BINRY is called to interrupt and act upon the binary control fields which apply in time after instruction execution is completed. This subroutine is called once per microinstruction.



j. Subroutine PRBIN

The microprocessor hardware design is such that the following control functions are performed, if enabled, prior to instruction execution:

<u>Field</u> (Ref. Figure 2)	<u>Octal</u> <u>Bit No.</u>	<u>Action if Bit = 1 (On)</u>
6	32	SR1 = 0 (MSR1 = 0)
10	36	Buss = Main(c) (MBUSS - MAINM(MEMC))
13	41	Buss = DATA IN = (Input Discretes) OR (A/D Output)
15	43	LSB or Buss = SR1 (MBUSS = OR (MBUSS, MSR1))
17	45	Carry (Cn) = 1
20	50	Select D/A 1
21	51	Select D/A 2
22	52	Select D/A 3
23	53	Clock A/D Mux Addr Register
24	54	Clock A/D conversion Start (per Bit.)

The subroutine checks each of these fields [micro(6) micro(10),... MICRO(23)] in turn: For each that is set (i.e., equal to 1), the indicated operation (or test and operation) is performed. Most of the required actions are the setting of one variable equal to another (i.e., MSR1 = 0), MBUSS = MAINM(MEMC), etc.), but not always. For example, if bit 43 octal = 1, MSR1 is Ored to the MBUSS, so that the only change that if MSR1 = 1 and the LSB of MBUSS is 0, it is changed to 1. The last four controls cause special keys (KDA for D/A, KAD for A/D) to be set at nonzero (1, 2, or 3) for the appropriate D/A register select, or equal to the MUX address [MICRO(25)] for A/D input. Timing for A/D setting delays must be managed by the microprogram. This subroutine is called once per microinstruction.

k. Subroutine BOLN (Boolean)

This is the first operation code execution subprogram, and is called when the effective operation code is in the range 00 to 06 inclusive. The operation specified are all Boolean except that generated by OP code 0. In this and all subsequent OP code execution routines, a temporary variable ITMP is first set to the value resulting from the operation, and the final effect on the status of registers and output lines is determined later, after analysis of the instruction modifier field. The status of the carry in register ICN affects the result of OP code 0. If ICN = 0, then ITMP = 177777, or all bits on. If ICN = 1, then ITMP = 0 (all bits off). For the other OP codes in this subroutine, ICN has no effect.

<u>OP Code</u>	<u>Result</u>
00	ITMP = 177777 if ICN = 0; = 0 if ICN = 1
01	ITMP = (A OPND) and (B OPND)
02	ITMP = (Data in) and (B OPND)
03	ITMP = (A OPND) or (B OPND) } Inclusive
04	ITMP = (Data IN) or (B OPND) } or
05	ITMP = (A OPND) XOR (B OPND) } Exclusive
06	ITMP = (Data IN) XOR (B OPND) } or

Note: The data IN lines are represented by the variable IDIN.

This subroutine then examines the instruction modifier field. If the modifier value is seven, then the Q-register (MICQ) is set equal to the resultant value of ITMP, and control is returned to the calling program. If the modifier is not seven, then the scratchpad address pointed to by the B-operand is set to ITMP, and the subprogram INMOD is called to complete the effects of the modifier.

#### 1. Subroutine INVRT (Invert)

This subprogram is called when the effective operation code is in the range 07 to 10 inclusive (07 to 12 octal). In the emulator, the operations are performed first, and then the effects of the carry (ICN) are applied.

<u>OP Code</u>	<u>Octal</u>	<u>Result</u>
7	07	ITMP = Complement of (A OPND)
8	10	ITMP = Complement of (Data IN)
9	11	ITMP = Complement of (B OPND)
10	12	ITMP = Complement of (Q REG)

Then ICN is examined if = 0, 177777 (all ones) are added to ITMP, and the bits to the left of the 16-bit simulated word length are masked off. If ICN = 1, ITMP is not changed. Then the modifier is examined, and, if = 7, the Q-register is set equal to ITMP, and control is returned. Otherwise, the B-operand word in the scratchpad is set equal to ITMP, and INMOD is called.

m. Subroutine CMPLT (Two's Complement)

This subroutine is entered when the OP code is 11 to 14 and performs almost identical operations to those of INVRT:

<u>OP Code</u>		
<u>Decimal</u>	<u>Octal</u>	<u>Result</u>
11	13	ITMP = Complement of (A OPND) + ICN
12	14	ITMP = Complement of (Data IN) + ICN
13	15	ITMP = Complement of (B OPND) + ICN
14	16	ITMP = Complement of (Q REG) + ICN

In this case, if ICN = 0, ITMP is not affected; and if ICN = 1, ITMP is increased by 1, thereby performing a 2's complement on the selected data. Then, if the modifier is 7, the Q-register is set to ITMP. If the modifier is other than 7, the value of the B-operand is set to ITMP and INMOD is called.

n. Subroutine TRINC (Transfer/Increment)

This subroutine is called when the OP code is 15 to 18, with the following results:

<u>OP Code</u>		
<u>Decimal</u>	<u>Octal</u>	<u>Result</u>
15	17	ITMP = (A OPND) + ICN
16	20	ITMP = (Data IN) + ICN
17	21	ITMP = (B OPND) + ICN
18	22	ITMP = (Q REG) + ICN

Here, when carry is 0, the effect is a simple transfer of the contents of the designated operand to the designated B-operand or the Q-register, depending on the modifier. Note that operation 17 (21 octal) will have a no OP effect if the modifier is 0. The emulator still performs the load ITMP from B and stores ITMP back in B, however. If carry = 1, the operation includes an increment. If the modifier is 7, the value in ITMP is stored in the Q-register. Otherwise, the value is stored in the designated B-operand and INMOD is called.

p. Subroutine DECTR (Decrement/Transfer)

This subprogram is called when the operation code is 19 to 22, with results similar to TRINC above:

<u>OP Code</u>		
<u>Decimal</u>	<u>Octal</u>	<u>Result</u>
19	23	ITMP = (A OPND)
20	24	ITMP = (Data IN)
21	25	ITMP = (B OPND)
22	26	ITMP = (Q REG)

When the basic operation of loading ITMP is completed, the value of carry is examined. If carry = 0, than all 1's (177777 octal) is added to ITMP, and ITMP is then masked back to 16 bits. Thus the effect is to decrement ITMP by 1, since the action constitutes addition of a minus one. This technique is used in the emulator because that is the way the operation is performed in the microprocessor hardware. If carry = 1, no further change is made yet to ITMP. Here again is a potential no-OP, in OP code 21 (25 octal), when carry is on and the modifier is 0. Again, ITMP is placed in Q-register if the modifier is 7; otherwise, it is placed in the B-operand and INMOD is called.

q. Subroutine SUM (Addition)

This subroutine is entered when the OP code is 23 to 25, and the following operations result:

<u>OP Code</u>		
<u>Decimal</u>	<u>Octal</u>	<u>Result</u>
23	27	ITMP = (A OPND) + (B OPND) + ICN
24	30	ITMP = (Data IN) + (B OPND) + ICN
25	31	ITMP = (A OPND) + (Q REG) + ICN
26	32	ITMP = (Data IN) + (Q REG) + ICN

Here, the effect of carry is to increase the sum by one if on (ICN = 1), or no effect if off (ICN = 0). If the instruction modifier value is 7, Q-register is loaded with the value in ITMP, and control is returned to the calling program. Otherwise, the B-operand is loaded from ITMP and INMOD is called.

r. Subroutine DIFF (Subtraction)

This subroutine is called when the operation code is 27 to 31, and is the last of the operation analysis/execution subroutines. The effects are:

<u>OP Code</u>		<u>Result</u>
<u>Decimal</u>	<u>Octal</u>	
27	33	ITMP = (A OPND) - (B OPND)
28	34	ITMP = (B OPND) - (A OPND)
29	35	ITMP = (Data IN) - (B OPND)
30	36	ITMP = (B OPND) - (Data IN)
31	37	ITMP = (Data IN) - (Q REG)

The effect carry has on this operation is to reduce the result by one when carry is off (ICN = 0), or no effect when on (ICN = 1). Again, ITMP is stored in the Q-register if the instruction modifier is minus 7; otherwise, ITMP is stored in the B-operand and INMOD is called.

s. Subroutine INMOD (Instruction Modification)

This subprogram is called from the applicable instruction interpretation/execution routine when the instruction modifier is not 7, but 0 to 6. At this point, the value produced by execution of the operation has been placed in the scratchpad word pointed to by the B operand of the microinstruction. The following actions are now taken based on the value of the modifier:

<u>Modifier</u>	<u>Action</u>
0	(Data OUT) = (B OPND)
1	(Data OUT) = (A OPND) ('A' Latch).
2	(Data OUT) = old (B OPND), before execution of operation changed its value ('B' Latch).
3	Shift (B OPND) left one bit - zero enters (B OPND) from the right, and the bit shifted off is inverted and Ored to SR1 (MSR1). Result is also placed in (Data OUT).
4	Shift (B OPND) right one bit - a one bit enters (B OPND) from left, and the bit shifted off is lost. Result is placed in Data Out.
5	Shift (Q-REG and (B OPND) together left one bit - a one bit enters q from right - MSB of (B OPND) → SR1. Data OUT is then set to the resultant (B OPND) value.
6	Shift (Q-REG) and (B OPND) together right one bit - a one bit enters the MSB of (B OPND), and the bit shifted off of the Q-REG is inverted and Ored to SR1 (MSR1). Data OUT is then set to the new value of (B OPND).

Note: Data OUT is represented by the variable IDOUT. Control is then returned to the calling routine.

t. Subroutine BINRY

The binary control bits which were not examined for required action prior to operation code execution are now evaluated. They are:

<u>Field</u> (Ref. Figure 2)	<u>Octal</u> <u>Bit No.</u>	<u>Action if BIT = 1 (on)</u>
7	33	SR2 = SR1 (MSR2 = MSR1)
8	34	H - REG = CM (addr) (MEMH = MICRO(5))
9	35	MEM (C) = Buss (MAINM (MEMC) = MBUSS)
11	37	Buss = ALU Data OUT (MBUSS = IDOUT)
12	40	Fetch (Confirm that H REG = 0; if not, ERROR = .TRUE.)
14	42	SRI = 1 if Data OUT = 0
16	44	H - REG = SRI Ored to LSB of H - REG
18	46	Telemetry = Buss (ITELM = MBUSS)*
19	47	C - REG = Buss (MEMC - MBUSS)

\*Note: Telemetry bit effect is inverted, i.e., telemetry = buss when bit 46<sub>8</sub> = 0.

This routine is called once per microinstruction.

u. Subroutine FINAL

This subroutine is entered following the completion of a complete macrooperation, and evaluates the run-termination criteria which were setup by the run control card. If the termination criteria are satisfied, then the logical variable FINIS is set to .TRUE., otherwise no action is taken, and control is returned to the calling routine (MAIN). This subroutine is called once per macro-operation.

v. Subroutine STATS

This subroutine is entered after the simulated microprocessor run has been terminated or aborted. The routine prints out the contents of all registers, data paths, and the 16-word scratchpad, plus the simulated run time, number of microinstructions, and the number of macros executed. Additional output can be added as desired. When control is returned to the main program, the program stops.

w. Subroutine REPT1

This subroutine is called when the level of diagnostic output required is high as indicated on the run control card. Currently, outputs result in the execution of individual microinstruction. It is anticipated that this subroutine will be expanded as more experience is gained in the development of microprograms.

x. Subroutine REPT2

Stub only - not yet implemented.

y. Subroutine XOR

Not used for CDC 6000 version: CDC function XOR.

This subroutine was developed prior to the availability of exclusive OR in the R-520 function library. It performs an exclusive OR on the second or third parameters, and returns the results in the first parameter. It uses the following algorithm:

```
CALL XOR (IANS, J, K)
IANS = ((J)AND(K))OR((J)AND(K)).
```

z. Subroutine FLEX

Not used for CDC 6000 version.

This subroutine contains all the required direct code (R-520 FLEXTRAN) for the emulator. Two functions are currently performed, based on the key in parameter one: If key = 1, the subroutine converts a right-adjusted real (double-word) variable to an integer variable. If K = 2, the subroutine increments the H-field (bit 31 octal) of a 48-bit microinstruction by 1, used in presetting control memory.

## 5. Preliminary Results

The basic design goal of providing a software development and test capability for the digital control computer application of the microprocessor has been met, and the emulator is now serving this capacity. It has been determined that the ability to vary the intermediate output over a very wide range has been difficult to implement, but further work is planned in this area. The current version allows essentially three options of output: (a) a full printout of simulated control and main memory after loading (Table 4), (b) a very detailed printout of the intermediate and final results of each instruction execution (Table 5), and (c) a final status of all registers and data paths after termination (Table 6). The last of these three is currently not under run card control, but the other two are. It is not yet known

TABLE 4. MICROPROCESSOR SIMULATED MEMORY CONTENTS

LOCATION		CONTENTS	
DECIMAL	HEX	MAIN MEMORY	CONTROL MEMORY
38	0046	00000046	4200001142000000
39	0047	00000047	4200001162000000
40	0050	00000050	4200001202000000
41	0051	00000051	4200001222000000
42	0052	00000052	4200001242000000
43	0053	00000053	4200001262000000
44	0054	00000054	4200001302000000
45	0055	00000055	4200001322000000
46	0056	00000056	4200001342000000
47	0057	00000057	4200001362000000
48	0060	00000060	4200001402000000
49	0061	00000061	4200001422000000
50	0062	00000062	4200001442000000
51	0063	00000063	4200001462000000
52	0064	00000064	4200001502000000
53	0065	00000065	4200001522000000
54	0066	00000066	4200001542000000
55	0067	00000067	4200001562000000
56	0070	00000070	4200001602000000
57	0071	00000071	4200001622000000
58	0072	00000072	4200001642000000
59	0073	00000073	4200001662000000
60	0074	00000074	4200001702000000
61	0075	00000075	4200001722000000
62	0076	00000076	4200001742000000
63	0077	00000077	4200001762000000
64	0100	00057000	4200002002000000
65	0101	00000101	3676742052004000
66	0102	00000102	4360702102000000
67	0103	00000103	4200002632000000
68	0104	00000104	0140702136002000
69	0105	00000105	4355702156000000
70	0106	00000106	4355702176000000
71	0107	00000107	4355702216000000
72	0110	00000110	4355702236000000
73	0111	00000111	4355702256000000
74	0112	00000112	4355702276000000
75	0113	00000113	4355702316000000
76	0114	00000114	4355702336000000
77	0115	00000115	4355702356000000
78	0116	00000116	4355702376000000
79	0117	00000117	4355702416000000
80	0120	00000120	4355702436000000
81	0121	00000121	4355702456000000
82	0122	00000122	4355702476000000
83	0123	00000123	4355702516000000
84	0124	00000124	4215702522000000
85	0125	00000125	3664202542004000
86	0126	00000126	4200000002000000
87	0127	00000127	3200040002002000
88	0130	00000130	4200000002000000
89	0131	00000131	3360702642000000
90	0132	00000132	0000202102002000
91	0133	00000133	4200002662000000
92	0134	00000134	4200002702000000
93	0135	00000135	4200002722000000
94	0136	00000136	4200002742000000
95	0137	00000137	4200002762000000
06	0140	00000140	4200003002000000

NO-OP, NEXT H = HERE

GENERAL PURPOSE  
MULTIPLY  
MACRO INSTRUCTION



TABLE 5. DETAILED EXECUTION OUTPUT

```

THIS INSTR AT:1425, H-FIELD = 1426 .
SUBROUTINE BOLN ENTERED.
INSTR U4 EXECUTED, TEMP VALUE = 013404.
INSTR MOD = 3 JUST SET DATA-OUT = 0027010.
EXECUTED OP CODE 04 WITH MODIFIFF 3.
A-REG 14 CONTENTS = 003001
B-REG 15 CONTENTS INITIALLY = 001400, NOW = 027010
Q-REG CONTENTS INITIALLY = 077777, NOW = 077777
IELEM CONTENTS INITIALLY = 001400, NOW = 016005

THE FOLLOWING CM INSTRUCTION HAS JUST BEEN EXECUTED:
1425 1074670542203490 04 03 14 15 M:1406 0 0 1 0 0 1 0 0 0 0 1 1 1 0 0 0 0 0 0

SCRATCH PAD(00) CONTAINS 001405 .
SCRATCH PAD(01) CONTAINS 000000 .
SCRATCH PAD(02) CONTAINS 000000 .
SCRATCH PAD(03) CONTAINS 000000 .
SCRATCH PAD(04) CONTAINS 000000 .
SCRATCH PAD(05) CONTAINS 000000 .
SCRATCH PAD(06) CONTAINS 000000 .
SCRATCH PAD(07) CONTAINS 000000 .
SCRATCH PAD(08) CONTAINS 004001 .
SCRATCH PAD(09) CONTAINS 016005 .
SCRATCH PAD(10) CONTAINS 000002 .
SCRATCH PAD(11) CONTAINS 000774 .
SCRATCH PAD(12) CONTAINS 003001 .
SCRATCH PAD(13) CONTAINS 027010 .
SCRATCH PAD(14) CONTAINS 077777 .
SCRATCH PAD(15) CONTAINS 000000 .
SCRATCH PAD(16) CONTAINS 000000 .
SCRATCH PAD(17) CONTAINS 000000 .

DATA IN = 00012004, DATA OUT = 0027010, BUSS = 00016005, C-REG = 00000005
CARRY = 1, SRI = 0, SR2 = 0.

```

TABLE 6. FINAL OUTPUT

RUN TERMINATED AT TIME : .10950 SECONDS AFTER 146 MICROS OR 34 MACROS EXECUTED.

SCRATCHPAD CONTAINS:

00001442  
00000000  
00000000  
00000000  
00177303  
00176606  
00076605  
00000000  
00171547  
00161212  
00010512  
00177776  
00177777  
00002364  
00077777  
00035376

DATA IN = 00001777, DATA OUT = 00077777, RUSS = 00077777, C-REG = 1777, H-REG = 0000, Q-REG = 177777

A/D S = 00000000 00000000 00000000 00000000, D/A S = 00000000 00000000 00000000

CARRY = 0, INPUT DISCRETES = 00000000

MSR1 = 0, MSR2 = 0

if the ability to vary more widely the intermediate detail will be worth the additional parameter testing that will be required to implement it, but further analysis is planned.

The structure of the control mechanisms of the emulator was of some concern, and it was not readily obvious what criteria should be used to manage a given emulation run. It was finally decided to use two logical (Boolean) variables, ERROR and FINIS, to control the runs. Both are initialized to .FALSE., and both are tested at the beginning of each simulated Macroinstruction execution. Any error condition in any subroutine causes an error message to be output at that point, and then causes the error variable to be set to .TRUE., which then causes the run to be terminated at the next macro-FETCH stage of execution. Upon completion of a macroinstruction, the normal run-termination conditions defined by the run control card are examined, and if the conditions are met, causes FINIS to be set .TRUE., with the same result. This technique allows the program termination to be controlled, and meets the structured programming criteria of one-entrance, one-exit for the main program. All subroutines have this same characteristic of one-in, out-out. In general, it is felt that valuable additional experience with the use of structured FORTRAN forms has been gained.

## 6. Conclusion and Future Work

The emulator described in this report is currently operational on the Raytheon R-520 and CDC 6600 computers, and is currently supporting the applications software development process for the first multi-purpose microprocessor feasibility application, that of guidance control computer on the T-6 missile. It is anticipated that extensions to the emulator will be made during the flight software development. Some of the planned extensions are:

- a) Experimentation with various forms and frequencies of emulator output, and with interactive control of emulator runs.
- b) Experimentation with different microprocessor software structures, such as the development of meaningful operation codes at the main memory level, as opposed to simply pointing to macros and data.
- c) Experimentation with variations in the word size of main and control memory.
- d) Efforts to implement the emulator on other host computers, including the HP 2100.

In addition to the above, but probably later in time, it is anticipated that studies will be made of the potential of generalizing from the current emulator form to allow external definition of instruction/control fields and their meanings. This will involve attempts to support microprogramming for other microprocessors, the accumulation of information on similarities and differences, and the analysis of this data

against the original structure of this emulation effort. Another planned extension will provide an interactive capability for testing and modifying microprograms.

One outstanding characteristic of this work that should be emphasized is the comparative ease of making necessary or experimental changes to the emulator. In a new-processor environment, where both unforeseen and planned hardware changes are frequent, the simplicity of making fast changes to the emulator program has been invaluable. The modular design coupled with the strict adherence to the principals of structured programming are primarily responsible for this capability. More specifically, when a hardware function was initially misunderstood, or later required modification, the exact location of the emulator representation of that function was immediately known, easily isolated, and readily changed. This feature is also expected to play a vital role in future experimentation with proposed hardware design variations, in that the effects as seen by software can be thoroughly evaluated very easily prior to making any actual hardware changes.

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**Appendix A. MULTIPURPOSE MICROPROCESSOR EMULATOR:  
DATA ELEMENT DEFINITIONS**

1. Common

CNTMEM (1024)	SIMULATED CONTROL MEMORY, 48 BITS/WORD
ICN	SIMULATED CARRY IN - 1 BIT (ACTUAL 24)
ICOUNT	INSTRUCTION COUNT REGISTER, INITIALIZED AT 0, INCREMENTED BY 1 IN EXECM (MICRO)
IDIN	SIMULATED DATA IN LINES - 16 BITS (ACTUAL 24)
IDOUT	SIMULATED DATA OUT LINES - 16 BITS (ACTUAL 24)
IDSCAR	SIMULATED INPUT DISCRETE REGISTER - 4 BITS (ACTUAL 24)
ITELM	SIMULATED TELEMETRY REGISTER - 16 BITS (ACTUAL 24)
MAINM (1024)	SIMULATED MAIN MEMORY, 16 BITS/WORD (ACTUAL 24)
MBUSS	SIMULATED DATA BUSS, 16 BITS (ACTUAL 24)
MEMC	SIMULATED MAIN MEMORY ADDRESS (C) REGISTER 10 BITS (ACTUAL 24)
MEMH	SIMULATED CONTROL MEMORY ADDRESS (H) REGISTER 10 BITS (ACTUAL 24)
MICAD (5)	SIMULATED A/D INPUT REGISTERS, 12 BITS EACH (ACTUAL 24)
MICDA (3)	SIMULATED D/A OUTPUT REGISTERS, 12 BITS EACH (ACTUAL 24)
MICQ	SIMULATED Q REGISTER - 16 BITS (ACTUAL 24)
MSCPAD (16)	SIMULATED MICROPROCESSOR SCRATCHPAD MEMORY - 16 BITS EACH (ACTUAL 24) MSCPAD (1) = PROGRAM COUNTER MSCPAD (2) THRU (4) = RETURN ADDRESSES MSCPAD (5) THRU (8) = X REGISTERS MSCPAD (9) THRU (12) = A REGISTERS MSCPAD (13) THRU (16) = B REGISTERS
MSR1	SIMULATED SR1
MSR2	SIMULATED SR2
NRUN (20)	RUN CONTROL PARAMETERS: NRUN (1) - PRESET VALUE FOR CONTROL MEMORY NRUN (2) - PRESET VALUE FOR MAIN MEMORY NRUN (3) - OUTPUT LEVEL NRUN (4) - INITIALIZATION OUTPUT LEVEL NRUN (5) - INITIAL PC VALUE (START) NRUN (6) - OUTPUT CONTROL INTERNAL - TIME NRUN (7) - OUTPUT CONTROL INTERVAL - INSTR. COUNT NRUN (8) - OUTPUT CONTROL - ADDRESS IN H NRUN (9) - TERMINATION CRITERIA NRUN (10) - TERMINATION VALUE NRUN (11) - FORMAT OF MEMORY LOAD USE REMAINING NRUN OPTIONS RESERVED FOR FUTURE USE -
FINIS	LOGICAL: NORMAL RUN TERMINATION FLAG
ERROR	LOGICAL: ERROR TERMINATION FLAG

MINSTR	MAIN MEMORY INSTRUCTION - 8 BITS (ACTUAL 24)
MOPND	MAIN MEMORY OPERAND - 8 BITS (ACTUAL 24)
MICRO (25)	MICROINSTRUCTION FIELDS: (ALL ACTUAL 24 BITS)
	MICRO (1) - OPERATION CODE - 5 BITS
	MICRO (2) - INSTRUCTION MODIFIER - 3 BITS
	MICRO (3) - OPERAND 1 ADDRESS - 4 BITS
	MICRO (4) - OPERAND 2 ADDRESS - 4 BITS
	MICRO (5) - NEXT MICRO (H) ADDRESS - 10 BITS
	MICRO (6) THU (24) - BINARY CONTROL FIELDS - 1 BIT EACH
	MICRO (25) - A/D MUX ADDRESS - 3 BITS
MCNT	MACRO COUNT - INCREMENTED IN MAIN
STIME	SIMULATED ELAPSED TIME - 750 NSEC/MICRO EXECUTION
ITIME	INTEGER VALUE OF STIME IN SECONDS
IETIM	ELAPSED EMULATION RUN TIME
KAD	KEY THAT D/A MUX HAS BEEN CLOCKED
KDA	KEY TO SELECTED A/D REGISTER

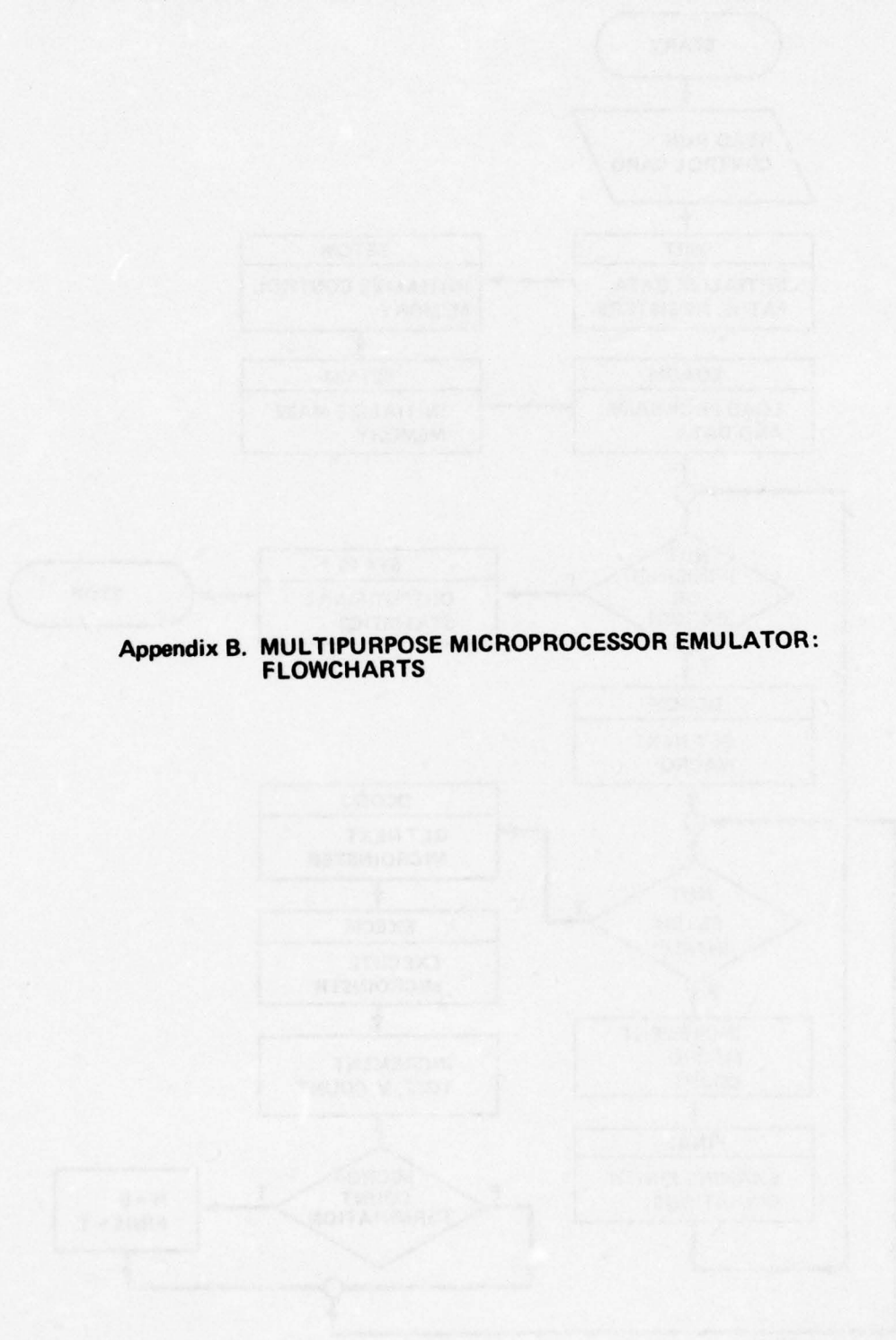
2. Noncommon

<u>Subprogram</u>	<u>Parameter</u>	
in EMUL (MAIN)	LFTMS	8-BIT MASK (377 OCTAL)
	TINCR	TIME INCREMENT (0.00000075 SEC = 75 NSEC)
in SETCM	MICS	MICROINSTRUCTION COUNT
	REPL /00/	TO PRESET CONTROL MEMORY TO CLEAR
	REPL 2	TO PRESET CM TO NOP TO HERE
	INDX	INDEX THRU MEMORY, 1 - 1024
SETMM LOADM	ADDR	INCREMENT H FIELD BY ONE (CDC VERSION ONLY)
	MSK	8-BIT MASK
	INDX	INDEX THRU MEMORY, 1 - 1024
	MSK 1	MASK FOR INVERSION OF BITS 2, 3 OF OP CODE
	KEY	MAIN OR CONTROL MEMORY, OR END LOAD
	MADR	OCTAL ADDRESS
	MAIN	VALUE FOR MAIN MEMORY
	CNTRL	VALUE FOR CONTROL MEMORY
	K	MAIN MEMORY WORD COUNTER
	L	CONTROL MEMORY WORD COUNTER
DCODC	IERR	CUMULATIVE ERROR FLAG
	IPTR	CALLING PARAMETER FOR MEMH
	MOP	CALLING PARAMETER FOR MICRO(N)
	INDX	MICRO INDEX
	NCOL	FIELD (COLUMN) INDEX
	IFLAG	ERROR RETURN FLAG
DCODM	MSK 1	MASK FOR INVERSION OF BITS 2, 3 OF OP CODE
	IOFF/01400	OFFSET FOR 1st INSTR OF EACH MACRO
	MIN	CALLING PARAMETER FOR MINSTR
	MOP	CALLING PARAMETER FOR MOPND

GETCM	IADR	ADDRESS OF SOURCE WORD
	IBITL	LEFT (START) BIT OF DESIRED FIELD
	IBITN	NUMBER OF BITS IN FIELD
	IBYTE	ADDRESS OF TARGET (FIELD) WORD
	I FLAG	ERROR FLAG
	IDR	IADR + 1 TO OFFSET 0 BASE FOR INDEX
	OPMSK/IMSK	MASK FOR EXTRACTING FIELD
	BYTE	48 - BIT ANSWER FIELD (R-520 VERSION ONLY)
	NMBR	FINAL SHIFT FOR RIGHT ADJUST
	ISTBIT	START BIT OFFSET FOR 60-BIT WORD (CDC VERSION ONLY)
GETMM	IADR	
	IBITL	
	IBITN	SAME AS GETCM
	IBYTE	
	I FLAG	
	IDR	
	IBIT	MACHINE-WORD ADJUSTMENT FOR START BIT
	IMASK	MASK FOR EXTRACTING FIELD
	NMBR	FINAL SHIFT FOR RIGHT ADJUST
INMOD	MOD	INSTRUCTION MODIFIER (MICRO(2)) - USED TO SPECIFY DESTINATION OF OUTPUT AND TO CONTROL SHIFT OPERATIONS.
	IA	INDEX OF A OPERAND
	IB	INDEX OF B OPERAND
	KMASK	RIGHTMOST 16-BIT MASK
	IHIBIT	LEFTMOST 1-BIT MASK (HIGH BIT)
XOR (R-520 ONLY)	IANS	ARGUMENT 1, RESULT OF EXCLUSIVE OR
	J	ARGUMENT 2, VALUES TO BE EXCLUSIVE
	K	ARGUMENT 3, OR ED
EXECM	IOP	OPERATION CODE (MICRO (1))
OPERATIONS	IOP	OP CODE (MICRO (1))
BOLN	LHIGH	OCTAL 177777 (FORCE ALL 1s), 16-BIT MASK
INVRT	MOD	INSTRUCTION MODIFIER (MICRO(2))
CMLPT	IAR	A OPERAND INDEX (MICRO(3))
TRINC	IBR	B OPERAND INDEX (MICRO(4))
DECTR		
SUM	ITMP	TEMPORARY HOLD FOR RESULTS OF EXECUTION UNTIL FINAL FORM/DESTINATIONS IS DETERMINED
DIFF		
PRBIN	ILOW	4 LSBs OF DATA IN (IDIN) OR DATA OUT (IDOUT)
BINRY	KOUNT	ELAPSED TIME (OPERATIONS) COUNTER FOR D/A OUTPUT REGISTER SELECTION
	MSK 10	10-BIT MASK FOR ADDRESSES
FLEX	K	KEY TO SELECTED DIRECT CODE OPTION

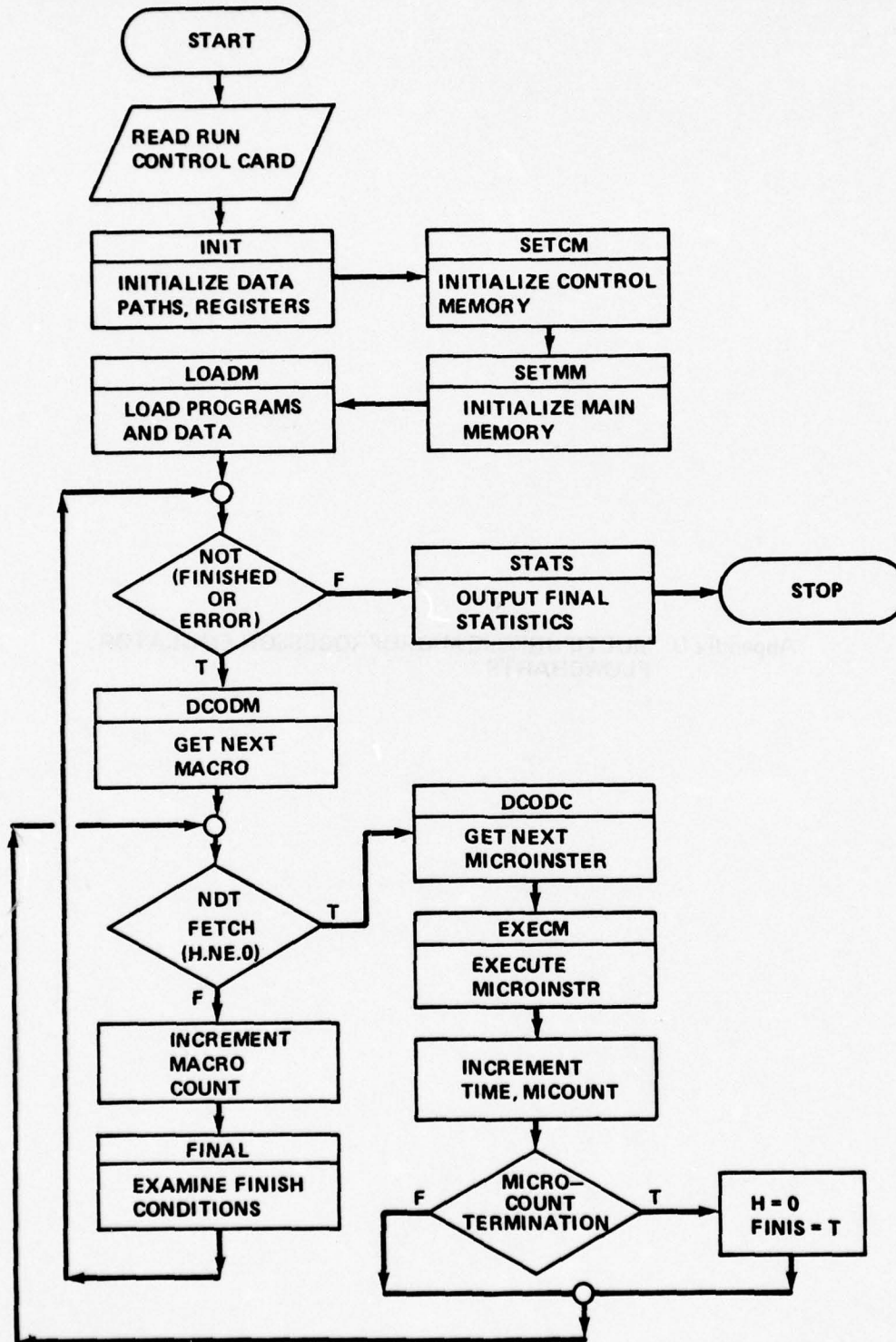


(R-520 ONLY)	FLTB	REAL (48-BIT) PARAMETER IN OR RETURN
	INTEGR	INTEGER (24-BIT) PARAMETER OR BOTH
FINAL	NEND	TERMINATION CRITERIA (NRUN(9))
	NVAL	TERMINATION VALUE (NRUN(10))
REPT1	ITEL2	PREVIOUS VALUE OF TELEMETRY REGISTER
	MICQ2	PREVIOUS VALUE OF Q-REGISTER

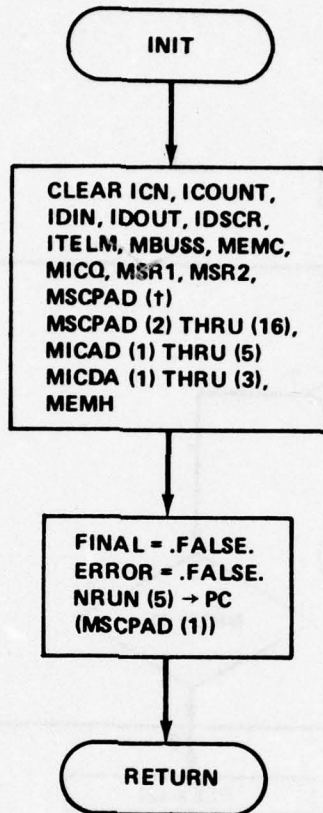


**Appendix B. MULTIPURPOSE MICROPROCESSOR EMULATOR:  
FLOWCHARTS**

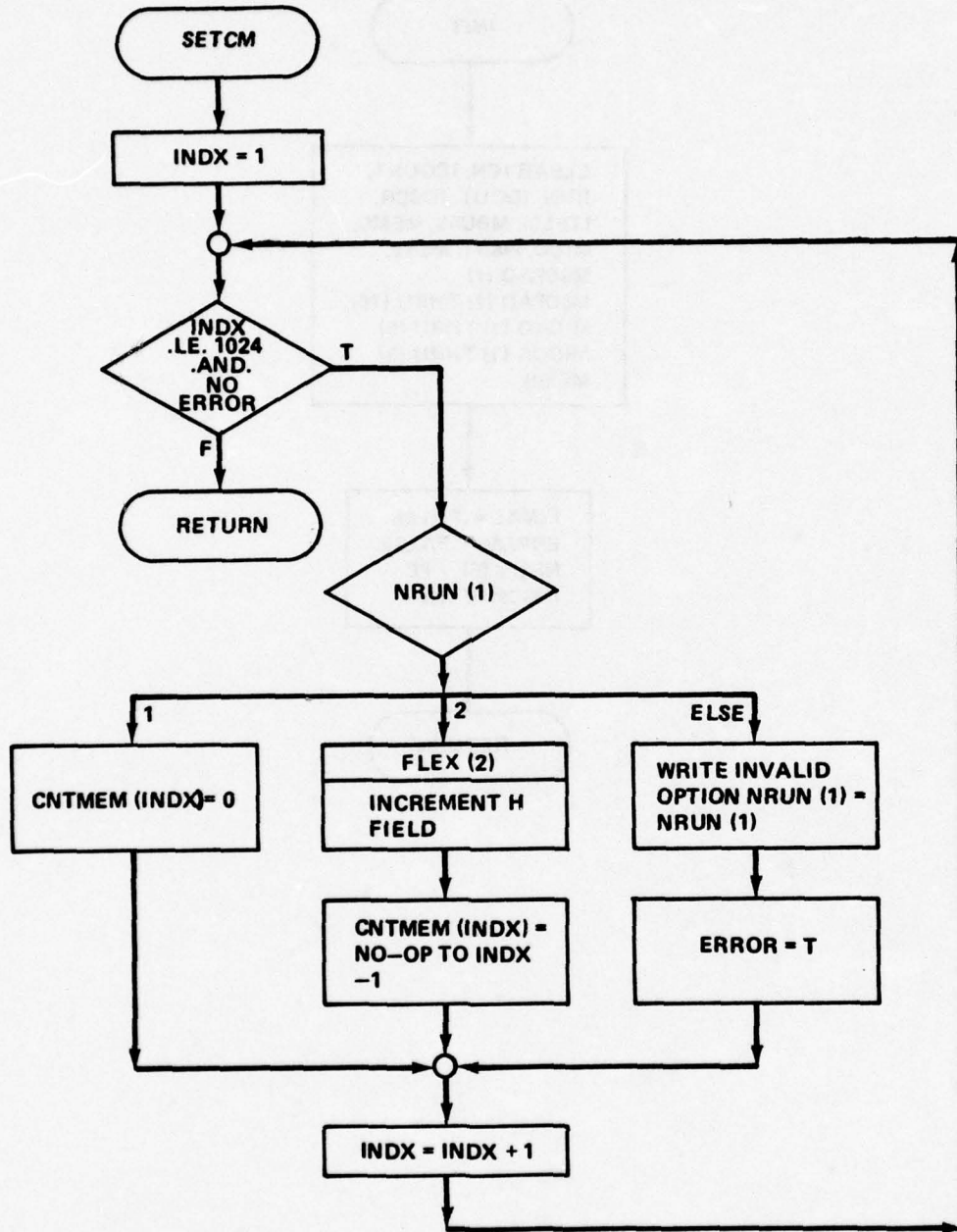
MULTIPURPOSE DIGITAL MICROPROCESSOR EMULATION MAIN PROGRAM



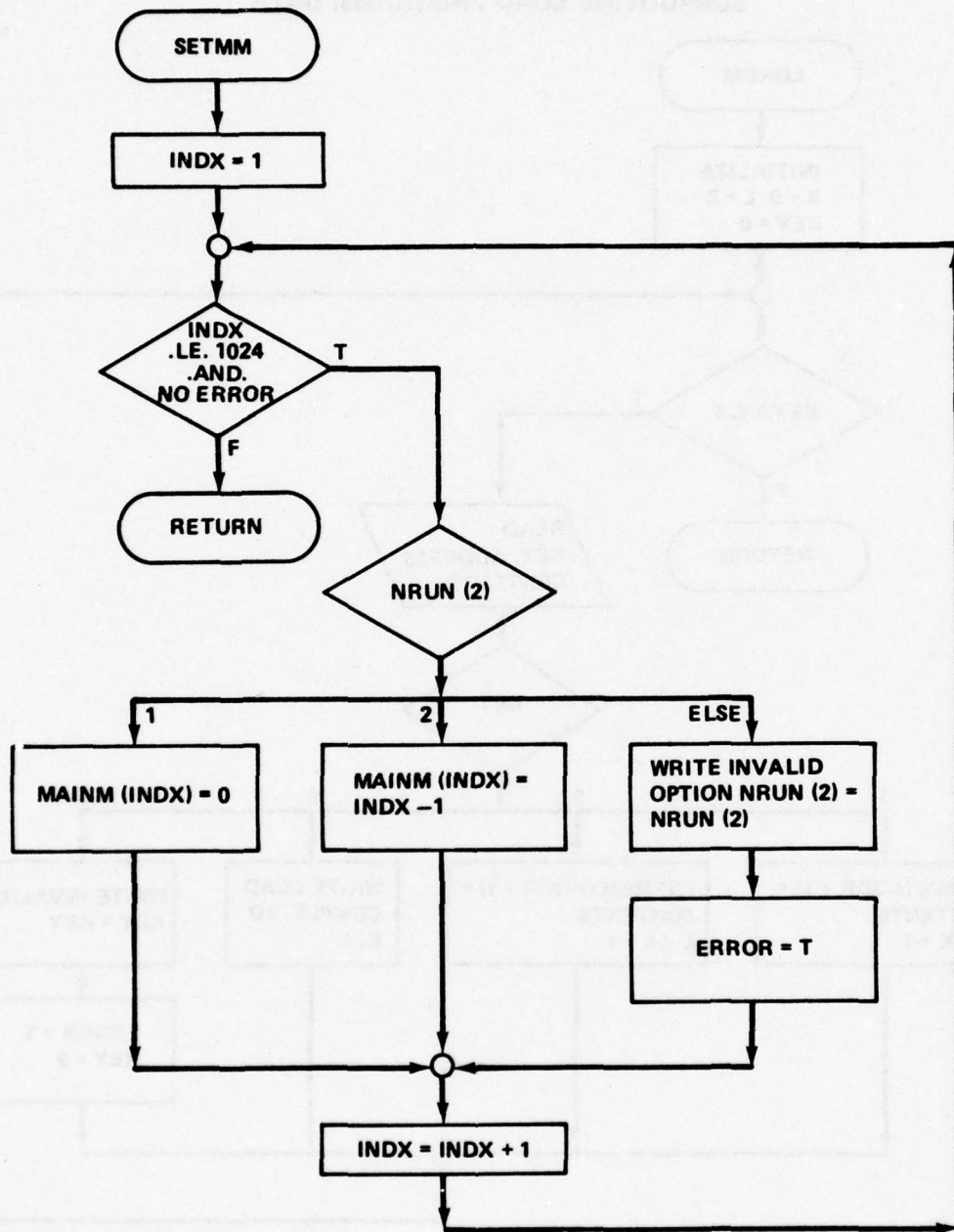
**SUBROUTINE INITIALIZE (REGISTERS AND DATA PATHS)**



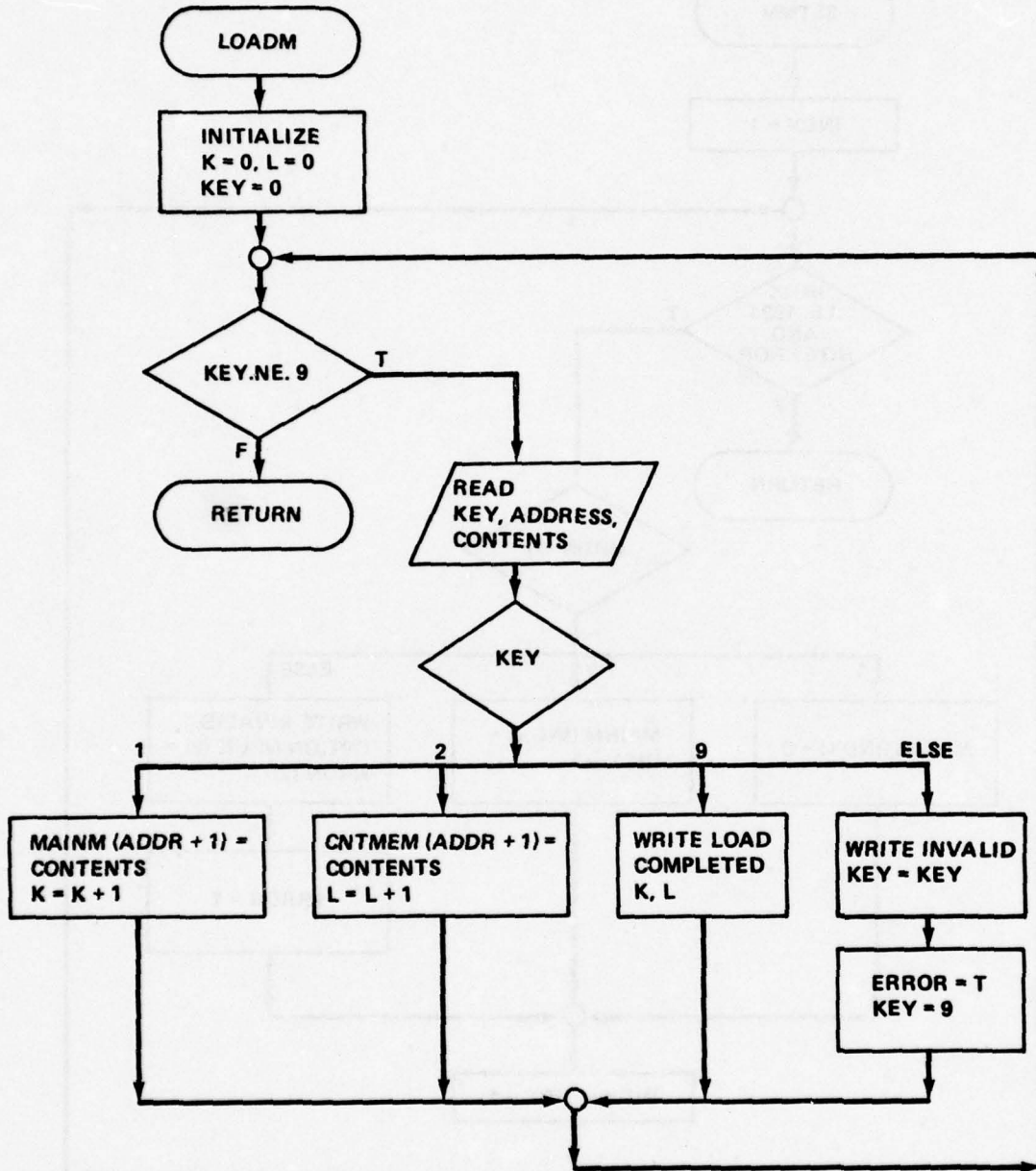
SUBROUTINE SET CONTROL MEMORY



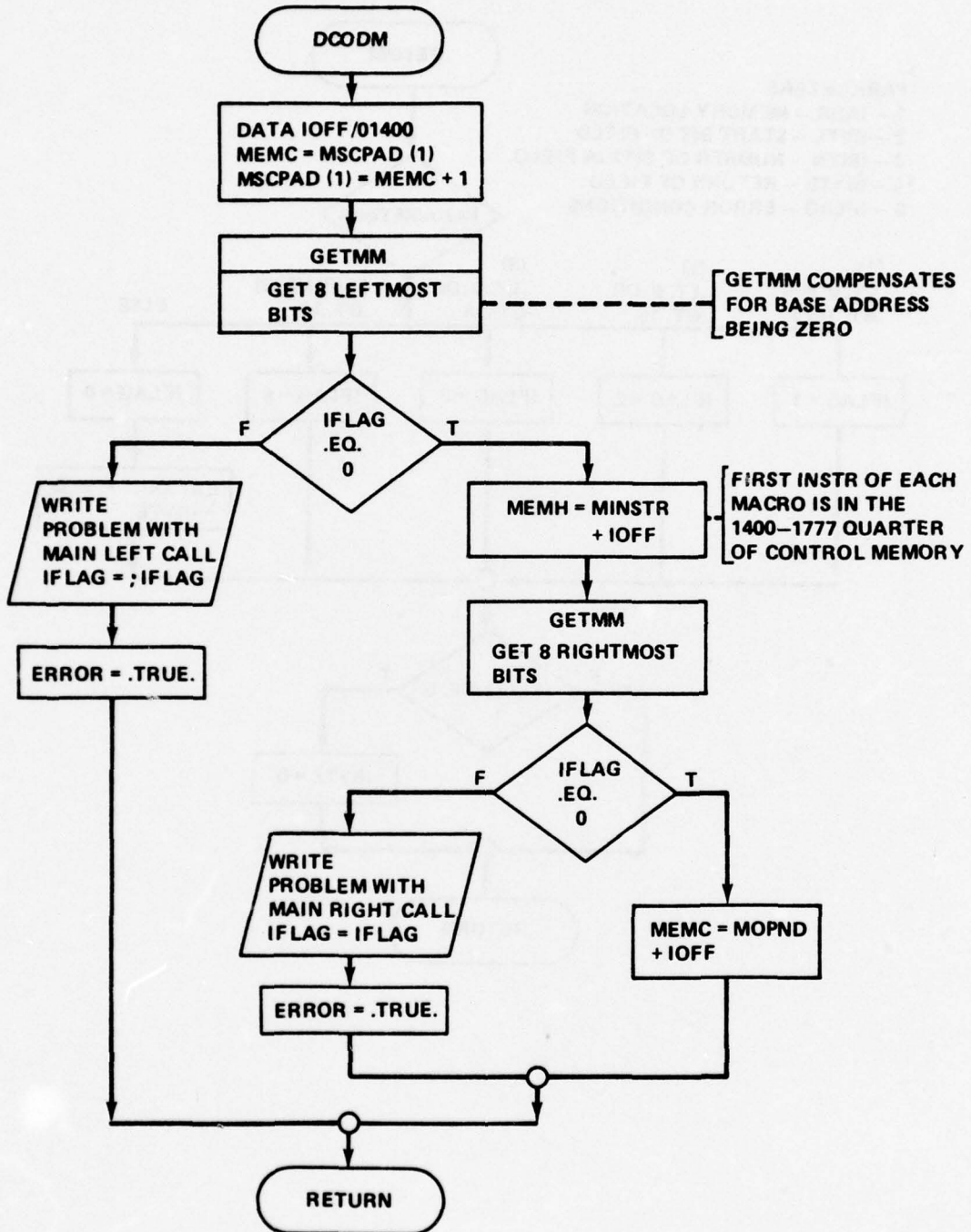
### SUBROUTINE SET MAIN MEMORY



SUBROUTINE LOAD PROGRAMS, DATA

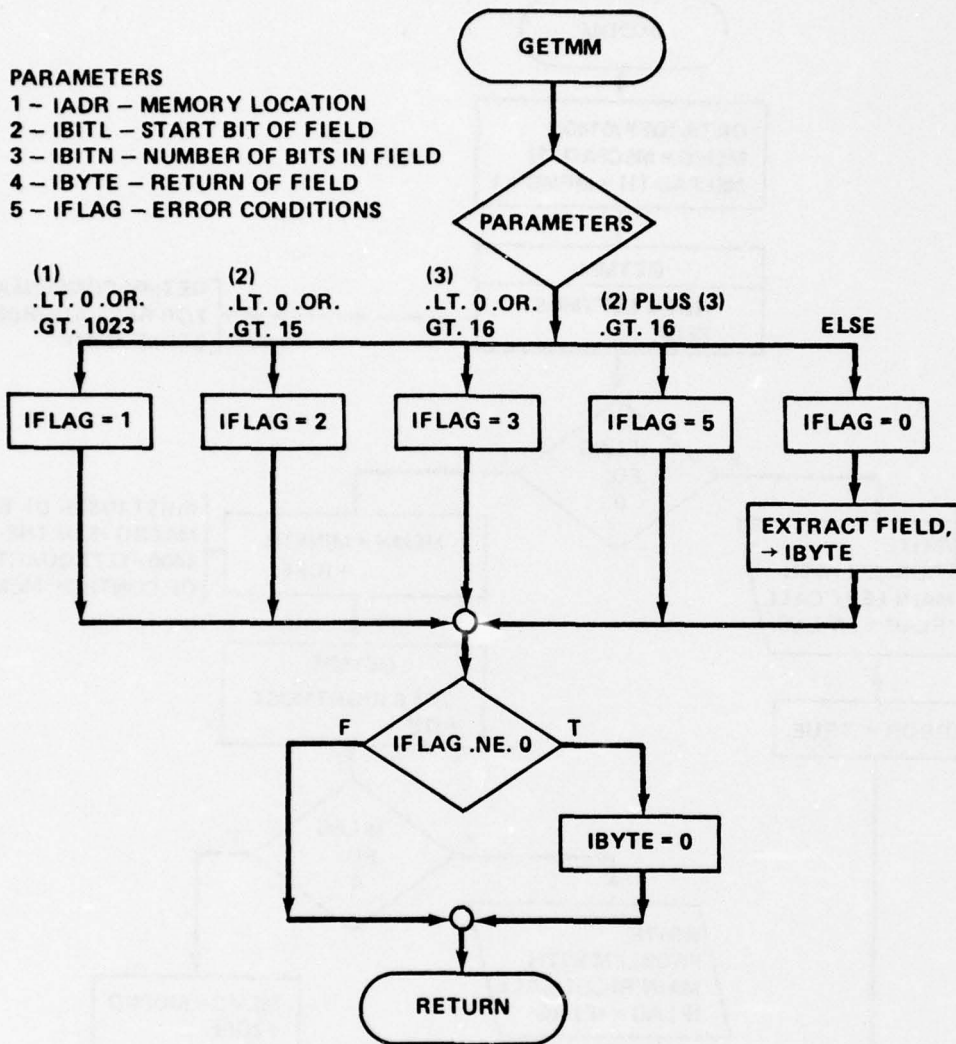


SUBROUTINE DECODE MAIN MEMORY WORD





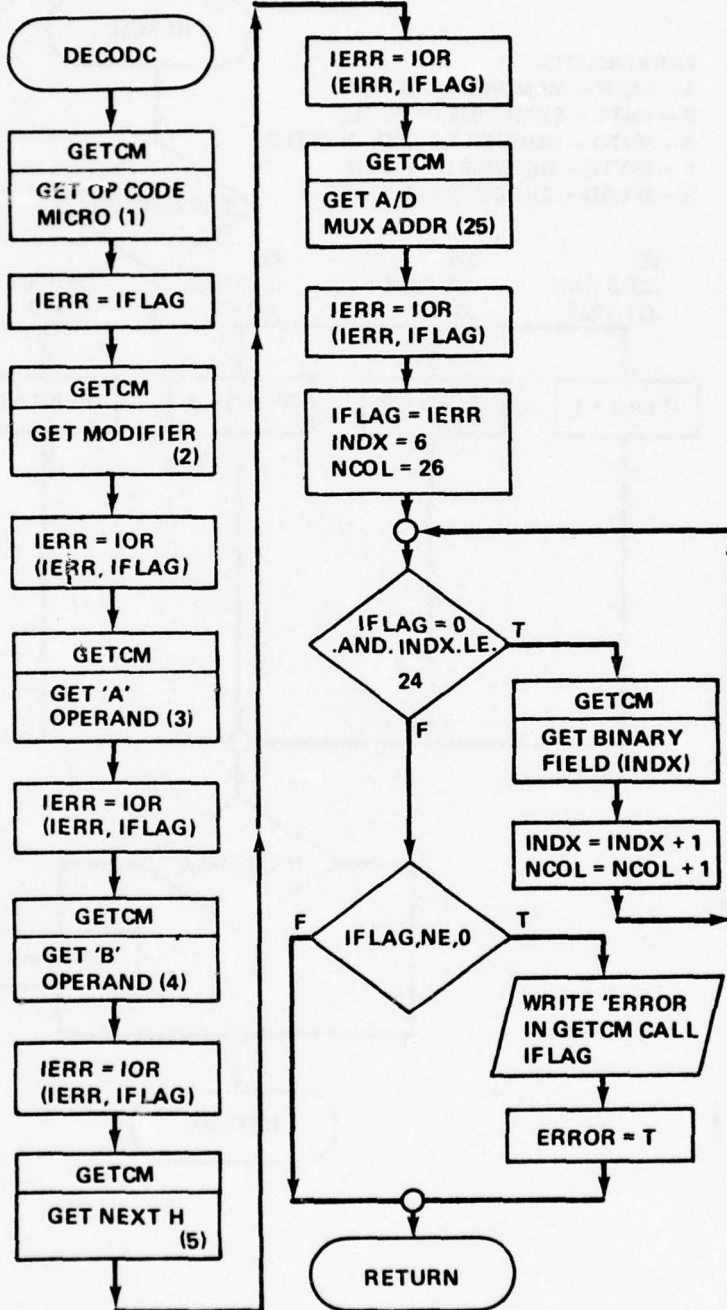
SUBROUTINE GET MAIN MEMORY FIELD



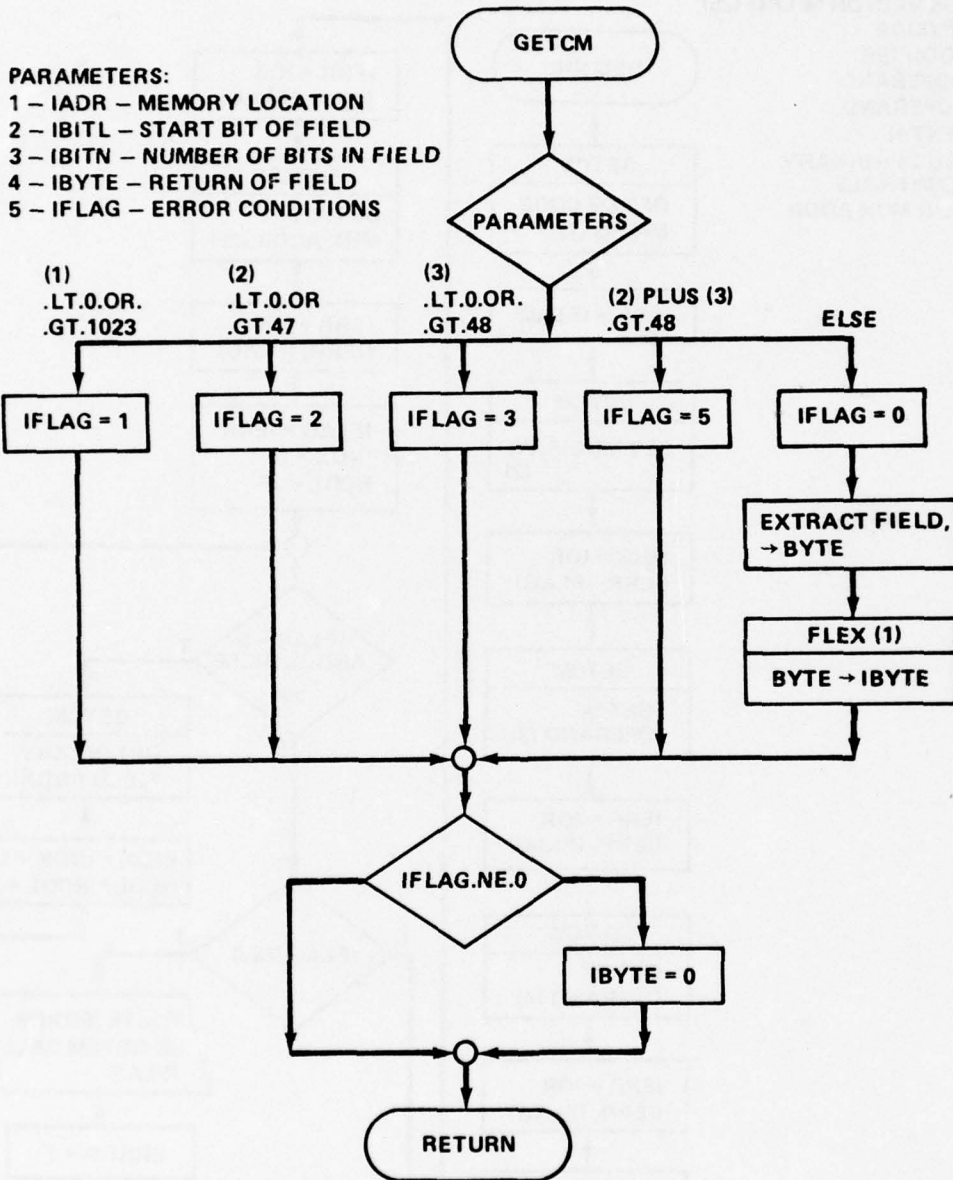
### SUBROUTINE DECODE CONTROL MEMORY WORD

LOADS VECTOR MICRO (25)

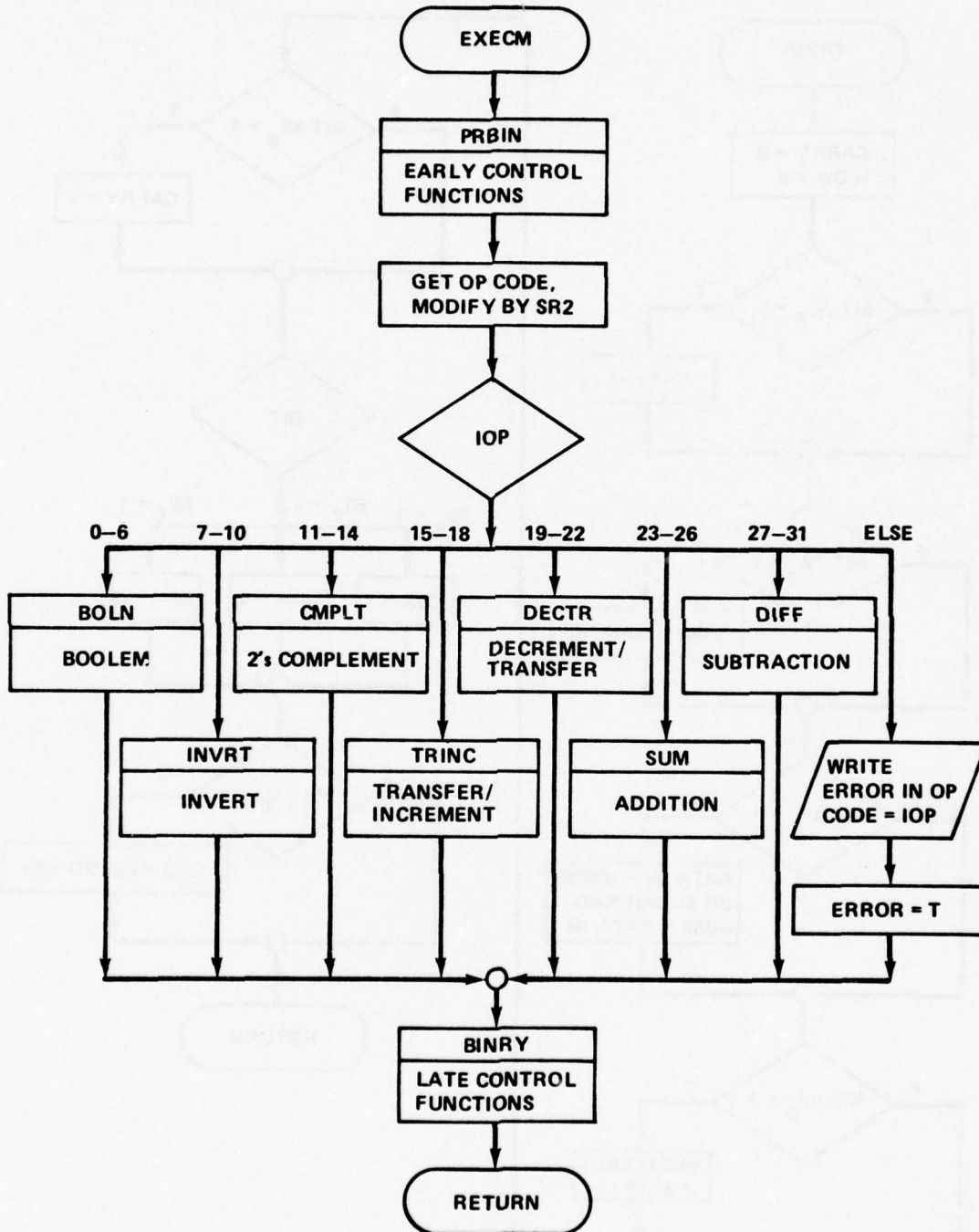
- 1 = OP CODE
- 2 = MODIFIER
- 3 = A OPERAND
- 4 = B OPERAND
- 5 = NEXT H
- 6 THRU 24 = BINARY CONTROLS
- 25 = A/D MUX ADDR



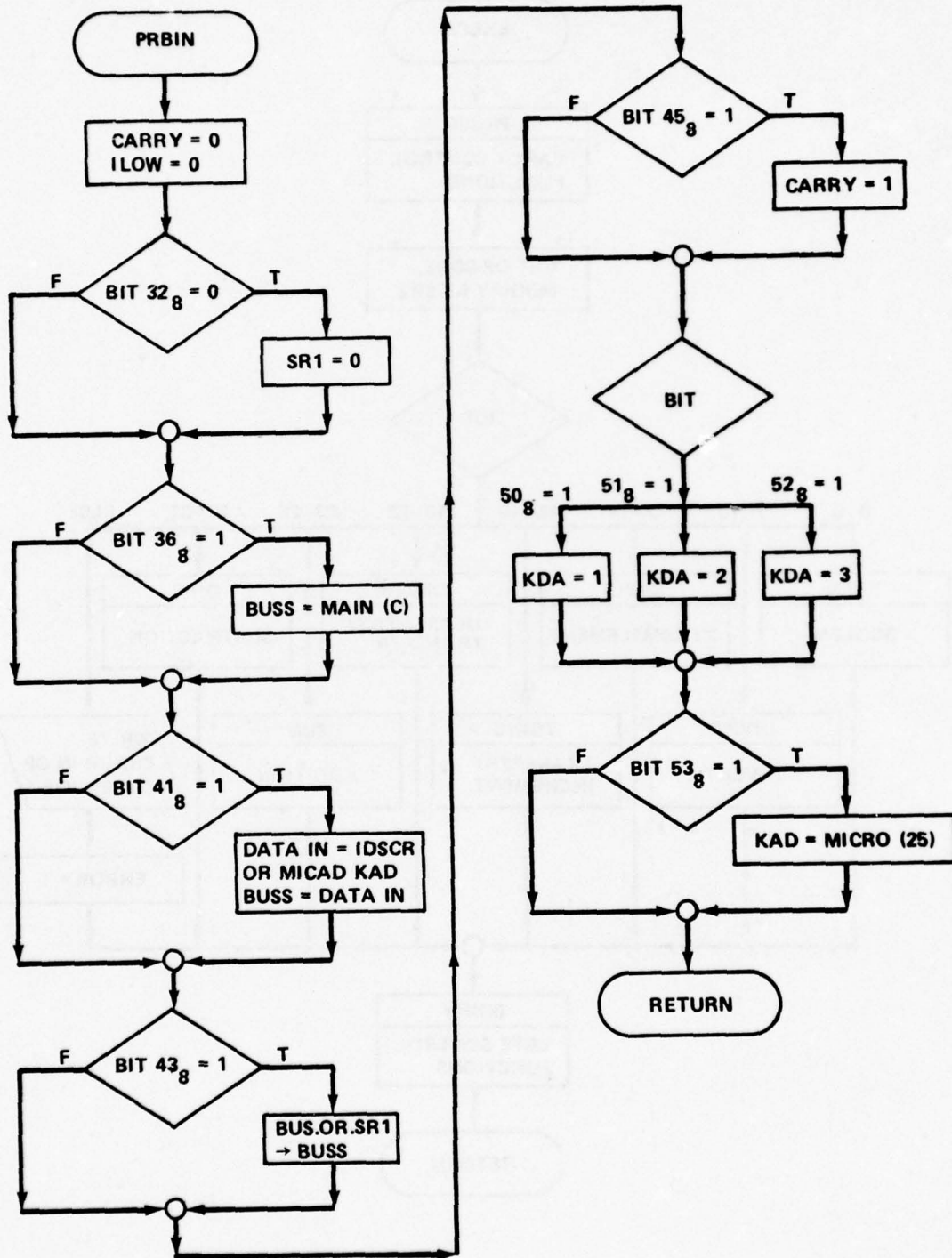
### SUBROUTINE GET CONTROL MEMORY FIELD



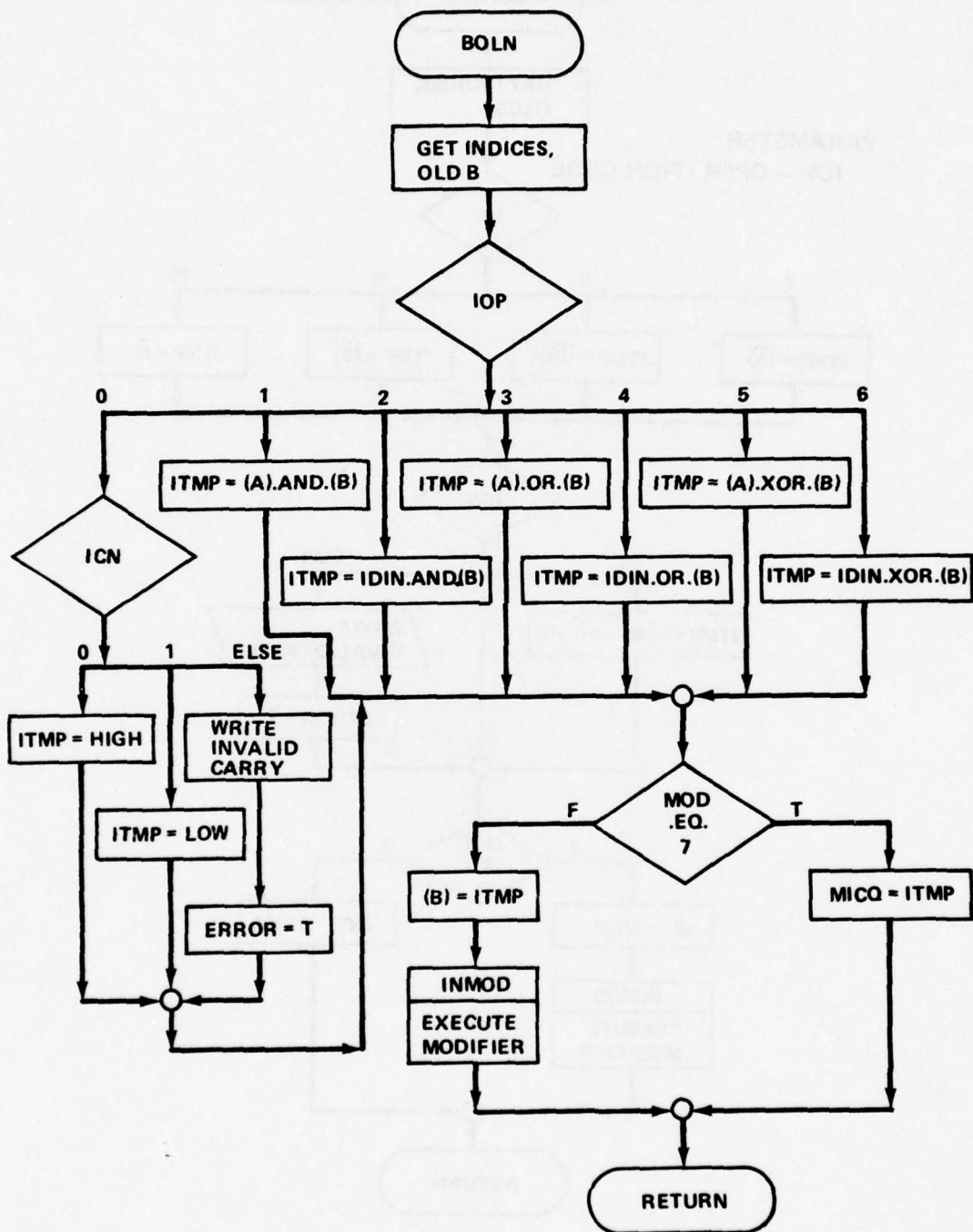
### SUBROUTINE EXECUTE MICROINSTRUCTION



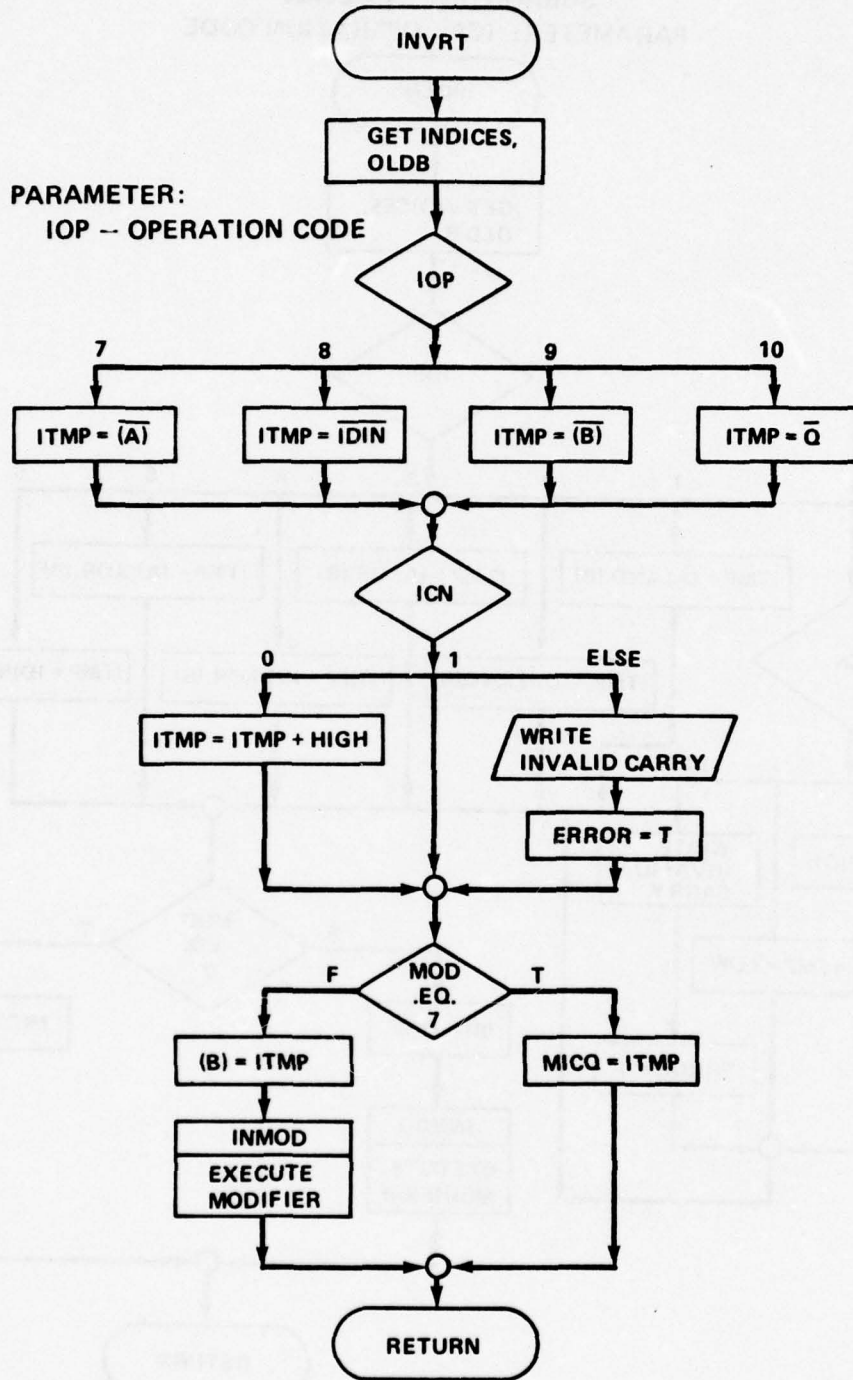
**SUBROUTINE PRE-BINARY EARLY CONTROL FUNCTIONS  
(BIT NUMBERS IN BINARY)**



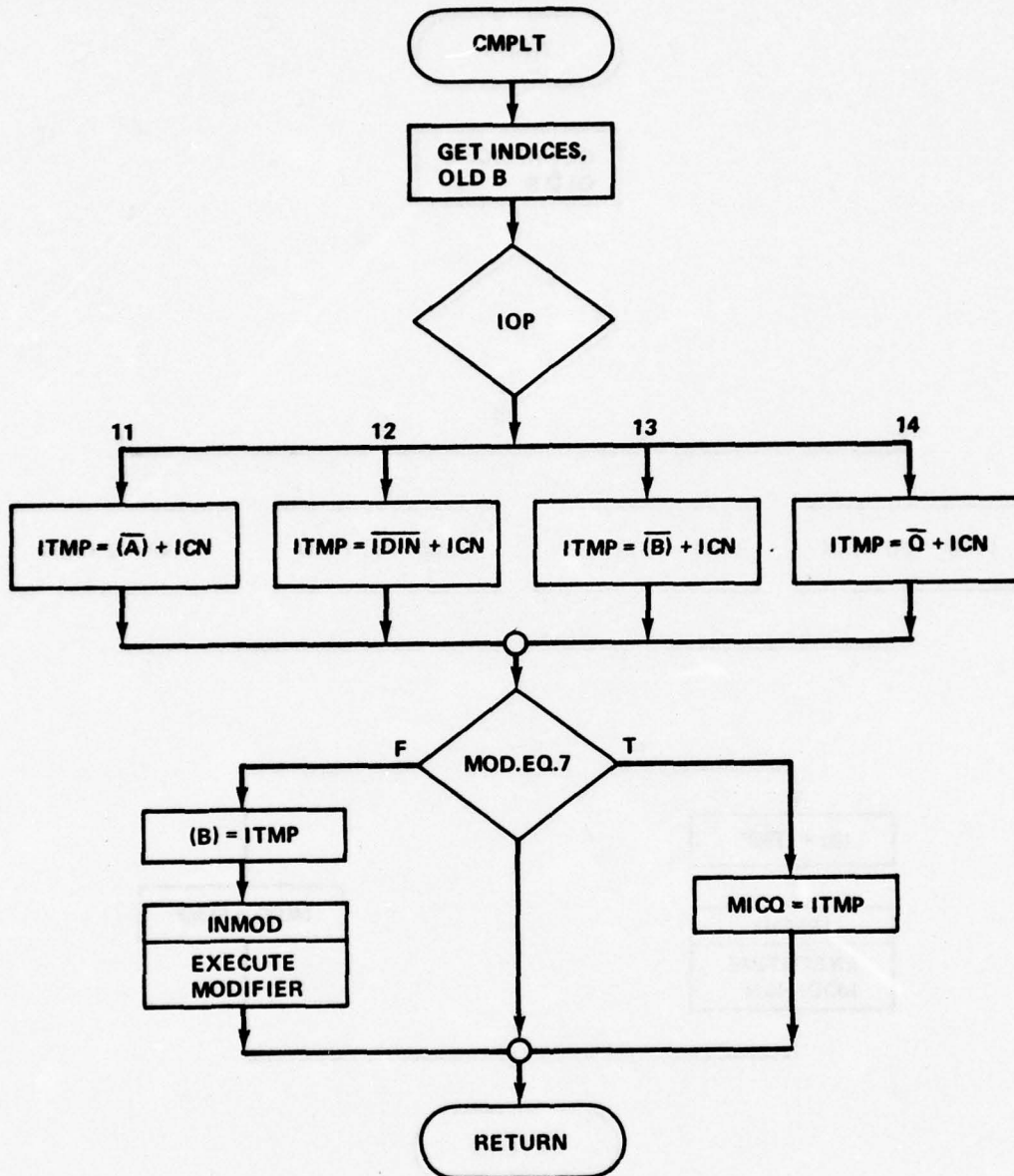
**SUBROUTINE BOOLEAN**  
**PARAMETER: IOP: OPERATION CODE**



### SUBROUTINE INVERT

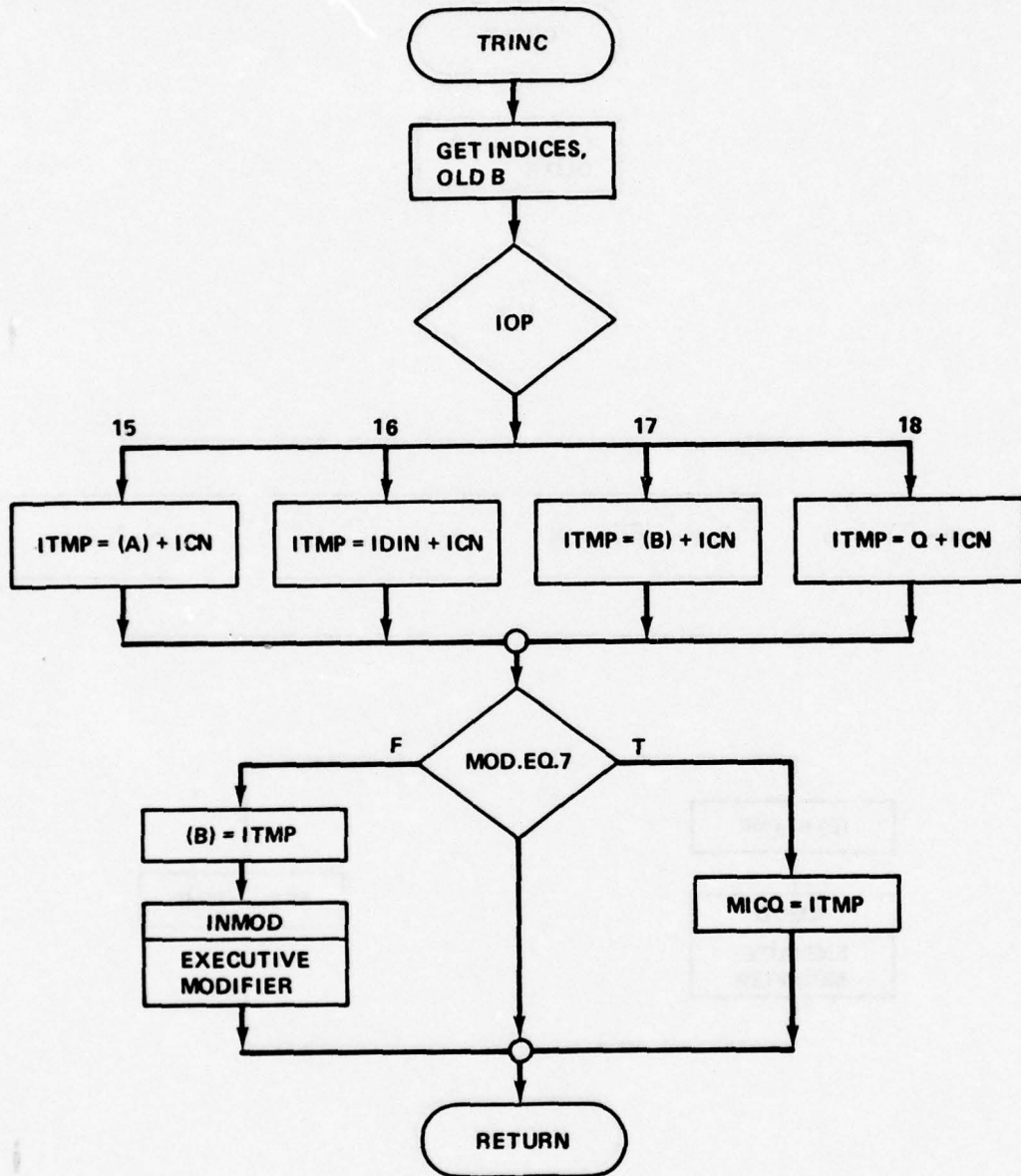


SUBROUTINE COMPLEMENT (2's) PARAMETER: IOP - OPERATION CODE

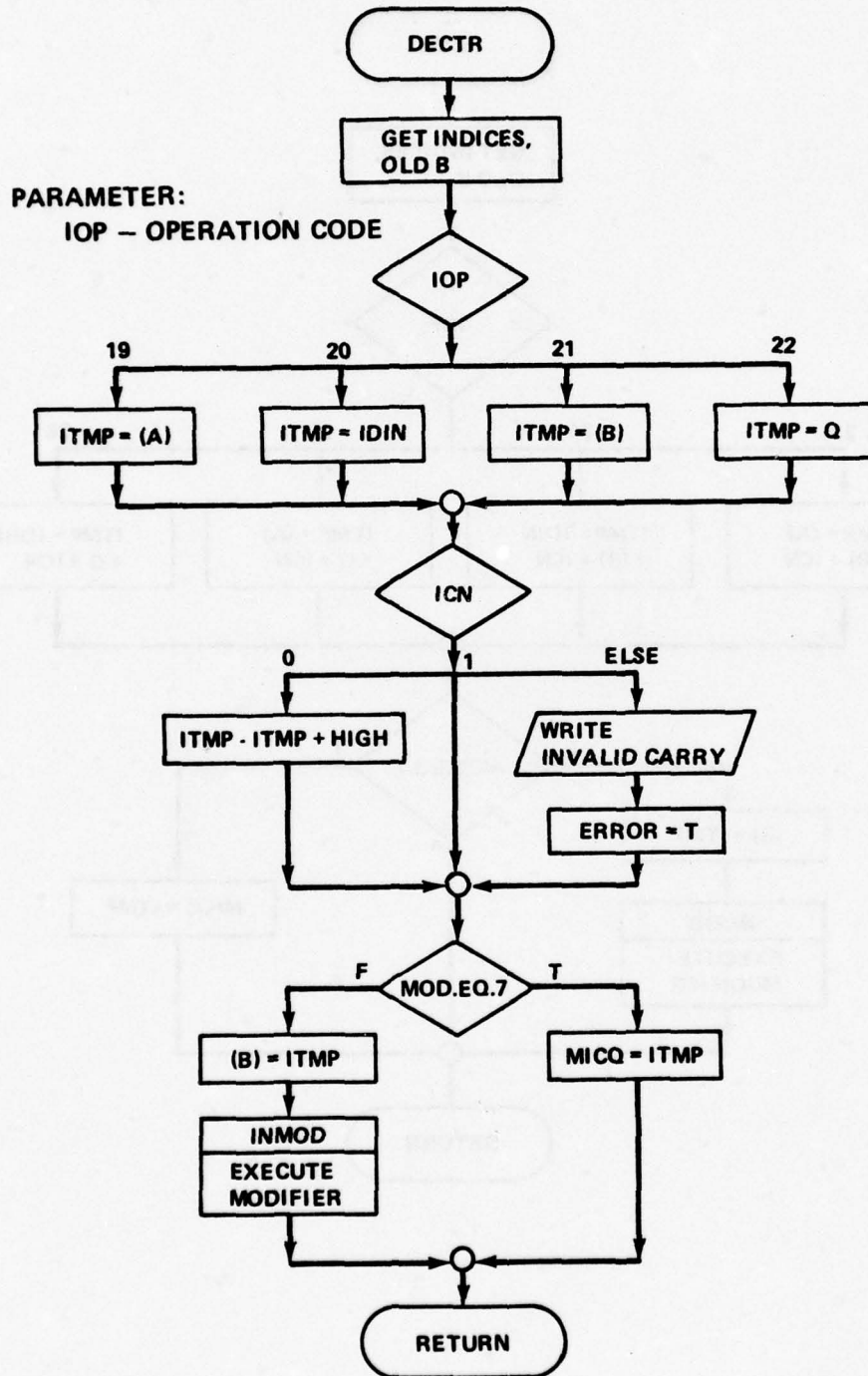




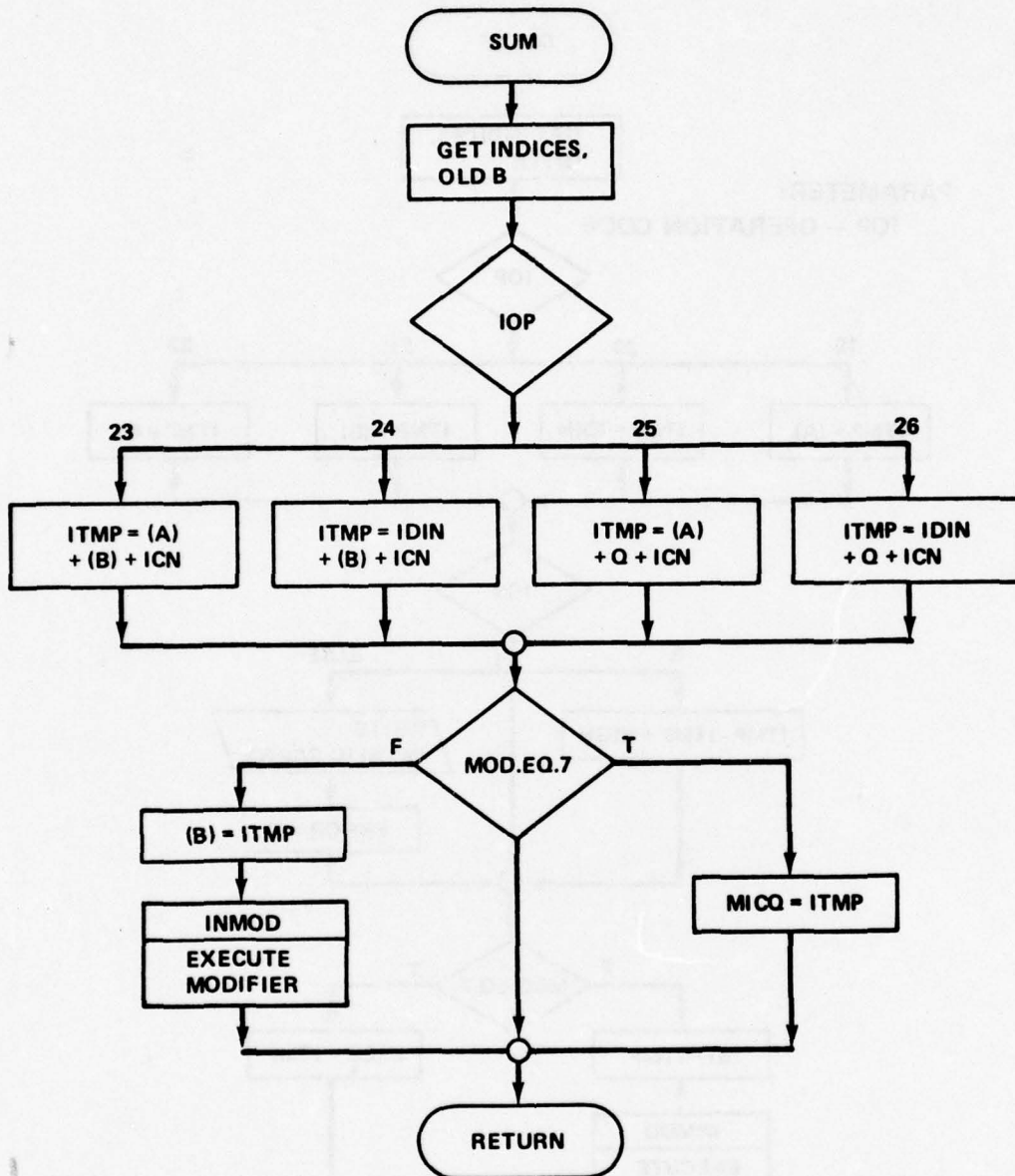
SUBROUTINE TRANSFER/INCREMENT PARAMETER: IOP - OPERATION CODE



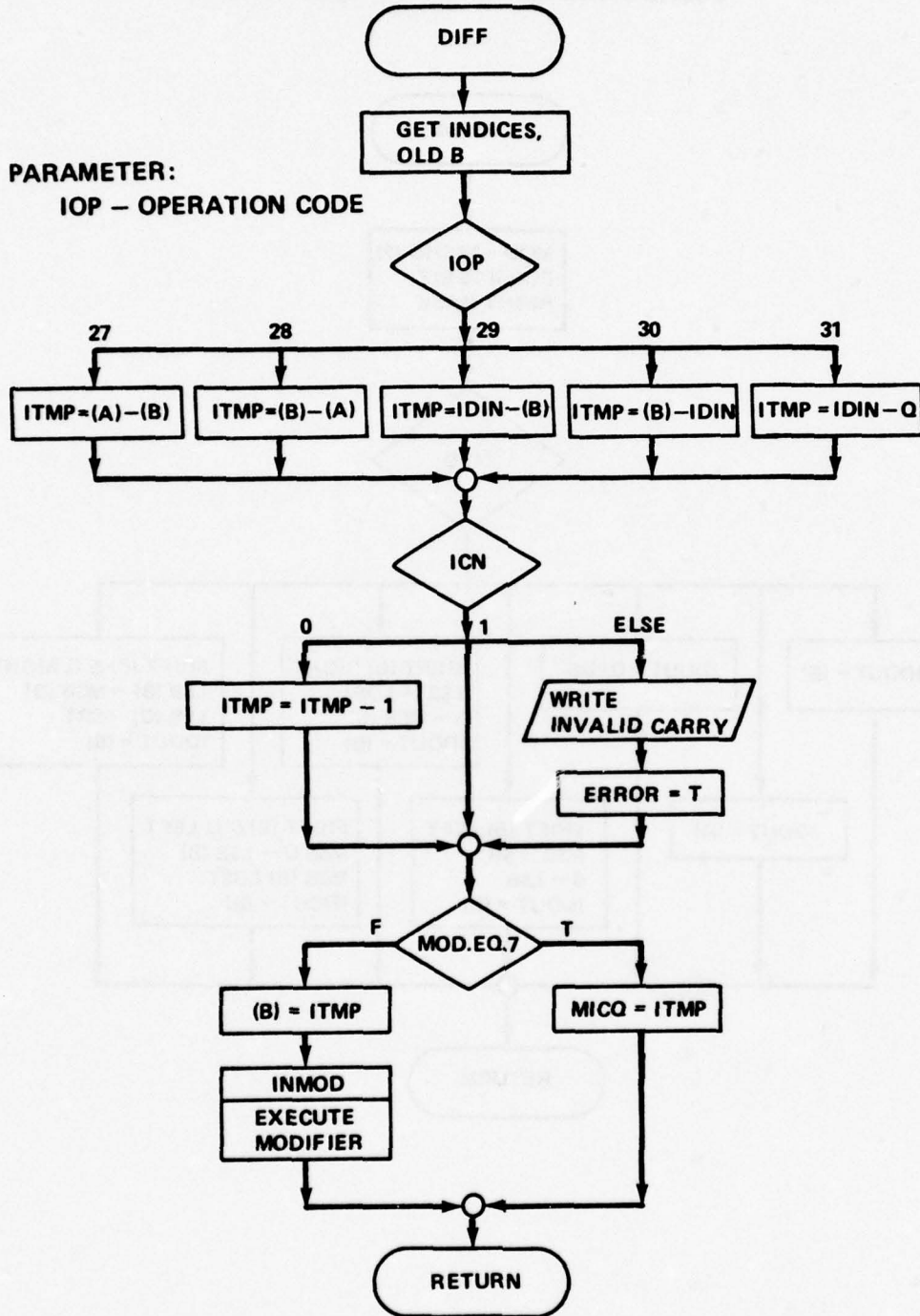
### SUBROUTINE DECREMENT/TRANSFER



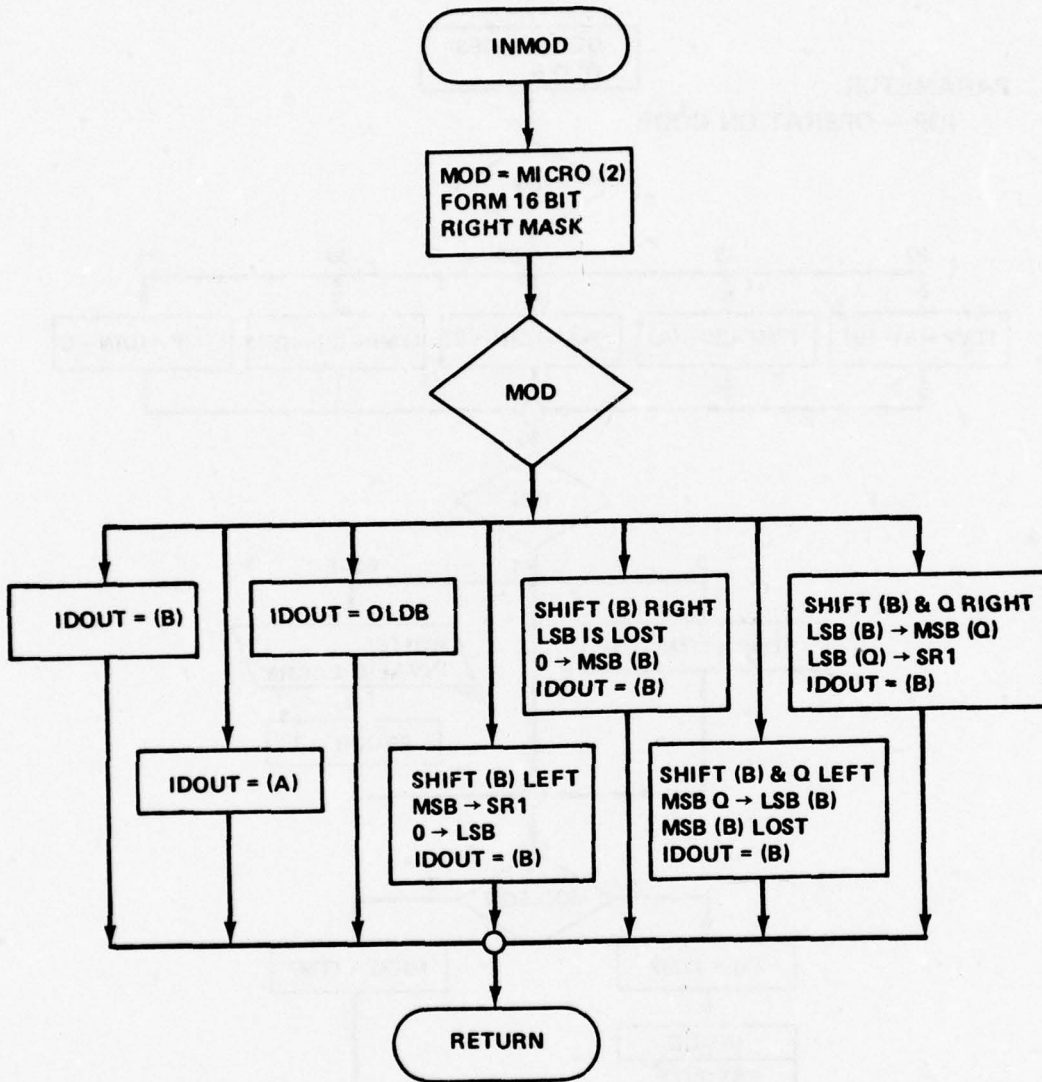
SUBROUTINE ADD PARAMETER: IOP - OPERATION CODE



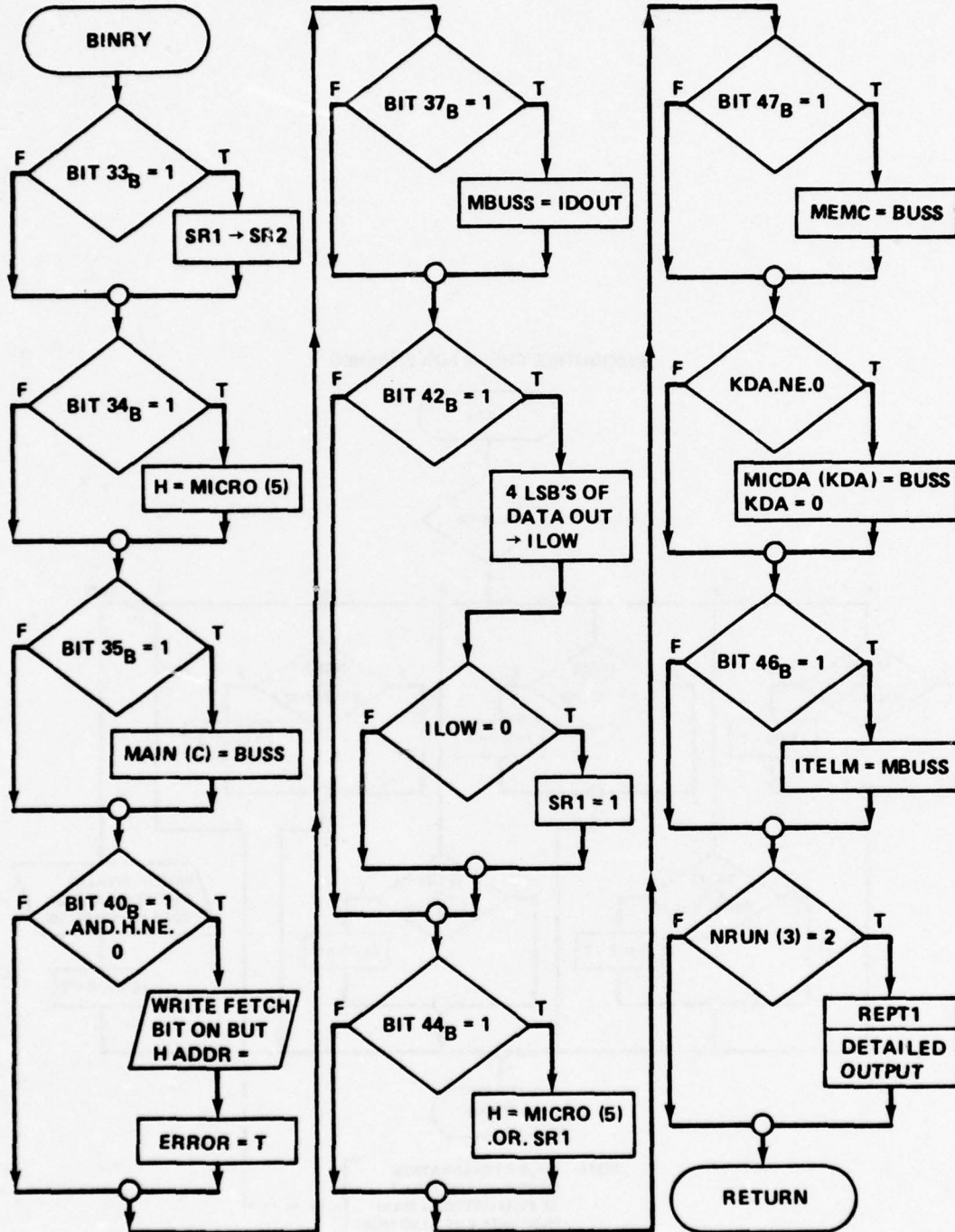
### SUBROUTINE SUBTRACT



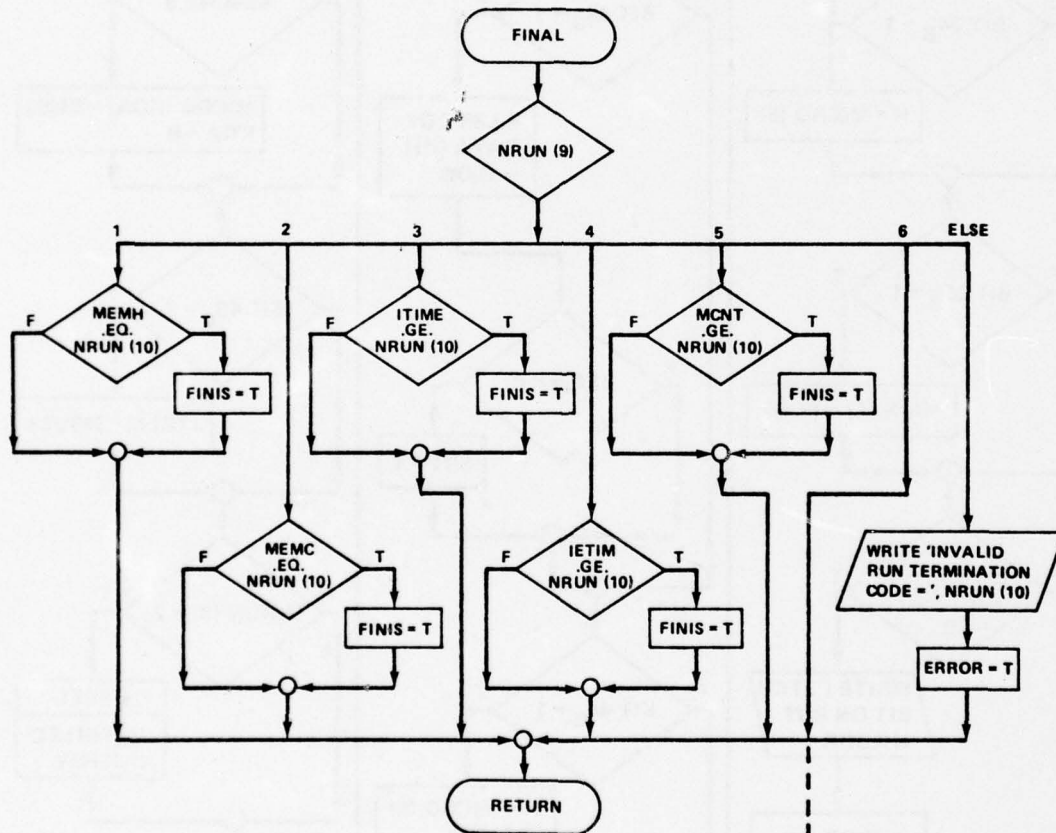
# SUBROUTINE INSTRUCTION MODIFICATION



SUBROUTINE BINARY BIT NUMBERS IN OCTAL

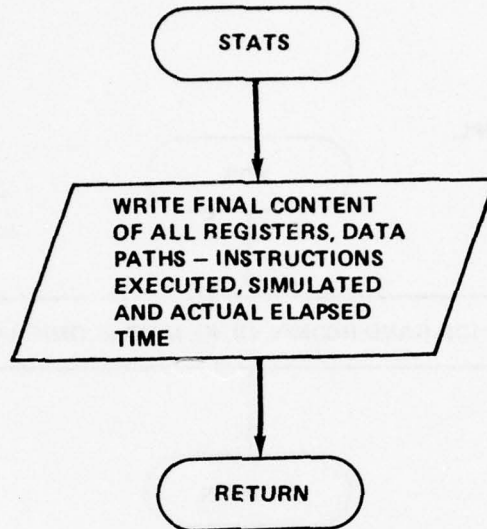


SUBROUTINE CHECK FOR FINISHED

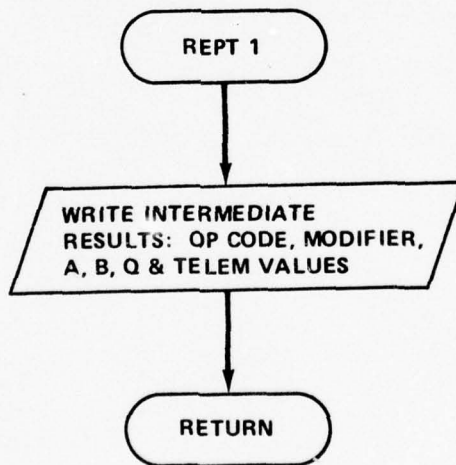


NOTE: CODE 6 TERMINATION (MICRO-COUNT) MUST BE EVALUATED IN MAIN PROGRAM, BUT ALSO MUST BE RECOGNIZED HERE.

**SUBROUTINE FINAL STATISTICS**



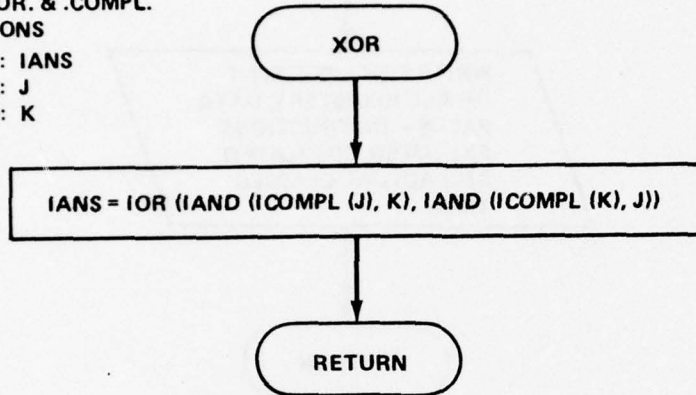
**SUBROUTINE DIAGNOSTIC OUTPUT**





**SUBROUTINE EXCLUSIVE OR (RAYTHEON R520 VERSION ONLY)**

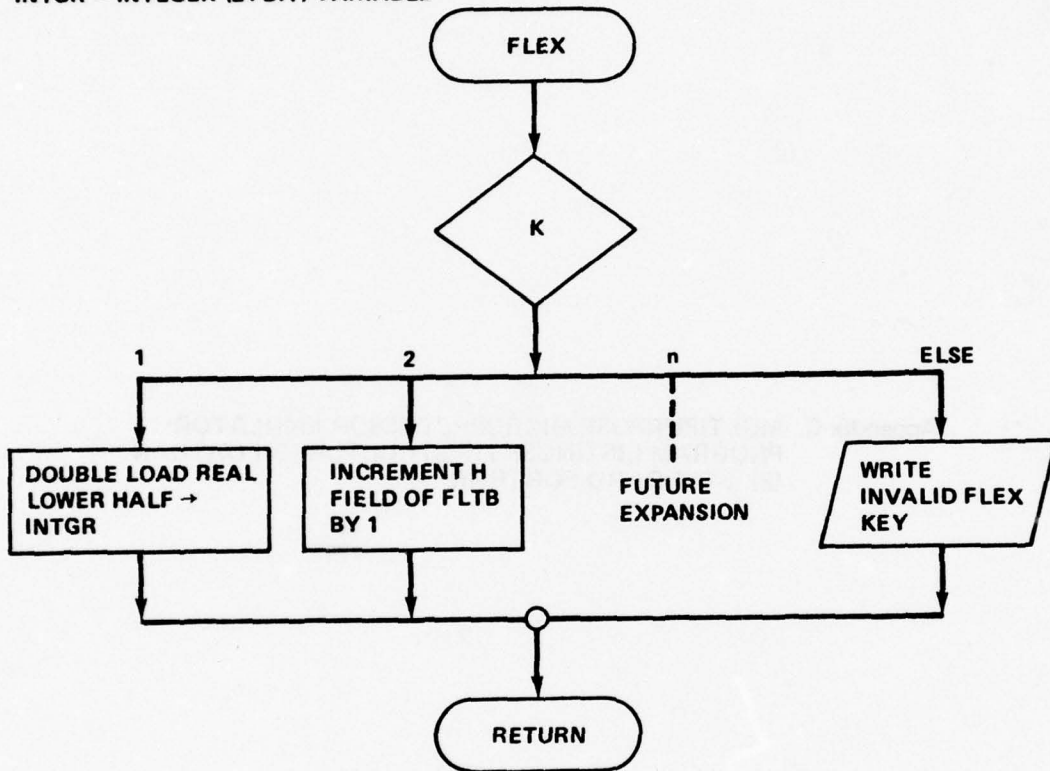
USING FORTRAN  
.AND., .OR. & .COMPL.  
FUNCTIONS  
ARG 1: IANS  
ARG 2: J  
ARG 3: K



**SUBROUTINE FLEXTRAN (RAYTHEON R520 VERSION ONLY)**  
**DIRECT R-520 CODE**

**PARAMETERS:**

**K** - KEY, = 1 FOR FLTB → INTGR  
          = 2 FOR INCREMENT H FIELD  
**FLTB** - REAL (48 BIT) VARIABLE  
**INTGR** - INTEGER (24 BIT) VARIABLE



**Appendix C. MULTIPURPOSE MICROPROCESSOR EMULATOR:  
PROGRAM LISTINGS: (1) STRUCTURED FORTRAN  
(2) STANDARD FORTRAN**

```

C
C PROGRAM ENUL (INPUT, OUTPUT, TAPES = INPUT, TAPE7=OUTPUT) 000110
C 000120
C 000130
C 000140
C PROGRAM NAME : MULTI-PURPOSE DIGITAL MICROPROCESSOR EMULATOR *000150
C T - 5 AUTOPILOT VERSION *000160
C *000170
C AUTHR : JERRY R BROOKSHIRE *000180
C US ARMY MISSILE COMMAND *000190
C *000200
C PROJECT : MULTI-PURPOSE DIGITAL MICROPROCESSOR *000210
C *000220
C DESCRIPTION : THIS PROGRAM ESTABLISHES THE MICROPROCESSOR *000230
C HARDWARE ENVIRONMENT, PRESETS MAIN AND CONTROL MEMORY *000240
C AREAS, LOADS THE 48-BIT CONTROL MEMORY AND THE 16-BIT *000250
C MAIN MEMORY, RETRIEVES, DECODES AND EXECUTES CONTROL *000260
C MEMORY (MICRO-) INSTRUCTIONS UNDER MAIN MEMORY SEQUENCE *000270
C CONTROL AND OUTPUTS COMPUTED VALUES PLUS PERFORMANCE *000280
C AND TIMING DATA UNDER RUN-OPTIONS AS SPECIFIED. *000290
C *000300
C CALLING SEQUENCE : MAIN PROGRAM *000310
C *000320
C SUBROUTINES CALLED : *000330
C SETCM - PRESET CONTROL MEMORY *000340
C SETMM - PRESET MAIN MEMORY *000350
C INIT - INITIALIZE ALL REGISTERS AND DATA PATHS *000360
C LOADM - LOAD MAIN AND CONTROL MEMORIES FROM CARDS (TAPE) *000370
C DCODE - DECODE MAIN MEMORY - SET PC, M, RESET C-REGS *000380
C EXECM - EXECUTE MICRO INSTRUCTION *000390
C FINAL - DETERMINE IF RUN IS COMPLETED OR ABORTED *000400
C *000410
C *000420
C *000430
C *000440
C *000450
C *000460
C *000470
C *000480
C *000490
C *000500
C *000510
C *000520
C *000530
C *000540
C *000550
C *000560
C *000570
C *000580
C *000590
C *000600
C *000610
C *000620
C *000630
C *000640
C *000650
C *000660
C
C LOGICAL FINISH ERROR
C COMMON CNTMEM(1024) , ICN , ICONT , IOIN ,
C IDOUT , IDSCR , ITEL4 , MAINM(1024) ,
C MBUSS , MEMC , MEM , MICAD(6) , MICDA(3) ,
C MICQ , MSCAD(16) , MSR1 , MSR2 ,
C NRUN(20) , FINIS , ERR01 , MINSTR , MOPND ,
C MICROTESTMENT , STEA , TTIME , IEFEM ,
C COMMON KAO , KDA , IOLJ3
C DATA LFTMS /3778/
C GET RUN CONTROL PARAMETERS
C READ (5, 10) NRUN
C LU FORMAT (23 0 4)
C WRITE (11, 80) NRUN

```

```

20 FORMAT (20) RUN CONTROL CARD = , 2304 , I
   LINCX = 0.00000075
   CALL INIT
   CALL SETCH
   CALL SETMM
   CALL LOADY
   MICS = 0
   IF (NRUN(1).EQ.1)
   THEN
C     PRINT MEMORY CONTENTS (PRE-EXECUTION) :
      M = 1
      WRITE (7, 80)
      FORMAT (10) MAIN DECODED, 26X, BHL LOCATION, 5X,
      17HMAIN DECODED, 11X, DEC, 90F, 3X, MEMORY LEFT ,
      5HRIGHT, 4X, IN CONTROL MEMORY, 7X, 9HDEC, OCT, 3X,
      17HMEMORY LEFT RIGHT, 8X, 15HCONTROL MEMORY // ,
      DO WHILE (N.LE.1024)
      MN = N - 1
      VR = N + 1
      MAIN = MAIN(M)
      MAINL = SHIF (MAIN, -8)
      MAINR = AND (MAIN, LFTMS)
      MAINJ = MAIN(MR)
      MAINS = AND (MAIN, LFTMS)
      WRITE (7, 90) (MAIN(M), MAIN(MR), MAINS, MAIN(MR))
      FORMAT (1H , 2X, 04, 3X, 06, 2X, 03, 2X, 03, 2X, 03, 2X, 03, 016 ,
      16, 2X, 04, 3X, 06, 2X, 03, 2X, 03, 2X, 03, 2X, 03, 016 )
      N = N + 2
      END DO
C     MAJOR CONTROL LOOP (EXECUTE MACRO) :
      DO WHILE (.NOT. (FINIS.OR.ERROR))
      CALL DCOM
      MINOR CONTROL LOOP (EXECUTE MICRO) :
      DO WHILE (MEM.NE.0)
      MMOLD = MEM
      CALL DCOM
      CALL EXEC
      IF (NRUN(1).EQ.2)
      THEN
C     OUTPUT EXECUTION DETAILS :
      N = MMOLD + 1
      WRITE (7, 10) MMOLD, MM(MEM), (MICRO(I), I = 1, 25)
      FORMAT (53) (THE FOLLOWING C4 INSTRUCTION HAS JUST BEEN EXECUTED: , 001120
      // 1H , 34, 5X, 015, 6(3X, 02), 4M H1 , 04, 2X, 20(1X, 11) // )
      M = 1
      DO WHILE (M.LE.16)
      K = M - 1
      WRITE (7, 30) K, MSCPAD(M)
      FORMAT (13) (3H SCRATCH PAD( , 02, 11H) CONTAINS , 06, 2H , )
      M = M + 1
      END DO
      WRITE (7, 50) IDIN, IDOJT, MBUSS, MEMC, ICH, MSR1, MSR2
      FORMAT (11) (DATA IN - 06, 13H, DATA OUT - 06, 9H, 0855 - 06,

```

```

*
*
*      1C, C-REG = ,08, /9M CARRY = ,11, 0H, SRL = ,11, 0H, SR2 = ,001230
*      IX, IX, I)
*
*      END IF
*      INCREMENT TIME AND MICRO COUNT
*      STIME = STIME + TINCRT
*      TIME = IFIX(STIME)
*      MICS = MICS + 1
*      IF (MICS.EQ.2)
*      THEN
*      WRITE (7, 99) STIME, TIME, MICS
*      FORMAT (1M0, F15.0, 5X, I6, 3X, I5)
*      END IF
*      CHECK FOR MICRO-COUNT TERMINATION
*      IF (MICS.EQ.8)
*      THEN
*      IF (MICS.GE. MRUN(10))
*      THEN
*      MEMM = 0
*      FINIS = .TRUE.
*      END IF
*      END DO
*      END DO
*      PRINT MEMORY CONTENTS (POST-EXECUTION)
*      N = 1
*      WRITE (7, 80)
*      DO WHILE (N.LE.1024)
*      NR = N + 1
*      MAIN = MAIN(N)
*      MAINR = SHFT (MAIN, -8)
*      MAINR = AND (MAIN, LTR8)
*      MAIN = MAIN(MR)
*      MAINJ = SHFT (MAIN, -6)
*      MAINS = AND (MAIN, LFT6)
*      WRITE (7, 9L) NR, MAIN(N), MAINL, MAINR, MAINS, MAINJ, MAINS, CMT ME(NR)
*      N = N + 2
*      END DO
*      END IF
*      CALL STATS
*      STOP
*      END

```

```

001253
001261
001270
001280
001290
001300
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001590
001600
001610
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001630
001640
001650
001660
001670
001680
001690
001700

```

0 ERRORS FOUND IN THIS ROUTINE. 15 CARDS READ. 130 CARDS OUTPUT.

```

SUBROUTINE INIT
C*****
C ONE TIME INITIALIZATION OF ALL REGISTERS AND DATA PATHS
C INCLUDING SETTING OF PC AND H REGISTERS FROM RUN CONTROL CARD
C*****
C
C LOGICAL FINIS , ERROR
COMMON CNTMEM(102) , ICN , ICOUNT , IOIM ,
1 IDOUT , IDSCR , ITEL , MAINM(102) ,
2 MRUSS , MENC , MEM , MICAD(6) , MICDA(13) ,
3 MICG , MSCP(101) , MSRI , MSR2 ,
4 MRUN(26) , FINIS , ERGR , MINSTR , MOPND ,
5 MICRO(125) , MCNT , STIME , IETIM , IETIM ,
COMMON KAD , KDA , IOL03
ICN = J
ICOUNT = J
IOIM = 0
IDOUT = 0
IDSCR = 0
I TELM = 0
KAD = 0
KDA = J
MRUSS = 0
MENC = 0
MICG = 0
MSRI = 0
MSR2 = 0
MSCP(101) = MRUN(15)
DO WHILE (MLE.16)
MSCPAD(1) = 0
N = N + 1
END DO
N = 1
DO WHILE (N.LE.5)
MICAD(N) = 0
N = N + 1
END DO
MICDA(1) = 0
MICDA(2) = 0
MICDA(3) = 0
FINIS = .FALSE.
ERROR = .FALSE.
MCNT = 0
STIME = 0.6
IETIM = 0
IETIM = 0
RETURN
END

```

51 CARDS OUTPUT.

33 CARDS READ.

5 ERRORS FOUND IN THIS ROUTINE.

```

SUBROUTINE DQ00C
C
C*****
C      LOGICAL FINIS , ERROR
C      COMMON  CNTMR(1024) , ICN , ICOUNT , IDIN ,
C      IDOUT , IDSCR , ITELW , MAINH(1024) ,
C      INUSS , IMWC , IMEM , MICHA(10) , MICO(13) ,
C      MICQ , MSPAD(16) , MSRI , MSR2 ,
C      MRUN(20) , PIMS , ERROR , MINSTR , MOPND ,
C      MICRO(25) , MCNT , STIME , IETIM ,
C      COMMON  KAD , KDA , IOLOS
C      DATA MSK1 /50/
C      IPTR = MEMM
C      IERR = 0
C      CALL GETCM (IPTR, 0, 5, MOP, IFLAG)
C      OPERATION CODE BITS 2 AND 3 STORED INVERTED, SO FIX!
C      MICRO(1) = XOR (MSK1, MOP)
C      IERR = IFLAG
C      CALL GETCM (IPTR, 5, 3, MOP, IFLAG)
C      MICRO(2) = MOP
C      IERR = OR (IERR, IFLAG)
C      CALL GETCM (IPTR, 8, 4, MOP, IFLAG)
C      MICRO(3) = MOP
C      IERR = OR (IERR, IFLAG)
C      CALL GETCM (IPTR, 12, 4, MOP, IFLAG)
C      MICRO(4) = MOP
C      IERR = OR (IERR, IFLAG)
C      CALL GETCM (IPTR, 16, 10, MOP, IFLAG)
C      MICRO(5) = MOP
C      IERR = OR (IERR, IFLAG)
C      CALL GETCM (IPTR, 25, 5, MOP, IFLAG)
C      MICRO(25) = MOP
C      IERR = OR (IERR, IFLAG)
C      IFLAG = IERR
C      MCOL = 26
C      INDX = 6
C      DO WHILE (IFLAG.EQ.0)
C      CALL GETCM (IPTR, MCOL, 1, MOP, IFLAG)
C      MICRO(INDX) = MOP
C      MCOL = MCOL + 1
C      INDX = INDX + 1
C      ENDO DO
C      IF (IFLAG.EQ.0)
C      THEN
C      IF (MRUN(13).EQ.2)
C      THEN
C      WRITE (7, 5) MEMM, MICRO(15)
C      FORMAT ( ' SMITHS INSTR AT: , 04, 12M, M-FIELD = , 04, 2M . )
C      FORMAT ( '
C      ENDO IF
C      ENDO
C      WRITE (7, 10) IFLAG
C      FORMAT ( ' JMC INVALLD CALL TO GETCM FROM DQ00C, IFLAG = , 12, 14. )
C      END IF
C      RETURN
C      ENDO
C      0 ERRORS FOUND IN THIS ROUTINE. 55 CARDS READ. 59 CARDS OUTPUT.

```

```

002440
002290
002260
002270
002280
002290
002300
002310
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002940
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002960
002970
002980
002990
003000
003010
003020
003030
003040
003050
003060
003070
003080
003090
003100
003110
003120
003130
003140
003150
003160
003170
003180
003190
003200
003210
003220
003230
003240
003250
003260
003270
003280
003290
003300

```



## PREPROCESSOR FOR STRUCTURED FORTRAN IV PROGRAMS    U.S. ARMY MISSILE COMMAND, AMSMI-RGG(MISEI)

```

C
C *****
C SUBROUTINE INMOD (IA, IB)
C *****
C SIMULATE ACTIVITY GENERATED BY INSTRUCTION MODIFIER, MICRO(I2)
C *****
C
C LOGICAL FINIS , ERROR
COMMON CHMEM(I2), ICN , ICOUNT , IOIN ,
      IOOUT , IOSCR , ITELN , MAINM(I2),
      MBUSS , MEMC , MEMM , MICAD(I3) ,
      MLCQ , MSCPAD(I6) , MSRI , MSR2 ,
      MKONT(20) , PINEP , ERRCJ , SHSTR , MOPND ,
      MICRO(I2) , MCNT , STIME , IETIM
      COMMON KAD , KDA , IOLDB
DATA KMASK /177778/
DATA IIRBIT /1000000/
IOP = MICRO(I1)
MOP = MICRO(I2)
IF (MOD.EQ.0)
  THEN
    IOOUT = MSCPAD(18)
    OR IF (MOD.EQ.1)
      THEN
        IOOUT = MSCPAD(I2)
    OR IF (MOD.EQ.2)
      THEN
        IOOUT = IOLDB
    OR IF (MOD.EQ.3)
      THEN
        LEFT SHIFT OFF BIT FROM B GO:IS TO SKIT
        IIRBIT.EQ.1
        THEN
          MSRI = 1
        ELSE
          MSRI = 0
        END IF
        MSCPAD(I3) = AND ((SHIFT(MSCPAD(I3),I1),KMASK)
        IOOUT = MSCPAD(I3)
        OR IF (MOD.EQ.4)
          THEN
            RIGHT SHIFT OFF BIT FROM B
            MSCPAD(I3) = SHIFT(MSCPAD(I3),-1)
            MSCPAD(I3) = OR(MSCPAD(I3),IIRBIT)
            IOOUT = MSCPAD(I3)
        OR IF (MOD.EQ.5)
          THEN
            LEFT SHIFT OFF BIT FROM B RES-JOES TO L5B OF 0
            LEFT SHIFT OFF BIT FROM B GO:IS TO SR1
            IIRBIT = SHIFT(MSCPAD(I3),-1)
            IF (IIRBIT.EQ.1)
              THEN
                MSRI = 1
            ELSE
                MSRI = 0
          END IF
        END IF
  END IF

```

```

MSR1 = 0
003430
END IF
003440
IBIT = SHIFT (MICQ, -15)
003450
MICQ = AND ( SHIFT (MICQ, 1) , KMASK )
003460
MICQ = OR (MICQ, 1)
003470
MSPAD (IB) = AND (SHIFT (MSPAD (IB), 1) , KMASK)
003480
MSPAD (IB) = OR (MSPAD (IB), IBIT)
003490
IDOUT = MSPAD (IB)
003500
OR IF (MOD.EQ.6)
003510
THEN
003520
C RIGHT SHIFT OFF BIT FROM Q-REG TO SR1, LSB OF B INTO MSB OF Q:
003530
IF, LOW-BIT FROM Q = 1, SR1 = 0; ELSE SR1 = 1)
003540
IBIT = AND (MSPAD (IB), 1)
003550
IBIT = SHIFT (IBIT, 15)
003560
LOBIT = AND (MICQ, 1)
003570
IF (LOBIT.EQ.0)
003580
THEN
003590
ELSE
003600
MSR1 = 1
003610
ELSE
003620
MSR1 = 0
003630
END IF
003640
MICQ = SHIFT (MICQ, -1)
003650
MICQ = OR (MICQ, IBIT)
003660
MSPAD (IB) = SHIFT (MSPAD (IB), -1)
003670
MSPAD (IB) = OR (MSPAD (IB), IMIBIT)
003680
IDOUT = MSPAD (IB)
003690
ELSE
003700
WRITE (7, 5) MOD
003710
FORMAT (26H INVALID INSTR MODIFIER = ,04,15H. RUN HALTED. )
003720
ERROR = .TRUE.
003730
END IF
003740
IF (NRUN(3).EQ.2) WRITE (7, 10) MOD, IDOUT
003750
FORMAT (13H0 INSTR MOD = ,11,21H JJST SET DATA-OUT = ,08, 1H.)
003760
IF (NRUN(3).EQ.2.OR.NRUN(3).EQ.3)
003770
THEN
003780
CALL REPT2
003790
END IF
003800
RETURN
003810
END

```

0 ERRORS FOUND IN THIS ROUTINE. 35 CARDS READ. 103 CARDS OUTPUT.

```

C SUBROUTINE EXECM 003820
C***** 003830
C 003840
C EXECUTE CONTROL MEMORY INSTRUCTION 003850
C***** 003860
C 003870
C***** 003880
C 003890
C LOGICAL FINIS , ERROR 003900
COMMON CNTMEM(1024) , ICN , ICOUNT , IDIM , 003910
IDOUT , IDSCR , IELM , MAINM(1024) , 003920
MSUSS , MEMG , MEMY , MICAD(16) , MICDAT(3) , 003930
MICQ , MSCPAD(16) , MSRI , MSR2 , 003940
NRUNT(20) , FINIS , ERROR , MINSTR , MOPND , 003950
MICRO(25) , MCNT , STIME , ITIME , IETIM , 003960
COMMON KAD , KDA , IOLDS 003970
EXECUTE APPLICABLE CONTROL FUNCTIONS BEFORE INSTR EXECUTION: 003980
CALL PRBIN 003990
IF (MSR2.EQ.1) 004000
THEN 004010
MICRO(1) = OR (MICRO(1) , 6) 004020
IF (NRUM(3).EQ.2) WRITE (7 , 23) MICRO(1) 004030
FORMAT (15H)OP CODE NOW = , 02, 15H DUE TO SR2 = 1. ) 004040
20 END IF 004050
IOP = MICRO(1) 004060
IF (IOP.EE.5.AND.IOP.LE.6) 004070
THEN 004080
CALL B0LN (IOP) 004090
OR IF (IOP.EE.7.AND.IOP.LE.10) 004100
THEN 004110
CALL INVRT (IOP) 004120
OR IF (IOP.EE.11.AND.IOP.LE.14) 004130
THEN 004140
CALL CMLPT (IOP) 004150
OR IF (IOP.EE.15.AND.IOP.LE.18) 004160
THEN 004170
CALL TRINC (IOP) 004180
OR IF (IOP.EE.19.AND.IOP.LE.22) 004190
THEN 004200
CALL DECTR (IOP) 004210
OR IF (IOP.EE.23.AND.IOP.LE.26) 004220
THEN 004230
CALL SUM (IOP) 004240
OR IF (IOP.EE.27.AND.IOP.LE.31) 004250
THEN 004260
CALL DIFF (IOP) 004270
ELSE 004280
WRITE (7 , 18) IOP 004290
FORMAT (18H)INVALID OP CODE: , I2, 22H ENCOUNTERED IN EXECM. ) 004300
ERRR = .TRUE. 004310
END IF 004320
CALL GINRY 004330
ICOUNT = ICOUNT + 1 004340
RETURN 004350
END 004360
0 ERRORS FOUND IN THIS ROUTINE. 35 CARDS READ. 62 CARDS OUTPUT.

```

```

C
C SUBROUTINE FINAL
C *****
C
C EVALJATE RUN TERMINATION OPTIONS - SET FINIS = .TRUE. WHEN TRUE
C *****
C
C LOGICAL FINIS ; ERROR
COMMON CMTMEM(1024) ; ICM ; ICOUNT ; IOIN ;
1 IOOUT ; IDSCR ; IEL4 ; MAINM(1024) ;
2 MBUSS ; MEMC ; MEMY ; MICRO(16) ; MICRO(13) ;
3 MICQ ; MSCPAD(16) ; MSRI ; MSR2 ;
4 NRUNT(20) ; FINIS ; ERR3 ; MINSFR ; MOPND ;
5 MICRO(25) ; MCNT ; STIME ; IETIM ;
COMMON KAD ; KDA ; IOL3 ;
NEND = NRUN(9)
NVAL = NRJN(10)
IF (NEND.EQ.1)
THEN
IF (MEMH.EQ.NVAL)
THEN
FINIS = .TRUE.
END IF
OR IF (NEND.EQ.2)
THEN
IF (MEMC.EQ.NVAL)
THEN
FINIS = .TRUE.
END IF
OR IF (NEND.EQ.3)
THEN
IF (ITIME.GE.NVAL)
THEN
FINIS = .TRUE.
END IF
OR IF (NEND.EQ.4)
THEN
IF (IETIM.EQ.NVAL)
THEN
FINIS = .TRUE.
END IF
OR IF (NEND.EQ.5)
THEN
IF (MONT.GE.NVAL)
THEN
FINIS = .TRUE.
END IF
OR IF (NEND.EQ.6)
THEN
ELSE
WRITE (7, 5) NEND
FORMAT (31HCINVALID RUN TERMINATION CODE = , I3, 1H. )
ERROR = .TRUE.
END IF
RETURN
END
0 ERRORS FOUND IN THIS ROUTINE. 571 CARDS READ. 67 CARDS OUTPUT.

```

```

SUBROUTINE SETMM
C      004940
C      004950
C*****
C      004960
C      004970
C      004980
C      004990
C      005000
C      005010
C*****
C      005020
C      005030
C      005040
C      005050
C      005060
C      005070
C      005080
C      005090
C      005100
C      005110
C      005120
C      005130
C      005140
C      005150
C      005160
C      005170
C      005190
C      005200
C      005210
C      005220
C      005230
C      005240
C      005250
C      005260
C      005270
C      005280
C      005290
C      005300

      THIS ROUTINE PRESETS MAIN MEMORY TO A VALUE DESIGNATED BY THE
      RUN CONTROL CARD, INCLUDING THE ABILITY TO SET EVERY LOCATION
      TO BE A NO-OP POINTING TO ITSELF

      LOGICAL FINIS , ERROR
      COMMON CNTMEM(1024) , ICN , ICOUNT , IDIN ,
      IOUT , IOSCR , ITEL , MAINM(1024) ,
      MBUSS , MEMC , MEMT , MICAD(16) , MICDA(3) ,
      MICQ , MSCPAD(16) , MSR1 , MSR2 ,
      NRUN(26) , FINIS , ERROR , MINSTR , MOPND ,
      MICRO(25) , MCNT , STIME , ITIME , IETIM ,
      COMMON KAD , KDA , IOLDB
      DATA MSK / 377B /
      INDX = 1
      DO WHILE (.NOT.ERROR.AND.INDX.LE.1024)
      IF (NRUN(2).EQ.1)
      THEN
      MAINM(INDX) = 0
      OR IF (NRUN(2).EQ.2)
      THEN
      NEIDX = INDX - 1
      MAINM(INDX) = AND (NEIDX, MSK)
      ELSE
      WRITE (7, 1) NRUN(2)
      FORMAT (4MCSETHM CALLED WITH INVALID OPTION NRUN(2) = , I3, 1H.)
      ERROR = .TRUE.
      END IF
      INDX = INDX + 1
      END DO
      RETURN
      END
  
```

0 ERRORS FOUND IN THIS ROUTINE. 37 CARDS READ. 35 CARDS OUTPUT.

```

SUBROUTINE SETCH
005310
C*****005320
C*****005330
C*****005340
C THIS ROUTINE PRESETS CONTROL MEMORY TO A VALUE DESIGNATED BY THE *005350
C RUN CONTROL CARD, INCLUDING THE ABILITY TO SET EVERY LOCATION *005360
C TO BE A NO-OP POINTING TO ITSELF. *005370
C REPL A DOUBLE-WORD ZERO, REPL2 IS ALIGNED TO INCREMENT THE *005380
C H-FIELD BY 1, PRESET -1 SO 1ST WILL BE 0, AND LOAD NEXT H BIT ON *005390
C*****005400
C*****005410
C*****005420
C*****005430
C*****005440
C*****005450
C*****005460
C*****005470
C*****005480
C*****005490
C*****005500
C*****005510
C*****005520
C*****005530
C*****005540
C*****005550
C*****005560
C*****005570
C*****005590
C*****005600
C*****005610
C*****005620
C*****005630
C*****005640
C*****005650
C*****005660
C*****005670
C*****005680
C*****005690
C*****005700
C*****005700

LOGICAL FINIS , ERROR
COMMON CNTMEM(1024) , ICN , ICOUNT , IDIN ,
1 IDOUT , IOSCR , ITELN , YAINM(1024) ,
2 MBUSS , MEMC , MEMH , MICAD(6) , MICOA(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 NRUN(20) , FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25) , MCNT , STIMEI , ITIME , IETIM
COMMON KAD , KDA , IOLDR
DATA REPL /08/, REPL2 /5377777620.00008/
DATA ADDR /200000008/
INDX = 1
DO WHILE (.NOT.FERROR.AND.INDX.LE.1:24)
IF (NRUN(1).EQ.1)
THEN
CNTMEM(INDX) = REPL
OR IF (NRUN(1).EQ.2)
THEN
REPL2 = REPL2 + ADDR
CNTMEM(INDX) = REPL2
ELSE
WRITE (7, 10) NRUN(1)
FORMAT (44H)SEICH CALLED WITH INVALID OPTION NRUN(1) = , I3,1H. )05640
ERROR = .TRUE.
END IF
INDX = INDX + 1
END DO
RETURN
END

```

0 ERRORS FOUND IN THIS ROUTINE. 40: CARDS READ. 36 CARDS OUTPUT.

```

C*****
C SUBROUTINE LOADM
C*****
C COL 1 = 1; MAIN MEMORY
C COL 1 = 2; CONTROL MEMORY
C COL 1 = 9; LOAD COMPLETED
C CONTIGUOUS MEMORY IMAGES (NRUN(1)) = 1;
C COLS 5-12 = ADDRESS, OCTAL
C COLS 13-20 = MAIN MEMORY CONTENTS - OCTAL
C COLS 21-35 = CONTROL MEMORY CONTENTS - OCTAL
C MICRO-FIELD IMAGES (NRUN(1)) = 2;
C COLS 3-6 = ADDRESS, OCTAL
C COLS 15-18 = INSTRUCTION TOP CODE - OCTAL
C COL 17 = INSTRUCTION MODIFIER (OCTAL)
C COLS 18-19 = A OPERAND (OCTAL)
C COLS 20-21 = B OPERAND (OCTAL)
C COLS 22-25 = NEXT M ADDRESS (OCTAL)
C COLS 26-33 = BINARY CONTROL FIELDS PLUS A/D MUX ADDR
C*****
C LOGICAL FINIS , ERROR
COMMON CNTRM(1024) , ION , ICOUNT , IDIN ,
1 IOUT , IOSCR , ITELN , MAINM(1024) ,
2 MBUSS , MEMC , MEMY , MICRO(6) , MICORT(3) ,
3 MICQ , MSCPAD(16) , MSKI , MSK2 ,
4 MRUN(24) , FINIS , ERRQ , MINSTR , MOPND ,
5 MICRO(25) , MCNT , STIME , IETIM
COMMON KAD , KDA , IOLDB
DIMENSION CNTRFLD(16)
DATA MSKI /1400000000000000/
KEY = 0
K = J
L = J
IF (NRUN(1).EQ.1)
THEN
DO WHILE (KEY.NE.9)
READ (5, 10) KEY, MADR, MAIN, CNTRL
FORMAT (I1, 7X, 04, 2X, 05, 016)
IF (KEY.EQ.1)
THEN
MAIN(MADR+1) = MAIN
K = K + 1
OR IF (KEY.EQ.2)
THEN
INVERT BITS 2,3 OF 02 CODE (0-01)
CNTRM(MADR+1) = XOR (MSKLY CNTRL)
L = L + 1
OR IF (KEY.EQ.9)
THEN
WRITE (7, 23) K,L
FORMAT (24H MEMORY LOAD COMPLETED , 15, 19H WORDS OF MAIN AND
15H 32H WORDS OF CONTROL MEMORY LOADED, //)
ELSE
WRITE (7, 33) KEY

```

005710

005720

005730

005740

005750

005760

005770

005780

005790

005800

005810

005820

005830

005840

005850

005860

005870

005880

005890

005900

005910

005920

005930

005940

005950

005960

005970

005980

005990

006000

006010

006020

006030

006040

006050

006060

006070

006080

006090

006100

006110

006120

006130

006140

006150

006160

006170

006180

006190

006200

006210

006220

006230

006240

006250

006260

```

30      FORMAT (49HJINVALID CONTROL CHARACTER IN MEMORY LOAD CARD = , 006270
      11, 18H.  RJN TERMINATED. ) 006280
      KEY = 9 006290
      ERROR = .TRUE. 006300
      END IF 005310
      END DO 006320
      OR IF (NRUN(11).EQ.2) 006330
      THEN 006340
      DO WHILE (KEY.NE.9) 006350
      READ (5, 40) KEY, MADR, MAINL, MAINR, (CNTFLD(I), I = 1,6) 006360
      FORMAT (I1,I1,04,I1,03,03,I1,02,01,02,02,04,08) 006370
      IF (KEY.EQ.1) 006380
      THEN 006390
      MAIN(MADR+1) = OR (SHIFT (MAINL, 8), MAINR) 006400
      K = K + 1 006410
      OR IF (KEY.EQ.2) 005420
      THEN 006430
      CNTRL = OR (SHIFT (CNTFLD(1), 3), CNTFLD(2) ) 006440
      CNTRL = OR (SHIFT (CNTRL, 4), CNTFLD(3) ) 006450
      CNTRL = OR (SHIFT (CNTRL, 4), CNTFLD(4) ) 006460
      CNTRL = OR (SHIFT (CNTRL, 10), CNTFLD(5) ) 006470
      CNTRL = OR (SHIFT (CNTRL, 22), CNTFLD(6) ) 006480
      INVERT BITS 2,3 OF JP CODE (0,+); 006490
      CNTRM(MADR+1) = XOR (MSK1, CNTRL) 006500
      L = L + 1 006510
      OR IF (KEY.EQ.9) 005520
      THEN 006530
      WRITE (7, 20) K, L 006540
      ELSE 006550
      WRITE (7, 30) KEY 006560
      KEY = 9 006570
      ERROR = .TRUE. 006580
      END IF 006590
      END DO 006600
      E-SE 006610
      WRITE (7, 50) NRUN(11) 006620
      FORMAT (2,H0INVALID NRUN(11) = ,04, 18H.  RUN TERMINATED. ) 006630
      ERROR = .TRUE. 006640
      END IF 006650
      RETURN 006660
      END 006670
      ERRORS FOUND IN THIS ROUTINE. 97/ CARDS READ. 96 CARDS OUTPUT.

```



```

C *****
C SUBROUTINE GETCM (IADR, IBITL, IBITN, IBYTE, IFLAG)
C *****
C
C USED TO EXTRACT A FIELD FROM THE SIMULATED 48-BIT MICRO-
C PROCESSOR CONTROL MEMORY - PARAMETERS -
C IADR - RELATIVE CONTROL MEMORY LOCATION - 0 TO 1023
C IBITL - STARTING BIT OF DESIRED FIELD - 0 TO 47
C IBITN - NUMBER OF BITS IN FIELD - 1 TO 48 (24 MAX RETURNED)
C IBYTE - RETURN WORD, FIELD RIGHT ADJUSTED, ZERO FILLED
C IFLAG - ERROR RETURNS - ZERO, N3 ERROR - 1, 2, OR 3 - ERROR IN
C PARAMETER 1, 2, OR 3. CODE 3, BITS WRAPAROUND WORD
C *****
C LOGICAL FINIS, ERROR
C COMMON CNTRM(1024), ICN, ICGUNT, IOIN,
1 IOOUT, IISCR, ITELX, IAINM(1024),
2 MBUSS, MEMC, MEMH, MICAD(16), MICOA(3),
3 MICG, MSCPAD(16), MSKI, MSRE,
4 MRUN(20), FINIS, EROR, IINSTR, MOPND,
5 MICRO(25), MGMT, STIME, IETIM
C COMMON KAD, KDA, IOLDB
C TEST PARAMETERS FOR VALIDITY
C IF (IADR.LT.0.OR.IADR.GT.1023)
C THEN
C OR IF (IBITL.LT.0.OR.IBITL.GT.47)
C THEN
C IFLAG = 2
C OR IF (IBITN.LT.0.OR.IBITN.GT.48)
C THEN
C IFLAG = 3
C OR IF ((IBITL + IBITN).GT.48)
C THEN
C IFLAG = 3
C ELSE
C IFLAG = 0
C GET FIELD -
C IOR = IADR + 1
C ADJUST START BIT FOR 60-BIT #3301
C ISBIT = 48 - IBITL
C INSK = SHIFT (MASK(IBITN), ISBIT)
C IBYTE = AND (CNTRM(IOR), INSK)
C RIGHT ADJUST
C NMBR = 48 - (IBITL + IBITN)
C IBYTE = SHIFT (IBYTE, -NMBR)
C END IF (IFLAG.NE.0)
C IF (IFLAG.NE.0)
C THEN
C IBYTE = 0
C END IF
C RETURN
C END
0 ERRORS FOUND IN THIS ROUTINE. 30 CARDS READ. 45 CARDS OUTPUT.

```

```

SUBROUTINE DCODM
C
C*****
C
C DECODE MAIN MEMORY INSTRUCTION POINTED TO BY PC (MSCPAD(1)
C RESET PC = PC + 1. LOADH-REG FROM 1ST HALF, C-REG
C LOADED FROM 2ND HALF OF MAIN MEMORY WORD.
C
C*****
C
LOGICAL FINIS , ERROR
COMMON CNTMEM(1024) , ICN , ICOUNT , IDIN ,
IDOUT , IDSCR , ITELH , MAINM(1024) ,
MBUSS , MEMC , MEMH , MICAD(6) , MICAD(3) ,
MICQ , MSCPAD(16) , MSR1 , MSR2 ,
NRJN(20) , FINIS , ERROR , MINSTR , MOPND ,
MICRO(25) , MCNT , STIME , ITIME , IETIM
COMMON KAD , KDA , IOLDS
DATA IOFF /1408/
MEMC = MSCPAD(I)
CALL GETMH (MEMC, 0, 8, MIN, IFLAG)
MINSTR = MIN
IF (IFLAG.EQ.0)
THEN
MEMH = MINSTR + IOFF
CALL GETMH (MEMC, 8, 8, MOP, IFLAG)
MOPND = MOP
IF (IFLAG.EQ.0)
THEN
MEMC = MOPND + IOFF
ELSE
WRITE (7, 10) IFLAG
FORMAT (43H) INVALID CALL TO GETMH FROM DCODM, IFLAG = , I2, 1H. )
ERROR = .TRUE.
END IF
ELSE
WRITE (7, 10) IFLAG
ERROR = .TRUE.
END IF
RETURN
END

```

007220  
007230  
007240  
007250  
007260  
007270  
007280  
007290  
007300  
007310  
007320  
007330  
007340  
007350  
007360  
007370  
007380  
007390  
007400  
007410  
007420  
007430  
007440  
007450  
007450  
007470  
007480  
007490  
007500  
007510  
007520  
007530  
007540  
007550  
007560  
007570  
007580  
007590  
007600  
007610  
007620  
007630

0 ERRORS FOUND IN THIS ROUTINE. 42 CARDS READ. 37 CARDS OUTPUT.

```

C *****
C SUBROUTINE GETMH (IADR, IBITL, IBITN, IBYTE, IFLAG)
C *****
C USED TO EXTRACT A FIELD FROM THE SIMULATED 16-BIT MICRO-
C PROCESSOR MAIN MEMORY. PARAMETERS:
C IADR - RELATIVE MEMORY LOCATION - BASE ZERO
C IBITL - STARTING BIT OF DESIRED FIELD - J TO 15
C IBITN - NUMBER OF BITS IN FIELD
C IBYTE - RETURN LOCATION - RIGHT ADJUSTED, ZERO FILLED
C IFLAG - ERROR CONDITIONS - ZERO, NINE. 1-3, CORRESPONDS TO
C INVALID PARAMETER 1-3 3RD BITS WRAPAROUND
C *****
C LOGICAL FINIS , ERROR
C COMMON CNTMEM(1024) , ICN , ICONF , IOIN ,
1 IOOUT , IOSCR , ITEL4 , MAINM(1024)
2 MRUSS , MEMC , MEM4 , MICAD(16) , MICDA(13) ,
3 MRCC , MSCP(1016) , MSR1 , MSR2 ,
4 MRUN(24) , FINLS , ERR02 , MINSTR , MOPND ,
5 MICRO(25) , MCNT , STIME , ITIME , IETIM
C COMMON KAD , KDA , IOLJB
C TEST PARAMETERS FOR VALIDITY
C IF (IADR.LT.0.OR.IADR.GT.1323)
C THEN
C IFLAG = 1
C OR IF (IBITL.LT.0.OR.IBITL.GT.15)
C THEN
C IFLAG = 2
C OR IF (IBITN.LT.0.OR.IBITN.GT.16)
C THEN
C IFLAG = 3
C OR IF ((IBITL + IBITN).GT.16)
C THEN
C IFLAG = 5
C ELSE
C IFLAG = 0
C IOR = IADR + 1
C IBIT = 16 - IBITL
C IMASK = SHIFT (MASK(IBITN), (IBIT))
C IBYTE = END (MAINM(IOR), IMASK)
C NMBR = 16 - (IBITL + IBITN)
C IBYTE = SHIFT (IBYTE, -NMBR)
C END IF
C IF (IFLAG.NE.0)
C THEN
C IBYTE = 0
C END IF
C RETURN
C END
C *****
C 45 CARDS OUTPUT.

```

```

C
C*****
SUBROUTINE BOLN (ICP)
C*****
C
C ALU SIMULATION FOR DP CODES ZERO THRU SIX (BOOLEAN)
C*****
C
C LOGICAL FINIS , ERROR
COMMON CNTM(1024) , ICN , ICOUNT , IDIN ,
1 IDOUT , IOSCR , ITEL , MAINM(1024) ,
2 MBUSS , MEMC , MEMH , MICA(16) , MICOA(3) ,
3 MICQ , MSCPAD(16) , MSRI , MSR2 ,
4 MRUNTED , FINIS , ERRO , MINSTR , MOPRD ,
5 MICRO(25) , MCNT , STINE , ITIME , IETIM
COMMON KAD , KDA , IOLD9
DATA LHIGH /177778/
5 IF (VRUN(3).EQ.2) WRITE (7, 5)
FORMAT (27H0SUBROUTINE BOLN ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
ISR = MICRO(4) + 1
IOLD3 = MSCPAD(1BR)
IF (IOP.EQ.0)
THEN
IF (ICN.EQ.0)
THEN
IOMP = LHIGH
OR IF (ICN.EQ.1)
THEN
IOMP = 0
ELSE
ERROR = .TRUE.
WRITE (7, 15) ICN, IOP
FORMAT (17H0INVALID CARRY = , I2, 1H, )
OR IF (IOP.EQ.1)
THEN
IOMP = AND (MSCPAD(IAR), MSCPAD(ISR) )
OR IF (IOP.EQ.2)
THEN
IOMP = AND (IOLDM, MSCPAD(ISR) )
OR IF (IOP.EQ.3)
THEN
IOMP = OR (MSCPAD(IAR), MSCPAD(ISR) )
OR IF (IOP.EQ.4)
THEN
IOMP = OR (IOLDN, MSCPAD(ISR) )
OR IF (IOP.EQ.5)
THEN
IOMP = XOR (MSCPAD(IAR), MSCPAD(ISR) )
OR IF (IOP.EQ.6)
THEN
IOMP = XOR (IOLDM, MSCPAD(ISR) )
END IF
IF (VRUN(3).EQ.2)

```

```
THEN                                008710  
WRITE (7, 25) IOP, ITMP            008720  
25  FORMAT ( 7H0INSTR , 02, 24H EXECUTED, TEMP VALUE = , 06, 1H.) 008730  
END IF  
IF (MOD.EQ.7)                      008740  
THEN                                008750  
    MICQ = ITMP                    008760  
    IOOUT = ITMP                   008770  
ELSE                                  008780  
    MSCPAD(I8R) = ITMP             008790  
    CALL INMOD (IAR, I8R)          008800  
END IF                               008810  
RETURN                              008820  
END                                  008830  
END                                  008840
```

0 ERRORS FOUND IN THIS ROUTINE. 7:: CARDS READ. 84 CARDS OUTPUT.

```

C *****
C SUBROUTINE INVRT (IOP)
C *****
C ALU SIMULATION FOR OP CODES 7 THRU 10 (INVRT)
C *****
C LOGICAL FINIS , ERROR
COMMON CNTRM(1024) , ICM , ECOUNT , IOIN ,
1 IOUT , IOSCR , ITEL , MAINM(1024) ,
2 MBUSS , MEMC , MEMH , MICAD(64) , MICOA(32) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 WRUN(207) , FINIS , ERROR , MINSTR , POPND ,
5 MICRO(25) , MCNT , STIME , IETIM ,
COMMON KAD , KDA , IOLDB
DATA LHIGH /177776/
IF (VRUN(3).EQ.2) WRITE (F, 9)
5 FORMAT (27H0SUBROUTINE INVRT ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOLDB = MSCPAD(1BR)
IF (IOP.EQ.7)
THEN
ITMP = COMPL(MSCPDI(1BR))
OR IF (IOP.EQ.8)
THEN
ITMP = COMPL (IDIN)
OR IF (IOP.EQ.9)
THEN
ITMP = COMPL (MSCPDI(1BR))
OR IF (IOP.EQ.11)
THEN
ITMP = COMPL (MICQ)
END IF
ITMP = AND(ITMP, LHIGH)
IF (ICW.EQ.0)
THEN
ITMP = ITPM + LHIGH
ITMP = AND (ITMP, LHIGH)
OR IF (ICW.LT.0.OR.ICW.GT.1)
THEN
WRITE (F, 10) ICM, IOP
10 FORMAT (17H0INVALID CARRY = ,J6,214 IN INVRT, OP CODE = ,I2,1H.)
ERROR = .TRUE.
END IF
IF (VRUN(3).EQ.2)
THEN
WRITE (F, 25) IOP, ITMP
25 FORMAT ( 7H1INSTR , 02, 24H EXECUTED, TEMP VALUE = ,06, 14.)
IF (400.EQ.7)
THEN
MICQ = ITPM
IOPUT = ITPM
ELSE
MSCPDI(1BR) = ITPM
CALL INHOG (IAR, IBR)
END IF
RETURN
END

```

6 ERRORS FOUND IN THIS ROUTINE. 85 CARDS READ. 70 CARDS OUTPUT.

```

SUBROUTINE CHPLT (IOP)
C*****
C
C ALU SIMULATION FOR OP CODES 11 THRU 14 (THO'S COMPLEMENT)
C*****
C
LOGICAL FINIS , ERROR
COMMON CNTMEM(1624) , IGN , ICOUNT , IDIN ,
1 IDOUT , IOSCR , ITEL4 , MAINH(1024) ,
2 MBUSS , MEMC , MEMH , MICAD(16) , MICDA(3) ,
3 MICQ , MSCPAD(16) , MSRI , MSR2 ,
4 WROTEOF, FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25) , MCNT , STIMEI , ITIME , IETIM ,
COMMON KAD , KDA , IOLE3
DATA LMIGH /177778/
IF (NRUN(3).EQ.2) WRITE (7, 5)
5 FORMAT (27H0SUBROUTINE COMPL ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
TBR = MICRO(4) + 1
IOLB = MSCPAD(IAR)
IF (IOP.EQ.11)
1 THEN
ITMP = COMPL(MSCPAD(IAR))
OR IF (IOP.EQ.12)
1 THEN
ITMP = COMPL (IDIN)
OR IF (IOP.EQ.13)
1 THEN
ITMP = COMPL (MSCPAD(IAR))
OR IF (IOP.EQ.14)
1 THEN
ITMP = COMPL (MICQ)
END IF
ITMP = AND (ITMP, LMIGH)
ITMP = ITHP + ICW
ITMP = AND (ITMP, LMIGH)
IF (NRUN(3).EQ.2)
1 THEN
WRITE (7, 25) IOP, ITMP
25 FORMAT ( 7H0INSTR , 02, 24H EXECUTED, TEMP VALUE = ,06, 14.)
END IF
IF (MOD.EQ.7)
1 THEN
MICQ = ITHP
IDOUT = ITMP
E.SE
MSCPAD(IAR) = ITMP
CALL INHOD (IAR, IGR)
END IF
RETURN
END

```

0 ERRORS FOUND IN THIS ROUTINE. 37 CARDS READ. 56 CARDS OUTPUT.

```

C
C SUBROUTINE TRINC (IOP)
C*****
C ALU SIMULATION FOR OP CODES 15 THRU 18 (TRANSFER/INCREMENT)
C*****
C
C LOGICAL FINIS , ERROR
COMMON CNTRM(1024) , ICN , ICOUNT , IGIN ,
1 IDOUT , IDSCR , ITEL4 , IAINM(1024) ,
2 MBUSS , WENC , MEMH , MICAD(6) , MICDA(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 MKUNT(20) , FINIS , ERROR , IINSTR , MOPND ,
5 MICRO(25) , MCNT , STIME , ITIME , IETIM ,
COMMON KAD , KDA , IOLDB
DATA LHIGH /177778/
5 IF (VRUN(3).EQ.2) WRITE (7, 5)
FORMAT (27H0SUBROUTINE TRINC ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOLB = MSCPAD(18)
IF (IOP.EQ.15)
THEN
ITMP = MSCPAD(IAR) + IGN
OR IF (IOP.EQ.16)
THEN
ITMP = IGIN + ICN
OR IF (IOP.EQ.17)
THEN
ITMP = MSCPAD(18) + IGN
OR IF (IOP.EQ.18)
THEN
ITMP = MICQ + ICN
END IF
ITMP = AND (ITMP, LHIGH)
IF (VRUN(3).EQ.2)
THEN
WRITE (7, 25) IOP, ITMP
25 FORMAT (7H0INSTR ,02.24H EXECUTED, TEMP VALUE = ,08, 1H.)
IF (400.EQ.7)
THEN
MIC1 = ITMP
IBOJF = ITMP
E-SE
MSCPAD(18) = IFMP
CALL INMOD (IAR, IBR)
END IF
RETURN
END

```

```

010010
010020
010030
010040
010050
010060
010070
010080
010090
010100
010110
010120
010130
010140
010150
010160
010170
010180
010190
010200
010210
010220
010230
010240
010250
010260
010270
010280
010290
010300
010310
010320
010330
010340
010350
010360
010370
010380
010390
010400
010410
010420
010430
010440
010450
010460
010470
010480
010490
010500
010510
010520

```

0 ERRORS FOUND IN THIS ROUTINE. 32 CARDS READ. 56 CARDS OUTPUT.



```

SUBROUTINE DECTR (IOP)
C*****
C ALU SIMULATION FOR OP CODES 19 THRU 22 (DECREMENT/TRANSFER)
C*****
LOGICAL FINIS , ERROR
COMMON CNTMEM(1024) , ICN , ICOUNT , IDIN ,
1 IDOUT , IDSCR , ITEL4 , MAINM(1024) ,
2 MBUSS , MEC , MEMH , MICAD(6) , MICRO(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 MRUNT(2) , FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25) , MCNT , STIME , ITIME , IETIM
COMMON KAO , KDA , IOLDB
DATA LK1G /177778/
IF (NRUN(3).EQ.2) WRITE (7, 5)
5 FORMAT (27H SUBROUTINE DECTR ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOLDB = MSCPAD(IAR)
IF (IOP.EQ.19)
THEN
IOP = MSCPAD(IAR)
OR IF (IOP.EQ.20)
THEN
IOP = IDIN
OR IF (IOP.EQ.21)
THEN
IOP = MSCPAD(IAR)
OR IF (IOP.EQ.22)
THEN
IOP = MICQ
END IF
IF (ICN.EQ.8)
THEN
IOP = IOP + LK1G
IOP = AND (IOP, LK1G)
OR IF (ICN.LT.8.OR.ICN.GT.1)
THEN
WRITE (7, 10) ICN, IOP
10 FORNAT (17H INVALID CARRY = ,00Z11 IN DECTR, OP CODE = ,I2,I10, )
END IF
IF (NRUN(3).EQ.2)
THEN
WRITE (7, 25) IOP, IOP
25 FORNAT ( 7H INSTR , 02, 24H EXECUTED, TEMP VALUE = ,06, 14, )
IF (IOP.EQ.7)
THEN
MICQ = IOP
IDOUT = IOP
E.5E
MSCPAD(IAR) = IOP
CALL INMOD (IAR, IAR)
END IF
RETURN
END

```

010530  
010540  
010550  
010560  
010570  
010580  
010590  
010600  
010610  
010620  
010630  
010640  
010650  
010660  
010670  
010680  
010690  
010700  
010710  
010720  
010730  
010740  
010750  
010760  
010770  
010780  
010790  
010800  
010810  
010820  
010830  
010840  
010850  
010860  
010870  
010880  
010890  
010900  
010910  
010920  
010930  
010940  
010950  
010960  
010970  
010980  
010990  
011000  
011010  
011020  
011030  
011040  
011050  
011060  
011070  
011080  
011090  
011100  
011110  
011120

8 ERRORS FOUND IN THIS ROUTINE. 5 CARDS READ. 66 CARDS OUTPUT.

```

C
C SUBROUTINE SUM (IOP)
C *****
C ALU SIMULATION FOR OP CODES 23 THRU 26 (A00)
C *****
C LOGICAL FINIS , ERROR
COMMON CNTMHI(24) , ICN , ICOUNT , IOIN ,
1 IOOUT , IDSCR , ITELN , MAINM(1024)
2 MBUSS , MEMC , MEMH , MICAD(6) , MICDA(3) ,
3 MICQ , MSCPAD(16) , MSK1 , MSR2 ,
4 MRUN(20) , FENIS , ERR2 , INSTR , HOPND ,
5 MICRO(25) , MCNT , STIME , IELIM ,
COMMON KAD , KDA , IOL3
DATA LHIGH /177778/
5 IF (NRUN(3).EQ.2) WRITE (7, 9)
FORMAT (27H0SUBROUTINE SUM ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOLB = MSCPAD(1BR)
IF (IOP.EQ.23)
THEN
ITMP = MSCPAD(IAR) + MSCPAD(1BR) + ICN
OR IF (IOP.EQ.24)
THEN
ITMP = IOIN + MSCPAD(1BR) + ICN
OR IF (IOP.EQ.25)
THEN
ITMP = MSCPAD(IAR) + MICQ + ICN
OR IF (IOP.EQ.26)
THEN
ITMP = IOIN + MICQ + ICN
END IF
ITMP = AND (ITMP, LHIGH)
IF (NRUN(3).EQ.2)
THEN
WRITE (7, 25) IOP, ITMP
25 END IF
FORMAT ( 7HINSTR , 02, 24H EXECUTED, TEMP VALUE = ,06, 14.)
IF (MOD.EQ.7)
THEN
NICQ = ITMP
IOOUT = ITMP
E-SE
MSCPAD(1BR) = ITMP
CALL INHOD (IAR, 1BR)
END IF
RETURN
END

```

0 ERRORS FOUND IN THIS ROUTINE. 52 CARDS READ. 56 CARDS OUTPUT.

```

SUBROUTINE DIFF (IOP)
C ***** 011650
C ***** 011660
C ***** 011670
C ***** 011680
C ***** 011690
C ***** 011700
C ***** 011710
C ***** 011720
C ***** 011730
C ***** 011740
C ***** 011750
C ***** 011760
C ***** 011770
C ***** 011780
C ***** 011790
C ***** 011800
C ***** 011810
C ***** 011820
C ***** 011830
C ***** 011840
C ***** 011850
C ***** 011860
C ***** 011870
C ***** 011880
C ***** 011890
C ***** 011900
C ***** 011910
C ***** 011920
C ***** 011930
C ***** 011940
C ***** 011950
C ***** 011960
C ***** 011970
C ***** 011990
C ***** 012000
C ***** 012010
C ***** 012038
C ***** 012040
C ***** 012050
C ***** 012060
C ***** 012070
C ***** 012090
C ***** 012100
C ***** 012110
C ***** 012120
C ***** 012130
C ***** 012140
C ***** 012150
C ***** 012160
C ***** 012170
C ***** 012180
C ***** 012190
C ***** 012200

LOGICAL FINIS , ERROR
COMMON
  CNTREM(1024) , IGN , ICOUNT , IDIN ,
  IDOUT , IOSCR , ITEL , MAINM(1024) ,
  MBUSS , MHC , MEM , MICAD(16) , MICOA(3) ,
  MICQ , MSCPAD(16) , MSR1 , MSR2 ,
  NRUN(26) , FINIS , ERROR , MINSTR , MOPND ,
  MICRO(25) , MCNT , SIME , ITELIM ,
  COMMON , KAD , KDA , IOLD9
DATA LHIG4 /177778/
IF (NRUN(3),EQ,2) WRITE (7, 5)
5 FORMAT (27H SUBROUTINE DIFF ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
ICL03 = MSCPAD(18R)
IF (IOP.EQ.27)
  THEN
    ITHP = MSCPAD(IAR) + AND(1COMPL(MSCPAD(18R)), LHIGH) + IGN
  OR IF (IOP.EQ.28)
    THEN
    ITHP = MSCPAD(18R) + AND(1COMPL(MSCPAD(IAR)), LHIGH) + IGN
  OR IF (IOP.EQ.29)
    THEN
    ITHP = IDIN + AND(1COMPL(MSCPAD(18R)), LHIGH) + IGN
  OR IF (IOP.EQ.30)
    THEN
    ITHP = MSCPAD(18R) + AND(1COMPL(IDIN), LHIGH) + IGN
  OR IF (IOP.EQ.31)
    THEN
    ITHP = IDIN + AND(1COMPL(MICQ), LHIGH) + IGN
  END IF
  ITHP = AND (ITHP, LHIGH)
  IF (NRUN(3),EQ,2)
  THEN
    WRITE (7, 25) IOP, ITHP
25 FORMAT (7H INSTR = 02, 24H EXECUTED, TEMP VALUE = 106, 14H)
  END IF
  IF (MOD.EQ.7)
  THEN
    MICQ = ITHP
    IDOUT = ITHP
  END IF
  CALL INMOD(IAR, IBR)
  END IF
  RETURN
  END
  J ERRORS FOUND IN THIS ROUTINE. 55 CARDS READ. 61 CARDS OUTPUT.

```

```

SUBROUTINE PRBIN
C*****
C
C EXECUTE THOSE CONTROL FUNCTIONS REQUIRED PRIOR TO
C INSTRUCTION INTERPRETATION AND EXECUTION
C*****
C
C LOGICAL FINIS , ERROR
COMMON CNTMEM(1024) , ICN , ICONF , IDIN ,
1 IDOUT , IDSCR , ITELN , MAINM(1024)
2 MBUSS , MEMC , MEM , MICAD(6) , MICDA(3) ,
3 MICQ , MSCPAD(10) , MSRI , MSR2
4 NRUN(20) , FINIS , ERRO , MINSR , MOPND ,
5 MICRO(25) , MCNT , SYNE , ITIME , IETIM
COMMON KAD , KDA , IOLOB
IF (MICRO(6).EQ.1) MSRI = 3
IF (MICRO(10).EQ.1)
THEN
MBUSS = MAINMEMC + 1
IDIN = MBUSS
END IF
IF (MICRO(13).EQ.1)
THEN
MBUSS = NOT (OR (MICAD(KAD) , IDSCR) )
IDIN = MBUSS
END IF
IF (MICRO(15).EQ.1) MBUSS = OR (MBUSS , MSRI)
IF (MICRO(17)
OR (MICRO(20).EQ.1)
THEN
KDA = 1
OR IF (MICRO(21).EQ.1)
THEN
KDA = 2
OR IF (MICRO(22).EQ.1)
THEN
KDA = 3
ELSE
KDA = 0
END IF
IF (MICRO(23).EQ.1)
THEN
KAD = MICRO(25)
IF (KAD.EQ.6) KAD = 3
END IF
RETURN
END

```

6 ERRORS FOUND IN THIS ROUTINE. \*3 CARDS READ. 50 CARDS OUTPUT.

```

SUBROUTINE BINRY                                012690
C*****                                012700
C*****                                012710
C      EXECUTE CONTROL FUNCTIONS SPECIFIED BY BINARY BITS 27-45    *012720
C*****                                *012730
C*****                                *012740
C*****                                012750
C*****                                012760

LOGICAL FINIS , ERROR                                012770
COMMON CNTHM(1024) , ICN , ICOUNT , IGIN , IDOUT , IDSCR , ITELH , MAINH(1024) , 012780
1      MBUSS , MEMC , MEMH , MICAD(8) , MICOA(3) , MSR1 , MSR2 , 012790
2      MSCPAD(16) , 012800
3      NRUNT(20) , FINIS , ERROR , MINSTR , MOPND , 012810
4      MICRO(25) , MCNT , STIME , ITIME , IETIM , 012820
5      MICRO(25) , MCNT , STIME , ITIME , IETIM , 012830
COMMON KNO , KDA , IOLDB                                012840
DATA MSK10 /1,7778/                                012850
DATA IDPP /14428/                                012860
IF (MICRO(11).EQ.1) MBUSS = IDOUT                                012870
IF (MICRO(7).EQ.1) MSR2 = MSR1                                012880
IF (MICRO(8).EQ.1)                                012890
THEN
MEMH = MICRO(5)                                012910
ELSE
IF (NRUN(3).EQ.2) WRITE (7,4) MEMH                                012920
FORMAT ('31M M-REG LOAD BIT NOT SET AT LOC , 04,15H - RUN HALTED. ')012930
MEMH = 0                                012950
MICRO(5) = 0                                012960
ERROR = .TRUE.                                012970

END IF ERROR                                012980
IF (MICRO(9).EQ.1)                                012990
THEN
M = MEMC + 1                                013010
IF (NRUN(3).EQ.2)                                013020
THEN
WRITE (7,5) MEMC , MAINH(M) , MBUSS                                013030
FORMAT (17H MAIN MEMORY LOC , 04, 14H CHANGED FROM , 06, 4H TO , 013040
5      , 06, 19H BY CONTROL BIT 35. )                                013050
END IF                                013070
MAINH(M) = MBUSS                                013080
END IF                                013090
IF (MICRO(12).EQ.1.AND.MEMH.NE.0)                                013100
THEN
WRITE (7, 10) MEMH                                013110
FORMAT (34HERROR! FETCH BIT ON BUT M-ADDR = , 06, 14H. )                                013120
ERROR = .TRUE.                                013130
END IF                                013140
IF (MICRO(14).EQ.1)                                013150
IF (CHECK ALU OUTPUT) IF = ZERO, SET SR1 = 1:                                013160
THEN                                013170
END IF                                013180
IF (IDOUT.EQ.0) MSR1 = 1                                013190
IF (MICRO(16).EQ.1)                                013200
THEN
MEMH = OR (MICRO(5), MSR1)                                013210
IF (NRUN(3).EQ.2) WRITE (7,3) MEMH                                013220
END IF                                013230

```

```

30      FORMAT (29H0NEXT H MODIFIED BY MSRI TO: , 04 )          013250
      END IF
      IF BIT 47 ON, BOTTOM 10 BITS OF BUSS TO C REGISTER:
      IF (MICRO(19).EQ.1) MEMC = AND (MBUSS, MSK10)
      IF (MICRO(18).EQ.0) ITEL = MBUSS
      IF (KDA.NE.0)
      THEN
      MICRO(KDAT) = MBUSS
      KDA = 0
      END IF
      IF (NRUN(3).EQ.2) CALL REPT1
      RETURN
      END
0 ERRORS FOUND IN THIS ROUTINE.  63 CARDS READ.  68 CARDS OUTPUT.

```

```

SUBROUTINE STATS
C ***** 013380
C ***** 013390
C ***** 013400
C ***** 013410
C ***** 013420
C ***** 013430
C ***** 013440
C ***** 013450
C ***** 013460
C ***** 013470
C ***** 013480
C ***** 013490
C ***** 013500
C ***** 013510
C ***** 013520
C ***** 013530
C ***** 013540
C ***** 013550
C ***** 013560
C ***** 013570
C ***** 013580
C ***** 013590
C ***** 013600
C ***** 013610
C ***** 013620
C ***** 013630
C ***** 013640
C ***** 013650

      LOGICAL FINIS , ERROR
      COMMON  CNTHEM(1024) , ICN , ICOUNT , IOIN ,
      IDOUT , IDSCR , ITEL , MAINM(1024) ,
      MBUSS , MEMC , MEMH , MICAD(6) , MICDA(3) ,
      MICQ , MSCPAD(16) , MSR1 , MSR2 ,
      NRUN(20) , FINIS , ERROR , MINSTR , MOPND ,
      MICRO(25) , MCNT , STIME , ITIME , IETIM ,
      KAD , KDA , IOLD3
      COMMON  WRITE (7, 10) STIME, ICOUNT, MCNT, MSCPAD, IOIN, IDOUT, MBUSS,
      MEMC, MEMH, MICQ, MICAD, ICN, IDSCR, MSR1, MSR2
      10 FORMAT (26HIRUN TERMINATED AT TIME : ,F15.8,15H SECONDS AFTER ,013560
      . 15,11H MICROS OR ,15,17H MACROS EXECUTED. //
      . 21H0SCATCHPAD CONTAINS:,1H ,16( /5X, 08) , //
      . 11H0DATA IN = , 08,13H, DATA OUT = , 08, 9H, BUSS = , 08, 013590
      . 10H, C-REG = ,04,10H, H-REG = ,0,10H, Q-REG = , 06, //
      . 9H0A/D'S = ,5(2X,08),10H, 0/A S = ,3(2X,08)//
      . 11H0 CARRY = ,12, 20H, INPUT DISCRETES = , 08, //
      . 9H0 MSR1 = , 11, 9H, MSR2 = , 11 )
      RETURN
      END
  
```

0 ERRORS FOUND IN THIS ROUTINE. 28 CARDS READ. 21 CARDS OUTPUT.

```

C          SUBROUTINE REPT1
C          *****
C          DETAILED OUTPUT FROM MICRO-INSTRUCTION EXECUTION
C          *****
C          LOGICAL FINIS , ERROR
C          COMMON CNTHM(1024) , ICN , ICOUNT , IOIN ,
1          IDOUT , IDSCR , ITEL2 , ITEL1 , MAINM(1024) ,
2          MBUSS , MEMC , MEMH , MICAD(16) , MICDA(3) ,
3          MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4          NRUNT(20) , FINIS , ERROR , INSTR , MOPND ,
5          MICRO(25) , MCNT , STIME , ITIME , IETIM ,
          COMMON KAD , KDA , IOLDB
          INSTR = MICRO(1)
          MOD = MICRO(2)
          IA = MICRO(3) + 1
          IB = MICRO(4) + 1
          I = IA - 1
          J = IB - 1
          WRITE (7,10) INSTR,MOD,I,MSCPAD(IA),J,IOLDB,MSCPAD(IB),MICQ2,MICQ
          , ITEL2, ITEL1
10  FORMAT (18HEXECUTED OP CODE ,02,12H WITH MODIFIER ,11,1H, //
          , 7H A-REG ,02,12H CONTENTS = ,05,777H B-REG ,02,
          , 22H CONTENTS INITIALLY = ,05, 84, NOM = ,06, //
          , 28H Q-REG CONTENTS INITIALLY = ,06,84, NOM = ,06, //
          , 28H TELEM CONTENTS INITIALLY = ,06,84, NOM = ,06, // )
          ITEL2 = ITEL1
          MICQ2 = MICQ
          RETURN
          END
          J ERRORS FOUND IN THIS ROUTINE.      33 CARDS READ.      26 CARDS OUTPUT.
    
```

```

C          SUBROUTINE REPT2
C          DETAILED OUTPUT FROM INSTRUCTION MODIFICATION AND CONTROLS
C          RETURN
C          END
          J ERRORS FOUND IN THIS ROUTINE.      4 CARDS READ.      3 CARDS OUTPUT.
          J PREPROCESSOR ERRORS FOUND.      1392 TOTAL CARDS READ.      1367 TOTAL CARDS OUTPUT.
    
```



```

PROGRAM ENUL (INPUT, OUTPUT, TAPES = INPUT, TAPE7=OUTPUT)
LOGICAL FINIS, ERROR
COMMON CNTMEM(1024) , ICN , ICOUNT , IDIN ,
1 IDOUT , IDSCR , IELM , MAINM(1024)
2 MBUSS , MECG , MEMH , MICAD(16) , MICDA(3) ,
3 MICQ , MSPAD(16) , MSRI , MSX2 ,
4 NRUN(2) , FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25) , MENT , STIME , ITIME , IETIM ,
COMMON KAD , KDA , IOLDB
10 DATA LFTMS /3778/
READ (5, 10) NRJN
10 FORMAT (20 0 4)
WRITE (7, 20) NRJN
20 FORMAT (2JHRUN CONTROL CARD = , 2J04 )
CALL INIT
CALL SETCN
CALL SETRM
CALL LODJN
MICS = 0
IF (.NOT.
* (NRUN(4) .EQ.1)
* .) GO TO 99999
N = 1
25 WRITE (7, 80)
80 FORMAT (1JH1 LOCATION, 5X, 15HMAIN DECODED, 26X, 8HLOCATION, 5X,
* 15HMAIN DECODED, 11H DEC OCT, 3X, 12HMEMORY LEFT ,
* 5HRIGHT, 4X, 24HCONTROL MEMORY, 7X, 9HDEC OCT, 3X,
* 17HMEMORY LEFT RIGHT, 4X, 14HCONTROL MEMORY ?? )
30 99998 IF (.NOT. (N.LE.124)
* .) GO TO 99997
NR = N - 1
35 NR = N + 1
MAIN = MAIN(N)
MAINL = SHIFT (MAIN, -8)
MAINR = AND (MAIN, LFTMS)
MAIN = MAIN(NR)
MAINJ = SHIFT (MAIN, -8)
40 MAINS = AND (MAIN, LFTMS)
WRITE (7, 90) NR, MN, MAIN(N), MAINL, MAINR, CNTMEM(N),
* N, MAIN(NR), MAINJ, MAINS, CNTMEM(NR)
90 FORMAT (1H 1424, 3X, 06, 2X, 03, 2X, 03, 2X, 03, 2X, 03, 3X, 016 ,
* 14, 2X, 04, 3X, 06, 2X, 03, 2X, 03, 2X, 03, 3X, 016 )
45 N = N + 2
GO TO 99998
99997 CONTINUE
99999 CONTINUE
99998 IF (.NOT.
* .) GO TO 99995
CALL OCODN
99999 IF (.NOT. (MEMH.NE.0)
* .) GO TO 99993
MOLD = MEMH
CALL 9C03C
55
56
57

```

```

60 CALL EXECM
   IF (.NOT.
     * (NRUN(3).EQ.2)
     *150 TO 99992
     N = MMOLD * I
     WRITE (7, 15) M4LD, CMIME(N), (MICRO(I), I = 1, 25)
65 15 FORMAT (53H)THE FOLLOWING CH INSTRUCTION WAS JUST BEEN EXECUTED:
     //1H, 0H, 5A,016.4(13X,02)4H M1 04.2X, 20(1X,11//)
     M = I
     99991 IF (.NOT.
       *150 TO 99990
       K = M - 1
       WRITE (7, 30) K, M$CPAD(4)
70 30 FORMAT (13H) SCRATCH PA3( , 02, 11H) CONTAINS , 06, 2H .)
       M = M + 1
       GO TO 99991
75 99990 CONTINUE
       WRITE (7, 50) TIME, IDOUT, M$USS, MEMC, ICH, MSR1, MSR2
77 50 FORMAT (11H)DATA IN = 06,13H, DATA OUT = 08,9H, BUSS = 08,
       10H, C-REG = 08,9H CARRY = 11,0H, SR1 = 11,9H, SR2 = ,
       11, 1H.)
80 99992 CONTINUE
       STIME = TIME + TIMCR
       TIME = IFX(STIME)
       MICS = MICS + 1
       IF (.NOT.
85 * (NRUN(3).EQ.2)
     *150 TO 99989
     WRITE (7, 40) STIME, TIME, MICS
     *150 TO 99988
     99989 CONTINUE
     IF (.NOT.
90 * (NRUN(9).EQ.5)
     *150 TO 99988
     IF (.NOT.
95 * (MICS.GE.MRUNTIM)
     *150 TO 99987
     MEMM = 0
     FINIS = .TRUE.
     99987 CONTINUE
     99988 CONTINUE
100 99993 CONTINUE
     MCNT = MCNT + 1
     CALL FINAL
     GO TO 99996
105 99995 CONTINUE
     IF (.NOT.
     * (NRUN(4).EQ.1)
     *150 TO 99986
     M = 1
     WRITE (7, 80)
110 99985 IF (.NOT.
     * (M.LT.124)
     *150 TO 99984
     MM = M - 1

```

```

115      NR = N + 1
      MAIN = MAINM(N)
      MAINL = SHIFT (MAIN, -8)
      MAINR = AND (MAIN, LFTMS)
      MAIN = MAINM(NR)
      MAINJ = SHIFT (MAIN, -8)
      MAINS = AND (MAIN, LFTMS)
      WRITE (7, 90) NN, NY, MAINM(N), MAINL, MAINR, CNTMEM(N),
      *      N, N, MAINM(NR), MAINJ, MAINS, CNTMEM(NR)
      N = N + 2
      GO TO 99985
99984 CONTINUE
99985 CONTINUE
      CALL STATS
      STOP
      END
130

```

```

SUBROUTINE INIT
LOGICAL FINIS , ERROR
COMMON CNTMEM(1024) , ICN , ICOUNT , IDIM ,
1 IOOUT , IDSCR , ITELH , MAINM(1024)
5 MBUSS , MEMC , MEMH , MICAO(16) , MSR2 ,
3 MICQ , MSCPAD(16) , MSR1
4 NRUN(27) , FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25) , MCVT , STIME , ITIME , IETIM
10 COMMON KAD , KJA , IOLOB
ICN = 0
ICOUNT = 0
IDIN = 0
IOOUT = 0
IDSCR = 0
ITELH = 0
KAD = 0
KOA = 0
MBUSS = 0
MEMC = 0
MEMH = 0
MICQ = 0
MSR1 = 0
MSR2 = 0
MSCPAD(1) = NRUN(5)
N = 2
99999 IF(.NOT. (N.LE.17)
.160 TO 99998 (N.LE.17)
MSCPAD(N) = 0
N = N + 1
30 GO TO 99999
99998 CONTINUE
N = 1
99997 IF(.NOT. (N.LE.31)
.160 TO 99996 (N.LE.31)
MICRO(N) = 0
N = N + 1
40 99996 CONTINUE
MICAO(1) = 0
MICAO(2) = 0
MICAO(3) = 0
FINIS = .FALSE.
ERROR = .FALSE.
MCNT = 0
STIME = 0.0
ITIME = 0
IETIM = 0
50 RETURN
END

```

```

SUBROUTINE DC00C
LOGICAL FINIS , ERROR
COMMON CNTMEM(1024) , ICN , ICOUNT , IOIN ,
1 IOOUT , IOSCR , ITELH , MAINM(1324)
5 MBUSS , MEMC , MEMH , MICAD(6) , MICDAT(3) ,
3 MICO , MSCPAD(16) , MSR1 , MSR2 ,
4 NEUNT(1) , FINIS , ERROR , MINSTR , MOPNO ,
5 MICRO(25) , MCNT , STIME , ITIME , IETIM
COMMON KAD , KDA , IOLDB
10 DATA MSK1 /66/
IPTR = MEMH
IERR = 0
CALL GETCH (IPTR, 3, 3, MOP, IFLAG)
15 MICRO(1) = XOR (MSK1, MOP)
IERR = IFLAG
CALL GETCH (IPTR, 3, 3, MOP, IFLAG)
MICRO(2) = MOP
IERR = OR (IERR, IFLAG)
CALL GETCH (IPTR, 6, 4, MOP, IFLAG)
20 MICRO(3) = MOP
IERR = OR(IERR, IFLAG)
CALL GETCH (IPTR, 12, 4, MOP, IFLAG)
MICRO(4) = MOP
IERR = OR(IERR, IFLAG)
CALL GETCH (IPTR, 16, 16, MOP, IFLAG)
25 MICRO(5) = MOP
IERR = OR(IERR, IFLAG)
CALL GETCH (IPTR, 45, 3, MOP, IFLAG)
MICRO(25) = MOP
30 IFLAG = IERR
NCOL = 26
INDX = 5
9999 IF (.NOT. (IFLAG.EQ.3.AND.INDX.LE.24)
.160 TO 99998
CALL GETCH (IPTR, NCOL, I, MOP, IFLAG)
219 MICRO(INDX) = MOP
220 NCOL = NCOL + 1
40 INDX = INDX + 1
GO TO 99999
99998 CONTINUE
I = I + 1
.160 TO 99997
IF (.NOT. (NRUN(3).EQ.21
.160 TO 99996
WRITE (7, 9) MEMH, MICRO(5)
50 5 FORMAT ( 15HLT,IS INSTR AT: , 04, 12H, M-FIELD = , 04, 21. )
99996 CONTINUE
GO TO 99995
99997 CONTINUE
16 FORMAT (43HINVELID CALL TO GETCH FROM DC00C, IFLAG = , I2.1H, )
99995 CONTINUE
99995 RETURN
END

```

```

SUBROUTINE INH00 (IA, IB)
LOGICAL FINIS, ERROR
COMMON CMTM(1024)
1 IOUO, IOSCR, IICM, ICOUNT, IOIN,
2 MSUS, MSC, MEMH, MICAD(16), MICDA(13),
3 MICQ, MSCPAD(16), MSRL, MSR2,
4 NCON(2), FINIS, ERROR, MINSTR, MOPND,
5 MICRO(25), MCHT, STIME, ITIME, IETIH
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MSRI = 1
GO TO 99989
60 99990 CONTINUE
99989 CONTINUE
MSRI = 0
IBIT = SHIFT (MICQ, -15)
MICQ = AND (SHIFT (MICQ, 1), KMASK)
65 MICQ = OR (MICQ, 1)
MSPAD (IB) = AND (SHIFT (MSPAD (IB), 1), KMASK)
MSPAD (IB) = OR (MSPAD (IB), IBIT)
IDOUT = MSPAD (IB)
GO TO 99998
70 99991 IF (.NOT.
. (MOD, EQ, 6)
.160 TO 99988
IBIT = AND (MSPAD (IB), 1)
IBIT = SHIFT (IBIT, 15)
LOBIT = AND (MICQ, 1)
IF (.NOT.
. (LOBIT, EQ, 0)
.160 TO 99987
MSRI = 1
GO TO 99986
80 99987 CONTINUE
99986 CONTINUE
MSRI = 0
MICQ = SHIFT (MICQ, -1)
MICQ = OR (MICQ, IBIT)
MSPAD (IB) = SHIFT (MSPAD (IB), -1)
MSPAD (IB) = OR (MSPAD (IB), IBIT)
IDOUT = MSPAD (IB)
GO TO 99998
90 99988 CONTINUE
WRITE (7, 5) MOD
5 FORMAT (26H INVALID INSTR MODIFIER = ,04,15H. RUN HALTED. )
ERROR = .TRUE.
99998 CONTINUE
95 IF (NRUN (3), EQ, 2) WRITE (7, 10) MOD, IDOUT
10 FORMAT (13H INSTR MOD = ,11,21H JUST SET DATA-OUT = ,08, 1H.)
IF (.NOT.
. (NRUN (3), EQ, 2, OR, NRUN (3), EQ, 3)
.160 TO 99985
CALL REPT2
99985 CONTINUE
RETURN
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SUBROUTINE EXECB
LOGICAL FINIS, ERROR
COMMON ENTREN(1024), ICN, ICDUNT, IDIM,
1 IODUT, I3CR, ITELH, MAINM(124),
2 MBUSS, MEAC, MEH, MICAD(6), MSR1,
3 MICQ, MSCPAD(16), MSR2,
4 MRUNT(2), FINIS, ERROR, MINSTR, MOPMD,
5 MICRO(2), MCNT, STIME, ITIME,
COMMON KAD, NDA, IOLDB
CALL PRBIN
IF(.NOT.)
1 (MSR2.EQ.1)
*160 TO 99999
MICRO(1) = OR (MICRO(1), 6)
20 FORMAT (15HQOP:20E:21 WRITE (F, 20) MICRO(1)
99993 CONTINUE
IOP = MICRO(1)
IF(.NOT.)
* (IOP.GE.0.AND.IOP.LE.6)
*160 TO 99998
CALL BOLD (IOP)
GO TO 99997
99998 IF(.NOT.)
* (IOP.GE.7.AND.IOP.LE.10)
*160 TO 99996
CALL INVRT (IOP)
GO TO 99997
99996 IF(.NOT.)
* (IOP.GE.11.AND.IOP.LE.14)
*160 TO 99995
CALL CMPLT (IOP)
GO TO 99997
99995 IF(.NOT.)
* (IOP.GE.15.AND.IOP.LE.18)
CALL TRINC (IOP)
GO TO 99997
99994 IF(.NOT.)
* (IOP.GE.19.AND.IOP.LE.22)
CALL DECR (IOP)
GO TO 99997
99993 IF(.NOT.)
* (IOP.GE.23.AND.IOP.LE.26)
*160 TO 99992
CALL SUM (IOP)
GO TO 99997
99992 IF(.NOT.)
* (IOP.GE.27.AND.IOP.LE.31)
*160 TO 99991
CALL DIFF (IOP)
GO TO 99997
99991 CONTINUE
WRITE (F, 10) IOP
16 FORMAT (18BINVAL) OP CODE: , I2, 25H ENCOUNTERED IN EXECB. )
99997 CONTINUE
CALL BINRT
ICOUNT = ICOUNT + 1
RETURN
END

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SUBROUTINE FINAL
LOGICAL FINIS, ERROR
COMMON IOUT, IJSCR, ICM, ICOUNT, IDIN,
1 MBUSS, MEMC, MEMH, MAINM(1024),
3 MICQ, MSCPAD(16), MSK1, MSR2,
5 NRM(2,3), FINIS, ERROR, PMSTR, MOPND,
COMMON KAD, K04, IOLDB
NEND = NRUN(9)
NVAL = NRUN(10)
IF (.NOT.
    * (MEMD.EQ.1)
    * (.160 TO 99999
    * (.MEMH.EQ.NVAL)
    * (.160 TO 99998
    * FINIS = .TRUE.
99998 CONTINUE
    * GO TO 99997
99999 IF (.NOT.
    * (NEND.EQ.2)
    * (.160 TO 99996
    * (.IF.NOT.
    * (MEMC.EQ.NVAL)
    * (.160 TO 99995
    * FINIS = .TRUE.
99995 CONTINUE
    * GO TO 99997
99996 IF (.NOT.
    * (NEND.EQ.3)
    * (.160 TO 99994
    * (.IF.NOT.
    * (ITIME.EQ.NVAL)
    * (.160 TO 99993
    * FINIS = .TRUE.
99993 CONTINUE
    * GO TO 99997
99994 IF (.NOT.
    * (NEND.EQ.4)
    * (.160 TO 99992
    * (.IF.NOT.
    * (ITIME.EQ.NVAL)
    * (.160 TO 99991
    * FINIS = .TRUE.
99991 CONTINUE
    * GO TO 99997
99992 IF (.NOT.
    * (NEND.EQ.5)
    * (.160 TO 99990
    * (.IF.NOT.
    * (MCAT.EQ.NVAL)
    * (.160 TO 99989
    * FINIS = .TRUE.
99989 CONTINUE
    * GO TO 99997
99996 IF (.NOT.
    * (NEND.EQ.3)
    * (.160 TO 99988
    * GO TO 99997
99988 CONTINUE
    * WRITE (7, 5) NEWD
    * 5 FORMAT (3HJINWALD RUN TERMINATION CODE = , I3, 1H. )
    * ERROR = .TRUE.
99997 CONTINUE
RETURN
END
    
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AD-A031 782

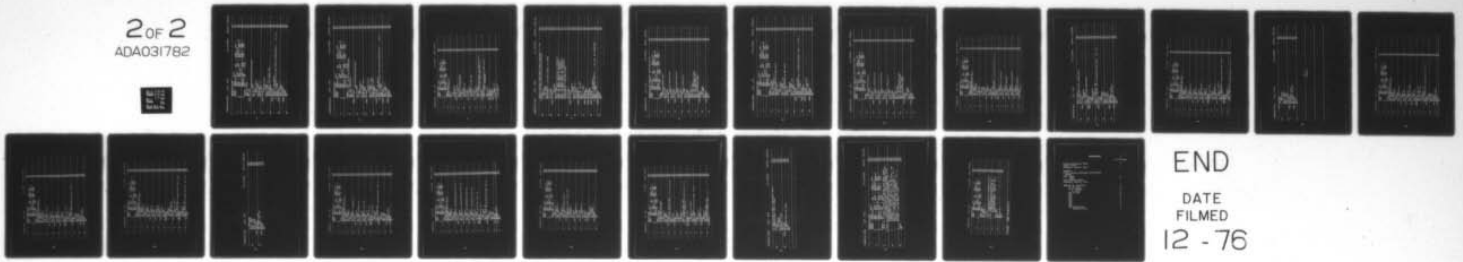
ARMY MISSILE RESEARCH DEVELOPMENT AND ENGINEERING LAB--ETC F/G 9/2  
MULTIPURPOSE DIGITAL MICROPROCESSOR EMULATOR.(U)  
MAY 76 J R BROOKSHIRE

UNCLASSIFIED

RG-76-62

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SUBROUTINE SETMH                                473
LOGICAL FINIS , ERROR                          474
COMMON CNTMEM(1024) , ICN , ICOUNT , IDIN ,    475
      IDOUT , IDSCR , ITELN , MAINM(1024) ,    476
      MBUSS , MEMC , MEMH , MICAD(6) , MICDA(3) , 477
      MICQ , MSCPAD(16) , MSR1 , MSR2 ,        478
      MRUN(2), FINIS , ERROR , MINSTR , MOPMU , 479
      MICRO(25) , MCNT , STIME , IETIME ,      480
COMMON KAD , KDA , IOLDB                       481
DATA MSK /3778/                                482
IMDX = 1                                        483
99999 IF (.NOT.                                484
.160 TO 99998                                  485
IF (.NOT.                                       486
. (NRUN(2).EQ.1)                                488
.160 TO 99997                                  489
MAINM(INDX) = 0                                490
GO TO 99996                                     491
20 99997 IF (.NOT.                               492
. (NRJN(2).EQ.2)                                493
.160 TO 99995                                  494
NEWDX = IMDX - 1                               495
MAINM(INDX) = AND1 (NEWDX, MSK)                496
GO TO 99996                                     497
25 99995 CONTINUE                               498
      WRITE (7, 10) NRJN(2)                    499
      10 FORMAT (4H0SETMH CALLED WITH INVALID OPTION NRUN(2) = , I3, 1H.)
      ERROR = .TRUE.                            500
30 99996 CONTINUE                               501
      IMDX = IMDX + 1                           502
      GO TO 99999                                503
      99998 CONTINUE                             504
      RETURN                                     505
      END                                        506
      99999                                     507

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SUBROUTINE SETCH
LOGICAL FINIS , ERROR
COMMON CNTMEM(1024)
1 IOOUT , IOSCR , ICN , ICOUNT , IOIN ,
2 MBUSS , MEMC , ITELH , MAINM(1024) ,
3 MICQ , MSCPAD(16) , MEMH , MICAD(6) , MICDA(3) ,
4 NRUN(2), FINIS , ERROR , HINSTR , HOPND ,
5 MICRO(25), MCNT , STIME , ITIME , IETIM
COMMON KAD , KDA , IOLOB
10 DATA REPL /08/, REPL2 /5377777620000008/
DATA ADDR /20J00J008/
INDX = 1
99999 IF(.NOT.
. (.NOT.ERROR.AND.INDX.LE.1024)
15 .160 TO 99996
IF(.NOT.
. (NRUN(1).EQ.1)
.160 TO 99997
CNTMEM(INDX) = REPL
20 GO TO 99996
99997 IF(.NOT.
. (NRUN(1).EQ.2)
.160 TO 99995
REPL = REPL2 + ADDR
25 CNTMEM(INDX) = REPL
GO TO 99996
99999 CONTINUE
WRITE (7, 10) NRUN(1)
30 FORMAT ('44H0SETCH CALLED WITH INVALID OPTION NRUN(1) = , I3,IH. )
ERROR = .TRUE.
99996 CONTINUE
INDX = INDX + 1
35 GO TO 99999
99998 CONTINUE
RETURN
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	SUBROUTINE LOAD					584
	LOGICAL FINIS , ERROR					585
	COMMON CMTMETH(28)					586
1	100UT , IDSCR , IDW , ICOUNT , IDIM ,					587
	100USS , WMC , WMA , MICA(16) , MICA(17) ,					588
2	MICQ , MSCAD(16) , MSRI , MSR2 ,					589
3	MICR(2), PINTS , EROR , MEMSTR , MOPMD ,					590
4	MICR(12), MCNT , STIME , IETIM ,					591
5	MICR(13), NDA , TOL(8)					592
	COMMON K80					593
10	DIMENSION CMTFLD(6)					594
	DATA MSKI 7140000000000000000000					595
	KEY = 0					596
	L = 0					597
15	IFT,NOT.					598
	(NRUN(1),EQ.13					599
	160 TO 99999					600
99998	IFT,NOT.					601
	(KEY.EQ.9)					602
20	160 TO 99997					603
	READ(5,10) KEY, MDR, MAIN, CTRL					604
10	FORMAT (11, 7X, 3A, 2A, 06, 016)					605
	IFT,NOT.					606
	(KEY.EQ.1)					607
25	160 TO 99996					608
	MAIN(MADR+1) = MAIN					609
	K = K + 1					610
	GO TO 99995					611
30	99996					612
	IFT,NOT.					613
	(KEY.EQ.2)					614
	160 TO 99994					615
	CNTR(MADR+1) = KOR (MSK1, CNTRL)					616
	L = L + 1					617
	GO TO 99995					618
35	99996					619
	IFT,NOT.					620
	(KEY.EQ.9)					621
	160 TO 99993					622
	WRITE(7, 20) K, L					623
20	FORMAT (20H MEMORY LOAD COMPLETED , 15, 15H WORDS OF MAIN AND ,					624
	15, 32H WORDS OF CONTROL MEMORY LOADED. ,//)					625
	GO TO 99995					626
99993	CONTINUE					627
	WRITE(7, 30) M51					628
30	FORMAT (45H INVALID CONTROL CHARACTER IN MEMORY LOAD CARD = ,					629
	11, 18H, RUN TERMINATED. )					630
	KEY = 9					631
	ERROR = .TRUE.					632
99995	CONTINUE					633
	GO TO 99996					634
99997	CONTINUE					635
	GO TO 99992					636
99999	IFT,NOT.					637
	(NRUN(1),EQ.2)					638
	160 TO 99991					639
99996	IFT,NOT.					640
	(KEY.EQ.9)					641
	160 TO 99989					642

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60 READ (5, 40) KEY, MADR, MAINL, MAINR, (CNTFLD(I), I = 1, 6)
   40 FORMAT (I1, I1, 04, I1, 03, 03, I1, 02, 01, 02, 04, 08)
   IF (.NOT.
     . (KEY.EQ.1)
     .160 TO 99988
     MAINM(MADR+1) = J2 (SHIFT (MAINL, 8), MAINR)
     K = K + 1
     GO TO 99987
99988 IF (.NOT.
     . (KEY.EQ.2)
     .160 TO 99986
     CNTRL = OR (SHIFT, (CNTFLD(1), 3), CNTFLD(2) )
     CNTRL = OR (SHIFT, (CNTRL, 4), CNTFLD(3) )
     CNTRL = OR (SHIFT, (CNTRL, 4), CNTFLD(4) )
     CNTRL = OR (SHIFT, (CNTRL, 10), CNTFLD(5) )
     CNTRL = OR (SHIFT, (CNTRL, 22), CNTFLD(6) )
     CNTMEM(MADR+1) = XOR (MSK1, CNTRL)
     L = L + 1
     GO TO 99987
75 99986 IF (.NOT.
     . (KEY.EQ.9)
     .160 TO 99985
     WRITE (7, 20) K, L
     GO TO 99987
99989 CONTINUE
     WRITE (7, 30) KEY
     KEY = 9
     ERROR = .TRUE.
99987 CONTINUE
     GO TO 99990
99989 CONTINUE
     GO TO 99992
99991 CONTINUE
     WRITE (7, 50) NRJN(11)
     50 FORMAT (20HINVALID NRUN(11) = ,04, 16H. RUN TERMINATED. )
     ERROR = .TRUE.
99992 CONTINUE
     RETURN
95 99992 CONTINUE
     RETURN
     END

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SUBROUTINE GETCH (IADR, IBIITL, IBITN, IBYTE, IFLAG)
LOGICAL FINIS, ERROR
COMMON CNTMEN(1024), ICN, ICOUNT, IOIN,
1 IDOUT, IDSCR, ITELN, MAINM(1024),
2 MBUSS, MENC, MEMH, MICAD(16), MICDAT(3),
3 MICQ, MSCPAD(16), MSR1, MSR2,
4 MROUT(2), FINIS, ERROR, MINSTR, MOPMO,
5 MICRO(25), MONT, STIME, ITIME
COMMON KAD, KDA, IOEOD
IF(.NOT.
. (IADR.LT.0.OR.IADR.GT.1023)
.160 TO 99999
IFLAG = 1
GO TO 99998
15 99999 IF(.NOT.
. (IBITL.LT.1.OR.IBITL.GT.47)
.160 TO 99997
IFLAG = 2
GO TO 99998
20 99997 IF(.NOT.
. (IBITN.LT.1.OR.IBITN.GT.48)
.160 TO 99996
IFLAG = 3
GO TO 99998
25 99996 IF(.NOT.
. ((IBITL + IBITN).GT.48)
.160 TO 99995
IFLAG = 5
GO TO 99998
30 99995 CONTINUE
IFLAG = 0
IOR = IADR + 1
ISTBIT = 48 - IBIITL
IMSK = SHIFT (MASK(1BITN), 1STBIT)
IBYTE = AND (CNTMEN(IOR), IMSK)
NBR = 48 - (IBITL + IBITN)
IYTE = SHIFT (IYTE, -NBR)
99998 CONTINUE
IF(.NOT.
. (IFLAG.NE.0)
.160 TO 99994
IYTE = J
99994 CONTINUE
RETURN
END

```

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SUBROUTINE DCODM
LOGICAL FINIS , ERROR
COMMON CNTMEM(124)
1 IOOUT , IJSCR , ITELN , ICN , ICOUNT , IOIN ,
2 MBUSS , MEYC , MEMH , MICAD(6) , MICDA(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 NRUNT(2) , FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25) , MCNT , STIME , ITIME , IETIM
COMMON KAD , KDA , IOLOB
DATA IOFF /14008/
MEMC = MSCPAD(1)
MSCPAD(1) = MSCPAD(1) + 1
CALL GETMH (MEMC, 0, 0, MIN, IFLAG)
MINSTR = MIN
IF(.NOT.
. (IFLAG.EQ.0)
.160 TO 99999
MEMH = MINSTR + IOFF
CALL GETMH (MEMC, 0, 0, MOP, IFLAG)
MOPND = MOP
IF(.NOT.
. (IFLAG.EQ.0)
.160 TO 99998
MEMC = MOPND + IOFF
60 TO 99997
99998 CONTINUE
WRITE (7, 10) IFLAG
10 FORMAT (43H0INVA-ID CALL TO GETMH FROM DCODM, IFLAG = , I2, 1H. )
ERROR = .TRUE.
99997 CONTINUE
60 TO 99996
99999 CONTINUE
WRITE (7, 10) IFLAG
ERROR = .TRUE.
99998 CONTINUE
RETURN
END

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SUBROUTINE GEIMM (IADR, IBITL, IBITN, IBYTE, IFLAG)
LOGICAL FINIS, ERROR
COMMON CNTMNT(1024), ICN, ICOUNT, IOIN,
1 IOOUT, IDSCR, ITELN, MAINM(1024),
2 MBUSS, MEMC, MEMH, MICAD(16), MICD(13),
3 MICQ, MSCPAD(16), MSR1, MSR2,
4 NRONT(2), FINIS, ERROR, MINSTR, MOPND,
5 MICRO(23), MCNT, STIME, ITIME, IETIM
COMMON KAD, KDA, IOLDB
IF(.NOT.
. IADR.LT.0.OR.IADR.GT.1023)
.160 TO 99999
IFLAG = 1
GO TO 99998
15 99999 IF(.NOT.
. (IBITL.LT.0.OR.IBITL.GT.15)
.160 TO 99997
IFLAG = 2
GO TO 99998
20 99997 IF(.NOT.
. (IBITN.LT.0.OR.IBITN.GT.16)
.160 TO 99996
IFLAG = 3
GO TO 99998
25 99996 IF(.NOT.
. ((IBITL + IBITN).GT.15)
.160 TO 99995
IFLAG = 5
GO TO 99998
30 99995 CONTINUE
IFLAG = 0
IDR = IADR + 1
IBIT = 16 - IBITL
IMASK = SHIFT (MASK(16), IBIT)
IBYTE = AND (MAINM(IADR), IMASK)
NBR = 16 - (IBITL + IBITN)
IByte = SHIFT (IByte, -NBR)
39998 CONTINUE
IF(.NOT.
. (IFLAG.NE.0)
.160 TO 99994
IByte = 0
99994 CONTINUE
RETURN
END
45

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SUBROUTINE BOLN (IOP)
LOGICAL FINIS, ERROR
COMMON CMTM(1024)
1 IOUT, IDSCR, ICN, ICOUNT, IOIN,
2 MBUSS, MEMC, MEMH, MICAD(16), MICDA(3),
3 MICQ, MSCPAD(16), MSR1, MSR2,
4 MRUNTS, FINIS, ERROR, HEMSTR, HOPMD,
5 MICRO(25), MCNT, STIME, IETIM
COMMON KAD, MICRO(25), KCA, IOLDB
10 DATA LMIGH /177778/,
IF (MRUNTS.EQ.1) WRITE (7, 9)
5 FORMAT (27H8SUBROUTINE BOLN ENTERED. )
999999
15 IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOLDB = MSCPAD(13)
IF (.NOT.
. (IOP.EQ.0)
.160 TO 99999
. IF (.NOT.
. (ICN.EQ.0)
.160 TO 99996
ITMP = LMIGH
GO TO 99997
29 99998 IF (.NOT.
. (ICN.EQ.1)
.160 TO 99996
ITMP = 0
GO TO 99997
30 99996 CONTINUE
ERROR = .TRUE.
WRITE (7, 10) IC4, IOP
16 FORMAT (17HINVALID CARRY = ,06,20H IN 80LN, 0P CODE = ,12, 1H.)
99997 CONTINUE
GO TO 99995
99999 IF (.NOT.
. (IOP.EQ.1)
.160 TO 99994
ITMP = AND (MSCPAD(IAR), MSCPAD(18R) )
GO TO 99995
99994 IF (.NOT.
. (IOP.EQ.2)
.160 TO 99993
ITMP = AND (IOIN, MSCPAD(18R) )
GO TO 99995
99993 IF (.NOT.
. (IOP.EQ.3)
.160 TO 99992
ITMP = OR (MSCPAD(IAR), MSCPAD(18R) )
GO TO 99995
99992 IF (.NOT.
. (IOP.EQ.4)
.160 TO 99991
ITMP = OR (IOIN, MSCPAD(18R) )
GO TO 99995
99991 IF (.NOT.
. (IOP.EQ.5)

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.160 TO 99990
ITMP = XOR (MSCPAD(IAR), MSCPAD(IBR) )
GO TO 99995
60 99990 IF(.NOT.
      (IOP.EQ.6)
      .160 TO 99989
ITMP = XOR (IOPIN, MSCPAD(IGR) )
65 99989 CONTINUE
99995 CONTINUE
IF(.NOT.
      (NRUN(3).EQ.2)
      .160 TO 99988
70 WRITE (7, 25) IOP, ITMP
25 FORMAT ( 7HINSTR , 02, 24H EXECUTED, TEMP VALUE = ,06, 1H.)
99988 CONTINUE
IF(.NOT.
      (TH00.EQ.7)
      .160 TO 99987
75 MICQ = ITMP
IDOUT = ITMP
GO TO 99986
99987 CONTINUE
MSCPAD(IGR) = ITMP
80 CALL INMOD (IAR, IBR)
99986 CONTINUE
RETURN
END
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SUBROUTINE INVRT (IOP)
LOGICAL FINIS, ERROR
COMMON
1 IOUT, IJSCR, ICN, ICOUNT, IDIN,
2 MBUSS, MERC, MEH, MICAD(6), MICAD(3),
3 MIC, MSCPAD(16), MSR1, MSR2,
4 MCRU(23), PIMS, ERROR, MEMSTR, MOPND,
5 MICRO(23), MENT, STIME, IETIM
COMMON KAD, KDA, IOL08
10 DATA LHIGH /177783/
IF (NRUN(3).EQ.2) WRITE (7, 9)
5 FORMAT (27H SUBROUTINE INVRT ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOL08 = MSCPAD(IAR)
IF (.NOT.
. (IOP.EQ.7)
) GO TO 9999
ITMP = COMPL(MSCPAD(IAR) )
60 TO 9999B
99999 IF (.NOT.
. (IOP.EQ.8)
) GO TO 99997
ITMP = COMPL (IDIN)
GO TO 99998
99997 IF (.NOT.
. (IOP.EQ.9)
) GO TO 99996
ITMP = COMPL (MSCPAD(IAR) )
60 TO 99998
99996 IF (.NOT.
. (IOP.EQ.10)
) GO TO 99995
ITMP = COMPL (MIC(3))
99995 CONTINUE
99996 CONTINUE
ITMP = AND (ITMP, LMIGH)
IF (.NOT.
. (ICN.EQ.0)
) GO TO 99994
ITMP = IFMP + LMIGH
ITMP = AND (ITMP, LMISHT)
GO TO 99993
99994 IF (.NOT.
. (ICN.LT.0.33, ICN.GT.1)
) WRITE (7, 10) ICN, IOP
10 FORMAT (17H INVERTED-CARRY = 100EIN IN INVRT OP CODE = 1E11H)
ERROR = .TRUE.
99992 CONTINUE
99993 CONTINUE
IF (.NOT.
. (NRUN(3).EQ.2)
) GO TO 99991
WRITE (7, 25) IOP, ITMP
25 FORMAT (17H INSTR = 02, 24H EXECUTED, TEMP VALUE = 106, 1H.)

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SUBROUTINE INVRT 74/74 OPT=1

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99991 CONTINUE
IF (.NOT.
. (MOD.EQ.7)
. ) GO TO 99990
MICQ = IIMP
IOOUT = IIMP
GO TO 99989
65 99956 CONTINUE
MSCPAD(I8R) = IIMP
CALL INMOD (IAR, I8R)
99989 CONTINUE
RETURN
END
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SUBROUTINE CHFLT (ICP)
LOGICAL FINIS, ERROR
COMMON CNTMEM(1024), ICN, ICOUNT, IOEM,
1 IOOUT, IDSCR, IELM, MAINM(1024),
2 MBUSS, MEFC, MEMM, MICRO(6), MICRO(3),
3 MICQ, MSCPAD(16), MSRI, MSR2,
4 NRM0(2), PINIS, ERROR, MINSTR, MOPND,
5 MICRO(23), MC4T, STIME, ITIME, IETIM
COMMON KAD, KDA, IOL08
DATA LHIGH /177778/
10 IF (NRM0(3).EQ.2) WRITE (7, 9)
5 FORMAT (27H0SUBROUTINE COMPL ENTERED. )
MOD = MICRO(2)
15 IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOL08 = MSCPAD(IAR)
IF (.NOT.
. (IOP.EQ.11)
.160 TO 99999
ITMP = COMPL(MSCPAD(IAR))
GO TO 99998
99999 IF (.NOT.
. (IOP.EQ.12)
.160 TO 99997
ITMP = COMPL (ITIM)
GO TO 99998
99997 IF (.NOT.
. (IOP.EQ.13)
.160 TO 99996
ITMP = COMPL (MSCPAD(IBR))
GO TO 99998
99996 IF (.NOT.
. (IOP.EQ.14)
.160 TO 99995
ITMP = COMPL (ME2)
99995 CONTINUE
99998 CONTINUE
ITMP = AND (ITMP, LHIGH)
ITMP = ITMP + ICY
ITMP = AND (ITMP, LHIGH)
IF (.NOT.
. (NRM0(3).EQ.2)
.160 TO 99994
WRITE (7, 25) ICP, ITMP
25 FORMAT (7H0INSTR, 02, 24H EXECUTED, TEMP VALUE = ,06, 14.)
99994 CONTINUE
IF (.NOT.
. (MOD.EQ.7)
.160 TO 99993
MICQ = ITMP
IOOUT = ITMP
GO TO 99992
99993 CONTINUE
MSCPAD(IBR) = ITMP
55 CALL FMM05 (IAR, ICR)
99992 CONTINUE
RETURN
END

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SUBROUTINE TRINC (IOP)
LOGICAL FINIS , ERROR
COMMON CNTNRY(1024) , ICN , ICOUNT , IOIN ,
1 IOOUT , IOSCR , ITELH , MAINH(1024) ,
2 MBUSS , MEMC , MENH , MICAD(6) , MICDA(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 MEMR2 , PFI5 , ERROR , WIMSTR , WOPND ,
5 MICRO(23) , MCNT , STINE , ITIME , IETIM
COMMON KAD , KDA , IOLOB
DATA LHIGH /177793/
IF (NRUN(3).EQ.2) WRITE (7, 9)
5 FORMAT (27#SUBROUTINE TRINC ENTERED. )
NOO = MICRO(2)
IAK = MICRO(3) + 1
ISR = MICRO(4) + 1
IOLOB = MSCPAD(I3R)
IF (.NOT.
. (IOP.EQ.15)
.160 TO 99999
ITMP = MSCPAD(IAR) + ICN
GO TO 99998
99999 IF (.NOT.
. (IOP.EQ.15)
.160 TO 99997
ITMP = IOIN + I24
GO TO 99998
99997 IF (.NOT.
. (IOP.EQ.17)
.160 TO 99996
ITMP = MSCPAD(I83) + ICN
GO TO 99998
99996 IF (.NOT.
. (IOP.EQ.19)
.160 TO 99995
ITMP = MICQ + ICN
99995 CONTINUE
99998 CONTINUE
ITMP = AND (ITMP, LMI34)
IF (.NOT.
. (NRUN(3).EQ.2)
.160 TO 99994
WRITE (7, 25) IOP, ITMP
25 FORMAT (7#MINSTR, 10E12#H EXECUTED, TEMP VALUE = ,08, 1#)
99994 CONTINUE
IF (.NOT.
. (MOD.EQ.7)
.160 TO 99993
MICD = ITMP
IOOUT = ITMP
GO TO 99992
99993 CONTINUE
MSCPAD(I3R) = ITMP
CALL IMOD (IAR, ISR)
99992 CONTINUE
RETURN
END
999 990
991 992
992 993
993 994
994 995
995 996
996 997
997 998
998 999
999 1000
1000 1001
1001 1002
1002 1003
1003 1004
1004 1005
1005 1006
1006 1007
1007 1008
1008 1009
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SUBROUTINE DECTR (IOP)
LOGICAL FINIS , ERROR
COMMON CNTMEN(I124) , ICN , ICOUNT , IDIN ,
1 IDOUT , IDSCR , ITEL , MAINK(I124) ,
5 MSOSS , MEYC , MEHH , MICAD(I16) , MICAD(I1) ,
2 MSR1 , MSR2 ,
3 NRUNTE(I) , PINES , ERROR , MINSTR , MOPHD ,
4 MICRO(I23) , MCVT , STIME , ITIME , IETEM ,
5 MICRO(I2) , KDA , IOL08
COMMON DATA LHIGH /177763/
10 IF (NRUN(I3).EQ.2) WRITE (7, 5)
5 FORMAT (27H0SUBROUTINE DECTR ENTERED. )
MDO = MICRO(I2)
IAR = MICRO(I3) + 1
IBR = MICRO(I4) + 1
IOL08 = MSCPAD(I13)
. (IOP.EQ.19)
. IGO TO 99999
20 ITRP = MSCPAD(IAR)
GO TO 99998
99999 IF (.NOT.
. (IOP.EQ.20)
. IGO TO 99997
25 ITRP = IDIN
GO TO 99998
99997 IF (.NOT.
. (IOP.EQ.21)
. IGO TO 99996
30 ITRP = MSCPAD(IBR)
GO TO 99998
99996 IF (.NOT.
. (IOP.EQ.22)
. IGO TO 99995
35 ITRP = MSCQ
99995 CONTINUE
99998 CONTINUE
IF (.NOT.
. (ICM.EQ.8)
. IGO TO 99994
40 ITRP = ITRP + LMIG4
ITMP = AND (ITMP, LMIG4)
GO TO 99993
99994 IF (.NOT.
. (ICM.LT.6.OR.ICM.GT.11)
. IGO TO 99992
45 WRITE (7, 18) ICM, IOP
18 FORMAT (17H0INVALID CARRY = ,08,21H IN DECTR, OP CODE = ,12,1H.)
99992 CONTINUE
99993 CONTINUE
IF (.NOT.
. (NRUN(I3).EQ.2)
. IGO TO 99991
50 WRITE (7, 25) IOP, ITRP
25 FORMAT (7H0SMGFT - 02V 24H EXECUTED, TEMP VALUE = ,06, 1H.)
99991 CONTINUE
IF (.NOT.

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FTN 4.2+74355 05/11/75 10.06.09.

SUBROUTINE DECTR 7474 OPT=1

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      . (MOD.EI.7)  
      .)60 TO 99990  
      MICQ = ITMP  
      IDOUT = ITMP  
      GO TO 99989  
      39990 CONTINUE  
      MSCPROTISR1 = ITMP  
      CALL INHOD (IAR, I3R)  
      99989 CONTINUE  
      RETURN  
      END
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SUBROUTINE SUM (IOP)
LOGICAL FINIS, ERROR
COMMON CATMEN(124), ICN, ICOUNT, IOIN,
1 IOOUT, IDSCR, ITELN, MAINH(124),
5 MBUSS, MEMC, MICAD(6), MICRO(3),
3 MICQ, MSCPAD(16), MSR1, MSR2,
5 NRUNIZ(2), FINIS, ERROR, MEMSTR, POPNO,
MICRO(23), MC47, STZME, ZETZM,
COMMON KAD, KDA, IOL08
10 DATA LMICH /177769/
IF (MRUN(3).EQ.2) WRITE (7, 5)
5 FORMAT (27H4SUBROUTINE SUM ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IBR = MICRO(4) + 1
IOL08 = MSCPAD(I3R)
IF (.NOT.
. (IOP.EQ.23)
.160 TO 99999
ITMP = MSCPAD(IAR) + MSCPAD(18R) + ICN
GO TO 99998
99999 IF (.NOT.
. (IOP.EQ.24)
.160 TO 99997
ITMP = IOIN + MSCPAD(18R) + ICN
GO TO 99998
99997 IF (.NOT.
. (IOP.EQ.25)
.160 TO 99996
ITMP = MSCPAD(IAR) + MICQ + ICN
GO TO 99998
99996 IF (.NOT.
. (IOP.EQ.26)
.160 TO 99995
ITMP = IOIN + MICQ + ICN
99995 CONTINUE
99998 CONTINUE
ITMP = AND (ITMP, LMICH)
IF (.NOT.
. (MRUN(3).EQ.2)
.160 TO 99994
WRITE (7, 25) IOP, ITMP
25 FORMAT (7H25) IOP, ITMP
99994 CONTINUE
IF (.NOT.
. (MOD.EQ.7)
.160 TO 99993
MICQ = ITMP
IOOUT = ITMP
GO TO 99992
99993 CONTINUE
MSCPAD(I3R) = ITMP
CALL EMMOD (IAR, I3R)
99992 CONTINUE
RETURN
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SUBROUTINE DIFF T10P1
LOGICAL FINIS , ERROR
COMMON CMTM(1224) , ICN , ICOUNT , IDIN ,
1 IDOUT , IJSCR , ITELN , MAINH(1024) ,
2 MBUSS , MEMC , MEMH , MICA0(6) , MICA(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 MQUIC(3) , TIMES , GRCOR , HEMSTR , HOPRO ,
5 MICRO(23) , MENT , STIME , IETIM
COMMON KAD , MDA , IOLOB
10 DATA LHIGH /1777793/
IF (NRUN(3).EQ.2) WRITE (7, 9)
5 FORMAT (27H8SUBSBJTIME DIFF ENTERED. )
MOD = MICRO(2)
IAR = MICRO(3) + 1
IGR = MICRO(4) + 1
IDLOB = MSCPAD(133)
IF (.NOT.
. (IOP.EQ.27)
. (IOP.EQ.29)
. (IOP.EQ.30)
. (IOP.EQ.31)
) THEN
ITMP = MSCPAD(IAR) + AND(OMPL(MSCPAD(IGR)), LHIGH) + ICN
GO TO 99998
99999 IF (.NOT.
. (IOP.EQ.28)
) THEN
ITMP = MSCPAD(IGR) + AND(OMPL(MSCPAD(IAR)) + LHIGH) + ICN
GO TO 99998
99997 IF (.NOT.
. (IOP.EQ.29)
) THEN
ITMP = IGIN + AND(OMPL(MSCPAD(IGR)), LHIGH) + ICN
GO TO 99998
99996 IF (.NOT.
. (IOP.EQ.30)
) THEN
ITMP = MSCPAD(IGR) + AND(OMPL(IGEN), LHIGH) + ICN
GO TO 99998
99995 IF (.NOT.
. (IOP.EQ.31)
) THEN
ITMP = AND(ITMP, -HIGH)
GO TO 99998
99994 CONTINUE
99993 CONTINUE
99992 CONTINUE
99991 CONTINUE
END

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SUBROUTINE PRBIN
LOGICAL FINIS , ERROR
COMMON CNTMEN(1024)
1 IDOUT , IDSCR , ICN , ICOUNT , IDIN ,
2 MBUSS , MEMC , MEMH , MICAD(6) , MICRO(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 MRUN(17) , FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25) , MCVT , STIME , ITIME , IETIM
16 COMMON KAD , KDA , IOLDB
IF (MICRO(6).EQ.1) MSRL = 0
IF (.NOT.
* (MICRO(10).EQ.1)
*160 TO 9999
15 MBUSS = MIN(MEMC + 1)
IDIN = MBUSS
9999 CONTINUE
IF (.NOT.
* (MICRO(13).EQ.1)
*160 TO 9999
20 MBUSS = NOT (OR (MICAD(KAD), IDSCR) )
IDIN = MBUSS
9998 CONTINUE
IF (MICRO(15).EQ.1) MBUSS = OR (MBUSS, MSR1)
ICN = MICRO(17)
IF (.NOT.
* (MICRO(20).EQ.1)
*160 TO 9997
KDA = 1
GO TO 9996
30 9997 IF (.NOT.
* (MICRO(21).EQ.1)
*160 TO 9995
KDA = 2
GO TO 9996
35 9995 IF (.NOT.
* (MICRO(22).EQ.1)
*160 TO 9994
KDA = 3
GO TO 9996
40 9994 CONTINUE
KDA = 0
9996 CONTINUE
IF (.NOT.
* (MICRO(23).EQ.1)
*160 TO 9993
KAD = MICRO(25)
IF (KAD.EQ.0) KAD = 3
9993 CONTINUE
RETURN
50 END

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SUBROUTINE BINRY
LOGICAL
COMMON
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SUBROUTINE BINRY
LOGICAL
COMMON
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COMMON
DATA MSK10 (/1773/)
DATA IOPP (/1889/)
IF (MICRO(11).E3.1) MBOSS = IOOUT
IF (MICRO(11).E3.1) MBOSS = MBOSS
IF (.NOT.
.160 TO 9999
MEMM = MICRO(5)
GO TO 9999
9999 CONTINUE
IF (NRUN(3).EQ.2) WRITE (7, 4) MEMM
MEMM = 0
MICRO(5) = 0
ERROR = .TRUE.
9999 CONTINUE
IF (.NOT.
.160 TO 9999
MEMM = MICRO(5)
M = MEMM + 1
IF (.NOT.
.160 TO 9996
WRITE (7, 5) MEMM, MAINMINI, MBOSS
5 FORMAT (17H MAIN MEMORY LOC. 06, 14H CHANGED FROM , 06, 4H TO ,
10 FORMAT (34H ERROR BIT ON SUB MEMORY = , 06, 4H )
9996 CONTINUE
MAINMINI = MBOSS
9997 CONTINUE
IF (.NOT.
.160 TO 9997
M = MEMM + 1
IF (.NOT.
.160 TO 9999
MEMM = OR (MICRO(5), MSK1)
IF (MAINMINI.EQ.2) WRITE (7, 30) MEMM
30 FORMAT (29H NEXT 4 MODIFIED BY MSK1 TO1 , 06 )
9999 CONTINUE
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SUBROUTINE BINRY 74/74 OPT=1

IF (MICRO(19).EQ.0) MEMO = AND (MBUSS, MSK10)

IF (MICRO(18).EQ.0) ITEL = MBUSS

IF (.NOT.

.(KDA.NE.0)

.)GO TO 99992

MICDA(KDA) = MBUSS

KDA = 0

99992 CONTINUE

IF (NRUN(3).EQ.2) CALL REPT1

RETURN

END

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SUBROUTINE STATS
LOGICAL FINIS , ERROR
COMMON CNTMEM(1024) , ICN , ICOUNT , IOIN ,
1 IOOUT , IDSCR , ITELH , MAINM(1024) ,
2 MBUSS , MEMC , MEMH , MICAD(6) , MICDA(3) ,
3 MICQ , MSCPAD(16) , MSR1 , MSR2 ,
4 NKONT(2), FINIS , ERROR , MINSTR , MOPND ,
5 MICRO(25), MCNT , STIME , ITIME , IETIM
COMMON KAD , KJA , IOLOB
WRITE (7, 10) STIME, ICOUNT, MCNT, MSCPAD, IOIN, IOOUT, MBUSS,
10 ME13, MEMH, MICQ, MICAD, MICDA, ICN, IDSCR, MSR1, MSR2
10 FORMAT (25H1RUN TERMINATED AT TIME : ,F15.0,15H SECONDS AFTER ,
. 16,11H MICROS OR , I9,17H MACROS EXECUTED. //
. 21H0SCRATCHPAD CONTAINS1, /1H , 16( /5X, 08) , //
. 11H0DATA IN = , 08,13H, DATA OUT = , 08, 9H, BUSS = , 08,
15 10H, C-REG = , 04,16H, M-REG = , 04,10H, Q-REG = , 06, //
. 9H0A/D S = , 5(2X,08), 10H, D/A S = , 3(2X,06), //
. 11H0 CARRY = , 12, 20H, INPUT DISCRETES = , 08, //
. 9H0 MSR1 = , 11, 9H, MSR2 = , 11 )
RETURN
END
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SUBROUTINE REPT1
LOGICAL FINIS , ERROR
COMMON CMTMEM(1024)
1 IDOUT , IDSCR , ICH , ICOUNT , IOIM ,
2 MESS , MEMC , ITEL , MAINH(1024)
3 MICQ , MSCPAD(16) , MEMT , MICRO(16) , MICDAT(1) ,
4 NCONT(27) , PINES , ERROR , MEMSTR , MOPMD ,
5 MICRO(25) , MENT , STIME , ITIME , IETIM
COMMON KAD , KDA , IOLDB
10 INSTR = MICRO(1)
MOD = MICRO(2)
IA = MICRO(3) + 1
IB = MICRO(4) + 1
I = IA - 1
J = IB - 1
WRITE (7,10) INSTR,MOD,I,MSCPAD(IA),J,IOLDB,MSCPAD(1B),MICQ2,MICQ
10 FORMAT (18HEXECUTED OP CODE ,02,15H WITH MODIFIER ,11,1M, //
11 A-REG ,05,12H CONTENTS = ,06,77 PH B-REG ,02,
12 H CONTENTS INITIALLY = ,06,8H, NOM = ,06, //
13 H B-REG CONTENTS INITIALLY = ,06,8H, NOM = ,06, //
14 H TELM CONTENTS INITIALLY = ,06,8H, NOM = ,06, // )
ITEL2 = ITEL
MICQ2 = MICQ
RETURN
END
SUBROUTINE REPT2
RETURN
END

```

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