HDL-TR-1745

Permanent and Transient Radiation Effects on Thin-Oxide (200-Å) MOS Transistors

June 1976

U.S. Army Material Development and Readiness Command
HARRY DIAMOND LABORATORIES
Adelphi, Maryland 20783

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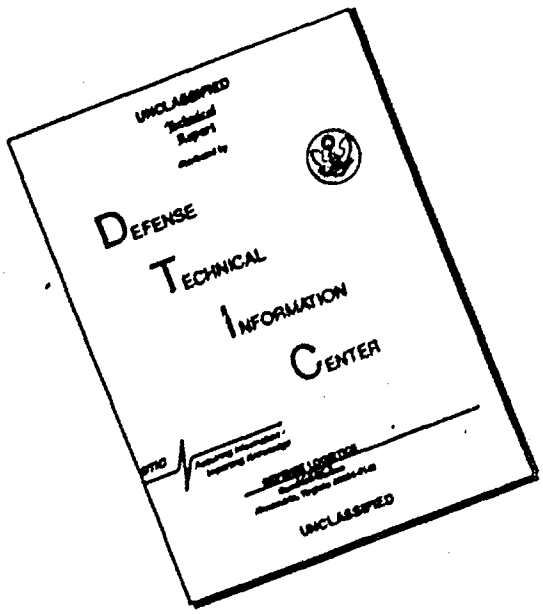

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: HDL-TR-1745

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle): Permanent and Transient Radiation Effects on Thin-Oxide (200-Å) MOS Transistors

5. TYPE OF REPORT & PERIOD COVERED: Technical Report

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s): Stewart Share, Robert A. Martin

8. CONTRACT OR GRANT NUMBER(s): DA: 1T161102AH44

9. PERFORMING ORGANIZATION NAME AND ADDRESS: Harry Diamond Laboratories, 2800 Powder Mill Road, Adelphi, MD 20783

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: Program: 6.11.02.A

11. CONTROLLING OFFICE NAME AND ADDRESS: U.S. Army Materiel Development & Readiness Command, Alexandria, VA 22333

12. REPORT DATE: June 1976

13. NUMBER OF PAGES: 25

14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)

15. SECURITY CLASS. (of this report): UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

DH-1-T-161102-11H-44

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

HLL-A44636

18. SUPPLEMENTARY NOTES

HDL Project No.: A44636
DRCMS Code: 61110211H4400

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Radiation effects
MOS transistor

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

An approach for hardening metal oxide semiconductor (MOS) transistors to ionizing radiation by reducing the thickness of the gate oxide is presented. It is shown that Si gate, n-channel MOS field-effect transistors with oxides 200 Å thick continue to operate in the enhancement mode after irradiation to 10^6 rads(Si) with a positive bias applied to the gate during the irradiation. This represents a considerable improvement

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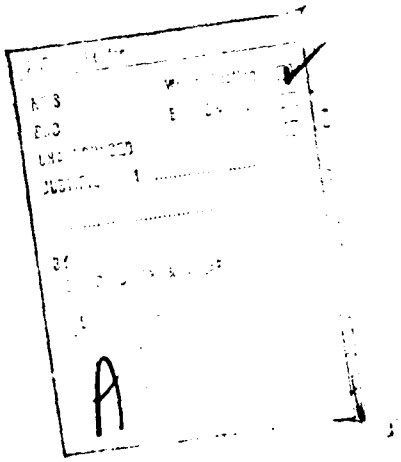
over conventional thick-oxide (~1000-Å) devices, which go into the depletion mode of operation at 10^5 rads(Si). The thin-oxide devices after exposure to pulsed ionizing radiation showed improved performance over that of thick-oxide devices. It was found also that device operation following irradiation depended on the source-drain spacing (channel length): Shortening the channel length leads to an increased shift of the threshold voltage induced by irradiation.



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1. INTRODUCTION

Utilization of metal oxide semiconductor (MOS) devices in military systems provides many advantages. These include reduced power consumption, increased packing density, and noise immunity. Particularly attractive applications include on-board computers, high-speed switching, and logic networks.

Ionizing radiation environments commonly encountered in strategic systems are particularly damaging to MOS devices. For doses as low as 10^4 rads(Si), commercially available transistors have been shown to go into depletion mode of operation,[1] making them unusable for complementary (C) MOS logic applications. Several schemes have been suggested and demonstrated to produce MOS transistors that are less sensitive ("hardened") to ionizing radiation. These include doping the gate oxide (SiO_2) with various impurities such as Al or Cr, using Al_2O_3 in place of SiO_2, and fabricating a clean SiO_2 oxide that is free of impurities. Whereas the first two techniques yield devices that are greatly improved from a radiation standpoint, problems of preirradiation operational stability and manufacturing yield still exist. Although clean oxide devices have exhibited radiation hardness to 10^6 rads(Si) on laboratory units,[2] they are not yet commercially available for system applications.

An alternative approach for hardening is discussed in this report. The magnitude of the oxide charge buildup induced by irradiation and therefore the magnitude of the transistor threshold voltage shift is dependent on the thickness of the oxide.[3,4] Conventional devices have gate-oxide thicknesses on the order of 1000 Å. Irradiation of MOS capacitors with various oxide thicknesses showed that, indeed, the effect of the oxide charge buildup decreased dramatically in going from 1500- to 30-Å-thick oxides.[3] These results suggested that an alternative approach for radiation hardening MOS transistors would be to reduce the oxide thickness.

In this report, we discuss the effect of ionizing radiation on n-channel MOS transistors with oxides 200 Å thick. The n-channel devices were chosen for the study because the irradiation is particularly severe, causing the devices to be converted to the depletion mode of operation. Both permanent and transient damage effects are discussed. Also included is a dependence of the voltage threshold shift on the distance between the source and drain (channel length).[5]

2. FABRICATION PROCEDURE

The transistors used in this study were obtained from the IBM Thomas J. Watson Research Center and were part of a program that incorporated the use of thin-oxide field-effect transistors (FET's) into integrated memory prototypes.[6]

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[1] *R. A. Burghard and C. W. Gwyn, IEEE Trans. Nucl. Sci., NS-20, No. 6 (1973), 300.*

[2] *[Silicon-on-sapphire CMOS research devices have recently been reported to exhibit radiation hardening to 10^6 rads(Si).] K. Aubuchon and E. Harari, IEEE Trans. Nucl. Sci., NS-22 (December 1975).*

[3] *S. Share, A. S. Epstein, V. Kumar, W. E. Dahlke, and W. Haller, J. Appl. Phys., 45 (1974), 4894.*

[4] *J. G. Fossum, G. F. Derbenwick, and B. L. Gregory, IEEE Trans. Nucl. Sci., NS-22 (December 1975).*

[5] *S. Share and R. A. Martin, IEEE Trans. Electron Devices, ED-22, No. 8 (1975), 619.*

[6] *D. L. Critchlow, R. H. Dennard, and S. E. Schuster, IBM J. Res. Dev., 17 (1973), 430.*

They were fabricated[7] with Si-gate n-channel technology using a SiO_2 gate-oxide thickness of 200 Å and a shallow phosphorus diffusion of 0.5 μm on a 0.7-ohm-cm B-doped <100> Si substrate. The thickness of the self-aligned n^+ polysilicon gate was kept at 3500 Å. The oxide was grown in dry O_2 at a temperature of 1000°C, followed by a N_2 anneal (1000°C, 10 min). Six devices were fabricated on a chip with the effective channel length, L_{eff}, varying from 1 to 9.3 μm. In table I, L_{eff} is listed for each of the six devices, along with the channel width, W, the ratio W/L_{eff}, and the preirradiation threshold voltage, V_t. The L_{eff} is obtained by reducing the dimension of the channel length mask by the contribution from the polyetch (0.7 μm) and the underdiffusion (0.8 μm).[7]

TABLE I. PREIRRADIATION DEVICE CHARACTERISTICS

Effective channel length (μm)	Channel width (μm)	Width/length ratio	Preirradiation threshold voltage (V)
1.0	11.4	11.4	0.32
1.3	11.4	8.7	0.46
1.6	11.4	7.0	0.50
2.0	11.4	5.9	0.52
3.5	33.0	9.3	0.50
9.3	89.5	9.7	0.48

3. RADIATION FACILITY

Permanent-damage studies were performed by subjecting the transistors to varying doses of gamma radiation to a total dose of 10^6 rads(Si). A ^{60}Co source was used for the irradiations (dose rate of 1.93 Mrads(Si)/hr).

Transient measurements were performed at the Naval Research Laboratory linear accelerator (LINAC). The LINAC was operated in the single-pulse electron mode at a nominal pulse width of 1 μs. The energy of the electron beam was 30 MeV. Dosimetry was performed by use of CaF thermoluminescent dosimeters read on a Harshaw thermoluminescent detector reader 2000-B.

4. THEORY

Ionizing irradiation generally affects the transistor by causing a shift of the drain-current (I_d)-gate-voltage (V_G) characteristic along the voltage axis. For a transistor operated above pinchoff, i.e., $V_{DS} > V_{GS} - V_t$ (where V_{DS} is the drain-to-source voltage, V_{GS} is the gate-to-source voltage, and V_t is the

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[7] *R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. Leblanc, IEDM, Technical Digest, Washington, DC (3 December 1973), 152; IEEE J. Solid-State Circuits, SC-9, No. 5 (1974), 256.*

threshold voltage) and for $V_{GS} > V_t$, the $I_d - V_G$ characteristic is given by[7]

$$I_d = \frac{\mu_{eff}\epsilon_{ox}\epsilon_o}{t_{ox}} \frac{W}{L_{eff}} \left(V_{GS} - V_t\right)^2 , \tag{1}$$

where

μ_{eff} is an effective channel mobility,

ϵ_{ox} is the SiO_2 dielectric constant,

ϵ_o is the free-space dielectric constant,

t_{ox} is the oxide thickness.

The threshold voltage, the gate-to-source voltage at which the device turns on, is written[7]

$$V_t = \frac{t_{ox}}{\epsilon_o\epsilon_{ox}} \left[-Q_{ss} - Q_{ox} + \left(2\epsilon_o \epsilon_{Si} qN_a \left(V_{sub} + \psi_s\right)\right)^{\frac{1}{2}} \right] + \Delta W_f + \psi_s , \tag{2}$$

where

Q_{ss} is the density of fast interface charge at the Si-SiO_2 boundary,

Q_{ox} is the effective (image) density of oxide charge,

ϵ_{Si} is the Si dielectric constant,

V_{sub} is the substrate bias,

ψ_s is the voltage across the depletion layer at the onset of conduction in the absence of a substrate potential,

N_a is the impurity concentration in the substrate,

q is the electronic charge,

ΔW_f is the metal (gate)-semiconductor work function difference (equal to 0 V for the polysilicon gates[8] studied here).

The effect of the ionizing radiation is to introduce positive charge ΔQ_{ox} into the oxide, and fast-interface states, N_{ss}, at the Si-SiO_2 boundary. This introduction produces a shift of the threshold voltage, ΔV_t,[9]

$$\Delta V_t = -\frac{t_{ox}}{\epsilon_o\epsilon_{ox}} \Delta Q_{ox} - \frac{t_{ox}}{\epsilon_o\epsilon_{ox}} qN_{ss} , \tag{3}$$

---

[7] *R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. Leblanc, IEDM, Technical Digest, Washington, DC (3 December 1973), 152; IEEE J. Solid-State Circuits, SC-9, No. 5 (1974), 256.*

[8] *G. D. Hachtel and M. H. Mack, IEEE Solid-State Circuits Conference, Digest of Technical Paper (1973), 110.*

[9] *K. H. Zaininger and A. G. Holmes-Siedle, RCA Rev., 28 (1967), 208.*

and therefore a shift of the $I_d - V_G$ characteristic. Because the induced charge is positive, the shift is in the negative voltage direction.

The variation of ΔQ_{ox} with oxide thickness depends on the location of radiation-induced positive charge in the oxide. For example, irradiation of MOS capacitors with wet oxides ranging in thickness from 30 to 1500 Å indicated that the trapped charge was located in a uniform sheet within 160 Å from the interface.[3]

For this case,

$$\Delta Q_{ox} = qN_t d\,(1 - d/2t_{ox}),\ d < t_{ox} \quad . \tag{4}$$

where d is the thickness of the sheet of charge and N_t is the density of hole-like trapping centers. If the trapped charge extends uniformly throughout the oxide, then

$$\Delta Q_{ox} = \frac{qN_t t_{ox}}{2} \tag{5}$$

The density of radiation-induced fast interface states also has been found to depend on the oxide thickness. For the wet oxides discussed above, the thickness dependence was found to be similar to that of the ΔQ_{ox}.[10]

5. EXPERIMENTAL PROCEDURE

The threshold voltage was obtained from the voltage intercept of the plot of $(I_d)^{\frac{1}{2}}$ versus V_g (see eq. (1)). For this measurement, V_S was held at 0 V, V_{sub} was at −1 V, and V_D was at 4 V. The I_d was obtained from the voltage drop across a 10-kilohm resistor in the drain circuit. Maximum I_d was 100 μA. The pre-irradiation threshold voltages (table I) were approximately 0.5 V for all channel lengths tested, except the 1-μm channel device, which was approximately 0.3 V. This reduced value is typical for devices with short channels and is due to the penetration of the drain field into the channel region normally controlled by the gate.[7] This short channel effect enhances the field in the channel and aids in turing on the device.[6]

For the permanent-damage studies, the devices were irradiated with V_{sub} at −1 V and V_S and V_D at 0 V. A gate voltage of 0.5 V was applied to six devices on one chip during the irradiation. Six devices on another chip were irradiated with zero bias (ground) applied to the gate. The $I_d - V_G$ characteristics were taken within 15 min after each irradiation without the devices being removed from the test fixture. The total time of irradiation was 31 min, resulting in a total dose of 10^6 rads(Si).

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[3] *S. Share, A. S. Epstein, V. Kumar, W. E. Dahlke, and W. Haller, J. Appl. Phys., 45 (1974), 4894.*

[6] *D. L. Critchlow, R. H. Dennard, and S. E. Schuster, IBM J. Res. Div., 17 (1973), 430.*

[7] *R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. Leblanc, IEDM, Technical Digest, Washington, DC (3 December 1973), 152; IEEE J. Solid-State Circuits, SC-9 No. 5 (1974), 256.*

[10] *W. Haller, S. Share, A. S. Epstein, V. Kumar, and W. E. Dahlke, J. Electrochem. Soc., 123 (1976), 578.*

Transient damage studies were performed at typical operating voltage levels, namely, V_{sub} at $-1.0V$, V_S at 0 V, V_D at 4 V, and V_G at 0 V. The I_d V_G characteristics were recorded on oscillograms prior to the electron pulse and at several times following it: 100 μs and 1, 10, 100, and 1000 s. A 1-V, 100-μs ramp was applied to the gate, and the current was read across a 10-kilohm resistor. The test setup is shown in figure 1.

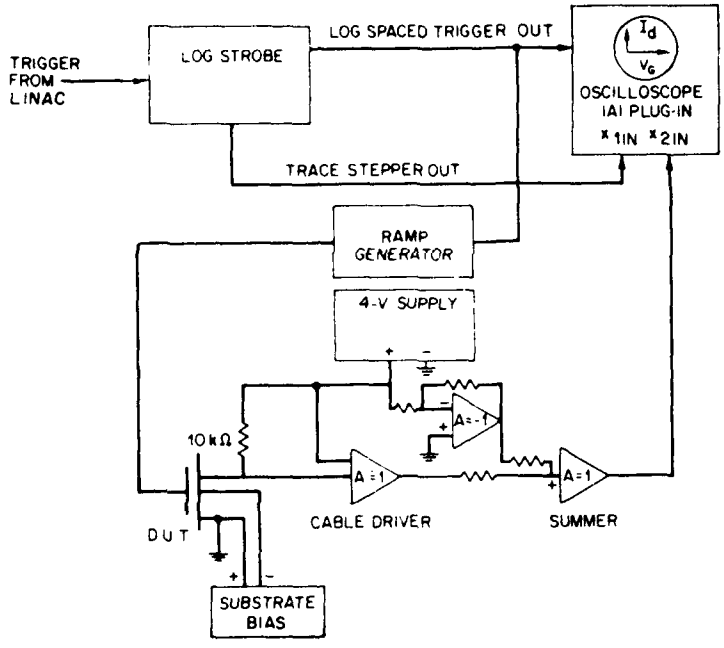

Figure 1. Test setup for transient radiation measurements.

6. EXPERIMENTAL RESULTS

6.1 Permanent Damage Effects

The effect of ^{60}Co irradiation on a transistor with a 0.3-μm channel length is given in figure 2. The $(I_d)^{\frac{1}{2}}$ is plotted against V_G after various irradiations ranging from 0 to 10^6 rads(Si) and with a positive gate bias (V_G = 0.5 V) applied during each irradiation. For $V_G > V_t$, the square-law dependence of gate voltage on drain current was observed as expected, since $V_{DS} > (V_G - V_t)$ in the current range tested. Increasing the gamma dose resulted in a nearly parallel shift of the $(I_d)^{\frac{1}{2}}$ V_G characteristic toward negative voltages. Irradiation with V_G at 0 during the irradiation resulted in a shift of the $(I_d)^{\frac{1}{2}}$ - V_G characteristic in the negative voltage direction though smaller than observed when a bias was applied to the gate. This

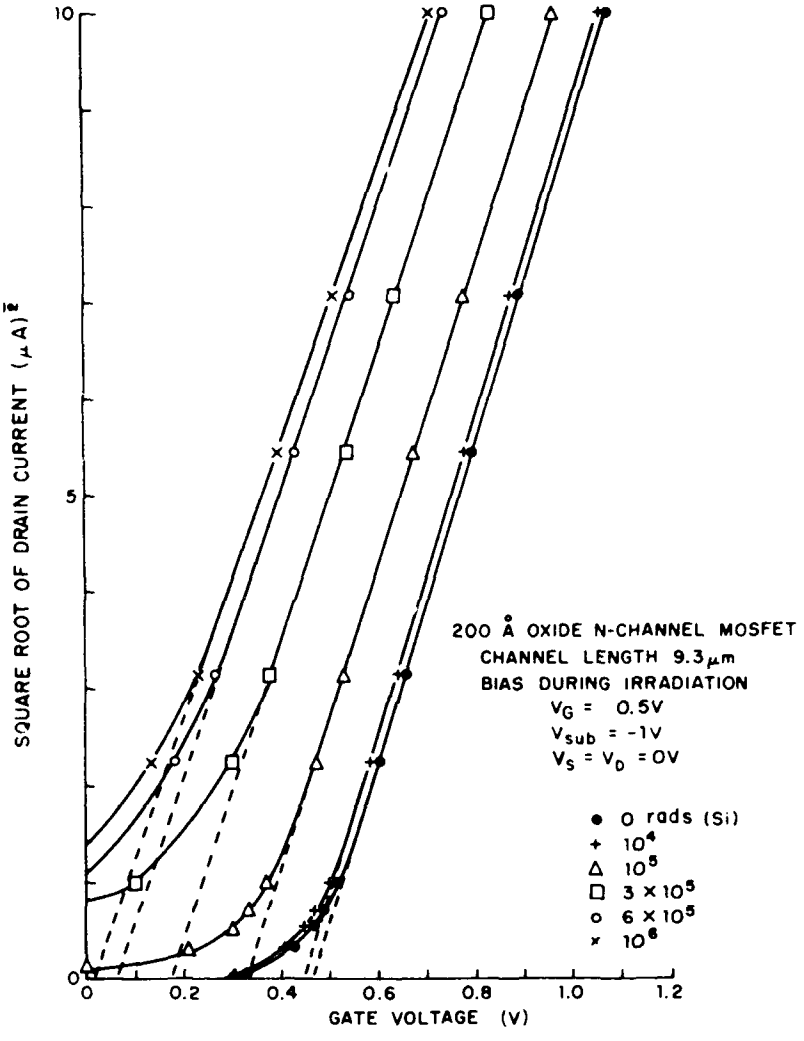

Figure 2. Square root of drain current versus gate voltage of 9.3-μm channel length transistor after various radiation doses.

shift is illustrated in figure 3, in which the threshold voltage shift, ΔV_t, is plotted versus gamma dose for the two bias conditions. The ΔV_t is equal to the difference between the post- and preirradiation threshold voltages. Similar results were obtained for transistors with shorter channel lengths, except that the shift of V_t induced by irradiation was observed to increase as the channel length was shortened. This increase is illustrated in figure 4, in which ΔV_t is plotted versus the gamma dose for the various channel lengths with a positive gate bias (0.5 V) applied during irradiation. Figure 5 shows the threshold voltage shift with V_G at 0 V during irradiation. The data for the devices of 1.3- and 1.6-μm channel length were nearly similar, so the 1.6-μm data are not shown. The lines in these two figures, as well as in figure 3, are drawn to indicate a trend of the data with gamma dose.

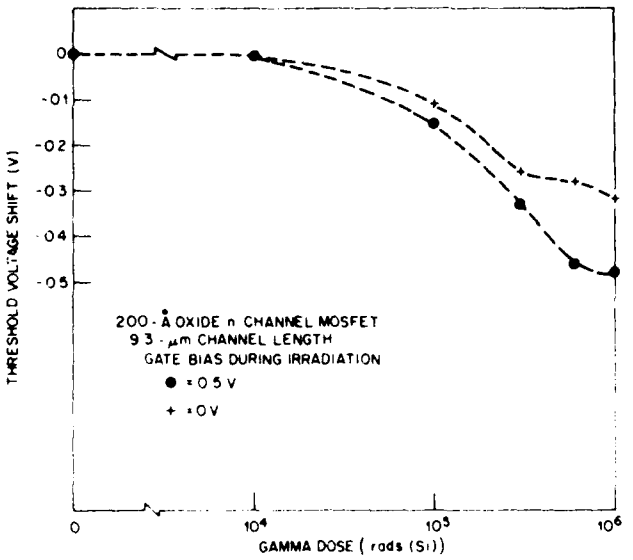

Figure 3. Threshold voltage shift of 9.3-μm channel length transistor versus dose for gate voltage = 0.5 and 0 V during irradiation. (The threshold voltage is obtained from the voltage intercept of the square root of drain current versus the gate voltage.)

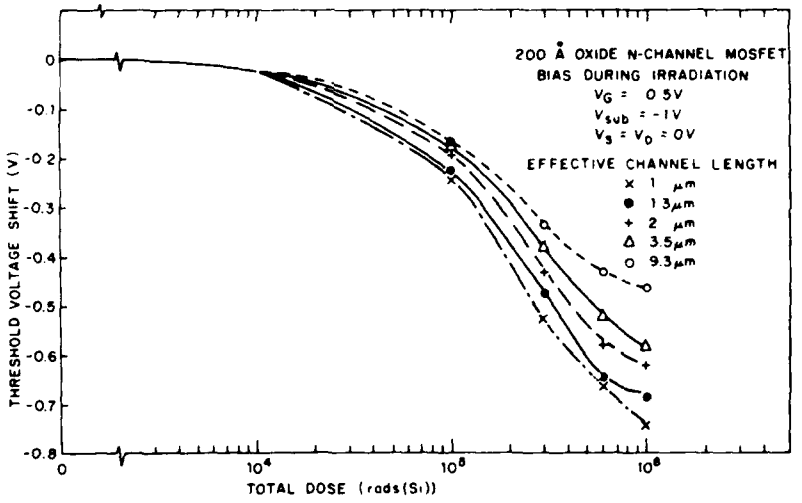

Figure 4. Threshold voltage shift versus radiation dose for various channel length transistors. The gate voltage = 0.5 V during irradiation. (The threshold voltage is obtained from the voltage intercept of the square root of the drain current versus the gate voltage.)

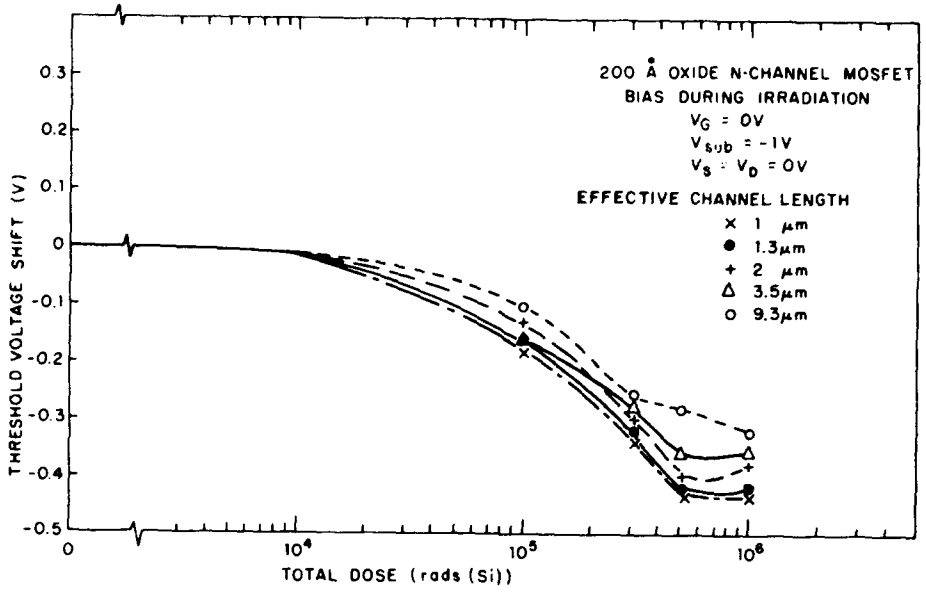

Figure 5. Threshold voltage shift versus radiation dose for various channel length transistors. The gate voltage = 0 V during irradiation. (The threshold voltage is obtained from the voltage intercept of the square root of the drain current versus the gate voltage.)

It is sometimes useful to define V_t as that V_G necessary to cause a particular I_d. In figure 6, the threshold voltage measured at 10 μA, V_t(10 μA), is plotted versus dose(V_G = 0.5 V during irradiation). With the threshold voltage defined in this way, devices with 2-, 3.5-, and 9.3-μm channel lengths continued to operate in the enhancement mode even for doses of 10^6 rads(Si) and with a positive gate bias applied during irradiation. This operation can be compared with biased *n*-channel devices with a 1200-Å SiO_2 gate insulator that go into depletion (V_t(10 μA) ≤ 0) for doses on the order of 10^5 rads(Si).[11] For transistors with channel lengths less than 2 μm, the devices do go into depletion (with the threshold voltage defined in this way) when irradiated to 10^6 rads(Si) under positive bias (V_G = 0.5 V). This is illustrated by the data for the 1- and 1.3-μm channel length (fig. 6).

[11] *E. E. King, G. P. Nelson, and H. L. Hughes, IEEE Trans. Nucl. Sci., NS-19, No. 6 (1972), 264.*

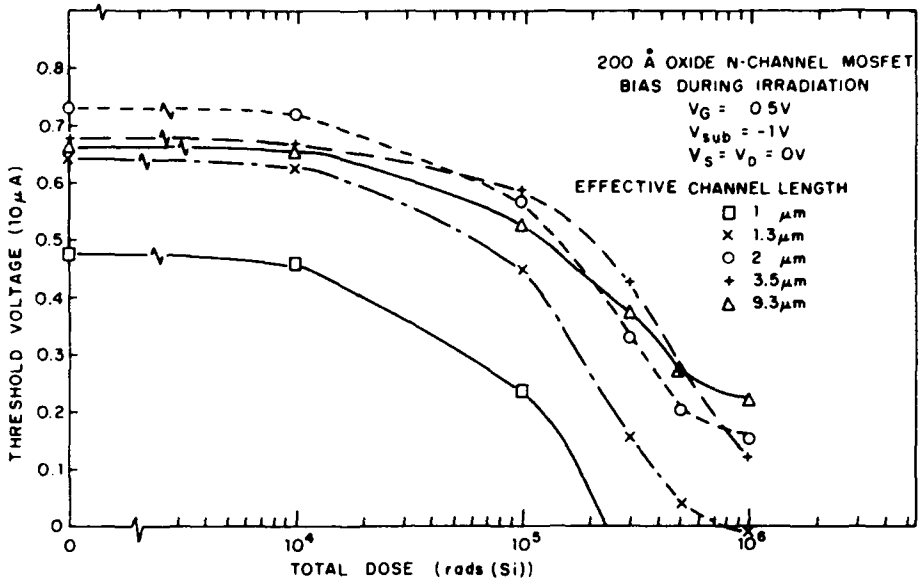

Figure 6. Threshold voltage (defined at 10-μA drain current) versus radiation dose for various channel lengths.

6.2 Transient Damage Effects

The effect of a 93-krad(Si) LINAC electron pulse on a transistor with a 9.3-μm channel is shown in figure 7. The $(I_d)^{\frac{1}{2}}$ - V_G curves are plotted prior to irradiation and at 100 μs, and 1, 10, 100, and 1000 s after the pulse. With a pulse width of 1 μs, the dose rate was about 10^{11} rads(Si)/s. The V_G was 0 V during the radiation pulse. These measurements were performed on a device that had been irradiated to 10^6 rads(Si) and then allowed to anneal at room temperature for 1 yr. Comparing the preirradiation $(I_d)^{\frac{1}{2}}$ - V_G curves in figures 7 and 2, one sees that complete annealing of the current-voltage characteristics took place in this time; the threshold voltage returned to its preirradiation value of 0.45 V.

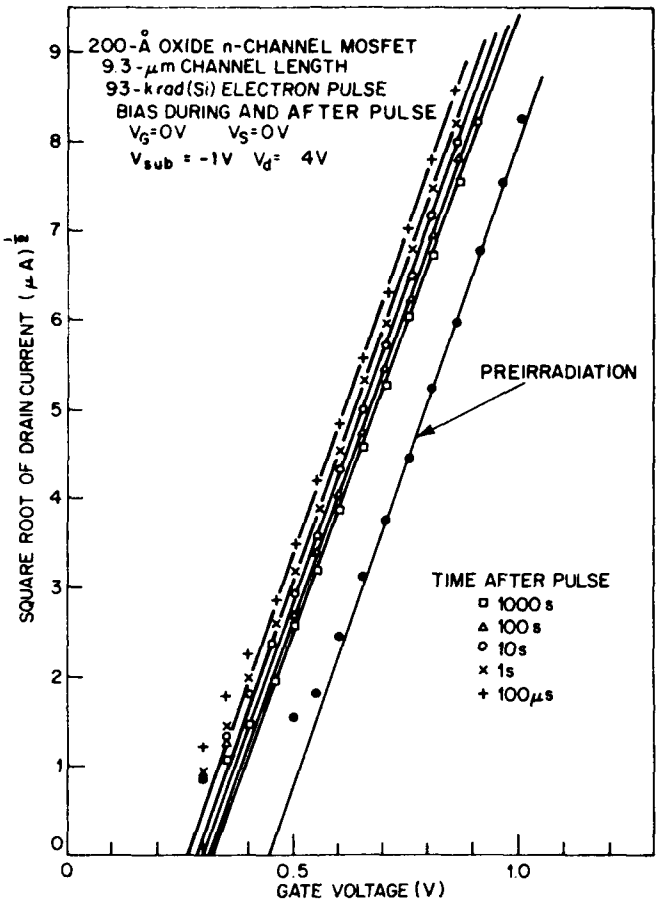

Figure 7. Square root of drain current versus gate voltage of 9.3-μm channel length transistor both before and at various times after an ionizing electron pulse.

Figure 7 shows that the ionizing electron pulse causes a shift of the current-voltage curve toward negative voltages. The data show a continuous annealing with time back toward the preirradiation curve. The fact that the postirradiation $(I_d)^{\frac{1}{2}} - V_G$ curves are parallel to the preirradiation curve indicates that little annealing took place during the time required to sweep out each current-voltage characteristic (100 μs). Figure 8 plots the threshold voltage shift obtained from figure 7 for various times after the radiation pulse. The broken line denotes a trend of the data with time. The threshold voltage shift at 100 μs after the pulse is -0.18 V. At 1000 s after the pulse, annealing reduces the shift to -0.13 V, which agrees (within error of the measurement) with the value obtained after 10^5 rads(Si) irradiation at the ^{60}Co source. At 100 μs after the pulse, the device continues to operate in the enhancement mode ($V_t > 0$ V).

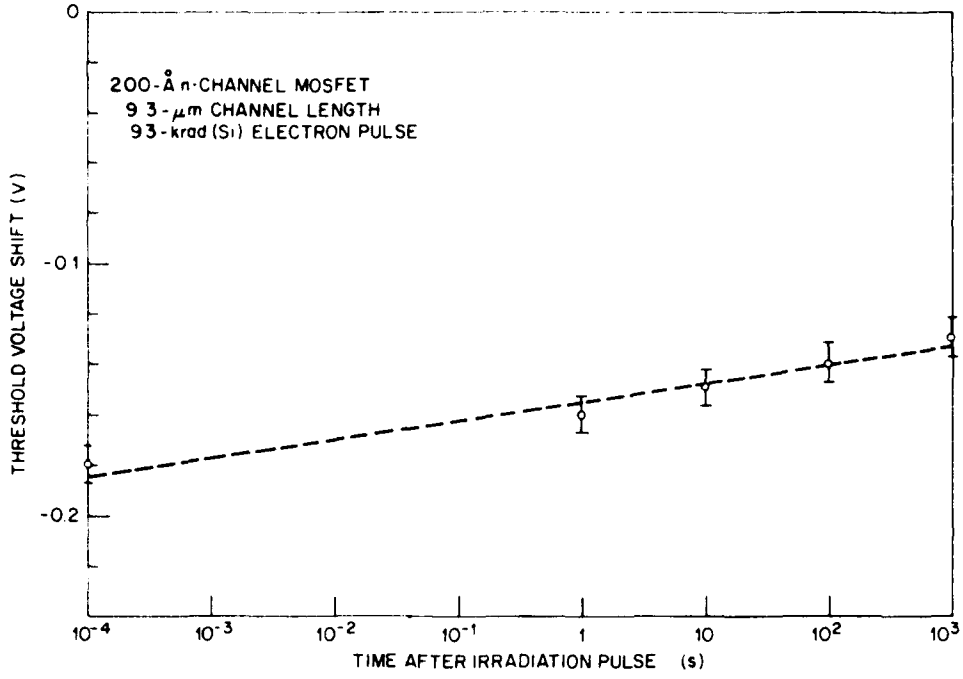

Figure 8. Annealing of threshold voltage shift at various times after an ionizing electron pulse.

7. DISCUSSION

7.1 Permanent Damage

The effect of ionizing radiation on the 200-Å transistor with a 9.3-μm channel length is discussed first. Figure 2 shows after each successive gamma dose a nearly parallel shift of the $(I_d)^{\frac{1}{2}} - V_G$ characteristic along the negative voltage direction. The 15-percent decrease in the slope of the $(I_d)^{\frac{1}{2}} - V_G$ characteristic (equivalent to a 25-percent decrease in the gain factor defined as the square of the slope) observed when the 10^6 rads(Si) irradiation value is compared with the preirradiation value is usually attributed to a decrease in the μ_{eff}. This is generally produced by increased scattering from surface states and trapped oxide charge near the interface introduced by irradiation.[12] The increased leakage current observed for the higher radiation doses ($>10^5$ rads(Si)) is thought to be due to radiation-inouced interface states.[1]

The threshold shift shown in figure 3 induced by the irradiation was observed to be larger with a positive gate bias (0.5 V) applied during the irradiation than with 0 V applied during the irradiation. The respective fields across the 200-Å oxide are 4.7×10^5 V/cm and 3.1×10^5 V/cm, respectively, for the two bias conditions. This bias dependence was also observed in the irradiation of devices with thicker

[1] *R. A. Burghard and C. W. Gwyn, IEEE Trans. Nucl. Sci., NS-20, No. 6 (1973), 300.*
[12] *J. Kassabov, N. Velcher, and S. Kashiena, Surf. Sci., 21 (1970), 366.*

oxides (1200 Å).[9] Experimentally it is observed that the threshold shift tends to saturate for fields in the range of 5×10^5 V/cm.[13]

The threshold shifts observed for the 200-Å devices studied here were much less than for conventional devices with thicker oxides. For example, a threshold shift of -0.16 V was observed for the 200-Å transistor (9.3-μm channel length) irradiated to a dose of 10^5 rads(Si) under a positive gate bias of 0.5 V. This is compared with typical threshold shifts of -1.5 V observed for n-channel transistors with 1200-Å oxides subjected to similar radiation conditions,[11] i.e., the same total dose and field across the oxide during irradiation. Assuming that the density of trapping centers, N_t, is the same for both oxide thicknesses, this thickness dependence of ΔV_t is consistent with the trapped charge residing in a uniform layer within 160 Å from the Si-SiO_2 interface (equations (3) and (4)),

$$\Delta V_t = \frac{t_{ox}}{\epsilon_{ox}\epsilon_o} qN_t d\left(1 - \frac{d}{2t_{ox}}\right). \tag{6}$$

The effect of N_{ss} on ΔV_t may be neglected, since it is smaller than ΔQ_{ox}.[10] Reducing the oxide thickness to 200 Å prevents the transistor from going into the depletion mode (at 10^6 rads(Si)). For conventional devices with 1200-Å thick oxides, a 1.5-V threshold shift is enough to convert the transistor to the depletion mode of operation.[11] Increasing the dose to 10^6 rads(Si) resulted in a 0.45-V threshold shift for the 200-Å device (9.3-μm channel length), which is considerably smaller than that predicted (and observed) for the thick-oxide devices (approximately 5 to 10 V).

The dependence of ΔV_t on channel length is shown in figures 4 and 5. For devices with the same channel length, ΔV_t was larger when a positive gate bias (0.5 V) was applied during irradiation than when 0 V was applied during irradiation. Decreasing the channel length from 9.3 to 1.0 μm results in an increase of ΔV_t on irradiation for either bias condition. There are two possible explanations for such an effect. First, as the channel becomes shorter, the contribution to the applied (fixed) field across the oxide from the source and drain depletion regions becomes larger. This is equivalent to irradiating the devices under a progressively increasing (more positive) gate bias as the channel length is decreased. As shown above, ΔV_t increased as the gate bias increased (during irradiation). Second, this channel length dependence could be due also to the fact that in short-channel devices, a greater portion of the oxide may be contaminated from the source-drain diffusion than in long-channel devices. This contamination could result in an accumulation of residual impurities in the oxide. The presence of these impurities may be responsible for the increased radiation sensitivity of the short-channel devices. However, more work is needed to determine which mechanism dominates.

7.2 Transient Damage

A pulse of ionizing radiation produces a negative shift of threshold voltage as shown in figure 8. Prior to the earliest time of measurement after the ionizing pulse (100 μs), the high-mobility electrons

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[9] *K. H. Zaininger and A. G. Holmes-Siedle, RCA Rev., 28 (1967), 208.*
[10] *W. Haller, S. Share, A. S. Epstein, V. Kumar, and W. E. Dahlke, J. Electrochem. Soc., 123 (1976), 578.*
[11] *E. E. King, G. P. Nelson, and H. L. Hughes, IEEE Trans. Nucl. Sci., NS-19, No. 6 (1972), 264.*
[13] *G. F. Derbenwick and B. L. Gregory, IEEE Trans. Nucl. Sci., NS-22 (December 1975), 2151.*

are swept out of the oxide under the action of the internal field, leaving only the low-mobility holes uniformly distributed throughout the oxide. The resultant hole density generated in the SiO_2 is given by[14]

$$N_+ = \frac{kD\rho_{ox}f}{\epsilon_\rho} \text{ (cm}^{-3}\text{)} , \tag{7}$$

where

D is the oxide dose in rads,

ρ_{ox} is the SiO_2 density,

ϵ_ρ is the ionization energy for generation of an electron-hole pair in thermally grown SiO_2 (equal to 18 eV/pair),[15]

f is the fraction of carriers escaping fast recombination at their point of origin following generation by the high-energy electron pulse,

$k = 6.25 \times 10^{15}$ eV/rads · g .

It is generally believed that an electric-field dependent geminate recombination process determines f. For an oxide field of 3.1×10^5 V/cm, corresponding to $V_G = 0$ and $V_{sub} = -1$ V during the radiation pulse, f is approximately 0.75 (G.A. Ausman, private communication). For a dose of 93 krads, N_+ is 6.5×10^{17} cm^{-3}. Substituting this into equation (5) yields a value of ΔQ_{ox} of 1.05×10^{-8} C/cm^2, which in turn gives ΔV_t −0.65 V from equation (3). This value assumes that none of the holes have moved out of the oxide. However, holes *are* mobile in SiO_2 at room temperature: the reduction in ΔV_t to −0.18 V at 100 μs after the ionizing pulse may be due to motion out of the oxide of the low-mobility holes in the intervening time prior to the measurement. The further annealing of ΔV_t to −0.13 V at 1000 s after the pulse may be attributed to a combination of further hole motion, and tunneling into trapped holes in the oxide and electron injection into interface states from the Si. Threshold shifts on the order of −1V at 100 μs after the pulse were observed when n-channel transistors with oxides 1200 Å thick were subjected to similar radiation conditions at the LINAC, i.e., the same total dose and field across the oxide during the pulse.[16] Based on equations (3), (5), and (7), the calculated value is 20 V. The observed value, much less than this, could be due to hole motion in times less than 100 μs. It could be due also to the reduced value of f in equation (7), which would occur if the field across the oxide were neutralized by the high density of electron-hole pairs generated during the pulse. If the field is reduced in the oxide, some of the electron-hole pairs recombine before the electrons are swept out of the oxide. This recombination effectively decreases N_+ and therefore ΔV_t through a decrease in f. Owing to the complexity of the annealing process at these high dose rates (~10^{11} rads(Si)/s), it is therefore difficult to compare quantitatively the dependence of the annealing on oxide thickness at times immediately (100 μs) after the ionizing pulse. A few qualitative remarks, however, may be made concerning the annealing rate in the 200-Å oxide from 100 μs to 1000 s after the pulse.

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[14] *H. E. Boesch, Jr., F. B. McLean, J. M. McGarrity, and G. A. Ausman, Jr., IEEE Trans. Nucl. Sci., NS-22 (December 1975), 2163.*

[15] *G. A. Ausman and F. B. McLean, Appl. Phys. Lett., 26 (1975), 173.*

[16] *M. Simons, Research Triangle Institute Report No. 43U-812 (January 1974).*

Various models have been proposed to explain the annealing of ΔV_t with time after an ionizing pulse. Thermal activation of the trapped holes into the valence band and the subsequent sweep out from the oxide without retrapping have been suggested.[17] This model predicts a logarithmic dependence of ΔV_t on time. While the data in figure 8 for the 200-Å oxide satisfies such a dependence, application of the model suggests that hole traps in SiO_2 lie less than 0.4 eV from the valence band. There is evidence from optical data, however, that these traps are much deeper into the SiO_2 energy gap. To circumvent this discrepancy, a model involving hole transport out of the oxide via phonon-assisted tunneling between localized states was successfully fit to voltage annealing data of n-type MOS capacitors.[14] An activation energy of 0.30 eV was determined. This process may play a role in detemining the annealing rate of a thin-oxide device. Interface-state charging has also been found to be effective in the ΔV_t annealing of n-channel devices beginning at times on the order of 1 s after the pulsed exposure.[16] In such cases, a linear dependence of ΔV_t on ln(t) is predicted assuming Schottky emission of electrons from the Si into the SiO_2.[18]

8. CONCLUSION

In the preceding discussion, it was shown that the performance of MOS transistors following ionizing radiation could be greatly improved by reducing the thickness of the gate oxide. The n-channel MOSFET's with oxides 200 Å thick continued to operate in the enhancement mode after irradiation to 10^6 rads(Si) with a positive bias applied to the gate. This operation would allow the MOSFET's to be used in CMOS application* that heretofore have been restricted to radiation environments on the order of 10^5 rads(Si) for conventional thick-oxide devices. Likewise, performance of thin-oxide devices following a transient ionizing pulse was improved over that of conventional devices.

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[14] *H. E. Boesch, Jr., F. B. McLean, J. M. McGarrity, and G. A. Ausman, Jr., IEEE Trans. Nucl. Sci., NS-22 (December 1975), 2163.*

[16] *M. Simons, Research Triangle Institute Report No. 43U-812 (January 1974).*

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**[It has since been shown that CMOS transistors with 400-Å oxides continue to operate after irradiation of 2×10^6 rads(Si).] J. G. Fossum, G. F. Derbenwick, and B. L. Gregory, IEEE Trans. Nucl. Sci., NS-22, (December 1975).*

This technique of reducing the oxide thickness, when applied with established procedures for fabricating clean oxides,[2,19] may provide a necessary step for producing radiation-hardened MOS devices. Questions such as stability, reliability, and yield must be answered before thin-oxide devices can be considered for system applications. Work is being actively carried out in these areas. In this regard, several recent developments further demonstrate that MOS technology is heading in the direction of thinner oxides. A particularly impressive example is the design and performance described by IBM of an 8192-bit FET memory chip.[20] The cell is made up of polysilicon gate n-channel transistors. The thickness of the gate oxide is *350* Å. Use of polysilicon gates on MOS structures has been shown to give superior dielectric reliability.[21] The times to failure are 8 to 16 decades longer at room temperature for the polysilicon gate devices than for aluminum gate devices and are nearly independent of oxide thickness (200 to 1500 Å).

In conclusion, use of thinner oxides for radiation hardening MOS devices appears to be a promising and viable technique within reach of current technological goals.

ACKNOWLEDGEMENT

The authors thank C. M. Osburn and R. H. Dennard of the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, for kindly supplying the MOSFET's used in this experiment.

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