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# STORAGE RELIABILITY OF MISSILE MATERIEL PROGRAM

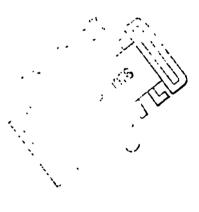
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RAYTHEON COMPANY EQUIPMENT DIVISION

LIFE CYCLE ANALYSIS DEPARTMENT HUNTSVILLE, ALABAMA STORAGE RELIABILITY

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#### MISSILE MATERIEL PROGRAM

STORAGE RELIABILITY ANALYSIS SUMMARY REPORT VOLUME I ELECTRICAL & ELECTRONIC DEVICES

LC--76-2

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May 1976

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Prepared by: Dennis F. Malik Approved by: Donald R. Earles

## FOR

HEADQUARTERS U. S. ARMY MISSILE COMMAND REDSTONE ARSENAL, ALABAMA



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IN COMPLIANCE WITH CONTRACT NO. DAAHO1-74-C-0853 DATED 4 JUNE 1974 DATA ITEM SEQUENCE NO. 3

> RAYTHEON COMPANY EQUIPMENT DIVISION

LIFE CYCLE ANALYSIS DEPARTMENT HUNTSVILLE, ALABAMA

#### ABSTRACT

This report summarizes analyses on the non-operating reliability of missile materiel. Long term non-operating data has been analyzed together with accelerated storage life test data. Reliability prediction models have been developed for various classes of devices.

This report is a result of a program whose objective is the development of non-operating (storage) reliability prediction and assurance techniques for missile materiel. The analysis results will be used by U. S. Army personnel and contractors in evaluating current missile programs and in the design of future missile systems.

The storage reliability research program consists of a country wide data survey and collection effort, accelerated testing, special test programs and development of a nonoperating reliability data bank at the U.S. Army Missile Command, Redstone Arsenal, Alabama. The Army plans a continuing effort to maintain the data bank and analysis reports.

For more information, contact:

Commander

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#### 1.0 INTRODUCTION

#### 1.1 Missile Reliability Considerations

Materiel in the Army inventory must withstand long periods of storage and "launch ready" non-activated or dormant time as well as perform operationally in severe launch and flight environments. In addition to the stress of temperature soaks and aging, they must often endure the abuse of frequent transportation and handling and the climatic extremes of the forward area battlefield environment. Missiles spend the majority of the time in this nonoperating environment. In newer missile systems, complexity is increasing significantly, longer service lives are being required, and periodic maintenance and checkouts are being reduced. The combination of these factors places great importance on selecting missile materiels which are capable of performing reliably in each of the environments.

The inclusion of storage reliability requirements in the initial system specifications has also placed an importance on maintaining non-operating reliability prediction data for evaluating the design and mechanization of new systems. 1.2 Storage Heliability Research Program

An extensive effort is being conducted by the U. S. Army Missile Command to provide detailed analyses of missile materiel and to generate reliability prediction data. A missile material reliability parts count prediction handbook, LC-76-1, has been developed and provides the current prediction data resulting from this effort.

This report provides a summary of the analyses performed under the storage reliability research program and background information for the predictions in LC-76-1. Included are summaries of real time and test data, failure modes and mechanisms, and conclusions and recommendations resulting from analysis of the data. These recommendations include special design, packaging and product assurance data and information on specific part type and part construction.

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For a number of the part types, detailed analysis reports are also available. These reports present details on part construction, failure modes and mechanisms, parameter drift and aging trends, applications, and other considerations for the selection of materiel and reliability prediction of missile systems.

The U. S. Army Missile Command also maintains a Storage Reliability Data Bank. This data bank consists of a computerized data base with generic part storage reliability data and a storage reliability report library containing available research and test reports of non-operating reliability research efforts.

For the operational data contained in this report, the user should refer to the following sources: MIL-HDBK-2173, Military Standardization Handbook, Reliability Prediction of Electronic Equipment; Reliability Analysis Center (RAC) Microcircuit Generic Failure Rates; RADC-TR-69-458, Revision to the Nonelectronic Reliability Handbook; and the Government-Industry Data Exchange Program (GIDEP) Summaries of Failure Rate Data.

## 1.3 Missile Environments

A missile system may be subjected to various modes of transportation and handling, temperature soaks, climatic extremes, and activated test time and "launch ready" time in addition to a controlled storage environment. Some studies have been performed on missile systems to measure these environments. A summary of several studies is presented in Report BR-7811, "The Environmental Conditions Experienced by Rockets and Missiles in Storage, Transit and Operations" prepared by the Raytheon Company, dated December 1973.

In this report, skin temperatures of missiles in containers were recorded in dump (or open) storage at a maximum of 165°F (74°C) and a minimum of -44°F (-42°C). In nonearth covered bunkers temperatures have been measured at a maximum of 116°F (47°C) to a minimum of -31°F (-35°C). In earth covered bunkers, temperatures have been measured at a maximum of 103°F (39°C) to a minimum of 23°F. (-5°C).

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Acceleration extremes during transportation have been measured for track, rail, aircraft and ship transportation. Up to 7 G's at 300 hertz have been measured on trucks; 1 G at 300 hertz by rail; 7 G's at 1100 hertz on aircraft; and 1 G at 70 hertz on shipboard. のないないないないないないないないないないないできたが、

Maximum shock stresses for truck transportation have been measured at 10 G's and by rail at 300 G's.

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Although field data does not record these levels, where available, the type and approximate character of storage and transportation are identified and used to classify the devices.

#### 1.4 System Level Analysis

. The primary effort in the Storage Reliability Research Program is on analysis of the non-operating characteristics of parts. In the data collection effort, however, some data has been made available on system characteristics.

This data indicates that a reliability prediction for the system based on part level data will not accurately project maintenance actions if the missile is checked and maintained periodically. Factors contributing to this disparity include test equipment reliability, design problems, and general handling problems. In many cases, these problems are assigned to the system and not reflected in the part level analysis.

In general, a factor of 2 should be multiplied by the device failure rate to obtain the maintenance rate. Three system examples are described below:

## 1.4.1 System A

For system A, a check of 874 missiles in the field indicates 142 failed missiles. These failed missiles were taken to a maintenance facility. At the maintenance facility, no fault could be found in 51 of the missiles. Two missiles faults were corrected by adjustments. This left 89 failures which could be attributed to part failure. The parts were failure analyzed and the analysis indicated 19 failures to be a result of electrical overstress. These failures were designated design problems.

Therefore only 70 (49%) of the original 142 failures were designated as non-operating part failures.

#### 1.4.2 System B

For system B, 26 missile failures were analyzed. Of these no fault was found in 2 missiles; adjustments were required for 2; external electrical overstress or handling damage was found in 10; a circuit design problem was assigned to 1, and component failures were assigned to 11. ( 1

#### 1.4.3 Gyro Assemblies

An analysis of gyro assembly returns indicated that two thirds of the returns were attributed to design defects,

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mishandling, conditions outside design requirements, and to erroneous attribution of system problems.

Therefore, only 33 percent of the returns were designated as non-operating part failures.

## 1.5 Limitations of Reliability Prediction

Practical limitations are placed in any reliability analysis effort in gathering and analyzing data. Field data is generated at various levels of detail and reported in varying manners. Often data on environments, applications, part classes and part construction are not available. Even more often, failure analyses are non-existant. Data on low use devices and new technology devices is also difficult to obtain. Finally in the storage environment, the very low occurrence of failures in many devices requires extensive storage time to generate any meaningful statistics. a. o. . its restained at the standard standard at the standard standard at the sign of the standard standard

Thes. difficulties lead to prediction of conservative or pessimistic failure rates. The user may review the existing data in the backup analyses reports in any case where design or program decision is necessary.

#### 1.6 Life Cycle Reliability Prediction Modeling

Developing missile reliability predictions requires several tasks. The first tasks include defining the system, its mission, environments and life cycle operation or deployment scenario.

The system and mission definitions provide the basis for constructing reliability success models. The modeling can incorporate reliability block diagrams, truth tables and logic diagrams. Descriptions of these methods are not included here but can be studied in detail in MIL-HDBK-217B or other texts listed in the bibliography.

After the reliability success modeling is completed, reliability life cycle prediction modeling for each block or unit in the success model is performed based on the definitions of the system environment and deployment scenario. This reliability life cycle modeling is based on a "wooden

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round" concept in order to assess the missile's capability of performing in a no-maintenance environment. The general equation for this modeling is:

 $R_{LC} = R_{T/H} \times R_{STOR} \times R_{TEST} \times R_{LR/D} \times R_{LR/O} \times R_{r} \times R_{r}$ 

where:

R<sub>LC</sub> is the unit's life cycle reliability

R<sub>T/H</sub> is the unit's reliability during handling and transportation

R<sub>STOR</sub> is the reliability during storage

R<sub>TEST</sub> is the unit's reliability during check out and test

- R<sub>LR/D</sub> is the unit's reliability during dorrant launch ready time
- R<sub>LR/O</sub> is the unit's reliability during operational (>10% electronic stress) launch ready time
- R<sub>L</sub> is the unit's reliability during powered launch .and flight
- R<sub>p</sub> is the unit's reliability during unpowered flight

The extent of the data to date does not provide a capability of separately estimating the reliability of transportation and storage for missile materiel. Also data has indicated no difference between dormant (>0 and <10% electrical stress) and non-operating time. Therefore, the general equation can be simplified as follows:

 $R_{LC}(t) = R_{NO}(t_{NO}) \times R_{O}(t_{O}) \times R_{L}(t_{L}) \times R_{F}(T_{F})$ 

where:

R<sub>NO</sub> is the unit's reliability during transportation and handling, storage and dormant time (nonoperating time)

- $t_{NO}$  is the sum of all non-operating and cormant time
- R<sub>0</sub> is the unit's reliability during checkout, test or system exercise during which components have electrical power applied (operating).

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- to is the sum of all operating time excluding launch and flight
- R<sub>L</sub> is the unit's reliability during powered launch. and flight (Propulsion System Active)
- tr. is the powered launch and flight time
- R<sub>F</sub> is the unit's reliability during unpowered flight
- t<sub>r</sub> is the unpowered flight time
- t is the sum of  $t_{NO}$ ,  $t_O$ ,  $t_L$  and  $t_F$

The values  $R_{NO}$ ,  $R_O$ ,  $R_F$  are calculated using several methods. The primary method is to assume exponential distributions as follows:

$$R_{NO}(t_{NO}) = e^{-\lambda}NO^{t}NO$$

$$R_{O}(t_{O}) = e^{-\lambda}O^{t}O$$

$$R_{L}(t_{L}) = e^{-\lambda}L^{t}L$$

$$R_{F}(t_{F}) = e^{-\lambda}F^{t}\Sigma$$

The failure rates  $\lambda_{NO}$ ,  $\lambda_O$ ,  $\lambda_L$  and  $\lambda_F$  are calculated from the models in the following sections.  $\lambda_{NO}$  is calculated from the non-operating failure rate models. The remaining failure rates are calculated from the operational failure rate models using the appropriate environmental adjustment factors. Each prediction model is based on part stress factors which may include part quality, complexity, construction, derating, and other characteristics of the device.

Other methods for calculating the reliability include wearout or aging reliability models and cyclic or one shot reliability models. For each of these cases, the device section will specify the method for calculating the reliability.

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## 1.7 Reliability Predictions During Early Design

Frequently during early design phases, reliability predictions are required with an insufficient system definition to utilize the stress level failure rate models. Therefore, a "parts count" prediction technique has been prepared. It provides average base failure rates for various part types and provides K factors for various phases of the system deployment scenario to generate a first estimate of system reliability. This prediction is presented in Report LC-76-1. 1.8 Summary of Report Contents

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The report is divided into five volumes which break out major component or part classifications: Volume 4, Electrical and Electronic Devices; Volume II, Electromechanical Devices; Volume III, Hydraulic and Pneumatic Devices; Volume IV, Ordnance Devices; and Volume V, Optical and Electro Optical Devices. Table 1-1 provides a listing of the major part types included in each volume.

#### TABLE 1-1. REPORT CONTENTS

#### Volume I Electrical and Electronic Devices

#### Section

2.0 Microelectronic Devices

- 3.0 Discrete Semiconductor Devices.
- 4.0 Electronic Vacuum Tubes
- 5.0 Resistors
- 6.0 Capacitors
- 7.0 Inductive Devices
- 8.0 Crystals
- 9.0 Batteries
- 10.0 Connectors and Connections
- 11.0 Printed Wiring Boards

## Volume II Electromechanical Davices

#### Section

- 2.0 Gyros
- 3.0 Accelerometers
- 4.0 Switches
- 5.0 Relays
- 6.0 Transducers
- 7.0 Hi Speed Motors
- 8.0 Synchros and Resolvers

#### Volume III Hydraulic and Pneumatic Devices

#### Section

- 2.0 Valves
- 3.0 Accumulators
- 4.0 Actuators
- 5.0 Pumps
- 6.0 Cylinders
- 7.0 Compressors
- 8.0 'Filters
- 9.0 Gaskets and Seals
- 10.0 Bearings
- 11.9 Regulators

#### Volume IV Ordnance Devices

#### Section

- 2.0 Solid Propellant Motors
- 3.0 Igniters and Safe and Arm Devices
- 4.0 Solid Propellant Gas Generators
- 5.0 Misc. Ordnance Devices

Volume V Optical and Electro Optical Device;

#### 2.0 Microelectronic Devices and Interconnections

Microelectronic devices have and continue to undergo a rapid development in design, materials, processes, screening and qualification procedures. Data applicable to one device may be significantly different from another device performing a similar function. This is a result of materials, processes, etc., and is particularly significant in the hybrid area. Based on the failure mechanism analysis, a detailed categorization of these devices will be necessary to assess assurance procedures to improve the storage reliability.

#### 2.1 Monolithic Microelectronic Storage Reliability Analysis

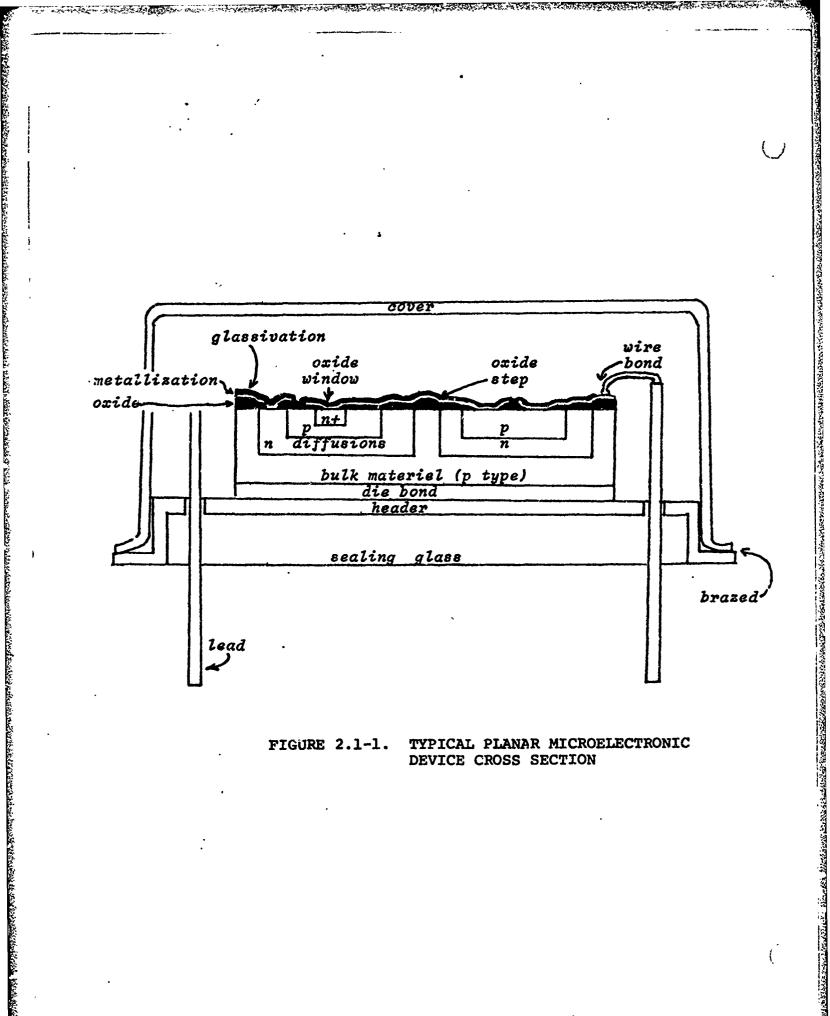
Monolithic refers to a one chip device. They can be of the bipolar or MOS (metal oxide semiconductor) variety. The term bipolar refers to the two polarities of carriers that exist in the device. Both holes and electrons are essential for operation. MOS devices are "unipolar" since only one type of a carrier is used. For P channel MOS, the carriers are "holes" while electrons are the carriers for n-channel MOS. 日本の日本の日本日本の「「「「「「「「「」」」」のためので、「」」」」

Another distinction arises from the differing location of active regions. Bipolar devices are "bulk" devices. The active region is the base, several microns beneath the surface between the emmitter and the collector. MOS devices are "surface effect" devices. Their active region consists of a channel that is induced at the silicon/silicon-dioxide interface.

Because of the difference in construction and operation between bigolar and MOS devices, they are treated separately in this analysis.

Microelectronic device reliability depends primarily upon construction; process control, screening, qualification; and use characteristics. A review of the literature was performed to identify these characteristics which are listed in Table 2.1-1.

For convenience, device construction was broken into seven major areas: Bulk materiel and diffusion, oxide; metallization; glassivation; die bonding; chip connections; and packaging characteristics. Each of these areas identified in Figure 2.1-1 were



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analyzed for failure mechanisms which would be applicable in a missile's use environment from acceptance into the inventory to firing.

TABLE 2.1-1. DEVICE CLASSIFICATION

Spanil Statistics

CONSTRUCTION

Die Properties Oxide Metallization Glassivation Die Bond Chip Connection Package

Parts Storestation

DEVICE LEVEL PRODUCT ASSURANCE

MIL-STD-883 Quality Level Screens Quality Conformance Inspection Process Controls

#### ASSEMBLY AND SYSTEM LEVEL PRODUCT ASSURANCE TESTS

COMPLEXITY

LOGIC TYPE

USE ENVIRONMENT

Transportation and Handling Temperature Humidity Storage Container & Location Field Test Duration & Frequency Derating

2.1.1 Failure Mechanisms

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The mechanisms of failures affecting semiconductors are generally the same regardless of the device type, however, the rate of occurrence varies between types. For this reason, the failure mechanism discussion applies to all of the monolithic device discussed in the succeeding sections.

The failure mechanisms contributing to microelectronic device failures appear to be identical whether the device is operational or in storage. The difference in the two environments is the frequency in which individual failure mechanisms occur. In general the mechanisms can be grouped into three categories: 1) Mechanisms for which failure occurrence is independent of the application environment.

2) Mechanisms for which failure occurrence is dependent on the application environment, and

3) Mechanisms for which the failure occurrence is timerelated and environment dependent.

The mechanishs in group 1 are simply undetected defects which passed through the screens such as improper diffusions, oxide pinholes, etc. The rate of occurrence of these mechanisms would be the same, whether the device was applied in an operational or a storage environment. The only difference would be the time at which the mechanism was detected.

The mechanisms in group 2 are defects which do not fail the device immediately. For example, bond and metallization defects which progress to failure due to temperature or mechanical stress.

The third group of mechanisms are similar to group 2, except they are more time dependent. Examples are metal migration, intermetallic compound formations, corrosion, etc.

The mechanisms in groups 2 and 3 are dependent on environment and occur at different rates depending on whether the device is operational or dormant. In most cases, the storage environment is more benign than the operating environment.

In considering both operational and storage failure rates, the complexity of the device is important. The greater number of circuits on a given substrate area increases the temperature at which the devices are subjected and also requires greater process control in the production. The diffusions, metallization patterns and interconnections are very critical in a high density device. In the operational environment, the rate of occurrence of particular failure mechanisms has differed between Bipolar Digital devices and Bipolar Linear and MOS devices. The major problem areas in digital devices have been contamination and oxide, wire bond and packaging defects. For Linear and MOS devices, contamination and metallization, die mount and oxide defects have been the the major problem areas. Linear and MOS device failure rates are higher than digital devices because of the circuit sensitivity to surface, metallization and oxide defects.

Conversely, in the storage environment, analysis has indicated that the rate of occurrence of particular failure mechanisms is roughly the same between bipolar digital and linear devices. Insufficient data is available to make a storage assessment of MOS devices.

Table 2.1-2 lists each failure mechanism with its acceleration environment. These acceleration environments are the surrounding conditions which can speed the defect or degradation to the point of failure. 

## 2.1.1.1 Bulk Materiel and Diffusion Characteristics

The primary reliability considerations in an operational environment associated with bulk phenomena are those which govern temperature of the device during operation. Devices are generally rated in terms of maximum allowable power dissipation. This power coupled with various thermal resistances and ambient temperature, determines the junction temperature of the device. Steps must be taken to maintain a controlled and uniform temperature since device degradation and failure modes, in most cases, are accelerated by increased temperature.

For most devices, the power requirements are not excessive and junction temperatures are controlled by using suitable heatsink packages. For high-power devices, wafer design may include junction-temperature control considerations to prevent localized high currents and resultant "hot spot" formation.

Bulk defects account for only a minor portion of the operational and storage failures. Primary areas of concern include dislocations (crystal lattice anomalies); impurity diffusions and precipitations; resistivity gradients; and cracks in the bulk materiel. These defects usually result during crystal preparation and are accelerated by mechanical, nuclear and thermal stresses.

The failure modes resulting from bulk defects include deviations in voltage breakdown and other electrical characteristics; secondary breakdown or uncontrolled p-n-p-n switching; or opens or shorts in the subsequent metallization.

Diffusion def.cts account for approximately 5 to 15% of operational and storage failures. Other than those diffusion problems associated with bulk materiel defects, the primary area of concern is the diffusion process itself. These include mask alignment; contamination; mask defects; cracks in the oxide layer; and improper doping profiles. Diffusions that are due to misalignment of masks reduce the base and emitter or base and collector junction spacings. Other faults include discontinuous isolation diffusions and odd shapes or edges of diffusions. Diffusion defects are primarily accelerated to failure by thermal cycling and high temperature. Principle failure modes resulting from diffusion defects include deviations in device characteristics and shorts between the emitter and base.

#### 2.1.1.2 Oxide Considerations

Junction passivation of silicon devices is generally accomplished by using thermally grown silicon dioxide  $(SiO_2)$ . Other devices use phosphorous pentoxide  $(P_2O_5)$  over the  $SiO_2$  layer. Beam Lead Sealed Junction (BLSJ) devices utilize a layer of silicon nitride  $(Si_3N_4)$  glass deposited over the grown  $SiO_2$ . Both  $P_2O_5$ and  $Si_3N_4$  overcoatings have been found to improve the surface stability of bipolar devices. These materials act as gettering agents for sodium ions, thus making the contamination far less mobile. The stability of the structural and electrical properties of the oxide play an important: role in determining the electrical characteristics and reliability of the passivated device.

Oxide defects are significant contributors to device failures. Approximately 5 to 50% of operational failures are attributed to these defects. Current data on non-operating failures indicates that approximately 5 to 35% of storage failures are attributable to oxide defects. Primary areas of concern are pinholes, cracks, thin oxide areas, and oxide contamination. Pinholes can be caused by faulty oxide growth, a damaged mask, poor photo resist or an undercut by the etching process. They vary in depth and in the worst case, expose the silicon to the metallized interconnections. Where the pinhole or metallization does not extend completely to the surface of the silicon, a time-dependent migration or low voltage breakdown mechanism may occur. Where the oxide is overcoated with a second layer, the frequency of pinhole defects decreases.

Oxide cracks occur as a result of the mismatch in the thermal expansion rate of silicon and silicon dioxide. Diffusion of metal to the silicon is then possible. Thin oxide and other oxide difficiencies cause electrical breakdown in the surface passivation from the metal conductor to component areas in the silicon. All of these defects lead to increased current leakages or shorts from the metallization to diffusion areas or substrate.

Ionic impurities in the oxide may cause inversion layers, channeling, and other related phenomena creating lower threshold voltage. Ionic contamination is generally a significant contributor to total oxide charge. The ions are usually mobile and, by drifting under the influence of an electric field, can cause appreciable device parameter instability. Silicon nitride has been shown to be an effective barrier to sodium migration. In Beam Lead Sealed Junction (BLSJ) devices, the silicon nitride seals the devices from sodium and since the platinum silicide and titanium metals also offer very low mobility to the alkaline ions, the BLSJ is inert to sodium.

Inversion and channeling phenomenon occurs only with an electric field present. Bipolar linear and MOS devices are affected by this phenomenon greater than bipolar digital devices.

#### 2.1.1.3 Metallization Considerations

A rather large number of metallization systems have been used on monclithic devices. The primary metals used have been aluminum, molybdenum-gold, and titanium-platinum-gold. Failures related to metallization defects range from 7 to 26% in operational devices and current storage data indicates approximately 15% of the failures related to metallization.

Aluminum metallization defects result from manufacturing deficiencies and also from mechanisms inherent to the metal system.

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Processing deficiencies which subsequently result in device failures include thin metal layers, poor metal-to-oxide adhesion due to oil or other impurities on the wafer, undercutting of Al during etching of the metallization pattern, bridging of Al between conductors due to unremoved photoresist, smears and scratches in conductor stripes, misalignment of masks, insufficient deposition at oxide steps, oxide steps too steep, incomplete removal of oxide, etc.

These defects are accelerated to failure primarily by thermal stresses and result in open and shorted conductors.

Mechanisms inherent to the aluminum metal system include electromigration formation, aluminum silicon eutectic, and intermetallic compound formations with gold.

Many of the failure mechanisms observed in molybdenum-gold metallization systems can be attributed to processing problems. These include failures due to unsatisfactory adhesion of molybdenum to the silicon dioxide and of the gold layer to the molybdenum layer. These can be attributed to contamination of the surface and oxidation of the molybdenum layer prior to deposition of the gold. Other processing problems include: molybdenum undercutting during etching; scratches which expose the molybdenum to oxidation and subsequent opens, and corrosion of molybdenum from impurities introduced in the processing.

Gold-silicon eutectics can occur if pinholes exist in the molybdenum layer.

Failure mechanism data on Platinum Silicide-Titanium-Platinum-Gold metallization systems is just becoming available. Improved or eliminated failure modes include wire bond defects, alkali ion contamination, metallization corrosion, and aluminum migration. Possible failure mechanisms identified for these devices are all due to processing deficiencies. They include pinholes in the silicon nitride; thin silicon nitride; shorted metallization; platinum migration into the silicon; gold or titanium migration resulting from thin platinum; and contamination.

#### 2.1.1.4 Glassivation Considerations

Both silicon nitride and phosphosilicate glass overcoatings have been found to greatly enhance the reliability of bipolar digital devices. These glassivation materiels act as gettering agents for sodium ions and when deposited over the total surface, including the metallization, the materiel provides an excellent protection against metallization scratches and loose particle shorts.

Inversion and increased metal migration are two failure mechanisms that have been reported caused by glassivation. These new mechanisms are not fully understood but some causes have been postulated.

The induced inversion formation may result from some defects or contamination in the oxide layer which allow high fields to accumulate electronic charge over the underlying silicon. A poor interface between the oxide and glass then allows lateral charge movement along the interface. The lateral charge movement can induce inversion extensive enough to form a conducting channel which can cause device instability. The increased metal migration is not as well understood but appears to be caused by the high pressure on the metal between the thermal and deposited glasses. Generally, the metal migration is associated with damage to the glass. Both aluminum and gold migration have occurred through the damaged glass to the adjacent conductor causing device failure.

A third possible failure mechanism has been discussed where condensation from any moisture in a package tends to concentrate on a crack in the glassivation, normally on the metal strips. This tends to increase the susceptibility for metal corrosion along the crack.

## 2.1.1.5 Die Bond Considerations

Die bonds provide mechanical support; in most cases, electrical contact; and also provide the principle path by which heat flows out of the silicon chip. Three techniques are in general use for attaching semiconductor devices to the package substrate: alloy mount, frit mount and epoxy mount.

Low strength chip-to-header bonds have been reported to result in approximately 2-7% of device failures, in both operational and storage environments.

The failure mechanisms include diffusion of the gold into the silicon producing void formations; brittle frit mounts resulting from impurities in the glass or improper firing cycles used for devitrification; mechanical stresses in epoxies where the temperature goes through the glass-transition temperature of the epoxy, and outgassing of organic materiel and separation of metal particles due to incomplete curing of the epoxy.

#### 2.1.1.6 Chip Connection Considerations

Device connections are created by connecting wire leads to the device package; or through the use of beam lead or aluminum bump techniques. Wire bonding is accomplished primarily by thermocompression or by ultrasonic bonding techniques. Wire bond defects are reported to account for 15 to 45% of all device failures in an operational environment. Storage or non-operating data currently indicates from 19 to 76% of all device failures are bond related.

The principle failure mechanisms are process deficiencies including underbonding, overbonding, misaligned bonds, contaminated bonding pads or wire, and wire nicks, cuts or abrasions.

Thermocompression bonding of aluminum wires has a history of cracks at the heel of the bond, which later failed under power cycling.

The gold wire bonding to aluminum metallization has been a major concern in microelectronic devices. Intermetallic compound formations between these two metals combined with the formation of voids in the aluminum from the Kirkendall effect create high resistance or weakened and brittle bonds. Formation of the compounds and voids is accelerated by thermal stresses. Design and processing criteria have been developed to minimize the occurrence of these formations. They include controlling the purity of the gold and providing thinner, metallization at the bonding pad.

The aluminum wire bond to the gold header post has not been a significant contributor to device failures and is attributed to two factors: 1) the ratio of aluminum to gold is small, and 2) the bonds are not exposed to the same temperature as the gold wire to aluminum bonds on the chip during operation.

Failure mechanism data on beam lead sealed junction device bonding is limited. Processing deficiencies would be expected to be the primary problem, however, these are significantly reduced since the chip connection is made in the beam forming process which leaves only bonding of the beams to the header. All of the bonds of a single device are made simultaneously.

#### 2.1.1.7 Package Considerations

Bipolar digital devices are packaged in a variety of materials and configurations. These materiels include: metal, ceramic, glass, metal ceramic, epoxy, phenolic and other plastics. Package configurations include cans, flatpacks, inline and dual inline.

Device failures attributed to package defects have been reported from 8 to 28% of operational failures. In many cases of failure reports, the resulting contamination and corrosion is reported and not the seal defect. Special test programs on devices have shown hermiticity problems to be substantial.

Failure mechanisms besides the seal leaks are fractured packages due to improper handling, loose solder balls formed in sealing the package which later short conductors, current leakage between leads from formation of lead from lead oxide in the glass, broken or burnt external leads and improper marking. All of these are process defects.

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FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
BULK DEFECTS				
Dislocation and Stacking Faults	Lattice strain due to steep concentration gradients finally released as dislocations.	Mechanical Stress Hi Temp	Degradation of junction character- istics.	Electrícal Test
Impurity Diffusions and Precipatations	Diffusions along dis- locations during epitaxial growth,	Hi Temp Power Burn-in Thermal Cycling	Low reverse breakdown voltage.	Electrical Test
Resistivity Gradiants	Large local stresses.	Mechanical Shock Vibration Nue_fon Bombardment	Change in component values.	<b>Blectrical</b> Test
Cracks in Bulk Materiel	Thermal shock during processing.	Mfchanical Shock Thermal Cycling Hi Temp	Opens or Shorts in metal. Junction degradation.	Frecap · Visual Electrical Test

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FALLURS MECFINIENCAUSECAUSEACCELERANTINGFALLUREDETER MODEDIFFUSION DEFECTSDIFFUSION DEFECTSENVIRONMENTMODEDETERDIFFUSION DEFECTS1)Faulty Mask AlignmentHi TempShortsYiauDIFFUSION DEFECTS1)Faulty Mask AlignmentHi TempShortsYiauDIFFUSION DEFECTS1)Faulty Mask AlignmentHi TempComponesPreceap1)Dust or other ContaminantsThermalOpensYiau1)Defects in maskCyclingChanges inElectr1)Defects in masktiselfCyclingCharacteris-1)Defects in maskThermalCharacteris-TeetProfileProcess control problem.ThermalCharacteris-TeetProfileProcess control problem.ThermalCharacteris-TeetProfileProcess control problem.ThermalComponentsTeetProfileProcess control problem.ThermalContenteris-TeetProfileProcess control problem.ThermalContenteris-TeetProfileProcess control problem.ThermalContenteris-TeetProfileProcess control problem.Process BiasContenteris-TeetProfileProfileProfileProfileProfileTeetProfileProfileProfileProfileProfileProfileProfileProfileProfileProfileProfileP					
I DEFECTS I DEFECTS 1) Faulty Mask Alignment 2) Dust or other Contaminants on mask 3) Defects in mask itself 4) Cracks in oxide boping Process control problem. Thermal Cycling Changes in Cycling Changes in Cycling Changes in Cycling Changes in Cycling Changes in Cycling Changes in Cycling Characteris- tics. Emitter to Storage 1) Thermal oxidation of t Iayer 1) Thermal oxidation of t Layer 2) Charged impurities. Reverse Bias Protect Shared inpurities. Reverse Bias Prote Data Contants. 2) Charged impurities. Reverse Bias Protect Contants. 2) Minute mask flaws. 2) Minute mask flaws. Power Burn-in Cycling	FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
1)Faulty Mask AlignmentHi TempShorts2)Dust or other ContaminantsThermalOpens0maskon maskCyclingOpens3)Defects in mask itselfCyclingCharacteris-4)Cracks in oxideCyclingCharacteris-DopingProcess control problem.ThermalCyclingDopingProcess control problem.ThermalUnstableCyclingProcess control problem.ThermalCyclingDopingProcess control problem.ThermalComponentsBCTSRiterStorageComponentsBCTSI.ayer1)Thermal oxidation ofHi Temp.FBCTSStorageBunn-inShortPayer1)Thermal oxidation ofPower Burn-inShort1< Layer	DIFFUSION DEFECTS				
DopingProcess control problem.Thermal CyclingUnstable Components'ECTSHi Temp.StorageComponents'ECTSHi Temp.StorageComponents'ECTSPermal oxidation of Silicon producing n or p type surface.Hi Temp.Emitter to Short'I Tayer1) Thermal oxidation of Silicon producing n or p type surface.Hi Temp.Emitter to Short'I Tayer2) Charged impurities.Reverse Bias Power Burn-in ShortIower Short'I Dust particles or other Contaminants.Hi Temp.Short Charge'I Dust particles or other Contaminants.Hi Temp.Short Cycling'I Dust particles or other Contaminants.Power Burn-in CyclingShort'I Temp.Power Burn-inShort	Improper Diffusions	Faulty M Dust or on mask Defects Cracks i	ні Тћ	Shorts Opens Changes in Device Characteris- tics.	Precap Visual Electrical Test
EFECTSEFECTSHi Temp.on Layer1) Thermal oxidation of Silicon producing n or p type surface.Hi Temp.Silicon producing n or p type surface.Reverse Burn-in Short Reverse Bias2) Charged impurities.Reverse Bias Nort Power Burn-in Short Short Threshold Voltage1) Dust particles or other contaminants.Hi Temp.2) Minute mask flaws.Short Cycling		control	Thermal Cycling Hi Temp. Storage	Unstable Components	'Electrical Test
on Layer 1) Thermal oxidation of Hi Temp. Silicon producing n or Power Burn-in Collector p type surface. 2) Charged impurities. Reverse Bias Lower Faulty Oxide Growth due to: Hi Temp. 1) Dust particles or other Thermal contaminants. 2) Minute mask flaws. 3) Etch undercut. Power Burn-in					
Faulty Oxide Growth due to: Hi Temp. Short 1) Dust particles or other Thermal contaminants. Cycling 2) Minute mask flaws. Power Burn-in		Thermal oxidation of Silicon producing n p type surface. Charged impurities.	Hi Temp. Power Burn-in Reverse Bias	Emitter to Collector Short Lower Threshold Vultage	Electrical Test
	Pinhole	ulty Oxide Dust parti contaminan Minute mas Etch under	Hi Temp. Thermal Cycling Power Burn-in	Short	Electrical Test

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FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
OXIDE DEFECTS -	CONTINUED			
Cracks	Mismatch in Thermal Expansion rate.	Hi. Temp.	Short	Electrical Test
Thin Oxide	Improper Process Control.	Hi. Temp.	Short	Electrical Test
METALLIZATION DEFECTS	scrs			
Surface Flaws	Scratched or smeared metalli- zation during processing.	Thermal Cycling	0p≘n Short	Precap Visual Electrical Test
Insufficient Coverage at Oxide step	<ol> <li>Misalignment of masks.</li> <li>Insufficient deposition at oxide steps.</li> <li>Oxide step too steep.</li> <li>Oversintering of metal to silicon.</li> <li>Incomplete removal of oxide</li> </ol>	Hi. Temp. Thermal Cycling Power Burn-in	Open Hi Resistance Connections	Precap Visual Electrical Test
Under etched Metallization	Improper Etching.	Hi. Temp. Thermal Cycling Power Burn-in	Short	Precap Visual Electrical Test

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FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
METALLIZATION DEFI	DEFECTS - CONTINUED			
Voids under Metallization	<ol> <li>Overetching causing under- cutting of metallization.</li> <li>Xirkendall effect of disimilar alloys.</li> </ol>	Hi. Temp. Thermal Cycling Mechanical Stress	ne Jo	Precap Visual Electrical Test
Non-adhesion of Metallization	<ol> <li>Contamination of surface.</li> <li>Improper alloying temp. or time.</li> </ol>	Hi. Temp. Thermal C/cling	Open	Precap Visual Electrical Test
Metal Migration (Hillccks, Voids, Whiskers, etc.)	Insufficient metal thickness, Scratches, grain size, etc.	Hi. Temp. & Current Density	Open Short Current Leakage	Precap Visual Electrical Test
Increased Resistance of Metallization	Thickness of oxide.	Hi. Temp.	Oit of Tolerance	Electrical Test
GLASSIVATION DEFECTS	· · SI			
Inversion Phenomenum	Poor Interface between oxide låyer & glassivation layer.	Hi. Temp. & Reverse Bias	Out of Tolerance	<b>Blectrical</b> Test

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FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
GLASSIVATION DEFECTS	CTS - CONTINUED			
Metal Migration	Damaged Glass - Pressure Between oxide & glassivation layers.	Hi. Temp. & Current Density	Open Short Current Leakage	Electrical Test
Oxide Cracks Corrosion	Thermal Shock During Processing.	Temp. Cycling	Open .	Precap Visual Electrical Test
DIE BONDING DEFECTS	· SI			
Voids between header & die	Incomplete coverage of bonding materiel.	Hi. Temp. Vibration Shock	Open	Precap Visual Electrical Test
Cracked or lifted die to header bond.	<ol> <li>Weak metal eutectic bond due to oxide on reverse side of silicon.</li> <li>Glass frit facture in flexible package.</li> </ol>	Acceleration Shock Vibration Hi. Temp.	Open	Precap Visual Electrical Test

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7ÅILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
DIE BONDING DEFECTS	rs - Continued			
Cracked Silicon Die	Strains during die attach.	Acceleration Shock Vibration	Open	Precap Visual Electrical Test
WIRE BONDING DEFECTS				
Separation of Bond	<ol> <li>Underbonding.</li> <li>Contamination of Bonding.</li> <li>Cracks in bond due to overbonding.</li> </ol>	Hi. Temp. Shock Vibration	Open	Precap Visual Electrical Test
Bond Shorts	<ol> <li>Overbonding.</li> <li>Insufficient bonding pad area or spacing.</li> <li>Improper bond alignment.</li> </ol>	Hi. Temp. Power Burn-in Vibration Shock Thermal Cycling	Short	Precap Visual Electrical Test
Broken wires ƙ Reduced wire size.	<ol> <li>Overbonding.</li> <li>Nicks, cuts or abrasions in wire during processing.</li> </ol>	Hi. Temp. Shock Vibration	Open	Precap Visual Electrical Test

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DETECTION METHOD Electrical Electrical Leak Tests **Precap** Visual Precap Visual Test Test Intermittent Opens, Shorts or Performance FAILURE MODE Degration. Corresion Causing Shorts Short Open Power Burn-in ACCELERATING ENVIRONMENT Mechanical Vibration Hi. Temp. Cycling Hi. Temp. Fractured Glass or Imcomplete Thermal & Weld, Braze, etc. Thermal Stress Shock Various Time-Dependent Forma-tions of a Chemical Compound Red Plague - Copper Oxide White Plague - Aluminum Hydroxide. Black Plague Au-Si-Al. on Silver Plate over at metal-metal contacts: 1) Purple Plague AuAl2. - Tin Unremoved pigtails. Silver Plague CAUSE Migration. - CONTINUED Coprer. WIRE BONDING DEFECTS 5) ົຕ 4 3 FINAL SEAL DEFECTS MECHANISM Intermetallic Hermetic Wire Shorts. Formation Compound FAILURE Poor ] Seal

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Radiographic lead Fatigue DETECTION Electrical Test Electrical Electrical METHOD Tests Tests Test Visual Visual Performance Opens, Shorts or Corrosion Degration Leakage FAILURE Operative Causing MODE Current Short Open Not ACCELERATING ENVIRONMENT Mechanical Stress Mechanical Temp. Cycling *lechanical* ß Hi. Temp. Hi. Temp. Stress Thermal Stress Reduction of  $P_{b}$ O Glass to  $P_{b}$ Improper Brazing or Handling Low Resistance Leak due to İmproper Handling or Improper Seal Leak Test Process Control Problem CAUSE Slack in leads. - CONTINUED FINAL SEAL DEFECTS or chip periphery Improper Marking Internal Wires Shorted to Con-ductive Lids Current Leakage Between Leads Broken or Bent External Leads MECHANISM Fractured Package FAILURE

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FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION ME JHOD
CONTAMINATION	•			
Surface, Wire or Bond Corrosion	<pre>Corrosive Residue &amp; Moisture such as: 1) Photo Resist 2) Chlorine in wire Lubricant 3) Etch pits in oxide,     trapping sodium or other     corrcsive agents 4) Outgassing from organic materiels. 5) Weld glasses 6) Incorrect atmosphere sealed in package 7) Loss of package hermi- </pre>	Hi. Temp. Storage	Open Ehort Degraded Operation	<b>Electrical</b> Tests
Conductive Particles in Package	<ol> <li>Solder particles</li> <li>Wire particles</li> <li>Flaking metallization</li> <li>Die particles</li> <li>Die bond materiel</li> <li>particles</li> </ol>	Vibration Shock Thermal Cycling	Short	Electrical Tests
Corrosion at Glass Ceramic Interface	Small lead materiel junction at interface exposed to environment after lead plating.	Hi. Temp. Storage	Open	Visual Electrical Tests
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#### 2.1.1.8 Device Level Product Assurance

Kanapan manapatéh kerangkangat Karang Aramatéh dan panapatéh dan panapatéh kerangkan kerangkan kerangkan kerang

The manufacturing controls and procurement methods for military equipment are normally determined by the criticality of the device in the system and the uniqueness of the device. Procurement specifications determine, to a significant degree, the reliability of the device in the field.

For standard devices in high volume production with established reliability, the parts may be procured according to the specifications in MIL-STD-883 and MIL-M-38510 or equivalent manufacturer specifications. The three quality levels defined in the military specifications are:

Class "A" - Devices intended for use where maintenance and replacement are extremely difficult or impossible, and reliability is imperative.

Class "B" - Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is imperative.

Class "C" - Devices intended for use where maintenance and replacement can be readily accomplished and down time is not a critical factor.

A Class "D" level has also been defined in this report to identify the manufacturer's commercial quality  $1e^{-1}$ 

#### 2.1.2 Monolithic Integrated Circuits Non-Operational Prediction Models

The general failure rate model for monolithic integrated circuits is:

$$\lambda_{\rm p} = \Pi_{\rm L} \Pi_{\rm Q} (\Pi_{\rm T} C_1 + \Pi_{\rm E} C_2) \times 10^{-6}$$

where:  $\lambda$ 

 $\lambda_{p} = \text{device non-operating failure rate}$   $\Pi_{L} = \text{learning adjustment factor}$   $\Pi_{Q} = \text{quality adjustment factor}$   $C_{1} = \text{temperature failure rate factor}$   $C_{2} = \text{environment failure rate factor}$   $\Pi_{T} = \text{temperature adjustment factor}$   $\Pi_{E} = \text{environmental adjustment factor}$ 

The values for each of these parameters are given in Figures 2.1-2 and 2.1-3 for Monolithic Bipolar SSI/MSI Digital and Linear Devices. These devices have complexities less than 100 gates (approximately 400 transistors). The model in Figure 2.1-2 applies to devices containing aluminum metallization with aluminum interconnecting wires. The model in Figure 2.1-3 applies to devices containing aluminum metallization with gold interconnecting wires. A description of the parameters is given in the following sections. No distinction is made in logic type or between complexity levels within the SSI/MSI complexity range.

At present insufficient data is available for devices with all gold systems including beam lead systems. Some data has shown that gold beam lead systems have a lower failure rate than the devices modeled. The model in Figure 2.1-2 can be used as a conservative prediction.

Data is insufficient at this time to develop models for Bipolar LSI, MOS and Memory devices.

2.1.2.1 Learning Adjustment Factor, IL

 $II_L$  adjusts the model for production conditions and controls the conditions as defined in the figures for each device type:

2.1.2.2 Quality Adjustment Factor, II

 $\Pi_Q$  accounts for effects of different quality levels as defined in MIL-M-38510 and MIL-STD-883.

2.1.2.3 Temperature Adjustment Factor,  $\pi_{\rm T}$ 

 $II_T$  adjusts the model for temperature acceleration factors. Two models are applicable:

> IITI is applicable to Bipolar Digital and Linear devices with aluminum metallization and aluminum interconnecting wires.

 $\pi_{\rm Tl} = 0.1 e^{\rm X}$ 

where x = -6544 ( $\frac{1}{T + 273} - \frac{1}{298}$ )

 $\Pi_{T,2}$  is applicable to Bipolar Digital and Linear devices with aluminum metallization and gold interconnecting wires.

 $\pi_{T2} = 0.1 e^{X}$ 

where x = -8121 ( $\frac{1}{T+273} - \frac{1}{298}$ )

In  $\Pi_{T1}$  and  $\Pi_{T2}$  above, T is the ambient storage temperature (°C) and e is natural logarithm base, 2.718.

2.1.2.4 Environmental Adjustment Factor, IE

 $I_E$  accounts for the influence of environmental factors other than temperature. Refer to the environment description in the Appendix.

2.1.2.5 Temperature Factor, C1

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 $C_1$  is a constant and is the temperature component of the base failure rate. Values are given in the figures.

2.1.2.6 Mechanical Stress Factor, C2

C<sub>2</sub> is a constant and is the mechanical stress component of the base failure rate. Values are given in the figures. FIGURE 2.1-2

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PREDICTION MODEL (FOR ALUMINUM METALLIZATION/ALUMINUM WIRE SYSTEM) MONOLITHIC BIPOLAR SSI/MSI DEVICE NON-OFERATIONAL FAILURE RATE

$$\lambda_{\rm D} = \pi_{\rm L} \pi_{\rm Q} [\pi_{\rm T} c_{\rm l} + \pi_{\rm E} c_{\rm 2}] \times 10^{-6}$$

IL (Learning Factor)

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10 for 1) a new device in initial production 2) a major change in design or

- process
- 3) extended line interruption or change in line personnel otherwise

-1

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L

 ${}^{
m I\!I}_{
m T}$  (Temperature Factor)

Temperature °C	Т
25	•
30	4
40	0.29
50	ŝ
0	3
125	0.2
ຄ	8.
2	2.3

C<sub>1</sub> (Temperature Base Failure Rate)

0.0013

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 $c_2 = 0.0007$ 

C2 (Mechanical Stress Base Failure Rate)

 $\pi_{\mathbf{E}}$  (Application Environment Factor)

.25

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A B C D

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MIL-STD-883

Class

ng (Quality Factor)

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001444

Airborne, Inhabited

Space Flight Ground, Fixed

Ground, Benign

Environment

Naval, Sheltered Ground, Mobile

5.0

Airborne, Uninhabited

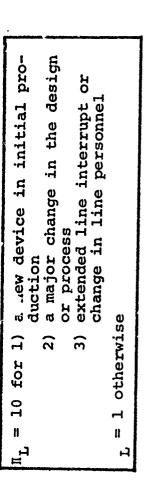
Naval, Unsheltered

# FIGURE 2.1-3

PREDICTION MODEL (FOR ALUMINUM METALLIZATION/GOLD WIRE SYSTEM) MONOLITHIC BIPOLAR SSI/MSI DEVICE NON-OPERATIONAL FAILURE RATE

$$\lambda_{\mathbf{p}} = \pi_{\mathbf{L}} \pi_{\mathbf{Q}} [\pi_{\mathbf{T}} \mathbf{c}_{\mathbf{1}} + \pi_{\mathbf{E}} \mathbf{c}_{\mathbf{2}}] \times 10^{-6}$$

IL (Learning Factor)



IIT (Temperature Factor)

ПТ	0.1 0.16 0.39 0.90 30.25 95.99 442.37 1091.57
°C	
Temperature	25 30 40 100 125 170

C<sub>1</sub> (Temperature Base Failure Rate)

 $c_1 = 9.00054$ 

T - Ambient Temperature °C

NQ Quality Factor)

δ <sub>II</sub>	1 3.5 4.5 135
L-STD-833 Class	<b>4</b> .83 U U
MIL-S Cla	*: A O O

 $II_E$  Application Environment Factor)

Environment	шE
Ground, Benign	0.2
Space Flight Ground Wined	0.2
~ d	
N,	• •
Ground, Mobile	•
Naval, Unsheltered	•
Airborne, Uninhabited	5.0

C2 (Mechanical Stress Base Failure Rate)

=0.0085 ບົ

2.1.3 Non-operational Failure Rate Data

2.1.3.1 <u>Bipolar Digital SSI/MSI Devices</u>

er men en state and the the state of the state was the state of the state of the state of the state of the

The failure rate models are based on a collection of data which includes over 5 billion hours of storage or non-operating field data with 132 device failures. In addition, over 170 million hours of high temperature storage life data was collected with 616 device failures reported.

Storage data collected is summarized in tables 2.1-3 through 2.1-6. This data is organized in accordance to the metallization and interconnection systems.

Data sources for this analysis were:

- a) RADC-TR-73-248 report "Dormancy and Power On-Off Cycling Effects on Electronic Equipment and Part Reliability," August 1973
- b) The Reliability Analysis Center Generic Failure Rate
   Publication December 1973
- c) Sandia Corp. W68 Field Experience
- d) Raytheon Improved Hawk Field Experience
- e) Planning Research Corporation Data on Standby Devices
- f) Special Test Data on the General Electric Site Defense Program.

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A first characterization of the storage or non-operating data identified a definite correlation between the device failure rate and the device quality and temperature. However, insufficient data was available to determine the effect of a learning factor or an application environment factor. The data on device complexity was analyzed but no significant differences were noted between the storage failure rate and the complexity of the device for SSI/MSI devices.

During the first characterization of the non-operating data, the failure experience indicated a sufficient difference between devices with aluminum metallization/aluminum wire systems and aluminum metallization/gold wire systems to require segregation of the data sets. This led to the segregation of data sets for other

metallization/interconnection systems even though sufficient data was not available to completely characterize them.

The initial data characterization divided the data into several data sets with the prime category being metallization/ interconnection systems; the first subcategory being quality level; and the second subcategory being ambient temperature.

Following this characterization several other potential reliability factors were investigated. The results of the investigations indicated that no significant reliability difference was apparent in the data for storage duration, logic type, or package type. The data was insufficient to determine any factors for the die attach method or glassivation.

Failure mechanisms for 28 of the 372 storage life test failures of aluminum metallization/aluminum wire devices were reported. In the aluminum metallization/gold wire case, failure mechanisms for 155 of the 243 storage life test failures were reported. The distributions of failure mechanisms for both aluminum and gold wire systems are shown in Table 2.1-7.

### 2.1.3.2 Bipolar Linear SSI/MSI Devices

The failure rate models are based on a collection of data which includes over 1.7 billion hours of storage or non-operating field data with 12 device failures reported. In addition over 39 million hours of high temperature storage life data was collected with 87 device failures reported.

Storage data collected is summarized in Tables 2.1-8 and 2.1-9 depending on the metallization and interconnection systems used:

Primary data sources include two missile programs, one special storage program and two reliability data banks.

QUALITY LEVEL	AMBIENT TEMPERATURE	STORAGE HOURS X 10 <sup>6</sup>	NUMBER FAILED	FAILURE RATE
Class A	25-30°C 22°C (Nitro-	5,861.4	5	.85
	gen Atmosp.)	1,071.2	0	(<.9)
	125°C	.113	0	(<8850.)
Class B	25-30°C	3,512.7	11	3.1
	150°C	.155	0	(<6452.)
	250°C	.009	2	222000.
Class C	25-30°C	2,103.0	8	.3.8
	125°C	.4	0	(<2500.)
	150°C	64.593	25	387.
	180°C	.11	0	(<9091.)
	200°C	5.954	16	2687.
	250°C	3.1	23	7420.
	300°C	3.656	59	16136.
	350°C	2.152	148	68760.
Class D	25-30°C	4.61	0	(<217.)
~~~	125°C	2.953	5	1693.
	150°C	42.207	39	924.
	175°C	1.643	9	5479.
	180°C	.205	0	(<4878.)
•	200°C	6.472	0 3	463.
	300°C	.788	43	54558.

TABLE 2.1-3. MONOLITHIC BIPOLAR DIGITAL NON-OPERATING DATA (ALUMINUM METALLIZATION, ALUMINUM WIRE)

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TABLE 2.1-4. MONOLITHIC BIPOLAR DIGITAL NON-OPERATING DATA (ALUMINUM METALLIZATION, GOLD WIRE)

QUALITY LEVEL	AMBIENT TEMPERATURE	STORAGE HOURS X 10 <sup>6</sup>	NUMBER FAILED	FAILURERATE IN FITS*
Class A	250°C	.01	0	(<100000.)
	300°C	.01	0	(<100000.)
	350°C	.01	0	(<100000.)
Class B	25-30°C	2,604.11	77	30.
Class C	150°C	15.848	50	3155.
	175°C	.282	0	(<3546.)
•	200°C	.758	9	11873.
	250°C	.315	13	41270.
Class D	25-30°C	.268	0	(<3713.)
	125°C	.307	0	(<3257.)
	150°C	16.875	25	1481.
	180°C	.086	7	81112.
	200°C	.119	40	336417.
	250°C	.063	99	1462000.

\* Failures per Billion Hours

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TABLE 2.1-5. MONOLITHIC BIPOLAR DIGITAL NON-OPERATING DATA (GOLD METALLIZATION, GOLD WIRE)

QUALITY LEVEL	AMBIENT TEMPERATURE	STORAGE HOURS X 10 <sup>6</sup>	NUMBER FAILED	FAILURE RATE
Class B	25-30°C	.354	0	(<2825.)
Class C	25-30°C	8.689	0	(<115.)
Class D	25-30°C	8.689	0	(<115.)

TABLE 2.1-6. MONOLITHIC BIPOLAR DIGITAL NON-OPERATING DATA (GOLD BEAM SEALED JUNCTION) 

QUALITY	AMBIENT	STORAGE	NUMBER	FAILURE RATE
LEVEL	TEMPERATURE	HOURS X 10 <sup>6</sup>	FAILED	IN FITS
Class B	150°C	.045	0	(<22200.)
Class D	150°C	2.41	0	(<415.)
	200°C	2.13	1	469.
	300°C	.062	0	(<16200.)

#### TABLE 2.1-7. PRINCIPLE FAILURE MECHANISMS

Aluminum Metallization, Aluminum Wire, Gold Post

Oxide Defects (31%) Wire Bond (19%) Diffusion Defects (16%) Surface Inversion (13%) Al-Au Post Bond (12&) Die Bond (3%) Lead Failures (6%) Aluminum Metallization, Gold Wire, Gold Post Wire Bond (76%) Resistive Output (16%) Oxide Defects (4%) Die Bond (2%) Wire Shore (2%) Cracked Die (1%) The initial data characterization divided the data into several data sets with the prime category being metallization/ interconnection systems; the first subcategory being quality level; and the second subcategory being ambient temperature.

No data was available, on gold metal system or beam lead systems.

Compared to the bipolar digital device data, considerably less data is available on the bipolar linear devices. A comparison of these two data sets indicated a close correlation. Coefficients of correlation for the linear data points to the digital prediction models were calculated to be 0.899 for quality class C and 0.933 for class D devices with aluminum metallization/ aluminum wire systems. Insufficient data points were available on devices with aluminum metallization/gold wire systems to estimate a correlation.

Based on this close correlation, a test of significance was performed to determine whether there was any significant difference in the linear and digital data points. The test indicated no significant difference and for the linear data a decision was made to use the same Arrhenius function developed for the digital data points. Following the decision to use the digital prediction models, data on storage duration, device function, package type, die attach method and glassivation was analyzed for linear devices and for digital and linear devices combined to determine potential reliability problems. The results of the investigation indicated that no significant reliability difference was apparent for these factors.

No data on failure mechanisms was available for the linear devices in storage. Since the bipolar linear device construction is identical to the digital device, no significant difference would be anticipated. The primary operational failure modes for linear devices which are not as predominant for digital devices are drift and inversion phenomenon. The failure modes may be

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QUALITY	AMBIENT	STORAGE	NUMBER	FAILURE RATE
LEVEL	TEMPERATURE	HOURS X 10 <sup>6</sup>	FAILED	
Class A	150°C	.038	0	(<26316.)
Class B	25-30°C	556.266	2	3.59
	150°C	.076	0	(<13158.)
Class C	150°C	9.709	4	411.
	180°C	7.959	0	(<126.)
	200°C	3.034	1	330.
	250°C	.338	3	8876.
	300°C	.292	3	10274.
	350°C	.069	4	58309.
Class D	100°C	.010	0	(<100000.)
	150°C	13.392	15	1120.
	300°C	.131	9	68702.
	350°C	.041	29	710784.
Class B-A	24°C-Ni- trogen Atmosphere	·289.966	1	3.45

#### TABLE 2.1-8. MONOLITHIC BIPOLAR LINEAR NON-OPERATING DATA (ALUMINUM METALLIZATION, ALUMINUM WIRE)

TABLE 2.1-9. MONOLITHIC BIPOLAR LINEAR NON-OPERATING DATA (ALUMINUM METALLIZATION, GOLD WIRE)

QUALITY LEVEL	AMBIENT TEMPERATURE	STORAGE HOURS X 10 <sup>6</sup>	NUMBER FAILED	FAILURE <sup>:</sup> RATE IN FITS*
Class B	25°-30°C	114.	6	53.
Class C	150°C	2.880	б	2083.
Class D	150°C	, 896	4	4463.

TABLE 2.1-10. MONOLITHIC BIPOLAR LINEAR NON-OPERATING DATA (METALLIZATION/WIRE TYPE UNKNOWN)

QUALITY	AMBIENT TEMPERATURE	STORAGE HOURS X 10 <sup>6</sup>	NUMBER FAILED	FAILURE RATE IN FITS*
Class A	25°-30°C	535.534	1	1.86
Class B	25°-30°C	235.534	2	8.49

caused by ionic contamination or defects in the chip surface and normally require a certain amount of operational time for their occurrence. Therefore, the bipolar linear device failure mechanisms in storage would be similar to those reported for digital devices which include oxide defects, failed wire bonds, diffusion defects, failed die bonds and lead failures.

#### 2.1.3.3 . MOS SSI/MSI Devices

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The data collected on MOS SSI/MSI Devices did not include any field data but consisted of approximately 4 million hours of high temperature storage life data with 81 device failures reported.

Storage data collected is summarized in Table 2.1-11. Data is given by metallization/Interconnection Systems, quality level, storage temperature and complexity.

Failure modes or mechanisms for 35 of the storage life test failures were reported. These modes and mechanisms are listed in Table 2.1-12.

#### 2.1.3.4 Bipolar & MOS LSI Devices

All data available on Bipolar and MOS LSI Devices was included in the memory section. This included complex (larger than dual 8-bit) static and dynamic shift registers. Smaller shift registers were included in the Digital SSI/MSI models.

#### 2.1.3.5 Memories

Data on two major categories of monolithic memories was collected: random-access memories (RAMS) and read only memories (ROMS). Complex (larger than dual 8-bit) static and dynamic shift registers were included with the RAM data.

Data on RAMS consisted of 3 million hours of storage data roughly equivalent to field storage with no failures reported. In addition, approximately 5 million hours of high temperature storage life data with 76 device failures was reported.

Data on ROMS consisted entirely of high temperature storage life data with slightly more than 1 million hours and 25 failures reported.

#### TABLE 2.1-11

Quality Level	Ambient Temperature	Metal/Inter-	Complex.	Part Stor. Hrs.x 10 <sup>6</sup>	No. of Failures	Fail.Rate in Fits
A	150°C	Al/Al	SSI MSI	.015 .017	0 5	(<66657.) 299401.
D	125°C 140°C 150°C	Al/Al Al/Al Al/Al	MSI SSI SSI MSI	.206 .011 2.232 .084	24 1 2 0	121654. 88889. 896. (<11905;)
С	150°C	Al/Au	MSI	.100	0	(<10000.)
D	130°C 150°C 250°C 300°C 350°C	Al/Au Al/Au Al/Au Al/Au Al/Au	MSI SSI MSI SSI SSI SSI	.510 .108 .242 .057 .110 .062	1 0 1 15 3J	1961. (<9259.) 4127. 17544. 136363. 497592.

#### MOS SSI/MSI DEVICE NON-OPERATING DATA

1. H. H. H.

TABLE 2.1-12

MOS SSI/MSI DEVICE REPORTED FAILURE MODES & MECHANISMS

No. Reported	Mode or Mechanism
5	Drift
10	Open
1	Short
1	Field Oxide Short
2	<b>Gate Oxide Short</b>
1 '	Lid Seal Defective
2	Al Wire Bond Defects
6	Au Ball Bond Defects
2	Al/Au Kirkendall Voids
1	Die Bond Defect
1	Resistive Junction
19	Contamination
2	Foreign Particles

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The storage data collect is summarized in Tables 2.1-13 through 2.1-15. Data is given by quality level, storage comperature, complexity, metallization/interconnection system and logic type.

Failure modes or mechanisms for 55 of the storage life test failures were reported. These modes and mechanisms are listed in Table 2.1-16.

arter distriction of the second second of the second s

(ALUMINUM METALLIZATION/ALUMINUM WIRE SYSTEM) STORAGE FAILURE HOURS X 10 QUALITY NUMBER RATE FAILED BITS LOGIC LEVEL TEMP IN FITS C 150°C 1024 MOS .050 0 (<20000.)85°C 64 MOS .400 0 (<2500.) D 125°C 256 TTL 7 .139 50360. D MOS .384 (< 2600.)16 0 64 MOS .180 18 (<100000.) 256 MOS .226 2 8850. (<25000.) 1024 MOS .040 0 D 150°C 8 TTL .025 0 (<40000.) .252 16 TTL 0 (<3968.)64 TTL .015 0 (<66700.) MOS .038 0 (< 26300.)\_ 32 MOS .028 0 (<35700.)

TABLE 2.1-13. RANDOM-ACCESS MEMORIES (RAMS) NON-OPERATING DATA (ALUMINUM METALLIZATION/ALUMINUM WIRE SYSTEM)

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# TABLE 2.1-14. RANDOM-ACCESS MEMORIES (RAMS) NON-OPERATING DATA

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64

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256

1024

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MOS

	(ALUMIN	UM MET	<b>FALLIZ</b>	ATION/GOL	D WIRE S	System)
				STORAGE		FAILURE
QUALITY				HOURS	NUMBER	RATE
LEVEL	TEMP	BITS	LOGIC	<u>x 10°</u>	FAILED	IN FITS
D	85°C	20	MOS	.220	0	(<4545.)
		21	MOS	2.200	0	(<454.)
	du	al 25	MOS	.220	0	(<4545.)
	125°C	-	MOS	.034	0	(<29400.)
		256	MOS	.375	0	(<2667.)
		512	MOS	.288	34	118000.
		1024	MOS	.218	0	(<4590.)
	130°C	-	MOS	.040	0	(<25000.)
		20	MOS	.470	0	(<2128.)
		21	MOS	.360	0	(<2778.)
	đu		MOS	.300	Ō	(<3333.)
		64	MOS	.060	0	(<16700.)
	150°C	20	MOS	.160	1	6250.
	du		MOS	.054	ō	(<18500.)
		64	MOS	.051	Õ	(<19600.)
		1024	MOS	.036	ŏ	(<26700.)
		64	TTL	.104	õ	(<9615.)
	160°C	256	MOS	.100	ŏ	(<10000.)
		1024	MOS	.144	Õ	(<6969.)

QUALITY LEVEL	TEMP	BITS	LOGIC	STORAGE HOURS X 10	NUMBER FAILED	FAILURE RATE IN FITS
(ALUMINU	JM META	L/ALUM	INUM WIRE	SYSTEM)		
С	180°C	1256	Schottky TTL	.019	0	(<52600.)
	150°C	512	TTL	.092	0	(<10870.)
		8256	TTL	.022	0	(<45400.)
D	125°C	64	Schottky TTL	.529	23	43500.
		2048	MOS	.058	0	(<17000.)
	150°C	1024		.050	2	40000.
			RTL	.211	0	(<4740.)
		1024	MOS	.018	Ō	(<57100.)
	160°C	64	Schottky TTL	.025	0	(<40000.)
		2048	MOS	.005	0	(<200000。)
(ALUMINU	JM META	L/GOLD	WIRE SYST	rem)		
В	160°C	256	Schottky TTL	.025	0	(<40000.)
D	150°C	2560	MOS	.052	0	(<19300.)
-	_~~ ~		MOS	.068	ō	(<14700.)
	160°C	2048	MOS	.025	ŏ	(<40000.)

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TABLE 2.1-15. READ ONLY MEMORIES (ROMS) NON-OPERATING DATA

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2.1-37

	- -		No. of <u>Units</u>	Mode or Mechanism
RAMS	- Al Metal/Al Wire	٤	? 18 1 2	Oxide Pinhole Gate Oxide Pinhole Field Oxide Pinhole Contamination
RAMS	- Al Metal/Au Wire		2 1 31	Gate Oxide Pinhole Field Oxide Pinhole Contamination
ROMS	- Al/Metal/Al Wire	<b>N</b>	?	Wire Bond Defects
ROMS	- Al Metal/Au Wire	- None	Reported	

## TABLE 2.1-16 MEMORIES REPORTED FAILURE MODES AND MECHANISMS

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# 2.2 <u>Monolithic Integrated Circuits Operational Prediction Models</u> The MIL-HDBK-217B general failure rate model for monolithic integrated circuits is:

 $\lambda_{p} = \pi_{L} \pi_{Q} (\pi_{T} C_{1} + \pi_{E} C_{2}) \times 10^{-6}$ 

where:

Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Contro

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 $\lambda_{p}$  = device failure rate  $II_{T}$  = learning adjustment factor

 $I_0 =$ quality adjustment factor

 $I_m = Temperature Adjustment Factor$ 

II = Environmental Adjustment Factor

The various types of microelectronic devices require different values for each of these factors. The specific factor values for each type of device are shown in Figures 2.2-1 through 2.2-7.

In the title description of each monolithic device type, SSI, MSI, and LSI represent Small Scale Integration, Medium Scale Integration, and Large Scale Integration respectively, and indicate the complexity level for which the device model is applicable. MOS represents all metal-oxide semiconductor microcircuits which includes NMOS, PMOS, CMOS, and MNOS fabricated on various substrates, such as sapphire, polycrystalline, or single crystal silicon.

Since different models are designated for the SSI/MSI and LSI Monolithic Digital devices, the following distinction in terms of complexity level is made in order to provide guidance in selection of the appropriate model. For the present, and until a new limit is established, devices having complexities less than 100 gates (approximately 400 transistors) are to be considered as SSI/MSI devices. More complex devices by gate count (or transistor count at 4 per gate) are to be considered as LSI devices. No distinction is made between SSI and MSI Monolithic Digital devices since the same model applies directly to both. Also, no distinction is made between the complexity factors for MOS and Bipolar devices in that the factors that define complexity are independent of the specific technologies.

2.2-1

For the purposes of this handbook, a gate is considered to be any one of the following logic functions: AND, CR, NAND, NOR, Exclusive OR, and Inverter. A J-K or R-S flip-flop is equivalent to 8 gates when used as part of a complex circuit. When the flip-flop is individually packaged (single, dual, or greater) the gate count should be determined from the schematic or logic diagram. For guidance in symbols used for these functions, see Standard ANSI Y32.14-1973, "Graphic Symbols for Logic Diagrams." This standard has been adopted by the Department of Defense and supersedes Mil-Std-806B (an earlier logic symbol standard).

Monolithic memories, because of their high gate-to-pin ratio, are not treated as a part of the SSI/MSI/LSI models. Their complexity factors are expressed in terms of the number of bits and are divided into the two major categories of monolithic memories: random-access memories (RAMS), and read-only memories (ROMS). However, for the purposes of this handbook, programmable-read-only memories (PROMS) and content-addressable memories (CAMS) are considered in the same categories as ROMS and RAMS, respectively; therefore, the same models are applicable. For complex (larger than dual 8-bit) static and dynamic shift registers, use the RAM model with bit count. For smaller shift registers, use the Digital SSI/MSI model. For linear devices, both MOS and Bipolar, the same model expressing complexity in terms of the number of transistors is presented. wedered there extends the way was to a

Table 2.2-1 provides a list of monolithic microelectronic generic groups with a cross reference to the corresponding figure number.

The failure rate model and adjustment factors are based on certain assumptions and sub models. See Sections 2.2.1 and 2.2.2 for a description of these parameters.

2.2.1 Model Description

In order to help clarify some of the parameter descriptions for the various models, all of monolithic device models are based on a " $\lambda_{\rm T}$  +  $\lambda_{\rm M}$  additive model concept" -- i.e.  $\lambda_{\rm P} = \lambda_{\rm T} + \lambda_{\rm M}$ ,

where:

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MONOLITHIC MICROELECTRONIC OPERATIONAL PREDICTION MODELS CROSS REFERENCE TABLE 2.2-1.

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Monclithic Microelectronic Type

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Monolithic Microelectronic Type	Figure No.
Bipolar Digital SSI/MSI IC's (TTL, DTL, etc., excluding Bipolar Beam Lead and Bipolar ECL)	2.2-1
Bipolar Beam Lead and Bipolar ECL Digital SSI/MSI IC's	2.2-2
Bipolar Linear SSI/MSI IC's	2.2-3
MOS Digital SSI/MSI IC's	2.2-2
MOS Linear SSI/MSI IC's	2.2-3
Bipolar Digital LSI IC's (TTL, DTL, etc., excluding Bipolar Beam Lead and Bipolar ECL)	2.2-4
Bipolar Beam Lead and Bipolar ECL Digital LSI IC's	2.2-5
MOS LSI IC'S	2.2-5
Bipolar Memory IC's (TTL, DTL, etc. excluding Bipolar Beam Lead and Bipolar ECL)	2.2-6
Bipolar Beam Lead and Bipolar ECL Memory IC's	2.2-7
MOS Memory IC's	2、2-7

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MONOLITHIC BIPOLAR DIGITAL SSI/MSI INTEGRATED CIRCUITS (TTL, DTL, etc. excludes Beam Lead & ECL) MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FIGURE 2.2-1

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 $\lambda_{\rm y}$  =  $\pi_{\rm L}\pi_{\rm Q}$  (  $\pi_{\rm T}c_{\rm l}$  +  $\pi_{\rm E}c_{\rm 2}$  ) x 10<sup>-6</sup>

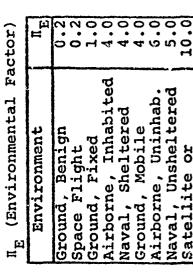
 $\pi_{\mathrm{L}}$  (Learning Factor)

for 1) a new device in initial production 2) a major change in design or process 3) extended line interunption or change in line personnel
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Factor)	β			5		2			10				16		150	-
II <sub>Q</sub> (Quality Fa	Quality Level	85	3	L-M-385	Class B (JAN)	L-STD-8	Method 5004	Class B	Vendor Equiv.	MIL-STD-883	Method 5004	Class B	MIL-M-35810	Class C (JAN)	Commercial	Class D

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		25												



Airborne, Inhabited

Ground, Fixed

Naval, Sheltered

Ground, Mobile

Naval, Unsheltered Satellite or Airborne, Uninhab

Missile, Launch

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL MUNOLITHIC BIPOLAR BEAM LEAD, BIPOLAR ECL & MOS FIGURE 2.2-2

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DIGITAL SSI/MSI INTEGRATED CIRCUITS

 $\lambda_{\rm p} = \pi_{\rm L} \pi_{\rm Q} \ ( \pi_{\rm T} c_{\rm l} + \pi_{\rm E} c_{\rm 2} \ ) \ x \ 10^{-6}$ 

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Space Flight	0.2
T T	1.0
Airborne, Inhabited	4.0
Naval, Sheltered	4.0
Ground, Mobile	4.0
Airborne, Uninhab.	6.0
Naval, Unsheltered	5.0
Satellite or	10.0
Missile, Launch	

2.2-5

FIGURE 2.2-3

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL MONOLITHIC BIPOLAR & MOS LINEAR SSI/MSI INTEGRATED CIRCUITS

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 $\lambda_{p} = \pi_{L}\pi_{Q} (\pi_{T}c_{1} + \pi_{E}c_{2}) \times 10^{-6}$ 

(Learning Factor) J.L.

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	FIGURE 2.2-4	MIL-HDBK-217B MONOLITHIC BI (TTL, DTL, et	ά D	ATION LSI clude	- E M	(O	RATE MODEL CIRCUITS 1 & ECL)	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
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IT. 28. 32. 42.56. 73. 94. 155. 25**0.** 39**0.** 610. 920 1.02 10.0000 μ (Environment Factor) ິບູ 125 135 145 155 165 175 110 20 105 e. E S (Temperature Factor) IT. 9 3.5 6.5 7.5 Airborne, Inhabited 11. 14. 16. 233. ່. ເດ Naval, Unsheltered თ Airborne, Uninhab Naval, Sheltered Launch . С, С, 833 83 89 16 0 0 0 0 0 81 87 97 66 79 101 Ground, Mobile Environment Benign Ground, Fixed Space Flight Satellite or 1.9 2.2 т.4 1.6 ПТ σ. <u></u>е C 68. • 2 ω d s Missile, Ground, မ် ရိ 67 σ 17 73 MONOLITHIC BIPOLAR BEAM LEAD, BIPOLAR ECL & MOS пЕ μŢ .17 .65 .20 .24 .29 .34 .40 .47 .56 .14 76 н ш ູ່ວ 29 33H 33H 37 4470 1010 1010 47 49 2 2 27 E .40 Factors) .19 .20 .22 .24 .26 .29 .31 • 34 .37 .44 .48 .52 .62 .67 .73 .79 86 ບິ່ງ യ 4 2 • 2  $( \pi_{T}c_{1} + \pi_{E}c_{2} ) >: 10^{-6}$ .36 .40 .44 .48 .53 .58 .64 .70 .93 . 77 extended line interruption or change ບົ • 2 ۍ ک <u>و</u> 2.0 2.6 3.3 4.2 5.3 major change in design or process 4. ້. ເວ new device in initial production ω (Complexity Gates 630 650 670 690 710 750 810 850 870 890 910 930 950 066 1100 No. 610 730 770 790 830 970 1050 1150 1200 1250 .088 .038 .041 .044 .053 .057 .062 .068 .020 .021 .023 .025 .028 .029 .032 .034 .048 .074 .080 CIRCUITS ບິ .10 3 .046 .061 .073 .088 .034 .038 .042 055 .080 .097 .030 .031 ວິ .12 .19 .14 .16 .23 .25 ບົ .21 27 Ч. ß INTEGRATED Gates in line personnel No. 110 130 150 190 210 310 350 370 390 410 430 450 470 490 510 530 550 230 250270 290 590 100 บ้  $\lambda_p = \pi_n \pi_0$ (Learning Factor) (Quality Factor) ц о 10 **1**6 150 2 S ർ đ otherwise ନିନିନ Quality Level (JAN) Class A (JAN) Vendor Equiv Class C (JAN) л, for MIL-M-38510 MIL-STD-883 MIL-M-38510 MIL-STD-883 MIL-M-35310 Method 5004 Method 5004 Commercial **Class B** 10 Class B Class B Δ -1 Class 11 ł °<sup>u</sup> L П,

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL

FIGURE 2.2-5

2.2-8

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FIGURE 2.2-6

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FOR BIFOLAR MEMORIES

(TTL, ETL etc., excludes Bipolar Beam Lead and Bipolar ECL)

 $\lambda_{p} = \pi_{L}\pi_{Q} (\pi_{T}c_{1} + \pi_{E}c_{2}) \times 10^{-6}$ 

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ictor)	пE	0.2	0.2	1.0	4.0	4.0	4.0	6.0	5.0	10.01
<sup>II</sup> (Environmental Factor)	Environment	Ground, Benign	Space Flight	Ground, Fixed	Airborne, Inhabited	Naval, Sheltered	Ground, Mobile	Airborne, Uninhab.	Naval, Unsheltered	Satellite or

Missile, Launch

FIGURE 2.2-7

FOR BIPOLAR BEAM LEAD, BIPOLAR ECL and MOS MEMORIES MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL

 $\lambda_{p} = \pi_{L}\pi_{Q} (\pi_{T}c_{L} + \pi_{E}c_{2}) \times 10^{-6}$ 

N<sub>L</sub> (Learning Factor)

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(Complexity	ROMS	c2			4	5	.012							.044		.051		-11	.12	.13	.14	.16	.17
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MIL-STD-883 Method 5004 16

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Class C (JAN)

Commercial

**Class D** 

MIL-M-35810

**Class B** 

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Satellite or Missile,

Launch

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Airborne, Inhabited

Naval, Sheltered

Ground, Mobile

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Quality Level

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Class A (JAN) MIL-M-38510 Class B (JAN)

MIL-M-38510

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MIL-STD-883 Method 5004

- $\lambda$  is the overall device failure rate for monolithic p devices.
- $\lambda_{\rm T}$  is the failure rate component due to time degradation causes, and represents degradation mechanisms which are accelerated by temperature and electrical bias; composed largely of phenomena which follow the Arrhenius type rate acceleration.
- $\lambda_{M}$  is the failure rate component due to mechanical (application environment) causes, and represents failure mechanisms resulting from mechanical stresses directly, or indirectly (such as stresses set up by thermal expansion).

#### 2.2.2 Parameters

The circuit complexity factors,  $C_1$  and  $C_2$ , are based on the models presented below.

2.2.2.1.1 Digital SSI/MSI Devices

Tabulated values are derived from the following equations:

$$C_1 = 1.29 (10)^{-3} (N_G)^{0.677} C_2 = 3.89 (10)^{-3} (N_G)^{0.389}$$

where  $N_{G}$  = number of gates (assumes 4 transistors per gate). The tabulated values are applicable to devices in packages containing up to 22 pins. For larger packages multiply the values by:

No. of Pins	Multiplier
24 to 40	1.1
42 to 64	1.2
>64	1.3

2.2.2.1.2 Linear SSI/MSI Devices

Tabulated values are derived from the following equations:

$$C_1 = .00056 (N_T)^{0.763}$$
  $C_2 = .0026 (N_T)^{0.547}$ 

where  $N_{\eta}$  = number of transistors.

2.2.2.1.3 LSI Devices

Tabulated values are derived from the following equations:

 $C_1 = .0187e^{(.00471)N}G$   $C_2 = .013e^{(.00423)N}G$ 

where  $N_{G}$  = number of gates (assume 4 transistors per gate) and e = natural logarithm base, 2.718.

The tabulated values are applicable to devices in packages containing up to 24 pins. For larger rackages, multiply values by:

No. of Pins	Multiplier
26 to 64	1.1
>64	1.2

Tabulated values are derived from the following equations: For ROMS -  $C_1 = .00114(B)^{0.603}$   $C_2 = .00032(B)^{0.646}$ For RAMS -  $C_1 = .00199(B)^{0.603}$   $C_2 = .00056(B)^{0.644}$  where: B = number of bits.

The tabulated values are applicable to devices in packages containing up to 24 pins. For packages with greater than 24 pins, multiply tabulated values by 1.1.

2.2.2.2 Learning Adjustment Factor, IIL

 $I_L$  adjusts the model for production conditions and controls. The conditions are defined in the figures for each device type.

2.2.2.3 Quality Adjustment Factor, IQ

 $II_Q$  accounts for effects of different quality levels as defined in MIL-M-38510 and MIL-STD-883.

2.2.2.4 Temperature Adjustment Factor, IT

 $I_T$  adjusts the model for temperature acceleration factors. Two models are applicable:

ITL is applicable to Bipolar Digital devices, i,e.
TTL and DTL, not included in ITTL below.
ITTL = 0.1eX

where  $x = -4794 \left( \frac{1}{T_j + 273} - \frac{1}{298} \right)$ 

 $I_{T2}$  is applicable to Bipolar and MOS Linear, Bipolar Beam Lead, Bipolar ECL, and all other MOS devices.

$$\Pi_{T2} = 0.1e^{x}$$
  
where: x = -8121 ( $\frac{1}{T_{j}} + \frac{1}{273} - \frac{1}{298}$ )

In  $I_{T1}$  and  $I_{T2}$  above,  $T_j$  is the worst case junction temperature (°C) and e is natural logarithm base, 2.718.

If T<sub>i</sub> is unknown, use the following approximations:

For packaged monolithic devices use:

 $T_j$  = ambient T + 10°C if number of transistors < 120.  $T_j$  = ambient T + 25°C if number of transistors >120.

2.2.2.5 Environmental Adjustment Factor,  $I_E$ 

 $I_E$  accounts for the influence of environmental factors other than temperature. Refer to the environment description in the Appendix.

#### 2.3 Hybrid Integrated Circuits Storage Reliability Analysis

A hybrid integrated circuit is any combination of solid state active circuit components (IC or discrete) and of thin or thick film-deposited passive circuit elements, in combination with other compatible discrete parts when called for, interconnected by film patterns on one or more substrates in a single device package, to perform one or more circuit functions. Hybrid IC's are commonly classified as either thin or thick film.

A vapor deposited or vacuum-evaporated, or also sputtered, plated or grown film circuit is called "thin film" when the mean free path of its current carriers (mainly electrons) is comparable in length to the thickness of the film, usually in the range of a few thousand Angstroms. In practice thin film is limited to a maximum of 10,000 Angstroms (1 micron).

A film circuit deposited by screen printing (or also by spraying) with subsequent air drying and high temperature firing steps, applied in sequential cycles, is commonly known as "thick film," denoting also that its structure came about by fusing originally separated and dispersed microscopic particulate matter into a self-passivating glaze. Thick film thickness overlaps the range of thin film thickness and extends approximately to 2.5 mils (63 microns).

#### 2.3.1 Hybrid Device Failure Mechanisms

The hybrid failure mechanisms include all those listed for the monolithic devices plus those that are unique to the hybrid technology. Hybrid devices exhibit problems as a result of the number of different materiels used in one package; the number of interconnections and bonds; the amount of processing with the chance of error or inclusion of contaminating materiels; and the hermetic sealing of a larger package. Careful selection of materiels and control of processing and temperatures are required to prevent thermal mismatches between materiels; leaching, diffusion and migration of materiels; intermetallic compound formations; and corrosion. and a second 
Tables 2.3-1 and 2.3-2 summarize the mechanisms unique to thick and thin film devices. Many of these mechanisms would be detected in formal processing and screening.

In thick film devices, the faulty substrate bond or cracked substrate which is undetected or non-failed during processing will be accelerated to failure by mechanical vibration and shock. The frequency of this failure, whether in operation or not, is dependent on the transportation and handling of the equipment in the depots and field.

The failure mechanisms for thick film resistors include those failures in processing which would slip through the screens; those that are defects which are accelerated by high temperature or thermal cycling; and those that are a result of corrosion. The two latter groups of defects may be accelerated or decelerated to failure depending on the storage environment.

The chip element failure mechanisms in thick film devices are the same as monolithic except that bonding materiels or processes may be different.

The number of conductors and interconnections in the hybrid device lead to shorted conductors, faulty bonds, etc. Most of these defects are accelerated to failure by thermal or mechanical stresses. The silver migration depends on a high current density and would be decelerated in a storage environment.

The thin film devices exhibit similar types of failure mechanisms as thick film The unique mechanisms of thin film devices are those associated with the element films. Many of these defects are accelerated to failure by thermal stresses. The rate at which defects progress to failure is dependent on the environment. The ionic migration between resistor strips is a function of high voltage and temperature and would be decelerated in a storage environment.

Most hybrid devices are custom designed for each application. The materiel selection, device design and processing for each application will determine the particular set of failure mechanisms experienced.

2.3-2

TABLE 2.3-1. HYBRID THICK FILM FAILURE MECHANISMS

The ALL DESCRIPTION OF A D

	<b>FAILURE</b> MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
	Substrate Faulty Substrate Bond	Insufficient or Incomplete Substrate Bonding	Mechanical Stress	Open	<b>Electrical</b> Test
	Cracked or Broken Substrate	<ol> <li>1) High Thermal stressed during processing</li> <li>2) Thin Substrate</li> </ol>	Mechanical Stress Mechanical	Open Open	Precap visual, electrical test Precap visual,
	Film Resistors	1) Overenter of shracive		, ro ro	Rlectrical
2.3-	Damaged Nestacor	overspray ur trimming mate adjacent resi during proces		open of out of tolerance	Probing
•3		<ol> <li>2) Electrostatic discharge during processing</li> <li>3) Leaching or diffusion at resistor-conductor inter- face</li> </ol>	Hi Tempera- ture	Open or Jut of tolerance Open or out of Tolerance	Electrical Probing
	Cracked Resistor	<ol> <li>Insufficient quantity of slow drying solvent, wetting agent, or flow</li> </ol>		Open	Electrical Probing
		2) Mismatch in thermal coefficient of expan- sion of the resistor, conductor and ceramic substrate	Thermal Cycling	Open	Open Electrical Probing

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TABLE 2.3-1 (continued)

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- HYBRID THICK FILM FAILURE MECHANISMS -

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1	FAILURE Mechanism	CAUSE	ACCELERATING ENVIR.ONMENT	FAILURE Mode	DETECTION . Method	
	Film Resistors (cont.)					· · · · · ·
	Out-of-tolerance Resistors	<ol> <li>Pailadium-silver re- sistor change in hydrogen atmosphere</li> <li>Hot spots at sharp corners or resistors</li> </ol>		Out of tolerance Out of tolerance	Electrical Probing Infrared scanning prior , to capping	
2.3-	Chip Elements					(H 2
	Faulty Bonds	<ol> <li>Insufficient or in- complete bonding</li> </ol>	Mechanical Stress	0pen	Bond Pull Test, Electrical Test	
		<pre>2) Leaching of silver- gold-solder combi- nations</pre>	Mechanical Stress	Open	Bond Pull Test, Electrical Test	
		3) Glass Frit Fracture	Mechanical Stress	Open	Bond Pull Test, Electrical Test	
	Cracked Dice	Mechanical stress during Processing	Thermal & Mechanical Stress	Open	Precap visual, Electrical Test	
		·				

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TABLE 2.3-1 (continued)

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- HYBRID THICK FILM FAILURE MECHANISMS

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	DETECTION METHOD	Precap visual, Electrical Test	Precap visual, Electrical Test Precap visual, Electrical Test	Precap visual, Electrical Tèst	Electrical Test
	FAILURE MODE	Short	Short Short	Short	Out-of- Tole:ance
FALLUAS RECORMENDED	ACCELERATING ENVIRONMENT	High Current Density with potentiaï dif- ference	Thermal & Mechanical Stresses Thermal & Mechanical Stresses	Thermal & Mechanical Stresses	
NULAR WILY AUTAL VULA	CAUSE	<ol> <li>Silver migration</li> <li>Silver migration</li> <li>Holes in glass insula- tion at crossover or insufficient thickness of glass.</li> </ol>	<ol> <li>Downbonding from a highar surface to a lowar one</li> <li>Improper lead length</li> </ol>	Insufficient or Imcom- plete Bcuding	Long parallel conductors resulting in capacitive coupling
	FAII.URE MECKANISM	Conductors Shorted Conductors	Shorted Intercon- necting wires	- Faulty Bonds	Capacít ve Coupling
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TABLE 2.3-2. HYBRID THIN FILM FAILURE MECHANISMS

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Electrical Test. Electrical Test Precap Visual, Precap visual Measurements, Capacitance DETECTION Substrate METHOD Tolerance Tolerance Out-of-Out-of-FAILURE MODE Open Thermal & Mechan-Thermal Stresses Thermal Cycling Thermal Cycling ical Stresses H1 Voltage & Temperature ACCELERATING ENVIRONMENT  $r_1O_2$  film exhibiting semi-Surface Alkali Concentratween film and substrate Diffusion of Alkali Ions rain size uncontrolled and Excess die bonding times during lapping, buffing or expansion mismatch be-. Ionic migration between from Substrate into re-Stresses during Processing Separation of Nichrome Thermal coefficient of large grains pulled out conductor properties during deposition Thermal & Mechanical and temperatures resistor strips Uneven surface CAUSE sistor film polishing. ttons ភ 5 9 2 3 64 3 Substrate Drif: of Electri-Craters or Pits cal parameters in Substrate MECHANISM Element Films Cracked FAILURE Substrate 2.3-6

and the second 
TABLE 2.3-2 (continued)

- HYBRID THIN FILM FAILURE MECHANISMS -

	FAILURE Mechanism	CAUSE	ACCELFRATING ENVIRONMENT	FAILURE Mode	DETECTION METHOD ·
<u> </u>	<u>Element Films</u> (cont.)				
	Cracked or Open Element	Thermal runaway due to constriction & oxidation		Open resis- tor, open or shorted capa- citor	Electrical Test
	Shorted Capacitor	Explosion of gases during vaporization		Short	Precap visual, electrical test
2.3	Chir & Wire Bonding				
	Bond Separation	<ol> <li>Irsufficient Bonding</li> <li>Jamage caused by probe testing</li> </ol>	Thermal & Mechanical Stresses A	Open	Precap visual, electrical test

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2.3-7

#### 2.3.2 Storage Reliability Data

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The storage data collected on hybrid integrated circuits consists of 799.2 million storage hours with 23 failures reported and 1.5 million hours of accelerated storage life tests with 7 failures reported. This data represents a quality level approximately equivalent to Class B in MIL-STD-883.

Based on the number of storage hours and failures, the storage failure rate for these devices is 28.8 failures per billion hours. However, the range of types and complexities of hybrid circuits precludes the use of a single failure rate for all devices. More data will be required to adequately evaluate hybrids in the storage or non-operating environment.

The data that has been collected is summarized in Table 2.3-3.

Of the thirty reported failures, twenty six failure causes were reported: one failed due to a failed zener diode, four due to open wire bonds; and twenty one due to open wire bonds at the aluminum/gold interface.

Ambient Temperature	Technology	Storage Hours (millions)	No. of Failures	Failure Rate in Fits
25°C	Thin Film	43.246	1	23.1
25°C	Thick Film	474.914	19	40.0
25°C	Thick Film	146.000	1	6.85
25°C	Thick Film	135.080	2	14.8
70°C	Thick Film	.400	0	(<2500.)
125°C	Thin Film	.098	2	20408.0
150°C	Thin Film	.680	3	4412.
150°C	Thick Film	.261	2	7663.
200°C	Thick Film	.011	0	(<90090.)

TABLE 2.3-3. HYBRID IC NON-OPERATING DATA

#### 2.4 Hybrid Integrated Circuits Operational Prediction Model

The MIL-HDBK-217B failure rate model for hybrid microelectronic devices is:

$$\lambda_{p} = \lambda_{b} (\Pi_{T} \times \Pi_{E} \times \Pi_{Q} \times \Pi_{F}) \times 10^{-6}$$

where:

 $\lambda_b$  = base failure rate  $I_T$  = temperature factor  $I_E$  = environmental factor  $I_Q$  = quality factor  $I_F$  = circuit function factor

From the I.C. chip standpoint, the hybrid model is structured to accommodate all of the monolithic chip types and the various complexity levels indicated in Section 2.2.

Figure 2.4-1 gives the hybrid model and values for each parameter. The base failure rate must be calculated and a description of this calculation is given below.

2.4.1 Base Failure Rate, 
$$\lambda_{h}$$

The base failure rate equation is:

 $\lambda_{b} = \lambda_{S} + A_{s}\lambda_{c} + \Sigma\lambda_{RT}N_{RT} \text{ (substrate contribution)}$  $+ \Sigma\lambda_{DC}N_{DC} \text{ (contribution of attached components)}$ 

+  $\lambda_{pF} \Pi_{pF}$  (package contribution)

#### A. Substrate Contribution

 $\frac{\lambda_S}{\Delta}$  is the failure rate due to the substrate and film processing. It has a value of either 0.02 or 0.04 and is independent of the number of substrates. The value 0.02 applies if only thick film or only thin film substrates are used. The value 0.04 applies if both types are used.

<sup>A</sup>s^c

is the failure rate contribution due to network complexity and substrate area. The values of  $\lambda_{C}$  (complexity term) are a function of the element density,  $N_{E}/A_{S}$ .  $A_{S}$  is the substrate area in square inches.

To compute complexity,  $A_S$  is obtained by summing the areas of all thick film substrates resulting in a single equivalent thick film substrate. An equivalent thin film substrate is determined similarly. However, when substrates are stacked, only the area of the bottom substrate shall be used to compute  $A_S$ . If a substrate contains only one device, it shall be considered a <u>chip</u> and shall not be considered a substrate for purposes of failure rate prediction.

 $N_{\rm F}$  is the total complexity expressed as

$$N_E = N_{LT} + N_{RT} + N_{DC}$$

where:

- N<sub>LT</sub> = number of internal lead terminations. Normally, this would be 2 times the number of leads, but for beam leads and flip chips, this would be one for each connection. This includes the leads from substrate to external leads.
- $N_{pm}$  = number of film resistors

As a convenience in estimating the number of terminations from the schematic, the following approximations may be used (it is always more desirable to count the actual lead terminations than to use the approximation):

$N_{LT} = No. of transistors$ .	x 4
+ No. cf diodes	x 2
+ No. of capacitors	x 4
+ No. of chip resistors	x 4
+ No. of conventionally pack- aged integrated circuit leads	x 2
+ No. of integrated circuit chip bond pads	x 2
+ No. of external hybrid package leads	x 2
2.4-2	

For the single equivalent thick film substrate, the value for  $N_E$  is determined from the above rules. Then  $N_E/A_S$  is computed using the  $A_S$  obtained in accordance with the above rules. The value of failure rate per square inch,  $\lambda_C$ , is obtained from the following equations.

For thin film :

$$\lambda_{C1} = 4.7(10)^{-8} \frac{N_E}{(\frac{A_S}{A_S})}^{2.082} \text{ for } 120 \leq \frac{N_E}{A_S} \leq 10,000$$
  
= .001 for 10 \leq \frac{N\_E}{A\_S} \leq 120

For thick film:

$$A_{C2} = 2.4(10)^{-14} \binom{N_E}{A_S}^{4.429} \text{ for } 250 \leq \frac{N_E}{A_S} \leq 2,000$$
  
= .001 for 10 <  $\frac{N_E}{A_S} \leq 250$ 

The final value of  $A_{S\lambda C}$  requires the use of the same  $A_S$  used to determine  $N_E/A_S$ 

This procedure is ther repeated for the chin film equivalent substrate. It should be noted that when  $N_E$  is computed for stacked substrates, the elements of the upper substrates are included with the bottom substrate, even though the upper substrate uses a different resistor technology than the bottom substrate (thin film or thick film or vice versa).

- $\frac{\Sigma N_{\rm RT} \lambda_{\rm RT}}{{}^{\rm as a function of the failure rates for each resistor}}$ is the sum of the required resistance tolerance.  $N_{\rm RT}$ is the number of film resistors of a given tolerance.
  - $\lambda_{\rm RT}$  is the failure rate to be used for each resistor of a given tolerance as specified in Figure 2.4-1.

2.4 - 3

#### B. Attached Components Contribution.

<sup>2</sup> $\lambda_{DC}N_{DC}$  is the sum of the attached device failure rates for semiconductors, integrated circuits, capacitors and resistors, both packaged and unpackaged. The failure rate is computed by multiplying the  $\lambda_{DC}$  by  $N_{DC}$ , the quantity of each type. The  $\lambda_{DC}$  is the same for a packaged or unpackaged device. The  $\lambda_{DC}$  values are in Figure 2.4-1.

#### C. Package Contribution.

is the hybrid package failure rate which is a function of the package style or configuration and the materials used in its construction.  $\lambda_{\rm PF}$  is 0.01 failure/10<sup>6</sup> hr. This is a normalized value of base failure rate for all hybrid packages.  $\Pi_{\rm PF}$  is an adjustment factor which modifies  $\lambda_{\rm PF}$  as a function of the package style and materials. Its values are in Figure 2.4-1.

#### 2.4.2 I Adjustment Factors

## 2.4.2.1 Temperature Adjustment Factor, Nm

 $\Pi_{T}$  adjusts the model for temperature acceleration factors. The values in Figure 2.4-1 are derived from

 $I_{T} = e^{X}$ where x = -3411 ( $\frac{1}{T + 273} - \frac{1}{298}$ ) for  $I_{T1}$  if the temperature (°C) of the package mounting base is known, and x = -3794 ( $\frac{1}{T + 273} - \frac{1}{318}$ ) for  $I_{T2}$  if the highest temperature (°C) within the hybrid package is known.

 $I_T$  values are invalid at package mounting base temperatures above 125°C or for hot spot temperatures above 175°C.

## 2.4.2.2 Environmental Adjustment Factor, N<sub>E</sub>

 $I_E$  accounts for the influence of environmental factors other than temperature. Refer to the environment description in the appendix.

2.4-4

# 2.4.2.3 Quality Factor, MQ

 $I_Q$  accounts for effects of different quality levels. Classes A, B and C devices are those which have been subjected to, and passed all requirements, tests, and inspections specified in Methods 5004 and 5006 of MIL-STD-883, including screening, qualification, and quality conformance inspection requirements for the specified class. やためとうながなりなどではスタ

## 2.4.2.4 Circuit Function Adjustment Factor, $II_{F}$

 ${\rm I\!I}_{\rm F}$  adjusts the model for circuit function, (i.e., digital or linear).

MIL-HDBK-217B OPERATIONAL FAILURE FIGURE 2.4-1

RATE MODEL

+  $\sum \lambda_{RT}^{N}_{RT}$  +  $\sum \lambda_{DC}^{N}_{DC}$  +  $\lambda_{PF}^{\Pi}_{PF}$ (и<sub>т</sub> хи<sub>Е</sub> хи<sub>Q</sub> хи<sub>F</sub>) х 10<sup>-6</sup> FOR HYBRID MICROELECTRONIC DEVICES Ashc q q 11 + م ع ÿ, t ç, Ç

if highest temperature in 6.66 7.6 8.6 9.7 if package mounting base IT2 Temperature is known. 21. 24. 26. 29. 12. 16 19 4 11 2.2 1.0 4.0 4.0 6.0 0 0 0 0.2 496 13 package is known Factor) ПТТ  ${\tt I}_{\rm T}$  (Temperature Factor) 1 (°C) 105 110 20 125 130 135 140 145 150 155 165 170 175 ហ Naval, Sheltered Airborne, Inhab. I<sub>E</sub> (Environment Ground, Mcbile Environment Benign Ground, Fixed Space Flight .55 .68 . 83 .45 ကထ IIT2 4.U.8. 6.U.8 8 O 4 4. Ground, пт 6.8 °, 8. 8.8 5. 4.5 6.0 0.0 4 пт2 л<sup>л</sup>г T (°C) Use Use ກ ເວ ເວີຍ 60 70 80 40 S 30 S ŝ 0 4 Ø 4.0 3.0 1.5 2.0 2.5 2.5 4.0 4.0 5 0 0 with 1.5 2.0 "PF 0.1 Dual-In-Line (<16 leads)2.0 Top Hat Type (I.e. TO-3, (soldered lid) (soldered lid) up to 16 leads) Flat Pack (soldered lid, Vertical Sidewall (cold Substrates Dihedral (soldered lid) lid) Note: Forrall packages λ<sub>PF</sub>(Packaçe Failure Flat Pack (welded lid, (welded lid) (welded lid) outer seal perimeter or <0.625" diameter) Multiple Substrate seal perimeter or >0.625" diameter) Rate) Package Type (>2.25" (<2.25 Single Substrate Package Description Platform (soldered П<sub>PF</sub> (Package Factor) Multilayer Ceramic Modular Packages up to 16 leads) Package Type welded lid) Flat Pack Flat Pack Butterfly Butterfly outer TO-5) Thin Film Thick Film Resistors a Given 0.00050 0.00012  $\lambda_{\mathrm{RT}}$  (Resistor Tolerance Factor) Tolerance thick film if both thick film ADC (Attached Devices Term) thin film λ<sub>S</sub>(Substrate Failure Rate) A<sub>S</sub> (Substrate Failure Rate Square Inches λ<sub>C</sub> (Complexity Term) and thin film Substrate Area in # of attached Modifier) of Resistors of devices of a See next page given type. See next Page Resistors 0.00050 0.00025 0.00010 only only чн •न чо 5 0 0 0 .02 11 .04 Tolerance (-Percent) DC N Resistor # 11 t t ę 11 11 11 S. 5.0 Ś م م |<sup>N</sup>RT 1.0 0.1

Airborne, Uninhab Naval, Unshelt. Missile, П<sub>Р</sub> Е >16 leads, add 0.15 to leads >16. each 4 for

0.0

Launch

2.4-6

FIGURE 2.4-1 MIL-HDBK-217B OPERATIONAL FALLURE PATE MODEL FOR HYBRID MICROELECTRONIC DEVICES (continued)

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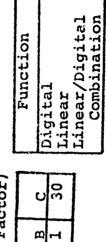
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λ<sub>DC</sub> (Attached Devices Failure Rate)

Attached Device Description	A DC
Capacitor Ceremin Ceneral Durnoco	
7、	0.004
J	1000.0
оr	0.0002
Here I	
Switch	0.0048
Signal ( <50	1800.0
Rectifier	0.012
Zener (volt. reg)	0.022
	0.05
Varactor; Step Rec; Tunnel	0.19
uerector Mixers	81.0
Transistor, Silicon*	
Ъ.	0 . 0053
NPN, Linear	110.
	0.5
	00
, Linear	.01
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olar digital de	*
& DTL types not included helow)	
& MOS	***
lead, bipolar E	
all other MOS devices.	
*For JAN TX or TXV multiply by 0 For NON-JAN/Commercial multiply	<b>م</b> ہم
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510 Quali - = 1.0.	24
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λ<sub>C</sub> (Complexity Term)

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	×	Thin										4					,	-1			Terminations		Devices	
/mrta	N EN		1500	ວິທີ		50	8	600			20	8	20	20	2 S	2	Š Š	2			Lead	Resistors	Chip D	II <sub>F</sub> (Circuit
בסדרא ד	AC2	Thi	ā	0100.	d	5	02	400	0 7	10	i m	<t< td=""><td>10 0</td><td><b>m</b> (</td><td>5 T T</td><td>71,</td><td>. ku</td><td>2 K 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td><td>.46</td><td><math>\frac{1}{N}</math></td><td>ernal</td><td>ilm Resi</td><td>screte (</td><td></td></t<>	10 0	<b>m</b> (	5 T T	71,	. ku	2 K 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	.46	$\frac{1}{N}$	ernal	ilm Resi	screte (	
+dimon 1 0	у СЪ У	Thin F.	· r	.0016	02	40	00	5,0	-	- C+		$\sim$	с	ົ່		$ \sim 1 $	<b>Λ</b> ι	$\sim$	$\sim$	$LT + N_{RT}$	of	# of Fi	# of Di	
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Level Pr Class

1-08 1-08 1-08

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#### 2.5 Operational/Non-Operational Failure Rate Comparison

#### 2.5.1 Bipolar Digital SSI/MSI Devices

A comparison of the failure rates for non-operational and operational environments was made using the non-operating model and the MIL-HDBK-217B operational model. The comparison is presented in Figure 2.5-1. Failure rates for several operating conditions were predicted to present a range for comparison. The non-operating prediction was made at a nominal ambient temperature of 25 degrees centigrade.

Comparing the digital devices with aluminum metallization and aluminum wire gave an operating to non-operating ratio of 7 and 9 for Class A, small scale integration (SSI), digital devices at two operation junction temperatures: 35°C and 75°C; for Class B the ratios were 4 and 5; for Class C devices, 23 and 30; and for Class D, 86 and 114.

For medium scale integration (MSI), the ratios for Class A were 15 and 25; Class B, 9 and 14; Class C, 54 and 89; and Class D, 204 and 334.

Failure rates for digital devices with aluminum metallization and gold wire were also compared. Since MIL-HDBK-217B uses one prediction model for both metallization systems, the operating failure rates are the same. For the non-operating failure rate, the aluminum metallization,gold wire systems exhibited a significantly higher failure rate, therefore the ratios are considerably different so different that in many cases, the non-operating failure rate is higher than the operating failure rate. The ratios for Class A, SSI Digital devices at the two junction temperatures are 0.6 and 0.8; for Class B, 0.4 and 0.5; for Class C, 2.2 and 3.0 and for Class D, 0.7 and 0.9.

For MSI devices, the ratios for Class A were 1.5 and 2.4; Class B, 0.9 and 1.4; Class C, 5.3 and 8.7; and Class D, 1.7 and 2.7.

Since most missile materiel are in the Class B or Class A quality range, average operating to non-operating factors can be defined as presented in Table 2.5-1.

2.5-1

OPERATING FAILURE RATES PER MIL-HDBK-217B*(GROUND FIXED ENVIRONMENT)
FIXED
(GROUND
-217B*(
MIL-HDBK
PER
RATES
FAILURE
OPERATING

$\frac{\text{Condition 1}}{\text{T}_{\text{J}} = 35^{\circ}\text{C}, 2 \text{ Gates}$	$\frac{\text{Condition 2}}{T_J = 35^{\circ}\text{C}, 20 \text{ Gates}}$	Condition 3 T = 75°C > Gates	n 4 C, 20
PARTS COUNT	14.5 29.0	232.0	1
CONDITION 4	20.8 41.6	NC	2 1 1
CONDITION 3	7.1 14.2	ີ ຕີ ແ	•
CONDITION 2	12.7 25.4	202.9	•
CONDITION 1	5.4 10.7	85.7 803 5	•
QUALTIY CLASS	4 A	טב	۵ د

NON-OPERATING FAILURE RATE & NON-OPERATING/OPERATING RATIO

1

ALUMINUM METALLIZATION, ALUMINUM WIRE:

	PARTS	COUNT	17	10	62	233		פיויק ממ	COUNT		1.0	6.1	1,9	
	RATIO	CONDITION 4	25	14	89	334		DTTD DTTD	CONDITION 4	Р С		8.7	2.7	
	RATIO	S NDITION 3	6	Ŋ	30	114		PATTO	CON	α	<u>،</u>	3.0	6.	
	RATIO	CONDITION 2	15	6	54	204	WIRE:	ратто	CONDITION 2	ע רי	0 1	5.4	1.7	
	RATIO	CONDITION 1	7	4	23	86	ALUMINUM METALLIZATION, GOLD WIRE:	DATTO	CONDITION 1	ų		2,2		Billion Hours.
do-non	FAILURE	RATE*	.83	2.91	3.73	9.34	METALLIZ	FATI HEF	RATE*	α α	29.8	38.3	1150.0	
LOWTHORY	QUALITY	CLASS	A	Ð	U	D	ALUMINUM	011AT T T V		A	; m	υ	D	*Failures per

FIGURE 2.5-1. MONOLITHIC RIPOLAR DIGITAL DEVICE OPERATIONAL/ NON-OPERATIONAL FAILURE RATE COMPARISON

2.5-2

TABLE 2.5-1.

## AVERAGE OPERATING TO NON-OPERATING FAILURE RATE RATIO ALUMINUM METALLIZATION/.LUMINUM WIRE

Complexity Level	Average Operating to Non- Operating Failure Rate Ratio
SSI	5.
MSI	14

#### ALUMINUM METALLIZATION/GOLD WIRE

Complexity	Average Operating to Non-
Level	Operating Failure Rate Ratio
SSI	0.5
MSI	1.4

The quality factors in the non-operating prediction model for a device with aluminum metal/gold wire systems were estimated from the aluminum metal/aluminum wire system. Therefore, these are preliminary and will be further investigated in subsequent reports.

2,5-3

#### 2.5.2 Bipolar Linear SSI/MSI Devices

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A comparison of the failure rates for non-operational and operational environments was made using the non-operating model developed here and the MIL-HDBK-217B operational model. The comparison is presented in Figure 2.5-2. Failure rates for several operating conditions were predicted to present a range for comparison. The non-operating prediction was made at a nominal ambient temperature of 25 degrees centigrade.

Comparing the digital devices with aluminum metallization and aluminum wire gave an operating to non-operating ratio of 10 and 26 for Class A, small scale integration (SSI), linear devices at two operation junction temperatures: 35°C and 75°C; for Class B the ratios were 6 and 15; for Class C devices, 38 and 93; and for Class D, 140 and 347.

For medium scale integration (MSI), the ratios for Class A were 40 and 131; Class B, 23 and 75; Class C, 141 and 468; and Class D, 527 and 1751.

Failure rates for linear devices with aluminum metallization and gold wire were also compared. Since MIL-HDBK-217B uses one prediction model for both metallization systems, the operating failure rates are the same. For the non-operating failure rate, the aluminum metallization, gold wire systems exhibited a significantly higher failure rate, therefore the ratios are considerably different - so different that in some cases, the non-operating failure rate is higher than the operating failure rate. The ratios for Class A, SSI linear devices at the two junction temperatures are 1.0 and 2.5; for Class B, 0.6 and 1.4; for Class C, 3.6 and 13.7 and for Class D, 1.1 and 2.8.

For MSI devices, the ratios for Class A were 3.8 and 12.8; Class B, 2.2 and 7.3; Class C, 13.7 and 45.5; and Class D, 4.3 and 14.2.

Since most missile materiel are in the Class B or Class A quality range, average operating to non-operating factors can be defined as presented in Table 2.5-2.

2.5-4

SNT)	tion 1 <u>35°C, 8</u> transistors	<b>a</b> 80	4 ° 80			٤		•		
D FNVIRONMENT	$\frac{\text{Condition}}{\text{T}_{-}} = \frac{35^{\circ}\text{C}}{2},$	T COndi COndi		OT.LAY ONT	PARTS COUNT	31	418	PARTS COUNT	3.0 10.9 3.4	OPERATIONAL/ ON
(GROUND FIXED	N 4 COUNT			NON-OFEKATING/ OFEKATING	RATIO CONDITION 4	131 75	468 1751	RATIO CONDITION 4	12.8 45.5 14.2	DEVICE
PER MT1-HDBK-217B* (GROUND	3 CONDITION		•	ð	RATIO CONDITION 3 C	26 15	347	RATIO CONDITION 3 0	29-1-2 -80-4-5 -80-4-5	BIPOLAR LINEAR FAILURE RATE C
RATES PER MTT	2 CONDITION	1		ALUMINUM WIRE:	RATIO CONDITION 2 C	40 23	527	WIRE: RATIO CONDITION 2 C	3.8 13.7 4.3	TTHIC
FAILURE	1 CONDITION			IZATION, ALUMINUM WIR	RATIO CONDITION 1 C	10 9 6	140	GOLD GOLD	1.0 1.6 0.1 1.6 1.1 1.0	Billion Hours. FIGURE 2.5-2. MONOL NON-OPERA
OPERATING	CONDITION	8.7 17.5 140.0 1312.0	č	ALUMINUM METALLIZATION,		.83 2.91 2.73	9.34	ALUMINUM METALLIZATION, NON-OP QUALITY FAILURE RATIC CLASS RATE* CONDITIC	8.5 29.8 38.3 1150.0	per
	QUALITY CLASS	えるじひ		ALUMINUA	QUALITY CLASS	<b>≮</b> ¤ (	20	ALUMINUM QUALITY CLASS	≪ ¤ ∪ D	*Failures

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2.5-5

#### TABLE 2.5-2.

### AVERAGE OPERATING TO NON-OPERATING FAILURE RATE RATIO ALUMINUM METALLIZATION/ALUMINUM WIKE

Complexity	Average Operating to Non-
Level	Operating Failure Rate Ratio
SSI	15
MSI	75
-	

#### ALUMINUM METALLIZATION/GOLD WIRE

Complexity Level	Average Operating to Non- Operating Failure Rate Ratio
SSI	1.4
MSI	7.3

The quality factors in the non-operating prediction model for a device with aluminum metal/gold wire systems were estimated from the aluminum metal/aluminum wire system. Therefore, these are preliminary results which should be further investigated.

2.6 Conclusions and Recommendations

The models presented in section 2.1 for monolithic bipolar SSI/MSI digital and linear integrated circuits can be used as a method of prediction failure rates for these devices.

The analysis indicates that a single metal should be used for the contact metallization and interconnection interface. The all-aluminum system shows a definitely more reliable storage capability than the aluminum metallization/gold wire system. Data on the Beam Lead Sealed Junction device with gold beams is not available on the linear devices.

In both user surveys and high temperature storage tests, wire bond failures were prominent. For the aluminum metallization/aluminum wire systems, the principle problems were wire bonds and oxide defects or contamination.

 $\left\{ \right\}$ 

Screens or tests recommended for wire bonds include centrifuge, temperature shock/cycling, power cycling, mechanical shock and bond pull tests. Due to the low mass of aluminum wires, the temperature shock/cycle, power cycle, and bond pull tests would be most effective.

Screens or tests recommended to weed out oxide defects include: Operating AC and DC with temperature; high temperature reverse bias; power cycling; elevated temperature storage; and visual inspection.

In the MIL-STD-883 screen, temperature cycling is required for Class A, E and C devices while temperature shock is only required for Class A devices. Burn-in and final electrical tests at maximum and minimum operating temperatures are required for Class A and B devices. Reverse bias burn-in is only required for Class A MOS and linear devices when specified. Visual inspection is required for Class A and B devices.

Depending on whether Class A, B or C devices are specified in the procurement, it may be desirable to specify more screens and/or quality conformance tests which are related to wire bond and oxide reliability.

Effects of periodic testing or operational cycling of devices which are in a storage or dormant environment has not been addressed here. The data does not identify the effects of cycling. One special test was performed to determine cycling effects on 1000 digital devices but after 18 months, no failures were experienced. The testing was performed under controlled conditions.

Lack of sufficient data on LSI devices, MOS devices and memories precludes any conclusions on these devices.

2.6-2

#### 2.7 Reference

The information presented for digital and linear devices is a summary of document numbers LC-76-ICl, "Monolithic Bipolar SSI/MSI Digital Integrated Circuit Analysis," dated May 1976 and LC-76-IC2 "Monolithic Bipolar SSI/MSI Linear Integrated Circuit Analysis," dated May 1976. Refer to those documents for details of the data collection and analysis, development of models, definition of failure mechanisms, and technical description of the devices themselves.

2.7-1

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2.7-3

#### 3.0 Discrete Semiconductors

This section contains a summary of the analyses and data on discrete semiconductors-transistors and diodes. Being special types of semiconductors, failure modes and mechanisms affecting transistors and diodes are similar to those found in other semiconductors discussed in Section 2.1. Also applicable are the causes, accelerating environments and detection methods. That information is well covered in Section 2.1 and will not be repeated in detail. Only differences between discrete semiconductors and integrated circuits will be discussed.

#### 3.1 Storage Reliability Analysis

#### 3.1.1 Failure Mechanisms

The failure mechanisms, causes, accelerating environment: and detection methods characteristic of transistors are found in Table 2.1-2. As in all semiconductors, transistors do not appear to have failure mechanisms inherent to the concept of the device. All of the mechanisms are initiated by deficiencies in the materials and fabrication processes used during manufacture of the devices.

The difference between discrete transistors and integrated circuits lies in the physical size and number and complexity of manufacturing processes. Compared to the average integrated circuit, a transistor is a relatively simple device. There are fewer number of junctions and leads. The distances between different parts of the device are larger. The manufacturing processes are fewer and simpler. Although the failure mechanisms are similar to those in integrated circuits, the above differences tend to shift their emphasis. Bulk defects are more common due to the larger blocks of silicon required thus increasing the probability of crystal imperfections. Imperfections collect mobilized contaminants resulting in breakdown, leakage, gain failures and, in high power devices, thermal runaway. Diffusion defects are not as critical due to the lower density of diffusions. Oxide and metallization defects are not as pronounced as in integrated circuits because the metallization patterns are much simpler.

A large percentage of transistor failures are the result of die and wire bonding defects. Contamination, both ambient and within the material, is also a serious problem in transistors.

The failure mechanisms of diodes are similar to those fo 1in transistors. The mechanisms, causes, accelerating environmencs and detection methods presented in Table 2.1-2 apply and will not be repeated here. In addition to those mechanisms in Table 2.1-2, alloy bonded and point contact diodes can develop intermetallic compounds at the junction, however, this has not been noticed to be a severe problem. Loss of contact is also a potential problem in spring loaded contacts. This happens when the contact material loses its compression strength or by slipping off the contact.

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3.1.2 Discrete Semiconductor Non-Operational Prediction Models

The non-operational failure rate model for discrete semiconductors is:

 $\lambda_{\rm p} = \lambda_{\rm b} (\Pi_{\rm Q} \times \Pi_{\rm E}) \times 10^{-6}$ 

where:

(

e:  $\lambda_p$  = device failure rate  $\lambda_b$  = base failure rate  $\Pi_Q$  = quality adjustment factor  $\Pi_E$  = environmental adjustment factor

The model and values for Silicon NPN & PNP and Germanium NPN & PNP Transistors are presented in Figure 3.1-1; and for Field Effect Transistors in Figure 3.1-2.

Non-operating data on Unijunction transistors was insufficient to develop a non-operating prediction at this time.

The model and values for General Purpose Silicon and General Purpose Germanium Diodes are presented in Figure 3.1-3; for Zener and Avalanche Diodes in Figure 3.1-4; and for Microwave Diodes in Figure 3.1-5.

Non-operating data on thyristors and varactors was insufficient to develop a non-operating prediction at this time.

In the models, the base failure rate,  $\lambda_{b}$ , is 0.82 fits (failures per billion hours) for silicon transistors; 0.77 fits for field effect transistors; 1.1 fits for general purpose diodes; and 0.55 fits for Zener and Avalanche Diodes; and 3.3 fits for microwave diodes.

The quality adjustment factor,  $\Pi_Q$ , accounts for effects of the quality levels (JAN and JANTX) as defined in MIL-S-19500.

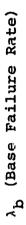
The environmental adjustment factor,  $\pi_E$ , accounts for the influence of factors other than temperature. Refer to the environmental description in the Appendix.

3.1-3

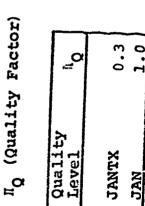
NON-OPERATIONAL FAILURE RATE PREDICTION MODEL FOR TRANSISTORS (Includes Silicon NPN & PNP, and Gernanium NPN & PNP) FIGURE 3.1-1.

たときないようというたいなどにためというというである

$$\lambda_{p} = \lambda_{b} (\Pi_{Q} \times \Pi_{E}) \times 10^{-6}$$







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al Factor)		-	Space Flight		ibited	red	•	cered	fnhab.	h.
(Eavironmental	Environment	Benign	light	Fixed	e, Inhe	Shelter	Mobile	Unsheltered	ie, Unir	, Launc
(Envir	Envi	'punoi	pace F	iround,	irborn	aval,	iround,	aval,	irborn	itssile
ы Ц		0	03	<u> </u>		4		Z	4	2

NON-OPERATIONAL FAILURE RATE PREDICTION MODEL FOR FIELD EFFECT TRANSISTORS FIGURE 3.1-2.

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$$\lambda_{\rm p} = \lambda_{\rm b} (\pi_{\rm Q} \times \pi_{\rm E}) \times 10^{-6}$$

λ<sub>b</sub> (Base Failure Rate)

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Π<sub>Q</sub> (Quality Factor)

ц	0.2	1.0	
Quality Level	JANTX	JAN	

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IL (Environmental Factor)

Environment	= E
Ground, Benign	1
Space Flight	-
Ground, Fixed	
Mirborne, Inhabited	2
Naval, Sheltered	2
Ground, Mobile	25
Naval, Unsheltered	2
ninha	
Missile, Launch	

3.1-5

NON-OPERATIONAL FAILURE RATE PREDICTION MODEL FOR CENERAL PURPOSE SILICON & GERMANIUM DIODES FIGURE 3.1-3.

$$\lambda_{\rm p} = \lambda_{\rm b} (\pi_{\rm Q} \times \pi_{\rm E}) \times 10^{-6}$$

λ<sub>b</sub> (Base Failure Rate)

4

NQ (Quality Factor)

а <sup>п</sup>	60.0	1.0
Quality Level	JANTX	JAN

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tal Factor)	nt <sup>n</sup> E	t us			Inhabited 25	d 2	7	Unsheltered 25	Uninhab. 40	4
I <sub>E</sub> (Environmental	Environment	Ground, Benign	Space Flight	Ground, Fixed	Airborne, Inl	Naval, Sheltere	Ground, Mobile	Naval, Unshe		Missile, Launch

NON-OPERATIONAL FAILURE RATE PREDICTION AND MODEL FOR ZENER AND AVALANCHE DIODUS FIGURE 3.1-4.

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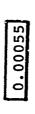
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 $\lambda_p = \lambda_b (\pi_Q \times \pi_E) \times 10^{-6}$ 

λ<sub>b</sub> (Base Failure Rate)



MQ (Quality Factor)

δ <sub>μ</sub>	1.0	1.0
Quality Level	JANTX	JAN

Factor)	
(Environmental	
ы ц	

Environment	e ۳
Ground, Benign	
Space Flight	-
Ground, Fixed	S
Airborne, Inhabited	
Naval, Sheltered	
Ground, Mobile	25
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Airborne, Uninhab.	
Missile, Launch	

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NON-OPERATIONAL FAILURE RATE PREDICTION AND MODEL FOR MICROWAVE DIODES FIGURE 3.1-5.

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$$\lambda_{p} = \lambda_{b} (\Pi_{Q} \times \Pi_{E}) \times 10^{-6}$$

λ<sub>b</sub> (Base Failure Rate)

ng (Quality Factor)

ц	.6	1.0
Quality Level	JANTX	JAN

RE (Environmental Factor)

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Environment	ΠE
Ground, Benign	1
Space Flight	Ч
Ground, Fixed	10
ne,	50
Naval, Sheltered	50
Ground, Mobile	50
Naval, Unsheltered	50
Airborne, Uninhab.	80
Missile, Launch	200

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### 3.1.3 <u>Non-Operating Failure Rate Data and Analysis</u> 3.1.3.1 Transistors

The failure rate models in Section 3.1.2 are based on storage data consisting of over 18 billion hours with 36 failures reported. This includes data from six different programs. The breakdown of storage hours and failures for each source (identified by code names A through F) is shown in Tables 3.1-1 through 3.1-6). In cases where definition of device type and application was not possible, the data was aggregated into an "all types" category. For example, programs E and F utilized JANTX transistors, however further designation was not possible.

The aggregation of storage hours and failures from all five programs is shown in Table 3.1-7. This table presents the aggregated data for both JANTX and JAN rated devices.

Analysis of this data together with the parameters in the MIL-HDBK-217B model indicated very little difference between the failure rates of silicon NPN and PNP transistors.

The storage data indicated a difference between JAN and JANTX device failure rates in the operational and non-operational environments. While the MIL-HDBK-217B operational model shows a factor of five, the storage data indicated a factor of 3+. Field effect transistor data indicates for JANTX devices to be in the same general failure rate range as the silicon NPN and PNP devices. No JAN data was available on the field effect transistors and a factor of 5 from MIL-HDBK-217B was used.

Insufficient data on Unijunction Transistors is available for analysis.

3.1.3.2 Diodes

The failure rate tables in Section 3.1.2 are based on storage data consisting of over 30 billion part hours with 57 failures reported. This includes data from four different programs. The breakdown of storage hours and failures for each program (identified by code names A through D) is shown in Tables 3.1-8 through 3.1-11. In cases where the definition of device type and application was not possible, the data was aggregated into an "all types" category.

3.1-9

The aggregation of storage hours and fialures from all three programs is shown in Table 3.1-12.

Analysis of this data together with the parameters in the MIL-HDBK-217B model indicated very little difference between the failure rates of Silicon and Germanium General Purpose Diodes. ٩.,

The storage data did indicate a greater difference between JAN and JANTX device failure rates than in the operational environment. While the operational model shows a factor of 5, the storage data indicates a factor of 11+.

The present storage data on Zener Diodes does not show a difference between the JAN and JANTX devices. The JANTX data shows 3 tailures in approximately 1.1 billion hours for a storage failure rate of 2.8 fits while the JAN data shows no failures in 0.8 billion storage hours for a failure rate of less than 1.2 fits. This rate is approximately five times that of the Silicon Ceneral Purpose Diodes JANTX quality.

Only JANTX data was available on microwave diodes showing a failure rate of 20 fits.

Insufficient data on Thyristor and Varactor diodes is available for analysis.

TABLE 3.1-1. SOURCE A TRANSISTOR NON-OPERATING DATA

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FAILURE RATE IN FITS	1.93	(<19.59)	(<26.12)	ı	(<78.37)	4.61	4.90	(<78.37)	ı
NUMBER FAILED	N	0	0	ł	0	2	N	0	ł
STORAGE HOURS X 10	1.034	.051	.038	ł	.013	.434	.408	.013	t
NUMBER	70794	3496	2622		874	29716	27968	874	
DEVICE TYPE	Transistors JAN All Data	Silicon PNP (All)	Signal	Power	Switching	Silicon NPN (All)	Signal	Power	Switching

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TABLE 3.1-2. SOURCE B TRANSISTOR NON-OPERATING DATA

							à				
FAILURE RATE IN FITS	1.010	1.633	1.752	(<12.002)	.803	.819	(<20.004)	.816	.930	(<6 ° 668)	(<120.)
NUMBER	IJ	5	N	0	7	7	0	ы	н	0	0
STORAGE HOURS X 10 <sup>6</sup>	4949.075	1224.771	1141.453	83.318	2491.201	2441.210	49.991	1224.771	1074.799	149、972	8.332
NUMP.ER DEVICES	376596	93198	86858	6340	189566	185762	3804	93198	81786	11412	634
DEVICE TYPE	Transistors JANTX All Data	Silicon PNP (All)	Single	Dual	Silicon NPN (All)	Single	Dual	FET (All)	Single	Dual	Microwave Power

TABLE 3.1-3. SOURCE C TRANSISTOR NON-OPERATING DATA

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FAILURE RATE IN FITS	1.13	.75	1.46	(<2.30)	(<2.21)	1.47	1.32	(<4.01)	2.53	(<48.0)	(<22.32)	(<13.95)	(<973.)	10.47
NUMBER	12	Ч	Ч	0	0	ę	4	0	2	o	0	0	0	16
STORAGE HOURS X 10	10662	1327	686	189	452	4076	3036	249	101	21	45	72	Ч	1528
NIJMBER DEVICES														
DEVICE TYPE	Transistors JANTX All Data	Silicon PNP (All)	LOW POWEr	Medium Power	High Power	Silicon NPN (All)	LOW POWEr	Medium Power	High Power	Germanium NPN	Germanium PNP	FET	Unijunction	Transistors JAN All Data

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in starting Starting TABLE 3.1-4. SOURCE D TRANSISTOR NON-OPERATING DATA

DEVICE TYPT	NUMBER	STORAGE HOURS X 10	NUMBER	FAILURE RATE IN FITS
Transistor JANTX All Data		27.342	0	(<36.6)
Silicon NPN (Ali)	547	16.911	0	(<59.1)
Single	315	10.005	0	(<99.9)
Dual	232	6.906	0	(<144.8)
Silicon PNP	239	7.669	0	(<130.4)
Silicon PNPN	30	.562	0	(<1779.)
Unijunction	IO	.317	0	(<3154.)
FET	55	1.883	0	(<531.1)

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TABLE 3.1-5. SOURCE E TRANSISTOR NON-OPERATING DATA

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	STORACTE		F2T1.17PF
	HOURS	NUMBER	RATE
DEVICE TYPE	401 X	FAILED	IN FITS
Transistors JANTX All Data	3.3	0	(<303.)

TABLE 3.1-6. SOURCE F TRANSISTOR NON-OPERATING DATA

FAILURE RATE IN FITS	62.89
NUMBER FAILED	ы
STORAGE HOURS X 10 <sup>6</sup>	15.9
DEVICE TYPE	Transistors JANTX All Data

TABLE 3.1-7. TRANSISTOR NON-OPERATING DATA - ALL SOURCES

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		COMB	COMBINED DATA - ALL SOURCES	ALL SOURC	。 して い い い い い い い い い い い い	
	PARTS	AN PARTS	8 8 8 7 8 7	JANTX PARTS	ANTX PAF	SL
DEVICE TYPE	STORAGE HOURS X 10	NUMBER	FAILURE RATE IN FITS	STORAGE HOURS X 10	NUMBER	FAILURE RATE IN FITS
Transistors All Data	2562.	18	7.02	15658.	18	1.15
Silicon PNF	51.	0	(<19.6)	2559.	m	1.17
Silicon NPN	434.	7	4.61	6584.	80	i.21
Germanium NFN	ı	l	ł	21.	0	(<48.0)
Germanium PNP	I	1	t	45.	ο	(<22.3)
FET	I	1	1	1299.	г	.77
Unijunction	ł	1	1	2.	0	(<500.)
M:crowave Power	I	I	ı	в.	0	(<125.)

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3.1-16

DEVICE TYPE	NUMBER DEVICES	STORAGE HOURS X 10	NUMBER FAILED	FAILURE RATE IN FITS
Diodes JAN				
All Data	146832	2144.	5	2.33
Silicon	67298	982.	0	(<1.18)
Switching	24472	357.	0	(<2.80)
Signal	42826	625.	0	(<1.60)
Zener	16606	242.	0	(<4.12)
Regulator	13110	191.	0	(<5.22)
Reference	3496.	51.	0	(<19.6)

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TABLE 3.1-8. SOURCE & DIODES NON-OPERATING DATA

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### TABLE 3.1-9. SOURCE B DIODES NON-OPERATING DATA

DEVIC: TYPE	NUMBER DEVICES	STORAGE HOURS X 10	NUMBER FAILED	FAILURE RATE IN FITS
Diodes JANTX				
All Data	182592	2399.567	3	1.25
Silicon	152794	2007.971	0	(<.498)
Switching	51988	683.210	C	(<1.46)
Signal	100806	1324.761	0	(<.755)
Zener	13314	174.968	1	5.71
Microwave	7608	99.982	2	20.0
Power	8878	116.646	0	(<8.57)

3.1-17

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TABLE 3.1-10. SOURCE C DIODES NON-OPERATING DATA

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FAILURE RATE IN FITS ----- JANTX -------.37 1.11 (<523.) (<523.) 1 NUMBER FAILED 5 0 O STORAGE HOURS X 10 18761. .838 3 3 1 1 I I I FAILURE RATE IN FITS (<1.65) 5,97 ----- JAN ------6.54 I t ł I I NUMBER 41 41 0 I I STORAGE HOURS X 10 6871. 6264. 607. 1 ł I Switching Regulator Reference DEVICE TYPE Diodes All Data Signal Varactor Silicon Tunnel Zener

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3.1-18

TABLE 3.1-11. SOURCE D DIODES NON-OPERATING DATA

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FAILURE RATE IN FITS	38.6	(<69.4)	87.0
NUMBER	Ч	0	Ч
STURAGE HOURS X 10	25.894	14.403	11.491
NUMBER DEVICES	842	465	377
DEVICE TYPE	Diodes JANTX All Data	Silicon	Zener

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TABLE 3.1-12. DIODES NON-OPERATING DATA - ALL SOURCES

		JAN			JANTX -	JANTX
DEVICE TYPE	STORAGE HOURS X 10 <sup>5</sup>	NUMBER	FAILURE RATE IN FITS	STORAGE HOURG X 10	NUMBER	FAILURE RATE IN FITS
Diodes All Data	9015.	46	5.10	21186.	ΤT	.519
Silicon	7246.	41	5.66	2022	0	(<.494)
Zener	849.	0	(<1.18)	1084.	m	2.77
Tunnel	ı	1	ł	2.	0	(*200•)
Varactor	I	ł	1	2.	0	(<500.)
Power	t	ł	ł	117.	0	(<8.55)
Microwave	I	1	ł	100	7	20.0

#### 3.2 Discrete Semiconductor Operational Prediction Models

The MIL-HDBK-217B general failure rate model for transistors and diodes is:

$$\lambda_{p}^{\cdot} = \lambda_{b} (\Pi_{E} \times \Pi_{A} \times \Pi_{Q} \times \Pi_{S2} \times \Pi_{C}) \times 10^{-6}$$

Where:

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The various types of semiconductors require different failure rate models that vary to some degree from the basic model. The specific failure rate model and the  $\pi$  factor values for each group are shown in figures 3.2-1 thru 3.2-15.

The base failure rate and adjustment factor values presented in the figures are based on certain assumptions. See section 3.2.1 and 3.2.2 for a description of these parameters.

Table 3.2-1 provides a list of the semiconductor generic groups with a cross reference to the corresponding figure number.

3.2.1 Base Failure Rate  $(\lambda_b)$ 

The equation for the base failure rate,  $\lambda_{\rm b}$ , is:

$$\lambda_{\rm b} = {\rm Ae} \left(\frac{N_{\rm T}}{273 \div {\rm T} + (\Delta {\rm T}) {\rm S}}\right)_{\rm e} \left(\frac{273 + {\rm T} + (\Delta {\rm T}) {\rm S}}{{\rm T}_{\rm M}}\right)^{\rm P}$$

Where

A is a failure rate scaling factor.

e is the natural logarithm base, 2.718

 $N_{m}$ ,  $T_{M}$  and P are shaping parameters.

- T is the operating temperature in degrees C, ambient or case, as applicable (see Section 3.2.3 for instructions).
- AT is the difference between maximum allowable temperature with no junction current or power (total derating) and the maximum allowable temperature with full rated junction current or power.

# TABLE 3.2-1DISCRETE SEMICONDUCTOR OPERATIONALPREDICTION MODELS CROSS REFERENCE

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DISCRETE SEMICONDUCTOR TYPE	GROUP	FIGURE #
Silicon NPN Transistors	I	3.2-1
Silicon PNP Transistors	I	3.2-2
Germanium PNP Transistors	I	3.2-3
Germanium NPN Transistors	I	3.2-4
Field Effect Transistors	II	3.2-5
Unijunction Transistors	III	3.2-6
Silicon (General Purpose) Diodes	IV	3.2-7
Germanium (General Purpose) Diodes	IV	3.2-8
Voltage Regulator & Voltage Reference (Temp. Compensated)(Zener, Avalanche) Diodes	5 V	3.2-9
Thyristors	VI	3.2-10
Silicon Microwave Detectors	VII	3.2-11
Germanium Microwave Detectors	VII	3.2-12
Silicon Microwave Mixers	VII	3.2-14
Varactors, Step Recovery & Tunnel Diodes	VIII	3.2-15

3.2-2

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S is the stress ratio of operating electrical stress to rated electrical stress (see Section 3.2.3 for S calculation).

The values for the constant parameters are shown in Table 3.2-2. The resulting base failure rates as functions of temperature and electrical stress are shown for each part type in Figures 3.2-1 through 3.2-15. These failure rates are based on the typical maximum junction temperatures (fully derated) of 100 degrees C for germanium (70 degrees C for microwave types) and 175 degrees C for silicon (15C degrees C for microwave types) as well as a value of 25 degrees C for the maximum temperature at which full rated operation is permitted. If device temperature ratings are different from these values, see Section 3.2.3 for S calculations to compensate for these differences.

The base failure rate tables contain failure rates up to full rated conditions. If a particular operating condition of S and T is high enough to fail into a blank portion of the table, the device is over-rated and should not be used.

3.2.2 I Adjustment Factors

3.2.2.1 Environmental Adjustment Factor, IIE

 $II_E$  accounts for the influence of environmental factors other than temperature. Refer to the environmental description in the Appendix.

3.2.2.2 Application Adjustment Factor, IIA

 $I_A$  accounts for effect of application in terms of circuit function.

3.2.2.3 Quality Adjustment Factor, IIO

 $II_Q$  accounts for effects of different quality. The quality levels (JAN, JANTX, JANTXV) are as defined in MIL-S-19500.

		•		$\lambda_{b}$ Cons			
	Group	Part Type	A	NT	т <sub>м</sub>	P	ΔTT
Tra	insistors						
		SI, NPN	0.13	-1052	448	10.5	150
	I	SI, PNP	0.45	-1324	448	14.2	150
	Ŧ	Ge, PNP	6.5	-2142	373	20.8	75
		Ge, NPN	21.	-2221	373	19.0	'75
	II	FET	0.52	-1162	448	13.8	150
	111	Unijunction	3.12	-1779	448	13.8	150
Dio	des						
	IV.	Si, Gen. Purp.	0.9	-2138	448	17.7	150
	<b>IV</b> .	Ge, Gen. Purp.	126	-3568	373	22.5	75
	v	Zener/Avalanche	0.04	-800	448	14	150
	VI	Thyristors	0,82	-2050	448	9.6	150
		Microwave					
		Ge, Detectors	6.33	-477	343	15.6	45
		Si, Detectors	0.14	- 392	423	16.6	125
	VII	Ge, Mixers	0.56	-477	343	15.6	45
		Si, Mixers	0.19	-394	423	15.6	125
		Varactor,					
<b>^</b>	VIII	Step Recovery & Tunnel	.93	-1162	448	·13.8	150

## TABLE 3.2-2DISCRETE SEMICONDUCTOR BASE FAILURE RATE PARAMETERS

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3.2.2.4 Voltage Stress Adjustment Factor, II S2

 $II_{S2}$  adjusts the model for a second electrical stress (application voltage) in addition to wattage included in the base failure rate,  $\lambda_b$ . The voltage stress, S2, is defined as:

$$S2 = \frac{\text{Applied (V_{CE})}}{\text{Rated (V_{CEO})}} \times 100$$

3.2.2.5 Complexity Adjustment Factor, IIC

an markatak di seberah kising pangkanaking marka walaran di siban inin mananar wan din. Ban hising king bing bi

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 $I_{\rm C}$  accounts for effect of multiple devices in a single package. Each transistor in a case must be treated individually for complexity factor. Its failure rate,  $\lambda_{\rm b}$ , modified by other I factors and then multiplied by this complexity factor. If only one transistor of a pair is used, treat as an independent item with  $I_{\rm C} = 1.0$ .

FIGURE 3.2-1 MIL-HDBK-2

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR SILICON NPN TRANSISTORS

 $\lambda_p = \lambda_b$  (  $\pi_E \times \pi_A \times \pi_Q \times \pi_{S2} \times \pi_C$  ) × 10<sup>-6</sup>

λ<sub>h</sub> (Base Failure Rate)

																	~	-				_									-	
Г	С	œ	<u>ო</u>	6												100×+	0 LL GUD		3	ر- در-	N	• •	2	٠	2	•	5	4.	<b>с</b> .	0.30	<b>.</b>	<b>۳</b>
	E		2	02	03			2									0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			t)												
ŀ	6		r d	.020	3	2	ŝ	\ 	\	7						(VOI +a	"S2 / VUL LAGE O	5	2 2 2	(percent			δ							20		0
	ß		10	.015	5	깅	02	02	03				7			E	S"	i.				l			Or)							
	10	.0095	r-1	.012	Ч	깅	-	2	2	2	2	n			\	7									Y Factor		L L		.2	.4	3	e
Vare	s kat	6	0	.010		님	-i	Ч.	Ч.	-	2	2	2	2	m				7					7712	<sup>11</sup> 0 (UUALITY		ATTANA	тәла	UXTNAU	ANTX	JAN	ower
	stres	90	07	.9984	08	60	-1	5	5	-	5	10	-	03	2	$\mathbf{N}$	N	က						F	ο ≓			ī	5	5	5	<u>Ă</u>
3 2000	4	05	06	00	07	5	80	1	-	Ч.	5	T	1	-1	L,		2	2	N	N.	3											
a c	6	04	05	.0060	06	90	07	80	80	60	-		-	5	H.	-	5	Ч	01	2	02	02	2	3								
	-2	40	04	.0051	05	05	06	07	07	07	08	08	60	Ы.	-		-		01	1	-1		2	$\mathbf{N}$	$\sim$	2	$\mathbf{n}$					
	1.	6	003	.0043	04	004	005	06	06	06	002	07	07	08	08	09	<b>H</b>	Ч	H.	Ч		.014	L I	1	L.	2	2	2	2	m		
			10	20	25	30	40	50	55	60	63	70	75	80	85	90	95	0	0	110	-	120	2	n	ŝ	4	4	S	155	ပါ		

 $\pi_{\mathbf{E}}$  ( rironmental Factor)

	лЕ		25	2	2	40	ົີ
1	Environment	Ground, Benign Space Flight Ground, Fixed	irborne, Inhabited aval. Sheltered	round, Mobile	aval, Unsheltered	Airborne, Uninhab. Missile. Launch	<pre>nc (Complexity Factor)</pre>

0	1.0	0.7	٠	8. 0	ר ר	1.2	0.1
comptent of	Single Transistor	Dual (Unmatched)	Dual (Matched)	<b>Larlington</b>	Dual Emitter	Multiple Emitter	Complementary Pair

Π<sub>A</sub>(Application Factor) Application Π<sub>A</sub>

Application IIA Linear 1.5 Logic Switch 0.7 High Frequency 5.0 (R.F. >400 MHz) 1.1.2.3

MIL-HDBX-217B OPERATIONAL FAILURE RATE MODEL FOR SILICON PNP TRANSISTORS FIGURE 3.2-2

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 $\lambda_{p} = \lambda_{b} ( \pi_{E} \times \pi_{A} \times \pi_{Q} \times \pi_{S2} \times \pi_{C} ) \times 10^{-6}$ 

)r)	ы Ц	-1		ົດ ເ ເ	20	25	25	25	40	40				L L	J.	•					10											
Environmental Factor	Environment	Ground, Benign	н.	Ground, Fixed	С Н	U2	•	N.	à	Missile, Launch	•	(Complexity Factor)	- 1	Complexity	. 1	Single Transistor	Dual (Unmatched)	Dual (Matched)	<b>H</b>		Multiple Emitter	COMPLEMENCALY FALL			10.01 i t t	I (MATTER FACENT)	Quality n	Level "Q	JANTXV .2	•	٠	Lower 10.0
n <sub>E.</sub>		1.0	030	, C	500	.063						=	Ŧ				Stress				<sup>n</sup> S <sub>2</sub>		3.0	2.25	ŝ		_	0.75	0.48	00		0.30
		6	22	120.	40	ъ I	.045	.063	\ 	\	7						(Voltage	Factor)		20 0	(percent)		100	06	80	70	60	50	40	000		0
		• 8	-1 (	NO	N	027	m	039	n I	0.063		Ì		7			ŧ	11 S.2	L						г) г)			10		0		d
		.7		.016	610.	.021	.022	.027	.034	•039	.045	500.	.063				7								Factor		ПД		0.7		()	
Rate)	io		.012	.013	.015	.016	.018	.021	024	.027	.030	.034	.039	.045	.053	.063				7					polication		rion		Switch	Couenca	. >400 MHz)	
lure Re	ss Ratio	•	010.	$\mathbf{c}$	0	0	Oi	0	$\mathbf{c}$	0	.022		C) (	<b>(</b> )	0	0	$\mathbf{O}$		0			7			Appli		plication	near	U V	High Fre	5.	
e Fai	Str		0	600	L L	d C	5	L L	H C	H C	I 1	레	02	02	20	00	EO	EO	eo	04	.053	ωi			_ _	<b>4</b>	App	F	<u>i</u> <u>i</u>	H	5	
AL (Bas		с.	5	$\circ$	δ	60	5	10	5	5	-	립	5	5	5	02	02	02	07	EO	.034	8	<"	50	ഗ	\ 	7	7				
~		.2	S	$\sim$	2	õ	80	60	01	5	5	김	10	5	5	5	5	5	02	03	.624	20	<b>~</b> .	e O	e o	4	ഗ	S O		7		
			004	$\sim$	006	006	007	008	600	600	5	5	01	5	ธ	5	10	6	5	5	.019	03	02	07	02	0	0	11.3 .	00			
			6	20	20	25	30	40	50	່ເບ ເບ	60	65	20	75	80	85	60	95	0	0	110		N	2	ന	C	<b>. .</b> .	4	u i	n d		

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1. J. S. S. See.

FIGURE 3.2-3 MIL-HDB

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR GERMANIUM PNP TRANSISTORS

 $\lambda_p = \lambda_b$  (  $\pi_E \times \pi_A \times \pi_Q \times \pi_{S2} \times \pi_C$  ) × 10<sup>-6</sup>

λ. (Base Failure Rate)

m_ (Environmental Factor)		Environment II.	l, Benign		e, Inhabited 2	Naval, Sheltered 25 Ground, Mobile 25	Unsheltered 2	Airborne, Uninhab. 40 Missile, Launch 40	<pre>If (Complexity Factor)</pre>		Complexity IC	le Transistor 1.	•	ਂਸ	tter 1.	ter 1.	ementery rait 0.		II (Quality Factor)	14+ Leno	Level <sup>II</sup> O		•	er 10
		1.0	010	$\mathbf{o}$	- 031 - 031	.056					Stress			IIS <sub>2</sub>		0, 0	•	50	0,1	n a	r	0.30	ຳຕໍ	
		6.	.013	1	$\alpha$	vim.	.047				(Voltage	actor)		(percent)		00		00	0	<b>5</b> c	00	0	0	
		. 8	110-	0	$\circ c$	.025	1031	0	Ž		л <sub>S2</sub> (Vo	14 1	, S	(per	- 14		n α	<u>,                                    </u>	<u> </u>	0 4	r	0 r		
		1.7	.010	5	.013	.018	.022	.035	<u>۱</u> ۱	7		•						Factor	ПЪ	1.5	0.7	5.0	]	
kate)	tio	• 6	0600.	0	- 017	.015	020	025	10 C	000.								pplication	uo		tch	Frequency >400 MH%)		
Jure	ss Ra	•	.0067	.0084	600	.012	.016	018	.027	. C . J	.047							(Applic	lication	ear				
ase rai	Stre	4	000	002	800		50	.015	02		e c	។ ហ	1						App	Lin	Log	High (R.F		
v <sup>b</sup> d (b		3	$\circ \circ$	05	000	008	010 010	.012	10	-1 0	2 0	s m	1						~					
		2	$\circ \circ$	04	0 2 0 2	007	α 0 0	010	50	7 r 5 c	ょう	021	m.	4' S	1									
			m m O O	04	004 005 005	005	000	.0084	010	1,		1	03	2 0	04	Í								
	۲-		0 0		ນ ຕ		ວ ທີ	40 45	0 1	n d	יו כ	0	10		0									

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR GERMANIUM NPN TRANSISTORS FIGURE 3.2-4

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= λ<sub>b</sub> ( Π<sub>E</sub> X Π<sub>A</sub> X Π<sub>Q</sub> X Π<sub>S2</sub> X Π<sub>C</sub> ) X 10<sup>-6</sup> م ۲

Data Data (Base Failure 5

In (Environmental Factor)	Environment	E.	l, Benign	rrðuc	xed	ne, Inhabited 2	sheltered 2	-	sheltered 2	rborne, Uninhab. 4	MISSILE, LAUNCH 40	<pre>nC (Complexity Factor)</pre>		Du Katty IIC	л ло		nea) 1.	Dual Emitter 0.8	inle Fmitter	bilt tet T	CINCILLAT Y			<pre>n (Quality Factor)</pre>	Ouality	Level ID	TANTAVI	DANTX		LOWER 10.0
		1.0	.046	.055	.067	.083	1.10	.14		7					stress	F		IIS,	7	3.0	2	1.65	1.2			0.48			•	
		6.	.036	.042	.050	.060	074	.095	.12		7				Factor)			(percent)					_		_	-				
		. 8	.029	.034	.039	.046	.055	.067	.083	.10	.14	7			<sup>II</sup> S2 <sup>V</sup>		s S	(perc		100	6	8	20	9 i				10		
Rate)		6.	.024	028	032	.036	.042	.050	.060	.074	.095		7									Factor)		LA L	1.5	0.7	5.0 0	7		
Lure Ra	Ratio	9.	.020	.023	.026	.029	.034	.039	.046	.055	.067	.10	,14		7							ation F		c		tch	uency	MHz)		
e Fail	ress R	5	10	5	2	02	03	6	03	04	.050	610	60	N	· /	1						(Applica	ŀ	lcation	ar	ĬWİ	50	6		
b (Basi	+	.4		н.		2	N	$\sim$	02	бÖ	.039	വവ	ശ	8	0 5		7					П <sub>А</sub> (А		Tddy	Line	Logic	High	H H		
۲		•1		-	Ч.	-	-1	$\sim$	2	2	.032		ິ	Ø	P C	אות														
		•	0	-1	01	07	5	1	02	02	.026	m.	03	04	24 :	20	<b>C</b> r	27.	4 \	7										
		-	0	080	01	01	5	07	01	5	021	5	m	$\mathbf{m}$	0 C	3	7 Q	> σ	50	1										
	Еч С			<u>ה</u>	10	5 	20	25	8	35	4 4 0	50	÷ S S	0.0	0 C			ວ ທີ		2										

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FIGURE 3.2-5

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR FIELD EFFECT TRANSISTORS

=  $\lambda_b$  (  $\pi_E$  X  $n_A$  X  $\pi_Q$  X  $\pi_C$  ) X 10<sup>-6</sup> م م

II <sub>E</sub> (Environmental Factor)	Environment II	Ξ	~	- Fixed	2	ltered	, Mobile	sheltered	, Uninhab.	MISSILE, Launch 40			I <sub>C</sub> (Complexity Factor)	$\left  \right $		1.	Jnmatched) 0.	(Matched)	mplementary 0.	Tetrode 1.1			II. (Application Factor)		Application n <sub>a</sub>	T.inear	Logic Switch 0.7	Frequency	. >400 MHZ)	
e )		.7 .8 .9 1.0	6 - 03	V 0.36 0.04/	0.00	052 076	.066	.088		.076	88	10										Π <sub>&lt;</sub> (Quality			Yualiy I	A Tavar	JANTXV .2	LX X	LAN 2.0	
ilure Rate	atio	• 9 •	†	<u> </u>			Γ			.052 .0		ŀ	.076	.088	.10	<b>``</b>														
() ()		•	610	120	240	026	629	03	03	03	04	047	052	058	66	~	0	.10				2								
λ <sub>b</sub> (Base	ţ	•	-016	102	2 0	02	02	02	02	S	е О	03	бO	04	04	05	05	06	07	ω	.10			7						
		•	1013			10	02	02	02	02	02	02	603	03	03	03	04	04	05	05	06	07	$\infty$	Ē			Δ			
		•		1 r 5 c	-	5	5	03	02	02	20	02	02	02	02	03	03	03	03	04	04	5	ດ 2	5	~	m		/	7	
		1.	1.0092	-1 r			-	10	<del>, 1</del>	-1 ·	21	$\sim$	03	02	$\sim$	N	$\sim$	02	$\mathbf{c}$	03	$\mathbf{m}$	m	-	5	10	10	0	$\sim 0$	. 088	
	E1 C	ິບ 2				30	40	50	55	09	65	0/	75	80	85	90	5	0	0	-1		2	2	S	S	4	4	ហ	2 2 1 2 0 9 1	

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR UNIJUNCTION TRANSISTORS FIGURE 3.2-6

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 $\lambda_{\rm P}$  =  $\lambda_{\rm b}$  (  $\pi_{\rm E}$  x  $\pi_{\rm Q}$  ) x  $10^{-6}$ 

(Base Failure Ra

(Environmental Factor)	Environment I		Benign icht	Ground, Fixed 5	rne, Inhabited 2	Sheltered 2	, Mobile 2	א א ש	, υπ <i>±</i> ππα <b>υ</b> . 4 Tannch Δ				T (Oislitu Factor)			Level "Q	TANTY O	• 	-i a									
а п		1.0	.073	- 095 - 13	.15					]																		
		┝	39		64 0.0	73  .1	1. Seo	13	15	7	$\mathbb{N}$																	
ce Rate)		- <u>-</u> -	1	043			.064 .	.083	.095	101	.15		\	/	7													
Failure	Ratio	• 6	.024	.033	.036	.039	.047	.058	.064	.083	.095	.11	.13	.15				7										
(Base	ខន	.5	610.	.026	.028	.031	.036	.043	.047	.058	.064	.073	.083	.095	.11	[]	.15				k							
۹	Stre	4	-015	1 N	02	2	02	ဗီဝ	n c D c	20	2	SO	02	06	07	80	60	Ц	-	-								
		•	.110.	.016	5	깅	02	020		n n o	03	03	04	04	05	50	06	07	80	60	H.	.13	H			Ν		
		•	• 0088	.012	10	깅	10	02	2 6	201	02	63	03	03	03	04	04	05	05	9	2	ωd	5	.11	.13	.15		
		-	.0064	200 000	-	리	50	50	15	1 🔿	02	02	02	02	80	03	03	03	04	04	05	ы О	06	07	08	60	-	
	EH C		0 0	2 C 7 F	25	0	0	0.	ດ ຕ	ເມ	0	ហ	0	ы	0	95	8	0 20	50	15	20	20 20 20	202	35	40	45	01	

MIL-HDEK-217B OPERATIONAL FAILURE RATE MODEL FOR SILICON (GENERAL FURPOSE) DIODES FIGURE 3.2-7

 $\lambda_p = \lambda_b$  (  $\pi_E \times \pi_A \times \pi_Q \times \pi_{S2} \times \pi_C$  ) × 10<sup>-6</sup>

II <sub>E</sub> (Environmental Factor)	Environment N <sub>F</sub>	Renian		birbound, rixed	Alliaut Leo al tered	d Mobile	Unsheltered	ne, Uninhab.	Launch		T (Annlication Factor)		Application RA		Switching	Rectifier 1.	(>500ma)	Power Rectifier 2.5/		>600	lildx		Ne. (Voltage Stress Factor)	S,	ent)		70 00	0.8	90 0.0	
Rate)	Ratio	1.7 .8 .9 1	33 .0043 .0057 . 39 .0052 .0072 .	.0047 .0064 .0095 .0	0052 0072 011 00	.0057 .0082 .01	1.0072 .01	0095 0.01			10	13	.016	.020 - /	-				Quality n.	Level V	JANTXV .5	JANTX 1.0		LOWER 25.0	II <sub>C</sub> (Construction Factor)	+ Construction		Metallurgically Bonded	Non-Metallurgicaíly Bonded (suring loaded contacts)	TOALCT
Failure I	tress	•	14 .0019 17 .0023	1.000	3 .00	5 1.00	00.00	6  .00	۲. د ا		2 1.00	7 1.00	4 00	2 01.	2 1.0	5 . OL	•		\ 	0						N		<b>A</b>		
λ <sub>b</sub> (Base		_	00 0100 00 0100	0016 .0	017  .0	0.1 0100	0023 .0	027 1.0		0.135 0.0	0.999 0	0043 .0	047 .0	0052 .0	0057 .0	054 .0	0072 .0	0082 .0	0.95 .0	11 1.0		-H (	N	\.						
			7000. 7000	20	10	0	10	00	200		200	003	003	003	004	04	02	00	0	0	08	60,	-1 -		10			7		
		.1	.0006 20006	000	000	100	100	100	100		002	002	002	003	003	003	003	004	004	005	005	000		οσ		.013	.016	) ) ) )		
		(0)	00	0	ۍ د	0	0	01	ົບ	ວນ		<b>ა</b> თ	0	ഹ	0	95	00	05	5	1.5	20	50	ם ה כ	0 A	145	5	ŝ	o I		

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(a) A set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the se

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FIGURE 3.2-8

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR GERMANIUM (GENERAL PURPOSE) DIODES

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 $\lambda_p = \lambda_b$  (  $\pi_E \times \pi_A \times \pi_Q \times \pi_{S2} \times \pi_C$  )  $\times 10^{-6}$ 

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	ц <sub>С</sub>	10
IIC (Construction Factor)	Contact Construction	Metallurgically Bonded Non-Metallurgically Bonded (Spring loaded contacts)

ntal Factor)

ਮ ਜ	ΠE
Ground, Benign	۲
Space Flight	Ч
Ground, Fixed	ហ
Airborne, Inhabited	
Naval, Sheltered	
Ground, Mohile	25
Naval, Unsheltered	
Airborne, Uminhab.	40
Missile, Launch	40

on Factor)

mall Signal(≤500m≥) 1.0 mall Signal(≤500m≥) 1.0 ogic Switching 0.6 ower Rectifier 1.5 (>50ma) cwer Rectifier 2.5/ (H.V. Stacks) junct		10+1 0×	F
Signal (<500ma) 1 Switching 0 Rectifier 1 Rectifier 2 V. Stacks) june	1 + + 4 4	a ct Oll	۲ ۲
Switching Rectifier 1. (>500ma) Rectifier 2. V. Stacks) jund	mall	Signal (<500m2)	1.0
Rectifier 1. (>500ma) 2. Rectifier 2. V. Stacks) junc	ogic	Switching	0
(>5COma) Rectifier V. Stacks) junc	ower	Rectifier	ч
Rectifier 2. .V. Stacks) junc 2. >600		(>5C0ma)	
V. Stacks) Junc v >600	cwer	Rectifier	-
>600	(н.	-	unct
	V ma	>600	

IIS2 (Voltage Stress Factor)

ent.) $n_{S_2}$	60 0.75 0.75 0.80	•
s <sub>2</sub> (percent	0 to 70 80	

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FIGURE 3.2-9

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR ZENER AND AVALANCHE DIODES

 $\lambda_p$  =  $\lambda_b$  (  $\pi_E \propto \pi_A \propto \pi_Q$  ) x 10<sup>-6</sup>

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If (Environmental Factor)	-	<b></b>	, , , , , , , , , , , , , , , , , , ,	40	d. Mobile	Unsheltered 2	, Uninhab. 4	Missile, Launch 40			II (Application Factor)	01; cation			Voltage Negulatoli 1.01	c relefence L	(TEMP. COMPONSATED)			T (Out fits Factor)			-+	>	JANTX 1.0	or	1
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		.0073	.0079	.0086	.0094						7																
e)	1	2 .0061 0 .0058								.018				4													
te Rate)	-11	0052									10.	101	.01				7										
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e i		.0036 .0039	004	004	004	002	200 200 200	000	006	90	002	002	008	600	10	5	5	r-1 r	빐								
, <sup>q</sup> γ.		.0032 .0035	003	003	004	004	0 C 4 R	002	005	005	000	000	000	007	200	008	600	Ч,	ᆀ	1 6		l )		Ν			
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L.		00	20	25	30	40	ວ ແ ເກ ແ	000	<del>ر</del> ان	0	- 1 - 1 - 1 - 1 - 1	02	85	60	6	0	0	110	-10	N (	7 10	) m	) 🦛	4	5	5	0

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MIL-HDBK-217B CPERATIONAL FAILURE RATE MODEL FOR THYRISTORS FIGURE 3.2-10

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$$\lambda_{p} = \lambda_{b} ( \pi_{E} \times \pi_{Q} ) \times 10^{-6}$$

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II <sub>E</sub> (Environmental Factor)	Environment	Ш	-	Ground, Fixed 5	ne, Inhabited 2	Sheltered 2	, Mobile 2	Isheltered 2	rborne, Uninhab. 4	MISSILE, LAUNCH 40					T (Ouslitu Factor)		Quality	[revel 1 "O	-		XI		0.c2 Tewor							
		1.0	110	014	.022		Ν																							
		6.	0,	010	c	.017	.022	- <b>-</b>			7																			
		8.	* 0059 * 0059	2/00.	010	110.	.014	.019	.022																					
Rate)		<i>.</i>	2	.0065						.017	.019	.022																		
Failure	Ratio	9.	.0033	.0048	.0053	.0059	.0072	0600.	.010	.011	.012	.014	.017	.019	.022															
se	ess Ra	2	õ õ	.0036	$\sim$	$\sim$	i C	0	0	0	$\mathbf{C}$		C	$\mathbf{c}$	63			-	4			X								
λ <sub>b</sub> (Ba:	Str	.4	0018	027	0030	0033	0039	0048	0053	0059	0065	0072	0081	0090	oro	011	012	014	5	d	02				•					
		• 3	0013	020	0022	0024	0030	0036	0039	0044	0048	0053	0059	0065	0072	0081	0600	10	011	12	14	H	H.	N	1		N			
		.2	6000	015	9100	0018	022	0027	0030	0033	0036	0039	0044	0048	053	0059	0065	07	008	60			1	1	1	-				
		.1	.0006	>	- <del></del>	100	-1	002	002	005		003	003	003	C 0 3	004	004	005	S	000	2	008	000	5	.011	10	.014	50	00	0.22
	EI C	(C) )	00	0, C) 4 N F	l 25	30	40	50	ີ	60	65	70	75	80	85	90	σ	0	0	Ч	H	2	2	n	n	4	4	ŝ	155	و ا

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR SILICON MICROWAVE DETECTORS FIGURE 3.2-11

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 $\lambda_p = \lambda_b$  (  $\pi_E \times \pi_Q$  ) × 10<sup>-6</sup>

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Factor)		មា ដ	-1		0	50	50	50	50	80	200							ਜਿ						•						
II <sub>R</sub> (Environmental Fac	Enui ronment		Ground, Benign	Space Flight	Ground, Fixed	54		Ground, Mobile	Naval, Unsheltered		Missile, Launch							In (Quality Factor				JANTXV   1.0	JANTX 2.0		Lower 5.0					r
		1.0	.075	.082	.092	1.10	.12	.15																						
		6.	062	.066	.072	.078	.087	.098	.11	.13			N																	
		8.	.055	.057	.060	.064	.069	.075	.082	.092	.10	.12	.15																	
Rate)		. 7	.050	.052	.054	.056	.059	.062	.066	.072	.078	.087	.098	.11	.13															
ailure Ra	io	• 6		.048	.049	.051	.053	.055	.057	.060	.064	.069	.075	.082	.092	.10	.12	.15												
Гч O	ນ ຮ		.044 .0.	õ	õ	ပိ	ò	õ	ö	ä	.056	õ	ő	õ	0	0	õ	ö	Ч	Ч										
Ab (Bas	Stre	4	.042	4	4	4	04	04	04	04	.051	05	05	05	06	06	06	07	08	60		<b>H</b>	-							
~			.039	4	4	4	04	04	04	04		04	S	05	05	S	S	0	06	7	7	8	σ	.11	.13					
				03	03	04	04	04	04	04	04	04	04	04	04	05	05	05	05	c 0	06	06	07	08	60		T	.15		
			035	36	037	038	038	039	040	041	42	043	044	045	046	047	049	020	05.2	054	056	059	062	066	072	78	087	b S	11.	
	Ē	(ບ <sub>ິ</sub> ງ)]	0	ທ 	10	15	20	25	30	3 U	40	45	50	55	60	65	70	75	80	85	60	95	0	Ο	-	Ч	2	2	130	$\mathbf{m}$

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR GERMANIUM MICROWAVE DETECTORS FIGURE 3.2-12

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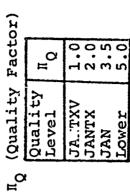
 $\lambda_{\rm p}$  =  $\lambda_{\rm b}$  (  $\pi_{\rm E} \ge \pi_{\rm Q}$  )  $\ge 10^{-6}$ 

λ<sub>b</sub> (Base Failure Rate)

		1.0	.10	<u>.</u>	.12	.14	.17	.22	7							
		6.	.092	.10		.12	.15	.18	.22							
		• 8	.085	.092	.10	.11	.13		.18							
		.7	.080	.086	.093	.10	.11	.13		.18						
	io	• 6	.076	.081	.087	.094	.10	, II	.13		.19	.24				
	ss Ratio	.5	.072	.076	.081	.087	.095	.10	11.	.13	.16	.19				
	Stress	.4	• 069	.072	.077	.082	.088	.096	.10	.12	.13	.16	.20			
Q		• 3	.066	.069	.073	.077	.082	.089	.097	.10	.12	.14	•16	.20		
		. 2	.063	.066	.069	.073	.078	.083	.089	.098	.10	.12	.14	.17	.21	
			.061	.064	.066	.070	.074	.078	.083	060.	.099	.11	.12	.14	.17	.21
	6-1	( <sup>0</sup> 0)	0	5	10	15	20	25	30	35	40	45	50	55	60	65

R<sub>E</sub> (Environmental Factor)

Environment	$\pi_{E}$
Ground, Benign	1
Space Flight	Ч
Ground, Fixed	10
Airborne, Inhabited	50
Naval, Sheltered	50
Ground, Mobile	50
Naval, Unsheltered	50
Airborne, Uninhab.	80
Missile, Launch	200



MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR SILICON MICROWAVE MIXERS FIGURE 3.2-13

 $\lambda_{p} = \lambda_{b} (\pi_{E} \times \pi_{Q}) \times 10^{-6}$ 

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IE (Environmental Factor)	Environment		Space Flicht		/ FIXEU	Innapited	snettered	Marina Mobile 50	nsneltered	aD.	Sette, Launch [2						H (Ouslitu Bactor)	i t	$ $ 2uality $ _{\pi}$	Level "Q			JAN 3.5	2 						
		1.0	01.	- 11	.12	.14	.16	.20	7																					
		• •	•086	.092	.099	.10	.12	.13	.15	.18			Ν																	
		. 8	•076	. 610.	.083	.089	.095	01.		.12			.20																	
(ə:		. 7	• 069	.071	.074	.077	.081	.086	.092	.099	.10	.12	.13	.15	.18															
ailure Rate)	Ratio	•6	.064	.066	.068	.070	.072	.076	.079	.083	•089	.095	.10	.11	.12	.14	1.16	, 20		7										
e Failt	ess Rat		090															.13												
(Bas	Str	4	.056	02	05	90	9	90	90	90	7	07	07	07	ω	08	5								7					
٩			0	O V	05	05	05	06	36	90	9	06	90	01	01	07	08	08	σ	60	Ч	<b>H</b>	•13	-1	Ч					
		.2	0	03	S	05	05	05	05	05	9	06	90	06	06	07	07	2	07	08	08	09	.10							
			4	4	S	ഹ	ഹ	S	05	ហ	05	ខ	9	90	06	9	06	06	7	0	7	8	.086	5	S	.10	.12	.13		07.1
		ິບ ຄູ	0	ლ 	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90	95	0	0	1	1	2	$\mathbf{N}$	130	າ

(TEN) CONT

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR GERMANIUM MICROWAVE MIXERS FIGURE 3.2-14

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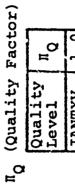
.

 $\lambda_p = \lambda_h$  (  $\pi_E \times \pi_Q$  ) × 10<sup>-6</sup>

пЕ	ſ	1.0		.18 Spac		.25		.37 Grou	Vava Nava	Airb	τw	B				
		6.	1.15		1.19	2	.25	. 30	.38							
		. 8	1.14	.15	1.17	.19	.22	.25	.31	.39	1					
ate)		.7	1.13	.14	.15	.17	.19			l.32		7				
Failure Rate)	i o	• 6	1.12	.13	.14	.16	.17	1.19	.22	.]6	.32		7			
se Fai	ss Ratio	•	1.12		.13	.14	.16	.17	.20	.23	.27	.33				
λ <sub>b</sub> (Base	Stres	• 4	11.	.12	.13	.13	.15	.16	1.18	.20	.23	.27	.34			
		• 3	1.11	.11			.14	.15	.16	.18	.20	.23	.28	.35		
		.2	.10	.11		.12	.13	.14	.15	. i 6	.18	.20	.24	.29	.36	/
			01.	.10			.1		<u>н</u>		<u></u>	<u> </u>	.21	.2	5	•
	E-C	ί Σ	0	<u>ທ</u>	0	1.5	20	25	30	35	40	45	50	22	00	50

(En 'ironmental Factor)

Ervi ronment	រ ម
Benign	7
ight	Ч
Ground, Fixed	10
, Inhabited	50
Sheltered	50
Mobile	50
Naval, Unsheltered	50
, Uninhab.	80
Launch	200



0000 0000 JANTXV JANTX JAN Lower A. 1

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR VARACTORS, STEP RECOVERY & TUNNEL LIODES FIGURE 3.2-15

 $\lambda_{p} = \lambda_{b} (\pi_{E} \times \pi_{Q}) \times 10^{-6}$ 

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II <mark>E</mark> (Environmental Factor)	Environment I.		Space Flight 1	1, Fixed	rne, Inhabited 2	Snettered 2	Navel Thebeltown 22	Ullsliet Lefed Z		7 - <b>Maullon</b>							"O NUALLEY FACEUL)	Quality	Level "Q	JANTXV 5			Lower 25.0						
		1.0	.093		.18																								
		6.	.070		.11	.13	.18			7																			
		. 8	.056	.072	.084	.093	.11	.15	.18				7																
Rate)		.7	.047	.061	.065	.070	.084	.10	.11	.13	.15	.18		\		<b>X</b>													
Failure R	cio	• 6	.040	.050	.053	.056	.065	.077	.084	.093	.10	.11	.13	.15	.18			7											
۵ ۵	ຮ	•	юc	7 7	04	04	05	06	00	010	5	08	60	-	н	H	H-	Ч	\ 		7								
b (Basi	Stre	4	.028	ი ო	03	04	04	05	SO	0	00	00	07	07	08	09	-+		Ч	-				7					
^		•	.024	<b>v</b> m	03	03	03	04	04	40	02	05	05	Q	00	07	07	08	60		-1	1	1	4					
		.2	.020	.025	02	02	03	03	03	04	04	04	50	05	05	05	90	06	07	07	80	60	01	.11	.13	.15	.18		7
		• 7	þc	2010	02	02	02	03	03	e o	03	63	04	04	04	04	02	05	05	06	80	07	0	80	60		1	-	.18
				2 C 7 F 7 F	25	30	40	50	55	60	65	07	75	80	85	90	95	0	0	- H	-4	2	2	က	n	4	4	ທ ເ	160 160

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فتحت للافعالي المتحالمين ومرابكته فحثم فترس الكافريس الالتصويرا فيلافهم فليتم فالمحال والمناسب فلاليا والمتحدية والمتحد وكالمتحد والمتحد والمتحد والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدين والمحدول والمحدين والمحدول والمحدون والمحدين والمحدول والمحدين والمحدول والمحدول والمحدول والمحدول والمحدين والمحدول والمحدول والمحدول والمحدول والمحدول والمحدول والمحدول والمحدول والمحدول و

3.2.3 Instructions for Use of Semiconductor Models 3.2.3.1 Device Power Ratings

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Semiconductor base failure rates,  $\lambda_b$ , are commonly related to the junction temperature. This junction temperature consists of the heat rise within the device caused by power dissipated in the junction plus the case temperature. In turn, the case temperature is related to the ambient air or to the attached heat sink temperature.

Transistors are normally rated at maximum power dissipation and diodes at maximum current permissible. Certain special-purpose devices are rated at artificial maximum ratings many times higher than normal operating conditions and at rating values which are based on burn-out of the device (e.g., Microwave Mixers).

Some maximum ratings are based on operation at a 25 degree C ambient temperature and others on a 25 degree C case temperature (the latter primarily for power devices used on heat sinks). Usually this double-type of rating is trouble-free as long as the device is used according to the type of rating.

Usually each device is given two rating points. One for maximum permissible junction temperature and the other for the maximum case or ambient temperature at which 100 percent of the rated load can be dissipated without causing the sum of ambient or cas plus internal temperature rise to exceed the specified maximum junction temperature (derating point,  $T_S$ ). As the ambient or case temperature rises above  $T_S$  value, the internal temperature rise and power load must be decreased if the combined temperature is not to exceed the maximum junction temperature. See Figure 3.2-16.

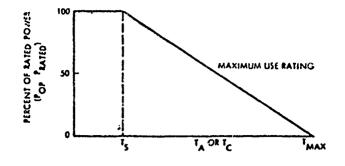


FIGURE 3.2-16 CONVENTIONAL DERATING CURVE

where:

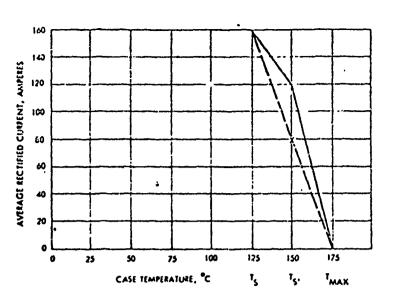
'Г <sub>S</sub>	is the temperature derating point (degrees C)
TMAX	is maximum junction temperature (degrees C)
T <sub>A</sub>	is ambient temperature (degrees C)
тс	is case temperature (degrees C)

Maximum junction temperature  $(T_{MAX})$  is normally 175 degrees C for silicon and 100 degrees C for germanium devices. Usually 25 degrees C, T<sub>c</sub> can be other values of temperature.

Some devices have a multi-point derating curve as shown by the solid line in the example of Figure 3.2-17. The failure rate of a device with multi-point derating can be estimated with the present models by assuming the device to be linearly derated from  $T_S$  to  $T_{MAX}$  as shown by the dashed line. The use of this assumption will result in a predicted failure rate higher than what the device might actually experience, with the amount of error dependent upon the difference between the two rating values where  $T_S$ , intersects the assumed and actual rating plots.

Since semiconductors may be rated based upon ambient or case temperatures, the following guidance is included:

1) When determining failure rate for a device with rating based upon ambient temperature and is used without a heat sink, calculate S per Section 3.2.3.2. Enter base failure rate table with actual operating ambient temperature or a corrected temperature if indicated in Section 3.2.3.2.



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FIGURE 3.2-17 MULTIPOINT DERATING CURVE FOR 1N3263 POWER DIODE

2) When determining the failure rate for a device with rating based on case temperature and is used with a heat sink, calculate S per Section 3.2.3.2. Enter base failure rate table with actual operating heat sink temperature or a corrected temperature if indicated in Section 3.2.3.2.

3) When a device has ratings based upon ambient temperature and on case temperature, it can be used with or without a heat sink. If used with a heat sink, proceed as in (2) above. If used without a heat sink, proceed as in (1).

4) When a device is rated based upon ambient temperature and is used with a heat sink, no failure rate can be determined unless the device rating based upon case temperature can be found. If this cannot be determined, calculate the base failure rate as in (2) above.

5) When a device is rated based upon case temperature and is used without a heat sink, no failure rate can be determined unless the device rating based upon ambient temperature can be found. If this cannot be determined, calculate the base failure rate as in (1) and multiply by 10.

3.2.3.2 Determining Appropriate Stress Ratio & Temperature

The base failure rate tables are based upon ambient or case temperature (T degrees C) and electrical stress ratio (S). The following instructions show the methods for calculating S.

In some cases, the operating ambient or case T must be corrected before entering the failure rate tables. These corrections, where needed, are indicated in (7) below. Operating junction temperatures do not have to be calculated to use the models.

- 1) Groups I, II & III Transistors.
  - a. Single device in case.

For Silicon, 
$$S = \frac{P_{OP}}{P_{MAX}}$$
 (C.F.) For Germanium,  $S = \frac{P_{OP}}{P_{MAX}}$ 

where:

 $P_{OP}$  = actual power dissipated  $P_{Max}$  = maximum rated power at  $T_{S}$ 

C.F.= stress correction factor per (7) below b. Dual device in single case (equally rated).

$$S = \left[\frac{P_1}{P_S} + P_2 \left(\frac{2P_S - P_T}{P_T \times P_S}\right)\right] \quad (C.F.)$$

where:

S = stress ratio of side being evaluated

- P<sub>1</sub>= power dissipation in side being evaluated
- $P_2$  = power dissipation in other side of device
- P<sub>S</sub>= maximum power rating at T<sub>S</sub> of one side of the dual device with the other side not operating (one side rating)
- $P_{T}$  = maximum rating at  $T_{S}$  with both sides operating (both side rating)

NOTE: Specifications for dual devices in one case usually give a maximum rating for each device and a total power rating which is significantly less than the sum of individual ratings.

C.F. = stress correction factor per (7) below for

silicon

C.F. = 1.0 for germanium

2) Groups IV & VI General Purpose Diodes & Thyristors.

For Silicon, 
$$S = \frac{I_{OP}}{I_{MAX}}$$
 (C.F.) For Germanium,  $S = \frac{I_{OP}}{I_{MAX}}$ 

where:

 $I_{OP}$  = operating average forward current  $I_{MAX}$  = maximum rated average forward current at  $T_{S}$ C.F.= stress correction factor per (7) below

3) Group V Zener Diodes

Zener diodes are rated for maximum current or power or both. Either rating may be used as follows:

$$S = \frac{P_{OP}}{P_{MAX}} (C.F.) \text{ or } S = \frac{I_Z(OP)}{I_Z(MAX)} (C.F.)$$

where

 $P_{OP}$  = actual power dissipated  $P_{MAX}$  = maximum rated power at  $T_S$   $I_{Z(OP)}$  = actual operating zener current  $I_{Z(MAX)}$  = maximum rated zener current at  $T_S$ C.F. = stress correction factor per (7) below

4) Group VII Microwave Mixer Diodes

5) Group VII Microwave Detector Diodes  

$$S = \frac{P_{OP} \text{ (Operating Power Dissipation)}}{P_{MAX} \text{ (Rated Power at 25 degrees C)}}$$

6) Group VIII Varactor, Step Recovery, and Tunnel Diodes  $S = \frac{P_{OP}}{\frac{P_{OP}}{P_{MAX}}} (C.F.)$ 

where:

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$$P_{OP} = operating power dissipated$$

$$P_{MAX} = maximum rated power at T_{S}$$
C. F.= stress, correction factor per (7) below
7) Stress Correction Factor (C.F.)
a. Devices with T\_{S} = 25 degrees C + T\_{MAX} = 175 degrees
C to 200 degrees C
C.F. = 1
b. Devices with T\_{S} \neq 25 degrees C + T\_{MAX} = 175 degrees
C to 200 degrees C
C.F. =  $\frac{175 - T_{S}}{150}$ 
c. Devices with T\_{S} = 25 degrees C + T\_{MAX} < 175 degrees C
C.F. =  $\frac{T_{MAX} - 25}{150}$ 

and enter  $\lambda_b$  table with  $T = T_A + (175 - T_{MAX})$ or  $T = T_C + (175 - T_{MAX})$ 

d. Devices with  $T_{S} \neq 25$  degrees C +  $T_{MAX}$  <175 degrees C

$$C.F. = \frac{T_{MAX} - T_{S}}{150}$$

and enter  $\lambda_{b}$  table with  $T = T_{A} + (175 - T_{MAX})$ 

or 
$$T = T_{C} + (175 - T_{MAX})$$

### 3.3 Operational/Non-Operational Failure Rate Comparisons

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# 3.3.1 Transistor Operational/Non-Operational Failure Rate Comparisons

Table 3.3-1 presents a comparison of base (ground), missile launch, and storage failure'rates and their equivalent K factors for JANTX and JAN devices. The active and non-operational failure rates were calculated for a ground, fixed environment using the models in the previous section. For these calculations the following assumptions were made:

Device:	Linear, Single Transistor
Operating Temp.:	25°C
Stress Ratio:	• <u></u> 5
Voltage Stress:	.75 (50% applied to rated voltage)

The comparison indicates factors of 17 to 94 between operating and non-operating failure rates for JANTX transistors and factors of 24 to 92 between operating and non-operating failure rates for JAN transistors.

The Missile, Launch to Ground, Fixed Operating Ratio is "8" as given by MIL-HDBK-217B.

### 3.3.2 Diode Operational/Non-Operational Failure Rate Comparisons

A comparison of operational and storage failure rates and the modifying K factors is presented in Table 3.3-2 for JANTX and JAN devices. The ground and missile launch failure rates were calculated using the procedures of MIL-HDBK-217B. The following assumptions were made:

Device:	Metallurgically bonded, Signal
Operating Temp.:	25°C
Stress Ratio:	.5
Voltage Stress:	.5

The comparison indicates factors of 9 to 50 between operating and non-operating failure rates for JANTX diodes and factors of 10 to 53 between operating and non-operating failure rates for JAN diodes.

3.3 - 1

The Missile, Launch to Ground, Fixed Operating Ratio is "8" as given in MIL-HDBK-217B with the exception of microwave transistors which shows a factor of 20.

2

TABLE 3.3-1. TRANSISTOR OPERATING AND NON-OPERATING DATA

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MISSILE LAUNCH TO G.FOPER- ATING RATIO		α	οα	ο α	з а	ο α	Ø	α	D 00	ۍ «	5 0	ο α
G.FOPERATING TO NON-OPERATING RATIO		17.	24.	23.	- C.	. 46	•	24.	36.	33.	6	92.
GROUND, FIXED, OPERATING FAILURE RATE X 10-9	ž	20.	29.25	27.00	72.00	72.00	• • •	100.	146.	135.	375.	360.
NON-OPERATING FAILURE RATE × 10 <sup>-9</sup>		1.2	1.2	1,2	1.2	.77		4.1	4.1	4.1	4.1	3.9
DEVICE CATEGORY TRANSISTORS	JANTX	Silicon PNP	Silicon NPN	Germanium NPN	Germanium PNP	Field Effect Trans.	JAN	Silicon PNP	Silicon NPN	Germanium 'PN	Germanium PNP	Field Effect Trans.

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3.3-3

TABLE 3.3-2.

DIODE OPERATING AND NON-OPERATING FACTORS

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DEVICE CATEGORY DIODES	NON-OPERATING FAILURE RATE X 10-9	GROUND, FIXED, OPERATING FAILURE RATE X 10-9	G.FOPERATING TO NON-OPERATING RATIO	MISSILE LAUNCH TO G.FOPER- ATING RATIO
JANTX				
Silicon	ň	10.5	21	8
Germanium	υ.	11.5	23	8
Zener & Avalanche	2.8	25.0	თ	Ø
Microwave	19.a	1000.0	50	20
JAN				
Silicon	5.5	52.5	10	8
Germanium	5.5	57.5	10	∞
Zener & Avalanche	2.8	125.0	45	Ø
Microwave	33.0	1750.0	53	20

## 4.0 Electronic Vacuum Tubes

This section contains reliability analysis and data on electronic vacuum tubes.

### 4.1 Storage Reliability Analysis

### 4.1.1 Failure Modes

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A summary of operational failure modes affecting vacuum tubes is shown in Table 4.1-1. Operating hours are not available.

Data storage failure modes is much less extensive. A summary of the failure modes is shown in Table 4.1-2.

### 4.1.2 Non-Operational Failure Rates

A preliminary estimate of non-operating failure rates is shown in Table 4.1-3 for various tube types. The relatively high failure rate for magnetron tubes is based on data which included some operation.

### 4.1.3 Non-Operational Reliability Data

Non-operating data was obtained from five sources and is shown in Table 4.1-4. Note that several different environments are represented. The one source (E) which had no periodic checkout on the tubes shows the lowest non-operating failure rates.

Source D data may not be completely applicable to the missile storage environment since the tubes were conditioned after removal from storage. The conditioning included slow heater warm-up; anode, cathode, and helix conditioning by applying high voltage gradually; and RF conditioning by gradually applying RF drive and increasing it to maximum level and pulse width.

4.1-1

												•			TRANSM.TUBES Ss:répt.)					
			TR RECEIV. PROTECTION	32	ı	11	32	21	1	I	ł	I	4	TYPES 	CEIV. & failure	15	38	15	31	T
BE TYPES	1 1 1 1 1 1		DIODE SERIES CHANGING	I	21	ł	43	15	21	ł	5	ł	ł	TUBE	RE( rept.) (1.3					
FAILURE MODES FOR DIFFERENT TUBE TYPES	1		TETRODE FINAL DRIVER	I	I	I	12	59	29	9	1	ŧ	I	FOR DIFFERENT This Mode	<b>MAGNETRON</b> failures	ı	ı	I	75	25
DES FOR I	Under Th		MIXER OR. DRIVER	I	71	1	14	I	t	I	1	15	ı	RE MODES es Under	rept.) (4					
L FAILURE MO	of Failures Under This Mode	KLYSTRON	MASTER OSCILLATOR	23	ł	5	IJ	1	ł	23	23	I	21	rIONAL FAILURE it of Failures	TWT (1 failure	I	I	t	100	1
OPERATIONAL	Percent		FINAL AMP.	27	16	22	18	Q	1	I	I	1	11	NON-OPERATIONAL	KLYSTRON failure rept.)	100	I	I	ŧ	ł
TABLE 4.1-1.			FAILURE MODE	Low Emission	Incorrect Output	Arcing	Open Filament	Shorted	Gassy	Noisy	No Oscillation	Unstable	Misc.	TABLE 4.1-2.	FAILURE MODE KLYS (1 fai	Open 10	Short	Open heater	Incorrect output	Arcing

4.1-2

TABLE 4.1-3. PRELIMINARY VACUUM TUBE NON-OPERATIONAL FAILURE RATES

<u> x 10<sup>-6</sup></u>	.012	.078	6.410	.826	.012	
TUBE TYPE	Receiver	Klystron	Magnetron	TWT	Transmitting	

à

\*\*\*\* (3) defective; (5) shorts; (2) opens; (1) low gain; (2) open heaters (20 months)

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\*\*\* Open (20 months)

Vibration after field return (12 months); Arcing (15 months); Spectrum too wide (8 months); Moding at start of oscillation (5 months)

No periodic checkout

Storage time 20 months

Missile Storage

0.078

1\*\*\*

12.760

874

1059.113

72542

Transmitting Tubes

(JAN)

Receiving and

Klystron

ы

0.012

13\*\*\*\*

(1967-68)

storage before turn

on.)

(conditioned after

6 to 22 months

Storage time -

Spacecraft orbit-

Standby

Unknown

(<2.439)

0 14 0

0.410

I ł

Sprytron (Hi Rel.)

4

(MIL-STD)

Tubes

TWT

ф

1.017

0.266

18

0.624

124

Magnetron

υ

TWT

0.624

] 24

13.756 (<3.159)

ENVI RONMENT

FAILURE RATE x 10<sup>-6</sup>

STORAGE

NO. OF FAILURES

STORAGE HOURS x 10<sup>6</sup> TOTAL PART

NO. OF UNITS

TUBE TYPE

SOURCE

VACUUM TUBE NON-OPERATING DATA

TABLE 4.1-4.

Periodic checkout

Missile Storage (1963 to 65)-

6.410

**1.663** 

\*\* 4\*

Operating time -1 to 20 hours

2 to 29 months

Shelf Storage

(<3.121)

0

0.320

25

TWT

Ω

(1970-72)

Storage time -

Excessive helix current (5 months)

\*\*

Failure Modes:

4.1-4

### 4.2 Electronic Vacuum Tubes Operational Prediction Model

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The MIL-HDBK-217B failure rate . del for electronic vacuum tubes is:

 $\lambda_{p} = \lambda_{b} \Pi_{E} \times \sqrt{-6}$ where:  $\lambda_{p} = de \times \Rightarrow$  failure rate  $\lambda_{b} = base$  failure rate  $\Pi_{E} = Environmental$  adjustment factor

The values for these parameters are presented in Figure 4.2-1. The base failure rate is valid providing tubes are replaced before wearout.

The environmental adjustment factor accounts for the influence of factors other than temperature. Refer to the environment description in the Appendix. MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR ELECTRONIC VACUUM TUBES Figure 4.2-1

 $\lambda_{\rm p} = \lambda_{\rm b} \pi_{\rm E} \times 10^{-6}$ 

2, (Base Failure Rate)

Tube Type	٩ <sub>۲</sub>
RECEIVER Triode, Tetrode, Pentode Power Rectifier	5 10
KLYSTRON Low Power (e.g. local oscillator) High Power	30 200
MAGNETRON Medium Power ( <1Mw. peak) High Power ( <u>&gt;</u> 1Mw. peak)	70 150
TWT.	30
TRANSMITTINC Triode Tetrode & Pentode	75 100
CRT	15
THYRATRON	50
$\lambda_b$ valid providing tubes are replaced before wearout.	71

II<sub>E</sub> (Environmental Factor)

	<u>ы</u>			_				0		_
	Ш	0	0		9	 9	٠	٠	10.0	
ı ت	Environment	Ground, Benign	Space Flight	Ground, Fixed	Airborne, Inhabited	Naval, Sheltered	Ground, Mobile	Airborne, Uninhab.		. Launch

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4.3 <u>Operational/Non-Operational Failure Rate Comparison</u> Table 4.3-1 presents a comparison of operational and non-operational failure rates. The operational, ground fixed, failure rates were obtained from the MIL-HDBK-217B model assuming low power or medium power tubes as applicable.

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The missile launch to ground, fixed operating ratio was obtained directly from MIL-HDBK-217B.

TABLE 4.3-1. VACUUM TUBE OPERATING AND NON-OPERATING FACTORS

MISSILE LAUNCH TO G.FOPER- ATING RATIO	8 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0
G.FOPERATING TO NON~OPERATING RATIO	420 380 11 36 62500
GROUND, FIXED, OPERATING FAILURE RATE x 10-9	5000 30000 70000 30000 750000
NON-OPERATING FAILURE RATE x 10-9	12 78 6410 826 12
TUBE TYPE	Receiver Klystron Magnetron TWT .Transmitting

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5.0 Resistors

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Resistors used in electronic equipments are classified in four basic categories: Carbon Composition, Film, Wirewound types, and potentiometers (variable resistors).

The composition resistor (MIL-R-11) consists of a mixture of finely divided carbon and a binder, either in the form of a slug or a heavy coating, on a glass tube. Specially-formed wire leads are embedded in the resistance element. An insulating case, usually phenolic, is molded around the resistor forming a one-piece enclosure to support the leads and provide moisture sealing.

Fixed film resistors usually consist of resistive material, carbon or metal, deposited on the inside or outside of glass or refractory tubes and spirally-cut to achieve specific resistance. Leads in the ends of the tubes and various types of end caps provide connection to the resistance element. As with composition resistors, a molded plastic case provides physical strength and moisture protection.

The two basic types of wirewound resistors covered in this notebook are Precision styles (MIL-R-93) and Power styles (MIL-R-26).

Precision wirewound resistors are formed by winding a special alloy resistance wire on ceramic forms having expansion coefficients matched to that of the wire. By selecting and matching the resistance wire, almost any temperature coefficient of resistance can be obtained. Some types have special low-inductance and segmented windings which achieve good high-frequency response. These resistors are generally well-sealed in molded cases for use in highhumidity atmospheres.

Power wirewound resistors are similar in construction to precision wirewound types but less attention is given to close tolerances and noninductive winding. Greater attention is given to the means of mounting for the extraction of heat. Special silicome coatings are designed for maximum heat conduction and radiation.

Potentiometers used in electronic equipments are classified in five basic categories: Precision, Semi-Precision, Low Precision, Trimmers and Power types with subdivisions according to similar reliability characteristics.

Precision potentiometers (MIL-R-11974, Style RR)are generally wirewound potentiometers on precision coil forms which can be provided in almost any linear or nonlinear resistance configuration.

Semi-Precision Potentiometers, MIL-R-19, Style RA, are also wirewound but with less emphasis on precision and conformity. The bodies and cores of RA Style power potentiometers are constructed of phenolic or other plastic.

Low-Precision Potentiometers, MIL-R-94, Style RV, are generally composition resistor types commonly used for volume or gain control.

Nonwirewound, Trimmer Potentiometers, MIL-R-22097, Style RJ, are in many styles and types of nonwirewound resistance elements.

Wirewound, Trimmer Potentiometers, MIL-R-27208, Style RT, and MIL-R-35015, Style RTR, are similar except for the greater reliability control and burn-in provided for the Established Reliability (RTR) type.

Wirewound, Power Type Potentiometers, MIL-R-22, Style RP, are vitreous and ceramic power units.

### 5.1 Storage Reliability Analysis

### 5.1.1 Failure Mechanisms

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Most resistors are encapsulated in a molded plastic case or conformally coated to provide moisture protection. But no plastic is the equivalent of hermetic sealing so that moisture is a reliability consideration for all resistors depending on the resistor type. A carbon composition resistor will usually keep itself dry during operation because of its self-generated heat and heat from adjacent components. Longtime storage of carbon composition resistors without operation in a humid atmosphere will result in appreciable increase of resistance. Also, long-time storage in a very dry atmosphere will result in the reverse resistance change. These effects are reduced or eliminated if the composition resistors are potted or hermetically-sealed into higher-order assemblies.

The effect of moisture on film resistors varies according to type. Corrosion or electrolytic action involving impurities or surface contaminants is a major cause of open circuits in the film or between the film and end cap connections. Reduced resistance from this effect prior to final malfunction is frequently hard to detect because of the common localized nature of the effect. Moisture absorbed during storage frequently does not cause serious trouble until after a period of operation with voltage applied to stimulate electrolysis.

Moisture in wirewound resistors is frequently a cause for leakage between turns and between layers which ultimately results in insulation breakdown and shorts. Corrosion and electrolytic action results in open wires or in openings between resistor wire and end cap connections.

Potentiometers cannot be sealed in a complete encapsulated jacket. Even where the resistor element is encased in a plastic or vitreous case there must be a portion of each turn exposed for contact with the wiper arm. This provides many possible points (which can seldom be fully sealed) for the entrance of moisture. Operator-adjusted potentiometers must have movable shafts which protrude through the case and front panel. This opens the interior of the potentiometer to the environment exterior to protecting cases. Various types of shaft seals such as Elastomer "O" rings are at best imperfect moisture seals.

Interior-mounted trimmer potentiometers are given some shelter and moisture protection by the external case, but even these can seldom be potted or hermetically sealed inside a higher order assembly unit.

Potentiometers have additional failure modes relating to the wiper which are effected by moisture. Precision potentiometers may degrade in linearity or noise as a result of moisture absorption and corrosion.

### 5.1.2 Non-Operating Failure Rate Predictions

The non-operating failure rates in FITS (failures per billion hours) for various types of resistors are shown in Table 5.1-1.

Resistor Type	MIL-STD	HI-REL
Carbon Composition	0.11	0.11
Film	0.11	0.033
Wirewound	1.80	0.243
Variable	12.2	8.06
Thermistor	27.8	

TABLE 5.1-1. RESISTOR NON-OPERATING FAILURE RATES

### 5.1.3 Non-Operating Failure Rate Data

The failure rate table in section 5.1.2 is based on storage data consisting of over 61 billion part hours from several programs, with 10 failures reported. The breakdown of storage hours and number of failures for each type of resistor is shown in Table 5.1-2.

The small number of failures does not allow a detailed analysis of the data. It does indicate very little difference between MIL-STD and Hi-Rel carbon composition resistors in storage; a factor of 3 between MIL-STD and Hi-Rel film resistors; a factor of 7 for wire wound resistors; and a factor of 1.5 for variable resistors.

Data was obtained from four sources and are listed in Tables 5.1-3 through 5.1-6.

·		MIL-STI	)	]	HI-REL ·	
Device Type	Storage Hours X 10	Number Failed	Failure Rate In FITS	Storage Hours X 10	Number Failed	Failure Rate In FITS
Composition	9169	1	.109	6897	0	(<.145)
Film	9395	0	(<.106)	30504	1	.033
Wirewound	1109	2	1.803	4116	0	(<.243)
Variable	163	2	12.195	124	l	8.06
Thermistor	108	3	27.778	22	0	(<45.5)

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TABLE 5.1-2. RESISTOR NON-OPERATING DATA SUMMARY

SOURCE A RESISTOR NON-OPERATING DATA (MIL-STD) TABLE 5.1-3.

		STORAGE		FAILURE
DEVICE TYPE	NUMBER	HOURS X 10 <sup>6</sup>	NUMBER	RATE IN FITS
Composition	309396	4517	щ	.221
Film	417772	603	0	(<.164)
Wirewound	18354	268	0	(<3.731)
Variable	6118	89	Ч	11.236
Variable, Matched Pair	2622	38	0	(<26.316)
<b>Fixed Variable</b>	1748	26	0	(<38.462)
Thermal	874	13	0	(<76.923)

TABLE 5.1-4. SOURCE B RESISTOR NON-OPERATING DATA (HI-REL)

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FAILURE NUMBER RATE FAILED IN FITS	0 (<.056)	0 (<1.689)	0 (<17.241)	0 (<58.823)
STORAGE HOURS X 10	17838	592	58	1.7
NUMBER	1357394	45014	4438	1268
DEVICE TYPE	Film	Wirewound	Potentiometers	Thermistor

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TABLE 5.1-5. SOURCE C RESISTOR NON-OPFRATING DATA

----- HI-REL -- MIL-STD ---| | | |

	1 1 1 1 1	UTS-TTM	THEFT OLGUTTW THEFT	1 1 1 1 1		1 1 1 1 1 1 1
	STORAGE		FAILURE	STORAGE		FAILURE
	HOURS	NUMBER	RATE	HOURS	NUMBER	RATE
DEVICE TYPE	X 100	FAILED	IN FITS	X 100	FAILED	IN FITS
Carbon Composition	4652.	0	(<.215)	6897.	0	(<.145)
Carbon Film	6.	) 0	(<166.)	108.	0	(<9.26)
Metal Film	3290.	0	(<.304)	12533.	Ч	.08
Thermal	ł	1	I	2.	0	(<500.)
Thermistor	95.	m	31.6	5.	) 0	(<200.)
Tin Oxide	ł	I	ł	4655.	0	(<.215)
Wirewound						
General	136.	0	(<7.35)	602.	0	(<1.66)
Power	376.	7	5.32	2109.		(<.474)
Precision	329.	0	3.04	788.	0	(<1.21)
Hedter Element	1	1	ł	ч <b>.</b>	<ul><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li><li></li></ul>	1000.)
Variable						
General	11.	ч	90.9	37.	0	(<27.0)
Film	I	I	1	23.	н	43.5
Plastic	I	I	J	Ч	) 0	(~1000.)
Wirewound	ł	1	I		<b>`</b>	<500.)

5.1-6

# SOURCE D RESISTOR NON-OPERATING DATA (HI-REL) TABLE 5.1-6.

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FAILURE RATE IN FITS	(<39.98)	(<39.56)	(<286.7)
NUMBER FAILED	0	0	0
STORAGE HOURS X 10 <sup>6</sup>	25.012	25.278	3.488
NUMBER	797	808	111
DEVICE TYPE	Film	Wirewound	Variable

2

5.2

### Resistor Operational Prediction Models

The MIL-HE K-217B general failure rate model for resistors is:

$$\lambda_{\rm p} = \lambda_{\rm b} ( \pi_{\rm E} \times \pi_{\rm R} \times \pi_{\rm Q}) \times 10^{-6}$$

The general model for the variable resistors is as follows:

$$\lambda_{p} = \lambda_{b} (\Pi_{TAPS} \times \Pi_{R} \times \Pi_{V} \times \Pi_{C} \times \Pi_{E} \times \Pi_{Q}) \times 10^{-6}$$

where:

 $\lambda_{p}$  = device failure rate  $\lambda_{b}^{-}$  = base failure rate I TAPS = Tap Connections Adjustment Factor  $II_{p}$  = Resistance Adjustment Factor  $\Pi_{V}$  = Voltage Adjustment Factor  $\Pi_{c}$  = Construction Class Adjustment Factor  $\Pi_{E}$  = Environmental Adjustment Factor  $II_{O} = Quality Adjustment Factor$ 

The various types of resistors require different failure rate models that vary to some degree from the basic models. The specific failure rate model and the  $\pi$  factor values for each type of resistor are presented in figures 5.2-1 through 5.2-14. The base failure rate and adjustment factor values in the figures are based on certain assumptions. See sections 5.2.1 and 5.2.2 for a description of these parameters.

Table 5.2-1 provides a list of resistor generic types with a cross reference to the corresponding figure number of the failure rate model.

5.2.1 Base Failure Rate  $(\lambda_{b})$ 

The equation for the base failure rate,  $\lambda_{\rm b}$ , is:

$$\lambda_{\rm b} = Ae^{\rm B} \left( \frac{T + 273}{N_{\rm T}} \right)^{\rm G} e^{\rm E} \left[ \left( \frac{S}{\rm Ns} \right) \left( \frac{T + 273}{273} \right)^{\rm J} \right]^{\rm H}$$

where,

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- A is an adjustment factor for each type of resistor to adjust the model to the appropriate failure rate level.
- e is the natural logarithm base, 2.718
- T is the ambient operating temperature (degrees C)
- $N_{rp}$  is a temperature constant
  - B is a shaping parameter
- G, H, J are acceleration constants
  - N<sub>s</sub> is a stress constant
    - S is the electrical stress and is the ratio of operating power to rated power

The quantitative values for the base failure rate model factors are given in Tables 5.2-2 and 5.2-3 for the different resistor types.

FIXED RESISTOR BASE FAILURE RATE  $(\lambda_{b})$  FACTORS

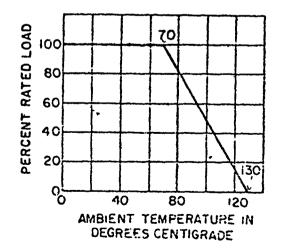
STYLE	MIL-R SPEC.	A	В	N <sub>T</sub>	G	<sup>N</sup> s	H	J
RB RBR RC	39005 11	$3(10)^{-3}$ 4.5(10)^{-9}	1 " 12	398 343	10 " 1	1 " 0.6	1.5 1	1 " <u>1</u>
RCR RD RE RER	39008 11804 18546 39009	0.11 3(10) <sup>-4</sup>	12 1 2.64 "	551 298 "	2.6 1 "	1.45 0.466 "	1.3 1 "	0.89 1 "
RL RLR	22684 39017	$6.5(10)^{-4}$	1	343	3	1	1,	1
RN RNR	10509 55182	1(10)-4 "	3.5 "	398 "	1	1"	1	
RTH RW RWR	NO. 26 39007	Nodel. 9.5(10)-4 "	1	298 "	2	See 0.5 "	rigui l "	ce 6.2-8 1 "

TYPE	MIL-R SPEC.	A	В	N <sub>T</sub>	G	<sup>N</sup> S	H	J
RA RK	19 39002	3.58(10)-2	1"	355 "	5.28	1.44	1	4.46
RJ	22097	0.423	1	400	7.3	2.69	1	2.46
RP	22	$4.81(10)^{-2}$	11	377	4.66	347	1	2.83
RR	12934	$7.35(10)^{-2}$	1	356	4.45	2.74	1	3.51
RT	27208	6.2(10)-3	1	358	5	1	1	1
RTR	39015	61	"	. "	n	n	n	н
RV	94	$6.16(10)^{-2}$	1	373	9.3	2,32	1	5.3

# TABLE 5.2-3 VARIABLE RESISTOR BASE FAILTERATE ( $\lambda_{h}$ ) FACTORS

The ER resistor family generally has four qualification failure rate levels when tested per the requirements of the applicable ER specification. These qualification failure rate levels differ by a factor of ten. However, field data has shown that these failure rate levels differ by a factor about three, hence the  $\Pi_0$  values have been set accordingly.

The use of the resistor models requires the calculation of the electrical power stress ratio, S = operating power/ratedpower, or per Section 5.2.3 for variable resistors. The models have been structured such that derating curves do not have to be used to find the base failure rate. The rated power for the S ratio is equal to the full nominal rated power of the resistor. For example, MIL-R-39008 has the following derating curve:



If a 1 watt resistor were being used in an ambient temperature of 90°C, the rated power for the S calculation would still

be 1 watt, <u>not</u> 60% of 1 watt. Of course, while the derating curve is not needed to determine the base failure rate, it must still be observed as the maximum operating condition. To aid in determining if a resistor is being used within rated conditions, the base failure rate tables show entries up to certain combinations of stress and temperature. If a given operating stress and temperature point falls in the blank portion of the base failure rate table, the resistor is <u>overrated</u>. Such misapplication would require an analysis of the circuit and operating conditions to bring the resistor within rated conditions.

### 5.2.2 I Adjustment Factors

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# 5.2.2.1 Tap Connections Adjustment Factor ITAPS

 $I_{TAPS}$  accounts for the effect of multiple taps on the resistance element. It is calculated as follows:

$$\Pi_{\text{TAPS}} = \frac{(N_{\text{TAPS}})}{25} + 0.792$$

where N<sub>TAPS</sub> is the number of potentiometer taps, including the wiper and end terminations.

5.2.2.2 Resistance Adjustment Factor, IR

 ${\rm I\!I}_R$  adjusts the model for the effect of resistor ohmic values.

5.2.2.3 Voltage Adjustment Factor, N<sub>V</sub>

<sup>II</sup>V adjusts for effect of applied voltage in variable resistors in addition to wattage included in the base failure rate. It is based on the ratio of applied voltage to rated voltage.

The applied voltage is defined as:

V applied = **V**RP applied

where R is the total potentiometer resistance and P applied is the applied power.

# 5.2.2.4 Construction Class Adjustment Factor, N<sub>C</sub>

I<sub>C</sub> accounts for influence of construction class of variable resistors as defined in individual part specifications.

5.2.2.5 Environmental Factor, II<sub>E</sub>

 $I_E$  accounts for the influence of environmental factors other than temperature. Refer to the environments description in the Appendix.

5.2.2.6 Quality Adjustment Factor, IIO

 $II_Q$  accounts for effects of different quality. The established reliability resistor family generally has four qualification levels when tested per the requirements of the applicable specification.

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TABLE 5.2-1 RESISTOR OPERATIONAL PREDICTION MODELS CROSS REFERENCE

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TYPE	MIL-SPEC	STYLE	FIGURE
Fixed, Composition (Insulated)	MIL-R-39008	RCR	5.2-1
	MIL-R-11	RC	5.2-1
Fixed, Film (Insulated)	MIL-R-39017	RLR	5.2-2
	MIL-R-22684	RL	5.2-2
Fixed, Film	MIL-R-55182	RNR	5.2-3
	MIL-R-10509	RN	5.2-3
Fixed, Film (Power Type)	MIL-R-11804	RD/P	5.2-4
Fixed, Wire Wound (Accurate)	MIL-R-39005	RBR	5 <b>.</b> 2-5
	MIL-R-93	RB	5.2-5
Fixed, Wire Wound (Power Type)	MIL-R-39007	RWR	5.2-6
	MIL-R-26	RW	5.2-6
Fixed, Wire Wound (Power Type)	MIL-R-39009	RER	5.2-7
Chassis Mounted	MIL-R-16546	RE	5.2-7
Thermistor (Bead and Disk Type)	MIL-T-23648	RTH	5.2-8
Variable, Wire Wound (Lead Screw	MIL-R-39015	RTR	5.2-9
Actuated)	MIL-R-27208	RT	5.2-9
Variable, Wire Wound, Precision	MIL-R-12934	RR	5.2-10
Variable, Wire Wound, SemiPrecision	MIL-R-19	RA	5.2-11
	MIL-R-39002	RK	5.2-11
Variable, Wire Wound, Power Type	MIL-R-22	RP	5.2-12
Variable, Non-Wire Wound(Trimmer)	MIL-R-22097	RJ	5.2-13
Variable, Composition, (Low Precision)	MIL-R-94	RV	5.2-14

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR INSULATED FIXED COMPOSITION RESISTORS (MIL-R-39008, Style RCR and MIL-R-11, Style RC)

$$\lambda_{\rm p} = \lambda_{\rm b}$$
 (  $\pi_{\rm R} \times \pi_{\rm E} \times \pi_{\rm Q}$ ) x 10<sup>-6</sup>

C È Ē

IR (Resistance Factor)

п В	1.0 1.1 2.5
Resistance Range (ohms)	Up to 100K >.lmeg to 1 meg >1 meg to 10 meg >10 meg

 $\Pi_{\mathbf{E}}$  (Environmental Factor)

Environment	пE
Ground, Benign	0.1
Space Flight	1.0
	2.0
1	4.0
Naval, Sheltered	5.0
Ground, Mobile	-
Naval, Unsheltered	7.5
Airborne, Uninhab.	8.0
Missile, Launch	15.0

N<sub>0</sub> (Quality Factor)

	ц	1.0	٠	0.1	0.03	0
۲	Failure Rate Level	W	д	ĸ	S	MIL-R-11

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FIGURE 5.2-2

MIL-HDBK-217B OPERATIONAL FAILURE RATE MCDEL FOR FIXED FILM (Insulated) RESISTORS (MIL-R-39017, Style RLR and MIL-R-22684, Style RL)

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 $\lambda_p$  =  $\lambda_b$  (  $\pi_R$  X  $\pi_E$  X  $\pi_Q$  ) X 10<sup>-6</sup>

(L)	<b>[</b>	л В	0		9	2		(ようた)とう	1 700 0		Ц.,	٠	٠	٠	6.5	٠	2		15.0				1 7	L.			•	5	ν ο ο			
II <sub>R</sub> (Resistance Factor	sistance Range		to 100K	lmeg to l meg {	to F	>10 meg 2.		(Enwindental		Environment	i	Ground, Benign	Space Flight	I, Fi	rne, Inhab		ď,	Naval, Unsheltered	ធ	Missile, Launch			KATTENAN Ön	Failure Rate Level	M	£ 6	ч р	4 C	MTTD.JJKQA			
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5,2-3 FIGURE

(MIL-R-55182, Style RNR and MIL-K-10509, Style FN) MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR FIXED FILM RESISTORS

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 $\lambda_p = \lambda_b$  (  $\pi_R \times \pi_E \times \pi_Q$  ) x 10<sup>-6</sup>

λ<sub>h</sub> (Base Failure Rate)

	$\vdash$	027 .002	030 .003	034 .003	0038 .004	0044	049 .005	0052 .000	056 .006	059 .006	0063 .007	00.67 .007	071 .008	0075  .008	0080 .009	085 .009	10.090	10. 960	10 .01	10. 010	10. 11	12 .0	Ч	Ч	ł		N				
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E A	.6	02	02	02	02	0	03	63	03	04	04	04	04	020	05	05	00	06	06	07	07	07	08	08	09	60	1	Ч	Ч	.012	Ч
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Rat		5	10	100	5	TOO	02	02	02	02	02	02	02	003	003	03	03	003	03	04	04	04	04	04	05	05	02	005	06	.0064	06
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N<sub>R</sub> (Resistance Range)

Ц	0 H O N	
E	ичччи	
Resistance Range (ohms)	Up to 100K >.lmeg to 1 meg >l meg to 10 meg >l0 meg	

(Environmental Factor) ម្ពុដ

Environment	ыE
Ground, Benign	1.0
F.	г. О
Ground, Fixed	2.5
Airkorne, Inhabited	•
Naval, Sheltered	7.5
Ground, Mobile	10.01
Naval, Unshelcered	Т
Airborne, Uninhab.	12.0
Missile, Launch	8.

I O II 1.0 0.1 0.03 1.0 IQ (Quality Factor) Failure Rate Level አዋዊሪ

MIL-R-10509

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FIGURE 5.2-4 MIL-H

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR POWER FILM RESISTORS (MIL-R-11804, Style RD/P)

 $\lambda_{\rm p}$  =  $\lambda_{\rm b}$  (  $\pi_{\rm R}$  x  $\pi_{\rm E}$  x  $\pi_{\rm Q}$  ) x 10^{-6}

λ <sub>b</sub> (Base Failure Rate)	Ratio of Operating to Rated Wattage	1 5. 1	41 .148 .157 .168 .180 .194 .210 .229 .24	44  .151  .161  .172  .186  .201  .218  .23	7  .155  .165  .177  .191  .208  .226  .247  .27	0  .159  .169  .182  .198  .215  .	3 1.163 1.174 1.188 1.204 1.223 1.244 1.26	57 .167 .179 .194 .211 .231 .	61  .171  .185  .200  .218  .240  .26	65  .176  .190  .207  .226  .24	0  .182  .196  .214  .235  .25	75 .187 .203 .222 .24	80 1 193 1.°10 1.230 1.25	5  . 200  .217  .2	. 206 . 225 . 24
	R		4	! 144	.147				.161	.165	7			ω	
		(ິບ <sub>ດ</sub> )	30	40	۰ ۲	6 Ú	70	80	06	100	110	じんて	130	140	

Π<sub>R</sub> (Resistance Factor)

пR	1.2 1.0 3.5 3
Resistance Range (ohms)	10 tc <100 100 to <100K 100K to <1 meg >1 meg

RE (Environmental Factor)

Environment	пЕ
Ground, Benign	1.0
Space Flight	1.0
ъ	5.0
Airborne, Inhabited	6.5
Naval, Sheltered	7.5
Ground, Mobile	12.0
Naval, Unshelterod	13.5
Arrborne, Uninhab.	15.0
Missile, Launch	35.0

In (Quality Factor)

	Ъ	0.4 0.0 0.0
7	Quality Level	Upper Mil-Spec Lower
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FIGURE 5.2-5

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR FIXED, WIPEWOUND (Accurate) RESISTORS (MIL-R-39005, Style RBR and MIL-R-93, Style RB)

 $\lambda_{p}$  =  $\lambda_{b}$  (  $\pi_{R}$  x  $\pi_{E}$  x  $\pi_{Q}$  ) x 10^{-6}

A, (Base Failure Rate)

													_															•				
	1.	$\infty$	0	60	60	60	H-	01	-	01	H	10	10	01	010	01	н	5	01	2	2	3	5	m	n	4	4					
	6.	61	.0076	002	008	30	008	08	000	000		1	5	5	Ч.	01		01	5	Ч	L.	2	02	02	02	m	n	4				
	.8	000	.0066	000	001	07	07	007	07	008	008	008	000	600	5	10	5	5	01	10	01		5	03	2	2	02	က	Ú4	1	$\mathbf{N}$	
1975	warra	05	.0053	05	06	06	000	000	006	06	0071	002	002	008	08	008	600	60	01	10	01	-	01	10	5	02	2	3	n	$\mathbf{c}$		
	Nd Led	05	0	05	03	05	055	056	058	060	190	06	06	06	07	07	07	08	08	60	-	<b>m</b>	01		-1	0	Ч	2	2	$\mathbf{m}$	038	41
ן ה ת ה ה	1.19 50	04	0	004	04	04	04	005	005	05	005	005	005	005	006	006	90	002	002	200	008	60	5	01	012	013	5	5	02	2	031	$\sim$
Ω.	5	004	0	004	004	004	0043	0044	0045	0046	0047	0048	0049	0051	0053	0055	0057	0060	0064	0068	0072	078	0085	0093	010	011	CI3	015	017	021	.025	B
	- 10 01 - 3	037	037	038	038	038	039	040	040	041	042	043	044	045	047	048	050	053	0056	059	063	067	073	080	088	093	11	12	15	17		26
		5	0	03	03	03	036	03	003	03	003	03	004	0041	C4	004	045	047	0050	005	005	06	06	07	07	08	60	5	Ч.	01	.018	$\sim$
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IIR (Resistance Factor)

п <sub>R</sub>	1.0 1.7 3.0 5.0
tance Range (ohms)	to 10K to 100K to 1 meg >3 meg
Resist (	1001 < 전 10 1 ~

Π<sub>E</sub> (Environmental Factor)

Environment	II E
Ground, Benign	1.0
Space Flight	1.0
round, F	6.0
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ŝ	00
g	0
	•
Airborne, Uninhab.	30.0
ile,	70.0

)r)	о <sup>п</sup>	1.0	0.3	0.1	0.03	5.0
MQ (Quality Factor	Failure Rate Level	W	գ	£	S	MIL-R-93

FIGURE 5.2-6

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR FIXED, WIREWOUND (POWER TYPE) RESISTORS (MIL-R-39007, Style RWR and MIL-R-26, Style RW)

ม่สมไปให้สูงสู่สังหมาในสารแล้วให้สารเร็าในสารเลือกเสียงสารในสารในกลางในสารและ รัฐสารและสารเป็นสารเร็กไลเล้าสาร

T. Garbert & Louis

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 $\lambda_{\rm F}$  =  $\lambda_{\rm b}$  (  $u_{\rm R} \times \pi_{\rm E} \times \pi_{\rm Q}$ ) x 10<sup>-6</sup>

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Factor)		1		3.0	•	•		ه . اسو ا	•	0			)r)	ŀ		1.	•	0.1	.03	5.01												
(Environmental Fac	Environment	1	Flight	ц, ғ.	orne, Inhabited	p. P.		.ບ	orne. Uninhab.	H	ł		n <sub>O</sub> (Quality Factor		lure Rate Level	W		R	S	-R-26				> 20K		NA	NA	1.6	NA	NN	NN	VN VN
п <sub>Е</sub> (Е	1	Ground	Space	Ground	Airborne	INAVAL	Ground	Naval	Airbo	Missile.			ш	ŀ	Farl					MIL-		hms)	> 15K	ţ	20K	1.6	NA	1.2	NA	NA	NA	٧N
																				120	170	de	PIOK	ţ	15K	1.6	1.6	1.2	NA	NA	1.6	AN
		1.0	016	018	$\sim$	2		N												20400B		c Ran	> 7.5K	to	lok	1.6	1.6	1.2	NA	NA	1.2	NA
		б ,	13	015	1 10		2	025 /												00 00 7 0	o Lallce	istanc	> 5 K	to	7.5K	•	1.2	٠	1.6	NA	1.2	NA
	Wattago	8	010		-1	-	-1	2	.023	2										in out	R (Resistance	Res	0 > 1K	رد 	5K		_		H	6   NA	0 1.1	0 1.4
( =	ced	.7	6300	660	110	12	14	910	018	020	02	026	030							t	H H		0 > 50		00 IK	.0 1.	.0 1.		.0 1.	.0 1.		.011.
e Ra e	to Rai	9	0073 .	80	60	-1	H		Ы	-1	-H	$\sim$	023 .	$\sim$	c.							-	5	e t	<u>5</u>	11	~	78	80	81	œ	- {
Failure	ating		059.	066	073 -	081	.060	10.	11 .	12 .	14	15 .	17 .	20	22	2	2	e						Styl		RWR	RWR	RWR	RWR	RWR	RWR	RWR
λ <sub>b</sub> (Base I	Oper	4	48	• ເມີນ ເມີນ		64	71  .	79 .	87	97  .	•	2.			-	<u>.</u> م		4														
י) מע	t 0 t		00.	$\circ$	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0		$\rightarrow$	7									
	ercen	3		004	004	002	005	000	006	007	008	600	1	01	5	10	5	01	S	02	02	02	m									
	д			e e	003	004	004	004	005	005	000	007	002	008	600	0J	리	1	4	Ч	Ч		$\sim$	N I	m							
			0026	028	0030	0033	0036	0033	042	0045	0030	0054	0059	000	002	07	008	60		01	01		01		02	2	$\mathbf{N}$	m				
		(j 0)		0	0	0	0	0	_	~		0	00	10	20	30	40	50	60	70	80		00	01	20	m ·	57 1	S				

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FIGURE 5.2-7

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR FIXED, WIREWOUND (Power Type, Chassis Mounted) RESISTORS (MIL-R-39009, Style RER and MIL-R-18546, Style RE)

 $\lambda_p$  =  $\lambda_b$  (  $\pi_R$  x  $\pi_E$  x  $\pi_Q$  ) x 10<sup>-6</sup>

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Factor)	Level					-Note	1	5K 12	50	X	0 10		2			10	0	ote	0 0		to	-	_	the second second second second second second second second second second second second second second second s	_				
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ilali	Rat		ደብ	~ .	-185,	Factor	+	신	ŭ	<u> </u>			0.0			50	-1	acto:	ce R	<u>^</u>	<u>א ר</u> א ר	거그							
л <sub>Q</sub> (Quality	lure		- 1-4		5 MIL-R-18546	tance	10	- - -										Ce F		^	4 0 7 4	_							
	Fai]				IM	ι Ω		> 100	0	21	• •	٠	0. 	•			- 1	stance	esi	> 100	$\sim$							144	-
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	ł	1	8 C	•••• > <**	····	+	• <u> </u>		Ĺ								ctor		ал	•	16		5						
	age	• 10	10.		$\alpha$	71 -	• –	10									l Fa	'				ted							
	14	7		50	9 0 0 0	입단	35	<b>C</b>	ע 18	าหา							nmental	-	u U	ц		abit	red	6 4 6 7 6	Jninhab.	નુ			
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ase.		Ŧ						.07	0.0	0.	.04		0.0	.06		7		L		<u>5</u>	លីប៊	A		5 ž	A	Ē	4	ы ПО ПО	
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											• 2						l	<b>`</b>				. <u>.</u> ,	02	с . <sup>2</sup>	ічі 4 0	l'ot	2 7	5	

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WIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR THERMISTORS (Bead and Disk Type) (MIL-T-23648, Style RTH) FIGURE 5.2-8

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Ratc)	
Failurc	
(Predicted	
$\lambda_{\rm P}$	

	24	
	Bead Type Style RTH 24,	Disk Type Style RTH 6, 8
Environment	34, 36, 38 to 40	and lu
Ground, Benign	0.021 X 10 <sup>-6</sup>	0.065 X 10 <sup>-6</sup>
Space Flight	0.021 X 10 <sup>-6</sup>	0.065 X 10 <sup>-6</sup>
Ground, Fixed	0.10 X 10 <sup>-6</sup>	0.31 X 10 <sup>-6</sup>
Ground, Mobile	0.52 X 10 <sup>-6</sup>	1.60 X 10 <sup>-6</sup>
Naval, Sheltered	0.30 X 10 <sup>-6</sup>	0.90 X 10 <sup>-6</sup>
Naval, Unsheltered	0.40 X 10 <sup>-6</sup>	1.20 x 10 <sup>-6</sup>
Airborne, Inhabited	0.25 X 10 <sup>-6</sup>	0.75 X 10 <sup>-6</sup>
Airborne, Uninhab.	0.24 X 10 <sup>-6</sup>	1.00 X 10 <sup>-6</sup>
Missile, Launch	1.20 × 10 <sup>-6</sup>	3.60 X 10 <sup>-6</sup>

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FICURE 5.2-9

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR VARIABLE, WIRE-WOUND, (Lead Screw Actuated) RESISTORS (MIL-R-39015, Style RTR and MIL-R-27208, Style RT)

والالمحالة فالمحال المحالية المراجعة والمحالية المحالية والمحالية والمحالية والمحالية والمحالية والمسالية والمسلي

 $\lambda_p$  =  $\lambda_b$  (  $\pi_R$  x  $\pi_V$  x  $\pi_E$  x  $\pi_Q$  ) x 10^6

II <sub>R</sub> (Resistance Factor)	sistance Range		to 2K 1.	2K to 5K 1.	to 20K		IIV (Voltage Factor)	Ratio of Applied	ltage t	Voltage * V	1.0 2.00	.9 1.4	0.3 1.22	0.7	0.13 <u>1</u> .0				I (Bunironaentel Bactor)		Environment N <sub>E</sub>		Flight 1.	LX00 Trhahitod 3.	haltered 0.	d. Mobile 8.	Unsheltered 10.	Airborne, Uninhab.  12.0  Míssile, Launch  60.0	
																								F	Ø.		2.0 2.1	0.03	•
1		6		4 M	4	9			5	4	0				2	7	2	-1					л <sub>Q</sub> (Quality Factor)	Rate Level		Σt	<u>л</u> қ	າ ເບີ	07/7-
		9 1 1.	9 02				4 .02 5 02		•	0 .03	0.	<u> </u>		<u> </u>	0.0	0 .05	4  .0		7	X			ά) <sup>Ο</sup> μ	ailme				7.77	
	ge	•	10.			.02	02.0	10	2	1.03	$\mathbf{c}$	ກເ	200		4	.05	.05	.05		7	<b>\</b>			<u>م</u>	<u>.</u> ]				]
ate)	Natta	• 8		010	02	.021	.022	10	025	.027	010	ກເ	ν υ υ υ υ υ υ	0.00		.044	048	.052		.063	7							\$ 27	к 22
æ	ted	•	10	10	5	01	.019	02	02	02	02		2 0 2 0	2 C C	03	03	04	04	ທ ເ	05	00							26	RT12
Failure	to Ra	9			5	10	210.	50	02	02	02			202	0 M	03	03	04	04	04	ເກ ເ	2						0	тог 24;
Base 1	ing	•5	013	014	014	015	015	010	018	<u> 619</u>	020		7 K 7 K 7 K	026	027	030	032	035	038	04	0 0 4 1	0 U 0 C	200	$\mathbb{N}$				20	90 ( . 22 &
γ <sub>b</sub> (F	perat	.4	11	121	013	013	014	015	016	017	018	510		022	024	026	028	030	033	036	040	044 020	054	090	1			ed =	11
	t of O	e.		10	110	012	.012 ].	013	014	015	510	9 T 0		020	021	023	024	026	029	031	034	0430	047	052	02			*V Rated	
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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR PRECISION WIREWOUND POTENTIOMETERS (MIL-R-12934, Style RR) 5.2-10 FIGURE

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<sup>π</sup><sub>Q</sub>) x 10<sup>-6</sup> × щ ш × цС х Л<sub>и</sub> × х п<sub>R</sub> ( <sub>Itaps</sub> ۹<sup>۲</sup> 11 х<sup>а</sup>

Π taps	taps Ntaps taps Ntaps taps	13 2.67 23 5.2 14 2.88 24 5.4	4         15         3.12         25         5.7           8         16         3.35         26         6.0	3 17 3.59 27 6.4 9 18 3.65 28 6.7	06     20     4.37     30     7.04       06     20     4.37     30     7.36       25     21     4.64     31     7.69	<u> </u>	<sup>Ⅱ</sup> E(Environmental Factor)	nvironment I		n Inhabited 10.	nd, Mobile 10.	- C A	Π <sub>Q</sub> (Quality Factor)	Quality Level NQ		<u></u>
-	Wattage .8 .9 1.0 <sup>N</sup> taps t	182 .192 .203 3 3 1 207 .220 .233 4 1 238 254 373	.278 .259 .322 .329 .357 .387	.395 .433 .473 8 1 .484 .534 .590 9	<u><u> </u></u>	4	R <sub>C</sub> (Construction Factor)	Class II	LC3 4.	0.11 0.0 0.0	<u>л ч</u>	Π <sub>R</sub> (Resistance Factor)	Resistance Range (ohms) ILD	100 to 10K 1. 10K to 20K 1.	50K 100K	00% to 200% 2. 00% to 500% 3.
λ <sub>b</sub> (Base Failure Rate)	C) 1 .2 .3 .4 .5 .6	0 1137 1145 1154 1148 1156 1164 117 0 1137 1145 1154 1164 1173 1184 119 0 1150 1160 1171 1183 1195 209 222	0 .166 .179 .192 .207 .223 .240 .25 0 .186 .202 .219 .237 .258 .279 .30	80 .211 .230 .252 .276 .302 .330 .36 90 .242 .267 .295 .325 .359 .397 .42	00 .281 .313 .349 .389 .434 .484 .54 10 .331 .373 .420 .474 .534 .602 20 .396 .451 .515 .587	0 .481 .556 .6 0 .596		" <sub>V</sub> (voitage	Ratio of Applied Voltage to Rated Voltage * <sup>II</sup> V	.0 2.0	8.	0.6 to 0.3 1.00 0.2 1.05	.1	* V Rated = 250V. for RR0900, 1100, 1300, 2000, 2000	000, 14	

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5.2-11 MIL-MDBK-217B OPERATIONAL FAILURE RATE MODEL FIGURE

FOR SEMIPRECISION WIREWOUND POTENTIOMETERS (MIL-R-19, Style RA and MIL-R-39002, Style RK)

 $\lambda_p = \lambda_b$  (  $\pi_{taps} \times \pi_R \times \pi_V \times \pi_E \times \pi_Q$  ) × 10<sup>-6</sup>

		taps	(4	.4		0	4.	5	0	́.,	7.69	•											Э"	;	z	້າ ຍ				Ì	$\mathbf{\mathbf{N}}$		
		taps	e E	4	<u>ں</u>	9		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	 ი თ	0	31	5								n_(Environmental	Factor)			Benign	JUE	l, Fixed ne Inhahited	sheltered	Mobile	Unsheltered	Uninhab.	Jaunch		
		taps	9	°.	Ч.	m.	່ ເ	8	)! 	• س ا	4.64									_ (Envir	भ	tuomon inu	1077 1177	Ground, Be	STT.4 301	Ground, Fi	ral She	M . Mu	ral. Uns	born	ssile, L		
SC		taps.									21									ш	•			V Gro	2de 00.	0	NO	5	0 1	n C	5		
I taps		taps	0.	-	2	3	) ທີ		° «	0	2.25	.4								Factor)		art i			2		<u>, ,</u>		<u>-i -</u>	<u></u>	1		
	N	taps	m	4	<u>س</u>	- v	7 (	. α	ა თ 											m(Voltage Fa		ш.	to Ra	* 0		6.0			.00.3 	۷ <b>۰</b>	+ • •	RA20X-XA	RK09 RAX-XA
		1.0	.167	$\infty$	-1	4	$\infty$	m	δ	9	9	$\infty$		<u></u>	m	ł				π (Vc	· A.,	Ratio o	ц Н	Voltage	-	.0.		,	0,0		1	for	н н for
	ttage	6.	•149	o	œ	-	4	ω	n	δ	.465	ഹി	.675	826	2								_	Factor)		сп		٠	1.4	•		2	= 275 = 320
()	Wa	·	.134	4	ര	ω		4	ω	2	ω	ഹ	.543	ហ	თ	ω	/							ance Fa		Range						Rated	
Rate	Rated		.120	<b>m</b>	4	S	$\infty$	0	23	~	<b>H</b>	$\sim$	.436	2	<b>N</b>	ഗ	$\alpha_{1}$	7	L.					istan		stance ] (ohme)		2	0 5K			V R	
ailure	q to	·	.107	1	$\sim$	4	15	5	20	2	26	O	.351	Ч	ω	8	0	പ	7					D (Res.		S. L.		t 0	2K t	5K			
se F	ratin	Ŀ	960.	$\mathbf{O}$	Ц	122	13	ഹ	17	σ	-	4	8	2	Ω.	4	ကျ	.635	o	7				ц	- 1	Re		<u> </u>	^	<u>ר</u>			ХС, F -ХС, F
λ <sub>h</sub> (Ba	f Ope	4.	.086	δ	0	10	11	m	14	15	17	20		ഹ	σ	4	0	.472	S O		7			actor)	ſ	л О	×	•	0.0	•		ALO	RA20X-XC,I RA30X-XC
٢	ent o	m.		Ω	08	σ	10		57	13	14	(0)	$\infty$	0	23	9	0	S I	$\circ$	487		7		F4		ty			ec. 2	4		ы	for R
	t m	2	lo l	~	~	08	08	JON	Ч	H	12	БЧ	14	S	18	0	2		ית	.345	וכ		7	(Quality		Qualit		рен	Mil-Sp	31		0	= 75
			ko.	5	06	~	07	ß	08	σ	10	0		$\sim$	4	ഹ	2	ത	-H '	.247	pα	<b>N F</b>	~1	п, сп	ЪĽ		<u>'</u>					Rated	
	1	() ()	30	35	40	45	50	55	09	65	70	75	80	8 8	90	95	0		<b>H</b>	115	N (	CA C	21									* V R	

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MIL-HUBK-217B OPERATIONAL FAILURE RATE MODEL FOR POWER WIREWOUND POTENTIOMETERS (MIL-R-22, Style RP) 5.2-12 FICURE

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х <sub>П</sub><sub>Q</sub>) х 10<sup>-6</sup> X n<sub>R</sub> X n<sub>V</sub> X n<sub>C</sub> X n<sub>E</sub> λ<sub>b</sub> ( Π<sub>taps</sub> 11 م م

	1-1	taps	5.20	4		6.09	4.			7.36	7.69	8.03	
	N,	raps	23	24	25	26	27	28	29	00	31	32	
	1-1	taps	9	2.88	3.12		3.59	3.85	4.10	4.37	4.64	4.92	
Π taps	N	raps		14		16	17	18	19	20	21	22	a an an an an an an an an an an an an an
Г	Ħ	taps	1.00	1.11		1.38		1.69	1.87	2.06	2.25	2.45	
		raps	e	4	ഗ	9	2	8	6	10	ГŢ	12	
		1.0	1.172	\ 		7							
	age	.9	.157	.180	Ч								
	Watta	. 8	143		ω	.219	ഗ	310	.376				
Rate)	Rated	1	131 .	.148	80	.194	.227	.269	.323	.394	.488	.615	
1	g to	• و	.119	.134	.151.	.172	.199	.234	.277	.334	.409	.509	.643
Failure	Operating	.5	.109	.121	.135	.153	.175	.203	.238	.284	4	$\sim$	.524
(Base	f ope	.4	.099	.109	.121	.136	.154	.176	.205	4		.347	.427
ا) م ا	0	• 3	160.	560.	1001	.121	.135	.153	.176	.204	.240	.287	.348
	Percent	.2	.083	.089	.097	.107	.119	.133	.151		.201	.237	.284
		.1	.076	.081	.087	.095	.104	1116	.130	.147	.169	.196	.231
	EI (	(ບ <sub>ິ</sub> ງ)	30	40	50	60	70	80	<u>е</u>	100	110	120	130

N/A 6.0 15.0 18.0 20.0 ្រុ 1.0] N/A II<sub>E</sub> (Environmental Factor) Airborne, Inhabited Naval, Unsheltered Naval, Sheltered Ground, Mobile Environment Grcund, Benign Space Flight Ground, Fixed 1.40 1.22 1.00 2.00 ц  $\pi_V$  (Voltage Factor) Ratio of Applied Voltage to Rated to 0.3 0.8 0 6. 0 6. Voltage 0.6

с ц

IC (Construction Factor)

1.0 2.0

other Styles

All

Unenclosed

Enclosed

RP07, RP11, RP16

Style

Construction

Class

ίðμ 4.00 Upper Mil-Spec. nQ (Quality Factor) Quality Level LOWOL п<sub>R</sub>] 2 H C Range R Resistance 2K 2K 10K Factor) Resistance t Ç (ohms) <del>с</del> с 

N/A N/A

Airborne, Uninhab. Missile, Launch

1.10

0.2

0.1

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о Н ß others **RP06** 250V for I 500V for c 11 11 \*V Rated

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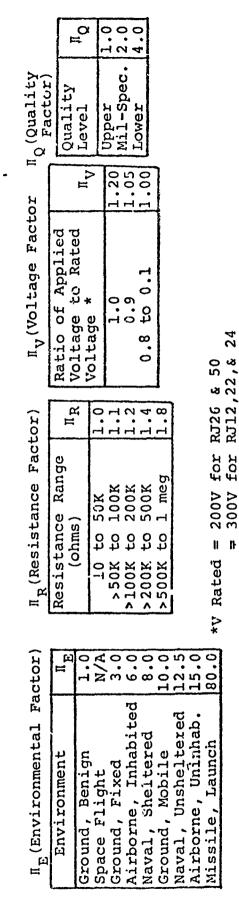
FIGURE 5.2-13

MIL-HDEK-217B OPERATIONAL FAILURE RATE MODEL FOR VARIABLE (NON WIREWOUND TRIMMERS) RESISTORS (MIL-R-22097, Style RJ)

х л<sub>Q</sub> ) х 10<sup>-6</sup> ц П л<sub>v</sub> х × л<sub>R</sub> × λ<sub>b</sub> ( π<sub>taps</sub> 11 ج<sup>م</sup>

$\sim$
Rate
Failure
(Base
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	U.	57	0	<u></u>	5	6	0	2	4	9	6	'n			
	t ar	4	Ś	3.		•	6.4	5	•	ີ. •	.0				
	Ntans	5	23	24	25	26	27	28	29	30	31	32			
	t ans	5	9.	<u>.</u>	Ч.	т.	3.59	8		4.37		4.92			
I taps	Ntans	3								20					
-	1 + anc	5	1.00	1.11	2	с. •	1.53	9.	°.	2.06	2.25	2.45	1		
	Ntang	<u>հ</u>	m	4	S	9	7	ω	თ	10	11	12			
λ <sub>b</sub> (Base Failure Rate)	to Rated Wattage	71 31 21 51 51 .71	1 5 5 1 5 5 5 5 5 5 5 1 6 1 6 4 4 6 7 5 7 0 9 1 7 4 4 1 7	27 555 584 615 648 683 719 758 798 84	52 584 618 653 691 731 773 818 866 91	522 1.201 1.01 1.701 1.744 1.791 1.840 1.893 1.949 11.0	35 657 -12 760 811 866 924 987 1.05 1.	727 787 836 897 962 1.03 1.11 1.19 1.2					34 1.48 1.53	9	
	E				ר כ ד ע	י כ י כ							130	140	



5.2-19

FOR COMPOSITION (LOW PRECISION) POTENTIOMETERS (MIL-R-94, Style RV) MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FIGURE 5.2.14

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 $\lambda_p$  =  $\lambda_b$  (  $\pi_{\texttt{taps}}$  X  $\pi_R$  X  $\pi_V$  X  $\pi_E$  X  $\pi_Q$  ) X 10<sup>-6</sup>

												(L)		4	2.5	0.	0.0	0.0	0.0	5.0	0	0						
		taps	5.20	4.1		. 4		•	<del>ر</del>	7.69		Factor			- 2 	н Т	ິ 	ى 	<u>س</u>	<u>ب</u>	9	TO		cor)	ſ	a	20	0
		taps								31 32		I <sub>r</sub> (Environmental	ent		- 1911 -	cđ	Inhabited	'O'	ile	Unsheltered	Uninhab.	aunch		ity Factor		≓  ,	5	5
	E	taps	2.67	2.88	• • ~	າ ເຊິ່		Ч.	<del>ر</del>	4.64		Enviro	Environment		u, senty Flicht		0	sho	ž,	•	•	le, I		N <sub>O</sub> (Quality	Quality	Level	Nil-Spec.	LOWGL
<b>I</b> taps		taps	13	ך ר 4 ת	י ע ד ר		18	16	20	21. 22		л <sub>в</sub> (	En		Space	Ground.	Airborne	Naval,	Groun	Naval	irbo	Missi		E				
<b>At</b> e		taps	1.00	+0	• "	) ເມ	9	8	•	2.25 2.45							cor)	•		IR R	ł		•	•	1.8			
	N	"taps	т.	לי ע קי ע	י ג 		· თ	9	10	121							ce Factor		Range	A	403	TOOK	200K	500K	1 meg			
		1.0	្រា ដ	n v	) co	0	N	9	0	350 413	N						Resistance		sistance	1		50K to	00K to	t t	COK to			
	aqe		29 .	52	67	85	06 .	33 33	65.	.358	.424						II. (Res)	R	Reg			·····	^ 	^		с К Г		
	Watt	8.	.121	.140	I	.168	.186	.208	.234	.268		m 1	7				ctor)				Λ <sub>II</sub>	~	1.05	Ċ.		RV4xC		
e Rate	Rated	. 7	-H C	2 1	14	15	16	ω	0	. 234 . 268		9 0	っ ヽ	1			de Fac		oli	Rated				Ч		xA;F	pes	
ailure	ng to				12	13		16	8	.205	6	0 4	ი ო	1	1		(Volta		f Ap	e to		•	6.0	。 。	ĸ	RV6x	r ty	
ase F	erati	• 5	60	) m	H	12	13	14	9	.201	2	26	ວ ທ	2	IV -			>	t.	Voltag	H			0.8		72, RV5	1x-1	
λ <sub>b</sub> (B	of Op	•	60.	0 	.10	.11	.12	.13	-14	1.157 1.174	.19	.22	.29	.34	.41	7			H	2	2	<u>I</u>				OL R	or RI or al	
	cent	•	8 0 8 0	0 0 0	60	10			12	.137	16	ω-	24	7	32	δ	7								Ċ	20	250 200 £	
		•	0 8 0 8	ာထ	60	60	60	0		.120	14	5	19,4	2	26	H I	~ '	7									11 12	
		•	00	50	08	08	08	60	60	.113	12	13	101 1	18	21	24	28	5								v Ivareu		
										ده 70					0	0		-1 [					•		•	:		

• 5.2-20

5.2.3 <u>Calculation of Stress Ratio for Potentiometers</u> The stress ratio (S) is defined by the equation:

$$S = \frac{P_{applied}}{\Pi_{eff} \cdot \Pi_{ganged} \cdot P_{rated}}$$

where:

P

applied is the equivalent power input to the potentiometer when it is not loaded (i.e., wiper lead disconnected). Its value is computed as the square of the input voltage, divided by the potentiometer total resistance.

$$W_{\text{operate}} = (V_{\text{in}}^2/R_{\text{P}}).$$

Ρ

rated is the power rating of the potentiometer.

<sup>II</sup>ganged is a correction factor to correct for the reduction in effective rating of the potentiometer due to the close proximity of two or more potentiometers when they are ganged together on a common shaft. the values of  $II_{ganged}$  are obtained from Table 5.2-6.

<sup>II</sup>eff is a correction factor for the electrical loading effect on the wiper contact of the potentiometer. Its value is a function of the type of potentiometer, its resistance, and the load resistance. The value of II<sub>eff</sub> may be computed as follows:

 $\Pi_{eff} = \frac{R_{L}^{2}}{R_{L}^{2} + K_{H}^{2} (R_{p}^{2} + 2R_{p}R_{L}^{2})}$ 

5.2-21

where:

K<sub>H</sub> is a constant dependent upon the style shown in Table 5.2-4. R<sub>L</sub> = load resistance (If R<sub>L</sub> is variable, use lowest value).

R<sub>p</sub> = potentiometer resistance

The value of  $\Pi_{eff}$  can be obtained directly from Table 5.2-5.

Potentiometer Type (Mil Spec)	Style	К <sub>Н</sub>
MIL-R-19	RA	0.5
MIL-R-22	RP	2.0
MIL-R-94	RV	0.5
MIL-R-12934	RR1000,2100, 1001, 2101,	
	2102, 2103, 1400, 1003	0.3
MIL-R-12934	All other types	0.2
MIL-R-22097	RJ11, RJ12	0.3
MIL-R-22097	All other types	0.2
MIL-R-27208	RT22, 24, 26, 27	0.2
MIL-R-27208	All other types	0.3
MIL-R-39002	RK	0.5
MIL-R-39015	RTR22, 24	0.17
MIL-R-39015	RTR12	C.3

TABLE 5.2-4

TABLE 5.2-5. LOADED POTENTIOMETER DERATING FACTOR, <sup>II</sup> eff.

R <sub>T.</sub>		к <sub>н</sub>			
<sup>R</sup> L/ <sub>Rp</sub>	0.5	01.0	0.167	0.2	0.3
0.1	.02	.008	.05	.04	.03
0.2	.05	.03	.15	.13	.07
0.3	.10	.05	.25	.22	.16
0.4	.15	.08	.35	.31	.23
0.5	.20	.11	.43	.38	.29
0.6	.25	.14	.49	.45	.35
0.7	.29	.17	.55	.51	.40
0.8	.33	.20	.60 .	.55	.45
0.9	.37	.22	.63	.59	.49
1.0	.40	.25	.67	.63	.53
1.5	.53	.36	.77	.74	.65
2.0	.62	.44	.83	.80	.72
3.0	.72	.56	.89	.87	.81
4.0	.78	.64	.91	.90	.86
5.0	.82	.69	.93	.92	.88
10.0	.90	.83	.96	.96	.94
100.0	.99	.98	1.00	1.00	.99

Number of Sections	First Potentiometer Next to Mount	Second in Gang	Third in Gang		Fifth in Gang	Sixth in Gang
Single	1.0	No	C Applica	able		
Two	0.75	0.60	Not A	oplicable	3	
Three	0.75	0.50	0.60	Not App	plicable	
Four	0.75	0.50	0.50	0.60	Not App	licable
Five	0.75	0.50	0.40	0.50	0.60	Not Appli- cable
Six	0.75	0.50	0.40	0.40	0.50	0.60

# TABLE 5.2-6. GANGED-POTENTIOMETER FACTOR, I ganged

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5.2-23

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### 5.3 Operational/Non-Operational Failure Rate Comparison

Table 5.3-1 presents the operational failure rates with the operation to non-operation failure rate ratio. The operational failure rates were calculated using the MIL-HDBK-217B prediction models and the following assumptions:

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For carbon composition, film and wirewound resistors, a quality level 'M' with less than 100K resistance at 25°C was assumed with a 50 percent ratio of operating to rated wattage.

For variable resistors, a precision wirewound potentiometer with 3 taps, upper quality, less than 10K resistance and 50 percent derating was assumed.

The launch operation factors were extracted directly from MIL-HDBK-217B.

IGSISTOR OPERATING AND NON-OPERATING FACTORS 5.3-1. TABLE

DEVICE CATEGORY	NON-OFERATING	GROUND, FIXED,	G.FOPERATING TO	MISSILE LAUNCH
RESISTORS	EALLUKE RATE x 10-9	OPERATING FAILURE RATE × 10 <sup>-9</sup>	NON-OPERATING RATIO	TO G.F. OPER- ATING RATIO
Composition	0.11	0.6	5.	7.5
Film	.033	10.5	318.	7.
Wirewound	.243	29.4	121.	11.7
Variable	8.06	780.0	97.	20.
Thermistor	27.80	310.0	11.	12.

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6.0 Capacitors

Capacitors used in electronic equipment are usually categorized into types based on the dielectric material used and their physical construction.

The following summarizes some characteristics of specific capacitor types.

Film dielectric capacitors with paper, paper/plastic, or plastic dielectrics are commonly made by interleaving thin films of dielectric material with metallic foils which serve as electrodes. The resulting four-layer wedge is spiral-wound into a tight cylindrical roll. Leads are attached to this capacitor section by soldering or welding. There are two basic internal constructions. The inserted tab construction utilizes flat metal tabs which are laid against the electrode during winding. These tabs are brought out within one turn of each other and are connected to external leads. The tabs are usually connected to the electrodes without solder. In the extended foil type of construction, the electrode foils are offset from each other such that the end of each electrode turn is exposed only at one end of the roll assembly. The leads are attached at opposite ends and connect all turns of each electrode in parallel.

Paper dielectric capacitors have several constructions: metallic cases with leads existing through glass-to-metal hermetic seal.;, mylar wrap encasement, and polystyrene.

Electrolytic capacitors include aluminum, non-solid tantalum and solid tantalum.

Glass and mica dielectric capacitors have non-flexible dielectric materials. To obtain the higher capacitance units, thin layers of the dielectric are stacked between multiple electrodes. Alternate electrodes are connected in parallel. The electrodes can be either metallic foil or a metallic film painted directly on the dielectric. The assembled stack of electrodes and dielectrics is held in close contact by clamps or by the capacitor encasement.

Mica dielectric capacitors are available either with a molded

encasement or with a conformal dipped encasement.

Glass and procelain dielectric capacitors are encased in glass and the leads are pretreated to give a good glass-to-metal seal. This provides high resistance to humidity. Flexible or semi-rigid conformal coating is recommended for these capacitors.

Ceramic dielectric capacitors are generally available either as tubular designs, as flat disc designs, or as flat plate designs. Mechanically the tubular designs consist of a ceramic tube with silver bands (electrodes) fired on the inside and outside surfaces. Capacitance is formed between the silver bands with the ceramic as the dielectric. Leads are wrapped around each end and soldered to the bands. Leads exit radically from the tube and are parallel. The assembly is encapsulated in Durez resin which is subsequently vacuum-impregnated with a high melting point wax. The disc capacitors consist of a disc with a thin coating of metallic paint fired on each face. Parallel leads are soldered to the metallic electrodes. The assembly is encapsulated in Durez and impregnated with a high melting point wax. Flat plate capacitors consist of a monolithic stack in a molded case. The internal stack consists of multiple films of a noble metal spaced with thin films of ceramic. This assembly is fired to give a monolithic construction. Feedthrough or standoff capacitor designs are essentially a modification of one of the above three capacitor types in which one plate of the capacitor becomes an integral part of the chassis.

Variable ceramic dielectric capacitors consist of a thin ceramic disc mounted in contact with a ceramic frame so that it can be rotated about its center. The electrodes consist of semicircular silver patterns. Capacity is changed by varying the overlap of the electrodes. Contact to the rotatable electrode is made by a spring-loaded spider washer which holds disc in contact with adjacent electrode.

Air dielectric variable capacitors consist of a fixed stator with parallel metal plates and a rotor with similar parallel plates located so that these plates are spaced between the stator plates.

6.0-2

Glass piston trimmers consist of a metal piston which moves axially within a glass sleeve. One electrode consists of a metal band either outside or embedded within the glass sleeve. The close fitting piston forms the adjustable electrode of the capacitor.

# 6.1 Storage Reliability Analysis

### 6.1.1 Failure Mechanisms

Capacitors are susceptible to water vapor. Even in hermetically-sealed units, moisture present during manufacture can lead to deterioration of insulation or dielectric materials. This can be a more serious consideration in certain poorer grade capacitors.

The entrance of moisture through cracks in the seals can be minimized in several ways. Capacitors with seal cracks prior to installation in equipment should be screened out and removed from manufacturing stock. Cracks developed during assembly into equipment can be prevented by careful process control and sometimes can be screened out by final assembly inspection. Cracks which develop during use in later life of the equipment can sometimes be traced to low-quality seals or stresses placed on the leads during equipment manufacture. Certain seal cracks are traceable to a combination of these causes plus stress resulting from use environment.

Electrolytic capacitors have experienced problems in storage. Table 6.1-1 summarizes the predominant failure mechanism associated with the solid tantalum capacitors. Table 6.1-2 summarizes those for wet tantalum capacitors. Electrolyte leakage in the wet tantalum capacitor has been the major source of problems while impurities in the solid tantalum capacitor has caused problems. Most of the failure mechanisms associated with these capacitors are accelerated to failure by a temperature cycling environment. andar versanden hemberen siet werditen stelften die Sons Niemtan verstebenden die eiten die Stiet bestelfteben

#### 6.1.2 Non-Operating Failure Rate Predictions

The non-operating failure rate table for various types of capacitors is shown in Table 6.1-3.

TABLE 6.1-1.

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FAILURE MECHANISM ANALYSIS, SOLID TANTALUM CAPACITORS

	DETECTION METHOD	High leakage currents, or outliers					Short circuits	High leakage currents, or outliers. High dissipation factor.	Dicsipating, capacitance, radiographic inspection	Radiographic inspection
APACL'TURS	FAILURE MODE	Out-of- tolerance					Short	Cut-of- tolerance	Out-of- tolerance	
ANALYSIS, SOLLD TANTALUM CAPACITORS	ACCELERATING . ENVIRONMENT	Temperature cycling, burn in, surge test					Surge test	Temperature cycling, burn in, surge test	Temperature cycling, burn in	Temperature cycling, burn in
FALLURE MECHANISM ANALYSIS,	CAUSE	Impurities in starting tan- talum impede cxide growth at sites during anodization.	Abrasions of sintered pellets expose impurities prior to anodization.	Binder or die impurities on sintered pellet.	Handling damage during anod- ization processes and as- sembly.	Crystalline tantalum pent- oxide.	Oxide shorts due to exces- sive power surges under flicker or scitillation conditions.	Thin MnO2 or silver paint penetrating MnO2 and pre- venting healing of defect sites.	Inadequate wetting of solder to silver paint. Silver paint dissolving into the solder.	Low solder level, pocr anchorage of slug to case, flux between solder and paint
	FAILURE MECHANISM	Oxide Defects					•		Poor Slug Adhesion	
					•			·		

6.1-2

	·····		
ont'a.)	DETECTION METHOD	Radiographic inspection	Radiographic inspection
PACITORS (cc	FAILURE MODE		
S, SOLID TANTALUM CA	ACCELERATING ENVIRONMEN'I		
FAILURE MECHANISM ANALYSIS, SOLID TANTALUM CAPACITORS (cont'a.)	CAUSE	Excessive heat applied during assembly of capacitor into circuit.	Solder distributions, voids, slugs canted in case, bent risers, etc.
	FAILURE MECHANISM	Solder Reflow	Mechanical Defects

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TABLE 6.1-1.

6.1-3

TABLE 6.1-2.

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FAILURE MECHANISM ANALYSIS, TANTALUM FOIL CAPACITORS

DETECTION METHOD	Visual in- spection, electrical test	Electrical test	Electrical test	Visual, elec- trical test
FAILURE MODE	Shorts, open, ca- pacitance, leakuy3	Short, dissipa- tion fac- tor	Capaci- tance, dis- sipation factor	Open
ACCELERATING ENVIRONMENT	Temperature cycling, burn in	Temperature cycling, burn in	Temperature cycling, burn in	Temperature cycling, burn in
CAUSE	Leakage past center of seal causing electro- lyte to bridge between internal nickel wire and case.	Metallic contamina- tion in mylar sleev- ing, improperly cured cured epoxy compound	Reactive impurities in electrolyte or in paper spacer	Machine and operator errors cause inade- quate welds
FAILURE MECHANISM	Electrolyte Leakage	Insulation Defects	Foil Separation	Faulty Lead to Fcil Welds

6.].-4

TABLE 6.1-3. CAPACITOR NON-OPERATING FAILURE RATE

	Failure Rate	<u>in Fic</u> s Hi Rel
	MIL-STD	ni vei
Paper & Plastic	3.8	3.8
MICA	1.2	.97
Glass	.84	.84
Ceramic	.35	.35
Tantalum		
Solid	-	.25
Non-Solid	2500.	9.3
Aluminum Oxide		7.0
Variable	11.	11.

## 6.1.3 Non-Operating Failure Rate Data

The failure rate table in Section 6.1.2 is based on storage data consisting of over 23 billion part hours with 24 failures reported. Storage hours and failure data for each type of capacitor is shown in Table 6.1-4. No significant differences can be seen in this data between MIL-STD and Hi-Rel parts with one exception. The MIL-STD wet tantalum capacitors show a significantly higher failure rate than the Hi-Rel parts.

Data was obtained from four sources and are listed in Tables 6.1-5 through 6.1-8.

6.1-5

TABLE 6.1-4. CAPACITOR NON-OFERATING DATA SUMMARY

**(**\_\_\_\_\_\_

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		WIL-STD			HI-REL	
	STORAGE HOURS X 10	NUMBER	FAILURE RATE / IN FITS	STORAGE HOURS X 10	NUMBER	FAILUNE PATE IN FITS
Paper and Plastic	2103.	ø	3.8	336.	2	5.95
MICA	858.	0	(<1.16)	1033.	Ч	.968
Glass	1192.	0	(<.84)	.396.	0	(<3.38)
Ceramic	2916.	0	(< . 34)	6557.	m	.458
Electrolytic						
IIA	800.	2	2.5	7124.	2	.983
General Class	1	ī	I	2612	7	.766
Solid Tantulum	1	ł	I	3935.	ч	.254
Non-Solid Tantalum	1um .8	2	2500.	430.	4	9.3
Aluminum Oxide	I	I	I	147.	0	(<6.80)
Variable						
All	84.	0	(<11.9)	91.	ч	11.0
Glass	84.	0	(<11.9)	50.	0	(<20.0)
Ceramic	t	ſ	I	е.	) 0	(<3330.)
Air	1	ſ	I	41.	щ	24.4

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6.1-6

TABLE J.1-5. SOURCE A CAMACITOR NON-OPERATING DATA (MIL-STD)

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FAILURE RATE IN FITS	3.41	(<76.92)	(<1.78)	(<.84)	(<î.28)	(<.72)	(<11.23)	(<76.92)	( <l.26)< th=""><th>(&lt;15.62)</th></l.26)<>	(<15.62)
NUMBER	ę	0	0	0	0	0	0	0	0	0
STORAGE HOURS X 10	1761	13	561	1187	778	1391	89	13	I6L	64
NUMBER DEVICES	120612	874	38456	81282	53314	95266	6118	874	54188	4370
DEVICE TYPE	Paper	Film	MICA	Glass	Ceramic	Porcelain	Titanium	Tubular Temp.	Tantalum	Differential, Dual Mode

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CAPACITOR
SOURCE B
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TABLE

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DEVICE TYPE	NUMBER DEVICES	STORAGE HOURS X 10	NUMBER	FAILURE RATE IN FITS
Paper	19020	249.955	0	(<4.00)
MICA	50720	666.546	0	(<1.50)
Ceramic	261842	3441.046	Ч	.291
Tantulum, Solid	143918	1891.325	0	(<.529)
Variable, Glass	3170	41.659	0	(<24.0)

.

TABLE 6.1-7. SOURCE C CAPACITOR NON-OPERATING DATA

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		MIL-STD	# 8 9 3 8		HI-REL	3288888
	STORAGE HOURS	NUMBER	FAILURE RATE	STORAGE HOURS	NUMBER	FAILURE RATE
DEVICE TYPE	X 10 <sup>6</sup>	FAILED	IN FITS	X 10 <sup>6</sup>	FAILED	IN FITS
Paper	329.	7	6.08	19.	O	(<52.6)
Plastic	1	1	I	30.	ы	33.3
Polycarbon Film	ı	1	I	24.	н	41.7
Mylar	Ч.	0	(<100.)	I	t	I
Polystyrene	I	I	T	.01	0	(<100.)
Metallic Film	ł	8	I	2.	0	(<500.)
MICA	297.	0	(<3.37)	354.	н	2.82
MICA, Dipped	I	1	I	.6	0	(<111.)
MICA, Reconstituted	ı	I	I	• 4	0	(<2.5)
Glass.	5.	0	(<200.)	295.	0	(<3.39)
Ceramic	729.	ო	4.12	3103.	7	.64
Feedthrough	1	1	ł	12.	0	(<83.3)
Chip	18.	0	(<55.5)	I	I	ł
Electrolytic General Class	1	1	ł	2612.	2	.76
	8.	0	(<125.)	145.	0	(<.69)
Solid Tantalum Non-Solid Tantalum		10	- 2500.	2030. 430.	-1 -7	.49 9.3
Variable Piston Trimmer	84.	0	(6.11>)	ł	ł	1
Air	•	1	I	41.	-1	24.4
Ceramic	ł	1	1	۳ <b>.</b>	00	(<3033.)
Glass	ł	1	I	•	5	(*927>)

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6.1-9

SOURCE D CAPACITOR NON-OPERATING DATA (HI-REL) TABLE 6.1-8.

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DEVICE TYPE Paper	SUMBER DEVICES 35	STORAGE HOURS X 10 1.220	NUMBER FAILED 0	FAILURE RATE IN FITS (<819.)
	96	2.877	0	(<348.)
	20	.605	0	(<1650.)
	20	.626	0	(<1600.)
	400	13.599	0	(<73.5)
	63	1.771	0	(<565.)
	Ŋ	.133	0	(<; 320.)

#### 6.2 Capacitor Operational Prediction Models

The MIL-HDBK-217B general failure rate model for capacitors is:

$$\lambda_{p} = \lambda_{b} (\Pi_{E} \times \Pi_{CV} \times \Pi_{SR} \times \Pi_{Q}) \times 10^{-6}$$

where:

 $\lambda_{n}$  = device failure rate  $\lambda_{\mathbf{b}}^{-}$  = base failure rate  $II_{r}$  = Environmental Adjustment Factor I = Capacitance Value Adjustment Factor II<sub>SP</sub> = Series Resistance Adjustment Factor  $\Pi_{O}$  = Quality Adjustment Factor

The various types of capacitors require different failure rate models that vary to some degree from the basic models. The specific failure rate model and the I factor values for each type of capacitor are presented in Figures 6.2-1 through 6.2-16. The base failure rate and adjustment factor values in the figures are based on certain assumptions. See sections 6.2.1 and 6.2.2 for a description of these parameters.

Table 6.2-1 provides a list of capacitor generic types with a cross reference to the corresponding figure number of the failure rate model. As indicated in the table, the models are broken out by capacitor style, characteristic and temperature rating. These can be identified from the capacitor type designation. For example, CQR09 A 1 M C152K1M indicated style CQR09, "A" rated temperature, and characteristic "M."

6.2.1 Base Failure Rate  $(\lambda_{b})$ 

The equation for the base failure rate,  $\lambda_{b}$ , is:  $\lambda_{b} = A [(\frac{S}{N_{s}})^{H} + 1]e \frac{B(\frac{T+273}{N_{T}})G}{N_{T}}$ 

where:

is an adjustment factor for each different type of Α capacitor, to adjust the model to the proper failure rate. represents the ratio of operating to rated voltage. S

- N<sub>c</sub> is a stress constant
- e is the natural logarithm base, 2.718
- T is the operating ambient temperature in degrees Centigrade
- $N_m$  is a temperature constant.
- B is a shaping parameter
- G and H are acceleration constants.

The quantitative values for the base failure rate model factors are given in Table 6.2-2 for the different capacitor types. The last column of this table lists the figure number that presents the resulting base failure rate values.

6.2.2 Adjustment Factors

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6.2.2.1 Environmental Factor  $II_E$ 

 $\mathbb{R}_{\underline{2}}$  accounts for the influence of environmental factors other than temperature. Refer to the environment description in the Appendix.

6.2.2.2 Capacitance Value Adjustment Factor, <sup>II</sup>CV

 $\Pi_{\rm CV}$  adjusts the model for effect of capacitance related to case size.

6.2.2.3 Series Resistance Adjustment Factor, <sup>R</sup>SR

IL R adjusts the model for the effect of series resistance in circuit application of some electrolytic capacitors.

6.2.2.4 Quality Adjustment Factor, NO

 $II_O$  accounts for effects of different quality levels.

The Established Reliability (ER) capacitor family generally has four qualification failure rate levels when tested per the requirements of the applicable ER specification. These qualification failure rate levels differ by a factor of ten. However, field data indicates that these failure rate levels differ by a factor about three, hence the  $I_0$  values have been set accordingly. TABLE 6.2-1 CAPACITORS OPER.JIONAL PREDICTION MODEL CROSS REFERENCE

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FIGURE	6.2-1	6.2-2	6. 2 - 3	6.2-4		6.2-5	6.2-6	6.2-7	6.2-3	6.2-9
STYLE	CPV07 CQ08,09,R,3,-Characteristic P	CPV17 CHR09 (50 Volt Rated) CHR39 & 49 CQ08,09,12,13-Characteristic M CQ72,-Characteristic E CDR32 & 33	CHR09 (above 50 Volt Rated) CHR01, 12,19,29 & 59 CQ08, 09,12,13,20,72, Charac- teristic K CQ06 & 07-Characteristic Q CQR01,07,09,12,13,39,42	CM (Molded)	CMR (Dipped)	CB	CYR	Designated'A' rated temperature CKR13,48,64,72	Designated 'B' rated temperature CKR05-12,14-16,17-19,73,74	Designated 'C' rated temperature
MIL-SPEC	MIL-C-14157 MIL-C-19978	MIL-C-14157 *MIL-C-39022 MIL-C-19978	MIL-C-39022 MIL-C-19978	MIL-C-5	MIL-C-39001	MIL-C-10950	MIL-C-23269	MIL-C-11015 MIL-C-39014	MIL-C-11015 MIL-C-39014	MIL-C-11015
TYPE	Paper and Plastic Film 65° Max Rated	Paper and Plastic Film 85°C Max Rated	Paper and Plastic Film 125°C Max Rated	MICA		Button MICA	Glass	Ccramic (General Purpose) 85°C Max Rated	Ceramic (General Purpose) 125°C Max Rated	Ceramic (General Purpose) 150°C Max Rated

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. 6.2-3

TABLE 6.2-1 CAPACITORS OPERATIONAL PREDICTION MODEL CROSS REFERENCE (CON'T)

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FIGURE	6.2-10	6.2-11	6.2-12	6.2-13	6.2-14	6.2-15	6.2-16
STYLE							
	S	CSR	CLR CL	cu	CE	CV	PC
MIL-SPEC	MIL-C-20	MIL-C-39003	MIL-C-39006 MIL-C-3965	MIL-C-39018	MIL-C-62	MIL-C-81	MIL-C-14409
TYPE	Ceramic, Temperature Compensating	Tantalum Electrolytic (Solid)	Tantalum Electrolytic (Non-Solid)	Aluminum Electrolytic (Aluminum Oxide)	Aluminum Dry Electrolytic	Variable Ceramic	Variable, Piston Type (Tubular Trimmer)

6.2-4

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(MIL-C-14157, Style CPV07 and MIL-C-19978, Style CQ08,09, FOR PAPER & PLASTIC FILM CAPACITORS -65°C MAX. RATED MIL-HDEN-217B OPERATIONAL FAILURE RATE MODEL 6 \_ 2-1 FIGURE

in the second second and the standard and the second second second second second second second second second s

(Mil-C-1413/, Suyle Cryon and 12, 13 - Characteristic P)

$$\lambda_{\rm p} = \lambda_{\rm b}$$
 (  $\pi_{\rm E} \times \pi_{\rm Q}$  ) X 10

λ<sub>b</sub> (Base Failure Rate)\*

F			S, Ra	Ratio of	Operating		to Rated	d Voltage	age	
(ບ 0)	г.	.2	.3	.4	•5	• 6	.7	• 8	6.	1.0
0	.00006	.00006	.00007	1000.	.0002	.0004	0100.	6100.	.0034	.0057
ະກ 	. 20006	.00006	00007	.0001	.0002	.0005	.0010	<b>6100.</b>	.0034	.0058
10	00006	.00006	00008	1000.	.0002	.0005	0100.	.0020	.0035	.0060
15	.00006	00007	.00008	.0001	.0002	.0005	°0011	.0020	.0037	.0062
20	.00007	.00007	.00008	.0001	.0002	.0005	.0011	.0021	.0039	.0065
25	.00007	.00007	.00009	.0001	.0002	.0006	.0012	.0023	.0041	.00701
30	.00008	.00008	1000	.0001	.0003	.0006	.0013	.0025	.0045	.0076
35	.00009	.00009	.0001	.0001	.0003	.0007	.0015	.0029	.0051	.0086
40	1.0001	10001	1000.	.0002	.0004	.0003	.0017	.0033	.0060	010.
45	0001	1000.	1000.	.0002	.0005	.0010	.0022	.0041	.0074	.012
50	1000	.0001	.0002	.0003	· 0005	.0014	.0028	.0054	1.600.	.016
55	l. 0032	.0002	.0002	.0004	.0009	.0020	.C041	.0077	.013	.023
	.0003	.0003	0004	.0007	.0015	.0031	.0064	.012	021	.036
65	.0006	.0006	.0008	.0013	.0027	.0057	110.	.022	.039	.066
									1	
	ц,	<sub>e</sub> (Envir(	л <sub>ह</sub> (Environmental	I Factor	)X)		nu o	A VILLA F	FACTOR	
	•	1								Į

Observe ac voltage limits of Figure 6.2-1-a and corresponding temperature rise from Figure 6.2-1-b in determining stresses for table look-up.

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MIL-C-19978 Non-ER

10/444000 00/444000

Airborne, Inhabited

Space Flight Ground, Fixed Naval, Sheltered

Grounâ, Mobile

Naval, Unsheltered Airborne, Uninhab.

Launch

Missile,

ЛO.

Failure Rate Level

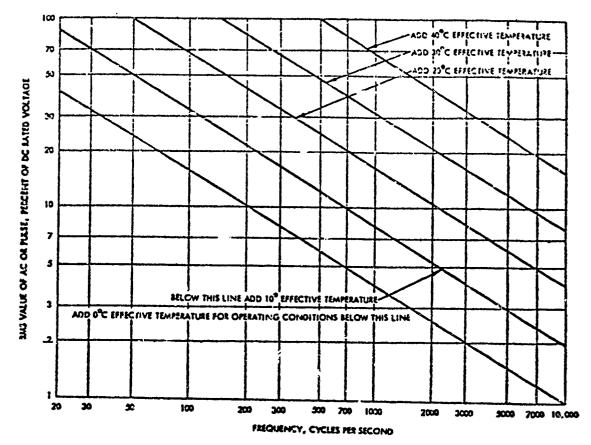
ЦЕ

Environment

Benign

Ground,

بطيعها يكلم لأطرائهم مناطر الموادرة والمراجع والمراكبة والمعود



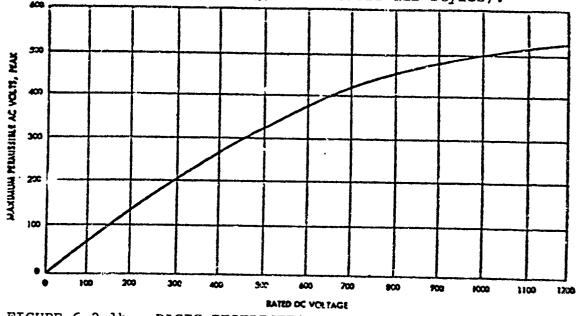
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accessively the desired

FIGURE 6.2-1a. EQUIVALENT TEMPERATURE INCREASE FOR EFFECTS OF AC OR PULSES FOR PAPER & PLASTIC FILM CAPACITORS (Applicable to MIL-C-14157 & MIL-C-19978, Chars. E, K, M & Q; MIL-C-39022 all styles).



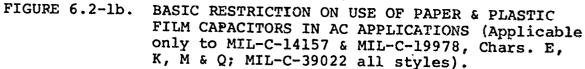


FIGURE 6.2-2 1

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR PAPER & PLASTIC FILM CAPACITORS - 85°C MAX RATED (MIL-C-14157,Style CPV17; MIL-C-39022,Style CHR09(50 volt rated), CHR39 & 49; MIL-C-19978,Style CQ08,09,12,13-Characteristic M, CQ72-characteristic E, CDR32 & 33)

 $\lambda_{p}$  =  $\lambda_{b}$  (  $\pi_{E} \times \pi_{Q}$  ) x 10<sup>-6</sup>

 $\lambda_{\rm b}$  (Base Failure Rate) **\*** 

a	Environm	Ground Ban	1 ** 	ን፦ ት ቤ ት		She	Ground Mob		- u - u - u - u - u - u - u - u - u - u	Missile La			II. (Quality	2	Failure Rat		4 Z	: D			
		1.0	no.	ŝ	ŝ	in	0058	ko.	5	90		007	008	60	гì,	0013	10	024	m	066	•
		<b>6</b> •	03	3	03	.0033	.0034 .	03	036	38	040	04	4	05	.0063	07	H	,014 1.		m	
	Voltage	. 8	10	5	5	H	.0019	10	2	2	2	N	3	03	0	04	(C)			.022	
	Rated V		00	0	Ο	r	.0010	-	m	1	-	.0012	10	ч	Ч	0023	.0030	.0042	Q	1.10.	
	t	ا . 6	00		Ο	0	.0005		00	00	00		00	00	8	5		02		S	
	Operating	.5	00	00	0	0002	.0002	.0002	00	000	.0002	00	00	8	.0004	8	00	0100.	5		
	of	4.1	0	0001	.0001	1.000.	1000.	0	00	.0001	00	1000.	00	00	Ο	.0002	.0003	1.0004	.0007	.0013	
3	Ratio	.3	.00007		.00007	00007	.00007	1.00007	000	.00008	.00009	.00009	1000	10001	10001	0001	.0002	.0003	0004	.0008	
	S,	.2	000	000	00	000	<b>00000</b>	000	000	.00007	000	000	00	0	1000.	00	1000.	0	.0003	00	
		• 1	Õ	Ō	00	,00006	.00006	0	0	.00007		0	0			1000.	1000.		.0003		
	FI	ົບ ()	0	S			20														

\*Observe ac voltage limits of Figure 6.2-1-a and corresponding temperature rise from Figure 6.2-1-b in determining stresses for table look-up.

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N<sub>E</sub> (Environmental Factor)

Environment.	ΞIJ
Ground, Benign	7
Space Flight	ri,
d, F	2
Airborne, Inhabited	4
Naval, Sheltered	4
Ground, Mobile	4
Naval, Unsheltered	σ
Airborne, Uninhab.	
Missile, Launch	20
- V - V - V - V - V - V - V - V - V - V	U

ality Rate M M R R R R R R R R R -ER	~	ο <sub>п</sub>	1.5 1.0	٠	1.0	0.03		10.01
X X	<sup>II</sup> Q (Quality Factor)		μw	գ	R	S	MIL-C-19978	Non-ER

6.2-7

6.2-3 FIGURE

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(above MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR PAPER & PLASTIC FILM CAPACITORS -125°C MAX RATED (MIL-C-39022, Style CHR09 (above 50 volt rated), CHR01, 12, 19, 29 & 59; MIL-C-19978, Style CQ08, 09, 12, 13, 20, 72-characteristic K, CQ06 & 07-characteristic Q, CQR01, 07, 09, 12, 13, 19, 39 & 42)

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π<sub>E</sub> x π<sub>Q</sub> ) x 10<sup>-6</sup> ) , = ۲ P

)r)	L L	a,		2				s, c									╞	=~ l	٠	1.0	٠	1.0	.031		0.0			
ment Factor	ment		benign iaht	l. Fixed	inhahiter	itorod i		MODJ.LE	unsner tered		<b>L</b> AURCH					Y ractor/	I LOUGT O	+ 2 > 2 + 2 + 2 + 2 + 2 + 2 + 2 + 2 + 2					<u>ں</u>		T			
(Environment	Environment		Grouna, Be Space Flic	Ground. Fi	ai rhorne.	ATTEN Shell	י ייי	rouna,	Val,	irporne,	. 01-100					AILLEUGY C		27077	Ч	£	ጨ	ĸ	S	MIL-C-1997	Non-ER			
ΠE	<b>b</b>										~~				•			4								l		-
		1.0	.0054	.0004	• 0024	0054	.0054	.0055	.0055	.0055	0056	.0056	.0057	.0058	.0000	1.0061	.0064	1.0057	.0072	.0078	,0067	.0099					3	
	ge	. 9	°0032	n (	5	e o		03	.0032	03	e	Ο	.0034	0	0	.0036	0038	.0040	.0043	.0046	.0051	.0059			rf.	-		.039
	Voltag	. 8		55		5	01	.0018	5	5	5	5	.0019	5	02	N.	03	02	02	.0026	02	,0033	m	.0048	06	80	rd.	. 922
Rate) *	Rated		0		n o	00	0	S	.0009	.0009	00	.0010	.0010	0	Ο	.0010	.0011	1100.	5	S)	-	.0017	.0020		.0033	.0046	.00.70	110.
Failure	ing to	• 6	00	<b>D</b> (		.0004	.0004		.0004	.0004	.0004	.0004	.0005	.0005	.0005	.0005	.0005	.0005	.0006	.0006	.0007	.0008	0100.	0	10	02	ω	
ase	perati	<b>•</b> ک	.0002	2000.	- nonz	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0002	.0.03	.0003	.0004	.0004	.0005	00	5	5	$\sim$
λ <sub>b</sub> (B	0 0f 0	.4	1000.		TOO	100	001	100	100	100	100	1000	1000	₹00	100	1000	1000	100	0001	1000	100	0002	002	00	80	00	8	5
	, Rati	•	20000.		000	000	0000	000	000	0000	000	0000	000	000	000	000	000	000	000	80	00	00	00	00	00	80	00	800
	S		.00006		000	000	000	000	000	000	000	000	000	000	000	000	000	000	000	000	000	00	00	00	00	80	8	8
		1.	00006		0000	<u>o</u>	00	00	00	00	00	00	00	00	00	00	0	00	00	00	00	10	C	0	0	Ο	0	0
		() ()	01	<u> </u>	2	12	20	25	0 M	5 S	0	45	0	ເກ ເ	0	S	70	S	0	ຽ	0	95	00	105	Ч	Ч	2	2

\*Observe ac voltage limits of Figure 6.2-1-a and corresponding temperature rise from Figure 6.2-1. b in determining stresses for table look-up. av a versioners i sourced state the markine marking atomatic here were detailed at the state of Keyter atomatic feet and

FIGURE 6.2-4

MIJ.-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR MICA CAPACIFORS (MIL-C-5, Style CM(Melded) and MiL-C-39001, Style CMR(Dipped)

 $\lambda_{p} = \lambda_{b}$  (  $\pi_{E} \times \pi_{Q}$  ) x 10<sup>-6</sup>

λ<sub>h</sub> (Base Failure Rate)

S, Ratio 05 .00006 .00 06 .00007 .00 08 .0001 .00 1 .0001 .00 1 .0002 .00 2 .0002 .00 3 .0004 .00 4 .0005 .00	001 000 008 000 009 000 01 000 01 000 02 000 02 000 02 000 03 000 03 000	ting to 6 1 .0001 1 .0002 2 .0003 3 .0004 3 .0005 6 .0008 8 .0010 8 .0013	.0005 .0003 .0003 .0003 .0005 .0005 .0010 .0010	Voltaq •8 •0003 •0005 •0008 •0008 •0012 •0012	6.0004 00004 00006 00011 00011 00015 00015 00015	1.0 .0006 .0008 .0010 .0014 .0018 .0018 .0022
.00006 .00006 .00001 .0001 .0001 .0001 .0001 .0002 .0002 .0003 .0003 .0005 .0005	4    5       008     .000       001     .000       01     .000       01     .000       01     .000       01     .000       01     .000       02     .000       03     .000       03     .000       03     .000       04     .000	9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			•9 004 005 007 001 011 013 015 024 024	1.0 000 001 001 001 002 002 002 003
5 .00006 .0 6 .00007 .0 8 .0001 .0 8 .0001 .0 .0001 .0 .0002 .0 .0003 .0 .0005 .0	008 .000 01 .000 01 .000 01 .000 01 .000 02 .000 02 .000 03 .000			000000000000000000000000000000000000000	0004 0006 011 011 020 020 020 020 020 020 020	000 001 001 001 002 002 002
6 .00007 .0 8 .0001 .0 8 .0001 .0 .0001 .0 .0002 .0 .0003 .0 .0005 .0 .0005 .0	009 000 01 000 01 000 01 000 02 000 02 000 03 000 03 000			000000000000000000000000000000000000000	000 011 00 01 00 02 00 02 00 02 00 02 00 02 00 00 00	000100000000000000000000000000000000000
7 .0009 .0 8 .0001 .0 .0001 .0 .0001 .0 .0002 .0 .0003 .0 .0005 .0	01 .000 01 .000 01 .000 02 .000 03 .000 03 .000 03 .000			000000000000000000000000000000000000000	0007 0013 0013 0015 0015 0015 0024	000100000000000000000000000000000000000
8 .0001 .0 .0001 .0 .0001 .0 .0002 .0 .0003 .0 .0003 .0 .0005 .0	01 .000 01 .000 02 .000 02 .000 03 .000 03 .000		000000000000000000000000000000000000000	000000000000000000000000000000000000000	001 013 013 026 024 026	000100000000000000000000000000000000000
.0001 .0001 .0001 .0002 .0002 .0003 .0003 .0003 .0005 .0005	01 .000 02 .000 02 .000 03 .000 04 .000	000 000 000 000 000 000	000000000000000000000000000000000000000	000000000000000000000000000000000000000	011 013 020 024	00200
.0001 .0 .0001 .0 .0002 .0 .0003 .0 .0003 .0 .0005 .0	02 .000 02 .000 03 .000 04 .000	000 000 100 100 100	100 100 000	000000000000000000000000000000000000000	013 015 020 024	005 002 002
.0001 .0002 .0002 .0003 .0003 .0004 .0005	02 .000 03 .000 04 .000	0000	100	00010000	015 020 024	002003
.0002 .0002 .0003 .0003 .0004 .0005	03  .000 04  .000	000 1000	100	001002	020 024 024	002
.0002 .0 .0003 .0 .0004 .0 .0005 .0	04 .000	.000 .001	10	001002	024	003
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0017 .0	24  .003	.005	07	1	1	02
0021 00	30  .004	.006	60	Ч	5	02
0026 .0	36  .005	.008	7-1	-H	2	3
0.031 .0	44 .006	1.009	-	3	2	3
0.039 .0	54  .008	-01	H	2	e	4
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.0071 .0	0 [.01	2	m	4	9	ω
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N<sub>E</sub> (Environmental Factor)

Environment	ы ш	
Ground, Benign	F	
Space Flight	Ч	
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ne,	9	
Naval, Sheltered	9	
Ground, Mobile	9	
Naval, Unsheltered	14	
Airborne, Uninhab.	24	
Missile, Launch	30	

(Juality Factor)

	л <sup>о</sup> п	1.0	0.3	0.1	0.03	10.01
×	Failure Rate Level	W	Сł	R	S	MIL-C-5 (molded)

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MIL-HDBK-217E OPERATIONAL FAILURE RATE MODEL FOR BUTTON MICA CAPACITORS (MIL-C-10950, Style CB)

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 $\lambda_{\rm p}$  =  $\lambda_{\rm b}$  (  $\pi_{\rm E}$  x  $\pi_{\rm Q}$  ) x 10^{-6}

λ<sub>b</sub> (Base Failure Rate)

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Factor)	ы Ц Ц	44400	17.5	24	30
II <sub>E</sub> (Environmental Fa	iΥ	<u></u>	ns	Alrborne, Uninlab.	Missile, Launch

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MIL-HDBK-217E OPERATIONAL FAILURE RATE MODEL FOR GLASS CAPACITORS (MIL-C-23269, Style CYR)

 $\lambda_{\rm P}$  =  $\lambda_{\rm b}$  (  $\pi_{\rm E}$  x  $\pi_{\rm CV}$  x  $\pi_{\rm Q}$  ) x 10^{-6}

λ<sub>b</sub> (Base Failure Rate)

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	.010	.011	.012	.015	.021	.032	.051	.081	.12	.18
	<b>H</b>	5	-	Ч	2	04	06	60	.15	.22
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Capac	ance					39			150		õ		680		1300	80		5100	(Envi
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<pre>IQ(Quality Factor Failure Rate Level</pre>	니 ≍ 다 ĸ い

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MIL-HDRK-217B OPERATIONAL FAILURE RATE MODEL FOR CERAMIC (General Purpose) CAPACITORS - 85°C MAX RATED (MIL-C-11015, 'A' rated temperature; MIL-C-39014, Style CKR13, 48, 64, 72)

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 $\lambda_{p} = \lambda_{b}$  (  $\pi_{E} \times \pi_{Q}$  ) x 10<sup>-6</sup>

λ<sub>b</sub> (Base Failure Rate)

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ILE (Environmental Factor)

ПЕ	-1	r-1	2	4	4	4	8	101	15
7	Ground, Benign	Space Flight	Ground, Fixed	Airborne, Inhabited	Naval, Sheltered	Ground, Mobile	Naval, Unsheltered	Airborne, Uninhab.	н

Factor)	
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II <sub>Q</sub> (Qual	

П	1.5	1.0	0.3	0.1	0.03	10.01
Level						
Rate	J	E	٥.	æ	ro	-11015
Failure		~	н		J	MIL-C-11015

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FOR CERAMIC (General Purpose) - 125°C MAX RATED (MIL-C-11015, 'B' Rated Temperature and MIL-C-39014, Styles CKR05-12, 14-16, 17-19, 73 & 74) MIL-HDBK-217B OPERATICNAL FAILURE RATE MODEL

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 $\lambda_p = \lambda_b$  (  $\pi_E \times \pi_Q$  ) x 10<sup>-6</sup>

λ<sub>b</sub> (Base Failure Rate)

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		Aug			•													_									
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Rated		5	2	2	2	2	N	2	2		N	2	<b>N</b>	N	2	2	2	2	2	S	3	S	m	m	m	.032	m
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of Op	.4	50	06	90	06	00	90	06	06	06	06	90	06	06	07	5	07	07	0	01	01	0	0	07	07	.0080	08
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N<sub>n</sub> (Environmental Factor)

	пЕ	-	1			4	4	3		15	
a	Environment	Ground, Benign	Space Flight	Ground, Fixed	Airborne, Inhabited	Naval, Sheltered .	Ground, Mobile	Naval, Unsheltered	Airborne, Uninhab.	Missile, Launch	

IQ (Quality Factor) ailure Rate Level

ц б 1.5 0.3 0.03 10.03 MIL-C-11015 エMPRS

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR CERAMIC (General Purpose) - 150°C MAX RATED (MIL-C-11015, 'C' RATED TEMPERATURE)

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 $\lambda_{p} = \lambda_{b}$  (  $\pi_{E} \times \pi_{Q}$  ) x 10<sup>-6</sup>

λ<sub>b</sub> (Base Failure Rate)

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n (Environmental Factor)

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Factor)	ы <sup>п</sup> о	. 1.5	1.0	0.3	0.1	0.03	10.01
IIQ (Quality Fact	Failure Rate Level	L	W	ρι	R	S	MIL-C-11015

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR CERAMIC, TEMPERATURE COMPENSATING CAPACITORS (MIL-C-20, Style CC) FIGURE 6.2-10

 $\lambda_{p} = \lambda_{b} ( \pi_{E} \times \pi_{Q}) \times 10^{-6}$ 

λ<sub>b</sub> (Base Failure Rate)

			s,	Ratio o	f Opera	ting to	Rated	Voltage		
(၁ <sub>0</sub> )			• 3	.4	•5	•6	٤.	. 8	6.	•
0	005	200	010	018	030	048	74	108	H	206
Ŋ	000	008	013	022	037	059	90	132	0185	252
35	008	010	910	027	045	0072	110	161	226	307
40	00102	012	S)	033	S	ω	135	197	9	75
45	.00125	00156	.00241	.00407			.01654	.02410	.03380	.04591
50	015	119	29	049	083	132	202	294	412	560
55	018	023	036	060	101	<b>162</b>	246	359	0504	684
60	00228	028	044	074	123	197	301	439	615	836
65	027	034	053	060	151	241	368	536	752	021
70	034	042	ហ	110	4	ິ	449	655	.09187	48
75	041	)52	080	0135	225	360	549	800	1122	524
80.	050	063	097	<b>165</b>	275	440	670	977	370	861
8 22	062	770	119	201	336	538	819	193	674	274
90	075	994	<b>146</b>	246	411	657	000	457	044	777
95	00925	S	178	300	502	802	222	780	497	392
100	113	141	217	67	613	80	492	174	050	143

IE (Environmental Factor)

Environment	ЯΕ
Ground, Benign	H
Ե	2
Ground, Fixed	4
Airborne, Inhabited	9
Naval, Sheltered	9
Ground, Mobile	9
Naval, Unsheltered	18
Airborne, Uninhab.	24
Missile, Launch	30
	)

Factor)	Γ
Quality	
ğ a	

Quality Level	пΩ
Upper	1.0
. il-Spec	5.0
Lower	15.0

RATE MODEL CAPACITORS MIL-HDBK-217B OPERATIONAL FAILURE FOR TANTALUM ELECTROLYTIC (Solid) (MIL-C-39003, Style CSR) FIGURE 6.2-11

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 $\lambda_p$  =  $\lambda_b$  (  $\pi_E$  x  $\pi_{SR}$  x  $\pi_Q$  ) x 10^{-6}

(Base Failure 0f Operating t 00065 00996 0 00066 00998 0 00072 0010 0 00072 0010 0 00074 0011 0 00074 0011 0 00074 0011 0 00074 0010 0 00094 0013 0 0019 0014 0 0013 0019 0 0013 0019 0 0014 0 0013 0019 0 0013 0019 0 0013 0019 0 0013 0 0014 0 0013 0 0013 0 0013 0 0014 0 0013 0 0014 0 0013 0 0013 0 0014 0 0013 0 0014 0 0013 0 0013 0 0014 0 0013 0 0013 0 0013 0 0014 0 0013 0 0014 0 0013 0 0015 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0010 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 0000 0 00000 0 0000 0 0000 0 0000 0 0000 0
Ab       (Base Failure Rate)         S. Ratic of Operating to Rated Volta         S. Ratic of Operating to Rated Volta         3 0037 0047 0066 0098 014 021 029         3 0037 0047 0066 0098 014 021 029         5 0038 0048 0067 0099 014 021 029         6 0039 0059 0070 010 015 021 003         6 0040 0053 0074 011 015 021 031         6 0043 0055 0077 011 015 022 031         6 0043 0055 0077 011 015 024 034         6 0043 0055 0077 011 016 023 033         7 0053 0077 011 016 024 033         7 0053 0077 011 017 025 033         7 0053 0077 011 017 025 033         7 0053 0077 011 017 025 033         7 0053 0071 010 014 013         7 0054 0071 010 014 013         7 0055 0077 011 017 025 033         7 0053 0071 010 014 021         7 0053 0071 010 014 021         7 0053 0071 010 014 021         7 0051 0071 010 014 021         7 0051 0071 010 014 021         7 0051 0071 010 014 021         7 0051 0013 0014 021         7 0051 0014 021         7 0051 0017 016         7 0051 0017 010         7 0051 0013 0014 021         7 0051 0013 0015         7 0051 0014 0015         7 0051 0017 010         7 0051 0017 016         7 0051 0013 0014 0021
Ab       (Base Failure Rate)         S. Ratic of Operating to Rate         S. 0037       0066         S. 0037       0067         S. 0038       0069         S. 0039       0050         S. 0039       0067         S. 0039       0067         S. 0053       0074         S. 0053       0074         S. 0054       0010         S. 0055       0077         S. 0057       0010         S. 0057       0011         S. 0057       0013         S. 0057       0014         S. 0057       0013         S. 0057       0014         S. 0057       0013         S. 0056       0014         S. 0057       0013         S. 0057       0014         S. 0057       0014         S. 0057       0014         S.
$\lambda_{b}$ (Base Failure S, Ratic of Operating S, Ratic of Operating 13.0038 .0046 .0065 .0096 5.0038 .0049 .0067 .0099 5.0038 .00447 .0067 .0099 5.0038 .00442 .0072 .010 5.0042 .0053 .0074 .011 5.0042 .0053 .0067 .0099 5.0053 .0067 .0089 .011 5.0053 .0057 .0089 .011 5.0053 .0057 .0089 .011 5.0053 .0057 .0089 .011 5.0053 .0057 .0089 .011 5.0053 .0057 .0094 .011 5.0055 .0071 .010 5.0053 .0057 .0014 .011 5.0051 .0077 .010 5.0053 .0057 .0014 .011 5.0051 .0014 .011 5.0055 .0051 .0014 .011 5.0051 .0014 .011 5.0055 .0051 .0014 .011 5.0055 .0057 .0014 .011 5.0056 .0084 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0014 .011 5.0051 .0051 .0014 .011 5.0051 .0050 .0050 .0014 .011 5.0051 .0051 .0014 .011 5.0051 .0051 .0014 .011 5.0051 .0050 .0050 .0050 .014 .011 5.0051 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .0050 .005
Ab (Bas S. Ratic of O S. 0038 .0047 .0065 .0039 .0055 .0075 .0042 .0055 .0077 .0042 .0055 .0077 .0042 .0055 .0077 .0042 .0055 .0077 .0042 .0055 .0077 .0042 .0055 .0077 .0042 .0019 .0014 .011 .012 .015 .013 .014 .011 .013 .019 .014 .011 .013 .019 .014 .011 .013 .019 .014 .011 .013 .019 .014 .011 .013 .019 .014 .011 .014 .018 .022 .013 .0014 .017 .022 .013 .019 .017 .022 .013 .019 .019 .019 .019 .010 .010 .010 .010
S. Rat 00038 .00038 .00037 .00038 .00038 .00038 .00038 .00038 .00038 .00038 .00038 .00038 .00038 .000056 .00038 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .000056 .00005
S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S       S

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR TANTALUM ELECTROLYTIC (Non-Solid) CAPACITORS (MIL-C-39006, Style CLR and MIL-C-3965, Style ~L)

 $\lambda_{\rm P}$  =  $\lambda_{\rm b}$  (  $\pi_{\rm E}$  x  $\pi_{\rm Q}$  ) x 10<sup>-6</sup>

(Base Failure Rate) م ح

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	atio o		05	90	06	06	06	00	06	01	01	07	08	08	60	60	10	11	13	14	16	5	2	27	33	42	.0547	~
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 $\pi_{\rm E}$  (Environmental Factor)

Environment	ы Ц
Ground, Benign	
Space Flight	Ч
Ground, Fixed	2
Airborne, Inhabited	9
Naval, Sheltered	9
Ground, Mohile	6
Naval, Unsheltered	14
Airborne, Uninhab.	20
Missile, Launch	30

IIQ (Quality Factor)

0 II	1.0	• •	0.1	0.03	10.01
Level					
Rate	<u>ل</u> ا	: ሲ	æ	to	-3965
Failure		• • • •	14	51	MIL-C-3965

6.2-13 MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR ALUMINUM ELECTROLYTIC CAPACITORS (MIL-C-39018, Style CU (Aluminum Oxide)) FIGURE

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 $\lambda_{\rm p} = \lambda_{\rm b} ( \pi_{\rm E} \times \pi_{\rm Q}) \times 10^{-6}$ 

λ<sub>b</sub> (Base Failure Rate)

		0	64				G.		~	~	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	10		~	~		e		60	~	1							
			°,																									
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	ating t		610.	3	2	2	2	2	e	3	4	4	ഹ	Q	7	08											1.0	
	Oper	٠	.014	-	-	<b>H</b>	1	3	2	2	e	n	m	4	S	9	~	8	.10	.13	.16	.20	.26	.33	.44	• 58	. 78	<
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	S	.2	07	08	Ο	60	H	-	-1	Ч	Ч	<b>H</b>	2	2	2	S	n	マ	ഗ	7	ω	.10	.13	.17	.23	ίĩ.	.41	1
				07	008	600	E	10	01	Ч	5	01	01	02	2	03	m)	04	ហ	90	08						• 39	
	Ę	(c))	0	<u>س</u>	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90	95	0	0	-	-	120	¢

II (Environmental Factor)

Environment	$\pi_{\rm E}$
Ground, Benign	7
Space Flight	Ч
Ground, Fixed	2
Airborne, Inhabited	12
Naval, Sheltered	12
Ground, Mobile	12
Naval, Unsheltered	20
Airborne, Uninhab.	3ù
Missile, Launch	40

m\_Quality Factor)
Quality IQUPPER 1.0
Mil-Spec 3.0
Lower 10.0

6.2-14 MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR ALUMINUM DRY ELECTROLYTIC CAPACITORS (MIL-C-62)

FIGURE

 $\lambda_{\rm p}$  =  $\lambda_{\rm b}$  (  $\pi_{\rm E}$  x  $\pi_{\rm Q}$  ) x 10^{-6}

 $\lambda_{\mathbf{b}}$  (Base Failure Rate)

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(c))	.1	.2	• 3	•4	•5	• 6	.7	• 8	- 6.	1.0
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ຽ	0 H	H	12	14	18	24	32	42	56	73
10	01	12	БЧ	16	20	26	35	47	62	81
15		.0137	ഹ	.0180	.0228	.0299	9	.0531	0	16
20	4	15	17	2	25	33	4	60	79	03
25	10.	5	61	2	29	38	21	68	06	17
30	19	0	22	2	.0339	44	59	78	04	35
35	22	23	26	m	39	51	69	92	21	58
40	26	ω	E	.0370	46	-1	-1	08	43	87
45	.0322	.0336	.0372	.0444	.0561	.0736	98	.1306	.1724	.2246
50	σ	40	5	.0540	68	89	61	58	60	73
55	48	50	52	9	84	10	47	96	59	37
60	0	63	50	8	05	38	85	46	25	23
65	77	0	89	0	35	77	.2364	14	15	41
70	1	05	2	.1392	76	-1	01	60	40	04
75	34	39	പ്പ	8	.2336	00	0		2	S
80	8131.	1.1894	207	.2505	16	r-i	.5533	1.7369 <b>.</b> 1	72	66
85	1	62	90	.3465	.4382	75	9	.02031	46	2

(Quality Factor) цоп 10.0 10.0 Upper Mil-Spec Quality Lével LOWer а н

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viro	IVİFC	Id, E	ounc, r rborne,	•	<u>،</u>		sile,
	มัล	Ground Space	Ground, Airborne	Naval, Ground	Naval,	Airborne	Missi
ы П	L						1

(Environmental Factor)

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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FCR VARIABLE CERAMIC CAPACITOR (MIL-C-81) FIGURE 6.2-15

 $\lambda_{\rm p} = \lambda_{\rm b}$  (  $\pi_{\rm E} \times \pi_{\rm Q}$  ) x 10<sup>-6</sup>

2. BA

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λ<sub>b</sub> (Base Failure Rate)

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of Operating	• 9• 1	.0865 .13	.0905 .14	.0955 .15	015 .15	.1090 .17	.1182 .18	1.1299 .20	.1448 .22	.1639 .25	.1889 .29	.2222 .34	.2672 .42	.3297 .51	.4186 .65	.5486 .86	<b>7</b>
S, Ratio of	.4 .5	270 .050	282 .053	98 .056	317 6059	40 .064	369 .069	405 -076	52 .085	511 <b> .</b> 096	589 .111	93 1.130	34 .157	029 .193	306 .246	2	001   100
	• 3	12	13	13	.0147	15	11	18	.0209	23	.0273	32	38	.0476	0	63	
	.2	05	05	S	.0059	9	06	.0076	ω	.0096	H	13	15		24		
	.1	0023	.0024	.0026	0027	.0029	03	.0035	.0039	.0044	.0051	05	7	08	H	.0147	C
E	(0 <sup>0</sup> )				40												

IIE (Environmental Fac	Factor)	$\widehat{}$
Environment	ΠE	
Ground, Benign		
Space Flight		
Ground, Fixed	4	
Airborne, Inhabited	8	
Naval, Sheltered	8	
Ground, Mobile	8	
Naval, Unsheltered	24	
Airborne, Uninhab.	50	
Missile, I aunch	70	

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(Quality	Quality Level	Upper Mil-Spec Lower
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MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR VARIABLE, PISTON TYPE (Tubular Trimmer) CAPACITOR (MIL-C-14409)

 $\lambda_{p} = \lambda_{b}$  (  $\pi_{E} \times \pi_{Q}$  ) x 10<sup>-6</sup>

λ<sub>b</sub> (Base Failure Rate)

 •
89 .1131 69 .1531 47 .2073 47 .2073 53 .3800 92 .5145 63 .6966 84 .9432

(Environmental Factor) л<sub>Е</sub>

4	
Environment	ы =
Ground, Benign	F
Space Flight	٠
Ground, Fixed	•
Airborne, Inhabited	Ч.
Naval, Sheltered	ч.
Ground, Mobile	н.
Naval, Unsheltered	ບ •
Airborne, Uninhab.	α
Missile, Launch	

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Factor)	β <sup>π</sup>	1.0 10.0
(Quality	Quality Level	Upper Mil-Spec Lower

Style	MIL-C- SPEC	A .	В	N <sub>T</sub>	G	N <sub>S</sub>	н	FIGURE NOS. $^{\lambda}$ b
СВ	10950	8.9(10)-4	1	358	1	.3	3	6.2-5
сс	20	3.6(10) <sup>-9</sup>	1	25	1	.3	3	6.2-10
CE	62	4.2(10) <sup>-3</sup>	1	282	5.9	.55	3	6.2-14
CHR	39022	5.5(10) <sup>-5</sup>	2.5	358	1.8	.4	5	6.2-2
CHR	39022	5.5(10) <sup>-5</sup>	2.5	398	18	.4	5	6.2-3
СК	11015 Max Rated T=85°C	8.9(10)-4	1	358	1	.3	3	6.2-7
	Max Rated T=125°C	8.9(10)-4		398	l	.3	3	6.2-8
	Max kated T=150°C		1	423	1	.3	3	6.2-9
CKR	39014	See Styl	e CK.					
CL	3965	3.8(10) <sup>-3</sup>	1	358	9	.4	3	5.2-12
CLR	39006	See Styl	e CL.					
СМ	5	6.9(10) <sup>-10</sup>	16	398	1	.4	3	6.2-4
CMR	39001	6.9(10)-10	16	398	1	.4	3	6.2-4
CPV	14157	5.5(10) <sup>-5</sup>	2.5	338	18	.4	5	6.2-1
CPV	14157	5.5(10) <sup>-5</sup>	2.5	358	18	.4	5	6.2-2
CPV	14157	5.5(10) <sup>-5</sup>	2.5	398	18	.4	5	6.2-3
CQ & CQR	19978	See Styl	e CPV.					
CSR	39003	3(10) <sup>-3</sup>	1	358	9	.4	3	6.2-11
ເບ	39018	3.3(10) <sup>-3</sup>	3	358	5	.5	3	6.2-13
cv	81	1.5(10) <sup>-3</sup>	1	342	10.1	.17	3	6.2-15
CYR	23269	·3.3(10) <sup>-9</sup>	16	398	1	.5	4	6.2-6
PC	14409	1.46(10) <sup>-6</sup>	1	33	1	.33	3	6.2-16

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TABLE 6.2-2 CAPACITOR BASE FAILURE RATE  $(\lambda_b)$  FACTORS

6.2-22

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6.3 Operational/Non-Operational Failure Rate Comparison

Table 6.3-1 presents the operational failure rates and the operating to non-operating failure rate ratio. The operating failure rates were calculated using the MIL-HDBK-217B prediction models assuming the following factors:

For paper, mica, glass and ceramic capacitors, a voltage derating of 50 percent was assumed for a quality level 'M' part at 25°C.

For tantalum capacitors, a 50 percent voltage derating was assumed for a quality level 'M' part with ^.1 ohms per volt circuit resistance.

For aluminum electrolytic capacitors, a voltage derating of 50 percent for an upper quality level part was assumed.

For variable piston type capacitors, a 50 percent voltage derating was assumed for an upper quality level part at 25°C.

The comparison between operational and non-operational shows a higher failure rate in storage for paper and plastic capacitors.

Missile launch ratios were obtained directly from MIL-HDBK-217B. በሚያን አለ እስለ የቆጠቀም በት እስለ የሰላ እንደ እስት የሚያን እንደ እስት የሆኑ እንደ እስት የሆኑ እንደ እስት በት እስት እስት እስት እስት እስት እስት እስት እስት እ

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CAPACITOR OFERATING AND NON-OPERATING
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CAPACITOR
TABLE 6.3-1.

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MISSILE LAUNCH TO G.FOPER- ATING RATIO	10	7.5	7.5	7.5		10	15	20	40
G.F.~OPERATING TO NON-OPERATING RATIO	г.	1.2	S	67		80		9	9
GROUND, FIXED, OPERATING FAILURE RATE X 10 <sup>-9</sup>	4.	1.2	4.0	20.0		20.0	28.0	42.0	63 <b>.</b> 5
NON-OPERATING FALLURE RATE x 10-9	3.0	.97	0.8	0.3		.25	9.3	۲.۵	٥.11
DEVICE CATEGORY CAPACITORS	Paper & Plastic	Mica	Glass	Ceramic	Electrolytic	Tantalum Solid	Tantalum Non-Solid	Aluminum Oxide	Variable .

6.3-2

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#### 7.0 Inductive Devices

This section contains reliability analyses on inductive devices. Information has been collected and analyzed for the following types of devices: coils, filters and transformers.

## 7.1 Storage Reliability Analysis

#### 7.1.1 Non-Operational Failure Rate Predictions

The non-operational failure rates for the three types of components analyzed are shown in Table 7.1-1. The available storage data on filters did not report a single failure. The failure rate shown assumes one failure and therefore it is a worst case failure rate. No difference was apparent in the data between MIL-STD and Hi-Rel coils.

## TABLE 7.1-1. INDUCTIVE DEVICES NON-OPERATIONAL FAILURE RATES

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Device	$\frac{MIL-STD}{\lambda \text{ in FITS}}$	$\frac{\text{HI-REL}}{\lambda \text{ in FITS}}$
Filters & Chokes	9.6	.99
Coils & Inductors	1.3	.94
Transformers	13.9	.99

#### 7.1.2 Non-Operational Failure Rate Data

Information on inductive devices represents data from three sources with a total of over seven billion hours of storage for inductive devices. The breakdown of storage hours and failures for each device is shown in Table 7.1-2. Information as to the specific type of each device and quality levels is broken out by source in Tables 7.1-3, 7.1-4, and 7.1-5. TABLE 7.1-2. SUMMARY OF INDUCTOR NON-OPERATING DATA

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	8 8 8 8 8 8	MIL-STD	2 1 1 1 1 1	               	HI-REL	
DEVICE TYPE	STORAGE HOURS X 10 <sup>6</sup>	NUMBER	FAJLURE RATE IN FITS	STORAGE HOURS X 10	NUMBER FALLED	FAILURE RATE IN FITS
Filters & Chokes	104.	Ч	9.62	201.6.	8	.992
Coils & Inductors	744.	0	(<1.34)	1060.	Ч	.943
Transformers	649.	6	13.9	3037.	m	.988
Reactors	13.	0	(<76.9)	27.	0	(<37.0)

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SOURCE A NON-OPERATING DATA FOR INDUCTIVE DEVICES (MIL-STD) TABLE 7.1-3.

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FAILURE RATE IN FITS	(<13.1)	(<2.0) (<78.4) (<9.8)	<pre>(&lt;13.1) (&lt;39.2) (&lt;78.4) (&lt;39.2) (&lt;39.2)</pre>	(<7.1) (<39.2)	(<78.4)
NUMBER FAILED	o	000	0000	00	0
STORAGE HOURS X 10 <sup>6</sup>	76.562	497.656 12.760 102.083	76.562 25.521 12.760 25.521	140.364 25.521	12.760
NUMBER DEVICES	5244	34086 874 6992	5244 1748 874 1748	9614 1748	874
DEVICE TYPE	Filters General Class	Coils RF Toroidal IF	Transformers Reference Audio Power Signal	Inductors General Class Toroidal	Reactors

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SOURCE B NON-OPERATING DATA FOR INDUCTIVE DEVICES (HI-REL) TABLE 7.1-4.

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FAILURE RATE IN FITS	1.05	2.31	(<9.23)	(<120.)
NUMBER	2	н	0	0
STORAGE HOURS X 10	1907.989	433.255	108.314	8.332
NUMBER	145186	32968	8242	634
DEVICE TYPE	Filters General Class	Coils General Class	Transformers General Class	Reactors

SOURCE C NON-OPERATING DATA FOR INDUCTIVE DEVICES TABLE 7.1-5.

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HI-REL	FAILURE NUMBER RATE FAILED IN FITS	0 (<11.3)    0 (<99.6)	0 (<106.)	0 (<12.6) 0 (<3.5)	3 (<1.0)	0 (<3.8)	0 (<53.2)
1 1 1 1 1 1 1	STORAGE HOURS X 10	88.488 	9.437	79.181 285.800	2928.309	261.557	18.8
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	FAILURE RATE IN FITS	<pre>- (&lt;7936.) 2645. (&lt;2645.) (&lt;38.9)</pre>	(<1323.)	- (<185.)	17.7	I	ę
MIL-STD	NUMBER	104001	0	10	σ	t	I
8 9 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	STORAGE HOURS X 10	- 126 1126 - 378 - 378 - 378 	.756	- 5.418	509.000	ł	ı
	DEVICE TYPE	Filters General Class Ceramic Bandpass Ceramic Feedthrough Transmittal RC, Low Pass EMI	Chokes	Coils General Class RF	Transformers	Inductors	Reactors

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7.2 Inductive Devices Operational Prediction Models

The MIL-HDBK-217B general failure rate model for inductive devices is:

 $\lambda_{p} = \lambda_{b} (\Pi_{E} \times \Pi_{f}) \times 10^{-6}$ where:  $\lambda_{p}$  = device failure rate  $\lambda_{b}$  = base failure rate  $\Pi_{E}$  = Environmental factor  $\Pi_{f}$  = family type factor

Specific model parameter values are given in Figure 7.2-1 for MIL-T-27 Transformers and Inductors (Audio, Power and HiPower Pulse) and MIL-C-15305 Radio Frequency Coils; and in Figure 7.2-2 for MIL-T-21038 Low Power Pulse Transformers.

The base failure rate and adjustment factor values presented in the figures are based on certain assumptions. See sections 7.2.1 and 7.2.2 for a description of these parameters.

7.2.1 Base Failure Rate  $(\lambda_{b})$ 

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The equation for the base failure rate,  $\lambda_{b}$ , is:

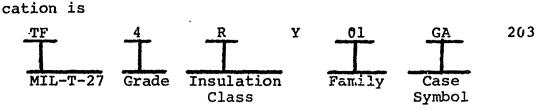
$$\lambda_{\rm b} = {\rm Ae}^{\rm X}$$
 where  ${\rm x} = \left(\frac{{\rm T}_{\rm HS} + 273}{{\rm N}_{\rm T}}\right)^{\rm G}$ 

 $T_{HS}$  = Hot stop temperature in degrees C, e is natural logarithm base, 2718,

A,  $N_{T}$ , and G are model equation constants The determination of hot spot temperature is described in Section 7.2.3.

The model equation constants are given in Tables 7.2-1 and 7.2-3. The models are valid only if  $T_{\rm HS}$  is not above the temperature rating for a given insultation class.

Devices in accordance with the three specifications included in this section are identified by the classification scheme used in each specification. The following information will help in determining the Insultation Class, the Family Type and the Construction Grade if only the specification and type designation are known: a. MIL-T-27. An example type designation per this specifi-



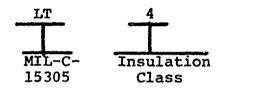
The Grade and Insulation Class symbols are the same as used in Figures 7.2-1 and 7.2-2. The codes used for Family Type are

> Power transformer + filter: 01 thru 09, 37, thru 41 Audio transformer: 10 thru 21, 50 thru 53 Pulse transformer: 22 thru 36, 54

> > 001

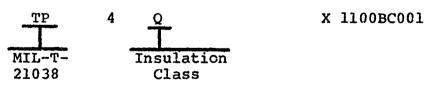
b. MIL-C-15305. All parts in this specification are r.f. coils. An example type designation is

K



The codes used for the Insulation Class are Class B: 4, 5, 6 Class 0: 7, 8, 9 Class A: 10, 11, 12

c. MIL-T-21038. All parts in this specification are pulse transformers. An example type designation is



The Insulation Class symbols are the same as used in Figures 7.2-1 and 7.2-2.

## 7.2.2 I Adjustment Factor

# 7.2.2.1 Environmental Adjustment Factor, $M_{\rm E}$

 $I_E$  accounts for the influence of environmental factors other than temperature. Refer to the environment description in the Appendix.

Grade 6 transformers require adequate environmental protection through encapsulation, or sealing; otherwise, application in any of these environments is unacceptable, and values not valid.

## TABLE 7.2-1.

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MODEL EQUATION CONSTANTS, MIL-T-27 INSULATION CLASS & MAX OPERATING TEMP. (MIL-C-15305 Class in Parenthesis)

#### Insulation Class

Constants	Q (O) 85°C	R (A) 105°C	S (B) 130°C	V* 155°C	т* 170°С	U* >170°C
A	6.37x10 <sup>-4</sup>	$7.20 \times 10^{-4}$	6.06x10 <sup>-4</sup>	$1.83 \times 10^{-3}$	$2.03 \times 10^{-3}$	2.6x10 <sup>-3</sup>
N <sub>T</sub>	329	352	364	409	398	477
G	15.6	14.0	8.7	10.0	3.8	8.4

\* Temperature ratings for these "letters" are different from Table 7.2-2.

## TABLE 7.2-2.

#### MODEL EQUATION CONSTANTS, MIL-T-21038 INSULATION CLASS & MAX OPERATION TEMPERATURE

#### Insulation Class

Constants	Q 85°C	R 105°C	s 130°C	т* 155°С	U* 170°C	V* >170°C
A	6.37x10 <sup>-4</sup>	$7.20 \times 10^{-4}$	6.06x10 <sup>-4</sup>	$1.83 \times 10^{-3}$	$2.03 \times 10^{-3}$	2.6x10 <sup>-3</sup>
N <sub>T</sub>	329	352	364	409	398	477
G	15.5	14.0	8.7	10.0	3.8	8.4

\* Temperature ratings for these "letters" are different from Table 7.2-1.

FIGURE 7.2-1 MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR MIL-T-27, TRANSFORMERS AND INDUCTORS (AUDIU, POWER & HI POWER PULSE) AND MIL-C-15305, COILS, RADIO"FREQUENCY

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 $\lambda_{p} = \lambda_{b}$  (  $\pi_{E} \times \pi_{f}$  ) X 10<sup>-6</sup>

MIL-T-2	7, Ba	Fai		Rate, $\lambda_{h}$	**	(MIL-C-1530	S	ass	in Pare	Parenthese	
5	1	S (B)	Δ*	· · · ·	*0		R (A)	(8) S	×A	Tu*	40
ບ	10°°C	130°C	155°C	170°C	>170°C	$\mathbf{T}_{\mathrm{HS}}$	105°C	130°C	155°C	170°C	>170°C
		.0007	5	02			04	5		.0042	
			5	2	2	0	.0068	02			.0030
	0	.0000		02		0	O	02	2	.0046	
01	.0008	.0007	0	.0027	.0026	110		.0029	.0031	.0049	.0031
08	00	O	5	02	02	<b>H</b>		03	03	ហ	
0	0		10	02	2	2		04	03		.0032
0	00		10	02	02	2		05	04	05	ε
0	00		Ч	03	2	ŝ		06	4	05	03
-	00	.0008		m	.0027	S			4	Q	
Ч	Ο	.0008				4				9	
Ч	-H				2	4				9	
Ч	-	.0009			2	ŝ				5	.0037
2	н		2	.0034	2	S			.0088	5	.0039
	0		2	03	02	Ö				ω	.0041
4	Ч	1100.	2	n	2	Ó				ω	.0042
7		.0012	.0022			~				60	.0045
	2	.0013	.0023		.0028	5					
9		.0014	.0024	.0040	.0028	œ					.0050
	1.0034	.0016	.0025	.0041	.0029	8					.0053
ipei	Temperature	rating	s fo	0	"letter		re d	44	from	Figure	7.2-2.
th	ere is	no A <sub>h</sub>	for a	given	Tuc and	I Cla	ss, ð	>	s over	н Т	•
					110						

 $\pi_{\mathrm{F}}$  (Family Type Factor)

		ľ	
ramity Type	Upper	MIL-Spec	LOWer
ansformers	1.0	1.5	5.0
ransformers	1.5	3.0	7.5
Transformers and Filters	4.0	8.0	20.0
Transformers and Coils	6.0	12.0	30.0

IE (Environment Factor)

Environment	ΠΕ
Ground, Benign	Ч
Space Flight	Ч
Ground, Fixed	2
Ground, Mobile	m
Airborne, Inhab.	ŝ
Naval	ŋ
Airborne, Uninhab.	7
Missile, Launch	10

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MIL-HDBK-217B OPERATIONAL FAILURE EATE MODEL FOR MIL-T-21038, TRANSFORMERS, PULSE, LOW POWER FIGURE 7.2-2

 $\lambda_p = \lambda_b$  (  $\pi_E \times \pi_f$  ) x 10<sup>-6</sup>

 $\lambda_{\rm b}$  (Base Failure Rate for MIL-T-21038) \*\*

				Q					4	~>>>+		
	a	R	S	1×	n*	Λ*		R	S	11 ×	*11	1/*
THS HS	85°C	105°	130°C	155°C	170°C	>170°C	TES	0	0	155°C	170°C	>170°C
0	00	<u> </u>	0	01	02	02	95	0	8	002	4	02
2	00	000.	00	5	02	02	C	9	02	002	40	(m
10	80	.000	00	Ч	02	02	0	10	02	002	04	03
12	00	000.	00	Ч	02	02	Ч		02	03	04	03
20	00	0000	00	10	02	02	-1		003	003	05	03
25	.0008	000.	.0001	.0019	.0028	2	120		004	.0036	.0053	0.00
30	00	.000	00	5	02	02	2		05	003	005	03
35	00	.000	00	5	03	03	3		90	004	05	03
40	10	0000	80	0 <b>2</b>	03	02	ŝ			004	000	03
45	01	000.	00	02	03	02	4			002	000	03
50	5	100.	00	02	03	02)	1			90	000	03
ίΩ Π	5	100.	80	02	603	02	S	-7		0.7	002	03
60	02	100.	10	02	603	02	ഗ			008	07	03
65	02	100.	5	2	03	02	9			•	080	04
70	04	100.	10	02	03	02	9				08	04
75	07	.001	ч	02	03	02	7				60	04
80	12	.002		2	603	02	7					4
85	26	002	.0014	.0024		0	180	<b>1</b>				Ō
O		003	.0016	02	.0041	N	185					002
1 1	Tempera Tf the	tur	ting	for	hese	lette	ar H	dif	ent	шол	Jur	•
			10 Ab S	I UMOU	or a g	LVen T <sub>F</sub>	S S S	lass,	device	is ov	'er-rat	Ŏ

Factor)	
Type	
$\pi_{\mathbf{F}}$ (Family	

$\pi_{F}$ (Family Type F	Factor)	-		IIE (Environment Factor)	tor)
Family Type	Upper	Upper Mil-Spec Lower	Lower	Environment	<u>ل</u>
Pulse Transformers	1.0	1.5	5.0	Ground, Benian	1
Audio Transformers	1•5	о. С	7.5	Space Flight	
Power Transformers and Filters	4.0	8.0	20.01	14 7	2
RF Transformers and Coils	6.0	12.0	30.0		e
				rne	2 L
					1

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Launch

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7.2.3 Hot Spot Temperature

The failure rate,  $\lambda_p$ , of the inductive device is a function of the hot spot temperature of the inductive device. This hot spot temperature can be obtained by direct measurement or by approximation. Although the latter method is normally used, there may be times when the direct measurement technique would be advisable.

#### 7.2.3.1 Determination of Hot Spot Temperature - Direct Measurement

a) Average Temperature Rise, Change in Resistance Method as described in MIL-T-27 (4.8.14) or MIL-T-21038 (4.7.14)

$$\Delta T = \frac{R - r}{r} (t + 234.5) - (T - t)$$

where

- AT = Temperature rise in degrees Centigrade above specified maximum ambient temperature
- R = resistance of winding in ohms at temperature  $(T + \Delta T)$
- r = resistance of winding in ohms at temperature
   (t)
- t = specified initial ambient temperature in degrees Centigrade
- T = maximum ambient temperature in degrees Centigrade (at time of power shutoff); T shall not differ from t by more than 5°C.

For transformers, rated voltage shall be applied to the primary with the specified loads across the secondaries. For inductors, rated d-c and a-c, current shall be applied to the windings.

b) Hot Spot Temperature Rise

Approximate value by assuming temperature-rise of hot spot is 10 percent greater than highest average temperature-rise as measured or as estimated by approximate methods. See para. 7.2.3.2.

Actual measurement requires burying of thermocouples or thermistors in coils; hence is not feasible to measure on complete part. However, for developmental devices, this step should be seriously considered where temperature is significant.

## 7.2.3.2 Determination of Hot Spot Temperature - Approximation

Approximation of the hot spot temperature can be determined by referring to Figures 7.2-3 through 7.2-6. which gives the average temperature rise. Use the figure which best correlates to the known input data. If Figure 7.2-4 is used to determine the temperature, use of a MIL-T-20138 transformer, case AF will give the most practical result. The hot spot temperature is then calculated as follows:

> $T_{HS} = T_A + 1.1$  (T)  $T_{HS} = Hot$  spot temperature (C°)  $T_A = ambient$  temperature (C°)  $\Delta T = temperature$  rise (C°)

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When using Figures 7.2-3 through 7.2-6, it is advisable to follow the order of precedence established via Table 7.2-3.

TABLE 7.2-3 ESTIMATE OF AVERAGE TEMPERATURE-RISE\*

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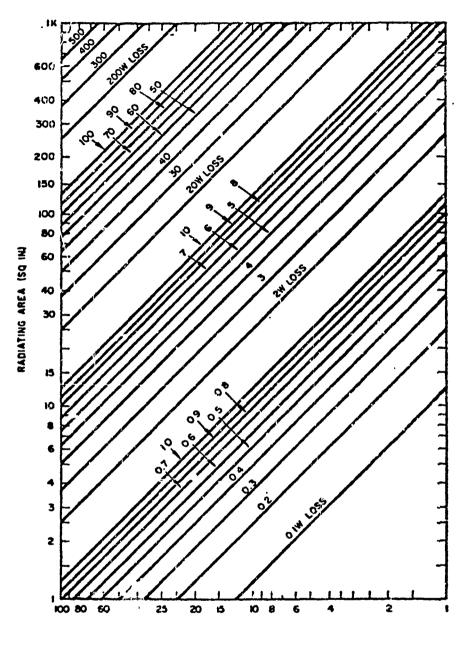
preferred include heat losses due to assumption; use both radiation and convecpossible because of actual and weight of conventional relationship between size Note error possibility in \*\*Graphs give predicted temperature rise in still air and in absence of nearby heat \*Hot-Spot Température = Ambient Air Temperature plus 1,1 times average temperature radiation from other components, if forced air cooling or heat radiation is used, Figure 7.2-3, and 7.2-6 Radiating area readings Cise symbols represent It is preferable to measure transformer temperature under operating conditions. standard case sizes. This calculation is tion. This method for MIL-T-21038.& Comment transformers, preferably. efficiency MLL-C-15305. 2 0 с 0 symbol on ordinate, locate Average Temperature-Rise\*\* graph with radiating read probable temperatureriate line for power loss and read temperature-rise on absrissa. To Calculate Approximate intersection with appropriate line for power loss and read temperature-rise sections with appropriate temperature-rise intersection with approparea on ordinate, locate section with appropriate line for power input and Enter graph with weight Enter graph with weight abscissa; locate interpower and loss abscissa; locate inter-Measure power loss or input at normal use frequency. graph with case rise on ordinate. on abscissa; on ordinate. line for and read rise (or measured coil temperature). Enter Enter (watts) Power loss (watts) Power loss (watts) Radiating surface Case symbol per Input Data area of case Transformer Power input Transformer Power loss weight (1b) weight (lb) 80 efficiency MIL-T-27 (sq in.) Assumed percent (watts) (Step 1D) (Step 1B) (Step 1C) Reference (Step 1A) Figure Figure Figure Figure . 2-5 7.2-6 7.2-3 7.2-4

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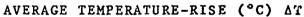
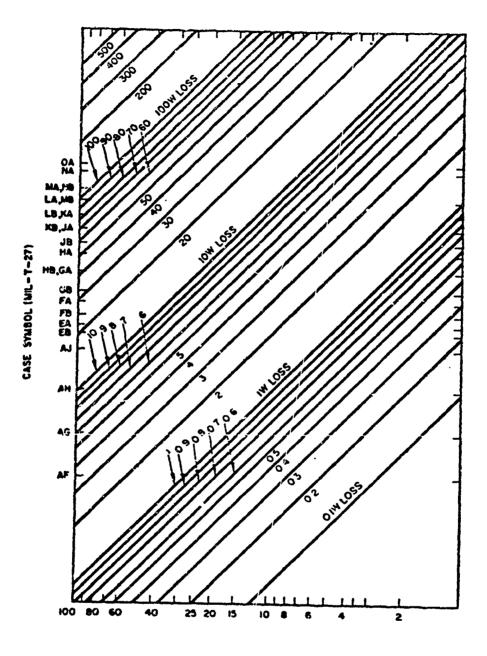


FIGURE 7.2-3. POWER LOSS AND RADIATING AREA KNOWN: ESTIMATE AVERAGE TEMPERATURE-RISE (Step 1A)



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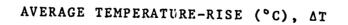
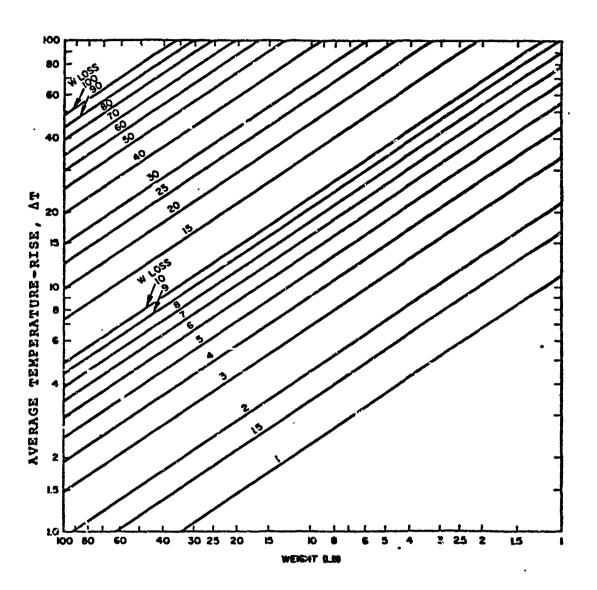


FIGURE 7.2-4. POWER LOSS AND CASE SYMBOL KNOWN: ESTIMATE AVERAGE TEMPERATURE-RISE (Step 1B)



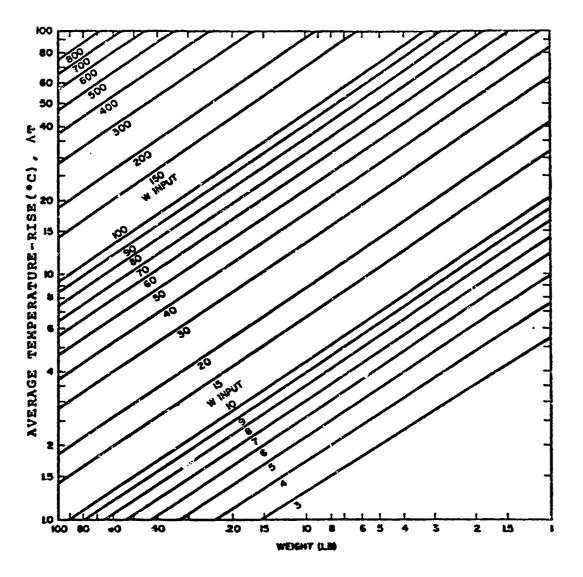
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FIGURE 7.2-5. POWER LOSS AND WEIGHT KNOWN: ESTIMATE AVERAGE TEMPERATURE-RISE (Step 1C)



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FIGURE 7.2-6. POWER INPUT AND WEIGHT KNOWN: ESTIMATE AVERAGE TEMPERATURE-RISE (Based on 80 PERCENT EFFICIENCY) (Step 1D)

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7.3 Operational/Non-Operational Failure Rate Comparisons

Table 7.3-1 summarizes the operational to non-operational failure rate ratios. Operational failure rates were computed using the models in Section 7.2 with the following assumptions.

a) For coils a hot spot temperature of 20°C was assumed.

b) For transformers insulation class "Q" and a temperature rise of 20°C were assumed.

The missile launch to ground, fixed operating ratio was obtained directly from MIL-HDBK-217B

TABLE 7.3-1. INDUCTIVE DEVICES OPERATING AND NON-OPERATING FACTORS

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DEVICE CATEGORY DIODES	NON-OPERATING FAILURE RATE X 10 <sup>-9</sup>	GROUND, FIXED, OPERATING FAILURE RATE x 10 <sup>-9</sup>	G.FOPERATING TO NON-OPERATING RATIO	MISSILE LAUNCH TO G.FOPER- ATING RATIO
Filters Coils Transformers -Std	. 99 49.	9、6 6.4 9.6	10 7 10	សល
Filters Coils Transformers	9.6 1.3 13.9	12.8 19.2 19.2	1.3 1.5 1.4	ហហ

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## 8.0 Crystals

This section contains reliability information and analysis on crystals. Available information did not specify crystal material, therefore the failure rate must be considered only under the general classification of crystals.

#### 8.1 Storage Reliability Analysis

## 8.1.1 Non-Operational Failure Rate

The non-operational failure rate for crystals was estimated at 44 failures per billion hours.

#### 8.1.2 Non-Operational Failure Data

Forty five million storage hours of crystals with two failures were reported.

## 8.2 Operational Failure Rate Information

The operational failure rate for quartz crystals is listed in MIL-HDBK-217B as 0.2 failures per million hours.

## 8.3 Operational/Non-Operational Failure Rate Comparison

Operational to non-operational failure rate ratio for crystals is 5 based on the above failure rates.

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### 9.0 Batteries

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This section contains reliability information on batteries. Missile battern are usually one shot devices. However, being chemically activated devices, batteries are susceptible to degradation after lon prieds of storage. The available information did not permit evaluation of aging characteristics.

## 9.1 Storage Reliability Analysis

#### 9.1.1 Failure Modes and Mechanisms

The principal failure modes and mechanisms and corrective measures for nickel-cadmium batteries are summarized in Table 9.1-1.

### 9.1.2 Guidelines for Long Life Assurance

## 9.1.2.1 Design Guidelines

a) Design excess capacity into the battery to reduce the percent depth of discharge and compensate for capacity decrease with usage. The penalty is cost and watt-hours/pound;

 b) The negative to positive plate area should be at least
 1.5:1 so that the negative plate area can absorb the oxygen generated during recharging, preventing battery overpressure;

c) Use non-woven polyproplene separators since they degrade slower than nylon at higher temperatures. The non-woven configuration wets more readily;

d) Hermetically seal the battery to avoid degradation of other parts by the electrolyte;

e) Either plate the terminal seal braze with nickel or consider using a nickel-titanium braze material to reduce the probability of electrolyte attacking materials containing copper;

f) Use 304 or 304L stainless steel for case and cover material. These materials have proven satisfactory;

g) Use ceramic to metal terminal seals that are more KOH resistant than glass.

### 9.1.2.2 Process Control Guidelines

a) Employ clean areas during processing and manufacturing to reduce the amount of harmful contaminants. Also, use clean

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lintfree cotton gloves when handling components. Store components in clean plastic bags when not being processed;

 b) Employ clean processes, remove the carbonates and keep the nitrates content down to prevent gas pockets that pop off active material;

c) Flush plates after KOH is used in the process to form active hydroxides to remove carbonates;

d) Flush and brush plates prior to installation to remove contaminants;

e) Coin plates flat. Flex and clean plates prior to assembly. Have resident inspector examine plates for conformity just prior to cell assembly. These actions will reduce the probability of short by either projection of jagged wire filament through the separator or loose particles of plate material or sometimes tab failures;

f) Weigh each plate to be certain weights are within  $\pm 3 1/2$ % of mean. Also, perform actual capacitance measurements to check plate matching. Mismatched cells can prevent full battery charge.

g) Control the brazing temperature-time relationship to prevent excess dwell during brazing operations that can cause active material penetration of ceramic seals;

h) Avoid rapid cocling after brazing to prevent cracked ceramics and brazing voids.

i) Purge cells of air prior to injecting electrolyte to prevent KOH reacting with CO<sub>2</sub> to form carbonates;

j) Place plates under serialized control and provide traceability for separators and electrolyte material to improve the quality of individual cells which has varied more than desired;

k) Require process and test controls for each active element -- plates, separators and electrolyte to reduce end product variability.

9.1.2.3 Test Guidelines

a) Helium leak check the assembled cells. Option-chemical leak check with phenolphthalein;

9.1-2

b) Subject battery during acceptance test to a minimum of three charge/discharge cycles, high impedance short test, and leakage tests. These tests should provide assurance that the basic operating characteristics and construction are satisfactory;

c) X-ray along three axes to find gross battery defects;

d) Conduct a minimum of 30 charge/discharge cycles on assembled cells to eliminate infant mortality and to confirm these tests.

9.1.2.4 Application Guidelines

a) Maintain battery within a -20°C to +22°C temperature range to retard separator deterioration;

b) Store Ni-Cd batteries discharged, shorted and about 0°C to obtain a storage life of about five years.

## 9.1.3 Non-Operational Failure Rate Data

A total of .2 million storage hours without a single failure were reported. Since no failures occurred and the specifics of the stored batteries were not available it was impossible to assess the aging characteristics.

Based on this information, the failure rate of batteries is less than 5000 failures per billion hours.

# TABLE 9.1-1. FAILURE MECHANISM ANALYSIS - NICKEL CADMIUM BATTERIES

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Part and Function	Tailure Mode	Effect on Battery Output	Rel. Rank	Failure Mechanisms	How to Eliminate/Minimize Failure Mode
A. Plates (Contain charge)	Loss of active material	Lessens capa- city available	2	<ol> <li>Permanent passivation</li> <li>Shedding</li> <li>Redistribution or migra- tion of Cd</li> </ol>	<ol> <li>Operate within 0 to 22°C range.</li> <li>Use proper plate geometry for greater heat dissipation.</li> <li>Don't overcharge excessively.</li> <li>Employ clean processes, recove nitrates and keep carbonate content down to prevent gas pockats from forming underneath that pops off material.</li> <li>Provide excess of cadmium oxide.</li> <li>Start with battery with excess capacity, penalties permitting.</li> </ol>
	Short	Lower capacity Lowers voltage High tempera- tures		<ol> <li>Plate tabs broken, burned or shortened against cace or other plate</li> <li>Plate buckling</li> <li>Projections of jagged wire filaments pane- trates separators.</li> <li>Loost particles of plate material or metallic particales introduced during processing.</li> <li>Hechanical environments.</li> </ol>	<ol> <li>Don't weld tabs on - make part of substrate. Use wider tabs. Option: coin plates -&gt; receive welded tab.</li> <li>Coin plates including all four edges, smooth.</li> <li>X-ray for misalignment deter- mination.</li> <li>Employ clean processes and materials. Flex and brush off plates just prior to assembly.</li> </ol>
	Plate mis- matches	Capacity decreased		<ol> <li>Active material applied uneven or wt. out of tolerance.</li> </ol>	<ol> <li>Require wt. of plates to be within ±3% of that required.</li> </ol>
	Henory	Capacity avail- able limited.		<ol> <li>Temporary passivation.</li> <li>Depressed operating voltage</li> </ol>	<ol> <li>Completely discharge, short, and recharge to wipe out most of memory.</li> </ol>
	Contam- inates	Lower voltage & current		Carbonate contaminates in plates.	<ol> <li>Brush and flush plates prior to sealing cells.</li> </ol>
B. Separators (separate, insulate, absorb, and con- ducts)		Capacity decrease	1	Separator deterioration including dissolved, burned, pinpoint penetration, and impregnated with negative plate material.	<ol> <li>Limit operating temp. range of battery to 0 to 22°C; 0°C pra- ferred.</li> <li>Use alkali resistant material such as polyproplene or nylon.</li> <li>Strict material and process controls.</li> <li>Perform insulation resistance tests on material.</li> </ol>
	Contam- inates	Lower voltage & currant		Material deteriorates, car- bonater formed.	<ol> <li>Use polypropleme for long-life applications.</li> <li>Low battery temps (0°C) retards deterioration.</li> </ol>

\* Extracted directly from Reference 1.

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# TABLE 9.1-1. FAILURE MECHANISM ANALYSIS-NICKEL CADMIUM BATTERIES (cont'd)

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Fart and Function		Effect on Battery Output	Rel. Rani		How to Eliminate/Minimize Failure Hode
	Foor KOH absorp- tion and distri- bution	Higher temper- atures. Lower capacity over charging. High volcage on charge and low voltage on dis- charge	1.	Improper material and veave configuration.	<ol> <li>Don't use woven nylon.</li> <li>No non-woven configurations except for nylon material. (Polypropleme more difficult to wet than nylon.)</li> </ol>
C. Case (Cont and a port)	up-	Lower capacity, eventually be- coming an open circuit.	3	<ol> <li>Oxygen overpressure due to overcharging.</li> <li>Seal or veld leskage or failure.</li> <li>KOH-case material not compatible.</li> <li>Under designed structure</li> </ol>	<ol> <li>Employ high pressure relief valve/ burst disc for manned mission.</li> <li>Limit overcharge, especially above 80% full charge (third electrode, coolometer, voltage limit, thermistor, stabistor or 2-step regulator).</li> <li>Proper ratio of negative to positive plate capacity.</li> <li>Proper quantity of electrolyte- just enough to wet plates and separator.</li> <li>Leak test assembled cell.</li> <li>Proper process control. Weld per MIL-W-8611A. Passivate per MIL-F-14072, finish 300.</li> <li>Use 304L, cond. A per QQS - 766 or equiv.</li> <li>Ceramic-to-metal seal preformed. Suggest stress relieving design such as a "floating" seal. Con- sider redundant sealing surfaces.</li> </ol>
	Post to cell cover short	Loss of capa- city, heating		1. Ceramic failure 2. Electro-metallic bridging across ceramic	1. Minimize quantity of braze used with attention given to its elimination on interior side.
D. Elect lyte	TO- Franze	No output.	5	1. Low temperatures.	1. Keep storage tamp. abovo - 48°C.
1	Contami- nate			2. Carbonate'é nitrate contrainates	<ol> <li>List carbonate and mitrate con- centrations to 0.01 gm/liter and 1 mg/liter or less respec- tively.</li> <li>Don't expose to air as KOH has infinity for CO2.</li> </ol>
E. Inter Elect cal c necti (Cond curre	ri- on- ons uct	Partial or com- plate loss of capacity, vol- tage.	4	<ol> <li>dechanical breakage of cell terminals, plate lugs or welded joints.</li> </ol>	<ol> <li>Strict QG.</li> <li>Avoid overly severe dynamic stresses during usage.</li> </ol>

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## 9.2 Operational Failure Rate Data

Operational data collected consisted of three different battery types as shown in Table 9.2-1.

#### TABLE 9.2-1. BATTERY OPERATIONAL FAILURE DATA

BATTERY	NO. OF FAIL.	OPERATING HRS.	$\lambda \times 10^{-6}$
A	2	60	33333
В	6	1580	5084
С	9	29750	302

The wide discrepancies in failure rates suggest different battery types and applications. Unfortunately the detailed information to verify this is not available. By pooling all the information in Table 9.2-1, the average failure rate is 542 failures per million hours.

### Reference:

MCR-72-169, Volume 3, Long Life Assurance Study for Manned Spacecraft Long Life Hardware, K. W. Burrows, Martin Marietta Corp., dated September 1972.

# 10.0 Connections and Connectors

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## 10.1 Storage Reliability Analysis

The available data on storage failure rate of electrical connections and connectors is shown in Table 10.1-1.

The average failure rate for the data in Table 10.1-1 is 0.13 fit, but all of the failures occur in one classification. Statistical analysis shows that the classification containing the failures is wildly discordant: the expected number of failures for 11603 hours is 1.486 and the probability of seeing even as many as 10 failures in this number of hours is less than 0.00001. Unfortunately, this classification is not further identified, and except for the submarine data, it is not clear to what it could be compared.

The line of data containing the 17 failures gives a worst case failure rate of 1.46 fit. Pooling the remaining data gives a gest case failure rate of .0080 (one failure assumed).

Combining the three sets of data referring to pins gives a total of 80,071.4 million hours with no failures, which gives 90% confidence that the true failure rate lies below 0.028 fit.

Combining the three sets of data referring to soldered connections gives a total of 35,385 million hours with no failures, which gives 90% confidence that the true failure rate lies below 0.065 fit.

STORAGE FAILURE DATA FOR ELECTRICAL CONNECTIONS TABLE 10.1-1.

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Comment	Soldered	stud and nut 20 pin, gold plated	Soldered	Welded	Pins	General	Submarine, general	Pins	Soldered	
Hours (million)	169. 24 E	24.5 163.	316.	5580.	47.4	11603.	6.3	79861.	34900.	136.115
Failures	0 0	00	0	0	0	17	0	0	0	17
Source	A a	A A	æ	В	Д	υ	υ	υ	U	
Failure rate (fit	1 1	I	I	8	ł	1.5	I	•	ł	

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## 10.2 Connector and Connection Operational Prediction Models

#### 10.2.1 Connectors

The MIL-HDBK-217B general failure rate model for a mating pair of connectors is:

$$\lambda_{\rm p} = [\lambda_{\rm b} (\Pi_{\rm E} \times \Pi_{\rm p}) + N\lambda_{\rm cyc}] \times 10^{-6}$$

where:  $\lambda_{p} = \text{device failure rate}$ 

 $\lambda_{b}$  = base failure rate

 $I_{r} = Environmental Adjustment Factor$ 

 $\Pi_{p}$  = Pin Quantity Adjustment Factor

N = Number of active pins

 $\lambda_{\rm cyc}$  = Cycling Rate Factor

The term containing  $\lambda_{\rm cyc}$  may be ignored for connectors experiencing cycling rates  $\leq 40$  cycles/1000 hr. Figure 10.2-1 gives the connector model and parameter values. Use of the model requires identification of insert materiel. Table 10.2-1 lists insert materiels classifications for the various types of connectors and Table 10.2-2 identifies these insert materiel classifications and the temperature ranges.

The base failure rate and adjustment factor values presented in Figure 10.2-1 are based on certain assumptions. See Sections 10.2.1 and 10.2.2 for a description of these parameters.

10.2.1.1 Base Failure Rate  $(\lambda_{\rm b})$ 

The equation for the base failure rate  $\lambda_{\rm b}$  is:

$$\begin{array}{l} \lambda_{\rm b} = {\rm A} \ {\rm e}^{\rm X} \\ {\rm where} \quad {\rm x} = \left( \begin{array}{c} {\rm T} + 273 \\ {\rm N}_{\rm T} \end{array} \right)^{\rm G} + \left( \begin{array}{c} {\rm T} + 273 \\ {\rm T}_{\rm G} \end{array} \right)^{\rm P} \\ {\rm e} = 2.718 \, , \, {\rm natural \ logarithm \ base} \\ {\rm T} = {\rm cperating \ temperature \ (^{\circ}{\rm C})} \, . \\ {\rm = \ ambient \ + \ temp. \ rise \ (See \ Table \ 10.2-4)} \, . \\ {\rm A}, \ {\rm T}_{\rm O}, \ {\rm N}_{\rm T}, \ {\rm G \ and \ P \ are \ model \ constants \ (See \ Table \ 10.2-3)} \, . \end{array}$$

MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL FOR CONNECTURS FIGURE 10.2-1

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 $\lambda_p = [\lambda_b (\pi_E \times \pi_p) + N\lambda_{cyc}] \times 10^{-6}$ 

A<sub>b</sub> (Base Failure Rate)

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the two insert types two types of insert material, the base failure rates for if a mating pair of connectors uses use the average of \*For  $\lambda_{b}$ ,

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Configuration	Specification	In	sert Ma Table	terial 10.2-2	
		Ā	В	C	D
Rack and Panel	MIL-C-28748 MIL-C-83733 MIL-C-24308	х	X X X		
Printed Wiring Board	MIL-C-21097 MIL-C-55302		x x		
Cable, Circular	MIL-C-5015 MIL-C-26482 MIL-C-38999 MIL-C-81511 MIL-C-83723	x x	X X X X X		x x
Power Coaxial, RF	MIL-C-3767 MIL-C-3607 MIL-C-3643 MIL-C-3650 MIL-C-3655 MIL-C-25516 MIL-C-39012			X X X X X X X	х

## TABLE 10.2-1. CONFIGURATION, APPLICABLE SPECIFICATION, AND INSERT MATERIAL FOR CONNECTORS

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## TABLE 10.2-2. TEMPERATURE RANGES OF INSERT MATERIALS

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Туре	Common Insert Materials	Temperature Range, °C *
A	Vitreous Glass, Alumina Ceramic, Polyimide	-55 to 250
В	Diallyl Phthalate, Melamine, Fluorosilicone, Silicone Rubber, Polysulfone, Epoxy Resin	-55 to 200
с	Polytetrafluoroethylene (Teflon) Chlorotrifluoroethylene (Kel-F)	-55 to 125
D	Polyamide (Nylon), Polychloroprene (Neoprene), Polyethylene	-55 to 125

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\* These temperature ranges indicate maximum capability of the insert material <u>alone</u>. Connectors using these materials generally have a reduced temperature range caused by other considerations of connector design. See applicable connector specification for connector operating temperature range.

Constants	Insert Material (see tables 10.2-1 and 10.2-2)								
	A	В	С	D					
A	0.324	6.9	3.06	12.3					
т <sub>о</sub>	473	423	373	358					
N <sub>T</sub>	-1592	-2073.6	-1298	-1528.8					
G	-1	-1	-1	-1					
Р	5,36	4.66	4.25	4.72					

## TABLE 10.2-3. MODEL CONSTANTS

TABLE 10.2-4.INSERT TEMPERATURE RISE (°C) vs.CONTACT CURRENT & CONTACT SIZE

AMPERES PER CONTACT	22 Ga.	20 Ga.	16 Ga.	12 Ga.
2 3 4 5 6 7 8 9 10 15 20 25 30 35 40	3.7 7.7 13. 20. 27. 36. 46. 58. 70.	2.4 5.0 8.5 13. 18. 24. 30. 37. 45. 95.	1.0 2.2 3.7 5.5 7.7 10. 13. 16. 20. 41. 70. 105.	0.4 0.8 1.4 2.0 2.8 3.7 4.8 5.9 7.2 15. 25. 38. 53. 71. 91.

CONTACT SIZE

NOTE: 1:  $\Delta T = .989(i)^{1.85}$  for 22 gauge.  $\Delta T = .64(i)^{1.85}$  for 20 gauge.  $\Delta T = .274(i)^{1.85}$  for 16 gauge.  $\Delta T = 0.1(i)^{1.85}$  for 12 gauge.  $\Delta T = ^{\circ}C$  insert temperature rise. i =amperes per contact

NOTE 2: The operating temperature of the connector is usually assumed to be the sum of the ambient temperature surrounding the connector plus the temperature rise generated in the contact. If the connector is mounted on a suitable heat sink (not or cold plate), the temperature of this sink is usually taken as the ambient. For those circuit design conditions which generate a contact hot spot, this hot-spot temperature rise is added to the ambient to obtain the operating temperature.)

## 10.2.1.2 Adjustment Factors

10.2.1.2.1 Invironmental Adjustment Factor, T<sub>E</sub>

 $I_E$  accounts for the influence of environmental factors other than temperature. Refer to the environment description in the Appendix.

10.2.1.2.2 Pin Quantity Adjustment Factor, IIp

I accounts for the quantity of contacts. For coaxial and triaxial connectors, etc., the shield contact is counted as an active pin.

$$\Pi_{p} = e \left( \frac{N-1}{N_{O}} \right)^{q}$$
where  $N_{O} = 10$ 
 $q = 0.51064$ 

N = Number of active pins

10.2.1.2.3 Cycling Rate Factor,  $\lambda_{cyc}$ 

 $\lambda_{cyc}$  adjusts the model for cycling rates. The term is ignored for connectors experiencing cycling rates  $\leq 40$  cycles/1000 hr.

The values for  $\lambda_{cyc}$  are derived from the following equation:

 $\lambda_{\rm cyc}$  = .001 e <sup>(f/100)</sup>

where f is the cycling rate in cycles/1000 hrs.

### 10.2.2 Connections

The MIL-HDBK-217B failure rate predictions for solder, crimp, weld and wire wrap connections are presented in Figure 10.2-2. Comparable rates from LC-76-EM5 are shown in Figure 10.2-3, 'The rates shown are the best statistically significant.

### FIGURE 10.2-2. CONNECTIONS OPERATIONAL FAILURE RATE PREDICTIONS

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Connections	$\frac{\lambda_{p}}{(10^{-6}/hr.)}$
Solder, reflow lap to P.C. boards	0.00012
Solder, wave to P.C. boards	0.00044
Other hand solder connections (e.g., wire to terminal board)	J.0044
Crimp	0.0073
Weld	0.002
Wirewrap	0.0000037

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## FIGURE 10.2-3. BEST CONNECTIONS FAILURE RATES FROM LC-76-EM5

Connections	$\frac{\lambda_{p}}{(10^{-6}/hr.)}$
Solder	0.00134
Weld	0.00171
Wrap	0.0000103
Crimp	0.0162

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## 10.3 Operational/Non-Operational Failure Rate Comparisons

Using the model in Section 10.2, the operational failure rate is estimated at .09 failures per million hours under the following assumptions.

a) Configuration and insert material-printed wiring board

- b) Operating temperature 30°C
- c) Number of pins 20
- d) Operating environment ground fixed

e) Cycles - less than 40 cycles per 1000 hours.

The 90% conf<sup>†</sup>once level for pin connectors in Section 10.1 was .028 fit. The operational to non-operational failure rate ratio is 3.2.

### 11.0 Printed Wiring Boards

1.

#### 11.1 Storage Reliability Analysis

### 11.1.1 Failure Mechanisms

Printed circuits have a dominant failure mechanism which imposes a definite limitation on life. It is caused by the difference in the thermal coefficient of expansion of the substrate and the plated copper. The copper yields to accomodate temperature changes, but eventually a fatigue failure causes an open circuit, usually in one of the plated thru holes. Use of very pure copper and control of the cross section help to extend the life.

Research results show that over 200 cycles from -65° to 110°C are obtainable, 50 cycles on a test coupon of 80 or more holes is recommended as a screening test.

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#### 11.1.2 Non-Operational Failure Rate

Non-operational failure rate of printed wiring boards is estimated at .83 failures per billion hours.

#### 11.1.3 Non-operational Data

Non-operational data collected consisted of 1210 million hours with one failure reported. Storage conditions are unknown. 11.2 Printed Wiring Boards Operational Prediction Model

The MIL-HDBK-217B failure rate model for MIL-P-55110 Printed Wiring Boards and MIL-P-55640 Multilayer (Plated-Through-Hole) Printed Wiring Boards is

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 $\lambda_p = \lambda_b NIE \times 10^{-6}$ 

where:  $\lambda_{p}$  = board failure rate

 $\lambda_{b}^{T}$  = base failure rate

- N = number of plated-through holes
- $\Pi_{\mathbf{F}}$  = Environmental Adjustment Factor

The above model is applicable only to high quality boards that have received screening and burn-in and that use G-10 or equivalent epoxy materials.

Figure 11.2-1 gives the specific values for the model. See the Appendix for a description of the environments.

MIL-HDEK-217B OPERATIONAL FAILURE RATE MODEL FOR PRINTED WIRING BOARDS FIGURE 11.2-1

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$$\lambda_{\rm p} = \lambda_{\rm b} {\rm NII}_{\rm E} \times 10^{-6}$$

(	γ <sup>b</sup>	6 X 10 <sup>-6</sup>	5 X 10 <sup>-4</sup>
λ <sub>b</sub> (Base Failure Rate	Type	Two-Sided Boards	Multi-layer Boards

N = Number of Plated Through Holes.

**Π<sub>E</sub> (Environmental Factor)** 

Environment	лЕ
Ground, Benign	
H	
Ground, Fixed	(1)
Naval, Sheltered	'শ
Ground, Mobile	4
Airborne, Inhabited	6
Naval, Unsheltered	ЪС
Airborne, Uninhab.	20
Missile, Launch	20

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## 11.3 Operational/Non-Operational Failure Rate Comparison

Using the model in Section 11.2, the operational failure rate of a multilayer board with 100 holes in a ground environment is 100 failures per billion hours. The operational to nonoperational failure rate ratio is 120.

## 11.4 Conclusions and Recommendations

1

Fatigue failure due to thermal cycling is the dominant failure mechanism. A coupon is taken from the printed circuit board to use in verifying the quality of the plated thru holes.

Constant temperature storage would be ideal. Lacking that, it is desirable to limit both the frequency and amplitude of the temperature excursions.

Some studies on matching the expansion coefficients have been made.

In application of printed circuit boards, cracking of solder joints is also a problem. The problem is more severe if encapsulating or potting are used. The principle design process for alleviating this problem is stress relief.

## APPENDIX

# ENVIRONMENTAL DESCRIPTION

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Environment	Nominal Environmental Conditions
Ground, Benign	Nearly zero environmental stress with optimum engineering operation and main-tenance.
Space, Flight	Earth orbital. Approaches Ground, Be- nign conditions without access for maintenance. Vehicle neither under powered flight nor in atmospheric re- entry.
Ground, Fixed	Conditions less than ideal to include installation in permanent racks with adequate cooling air, maintenance by military personnel and possible installa- tion in unheated buildings.
Ground, Mobile (and Fortable)	Conditions more severe than those for Ground, Fixed, mostly for vibration and shock. Cooling air supply may also be more limited, and maintenance less uniform.
Naval, Sheltered	Surface ship conditions similar to Ground, Fixed, subject to occasional high shock and vibration.
Naval, Un- sheltered	Nominal surf ce shipborne conditions but with repetitie high levels of shock and vibration.
Airborne, Inhabited	Typical cockpit conditions without en- vironmental extremes of pressure, tem- perature, shock and vibration.
Airborne, Uninhabited	Bomb-bay, tail, or wing installations where extreme pressure, temperature, and vibra- tion cycling may be aggravated by contami- nation from oil, hydraulic fluid, and engine exhaust. Classes I and Ia equip- ment of MIL-E-5400 should not be used in this environment.
Missile, Launch	Severe conditions of noise, vibration, and other environments related to missile launch, and space vehicle boost into orbit, vehicle re-entry and landing by parachute. Conditions may also apply to installation near main rocket engines during launch operations.

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