DAMAGE PROFILES IN SILICON AND THEIR IMPACT ON DEVICE RELIABILITY

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Prepared for:

Advanced Research Projects Agency

15 January 1976

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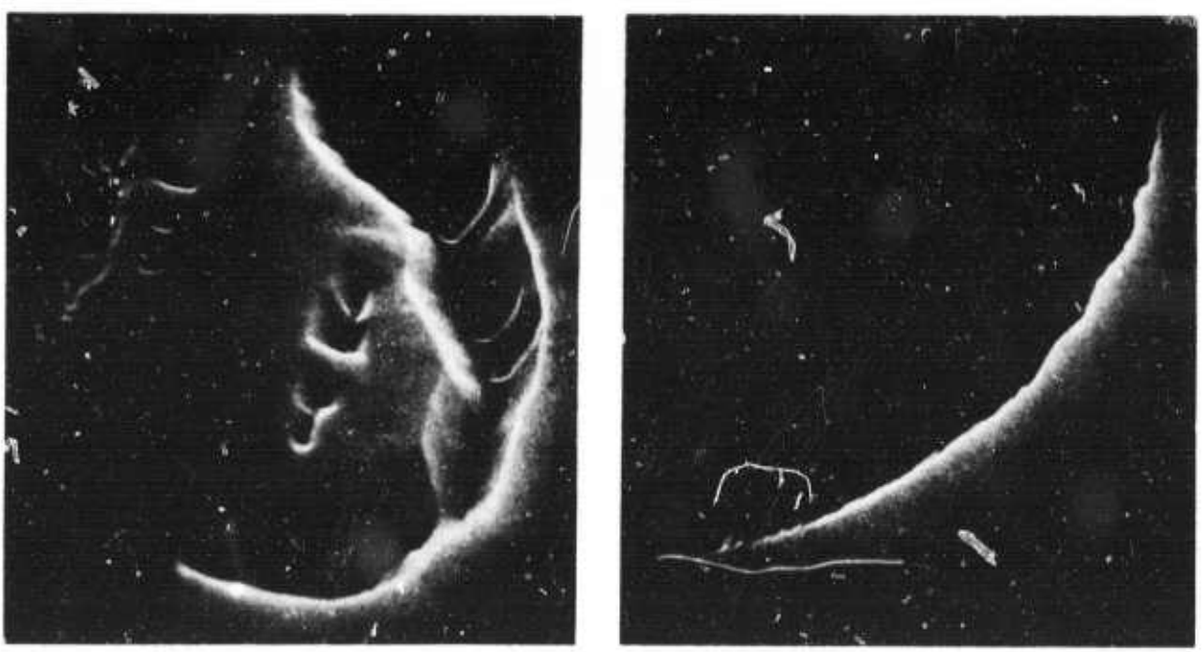
TECHNICAL REPORT No. 7, Part I
January 1976

Contract No. DAHC15-72-C-0274
Contract Monitor: Dr. C. M. Stickley

Sponsored by
Advanced Research Projects Agency
ARPA Order No. 2196, Program Code No. P2D10



SEM micrograph of fracture cone.
(Left) After cupric ion polish.
(Right) After silicon dioxide polish.

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by H Kappert, G. H. Schwuttke, and K. Yang

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by

G. H. Schwuttke and A. Oster

INTRODUCTION

A damage-free wafer surface is one of the most stringent materials requirements of today's advanced silicon device technology. In semiconductor processing it is traditional to assume that all problems related to surface damage of wafers are easily avoided either by polishing the wafer chemically or by polishing it using more advanced chemical-mechanical methods. Such techniques are thought to be very successful in removing mechanical damage present in silicon surfaces after slicing and lapping operations.

Polishing techniques are obviously effective in removing surface damage such that a specular wafer surface is obtained after polishing. A wafer surface is defined "damage-free" whenever all visible damage has been removed according to standard inspection techniques using light reflection and optical microscopy.

Through a number of investigations (1) we have established that chemical or chemical-mechanical polishing of silicon surfaces does not always guarantee a damage-free wafer surface if the minority carrier lifetime of the silicon is an important criterion of wafer quality.

Measurements of mechanical damage on silicon surfaces are difficult to perform. The basic intent of all damage measurements on silicon wafers is to associate a characteristic "depth of damage" with a particular wafer shaping operation, such as slicing, lapping, and polishing. The underlying idea is that once this value is known the damaged layer can be chemically removed with a minimum of material wasted.

It is interesting to note that the agreement between differently measured values of saw damage published in the literature (2-7) is quite poor, indicating certain difficulties with such measurements primarily related to the different measurement techniques. In this context it is also noteworthy to observe that polishing techniques are generally assumed to be equal in terms of "effectiveness" of damage removal although the subject of effectiveness of damage removal of silicon polishing techniques has not yet been investigated.

It is the intention of this study to show that wide variations in damage removal and damage propagation are characteristic for the different polishing techniques practiced today in the semiconductor industry. Accurate measurements are performed to evaluate standard chemical and

advanced chemical-mechanical polishing techniques and are reported in the following.

EXPERIMENTAL

Three polishing techniques are compared in this investigation.

1. Chemical polishing using nitric, acetic and hydroflouric acid mixtures.

2. Chem-mech cupric ion polishing.

3. Chem-mech silicon dioxide polishing.

The comparison is based on the idea that first mechanical damage is introduced into highly perfect silicon surfaces in a controlled manner. Subsequently, the damage removal effectiveness of a polishing technique is measured as the amount of material necessary to be removed to again obtain a "perfect" surface. The damage is introduced through the technique of Impact Sound Stressing (ISS). The technique is unique in so far as it allows generation of low or high densities of microsplits in the surface in the form of fracture cones. The Hertzian fracture cones produced are

approximately 50μm in diameter and penetrate as deep as 15 to 20μm into the bulk. The fracture cones are induced in the silicon surface by impacting the wafer surface with 300μm diameter tungsten balls under acoustic stressing. The acoustic stressing is done with a high intensity loudspeaker at a resonance frequency of the clamped wafer at 1380Hz. Consequently, the tungsten balls impacting the wafer surface replicate an acoustic mode pattern of the clamped vibrating wafer through a Hertzian fracture cone pattern. The density of microcracks thus achieved is determined by the vibration time, the number of tungsten balls on the wafer, and through the power put into the speaker. A density of 10^5 splits per cm^2 is easily achieved without breaking the wafer. The technique has been described in detail in ARPA Report Number 4 (1).

Examples of ISS wafers are shown in the x-ray topographs of Fig. 1. The topograph shown in Fig. 1a is before stressing and reveals the high quality (zero dislocation) of the substrate used. Figures 1b through 1d are topographs of ISS silicon wafers stressed at 12 watts, 40 watts and 60 watts respectively. The black contrast in the topographs reveals the damage distribution in the wafers. Note that the damage is not uniform across the wafer surface but is localized in certain areas. With rising power the damage distribution

Fig. 1a. X-ray topographs of wafer before ISS.

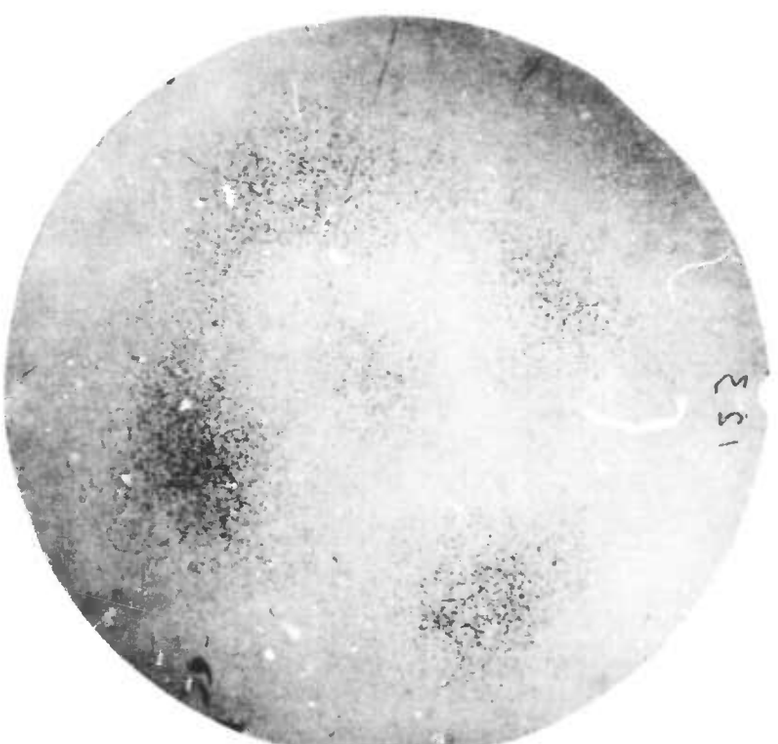

Fig. 1b. X-ray topograph of ISS stressed: 12 watt.

Fig. 1c. X-ray topograph of ISS stressed: 40 watt.

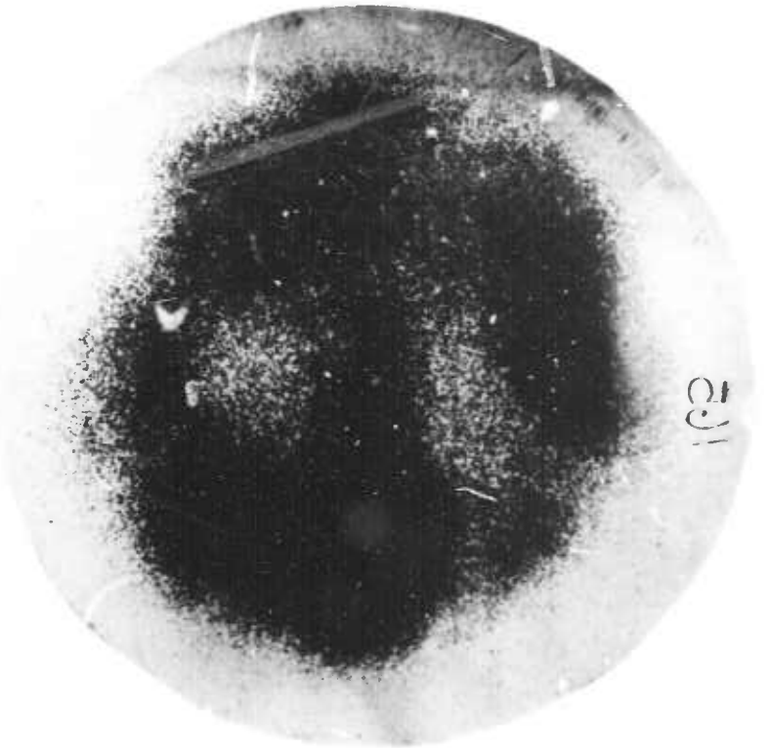

Fig. 1d. X-ray topograph of ISS stressed: 60 watt.

covers more wafer area. A similar effect can be achieved by keeping the power constant but increasing the number of tungsten balls. The amount of damage produced is readily controlled by the number of tungsten balls vibrating on the wafer surface. X-ray topographs provide convenient and accurate damage maps for device evaluation and defect analysis.

CHEMICAL POLISHING

The etching is performed in a rotating cup (approximately 60 rpm) using nitric-acetic-hydroflouric acid mixtures. The following conditions are used:

A. Fast etching is done with a standard 3/2/1 mixture composed of 3 parts HNO_3 (70%), 2 parts CH_3COOH and 1 part HF (49%). The etch rate for this composition is 12 to 13µm per minute.

   The etch rate drops to 6µm per minute when the wafer backside is protected with black wax.

B. Slow etching is done with a mixture of 30 parts HNO_3 and 1 part HF. For this composition the etch rate slows down to approximately 1.5µm/min. This value is comparable to the silicon dioxide polishing rate.

CHEM-MECH POLISHING

In chem-mech polishing one attempts to form chemically a reaction product at the specimen surface. This reaction product is removed from the specimen surface either chemically by a dissolution process or mechanically by abrasive action or by a shear or "rubbing-off" mechanism. Concurrently, more reaction product forms. Polishing is achieved as the substrate surface is controllably consumed to form the intermediate reaction product layer.

The two chem-mech polishing techniques compared in this investigation are briefly described in the following:

CUPRIC ION CHEM-MECH POLISHING OF SILICON

The polishing slurry consists of a solution of cupric nitrate and ammonium fluoride in DI water at a pH of approximately 4.5. Conventional polishing equipment is used. However, the slurry is corrosive and, because of the presence of environmentally sensitive chemical species, appropriate precautions must be taken.

Polishing occurs in the following way in the cupric ion process. Silicon specimens, usually in thin wafer form (2 1/4" diameter x 0.015" thick), are in contact with a suitable polishing cloth. The slurry is fed onto the rotating wheel with the following results:

Copper plates on to the silicon wafer surface.

Simultaneously, silicon undergoes a number of reactions to form soluble silicates.

The uniformly thick copper that adheres loosely to the surface of the silicon wafer is wiped away by the action of the "polishing cloth".

Silicates dissolve.

More copper deposits on the nascent silicon surface, silicon continues to dissolve chemically, and the net result of this action is a continuous polishing process.

These steps in the polishing process are schematically shown in Fig. 2. The chemical reactions may be written as:

$$Cu^{++} + 2e^{-} \longrightarrow Cu^{o} \qquad (1)$$

$$Si^{o} \longrightarrow Si^{+4} + 4e^{-} \qquad (2)$$

$$Si^{+4} + 6F^{-} \longrightarrow SiF_6^{-} \qquad (3)$$

$$SiF_6^{=} + 2NH_4^{+} \longrightarrow (NH_4)_2\ SiF_6 \qquad (4)$$

Overall:

$$Si + 2\ Cu(NO_3)_2 + 6NH_4F$$

$$\longrightarrow (NH_4)_2\ SiF_6 + 4NH_4 + 2\ Cu + 4HNO_3 \qquad (5)$$

SILICON DIOXIDE FOR CHEM-MECH POLISHING OF SILICON

The polishing slurry consists of aqueously dispersed silica at a pH of 9 to 11. The SiO_2 particles are of the order of 100μm in size (colloidal range). As this slurry is fed onto the polishing wheel, the following mechanism is activated to produce highly polished surfaces:

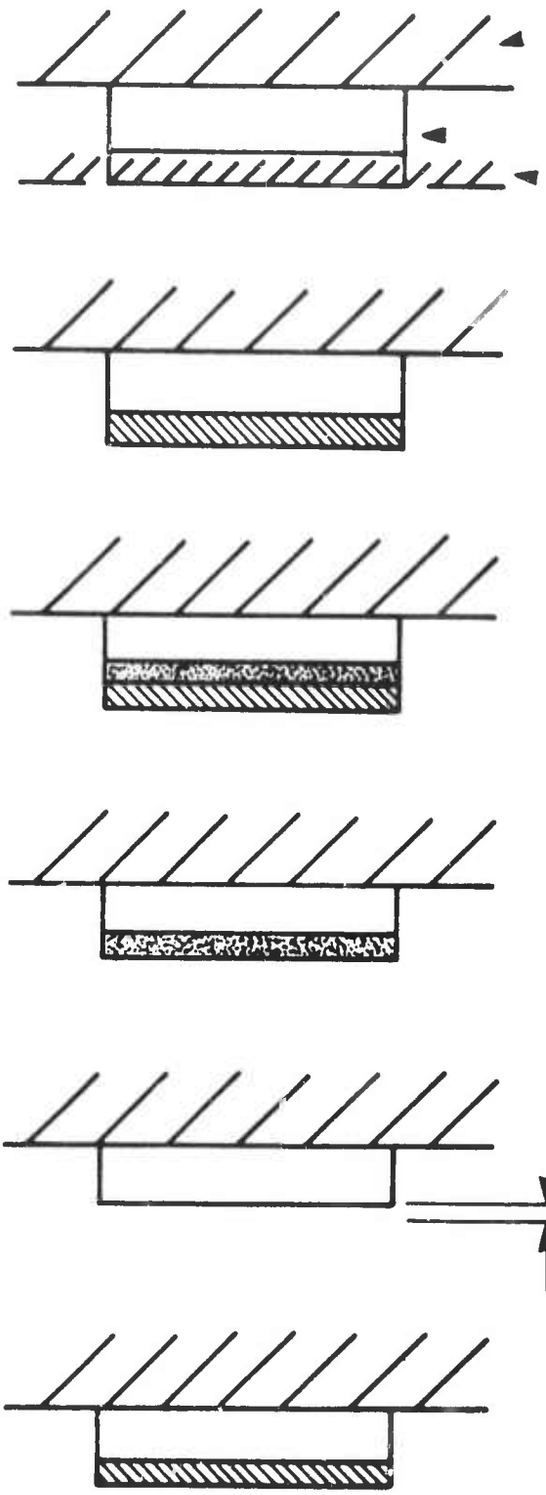

Fig. 2. Cupric ion process.

Silicon reacts chemically to form a soft glass-like silicate layer on the specimen surface.

The silica particulates in the slurry abrasively remove the silicate-layer reaction product.

More silicate forms on the nascent silicon surface and the polishing process is continued.

It must be pointed out that the soft silicate-layer reaction product does not harden when kept wet and is easily removed by the harder SiO_2 particles in the slurry.

The primary silicon surface, in turn, is harder than the SiO_2 abrasive particles, and it remains unaffected. These steps in the process are illustrated schematically in Fig. 3.

EXPERIMENTAL PROCEDURE

Standard 2 1/4 inch diameter silicon slices, silicon dioxide polished, (100) orientation, p-type, resistivity 20, 15 or 2 ohm-cm were ISS'ed as described. After sound-stressing the wafers were x-ray topographed to ascertain their defect

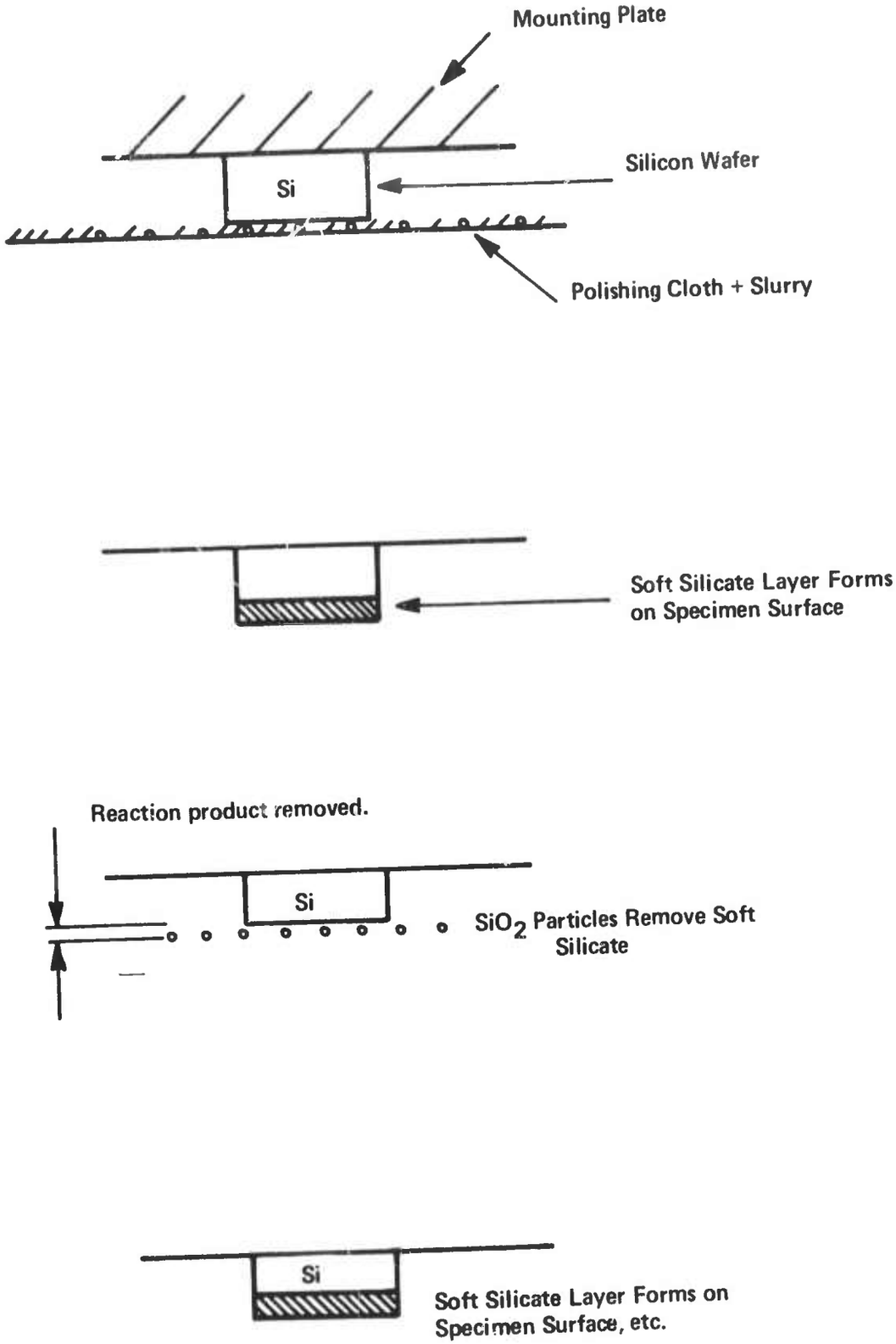

Fig. 3. Silicon dioxide process.

level. Three batches of wafers were prepared, each batch consisting of 50 wafers. Every batch was subdivided into five groups, each group containing ten wafers for repolishing. Repolishing was performed in four steps. The wafers appeared damage-free in the x-ray topograph after the fourth polishing step. The damage removal was monitored through x-ray topography, optical microscopy, and scanning electron microscopy. In addition, minority carrier lifetime measurements were made using MOS capacitors processed on the wafers as described in Technical Reports No. 2 and 4 (1). Accordingly, each wafer contained 36 circular devices of 60 mil diameter. A 5000Å thick oxide was used, grown at 1000°C, using a dry-wet-dry (15 minutes - 90 minutes - 15 minutes) oxidation cycle. Aluminum metallurgy was used. After metalization the wafers were annealed in forming gas at 400°C for 30 minutes. The lifetime was measured after every damage removal step using the MOS technique published in Technical Report No. 4. Perfect silicon wafers were MOS processed as standards with every set of damaged wafers.

RESULTS

DAMAGE TOPOGRAPHY AND DAMAGE DEPTH

The detailed structure of ISS damage produced on a wafer surface is described in Technical Report No. 4 (1).

Accordingly the damage consists of Hertzian fracture cones and shallow abrasion marks. The abrasion penetrates the wafer surface only a few thousand angstroms and is removed after the first polishing step. This work relies on the fracture cones which extend approximately 20μm into the bulk.

Fracture cones on (001) surfaces are shown in Figs. 4. In Fig. 4a the surface is shown directly after ISS while the surface shown in Fig. 4b has been Sirtl etched for ten seconds after ISS to show the fracture cones more clearly. The direction of the long arms of the cracks is <110>. The depth of the cracks was determined by two different methods. The first technique evaluates the crack depth with the help of a one and a two degree bevel. This is shown in Figs. 5. The damage depth profile introduced by sound stressing is clearly visible on the bevel. The damage depth calculated from the damage profile ranges from 15μm to 20μm and is indicated on the photomicrographs. The second technique uses cross sections of cracks produced by cleavage for depth evaluation. After cleavage the samples are ... seconds Sirtl etched to show the cracks more clearly. An example is given in Figs. 6. Figure 6a shows the surface of the sample and Fig. 6b the cross section. The corresponding parts of one crack on the two photos are indicated by an arrow.

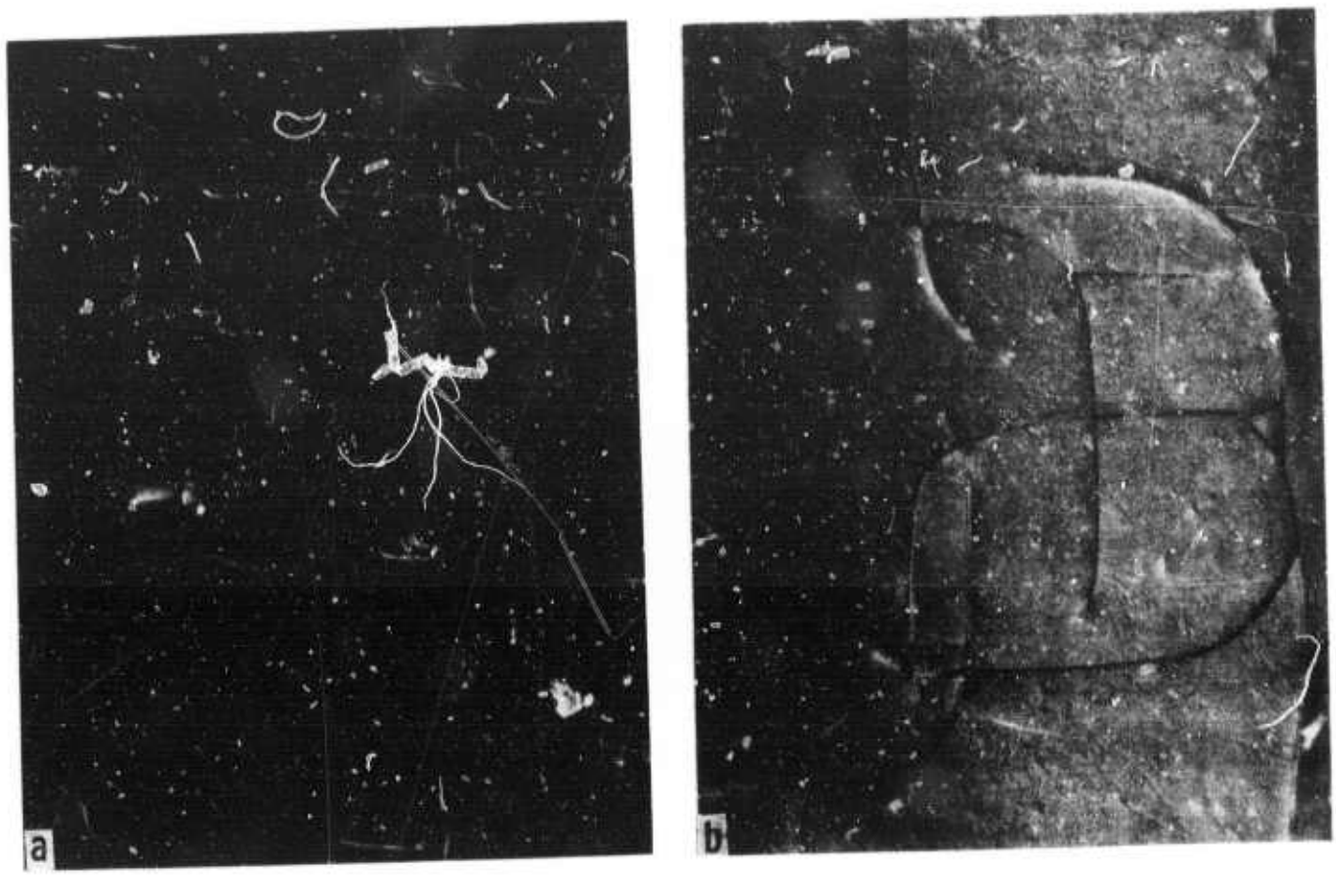

Fig. 4. Impact sound stressed (ISS) silicon, (001) surface, showing Hertzian fracture cones.

a. As stressed (320X).
b. As stressed, 10 seconds Sirtl etched (855X).

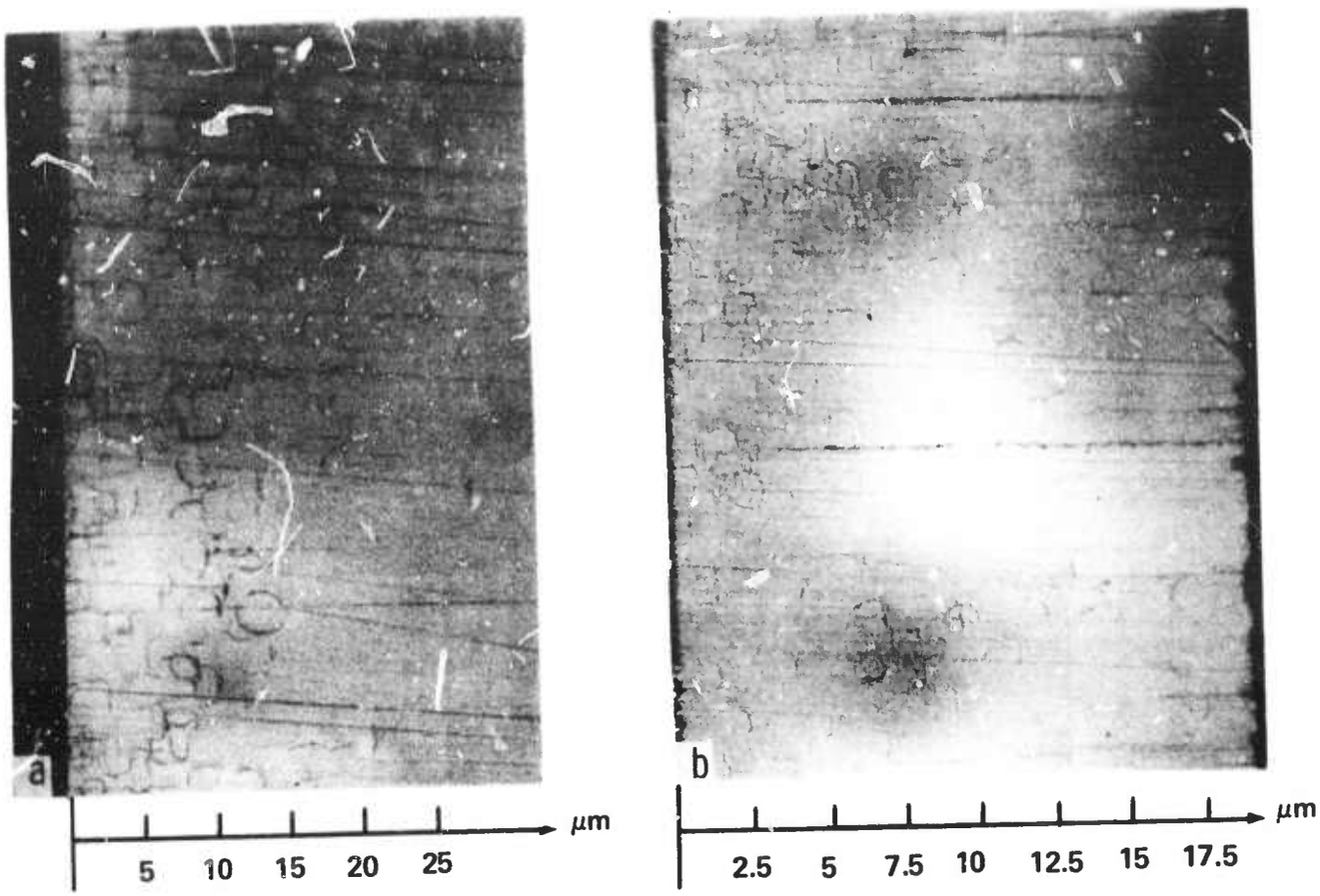

Fig. 5. Damage profile of ISS silicon displayed by the bevel technique.

a. 2 degree bevel (67X).
b. 1 degree bevel (67X).

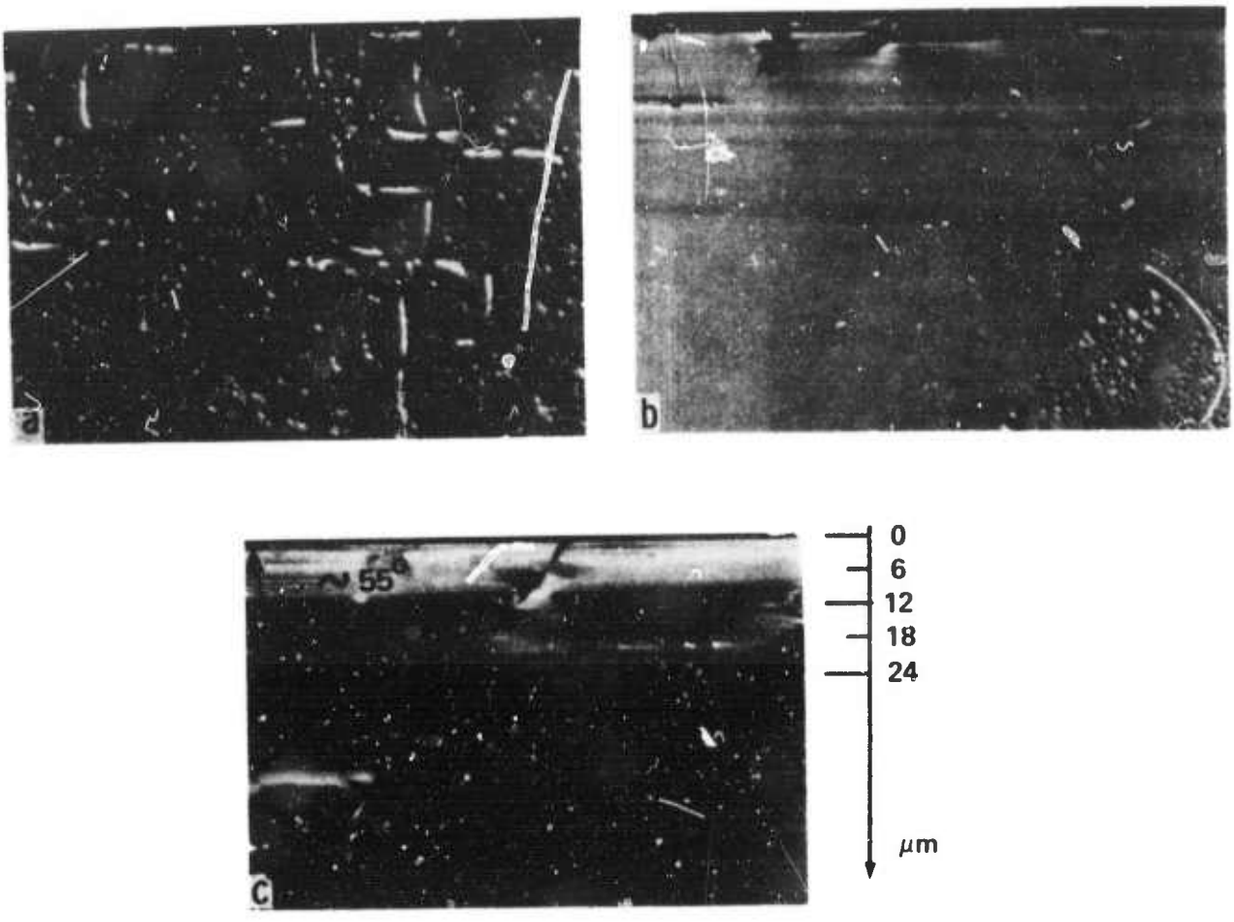

Fig. 6. Damage profile of ISS silicon displayed by the cleavage technique.

a. Surface (320X).
b. Cleavage plane (320X).
c. Note propagation of fracture cone in (111) plane (855X).

The cross section is shown magnified in Fig. 6c. It can be seen that the angle between the wafer surface and the crack is 55 degrees. This is very close to the interplanar angle between the (100) and (111) planes which is 54.8 degrees. The depth of the crack can also be measured on such cross sections. For this crack the depth is 18μm, which is in good agreement with the values found by the beveling technique.

CHEMICAL ETCHING

A. 3/2/1 - backside not protected:

The acid mixture $3HNO_3$-2 CH_3COOH-1HF produces a fast etching effect on both sides of the wafer. Since only the front side is mechanically damaged the etch rate is not necessarily equal on both sides. It is assumed that the etch rate initially is more rapid on the front side. An average etch rate of 25μm/minute was registered during the two first minutes. The micrographs of Figs. 7(a,b,c,d) illustrate four steps of the fast acid attack: this fast acid tends to smooth the silicon surface. After removal of 115μm on both sides, or at most 65μm on the front side, this surface appears damage free.

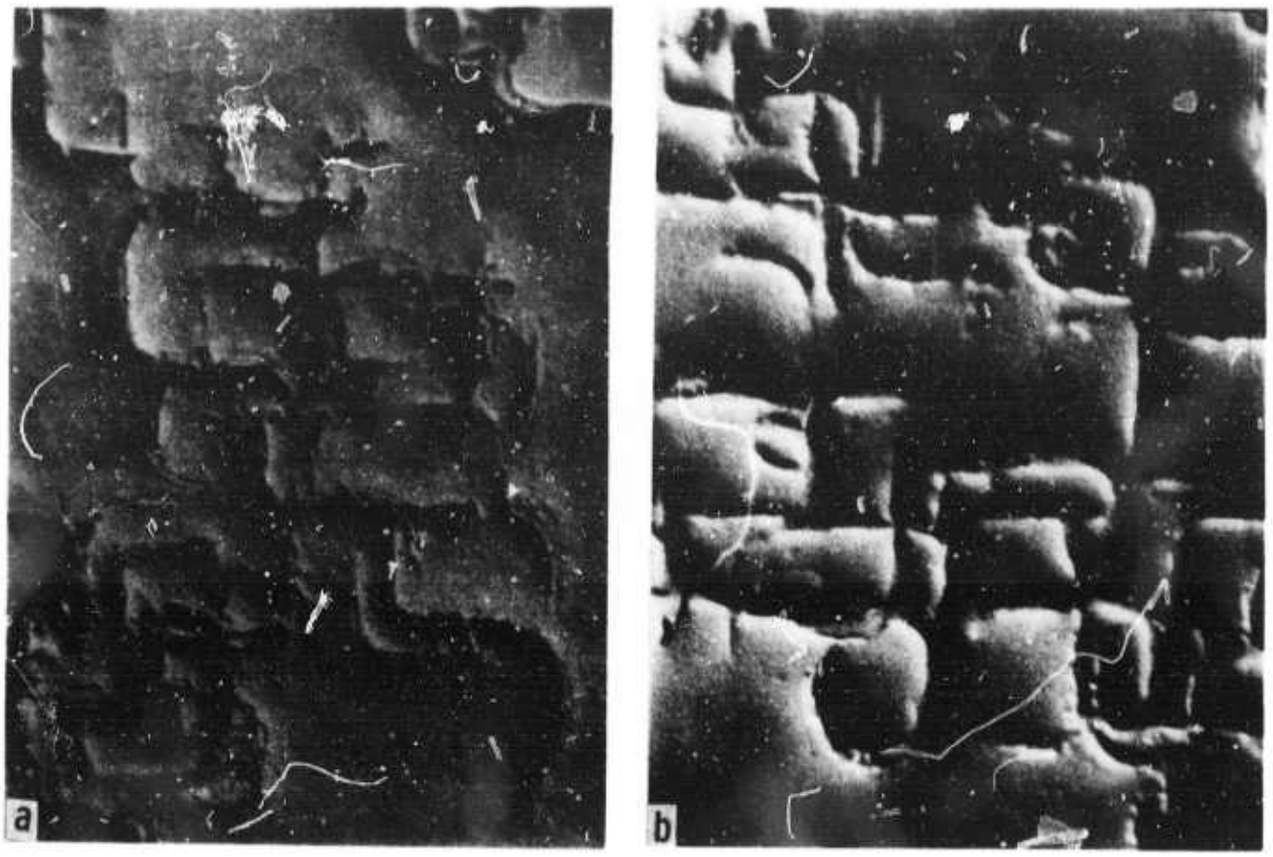

Fig. 7. Damage removal with 3/2/1 etch. Wafer backside not protected (320X).

a. 25 μm removed.
b. 50 μm removed.

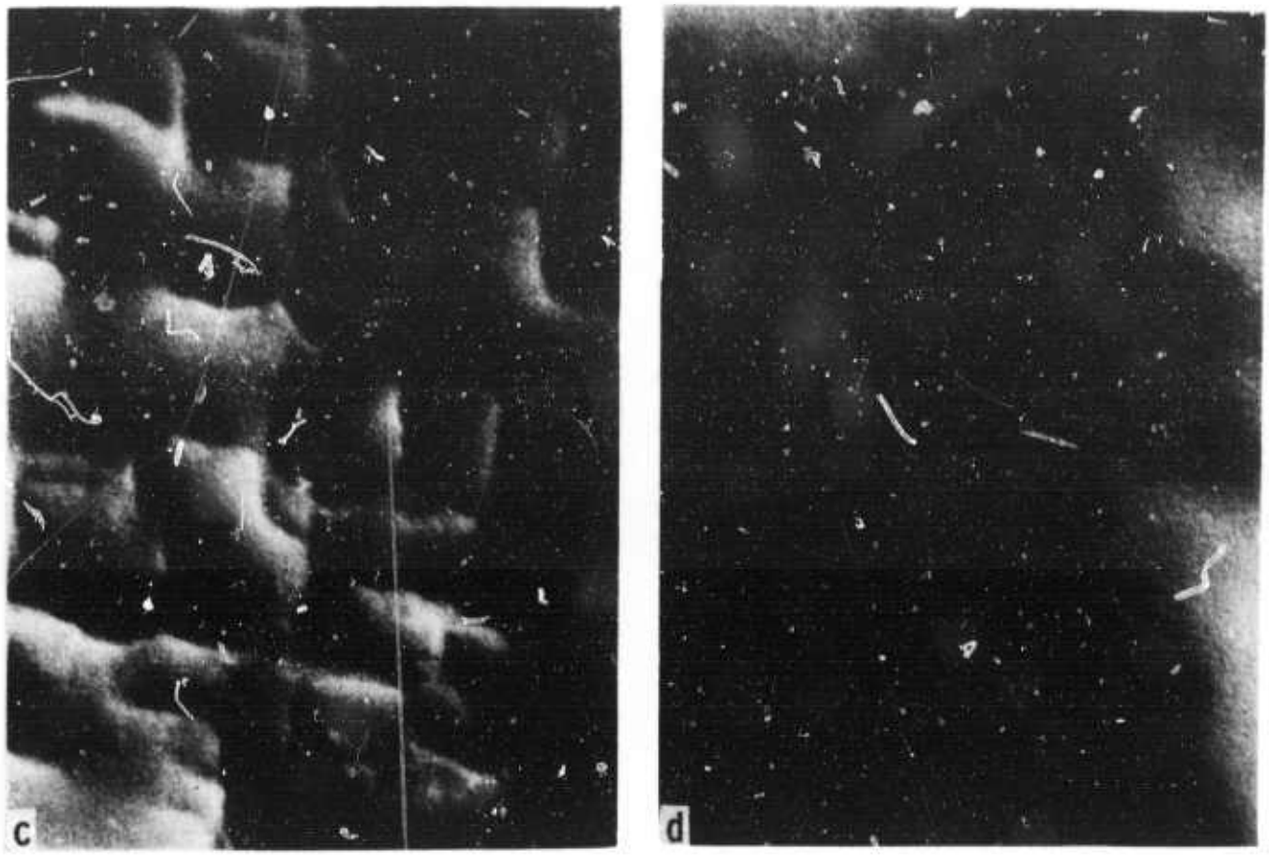

Fig. 7. Damage removal with 3/2/1 etch. Wafer backside not protected (320X).

c. 85 μm removed.
d. 115 μm removed.

B. 3/2/1 etch - backside protected with black wax:

Protecting the wafer backside drops the etch rate to approximately 5.5μm/min. The results are presented in Table I and typical micrographs are displayed in Figs. 8(a,b,c). Note that 60 to 70μm must be removed to eliminate the fracture cones.

TABLE I

3/2/1 Fast Etch

Substrate: 20 ohm-cm, p-type, <100>

Group No.	Repolish [μm]	Lifetime Average (12 devices/wafer) μsec
Control	-	600
I	12	15
II	28	29
III	40	45
IV	54	100
V	90	180

3/2/1 etch, backside of wafer black wax protected.

Surface is featureless after 90μm repolish.

Note difference in lifetime between control sample and etch repolish.

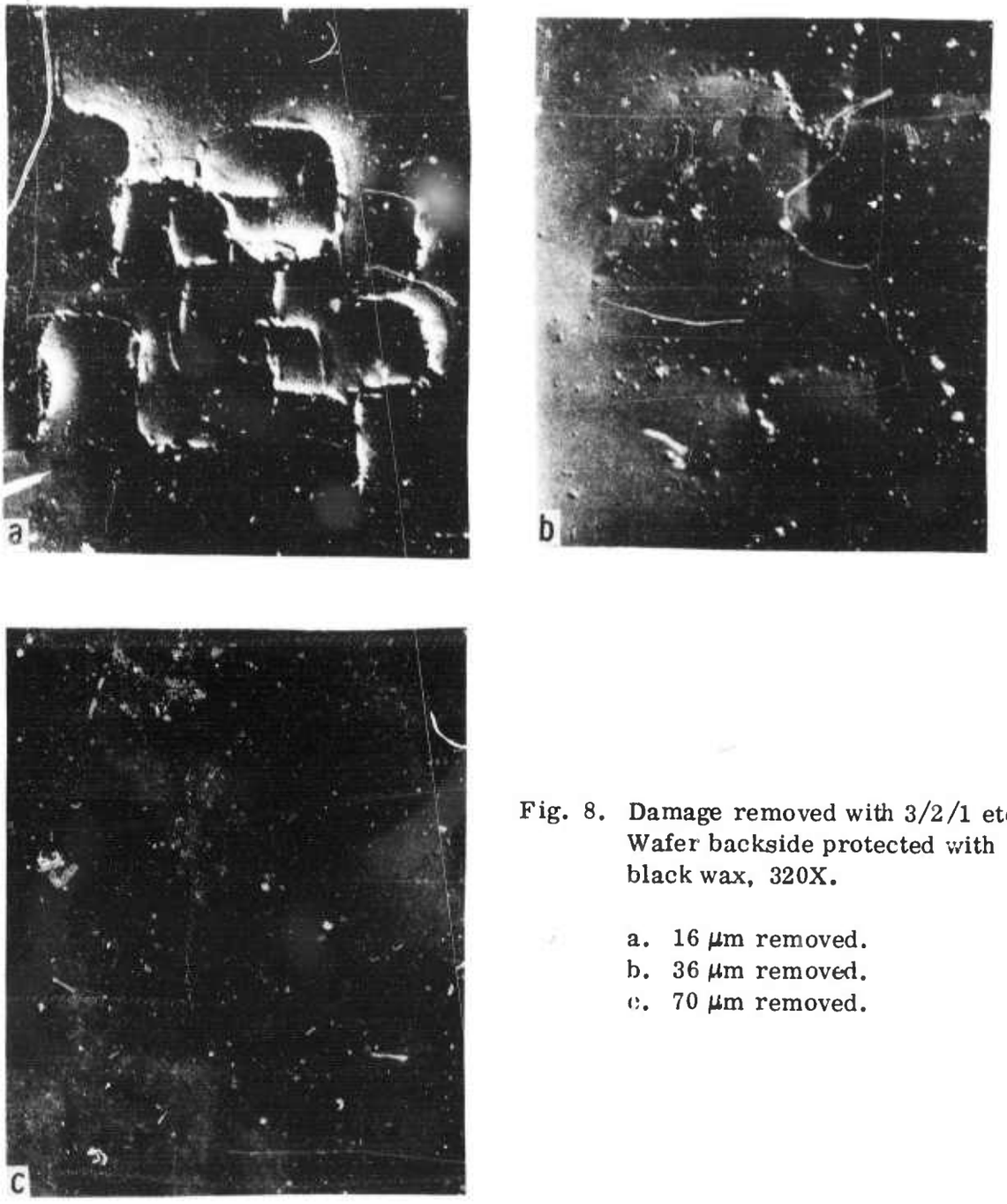

Fig. 8. Damage removed with 3/2/1 etch. Wafer backside protected with black wax, 320X.

a. 16 μm removed.
b. 36 μm removed.
c. 70 μm removed.

C. Slow etch:

Damage removal using an acid of composition 30 parts HNO_3- 1 part HF provides a relatively slow etching action on silicon. The etch rate for this solution is $1.4 \pm 0.2 \mu m$/minute for backside protected wafers. Typical etching steps are shown in Figs. 9(a,b,c,d). Interesting characteristics concerning the etching behavior are noticed:

- the slow acid leaves sharper edges delineating the cracks (Fig. 9a).

- the cracks stay visible longer and are well defined (Fig. 9b). When the etching progresses, the cracks look like worms. The surrounding areas are much less affected than with the fast acid. Therefore,
- the slow etching action can be qualified as more preferential than the fast acid attack.

- approximately 90μm must be removed to eliminate the surface damage.

The results are summarized in Table II.

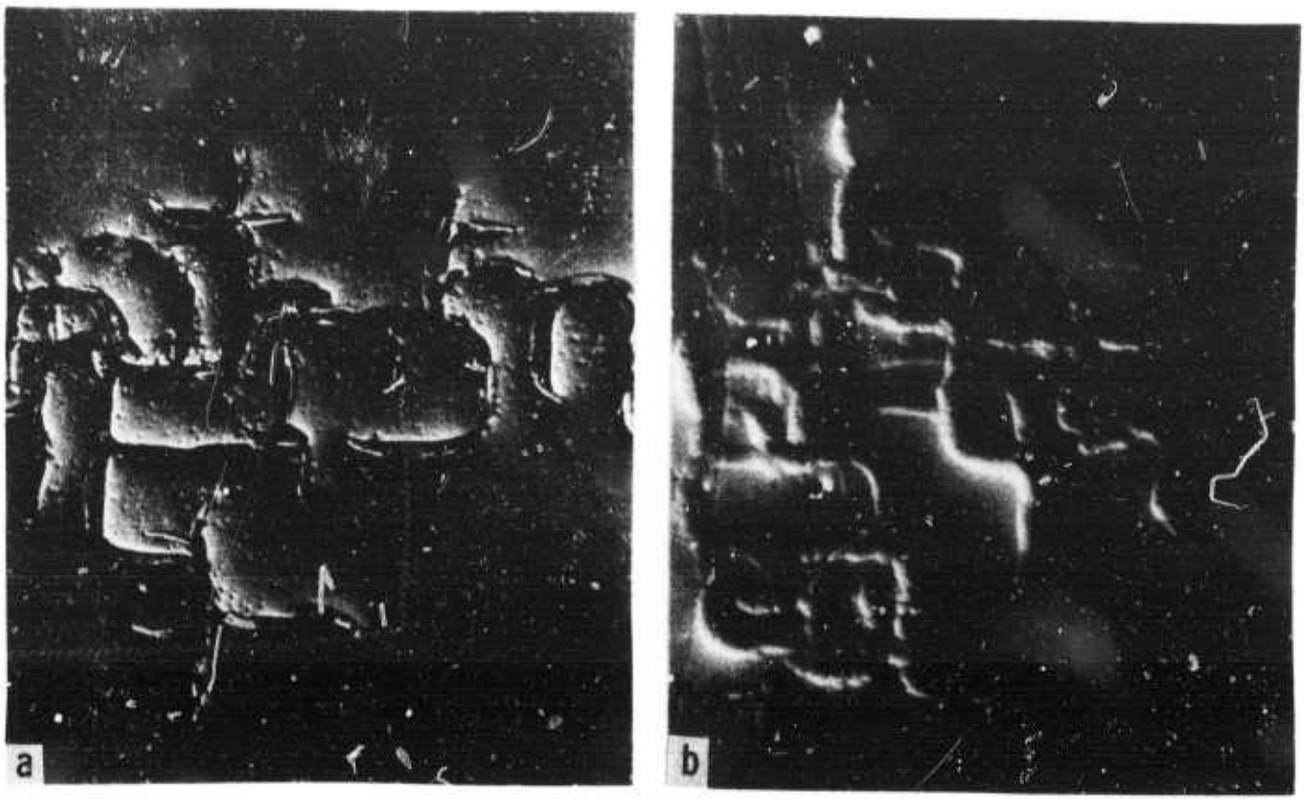

Fig. 9. Damage removal with slow etch. Wafer backside protected (320X).

a. 5 μm removed.
b. 70 μm removed.

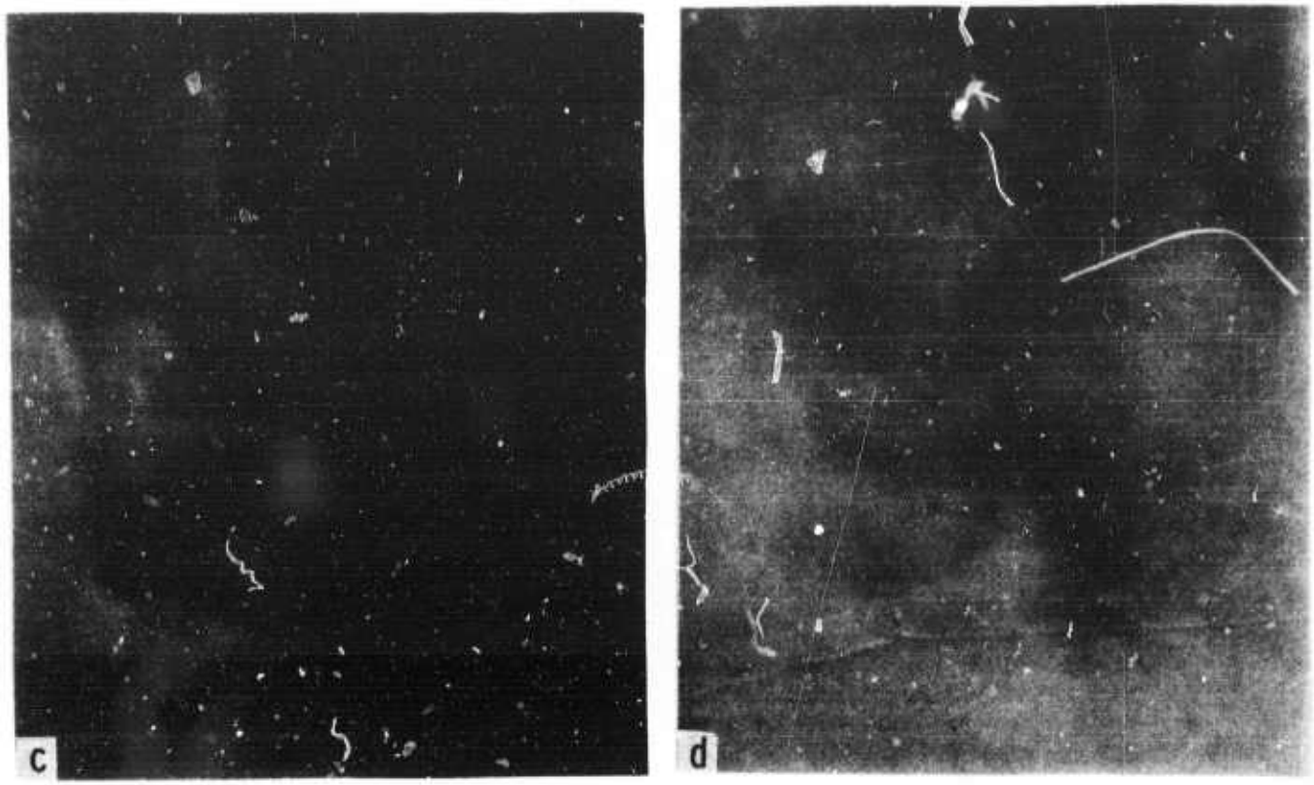

Fig. 9. Damage removal with slow etch. Wafer backside protected, (320X).

c. 90 μm removed.
d. 100 μm removed.

TABLE II

Slow Etch

Substrate: 20 ohm-cm, p-type, <100>

Group No.	Repolish [μm]	Lifetime Average (12 devices/wafer) μsec
Control	-	600
I	10	35
II	15	50
III	50	-
IV	90	-

Slow etch (30 p. HNO_3 - 1p. HF).

Surface is featureless after 90μm repolish.

No lifetime data available for steps III and IV due to leaky oxide.

CHEM-MECH POLISHING

CUPRIC ION POLISHING

The action of the cupric ion polish* during damage removal is shown in the photomicrographs of Figs. 10. After the first repolishing step of about 10-15μm, an "opening" of the cracks is observed. The surface around the cracks becomes lightly wavy; the abrasion spots, however, have almost completely disappeared. This is shown in Fig. 10a. In Fig. 10b, 20μm have been removed. The density of the remaining defects has decreased but the more intense cracks are now wider and bigger than before. This is also shown in Fig. 10c, where a heavily stressed sample has been repolished to about 25μm. 30μm have been removed in the sample shown in Fig. 10d. A few defects are still left which coincide mainly with the central part of the fractures. Fig. 10e shows the last step in the repolishing process of this type of defect before a perfect looking surface is obtained again. At least 40μm to 50μm have to be removed by copper polishing to reproduce a perfect surface.

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* Cupric ion polish normally removes silicon faster than silicon dioxide polish. For our measurements the cupric ion polishing rate was kept equal to the silicon dioxide polishing rate of approximately 2μm per minute.

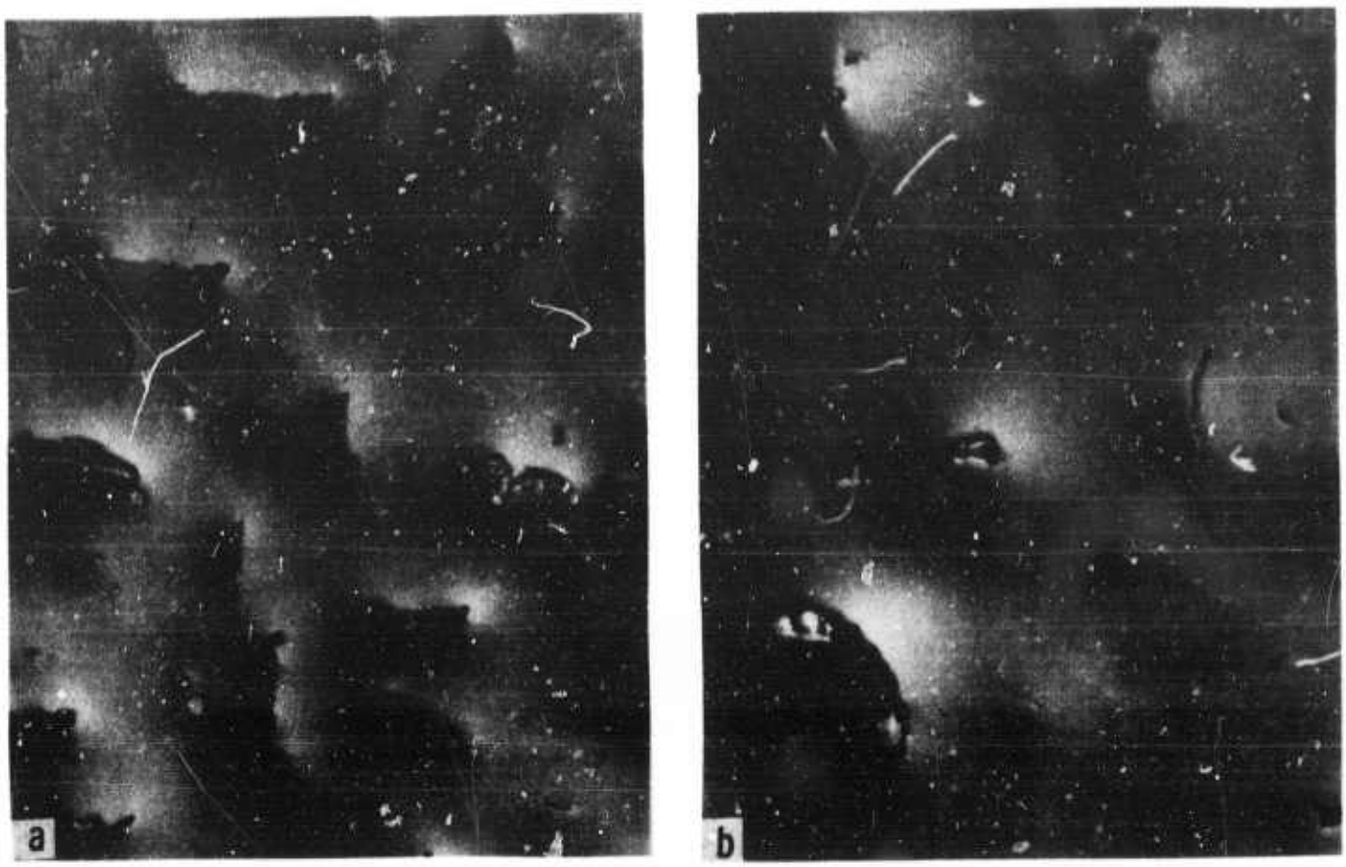

Fig. 10. Damage removal with cupric ion polish (320X).

a. 10-15 μm
b. 15-20 μm

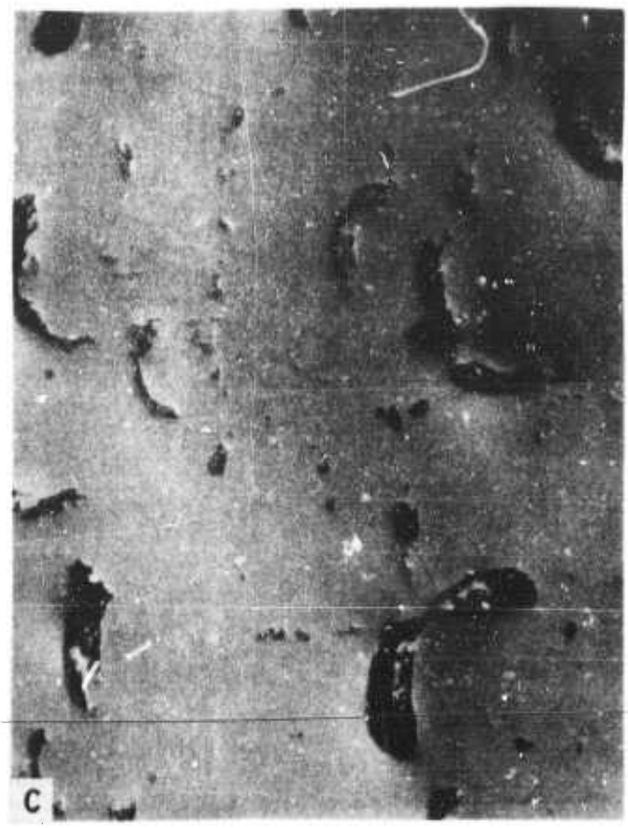

Fig. 10. Damage removal with cupric ion polish (320X).

c. 20-25 μm
d. 30 μm
e. 40 μm

SILICON DIOXIDE POLISHING

Similar measurements were made using silicon dioxide to repolish the samples. There is one important difference between this technique and the chemical and the cupric ion polishing techniques. Silicon dioxide polish rapidly decreases the density and the size of the cracks in the repolished surfaces. This is shown in the photo-micrographs given in Figs. 11. Figure 11a is obtained after the 10μm step. It can be seen that this time the narrow fracture lines show no opening. The abrasion spots have totally disappeared. Figure 11b shows that after 15μm, the crack density and the length of the fracture lines have sharply decreased. The surface in between already looks perfect. As shown in Fig. 10c, only a few very small defects can be detected after removing 20μm, whereas the surface is always perfect after removal of 25μm. Thus silicon dioxide does not propagate the damage. Consequently, only a few microns more than the damage depth has to be removed to obtain a perfect surface. The silicon dioxide polish regenerates the surface perfection most efficiently and most completely.

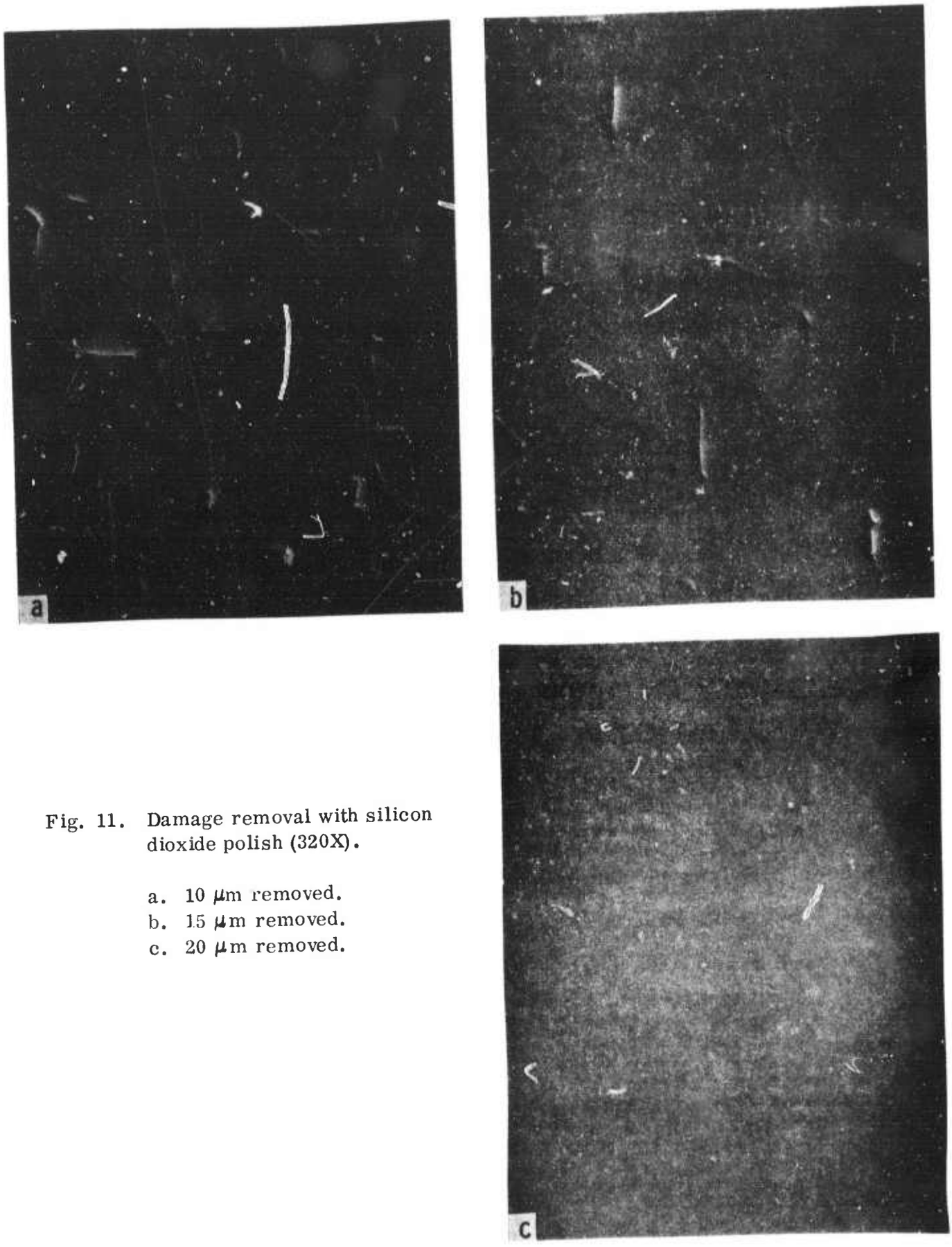

Fig. 11. Damage removal with silicon dioxide polish (320X).

a. 10 μm removed.
b. 15 μm removed.
c. 20 μm removed.

A SEM study illustrates and corroborates the results obtained above. The strong etching effects of the cupric ion solution are shown in Figs. 12a and 12b. Figures 13a and 13b are SEM micrographs of a silicon dioxide repolished sample (10 and 15μm). In these pictures no deepening of the crack and no walls with sharp edges are seen.

The cupric ion and the silicon dioxide polishing data are summarized in Tables III and IV. Lifetime measurements were also performed on these samples and are included in the tables.

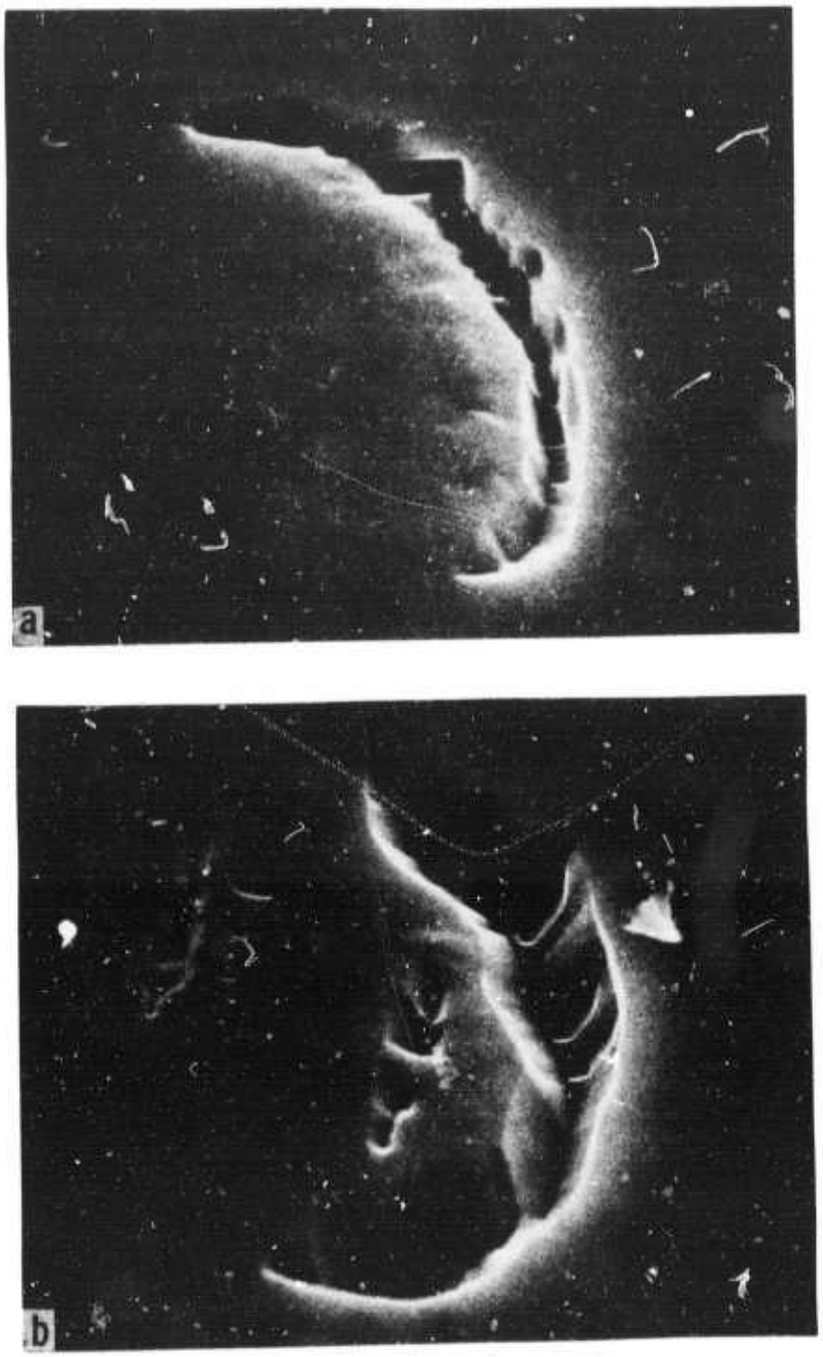

Fig. 12. SEM micrograph of fracture cone after cupric ion polish recorded at 30 kV, 45 degree view (1.8 KX).

a. 10-20 μm removed.
b. 25-35 μm removed.

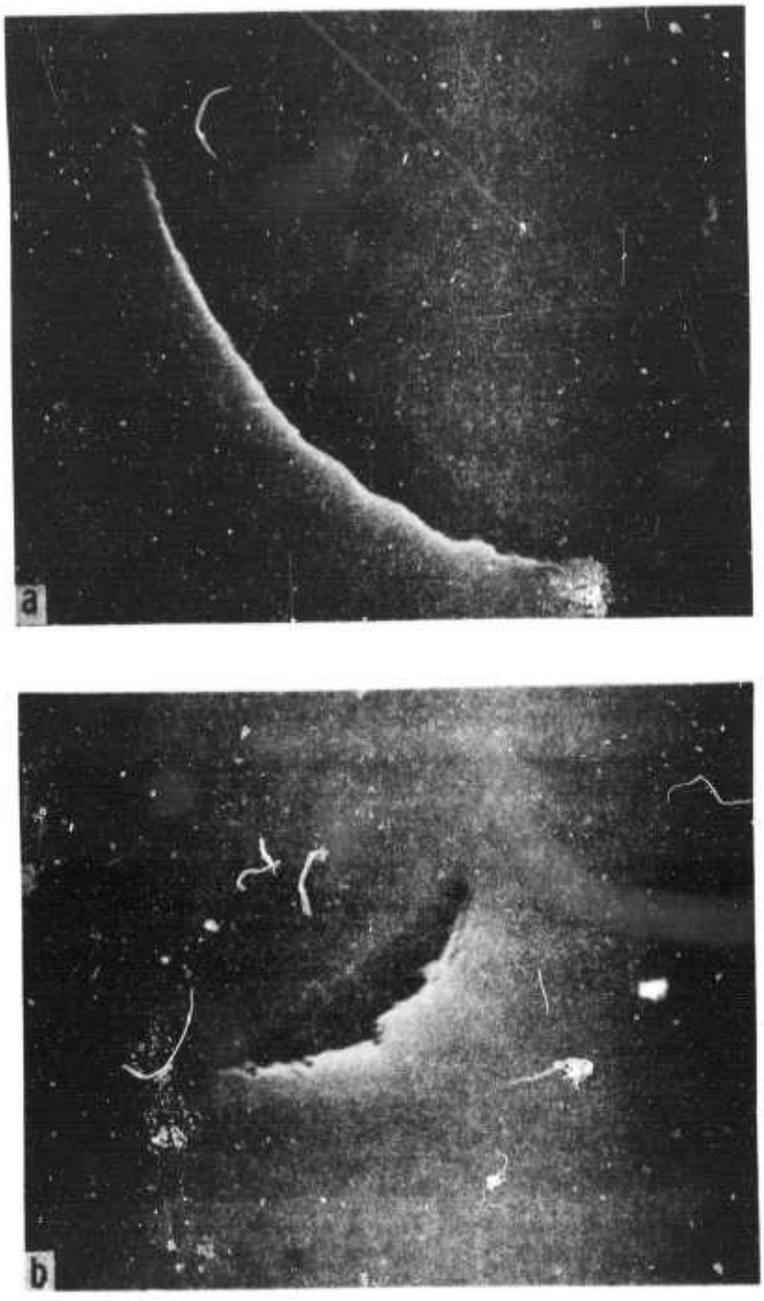

Fig. 13. SEM micrograph of fracture cone after silicon dioxide polish, recorded at 30 kV, 45 degree view (1.8 KX).

a. 10 μm removed.
b. 15 μm removed.

TABLE III

Cupric Ion Polish

Substrate: 10 ohm-cm, p-type, <100>

Group No.	Repolish [μm]	Lifetime Average (12 devices/wafer) μsec	Std. Deviation Lifetime μsec
Control	-	330	150
I	15*	-	-
II	25	15	5
III	35	88	80
IV	45	150	70

* At this stage the surface of the stressed area was still so much damaged that voltage breakdown due to leaky oxide prevented lifetime measurements.

TABLE IV

Silicon Dioxide Polish

Substrate: 2 ohm-cm, p-type, <100>

Group No.	Repolish [μm]	Lifetime Average (12 devices/wafer) μsec	Std. Deviation Lifetime μsec
Control	-	170	143
I	10	0.5	0.4
II	15	5.8	3
III	20	64	61
IV	25	73	43

Note lower substrate resistivity compared to cupric ion and chemical polish which accounts for lower lifetime of control wafer.

DISCUSSION

The results presented in Tables I to IV show clearly that all polishing techniques are faced with certain limitations. Such limitations are encountered whenever an effective removal of microcracks or microsplits is in question.

Silicon is a brittle material. Any wafer slicing or shaping operation as practiced in the industry introduces small cracks into the material. Silicon is so brittle that even a single hard particle as, for instance, silicon-carbide, rubbing across a wafer surface, can introduce tiny cracks. One of the major physical shortcomings of a silicon crystal is its great susceptibility to crack formation.

Recently, it was shown that microsplits are detrimental to the minority carrier lifetime in silicon. It was also shown that they are the cause of leakage currents in devices (1). As a result of such investigations (1) the presence of oxidation induced stacking faults in a silicon surface is evidence of incompletely removed microsplits.

One of the interesting results of this investigation is that none of the polishing techniques discussed recovers the original minority carrier lifetime of the undamaged wafer

completely. This follows from a comparison of the lifetime data of repolished wafers and control wafers processed simultaneously. It was found that such a loss in lifetime correlates well with the presence of incompletely removed microsplits. To support these findings we have performed the following experiment.

Two groups of repolished silicon wafers were selected. The wafers were first MOS processed 36 devices per wafer and the lifetime of the MOS devices/wafer was determined (1). After the measurements the devices were removed from the surface and the wafers were reprocessed. Similar devices were produced at identical locations and the lifetime was measured again. The results obtained are summarized in Table V.

For the silicon dioxide as well as for the cupric ion polish two sets of data are compared in this table. The first set relates to samples selected after the last repolishing step before the wafer appears defect free in x-ray topographs. This is after 20μm repolish for the silicon dioxide and after 40μm repolish for the cupric ion polish. The second set of data is obtained from wafers that experienced one additional repolishing step. For silicon dioxide this is after 25μm and for the cupric ion polish this is after 50μm.

TABLE V

Silicon Dioxide Polish - Second Oxidation

(Based on 36 devices/wafer)

Repolish (μm)	1st Oxidation Lifetime in μsec		2nd Oxidation Lifetime in μsec	
20	Average Std. Dev.	20 30	Average Std. Dev.	102 113
25	Average Std. Dev.	86 104	Average Std. Dev.	66 80
25	Average Std. Dev.	102 100	Average Std. Dev.	110 115

Cupric Ion Polish - Second Oxidation

(Based on 36 devices/wafer)

Repolish (μm)	1st Oxidation Lifetime in μsec		2nd Oxidation Lifetime in μsec	
40	Average Std. Dev.	20 30	Average Std. Dev.	21 50
50	Average Std. Dev.	137 175	Average Std. Dev.	175 186

Control Wafer - Second Oxidation

(Based on 36 devices/wafer)

Repolish (μm)	1st Oxidation Lifetime in μsec		2nd Oxidation Lifetime in μsec	
--	Average Std. Dev.	172 43	Average Std. Dev.	283 111

A comparison of the lifetime of the devices/wafer obtained after the first and second processing indicates that reoxidation of wafers can improve the lifetime distribution across a wafer surface.

A defect analysis of the wafer areas corresponding to short and long lifetimes revealed the presence of oxidation induced stacking faults in the low lifetime areas whereas the long lifetime areas were found to be practically free of defects. Since oxidation induced stacking faults are the annealing product of microsplits (1) we take this as an indication that splits in the surface of a silicon wafer are very difficult to remove by polishing alone. However, these measurements indicate also that split healing can be initiated through annealing; otherwise, there could be no improvement in lifetime distribution after oxidation. Such conclusions may appear more convincing and less surprising if one briefly considers possible closure mechanisms of a Hertzian fracture.

The mechanics of growth and closure of a Hertzian fracture are quite complicated (8,9) but a short qualitative picture of the process is sufficient to allow us to discuss our experimental results.

Three different types of crack closure have been proposed. The first one assumes that a crack can completely close and perfect healing occurs along the entire length of the crack. This model is based on such ideal conditions as are encountered during cleavage experiments conducted on mica in ultra high vacuum (10^{-13} Torr) (10) and does not apply to our situation.

The second model assumes complete closure of the crack but zero healing. This would imply that the fracture interface recontacts over the entire length of the crack and thus relieves the residual elastic strain energy in the specimen; but no atomic bonding is established across the interface because the broken bonds are saturated by contaminants. Experimental evidence, also obtained on mica, indicates that contamination can reduce the interfacial adhesion to a negligible level (11). Work on fused silica has shown that fracture cones can close "optically perfect" and that the fracture interface will disappear completely (12). However, such results are based on optical observations and a fracture interface in "optical contact" may well be separated a few hundred angstroms. Thus this model also appears unlikely in the context of our work.

The third model assumes zero closure and zero healing. This type of behavior is supported through optical observations of residual cracks in diamonds after Hertzian fracture tests (13) and implies a closure prevention mechanism capable of withstanding substantial elastic restoring stresses. Such a mechanism is easily envisioned by the wedging action of fracture debris or from the inability of structurally complex fracture surfaces to "key together" along the entire length of the crack.

This behavior of crack closure is well supported for silicon through experimental evidence (see Chapter 2 of this report) and thus supports our results. X-ray topographic measurements exclude an effective crack closure and crack healing mechanism at room temperature in silicon (14). Thus it appears reasonable that polishing techniques utilizing chemical action are very effective in crack propagation during polishing while the more mechanical polishing techniques are less effective for crack propagation in silicon.

This is in complete agreement with our experimental findings that relate to the effectiveness of damage removal of polishing agents. Such data are summarized in Fig. 14. It is evident that the more mechanical acting polishing technique - silicon-dioxide - is also the most effective one

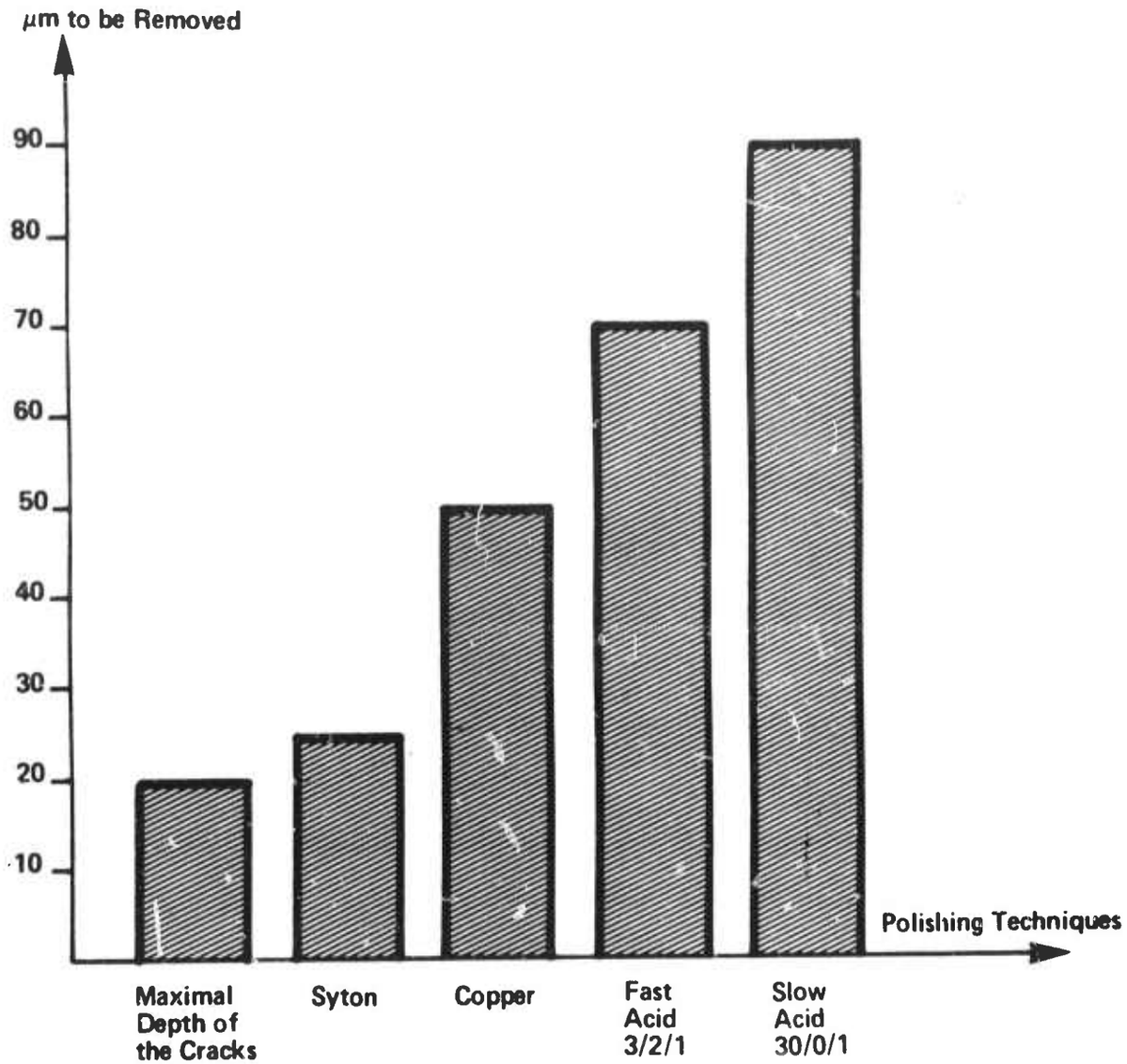

Fig. 14. Comparison of polishing techniques (damage depth 20 μm).

for damage removal but the least effective one for crack propagation. This tendency reverses with the increasing chemical activity of the polishing media. The least effective polish is the slow chemical etch but this etch is very effective in crack propagation.

Based on x-ray topographic interferometry it has also been shown (14) that silicon microsplits show residual mismatch at the crack interfaces which is measured on the angstrom scale. Such measurements are well supported through our transmission electron microscopy results (Chapter 2 of this report) which used Moire contrast to make microsplits visible in transmission electron micrographs. Thus it becomes completely feasible that crack healing can be initiated and induced through artificial means, such as high temperature oxidations. This again is in good agreement with the findings presented in this paper and explains why careful reprocessing of wafers -- as was done here -- can improve the lifetime distribution as shown in Table V.

Healing is more likely for the smaller splits in agreement with the results obtained for the silicon dioxide polish after 20 and 25μm repolish. Larger splits are more difficult to anneal and lead to stacking fault formation as shown for the cupric ion polish after 40 and 50μm repolish;

consequently, degradation of minority carrier lifetime in repolished wafers depends on the number of splits that cannot heal free of faults.

SUMMARY

Damage removal on silicon surfaces has been studied. The damage is introduced through Impact Sound Stressing (ISS). The damage consists primarily of Hertzian fracture cones. The cones are approximately 50μm in size and extend 20μm below the surface. A damage density of approximately 10^4 to 10^5 fracture cones per cm^2 is achieved. The damage can be introduced reproducibly.

The damage removal rate of chemical and mechanical-chemical polishing techniques is measured. Silicon etch solutions consisting of mixtures of nitric, hydrofluoric and acetic acids are compared to cupric ion and silicon dioxide polish.

It is found that silicon dioxide repolishes the damaged wafer most effectively. A perfect surface is obtained after removal of the actual damage depth of 20 to 25μm. A minimum of crack propagation occurs. Cupric ion polish, with a polishing speed reduced to equal the one of silicon dioxide, requires twice the amount of damage depth removed to obtain a perfect surface. Chemical etching requires removal of at least four times the original damage depth.

Surface perfection is ascertained through optical microscopy, electron microscopy, x-ray topography and minority carrier lifetime measurements. It is shown that the polishing techniques investigated are limited in the effective removal of microsplits. Silicon dioxide polish is most effective in re-generating minority carrier lifetime in ISS wafers through surface repolish.

ACKNOWLEDGEMENT

Technical support was provided by Mr. C. P. Schneider for MOS measurements and by Mr. J. F. Francis for x-ray topography. The SEM work was done by Mr. R. G. Dessauer.

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Chapter 2

DEFECT PROFILES IN SILICON AFTER IMPACT SOUND STRESSING

by

H. Kappert, G. H. Schwuttke, and K. Yang

INTRODUCTION

Advanced silicon technology relies on the "perfect" silicon wafer. The silicon wafer is manufactured from a large single crystal silicon boule using high speed slicing techniques. Subsequently, sophisticated processing efforts are made to produce a "damage-free" wafer surface. Key processing steps to achieve this goal rely on chemical-mechanical polishing techniques as described in Chapter 1 of this report. Accordingly, all polishing techniques used in semiconductor manufacturing produce a more or less perfect surface. Complete removal of saw damage is very difficult and is practically impossible.

From the viewpoint of low leakage silicon technology it is important to understand the mechanism of surface damage and its subsequent annealing during oxidation or other high temperature processing steps. One of the main results of this contract work shows that residual mechanical damage in silicon surfaces can cause undesirable leakage currents in advanced silicon devices[1].

It is interesting to note that even today surface damage in covalently bonded crystals, such as silicon, is ill understood. Numerous workers in the field have studied damage in semiconductor crystals caused by grinding, polishing or lapping. These studies are aimed primarily at determining the "damage depth". For a review of this work see Technical Report No. 3 of this contract.

The crystallographic nature of such damage has also been studied and has been the subject of some controversy. Some investigators concluded that damage introduces dislocations into the crystals; others concluded that damage consists entirely of cracks. There seems to be general agreement at least on the formation of dislocations whenever damaged semiconductor samples are annealed. Excellent data on surface damage of abraded silicon wafers are given by R. Stickler and G. R. Booker.[2] These authors examined single crystal silicon specimens after unidirectional abrasion. The abrasives ranged from 0.25 micron diamond to No. 240 SiC paper. Their transmission electron microscopy data showed that the damage varied in a progressive manner with the severity of the abrasive treatment.

The damage ranged from rows of single dislocations to bands of dislocations and cracked material. The corresponding depth of damage ranged from 0.2μm to 25μm. For fine abrasion they observed an anisotropy of damage. This feature disappeared for the coarse

abrasive. They noted also that annealing changed the dislocation configurations and also that new dislocations were propagated to achieve relief of elastic strains.

Due to the complexity of "damage" in silicon surfaces none of the previous investigations could provide a dislocation analysis. Consequently, the annealing of damage is only partially understood and no experimental facts are available to support a cause and effect relationship between damage and stacking fault generation.

Impact Sound Stressing of silicon is a novel approach to introduce damage into silicon surfaces. This technique has found unique utilization not only in degrading silicon surfaces in a controlled manner, thus enabling one to make detailed damage studies, but also in using mechanical damage to improve silicon surfaces. This may sound paradoxical, but only confirms the old contention that mechanical damage on the wafer backside can be beneficial for device processing on the front side of the wafer.[3,4]

Consequently, it is important to understand the ISS damage profile in silicon existing before and after device processing. In this context Chapter 2 of this report describes detailed transmission electron microscopy investigations undertaken to provide data on the defect state of silicon after ISS and subsequent annealing through high temperature oxidation. Chapter

2 also provides a good example of the usefulness of ISS in damage studies of covalently bonded crystals. It provides results that are otherwise very difficult or impossible to obtain.

EXPERIMENTAL

Transmission electron microscopy (TEM) specimens of impact sound stressed wafers were prepared by ultrasonically cutting 3 mm diameter pieces out of the wafers and subsequently thinning the specimens in a standard manner using the jet-etching technique. On some wafers the sound stressed surface was repolished 10 to 15 μm before TEM specimen preparation. Thus it was actually possible to investigate crack tips of fracture cones. Post annealing properties of ISS'ed samples were also investigated. Two types of differently prepared samples were used for such investigations. The first type consisted of 3 mm diameter specimens ready for the microscope. Such specimens were investigated before and after heat-treatment. Thus the same defect area was observed in the TEM before and after heat-treatment. Other experiments used specimens cut out of as-stressed wafers. Subsequently, the wafers were heat-treated and new specimens were cut out from the heat-treated wafers. Good agreement was observed between such differently prepared specimens.

Wafers or TEM specimens were heat-treated mainly through short and long time oxidations. In some instances annealing was done

in nitrogen. Short time oxidations were made on 3 mm diameter TEM specimens at 1000°C or 1100°C in dry oxygen for time intervals of 5, 10, 15, and 20 minutes. For long time oxidations sound stressed wafers were oxidized at 1000°C using a 10-90-10 minute standard dry-wet-dry oxidation cycle. Oxide thickness after such cycles was 5000Å. For the TEM investigations the oxide layer was removed.

Nitrogen annealing, when used, was done for 30 minutes at 1000°C.

The TEM examinations were made through use of various microscopes such as a 200 keV Hitachi HU 200, a 200 keV JEOL and a 100 keV Philips EM 300. Double tilt stages providing specimen tilt up to 45 degrees are available with the microscopes.

Sound stressing of the wafers was normally done at a power of 40 watts for 5 minutes at a frequency of 1380 cycles as described in Chapter 1 of this report. For details of the ISS technique see Technical Report No. 4.

In several instances lifetime measurements were made using the MOS capacitor technique developed by W. Fahrner and C. Schneider. For details on this measurement technique see Technical Report No. 6 or J. Electrochem. Soc. 123, 100 (1976).

RESULTS

1. Optical Survey of ISS Damage

ISS of silicon wafers produces two damage features: a fine, strongly directional abrasion leading to shallow grooves, and the formation of Hertzian fracture cones. Both features are displayed in the optical micrographs of Figs. 1a,b. The abrasion is more pronounced at low stressing power (Fig. 1a). The crack density increases dramatically with power input and is the leading feature at high power (Fig. 1b).

The grooves are bunched together in clusters and are indicated in the photomicrograph of Fig. 1a at positions marked A, B, C, D. A scanning electron micrograph of such a damage cluster shows clearly their groovelike nature. An example is given in Figs. 2. A typical cluster area in the examples shown in Figs. 1 and 2 is approximately 10 to 15μm^2 large and the density of grooves in a cluster is 1 per μm^2. A fracture cone measures approximately 50μm along one side. The damage depth for the grooves is approximately 0.2 to 0.4μm and the fracture cone depth varies from approximately 10 to 20μm.

Detailed electron microscopy studies of both types of damage have been made and are reported in the following sections.

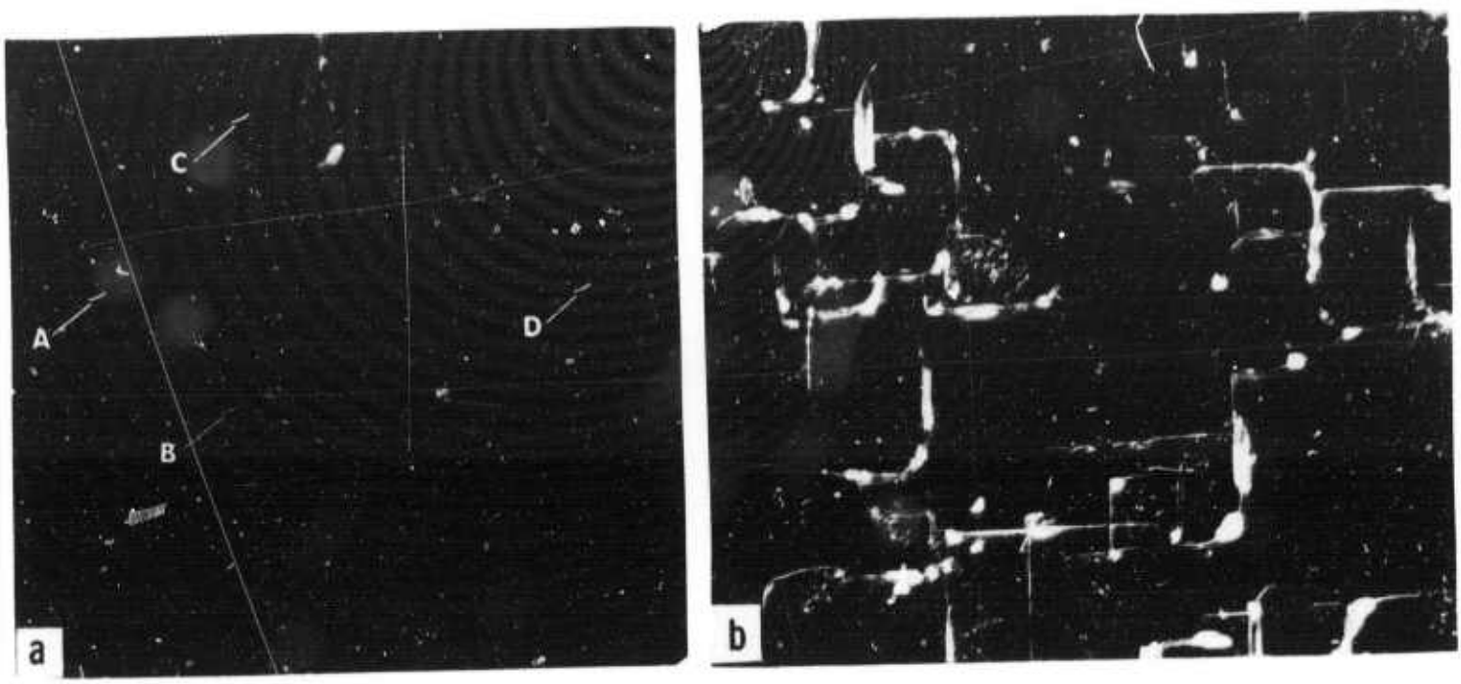


Fig. 1. Photomicrographs of damage in (001) silicon wafer surface after ISS showing abrasion and Hertzian cone fracture.

a. Abrasion. (~370X)
b. Fracture. (~370X)

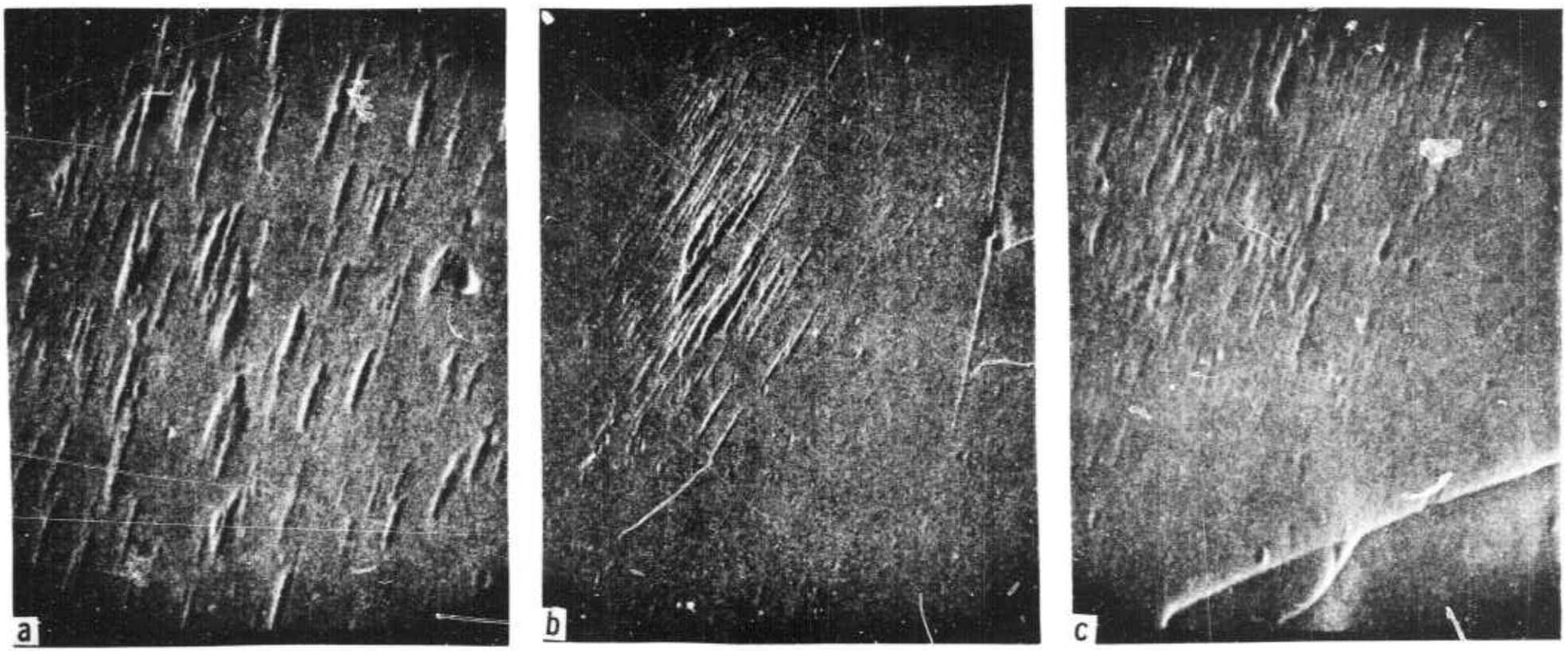


Fig. 2. Scanning electron microscope picture of cluster damage due to grooves as seen in Fig. 1a.

a. at position A.
b. at position B.
c. at position C.

2. Transmission Electron Microscopy (TEM) of ISS Damage

2.1 Fracture Cones - General Observations

Impact sound stressing of silicon results in perfect Hertzian fracture cones (Figs. 1a,b). Such cones can be produced with any desired density up to a concentration of about $10^6/cm^2$. A larger density results in wafer breakage.

Specimen preparation for electron microscopy of samples containing fracture cones is possible using standard jet etching techniques. Crack tips can be investigated when part of the sound stressed surface layer is removed by silicon dioxide polishing. A composite micrograph of a fracture cone split is shown in Fig. 3. This picture is unique because practically the entire split is available for inspection in the microscope. Only a small part around the 90° - bend is etched out during specimen preparation. The split in the silicon lattice is revealed through electron interference (Moire) fringes. Such fringes are characteristic for the fracture cones and indicate imperfect closure (out of registry) of the lattice.

A cone fracture on a wafer surface causes three different types of lattice distortion:

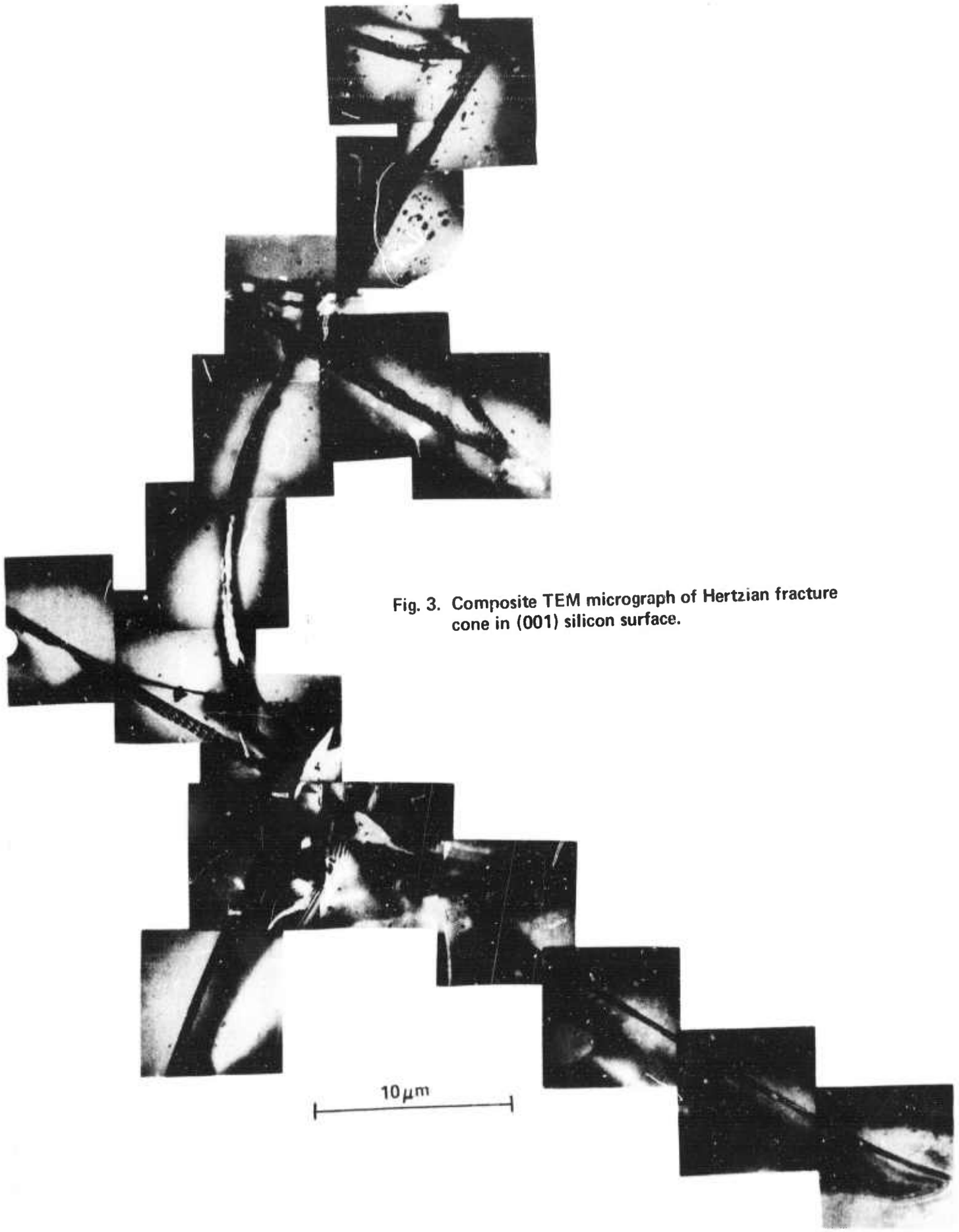


Fig. 3. Composite TEM micrograph of Hertzian fracture cone in (001) silicon surface.

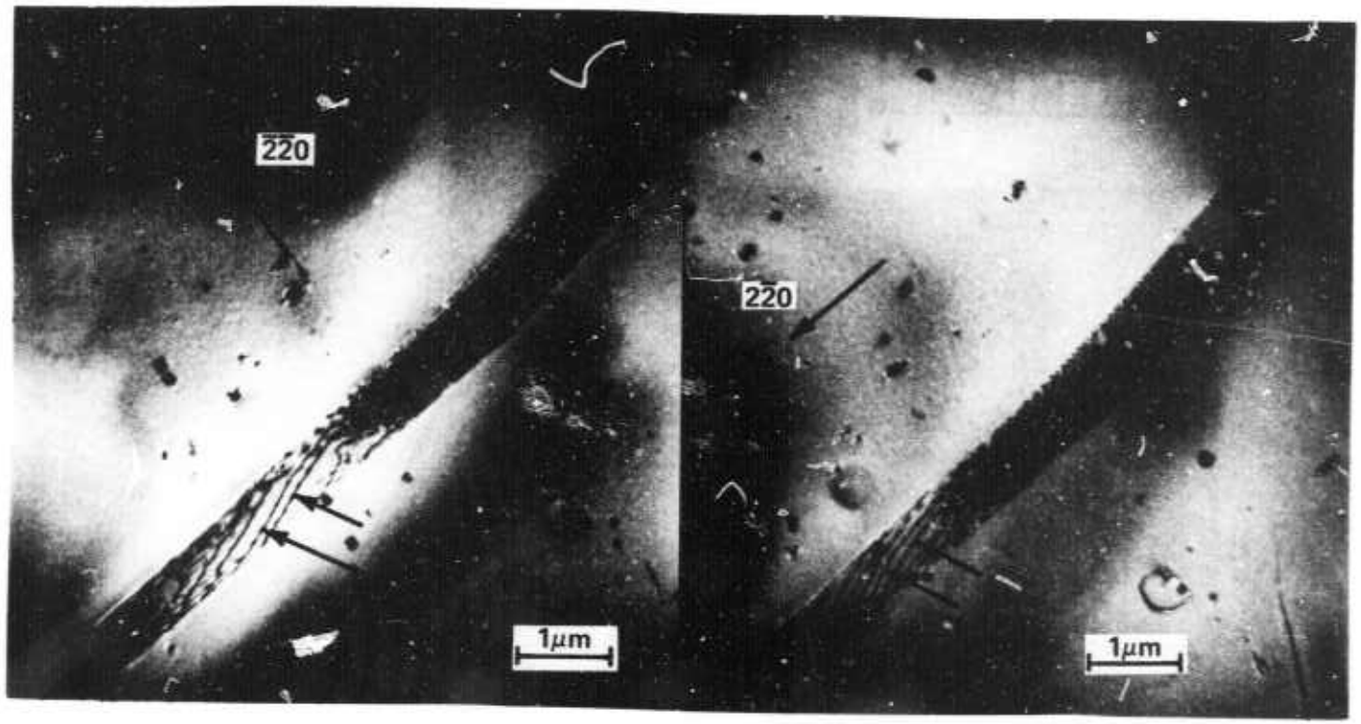
A. A rotation of both surface parts of the fractured wafer surface around an axis perpendicular to the surface.

B. A rotation of both surface parts of the fractured wafer surface around an axis parallel to the surface and parallel to the crack (bending).

C. Translation of the split crystal parts by a vector R mainly in (011) or (101) type directions for (001) surfaces in (111) or (011) planes (block slip).

In general all three effects are present simultaneously. Thus the lattice distortions overlap and produce a rather complicated Moire pattern. Simple patterns are seen for cracks lying in the cleavage planes. Such Moires consist of pure translational fringes and the crack image looks very much like a stacking fault. This similarity is very striking if "closure" of the crack has taken place. This is always the case for areas close to the crack tip. Examples are given in the micrographs of Figs. 4a and 4b. These micrographs are obtained from partially repolished samples.

The degree of bending introduced into the wafer surface as described in (B) can be estimated quite accurately by observing the shift of Kikuchi lines in the diffraction patterns generated by the two crystal parts. This is shown in the micrographs of Figs. 5 and 6. The amount of bending introduced by the fracture



a b

Fig. 4. Microcrack on a (111) plane showing cleavage dislocations and Moire pattern. (a) g = 220 and (b) g = 220. Note: Cleavage dislocations stay in position.

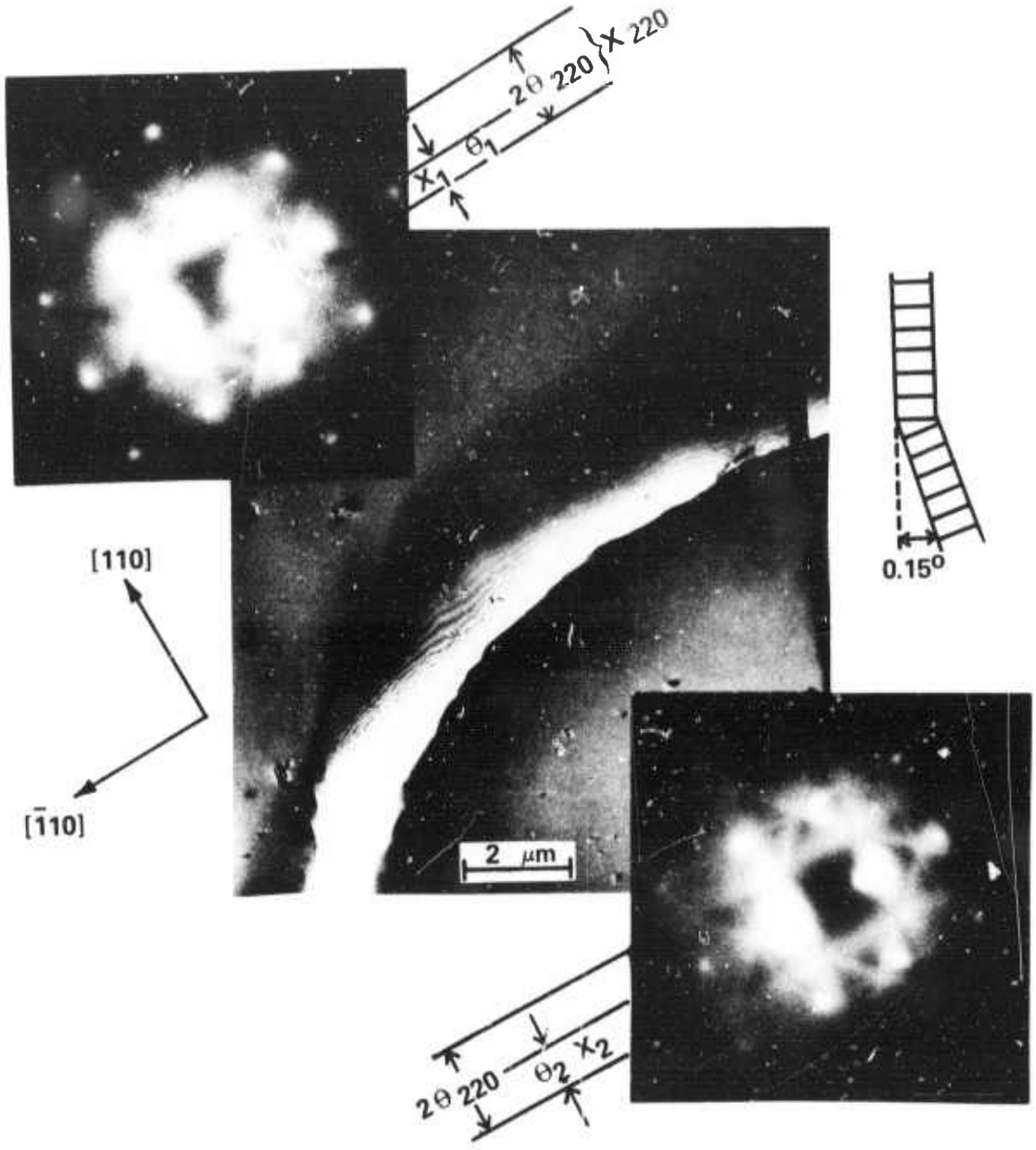


Fig. 5. Determination of crystal bending $\Delta\theta$ from the shift of the Kikuchi lines on one side of the crack with respect to the other. In the microcrack shown, $\Delta\theta = \theta_2 - \theta_1 \approx (X_2 - X_1)(2\theta_{220})/X_{220} \approx 0.15^o$ where $2\theta_{220} \approx 0.75^o$.

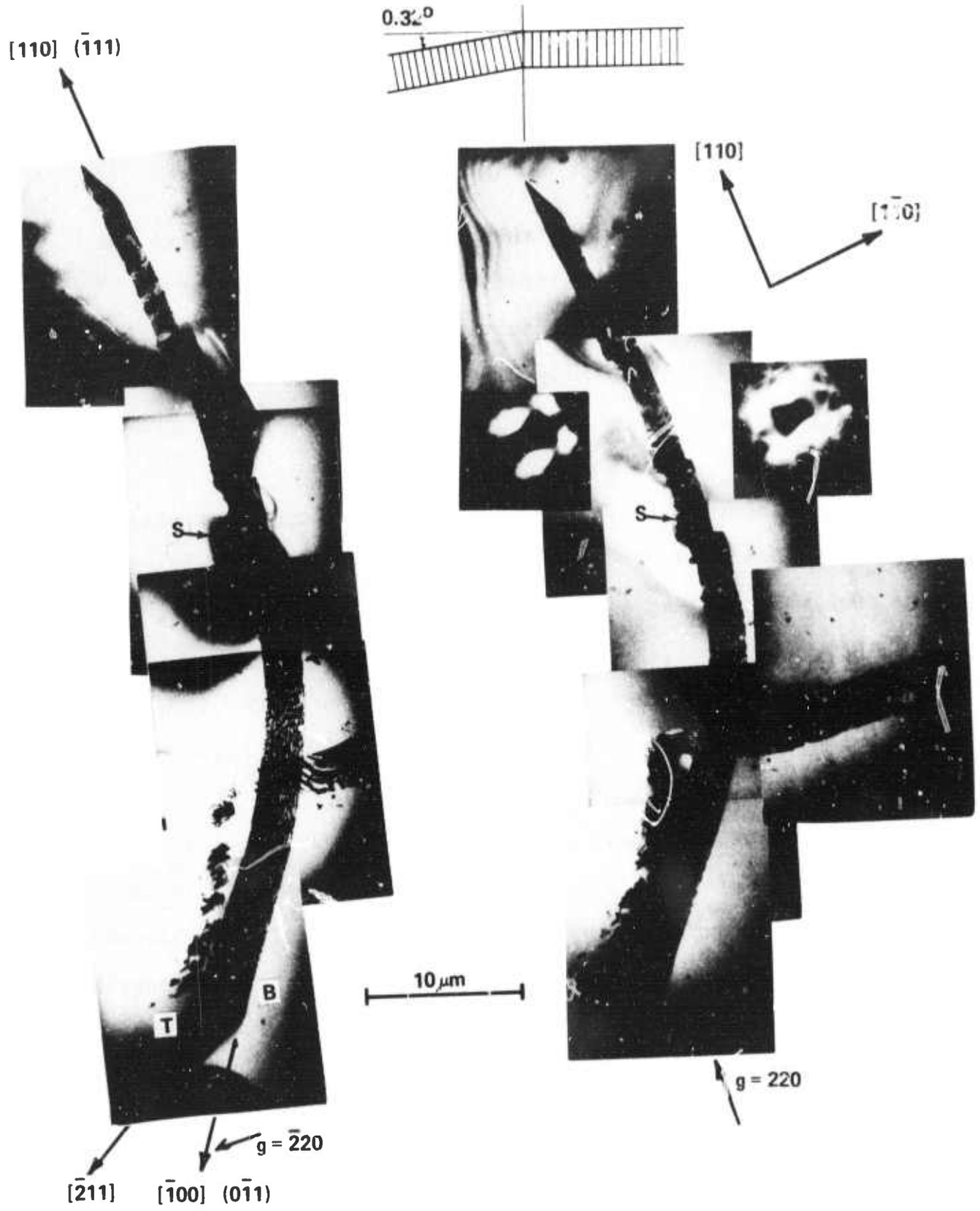


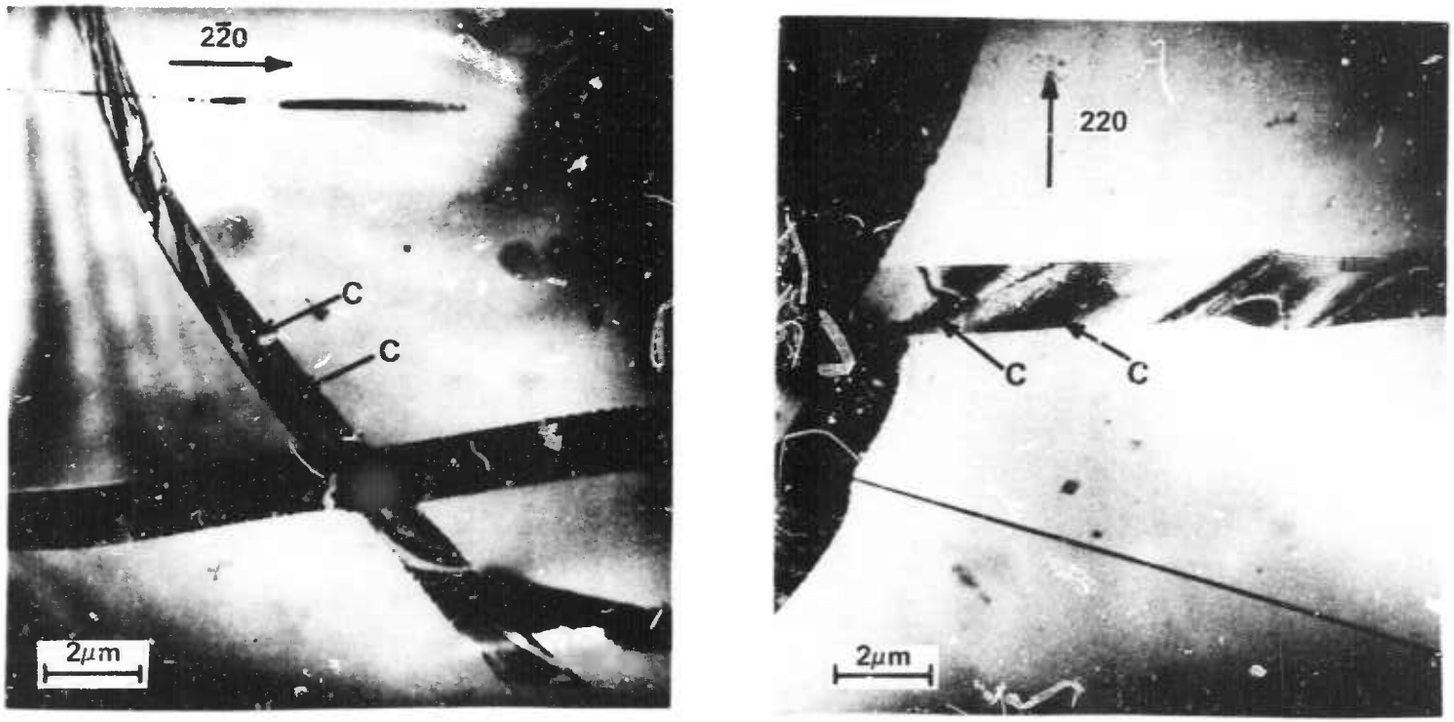
Fig. 6. Microcrack in <110> and <100> direction. The crack is located on a (1̄11) plane at the upper section of the photomicrograph and on a (01̄1) plane at the lower section of the micrograph. Note: T = Top of crack; B = Bottom of crack; S = Stress center.

cones is approximately several 10ths of a degree.

The boundary line terminating the crack inside the crystal has been compared to an edge dislocation[5]. In (001) silicon we find that such boundary lines terminating cracks lie on (111) planes and have (011) or (112) directions. This is shown in the micrographs of Fig. 7.

Cleavage dislocations have also been discussed in the context of crack formation[5]. Such cleavage dislocations stay in position within the crack whenever the operating g-vector of the recording reflection is changed (Figs. 4a,b). Cleavage dislocations appear whenever the crack direction starts to deviate from the <110> direction. Examples of cleavage dislocation are also shown in Figs. 7a,b.

Changes in crack direction can be as large as 45 degrees for fracture cones on (001) surfaces. A 90 degree turn in crack direction is accomplished by two 45 degree directional changes of the crack. Such a large change in crack direction is possible through "cleavage plane hopping." This is demonstrated in the TEM micrographs in Fig. 6. Comparing the directions of the crack as indicated in the micrograph for the upper and lower part of the crack and considering that the crack intersects the (001) wafer surface (front and back) it follows that the (110) part of the crack lies in a $(\bar{1}11)$ plane while the $(\bar{1}00)$ part of the crack is positioned in the $(0\bar{1}1)$ plane. This "cleavage plane



a b

Fig. 7. Microcrack 10 μm below the surface showing cleavage dislocations and Moire pattern similar to stacking fault contrast. (a) g = 2$\bar{2}$0, (b) g = 220 reflection. Note cleavage dislocations at C.

hopping" is accomplished through the presence of "cleavage dislocations" which divide the crack into several sections for successful turnaround.

A large strain field is observed in the center part of the crack shown in Fig. 8 which is recorded with the g-vector perpendicular to the crack direction. Such large strains inside the cracked crystal area are relieved during sample annealing. However, sample annealing causes the formation of dislocations outside the crack area. A typical example is shown in the micrographs of Fig. 9 and reveals dislocation formation in ISS'ed samples after annealing in nitrogen. Similar results are obtained for annealing in oxygen.

The simple equation $\theta = N.b/D$ can be used to estimate the number of dislocations necessary to relieve the strain connected with a crack in the lattice (θ = lattice tilt due to crack, N = number of dislocations, b = Burgers vector of dislocation, D = spacing between dislocations). The lattice tilt θ can be measured using the Kikuchi technique as described in connection with Fig. 5. This tilt is approximately 0.15 degrees. Thus it is calculated that only 6 dislocations are necessary to relieve the strain field connected with a fracture cone line in silicon. This value is in good agreement with the experimental findings (Fig. 9).

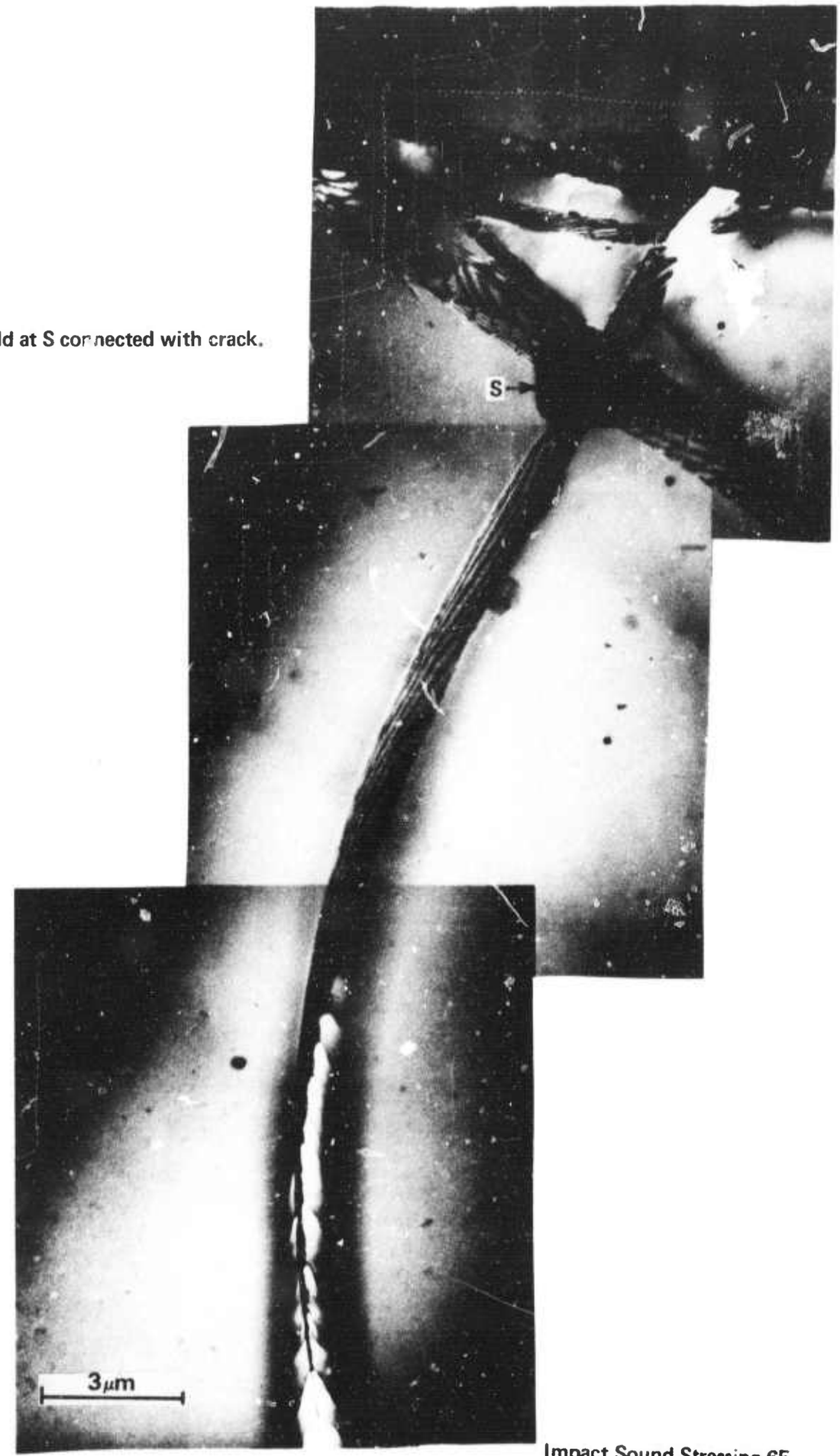


Fig. 8. Strain field at S connected with crack.

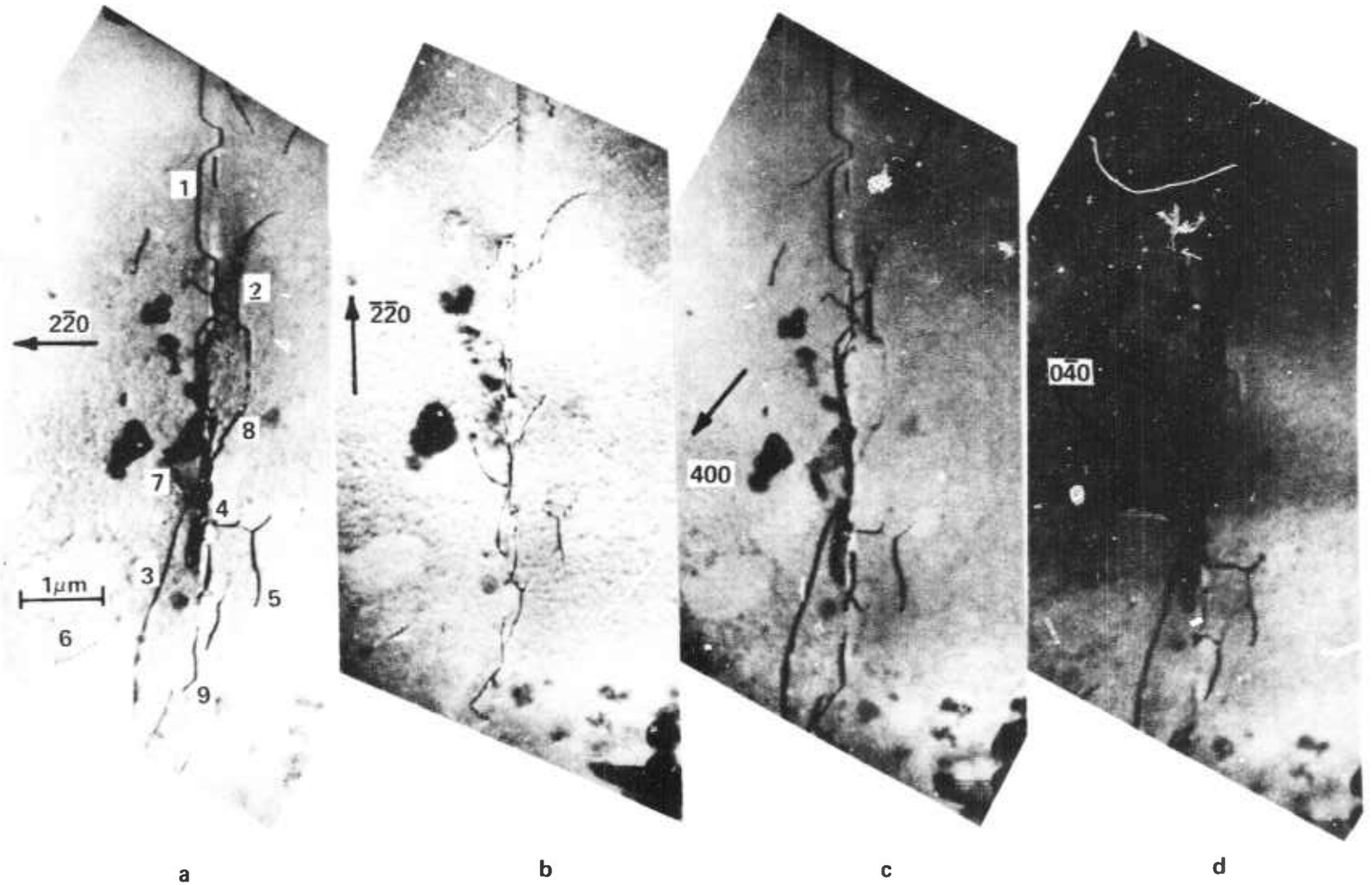


Fig. 9. Area of a microcrack after 1 hr anneal at 1100°C. Micrographs recorded with different operating g-vectors for Burgers vector analysis. (a) $2\bar{2}0$, (b) $\bar{2}\bar{2}0$, (c) 400, (d) 311 reflection.

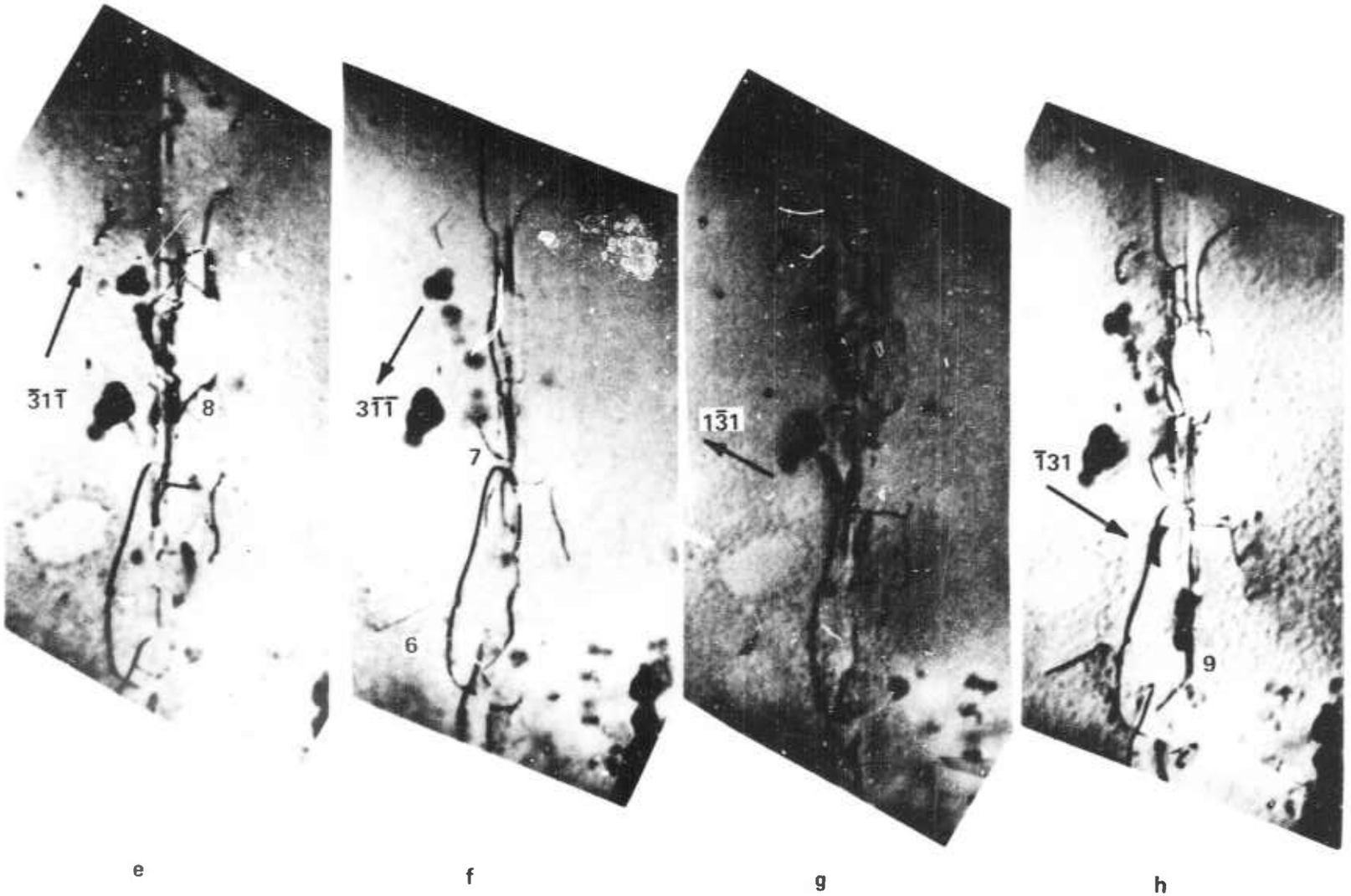


Fig. 9. Area of a microcrack after 1 hr anneal at 1100°C. Micrographs recorded with different operating g-vectors for Burgers vector analysis. (e) $3\bar{1}\bar{1}$, (f) $0\bar{4}0$, (g) $1\bar{3}1$, (h) $\bar{1}31$ reflection.

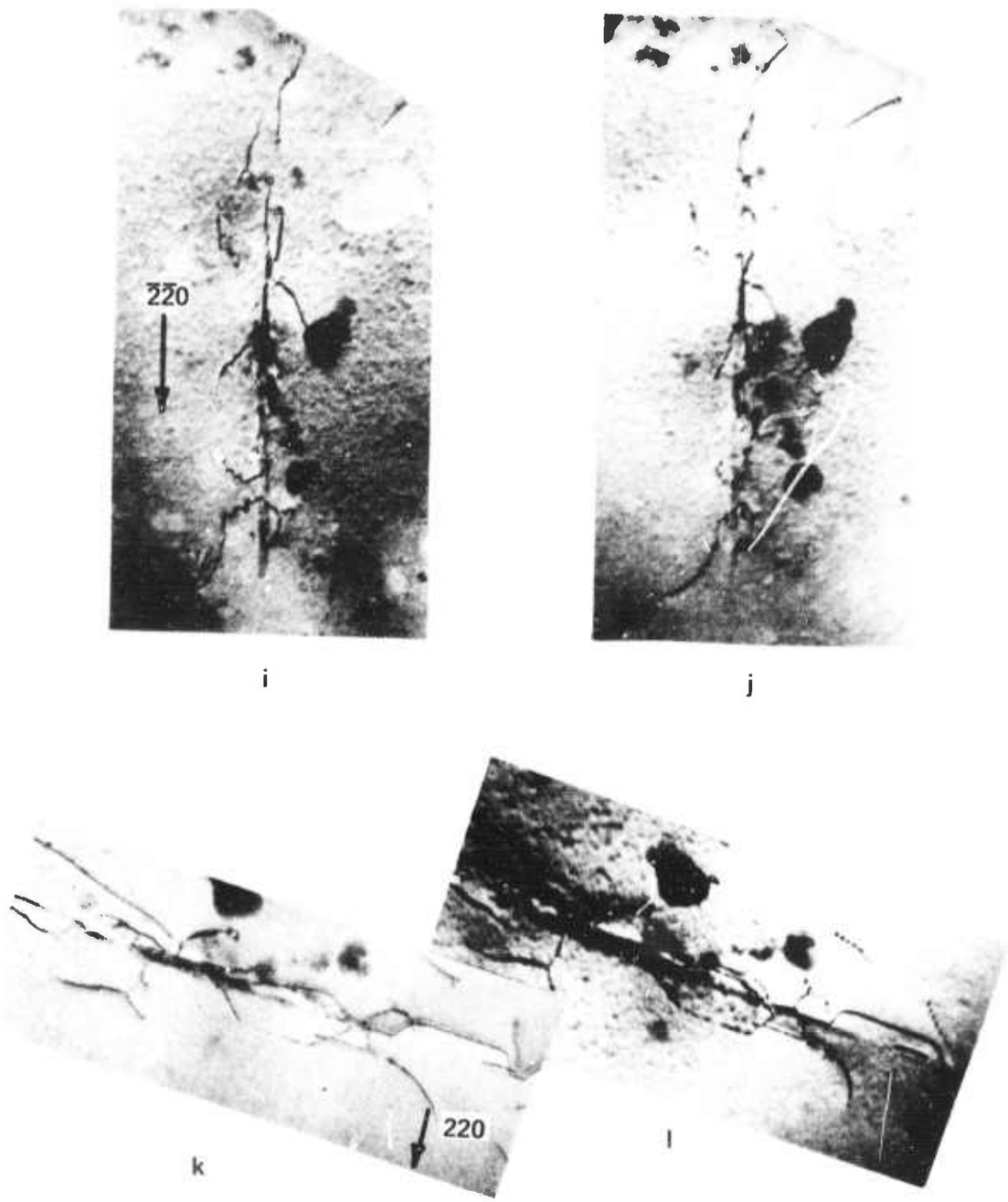


Fig. 9. Area of a microcrack after 1 hr anneal at 1100°C. Micrographs recorded with different operating g-vectors for Burgers vector analysis.

(i) and (j) stereo set taken with $\bar{2}\bar{2}0$ reflection;
(k) and (l) stereo set taken with $2\bar{2}0$ reflection.

2.2 TEM of Fracture Cones - Dislocation Analysis

In the context of the overall goals of the contract work it is important to assess the final "defect profile" present in impact sound stressed wafers, specifically after various high temperature processes have been imposed on such wafers. The leading question to be answered relates to the position and distribution of the dislocations generated during the annealing (oxidation) cycles. Such questions can only be answered through extensive Burgers vector analysis of the dislocations surrounding fracture cones after annealing cycles.

Numerous Burgers vector investigations of dislocations around fracture cones after different annealing cycles were performed. All the Burgers vectors observed in connection with strain relief through dislocation generation in ISS'ed wafers are summarized in Table I. Representative electron micrographs of the detailed analyses performed are given in the various micrographs of Fig 9. A Kikuchi line map indicating the different tilt position of the specimen for the recording of the micrographs of Fig. 9 is given in Fig. 10.

Only two Burgers vectors are connected with the dislocations. Accordingly, we are dealing with 60 degree

Table I

Determination of Burgers Vectors for Dislocations Generated in ISS'ed Wafers

Disl. No.	Burgers Vector	g.b=0 if g=	See Fig No.	Line Direction	Type
1	$\bar{1}10$	$\bar{2}\bar{2}0$	9b	$\bar{1}\bar{1}0$	90°
2	$\bar{1}10$	$\bar{2}\bar{2}0$	9b	$\bar{1}\bar{1}0$	90°
3	$\bar{1}$ 0	$\bar{2}\bar{2}0$	9b	$\bar{1}\bar{1}0$	90°
4	$\bar{1}10$	$\bar{2}\bar{2}0$	9b	$\bar{1}10$	0°
5	$\bar{1}10$	$\bar{2}\bar{2}0$	9b	$\bar{1}\bar{1}0$	90°
6	011	400 and $\bar{3}1\bar{1}$	9c and 9e	101	60°
7	011	400 and $\bar{3}1\bar{1}$	9c and 9e	$0\bar{1}1$	90°
8	$01\bar{1}$	400 and $3\bar{1}\bar{1}$	9c and 9f	101	60°
9	$10\bar{1}$	$0\bar{4}0$ and $1\bar{3}1$	9d and 9g	110	60°

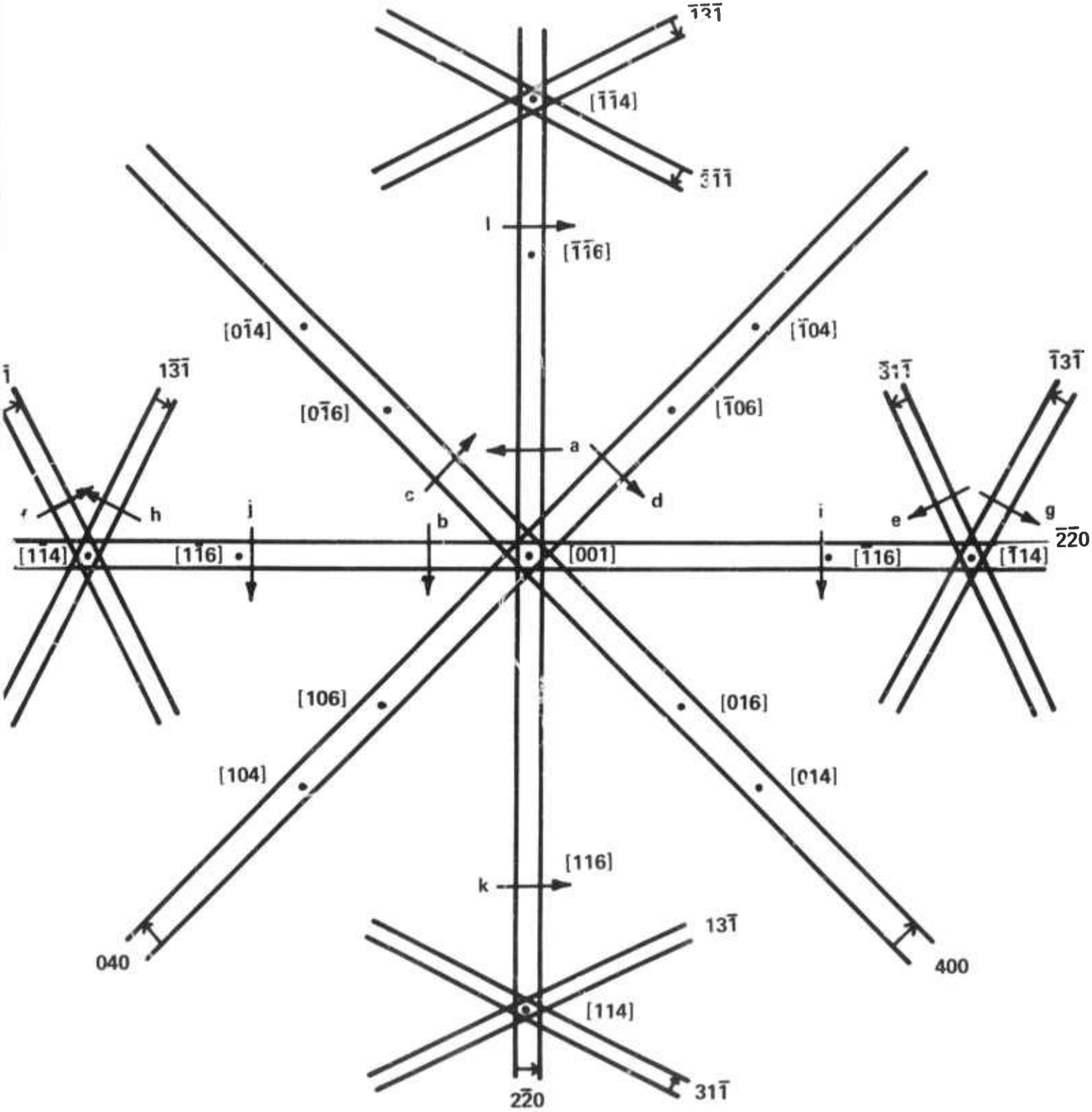


Fig. 10. Kikuchi line map showing position of the operating g-vectors indicated by arrows used for taking the micrographs shown in Fig. 9.

and 90 degree dislocations. The 90 degree dislocation in silicon is a sessile dislocation and a reaction product of two 60 degree dislocations according to the equation: $(a/2)[\bar{1}10] + (a/2)[0\bar{1}1) \rightarrow (a/2)[\bar{1}01)$

Based on the Burgers vector analysis we reach the following conclusion:

The defect profile obtained after high temperature annealing of fracture cones in (001) silicon wafers consists of a dislocation network located in the vicinity of the fracture cone tips - approximately 20 to 30μm below and parallel to the Impact Sound Stressed (001) surface. Dislocation propagation to the other side - the non-stressed wafer surface is not observed.

These structural findings are in agreement with generation lifetime measurements made on the undamaged silicon surface of sound stressed wafers.[6] Such electrical measurements indicated that generation lifetime distribution of minority carriers across the undamaged wafer surface improved considerably through wafer backside Impact Sound Stressing.

This again confirms that dislocations do not propagate to the undamaged wafer surface. It follows that back-

side ISS of silicon wafers can be advantageously used to improve the electrical characteristics of the wafer frontside. Such experiments have been made and improved lifetime characteristics have been obtained on ISS'ed substrates as well as on epitaxial layers deposited on ISS'ed substrates. Such experiments are discussed in Part II of this report.

3. TEM Analysis of Abrasion Damage

This section discusses the defect profiles connected with the abrasion or groove damage which is present in Impact Sound Stressed silicon wafers. The groove analysis is made before and after annealing the wafers.

3.1 Post ISS Properties of Grooves

This type of ISS damage on silicon surface is responsible for dislocation bands. A typical example is given in Fig. 11. Such dislocation bands are composed of dislocation loops and appear in rows oriented along <100>, <110> or <120> directions (Fig. 1a). However, the intersections of all loops with the (001) surface is always a <110> direction indicating that the loops are located on (111) glide planes. Stereo-micrographs of such dislocation bands are given in Figs. 12 and show loops in (111) and ($\overline{1}\overline{1}1$) planes.

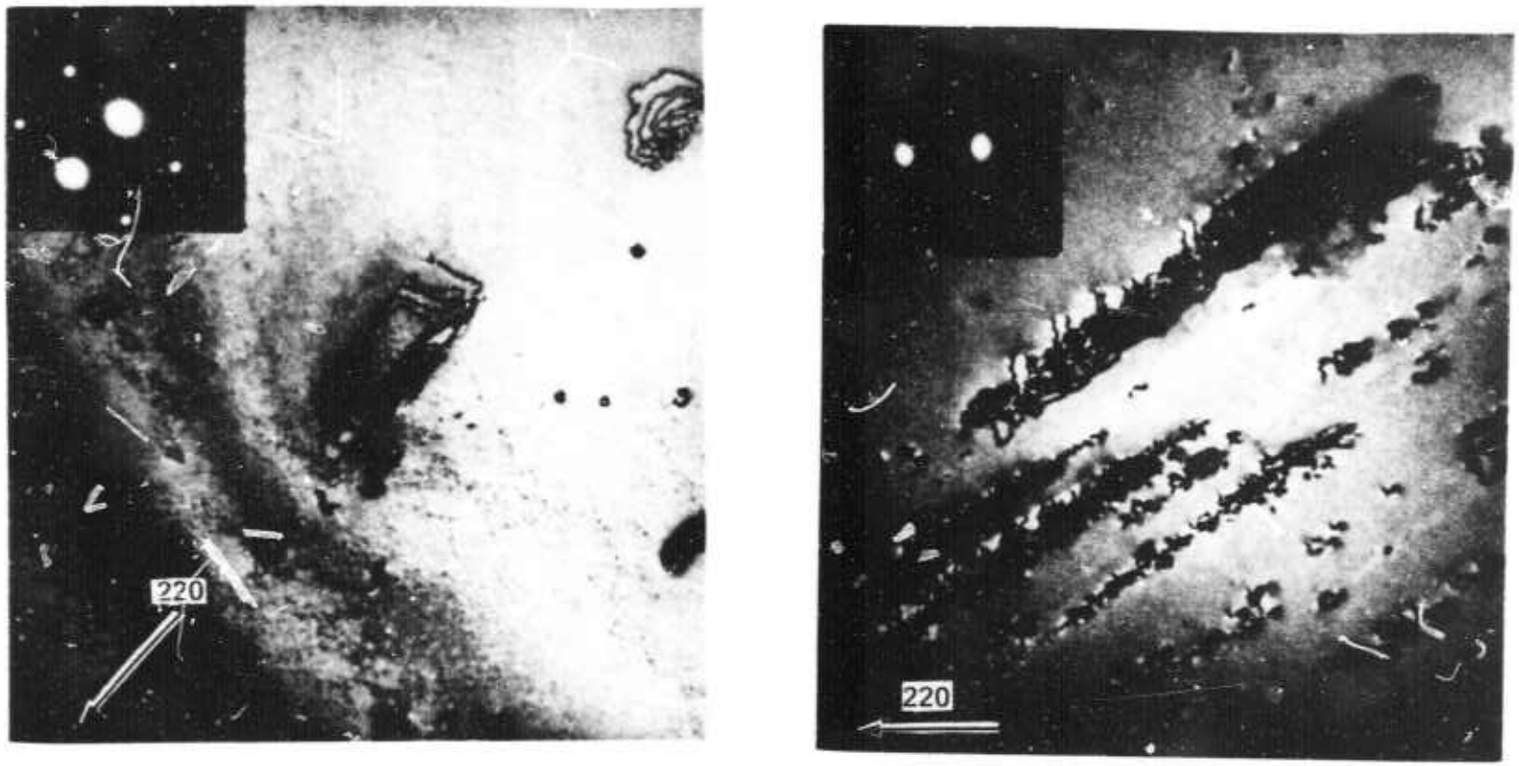


Fig. 11. TEM micrograph of grooves showing dislocation bands.

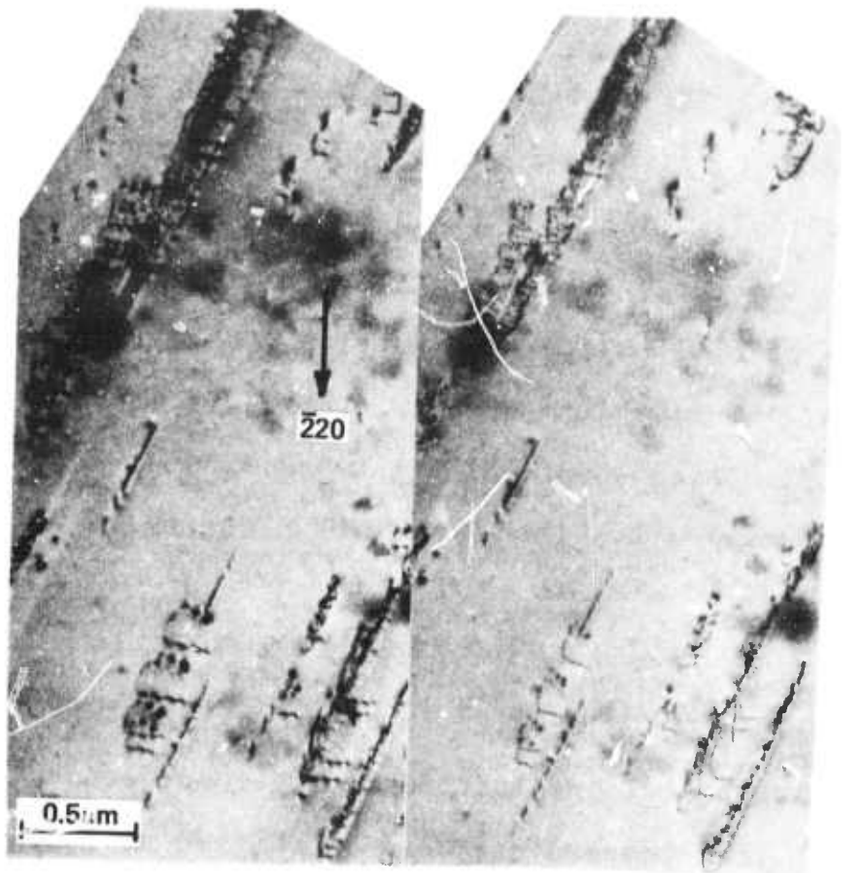


Fig. 12. Stereo set of dislocation loops for slip plane analysis.

To understand the annealing properties of the dislocation bands Burgers vector determination of the dislocations are necessary. Such an analysis leads to the loop structure drawn schematically in Fig. 13.

The detailed loop structure shown in Fig. 13 is obtained from the analysis of several sets of TEM micrographs recorded for (400), (111) and (113) reflections (Fig.14). Accordingly, the Burgers vector of the loops is contained in the (111) or ($\bar{1}\bar{1}$1) plane with Burgers vector (a/2) [01$\bar{1}$] or (a/2)[101]. Consequently, these dislocations are mixed dislocation loops which lie and expand in the {111} slip planes. Thus the loops are of the shear type.

It is considered a main result of this investigation that the dislocation loops introduced by Impact Sound Stressing (at room temperature) are identified as "shear loops" consisting of segments of 60 degree and 30 degree dislocations. This confirms again that "plastic flow" in silicon at room temperature is possible. However, the types of dislocations and their arrangements observed differ from those observed in silicon deformed at higher temperature where screw and 60 degree dislocations predominate. Typically, for silicon after low temperature deformations are arrays of 30 degree dislocations, which are absent in high temperature plastic flow. Consequently,

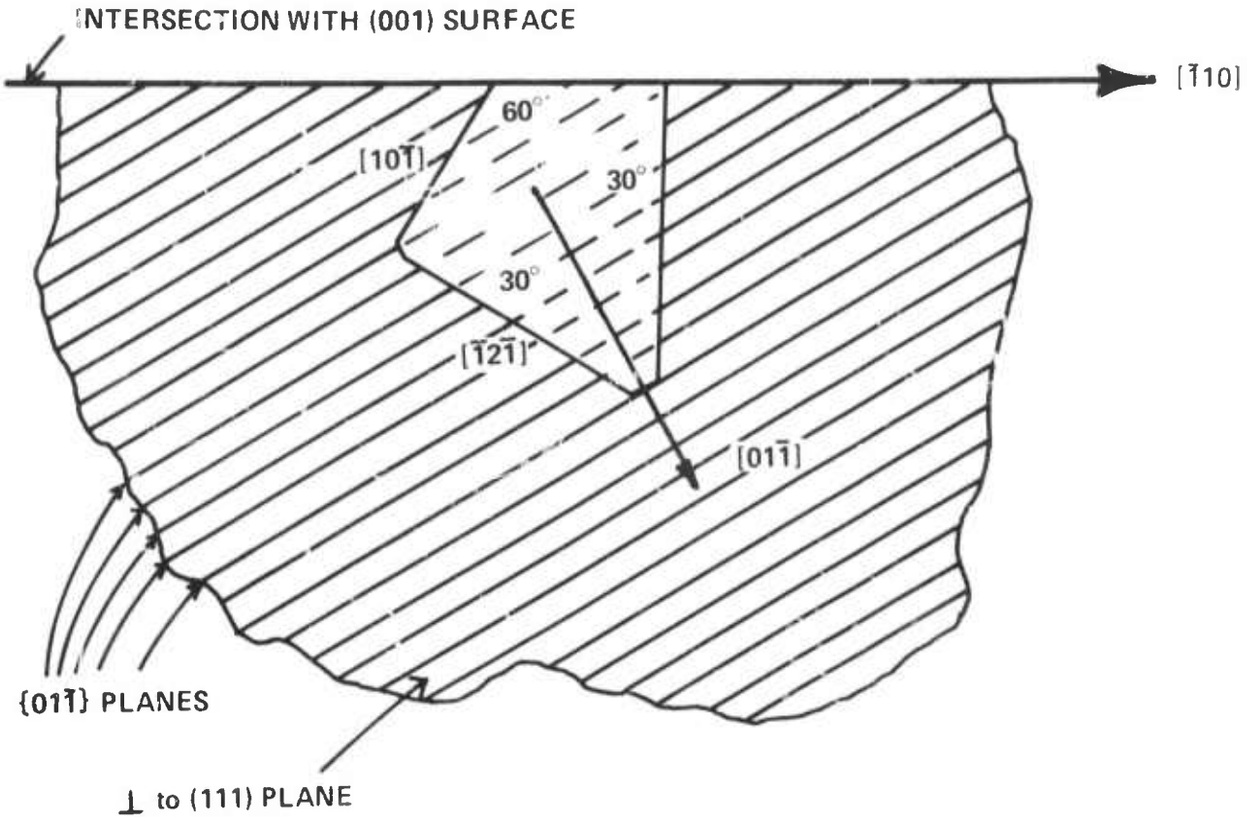


Fig. 13. Structure of shear loop. Loop expands in (111) loop plane and consists of 60^{o} - and 30^{o} - segments with Burgers vector along $[01\bar{1}]$. Analysis is based on micrographs of Fig. 14.

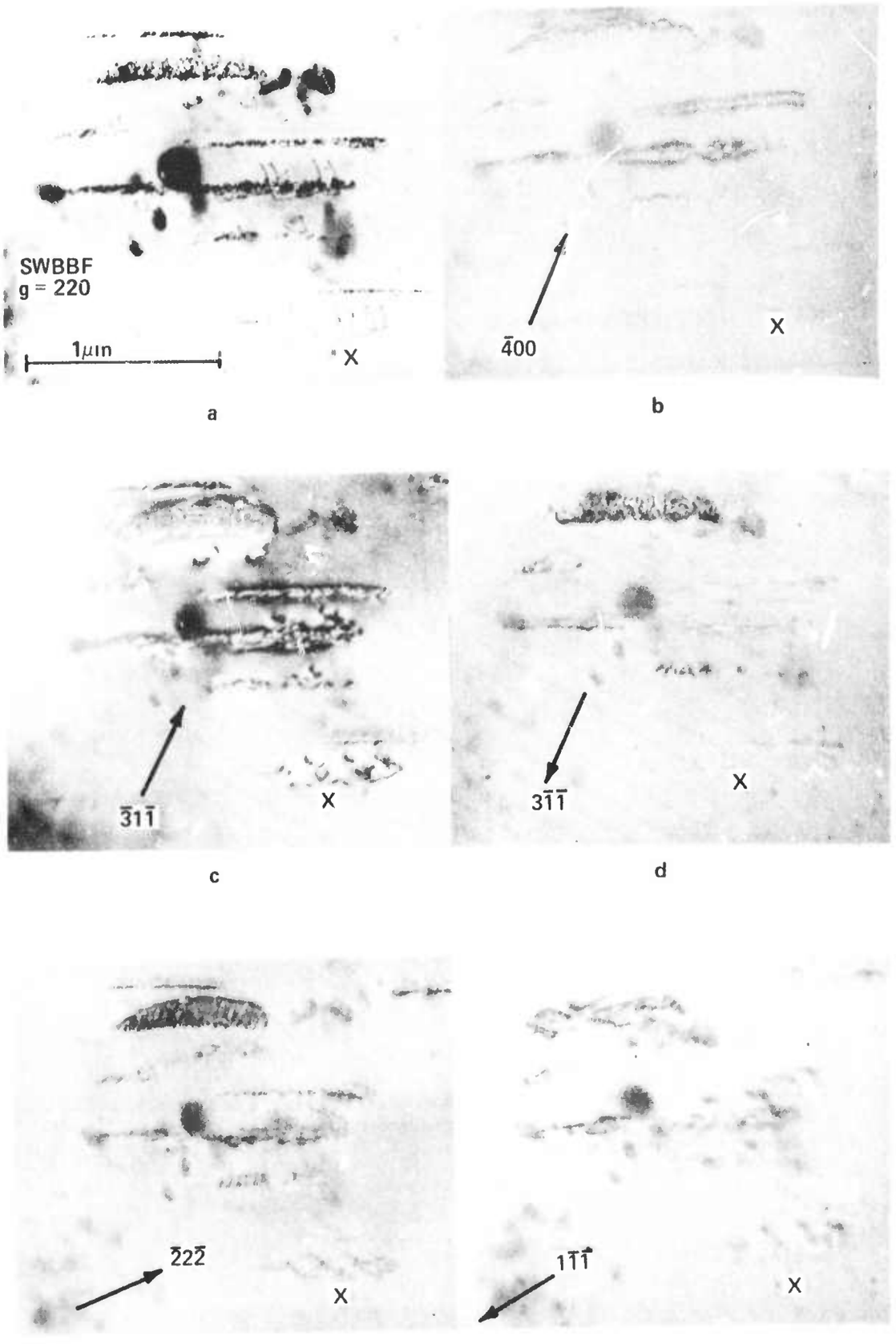


Fig. 14. Set of TEM micrographs taken in a Philips EM 301 with (a) SWBBF (220), (b) $\bar{4}00$, (c) $\bar{3}1\bar{1}$, (d) $31\bar{1}$, (e) $\bar{2}2\bar{2}$, (f) $1\bar{1}\bar{1}$ reflection.

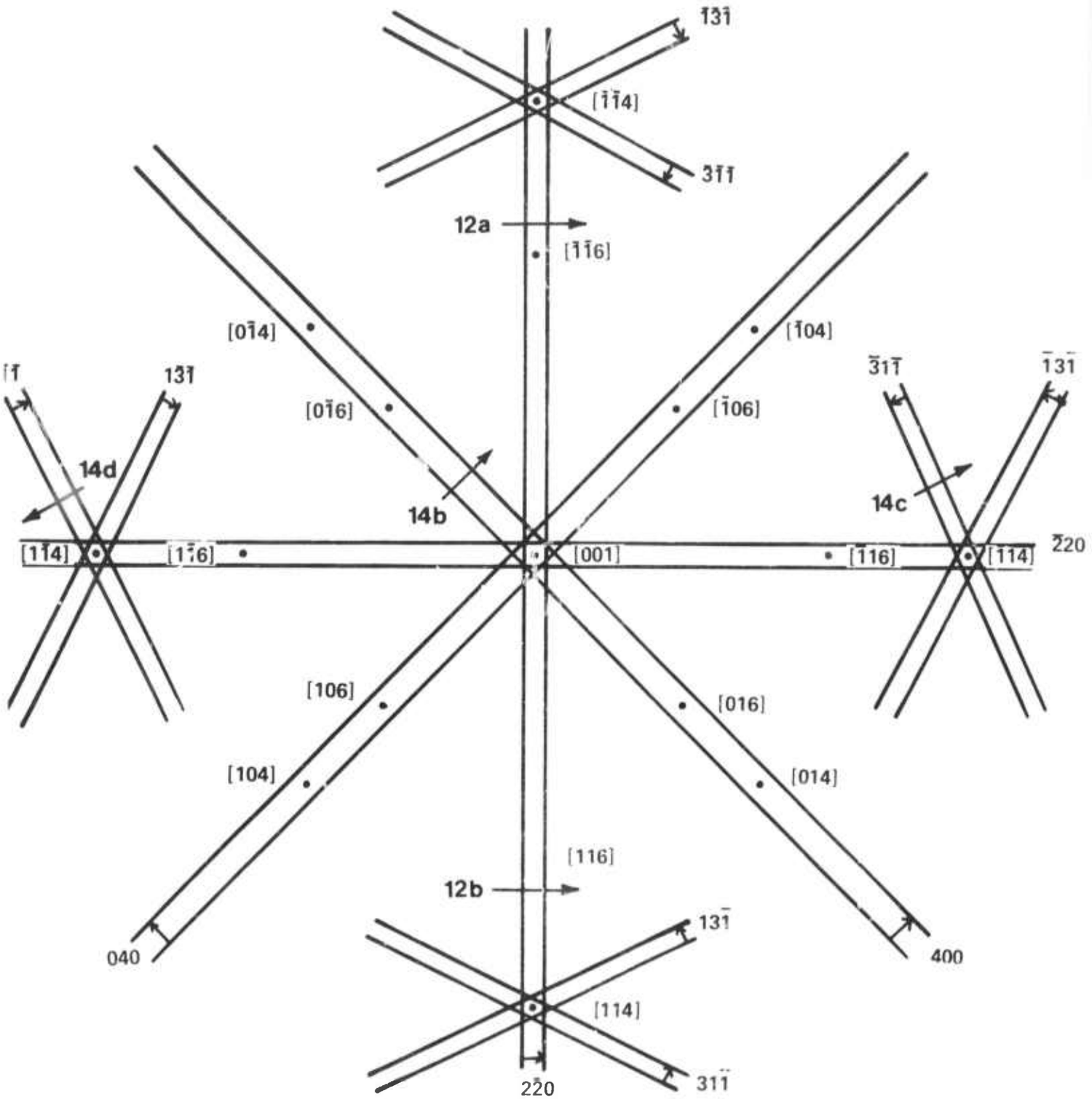
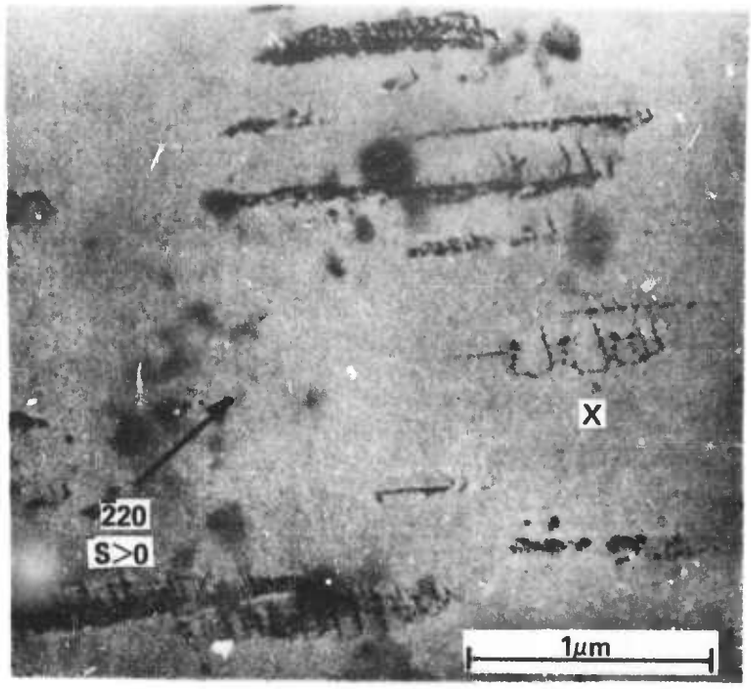


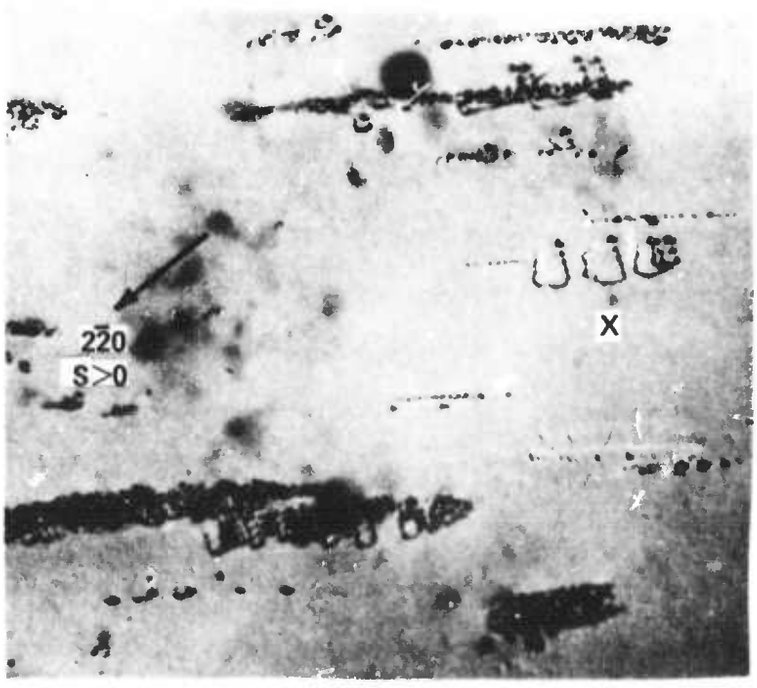
Fig. 14. (g) Kikuchi map giving position of reflections in the diffraction pattern for Burgers vector analysis of dislocation loops.

the mechanism that controls dislocation motion at low and high temperature must be different. Thus plastic flow of silicon at room temperature cannot be described in terms of thermally activated flow. Likewise we expect differences in annealing of damage introduced at room temperature or at elevated temperature.

More insight into the structure of the shear loop is obtained through determining the position of the extra lattice plane characteristic for this defect. The position of the extra lattice plane connected with a shear loop can be determined from its diffraction contrast observed in the electron microscope. Such techniques are described by Hirsch et al.[7], and by Amelincks.[8] We have applied this procedure to determine the nature of the dislocation loop. Such measurements are shown in Figs. 15a, b and 15c, d. According to these results, the displacement of the loop image in a micrograph is clearly seen by comparing the width of two specific loops in the set of micrographs recorded with $g = \pm (2\bar{2}0)$ (Fig. 15a, b) or recorded with $g = \pm (220)$ (Fig. 15c, d). By knowing the Burgers vector from the analysis described above and the loop habit plane obtained from the stereo set given in Fig. 12, the position of the pushed-in extra half plane can be evaluated.

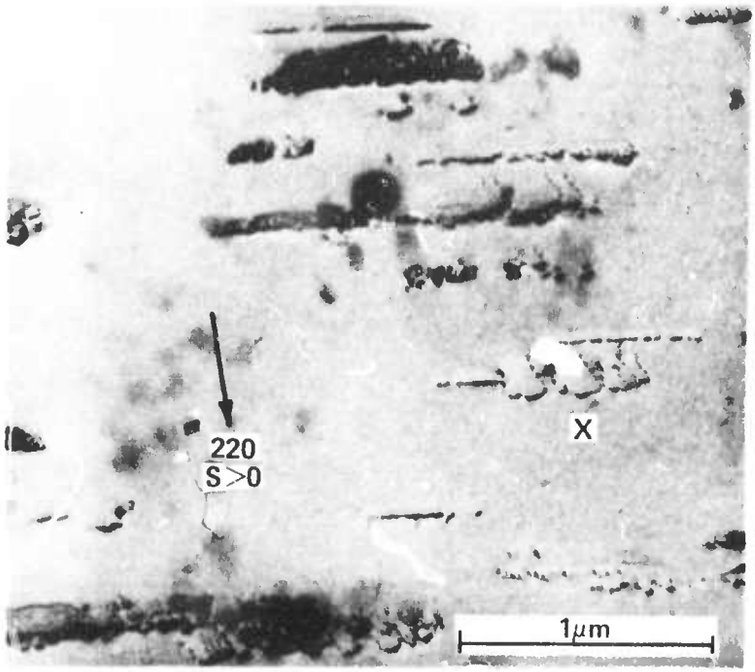


a

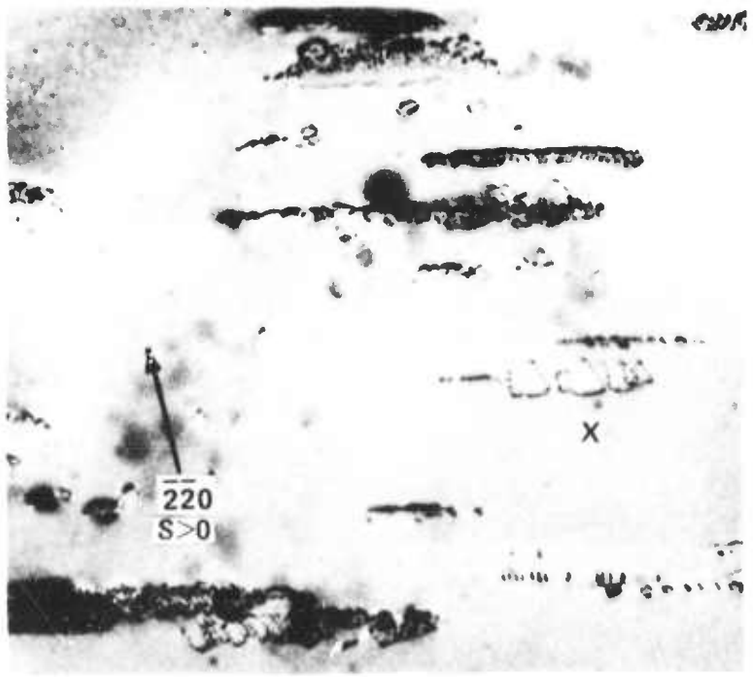


b

Fig. 15. TEM micrographs for determining the nature of dislocation loops. (a) g = $\bar{2}$20, (b) g = 2$\bar{2}$0, excitation error S > 0.



c



d

Fig. 15. TEM micrographs for determining the nature of dislocation loops. (c) g = 220, (d) g = $\bar{2}\bar{2}$ 0.

The analysis indicates that the dislocation loops are due to extra half planes -- pushed in from the surface and positioned at the lowest point of the loop inside the crystal at the position where the two 30 degree dislocation segments meet (Fig. 13). Considering the damage mechanism -- tungsten balls hitting the surface -- this kind of damage, picturing a pushed-in lattice plane, appears plausible and appealing to naive expectation.

3.2 Post Annealing Properties of Grooves

Oxidation of silicon is a fundamental processing step in semiconductor technology. Oxidation of silicon at high temperature is known to generate stacking faults in the surface layer of the wafer. Such faults have a negative influence on device reliability and also on device yield during the fabrication of integrated circuits.

Nucleation and growth of stacking faults on silicon surfaces is not yet understood in detail. The most frequently studied nucleation model is related to sites of mechanical surface damage. It relies on a dislocation reaction first pointed out by Hirsch[9] and assumes that mechanical damage induces prismatic dislocations into the silicon surface. No experimental facts are available

to support this nucleation model. All available experimental evidence is limited due to the complexity of mechanical damage introduced deliberately into silicon surfaces by such techniques as abrasion, sand blasting, scratching, etc.

Detailed damage studies can be made with the help of the ISS technique because the annealing properties of grooves provide further insight into the nucleation of oxidation-induced stacking faults. For groove annealing, standard and short time oxidation cycles at temperatures of 1000°C and 1100°C, respectively, are used. In the following section the annealing experiments are discussed and the nucleation of stacking faults is related to our experimental findings.

3.2.1 Stacking Fault Nucleation Through Prismatic Loops

ISS groove damage is very similar to the abrasive damage normally encountered on wafer surfaces and is described and investigated in detail by Booker and Stickler[2]. The TEM results in Fig. 16 compare abrasive damage produced by abrading a silicon surface unidirectionally with SiO_2 particles of 0.5 µm size in the <110> direction (Fig.16a) with ISS damage (Figs. 16b,c). The difference between these two types

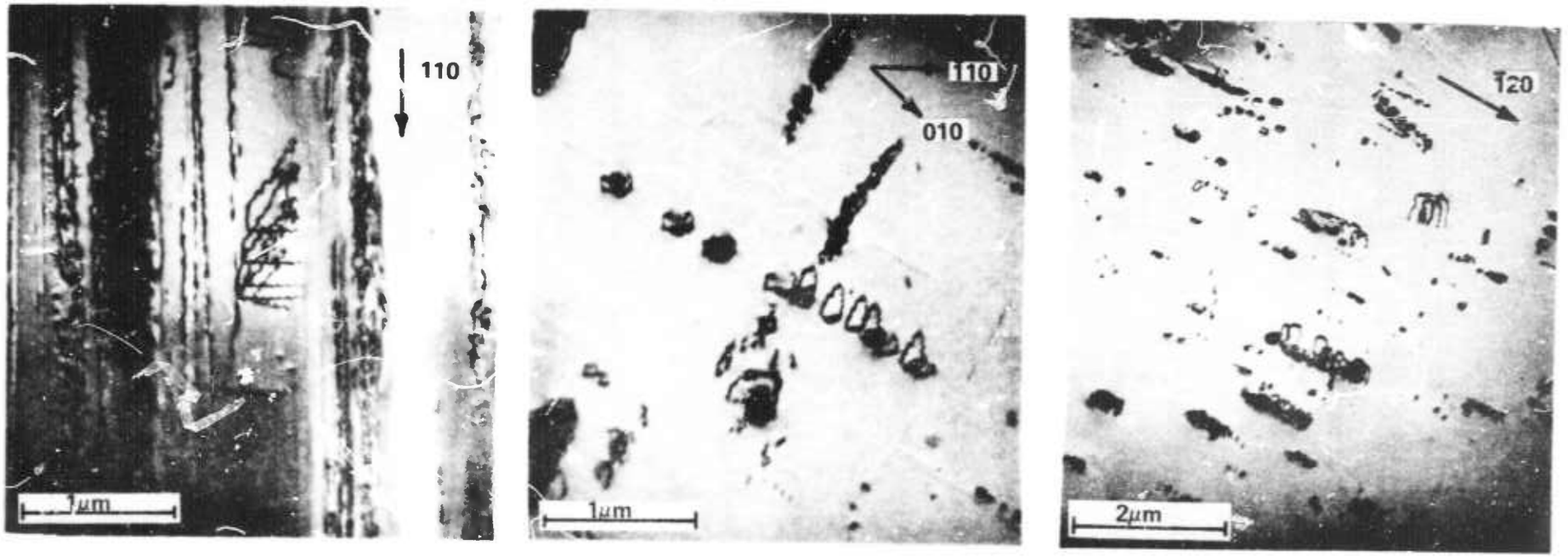


Fig. 16. TEM micrographs of abrasive damage (a) after surface abrasion and (b, c) ISS treatment, showing similarities and differences.

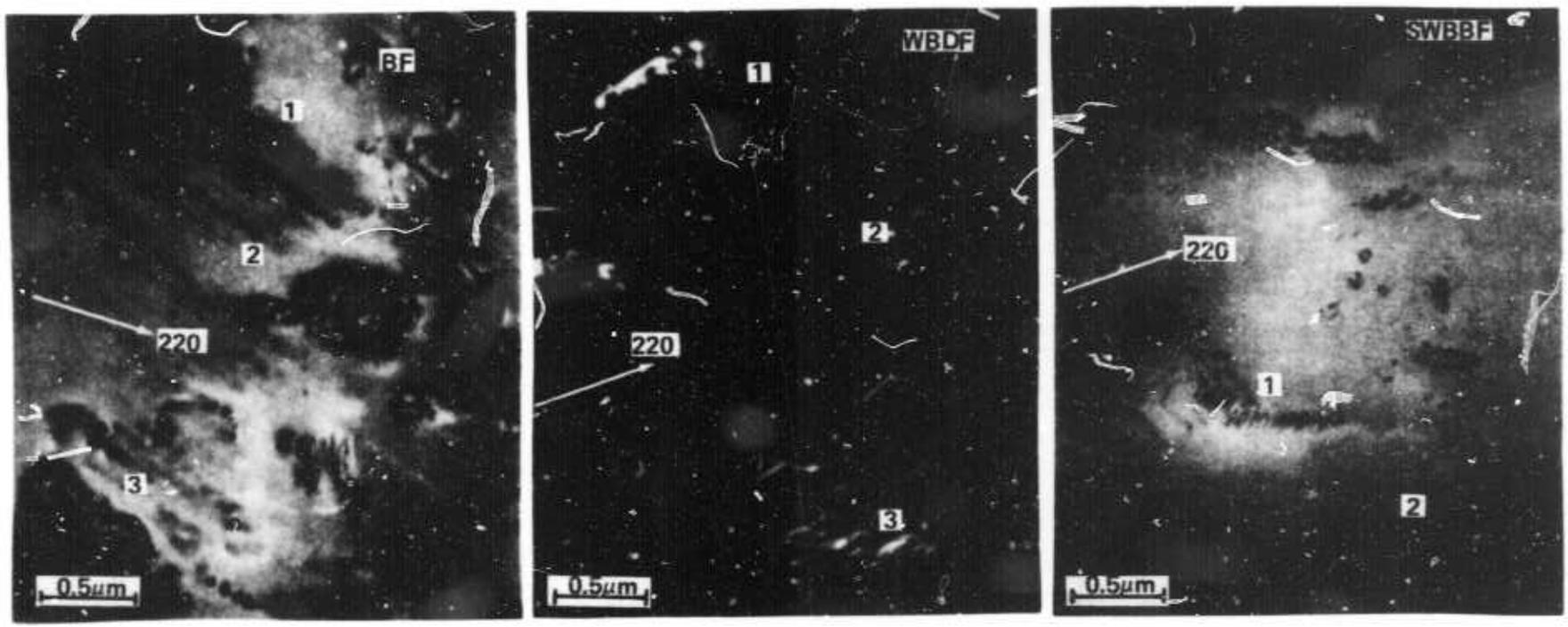
of damage is simply that the polishing damage is more dense and lined up in one direction while the ISS damage clusters can be considerably less dense but appear -- due to the randomness of the ball bouncing -- in several different directions.

Based on such measurements we imply that the ISS loop analysis is also valid for standard abrasive damage. Consequently, we consider the hypothesis describing the generation of stacking faults during high temperature oxidation of mechanically damaged silicon surfaces as not valid. This hypothesis relies on the dislocation reaction: $(a/2)[1\bar{1}0] \longrightarrow (a/3)[1\bar{1}1] + (a/6)[1\bar{1}\bar{2}]$ and indicates that a "prismatic" dislocation loop can dissociate during oxidation into a sessile Frank loop and into a glissile Shockley loop. The crystal area bounded by the Frank partials is the oxidation induced stacking fault. However, our measurements clearly indicate that dislocation loops introduced through abrasive damage are shear loops. A shear loop cannot dissociate as required by the discussed reaction. Consequently, the generally accepted prismatic loop nucleation mechanism for oxidation induced stacking faults cannot explain stacking fault nucleation.

3.2.2 Stacking Fault Nucleation Through Microsplits

Since shear loops cannot account for stacking fault generation during thermal oxidation of ISS'ed (or any other abrasive damaged) silicon surfaces high resolution electron microscopy was employed to study dense dislocation bands for additional details. In the course of this study it was noted that stacking fault generation during oxidation was invariably connected to high density dislocation clusters while low density dislocation clusters always annealed out completely. Using the symmetric weak beam bright field (SWBBF) and the weak beam dark field (WBDF) techniques, TEM micrographs with a magnification of up to 50,000X were recorded. Examples of dense cluste areas resolved by these techniques are given in Figs. 17b,c while the dislocation cluster shown in Fig. 17a was obtained by the usual transmission technique. Accordingly, the clusters marked 1, 2, 3 in Fig. 17a are identified as dense rows of shear loops in the <100> and <110> direction.

An additional result from such investigations is the finding that dislocation pile-ups are present on neighboring slip planes which are separated by only 200Å. (Fig. 18a,b,c,d). This is shown schematically in Fig. 18e. This would mean that such dislocation clusters



a b c

Fig. 17. Dislocation cluster areas taken with high resolution techniques in the TEM. (a) Usual bright field image (BF), (b) weak beam dark field image (WBDF), (c) symmetric weak beam bright field image (SWBBF).

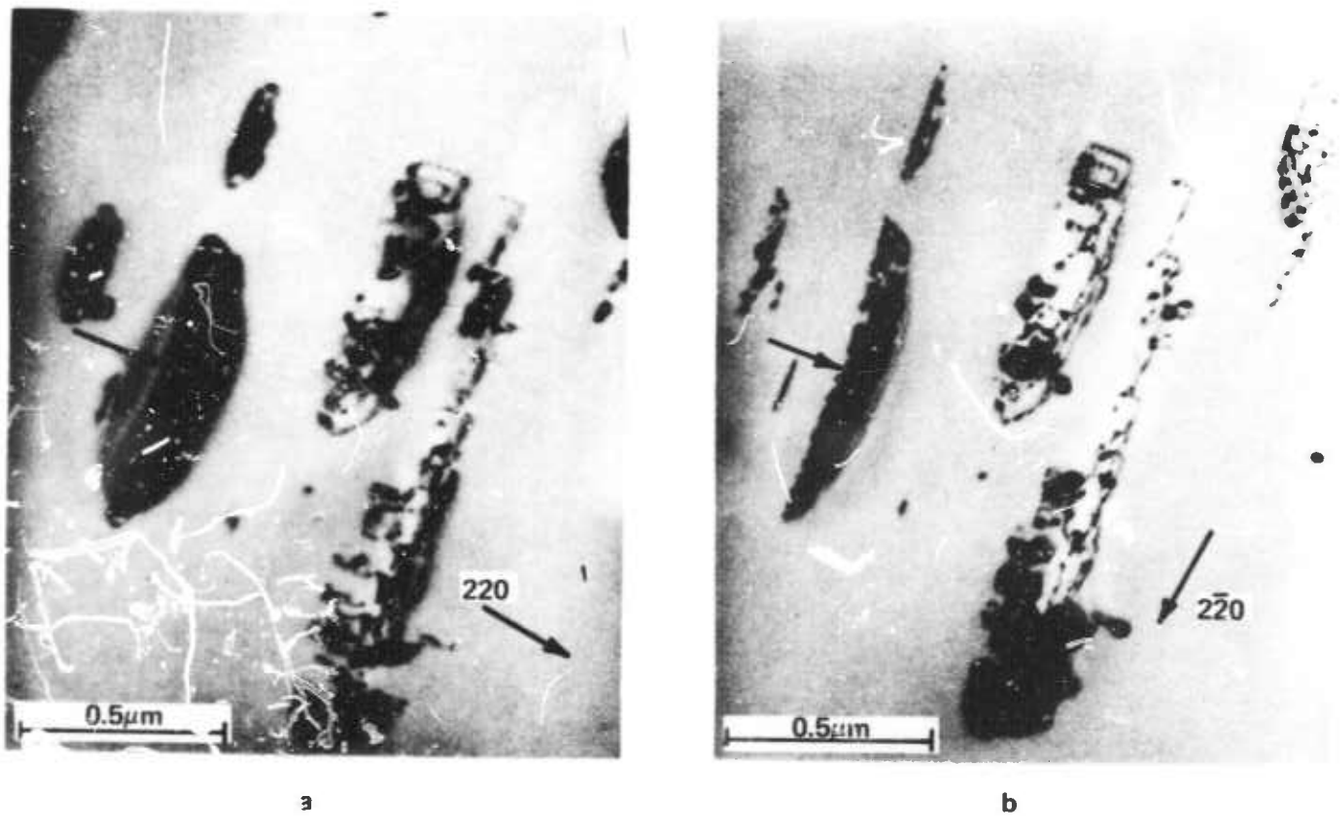
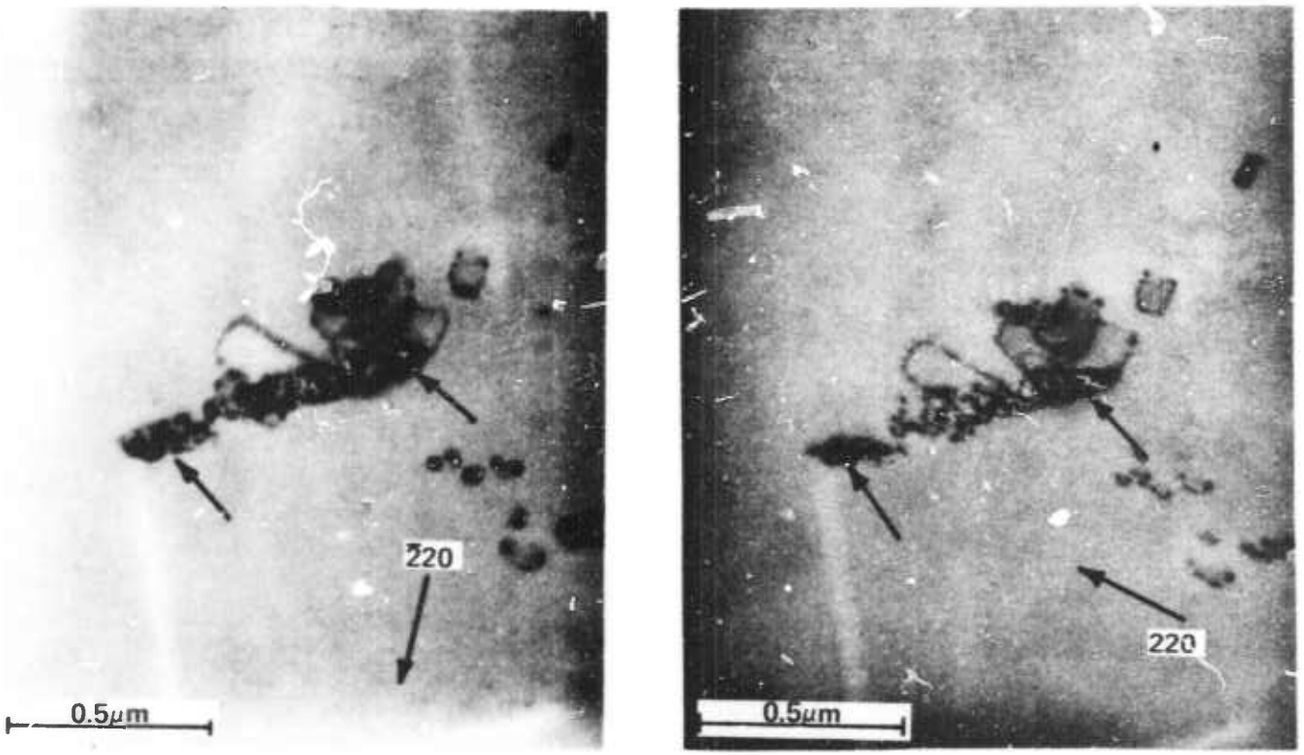


Fig. 18. SWBDF images of dislocation cluster areas where dislocations are piled up to a distance of about 200 Å so that small crack formation is possible. (a) g = 220, (b) g = 2$\bar{2}$0.



c d

Fig. 18. SWBBF image of another dislocation cluster area. (c) g = $\bar{2}20$, (d) g = 220.

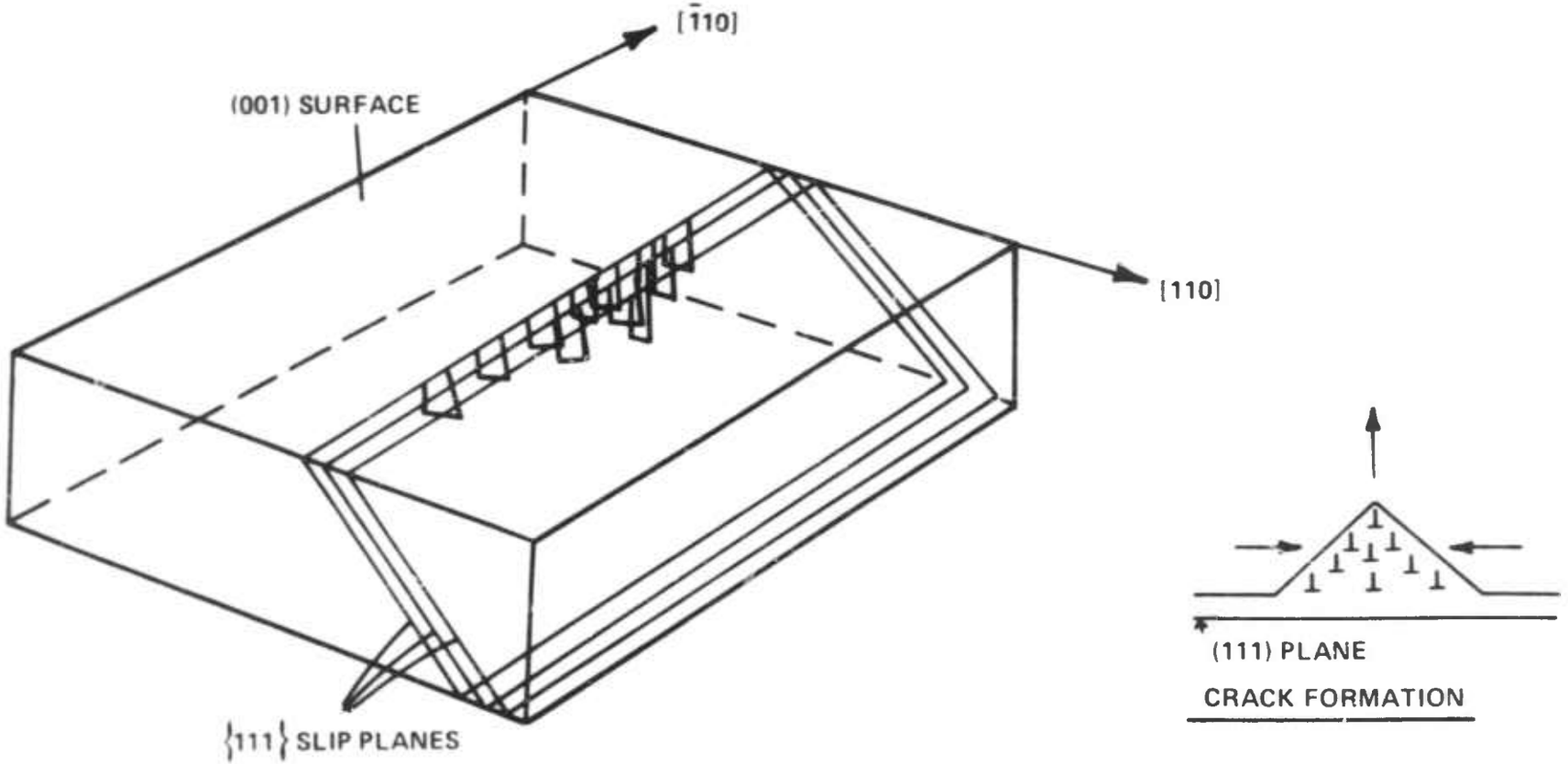


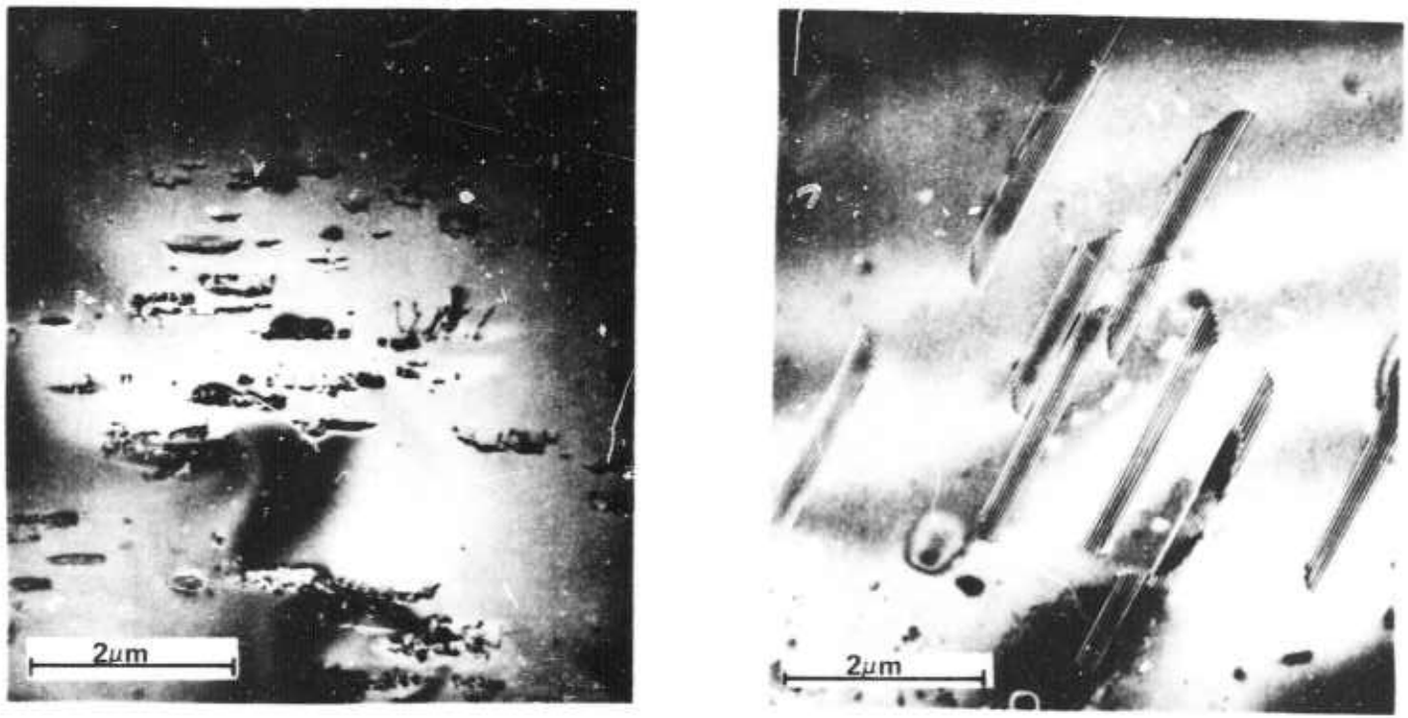
Fig. 18e. Schematic of dislocation pile-up formation.

contain dislocation pile-ups approximately 50 lattice planes apart. The corresponding dislocation density would be $10^{10}/cm^2$ or higher. Based on the work of Fujita[10], Cottrell[11], and specifically of Abrahams and Ekstrom[12] such dense dislocation pile-ups favor micro-crack formation. Consequently, we must assume that abrasive type of damage produces microcracks in silicon and this appears to be reasonable for a material as brittle as silicon at room temperature.

The contention that microsplits in the silicon surface -- caused by dislocation pile-ups -- act as sources for stacking fault generation during oxidation, is supported by experimental evidence. We have observed many examples of small Moire patterns connected with high density dislocation clusters. Such patterns are only 2000Å in size or even smaller. Stacking fault nucleation during oxidation of such cluster is discussed in more detail in the next section of this report.

3.2.3 TEM Observation of Stacking Fault Nucleation

Stacking faults are definitely nucleated at sites of high density damage clusters. This is clearly seen by comparing the TEM micrographs shown in Figs. 19a,b. The defect structure of the sample after ISS is seen



a b

Fig. 19. TEM micrograph of Si wafer surface. (a) Immediately after sound stressing showing dislocation clusters; (b) after sound stressing and standard oxidation showing stacking faults. Density of faults is comparable to number of dense clusters in Fig. 19a.

in Fig. 19a. An oxidation cycle anneals the low density dislocation clusters out of the samples while in the area of high density clusters stacking faults are nucleated* (Fig. 19b). The size of the stacking faults depends on the oxidation time.

To obtain a one-to-one correlation between dislocation clusters and oxidation induced stacking faults we had to rely on the investigation made on "TEM specimens" before and after short time oxidations. Such samples were first completely "mapped" using TEM micrographs to ascertain the defect state after ISS. Subsequently, the samples were oxidized outside the microscope and re-inserted. Using short time dry oxidation steps the thin oxide film on the sample surface did not have to be removed for TEM investigation and thus supplied us with a "replica" of the original defect state (before oxidation) of the sample. The traces of practically all defects present before oxidation are found replicated in the thin oxide film. Examples are shown in Figs. 20 to 22.

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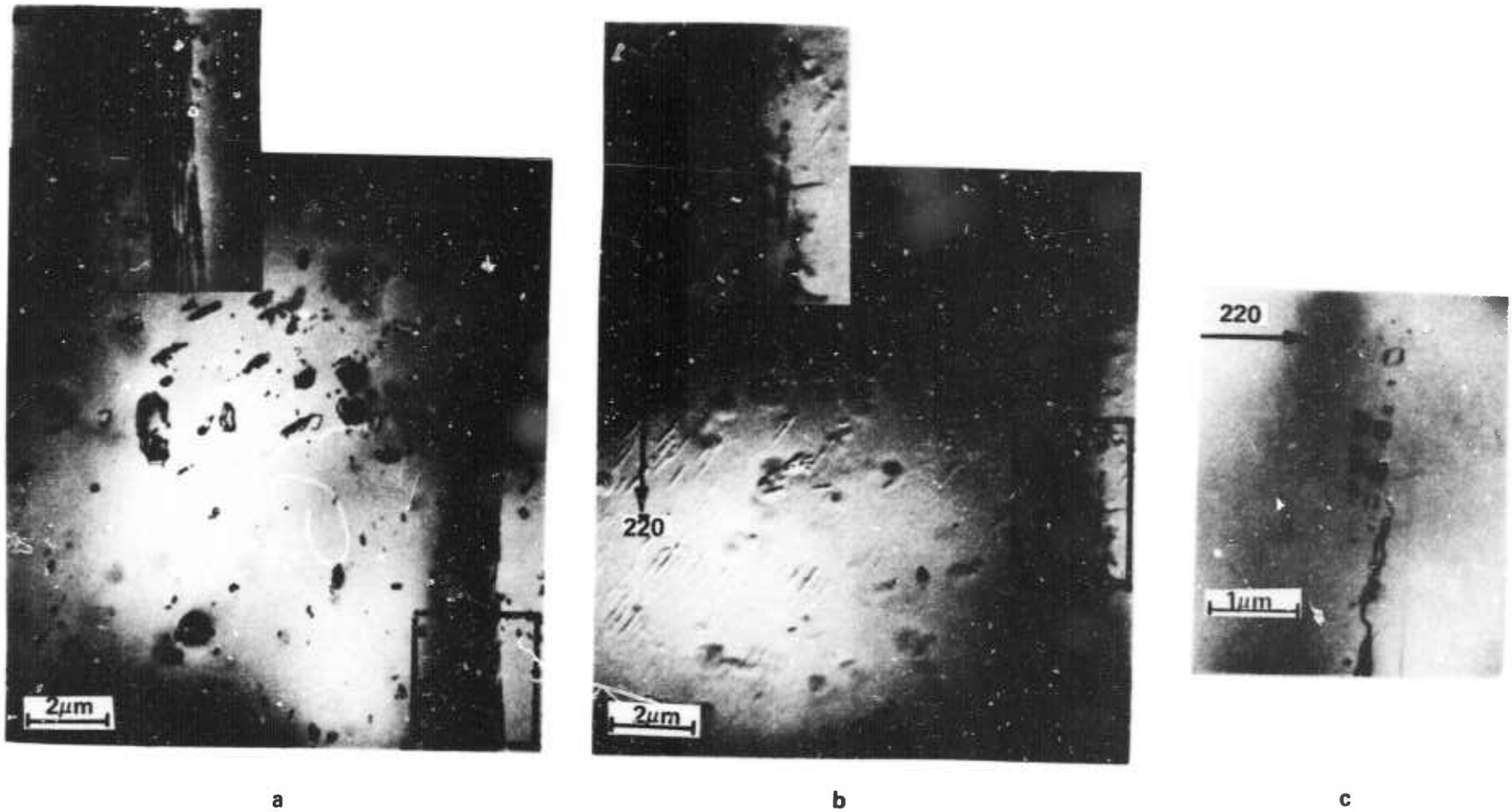
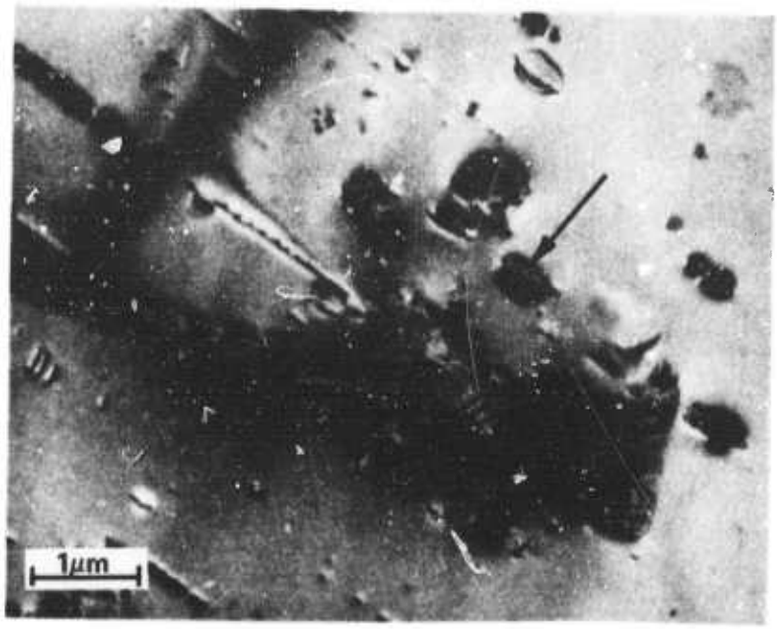
*Sometimes stacking faults can also be found in areas of fracture cones after oxidation. However, the generation of dislocations, as discussed in Section 2.2 of this report, is more characteristic for the larger cones.

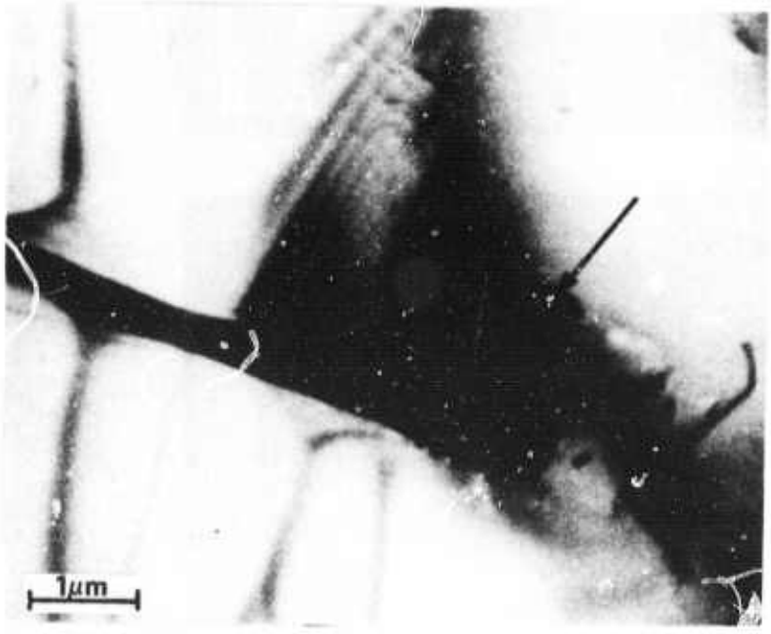


a b c

Fig. 20. TEM micrographs of Si wafer surface. (a) After sound stressing with dislocation loops, clusters and one microcrack; (b) after 10 min dry oxidation with the oxide film still on to show all the traces of the defects in (a); (c) after SiO_2 removal.

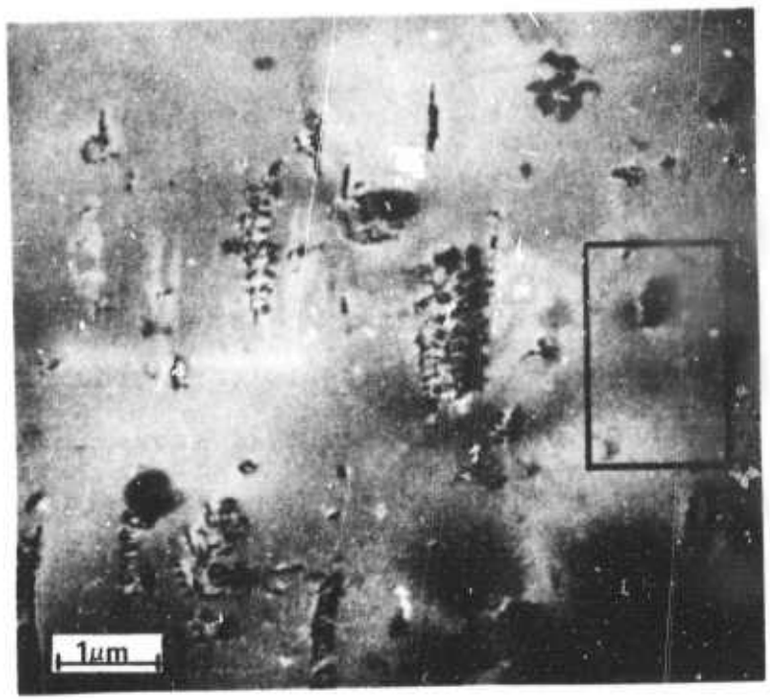


a

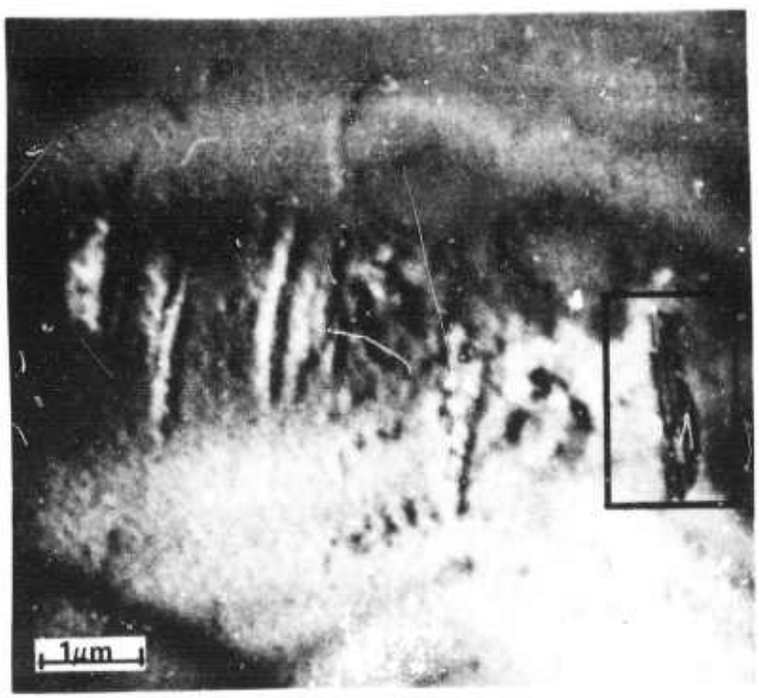


b

Fig. 21. TEM micrographs of Si wafer surface, (a) after sound stressing with dislocation loops, clusters and one microcrack; (b) after 10 min dry oxidation showing a stacking fault generated at a position of a cluster in (a).



a



b

Fig. 22. Another example of one-to-one correlation of (a) cluster after ISS and (b) stacking faults after 10 min oxidation.

In Fig. 20a it can be observed that most of the defects are annealed out even after a short 10 minute oxidation at 1050°C. In the area of the large crack in Fig. 20b, observed are dislocation lines, prismatic loops inside the crystal and stacking faults at the intersection of the crack and specimen surface. Figure 21 shows an example of a crack only partially annealed. A stacking fault is generated at the exact location of a dislocation cluster. A similar observation is made in Fig. 22 for a different sample.

In several samples stacking faults as well as 90°- and 60°- dislocations were generated after 10 minute dry oxidation at 1050°C within the area corresponding to a high density dislocation cluster mixed with small cracks (Fig. 23). No indication is found that such 90°- dislocation dissociate into a stacking fault bounded by Frank and Shockley partials. Such a dislocation reaction is possible according to the equation: $1/2(110) \longrightarrow 1/3(111) + 1/6(11\bar{2})$. However, this reaction was not verified experimentally.

During the annealing study of stacking faults it was noted that stacking faults growing on intersecting {111} planes would annihilate upon meeting. The

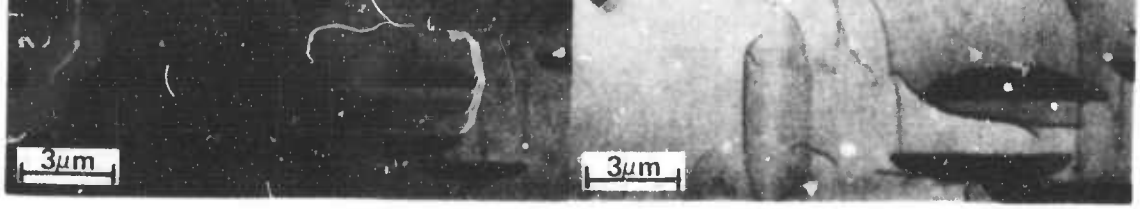
Fig. 23. TEM micrograph showing the simultaneous generation of stacking faults and 90° and 60° dislocation after 10 min dry oxidation at 1050°C of a sound stressed wafer surface.

outcome of such a reaction is a perfect dislocation (90 degree Burgers vector). Such dislocations are indicated in the micrographs presented in Fig. 24. Accordingly the dislocations presented in Fig. 23 are identified as annealing products of intersecting stacking faults.

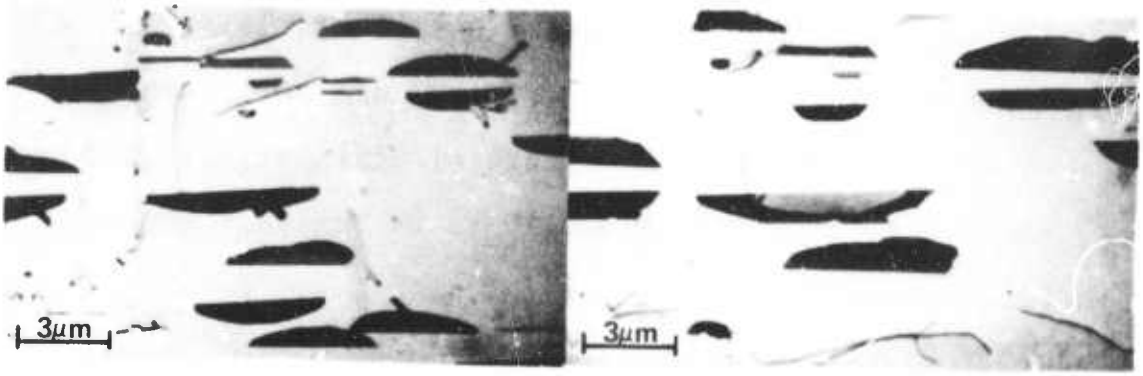
4. TEM Analysis of Oxidation Induced Stacking Faults

The first and only available exact analysis of oxidation induced stacking faults was made by Booker and Tungstall.[13,14] According to these authors oxidation induced stacking faults in silicon are extrinsic and bounded by a Frank partial dislocation.

It is interesting to note that all additional work on oxidation induced stacking faults relies on this analysis and assumes that the results are of general applicability. In view of our results presented in Section 3 of this report we consider it necessary to undertake a complete analysis of stacking faults observed after oxidation of ISS'ed silicon wafers. In addition we find it of general interest to confirm the original results of Booker and Tungstall.[13] Consequently, our analysis follows their procedure exactly. The first part of this section describes the analysis of the bounding partial dislocation.



a b



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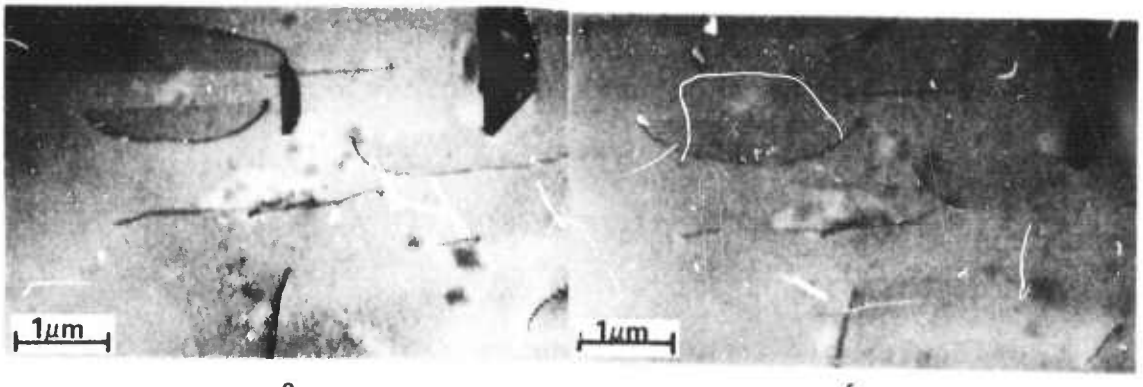


e f

Fig. 24. TEM micrograph of a wafer surface. (a) (c) (e) After ISS and standard oxidation; and (b) (d) (f) after additional 10 min dry oxidation at 1050°C. Most of the stacking faults grow further. Some react and form perfect dislocations.

The extrinsic or intrinsic nature of the oxidation induced stacking faults is determined in the second part of this section.

4.1 Analysis of Partial Dislocation

The bounding dislocation of a stacking fault is a partial dislocation; therefore, the $g.b=0; \pm 1/3$ and the $g.(b \wedge u)$ criterion must be considered jointly for correct interpretation of the contrast features of the dislocation line. Partial dislocations show strong contrast for $g.(b \wedge u)>0$ (u is the unit vector in the direction of the dislocation line) even if $g.b = 0; \pm 1/3$.

Table II summarizes all the reflections taken and the g.b, $g.b_e$ and $1/8\ g.(b \wedge u)$ values for the Frank and the three possible Shockley partials on a $\bar{1}\bar{1}1$ plane (b_e is the edge part of the dislocation).

Figure 25 shows some examples of TEM micrographs of the bounding dislocation of a stacking fault. Considering the values given in Table II and the contrast features shown in the micrographs (see stacking faults 1, 2, and 3 as marked in Fig. 25a), the conclusion is that the bounding dislocation

Table II

Contrast Condition for Partial Dislocations on $(\bar{1}\bar{1}1)$ Planes

g	b	g.b	$g.b_e$	$\frac{1}{8}$ g.(b∧u)		No. of TEM Micrographs
220	$\frac{1}{3}[\bar{1}\bar{1}1]$	$-\frac{4}{3}$	$-\frac{4}{3}$	0	0.118	Fig. 25b
	$\frac{1}{6}[112]$	$\frac{2}{3}$	$0 \rightarrow \frac{2}{3}$	0	-0.118	
	$\frac{1}{6}[\bar{2}1\bar{1}]$	$-\frac{2}{3}$	$0 \rightarrow -\frac{2}{3}$	0	-0.118	
	$\frac{1}{6}[1\bar{2}\bar{1}]$	$-\frac{2}{3}$	$0 \rightarrow -\frac{2}{3}$	0	-0.118	
$\bar{2}20$	$\frac{1}{3}[\bar{1}\bar{1}1]$	0	0	0	+0.2042	Fig. 25a
	$\frac{1}{6}[112]$	0	0		0	
	$\frac{1}{6}[\bar{2}1\bar{1}]$	+1	$0 \rightarrow +1$		0	
	$\frac{1}{6}[1\bar{2}\bar{1}]$	-1	$0 \rightarrow -1$		0	
400	$\frac{1}{3}[\bar{1}\bar{1}1]$	$-\frac{4}{3}$	$-\frac{4}{3}$	0	0.239	
	$\frac{1}{6}[112]$	$\frac{2}{3}$	$0 \rightarrow \frac{2}{3}$	0	-0.118	
	$\frac{1}{6}[\bar{2}1\bar{1}]$	$-\frac{4}{3}$	$0 \rightarrow -\frac{4}{3}$	0	-0.118	
	$\frac{1}{6}[1\bar{2}\bar{1}]$	$\frac{2}{3}$	$0 \rightarrow \frac{2}{3}$	0	-0.118	
040	$\frac{1}{3}[\bar{1}\bar{1}1]$	$-\frac{4}{3}$	$-\frac{4}{3}$	0	0.239	
	$\frac{1}{6}[112]$	$\frac{2}{3}$	$0 \rightarrow \frac{2}{3}$	0	0.118	
	$\frac{1}{6}[\bar{2}1\bar{1}]$	$\frac{2}{3}$	$0 \rightarrow \frac{2}{3}$	0	0.118	
	$\frac{1}{6}[1\bar{2}\bar{1}]$	$-\frac{4}{3}$	$0 \rightarrow -\frac{4}{3}$	0	0.118	
$3\bar{1}1$	$\frac{1}{3}[\bar{1}\bar{1}1]$	$-\frac{1}{3}$	$-\frac{1}{3}$	0	$\pm$0.236	Fig. 25g
	$\frac{1}{6}[112]$	$\frac{2}{3}$	$0 \rightarrow \frac{2}{3}$	0	0.029	
	$\frac{1}{6}[\bar{2}1\bar{1}]$	$-\frac{4}{3}$	$0 \rightarrow -\frac{4}{3}$	0	0.029	

g	b	g.b	$g.b_e$	$\frac{1}{8}$ g.($b \wedge u$)		
	$\frac{1}{6}$ [1$\bar{2}\bar{1}$]	$\frac{2}{3}$	$0 \rightarrow \frac{2}{3}$	0	0.029	
13$\bar{1}$	$\frac{1}{3}$ [$\bar{1}\bar{1}$1]	$-\frac{5}{3}$	$-\frac{5}{3}$	0	$\pm$0.239	
	$\frac{1}{6}$ [112]	$\frac{1}{3}$	$0 \rightarrow \frac{1}{3}$	0	0.147	
	$\frac{1}{6}$ [$\bar{2}$1$\bar{1}$]	$\frac{1}{3}$	$0 \rightarrow \frac{1}{3}$	0	0.147	
	$\frac{1}{6}$ [1$\bar{2}\bar{1}$]	$-\frac{2}{3}$	$0 \rightarrow -\frac{2}{3}$	0	0.147	
31$\bar{1}$	$\frac{1}{3}$ [$\bar{1}\bar{1}$1]	$-\frac{5}{3}$	$-\frac{5}{3}$	0	$\pm$0.239	
	$\frac{1}{6}$ [112]	$\frac{1}{3}$	$0 \rightarrow \frac{1}{3}$	0	0.147	
	$\frac{1}{6}$ [$\bar{2}$1$\bar{1}$]	$-\frac{2}{3}$	$0 \rightarrow -\frac{2}{3}$	0	0.147	
	$\frac{1}{6}$ [1$\bar{2}\bar{1}$]	$-\frac{1}{3}$	$0 \rightarrow -\frac{1}{3}$	0	0.147	
1$\bar{3}\bar{1}$	$\frac{1}{3}$ [$\bar{1}\bar{1}$1]	$\frac{1}{3}$	$\frac{1}{3}$	0	$\pm$0.236	Fig. 25h
	$\frac{1}{6}$ [112]	$-\frac{2}{3}$	$0 \rightarrow -\frac{2}{3}$	0	0.029	
	$\frac{1}{6}$ [$\bar{2}$1$\bar{1}$]	$-\frac{2}{3}$	$0 \rightarrow -\frac{2}{3}$	0	0.029	
	$\frac{1}{6}$ [1$\bar{2}\bar{1}$]	$\frac{4}{3}$	$0 \rightarrow \frac{4}{3}$	0	0.029	
311	$\frac{1}{3}$ [$\bar{1}\bar{1}$1]	-1	-1	0	$\pm$0.239	Fig. 25f
	$\frac{1}{6}$ [112]	1	$0 \rightarrow 1$	0	0.087	
	$\frac{1}{6}$ [$\bar{2}$1$\bar{1}$]	-1	$0 \rightarrow -1$	0	0.087	
	$\frac{1}{6}$ [1$\bar{2}\bar{1}$]	0	0	0	0.087	
3$\bar{1}\bar{1}$	$\frac{1}{3}$ [$\bar{1}\bar{1}$1]	-1	-1	0	$\pm$0.239	Fig. 25d
	$\frac{1}{6}$ [112]	0	0	0	0.087	
	$\frac{1}{6}$ [$\bar{2}$1$\bar{1}$]	-1	$0 \rightarrow -1$	0	0.087	
	$\frac{1}{6}$ [1$\bar{2}\bar{1}$]	1	$0 \rightarrow 1$	0	0.087	
131	$\frac{1}{3}$ [$\bar{1}\bar{1}$1]	-1	-1	0	$\pm$0.239	Fig. 25e
	$\frac{1}{6}$ [112]	1	$0 \rightarrow 1$	0	0.087	
	$\frac{1}{6}$ [$\bar{2}$1$\bar{1}$]	0	0	0	0.087	
	$\frac{1}{6}$ [1$\bar{2}\bar{1}$]	-1	$0 \rightarrow -1$	0	0.087	

g	b	g.b	$g.b_e$	$\frac{1}{8}$ g.(b∧u)		
	$\frac{1}{3}$ [$\bar{1}\bar{1}$1]	- 1	- 1	0	$\pm$0.239	Fig. 25c
$\bar{1}3\bar{1}$	$\frac{1}{6}$ [112]	0	0	0	0.087	
	$\frac{1}{6}$ [$\bar{2}1\bar{1}$]	1	0 → 1	0	0.087	
	$\frac{1}{6}$ [$1\bar{2}\bar{1}$]	- 1	0 → - 1	0	0.087	

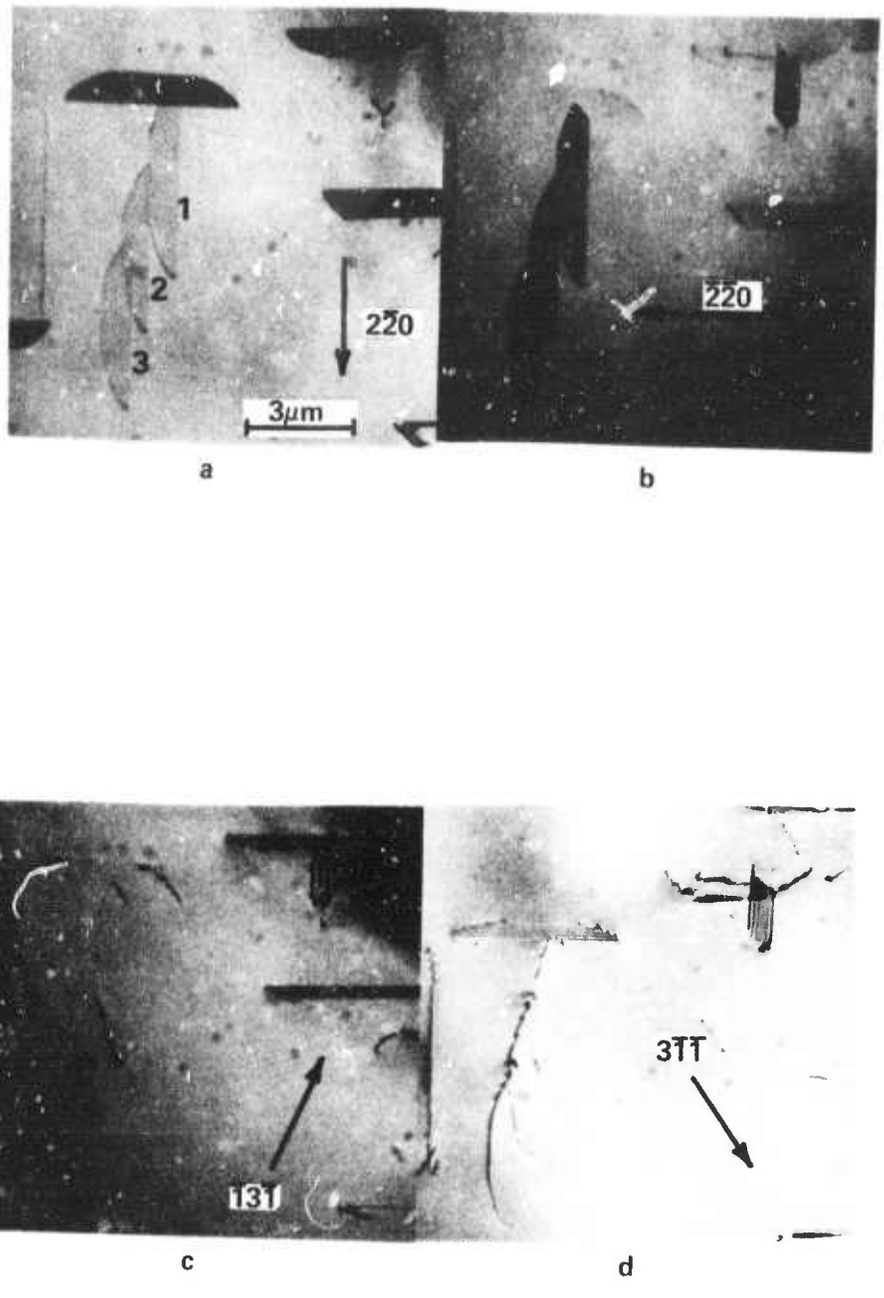


Fig. 25. TEM micrographs of oxidation stacking faults taken with (a) $2\bar{2}0$, (b) $\bar{2}\bar{2}0$, (c) $(\bar{1}3\bar{1})$, (d) $(3\bar{1}\bar{1})$ reflections.

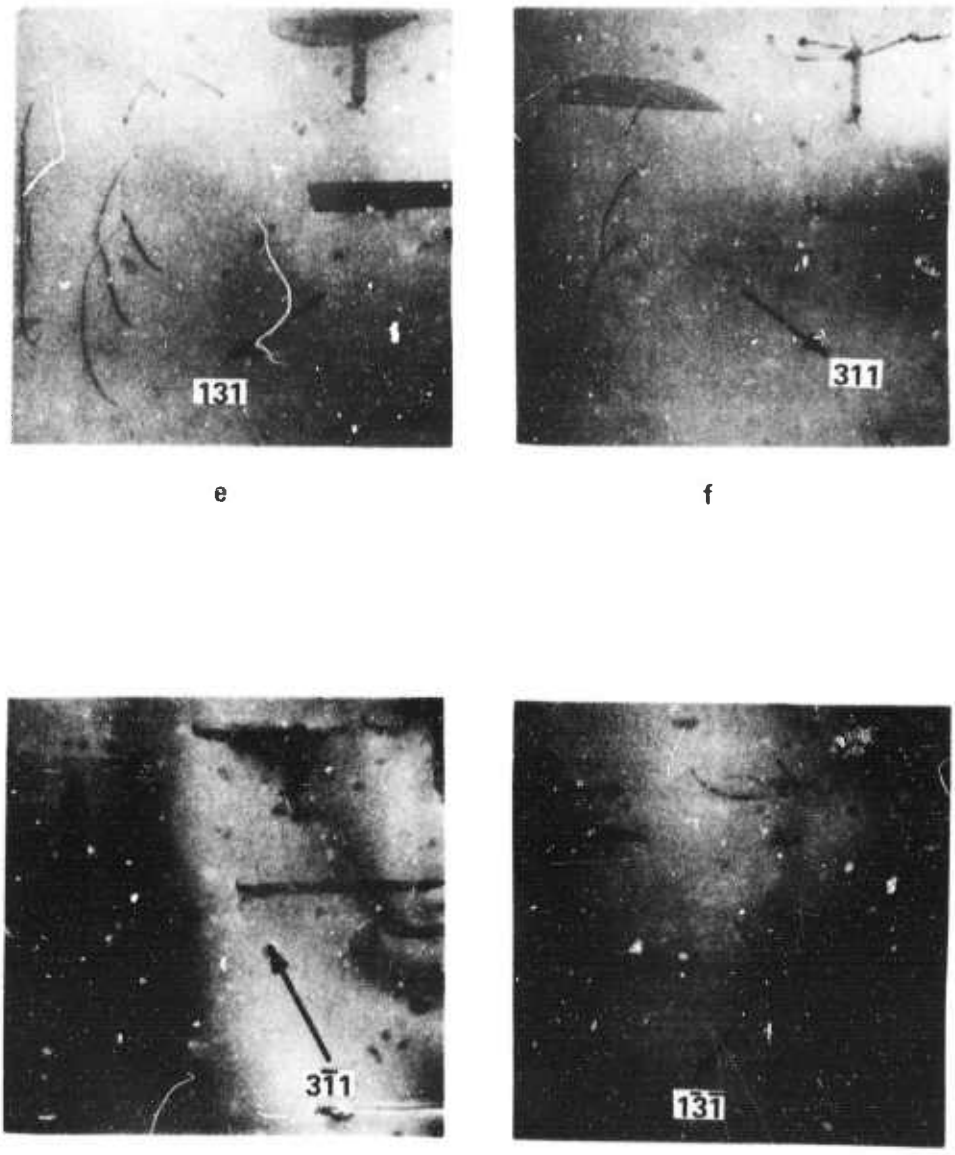


Fig. 25. TEM micrographs of oxidation stacking faults taken with (e) 131, (f) 311, (g) 3$\bar{1}$1, and (h) 1$\bar{3}$1 reflections.

is an a/3 ($\bar{1}\bar{1}1$) Frank partial. Each possible Shockley is excluded by a micrograph taken with one of the (113) reflections, e.g. Burgers vector (B.V.) a/6 [112] is excluded by the ($\bar{1}3\bar{1}$) and ($3\bar{1}\bar{1}$) reflections (Fig. 25c,d); B.V. a/6 [$\bar{2}1\bar{1}$] is excluded by (131) (Fig. 25e); and B.V. a/6 [$1\bar{2}\bar{1}$] is excluded by (311) (Fig. 25f). Since contrast is seen for the dislocation line in all cited reflections the partial dislocation is identified as a Frank partial. In addition for g.b = 0; ±1/3 it can be observed that the line contrast is weak when the g-vector is more or less parallel to the line direction and that the line contrast is strong when the g-vector is perpendicular to it. It follows that for ($\bar{2}20$), ($3\bar{1}\bar{1}$) and ($1\bar{3}\bar{1}$) reflections (Figs. 25e,f) assuming b = a/3 ($\bar{1}\bar{1}1$), the line contrast is weak, if g.($b \wedge u$) is small, because g.b = 0; ±1/3, but that the line contrast is strong when g.($b \wedge u$) reaches larger values. This confirms again that the bounding partial dislocation is of the Frank type.

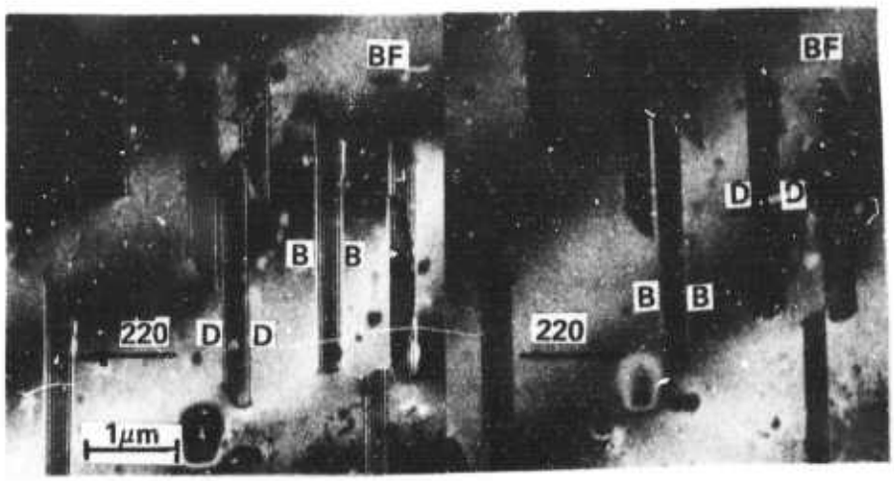
4.2 Analysis of Stacking Fault Nature

Oxidation stacking faults grow from the surface into the bulk. The intersection with the upper surface of the specimen is a straight line while the bounding

dislocation inside the bulk material has a round shape. During the thinning process for the TEM preparation parts of these round dislocations are cut off. However in most cases it is easy to recognize the top of the defect by looking at the partials. The specimen is inserted into the TEM with the non-etched side up. Depending on fault inclination the fault shows, respectively, bright or dark outer fringes (Fig. 26a). The fringe contrast is reversed when the opposite g-vector is used (Fig. 26b). Using well established rules[8,13,14] the nature of the fault can be determined from a bright field image alone (Fig. 26). It follows that this type of stacking faults is extrinsic. Figure 27 shows another set of bright and dark field images of the same faults. Here the change in fringe contrast at the bottom can also be observed and thus each micrograph can be used to determine the extrinsic nature of the faults.[14] It follows, again, that oxidation induced stacking faults are extrinsic.

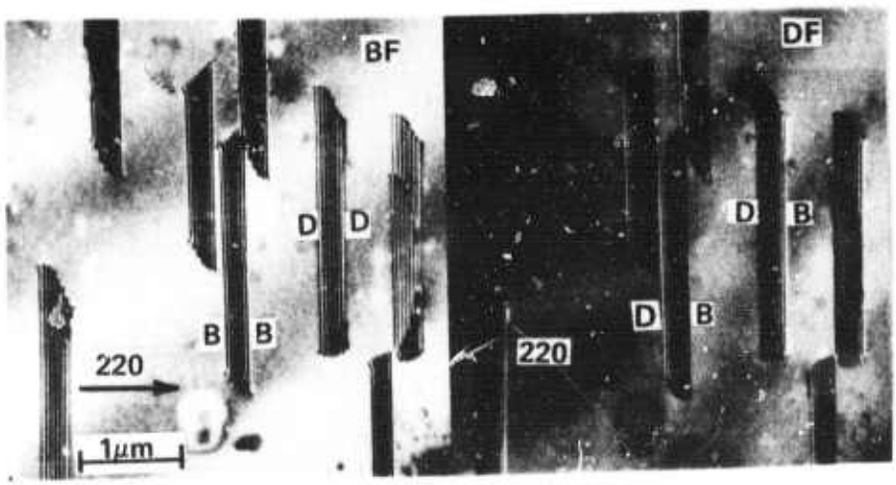
DISCUSSION

The mechanical deformation of covalently bonded crystals at room temperature is not only of scientific interest but also of great practical importance in today's modern semiconductor



a b

Fig. 26. Bright field TEM micrographs of the same stacking faults with opposite operating g-vectors and S = 0 to determine the nature of the fault. (a) g = $\bar{2}\bar{2}0$, (b) g = 220.



a b

Fig. 27. TEM micrographs to show the contrast change of the outer fringes and to determine the nature of the stacking faults. (a) Bright and (b) dark field.

technology. Until recently, this part of solid state physics has received a minimum of attention. Most of the technological efforts were directed into studies of saw damage depth, and into the removal of saw damage through proper polishing techniques. However, serious manufacturing problems encountered in the mass fabrication of such devices as the Picturephone*, charge coupled imaging devices, and other products of low leakage technology, indicated that the defect state in the surface layer of a silicon wafer can significantly influence economical fabrication of such devices.

Detailed studies of deformation mechanism at low temperature in crystals, such as silicon wafers, were primarily hindered in the past by the complexity of the defect state in the crystal encountered after conventional deformation procedures such as grinding, uniaxial stressing, or indentation. Many of the grinding results are summarized by Buck and Meek.[15] Only Stickler and Booker[2] were able to investigate this type of damage successfully in the transmission electron microscope and were also able to show that deformation of silicon at room temperature is connected with the generation of dislocations and cracks in the crystal. Due to the complexity of the damage picture encountered a dislocation analysis could not be performed.

Uniaxial stressing of silicon and germanium at room temperature has not been able to produce evidence of dislocation motion.

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*Trademark

The specimen always broke at too low a stress indicating the presence of flaws in the test crystals which could not be removed through chemical etching techniques. However, such results, indicating the futility of etching in producing defect-free surfaces, were never looked at in proper perspective. Thus the semiconductor industry was not aware that chemical-mechanical etching of silicon surfaces was not capable of producing a defect-free surface (see Chapter 1).

Indentation experiments made at room temperature have shown that plastic flow occurs during the deformation of covalently bonded crystal. Details of plastic deformation during indentation have recently been obtained by Hill and Rowcliffe.[16] Their excellent transmission electron microscopy work of indentations produced in silicon under light load showed that indentation produces dislocations of the shear type. The shear loops introduced through indentation into silicon consist also of 30°- and 60°- dislocations and expand in $\{111\}$ planes.

To explain plastic flow in silicon at room temperature Hill and Rowcliffe introduced the concept of "block slip". Based on their dislocation analysis they also came to the conclusion that thermally activated flow cannot explain plastic flow in silicon at room temperature due to differences in the dislocation structure encountered after low and high temperature deformation.

Block slip provides a possible mechanism to understand plastic flow at room temperature. This mechanism suggests that the theoretical shear strength of the crystal is exceeded locally, thus the lattice effectively collapses, and a crystal "block" slips as a unit. Dislocations are generated simultaneously to accommodate the crystal displacement due to slip of a small lattice block.

ISS is a unique technique to introduce damage into crystals in a precisely controlled way. Thus it becomes not only routine to study the exact nature of damage features in silicon, such as cracks, abrasion and their annealing through transmission electron microscopy but also it becomes possible to ascertain the influence of these damage features on the electrical properties of the silicon surface.

The act of cleaving a covalently bonded crystal requires relative large energies because it must simultaneously create two free surfaces. Consequently, it cannot be produced instantly over a relatively large surface. It must propagate from one point to another as a crack starting from a nucleus. This is a delicate process and very precisely controlled through the application of the ISS technique. Consequently, large amounts of cracks can be generated in the silicon surface without breaking the wafer. Using the Griffith criterion for the crack length "L" (which is approx. 50μm) we estimate the active stress during ISS to be approximately 10^{-3} times the shear modulus μ.

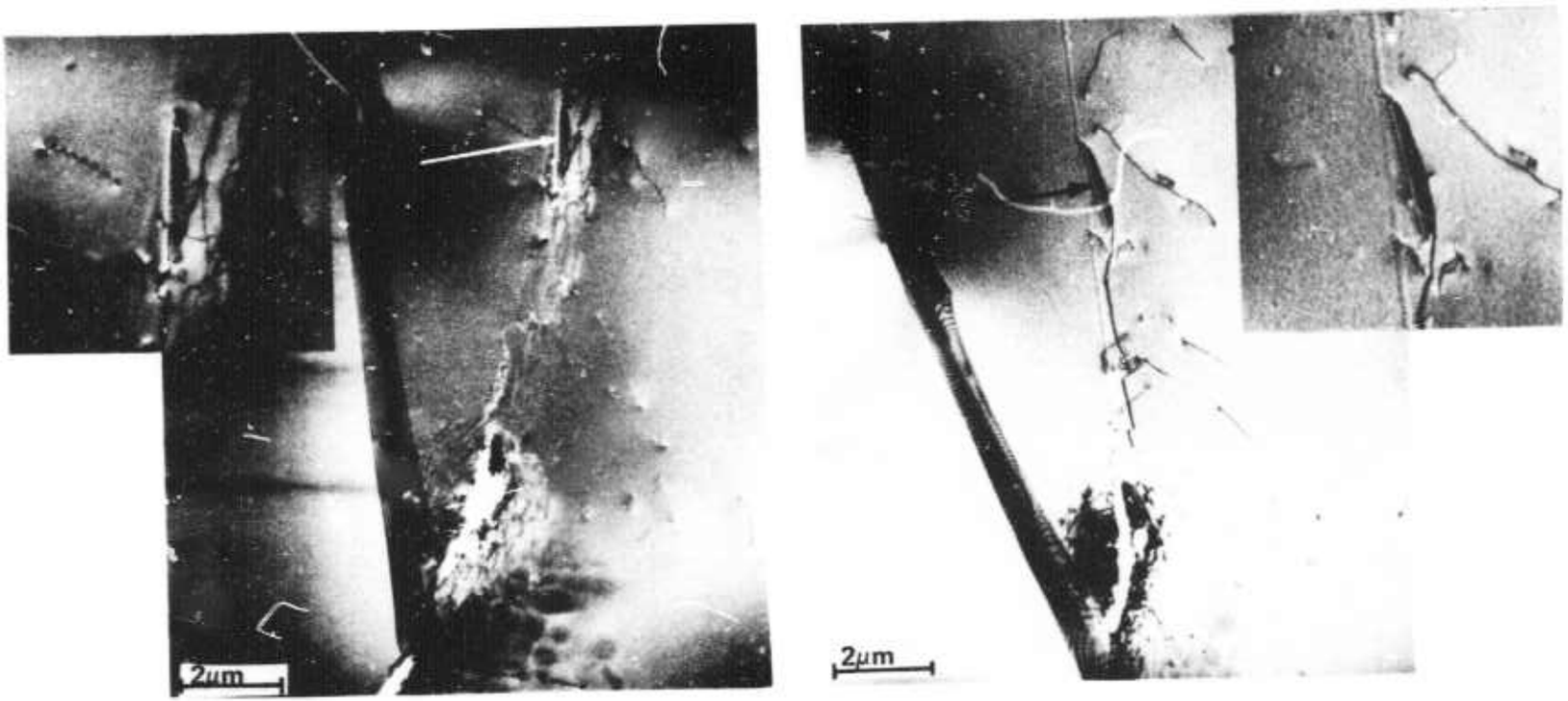
Breakage occurs for stresses around $\mu/10$.

Large numbers of small cracks in the silicon surface make TEM specimen preparation relatively simple and the display of crack tips in the TEM is achieved by controlled surface damage removal. Moire patterns of crack tips obtained in this manner reveal many interesting facts about the crystallographic nature of cracks in silicon. It can be clearly shown that cleavage does not introduce dislocations into the silicon at room temperature. The stresses around the crack tips are not plastically relieved at low temperature. The terminating boundary line of a crack inside the crystal can be observed and it is found that such "edge" dislocations terminating the crack lie on (111) planes and run in <011> or <112> type directions. The cleavage planes for silicon are found to be (111) and (110) type. The cleavage planes are well defined at room temperature. Moire patterns indicate that these cleavage planes are very smooth, particularly, the (111) planes. Cracks in (111) cleavage planes show Moire fringes which are strikingly similar to stacking fault fringes. This indicates that the free surfaces forming the crack are perfect but shifted against each other by a displacement R along the (111) slip plane. This experimental observation provides evidence to the hypothesis of "block slip" as advanced by Hill and Rowcliffe.[16] Assuming this point of view crack formation and abrasion (producing grooves which in turn are due to dislocation pile-ups) are due to a common mechanism which is considerably different from what is generally considered to be

"cleavage" on the one hand and "plastic deformation" on the other. Consequently, it is not surprising to find micro-splits connected with high density dislocation pile-ups.

Further, it also becomes clear that microcracks can be annealed, specifically, if such splits are in the (111) plane. Assuming that block slip governs crack formation it appears plausible to assume that bonding between the silicon atoms in the vicinity of the crack tip is re-established through high temperature relaxations. Thus fairly large crack areas (micron range) can heal and 60° - and 90° - dislocations are the healing product of this process. Submicron cracks cause a much smaller displacement between the split crystal parts and stacking fault nucleation may occur directly through rebonding of the silicon atoms if the displacement "R" of the free crystal surfaces is of the right order of magnitude. This is shown very clearly in the TEM - micrograph of Fig. 28.

This investigation cannot provide "direct" evidence of the stacking fault nucleation process because nucleation occurs at a scale smaller than 2000Å. However, we have obtained a one-to-one correlation between surface areas containing small cracks and/or dislocation pile-ups of a density of $10^{10}/cm^2$ on one side and oxidation stacking faults on the other. Since many smaller dislocation pile-ups were observed to anneal out without leaving any defect behind we assume that the high density dislocation pile-ups contain submicron cracks smaller than 2000Å.



a b

Fig. 28. TEM micrograph of fracture cone showing (a) dislocations after first annealing in oxygen. Note direct correlation between split and stacking fault observed at split site after second oxidation (b). Position of split and stacking fault marked in micrographs.

Likewise our investigations cannot provide experimental proof for the opinion advanced above that stacking faults are nucleated directly and are not the reaction product of dislocations. However our opinion can be supported by energy considerations. The cracks and the stacking fault nucleus we are dealing with are definitely smaller than 2000Å in size. Stability consideration, advanced for perfect and imperfect dislocations, indicates that partial dislocations of this size are more favored as a nucleus.[17] A perfect dislocation would only be a transient in this chain of events. In addition we never observed perfect dislocation (90°) of the required nucleation size (smaller than 2000Å) but many stacking faults of 2000Å or even smaller.

SUMMARY

Impact Sound Stresssing (ISS) of silicon wafers is used to study room temperature deformation of silicon and its annealing through high temperature oxidations. Surface damage produced through ISS of silicon wafers consists of Hertzian fracture cones and abrasion. The fracture cones have a side length of 50μm and penetrate up to 20μm into the silicon. The cracks can be produced with a density of $10^6/cm^2$. The abrasion produces grooves in the silicon surface. The grooves are bunched together in clusters of various densities. A typical cluster area measures 10 to $15\mu m^2$ and the average density of grooves in a cluster is 1 per μm^2. The grooves are approximately 0.2 to 0.4μm deep.

Transmission electron microscopy of Hertzian fracture cones shows that cleavage at room temperature does not introduce dislocations into the silicon. The crystal area surrounding the crack including the crack tip is free of dislocations. Stresses around crack tips are not relaxed at room temperature. The terminating boundary lines of cracks in (001) silicon surfaces are located on (111) planes and run in <011> and <112> type directions. The cleavage plane for (001) silicon is (111) and (110) type. Moire patterns of cracks indicate that these cleavage planes are well developed. Cracks in (111) cleavage planes show Moire fringes which are strikingly similar to stacking fault fringes. This indicates that some cracks in silicon produce simple lattice displacements along (111) slip planes.

Transmission electron microscopy of grooves shows that grooves are connected with dislocation bands. The bands consist entirely of pile-ups of shear loops. The shear loops lie on {111} planes. The dislocation loops are composed of 60°- and 30°- dislocation segments with Burgers vector $[01\bar{1}]$ in the (111) loop plane. Dislocation bands of various densities are produced. Maximum densities observed are estimated to be as large as $10^{10}/cm^2$. Large dislocation pile-ups are connnected with microsplits. Such splits are 2000Å in size, or smaller.

High Temperature oxidation partially anneals the damage out of the crystal. Fracture cone annealing produces a dislocation network of 60° - and 90° - dislocations in the vicinity of the crack tips. Low density dislocation bands anneal completely out of the crystal while high density bands produce stacking faults as an annealing product. The stacking faults are extrinsic, bounded by a Frank partial with (a/3) (111) Burgers vector and are nucleated by submicron splits present in high density dislocation pile-ups before annealing.

Damage propagation through the crystal towards the undamaged wafer surface before and after annealing does not occur. As a byproduct of this investigation it is found that ISS can be used advantageously to improve generation lifetime of minority carriers on the undamaged wafer surface.

ACKNOWLEDGMENT

Technical assistance for this investigation was provided for by H. Ilker, Electron Microscopy; H. Stellefson, Sample Preparation; Andre Oster, Impact Sound Stressing; Chris Schneider, Electrical Characterization.

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Unclassified

Security Classification

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY *(Corporate author)*
International Business Machines Corporation
System Products Division, East Fishkill
Hopewell Junction, N.Y. 12533

2a. REPORT SECURITY CLASSIFICATION
Unclassified

2b. GROUP

3. REPORT TITLE
DAMAGE PROFILES IN SILICON
AND THEIR IMPACT ON DEVICE RELIABILITY

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*
Scientific 1 July 1975 to 31 December 1975

5. AUTHOR(S) *(First name, middle initial, last name)*
G. H. Schwuttke

6. REPORT DATE
15 January 1976

7a. TOTAL NO. OF PAGES
125

7b. NO. OF REFS
32

8a. CONTRACT OR GRANT NO.
DAHC 15-72-C-0274

b. PROJECT, TASK, WORK UNIT NOS.

c. DOD ELEMENT

d. DOD SUBELEMENT

9a. ORIGINATOR'S REPORT NUMBER(S)
TR 22.1989

9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*

10. DISTRIBUTION STATEMENT

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

11. SUPPLEMENTARY NOTES

12. SPONSORING MILITARY ACTIVITY
Advanced Research Projects Agency

13. ABSTRACT

Impact Sound Stressing of silicon wafers is utilized to measure the effectiveness of various polishing techniques used to prepare silicon surfaces free of damage. Modern chemical-mechanical polishing techniques, such as silicon dioxide and cupric ion polishing are more successful in damage removal than chemical polishing techniques which use mixtures of nitric, hydrofluoric and acetic acids. All polishing techniques are more or less limited in regenerating minority carrier lifetime in mechanically damaged silicon surfaces through surface repolish.

Defect profiles in Impact Sound Stressed silicon wafers are determined. Transmission electron microscopy analysis of Hertzian fracture cones and abrasive damage introduced through ISS into (001) silicon surfaces is performed. The analysis is made before and after high temperature oxidation. Dislocation patterns are analyzed before and after oxidation annealing. It is shown that crack stresses in silicon are not relaxed at room temperature. Crack annealing generates 60° -- and 90° -- dislocations in the vicinity of the crack-tip. Abrasion damage is shown to be connected with pile-ups of shear loops. The shear loops lie on (111) planes and are composed of 60° -- and 30° -- dislocation segments with [110] type Burgers vector in the loop plane. Abrasion produces dislocation bands of various densities. Maximum dislocation densities observed are estimated to be as high as $10^{10}/cm^2$. Such large dislocation pile-ups are shown to be connected with microsplits. The splits are 2000Å in size, or even smaller. Annealing of dislocation bands produces stacking faults in areas of high density dislocation clusters. The stacking faults are identified as annealing products of microsplits. Finally, it is shown that damage propagation does not occur through the wafer towards the non-stressed surface before or after annealing.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Silicon Impact Sound Stressing Polishing Technique Transmission Electron Microscopy Defect Analysis						