R76-921337-19

SPUTTERED THIN FILM RESEARCH

See 1473

Final Technical Report

Summary of Work Performed:

15 April 1972 through 31 January 1976

FEBRUARY 1976

PREPARED UNDER CONTRACT N00014-72-C-0415

Sponsored By

Advanced Research Projects Agency
ARPA Order No. 2173, Amendment No. 5
Monitored By Office of Naval Research

UNITED TECHNOLOGIES RESEARCH CENTER
EAST HARTFORD, CONNECTICUT 06108

76-02-218-1

UNITED TECHNOLOGIES CORPORATION
RESEARCH CENTER
East Hartford, Connecticut

R76-921337-19

Final Technical Report Under Contract N00014-72-C-0415
Summary of Work Performed for the Period
15 April 1972 to 31 January 1976

ARPA Order No.:	2173, Amendment No. #5/7-1-75
Program Cost Code:	000006D10K21
Contractor:	United Technologies Research Center
Effective Date of Contract:	15 April 1972
Contract Expiration Date:	31 January 1976
Amount of Contract:	$522,055.00
Contract Number:	N00014-72-C-0415
Contract Management:	Dr. Anthony J. DeMaria (203) 565-3545
Principal Investigator:	Dr. Alexander J. Shuskus (203) 565-6498
Scientific Officer:	Dr. Van Nicolai
Short Title:	Sputtered Thin Film Optics
Report By:	A. J. Shuskus

Sponsored by Advanced Research Projects Agency
ARPA Order No. 2173, Amendment No. 5/7-1-75

Report No. R76-921337-19

Sputtered Thin Film Research

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Cont'd)

Report R76-921337-19

Sputtered Thin Film Research

ABSTRACT

This report discusses the results of an investigation regarding the potential of the high dielectric constant materials $SrTiO_3$, WO_3 and HfO_2 as alternate gate insulators for radiation hardened insulated gate field effect transistors. The insulators were deposited by rf sputtering. Capacitor structures fabricated with $SrTiO_3$ and WO_3 films did not show adequate stability under bias and temperature stress to be useful gate dielectrics. Reactively sputtered hafnium dioxide MIS capacitors exhibited far more stable characteristics with bias and temperature stress, although slow trapping effects were observed at high bias voltages. Hafnium dioxide MIS capacitors irradiated with Co(60) gamma rays to a dose of 10^7 rads showed a high degree of radiation tolerance. Based on these encouraging results, n-channel and p-channel transistors with hafnium dioxide gate insulators were fabricated. The devices exhibit excellent transistor characteristics. For a gate insulator thickness of 1,000 Å, and bias voltages of $\pm$ 6V, threshold voltage shifts in most instances did not exceed |1.5V| for a dose of 10^7 rads. The sense of the radiation induced threshold voltage shifts observed was not always consistent, although the same process conditions were used to fabricate devices. Further effort is required to achieve a high degree of process reproducibility and control or elimination of the slow trapping effect.

The work described in this report is the last phase of a multiyear program on sputtered thin film research. A compilation of the research activities which preceeded this work covering the period 15 April 1972 to 30 September 1974 is contained in Report Number N921337-15.

1.0 INTRODUCTION

A great deal of effort has been expended on the problem of improving the radiation tolerance of MIS devices exposed to ionizing radiation. Much of the effort has focused on the modification or optimization of thermally grown silicon dioxide. Several approaches investigated have included the substitution of chromium for aluminum as the gate metallization (Ref. 1), diffusion of chromium into silicon dioxide (Ref. 2, 3), implantation of the silicon dioxide gate insulator with aluminum (Ref. 4) and optimization of the MOS fabrication process (Ref. 5).

Generally, the above approaches with the exception of aluminum implantation have led to a decrease in radiation sensitivity under negative gate biases but increases in device sensitivity to ionizing radiation under positive gate biases. In contrast, aluminum implantation led to improved radiation tolerance under positive gate biases but increased the radiation sensitivity under negative gate biases. With the increased utilization of complementary MOS circuitry, a radiation hardening approach is required which will be compatible with both n- and p-channel devices.

A limited number of alternate insulators have been investigated with regard to radiation hardened MIS devices. They include silicon nitride (Ref. 6, 7), silicon oxynitride (Ref. 8, 9) and aluminum oxide (Ref. 10, 11, 12). Although a significant degree of hardness has been achieved with these materials, other problems have been introduced in the process. In many cases a field dependent instability is observed. In other cases, a large amount of oxide charge makes the technique unacceptable. For example, Schmidt, et al (Ref. 8, 9) developed silicon oxynitride films which exhibited an extreme degree of hardness under both polarities of bias but an unacceptably high flat band voltage of -10V. Modifications in the process to produce low threshold voltage silicon oxynitride devices resulted in a marked degradation of hardness and charge injection at low bias voltages (Ref. 9). Zaininger and Waxman (Ref. 10) reported that aluminum oxide formed by anodization showed excellent radiation insensitivity under both negative and positive bias. Schlesier and Norris (Ref. 12) fabricated aluminum oxide gate dielectric CMOS circuits which showed excellent radiation resistance up to radiation dose of 2×10^7 rads. The radiation resistance of the aluminum oxide gate insulator is attributed in part to charge injection. The major drawback of the aluminum oxide gate dielectric stems from charge injection at high electric field. This results in an undesired threshold voltage shift of the device. At elevated temperatures charge injection takes place at even lower bias voltages. This raises questions to the suitability of aluminum oxide gate dielectrics at elevated temperatures.

The radiation hardness of a gate insulator depends on a number of factors; such as, the density and distribution of electron and hole traps, electron-hole recombination rates, and charge injection. These factors, in turn, are dependent on the

choice of material and processing. There is no theoretical basis on which one may predict the behavior of a given insulator subjected to an impressed electric field and ionizing radiation. Radiation hardening of MIS devices has been based primarily on empirical studies.

The objective of the research reported herein was to investigate the suitability of several high dielectric constant insulators for use as gate dielectrics for radiation tolerant MIS devices. High dielectric constant insulators potentially offer two significant advantages over devices using silicon dioxide gate insulators. For an equivalent device geometry higher IGFET transconductances can be achieved. In addition, the high dielectric constant is more effective in shielding the silicon surface from the effects of trapped charge generated by exposure to ionizing radiation. This would result in a reduction of threshold voltage shift for an equivalent density of trapped charges. The three materials which were chosen for this investigation were strontium titanate, tungsten trioxide and hafnium dioxide. The dielectric constant of bulk strontium titanate (Ref. 13) is about 300 and a dielectric constant in excess of 1000 has been reported for tungsten trioxide (Ref. 14). Hafnium dioxide (Ref. 15) is known to have a dielectric constant of 25.

The research program spanned twelve months and consisted of two phases. Phase I involved the fabrication of MIS capacitors with WO_3, $SrTiO_3$ and HfO_2; their electrical characterization; and, finally, assessment of their radiation tolerance to Co 60 γ-irradiation. This screening period lasted nine (9) months. At the completion of the first phase, the results indicated that HfO_2 offered the most promise for radiation tolerant devices among the insulators evaluated. In the final phase, lasting three months, the program consisted of the tasks of fabricating transistors and a simple inverter circuit for additional data on the suitability of HfO_2 as a radiation tolerant gate dielectric

2.0 EXPERIMENTAL PROCEDURE

2.1 Sputtering System

The dielectric films were deposited by reactive rf sputtering of the appropriate target material in an oxygen ambient. The sputtering chamber was constructed of stainless steel. Sputtering pressure was measured by Varian Millitorr ion gauges. Two magnet coils which have been welded into stainless steel cases are mounted internal to the chamber to provide an axial field between the target and substrate. The magnets enhance as well as confine the rf plasma. Adjustment of field strength influences substrate heating and uniformity of the deposition. The chamber is evacuated by a Welsh 3103 turbomolecular pump which is capable of pumping 250 L/sec in the millitorr range. Use of the turbomolecular pump in place of a conventional oil diffusion pump eliminates the "backstreaming" of hydrocarbons which would result in contamination of the film during the sputtering process.

The substrate holder was constructed of stainless steel and contained an internal heater which provided the capability of achieving a deposition temperature up to 700 °C. Sample substrates were held in place by means of a ring clamp. The substrate heater assembly was designed to provide the capability for sputter etching of the sample prior to film deposition.

The sputtering targets were five inch diameter discs. The hafnium dioxide and tungsten trioxide were formed by reactive sputtering of the appropriate metal target in an oxygen ambient. The metal targets were analyzed to be 99.9 percent pure. Strontium oxide films were deposited using a sintered strontium oxide target (99.9 percent). A reactive oxygen ambient was required for the deposition of stoichiometric $SrTiO_3$ films. Ultrahigh purity oxygen (99.99 percent) was used as the sputtering gas. The target to substrate separation was maintained at 2.5 cm.

2.2 Silicon Substrates

The silicon used in this work was in the form of 1.25 inch diameter wafers prepared by the Czochralski methods. Both p- and n- type substrates of (100) orientation were used The resistivity ranged between 5-10Ω-cm for C-V studies and 0.01Ω-cm material was used for dielectric and optical evaluation of the films deposited. Prior to film deposition the wafers were degreased, boiled in nitric acid, rinsed in high resitivity deionized water, etched in hydrofluric acid, rinsed again in dionized water and blown dry in a dry nitrogen gas stream.

In the cases where $Si-SiO_2$-insulator structures were desired for study, the silicon dioxide growth was carried out at 900 °C in dry oxygen in a horizontal resistively heated furnace. The silicon dioxide was then annealed at the same temperature in nitrogen for 30 minutes.

2.3 Procedure for Film Deposition

At the outset of a run, the system was pumped down to 10^{-7} Torr. If the substrate was to be sputter cleaned, oxygen gas was introduced into the system to a pressure of 85 mTorr. With the shutters closed, sputter cleaning of the target was started at an rf power density of 1.5 W/cm^2. Sputter cleaning of the target was usually performed for an hour. Simultaneously the substrate was brought up to the desired deposition temperature. With the sample at the desired temperature, a 1 kV dc discharge was initiated for sputter etching of the substrate and continued for 1 to 5 minutes. At the end of the substrate sputter etching operation, the dc discharge was terminated, the system pumped down to the desired operating pressure (this operation takes approximately 30 sec.), the shutters were opened and film deposition was commenced. If no sputter etching of the substrate was required, the system was pumped down to 10^{-7} Torr, oxygen was introduced up to the desired pressure, the target was sputter cleaned, simultaneously the sample was brought to the desired deposition temperature and at the end of the sputter cleaning, the shutters were opened and film deposition was initiated.

After film deposition, heat treatments in nitrogen, hydrogen and oxygen were investigated.

2.4 Measurements

The electrical evaluations were performed on MIS structures. These were prepared by evaporating either 10 or 15 mil diameter aluminum or gold dots. Aluminum was evaporated on the bare backside of the silicon for contact.

Interface properties were studied by MIS capacitance techniques. The high frequency capacitance-voltage measurements were made at 1 MHz. Low frequency C-V characteristics were obtained using the quasi-static technique described by Kuhn (Ref. 16). Stability of the charge distribution was measured by applying positive and negative bias voltages across the MIS capacitors for varying periods of time while the sample was maintained in a nitrogen atmosphere at a temperature of 200 °C.

Film thickness and refractive index values were determined by using a Gaertner ellipsometer at a wavelength of 546 nm. The Taylor-Hobson Talysurf was used on thick specimens for thickness measurements.

The radiation sensitivity of the insulators was determined by irradiating MIS capacitors under positive and negative gate bias with CO (60) gamma rays. The radiation effects up to a total accumulated dose of 10^7 rads were investigated. The cobalt 60 source used in these studies was located at the University of Connecticut. The dose rate of the gamma source was 10^5 rads/hr.

3.0 FABRICATION AND EVALUATION OF MIS CAPACITORS

A wide range of deposition parameters and annealing treatments were investigated in an attempt to find the conditions which would provide MIS structures exhibiting the best characteristics with regard to, surface state density, flat-band voltage, and stability under voltage bias and temperature stress. Substrate deposition temperatures were varied between 100 °C and 600 °C. Oxygen sputtering pressure was varied from 1 to 5 x 10^{-2} Torr. Films were annealed in ambients of H_2, N_2 and O_2.

3.1 Strontium Titanate MIS Capacitors

Although strontium titanate films were sputtered from a ceramic target of the compound, sputtering in a pure argon atmosphere resulted in the deposition of oxygen deficient, highly conducting films. Sputtering in a reactive ambient of oxygen was required to produce stoichiometric films. The dielectric constant of the films was a strong function of the substrate deposition temperature and varied from 40 for films deposited at 100 °C to a dielectric constant of 200 for films deposited at 500 °C. A similar variation for rf sputtered $SrTiO_3$ films has been reported by Pennebaker (Ref. 17) and is correlated to crystallite size of the film. Films deposited at low temperatures are fine grained and the grain size increases with substrate deposition temperature. Sputtering pressure exhibited little effect on the dielectric constant. The loss tangent of the films measured at 100 kHz ranged between 0.01 to 0.02.

The index of refraction of the films was determined from measurements by ellipsometry. Films with a dielectric constant of 40 had an index of 2.1 and ranged up to a refractive index value of 2.3 for films with a dielectric constant of 200.

The requirement of a reactive oxygen ambient for the sputtering of strontium titanate films resulted in considerable difficulty in our attempts to deposit strontium titanate films on "bare" silicon. In order to achieve the condition of an oxide free silicon surface, the silicon substrate was sputter etched and deposition of strontium titanate followed immediately. In many cases, this did not lead to MIS capacitors with stable capacitance-voltage characteristics. Generally, the hysteresis was of the order of several volts with 2000 Å $SrTiO_3$ films for bias excursions of ±10V. The sense of flatband voltage shift was positive for positive biases and negative for negative bias. The threshold voltage for onset of charge transfer varied between 4 to 6 volts. This is indicative of the formation of a thin silicon oxide layer between the silicon and $SrTiO_3$ film which permits the tunneling of charge into traps in the $SrTiO_3$ film. The combination of a high dielectric constant film with a low dielectric constant film leads to the build up of very high fields across low dielectric constant material at normal gate bias

voltages and hence would result in the type of instability observed. The exact behavior was observed in an earlier variable threshold IGFET memory transistor study (Ref. 18) with $SrTiO_3$ films intentionally deposited on 20 Å layers of thermal SiO_2. In some cases devices were fabricated which did not exhibit the above instability but instead showed a weak polarization at room temperature of the order of a half a volt for bias voltage excursions of ±8V. The shift was positive for negative bias and negative for positive bias. High frequency C-V characteristics for n-type and p-type capacitors of such devices are illustrated in Fig. 1. The film deposition in both cases was done at a substrate temperature of 300 °C, a power density of 1.6 W/cm^2 and an oxygen pressure of 1.5×10^{-2} Torr. The samples were annealed in oxygen at 750 °C for one half hour. Unannealed samples showed a positive fixed surface charge density of the order of $10^{13}/cm^2$ and a smearing of the C-V characteristics which is indicative of a high surface state density.

The relationship between the flatband voltage V_{FB} of the experimental curve and the fixed surface charge density N_{fc} is given by the expression

$$V_{FB} = -\frac{N_{fc}\, qd}{\epsilon\epsilon_o} + \phi_{MS}$$

where ϕ_{MS} is the metal semiconductor work function difference, q is the electron charge, d is the thickness of the insulator, ϵ_o is the permittivity of free space, and ϵ is the dielectric constant of the insulator. The interfacial charge is found to be positive and the values of N_{fc} vary between $1\text{-}3 \times 10^{12}/cm^2$.

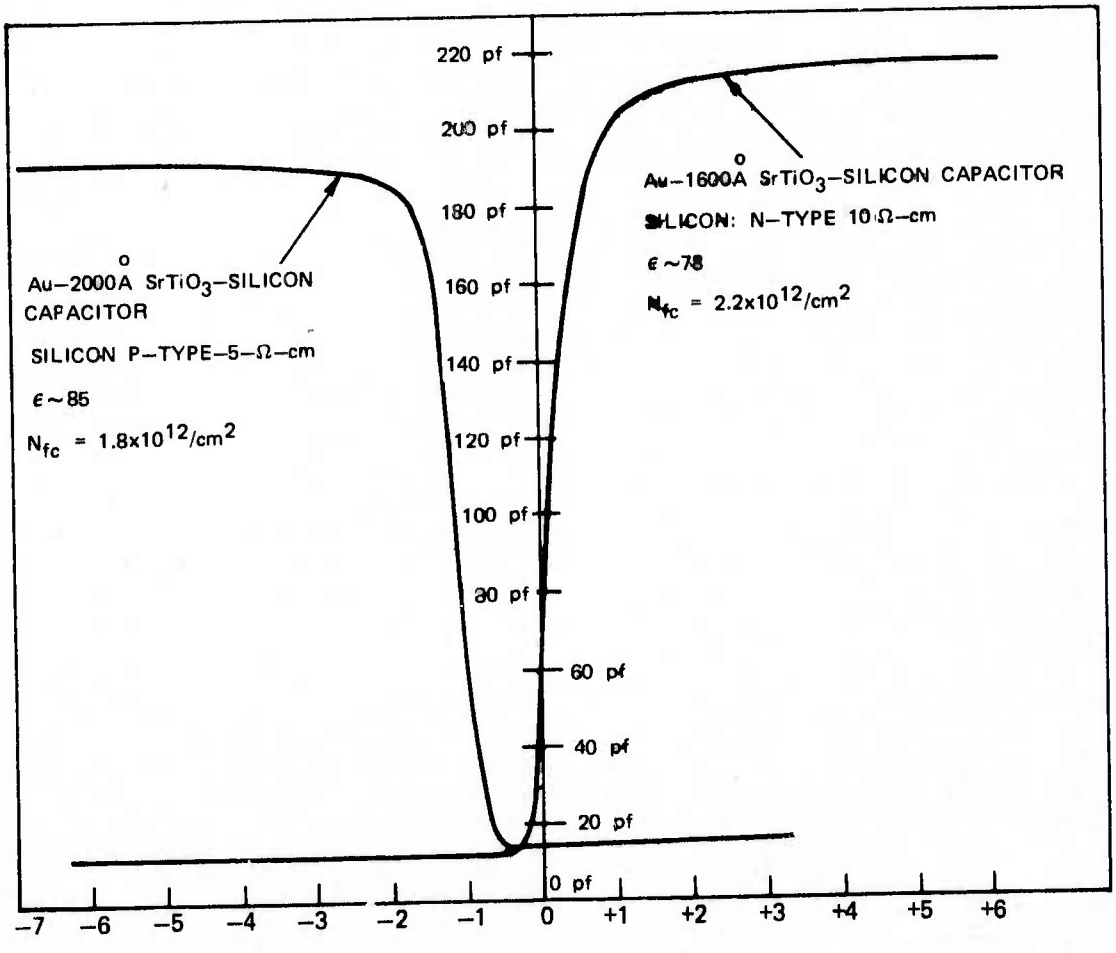
Introduction of a thermal silicon dioxide layer of approximately 100 Å stabilized the C-V characteristics to bias stressing at room temperature for voltages up to ±10V. Bias stressing of the thermal SiO_2-$SrTiO_3$ at 200 °C at ±10V for 15 minutes resulted in a marked hysteresis in the C-V characteristics. Positive bias resulted in negative flat band voltage shifts of 3 volts where as negative fias resulted in positive shifts of 2 volts. This polarization is due to the marked differences in the conductivity of $SrTiO_3$ and SiO_2. Similar effects have been observed with SiO_2-Si_3N_4 and SiO_2-Al_2O_3 capacitors employing SiO_2 films of the order of 100 Å in thickness.

In spite of the problems encountered with the fabrication of strontium titanate capacitors, units which exhibited relatively stable C-V characteristics for bias excursions of ±8V were examined for their radiation tolerance when exposed to ionizing radiation. The results obtained for several process variations are shown in Figs. 2 through 4.

A comparison of the results shows that the $SrTiO_3$ film (Fig. 2) with a dielectric constant of 200 deposited on "bare" silicon shows the higher degree of radiation tolerance for a Co 60 γ-ray doses of 10^7 rads and bias voltages of ±6V. The maximum flat band voltage shift is approximately 1/2 volt to more negative values.

FIG. 1

C-V CHARACTERISTICS OF N AND P-TYPE Au-$SrTiO_3$-Si CAPACITORS



76-02-108-6

FIG. 2

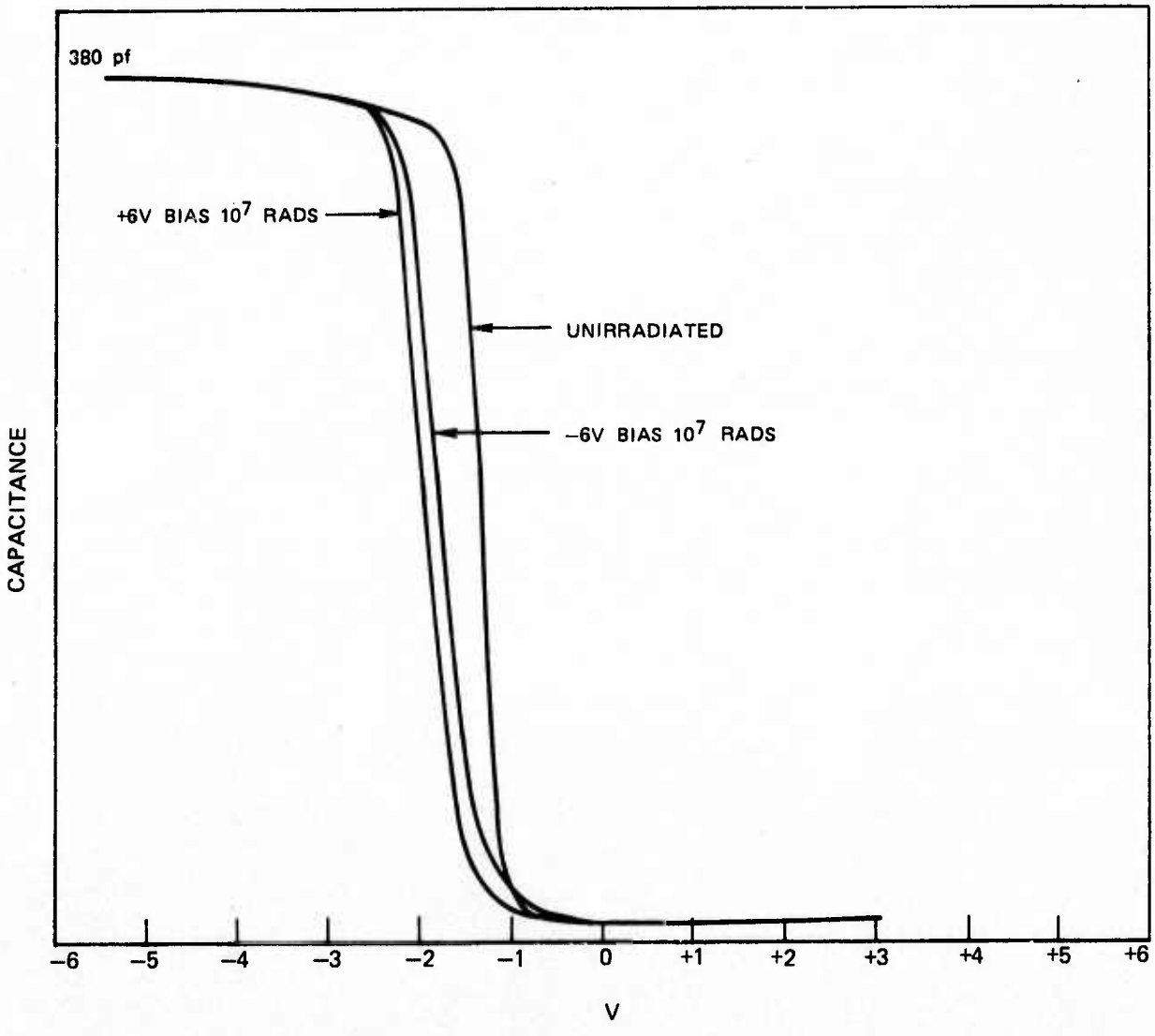
C–V CHARACTERISTICS OF γ–IRRADIATED Au–$SrTiO_3$–Si CAPACITOR

Au–$SrTiO_3$–SiO_2 CAPACITOR

Au DOT: 10 mil DIAMETER: Si: 6Ω–cm P–TYPE:

2400 Å $SrTiO_3$

$\epsilon \sim 200$



76–02–108–5

This film was deposited at 500 °C, oxygen pressure of 1.5×10^{-2} Torr, and an rf power density of 1.5 W/cm^2. The combination of a 100 Å SiO_2 film with a strontium titanate film with $\epsilon \sim 200$ leads to significant degradation in radiation hardness (See Fig. 4). A marked increase in surface state density under positive bias also occurs.

Figure 3 shows the radiation response for a $SrTiO_3$ film with a dielectric constant of 80 deposited on "bare" silicon. The radiation tolerance is significantly less than the film with a dielectric constant of 200. The flat band voltage shifts are not in the ratio of the dielectric constants. A possible explanation is an increased trap density for holes in the finer grained lower dielectric constant films.

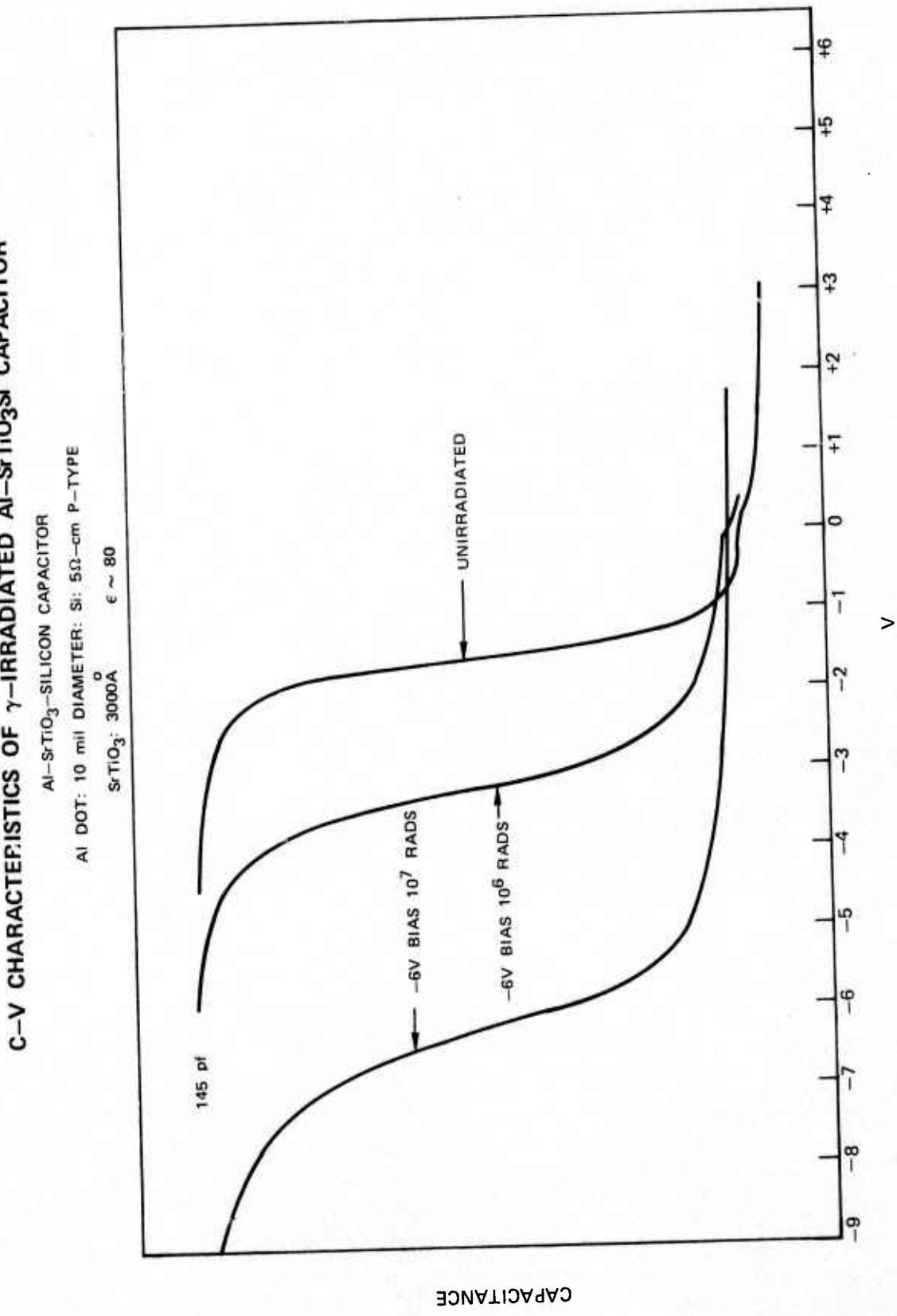
3.2 Tungsten Trioxide MIS Capacitors

Films of tungsten trioxide were deposited on sputter etched "bare" silicon at a substrate temperature of 400 °C, an oxygen pressure of 2×10^{-2} Torr, and a power density of 1.5 W/cm^2. After an anneal in oxygen at 750° for one half hour, the shift in flatband voltage tends to stabilize out. The index of refraction of these films was determined to be 2.3. The dielectric constant of the films measured at 1 MHz typically ranged between 120 to 160. The dielectric constant had a marked dependence on frequency. For example, ϵ = 120 @ 1 MHz, 162 @ 100 kHz and 182 @ 10 kHz. The loss tangent @100 kHz was 0.177 and 0.87 at 10 kHz. At low values of electric fields, the film resistivity was of the order of 10^9 Ω-cm.

Measurement of the C-V characteristics at room temperature of a 3000 Å thick film showed a small hysteresis of less than a 1/2 volt when the bias voltage was limited to ±10V. A positive (negative) bias on gate resulted in a small shift to more negative (positive) flatband voltages. At 200 °C, the films became highly conducting, but, when cooled to room temperature, the films exhibited the initial resistivity and C-V characteristics. The leakage current of the WO_3 films was significantly greater than the displacement current and prevented the measurement of the low frequency C-V characteristics by the quasi-static techniques.

The fixed surface charge density N_{fc} typically is of the order of -1×10^{12}/cm^2. Figure 5 shows the radiation response for an Al-WO_3-Si capacitor subjected to 10^7 rads of cobalt 60 radiation. The flat band voltage shift is limited to a half volt in the direction of a more negative value. Irradiation at zero bias produces virtually no flatband shift. Figure 6 shows the radiation response for a composite MIS capacitor consisting of 3000 Å of tungsten trioxide deposited on 100 Å of SiO_2. At a γ-ray dose of 10^6 rads, a significant degradation in the radiation tolerance occurs under positive bias. A dose of 10^7 rads under positive bias degrades the C-V characteristics to the point where it was barely distinguishable.

FIG. 3



76-02-108-4

FIG. 4

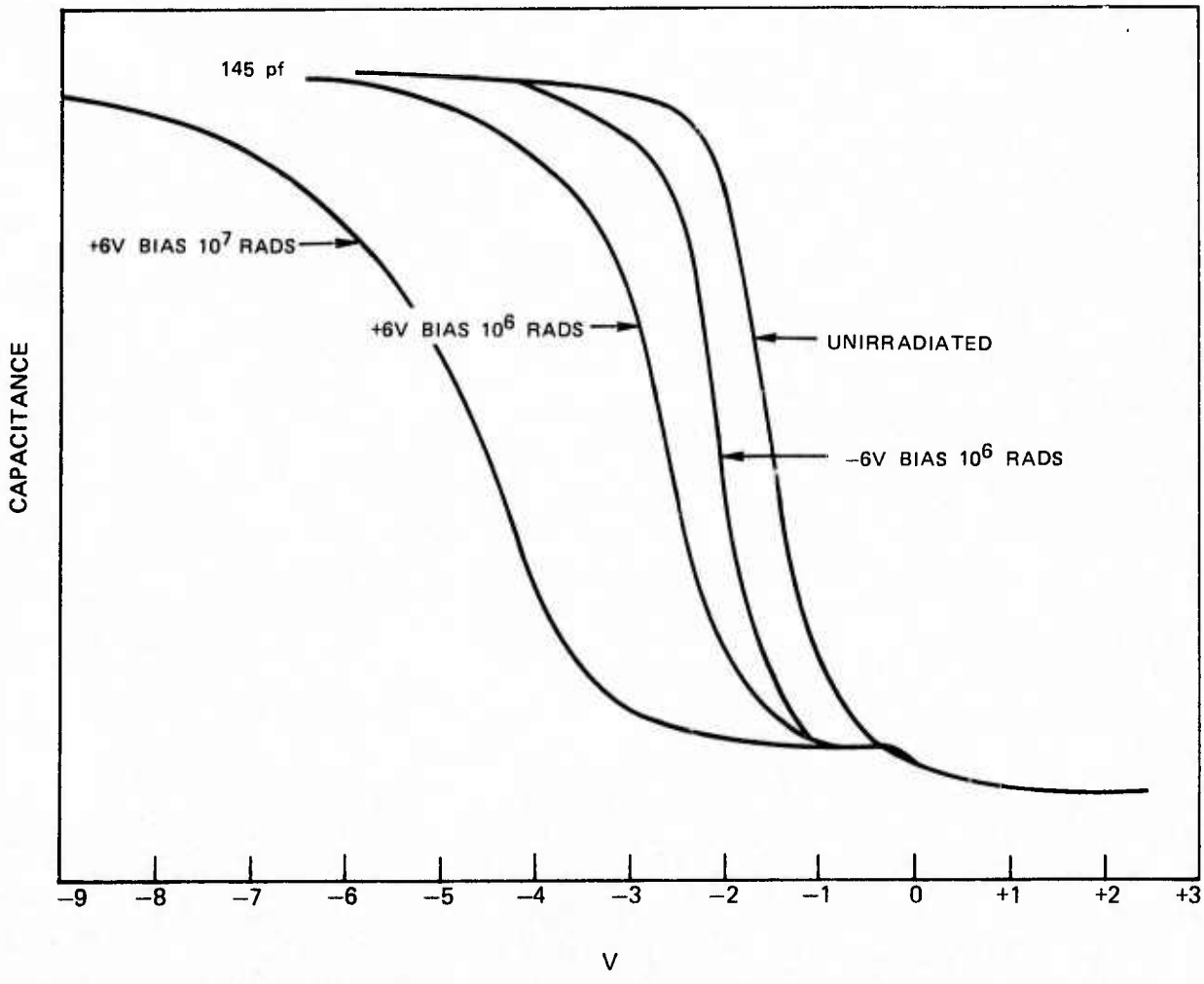
C–V CHARACTERISTICS OF γ–IRRADIATED Au–$SrTiO_3$–SiO_2–Si CAPACITOR

Au–$SrTiO_3$–SiO_2–SILICON CAPACITOR

Au DOT: 10 mil DIAMETER: Si: 5 Ω cm P–TYPE

100Å SiO_2; 2400Å $SrTiO_3$

$\epsilon \sim 200$



76–02–108–3

FIG. 5

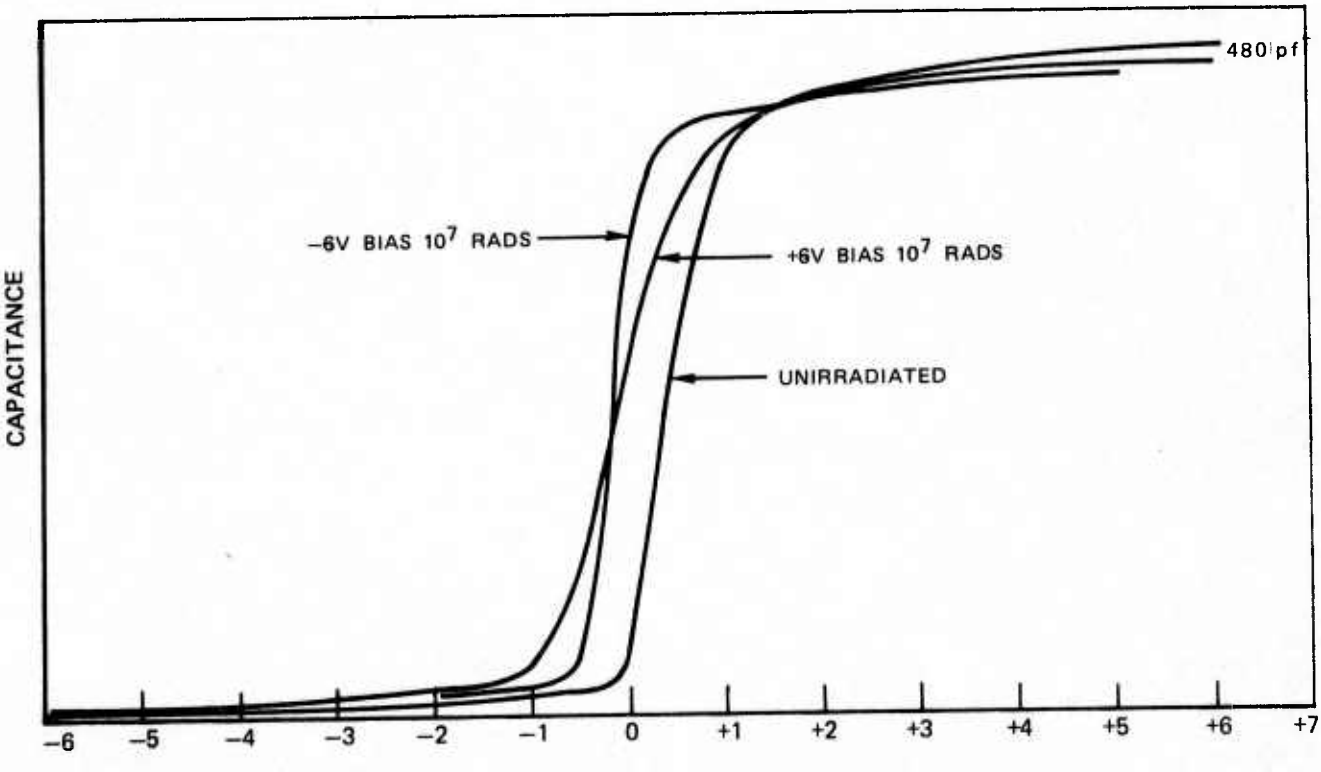
C–V CHARACTERISTICS OF γ–IRRADIATED Al–WO_3–Si CAPACITOR

Al–2700Å WO_3–SILICON: N–TYPE 8Ω–cm

15 mil DIAMETER Al DOT

$\epsilon \sim 147$

$N_{fc} = -1 \times 10^{12}/cm^2$

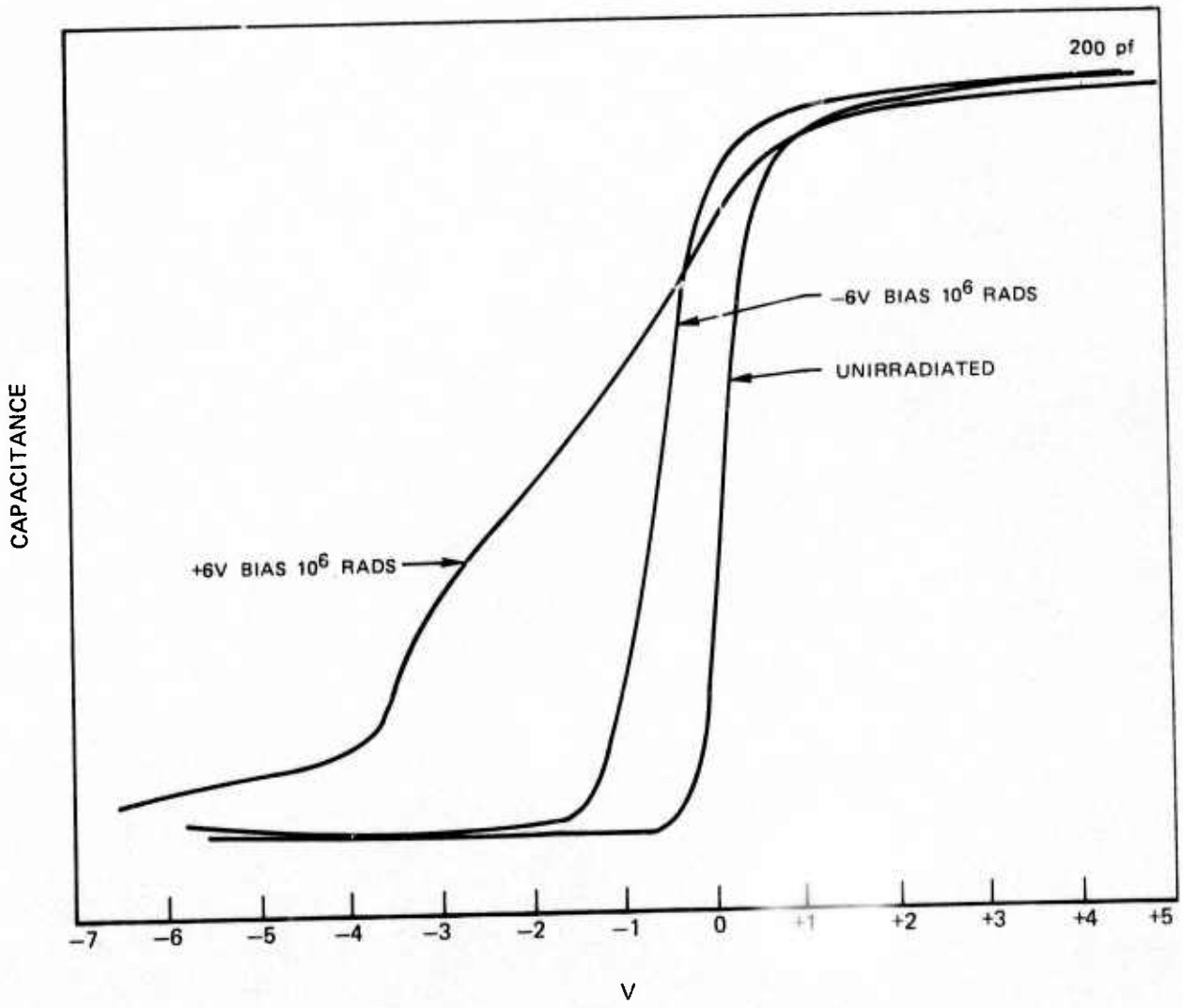


76–02–108–2

FIG. 6

C–V CHARACTERISTICS OF γ–IRRADIATED Al–WO_3–SiO_2–Si CAPACITOR

Al–3000Å WO_3–100Å SiO_2–SILICON CAPACITOR



76–02–108–1

3.3 Hafnium Dioxide MIS Capacitors

A wide range of deposition conditions for reactively sputtered hafnium dioxide films were investigated. The parameters which appeared to yield the better films corresponded to a substrate temperature of 400 °C, a power density of 1.5 W/cm^2 and an oxygen pressure of 1.5 x 10^{-2} Torr. Sputtered films prior to annealing, exhibited a positive surface charge density of approximately 10^{13}/cm^2 and a moderately high surface state density which was reflected by distortion in the high frequency C-V characteristic. Annealing in oxygen at 800 °C for one hour stabilized the insulator charge distribution.

The surface finish of the sputtered films is relatively smooth. An electron micrograph of a typical surface is shown in Fig. 7. All the sputtered films were polycrystalline over the range of deposition temperatures investigated (100°- 600°C). A typical relfection electron diffraction pattern for a hafnium dioxide film is shown in Fig. 8. The crystal structure of the films correspond to the monoclinic phase of HfO_2.

The dielectric constant of the films ranged from a low of 15 for depositions of 100 °C up to 22 for films deposited at 400 °C. Loss tangent measurements on hafnium dioxide films measured at 100 kHz typically fell near 0.005. The dc resistivity at low voltages was found to range between 10^{13} to 10^{16} ohm-cm.

These properties compare closely with the results reported by Goldstein (Ref. 19) and Pratt (Ref. 20) for sputtered hafnium dioxide films. Goldstein reported a value of 24.5 for the dielectric constant for dc reactively sputtered hafnium dioxide. Pratt reported a dielectric constant of 16 for films deposited by rf sputtering from a ceramic HfO_2 target.

The refractive index of the films varied from 2.0 for the low temperature deposits at 100 °C up to 2.2 for the 400 °C depositions.

Exposure of the films to acids, such as boiling HCl, hot H_2SO_4, 49 percent HF, and boiling aqua-regia, did not result in any significant etching of the HfO_2. Aqueous solutions of KOH and NaOH had no appreciable effect either. Only boiling phosphoric acid was found to slowly etch the HfO_2 films formed by reactive sputtering.

The C-V characteristics, for an MIS capacitor fabricated with sputtered hafnium dioxide on "bare" silicon is shown in Fig. 9. The interface charge density for this sample is -1 x 10^{11}/cm^2. For other depositions, the interface charge density ranges between -1 x 10^{11} to -5 x 10^{11}/cm^2. These films do show some effects of a slow trapping instability for bias fields exceeding ±10^6 V/cm at room temperature and ±4 x 10^5 V/cm at 200 °C. Shifts of 1-2 V in flatband voltage occur if the bias voltages corresponding to the above fields are maintained for a period of 10 min. The sense of the shift is positive for negative bias and negative for positive

FIG. 7

ELECTRON MICROGRAPH OF REPLICATED SURFACE OF 2500Å THICK HfO_2 FILM

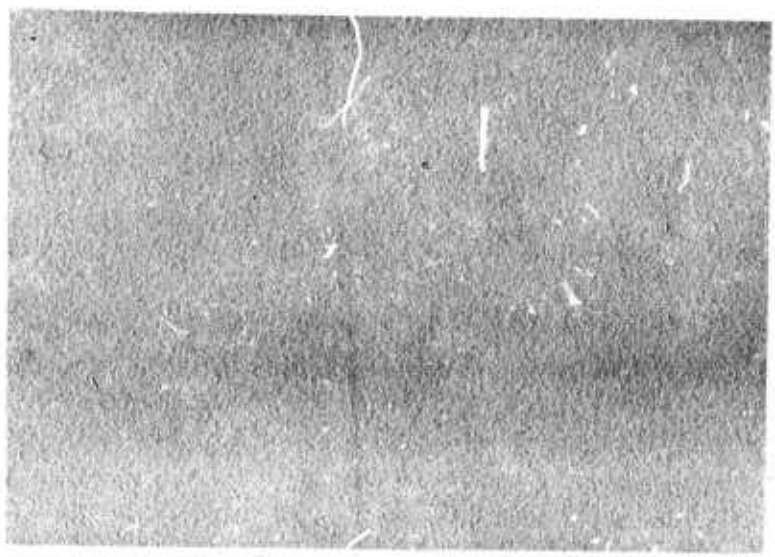


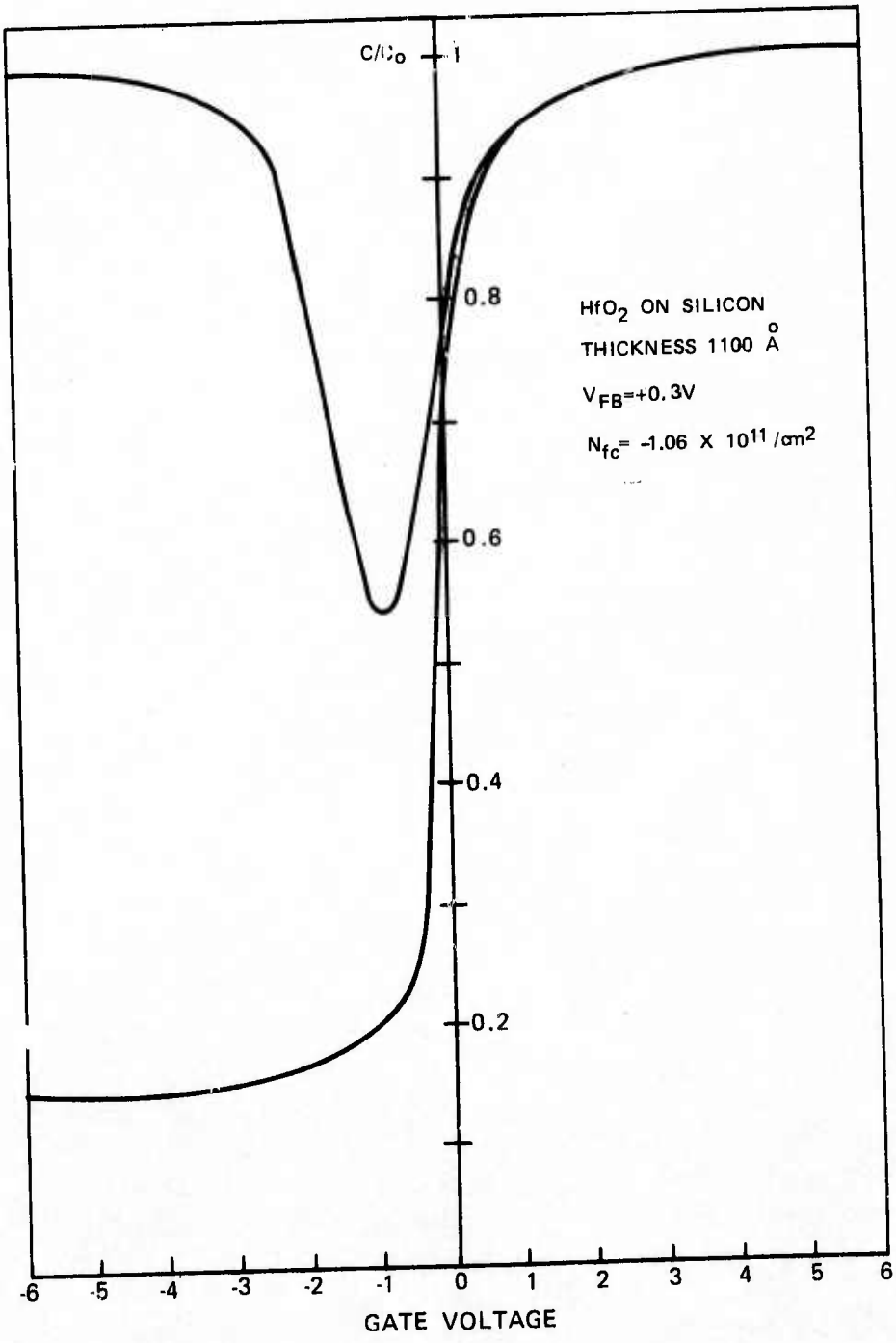
FIG. 8

REFLECTION ELECTRON DIFFRACTION PATTERN FOR HfO_2 FILM

76-02-105-9

FIG. 9

C-V CHARACTERISTICS OF Al-HfO_2-Si CAPACITOR



76-02-105-13

bias. When hafnium dioxide films are deposited over 100 Å thermal SiO_2 films, the slow trapping instability is reduced under positive bias for most samples but does not show significant improvement under negative bias. The C-V characteristics for a composite HfO_2-SiO_2 insulator is shown in Fig. 10. Positive flat band voltages are achieved with the HfO_2-SiO_2 composite insulator. Similar effects have been observed for Al_2O_3-SiO_2 composites.

Hafnium dioxide films were examined to determine if they would act as barriers to positive ion drift. The HfO_2 surface was contaminated by dipping the wafer into a salt solution prior to deposition of the aluminum electrodes. The film was stressed at 5×10^5 V/cm at 200 °C for one hour. This resulted in a flatband voltage shift of -12 volts. An anneal at 250 °C for 1/2 hour produced only a small recovery in flat band voltage. Flatband voltage shifts produced by charge injection normally recover to their initial state for a comparable anneal. The results show that polycrystalline HfO_2 will not act as a diffusion barrier for positive ions.

Fast surface state density near midgap can be estimated from the dispersion between the quasi-static capacitance and the low frequency capacitance (Ref. 15). Using this technique, the surface state density at midgap for sputtered HfO_2 capacitors is found to range between 5×10^{11} to $1 \times 10^{12}/cm^2$.

Capacitors exhibiting stable C-V characteristics were subjected to Co (60) γ-ray exposures up to 10^7 rads. In most cases the capacitors fabricated on "bare" silicon showed remarkable radiation resistance. In many cases, negative flatband voltage shifts of 1 to 3 V were observed for bias voltages of ±6V and a radiation exposure of 10^7 rads. Capacitors of the same group with zero bias and -6V bias also exhibited negative flatband shifts and these shifts ranged between 0 to 2V. Figure 11 shows a typical variation in C-V characteristics for an irradiation dose of 10^7 rads. Deviations from this behavior were also observed where the sense of flatband shifts for comparable bias were reversed, although comparable deposition conditions were used to fabricate the samples. Unfortunately, there was insufficient time to determine the cause of these discrepancies.

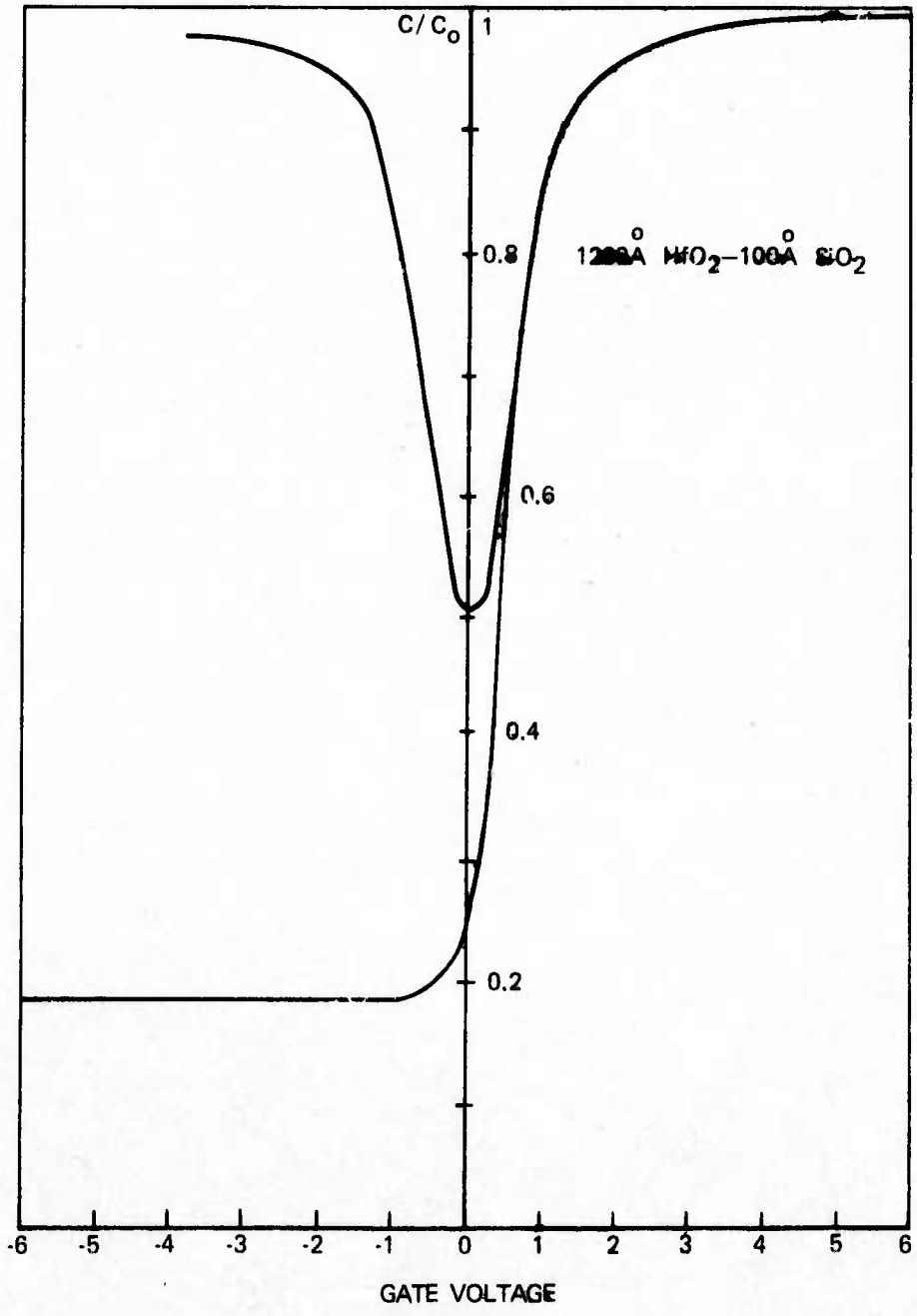
Capacitor structures fabricated with HfO_2 sputtered on 100 Å thermal SiO_2 films exhibited a greater degree of radiation sensitivity. Flatband voltage shifts were observed to range from 2 to 6 V for irradiations of 10^7 rads. In most cases the shifts were consistent with the development of positive charge in the insulator.

3.4 Discussion of Results

Since the nature of the investigation was a survey of the radiation tolerance of a selected group of high dielectric constant insulators, far from optimum deposition conditions for the various insulators could be determined. In spite of this limitation, samples could be selected which exhibited a reasonable degree of stability under bias and temperature stress to provide a vehicle for the evaluation of the radiation tolerance of the dielectrics HfO_2, $SrTiO_3$ and WO_3.

FIG.10

C–V CHARACTERISTICS OF Al–HfO_2–Si CAPACITOR

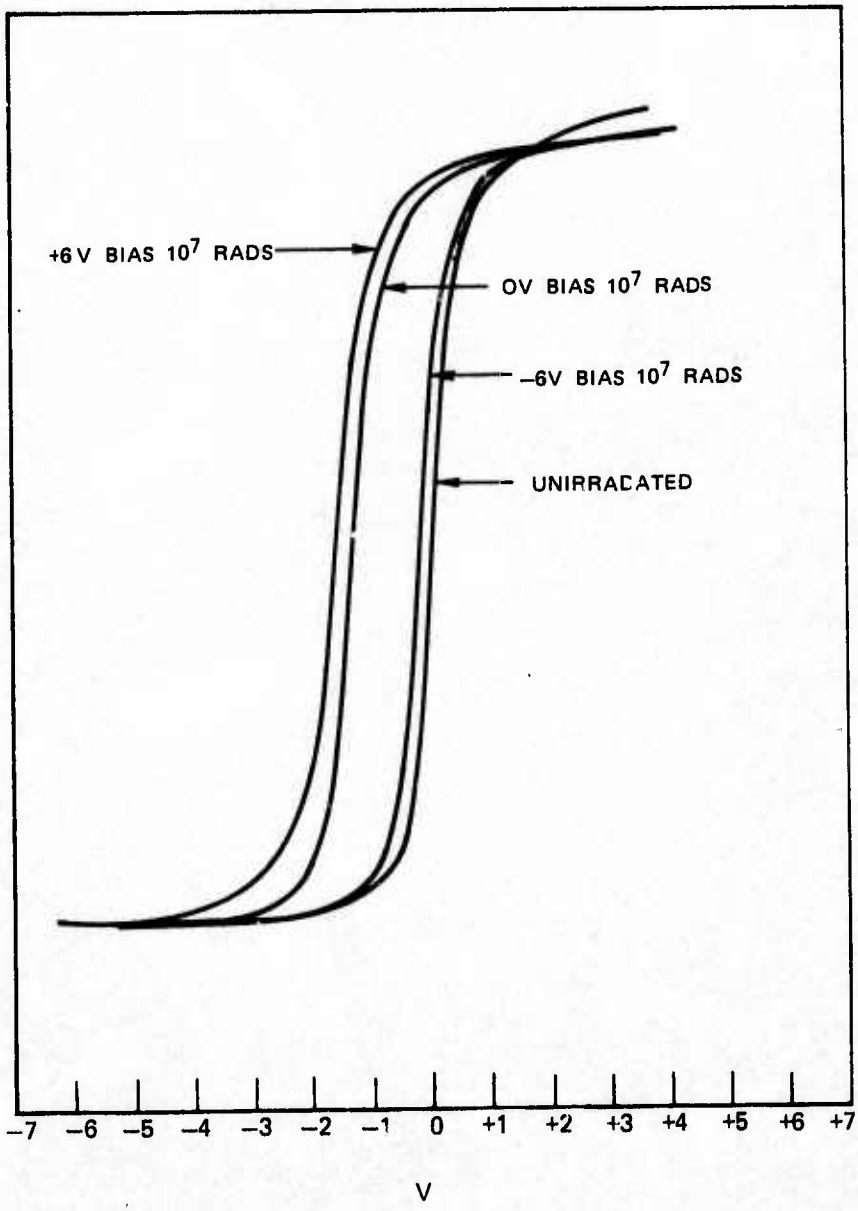


76-02-105-17

FIG. 11

C–V CHARACTERISTICS OF HfO_2 CAPACITOR SUBJECTED TO 10^7 RADS Co (60) γ – IRRADIATION

Al–1100Å HfO_2–SILICON CAPACITOR



76–02–108–7

Overall, a high degree of radiation tolerance was shown by all. The major drawback of $SrTiO_3$ and WO_3 is related to their poor insulator qualities. Both are known to be defect semiconductors in the nonstoichiometric state. Evidently the failure to produce films sufficiently near stoichiometry places a severe limitation on their usefulness in most applications. Because of hafnium dioxides superior insulating properties, it appears to have considerably more potential for the fabrication of radiation tolerant insulated gate field effect transistors. A higher degree of reproducibility for the process would be desirable for the fabrication of MIS structures exhibiting a high degree of stability under bias and temperature stress. In spite of these problems, the results obtained with irradiated HfO_2 MIS capacitors were sufficiently encouraging to justify the fabrication of transistors for further evaluation of the potential of HfO_2 for radiation hardened insulated gate field effect transistors. These results are covered in the following section.

4.0 HAFNIUM DIOXIDE TRANSISTOR FABRICATION AND EVALUATION

The insensitivity of hafnium dioxide to etching by acids and bases presented a problem regarding the fabrication of transistors. A method for making contact to the source drain electrodes was required. In order to achieve this end, a lift-off technique was developed which removed hafnium dioxide from all areas but the gate region. The processing of transistors forced elimination of the sputter etching of the substrate prior to deposition of the hafnium dioxide. It was found that this process modification did not have a significant effect on the radiation hardness.

4.1 Transistor Fabrication

P-channel devices were fabricated on 10Ω - cm phosphorous doped (100) silicon. N-channel units were fabricated on 5Ω - cm boron doped (100) silicon. The process steps, including the diffusion of the source and drain, followed standard processing procedures. The steps leading up to the deposition and definition of the hafnium dioxide gate dielectric are shown schematically in Fig. 12. The processing steps are as follows:

1) Sputter 500 Å film of chromium metal (Fig. 12a)
2) Photoresist first oxide, remove mask and etch chromium (Fig. 12b)
3) Etch silicon dioxide, leaving approximately 2000 Å of SiO_2 (Fig. 12c)
4) Photoresist second oxide, remove mask and etch chromium (Fig. 12d)
5) Etch remaining 2000 Å of SiO_2 in gate area. (Fig. 12e)

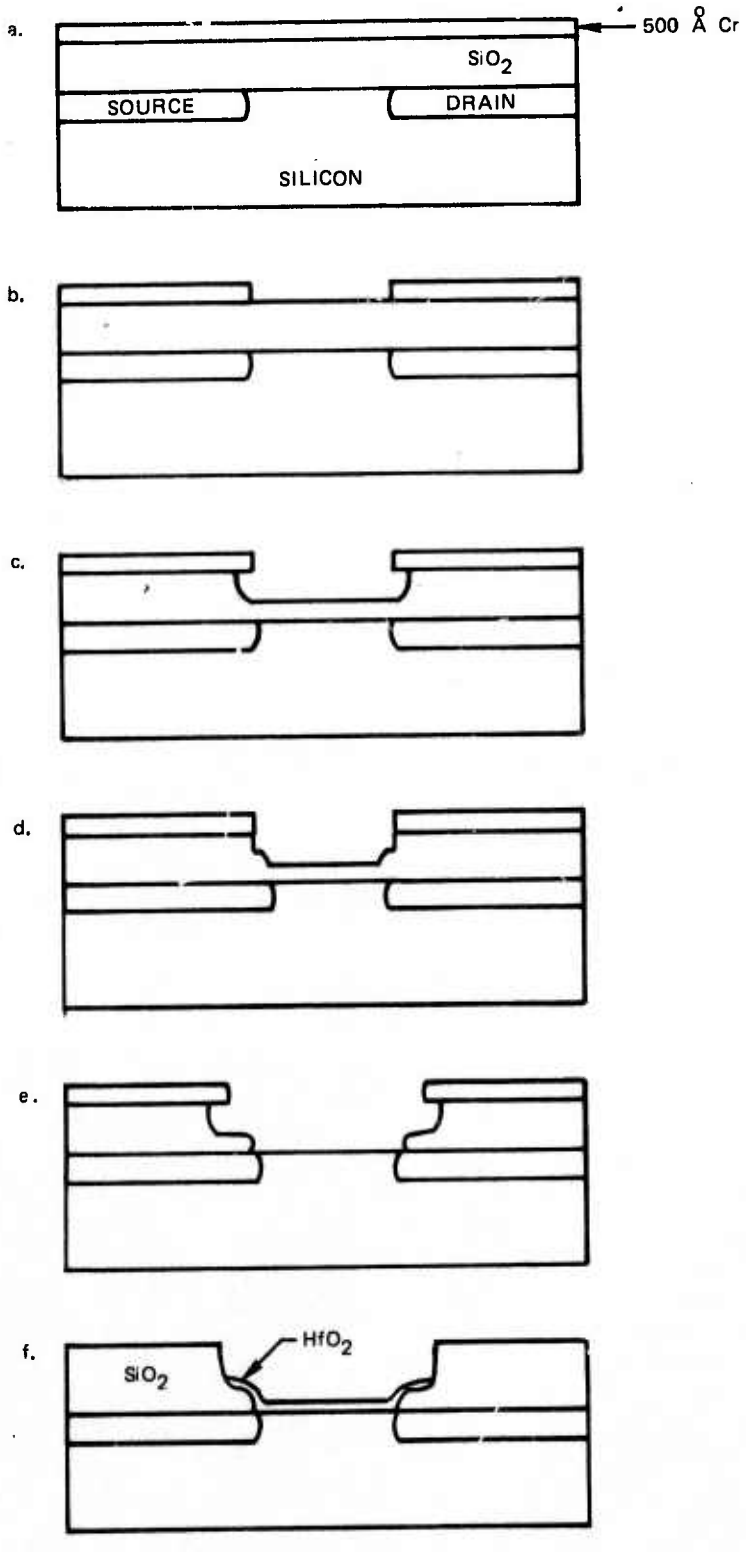
The etching of the chromium to define the gate area can be done either chemically or by ion milling. Devices were fabricated by both techniques. Figure 13 shows the gate region just before deposition of the HfO_2 film.

The purpose of process steps 4 and 5 may not be obvious but their function was to provide a stepless transition between the SiO_2 and sputtered HfO_2 film in the vicinity of gate and source-drain junctions. If the gate region were opened completely in step 3 and sputtered HfO_2 deposited, one would run the risk of a discontinuity between the SiO_2 and HfO_2. This is a consequence of the shadowing effect of the overhanging chromium film. Deposition of the gate metallization therefore, would result in the shorting of the gate to either the source or drain.

6) Following deposition of the HfO_2 ($400^{\circ}C$, 1.5×10^{-2} Torr O_2), the wafer was placed into a chrome etch (HCl) and ultrasonically agitated. The hafnium dioxide was removed from all but the gate regions (Fig. 12f). Following these steps, the wafer was annealed in O_2 at $800^{\circ}C$ for one hour. Contact holes are opened up, 5000 Å of Al is evaporated, and the metallization pattern was defined. The contacts are sintered for 15 minutes at $500^{\circ}C$ in a nitrogen ambient.

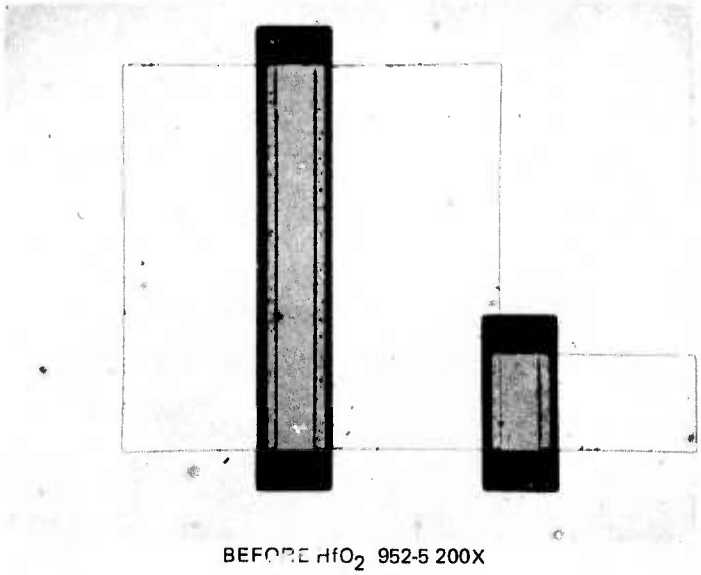
FIG. 12

PROCESS SEQUENCE FOR HFO_2 TRANSISTOR FABRICATION



76-02-105-12

GATE AREA AFTER SECOND ION MILL OF CHROMIUM MASK



BEFORE HfO_2 952-5 200X

76-02-105-4

The test chip designed for the evaluation is shown in Fig. 14. Two 15 mil diameter capacitors were provided for C-V measurements for the evaluation of the surface properties. A single transistor and simple inverter comprise the remaining chip elements. The single transistor and input transistor of the inverter were of identical geometries. The channel length of the transistors was one mil. The channel width to length ratio (Z/1) was 10 for the large transistors whereas this ratio was 2.5 for the load transistor of the inverter. The transistors were fabricated with gate protection diodes.

The wafers were scribed into chips and mounted in TO-5 packages for testing and irradiation.

4.2 Transistor Evaluation

Both n-channel and p-channel transistors were fabricated. The HfO_2 gate insulator thickness was 1200 Å. In all, three wafers of each variety were processed. The variation in device characteristics among the three separate p-channel runs were negligible. On the other hand, the results were quite varied between the processed n-channel wafers. The first of the processed n-channel wafers led to devices with threshold voltages centered about +0.1 to 0.3 volts while the second wafer yielded devices which were normally on at zero bias. The last n-channel wafer processed produced devices which had threshold voltages centered at V_T = +1.8V. Figure 15 shows typical I_D-V_G characteristics of the first processing run of n-channel and p-channel devices. The device transconductances were excellent. Surface mobility of holes was determined to be 235 cm^2/V-sec and electrons 500 cm^2/V-sec. These figures indicate that sputtering of the gate dielectric did not result in a serious degradation of device characteristics.

4.2.1 P-Channel Devices

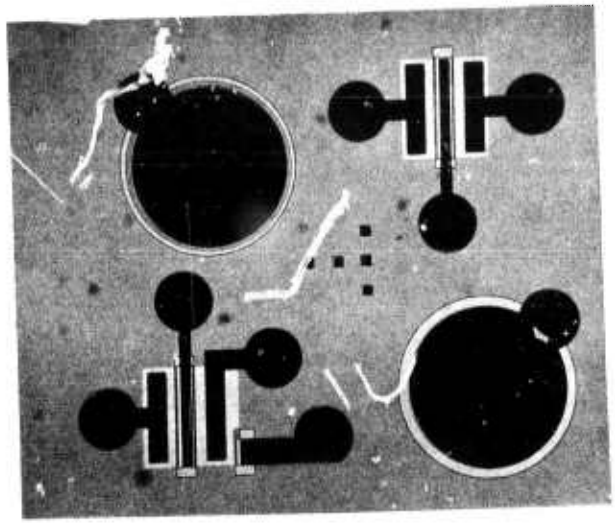
The distribution of threshold voltages observed for p-channel devices is shown in Fig. 16. It is evident that the bulk of the device threshold fall below V_T = -1V.

Circuits under bias were subjected to Co(60) γ-ray exposures of 10^5 rads, 10^6 rads and 10^7 rads. The dose rate was 10^5 rads/hour and therefore 100 hours were required to accumulate 10^7 rads. Higher dose levels were impractical due to time limitations.

Figure 17 shows the output characteristics of the large transistor (Z/1 = 10) as a function of irradiation level, and impressed bias of -6V. There is negligible degradation of device transconductance. The primary effect is a shift in threshold voltage to more negative values. This is illustrated more clearly in Fig. 18 which shows the transfer characteristics as a function of irradiation exposure. Transfer characteristics of the small transistor (Z/1 = 2.5) for irradiation with zero

FIG. 14

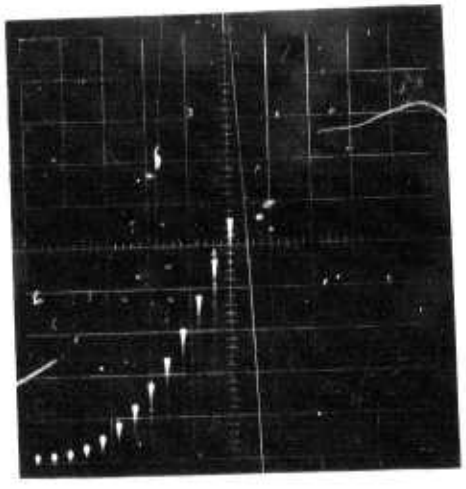
TEST CHIP FOR HfO_2 TRANSISTOR AND INVERTER EVALUATION



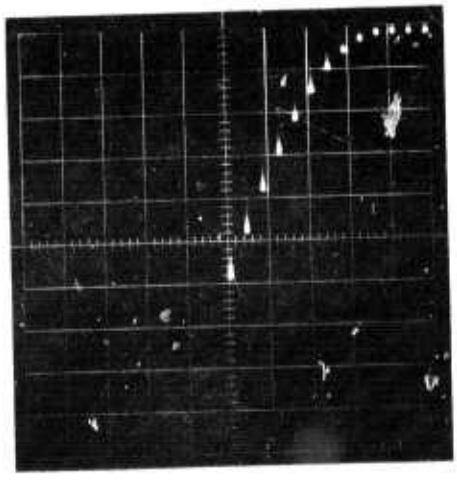
76-02-105-3

FIG. 15

$I_D - V_G$ CHARACTERISTICS OF HfO_2 N – CHANNEL AND P – CHANNEL HfO_2 INSULATED GATE FIELD EFFECT TRANSISTORS



N– CHANNEL TRANSISTOR
VERT – 0.1 ma/div
HORIZ – 0.5 V/div (GATE)
0.2 V/STEP (12 STEPS)

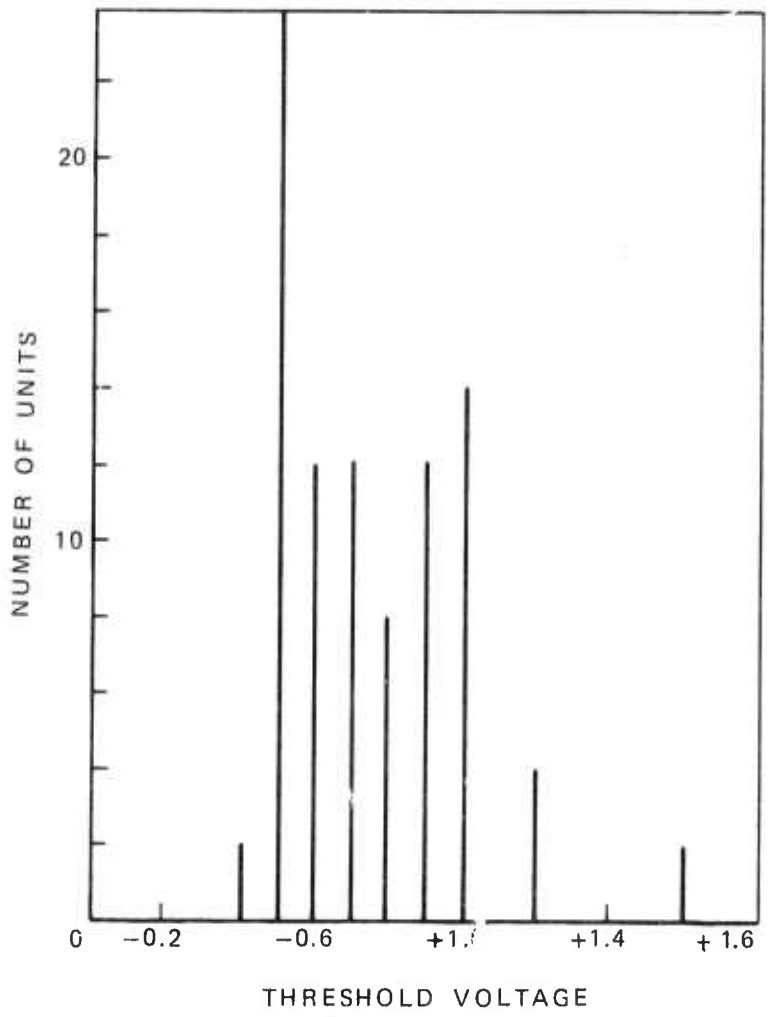


P –CHANNEL TRANSISTOR
VERT – 0.05 ma/div
HORIZ – 0.5 V/div (GATE)
0.2 V/ STEP (12 STEPS)

76-02-105-11

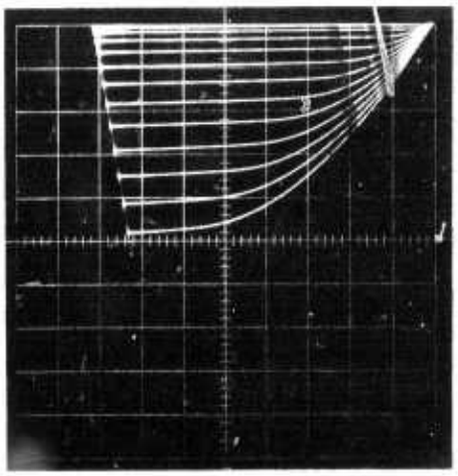
FIG. 16

DISTRIBUTION OF THRESHOLD VOLTAGES FOR HfO_2 P-CHANNEL TRANSISTORS (92 UNITS)



$I_D - V_D$ CHARACTERISTICS OF P–CHANNEL HfO_2 TRANSISTORS BEFORE AND AFTER Co (60) γ– IRRADIATION

BEFORE IRRADIATION

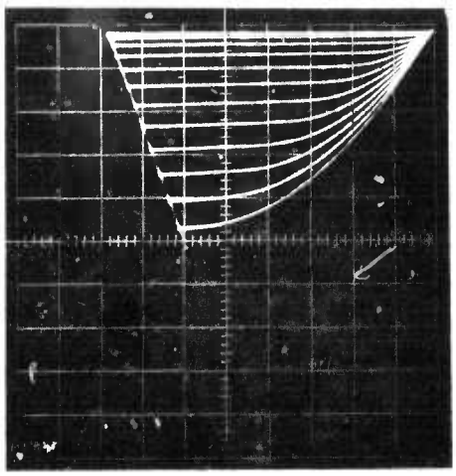


VERT – 0.5 ma/div

HORIZ– 1.0 V/div

V_G – 0.5 V/ STEP (12 STEPS)

10^5 RADS

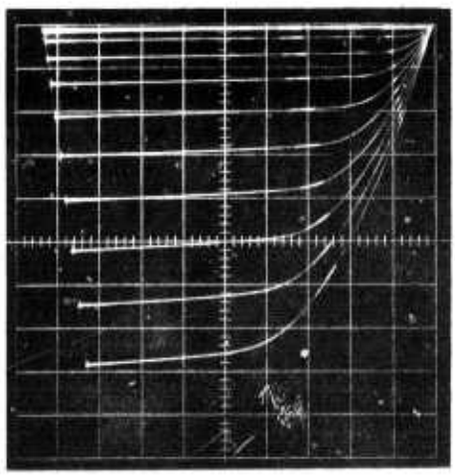


VERT – 0.5 ma/div

HORIZ – 1.0 V/div

V_G – 0.5 / STEP (12 STEPS)

10^6 RADS

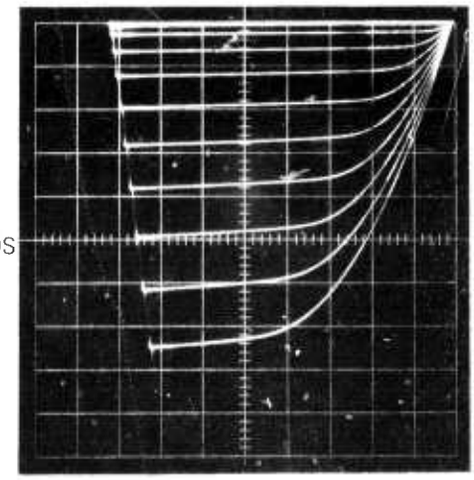


VERT – 0.2 ma/div

HORIZ – 1.0 V/div

V_G –0.5 V/ STEP (12 STEPS)

10^7 RADS



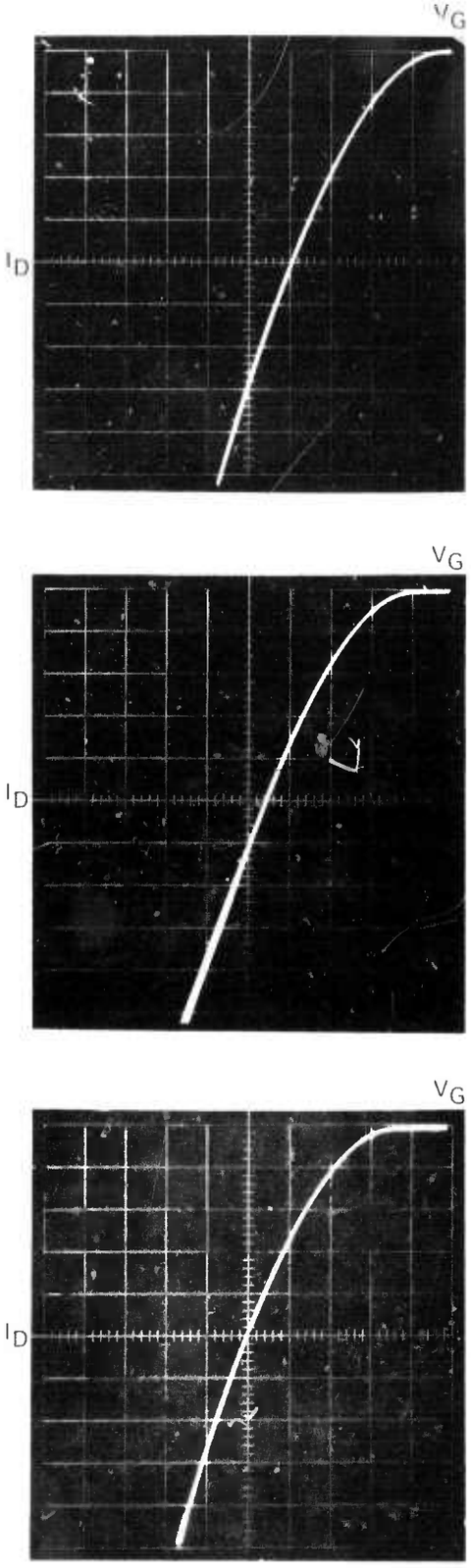
VERT – 0.2 ma/div

HORIZ – 1.0 V/div

V_G – 0.5 V/STEP (12 STEPS)

76-02-105-7

TRANSFER CHARACTERISTICS OF HfO_2 TRANSISTOR BEFORE AND AFTER γ– IRRADIATION



VERT – 0 2 ma/div

HORIZ – 1 0 V/div

76-02-105-8

gate bias shows a similar behavior (see Fig. 19). An accumulation of 10^5 rads results in a negligible effect on device characteristics. Irradiation to 10^6 rads at zero bias leads to negative threshold voltage shifts ΔV_T ranging between -0.5 to -0.9V with the distribution skewed toward -0.9V(see Fig. 20). For a -6V gate bias, and 10^6 rads, ΔV_T ranges between -0.4 to -1.1V (see Fig. 21). Two units from the 50 irradiated shorted out. Transistors with zero gate bias and a dose of 10^7 rads show an overall ΔV_T ranging between -0.8 to -2.0V (see Fig. 22). Those transistors biased at -6V showed a spread in ΔV_T between -0.5 to-2.2V with most of the units centered near -1V. Three devices shifted to positive values of threshold voltage. Four of the 48 units irradiated shorted out. Eleven units were lost due to open bonds due to the problems being experienced with the ultrasonic bonding unit at the time. Unfortunately, the bonding problems placed a limitation on the number of units which could be packaged for study.

4.2.2 N-Channel Devices

As indicated earlier, reproducibility problems were encountered with the fabrication of n-channel units. The first units fabricated had very low threshold voltages typically between +0.1 to 0.3V. When these devices were subjected to irradiation levels exceeding 10^5 rads, they no longer functioned as useful enhancement mode devices. The threshold voltage shifts were typically -0.4V for 10^5 rads and -3.0V for 10^6 rads with the devices biased at +6V. The effects of radiation on these devices is shown in Fig. 24. It was soon discovered that the chromium etch being employed for defining the gate dielectric area was an aqueous solution of $K_3Fe(CN)$, and NaOH which could result in ionic contamination of the devices. Subsequent devices were fabricated using ion milling of the chromium rather than a chemical etch to define the gate dielectric area.

The second attempt at processing n-channel units resulted in devices which were normally on and the third and final attempt produced devices with threshold voltages closely grouped about +1.8V. Irradiation of these devices under zero bias and +6V bias produced threshold voltage shifts to more positive values of threshold voltage. This is illustrated in Figs. 25 and 26. Typical for +6V bias and 10^6 rads produced ΔV_T ranging between +0.6 to 1.0V. Transistors irradiated with zero gate bias showed ΔV_T ranging between +0.4 to 0.8V. Irradiation to 10^7 rads and +6V bias produces threshold voltage shift ranging between +1.1 to 1.5V. Devices with zero gate bias exhibit ΔV_T between +0.9 and 1.4V.

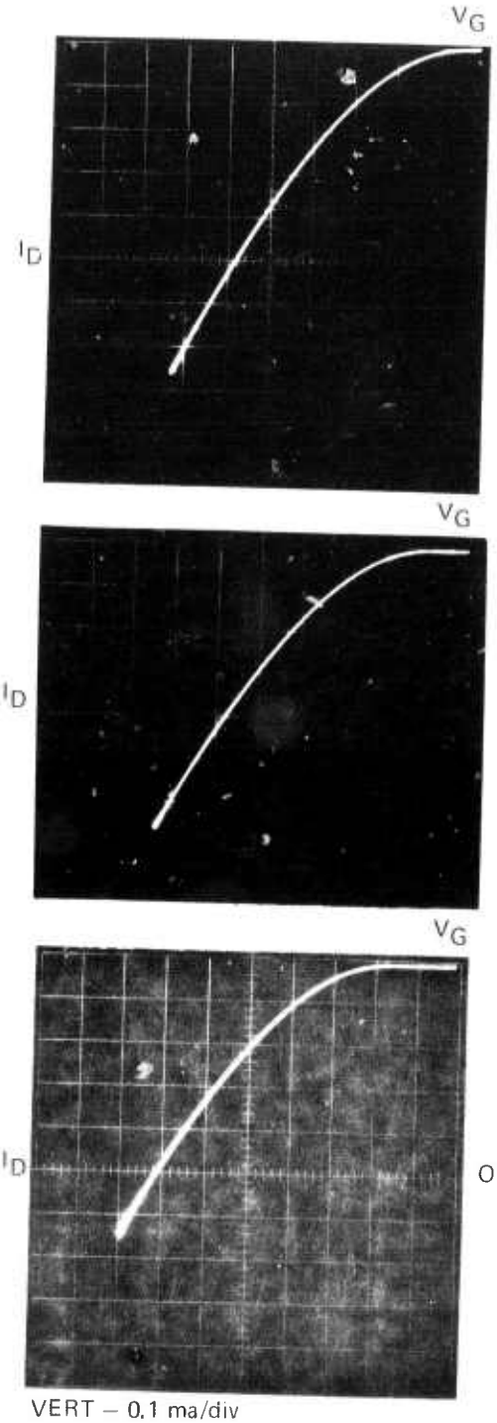
4.2.3 Inverters

Simple enhancement load p-channel and n-channel inverters were fabricated. The transconductance ratio of the input to load transistor was 4:1. Time limitations did not permit the process development for the fabrication of CMOS inverters.

The transfer characteristics for the inverters were obtained with a supply voltage V_{DD} of 6V. P-channel units showed a small change in transfer characteristics with irradiation as can be seen in Fig. 27. The rapid degradation with

FIG. 19

TRANSFER CHARACTERISTICS OF HfO_2 LOAD TRANSISTOR AS A FUNCTION OF γ– IRRADIATION (IRRADIATED WITH $V_G = 0$)

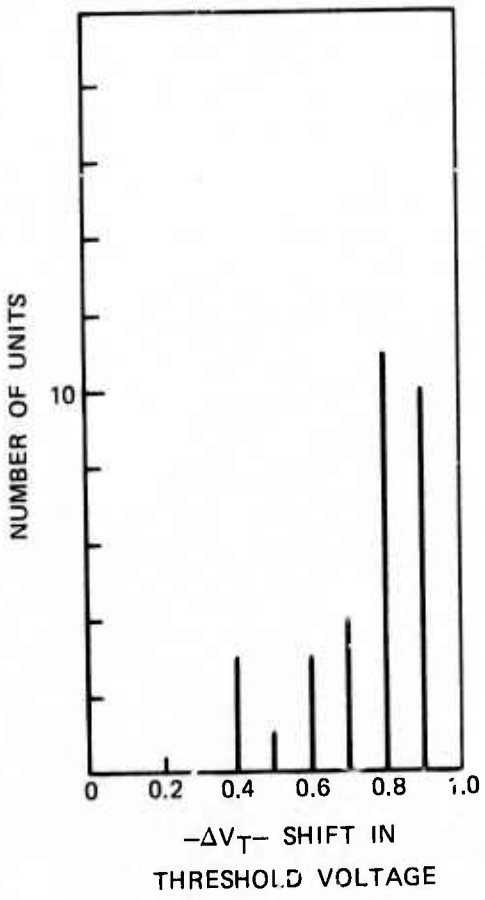


VERT – 0.1 ma/div
HORIZ – 1.0 V/div

76-02-105-6

FIG. 20

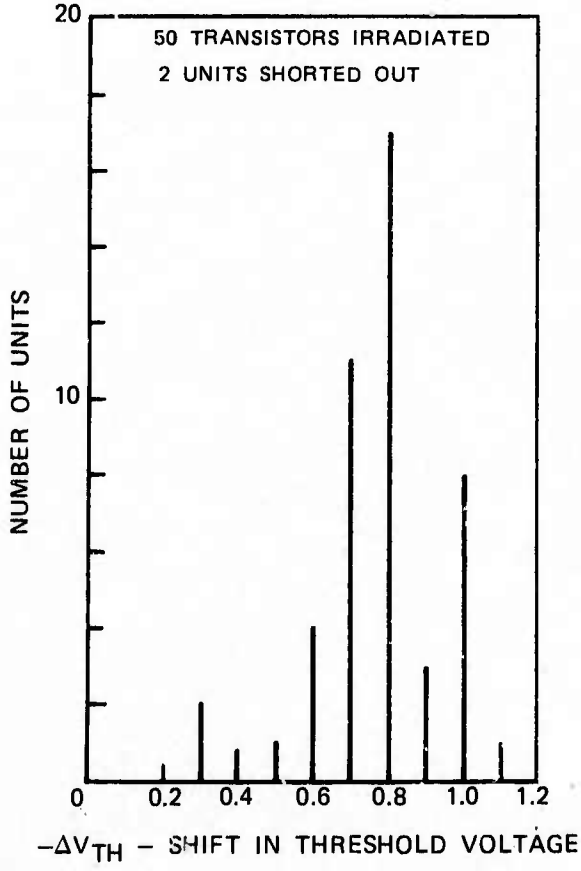
DISTRIBUTION OF THRESHOLD VOLTAGE SHIFT FOR P-CHANNEL HfO_2 TRANSISTORS SUBJECT TO OV BIAS AND 10^6 RADS Co (60) γ- IRRADIATION (32 UNITS)



76-02-105-15

FIG.21

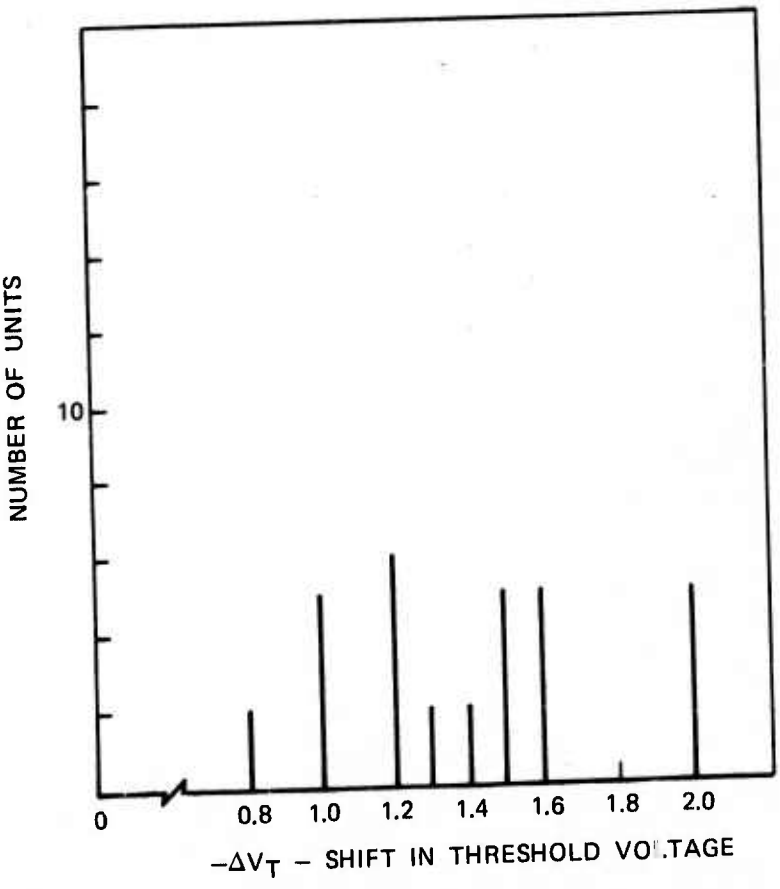
DISTRIBUTION OF THRESHOLD VOLTAGE SHIFTS FOR P–CHANNEL HfO_2 TRANSISTORS FOR –6V BIAS AND 10^6 RADS Co (60)γ– IRRADIATION



76-02-105-18

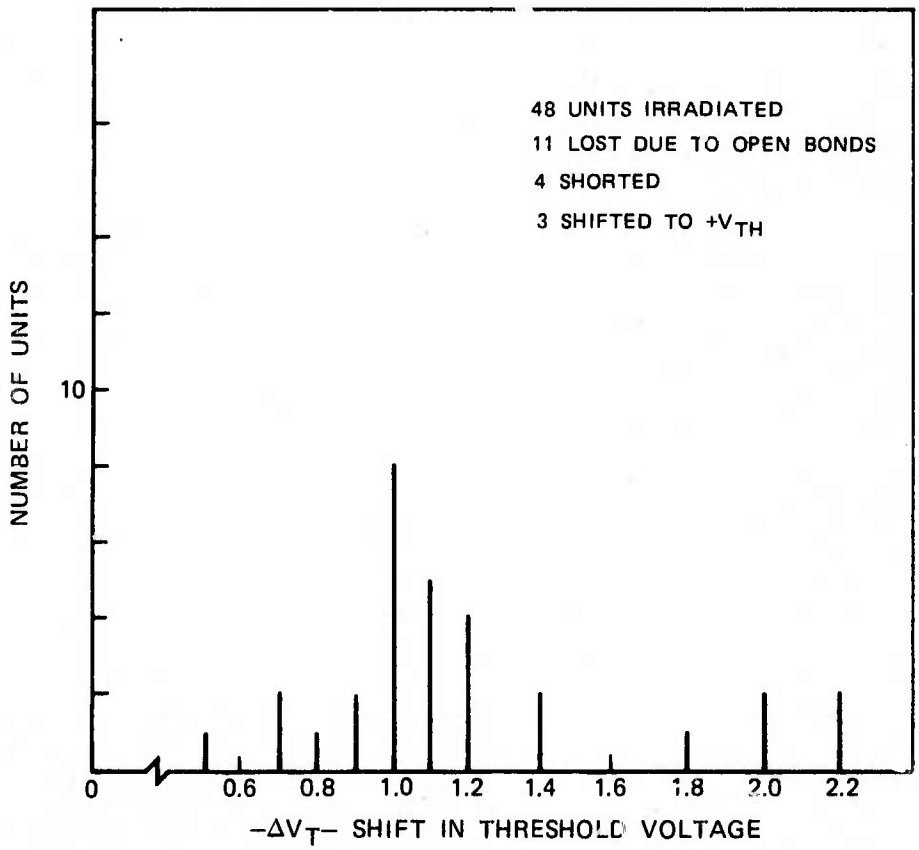
FIG. 22

DISTRIBUTION OF THRESHOLD VOLTAGE SHIFTS FOR P–CHANNEL HfO_2 TRANSISTORS SUBJECT TO OV BIAS AND 10^7 RADS Co (60) γ– IRRADIATION (32 UNITS)



76-02-105-14

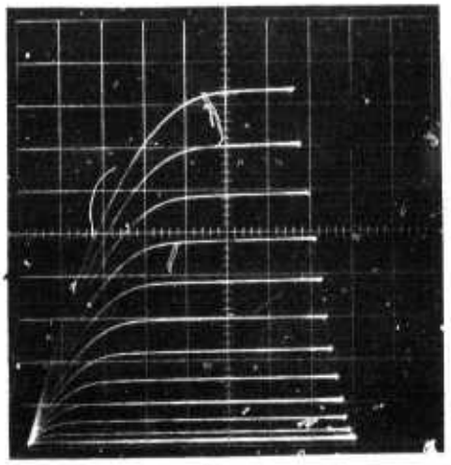
DISTRIBUTION OF THRESHOLD VOLTAGE SHIFTS FOR P–CHANNEL HfO_2 TRANSISTORS BIASED @ –6V AND 10^7RADS Co(60) γ–IRRADIATION



76-02-105-16

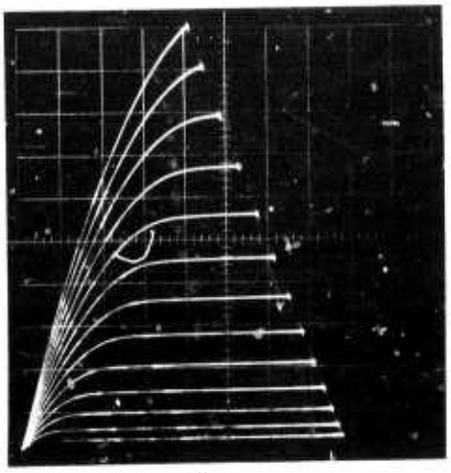
FIG. 24

$I_D - V_D$ CHARACTERISTICS OF N–CHANNEL HfO_2 TRANSISTORS BEFORE AND AFTER Co (60) γ-IRRADIATION



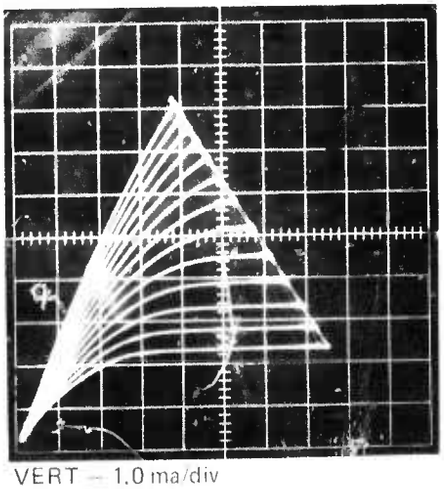
UNIRRADIATED

VERT – 0.5 ma/div
HORIZ – 1.0V/div
V_G – 0.5/STEP (12 STEPS)



+6V BIAS 10^5 RADS

VERT – 0.5 ma/div
HORIZ – 1.0 V/div



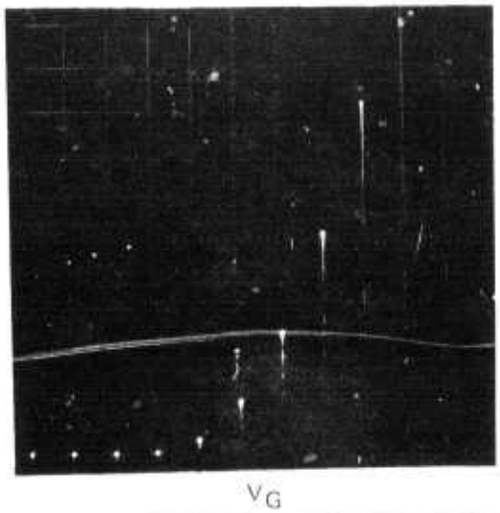
+6V BIAS 10^6 RADS

VERT – 1.0 ma/div
HORIZ – 1.0 V/div

76 02 105 5

FIG. 25

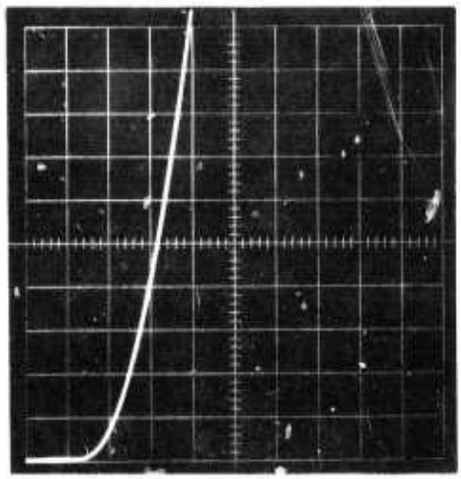
I_D–V_G CHARACTERISTICS OF SERIES III N–CHANNEL HfO_2 TRANSISTORS AS A FUNCTION OF γ– IRRADIATION



76 02-105-2

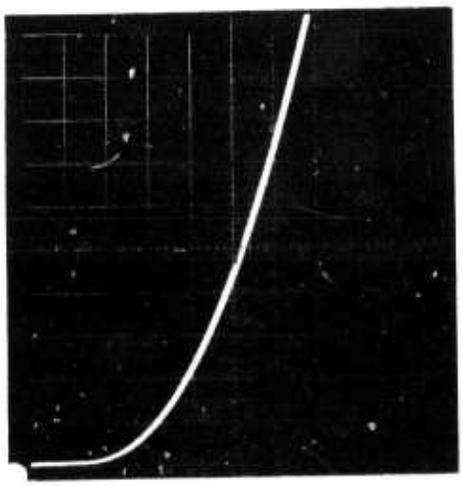
FIG. 26

TRANSFER CHARACTERISTICS OF SERIES III N–CHANNEL HfO_2 LOAD TRANSISTOR AS A FUNCTION OF γ– IRRADIATION



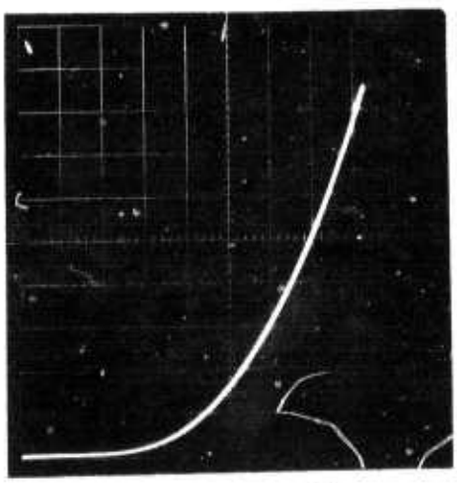
I_D UNIRRADIATED

V_G



I_D OV BIAS 10^6 RADS

V_G



I_D OV BIAS 10^7 RADS

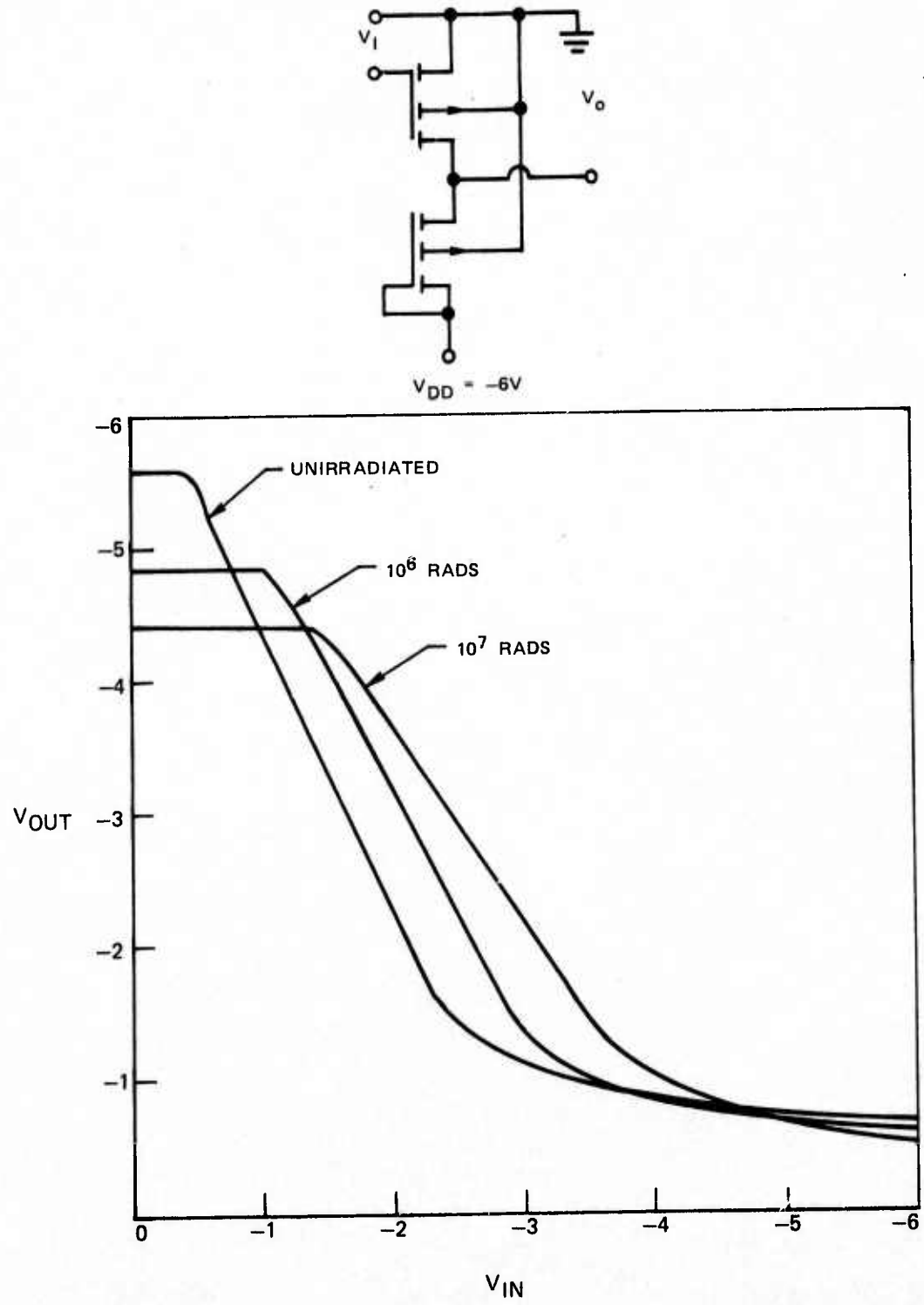
VERT – 0.05 ma/div V_G

HORIZ – 1.0 V/div

76–02–105–1

FIG. 27

TRANSFER CHARACTERISTICS FOR SATURATED LOAD P–CHANNEL INVERTER AS A FUNCTION OF Co(60) γ–RAY DOSE

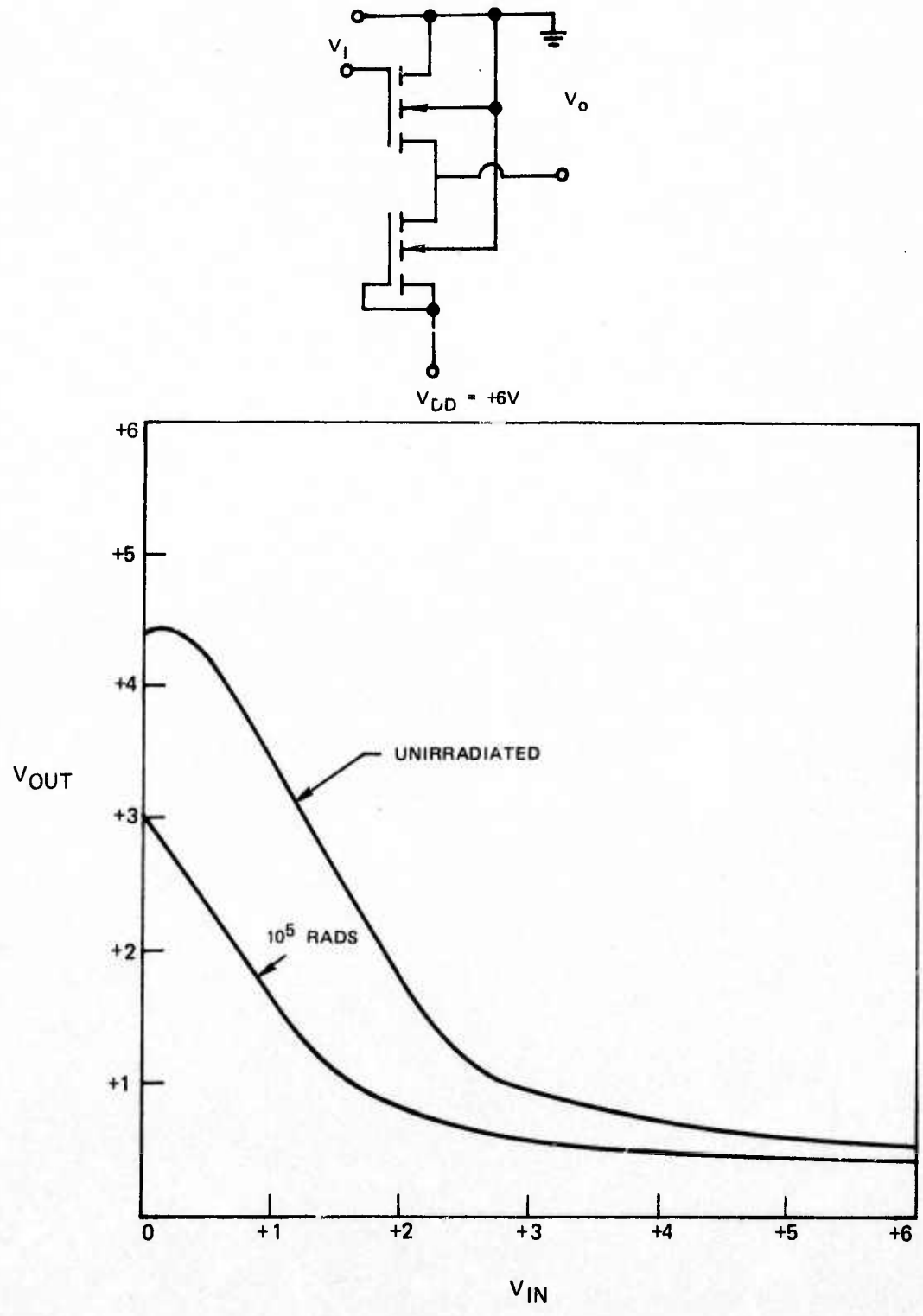


76–02–108–9

irradiation of the sodium contaminated n-channel inverters is shown in Fig. 28. N-channel inverters, from the series III wafer show a moderate degradation of the transfer characteristics after 10^7 rads as shown in Fig. 29.

FIG. 28

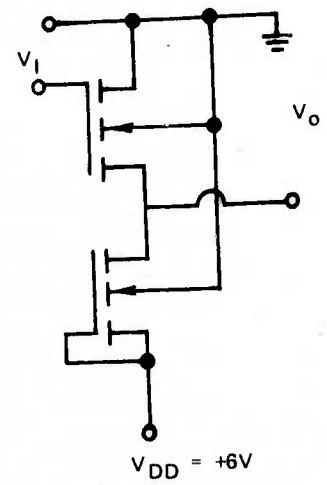
TRANSFER CHARACTERISTICS FOR SATURATED LOAD N–CHANNEL INVERTER AS A FUNCTION OF Co(60) γ–RAY DOSE

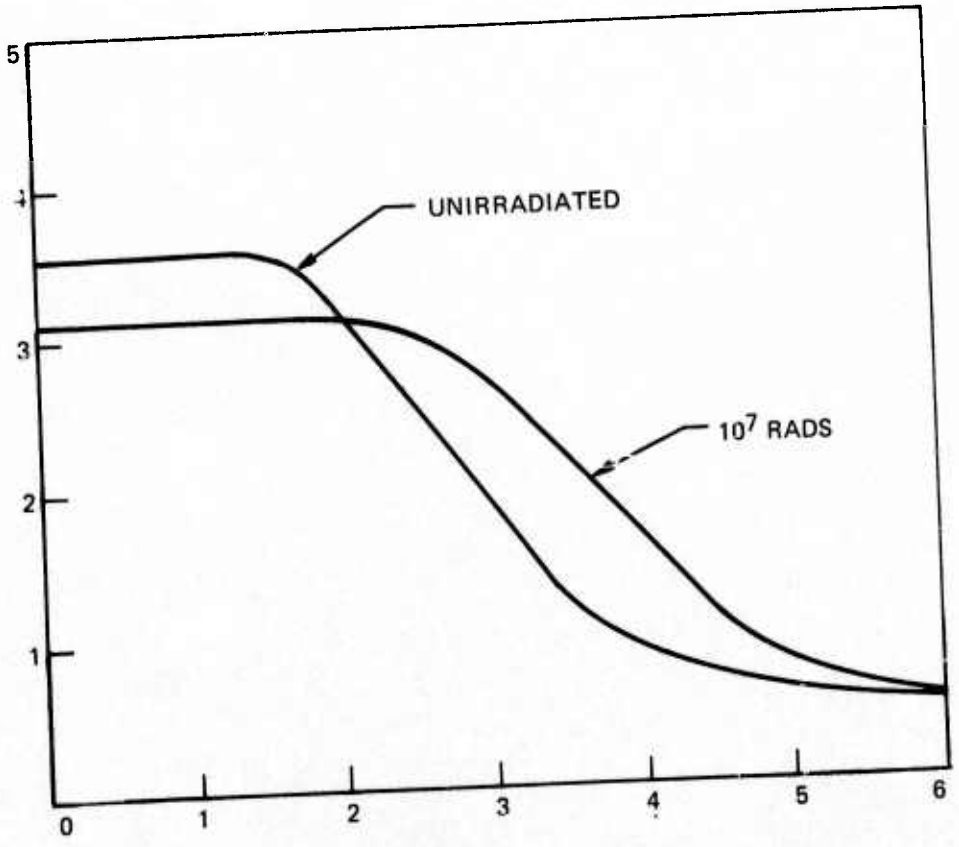


76–02–108–8

FIG. 29

TRANSFER CHARACTERISTICS FOR SATURATED LOAD N–CHANNEL (SERIES 41) INVERTER VS Co(60) a γ–RAY DOSE





76–02–219–1

5.0 DISCUSSION OF RESULTS AND CONCLUSIONS

Reactively sputtered hafnium dioxide has been demonstrated to be a radiation tolerant gate dielectric which holds potential for the fabrication of radiation hardened insulated gate field effect transistors. The threshold voltage shifts induced for Co(60) gamma ray exposures of 10^7 rads and gate biases of $\pm$ 6V usually did not exceed |1.5V| for transistors with 1200 Å HfO_2 gate insulators. The process for device fabrication was not optimized since there were problems encountered regarding reproducibility.

A prime example is the contrary sense of the shift of threshold voltages for devices irradiated with zero bias applied to the gate. For zero bias charge injection should play no role. The series III n-channel transistors shifted to more positive values of threshold voltage, whereas the transistors on the p-channel wafers showed a shift to more negative values of threshold voltage. In one case, the insulator exhibits characteristics in which electron trapping is predominant, and in the other case, hole trapping dominates. These results were obtained for devices which were fabricated using the same processing conditions but at different times. In the radiation tolerance screening with MIS capacitors, similar results were observed with hole trapping predominating in most of the samples prepared. This behavior suggests that the radiation response of hafnium dioxide is sensitive to subtle processing variations. Contamination may be playing a role since the film deposition was done in an area without special environmental control. It is unfortunate that time or funds did not allow for adequate process development, nor for an investigation as to the mechansims which play a role in making sputtered hafnium dioxide films relatively insensitive to ionizing radiation.

A disappointing feature of HfO_2 is that the polycrystalline films did not act as barriers to positive ion drift as was found for Si_3N_4 and Al_2O_3 but this consideration alone should not discourage the application of HfO_2 gate dielectrics. The resistance to attack by most aqueous acids and bases does add some degree of complexity by requiring the addition of nonstandard processing steps for device fabrication, but the situation is not much different for the application of aluminum oxide (Ref. 21) for radiation tolerant gate insulators. Charge injection at higher bias voltages leading to threshold voltage shifts probably is the most serious problem encountered with rf sputtered HfO_2 films. This problem is not unique to HfO_2 and problems of a similar nature have been encountered with aluminum oxide gate dielectrics (Refs. 11, 12, 21, 22). This slow trapping instability could limit the range of usefulness of the HfO_2 films particularly in applications at elevated temperature where the effect is more pronounced. One of several factors may be contributing to the instability. From the sense of the hysteresis, one could attribute the behavior to charge transfer at the gate electrode. An alternative explanation is that the instability may be due to ionic polarization of the oxide resulting from field ionization of defects in the HfO_2 film. This effect could be

particularly significant at the ill defined silicon-HfO_2 interface. The composition here probably is some form of mixed hafnium-silicon oxide. Additional effort is required to resolve this problem.

Aside from the slow trapping instability, reactively sputtered HfO_2 offers a number of attractive features.

1. The dielectric constant of HfO_2 ($\epsilon = 22$) makes it attractive from the standpoint of significantly higher IGFET transconductance relative to SiO_2 ($\epsilon = 3.9$) gate dielectrics.

2. Sputtered hafnium dioxide films exhibit a relatively low negative surface charge density (-1×10^{11} to $5 \times 10^{11}/cm^2$) permitting the fabrication of low threshold voltage n- and p-channel transistors.

3. The surface state density at mid-gap of sputtered films is moderate ($5 \times 10^{11}/cm^2$ to $1 \times 10^{12}/cm^2$).

4. Films did not etch appreciably in common aqueous acids and bases. This insensitivity of the HfO_2 films to acids and bases make them attractive coatings for application in corrosive environments.

In conclusion, it has been demonstrated that n-channel and p-channel transistors fabricated with a reactively sputtered gate dielectric of HfO_2 show a high degree of radiation tolerance for gamma-ray doses to 10^7 rads. However, the problems of the slow trapping effect must be brought under control.

6.0 REFERENCES

1. Lindmayer, J., and W. P. Noble, Jr.: IEEE Trans. Electron Device, ED-15, 637 (1968).

2. Kjar, R. A., J. L. Peel and C. Y. Wrigley: IEEE Trans. Nucl. Sci., NS-16, 207 (1969).

3. Hughes, H. L.: Trans. Nucl. Sci., NS-16, 195 (1969).

4. Perkins, C. W., K. G. Aubuchon and H. G. Dill: IEEE Trans. Nucl. Sci., NS-15, 176 (1968).

5. Aubuchon, K. G.: IEEE Trans. Nucl. Sci., NS-18, 117 (1971).

6. Perkins, C. W.: Appl. Phys. Letters, 12, 153 (1968).

7. Newman, P. A. and H. A. R. Wegener: IEEE Trans. Nucl. Sci., NS-14, 293 (1967).

8. Schmidt, P. F., M. J. Rand, J. P. Mitchell, and J. D. Ashner: IEEE Trans. Nucl. Sci., NS-16, 211 (1969).

9. Schmidt, P. F. and J. D. Ashner: IEEE Trans. Nucl. Sci.: NS-17, 11 (1970).

10. Zaininger, K. H. and A. S. Waxman: Trans. Electron Device, ED-16, 333 (1969).

11. Micheletti, F. B. and F. Kolondra: IEEE Trans. Nucl. Sci., NS-18, 131 (1971).

12. Schlesier, K. M. and P. E. Norris: IEEE Trans. Nucl. Sci., NS-19, 275 (1972).

13. Linz, A: Phys. Rev., 91, 753 (1953).

14. Sawada, S.: J. Phys. Soc. Japan, 11, 1237 (1956).

15. Gerstenberg, D.: 14th Nat. Vac. Symp. Am. Vac. Soc., (1967).

16. Kuhn, M.: Solid State Electron, 13, 873 (1970).

17. Pennebaker, W. B.: IBM J. Res. Develop., 13, 686 (1969).

18. Shuskus, A. J., D. J. Quinn, D. E. Cullen: App. Phys. Lett., 23, 184 (1973).

References (Continued)

19. Goldstein, R. M. and F. W. Leonhard: Proc. IEEE Components Conf. 1967, p. 312.

20. Pratt, I. H.: Proc. IEEE Components Conf., 1969, p. 335.

21. Duffy, M. T. and A. G. Revesz: J. Electrochem. Soc., 117, 372 (1970).

22. Harari, E. and B. S. H. Royce: IEEE Trans. Nucl. Sci., NS-20, 280 (1973).

Distribution of Report R76-921337-19

Director (3)
Advanced Research Projects Agency
Attention: Program Management
1400 Wilson Boulevard
Arlington, Virginia 22209

Office of Naval Research (3)
800 North Quincy Street
Arlington, Virginia 22217
Attention: Code 421

Director (6)
Naval Research Laboratory
Washington, D. 20390
Attention: Library, Code 2029 (ONRL)

Director (6)
Naval Research Laboratory
Washington, D.C. 20390
Attention: Technical Information Division

Office of the Director of Defense (3)
Research and Engineering
Information Office Library
The Pentagon
Washington, D.C. 20301

U.S. Army Research Office (2)
Box CM, Duke Station
Durham, North Carolina 27706

Defense Documentation Center (12)
Cameron Station
Alexandria, Virginia 22314

Director National Bureau of Standards (1)
Attention: Technical Library
Washington, D.C. 20234

Commanding Officer (3)
Office of Naval Research Branch Office
536 South Clark Street
Chicago, Illinois 60605

(3)

San Francisco Area Office
Office of Naval Research
50 Fell Street
San Francisco, California 94102

(1)

Naval Plant Representative
United Technologies Corporation
Pratt & Whitney Aircraft Division
East Hartford, Connecticut 06108

Air Force Office of Scientific Research
Department of the Air Force
Washington, D.C. 20333

(3)

Commanding Officer
Office of Naval Research Branch Office
1030 East Green Street
Pasadena, California 91101

(1)

Office of Naval Research
Branch Office
495 Summer Street
Boston, Massachusetts 02210

(1)

Director
U.S. Army Engineering Research and
Development Laboratories
Fort Belvoir, Virginia 22060

(3)

ODDR&E Advisory Group on Electron Devices
201 Varick Street
New York, New York 10014

(1)

Air Force Weapons Laboratory
Technical Library
Kirtland Air Force Base
Albuquerque, New Mexico 87117

(3)

New York Area Office
Office of Naval Research
207 West 24th Street
New York, New York 10011

Air Force Avionics Laboratory (1)
Air Force Systems Command
Technical Library
Wright-Patterson Air Force Base
Dayton, Ohio 45433

Air Force Cambridge Research Laboratory (1)
L.G. Hanscom Field
Technical Library
Cambridge, Massachusetts 01238

Harry Diamond Laboratories (1)
Technical Library
Connecticut Avenue at Van Ness, N.W.
Washington, D.C.

Naval Air Development Center (1)
Attention: Technical Library
Johnsville
Warminster, Pennsylvania 18974

Naval Weapons Center (1)
Technical Library (Code 753)
China Lake, California 93555

Naval Training Device Center (1)
Technical Library
Orlando, Florida 32813

Naval Research Laboratory (1)
Underwater Sound Reference Division
Technical Library
P.O. Box 8337
Orlando Florida 32806

Navy Underwater Sound Laboratory)
Technical Library
Fort Trumbull
New London, Connecticut 06320

Commandant, Marine Corps (1)
Scientific Advisor (Code AX)
Washington, D.C. 20380

(1)

Naval Ordnance Station
Technical Library
Indian Head, Maryland 20640

(1)

Naval Ship Engineering Center
Philadelphia Division
Technical Library
Philadelphia, Pennsylvania 19112

(1)

Naval Postgraduate School
Technical Library (Code 0212)
Monterey, California 93940

(1)

Naval Missile Center
Technical Library (Code 5632.2)
Point Mugu, California 93010

(1)

Naval Ordnance Station
Technical Library
Louisville, Kentucky 40214

(1)

Naval Oceanographic Office
Technical Library (Code 1640)
Suitland, Maryland 20390

(1)

Naval Explosive Ordnance Disposal Facility
Technical Library
Indian Head, Maryland 20640

(1)

Naval Electronics Laboratory Center
Technical Library
San Diego, California 92152

(1)

Naval Undersea Warfare Center
Technical Library
3202 East Foothill Boulevard
Pasadena, California 91107

(1)

Naval Weapons Laboratory
Technical Library
Dehlgren, Virginia 22448

(1)

Naval Ship Research and Development Center
Central Library (Code L42 and L43)
Washington, D.C. 20007

Naval Ordnance Laboratory White Oak (1)
Technical Library
Silver Spring, Maryland 20910

Naval Avionics Facility (1)
Technical Library
Indianapolis, Indiana 46218

I.H. Pratt (1)
AMSEL-TL-IF
U.S. Army Electronics Command
Fort Monmouth, New Jersey 07703

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Date Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: UTRC R76-921337-19	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): Sputtered Thin Film Research	5. TYPE OF REPORT & PERIOD COVERED: Final Report - Period of 15 Apr 72 - 31 Jan 76
6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s): A. J. Shuskus	8. CONTRACT OR GRANT NUMBER(s): N0014-72-C-0415
9. PERFORMING ORGANIZATION NAME AND ADDRESS: United Technologies Research Center, East Hartford, Connecticut 06108	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: ARPA Order 2173
11. CONTROLLING OFFICE NAME AND ADDRESS: Advanced Projects Agency, 1400 Wilson Blvd., Arlington, Virginia	12. REPORT DATE: Feb 1976
	13. NUMBER OF PAGES: 53
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Department of The Navy, Office of Naval Research, 800 North Quincy Street, Arlington, Virginia 22217	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Reactive sputtering, Strontium Titanate, Tungsten Trioxide, Hafnium Dioxide, Radiation Hardening, Insulated Gate Field Effect Transistors

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report discusses the results of an investigation regarding the potential of the high dielectric constant materials $SrTiO_3$, WO_3 and HfO_2 as alternate gate insulators for radiation hardened insulated gate field effect transistors. The insulators were deposited by rf sputtering. Capacitor structures fabricated with $SrTiO_3$ and WO_3 films did not show adequate stability under bias and temperature stress to be useful gate dielectrics.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE S/N 0102-014-6601

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Date Entered)

409 252

Reactively sputtered hafnium dioxide MIS capacitors exhibited far more stable characteristics with bias and temperature stress, although slow trapping effects were observed at high bias voltages. Hafnium dioxide MIS capacitors irradiated with Co(60) gamma rays to a dose of 10^7 rads showed a high degree of radiation tolerance. Based on these encouraging results, n-channel and p-channel transistors with hafnium dioxide gate insulators were fabricated. The devices exhibit excellent transistor characteristics. For a gate insulator thickness of 1200 Å, and bias voltages of ±6V, threshold voltage shifts in most instances did not exceed |1.5V| for a dose of 10^7 rads. The sense of the radiation induced threshhold voltage shifts observed was not always consistent, although the same process conditions were used to fabricate devices. Further effort is required to achieve a high degree of process reproducibility and control or elimination of the slow trapping effect.