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ELECTRONIC SOLID STATE WIDE ANGLE CAMERA

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Fairchild Space and Defense Systems

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FAIRCHILD SPACE & DEFENSE SYSTEMS
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The objective of this program was to develop a breadboard system to demonstrate the feasibility of a new class of reconnaissance camera, namely, a high resolution, low distortion, ultra-wide angle electronic image sensor matched to the silicon optical response spectrum and having no moving parts. To achieve this objective a prototype lens was developed in parallel with a technique for optically butting

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linear Charge Coupled Devices (CCD). A breadboard scanner/display was fabricated which served to demonstrate the achievement of the objective. Separate lens test results are included in the report.

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This technical report has been reviewed and is approved for publication.

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FOREWORD

This final report was submitted by Fairchild Space and Defense Systems, a Division of Fairchild Camera and Instrument Corporation, 300 Robbins Lane, Syosset, New York, 11791, under Contract F33615-74-C-1109, Project 2004, Task 20040117, with the Air Force Avionics Laboratory, Wright-Patterson AFB, Ohio. James J. Stewart, AFAL/RWI, was the Air Force Project Engineer.

This report was submitted by the authors in April 1975.

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SECTION I

INTRODUCTION

The Electronic Wide Angle Camera System (EWACS) utilizes a solid state airborne reconnaissance sensor. It operates as a strip mode, real-time, electro-optical sensor, with its lens pointing vertically downward. This system scans a line on the ground transverse to the flight path as the vehicle advances. This design is based on the use of two technologically advanced components:

- o A new ultra-wide-angle, high performance lens.
- o Solid state (silicon), charge coupled, linear image sensing arrays.

1.1 OBJECTIVE

The objective of this development program is to demonstrate the feasibility of a solid state wide angle airborne reconnaissance sensor by means of a breadboard system. The program will lead to the development of real time reconnaissance systems. Projected Air Force mission requirements for low cost, wide angle sensors used at low flight altitudes and high speeds will be fulfilled by these systems.

To realize the objective a proprietary lens design was implemented to fabricate a wide angle, low distortion, high resolution lens. This is a new class of lens which provides a set of performance and dimensional characteristics that, until now, have been considered mutually unattainable in a single device. Furthermore, to take full advantage of the capabilities of the lens, a beam splitting technique was devised to permit optically butting Charge Coupled Device (CCD) linear imaging arrays to produce "seamless" pictures.

1.2 SCOPE

The scope of this program is outlined below:

1) Fabricate a lens with the following design goals:

Effective Focal Length (EFL)	1.3 inch
Relative Aperture	f/4
Field-of-View	140° (±70°)
Spectral Range	0.4 - 1.1 microns*
Axial Transmission	80% (T-4.5 nominal)
Relative Illumination	30% at 70°
Distortion	Minimized at ± 60°
Image Quality	40% modulation at 40 lp/mm out to ± 60°
Overall Length	11.35 inches maximum

*Weighted in accordance with silicon CCD response

2) Thoroughly evaluate the lens in a series of laboratory tests.

3) Design and develop a breadboard scanner and display using three CCLID-500 arrays to demonstrate the compatibility of the new lens with the photosensing arrays.

4) Design and develop a beam splitter assembly to optically butt the CCD arrays.

SECTION II

BREADBOARD DESIGN AND FABRICATION

While the prime objective of this program was to manufacture and evaluate the new -ultra-wide-angle lens, another goal was to provide a small laboratory breadboard scanner to:

> Demonstrate the compatibility of the new lens with an array of multiple CCD chips;
>
> Clarify the nature of the solid state sensor and a sampled data optoelectronic system,
>
> Permit Air Force in-house investigations of sensor performance and signal processing.

Such a unit was designed and fabricated as described in the following paragraphs.

2.1 SYSTEM DESCRIPTION

The laboratory breadboard demonstration system consists of two sections as shown in Figures 1 and 2, and in the accompanying block diagram in Figure 3. The sensor unit consists of the EWACS lens mounted in a fixture such that a mirror in front of the lens driven by a servo system can be used to scan a scene at a rate of approximately 1.5 frames per second. A beam-splitting prism, three optically butted 500 element linear CCD arrays (on adjustable mounts with six degrees of freedom) and associated electronics are housed in an assembly at the rear of the lens.

The control and display unit consists of the necessary logic, control functions, video processing, sweep generators and C.R.T. display. Provision is made for connection to a Hughes Scan Converter for single frame storage and subsequent display of the image at 30 frames per second for analysis. A CCD channel selection control permits viewing imagery produced by each of the 500 element CCD's or the last 250 elements and the first 250 elements of adjacent pairs of CCD's. The latter mode permits studying the optical butting.

Details of the sensor and control and display units are presented in the following paragraphs.

2.1.1 Sensor Unit

A simplified schematic - block diagram of the sensor unit is shown in Figure 4 The EWACS lens is mounted with its optic axis vertical and a scanning mirror mounted in front of the lens deflects this axis

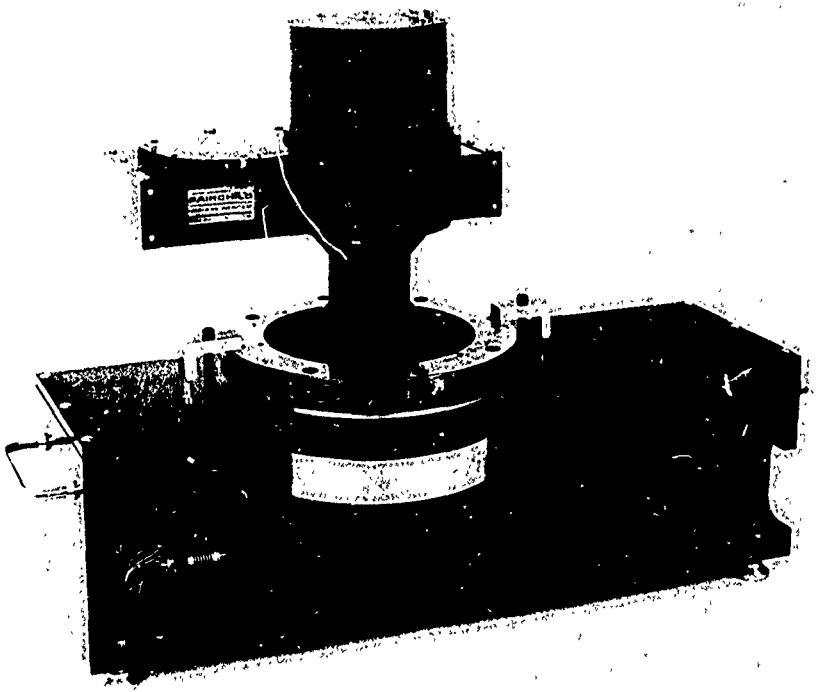


FIGURE 1 EWACS BREADBOARD-SENSOR UNIT

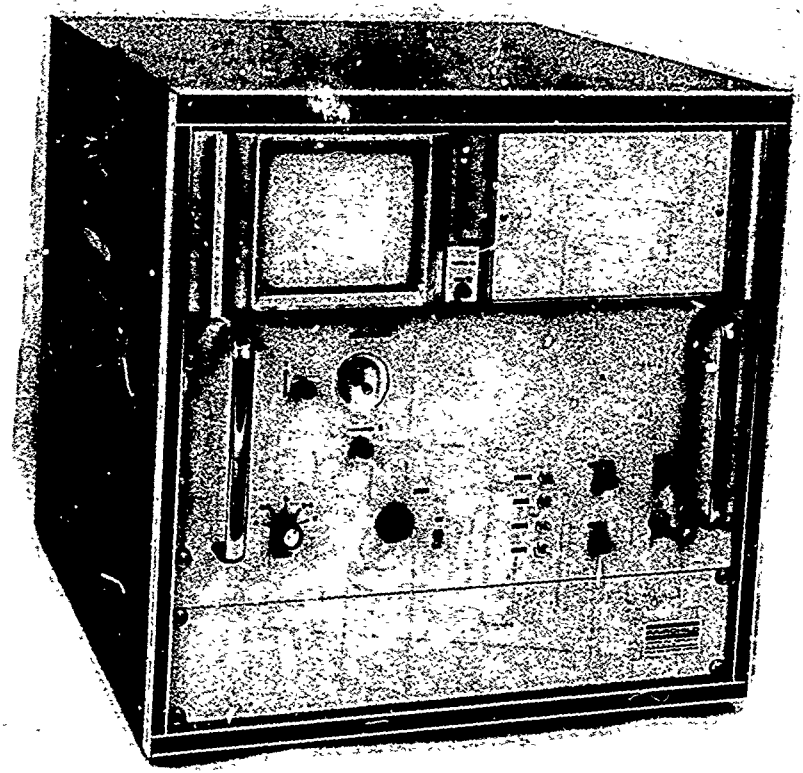


FIGURE 2 EWACS BREADBOARD - CONTROL & DISPLAY UNIT

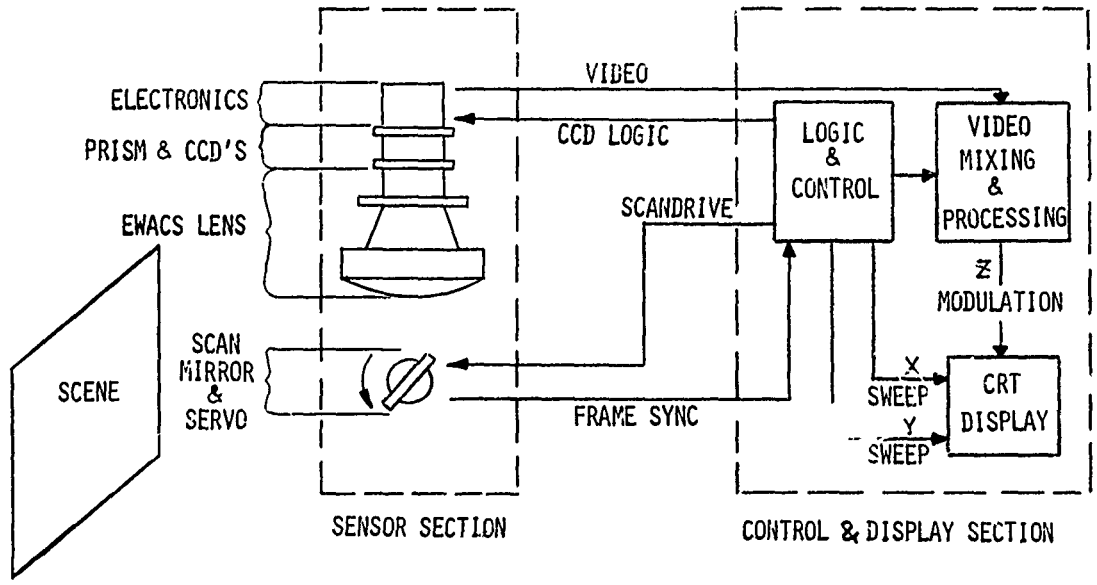


FIGURE 3 SYSTEM BLOCK DIAGRAM

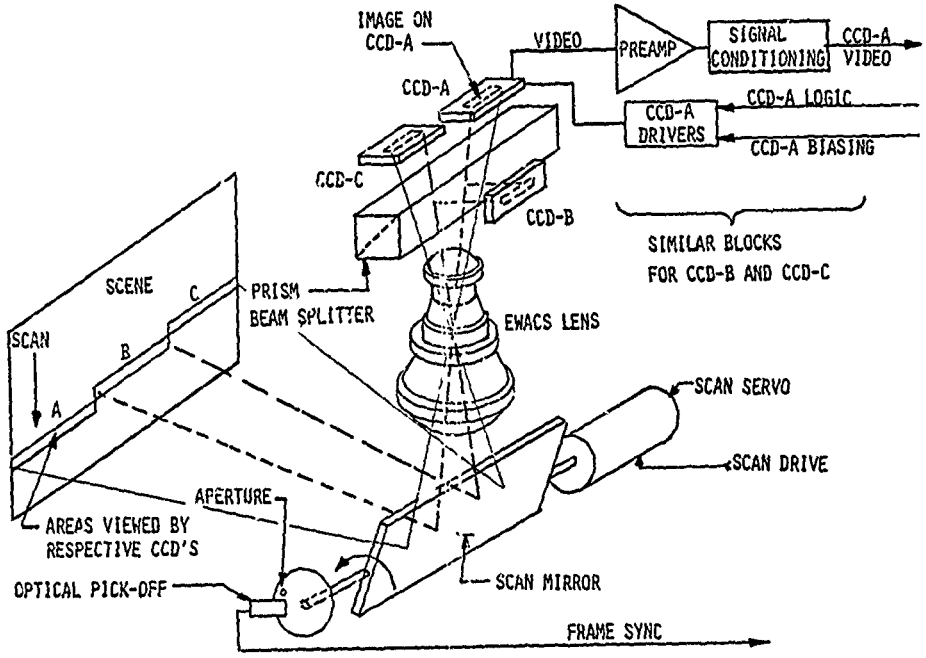


FIGURE 4 SIMPLIFIED SENSOR SECTION CONFIGURATION

to enable scanning a scene from top to bottom. This arrangement was used so that in the laboratory a distance from the lens to the scene of 36 feet could easily be achieved. Such a large distance was dictated by the design of the lens which called for viewing objects virtually at infinity. Objects substantially closer to the lens would have resulted in excessive curvature of the image plane which is not compatible with the flat plane construction of the CCD.

The scan mirror is driven by a servo system with a sawtooth voltage input. Rapid reset of the mirror is accomplished by the step edge of the sawtooth while the ramp provides the slow scan. A portion of the scan time is utilized to let transients settle out and actual video scan and display is initiated by means of an optical pick-off which generates a frame sync signal. The timing of this signal relative to the mirror position is adjusted by rotating the aperture disk about the mirror axis. When the required number of frame lines have been scanned, the step portion of the sawtooth is generated to reset the mirror.

At the rear of the lens, light which emerges from the exit pupil passes through a prism beam splitter and forms two perpendicular image planes as shown in Figure 4. Consecutive CCD's are alternated in these two planes to permit optical butting, since, their construction does not physically permit mechanical butting of the photosensitive elements. Each CCD is cemented to a mounting block which is capable of being adjusted in six degrees of freedom. A printed circuit card is provided as an interface for the CCD terminals and a flexible connecting cable carrying drive signals and bias levels. Video output from the device is carried separately on a sub-miniature coaxial cable.

Clock logic signals and various bias levels for each CCD are derived from the control and display unit and are converted into CCD drive signals by means of the CCD driver card. Video output of the CCD is fed into an AC coupled preamplifier and subsequently into a signal conditioning card. Signal conditioning consists of DC clamping, sample and hold and a line driver to send the video signal to the control and display unit via coaxial cable.

The CCD driver cards and signal conditioning cards are plugged into a hinged printed circuit mother board. Hard wiring connects this mother board to the CCD's and preamps as well as to connectors for the cabling between the sensor and the control and display units. The arrangement is such that when the cover is removed, the cables can be connected and the unit operated with the mother board swung to one side on its hinge so as to gain access to the alignment adjustments for CCD's "A" and "C". Access to the adjustments for CCD "B" is provided through a port in the mounting structure of this entire assembly to the rear of the lens.

2.1.1.1 Description of 1 x 500 CCD Array

The arrays used in this system are the CCLID-500A available now as the CCD101. It is a complex system consisting of an imaging section, a charge transport section and a pre-amplifier, all on one monolithic silicon chip. The array is a three phase, buried P' channel device and its 500 photoelements are positioned on a 1.2 mil pitch dimension. The width of the photo sensitive line of elements is 1.33 mils.

Figure 5 shows the structure of this chip. The photoelements comprise a linear array down the center line of the chip. The individual photoelements are separated from each other by a "channel stop" of serpentine construction. The channel stop surrounds each photoelement on three sides, thus enabling the charge accumulated in the photoelement to transfer only through the unobstructed side. This design enables the use of a common electrode (photogate) for all photoelements. Similarly, a common transfer gate is used for transferring the accumulated photocharges from the photoelement sites to the transport registers. The photogate is constructed of polysilicon, which is essentially transparent to wavelengths within the silicon sensitive range.

An examination of the diagram in Figure 5 shows that the serpentine channel stop forces the charges from adjacent photoelements to be transferred in opposite directions into two vertical transport registers corresponding to the odd and even numbered photoelements. This double register design was primarily chosen for two reasons:

1) The transport register requires three cells for each photoelement. By using two registers, the pitch of the transport register cells is doubled (2/3 that of the photoelement pitch instead of 1/3), thereby easing the compaction requirements of the shift registers.

2) The transfer frequency and the number of transfers in each of the vertical transport registers is halved, thus improving the total transfer efficiency of the CCD array.

The use of two vertical transport registers, however, creates an added complexity -- the need for a horizontal transport register. This register serves as a video combining register. It accepts the signals from both vertical registers simultaneously and forwards them to the preamplifier in succession, thus recombining the two interlaced video streams into a single stream.

The sink diode, surrounding the active area (including the on-chip amplifier), minimizes the migration of stray carriers from the bulk silicon into the active area. The array's active area, excluding the photosensitive

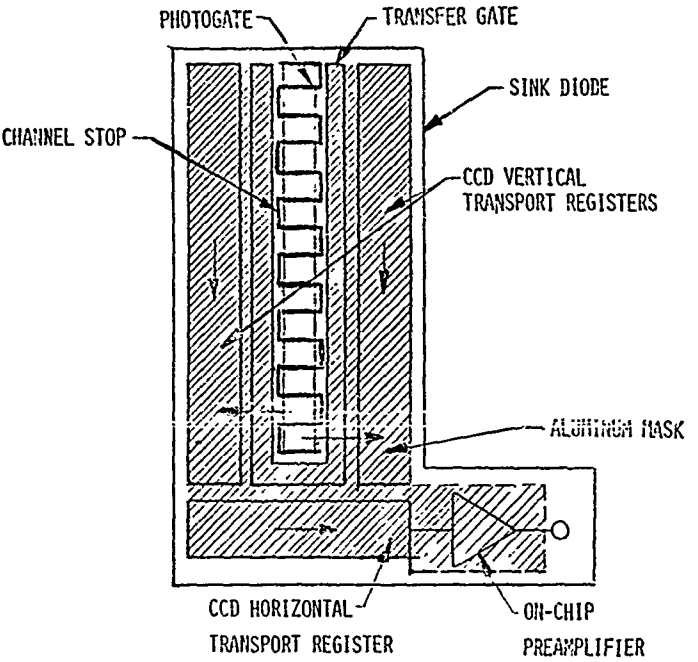


FIGURE 5 CCD LINEAR IMAGING DEVICE

elements, is masked by a layer of aluminum, thus preventing the generation of photocurrents within the transport registers and the amplifier area. Figure 6 is a photomicrograph of the CCLID-500A.

The charges in the CCD array are transported by applying clock pulses to the CCD electrodes in the proper sequence. Figure 7 is a schematic diagram of the device and shows the direction of charge flow from the photoelements to the output preamplifier.

One CCD cycle consists of the following sequence of events:

1) A parallel charge transfer from the photoelements to both odd and even vertical transport registers.

2) A series of transfers, transporting the video down the vertical registers and into the horizontal register.

3) Horizontal transfers and recombination of the vertical register's data into one video stream.

4) Charge to voltage conversion in the on-chip preamplifier.

Figure 8 shows the timing diagram for the CCLID-500A. The line integration time (T_1) consists of one full period of the parallel photo-transfer pulse (Φ_p). The direction of charge flow in the CCD is from a low electrode potential (shallow well) to a high electrode potential (deep well).

The parallel charge transfer from the photoelements to the vertical transport registers occurs when Φ_p goes low (T_2). During this period, the vertical registers are not clocked. Instead, Φ_{V1} is kept at a high potential, allowing the charge to move from the photoelements into the first cell of their corresponding 3-cell register. Since Φ_{V2} and Φ_{V3} are at a low potential, the photocharge will remain under the cells controlled by the Φ_{V1} electrode until the end of the parallel transfer. The parallel transfer gate Φ_x is used to allow charge transfer during the parallel transfer period and to block charge leakage (enable light current integration) from the photoelements during the remainder of the integration time.

At the end of the parallel transfer, the vertical registers are clocked at half the video element rate, and the horizontal register at the full video element rate. When Φ_{V1} is low and Φ_{V2} high, charge is transferred from the first to the second cell of each register element structure. The transfer from the second to the third cell occurs when Φ_{V2} is low and Φ_{V3} is

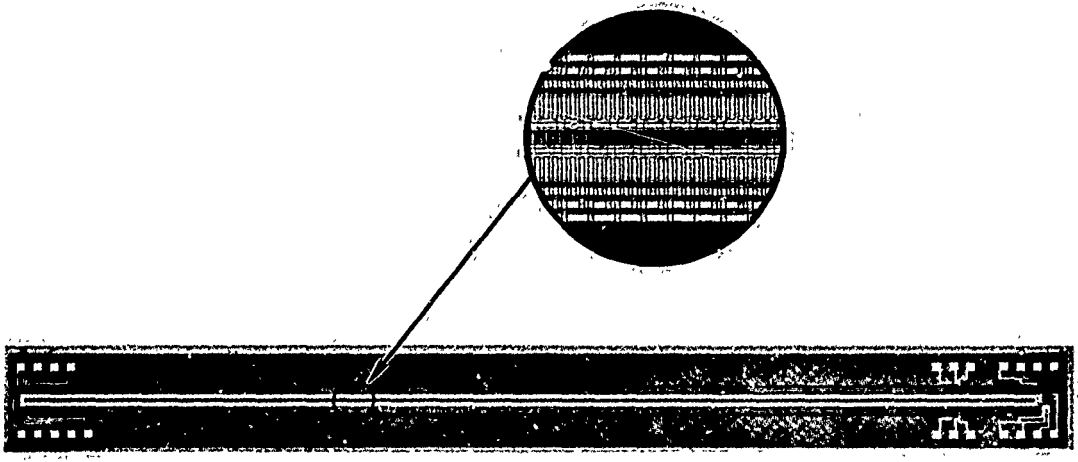


FIGURE 6 PHOTO MICROGRAPH OF CCLID-500A

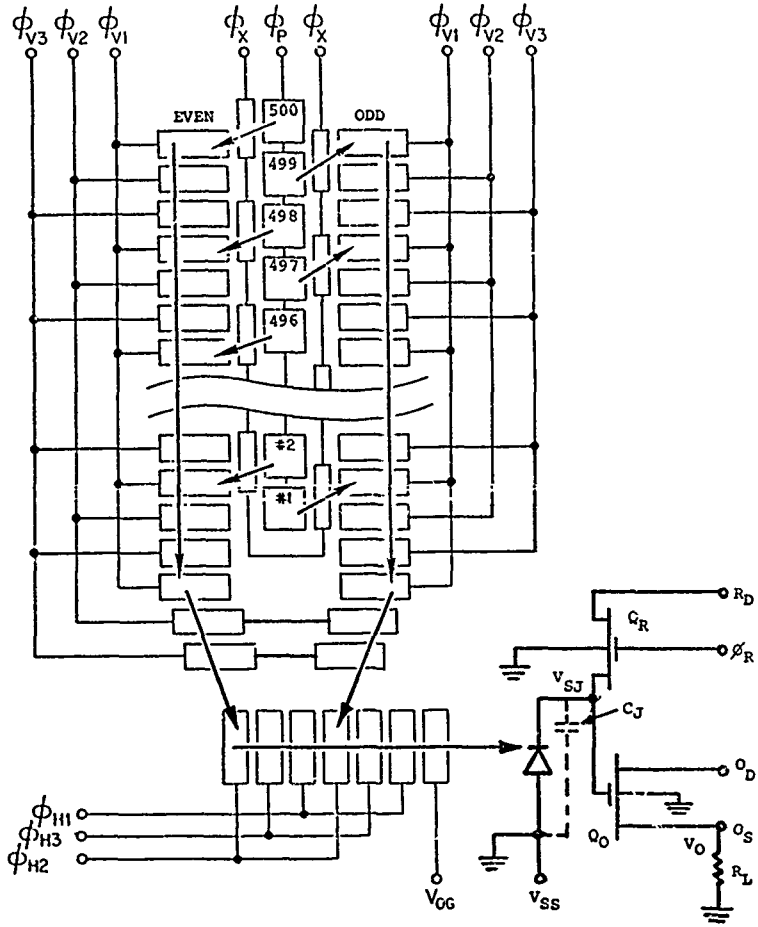
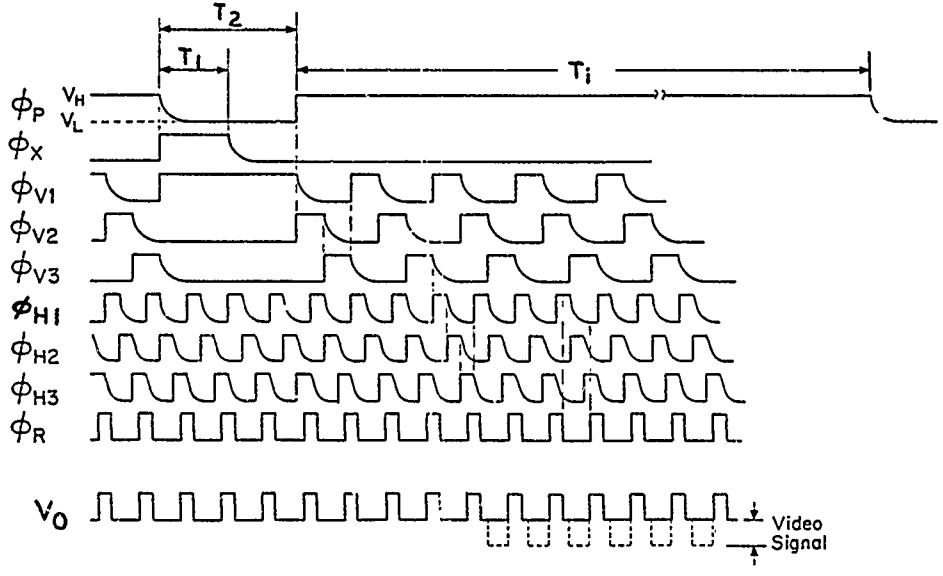


FIGURE 7 SCHEMATIC DIAGRAM OF CCLID-500A



Critical Relations are indicated by —·—·—

FIGURE 8 CLOCKING SEQUENCE FOR CCLID-500A

high. When ϕ_{V3} is low and ϕ_{V1} is high, the charge is transferred from the third cell of one register element to the first cell of the next register element.

At the horizontal combining register, when ϕ_{V3} goes low, the charges are transferred into the horizontal register by virtue of the fact that ϕ_{H2} is high and the other horizontal register wells are blocked by the channel stop. Subsequently, ϕ_{H1}, ϕ_{H2} and ϕ_{H3} transport the charges along this register toward the on-chip output preamplifier.

The falling edge of ϕ_{H1} transports the charge past an output gate (V_{OG}) into a charge detector. The charge detector is a junction capacitor (C_j) in a form of a back biased diode. The threshold voltage on the output gate is adjustable and is set for best array performance.

The on-chip preamplifier is a resettable MOS source follower. The charge transferred into C_j generates a voltage V_{sj} at the gate of the source follower Q_o. A proportional voltage V_o appears across the external load resistor R_L at the source of Q_o. The capacitor C_j is recharged once per element transfer as the reset MOS, Q_R is momentarily turned on with the positive reset pulse, ϕ_R. ϕ_R straddles the trailing edge of ϕ_{H3}. The resulting video signal at V_o is a pulsed video, going negative with increased light signal and resetting to a reference level at the end of each array element signal.

As shown in the timing diagram, the falling edges of the ϕ_V and ϕ_H clocks are sloped. The pulse slopes can be adjusted to peak the transfer efficiency of the device. ϕ_p and ϕ_x do not require a slope. ϕ_R is used to reset the on-chip amplifier and therefore has sharp transitions.

The CCLID-500A is mounted on a ceramic 24-pin dual-in-line package (DIP) (see Figure 9). The package size is 1.250" x 0.600".

Table I lists the pin connections for the CCLID-500A.

2.1.1.2 Electro-Optical Butting of CCD Arrays

Reference to Figure 4 shows the portions of the scene that each CCD sees during one integration time are offset. The amount of the CCD offset in the image plane is just equal to the distance that the scene is scanned during one integration interval. This offset arises from the fact that the CCD generates its video output for a given part of the image after one integration interval. In other words, while video for a given line is coming out, the photosensitive part of the CCD is looking at its portion of the next line in the scene.

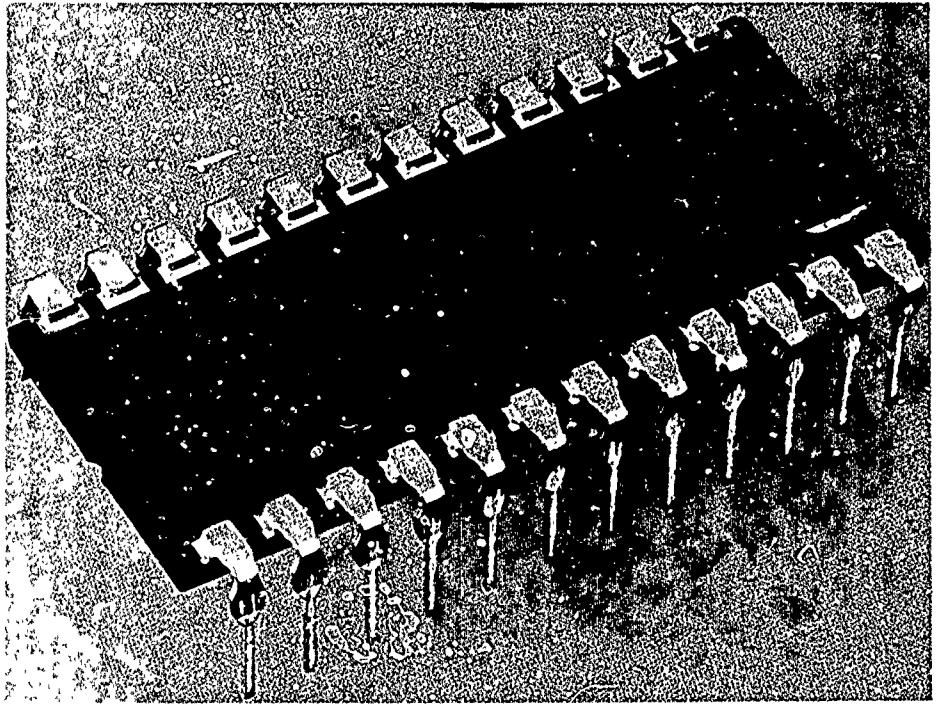


FIGURE 9 PACKAGED CCLID-500A

TABLE I

CCLID-500A (CCD 101) PIN CONNECTIONS

PIN NO.	SIGNAL NAME	DESCRIPTION
1	ϕ_P	Photo-Transfer Pulse
2	ϕ_X	Transfer Gate
3	ϕ_{V1}	Phase 1 Clock — VERTICAL
4	ϕ_{V2}	Phase 2 Clock — REGISTER
5	ϕ_{V3}	Phase 3 Clock — (EVEN)
6	ϕ_{V1}	Same as pin 3 — other end
7	ϕ_{V2}	Same as pin 4 — of clock busses
8	ϕ_{V3}	Same as pin 5 — on chip
9	ϕ_{H3}	Phase 3 clock — HORIZONTAL
10	ϕ_{H2}	Phase 2 clock — COMBINING
11	ϕ_{H1}	Phase 1 clock — REGISTER
12	V_{OG}	Output Gate Bias
13	O_S	Output Transistor Source
14	O_D	Output Transistor Drain
15	R_D	Reset Transistor Drain
16	ϕ_R	Reset Pulse
17	ϕ_{V3}	Phase 3 clock — VERTICAL
18	ϕ_{V2}	Phase 2 clock — REGISTER
19	ϕ_{V1}	Phase 1 clock — (ODD)
20	ϕ_{V3}	Same as pin 17 — other end of
21	ϕ_{V2}	Same as pin 18 — clock busses
22	ϕ_{V1}	Same as pin 19 — on chip
23	ϕ_X	Same as pin 2
24	V_{SS}	Substrate Voltage (Ground)

Consider two adjacent CCD's, say A and B. To avoid an observeable butt in the display of A and B simultaneously, the CCD's have to be arranged optically and electrically so that while A is spewing video for the line it had previously integrated, CCD - B is integrating on that line. When CCD - A is finished with its video, CCD - B starts its video output in phase synchronism with the video of CCD - A so that after mixing, the video stream appears continuous.

If the CCD's had all been arranged to look at adjacent portions of the same line, some sort of memory would have been required so that the parallel video streams could be arranged as a continuous serial stream. Undoubtedly, this memory would have been digital which would have also required D/A and A/D converters.

The electrical timing of the CCD array was arranged for the in the logic of the control and display unit and is described in paragraph 2.1.2.1. Mechanical adjustements are provided for locating the arrays precisely in the image plane. The adjustments permit translation and rotation in the image plane as well as focusing and rotation about a line in the image plane mutually perpendicular to the length of the array and optical axis.

2.1.1.3 CCD Clock Drivers

Each CCD array is driven by its own set of clock drivers on a printed circuit card. All of the drivers except those for ϕ_p and ϕ_x are hybrid circuits as shown schematically in Figure 10.

The clock drivers accept the logic pulses and convert them into the amplitude and shape required for proper CCD operation. The voltage swing and the fall time of the clock pulses can be manually adjusted. This hybrid circuit is a 14 pin flat package 3/8 inches square and is designed to accept inputs at nominal TTL logic levels. The input signal applied to pin 4, is AC coupled to the two transistors. When the input goes high, the NPN transistor is turned on and provides a path between its output pin and the negative supply. Conversely, when the input goes low, the PNP transistor is turned on and a path is provided from the positive supply to the output pin. In normal operation, the capacitive load of the CCD array is connected to pin 13 of the driver.

The three phase structure of the charge coupled register on the array requires a critical adjustment of fall time for the vertical and horizontal clocking signals. The drivers employed in this system provide for individual slope adjustment for each clock. A slope control resistor, R, is connected between pins 13 and 10. Thus, when the CCD is driven high there is a direct path to the positive supply which rapidly charges capacitance C.

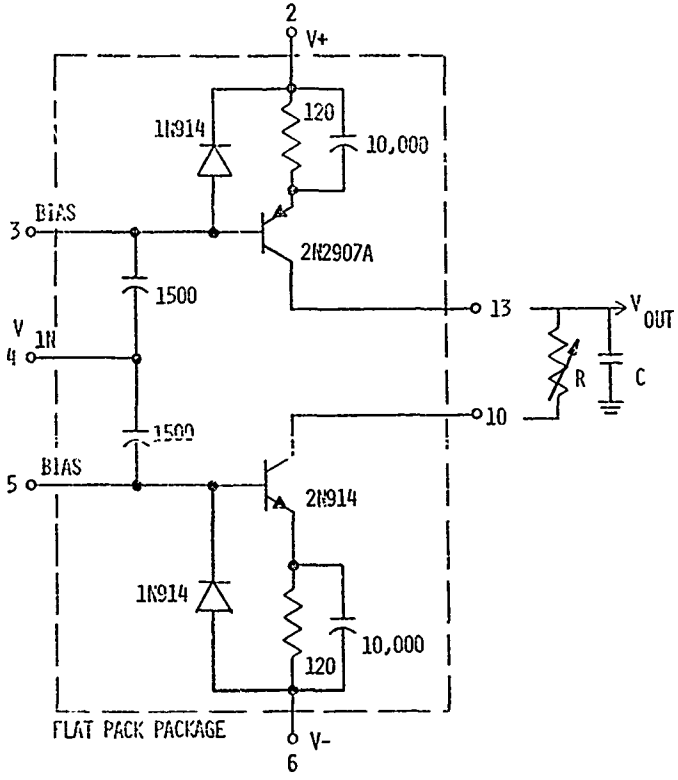


FIGURE 10 HYBRID DRIVER

However, when the CCD is driven low there is a resistance in the path which results in an RC time constant for the falling waveform.

Pins 3 and 5 of the driver are made available for biasing. If pin 3 is returned to the negative supply voltage through a large resistor, the PNP transistor is normally on and the output is normally high except when a positive pulse is applied at the input. Similarly, if pin 5 is returned to the positive supply through a large resistor, the NPN transistor would be on and the output would be normally low.

The voltage swing is adjusted by adjusting the V^+ and V^- voltages for each clocking function at the voltage regulator cards corresponding to a particular CCD. These regulator cards are located in the control and display unit. All of the horizontal and vertical clocks for a given CCD, have common V^+ and common V^- voltages. Six drivers are used thereby permitting individual fall time control for each phase. A separate driver is used for ϕ_R without the RC control of its fall time, (R is made zero by shorting pins 13 and 10). The high and low voltage levels for ϕR are independently adjustable at their respective voltage regulators.

The ϕ_p and ϕ_x clocks are each obtained from half of a commercial driver (SHOO-13). No fall time adjustment is utilized. Separate control of their voltage swings is provided.

2.1.1.4 Video Preamplifier

The video output of each CCD is fed into its respective preamplifier circuit (Figure 11) which consists of an AC coupled non-inverting operational amplifier designed to provide a nominal gain of 40 for video signals. The operational amplifier is a high slew rate, high input impedance, wide-band amplifier that is well-suited for video data handling applications.

Each of the three preamplifier circuit boards is physically mounted near its respective CCD array to decrease noise pick-up. Coaxial cables with grounded shields are also used to increase noise immunity between array and amplifier.

A two thousand ohm resistor is connected between the CCD output and ground to provide the proper loading for the CCD.

2.1.1.5 Signal Conditioning

The signal conditioning section in the video processing chain consists of a DC clamping network, a sample and hold network, and a line driver

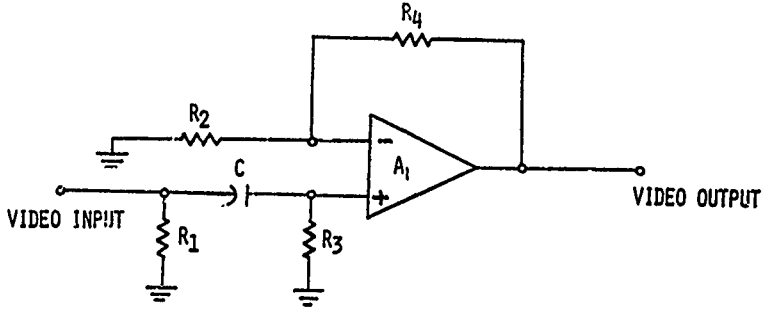


FIGURE 11 VIDEO PREAMPLIFIER

to send the video signal to the control and display unit via coaxial cable. These circuits are located on a printed circuit card for each array and the cards are mounted next to the CCD drivers at the back of the lens.

DC clamping is desired because it restores the DC component to the AC coupled video waveform. The video signal from the preamplifier is clamped using a transistor switch (Figure 12). This switch is controlled by a signal produced in the clamp pulse generator which consists of two monostable multi-vibrators interconnected so that both the pulse width and the position of the pulse (in relation to the video signal) are variable over a selected range. This is accomplished by using external timing components. The clamp pulse generator is triggered on the leading edge of the $\emptyset_{H2}$ logic pulse. As shown in Figure 13, the clamp pulse is adjusted to occur in the reset pedestal thereby clamping the reset pedestal to ground. This serves as the zero reference for the video signal.

A signal sampling and holding operation is performed to eliminate reset noise on the video signal. A commercially available sample and hold module having an ultra fast acquisition time, short aperture time and a wide frequency response as well as a fast output settling time is used. The pulse train controlling the sample and hold is generated in a manner similar to the generation of the clamp pulse. Width and position of the sample pulse are variable over a selected range using external timing components. The sample pulse generator is triggered on the leading edge of the $\emptyset_{H3}$ logic pulse, and is adjusted to sample the video in a stable noise free region of the video signal.

The video signal out of the sample and hold circuit is fed into a high input impedance current amplifier capable of driving the video signal into a 50 ohm coaxial cable. A 47 ohm resistor is connected in series with the output of the current amplifier to provide the correct source impedance for the transmission line. At this stage of video processing the video signal will become more negative with increasing light level.

2.1.1.6 Scanning System

As described in paragraph 2.1.1, a distance of 36 feet was required between the lens and the scene to be scanned. This necessitated the use of a scanning mirror rather than a picture mounted on a rotating drum.

The active CCD sensor length is 0.6 inch which combined with the 1.3 inch focal length, of the EWACS lens gives a horizontal field of view of 26°. A vertical field of view of 26° is required to yield a square 500 element by 500 line display. Thus, the mirror is required to linearly scan 13° for one frame. Clocking of the CCD's is such that one frame (500 lines) takes about 0.4 second. The angular rate for the mirror is therefore 32.5° per second or 5.4 R.P.M.

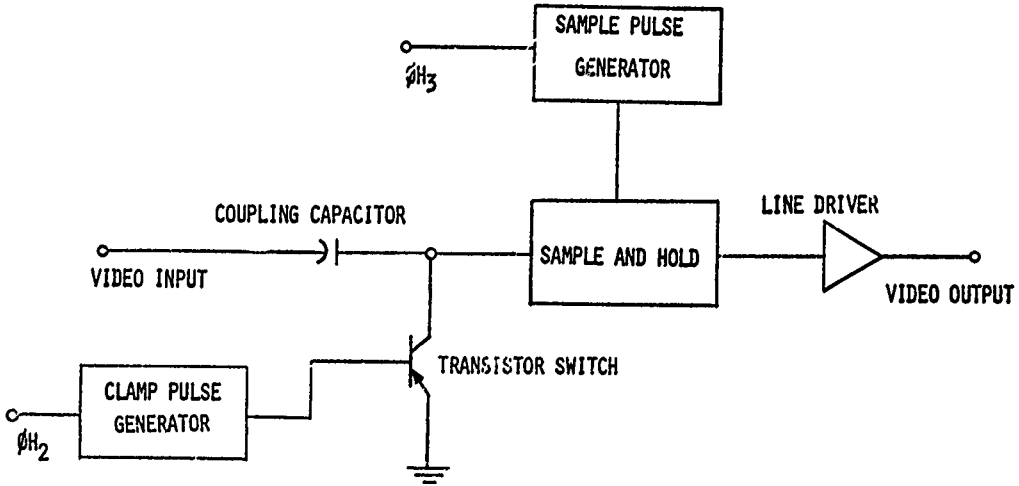


FIGURE 12 SIGNAL CONDITIONING BLOCK DIAGRAM

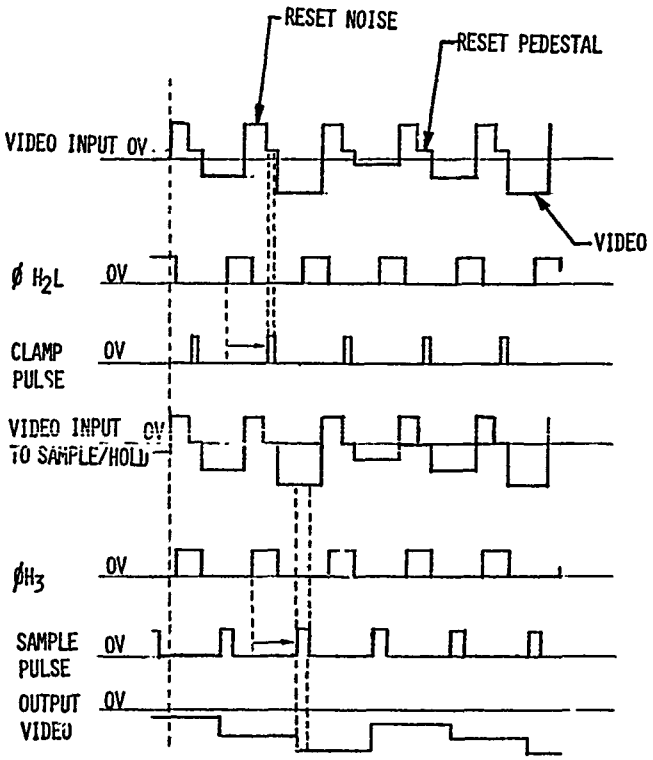


FIGURE 13 SIGNAL CONDITIONING WAVEFORMS

If the mirror were to continuously rotate at this speed, the frame would be displayed in 0.4 second but the repetition rate would be one frame per 11 seconds. A two-sided mirror would double this rate. Of course, a multi-faceted mirror could be utilized to further increase the repetition rate. However, a good optical quality reflecting polygon with sufficient facets to achieve a frame rate between one and two frames per second would have been prohibitive. Instead, a slow scan - fast reset mode of operation for a front surface mirror was chosen.

The scanning mirror consisted of a front surface, aluminized and coated, optically flat glass mounted in a stainless steel beveled frame. This frame was designed so that its weight counter-balanced the mirror weight since the axis of rotation coincides with the front surface of the mirror. The clear aperture of the mirror was one inch by five inches. It was one-quarter inch thick to help maintain its flatness.

2.1.1.6.1 Servo System

Figure 14 is a schematic diagram of the scanning servo system. The sawtooth input voltage from the control and display unit is applied to the non-inverting input of an operational amplifier. Its inverting input is fed the sum of the feedback voltage (mirror position) and the derivative of this voltage (velocity). The output of this op-amp is a voltage proportional to the positional and velocity errors of the mirror as determined by the feedback potentiometer.

The error signals are amplified by the power amplifiers which are arranged in push-pull to provide bipolar drive to the torque motor. A brushless two-pole torque motor was used to drive the mirror. This motor has a peak torque rating of 3.2 oz-in at a peak power of 50 watts. Its continuous ratings are 1.2 oz-in torque and 5 watts dissipation.

Mirror position is determined by means of a plastic film potentiometer connected to the shaft of the mirror frame. The voltage fed back attempts to null the input voltage. A potentiometer is provided to control the gain of the position loop. The mirror has a rather high inertia which tends to make the system oscillatory. Electrical damping is provided through velocity feedback. That is, the feedback voltage proportional to mirror position is differentiated by means of resistor R and capacitance C shown in the figure. Damping is controlled by varying the gain in the velocity loop.

2.1.1.6.2 Frame Scan Synchronization

The servo is driven by a sawtooth voltage from the control and display section. The step of the sawtooth, which resets the mirror, is generated

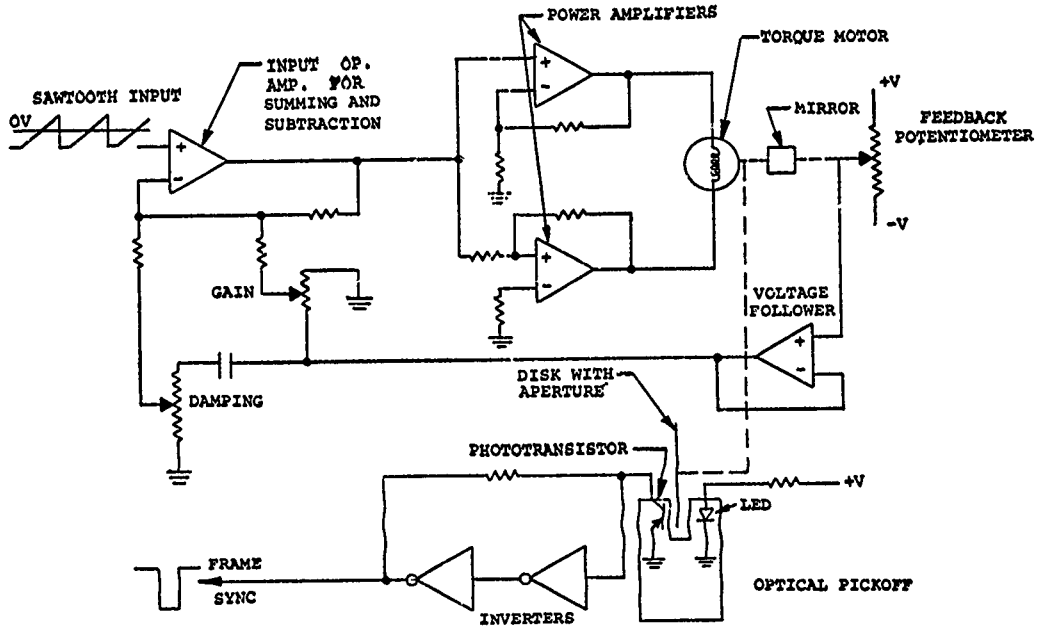


FIGURE 14 SCHEMATIC OF SCANNING SERVO

at the end of the last line of the frame. When the mirror is in the reset position, the optical axis of the system looks approximately 26° above the horizon. About 0.1 second is allowed for resetting the mirror.

As the ramp of the sawtooth begins, the mirror scans so as to move the optical axis toward the horizon. At the end of a 0.2 second interval, the optical axis is looking 13° above the horizon. It is at this point that an optical pick-off generates a frame sync signal. This signal starts the line counter and enables the display of video. At the last line, the optical axis is looking at 13° below the horizon; thus, 26° of the scene is scanned in approximately 0.4 second. The mirror reset step is generated at the end of the last line, and the whole cycle starts over.

The total time for a cycle is 0.7 second, which corresponds to 1.4 frames per second. At this rate, the long persistence phosphor of the CRT permits reasonable visual observation of the display. Furthermore, a total of 0.3 second is allowed to reset the mirror and bring the mirror up to a stable scan speed.

The optical pick-off used to obtain the frame start synchronizing signal consists of an LED source and a phototransistor in a single package arranged so that the light path between the two elements can be interrupted. A disk mounted on the shaft of the mirror frame interrupts the light path, except when a small aperture in this disk rotates into the light path. At this point the synchronizing signal is generated by the phototransistor.

The sync signal is generated twice during a scan cycle, one during the slow scan part of the cycle (this is the proper one) and another when the mirror is reset. A circuit is provided to eliminate the extraneous sync signal. This is accomplished by means of a one shot and gate which is timed to inhibit the sync signal for a period of 0.15 second after the mirror reset step of the input sawtooth. The proper sync signal occurs about 0.3 second after the reset step.

2.1.2 Control Electronics

The logic and control electronics are located in the control and display unit shown in Figure 2. Figure 15 is a simplified block diagram of the logic and control functions.

2.1.2.1 Logic

The logic section is packaged on a wirewrap board that can be divided into several parts according to function:

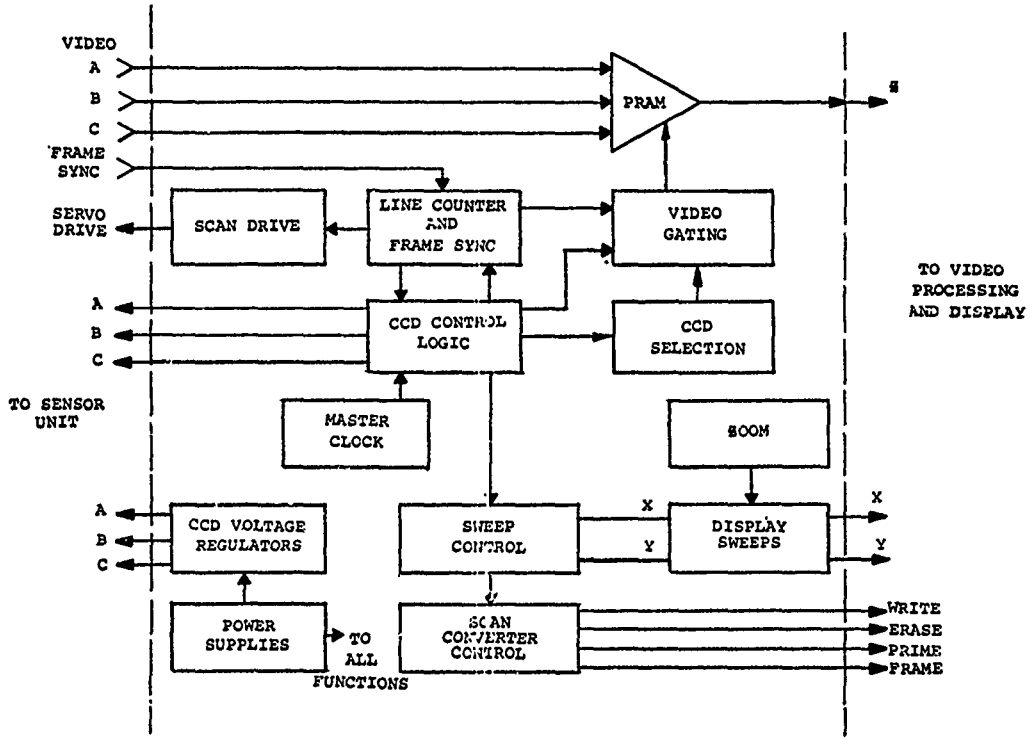


FIGURE 15 LOGIC AND CONTROL BLOCK DIAGRAM

1) Master clock

2) Line counter and frame synchronization logic

3) Control logic for CCD's

4) Control logic for sweep generators

5) Control logic for video gating and processing

The master clock is a crystal oscillator operating at a frequency of 15 megahertz. This master clock is applied to a counter that divides the frequency by a factor of 7 down to 2.14 megahertz.

The 2.14 megahertz clock is fed directly to a shift register configured to divide by 3 to generate the three-phase 714 kilohertz clocks for the CCD analog output registers (ϕ_{H1}, ϕ_{H2}, ϕ_{H3}). It is also sent through a divide-by-two flip-flop to a similar shift register which gives the three-phase vertical transfer clocks (ϕ_{V1}, ϕ_{V2}, ϕ_{V3}) at a frequency of 357 kilohertz. The ϕ_{H2} clock is used to trigger two monostable circuits to provide a reset pulse train. Provision is made to vary the reset pulse width and location relative to the ϕ_{H2} pulse.

The staggered photogate clocks and transfer gate clocks are generated by pairs of synchronous counters, one-of-ten decoders and set/reset latches. ϕ_{V2} clocks the counters and their decoded outputs set and reset the latches to provide the photogate and transfer gate clocks. The photogate clock for each array gates its respective vertical clock to produce the correct vertical analog transfer register clock.

The logic waveforms controlling the horizontal sweep circuit for the different arrays are generated in the same manner as the photogate clocks.

The line counter and frame synchronization logic consists of a set-reset flip-flop and four synchronous divide-by-sixteen counters. A "Clock On" signal at the output of the flip-flop will enable most of the integrated circuits on the wirewrap board to function in their normal operating mode. This occurs when the Frame Start signal from the optical pick-off is received at the reset terminal of the flip-flop. The Frame Start signal also enables the four synchronous counters to count 504 lines. After 504 lines the flip-flop sets and disables the integrated circuits until another Frame Start pulse arrives. The reset pulse train and analog output register clocks are always being produced.

Synchronous counters, decoders and latches are utilized to produce the logic required for video gating and video processing.

2.1.2.2 Video Gating

The three video signals arriving at the control and display unit from the sensor unit must be mixed and gated. The manner in which they are mixed is determined by the position of the CCD Select knob on the control panel.

A four channel programmable amplifier is used in the video gating circuitry. It is an operational amplifier with four identical input stages, any one of which may be electronically connected to the single output stage. The "On" channel is selected through TTL compatible address inputs. By turning the CCD Select knob to the desired video output mode, the proper logic signals will be routed to the address input to select the desired video input channel.

2.1.2.3 Display Sweep Control

The display sweeps to the monitor are generated from the circuitry on the copper clad board in the control and display unit. The circuit is an integrator whose output is a linear positive ramp. Both the horizontal and vertical sweeps are identical except for different component values.

A super beta operational amplifier with extremely low offset and bias currents is connected to function as an integrator. A reset transistor is connected across the integrating capacitor in the feedback loop. The integrator is controlled by a pulse train gated through a multiplexer to the base of the reset transistor. When the pulse is positive, the transistor saturates and discharges the integrating capacitor so that the output voltage drops rapidly to the reference potential. The reference potential (-0.6 volts) is obtained by means of a forward biased diode which clamps the noninverting input of the operational amplifier.

A constant current is fed to the inverting input of the amplifier which charges the integrating capacitor whenever the reset pulse train is low. The output of the integrator is a voltage increasing linearly with time. Both the horizontal and vertical deflection voltages are produced this way and differ only in the slopes of their respective ramps. Their amplitudes are nominally one volt and can be varied by means of a potentiometer which varies the charging current.

2.1.2.4 Scan Control

The sawtooth signal necessary to properly drive the servo mirror scanner is generated in a manner similar to that of the display sweeps described in the previous paragraph. In this case, however, the positive

reset pulse is the output of a one-shot whose width is variable. At the end of a frame the "Clock On" logic signal goes low and triggers the one-shot which resets the integrator.

When the one-shot recovers, the ramp is initiated by a constant current fed into the inverting input of the amplifier. The magnitude of this current controls the angular velocity of the mirror since it controls the output rate of the ramp. The amplitude of the ramp (0.75 volt) determines the range of deflection of the scanning mirror from its reference position. This reference position can be varied by means of the DC voltage applied to the non-inverting input of the amplifier which is variable between ±0.7 volts. A normally open pushbutton switch is connected across the integrating capacitor. When the switch is closed the output will go to the reference potential and the mirror will stop scanning. This switch is mounted inside the control chassis and is used to set up the servo system.

On the same circuit board, another one-shot, triggered by the "Clock On" low going logic signal is used to produce a sync inhibit pulse. This pulse, when gated withthe Frame Sync from the optical pick-off inhibits the spurious Frame Sync pulse generated during mirror retrace. During one frame of video, the sync inhibit pulse width is adjusted so that the mirror can be brought up to steady state scan speed and only the Frame Sync pulse generated during the normal mirror scan is permitted to activate the logic system.

2.1.2.5 Zoom Control

A variable 1x to 5x zoom of the picture on the display monitor is achieved at the flip of a switch. This provides expansion of the array readout, by displaying a portion of the array over the full width of the display. That is, with an expansion of 5 times 100 elements of each 500 element array are displayed. In this case, the display resolution is essentially limited by the CCD resolution.

When the front panel switch is in the "ZOOM" position, the non-inverting inputs to the operational amplifiers in the sweep circuitry are connected to one end of the zoom gain potentiometer. By turning the potentiometer clockwise, the horizontal and vertical sweep ramps will have a greater amplitude than they had in the normal sweep mode for the same line and frame time. Thus, a proportionately smaller part of the picture fills the display raster. A joy stick with X and Y trim potentiometers on the front panel of the cabinet delays the start of the horizontal and vertical sweeps in the magnified picture. This determines the part of the picture that is presented on the display.

2.1.2.6 Provision For Scan Converter

The EWACS breadboard has a frame scan time of 0.7 seconds. This relatively long scan time was dictated by the 500 x 500 element format of the picture and the 0.79 millisecond integration time.

At this frame rate, a real time display of video becomes difficult to observe due to the length of time between updates. This manifests itself in an inordinate amount of flicker, unless a long persistence phosphor is used, and, even then, the presentation suffers somewhat due to image smearing. In order to handle this type of video information, some means of frame storage must be employed.

It is therefore suggested that the EWACS System be interfaced with a commercially available scan converter. This would permit the user to obtain the full advantage of the breadboard's performance capabilities.

The system is designed to interface with the Hughes 639 Scan Converter. The display can be the Tektronix 604 or any standard or high resolution TV monitor.

The controlling logic signals to the scan converter have been incorporated into the logic and control electronics.

The control functions provided are:

- o FRAME
- o Erase
- o Prime
- o Write

The X and Y sweep ramps to the 639 Scan Converter together with the appropriate control signal voltages and timing sequences are capable of generating a 'single frame' picture with a "FRAME" command available as a front panel pushbutton. In addition, individual front panel controls for "Write", "Erase" and "Prime" are also provided to add flexibility to the system.

The existing sweep circuit will interface with the scan converter with no further modifications.

2.1.2.7 Power Supplies

Regulated power supplies are employed to convert the 120 volt AC line to the necessary DC voltages. The following voltages are bussed through the system:

+24 Volts

Supplies power to three positive voltage regulator boards. Each board has six precision voltage regulators supplying the positive bias voltages to the CCD arrays and to the array drivers.

-5 Volts

Used to supply the offset bias voltage to the positive regulators, and provide any necessary negative bias voltages.

-15 Volts

Supplies the input to 3 negative regulator boards which furnish the negative voltage levels to the CCD array drivers.

+5 Volts

All the logic circuits in the EWACS System are powered by this supply.

±15 Volts

All operational amplifiers, sample and hold circuits, linear integrated circuits and bias networks are powered by this supply.

± 30 Volts

Supplies the power amplifiers used to drive the scanning mirror motor.

2.1.3 Video Processing and Display

To achieve the objectives of this program, it was necessary to select three arrays having similar electro-optical characteristics. During the preliminary testing and selection of the CCD arrays, it was found that the arrays

exhibited slightly different sensitivities and saturation levels. To overcome this difficulty the three video channels in the video gate were provided with variable independent gain and DC offset adjustments. To obtain high resolution pictures with a good grey scale the composite signal from the video gate was fed through a video processing network with horizontal aperture and gamma correction circuitry. Gamma correction is adjustable to match the CRT display.

2.1.3.1 Video Channel Matching

The programmable amplifier (PRAM) used for video gating as described in section 2.1.2.2, has four independent inputs. Three of them were used for the CCD video streams while the fourth had a variable DC input which was used to establish a blanking level between video lines and frames.

The coaxial cables carrying the video for each array from the sensor unit were terminated with 51 ohm resistors and connected to the non-inverting PRAM inputs. Independent feedback loops were provided from the PRAM output to its inverting inputs so that the gain of each channel could be adjusted by means of a potentiometer. Furthermore, the low end of each inverting input resistor was connected to a variable DC source to control the DC offset of each channel.

It was necessary to use the non-inverting configuration of the PRAM to prevent channel crosstalk through the feedback loops. Since the horizontal aperture and gamma correction circuitry were configured to work with positive inputs a unity gain inverter, fed through a potentiometer, was used at the output of the PRAM. This control serves to independently adjust the composite video input to the horizontal and gamma correction circuitry after the gain and DC offset of each channel are adjusted to achieve the best picture on the display monitor.

Gain and DC level adjustments are necessary in matching the three video signals. The DC level determines the brightness of the picture while the gain determines the contrast. Each channel has a gain adjustment from 2x to 9x while the DC offset can be varied over a range of several volts above ground.

2.1.3.2 Horizontal Aperture Correction

The signal from the video gate is fed into a "phaseless" aperture correction circuit employing a delay-line as shown in Figure 16. This circuit applies amplitude enchancement to that part of the video signal that constitutes the fine details of the picture, that is, the high frequency

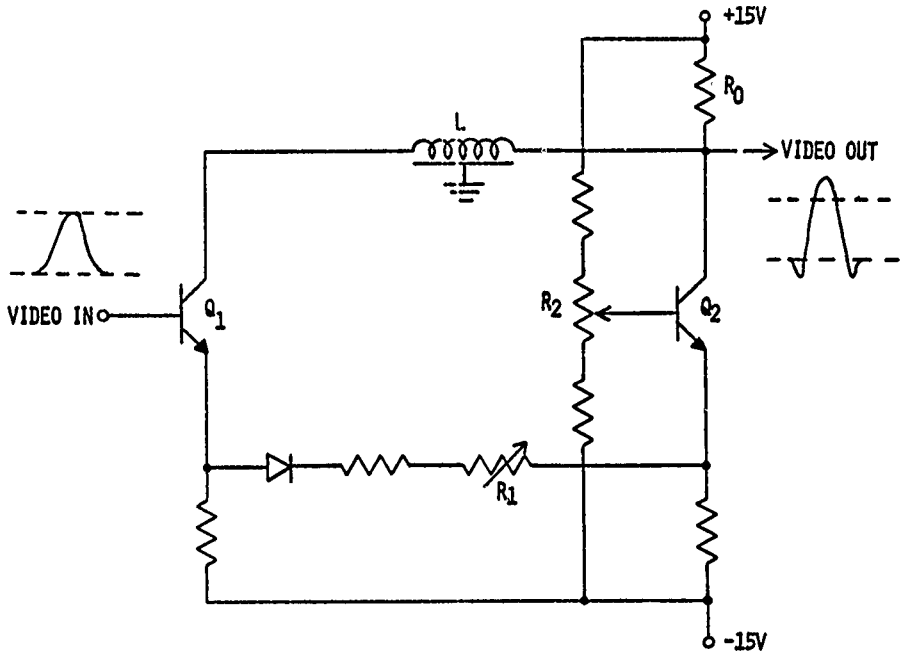


FIGURE 16
SIMPLIFIED SCHEMATIC OF HORIZONTAL APERTURE CORRECTION CIRCUIT

elements. The delay-line, L, has its sending end open by virtue of its connection to the collector of transistor Q_1 which has a high impedance. Its receiving end is terminated in its characteristic impedance by resistor Ro which is the load resistor in the collector circuit of transistor Q_2.

The input signal is divided into two parts: the delayed signal across Ro via the collector of Q_1 and the delay line, and the undelayed signal via the emitter of Q_1 and the collector of Q_2. This undelayed signal is of reverse polarity at the output and is anticipatory in effect. Furthermore, the undelayed component goes down the line and reflects from the "open" end of the line. The reflection arrives at Ro doubly delayed and still of reverse polarity, thus serving as a following overshoot on the falling edge of the delayed component via Q_1 and L. This results in symmetrical aperture correction as shown by the input and output waveforms.

Potentiometer, R_1, serves to adjust the ratio of main signal current to aperture-correction current. The gain of this circuit is near unity for low frequencies. Potentiometer, R_2, controls the threshold at which aperture correction is allowed to take place so that high frequency noise is not emphasized.

2.1.3.3 Gamma Correction

An important property of a cathode ray tube (CRT) is its brightness-transfer characteristic. The brightness of a CRT display can by approximated by:

$$B = K V^{\gamma}$$

where

B = display brightness

V = grid voltage (relative to cut-off)

K = a constant

γ = display gamma (experimentally determined constant)

For the CRT used in the EWACS System, the gamma was determined to be about 3.8. This means that the brightness-transfer characteristic is very non-linear and it will compress black levels and stretch white levels for a scene.

The output-transfer characteristic for the CCD exhibits a gamma typically about 0.9 to 0.95 hence they can be considered essentially linear. Gamma correction was incorporated to compensate for the non-linear brightness transfer function of the display monitor which has a gamma of 3.8. Figure 17 shows a simplified schematic of the gamma correction circuit.

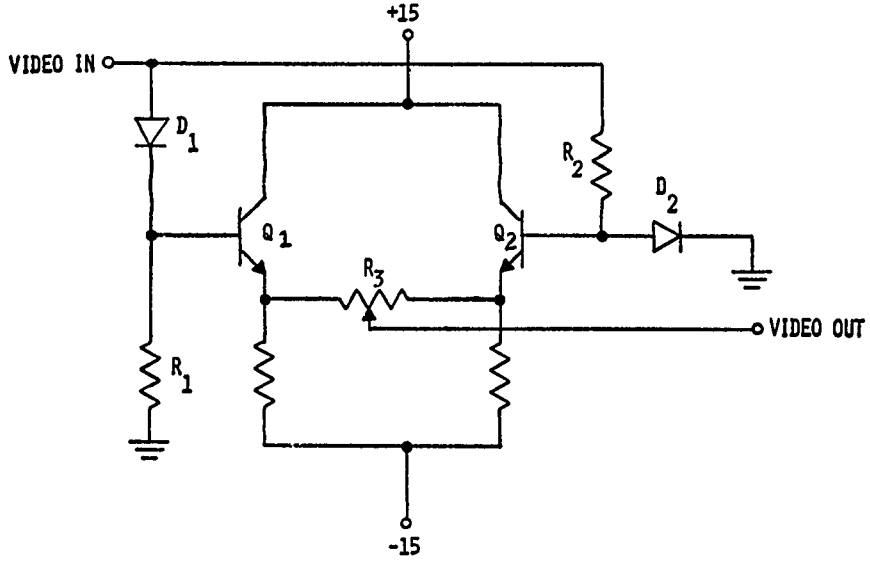


FIGURE 17 SIMPLIFIED SCHEMATIC OF GAMMA CORRECTION CIRCUIT

The circuit consists of two transistors Q_1 and Q_2 with the video applied in parallel to both bases. The response at the emitter of Q_1 is non-linear because of the variable conductance of diode D_1 and load resistor R_1. The response of Q_1 is such that a gamma greater than unit is obtained (whites are stretched). This occurs because the conduction of D_1 increases non-linearly as the signal voltage increases thus driving Q_1 harder. However, the response at the emitter of Q_2 is non-linear in the opposite sense, that is, the gamma is less than unity. This occurs because more of the signal voltage is dropped across resistor R_2 as the conductance of diode D_2 increases thus reducing the drive to transistor Q_2. In this case the black levels are stretched.

Outputs of both transistors are applied to opposite ends of potentiometer R_3, the GAMMA control. When the arm of the potentiometer is nearest Q_2 the video output signal is influenced primarily by the low gamma response of Q_2 which for this circuit corresponds to a gamma of 0.15. When the control arm is near Q_1 a high gamma is exhibited approaching 8. Any gamma between these two values can be selected by means of this control.

The overall system gamma is the product of the individual gamma of the sub-systems. To make the system linear in terms of its output-input transfer characteristic the control is adjusted to obtain an overall gamma of unity. In this case the gamma selected would be approximately $\frac{1}{(0.9)\ (3.8)}$ or 0.29. Note that it may be desireable to use a different gamma to enhance certain types of scenes being viewed.

2.1.3.4 Display

The Tektronix 604 monitor was selected to display the composite video signal because of its capabilities and size. The monitor has 6-1/2 inch flat-faced rectangular cathode-ray tube with long persistence phosphor. It is rack mounted in the control and display unit cabinet. Positive signals into the vertical and horizontal deflection amplifiers will deflect the electron beam upward and to the right respectively. One volt is required for full deflection along either axis. A front panel control is provided for adjusting the raster position.

A linear Z axis amplifier permits intensity modulation of the writing beam; a positive signal increases intensity with one volt required to produce maximum intensity. Brightness of the display is varied by means of an intensity control in the front panel of the monitor. Display contrast is adjusted by means of a front panel control that varies the gain of a video amplification stage in the control unit.

2.2 OPTICAL SYSTEM

This section of the report details the design and manufacture of the optics for the Electronic Wide Angle Camera System. Major components in the optical system are:

- An ultra-wide-angle lens
- Camera Back
- Optical butting assembly

Design and fabrication of these units are described in the following paragraphs.

2.2.1 Ultra-Wide-Angle-Lens

The unique design of this optical system provides a class of lens having a set of performance and dimensional characteristics that, until now, have been considered mutually unattainable in a single device. Paragraph 1.2.1) summarizes lens design goals. Figure 18 is a photograph of the prototype lens. The relatively compact overall length of this lens has been achieved by incorporating a severe elliptical curve on the second surface of the first element.

2.2.1.1 Optical Design

The lens is essentially a wide angle, inverted telephoto system designed to have low distortion and low chromatic residuals over a broad spectral region encompassing the visible and near-infrared regions. As shown in Figure 19, the second surface of the lens is aspheric. This surface simultaneously provides correction of astigmatism and distortion, free of zonal residuals, permitting an excellent degree of correction to be obtained at all field angles. The use of negative exterior elements provides both lower distortion and, through pupil enlargement, major compensation for the normal $\cos^4$ fall-off in illumination with field angle is achieved. These figures are a combination of concepts introduced by Hugues, E. (Jap. Jour. Applied Physics, 4, Suppl. I, 1965, p. 57) and Slussareff, G. (J. Physics U.S.S.R., 4 p. 557). The optical design of this objective was entirely under Fairchild's sponsorship, with the program effort covering the fabrication and testing of the prototype.

2.2.1.2 Mechanical Design

Figure 20 illustrates the lens mount design.

The basic design philosophy was to provide a simple stable mechanical mount allowing relatively easy component alignment, consistent with the

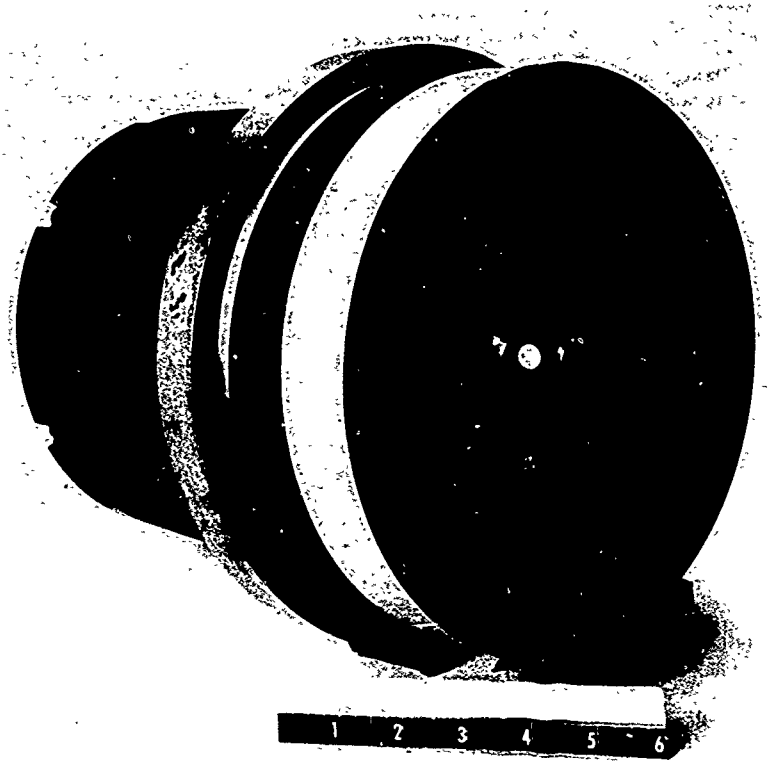


FIGURE 18 PROTOTYPE - WIDE ANGLE LENS

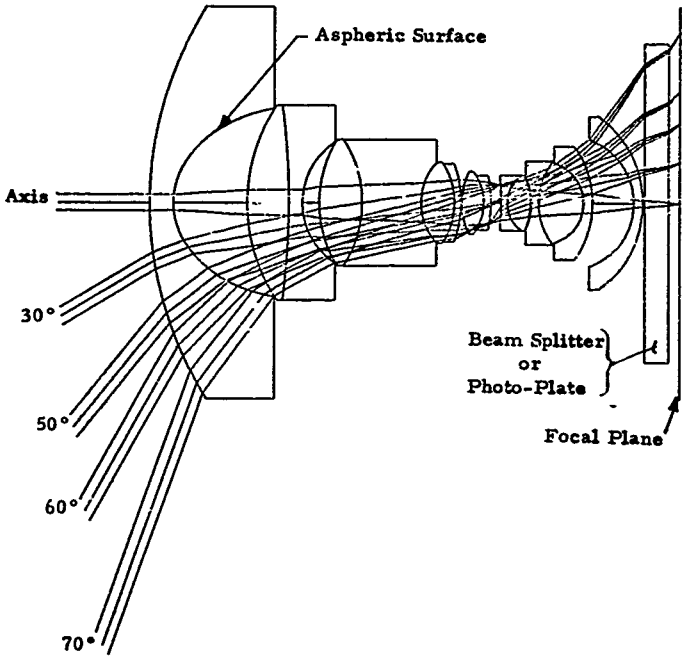


FIGURE 19 RAY TRACE OF EWAC LENS

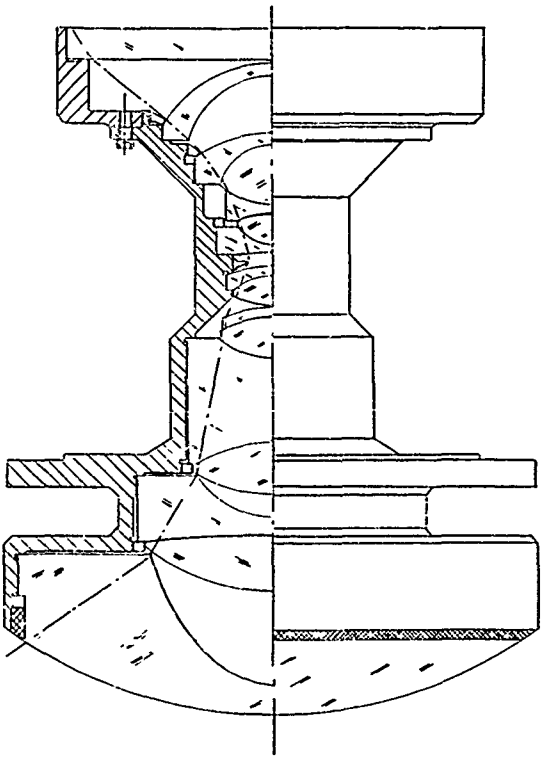


FIGURE 20 EWAC LENS MOUNT DESIGN

tolerance analysis, and insuring a high degree of confidence in the spatial location of lens elements. To satisfy these conditions a one-piece cast aluminum barrel was developed. Cast aluminum was chosen for stability, machinability and compatibility with laboratory conditions under which the lens is to be used.

Design features of the mount are:

1) A one-piece mount allowing good control over concentricity and parallelism of seating surfaces.

2) Narrow seats minimize the chance for locally uneven pressure. Retaining rings are designed to exert mainly axial thrust with little radial thrust components. These features avoid strains in the glass which could destroy the image as a result of bi-refringence.

3) All mounting seats are flat with the exception of element 9, to provide greater accuracy and repeatability.

4) As a result of the extremely tight centering tolerance requirements in the vicinity of the stop, element 9 is mounted on a radius shoulder. It is lapped to control centering between elements 9 and 10 to a tolerance less than fifty microinches. When element 9 is seated, it will automatically center itself with respect to element 10.

5) Mounting shoulders on elements are narrow to permit smaller clearances, thereby avoiding binding upon assembly.

6) Adequate clearance is provided around cemented components, thus avoiding strain, binding in assembly or potential damage under vibration. This also permits centering of finished elements without concern for clearances.

2.2.1.3 Fabrication

Owing to the unusual nature of this lens and the relatively short time span allotted for manufacturing and testing, a step-by-step manufacturing plan was established. Major phases of this plan are:

- An in-depth error and trade-off analysis
- Formulation of a processing strategy
- Lens manufacture

2.2.1.3.1 Error and Trade-off Analysis

The in-depth error and trade-off study was performed to establish the tolerances and a processing strategy for lens manufacture. The study first identified error sources contributing to a loss in quality and then evaluated their effects one by one.

Error sources were grouped by constructional parameters and local faults.

- Constructional parameters:

  1. Index and dispersion departure from catalog values
  2. Regular departures in surface shape
  3. Departures from specified thickness and separations.

- Local faults

  4. Inhomogeneity of material
  5. Irregularity of surface
  6. Decentration of components
  7. Decentration in mount

Constructional parameters are compensable. This lens being in the realm of a state-of-the-art development represents the highest achievable limits on performance. This consideration requires that most of the errors resulting from constructional parameters be compensated.

Compensable errors in the normal constructional parameters can, presumably, be corrected by changes in other constructional parameters. These corrections are made by re-optimizing with the measured errors applied. It is essential that tolerances be used which, in the worst case, are capable of being compensated only by changes in the dimensions remaining to be fixed. Thus the first step of any compensation strategy has many parameters available for compensation while the last step has none. It is, therefore, critical to determine the nature of the last step first and to insure that each preceding step has not accumulated an error effect large enough to prevent compensation to an acceptable level of performance. This has been done, using worst case analyses of each step. The acceptable level of performance criteria for each step of compensation was processed much closer to the nominal design performance than the budgeted departure for non-compensated errors.

Non-compensable errors are those which are local faults as listed above. Since these errors tend to be of a statistical nature, they are treated as RMS errors in the wavefront. Budgets for these degradations were established by setting an acceptable Modulation Transfer Function (MTF) degradation factor and converting this, by established procedures, into the total allowable RMS error.

The performance specification for this lens, over most of its field, is an MTF response of 50% at 40 c/mm. This is at 12.5% of the diffraction cutoff for a lens of this aperture and wavelength response. The ideal lens just meets this specification at a field angle of 50 degrees and exceeds it at smaller angles. Accepting a degradation of MTF to .8 or 40% response at 40 c/mm, the allowable budget becomes .125 waves of RMS error from all sources.

Tolerance budgets were established after analysis of compensatable and non-compensatable errors together with extensive calculation and review of:

- Worst case analyses,
- Smallest practical limits on tolerances,
- Sensitivity tables on thickness, separations, curvatures, indices, tilts and displacements,
- Possible processing strategies,
- Mount design.

As a result of this study, tables were established providing manufacturing tolerances for: radii, aspheric constants, component thicknesses, tilt sensitivities, and surface power and irregularities. These will be discussed in later paragraphs.

The tolerancing effort also indicated a processing procedure guaranteeing that compensable errors would be held to values which could be almost completely compensated in later re-optimization steps, and hold the degradation of non-compensable errors to an acceptable level. This final approach did require application of a few tolerances such as those on aspheric constants, centration of components adjacent to the stops and overall thickness of the quadruplets, to border on the practical limits of fabrication. Previous experience in fabrication techniques made attaining these tolerances possible.

2.2.1.3.2 Processing Strategy - Compensable Errors

As previously discussed, the processing strategy must systematically remove effects of errors resulting from constructional parameters. The

following list summarizes the final step by step procedure which was used to ensure these results:

1. Order glass, requesting melt sheets with measurements out to 1014 mu,
2. Recompute for melt indices variations,
3. Fabricate or fit the required curves to existing test glasses,
4. Recompute lens to measured test glass data,
5. Fabricate aspheric and spherical elements to tolerances specified. Do not complete the first surface of the last element, leaving it for final compensation of residual errors,
6. Measure deviation of aspheric constants and center thickness of all elements,
7. Assemble cemented components to specified tolerances and measure assembled center thickness,
8. Recompute for aspheric deviation and measured center thickness, changing the next to last curve as necessary, and generate final machining spacings,
9. Final machine lens mount and assemble first five components to spacings within specified tolerances. Measure spacings to within ±.0002 inch.
10. Recompute final two spaces,
11. Assemble final two components.

2.2.1.3.3 Processing Strategy - Non-Compensable Errors

As previously stated, .125 wave of RMS error will cause 50% MTF at 40 c/mm to drop to 40%. This has been established as the permissible budget for non-compensable errors, such as decentering, inhomogenity, and surface irregularity. Essentially, most of this budget was

allocated to centering tolerance with the proviso that:

1. All centering measurements are obtained in terms of TIR on surfaces, seats and bores as specified in the TIR sensitivity table. Also, that TIR tolerances would be reduced to .0001" when required and .00005" for the components near the stop position,

2. Surface irregularity and power be considered. A pencil of light for a 1.3 inch F/4.0 aperture is approximately 0.4 inches in diameter. This means that for most of the elements only a small portion of their total surface area is used by any one pencil of light. In general, the surface power tolerance is dictated by the permissible irregularity, since the irregularity cannot be detected if the power departure is too great. For most surfaces the relative bundle areas are small therefore surface irregularity and power tolerances were set at ±1 and ±5 rings respectively. However, for surfaces near the stop position where the full aperture is used, surface tolerance requirements were held to smaller values, ±0.25 rings irregular and ±1.5 rings of power. Cemented surfaces not being as sensitive were held to ±1 and ±5 rings of irregularity and power respectively. Analysis further showed that surfaces adjacent to the stop had the greatest effect on the RMS irregularity budget; therefore, these were kept well under the tolerance budgeted.

2.2.1.3.4 Lens Manufacture

In addition to the normal techniques used in the glass and metal fabrication of precision optics, the manufacture of this lens followed the processing strategy previously outlined and elaborated in the following paragraphs.

1. Glass Order and Melt Data

Glass ordered and melt sheets requested with index measurements out to 1014μ. These extended measurements were essential to avoid the errors which extrapolation would introduce in the polychromic balance.

2. Melt Recomputation

Upon receipt of the full set of melt data, the design was re-optimized for the measured values. The tolerance sensitivity tables indicated that an uncompensated index change of .001 in one element could introduce as much as 2.7 waves of RMS error - far beyond the allowed amount of .125λ for all uncompensated sources. All curves, thicknesses and separations were used in the rebalance to remove the effect of index tolerance.

3. Test Plate Fit

Test glasses were fitted or fabricated to a tolerance of .1% to .05% of design radii. They were then measured and data used to rebalance the design, thus removing the effect of test plate tolerances.

4. Fabrication and Measurement of Aspheric

The aspheric surface for the EWACS Lens is prolate spheroid. In the plane intersecting the optical axis this form of an ellipsoid may be written:

$$\frac{Z^2}{a^2} + \frac{y^2}{b^2} = 1$$

where: a = semi-major axis
b = semi-minor axis

In the formulation used for fabrication:

$$\frac{(cv)\, y^2}{1 + \left[1 - (1+K)\ (cv)^2\ y^2\right]^{1/2}}$$

where: cv (curvature) = $\frac{a}{b^2}$

R (base radius) = $\frac{1}{cv}$

K (conic constant) = $\frac{b^2}{a^2} - 1$

Worst case analysis indicated that errors in R, K, and slope could be compensated as long as the tolerance (R $\longrightarrow$ ±.1%), (K $\longrightarrow$ ± .2%) and (slope error of ±.001 (±.1%)) are not exceeded.

These tolerances were translated into the precision required in the test gear. The surface was tested by a device with a small reflective sphere centered on the short focus of the ellipsoid which, reflects light to the longer focus of the ellipsoid (Figure 21). A microscope having a large numerical aperture, with a beam splitter and pinhole within the microscope, is positioned to project an image at the long focus. The microscope objective is used in double pass, acting as a relay for the return beam reflections. The reflected image is suitable for knife edge testing. Separation of the two foci was translated into a function in base radius and K. A fixed relationship between the foci and the vertex of the ellipsoid was established. Tolerance on axial separation of foci was held to ±.004". Tolerance on the separation between the ellipsoid vertex and short focus, insertion tolerance was kept to ±.001" and measured to .00004". The test set-up was used in final surface correction (Figure 21). When optimum "null" condition for best fit is established, insertion dimension of the test ball is measured. In the prototype lens this distance was within +.0008" which allowed compensation by a re-space plus a .4% change in the first curve of the last spherical element.

Preliminary fabrication of the aspheric used numerical control techniques to generate the ellipsoidal surface to the desired shape. A uniform .010" shell of excess material was left for fine grinding and polishing. Two precision test templates were fabricated, one having the nominal elliptical shape, the other .010" over nominal. Templates were certified using sine bar gauging and were found to be closer than .0001" to the required ellipsoid. The .010" shell was fine ground uniformly to within .0001" of nominal ellipse, using the templates to maintain the required shape

As the surface approached the desired ellipse optical means were used to control its shape. The initial optical measurement setup (Figure 22) consisting of an illuminated fiber optic .002 inch in diameter located at the short focus and a knife edge tester at the long focus. The fiber optic was positioned at the short focus with the aid of a certified glass test sphere; its diameter known to be better than .0001". The illuminated fiber was positioned to just contact the sphere by viewing its reflection. The knife edge was positioned at the long focus. To bring the fiber and knife edge on axis, transverse adjustments were made until coma disappeared.

As the surface approached the final figure, the more sensitive setup shown in Figure 21 was substituted. The final figure met the desired shape and slope requirements except for some minor

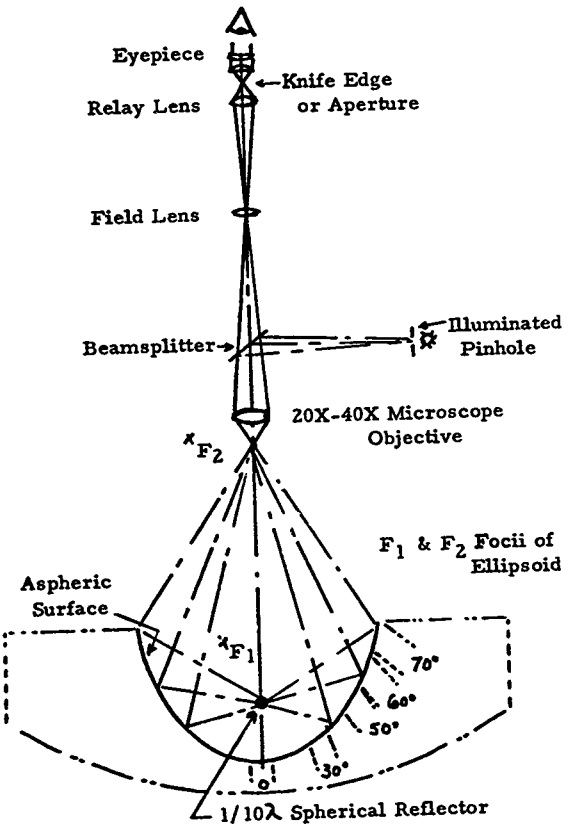


FIGURE 21 FINAL ASPHERIC TEST SET-UP

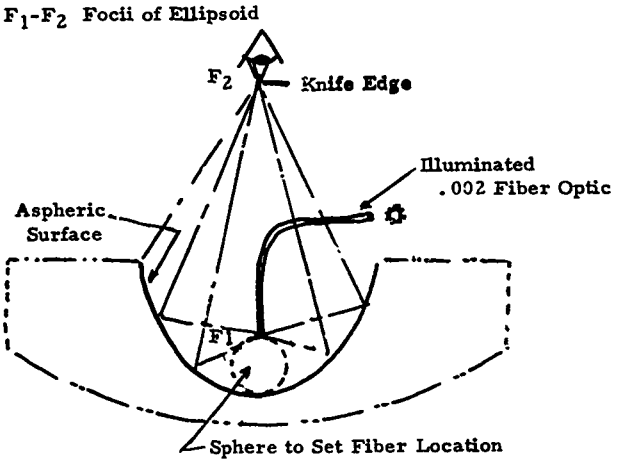


FIGURE 22 INITIAL ASPHERIC TEST SET-UP

edge zones. The area within this zone is utilized by the off-axis pencil of rays corresponding to the field of view from approximately 60 to 70 degrees.

5. Fabrication of Spherical Elements and Components

• Spherical elements were fabricated to the recomputed thicknesses. Thickness tolerances for individual elements were kept between ±.002 inches and ±.003 inches. For cemented components the assembled thickness tolerance was kept under ±.003 inches. For cemented components adjacent to the stop, thickness tolerances were kept to less than ±.001 inches.

The finished elements and components were measured to within ±.003 inches.

• Surface power and irregularity of spherical elements were held under the limited specified in paragraph 2.2.1.3.3.

6. Recomputation for Measured Thickness

This re-optimization was performed to arrive at the final desired set of air spaces from which the dimension for final machining of the lens mount were generated.

7. Partial Assembly

The first five components, starting with those adjacent the stop were installed into the mount holding airspace tolerance of ±.0005". Centration of components adjacent the stop were held to less than fifty millionths. During assembly, spacing measurements were made to an accuracy of ±.0001". These measured values were used to re-optimization for errors in spacing. The last remaining variables, the final two airspaces, were used to compensate the errors.

8. Final Assembly

The remaining two spherical components were installed, completing the lens assembly.

2.2.2 Camera-Back

This unit is a simple camera-back assembly incorporating a flat

glass focal plane, a resilient pressure plate to hold film, and a means for positioning the glass focal plane along the optical axis of the lens to provide a thru-focus capability. Means are provided to secure the assembly to the rear of the lens mount. The camera back is used in photographic evaluation of the wide-angle-objective.

2.2.3 Optical Butting Breadboard

Photographs of the prototype unit are shown in Figures 23 and 24. Major components of this unit are a beamsplitting prism, a CCD, prism mount, and front end electronic units. The breadboard serves a dual purpose, first it is used in preliminary electronic readout testing with a commercial lens and subsequently, it attaches to the rear of the wide-angle-objective lens during the final demonstration phase in which system performance is shown. The optical schematic of the breadboard is shown in Figure 25. As can be seen in the schematic and Figure 6, the active linear sensor array of the CCLID-500A occupied the central portion of the package. The border around the array prevents physical end-to-end butting of several arrays to form longer multi-array assemblies. The beam-splitter takes care of this by providing an optical means of butting the linear arrays.

2.2.3.1 Beamsplitting Prism and Mount

The beamsplitter is used to image the output of the objective lens on to the sensor arrays of optically adjacent chips. The beam splitter is fabricated from a cemented pair of right-angle prisms having a neutral high-efficienty dielectric beamsplitter coating at the cemented interface.

The optical path through the assembly is kept the same for both the reflective and transmissive channels. Optical thickness through the beamsplitter is also made the same as the camera's focal plane plate in order to provide optically interchangeability between the units. Mounting surfaces supporting the beamsplitter prism are lapped flat and resilient clamping is used to hold the prism rigid. This feature avoids strains in the glass which could degrade the image as a result of bi-refringence.

2.2.3.2 Multi-Chip Assembly and Alignment

To facilitate accurate chip positioning, adjustment were incorporated into the breadboard optics. These adjustments enabled focusing and butting alignments to be made while viewing the chips through the beamsplitter using a high power toolmaker's microscope comparator. The

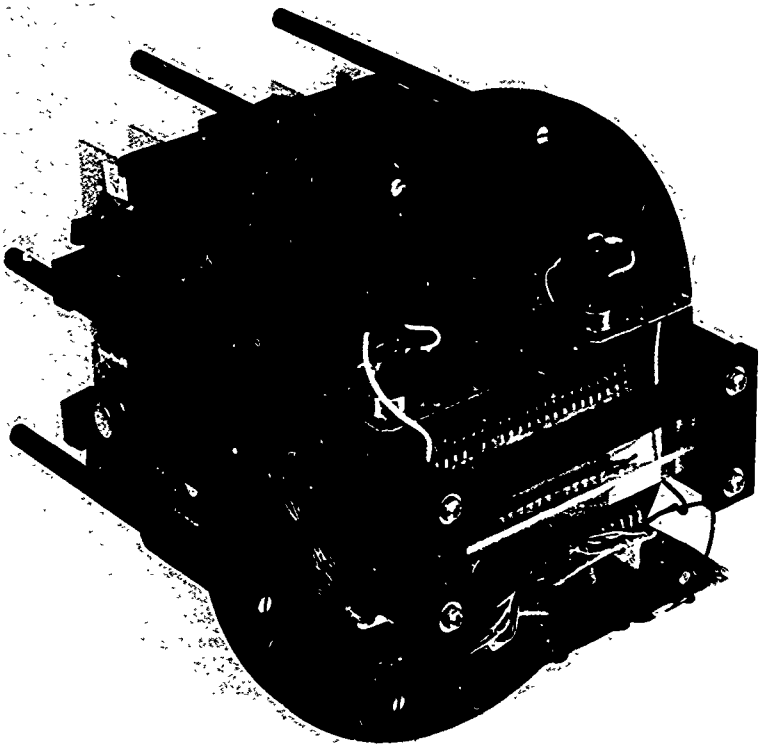


FIGURE 23 OPTICAL BUTTING ASSEMBLY

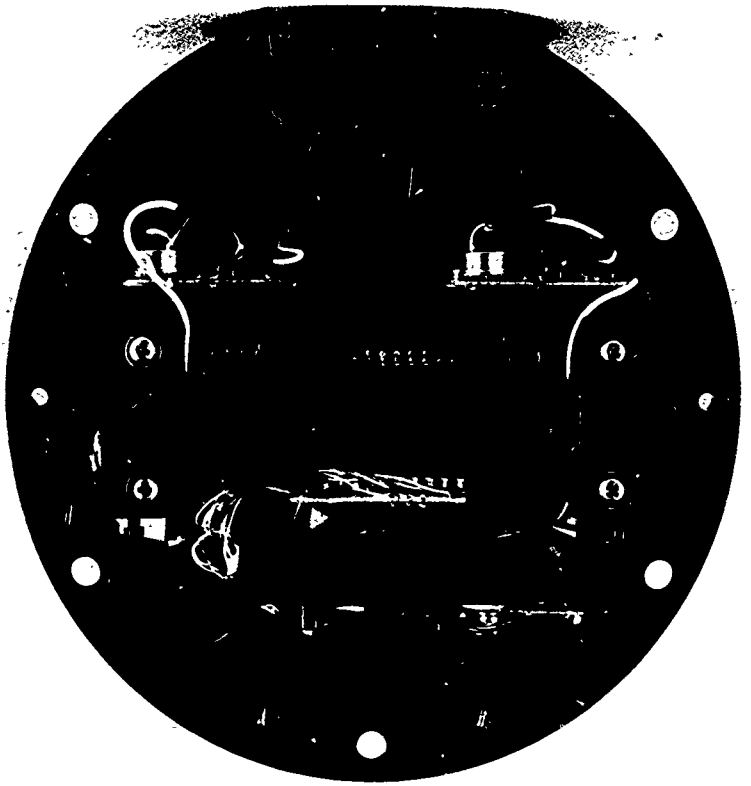


FIGURE 24 CONTIGUOUS SENSOR LOOKING THROUGH BEAM SPLITTER

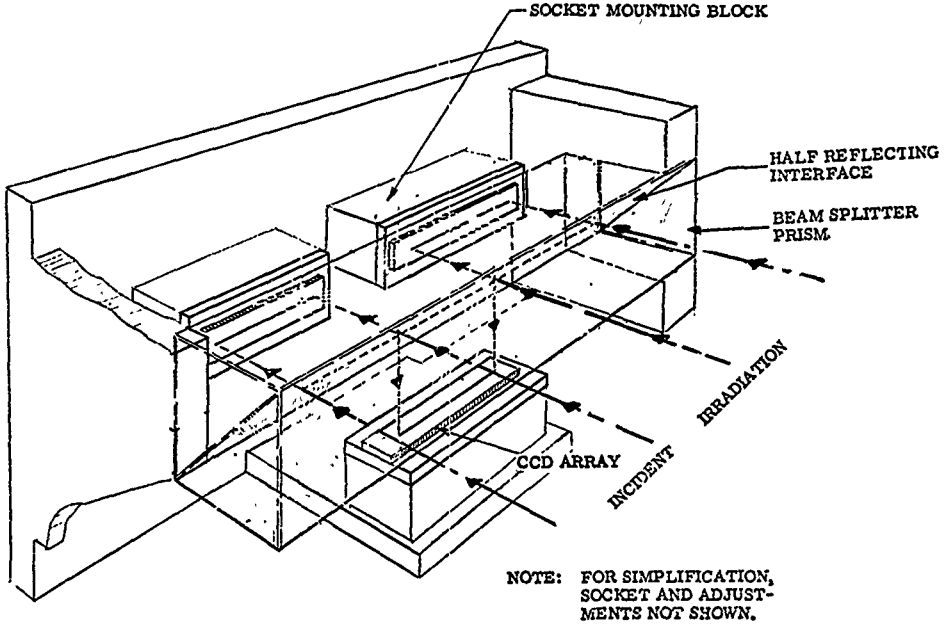


FIGURE 25 OPTICAL SCHEMATIC - OPTICAL BUTTING SCHEME

three CCLID's were first cemented on to individual base plates. These base plates formed part of a six-degree freedom adjustable mount. The base plates were then installed into the breadboard on their respective adjustment posts. The chips were visually focused and butted to better than 1/4 sensor element width. Adjusting screws for the two outboard chips are accessible from the rear so that final butting alignments could be made with the breadboard installed on the objective. These adjustments are performed by viewing the electrical output on an oscilloscope and on the breadboard system display.

SECTION III

PROGRAM TEST RESULTS

The test results described herein are two-fold in nature, namely:

- o The electro-optic performance of the EWACS lens with the CCD arrays, prism beam splitter and electronics to demonstrate the feasibility of optically butting the arrays.
- o The performance of the EWACS lens with respect to photographic resolution, distortion, modulation and transmittance.

3.1 ELECTRO-OPTICAL TEST RESULTS

The paragraphs that follow, not only present actual system performance, but also the methods of selecting matched CCD's and altering their packaging to permit optical butting. Data is also included on light transmission losses through the optical window of the CCD for oblique rays which are encountered near the edge of the field. The CCD's were installed without the covering windows to minimize this loss. Crosstalk in the video output signals of the butted chips was encountered and its causes and effects are described below.

3.1.1 Selection of CCD Arrays

Several important CCD linear array parameters were tested on an off-line array tester. These tests were designed to characterize the CCD array itself, rather than to measure the array's performance within the EWACS System. For these tests, the array clocking frequency was 500 KHz.

The linear CCD test setup is a modular system designed to characterize the array parameters with minimal setup changes. Optical and mechanical conditions are changed by additions, removal or substitution of interchangeable modules. Electrical conditions are changed mostly by screw driver adjustments. The linear CCD test setup includes the following sub systems: optical bench and light tight enclosure, calibrated light source, optical modules, and array controller and amplifier. A secondary test setup consisting of a linear CCD camera, a rotating drum with various targets and a display monitor is used for imaging tests.

The characteristics of specific interest in this program were saturation level, transfer characteristic linearity, line signature and modulation transfer function.

1) Saturation Level

The saturation level was determined with the array evenly illuminated with diffused light. Saturation was found by increasing the light level and observing when the corresponding increase in signal became non-linear. The criterion used to judge the non-linearity was to insert a neutral density filter with 50% transmission and observe when the signal was 55% instead of 50% of its initial value. Typically, the saturation levels were 155 to 320 MV for the ten arrays that were tested.

2) Linearity of Transfer Characteristic

The irradiance falling on the CCD array was varied in steps using neutral density filters starting at the saturation level. The array's average signal output at each irradiance level was recorded. Typically, the slope of the transfer characteristic when plotted on log-log coordinates (gamma) was 0.9 to 0.95.

3) Line Signature

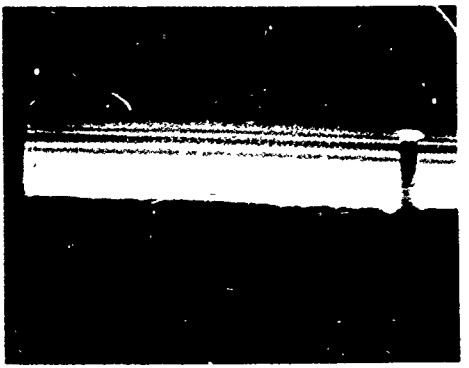
The line signature, that is, a line of video was observed on the oscilloscope for each array under two conditions. A "dark signature" was studied with the array in total darkness to determine if dark blemishes existed. These would show up as white streaks in the dark portions of the scene. Another signature was studied with the array evenly illuminated by diffuse light to determine the uniformity of response or if defective elements existed. Figure 26 shows typical photographs of the illuminated and dark signatures of a CCLID-500A array.

4) Modulation Transfer Function (MTF)

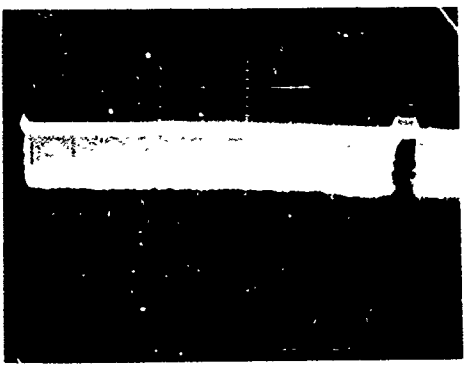
A bar target was imaged on the array using a 3-inch Super Baltar lens at f/8. The MTF of each array was determined at 1/2 the limiting resolution of the arrays, that is, 8 lp/mm.

3.1.2 Altering CCD Package to Permit Butting

The photosensitive length of the 1 x 500 array is 0.6 inch which means that the center-to-center distance for CCDs adjacent to each other on the same side of the beam splitter is 1.2 inch. This means that the CCD



Dark Signature
5 mv/cm



Signature at
0.5 Saturation
100 mv/cm

FIGURE 26 TYPICAL ARRAY SIGNATURES

TABLE II

LIGHT TRANSMISSION THROUGH CCD WINDOW AS A FUNCTION OF ANGLE

Angle of Incidence	TRANSMISSION		
	P Polarization	S Polarization	Average
0	0.920	0.920	0.920
10	.925	.920	.923
20	.935	.908	.922
30	.951	.887	.919
40	.972	.852	.912
50	.994	.789	.892
60	.996	.677	.837
70	.918	.490	.704

mounting substrate should be less than 1.2 inch to provide clearance and freedom of motion for adjustment. However, the CCLID-500 substrate normally measures 1.25 inch so that cutting of the substrate was required.

Consider the three CCDs in their functioning sequence A, B and C. A and C are adjacent to each other on the transmitting side of the beam splitter while B is on the reflecting side. Once the CCDs were selected, an optical tooling microscope was used to measure the respective distances from the last element on A to the nearest substrate edge and the first element of C to its nearest substrate edge. A sufficient piece of each substrate was then cut-off using a wet diamond wafering wheel to yield a clearance of 0.030 inch between the substrates when they were mounted in the system. The amount removed from each substrate was kept to a minimum so as not to interfere with connecting pins of the device. Typically, this amount was 0.04 inch.

Since the cutting operation is a wet process, silicone rubber (RTV) was used to seal the plastic CCD cover to the substrate where the connecting pins are mounted. The ends of this cover are epoxied to the substrate and not enough material was removed in the cutting process to break this bond. A piece of masking tape was used to seal the opening in the cover as these CCDs were furnished without optical glass windows for reasons described below.

3.1.3 Effects of CCD Optical Window

The optical window in the cover of the CCD is 0.006 inch thick. Its absorption effect on transmitted light is quite negligible. The transmission is about 0.99 for the longest path in glass. However, the effect of surface reflections at an oblique angle is severe. Table II shows the light transmission for thin glass window as a function of incident angle. Both the "P" (parallel to the plane of incidence) and "S" (perpendicular to the plane of incidence) polarizations are shown as well as their average. This table considers Fresnel reflections only.

It can be seen in the table that the light transmissionat an angle of incidence of 70° is about 92% for "P" polarization and 49% for "S" polarization. Their average is 70%.

3.1.4 CCD Video Crosstalk

A severe video crosstalk problem was encountered during the photo gate transfer times of each CCD. This crosstalk manifested itself in the display as several light or dark bands on each side of an optical butt. A good deal of the problem was traced to the interconnecting cable between the sensor and control units. Much of that part of the problem was alleviated by constructing the cable as three separately shielded sections. The

balance appeared to be due to the cabling between the CCD arrays and their drivers. In this case, very little could be done because of the requirement that the CCD array cabling be of small gauge and flexible wire so as not to interfere with mechanical adjustment and to avoid crowding. It was found that careful adjustment of the array parameters could minimize the problem.

Figure 3.1.4-2 shows a sketch of the mixed video output of CCD arrays A and B looking at a uniform white scene. This figure shows the last 20 elements of video A when "Enable A" is high and the first 20 elements of video B when "Enable B" is high. The odd-even video response is shown somewhat exaggerated for clarity. The crosstalk is seen as an upset of the odd-even balance and is observed on the display as light and dark lines, each being one resolution element wide.

The figure also shows the waveforms which appear to be partly responsible for the crosstalk, namely, the phototransfer pulses for adjacent arrays. The Enable gates are not responsible for any crosstalk. As described earlier in paragraph 2.1.1.2, the phototransfer pulse pairs (ϕ_p and ϕ_x) for each CCD are staggered in time in order that the video of the next adjacent array be available when a given array is finished with its line of video. The waveforms sketched show that the crosstalk occurs not only at the leading edges of these pulses, but also for their duration. This behavior was shown to be dependent on the fact that during the phototransfer pulse for array B, (ϕ_{PB}) the vertical register pulses for array B, (ϕ_{V1}, ϕ_{V2} and ϕ_{V3}), were absent. The conclusion one reaches is that the adjustment of the odd-even balance for a particular array is affected by the clocking signals of the other arrays. This indeed was the case and was further enforced by the fact that the odd-even could be balanced to look good in the crosstalk region, but poor for the rest of the video signal.

Through judicious adjustment of the CCD clocking voltages and biases, a reasonable compromise could be reached. That is, though the odd-even affect was not nulled out completely at least it was uniform for the entire video signal

3.1.5 EWACS Breadboard Performance

Figure 28 shows the results obtained looking at the optical butt between CCD arrays B and C. Three one scan photographs were taken of the display monitor. The one captioned "B" is a photograph of one scan of the last 250 elements of the B array alone, while "C" is a photograph of the first 250 elements of C alone. A photograph, "B and C", was then taken with both arrays operating simultaneously. All of the photographs were taken without any changes in the geometry of the photographic set up or adjustments to the system.

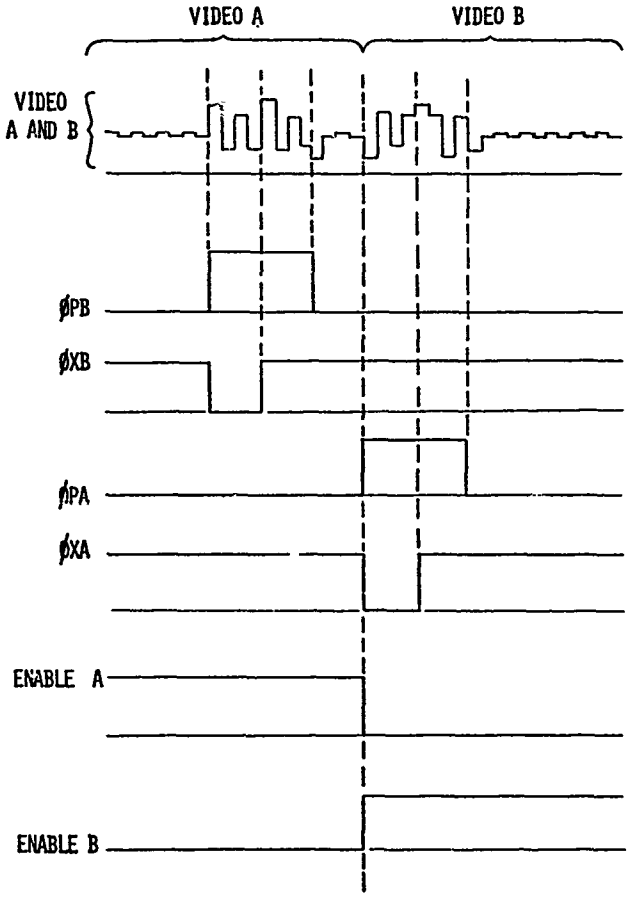


FIGURE 27 WAVEFORM SKETCHES SHOWING VIDEO CROSSTALK

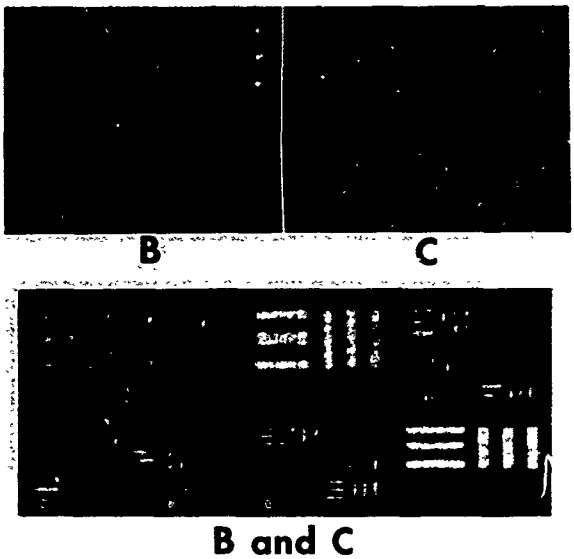


FIGURE 28 EWACS BREADBOARD PERFORMANCE

The optical butt can be detected but, by no means, is it obvious. Furthermore, the system limiting resolution is demonstrated by the smallest tri-bar test pattern which corresponds to 16 line pairs per millimeter. The non-linearity of the servo scanner is evident when the spacing of horizontal bars is examined.

The scene is compressed about 16% in the vertical direction. This resulted from the fact that a different CRT was used for photography than for visual observation. The system was adjusted to give proper display on the long persistence CRT built into the system which was used for all visual adjustments. A short persistence CRT was used in parallel for photography and its vertical deflection sensivity was 16% low.

The tri-bar target series was painted white on a 4 x 8 foot black panel. It was illuminated with tungsten flood lamps to an average level of 150 foot-candles incident on the target. The incident radiant flux between 0.41 and 0.98 μ was 3500 μ watts/cm^2.

This target departed from a standard target in that some target groups deviated considerably from $6\sqrt{2}$ ratio. The smallest white bar measured 10.4 x 52 mm with a corresponding black space so that the smallest line pair was 20.8 mm wide. A distance of 36 feet was achieved between the target and lens which has an effective focal length of 1.3 inches. Thus, the object to image reduction ratio was 333:1 resulting in a spatial frequency of 16 lp/mm for the smallest target. Figure 29 shows the spatial frequencies for all the target clusters.

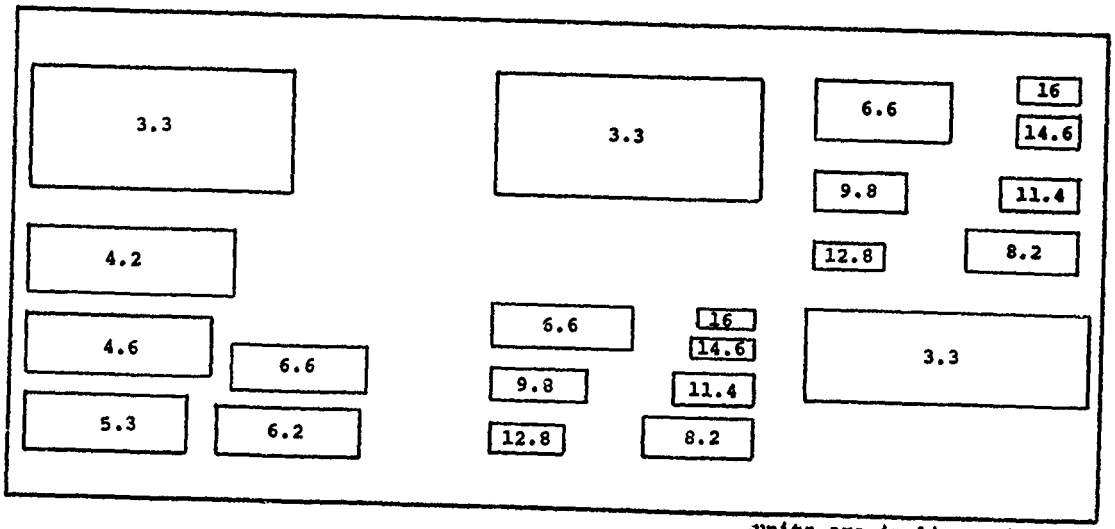


FIGURE 29 SPATIAL FREQUENCIES OF TEST TARGET IMAGE

3.2 EWAC LENS EVALUATION

The following paragraphs describe the comprehensive evaluation of lens performance which was made to demonstrate photographic resolution, distortion, transmittance, relative illumination, black and white photography, and modulation transfer function.

3.2.1 Resolution

EWAC lens resolution was determined photographically, utilizing Method 11, Collimator Method, of MIL-STD-150A. The general arrangement is shown in Figure 30. Test set-up employs a single 60-inch focal length collimator and a standard USAF-1951 target. The lens was mounted on a rotatable bench and its entrance pupil was located roughly at the center of rotation. Photographic exposures were made on axis and at five degree intervals up to ±70 degrees. A thru focus test to determine the optimum focal plane was made. Performance at the optimum focal plane was evaluated on the basis of photographic resolution using the following test conditions:

o	Film	3401	3401
o	Filter	Wratten 25	Wratten 25
o	Exposure	Strobe	Strobe
o	Processing	MX641	MX641
o	Target	High Contrast	6:1 Contrast

3.2.1.1 Resolution Test Results

Resolution test results for both high and medium contrast photography are shown in Table III and Figure 31. Comparison of the predicted high contrast performance is made to actual resolution data. Lens resolution compared very favorably with predictions. A tail-off is noted beyond 60 degrees - this is believed to be caused by aberrations introduced by zones near the edge of the aspheric surface. This condition could easily be rectified for production units.

Medium contrast target data shows the ultra-wide angle lens is capable of yielding an LWAR of 60 L/mm.

All indications show this type of lens can provide excellent resolution at very wide field angles which heretofore have been considered not possible.

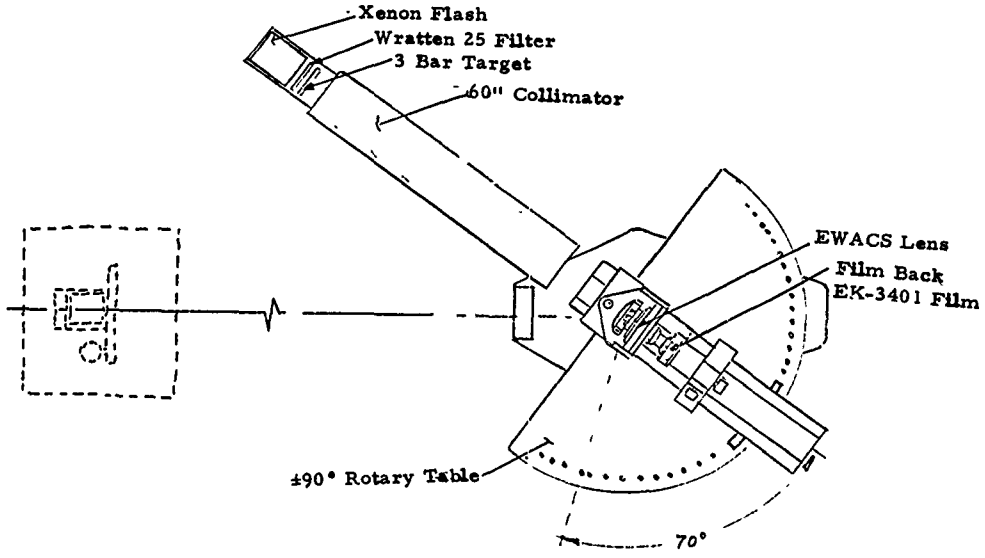


FIGURE 30 RESOLUTION TEST SET-UP

TABLE III

RESOLUTION TEST RESULTS

Conditions

Film	-	3401
Filter	-	Wratten 25
Illumination	-	Non-Strobe
Target	-	USAF-1951
Contrast	-	High Contrast 1000:1
		Medium Contrast 6:1
Chemistry	-	MX641, 68°F, One Minute

Field Angle	Predicted (L/mm) High Contrast	Resolution (L/mm) High Contrast	Resolution (L/mm) 6:1 Contrast
0	70/70	104/104	92/82
5	70/65	98/96	92/82
10	70/65	114/89	102/86
15	70/60	116/88	80/68
20	70/60	119/80	86/72
25	65/60	112/86	74/67
30	55/60	90/69	74/67
35	50/60	60/61	69/49
40	50/60	50/38	50/38
45	50/60	50/66	41/46
50	60/50	67/27	42/53
55	60/50	77/52	67/31
60	60/45	65/32	58/33
65	70/40	60/28	38/18
70	70/30	28/10	36/9

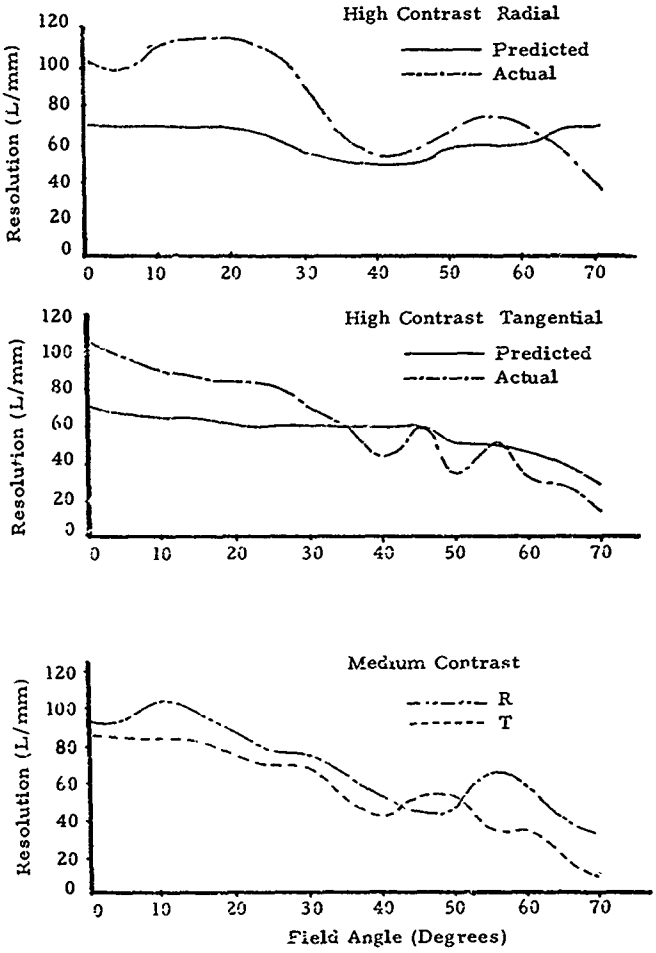


FIGURE 31 RESOLUTION vs. FIELD ANGLE

3.2.2 Distortion

Distortion test was performed utilizing Method 26 - collimator bank photographic method of MIL-STD-150A (Figure 32). The Fairchild multi-collimator metric camera calibration facility was used as the collimator bank. Distortion was photographically evaluated using photographic glass plates, cosine corrected high contrast distortion targets and flashed tungsten illumination. The photographic plates were measured utilizing a David-Mann plotting comparator.

3.2.2.1 Distortion Test Results

Resulting image height versus field angle data is reduced to a graph. Shown in Figure 33 is a plot comparing the predicted lens performance with actual lens performance for calibrated radial distortion. Figure 34 is a plot comparing predicted with actual performance of image height versus (tan U) field angle. Results show that actual distortion characteristics compare very favorably to predicted values.

3.2.3 Axial Transmission

Axial transmission test was measured utilizing Method 5 - extended source method of MIL-STD-150A. An integrating sphere, tungsten illuminated at approximately 2800°K (Figure 35) was used as the extended source. A Wratten minus blue filter was used to better approximate the spectral weighting of silicon CCD response.

3.2.3.1 Transmission Test Results

Resultant axial transmission was measured at 77% comparing favorably with the 80% predicted value.

3.2.4 Relative Illumination

Relative illumination was measured utilizing densitometric Method 9 of MIL-STD-150A. This method uses the same collimator set-up as used in resolution tests, except that an unformulated illuminated aperture acting as an extended source was substituted for the collimator target. The target was photographed axially and incremented to 70 degrees at intervals of 5 degrees. Densities of the exposed and developed images were measured and relative illuminance determined using the sensitometric curve of the emulsion, obtained by exposing a calibrated step-wedge.

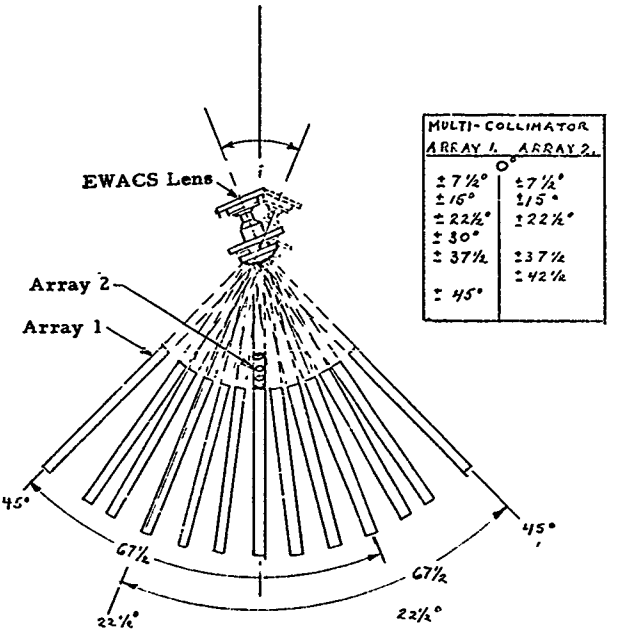


FIGURE 32 DISTORTION TEST SET-UP

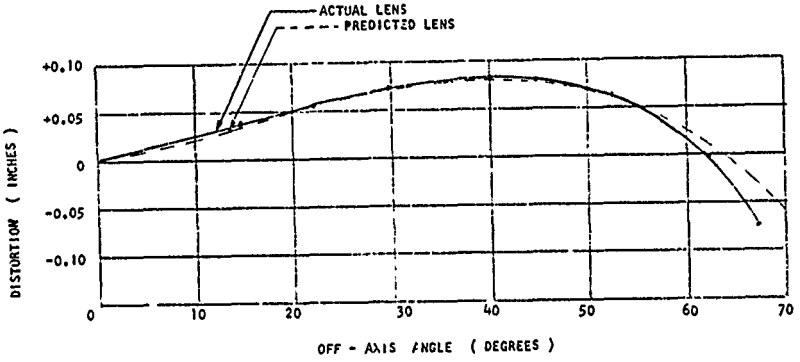


FIGURE 33 CALIBRATED DISTORTION

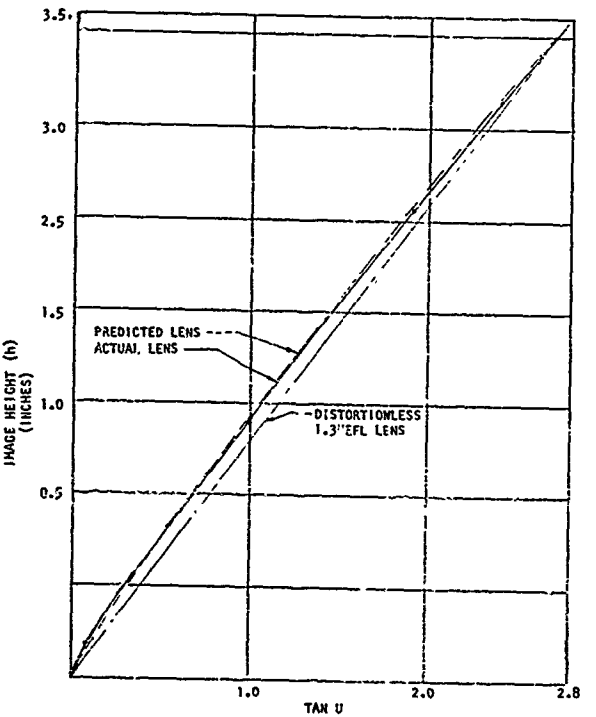


FIGURE 34 IMAGE HEIGHT vs. FIELD ANGLE

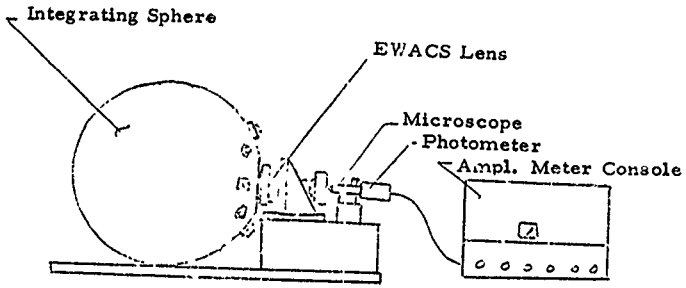


FIGURE 35 AXIAL TRANSMISSION TEST SET-UP

3.2.4.1 Relative Illumination Test Results

Relative illumination versus off axis angle is shown in Figure 36. Actual values closely follow predicted lens performance from 0° to 45° then departs to a maximum difference of 25% at 65 degrees. Computer analysis indicates that this difference results from the effects of single layer MgFl anti-reflection coating at large incident angles. MgFl coating was used to save the delay which would have had to be tolerated if a high efficiency anti-reflection multi-layer dielectric coating system was used. This condition can be improved by use of HEA coatings in production units. To verify the validity of this statement, footprints of entrance pupil projections were measured and compared to the axial bundle per Method 10 of MIL-STD-150A. Measurements compare favorably with predicted values indicating that controlled HEA coatings on critical components such as the aspheric and semi-hemispherical elements would improve relative illumination performance.

3.2.5 EWACS Photography

Photographs were made of the scene atop the roof at Fairchild. Film used was EK3404 developed in MX641 chemistry to a high gamma. Positives were dodged to show the relative illumination correction which the CCD electronics would provide. The result of this test is shown in Figure 37.

3.2.6 Modulation Transfer Function

The percent modulation 40 c/mm was measured, both in the tangential and radial directions across the format in 5 degree increments, beginning at 0 degrees and extending ±70° from the axis. Test was performed utilizing Fairchild's MTF optical bench. This bench schematically shown in Figure 38, comprises of a 248-inch collimator, moving bar target generator, slit-microscope-photomultiplier-detector assembly, servo controlled strip chart recorder and photometer amplifier console.

3.2.6.1 MTF Test Results

Figure 39 is a plot of resultant MTF measurements.

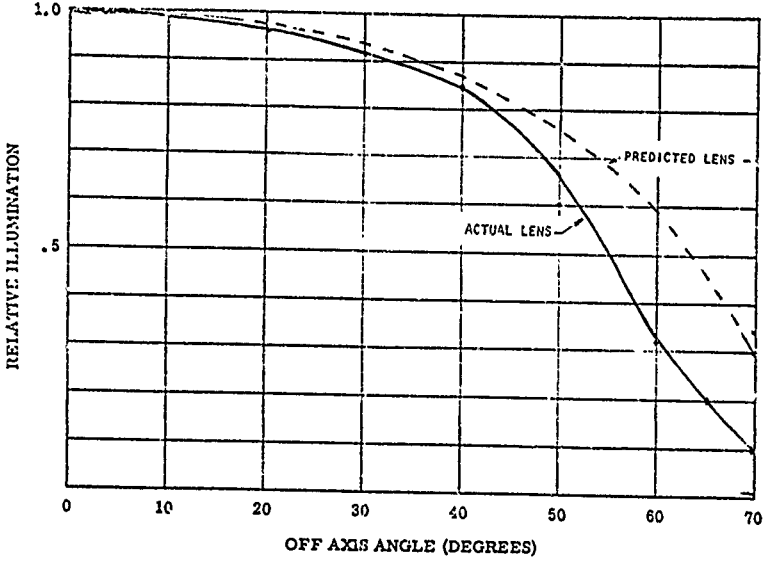


FIGURE 36 RELATIVE ILLUMINATION

2.75X ENLARGEMENT

FIGURE 37 EWACS PHOTOGRAPHY

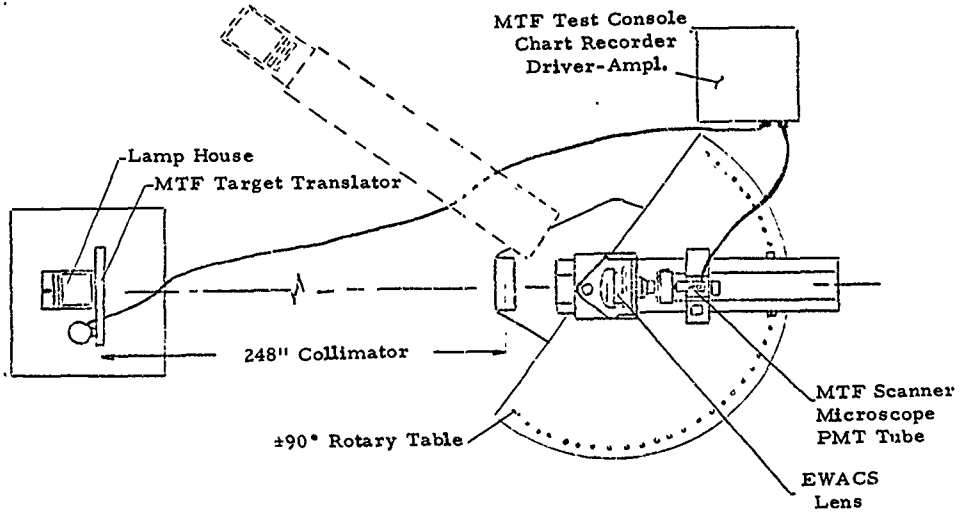


FIGURE 38 MTF TEST SET-UP

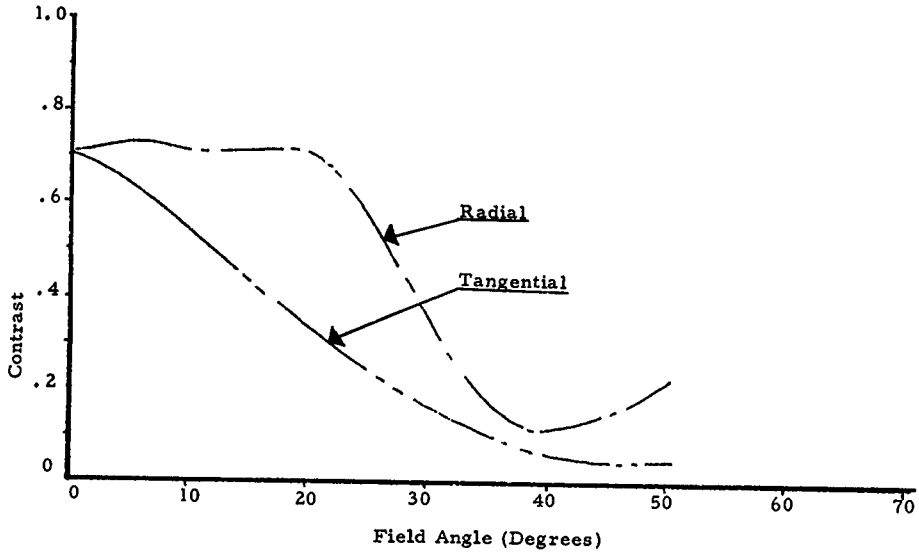


FIGURE 39 MTF AT 40 LINES/MM

SECTION IV

CONCLUSIONS

4.1 CONCLUSIONS

The objectives of this program were achieved in that:

1. A wide angle, low distortion high resolution lens was designed and fabricated.

2. The measured performance of the lens compares quite favorably with the design goals as tabulated below.

	Design Goal	Actual Lens
EFL	1.3"	1.3"
f/#	f/4	f/4
FOV	140° (±70°)	140° (±70°)
$\Delta\lambda$	0.4 - 1.1 μm	0.4 - 1.1 μm
% T Axial	80% (T/4.5)	77% (T/4.56)
% T relative	30% at 70°	30% at 62°
Distortion	Minimized at ±60°	as predicted
Resolution at 60°	60/45 (1) High Contrast	65/35 High Contrast 58/33 Medium Contrast
MTF	40% MTF at 40 lp/mm to ±60°	40% MTF at 40 lp/mm to ±60° (2)
Length	11.35 inches maximum	11 inches

(1) Radial/Tangential Resolution in lp/mm.
(2) This result is extrapolated from MTF measurements up to ±50°; resolution measurements predict MTFs better than those measured.

3. Optical butting by means of a beam splitter and mechanical adjustments of the CCD arrays was achieved.

4. Electro-optical butting of the CCD arrays was successfully demonstrated by means of the breadboard scanner/display which showed a seamless picture of a resolution target with the butt in the center of the picture.

5. Compatibility of the lens with the CCD sensors was demonstrated.

6. Resolution consistent with the limiting resolution of the CCLID-500A arrays was demonstrated.