INVESTIGATION OF TECHNOLOGICAL PROBLEMS IN GaAs

Fred H. Eisen, et al

Rockwell International Corporation

Prepared for:

Air Force Cambridge Research Laboratories
Defense Advanced Research Projects Agency

25 July 1975

AFCRL-TR-75-0435

INVESTIGATION OF TECHNOLOGICAL PROBLEMS IN GaAs

Fred H. Eisen, John A. Higgins, Anthony A. Immorlica, Jr.,
Reidar L. Kuvås, Burt W. Ludington, Bryant M. Welch,
Cheng P. Wen, and Ricardo Zucca

Science Center
Rockwell International
Thousand Oaks
California 91360

15 October 1975

Semi-Annual Technical Report No. 1

Sponsored by

Defense Advanced Research Projects Agency
ARPA Order No. 2489

Monitored by

AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
HANSCOM AFB, MASSACHUSETTS 01731

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: AFCRL-TR-75-0435

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle): INVESTIGATION OF TECHNOLOGICAL PROBLEMS IN GaAs

5. TYPE OF REPORT & PERIOD COVERED: Semi-Annual Technical Report No. 1

6. PERFORMING ORG. REPORT NUMBER: SC5017.4SAR

7. AUTHOR(s): Fred H. Eisen, John A. Higgins, Anthony A. Immorlica, Reidar L. Kuvas, Burt W. Ludington, Bryant M. Welch, Cheng P. Wen, Ricardo Zucca

8. CONTRACT OR GRANT NUMBER(s): F19628-75-C-0113

9. PERFORMING ORGANIZATION NAME AND ADDRESS: Science Center, Rockwell International, Thousand Oaks, CA 91360

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 2489-N/A-N/A, 61101E

11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Cambridge Research Laboratories, Hanscom AFB, MA 01731, Contract Monitor: Sven A. Roosild/LQD

12. REPORT DATE: 25 July 1975

13. NUMBER OF PAGES: ~~116~~ 115

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

A - Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

This research was supported by the Defense Advanced Research Projects Agency. ARPA Order No. 2489

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Ion Implantation
Semi-Insulating GaAs
Epitaxy
MESFET
IMPATT

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Various technological problems in the development of GaAs microwave devices are covered in this report. The goal is to advance the state-of-the-art in material and device technology. The work reported here includes epitaxial growth of high-resistivity and multiple ultra-thin films, study of the relationship between device performance and material parameters using FETs and p-n junctions, study of noise and impact ionization coefficients in IMPATT structures under high electric field, preparation of high-quality oxide films for surface passivation, growth of semi-insulating substrates, and characterization techniques and study

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE.

Unclassified

1. SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20 (Cont'd)

of ion implantation as a tool for microwave device fabrication. The activities and the progress made during the six-month period are described in separate sections. Future plans for the next reporting period are also included. This work is being carried out in cooperation with the California Institute of Technology, Cornell University, Crystal Specialties, and Stanford University.

K. Gamo, J. W. Mayer, M-A. Nicolet

California Institute of Technology
Pasadena, California 91109

J. Berenz, G. C. Dalman, L. F. Eastman,
D. Law, C. A. Lee, and M. Tomassini

Cornell University
Ithaca, New York 14853

B. L. Mattes, G. L. Pearson, Y. M. Houng

Stanford University
Stanford, California 94305

W. P. Allred

Crystal Specialties, Inc.
Monrovia, California 91016

TABLE OF CONTENTS

Table of Contents (Cont'd)

TABLE OF ILLUSTRATIONS

Table of Illustrations (Cont'd)

Table of Illustrations (Cont'd)

LIST OF TABLES

1.0 INTRODUCTION

GaAs devices have not realized their potential in microwave system applications despite their superior performance characteristics repeatedly demonstrated in laboratories. The combination of high electron mobility, the built-in negative differential mobility and the large difference in electron and hole ionization coefficients led to the realization of FETs operating at frequencies far beyond the cutoff of the bipolar transistor, Gunn effect devices and the high efficiency (> 30%) IMPATT devices. However, the advantages in performance offered by GaAs for these specific devices are often overshadowed by the lack of control in GaAs material technology. The essential criteria for system-ready devices, namely, reproducibility, reliability and low cost are not met. Meanwhile, the urgent need of better solid state microwave and optical devices for high data rate communication is rapidly approaching due to the increasing use of digital computers. Improvements in GaAs technology are expected to produce devices which will satisfy many of these near-term needs. In particular, the GaAs IMPATT diode has, in the laboratory, consistently yielded superior performance in power-amplifier applications up to 30 GHz, while the GaAs FET combines properties of very low noise and high efficiency to promise potential use in front ends as well as in power amplifiers up to and possibly beyond X-band frequencies.

A joint program between the Science Center and several leading universities was conceived and initiated in 1973 to investigate and solve the technological problems in the development of GaAs devices. Crystal Specialties, a leading

GaAs substrate material supplier, was brought in after October, 1974, to provide substrates for the research program. The IMPATT diode and the Schottky barrier field effect transistor were chosen as the experimental vehicles for the studies of GaAs material and technology. The areas of research relevant to these devices are:

1. Growth and quality evaluation of semi-insulating substrates in terms of electrically-active trap densities, crystal dislocations and inclusions of foreign materials.
2. Reproducible uniform growth of ultra-thin epitaxial layers and high-resistivity epitaxial material.
3. Formation of low-resistivity ohmic contacts.
4. Formation of semi-insulating areas by proton bombardment.
5. Ion implantation to form uniform ultra-thin n-type layers on insulating substrates for device structures.
6. RF measurement on GaAs devices for material characterization and technology evaluation.

The above activities are carried out at the Science Center closely coordinated with the participating universities. Improvement in reliability and yield of microwave devices is anticipated as a direct result of this GaAs technology program.

2.0 PROGRAM GOALS AND TECHNICAL APPROACH

2.1 Epitaxial Material Growth and Characterization

The goal is to investigate material and processing technology to improve the control of material preparation, enhancing the reproducibility and the reliability of devices. Problems related to device film properties such as the uniformity in thickness and carrier concentration, dislocation density, surface damage, and background impurity densities are studied.

2.1.1 High-Resistivity GaAs Layers

This research program is aimed at establishing parameters (temperature, dopants, distribution coefficients, etc.) necessary for the growth of thin layers of high-resistivity GaAs buffer layer material on semi-insulating GaAs substrates by means of liquid phase epitaxial (LPE) techniques. In addition, the electrical properties of these layers will be measured to study their electron transport mechanisms and to provide information for device applications.

2.1.2 Multiple Layer Liquid Phase Epitaxy

The purpose of this effort is to duplicate at the Science Center the high-resistivity epitaxial growth techniques developed at Stanford University. The primary goal is to incorporate these techniques in a multiple-layer LPE system suitable for growing FET epitaxial layers on high-resistivity epitaxial buffer material. Devices fabricated from these buffer layer structures will be measured and compared to those fabricated from epitaxial layers on Cr-doped substrates. Single-layer buffer material will also be made available for ion implantation studies.

2.1.3 Material Characterization--Theoretical and Experimental Investigation of the Effect of Material Properties on Device Performance

Electrical measurements performed on GaAs devices are employed to evaluate the effect of material parameters on device performance. Basic material parameters, such as the asymmetry of the hole and the electron ionization rate, are to be derived from data obtained on GaAs IMPATT amplifiers and carrier multiplication experiments. Surface passivation techniques will be studied. The effect of interface properties between the active layer and the semi-insulating substrate of GaAs FETs on device performance is to be investigated.

2.2 Semi-Insulating Material

The goal is to prepare and to establish methods to evaluate semi-insulating GaAs crystals with the emphasis placed on the effect of deep traps in FETs fabricated on such substrates. The roles of impurities such as O, Si, and Cr are investigated. Breakdown measurements of p-i-p, n-i-n, and n-i-m structures are employed to investigate the electrically active trap densities. The potential distribution in these structures under d-c bias is studied using high spatial resolution Auger spectroscopy and pulse measurement techniques.

2.3 Ion Implantation

The goal is to investigate the effect of ion beam energy, dosage, and species of impurities on the carrier concentration profile of ion-implanted GaAs substrates under various annealing conditions. The effectiveness of the annealing caps for the substrate surface during the annealing process is also being investigated. A combination of controlled stripping and C-V Hall measurements is being used to characterize the implanted layer.

3.0 RESULTS

3.1 Epitaxial Material Growth and Material Characterization

3.1.1 High-Resistivity GaAs

3.1.1.1 Growth Studies. In order to study the effects of the bakeout temperature in the SiO_2-BN(C)-H_2 system, two series of growths were made with the following growth conditions held constant: bakeout period, 15 hours; H_2 flow rate, 0.6 liter/min; growth temperature, 700°C, and cooling rate, 4.5°C/min.

In the 1200 series of growths, Table 3.1-1, the melt was baked out at 800°C before each growth. No intentional dopant was added in the first seven growths of this series. The first layer is n-type, probably due to incomplete chemical reactions between the melt and system components and residual impurities in the melt constituents. Subsequent layers are p-type with carrier concentrations and resistivities in the range of 5×10^{14} cm^{-3} and 20 ohm-cm ($\approx 1.5\times10^{4}$ ohm/□), respectively. This series continued for five additional growths with 0.5 atomic % Cr added to the melt. The first two layers (#1208 and 1209) changed back to n-type with a carrier concentration of $\approx 2\times10^{14}$ cm^{-3}. During subsequent growths, the layers (#1210-1212) again became p-type and the carrier concentration leveled off at approximately the same value as for the undoped layers. This suggests that at this bakeout temperature, Cr reacts with other impurities in the melt and becomes inactive. The initial change back to n-type is probably due to some impurities in the Cr source.

Table 3.1-1 Properties of Epitaxial GaAs Layers Grown in a SiO_2-BN(C)-H_2 Growth System. Growth Series 1200

Growth Conditions: Bakeout Temp., 800°C; Bakeout Period, 15 hrs
Growth Temp., 700°C; Cooling Rate, 4.5°C/min
H_2 Flow Rate, 0.6 ℓ/min

Growth No.	Dopant	Mobilities @ 300/77 K (cm^2/V-sec)	Carrier Densities @ 300/77 K (cm^{-3})	Resistivity @ 300 K (ohm-cm)	Conductivity Type
1201	"	8,200/66,000	$3.8/3.8 \times 10^{13}$	20	n
1202	"	240/--	3.6×10^{14}/-	72	p
1203	"	600/6,200	$4/3.4 \times 10^{14}$	26	p
1204	"	460/6,400	$6.8/6.6 \times 10^{14}$	20	p
1205	"	480/7,600	$5.2/4.3 \times 10^{14}$	25	p
1206	"	510/7,100	$6.1/5.4 \times 10^{14}$	20	p
1207	"	470/--	4.3×10^{14}/-	32	p
1208	Cr(0.5 atm %)	6,800/63,000	$2.2/2.2 \times 10^{14}$	4	n
1209	"	8,000/85,000	$2.0/1.9 \times 10^{14}$	4	n
1210	"	520/--	1.4×10^{14}/-	86	p
1211	"	510/--	2.9×10^{14}	43	p
1212	"	450/7,900	$4.4/3.3 \times 10^{14}$	31	p

In the 1300 series of growths, Table 3.1-2, the bakeout temperature was 700°C. All substrates except those noted on the table were high-resistivity, Cr-doped GaAs. The first layer was grown directly from a fresh Ga melt and GaAs source without a bakeout beforehand. This layer is n-type with a carrier concentration of 7.7×10^{14} cm^{-3}, which may be due to unknown impurities in the source. Following a 15-hour bakeout, the carrier concentration decreased in the second layer grown from this melt. After four additional growths, the layers became p-type with carrier concentrations in the range of 4.6×10^{13} cm^{-3}, and a resistivity as high as 290 ohm-cm. This indicates that for a bakeout temperature of 700°C, the shallow donors and acceptors are highly compensated. After these eight undoped growths, 0.5 atomic % of Cr was added to the same melt. The next three layers were n-type with carrier concentrations in the range of 10^{15} cm^{-3}. However, in subsequent growths, the carrier concentrations decreased sharply. Some of the layers became semi-insulating with carrier concentrations in the low 10^{11} to mid-10^{12} cm^{-3} range and resistivities as high as 10^{4} ohm-cm. The sign of the Hall coefficient for all of these Cr-doped layers (except #1318 at 300 K) indicates that they are n-type. The Hall mobilities are generally low (270-2,500 cm^2/V-sec). For sample #1318, the Hall coefficient indicates p-type material at 300 K but n-type at 77 K. All of these anomalies are probably a result of mixed conduction. Growth #1319 was grown on an oxygen-doped semi-insulating GaAs substrate. The carrier

Table 3.1-2 Properties of Epitaxial GaAs Layers in a SiO_2-BN(C)-H_2 Growth System. Growth Series 1300†

Growth Conditions: Bakeout Temp., 700°C; Bakeout Period, 15 hrs
Growth Temp., 700°C; Cooling Rate, 4.5°C/min
H_2 Flow Rate, 0.6 ℓ/min

Growth No.	Dopant	Mobilities @ 300/77 K (cm^2/V-sec)	Carrier Densities @ 300/77 K (cm^{-3})	Resistivity @ 300 K (ohm-cm)	Conductivity Type
1301*	--	8,200/70,000	$7.7/7.5 \times 10^{14}$	1.0	n
1302	--	8,500/58,000	$2.4/2.0 \times 10^{14}$	3.1	n
1303	--	9,000/65,000	$3.4/3.0 \times 10^{14}$	2.1	n
1304	--	7,700/58,000	$6.2/5.4 \times 10^{14}$	1.3	n
1305	--	7,200/59,000	$6.2/6.5 \times 10^{14}$	1.4	n
1306	--	580/--	4.6×10^{13}/-	230	p
1307	--	540/--	1.1×10^{14}/-	103	p
1308	--	220/--	9.8×10^{13}/-	290	p
1309	Cr(0.5 atm %)	8,000/37,000	$4.9/3.9 \times 10^{15}$	0.2	n
1310	"	7,000/46,000	$2.8/2.3 \times 10^{15}$	0.3	n
1311	"	7,900/60,000	$3.1/3.2 \times 10^{15}$	2.6	n
1312	"	290/--	6.8×10^{12}/-	3,200	n
1313	"	10,000/70,000	$1.7/1.9 \times 10^{12}$	3.5	n
1314	"	--	2.2×10^{12}/-		n
1315	"	1,700/--	3.6×10^{11}/-	1×10^4	n
1316	"	2,300/--	3.3×10^{12}/-	830	n
1317	"	360/--	4.0×10^{12}/-	4,400	n
1318#	"	570/20,000	$6.0 \times 10^{13}/7.7 \times 10^{12}$	180	p
1319**	"	7,600/77,000	$6.8/6.0 \times 10^{13}$	12	n
1320	"	2,500/--	2.0×10^{11}/-	1.3×10^4	n
1321	"	8,100/96,000	$2.9/3.3 \times 10^{14}$	2.6	n
1322	"	8,200/71,000	$7.6/7.5 \times 10^{14}$	1.0	n
1323	"	270/--	1.0×10^{12}/-	2.3×10^4	n
1324	"	(Grown on p^+ substrate)			
1325	"	690/--	1.0×10^{13}/-	870	n
1326	"	1,200/--	2.5×10^{12}/-	2,200	n
1327	"	(Grown on n^+ substrate)			
1328##	"	8,100/--	2.0×10^{14}/-	3.9	n

*No. 1301 was grown directly from fresh Ga melt and GaAs source without bakeout beforehand.
#No. 1318 shows p-type at room temperature and n-type at liquid nitrogen temperature.
**No. 1319 was grown on oxygen-doped semi-insulating GaAs substrate.
##No. 1328 was grown on Cr-doped semi-insulating GaAs substrate with $\rho = 10^4$ ohm-cm.
†All epitaxial layers were grown on Cr-doped semi-insulating substrates with $\rho > 10^6$ ohm-cm.

concentration and mobility of this layer were high, 6.8×10^{13} cm^{-3} and 7600 cm^2/V-sec, respectively. This may be due to the out-diffusion of oxygen. Another possible explanation is that the O-doped substrate may affect the segregation of impurities differently than the Cr-doped substrate. The carrier concentrations of some other layers, notably those grown after growths on p^+ and n^+ substrates, were also higher than the norm. This may be due to segregation effects in the previous growth which changed the relative concentrations of impurities in the melt and subsequently affected the compensation of shallow impurities. All of these results indicate that in order to grow semi-insulating GaAs epitaxial layers, chromium must be used to form deep levels and the shallow donors and acceptors must be highly self-compensated.

3.1.1.2 Photoluminescence Studies. Photoluminescence measurements were carried out on a series of layers grown from a melt before and after adding 0.5 atomic % of Cr (#1207-1212). The p-type layer, #1207, was grown from an undoped melt, and the n-type layer, #1208, was the first layer grown from the same melt after adding Cr. The photoluminescence spectra of these two layers, Fig. 3.1-1, show mid-band structure centered at 0.816 eV. However, for the layers from subsequent growths, this mid-band structure was not detected. This suggests that the deep level at 0.816 eV is due to oxygen, and when Cr is added to the melt, it reacts with oxygen in the melt to

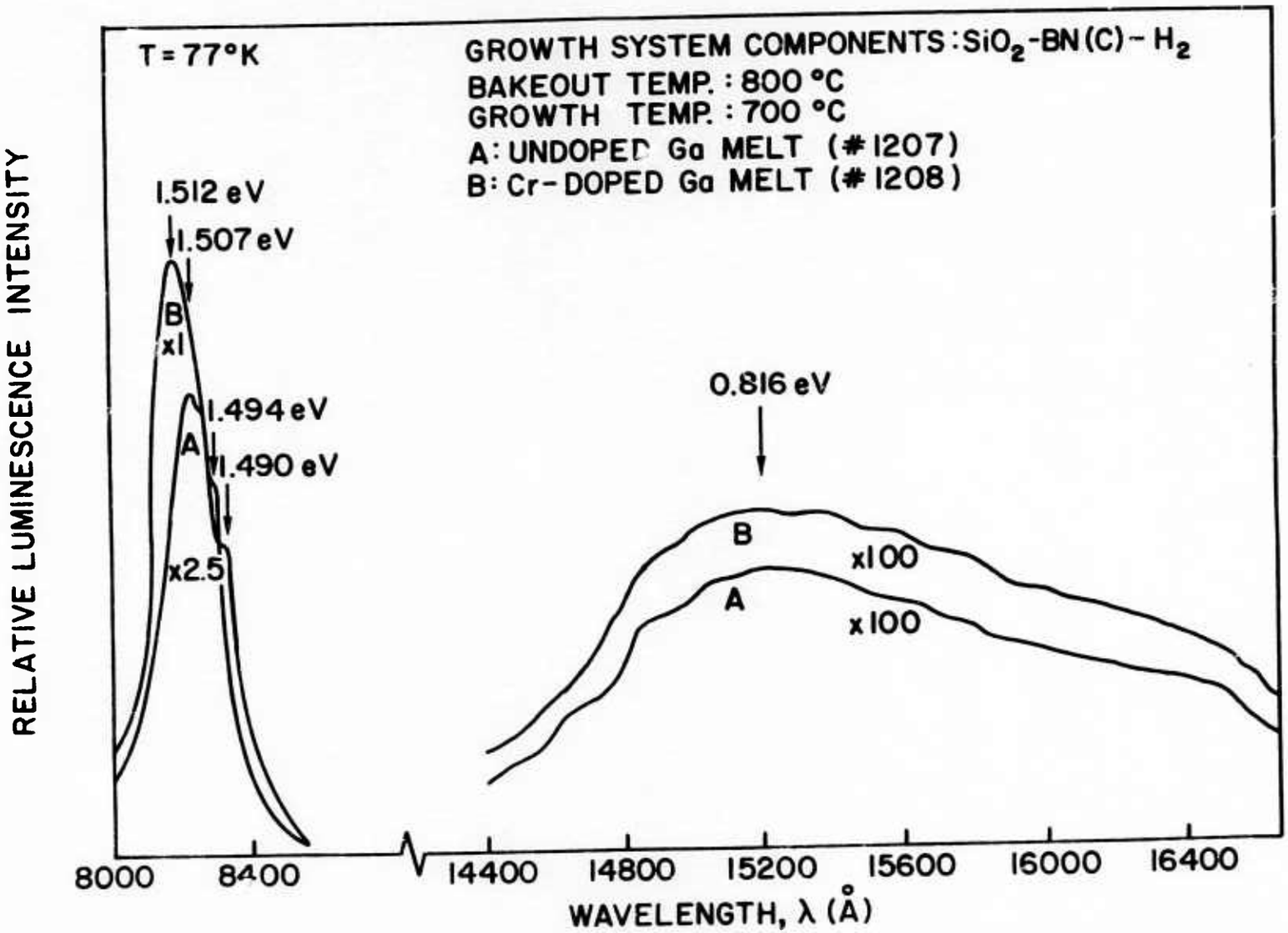


Fig. 3.1-1 Photoluminescence spectra of samples #1207 and #1208.

form an inactive complex which decreases the oxygen concentration in the layer. Chromium may also reduce Si and C oxides in the melt, thus freeing these impurities to be incorporated in the layer.

3.1.1.3 Thermally-Stimulated Capacitance Measurements. For thermally-stimulated capacitance measurements, gold Schottky barriers, 0.15 mm in diameter, were evaporated on n-type epitaxial layers grown from melts baked out at different temperatures (#1106, 1305, 1309, and 1209 with bakeout temperatures of 600°, 700°, and 800°C). The steady-state zero bias capacitances of these devices, Table 3.1-3, are larger at 77 K than at 300 K with one exception, #1309, which was grown from a Cr-doped melt and has a high carrier concentration of 4×10^{15} cm^{-3}. This suggests that some deep levels exist in the layers which are negatively charged (or neutral) at 300 K and are neutral (or negatively charged) at 77 K. The ratio of $C_{77\ K}/C_{300\ K}$ for the layer grown at a higher bakeout temperature is larger than that for layers grown from melts baked out at lower temperatures. This indicates that the incorporation of these deep impurities increases with increasing bakeout temperature of the melt. The activation energy associated with the deep level was also estimated from the thermally-stimulated capacitance measurements. The measurements were conducted as follows: first, the Schottky barrier was cooled down to 77 K under a reverse bias of 20V. At this temperature, all traps were then charged by zero biasing the Schottky barrier. After returning the bias to 20V, the Schottky

Table 3.1-3 Zero Bias Schottky Barrier Capacitance of n-type GaAs Epitaxial Layers

Sample	C(0) 300 K (pF)	C(0) 77 K (pF)	C(0) 77 K/C(0) 300 K
1106	96.09	98.57	1.03
1305	35.78	59.24	1.66
1309	211.5	197.1	0.93
1206	17.74	43.89	2.47

barrier was heated at a heating rate of 0.4°C/sec and the stimulated capacitance response was recorded on the X-Y recorder. Figure 3.1-2 shows the thermally-stimulated capacitance of these samples. From these curves, a temperature T_m was obtained which is the temperature at which dC/dT is maximum. From the value of T_m a crude estimate of the activation energy associated with this deep level can be made by[1,2]

$$\Delta E_t \approx 23\ kT_m \quad .$$

For samples #1106, 1209, and 1305, $T_m \approx 240$ K and $\Delta E_t \approx 0.5$ eV. Sample #1106, which was grown from a melt baked out at 600°C, has a second deep level which is neutral (or positively charged) at high temperatures and negatively charged (or neutral) at low temperatures. The activation energy of this level is ≈ 0.33 eV ($T_m \approx 160$ K).

Further study of these deep levels will be conducted in the near future by varying the heating rate. By analyzing the shift in T_m with heating rate the activation energies of these deep levels can be obtained. From the total change of capacitance due to deep levels, the concentration of the traps associated with these deep levels can be estimated.

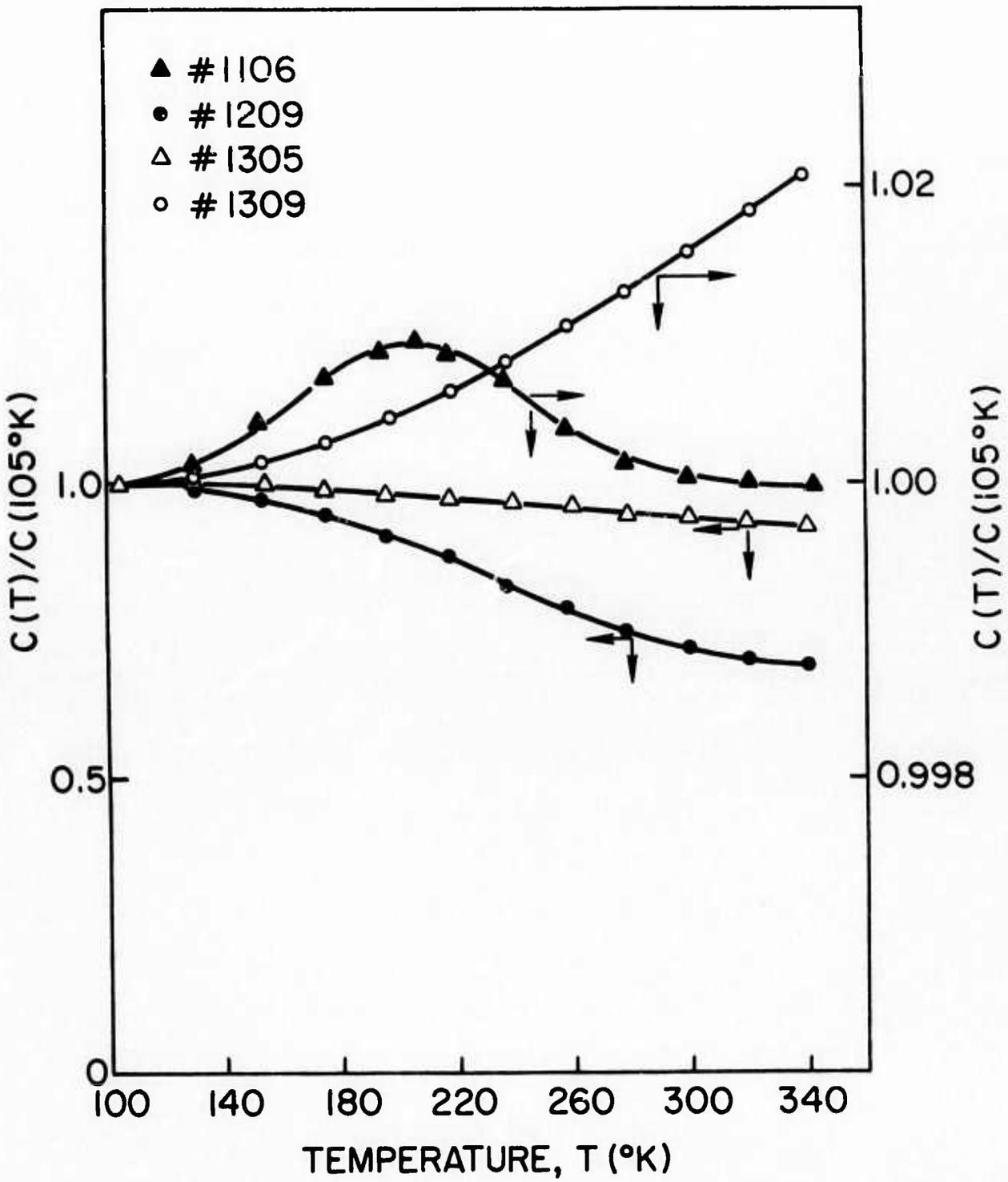


Fig. 3.1-2 Schottky barrier capacitance vs temperature for layers grown from melts baked out at: ▲-600°C; ○-800°C (Cr-doped); △-700°C, ●-700°C (Cr-doped).

3.1.1.4 Impurity Profile Studies. The impurity profiles of the epitaxial layers were determined by using depletion capacitance techniques. This was done by measuring capacitance vs voltage of the Schottky barriers on the epitaxial layers to calculate the net ionized impurity concentration ($N_D - N_A$) vs depth. The impurity concentrations obtained were consistent with the results obtained from Van der Pauw measurements. The impurity profiles along the direction of growth are shown in Fig. 3.1-3 for the three samples (#1106, 1209, and 1305) grown from melts baked out at different temperatures. The thickness of these layers are the same ($\approx 15\mu m$). The impurity profiles are fairly flat in the region within 10μm from the surface but the doping levels decrease toward the substrate interface.

3.1.1.5 Minority Carrier Diffusion Length Measurements. Scanning electron microscope techniques were used to measure the hole diffusion length in sample #1107 which is an n-type LPE layer grown on a p^+ GaAs substrate. Au-Zn and Au-Ge:Ni were evaporated onto the p- and n-sides, respectively, then alloyed at 450°C for three minutes. Several 1 mm × 1 mm diodes were prepared by wire-sawing. An electron beam with an energy of 21 keV and a diameter of 300Å was used to scan across the p-n junction of the diode. Analysis of induced current vs the position of the electron beam indicated that $L_p = 2.3\mu m$, Fig. 3.1-4. The layer had a carrier concentration of 1.5×10^{15} cm^{-3}.

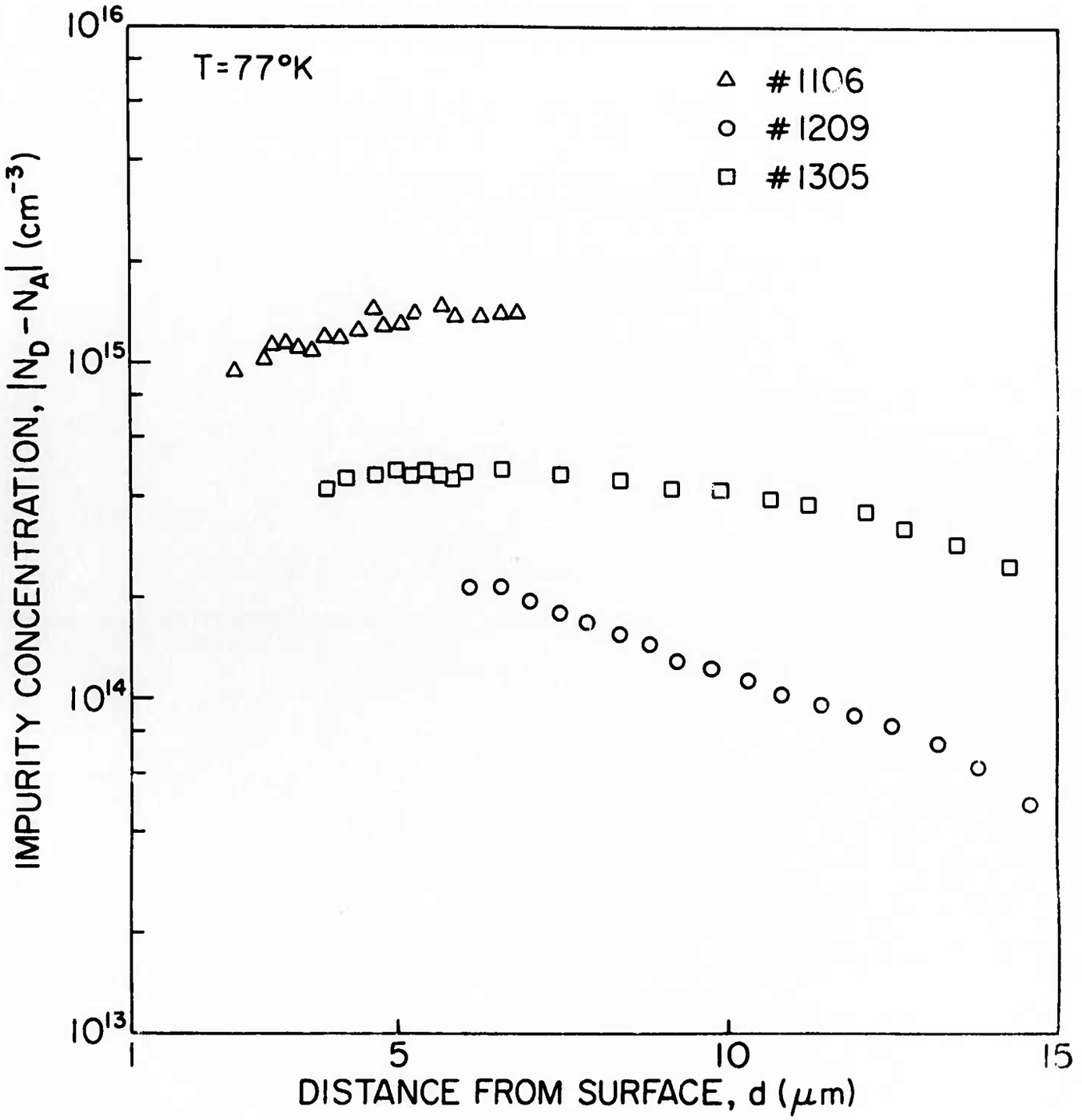


Fig. 3.1-3 Impurity profiles of LPE layers grown from melts with bakeout temperature: △-600°C; ○-800°C; □-700°C.

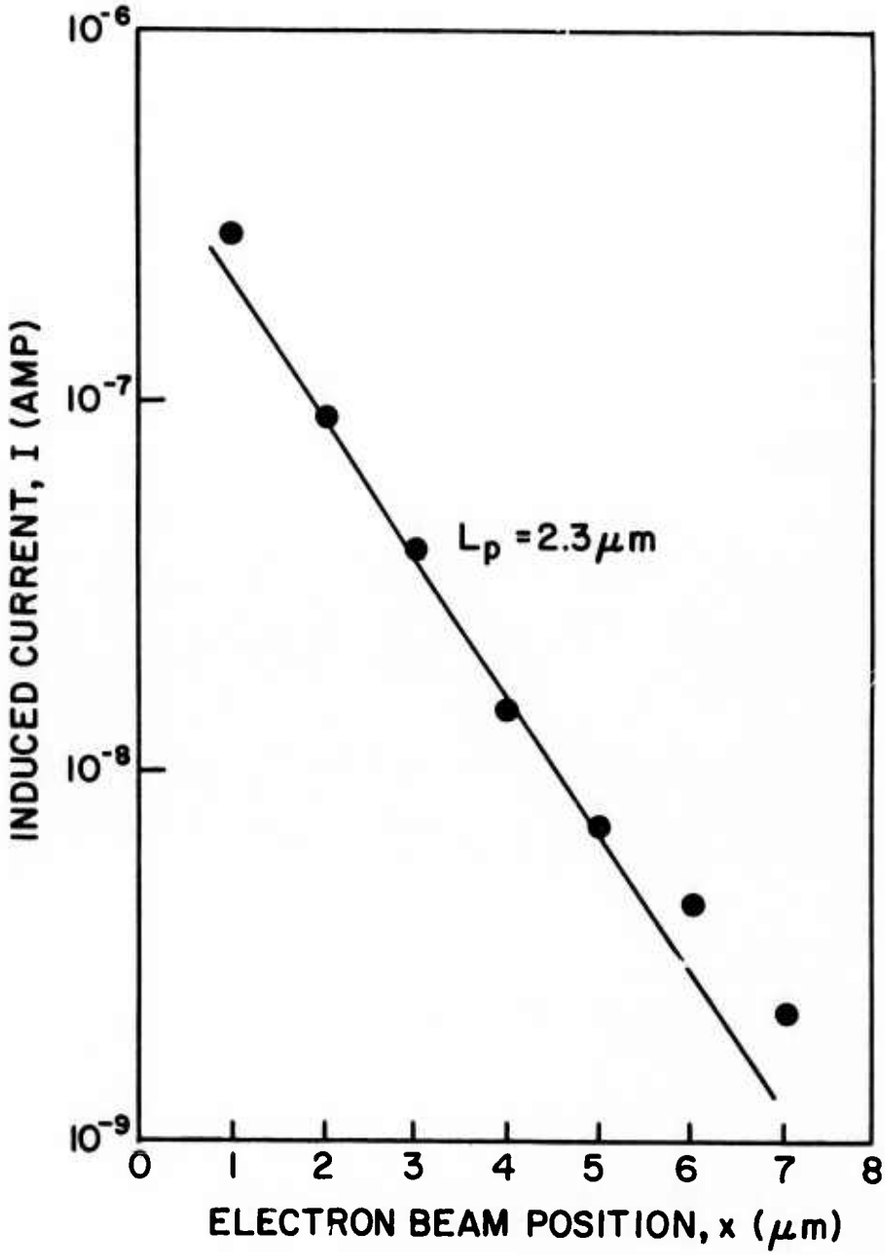


Fig. 3.1-4 Induced current vs electron beam position from the p-n junction of sample #1107 (see text). A scanning electron microscope was used to collect the data.

3.1.2 Multiple Layer Liquid Phase Epitaxy

A primary concern in this effort is the development of techniques at the Science Center which are compatible with the growth of both ultra-thin, high-conductivity epitaxial layers and high-resistivity buffer layers in the same growth cycle. The thin layer growth technique developed at the Science Center under this contract employs an As-saturated Ga melt, confined in thickness by a GaAs source wafer or "roof." To prevent the dissolution of this roof, it is imperative that the bakeout temperature not exceed the growth temperature. From an operational standpoint, considering that a large number of growth cycles may change the chemical composition of the melt if the growth and bakeout temperatures are different, it is advantageous to grow layers at the bakeout temperature.

The key result of the high-resistivity GaAs epitaxial growth studies at Stanford is that, in a given growth system, there exists a bakeout temperature at which shallow donors and acceptors, in an epitaxial layer grown from a systematically baked melt, are self-compensated. Introduction of a suitable impurity into such a properly conditioned melt will introduce a deep energy level in the crystal, resulting in high-resistivity material. This behavior has been observed in systems with SiO_2-C-H_2 as well as SiO_2-BN(C)-H_2 components. Best results to date have been realized with the BN(C) system due, in part, to experimental persistence with this system as well as the understanding gained from the early Cr doping experiments with

the C system. It is felt that results similar to those reported in Section 3.1.1.1 for the BN(C) system can also be expected with the C system. This fact, along with the superior machinability characteristics of high-purity graphite, led to a decision to employ a SiO_2-C-H_2 system for the multiple-layer epitaxy.

During this reporting period, a liquid phase epitaxial system employing a graphite boat with a multi-compartment slider was assembled. Since the transition temperature for such a SiO_2-C-H_2 system is thought to be in the vicinity of 775°C, FET layers were grown at that temperature to determine if the growth rate is compatible with thickness requirements ($\sim$ 0.25 microns for $N_D \sim 1\times10^{17}$). The growth rate increased approximately a factor of 3 over that at the former growth temperature of 675°C. (This is somewhat less than the change predicted by the increased solubility of As in Ga at the higher temperature.) Nevertheless, FET-quality layers were grown at this temperature by decreasing the growth time to approximately 20 seconds. Such a short growth time may adversely affect thickness reproducibility, however. Thus, further optimization of growth rate will be attempted by decreasing the furnace cooling rate, although the effect of a lower cooling rate on the incorporation of Cr into the buffer layer, ideally grown at the same rate, must be investigated.

Several layers were grown from an undoped melt baked out at 775°C. The first layer grown, after a 60-hour bakeout, had a carrier concentration of $\sim 10^{14}$ cm^{-3}, but subsequent layers were in the 10^{15} cm^{-3} range. The addition of 0.5 atom % Cr, with one exception, did not substantially alter the carrier density in the layers. The cause of these results are

being investigated. Mixing of the Sn-doped melt with the undoped melt due to poor wiping or mechanical difficulties in the multi-compartment boat may be a factor.

In spite of the relatively low resistivity (~ 1Ω-cm) buffer material, FET devices were fabricated from a double-layer growth. Reasonable dc characteristics were obtained with transconductances on the order of 5 to 10 millimhos. No RF data is available as yet.

3.1.3 Material Evaluation

3.1.3.1 Characterization of FETs Fabricated on Ion-Implanted and LPE Materials. MESFET devices have been fabricated from starting material prepared by liquid phase epitaxial growth as well as by ion implantation of sulfur and selenium atoms into semi-insulating bulk-grown GaAs. The LPE layers are grown directly on substrates and double-layer systems where the active device layer is deposited on top of a high-resistivity, freshly-grown layer which acts as a buffer layer. This availability of buffered and unbuffered layers provides the opportunity for study of the effects of buffering for LPE-derived devices. Also, substrate materials with known amounts of compensating dopant (normally chromium) are used for the single epi-layer devices so that we may evaluate how critical such considerations are in the design of FETs.

Ion-implanted layers with implanted sulfur have been the main source of our MESFETs. Selenium has also been used to fabricate devices. The MESFET devices have a gate length of 1μm and are single-gate devices; i.e., one gate only between source and drain. The gate width is 500μm and is composed of two 250μm sections. With the ideal layer characteristics this device should provide a frequency of maximum oscillation of approximately 40 GHz providing contact resistance, etc., are within specified limits.

3.1.3.1.1 Effect of Substrate on LPE GaAs FETs. The measurement of MESFET devices at low frequencies is directed to finding how the substrate quality and type affect the device properties. The first measurement is to obtain a trace of the saturation characteristic of the device using a Tektronix 576 curve tracer. The I_{dss} and transconductance are the two most important properties. However, "looping" of the saturation characteristic under conditions of 60 Hz drive on the drain-source bias does indicate a problem due to excessive conduction in the semi-insulating substrate and modulation of the depletion layer at the substrate interface.

Experiments have been conducted where the same type of active layers were grown simultaneously from one melt onto two different substrates of different type and quality. Transistors 43a were fashioned from a layer thus grown on an n^--type substrate (Crystal Specialties #1718) of low-Cr content and

transistors 43b were fashioned from a layer grown on a p^--type substrate of high chromium content (Crystal Specialties #2000, see Sec. 3.2). In Fig. 3.1-5 two traces of FET saturation characteristics are shown--one from each type of device. No excessive looping was noted for either substrate material and the dc properties were remarkably similar.

Some of the dc and RF characteristics of the FETs are shown in Table 3.1-4. The scattering parameters of the two types of devices mounted in a RF chip carrier were measured. They show considerable available gain for both types, and the only discernible difference at microwave frequencies is phase changes in the scattering parameters that consistently make the low chrome substrate transistors more stable than the devices on the p^- substrate.

3.1.3.1.2 Comparison of LPE and Ion-Implanted FETs. Ion-implanted thin n-type layers have been made. From these layers MESFETs have been fabricated. As noted briefly before, there is a distinct improvement in the yield and in the uniformity of electrical characteristics when ion implantation is the source of the material. This is because one variable--the thickness of the active layer--is made to be much more uniform. Figure 3.1-6 shows the spread of I_{dss} of some 21 transistors selected on the basis of being perfect under only visible inspection. Eighty percent of the devices fall in the

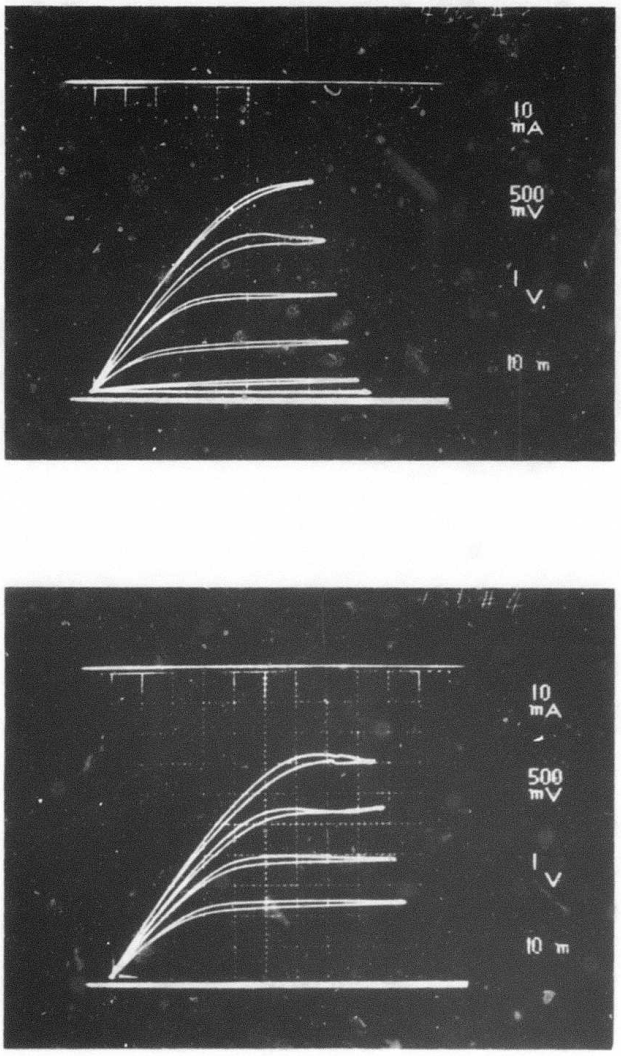


Fig. 3.1-5 Comparison of saturation characteristics of transistors grown on different substrates. Upper trace transistor has an n^- substrate, and the lower trace transistor a p^- substrate.

Table 3.1-4 Characteristics of Epitaxial GaAs FETs on n^-- and p^--type Semi-Insulating Substrates

Transistor	43a	43b
Substrate Type Chromium	n^- $< 10^{16}/cm^3$	p^- $\simeq 8 \times 10^{16}/cm^3$
Approx. Epi-Layer Carriers/Thickness	3.8×10^{16}/5000Å	3.8×10^{16}/5000Å
I_{DSS} Range (Based on 10 each) Maximum g_{mo} Range	70 to 150 mA 20 to 30 mA/V	40 to 120 mA 15 to 25 mA/V
S11 (10 GHz)	.55 /195	.6 /205
S12 (10 GHz)	.041 /60	.05 /40
S21 (10 GHz)	1.0 /50	1.0 /280
S22 (10 GHz)	.9 /285	.9 /280
K Stability Factor	1.14	.86
M.A. Gain	14.2	--

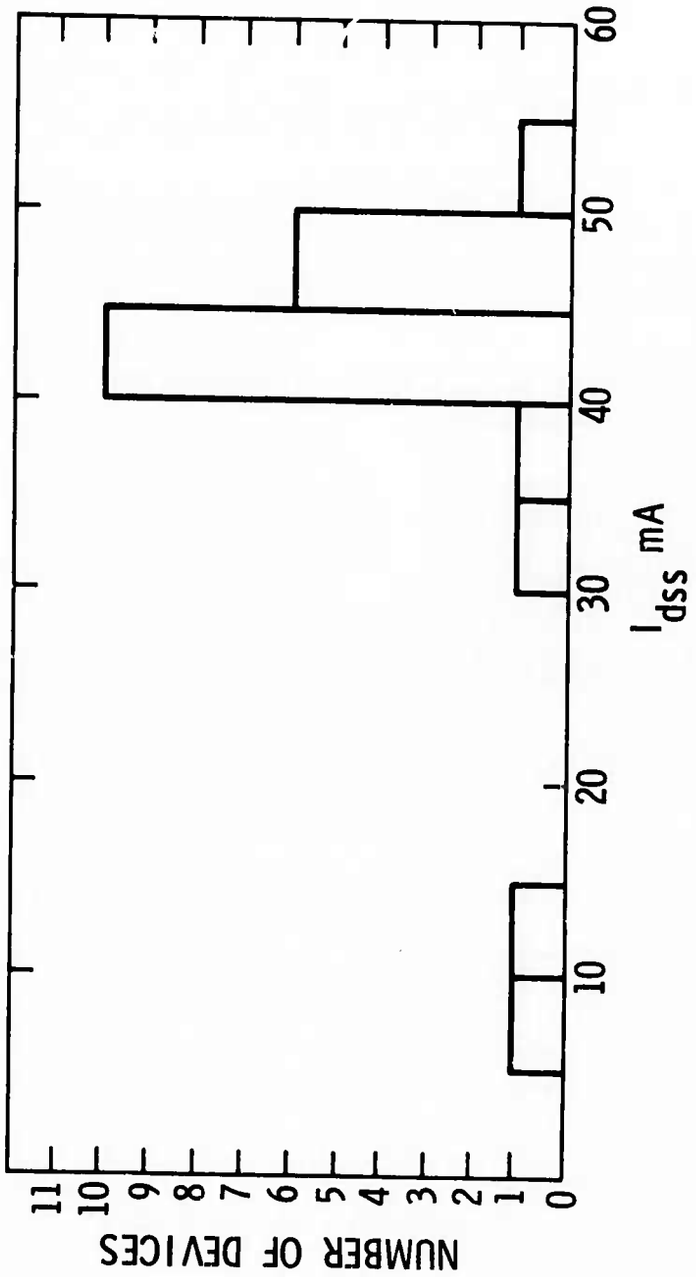


Fig. 3.1-6 Histogram of I_{dss} of 21 ion-implanted FETs from wafer 376.

40-50 mA range. Comparable uniformity from epitaxial layers requires self-limiting etching techniques. Such procedures are yet another complicated and risky step.

The RF performance of our ion-implanted transistors has been compared step-for-step with the transistors fabricated from epitaxial layers. It is found that the ion-implanted devices have, for exactly the same geometry, equal gain performance and possibly better noise performance. Figure 3.1-7 gives a comparison of the levels of performance as of June, 1975. The figure of gain vs frequency is for an epi-transistor. It is representative of the gain bandwidth available when the transistor is biased to low current to obtain optimum noise while the input is tuned for maximum gain.

When tuning the input circuit to a transistor for optimum noise, the best noise figure so far observed at 10 GHz for an ion-implanted transistor is 4.6 dB. The associated gain was approximately 4 dB. The improved noise performance in implanted FETs is presently attributed to the lack of an interface between the semi-insulating substrate and the active device layer.

3.1.3.2 Low-Frequency Noise Behavior of Avalanche Diodes. In studying the low-frequency noise of steady p-n junction avalanches, Haitz pointed out[3] the sensitivity of such measurements to the quality of the junction; inhomogeneities over the surface of the

PERFORMANCE LEVELS

	EPITAXIAL	ION-IMPLANTED
GAIN AT 10 GHz M.A.G. MEASURED	10 dB	10 dB
NOISE FIGURE TUNED FOR MAXIMUM GAIN	7.25 dB	5.7 dB
3RD ORDER INTERMODULATION INTERCEPT POINT	> +16 dBM	> +16 dBM

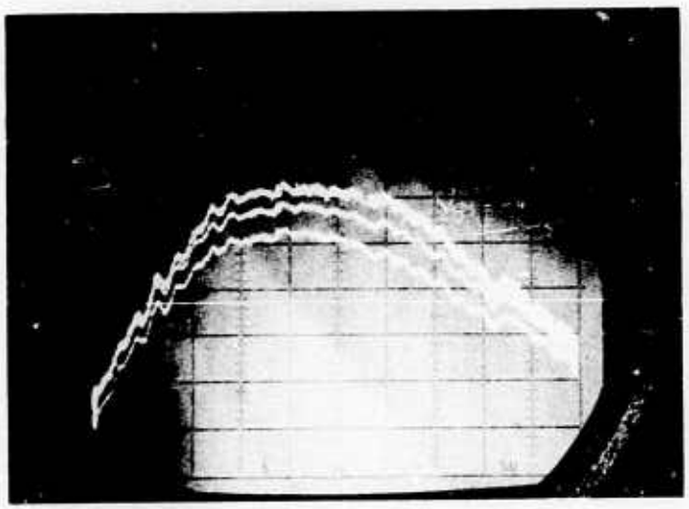


Fig. 3.1-7 Performance of epitaxial and ion-implanted GaAs FETs.

diode tended to produce very irregular noise as a function of the bias current. Although a number of detailed analyses of noise have been made,[4,5] the emphasis has been on the microwave performance of the diodes. In addition, there have been some reports noting the proportionality of the low-frequency noise to the reciprocal of the bias current.[6,7] Apparently no attempt has been made to analyze the noise behavior as a function of current from the onset of breakdown to normal operating bias currents in order to extract useful parameters of the diode.

An analysis of the short-circuit noise current is presented here and it is shown how experimental data may be fitted to uniquely determine the multiplication and the saturation current at the noise peak. Uniform diodes are shown to fit the theory very closely and for mildly-pathological diodes these parameters can still be obtained with reasonable accuracy. One of the most persistent difficulties in the manufacture of avalanche diodes has been and is now the control of generation centers in the active region. The low-frequency noise yields a qualitative measure of the density of those generation centers in the avalanching mode.

Experimentally one observes the short-circuit current noise to increase sharply with the onset of breakdown, but a peak is quickly reached at a few milliamperes and then the noise subsides smoothly if the diode is reasonably uniform. In a qualitative way one may understand the decreasing current fluctuations as being due to

compensating effects of space charge in the drift region. These effects are described by the balance equation of Read

$$\mathcal{E}_m(0,t) = \mathcal{E}_{po} + \frac{1}{w}\left\{V(t) - V_{po} - \frac{1}{\varepsilon}\int_0^w \rho(x)(w-x)dx\right\} \quad . \tag{1}$$

Equation (1) can be adapted to the case of a diode with a finite avalanche region to give the field fluctuations arising from the short-circuit noise current in the drift region

$$d_1 = -(1/\varepsilon v_s w) \int_{x_1}^{w} [J_a + J(d_1)](w-x)\exp[-j\omega(x-x_1)/v_s]dx \quad , \tag{2}$$

where J_a is the primary noise current and $J(d_1)$ is the additional current response of the avalanche caused by the voltage across the drift region. If one wished to consider a double-drift diode, then Eq. (2) would be modified by the addition of a similar integral over the electron charge in the region $(0,x_1')$ to the left of the avalanche region. Performing the integration in Eq. (2) one obtains

$$\varepsilon\omega d_1 = j[J_a + J(d_1)](1-f)(1-x_1/w) \quad , \tag{3}$$

where the transit angle delay is given by

$$f = [\sin\psi - j(1 - \cos\psi)]/\psi \quad .$$

The avalanche current generated in response to the ac field d_1 is

$$J(d_1) = \varepsilon\omega d_1 \beta\theta/(1 + j\theta) \quad , \tag{4}$$

where in the notation of the "quasi-static" approximation[8]

$$\beta = MJ_s|a_1|/\varepsilon\omega^2 \quad , \quad a_1 = \partial(1/M\tau_1)/\partial\mathcal{E}_c, \quad , \quad \text{and } \theta = M\omega\tau_1 \quad .$$

Substituting Eq. (4) into (3) gives the avalanche field perturbation caused by the primary noise current

$$\varepsilon\omega d_1 = j(1-f)J_a/[1 - j(1-f)\beta\theta(1-x_1/w)/(1+j\theta)] \quad . \tag{5}$$

The total short-circuit noise current then is the sum of the primary noise current, the responding current $J(d_1)$, and the displacement current

$$\begin{aligned} J_{tot} &= J_a + J(d_1) + j\varepsilon\omega d_1 \\ &= J_a\{(1+j\theta)[f(1-x_1/w) + (x_1/w)]/[1+j\theta-j(1-f)\beta\theta(1-x_1/w)]\} \quad . \end{aligned} \tag{6}$$

Multiplying the current described by Eq. (6) and taking the mean square one obtains in the limit of small transit angle

$$\langle i^2 \rangle = \langle i_a^2 \rangle [(1+\theta^2)[1-\psi^2(1+3x_1/w)(1-x_1/w)/12]/ \{[1+\beta\theta\psi(1-x_1/w)/2]^2 + \theta^2[1-\beta\psi^2(1-x_1/w)/3]\}] \quad . \tag{7}$$

The primary noise current is taken from Naqvi[9]

$$\langle i_a^2 \rangle = 2eI_{sn}M_n^3\Delta f[1-(1-k)(1-M_n^{-1})^2]/(1+\theta^2) + 2eI_{sp}M_p^3\Delta f[1-(1-k^{-1})(1-M_p^{-1})^2]/(1+\theta^2) \quad , \tag{8}$$

where $k = \beta/\alpha$ is assumed to be a constant ratio. For the remainder of this discussion k will be assumed to be unity, partly because $I_s M_{pk} = I_{pk}$ is independent of k so that fitting the peak or the tail region is not affected and partly because of the experimental uncertainty in k. With this assumption concerning k Eq. (7) takes the form

$$\langle i^2 \rangle = 2eI_s M^3 \Delta f[1-\psi^2(1+3x_1/w)(1-x_1/w)/12]/ \{[1+\beta\theta\psi(1-x_1/w/2]^2 + \theta^2[1-\beta\psi^2(1-x_1/w)/3]\} \quad . \tag{9}$$

Now let us examine Eq. (9) in the limits of small and large currents. For small currents

$$\lim_{I\to 0}\langle i^2\rangle = 2eI_s M^3 \Delta f[1-\psi^2(1+3x_1/w)(1-x_1/w)/12]/(1+\theta^2) \quad , \tag{10}$$

and for large currents

$$\lim_{I\to\infty}\langle i^2\rangle = 8e\varepsilon^2 v_s^2 A^2 \Delta f/I|a_1\tau_1|^2(w-x_1)^2(1-x_1/w)^2 \quad . \tag{11}$$

Note that the short-circuit noise current is inversely proportional to the bias current in a manner similar to the open circuit noise voltage.

In order to discuss fitting Eq. (9) to experimental data it is convenient to explicitly introduce the bias current

$$\langle i^2\rangle = a'I^3/[1(1+b'I^2)^2 + c'I^2(1-d'I)] \quad , \tag{12}$$

where $a' = 2e\Delta f/I_s^2$,

$b' = \mathscr{E}_m|a_1\tau_1|(w-x_i)(1-x_1/w)/\mathscr{E}_m 2\varepsilon v_s A I_s$,

$c' = (\varepsilon\tau_1/I_s)^2$,

$d' = |a_1|(w-x_1)^2(1-x_1/w)/3\varepsilon v_s^2 A$.

Differentiating Eq. (12) with respect to the current and setting the result equal to zero, one obtains

$$b'I^2 = (1+c'/2b') + [(1+c'/2b')^2 + 3]^{1/2} \quad . \tag{13}$$

By taking the noise measurements at a sufficiently low frequency, one can always make $c'/2b'$ negligible and then

$$b'I_{pk}^2 = 3 \tag{14}$$

at the noise peak. Since b is inversely proportional to I_s one comes to the result that $I_{pk}M_{pk}$ is a constant. Furthermore, the constant can be evaluated from the high current limit given in Eq. (11). Finally

$$I_{pk}M_{pk} = 3(I\langle i^2\rangle/2e\Delta f)^{1/2} \quad , \tag{15}$$

where the right-hand side is evaluated at high current.

The analysis of the experimental low-frequency noise data of a variety of silicon and GaAs avalanche diodes, shown in Table 3.1-5, has been made with very interesting results. One would expect that silicon would be more uniform and thus fit the theory better and that indeed is the case as is shown in Fig. 3.1-8. The diode is a high-quality X-band IMPATT manufactured by Hughes Aircraft Co. The saturation current density is approximately .007 A/cm^2 and although this is a low value for silicon IMPATTs it is still about three orders of magnitude higher than one would expect from the

Table 3.1-5 Parameters Describing Low-Frequency Noise Spectra of Si and GaAs IMPATT Diodes

	Si C-6	GaAs 4A-8	Si 2-22	
$I\langle i^2\rangle$	4.3×10^{-13}	6.2×10^{-14}	2.0×10^{-13}	1.0×10^{-13}
$M_{pk}I_{pk}$	4.16	1.58	2.84	2.05
I_{pk} (A)	.0028	.0075	.0027	.0014
M_{pk}	1480	209	1050	1470
I_s (A)	1.89×10^{-6}	36.1×10^{-6}	2.51×10^{-6}	$.95\times10^{-6}$
$a' = 2e\Delta f/I_s^2$	.0630	1.72×10^{-4}	.0337	.249
$b' = (a'/I\langle i^2\rangle)^{1/2}$	3.83×10^5	5.82×10^4	$4\times10\times10^5$	1.54×10^6
$c' = (\omega\tau_1/I_s)^{1/2}$	9.0×10^4	246.	4.80×10^4	3.56×10^5
$d' = (2b'\psi/3c'^{1/2})$	4.01	10.6	5.88	8.11
τ_1(sec) assumed	3×10^{-12}	3×10^{-12}	3×10^{-12}	3×10^{-12}
f (MHz)	30	30	30	30
ψ(rad.) assumed	.0047	.0047	.0047	.0047

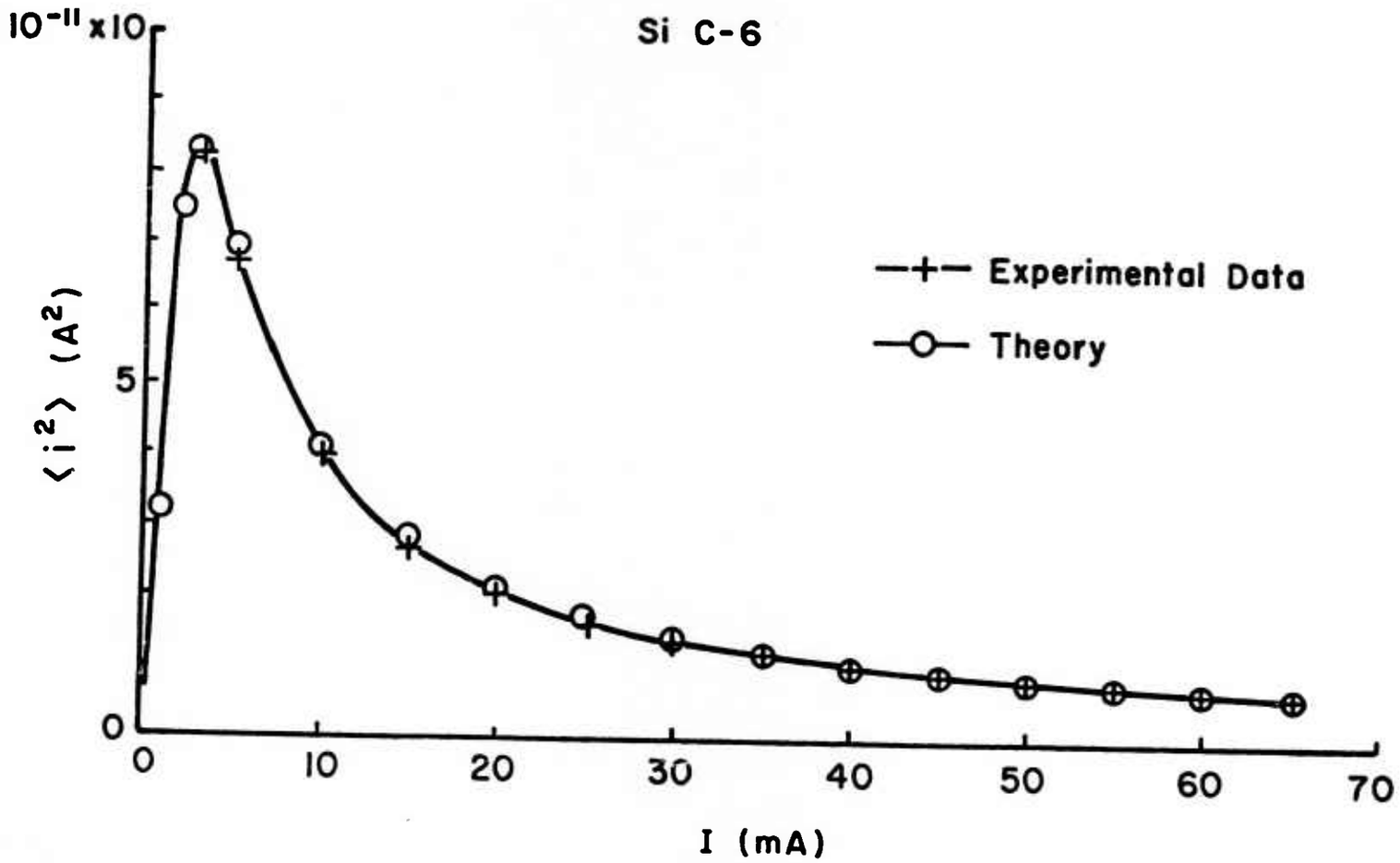


Fig. 3.1-8 Fit of the experimental short-circuit current noise data of a uniform silicon IMPATT by Eq. (13) using the parameters given in Table 3.1-1.

best available bulk silicon. The multiplication is about 1500 at the noise peak and may rise an order of magnitude at operating currents depending upon the temperature dependence of the saturation current.

The next example is a flat profile GaAs IMPATT manufactured by Raytheon and is illustrated in Fig. 3.1-9. Note that in spite of pronounced irregularities in the noise data the agreement with theory is still quite good. In contrast to the silicon diode the the multiplication is only around 200 at the noise peak and the saturation current is some 20 times higher. The saturation current density is greater than 0.1 A/cm^2. For some of the GaAs Read structures the saturation current density is even higher. A reasonably high saturation current seems to result in lower noise, but in a number of diodes the saturation current is high enough to deteriorate the avalanche phase lag at microwave frequencies and to make the diode operate perilously close to thermal runaway.

A mildly pathological diode is shown in Fig. 3.1-10. This is a silicon diode with no gross microplasmas but with either residual inhomogeneities or a current-dependent saturation current. A reasonable estimate of the multiplication and saturation current can still be made for this diode in spite of the distortions which are believed to be caused by a nonuniform avalanche.

3.1.3.3 Ionization Rate Study in GaAs. The ionization rates of holes and electrons are reported not equal in GaAs by Stillman,

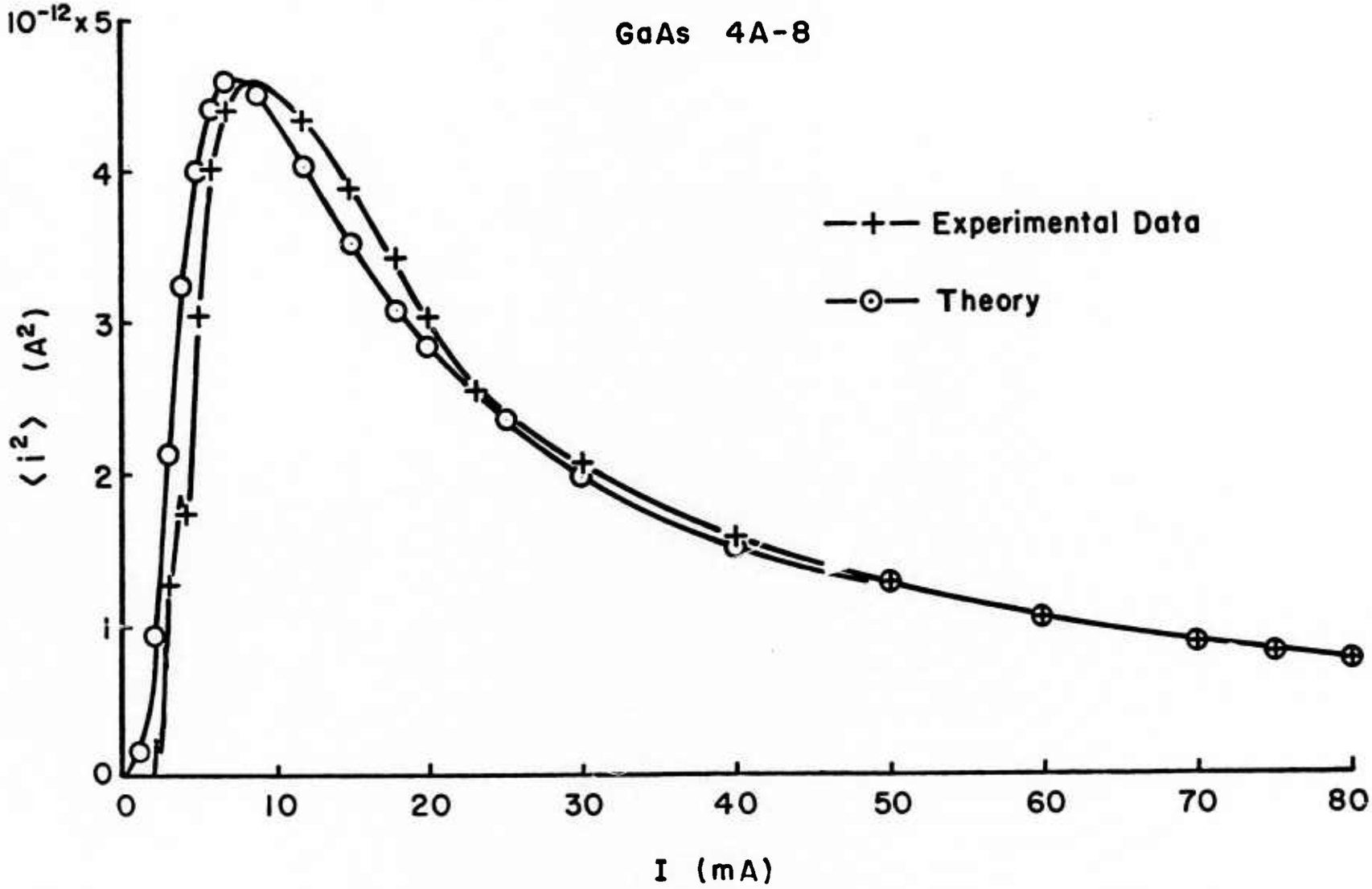


Fig. 3.1-9 Short-circuit current noise data and theoretical fit of Eq. (12) for a GaAs flat profile IMPATT; for this diode $M_{pk} \approx 200$ and the saturation current is an order of magnitude larger than that of the silicon diode shown in Fig. 3.1-8.

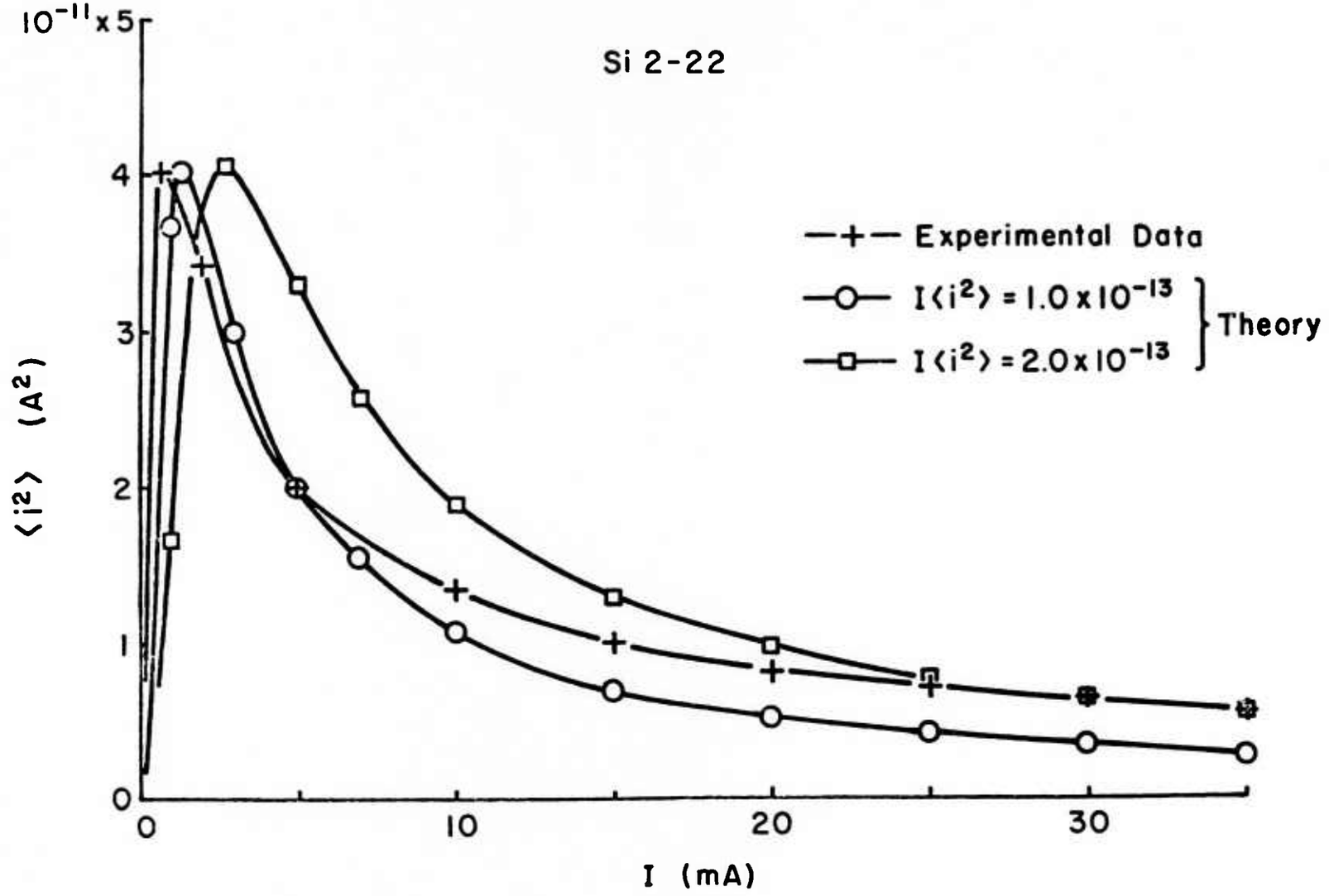


Fig. 3.1-10 Short-circuit current noise data of a silicon IMPATT for which the theoretical fit of Eq. (12) is rather poor, presumably because of non-uniformity of the avalanching zone.

et al.[10] To achieve an accurate measurement of the ionization rates, pure holes and pure electrons must be injected in a same junction. Figure 3.1-11a illustrates the structure which allows pure injection of holes and electrons. When light of frequency ν such that $E_g > h\nu > \theta$ (where E_g = bandgap of GaAs; θ = Schottky barrier height) is shone on the gold of the Schottky barrier, pure electron injection results. On the other hand, pure hole injection can be achieved by shining light with frequency ν such that $h\nu > E_g$ from the back of the diode. The generated minority carriers will diffuse to the junction to provide the needed holes.

A preliminary measurement on the Rockwell S11-5 diodes indicated that they were free of microplasmas and would be suitable for multiplication measurement. The sample was lapped down to ~ 7 mil thickness before it was masked with black wax. A small hole opposite to a diode was exposed, Fig. 3.1-11a. The hole was then electrolytically etched out as shown in Fig. 3.1-11b. The electrolyte used in this process was three parts CH_3COOH and one part $HClO_4$. The voltage source was set at 20V. The etching rate was nonlinear with time. It was believed that a white film built up on the surface after etching for some time limited the current flow and thus decreased the etching rate. Therefore, the sample was taken out and the white film was washed away with de-ionized water every two minutes. In that case, the etching rate was approximately 1 mil for every two minutes. This process was stopped

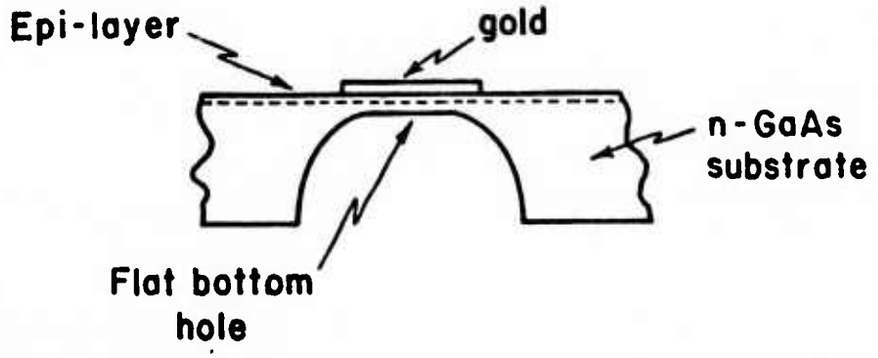


Fig. 3.1-11a Structure of dimpled diode for the separate injection of pure electron or hole current.

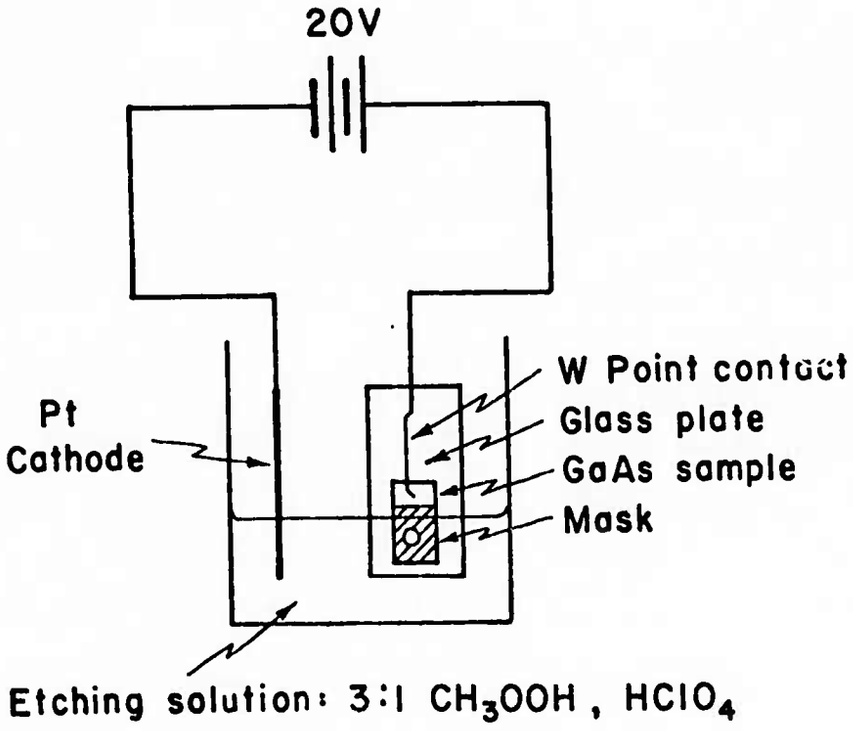


Fig. 3.1-11b Arrangement of the electrolytic cell for etching the dimple in the substrate.

when the thickness of the diode was less than 1.5 mil. A shiny flat bottom hole was obtained.

Capacitance vs bias voltage measurement was used to find the doping profile of the diode. The curve C^{-2} vs V is given in Fig. 3.1-12 and the doping profile is shown in Fig. 3.1-13. It was found that the doping close to the epi-layer surface was 1.4×10^{16} and around 0.8μm the doping changed abruptly to 2.0×10^{16}. These values are in good agreement with those measured at the Science Center of Rockwell International.

Homogeneity of the electric field inside a diode affects its performance. Especially for multiplication measurements, the field has to be very homogeneous inside. This sensitivity of the multiplication to electric field occurs because the ionization rates are strong functions of electric field. Thus, an inhomogeneous field will cause a large error in the calculation of the peak field. The homogeneity of the diode was tested before multiplication was measured to ensure accurate results. A focused laser beam was scanned across the diode while the photoresponse was measured. For the diode selected from sample S11-5 the same amount of multiplication was observed in different areas of the diode. This diode was the most homogeneous one over the whole area of the sample.

The setup for multiplication measurement was the same as that used by Lee, et al.[11] Light sources were taken from a He-Ne laser and a tungsten bulb. A green filter was also used to filter the

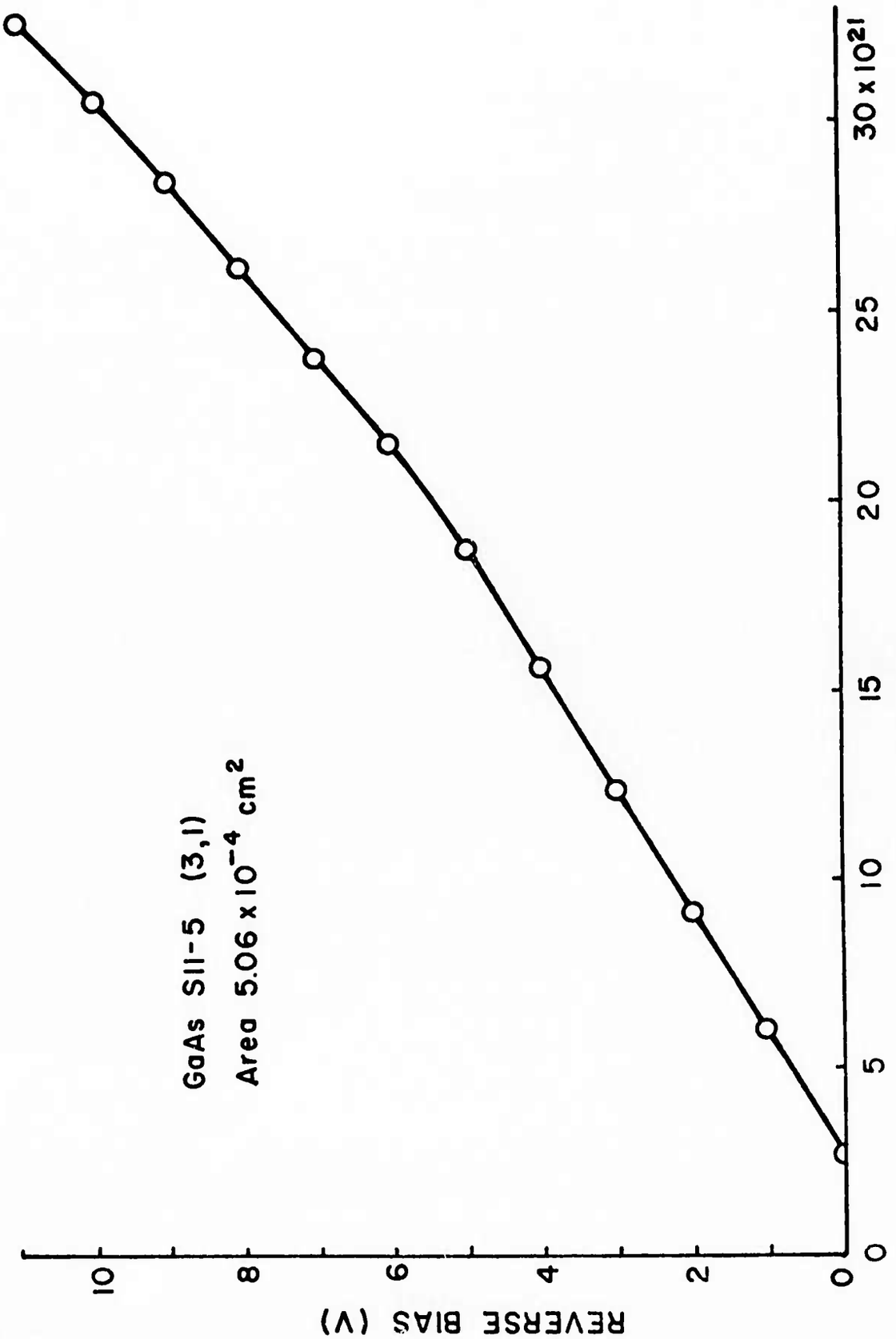


Fig. 3.1-12 Capacitance vs voltage of the gold Schottky barrier diode on wafer S11-5 for which multiplication data is presented.

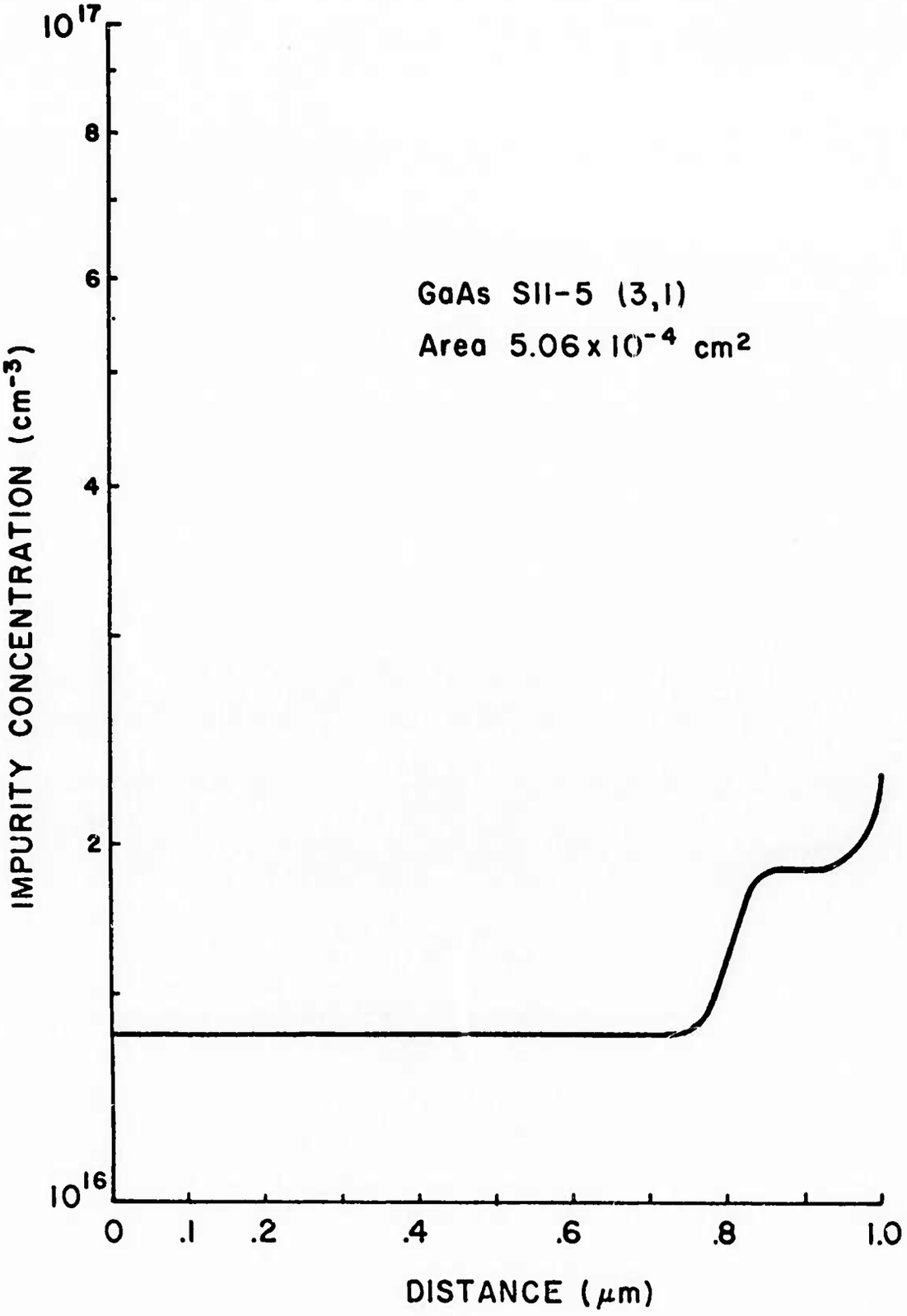


Fig. 3.1-13 Donor density as a function of depth in the epitaxial layer deduced from the capacity data of Fig. 3.1-12.

tungsten bulb. Different wavelengths of light were shone on top and from back of the diode. In all cases, sloping base lines were observed. This was partly due to the Schottky lowering effect of the barrier and partly due to the traps inside the epi-layer. For different wavelengths of illumination, different signal phases were observed on the lock-in amplifier. This further verified the presence of the traps. By extrapolating the base line from the low bias values, a plot of multiplication of holes and electrons vs bias voltage is given in Fig. 3.1-14.

Comment

The uniformity of doping over the whole area of a diode seems to be better in the sample S11-5 than in S11-4. However, an abrupt change in doping at ~ 0.85μm in S11-5 is still present. In both S11-4 and S11-5, deep level traps are present.

The multiplication measurement on S11-5 indicates that $\beta > \alpha$ in this field range (2.5×10^5 to 3.1×10^5 V/cm). However, multiplication measurements on S11-4 [experiment was carried out under the same conditions as in S11-5], α seems to be larger than β as shown in Fig. 3.1-15. In the case of S11-4, the field range is from 1.13×10^5 to 1.69×10^5 V/cm. The published data for α and β by Logan and Sze[12] which indicates $\alpha \cong \beta$ are in the intermediate field range. The measurements reported here do not contradict the results published by Logan and Sze.

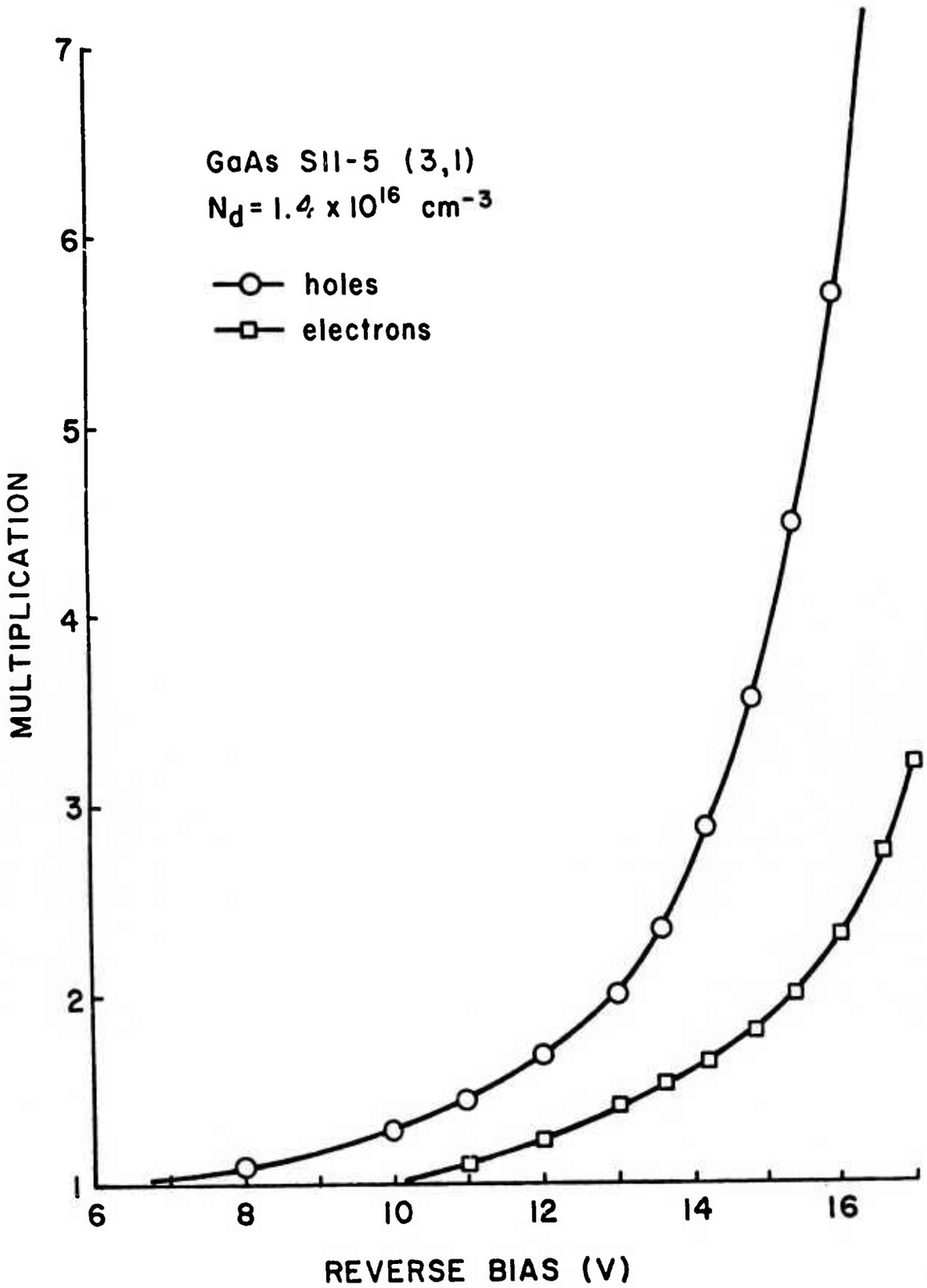


Fig. 3.1-14 Multiplication data for the more heavily-doped wafer ($N_d = 1.4 \times 10^{16}$ cm^{-3}) where the hole ionization coefficient exceeds that of the electrons.

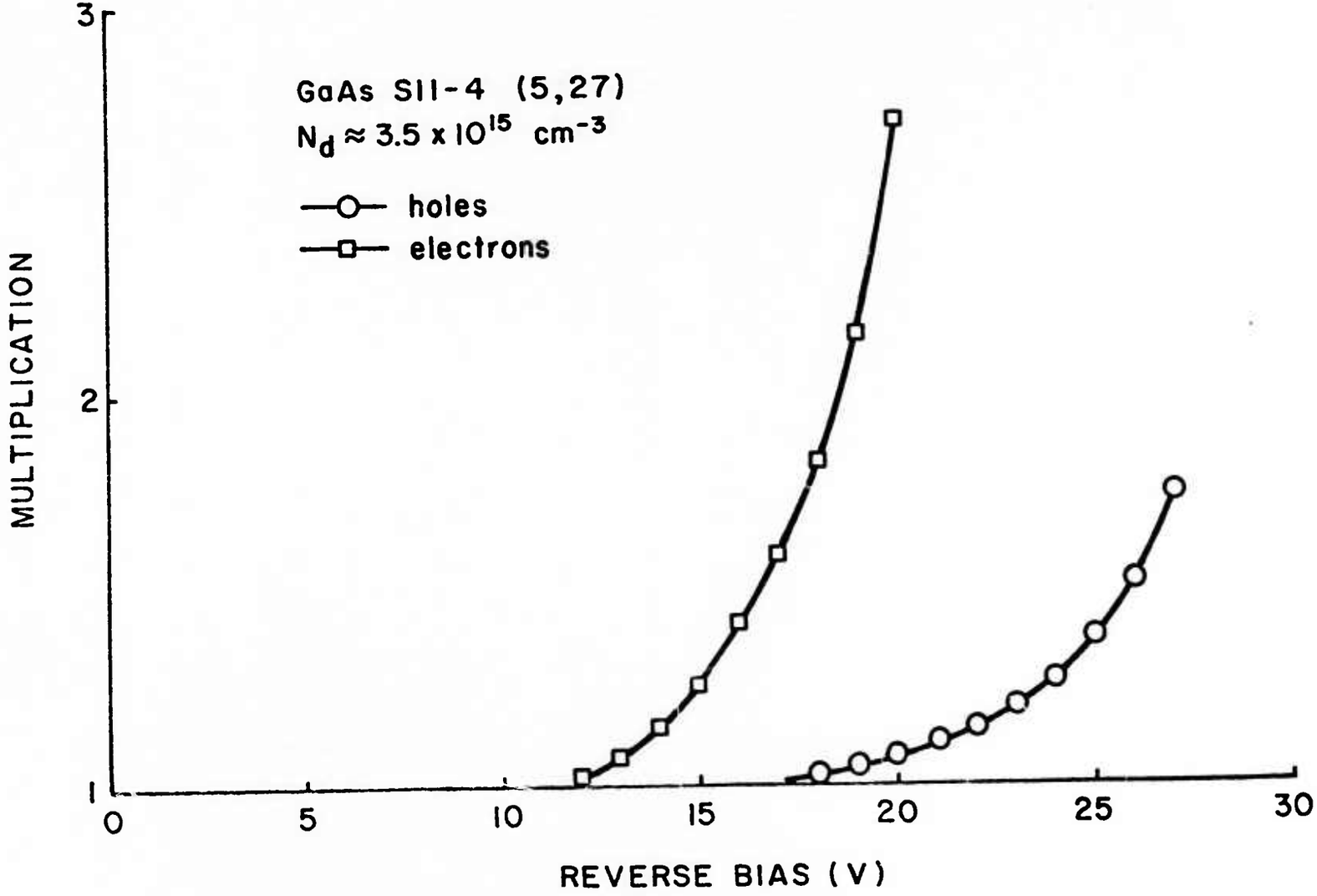


Fig. 3.1-15 Multiplication data for the lightly-doped wafer ($N_d = 3.5\times10^{15}$ cm^{-3}) where the electric field in the avalanche is much lower than for any previously published data and the ionization coefficient of electrons exceeds that of the holes.

3.1.3.4 Surface Passivation by Anodic Oxidation of GaAs. A number of reports have recently appeared[13,14] concerning the anodic oxidation of GaAs which utilize non-aqueous solvents. These solutions purport to give higher quality oxide films, in terms of density and and resistivity, than previously proposed aqueous solutions.[15,16] The deficiencies of these aqueous solutions variously involved dissolution of the oxide during growth, stability of the solution against impurities, and a tendency to produce a porous oxide of relatively low resistivity and dielectric strength.

In this section we present a new aqueous solution for the anodic oxidation of GaAs which produces films of equal quality compared to those produced by solutions containing non-aqueuous solvents and which is advantageous in a number of other respects. This new solution utilizes a common salt that is quite inexpensive compared to solutions containing ethylene glycol, or N-methylacetamide and is quite safe to handle as opposed to solutions of 30% hydrogen peroxide. Moreover, this new aqueous solution is more versatile in that it has been found to produce high-quality anodic oxide films on silicon, indium antimonide, and indium phosphide.[17] A particular advantage of this new solution applied to silicon is that the anodic oxide films can be made free of alkali ions by treating the solution with ion exchange resins. Thus passivating oxide films can be anodically formed on silicon of several thousand ohm-cm resistivity without inducing surface inversion layers.

The basic electrolyte is a 0.1 molar solution of dibasic ammonium phosphate in distilled water. Although this solution may be used directly for silicon, InSb, or InP, the pH of the solution is adjusted to a value of 4 by the addition of phosphoric acid when used with GaAs to prevent dissolution of the oxide film.

The experimental arrangement for preparing the films described below was to immerse an appropriately masked sample into a beaker of the solution and record the breakdown voltage of the film as a function of the time for a specified current. The masking technique employed was to anodize a polished sample of GaAs and mask it with Apiezon wax leaving a window of known area. The window and a contacting area were then cleared of oxide with hydrochloric acid prior to anodizing the area in the window. The GaAs wafers used in these experiments were of heavily-doped n-type substrate material. The anodization was carried out with the sample illuminated by a microscope lamp which served to reduce the contact potentials, but was otherwise not deemed necessary to obtaining good anodic films.

The first films were formed in an unbuffered solution (pH $\simeq$ 7) and the cell voltage vs time for several current densities is shown in Fig. 3.1-16. Note that for the lowest current density the cell voltage does not increase linearly with time, indicating a slight dissolution of the oxide. An oxide film of several thousand Angstroms was observed to dissolve if left overnight in the unbuffered solution.

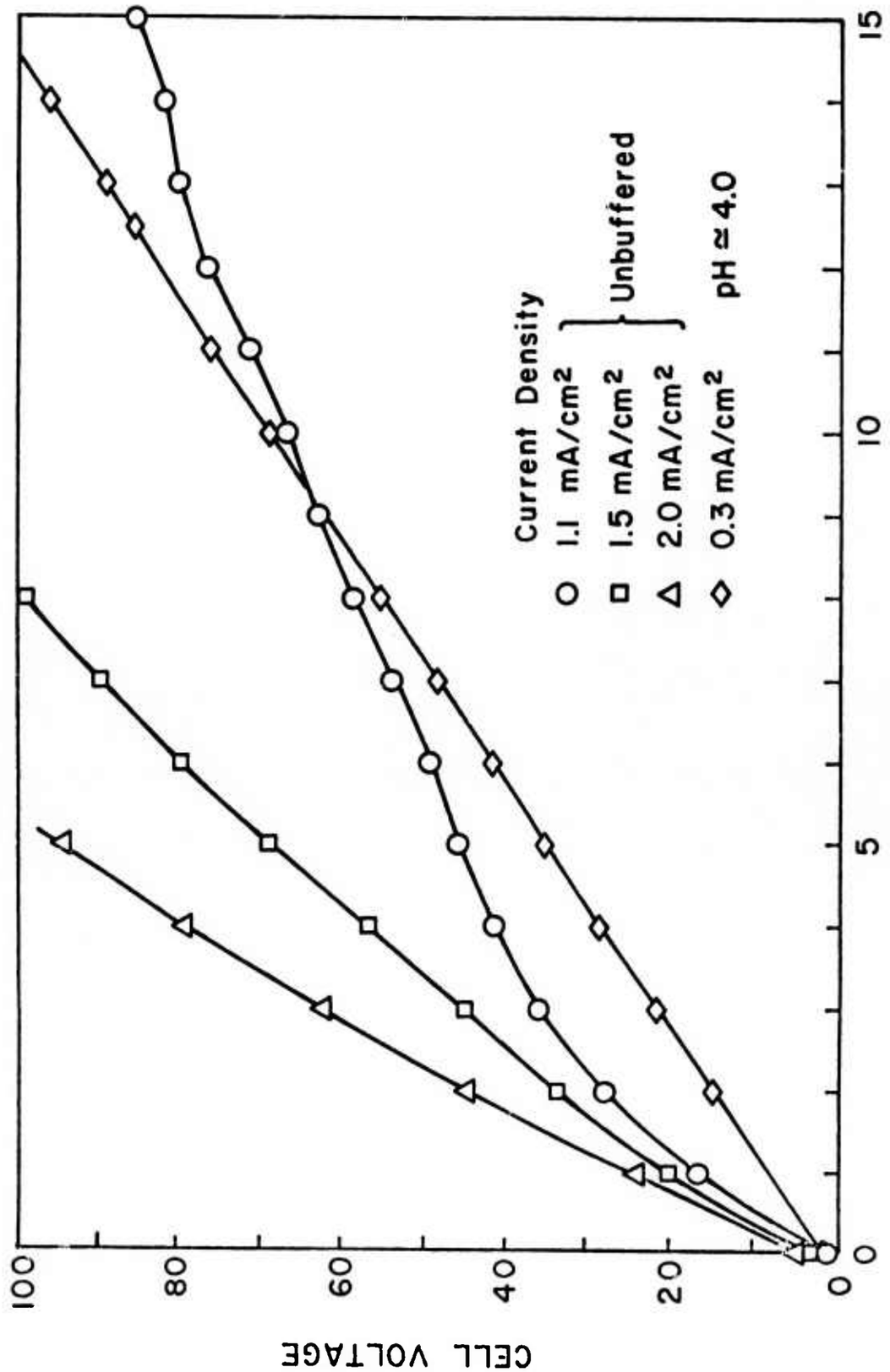


Fig. 3.1-16 Cell voltage vs time as a function of current density for buffered and unbuffered solutions.

Buffering the solution to a pH of 4 with phosphoric acid reduces the solubility of the film to a completely negligible value. The cell voltage vs time for this buffered solution, as also shown in Fig. 3.1-16 for 0.3 mA/cm^2, is quite linear down to the lowest measured current densities (~ 20μA/cm^2). Figure 3.1-17 shows that the rate at which the oxide film is formed is linearly proportional to the current density although the rate changed with solution concentration. Film thickness was measured by a Zeiss interference microscope and it agreed with published data.[13,15] The breakdown field in the oxide was observed to be at least 5×10^6 V/cm. Somewhat thicker films could be grown in a boiling solution as has been described by Spitzer, et al.[16]

3.2 Semi-Insulating Substrate Materials

3.2.1 Crystal Growth

It was pointed out in previous reports[18] that all semi-insulating GaAs grown in fused quartz boats by the horizontal Bridgman or gradient freeze methods required the addition of both chromium and oxygen to the growth ampoule. The addition of oxygen was found necessary to prevent the reduction of the quartz (SiO_2) and the resulting contamination of the GaAs by silicon. It was also necessary to maintain the entire growth ampoule at a minimum temperature of 900°C, to achieve effective compensation by this method. During the last six-month period, the arsenic (low temperature) zone of the growth ampoules was held at a temperature of 1000°C in all of the growth runs.

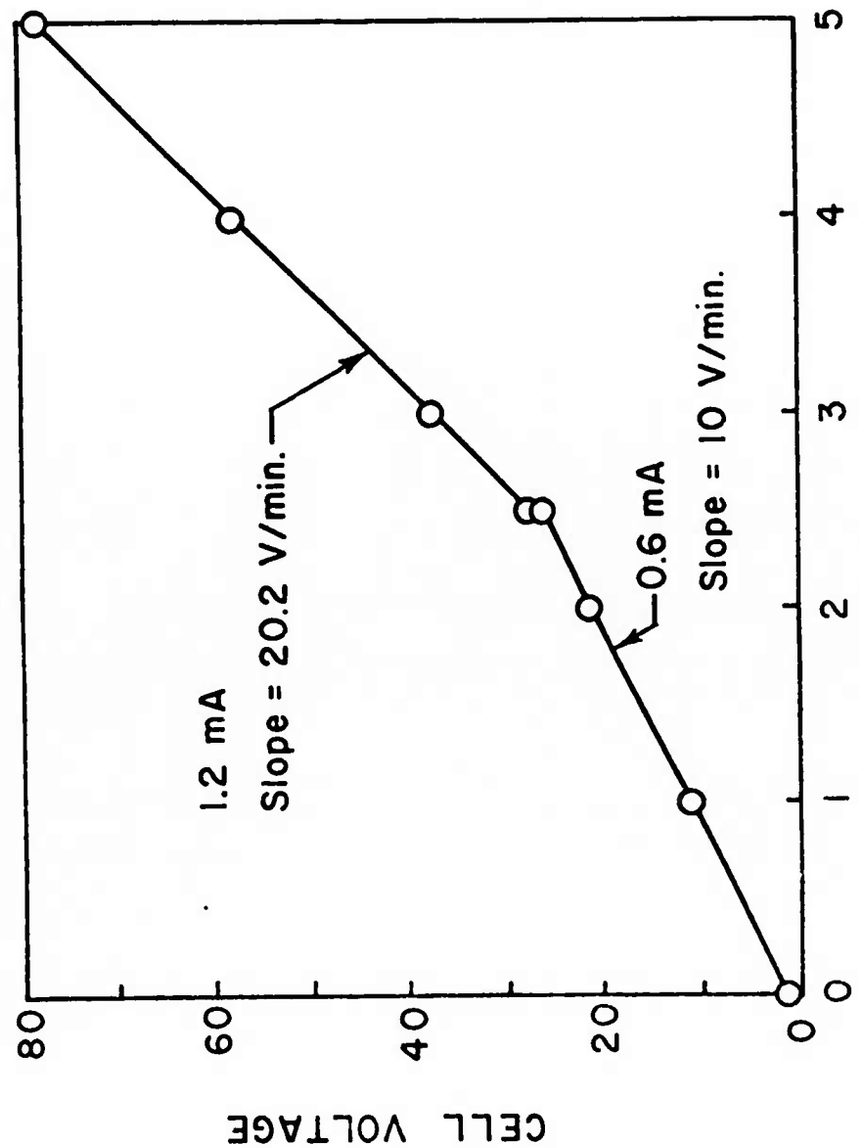


Fig. 3.1-17 Cell voltage vs time showing the direct proportionality of film growth rate to current density for a buffered solution.

In the more recent period, the emphasis has been to supply material with varying Cr-doping levels for device fabrication and evaluation. Table 3.2-1 gives the growth conditions for the Cr- and O_2-doped crystals grown during the reporting period, with some remarks regarding results.

Oxygen-doping alone (no Cr) was used in runs 1939, 1970, 1974A, and 1974B. In the first two of these experiments, the oxygen was added to the melt in the form of Ga_2O_3, while in the latter two runs the capsule was backfilled with oxygen gas. Results from Table 3.2-1 show that compensation has not been achieved in any of these runs, indicating that additions of Cr are necessary in the horizontal Bridgman method to obtain semi-insulating material when quartz boats are used.

For clarity, the data from Table 3.2-1 for those crystals in which Cr is added are listed in Table 3.2-2 in order of increasing estimated Cr-doping level. As indicated in the table, five Cr-doped ingots with Cr additives estimated from $4.0\times10^{15}/cm^3$ to $6.5\times10^{15}/cm^3$ have been evaluated, and of these only one is found to be semi-insulating. Two are uncompensated, the other two are only partially compensated. Two crystals grown with $7.8\times10^{15}/cm^3$ Cr-doping are compensated, and thus it appears that the threshold for reproducible compensation is at or near $7.8\times10^{15}/cm^3$ for current source materials and growth conditions.

These results are reflected in Table 3.2-3, which presents electrical data on all of the ingots evaluated during the period. Ingots doped with oxygen only are listed first, followed by Cr-doped ingots in order of increasing Cr-doping level. Of interest here is the fact that those Cr-doped ingots in which the Cr-level is 7.8×10^{15} or higher had resistivities

Table 3.2-1 Growth Conditions for Cr- and O_2-Doped Crystals

Ingot No.	O_2 Source	Cr Level Added to Melt (gm)	Estimated Cr (cm^{-3})	Results
1903	Ga_2O_3	0.125	4.0×10^{15}	Compensated
1939	Ga_2O_3	None	None	Did not compensate
1968	Ga_2O_3	0.125	4.0×10^{15}	Not sufficiently compensated
1970	Ga_2O_3	None	None	Did not compensate
1972	Ga_2O_3	0.125	4.0×10^{15}	Lost ingot due to furnace malfunction
1974A	100 mTorr O_2	None	None	(Poly) Did not compensate
1974B	100 mTorr O_2	None	None	(Poly) Did not compensate
1980	Ga_2O_3	0.200	6.5×10^{15}	Did not compensate
1997	100 mTorr O_2	0.161	5.4×10^{15}	Did not compensate
1999	100 mTorr O_2	0.165	5.4×10^{15}	Not fully compensated
2000	100 mTorr O_2	1.65	5.4×10^{16}	Compensated
2004	100 mTorr O_2	0.240	7.8×10^{15}	Compensated
2109	100 mTorr O_2	0.243	7.8×10^{15}	Compensated
2132	100 mTorr O_2	7.59	2.7×10^{17}	Compensated

Table 3.2-2 Doping Level and Results for Cr-Doped Crystals

Ingot No.	Estimated Cr (cm^{-3})	Results
1903	4.0×10^{15}	Compensated
1968	4.0×10^{15}	Not fully compensated
1997	5.4×10^{15}	Did not compensate
1999	5.4×10^{15}	Not fully compensated
1980	6.5×10^{15}	Did not compensate
2004	7.8×10^{15}	Compensated
2109	7.8×10^{15}	Compensated
2000	5.4×10^{16}	Compensated
2132	2.7×10^{17}	Compensated

Table 3.2-3 Electrical Data on Cr- and O_2-Doped Crystals

Ingot No.	Dopant (Estimated)	Resistivity ohm-cm	Mobility cm^2/volt-sec	Carrier Concentration cm^{-3}
1939	O_2 only	0.35	4,980	3.6×10^{15}
1970	O_2 only	0.63	6,140	1.6×10^{15}
1974A	O_2 only	Low ρ by ohmmeter		
1974B	O_2 only	Low ρ by ohmmeter		
1903	O_2 + 4.0×10^{15} cm^{-3} Cr	1×10^6		
1968	O_2 + 4.0×10^{15} cm^{-3} Cr	2.5×10^3		
1997	O_2 + 5.4×10^{15} cm^{-3} Cr	0.36	11,000	1.6×10^{15}
1999	O_2 + 5.4×10^{15} cm^{-3} Cr	1×10^4		
1980	O_2 + 6.5×10^{15} cm^{-3} Cr	0.44	1,170	1.2×10^{16}
2004	O_2 + 7.8×10^{15} cm^{-3} Cr	2×10^7		
2109	O_2 + 7.8×10^{15} cm^{-3} Cr	1×10^7		
2000	O_2 + 5.4×10^{16} cm^{-3} Cr	3.6×10^6		
2132	O_2 + 2.7×10^{17} cm^{-3} Cr	$> 10^7$		

in the 10^7 ohm-cm range, while the only ingot with a lower Cr-doping level which could be considered compensated, namely, #1903, had a resistivity at the bottom of the 10^6 ohm-cm range--just high enough to be considered semi-insulating.

It should be pointed out that the Cr-doping level in #2132 was so high, $2.7\times10^{17}/cm^3$, that precipitates are visually observed in polished slices from this crystal. Slices from this crystal as well as from four ingots with resistivities in the 10^7 ohm-cm range were cut on (100) planes, polished and submitted for device fabrication and evaluation. In addition, slices with various orientations, including (100) + 1° → (110), (100) + 2° → (110), (100) + 4° → (110), and (110) were cut from #2004, polished, and similarly submitted for tests of epitaxial growth. Lack of mobility data on the semi-insulating material is caused by inadequate instrumentation to perform reliable Hall measurements on high-resistivity material at the present time.

In addition to the samples supplied to the Science Center, polished slices from ingots 1939, 1997, 1999, and 2004, were submitted to Stanford University for growth of high-resistivity epitaxial layers.

Table 3.2-4 presents the results of mass spectrographic analysis of samples from three compensated Cr-doped ingots. The ingots chosen were those in which the estimated Cr-doping level was increased by approximately one order of magnitude from one to the next; namely, 2004, 2000, and 2132. The increasing trend is confirmed by the result of the analysis.

Table 3.2-4 Mass Spectrographic Analysis of Cr-Doped GaAs*

Impurities	Sample No.			Detection Limits
	2004	2000	2132	
C	4.1×10^{16}	3.4×10^{17}	6.2×10^{16}	2×10^{15}
N	2×10^{15}	2×10^{15}	2×10^{15}	2×10^{15}
O	1.0×10^{17}	1.5×10^{17}	8.9×10^{16}	2×10^{15}
F	ND	ND	ND	4×10^{14}
Na	9.0×10^{16}	9.0×10^{16}	9.0×10^{16}	9×10^{16}
Al	8.0×10^{16}	9.4×10^{16}	6.2×10^{16}	4×10^{14}
Si	ND	3.0×10^{15}	1.2×10^{17}	3×10^{15}
P	3.4×10^{16}	3.6×10^{16}	4.9×10^{16}	3×10^{15}
S	4×10^{15}	4×10^{15}	5.3×10^{16}	4×10^{15}
K	3.0×10^{16}	2.4×10^{16}	2.6×10^{16}	4×10^{14}
Cu	1.2×10^{17}	ND	9.4×10^{16}	4×10^{15}
Cr	3.0×10^{16}	7.6×10^{16}	5.3×10^{17}	4×10^{15}
Cr (Estimated)	7.8×10^{15}	5.4×10^{16}	2.7×10^{17}	**

*Analysis made by Micro-Trace Analytical Services. Results in cm^{-3}
**Based on distribution coefficient of 5.4×10^{-4}
ND: Not Detected

The agreement between measured and estimated Cr concentration is good for samples 2000 and 2132. For sample 2004 the Cr concentration determined by mass spectroscopy is four times higher than the estimated value. Part of the discrepancy may be accounted for by the fact that this particular specimen was taken from near the back end of the ingot where the Cr concentration tends to rise. Another item of interest in the mass spectroscopy data is the high oxygen concentration, due to the introduction of O as a dopant. There is a very pronounced increase in the detected silicon content as the Cr-doping level is increased. No explanation of this phenomenon is available as yet.

In summary, it seems evident that a Cr-doping level of approximately $3.0\times10^{16}/cm^3$, together with the technique of backfilling the growth ampoules with oxygen gas to a pressure of 100 mTorr, is sufficient to assure the production of semi-insulating GaAs from quartz boats by the horizontal Bridgman method. Further work in this area should concentrate on growth employing boats made from materials other than fused quartz, such as boron nitride. Boron nitride boats should eliminate the problem of silicon contamination, and permit the growth of crystals with higher resistivities and carrier mobilities.

In addition to the semi-insulating materials discussed above, Crystal Specialties, Inc., has grown single crystals of p-type, Zn-doped GaAs, and supplied polished slices cut on (100) orientation from these crystals to the Science Center for evaluation.

3.2.2 Material Evaluation

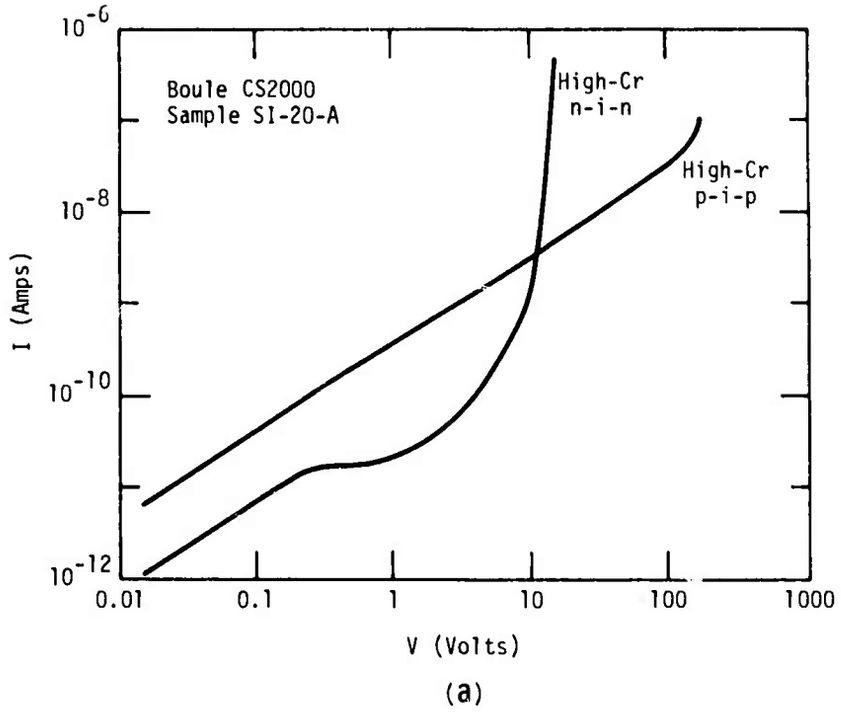
To review our approach, a new analytical technique for characterizing semi-insulating GaAs was described in our previous semi-annual report.[18] This technique, based on an application of Auger electron spectroscopy (AES), measures energy shifts of Auger electron peaks to determine the electrostatic potential at points on a specimen where the Auger electrons are emitted.[19] By using an Auger electron spectrometer in a scanning electron microscope (SEM) it was possible to profile the electrical potential across dc-biased specimens of semi-insulating GaAs with submicron resolution. The specimens investigated were n-i-n and p-i-p structures, where i indicates a thin layer (50-100μm) of Cr-doped semi-insulating GaAs of commercial quality (supplied by Laser Diode and Crystal Specialties). The AES-SEM potential profiles, in conjunction with I-V characteristics of the specimens, demonstrated that for both materials depleted junctions formed at the p-i interfaces in the p-i-p specimens. We therefore concluded that the semi-insulating material behaved as n-type despite the fact that the compensating impurity in semi-insulating GaAs is Cr, commonly considered an acceptor. To account for the n-type behavior we have speculated that O acting as a deep donor may play a significant role in the compensation mechanism.

Presently, work has been directed in two areas: (a) experiments leading to a better understanding of the material properties, and (b) efforts to simplify the evaluation analytical techniques. In the first instance, semi-insulating material with unusually high-Cr concentration was tested to determine the effect of Cr concentration on electrical behavior. These

measurements were particularly important because the Cr concentration chosen was the upper limit of Cr solubility. Measurements are still in progress, but already there are indications that high Cr concentration changes the semi-insulating material from n- to p-type. In the second area, that of simplification of the evaluation technique, measurements of current response to voltage transients were made on a p-i-p sample with promising results. In addition, an attempt was made to probe the interface between an n-type layer and a semi-insulating substrate by measurements of reverse-bias I-V characteristics of Schottky barrier contacts evaporated on the n-type layers.

The high-Cr material used in the present experiments belonged to boule #2000, grown at Crystal Specialties (Sec. 3.2.1). The chemical concentration of Cr is 7.6×10^{16} cm^{-3}. The high-Cr material contains a few Cr inclusions revealed by secondary ion mass spectrometry (discussed later in this section) indicating that the material is saturated with Cr. Therefore, our measurements are testing a limiting case of Cr concentration. The high-Cr material will be compared with semi-insulating material at the low end of Cr concentration. This material will be called low-Cr. To the low-Cr category belonged the Crystal Specialties boule #1718 (estimated Cr concentration, 4.1×10^{15} cm^{-3}) used for the measurements described in our previous report.[18] In parallel with the measurements described here, wafers of the same low- and high-Cr material were used as substrates for FET devices. The results of this test are discussed in Sec. 3.1.3.1.

In Fig. 3.2-1A the I-V characteristics of n-i-n and p-i-p samples of high-Cr material are shown. The p-i-p samples show an ohmic characteristic until breakdown. The n-i-n sample characteristic shows instead a region



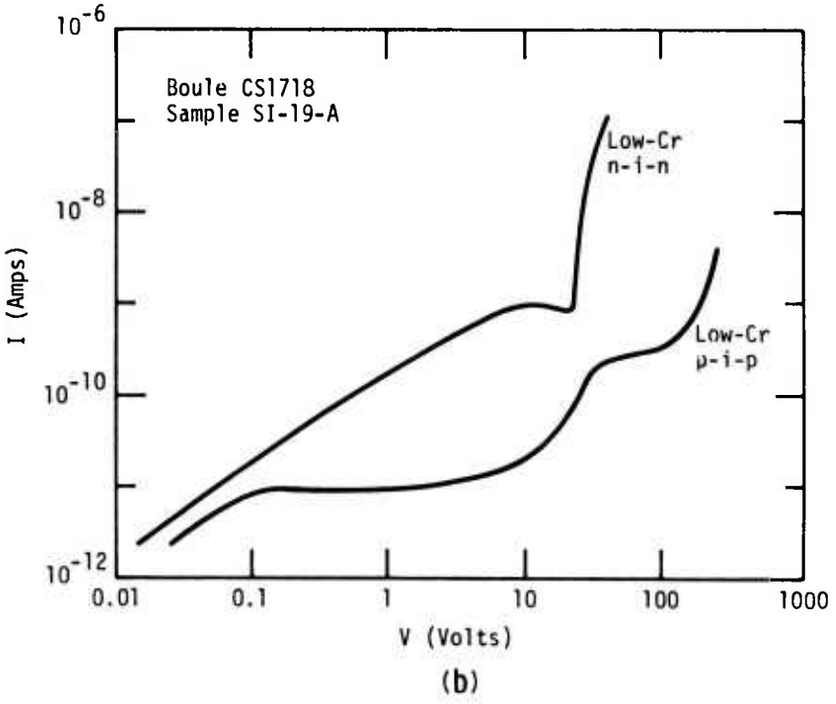


Fig. 3.2-1 I-V characteristics of n-i-n and p-i-p samples. (a) High-Cr semi-insulating GaAs (Crystal Specialties, boule 2000, Cr concentration, 7.6×10^{16} cm^{-3}). (b) Low-Cr semi-insulating GaAs (Crystal Specialties, boule 1718, estimated Cr concentration 4.1×10^{15} cm^{-3}).

of current saturation. Such a different behavior of the two types of samples had been observed before in the low-Cr material, but the behavior of the p-i-p and n-i-n samples appear now reversed. This reversal is exposed in Fig. 3.2-1b, which shows the I-V characteristics of an n-i-n and a p-i-p low-Cr. sample. In the low-Cr case the material behaves as n-type. The p-i-p characteristic has a saturation region as one of the p-i junctions is reverse-biased, while the I-V characteristic of the n-i-n samples is ohmic until near breakdown.

Saturation of the I-V characteristics of the high-Cr n-i-n sample suggests that a depleted junction is formed at the n-i interface. This is an indication that the high-Cr semi-insulating material is behaving as p-type. Such interpretation will be tested with AES-SEM measurements. Reversal from n- to p-type when the Cr concentration is increased is in agreement with the O-Cr model for compensation discussed in our previous report.[18] According to this model, which is basically the same as that proposed by Blanc and Weisberg for O-doped GaAs,[20] the Fermi level is pinned near the center of the gap by O acting as a deep donor and Cr acting as a deep acceptor. In this model the main compensating impurity is O. Cr is required with a concentration just sufficient to overcome the density of shallow donors, most likely Si. Under such circumstances the material can be n-type as observed in the low-Cr case. In this model an increase of Cr concentration may turn the material into p-type without a significant change in the position of the Fermi level (see Fig. 3.2-7 in Ref. 18) so that the high resistivity of the material remains nearly unchanged.

From the breakdown voltage of the high-Cr n-i-n sample, the acceptor states density is estimated to be $N_A \sim 1.9\times10^{12}$ cm^{-3}. This number will be

revised when the AES-SEM measurements are performed and, therefore, a detailed comparison between the high-Cr and the low-Cr sample is postponed. However, it is evident that an increase of Cr concentration by one order of magnitude up to its saturation limit has failed to produce a parallel increase in the concentration of electrically-active impurities. This agrees with the observation of insignificant differences between FET devices made on high- and low-Cr substrates (Sec. 3.1.3.1). All this reinforces the idea that a fundamental part of the compensation in semi-insulating GaAs takes place for formation of electrically-inactive complexes.[21-23] Recent observation of inclusions containing Si discussed later in this section opens new perspectives suggesting that impurities may segregate out of the bulk semi-insulating material.

AES-SEM potential profile measurements were made on an n-i-n specimen of low-Cr material (Crystal Specialties, boule 1718) for comparison with previous similar measurements on an n-i-n specimen made with Laser Diode material which yielded an anomalous potential profile (Fig. 3.2-6, Ref. 18). The potential profile is shown in Fig. 3.2-2 for a -5 volts dc bias applied to the top and to the bottom of the specimen. The potential drops in only a fraction of the width of the semi-insulating region as in the specimen made with Laser Diode material. As in this case, inverting the biased terminals reverses the profile. The same profiles was observed at lower bias voltage. To determine without ambiguity the location of the interfaces between the substrate and the n^+ epi-layers is critical in this

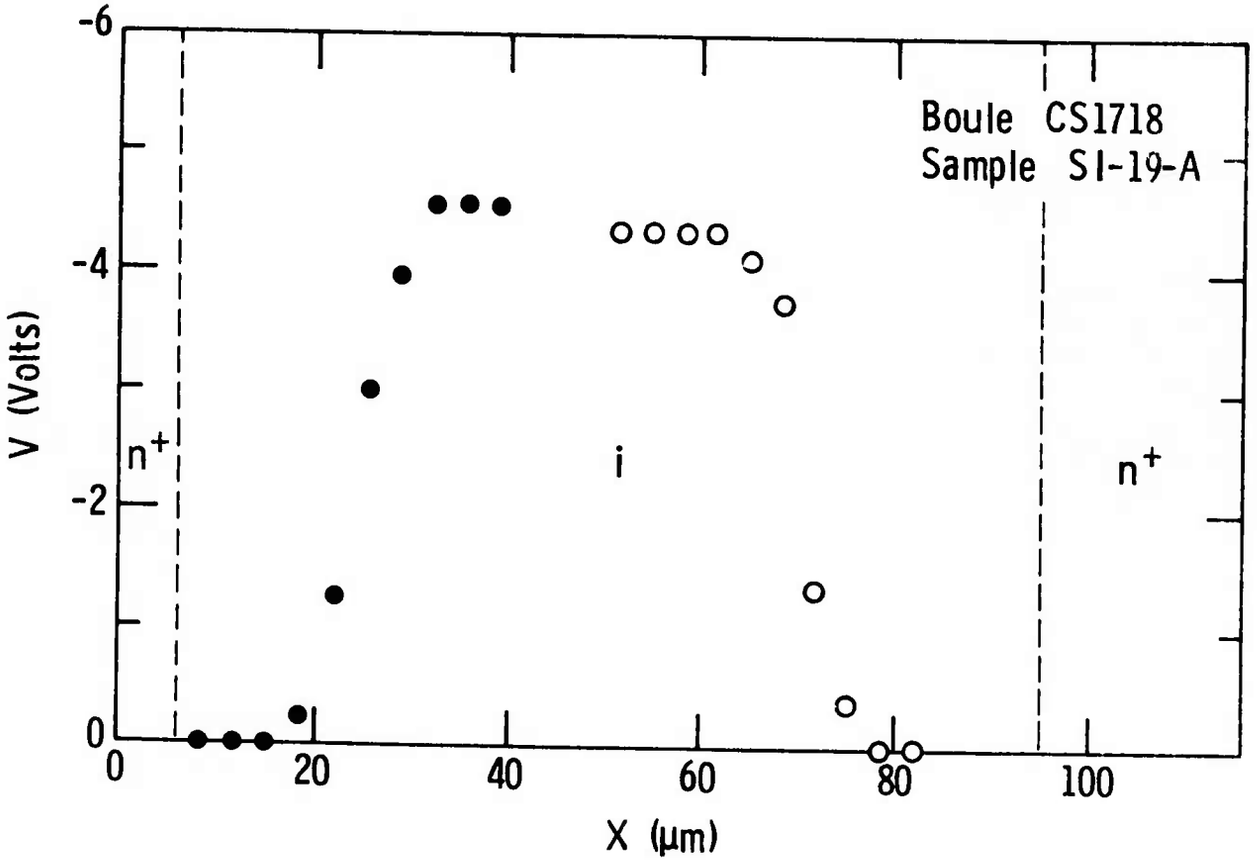


Fig. 3.2-2 Voltage profile across an n-i-n sample made with low-Cr semi-insulated GaAs (Crystal Specialties, boule 1718). ○: left side (sample top) biased -5V; ●: right side (sample bottom) biased -5V.

case. Cathodoluminescence in the SEM was used as in previous cases[18] taking advantage of the fact that the luminescent efficiency of semi-insulating GaAs is extremely low[18,19] in contrast with the normal luminescent behavior of the epitaxial layers. Figure 3.2-3 shows two SEM photographs of the specimen in the same position and with the same magnification using a secondary electron detector to see the specimen in one picture, and a photomultiplier with an S-1 photocathode to identify the epitaxial layers in the other picture. The validity of this technique was confirmed by staining on a disposable sample. The positions of the interfaces, shown with dashed lines in Fig. 3.2-2, prove that the sharp drop of the potential does not occur at the interfaces. A region of instability before breakdown was observed in obtaining the I-V characteristic of the sample shown in Fig. 3.2-1b. Such instability seems to be compatible with the existence of a high electric field due to the sharp potential change.

At this point we have no simple explanation for the localization of the potential drop across the low-Cr n-i-n samples. Failure of the Auger technique to faithfully measure the voltage profile should be ruled out in view of a recent demonstration on a well-characterized p-n junction.[24] Impurity diffusion from the heavily-doped epi-layers is unlikely because the potential drop occurs 20μm from the interfaces. A simple effect of carrier diffusion must also be ruled out despite the fact that electron diffusion can reach very deeply into a high-low (n^+-ν) junction[25] when the electrostatic screening length (Debye length) is large.[26] Assuming a free carrier concentration in semi-insulating GaAs as low as 3×10^{7} cm^{-3},

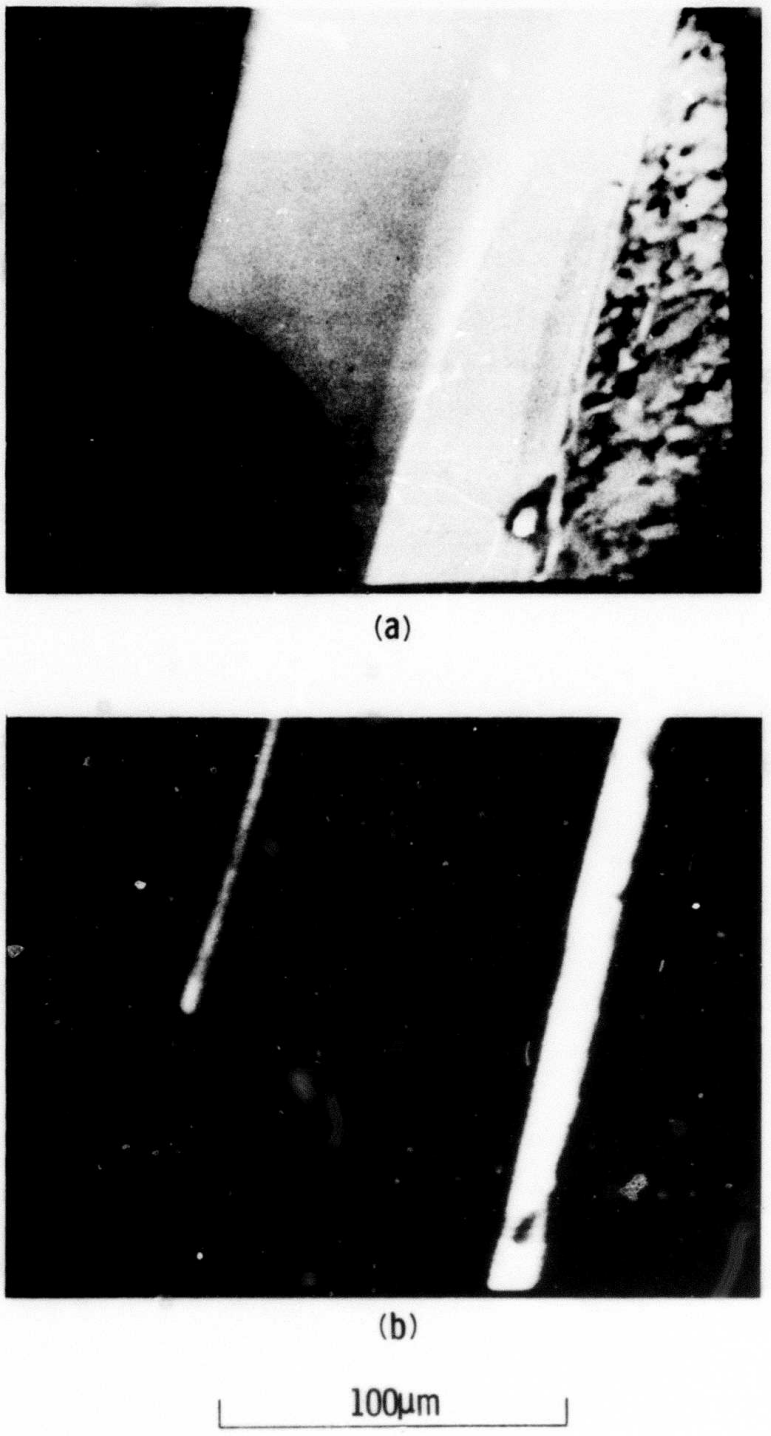


Fig. 3.2-3 Measurement of sample thickness by cathodoluminescence. (a) Normal scanning electron micrograph taken with a secondary electron detector; (b) Same as (a) in the cathodoluminescence mode using a photomultiplier with S-1 photocathode as detector.

the calculated free electron distribution is such that electrons diffuse from the n^+ contacts reaching the center of the semi-insulating layer. However, this excess charge makes the voltage required to sustain the current much lower than the experimental value, and the potential profile is just a slight modification of the built-in potential. If, on the contrary, diffused electrons do not reach the center of the semi-insulating layer, then the potential profile in the central region becomes linear. Further work will be done on this problem. The fact that semi-insulating GaAs belongs to the category of "relaxation"-type semiconductors[27] will be considered in future analysis of the problem.

In an attempt to find simplified analytical measurements for the doping density of semi-insulating GaAs, some measurements of capacitance were made on p-i-p samples of low-Cr material. The idea is based on previous observations that this material behaves as n-type forming a p-n junction with the p-type layer. Consequently, the reverse-biased junction of the p-i-p sample is expected to behave as a capacitor in series with the undepleted semi-insulating material acting as a resistor. However, the resistance R is large due to the high resistivity of semi-insulating GaAs. Therefore, the time constant RC is expected to be large, in the millisecond range, precluding use of capacitance bridges which operate at the too-high frequency of 1 MHz. Measurements of junction capacitance on semi-insulating GaAs has been attempted in the past without success[28] because such measurements were based on the wrong assumption that low-Cr semi-insulating GaAs was a p-type material.

For a first attempt to observe the p-i junction capacitance it is simple and convenient to work in the time domain. A block diagram of the measurement system is shown in Fig. 3.2-4. A 1-volt-square wave signal superimposed on a negative bias voltage is applied to the p-i-p sample. A slow repetition rate (1 Hz) insures that the square waves act as voltage steps. The current transients are amplified by a current amplifier followed by a voltage amplifier, and they are averaged for S/N improvement by a boxcar integrator. The sample chosen for this test belongs to the same group as the sample used for the I-V characteristic of Fig. 3.2-1b, and it has a similar I-V characteristic.

Figure 3.2-5 shows the current response at -1V bias voltage. This transient is exponential-like as expected for the current response of a series R-C circuit to a voltage step.

Figure 3.2-6 shows semi-logarithmic plots of the current transient due to a 1-volt step for three values of bias voltage. The slope of the curve increases when the negative bias voltage is increased, indicating that the time constant decreases. This is expected for a p-n junction because the capacitance C in RC decreases when the bias voltage increases.

All this is in qualitative agreement with the predicted capacitive behavior of the reverse-biased p-i junction, and it reconfirms the n-type behavior of low-Cr semi-insulating GaAs revealed by other measurement methods. However, caution is necessary before quantitative results are extracted from the data. In fact, departure of the curves in Fig. 3.2-6

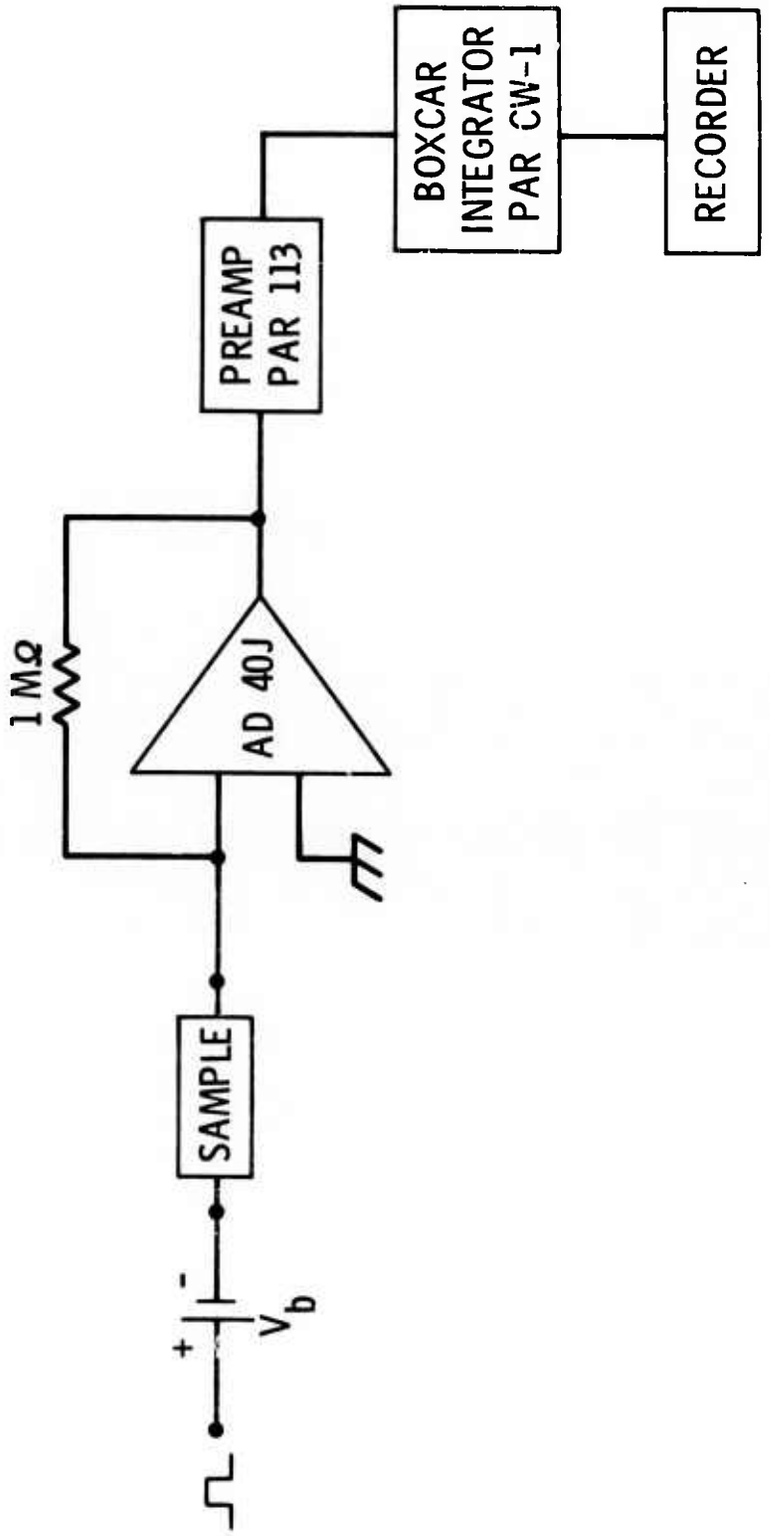


Fig. 3.2-4 Block diagram of the system for measurement of current transients.

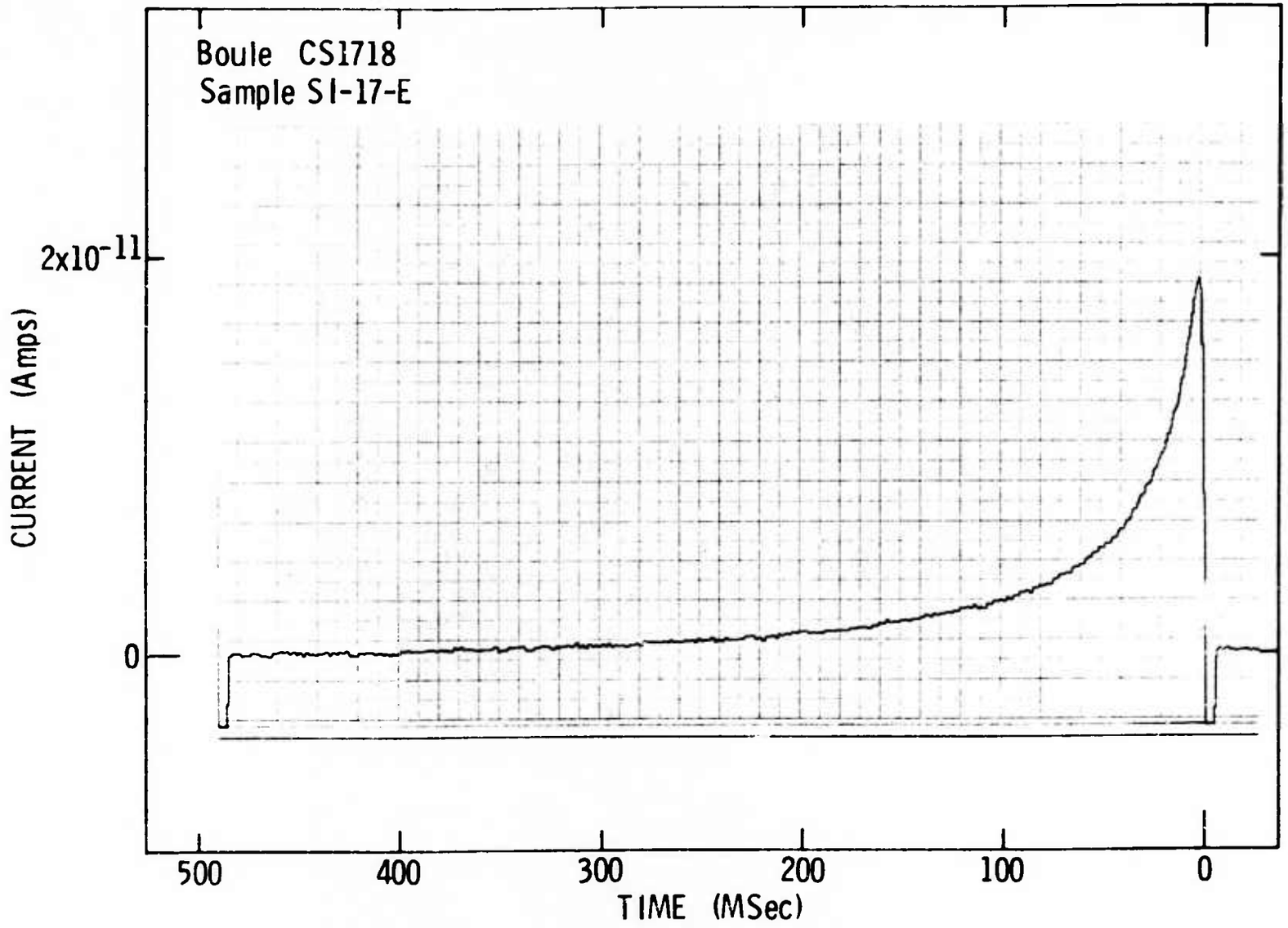


Fig. 3.2-5 Current transients in a low-Cr p-i-p sample when the voltage is stepped from -1.5 to -0.5 volts. (1 volt, 1 Hz square wave excitation superimposed on -1 volt bias.)

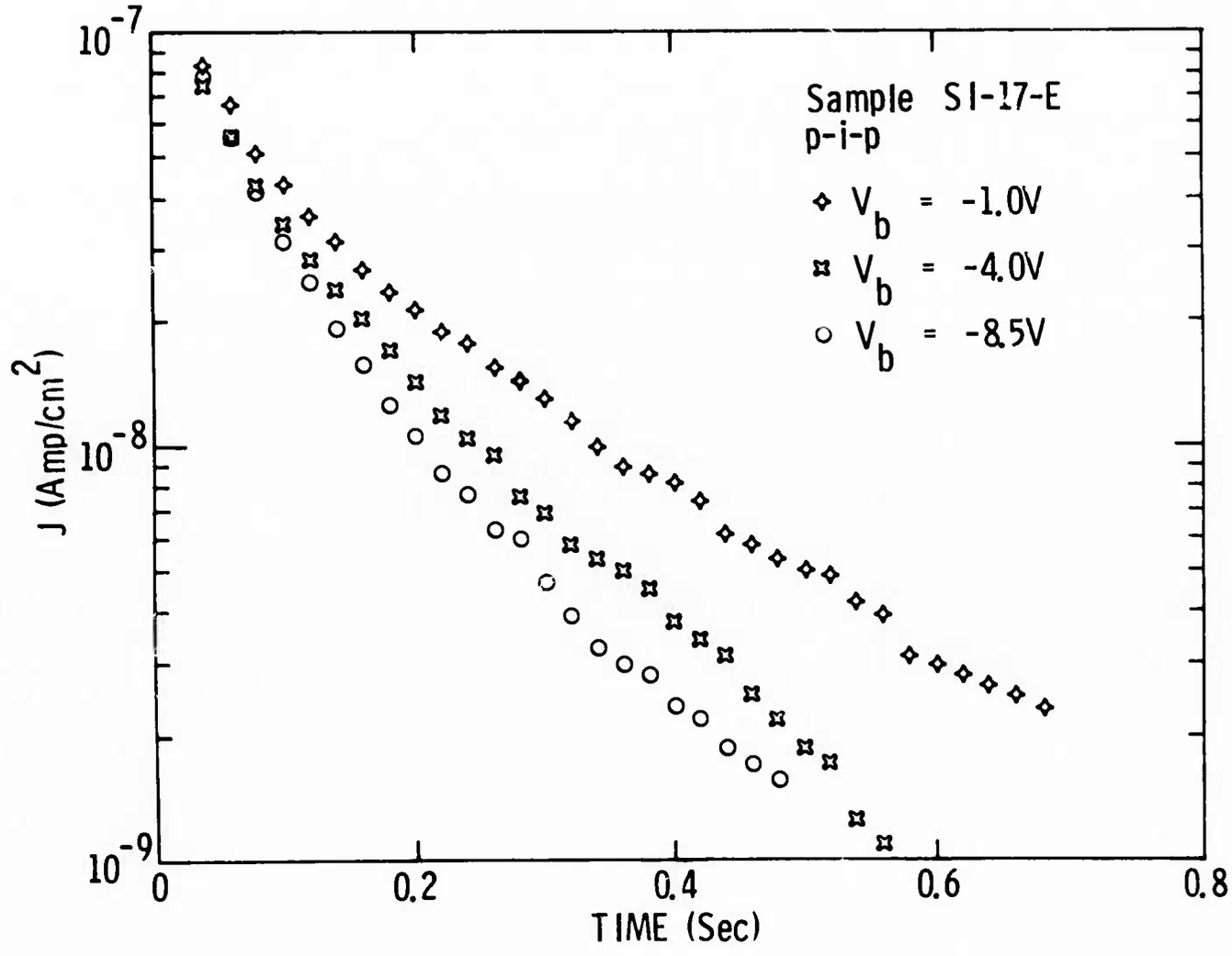


Fig. 3.2-6 Current density transients in a low-Cr p-i-p sample for 1 volt, 1 Hz square wave excitation superimposed on different bias voltages.

from pure exponentials indicates that more than one time constant may be involved. It is possible that thermal excitation from traps may have a time constant in the range of the measurements reported here.

These results encourage a more detailed measurement of the time response, eventually varying the temperature of the sample in order to measure activation energies. Similar measurements will be attempted on other samples.

Finally, an attempt was made to probe the interface between a thin n-type layer and the substrate. The experiment consisted of evaporating Ti-Au Schottky barrier dots on an n-type layer, and measuring the reverse-bias I-V characteristic of such Schottky barriers. The second contact was a large forward-biased Ti-Au dot, as it is common practice for C-V profiling. The rationale behind this measurement is that when the punch-through voltage is reached, the interface falls within the depletion region of the Schottky barrier. If the interface is a source of thermally-generated carriers, such generation source may increase the reverse current after punch-through.

Figure 3.2-7 shows the reverse I-V characteristic of three samples, selected such that they offer different combinations of film and substrate. The three samples are: an epitaxial layer on a semi-insulating substrate; an ion-implanted layer in a semi-insulating substrate, and an ion-implanted layer in an n-type partly-compensated buffer layer grown at Stanford.

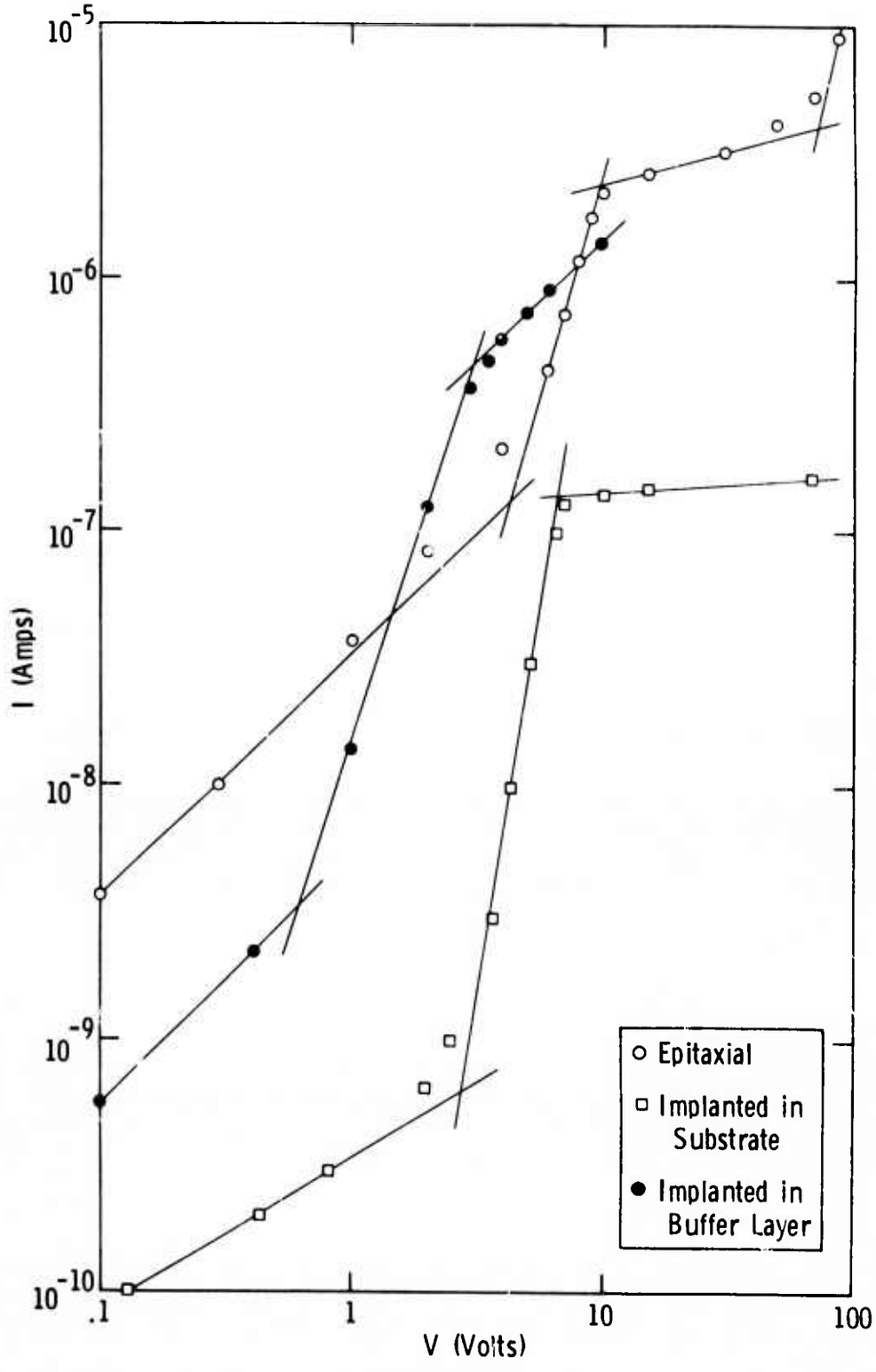


Fig. 3.2-7 Reverse I-V characteristics of Schottky barriers on n-type layers. The layers are either epitaxial or ion-implanted. The substrate is semi-insulating GaAs with or without a buffer layer.

It is striking in Fig. 3.2-7 how similar the three curves are in spite of the drastic differences between samples. The main feature, common to all three samples, is the sharp increase of the current followed by a higher saturation level. The voltage at which the current saturates coincides for each sample with the punch-through voltage measured by C-V. This current increase must not be mistaken as avalanche breakdown which occurs at a much higher voltage.

This sharp increase of the reverse current at punch-through cannot be due to an interface effect because the implanted sample, lacking a sharp interface, should have a different I-V characteristic. An effect due to the deep impurities in the substrate must also be ruled out because it would not be the same in the Stanford buffer layer, which was grown under quite different conditions.

Our interpretation is based on one feature in common between all three samples--that they have a quasi-intrinsic substrate, with the Fermi level near the center of the gap. The hole density in the substrate, although small, is much larger than that of the n-type layer, in which the Fermi level is near the conduction band. Therefore, at punch-through a higher density of holes is available to be swept by the electric field in the Schottky barrier depletion region. This is enough to raise the level of the saturation current. The rise is somehow gradual because holes can reach the Schottky barrier depletion region before punch-through by diffusion.

These observations identify a source of gate leakage current in the FET device. However, the level of such current is quite tolerable. As a probe for interface effects, the measurement of reverse current of Schottky barriers is not useful because the hole current from the substrate masks any effect due to generation at the interface. A different alternative consisting of the study of low-frequency noise in FET-like samples is being considered as a probe for the interface.

Secondary ion mass spectrometry (SIMS) is employed at Cornell to conduct a study of uniformity of concentration of chromium, and other ambient impurities, in the semi-insulating GaAs substrates. Two samples were tested, a high-Cr sample (Crystal Specialties, 2000) and a low-Cr sample (Crystal Specialties, 1718). These samples were taken from the same wafers used to make the p-i-p and n-i-n specimens described earlier in this section. Studies of Ga and arsenic showed the expected uniform, featureless concentration over the polished surfaces on both samples. Studies of the chromium in the lightly-doped sample showed no chromium above the sensitivity limit, just above 1 ppm. In the heavily-chromium-doped sample, however, isolated small inclusions of chromium were easily detected, and are shown as the three small, diffuse white spots in Fig. 3.2-8 (bottom, center, and upper right). The chromium over the rest of the surface was below the present sensitivity limit. The field of view is 250μm in diameter and the ion beam has 1μm transverse spatial resolution.

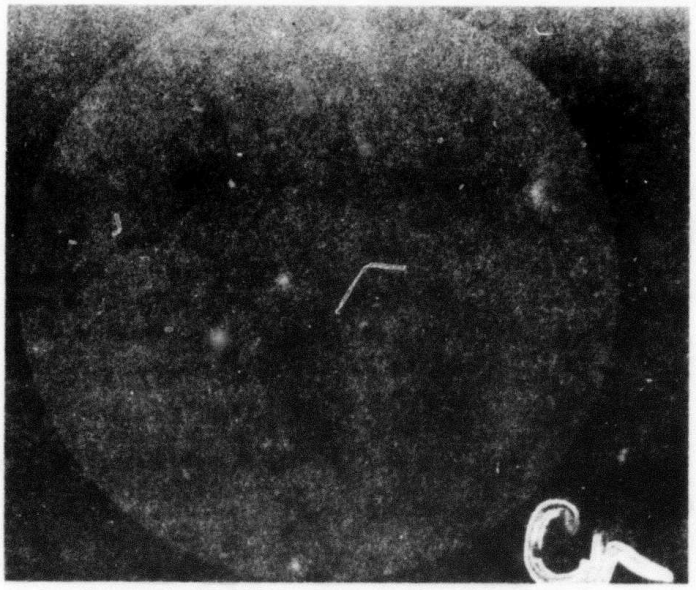


Fig. 3.2-8 Chromium impurity pattern in a heavily-doped semi-insulating substrate (Crystal Specialties 2000).

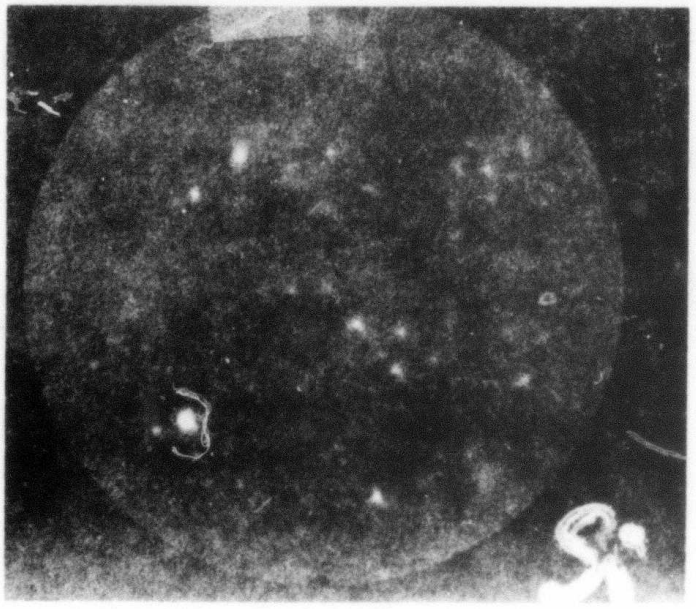


Fig. 3.2-9 Ambient silicon impurity pattern in semi-insulating GaAs.

The only other impurity that could be easily seen was silicon. The sensitivity limit of silicon is just below 1 ppm, so it is easier to sense than chromium, but it is very prominent and very inhomogeneous. Figure 3.2-9 shows silicon pattern over a 250μm field of view on the wafer.

On the clean polished surface, one dust spot was also found embedded into, or clinging to, the surface. A strong reading of Na, K and Al were present in that dust spot.

It appears that clusters of silicon more concentrated than the $5\times10^{16}/cm^3$ sensitivity limit of SIMS, are present. These could cause drastic compensation of the liquid phase epitaxial FET channel in patches near the substrate, due to diffusion, since silicon is an acceptor in liquid phase epitaxy below 850°C. Very poor performance could result from the doping and mobility inhomogeneities near these spots.

3.3 Ion Implantation--Results

3.3.1 Sulfur Implantation

We have used n-type layers formed on semi-insulating GaAs by the implantation of low doses of 100 keV sulfur ions for the fabrication of low-noise FETs. The RF performance of these devices is described elsewhere in this report. In this section we will discuss the characteristics and reproducibility of these n-type layers made by sulfur implantation.

In the course of preparing n-type layers for FET fabrication, about 20 samples have been implanted with a dose of 7×10^{12} 100 keV sulfur ions/cm^2 and annealed at 850°C for 30 minutes using a sputtered Si_3N_4 cap. Most of the implantations were performed at 350°C, but some were also carried

out at room temperature. Typical carrier concentration profiles obtained from Schottky barrier C-V measurements on some of these samples are shown in Fig. 3.3-1. Several different implantation substrates were used in obtaining the data in this figure. These include semi-insulating material obtained from Crystal Specialties and from Laser Diode, and a high-resistivity epitaxial layer prepared at Stanford University. The maximum electron concentration observed for the different samples is about the same. There is some difference, however, in the depth of penetration of the doping at lower electron concentrations. The Gaussian curve calculated from the LSS range parameters[29] for 100 keV sulfur in GaAs is also shown on the figure. The measured profiles extend well beyond the depth expected from the LSS range theory. These deep profiles are probably due to diffusion. There is considerable scatter in the published values for the diffusion coefficient of sulfur in GaAs making it difficult to decide whether or not the normal diffusion of sulfur could account for this deep penetration. However, we have observed that the profiles obtained after an anneal of more than 30 minutes at 850°C or for an anneal of 10 minutes at 900°C are essentially the same as those obtained for an 850°C, 30-minute anneal period. This suggests that normal diffusion of the sulfur is not the primary factor determining the deep penetration, and that enhanced diffusion due to the defects produced during implantation is probably involved. Such an enhanced diffusion might tend to be independent of anneal time or temperature as long as the anneal was sufficient to remove the defects contributing to the enhanced diffusion.

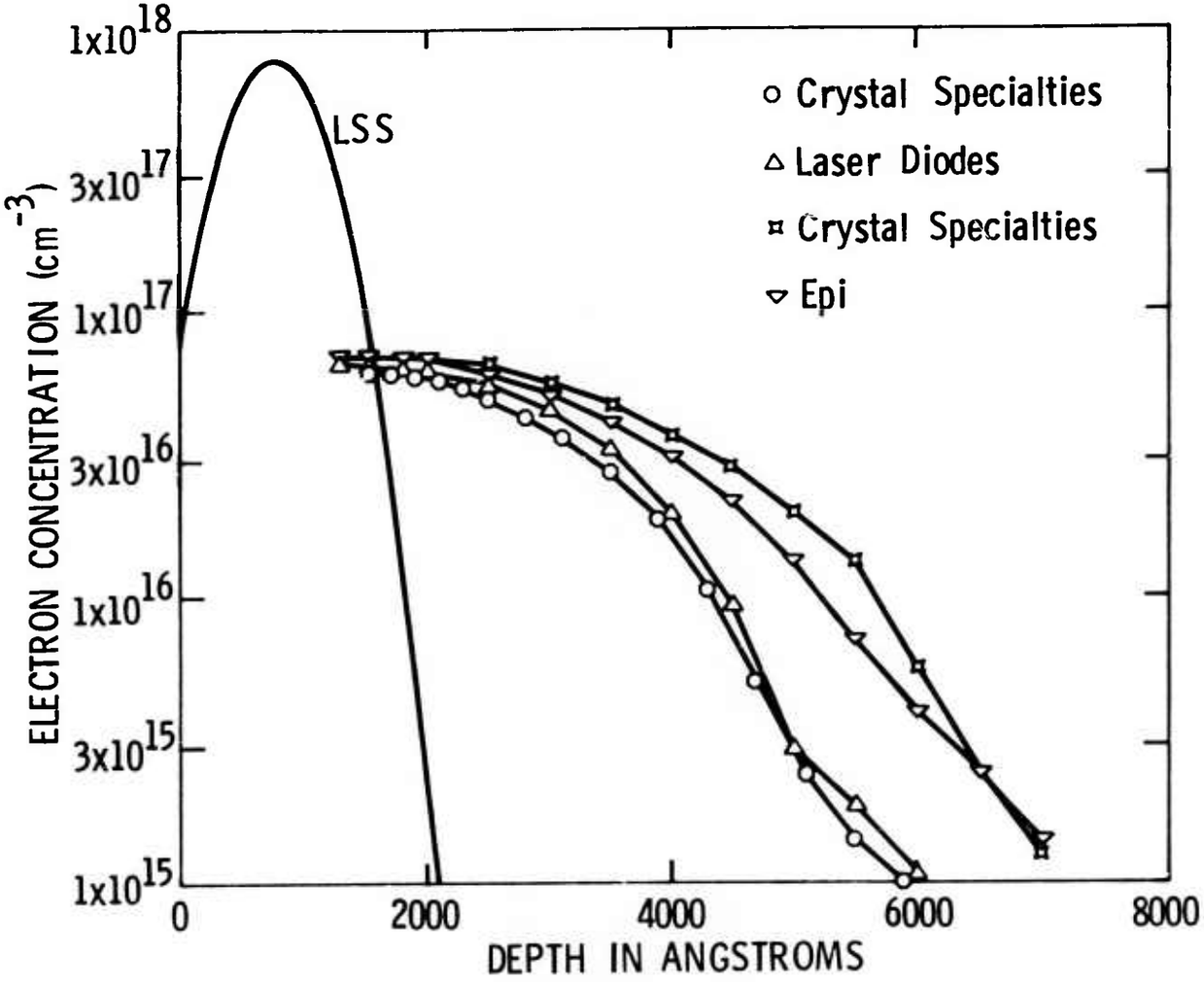


Fig. 3.3-1 Electron concentration profiles obtained from Schottky barrier C-V measurements of GaAs samples implanted at 350°C with 7×10^{12} 100 keV sulfur ions/cm^2 and annealed at 850°C for 30 minutes with a Si_3N_4 cap.

The distributions in the maximum observed carrier concentration, and the depths at which the carrier concentration was 70 percent and 10 percent of this maximum value for all the samples with the implant and anneal conditions mentioned in the preceding paragraph, are shown in Fig. 3.3-2. The maximum carrier concentration varies over a range of only about ±15 percent. The distribution in depth at both 70 percent and 10 percent of the maximum carrier concentration are grouped within a fairly narrow range except for a few samples which fall somewhat beyond this range. If the four samples, whose depths at 70 percent of the maximum electron concentration lie near 4000Å, are excluded from the distribution, then the remaining samples (79 percent of those studied) have an average depth of 2900Å with a standard deviation of 200Å. Material obtained from Laser Diode was used in two of the four samples excluded. This is a large fraction of the Laser Diode samples used, (2/3) and suggests that the greater depth at 70 percent of maximum concentration could be associated with the substrate material. However, because of the small number of samples of Laser Diode material used, it will be necessary to do further work before firm conclusions can be reached about the influence of substrate material on the electron concentration profile resulting from low-dose sulfur implantation.

Data for samples implanted at room temperature are indicated in Fig. 3.2-2 by the shaded regions and that for samples implanted at 350°C by clear regions. There does not seem to be a significant difference in

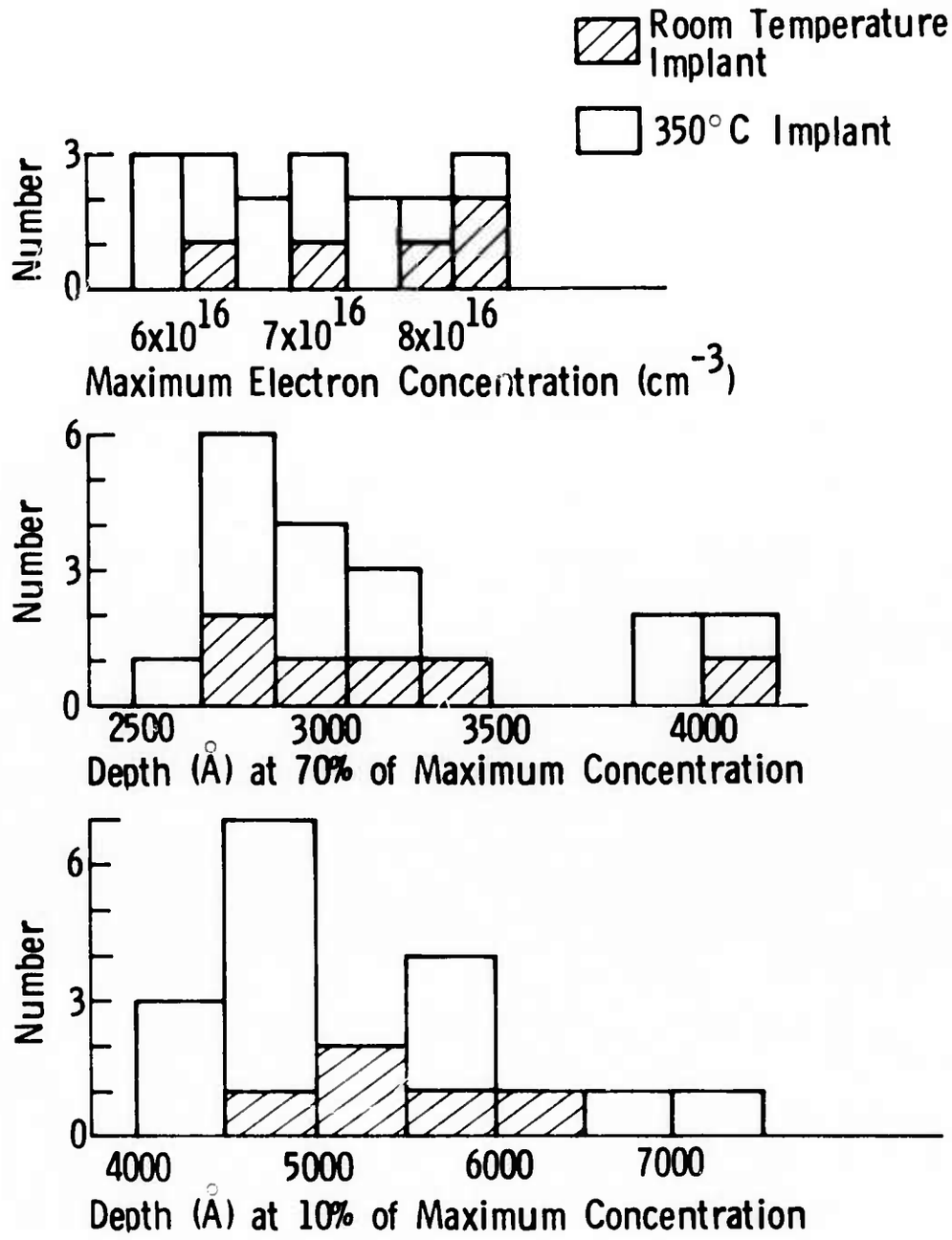


Fig. 3.3-2 Distributions of the maximum observed electron concentration and the depths at which the electron concentration is 70% and 10% of that maximum for GaAs samples implanted at 350°C with 7×10^{12} 100 keV sulfur ions/cm^2 and annealed at 850°C for 30 minutes with a Si_3N_4 cap.

the distributions for the two different implant temperatures. Previous work has indicated that a substantial difference might be expected in the results of room temperature and high-temperature implants when an amorphous layer was produced during implantation. The low sulfur doses employed in the present work are probably less than 10 percent of that required to make an amorphous layer. It is, therefore, not surprising that the profiles for room temperature and 350°C implants are similar. Mobility data are limited at present. Data for a pair of samples from the same substrate material and with cap layer deposited in the same sputtering run gave an effective mobility of 4600 cm^2/volt-sec for the sample implanted at room temperature and 5200 for the sample implanted at 350°C. Further work is required to determine whether or not there is a consistent mobility difference between samples implanted at room temperature and samples implanted at high temperatures.

3.3.2 Selenium and Tellurium Implantation

The implantation of high doses of selenium has been investigated in some detail using either Si_3N_4 or AlN as an annealing cap. We report the results of this work in this section together with some data on the annealing of tellurium implants with an AlN cap as well as results on the effect of a pre-anneal of tellurium implants in a hydrogen atmosphere before capping and annealing at 900°C.

Carrier concentration and mobility profiles for several samples implanted with different selenium doses and annealed at 900°C for 10 minutes with a sputtered Si_3N_4 cap are shown in Fig. 3.3-3. The maximum

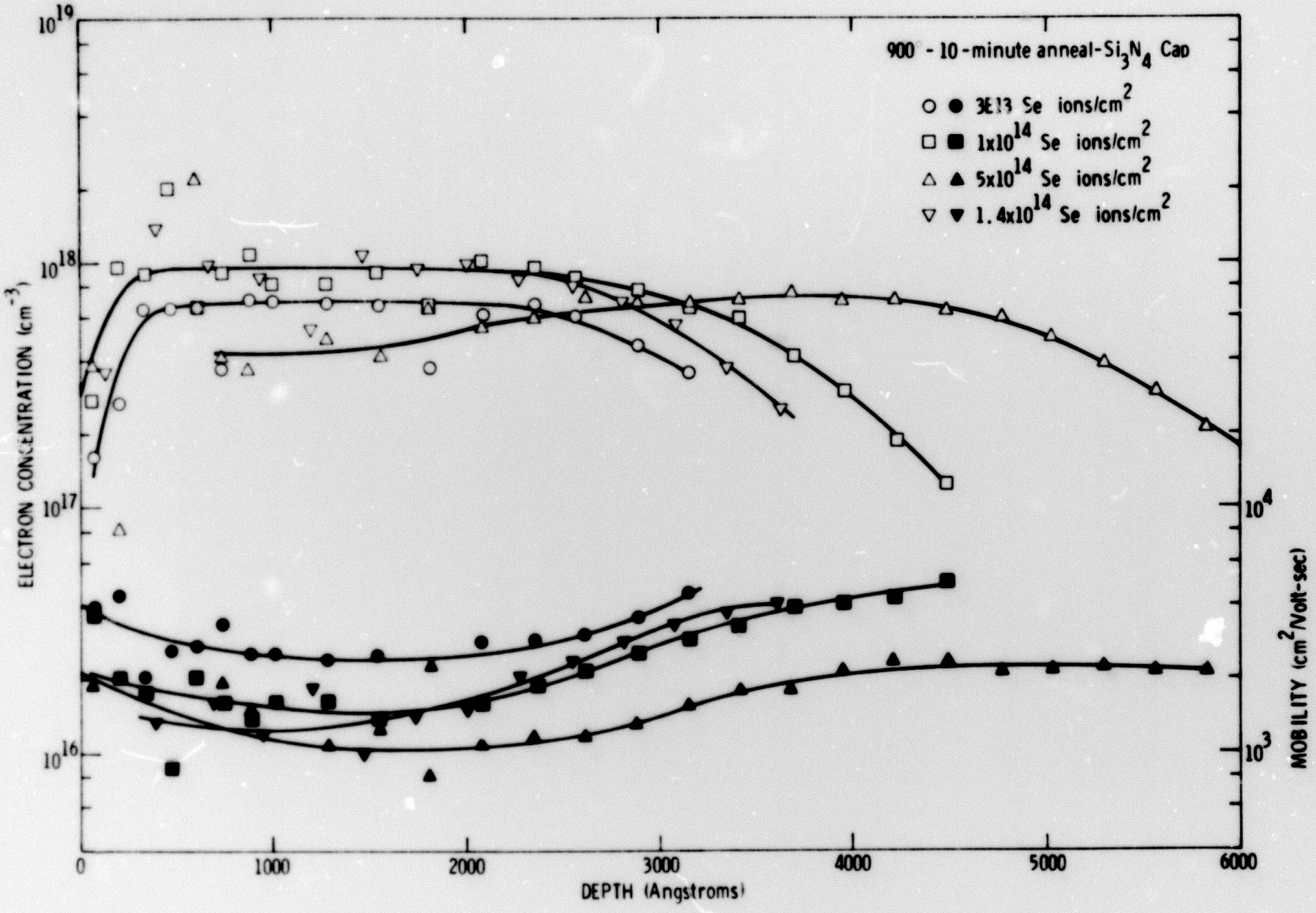


Fig. 3.3-3 Electron concentration and mobility profiles for GaAs samples implanted at 350°C with the indicated doses of 400 keV selenium ions and annealed at 900°C for 10 minutes with a Si_3N_4 cap.

carrier concentration achieved under these conditions was about $1\times10^{18}/cm^3$ for doses or 1×10^{14} and 1.4×10^{14} selenium ions/cm^2. A dose of 5×10^{14} selenium ions/cm^2 resulted in a slightly lower maximum carrier concentration, but a considerably deeper penetration of the doping profile. The results for the electron concentration profiles are similar to those obtained for 400 keV tellurium implantation in GaAs using a Si_3N_4 annealing cap except that in the tellurium case the maximum electron concentrations achieved were about 7×10^{17} rather than 1×10^{18} for a 900°C 10-minute anneal. The difference in the mobilities for the different samples is much larger than would ordinarily occur for the carrier concentrations observed. The mobility for the sample which received a dose of $5\times10^{14}/cm^2$ is significantly lower than that for the sample which received a dose of $3\times10^{13}/cm^2$ although the maximum carrier concentrations in these two samples are about the same. This suggests that compensating centers, which also act as scattering centers for the electrons, may be present in the higher dose sample, resulting in a reduced mobility.

Data for selenium-implanted samples annealed with a sputtered AlN cap at 900°C for 10 minutes are shown in Fig. 3.3-4. As in earlier work in which an AlN cap was used, the AlN film actually contains approximately as much oxygen as it does nitrogen. The carrier concentration obtained for the samples implanted with doses of 1×10^{14} or 5×10^{14} ions/cm^2 are significantly higher than the electron concentrations obtained using a Si_3N_4 cap on samples with these same doses, and the electron concentration profile

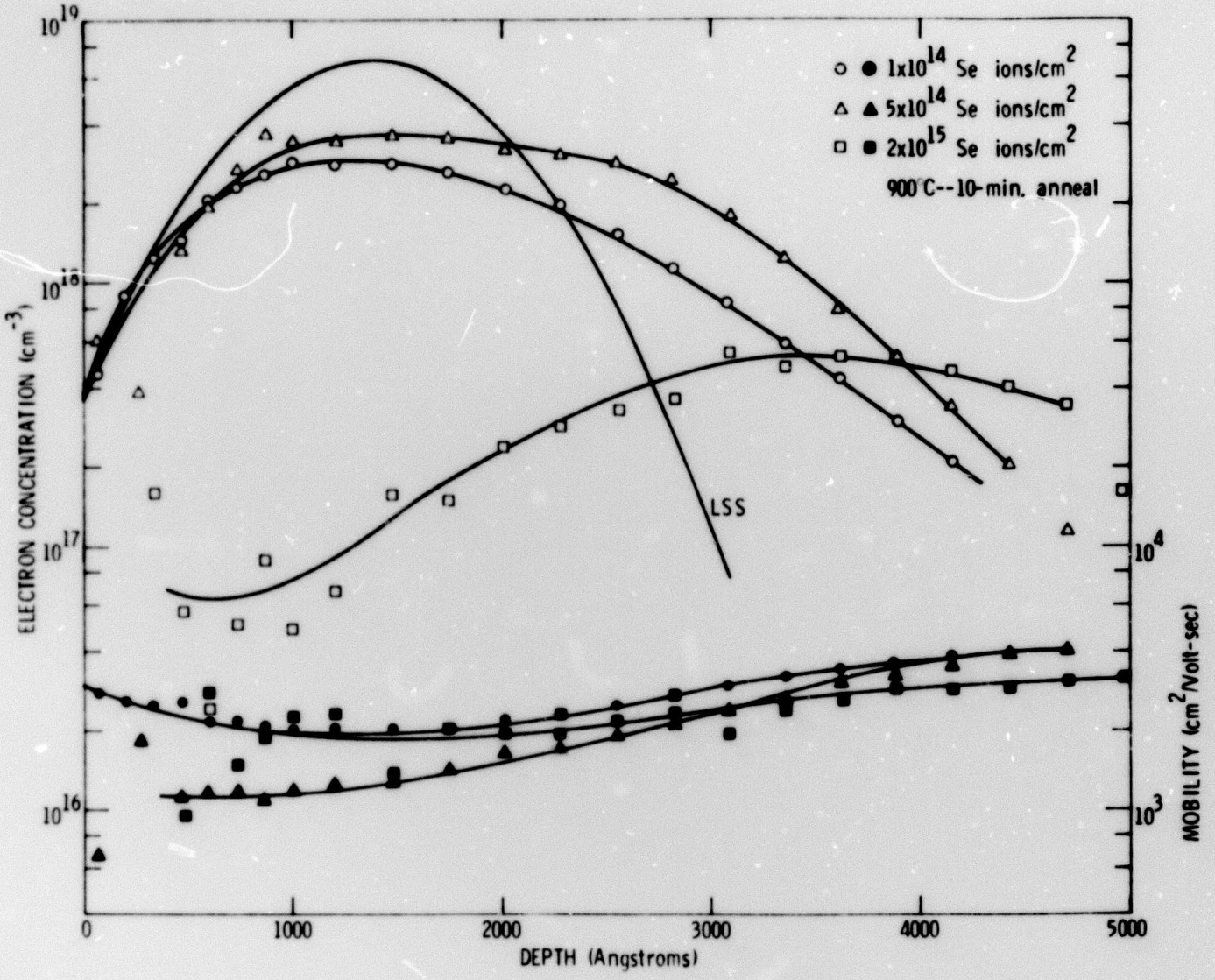


Fig. 3.3-4 Electron concentration and mobility profiles for GaAs samples implanted at 350°C with the indicated doses of 400 keV selenium ions and annealed at 900°C for 10 minutes with an AlN cap. The LSS range curve for a dose of 1×10^{14} selenium ions/cm^2 is also shown.

was not as deep when AlN was used as when Si_3N_4 was used. For a dose of 2×10^{15} selenium ions/cm^2, the maximum electron concentration occurs at a depth significantly beyond the peak of the LSS range distribution and is lower than the maxima obtained for the two lower doses previously mentioned. A few samples have been annealed at 950°C for a period of 10 minutes. The profile data for these samples is shown in Fig. 3.3-5. The sample, which was annealed with a Si_3N_4 cap, shows an increase in the maximum carrier concentration of a factor 1.5 over that obtained at the same dose using a 900°C anneal. For the samples annealed with AlN caps, the most dramatic increase is that shown by the sample with a 2×10^{15} dose where the maximum carrier concentration and the percentage of the implanted dose which is electrically active are both increased by nearly a factor of 10 by the use of the higher anneal temperature. The mobility for this sample is also increased significantly.

The data obtained using Si_3N_4 and AlN caps on selenium-implanted samples with annealing temperatures of 900°C or 950°C is summarized in Fig. 3.3-6 where the sheet electron concentration is plotted vs the implanted dose. The straight line on the figure indicates the results expected if 100 percent activation of the implanted ions were achieved. At a dose of 3×10^{12}, nearly 100 percent activation of the implanted selenium has been observed using a Si_3N_4 cap. As the dose increases, the percentage activation is seen to decrease, and the sheet electron concentration seems to level off at a value of about 3×10^{13}/cm^2. For the 900°C anneal temperature, appreciably higher sheet electron concentrations were

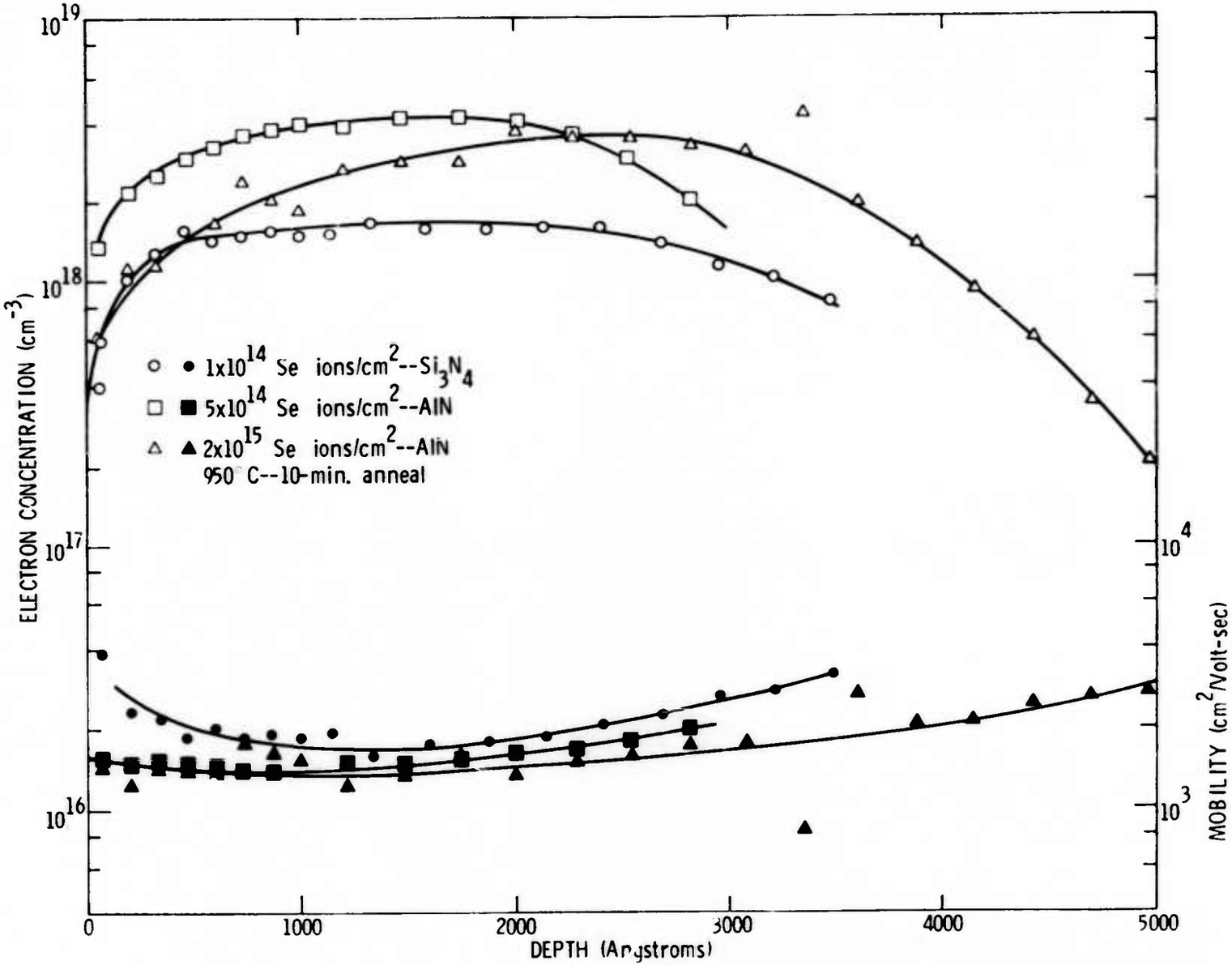


Fig. 3.3-5 Electron concentration and mobility profiles for GaAs samples implanted at 350°C with the indicated doses of 400 keV selenium ions and annealed at 950°C for 10 minutes with the indicated cap.

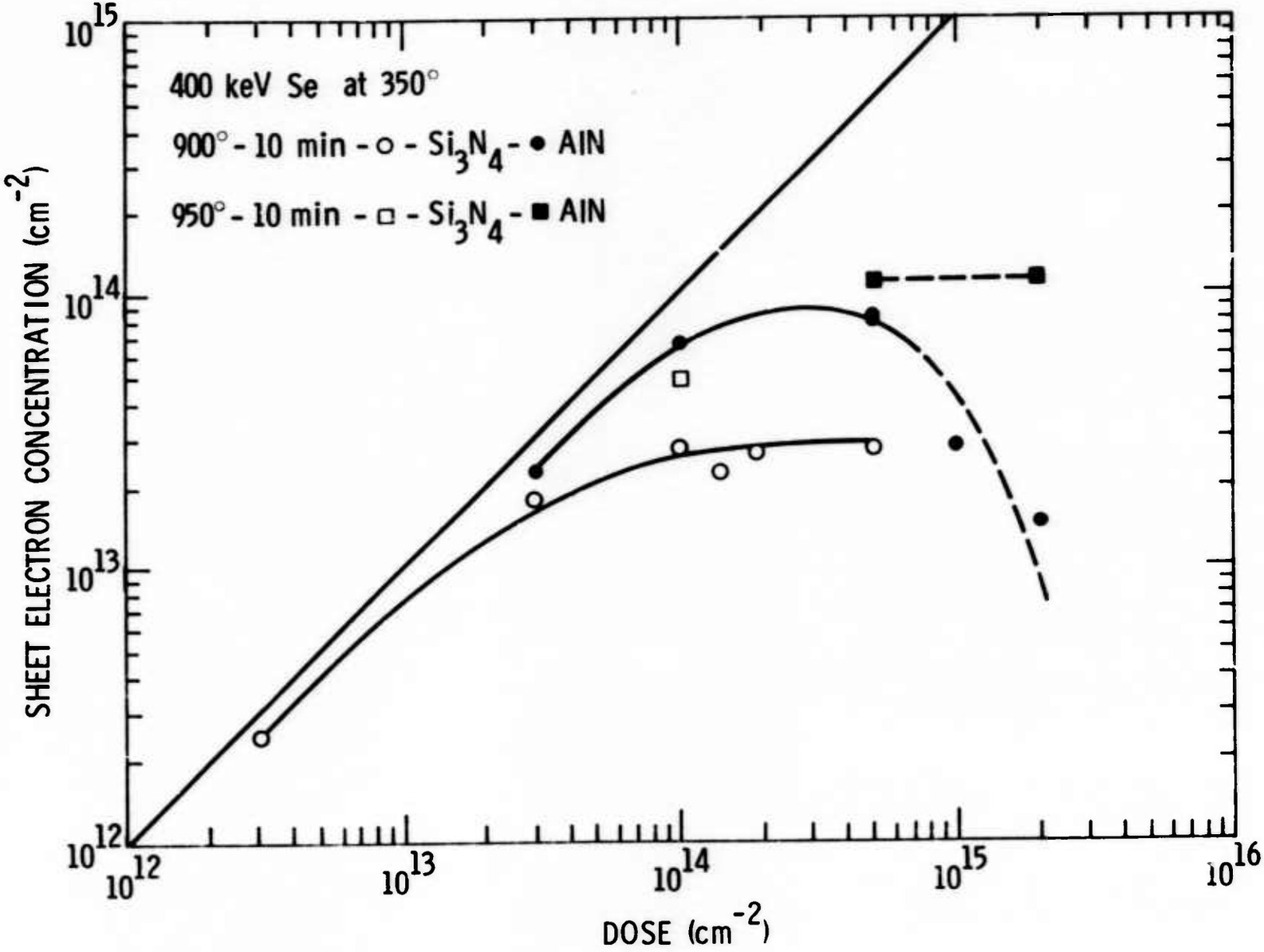


Fig. 3.3-6 Sheet electron concentration vs dose for GaAs samples implanted at 350°C with 400 keV selenium ions, and annealed under the conditions indicated on the figure.

observed at doses of 1×10^{14} and 5×10^{14} selenium ions/cm^2 when an AlN cap was used. However, the sheet electron concentration obtained with the use of an AlN cap seems to drop rapidly at doses beyond about 5×10^{14} ions/cm^2.

A few tellurium-implanted samples have also been annealed with AlN caps. Profile results for two of these are compared with a typical result obtained using a Si_3N_4 cap in Fig. 3.3-7. In the tellurium case, also, it seems possible to achieve significantly higher electron concentrations by using an AlN cap as compared with the Si_3N_4 cap. Again, the electron concentration profile for the same dose and energy is not as deep as that observed with the Si_3N_4 cap.

In the preceding technical report,[18] results were presented for several tellurium-implanted samples on which the Si_3N_4 cap lifted during annealing. A higher peak electron concentration was observed in these samples than was seen in similar tellurium-implanted samples, for which there was no lifting of the Si_3N_4 cap. One possibility suggested in that report[18] was that the lifting of the cap may have resulted in some limited introduction of arsenic vacancies which would tend to compensate for the excess gallium vacancy concentration produced by implanting tellurium. Such arsenic vacancy formation might result in a higher doping efficiency for the implanted tellurium. In an attempt to check the validity of this idea, experiments have been carried out in which tellurium-implanted samples were annealed in hydrogen without a cap, at temperatures ranging from 550°C to 700°C for a period of 10 minutes. Following this anneal,

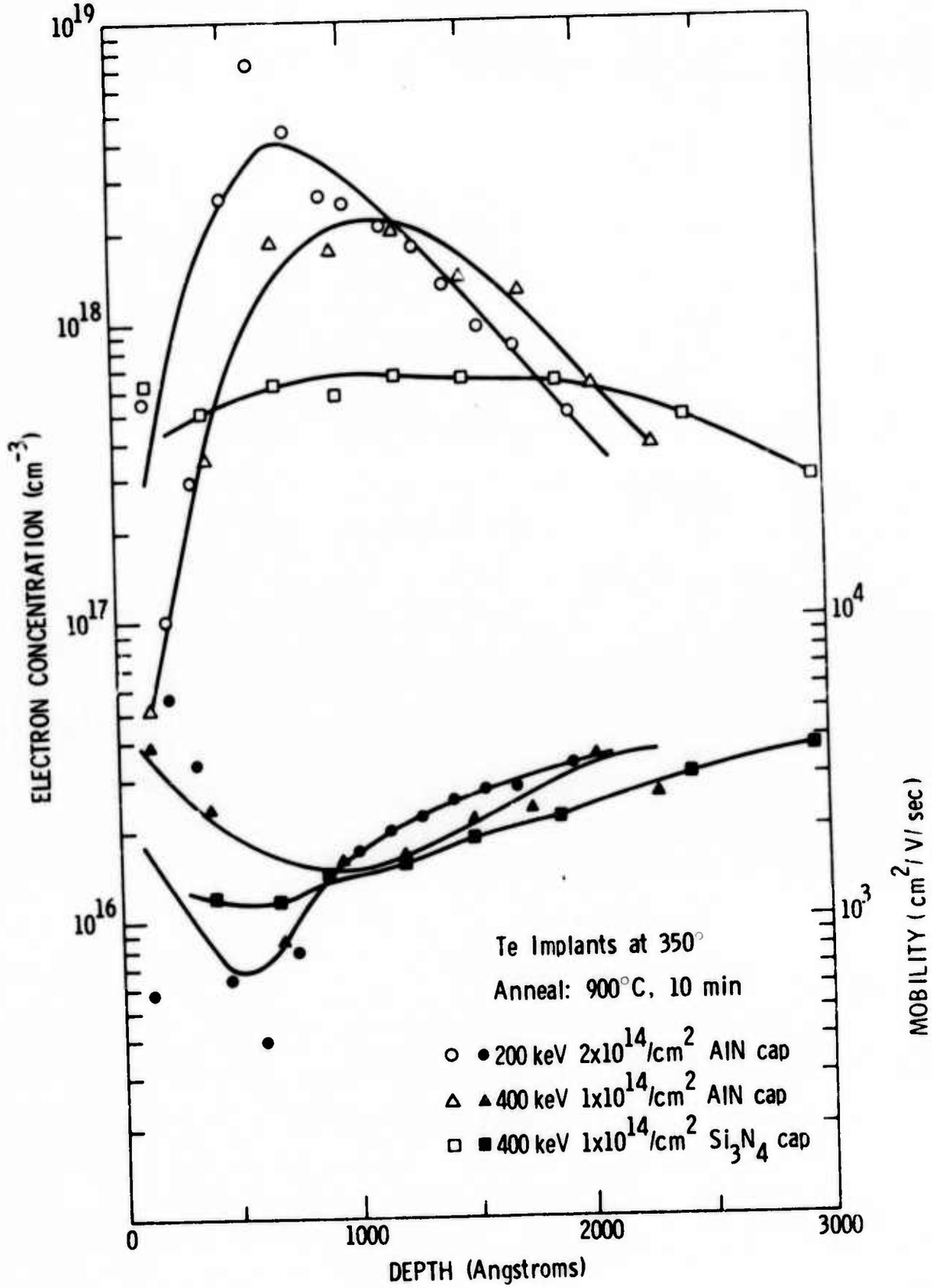


Fig. 3.3-7 Electron concentration and mobility profiles for GaAs samples implanted at 350°C with tellurium and annealed at 900°C for 10 minutes. Implant dose and energy and annealing cap are indicated on the figure.

they were capped with Si_3N_4 and annealed at 900°C for 10 minutes. It was thought that the pre-anneal might result in the introduction of arsenic vacancies which would diffuse into the sample during the subsequent capped 900°C anneal. The electron concentration and mobility profiles measured for a sample which received a 600°C pre-anneal are compared in Fig. 3.3-8 with similar data from a typical sample annealed at 900°C for which there was no lifting of the Si_3N_4. The profiles are quite similar for the two samples. Sheet electron concentration and mobility data for all the pre-annealed samples are listed in Table 3.3-1 together with the corresponding values for a sample in which there was no lifting of the nitride. There is little deviation in the values for the different samples except for one of the pre-annealed samples that exhibited lifting of the nitride cap during annealing. Since the pre-anneal-type of experiment does not exactly duplicate the conditions which might prevail in a sample for which the Si_3N_4 cap lifts during annealing, it is not clear at present whether or not this type of experiment is adequate to investigate the possibility that the introduction of arsenic vacancies may account for enhanced electron concentrations observed in samples on which the nitride cap lifts during annealing.

Work is still in progress to further investigate the doping levels which can be achieved by implantation of selenium and the use of an AlN annealing cap. Present results clearly show that it is possible to achieve electron concentrations at least as high as $3\text{-}4\times10^{18}$ and high doping efficiencies (66 percent in the case of a sample implanted with a

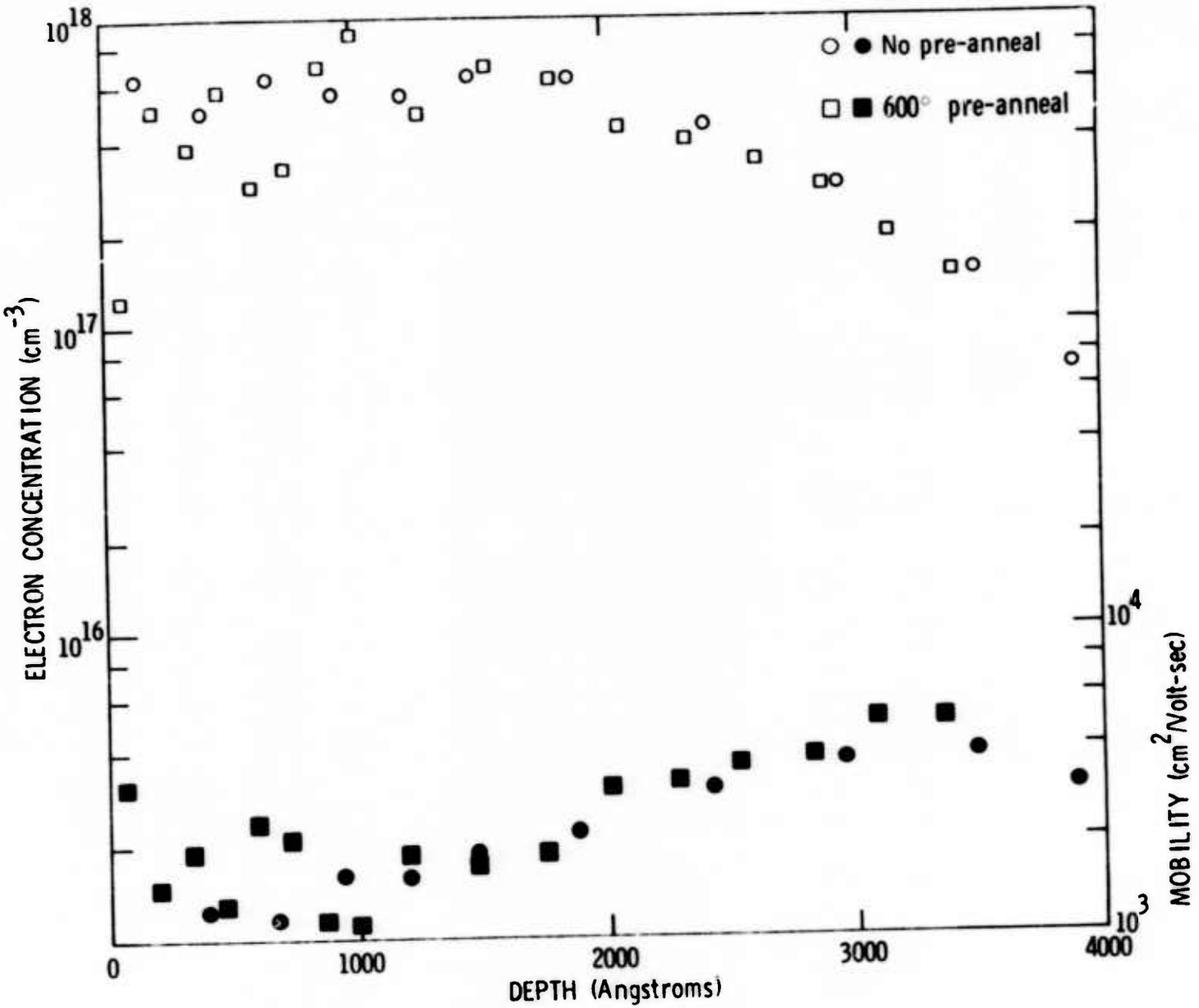


Fig. 3.3-8 Comparison of electron concentration and mobility profiles for two GaAs samples implanted at 350°C with 1×10^{14} 400 keV tellurium ions/cm^2 and annealed at 900°C for 10 minutes with and without a 600°C uncapped pre-anneal in hydrogen, as indicated.

Table 3.3-1 Sheet Electron Concentration and Mobility Values for GaAs Samples Implanted at 350°C with 1×10^{14} 400 keV Tellurium ions/cm^2, and Annealed in Hydrogen without a Cap at the Temperatures Shown before Annealing at 900°C for 10 Minutes with a Si_3N_4 Cap.

Pre-Anneal Temperature	N_s (cm^{-3})	μ(cm^2/volt-sec)
550°	1.16×10^{13}	2346
600	1.08×10^{13}	2433
600	1.29×10^{13}	2614
650	1.10×10^{13}	2490
650*	2.08×10^{13}	2805
700	1.19×10^{13}	1819
Test Sample without Pre-Anneal	1.44×10^{13}	2474

*Si_3N_4 cap lifted during annealing

dose of 10^{14} ions/cm^2 and annealed at 900°C). The results obtained with with both AlN and Si_3N_4 caps indicate that it should be possible to achieve doping levels of 10^{18} or higher to depths which are comparable to the thickness of the n-type channel region in FETs. The sheet resistance of such doped contact regions would be at least an order of magnitude lower than the sheet resistance of channel regions. Some samples annealed with AlN caps have shown ohmic behavior of evaporated Au-Ge contact dots without any alloying. It is possible that the probability of achieving non-alloyed ohmic contacts could be increased by implanting some selenium at a low energy so as to enhance the electron concentration near the surface of the GaAs where it falls to lower values in most samples.

The maximum electron concentration shown on the profile in Fig. 3.3-4 for the sample implanted with a dose of 10^{14} ions/cm^2 is about half the expected maximum selenium concentration calculated from LSS range parameters (7×10^{18}/cm^3). A similar peak electron concentration has recently been reported for 400 keV selenium implants with a dose of 1×10^{14} ions/cm^2 annealed at 900°C with a pyrolytically-deposited Si_3N_4 cap.[30] These results suggest that ideas recently advanced by Gibbons and Tremain[31] concerning limitation of doping levels in ion implantation of GaAs due to degeneracy effects may be incorrect, since the doping level achieved in the 10^{14} implants, is at least five times as high as that predicted by Gibbons and Tremain. The fact, that at doses higher than 10^{14}/cm^2 a significant increase in the maximum electron concentration is

not observed, may be due either to unannealed radiation damage effects or, possibly, to complexing of the implanted selenium. Comparison of mobilities in samples with various doses of selenium, and after annealing at different temperatures, may help decide between the two mechanisms; however, there does not seem to be sufficient data at present to establish a trend in the mobility results.

The difference in selenium levels achieved using sputtered Si_3N_4 or AlN caps clearly indicates the importance of the annealing cap or of the conditions at the surface of the GaAs sample during annealing. The aforementioned results with pyrolytically-deposited Si_3N_4[30] indicate that the method of deposition of the cap layer may be equally as important as the material which is used for that layer. The reasons for the difference in our results using Si_3N_4 or AlN caps are not clear at present. Experiments have been performed in which epitaxial layers of GaAs with electron concentrations near $10^{17}/cm^3$ have been annealed at temperatures as high as 900°C with either Si_3N_4 or AlN as a cap. The results indicate that our Si_3N_4 material can act as a good protection for the GaAs and prevent changes in carrier concentration greater than about 10 percent. However, the samples annealed with AlN as a cap have all shown large changes in the electron concentration. In addition, AlN has been used as an annealing cap on low-dose sulfur implants. Preliminary results indicate that lower electron concentrations are achieved when AlN is used than when Si_3N_4 is used as the annealing cap. These data suggest that AlN may not be as good a diffusion barrier for GaAs as Si_3N_4.

A clue to understanding the difference in results obtained in high-dose implants with sputtered AlN or sputtered Si_3N_4 caps may be contained in the photoluminescence results presented in Fig. 3.3-9. Samples annealed with an AlN cap typically show a peak at an energy near 1.4 eV which is absent in samples annealed with a Si_3N_4 cap. On the other hand, samples annealed with a Si_3N_4 cap show a peak at an energy of about 1.25 eV which is thought to be associated with gallium vacancies-donor complexes.[32] The nature of the center responsible for the peak at 1.4 eV in samples annealed with an AlN cap is not well established at present. There is some indication that it may be associated with arsenic vacancies; however, this must be regarded as only a preliminary conclusion. It is difficult to establish whether or not the presence of either of these peaks indicates a center which is significant in determining the carrier concentration observed in implanted samples. Further experiments will be required in order to elucidate the mechanisms responsible for the differences observed in doping levels when different materials are used as an annealing cap.

3.3.3 Recrystallization of Amorphous GaAs

In the implantation of silicon the formation of an amorphous layer, and its epitaxial regrowth, play an important role in obtaining high electrical activity at low annealing temperatures. The behavior of amorphous layers on GaAs have not been studied so far. We have begun an

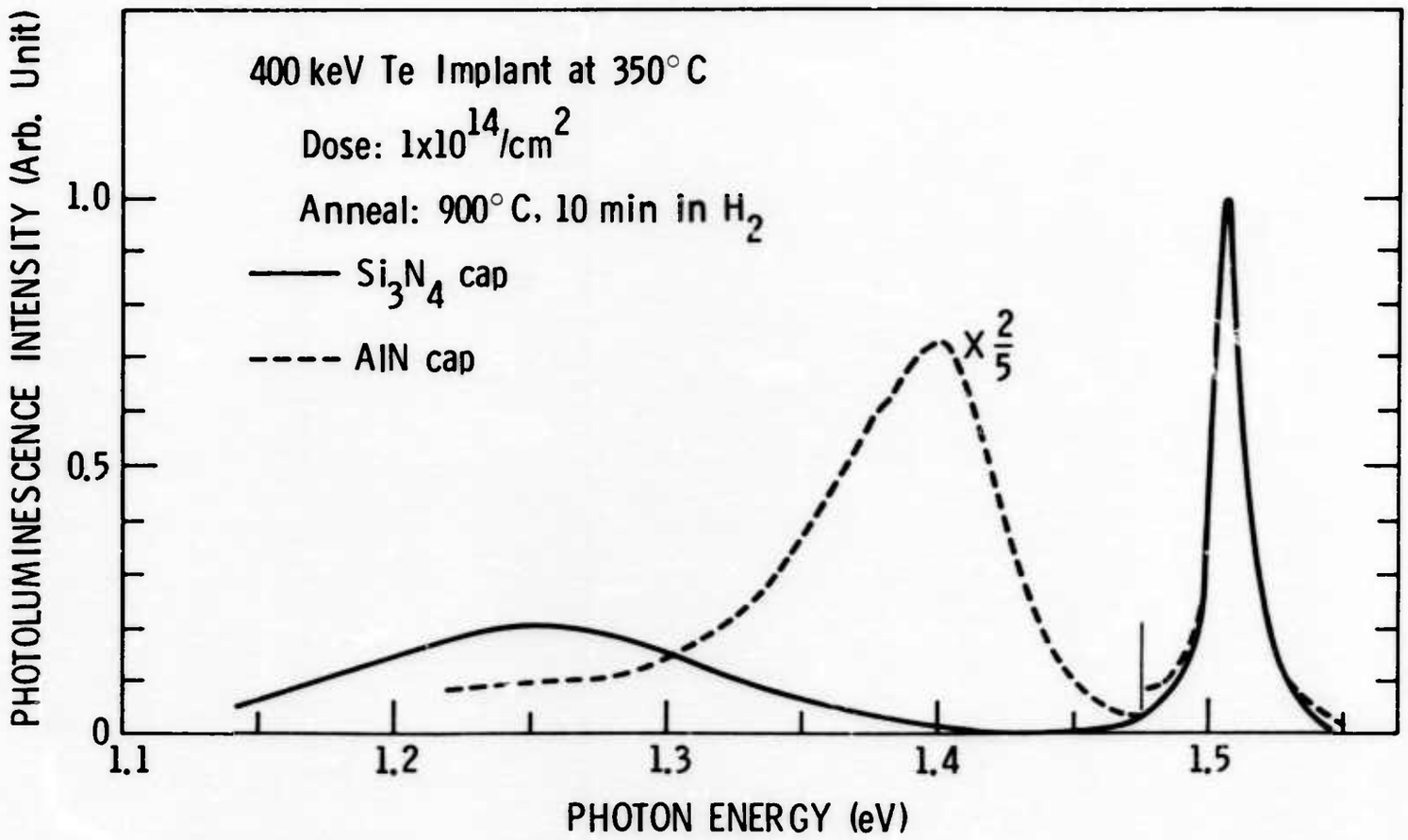


Fig. 3.3-9 Photoluminescence spectra for GaAs samples implanted at 350°C with 1×10^{14} 400 keV tellurium ions/cm^2 and annealed at 900°C for 10 minutes with the indicated caps.

investigation of the annealing behavior of amorphous layers produced by selenium implantation, including the dependence of the annealing on crystal orientation. Figure 3.3-10 shows the energy spectra of channeled 400 keV protons, backscattered from a (100)-oriented sample which was implanted at 80 K with 3×10^{13} 400 keV selenium ions/cm^2. The backscattered yield for the channeled beam is equal to the random yield near channel 160, for the unannealed sample and after annealing to 100°C and 200°C. This indicates that an amorphous layer was present on the surface of the sample. Some regrowth of this layer on the underlying crystal is indicated by the data taken following the 200°C anneal. After annealing at 300°C the amorphous layer has disappeared, and evidence for recrystallization from the surface as well as from the amorphous-crystalline interface is seen. Such recrystallization from the surface is undesirable, since it may result in high dislocation densities and the formation of twinned structures. Similar results have also been seen for (111)-oriented samples. These results suggest that it may be possible to produce epitaxial regrowth in the temperature region between 200°C and 300°C. This will be explored in future work.

4.0 FUTURE PLANS

4.1 Epitaxial Growth and Material Characterization

4.1.1 High-Resistivity GaAs Layers

A new system with a fused quartz cradle and BN boat has been assembled and is in operational condition. This system is significantly different from the former one in that the source of C, the graphite boat,

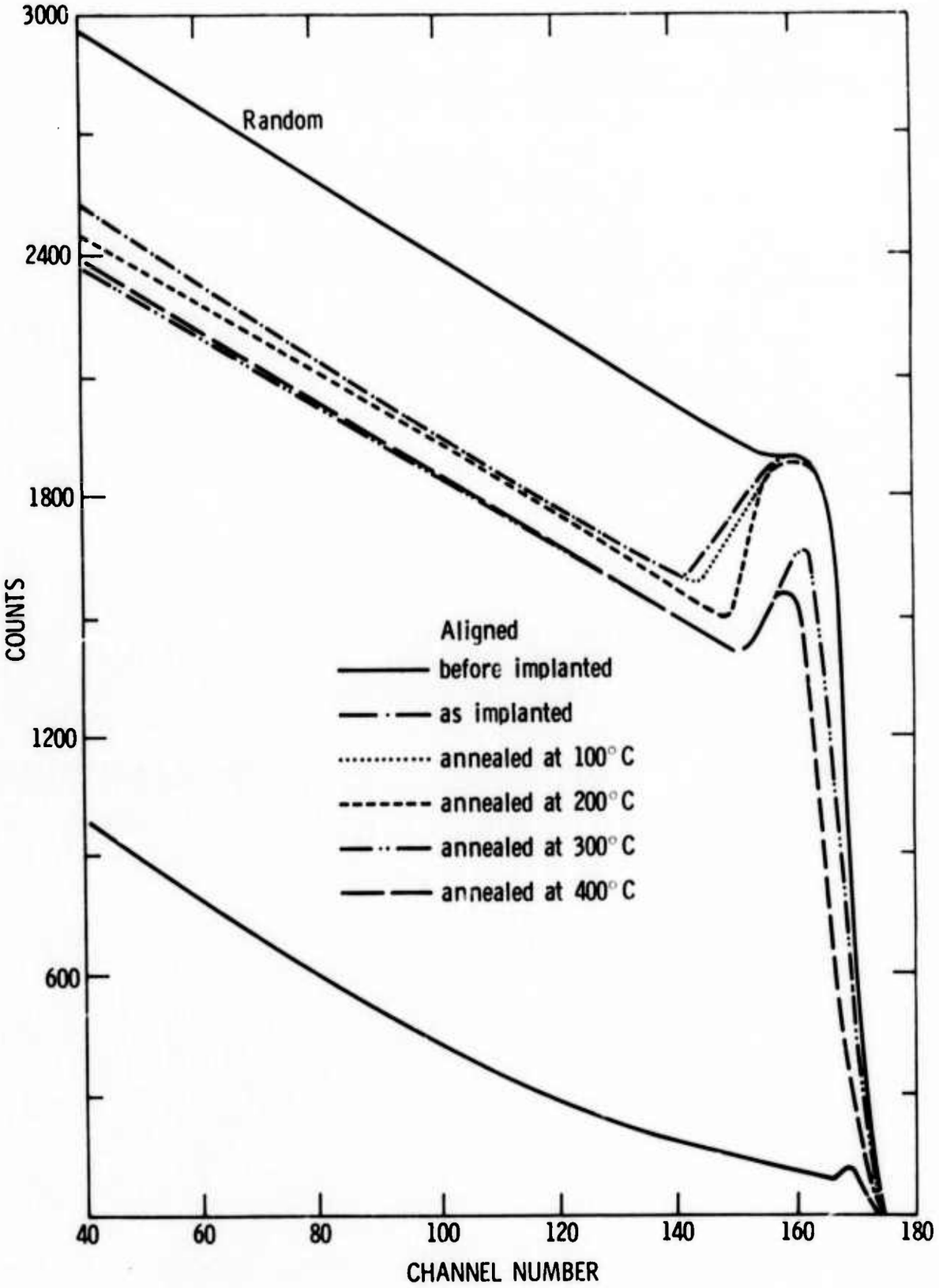


Fig. 3.3-10 Aligned and random backscattering spectra for 400 keV protons incident on a (100)-oriented GaAs sample which was implanted at 80 K with 3×10^{13} 400 keV selenium ions/cm^2. Spectra are shown before and after implantation and after annealing to the indicated temperatures.

has been eliminated. Growths are currently being made at a bakeout temperature of 700°C. The effects of growth conditions on the incorporation of residual impurities, chromium and oxygen in this SiO_2-BN-H_2 system will be studied.

Detailed studies of deep levels in the epitaxial layers using thermally-stimulated capacitance techniques will also be conducted.

4.1.2 Multiple Layer Liquid Phase Epitaxy

The immediate goal in this area of study at the Science Center will be to reproducibly grow high-resistivity buffer layers in the SiO_2-C-H_2 system. An attempt will be made to identify the source of impurities in the 10^{15} cm^{-3} carrier density material we have grown, and the bakeout temperature will be varied to locate the transition temperature in this sytem.

4.1.3 Material Evaluation

4.1.3.1 Characterization of FETs Fabricated on Epitaxial and Implanted GaAs. Emphasis will be placed on buffered epitaxy and ion implantation. Tests will be conducted under pulsed conditions to seek substrate effects and interface effects. Selenium will receive greater attention as an n-type implanted dopant and selective area implantation will also be used to enhance contacts.

4.1.3.2 Low-Frequency Noise Behavior of Avalanche Diodes. Further measurements of the short-circuit current spectrum at low frequencies vs current density will be made to gain more information about the effective multiplication factor and the intrinsic response time.

4.1.3.3 Ionization Rate Study in GaAs. In the coming term, further multiplication measurements will be made. The light source will be changed to a mercury vapor lamp with extreme narrow band dielectric filters. This modification allows a better understanding of the traps inside the material and provides better control of the illumination wavelengths. Data taken will be further analyzed to give α and β.

4.2 Semi-Insulating Materials

Study of high-Cr material will be completed with Auger measurements in order to further verify reversal from n- to p-type and to better calculate the impurity densities. Efforts will be made to interpret the voltage profiles of the low-Cr n-i-n samples. New materials produced by Crystal Specialties will be analyzed. Capacitance measurements in the time domain will be continued for the sake of more information on the samples and as a potential alternative to replace the Auger measurements for characterization of the material. Study of the interface between the substrate and n-type layers will be initiated. Noise measurements on FET devices will be used as tests for interface defects. Comparisons between devices made on ion-implanted and epitaxial layers will aid distinction between noise sources in the bulk and at the interface.

The use of the SIMS equipment to monitor intentional tin doping and other profiles through the thin FET channels and across the interface into the substrate is being planned, using steady ion beam erosion to slowly erode into the GaAs.

4.3 Ion Implantation

Investigation of the doping which can be achieved by selenium implantation using an AlN cap will be completed. The effect of using Si_3N_4 caps with different properties on both high- and low-dose implants will be studied by varying the sputtering conditions under which the nitride films are deposited, and measuring the properties of the implanted layers after annealing. The effect of different substrate materials on the electron concentration profile resulting from low-dose sulfur implants will be continued in an effort to determine whether or not it is possible to achieve epitaxial regrowth.

5.0 REFERENCES

1. R. H. Bube, in Physical Chemistry, Vol. 10 (Academic Press, New York, 1970), p. 543.
2. M. G. Buehler, Solid-State Electron. 15, 69 (1972).
3. R. H. Haitz, "Noise of a Self-Sustaining Avalanche in Silicon: Low Frequency Noise Studies," J. Appl. Phys. 38, 2935 (1967).
4. H. K. Gummel and J. L. Blue, "A Small-Signal Theory of Avalanche Noise in IMPATT Diodies," IEEE Trans. Electron Devices ED-14, 569 (1967).
5. R. L. Kuvås, "Noise in IMPATT Diodes: Intrinsic Properties," IEEE Trans. Electron Devices ED-10, 220 (1972).
6. D. H. Lee, "Low Frequency Noise of Ion Implanted Double-Drift IMPATT Diodes," Proc. of IEEE 61, 666 (1973).
7. J. A. Ringo and P. O. Lauritzen, "Low Frequency White Noise in Reference Diodes," Solid-State Electron. 15, 625 (1972).

8. R. Kuvås and C. A. Lee, "Quasistatic Approximation for Semiconductor Avalanches," J. Appl. Phys. 41, 1743 (1970).

9. I. M. Naqvi, "Effects of Time Dependence of Multiplication Process on Avalanche Noise," Solid-State Electron. 16, 19 (1973).

10. G. E. Stillman, C. M. Wolfe, J. A. Rossi, and A. G. Foyt, "Unequal Electron and Hole IMPATT Ionization Coefficients in GaAs," Appl. Phys. Lett. 24, 471 (1974).

11. C. A. Lee, R. A. Logan, R. L. Batdorf, J. J. Kleimack, and W. Wiegmann, "Ionization Rates of Holes and Electrons in Silicon," Phys. Rev. 134, A761 (1964).

12. R. A. Logan and S. M. Sze, "Avalanche Multiplication in Ge and GaAs p-n Junctions," J. Phys. Soc. Jap. Suppl. 21, p. 434 (1966).

13. H. Hasegawa, K. E. Forward, and H. Hartnagel, "Improved Method of Anodic Oxidation of GaAs," Electron. Lett. 11, 53 (1975).

14. H. Muller, F. H. Eisen, and J. W. Mayer, "Anodic Oxidation of GaAs as a Technique to Evaluate Electrical Carrier Concentration Profiles," J. Electrochem. Soc.: Solid-State Science and Technology 155, 651 (1975).

15. R. A. Logan, B. Schwartz, and W. J. Sandburg, "The Anodic Oxidation of GaAs in Aqueous H_2O_2 Solution," J. Electrochem. Soc.: Solid-State Science and Technology 120, 1386 (1973).

16. S. M. Spitzer, B. Schwartz, and G. D. Weigle, "Preparation and Stabilization of Anodic Oxides on GaAs," J. Electrochem. Soc.: Solid-State Science and Technology 122, 397 (1975).

17. V. Wrick and J. Berenz, "Anodic Oxidation of InP," to be published.

18. F. H. Eisen, et al., "Investigation of Technical Problems in Gallium Arsenide," Semi-Annual Technical Report No. 3, AFCRL-TR-75-0093, Section 3.2.2, February 5, 1975, Contract No. F19628-74-C-0038.

19. G. A. Allen, J. Phys. D 1, 593 (1968).

20. J. Blanc and L. R. Weisberg, Nature 192, 155 (1961).

21. Section 3.2.1 in Ref. 1.

22. G. R. Cronin and R. W. Haisty, J. Electrochem. Soc. 111, 874 (1964).

23. M. E. Weiner and A. S. Jordan, J. Appl. Phys. 43, 1767 (1972).

24. J. R. Waldrop and J. S. Harris, to be published, J. Appl. Phys., Dec., 1975.

25. D. P. Kennedy, P. C. Murley, and W. Kleinfelder, IBM J. Res. Develop. 12, 399 (1968); D. P. Kennedy and R. R. O'Brien, IBM J. Res. Develop. 13, 212 (1969); D. P. Kennedy, "Mathematical Simulation of the Effects of Ionizing Radiation on Semiconductors," Scientific Report No. 1, AFCRL-68-0246, April, 1968, Contract No. F19628-67-C-0116.

26. C. Goldberg, Solid State Electron. 7, 593 (1964); J. R. Hauser and M. A. Littlejohn, Solid State Electron. 11, 667 (1968).

27. W. van Roosbroeck, Phys. Rev. 123, 474 (1961); C. Popesco and H. K. Henisch, Phys. Rev. B11, 1563 (1975).

28. F. H. Eisen, et al., "Investigation of Technical Problems in Gallium Arsenide," Semi-Annual Technical Report No. 2, AFCRL-TR-74-0371, p. 72, July, 1974, Contract No. F19628-74-C-0038.

29. W. S. Johnson and J. F. Gibbons, Projected Range Statistics in Semiconductors (Stanford University Book Store, 1970).

30. J. P. Donnelly, W. T. Lindley, and C. E. Hurwitz, Appl. Phys. Lett. 27, 41 (1975).

31. J. F. Gibbons and R. E. Tremain, Appl. Phys. Lett. 26, 199 (1975).

32. W. E. Williams and H. B. Bebb, in Semiconductors and Semimetals, R. K. Willardson and A. C. Beer, eds. (Academic Press, New York, 1972), p. 321.