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CHARGE-COUPLED SCANNED IR IMAGING SENSORS

Elliott S. Kohn
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Princeton, New Jersey 08540

15 MAY 1975

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to produce the video signal. Operation is similar to that of a vidicon. The shift register had transfer losses as low as 5×10^{-4} per transfer as measured with an electrical input. Visible images were sensed directly by illumination of the shift register through the gaps as well as through the unthinned substrate. Infrared images ($1.1 \mu\text{m} < \lambda < 3.5 \mu\text{m}$) were sensed by the Schottky-barrier detectors illuminated through the (transparent) substrate. The two imaging modes could be easily distinguished by their spectral sensitivities as well as by their response to changes in their separate integration times. All IR measurements were made at 77°K . Uniformity was within a few percent, and objects at 110°C could be detected. A scheme for observing low-contrast, thermal scenes without requiring the charge-coupled shift register to carry the entire background signal has been implemented in the design of this chip. Operation in this mode was also demonstrated.

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PREFACE

This Technical Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-73-C-0282 and ARPA Order No. 2444. It describes work performed from 1 July 1974 to 30 April 1975, in the Integrated Circuit Technology Center, the Process and Applied Materials Research Laboratory, and the Materials Research Laboratory. E. S. Kohn and M. L. Schultz were the principal investigators; the respective Project Supervisors were K. H. Zaininger and H. Kressel. Other members of the Technical Staff who participated in the research were J. E. Carnes, P. Levine, and S. O. Graham. Sven Roosild and Freeman Shepherd were the AFCRL Contract Monitors.

The manuscript of this report was submitted by the author on 15 May 1975. The work on lead sulfide, as agreed, will be included in the Final Report under this contract. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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I. INTRODUCTION

Ever since the concept of charge-coupling was reported several years ago, imaging with charge-coupled devices has been an area of intense activity [1-3]. Visible imagers with full TV resolution have recently been demonstrated [4]. While devices with a variety of gate structures, channel types, and chip layouts have been reported, almost all of these have in common the use of silicon as the photo-absorbing material. Whether the photosensitive region is under the shift-register gates, under separate photogates, or at separate photodiodes, minority carriers photoexcited in the silicon form the charge packets to be clocked out. Since these devices have basically the spectral response and quantum efficiency associated with silicon photodiodes, they are useful as infrared imagers to wavelengths as long as 1.1 μm .

There is considerable interest in imagers sensitive to longer wavelength infrared radiation. Imagers sensitive in the 2- to 3- μm range are useful to the military for viewing high-contrast scenes involving jet and rocket plumes, while devices responding to radiation as far out as 4.5 μm can image 300°K scenes by their own thermal radiation, and are of interest for industrial and medical applications as well as military applications [5].

Infrared detector arrays which accomplish this are already in existence, and, in some cases, perform close to their theoretical limit. These imagers (FLIRs*) use linear arrays of cooled infrared detectors with mechanical scanning in the *orthogonal direction*. Their applications are restricted primarily by their high cost. A considerable amount of effort has gone into the development of vidicons for use in the infrared, but the technical problems

*Forward Looking InfraRed.

1. J. E. Carnes, "Charge-Coupled Imaging: State-of-the-Art," 1973 Solid State Devices, Conference Series #19, Inst. of Physics, London and Bristol, 1974.
2. W. F. Kosonocky, "Charge-Coupled Devices: An Overview," WESCON Technical Papers, Session No. 2, Sept. 1974.
3. D. F. Barbe, IEEE Proc. 63, 38 (1975).
4. RCA Data Sheet SID 51232, Lancaster, PA, Jan. 1975.
5. IEEE Proc., Special Issue on Infrared Technology for Remote Sensing, Jan. 1975.

encountered are formidable. Thus, an infrared, charge-coupled imager would be a welcome device.

A prime concern in the development of any thermal imager is the large background radiation present in the thermal scene. A typical requirement for a thermal viewer is to make possible recognition of an object at 300.1°K in a uniform 300°K scene. In this case, the "signal" is the difference between the number of photons arriving from the hotter object and the number arriving from an equal solid angle of the background. This signal can be less than 1% of the background, but, in order to detect it, the sensor must read the entire background. It is this requirement of handling the entire background that taxes the target storage and beam density capability of standard vidicons and makes the solid state alternative so attractive. But, regardless of the capability of the detector to handle the background without saturating, the presence of the background severely aggravates the problem of detector non-uniformity. If the detectors vary in sensitivity by just a few percent, the nonuniformities in the picture due to the background would overwhelm the signal with fixed pattern noise.

Complicating the problem is the fact that most types of infrared detectors cannot be produced even as uniformly as detectors fabricated for the visible region. Detector nonuniformity is not a problem for visible imagers because of the high contrast usually present in the reflected visible light from normal scenes, but it is always a major consideration for thermal imagers. That is why, in FLIRs, the separate amplifiers for the 100 or more detectors in the linear array must be individually trimmed to compensate for differences in detector sensitivities. This compensation method contributes to the high cost of line scanners and is clearly impractical for an area imager.

Thus, for thermal area imagers, excellent uniformity is an essential requirement. Fortunately, the requirement for high quantum efficiency can be relaxed for area arrays. Line scanners (FLIRs) require reasonably sensitive detectors to achieve background-limited performance, but area imagers, having frame storage, can achieve the same quality of performance with detectors whose quantum efficiency is two orders of magnitude lower. Thus, detectors with insufficient sensitivity for line arrays may be quite suitable for area arrays. The need for good uniformity and the modest requirement on sensitivity suggest the use of Schottky-barrier detectors. These detectors are discussed below.

There are several approaches to the design of infrared, charge-coupled imagers. One is the fabrication of charge-coupled shift registers on materials having the desired intrinsic response [6]. Such materials include InAs, InSb, and HgCdTe. Infrared radiation would be absorbed in the wafer, generating minority carriers which would then be transported just as in silicon devices. Unfortunately, at the present time, the fabrication of such devices on materials other than silicon creates severe technological problems. A second approach is the fabrication of charge-coupled shift registers on silicon wafers with separate infrared detectors prepared on the wafer. Schottky barriers are a natural choice though photoconductive films and heterojunction detectors are other possibilities. A third approach is the use of extrinsic silicon. Since the mode of operation requires freeze-out of carriers, the device would have to be cooled to a temperature considerably lower than that required for most other infrared detectors. The entire chip could be frozen out as reported by Nelson [7] and the shift register run in the accumulation mode, a very different mode of operation. Alternatively, different dopants could be used for the detectors and for the shift register so that the former would be frozen out but not the latter. Such a device could be run in the "normal" depletion mode.

Our approach to the design of infrared-sensitive, charge-coupled imagers has been to use well-known technologies, namely charge-coupled shift registers and Schottky-barrier detectors fabricated on silicon wafers. This requires that the majority-carrier signals from the detector be converted to minority-carrier packets for transport by the shift registers. A method for accomplishing this, using field-effect transistors, was proposed by Air Force Cambridge Research Laboratories.*

The method we adopted was proposed by W. F. Kosonocky and B. F. Williams of RCA Laboratories, and has the advantage that the large background signal from a thermal scene need not be transferred to the shift registers. While this technique does not, by itself, compensate for nonuniformities in the detector array, it does make better use of the shift register's dynamic range

*S. Roosild and F. Shepherd, private communication.

6. A. J. Steckl et al., Proc. IEEE 63, 67 (1975).

7. R. D. Nelson, Applied Physics Letters 25, 568 (1974).

and thereby makes possible the use of frame comparison techniques. To test these ideas, we fabricated 64×1 linear arrays of Schottky-barrier detectors coupled with three-phase, charge-coupled shift registers. The devices were designed to permit viewing of high-contrast scenes in the 2- to 3.5- μm range while making it possible for us to demonstrate operation of the background-suppression scheme.

II. SCHOTTKY-BARRIER DETECTORS

A. DESIGN OF THE CCD WITH SCHOTTKY-BARRIER DETECTORS

A simple Schottky-barrier device is shown in Fig. 1(a). It consists of a metal evaporated onto a semiconductor wafer through a hole in an insulator. The device has electrical characteristics similar to those of a p-n junction, its characteristics depending upon the barrier height at the interface in much the same way that the characteristics of the p-n junction depend upon the band-gap. The barrier height itself depends upon the choice of metal as well as the choice and polarity of the semiconductor. Its value is nearly independent of semiconductor doping and minority-carrier lifetime. A reverse-biased

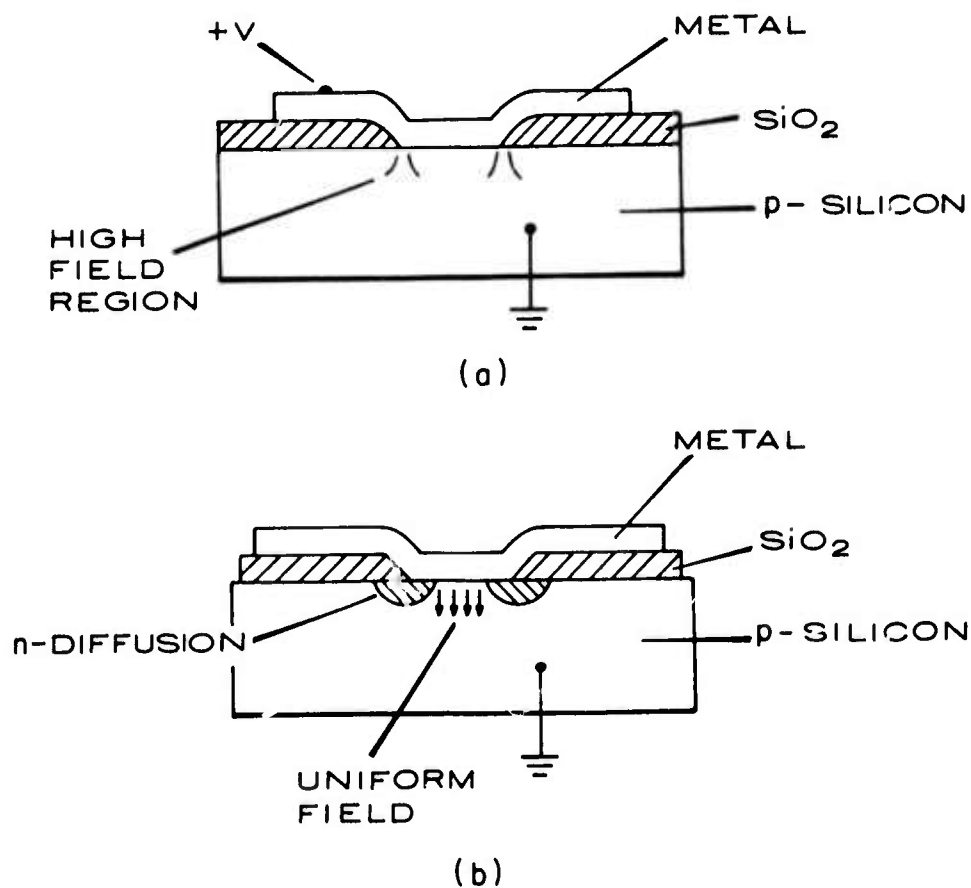


Figure 1. Schottky-barrier detectors: (a) without guard rings and (b) with guard rings.

Schottky-barrier diode exhibits dark current both from thermally generated minority carriers in the semiconductor being collected by the metal, and from majority carriers in the metal being thermally excited over the barrier into the semiconductor.

Since the barrier height in any detector of interest to us is smaller than half the bandgap of silicon, the latter process dominates. Similarly, the device can act as a photodetector by absorbing light either in the semiconductor or in the metal. In the former case, photoexcited carriers in the semiconductor are collected at the interface, and the spectral response is similar to that of a p-n junction. In the latter case, carriers are photoexcited over the barrier from the metal to the semiconductor where they become majority carriers.

The quantum efficiency in this case is relatively low, but the response extends to photon energies as low as the barrier height, a value that can be considerably smaller than the bandgap. The light to be detected by this process can be incident through either the semiconductor or the metal. If it is to be through the metal, the metal must be thin, and the uniformity of response is critically dependent upon the uniformity of the metal thickness. With light incident on the semiconductor, however, absorption takes place at the interface regardless of metal thickness, and a thick layer of metal ensures uniformity. The semiconductor need not be thinned since it is transparent in the spectral region of interest. Since the spectral yield in this mode depends almost entirely on the absorption process in the metal and transport over the barrier, the sensitivity is almost independent of such parameters as semiconductor doping and minority-carrier lifetime, thus eliminating major sources of nonuniformity in semiconductor detectors. It is for this reason that an array of Schottky-barrier detectors is potentially much more uniform in response than other types of semiconductor detectors and is probably limited in uniformity by the accuracy of the photolithographic process defining the boundaries of the detectors. There is experimental evidence that this is so [8]. For these reasons, we chose to use Schottky-barrier detectors

8. F. D. Shepherd et al., "Silicon Schottky-barrier Monolithic IR TV Focal Planes," to be published in *Advances in Electronics and Electron Physics*.

illuminated through the substrate. For our detectors, we chose palladium on p-type silicon.

Palladium is one of several metals that react chemically with silicon to form silicides having metallic properties. The actual Schottky barrier is therefore between the silicon substrate and the palladium silicide film formed beneath the original silicon surface. One advantage of this reaction is that surface oxides and other contaminants cannot influence the barrier as they could if the barrier were between silicon and a nonreacting metal. Another advantage is that the excess palladium can be removed, by etching, and the device contacted with a more conventional metal such as aluminum.

The structure used for coupling the Schottky-barrier detectors to the charge-coupled shift register is shown in Figs. 2 and 3. A row of Schottky-barrier metallizations is seen in the center of the chip. The center area of

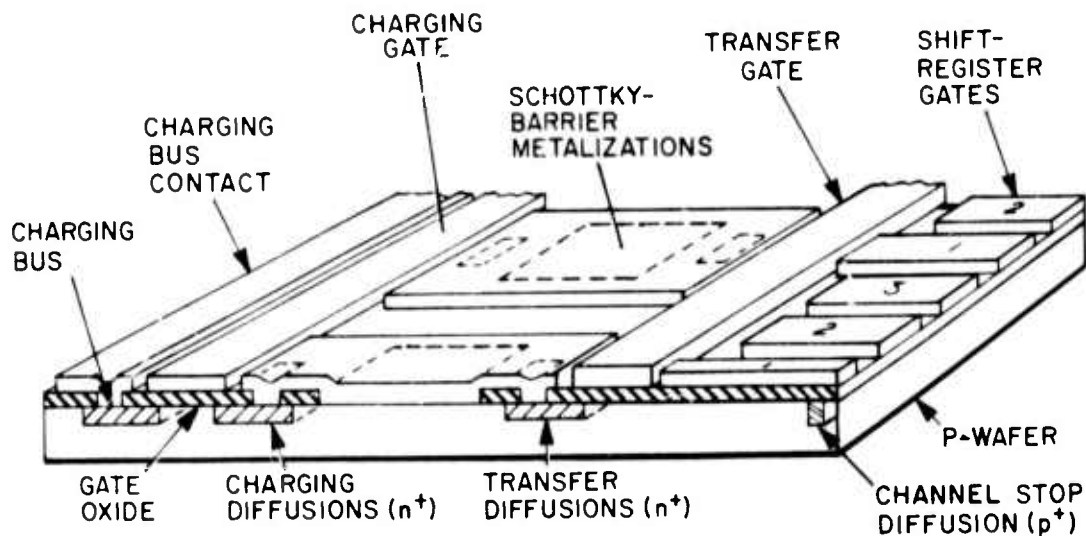


Figure 2. Structure used to couple Schottky-barrier detector to the charge-coupled shift register.

each metallization contacts the p-wafer forming the infrared-sensitive area. Each metallization also contacts individual charging and transfer diffusions. The transfer gate overlaps the transfer diffusions, and can couple them individually to the phase-1 gates of the shift register. The phase-1 gates are

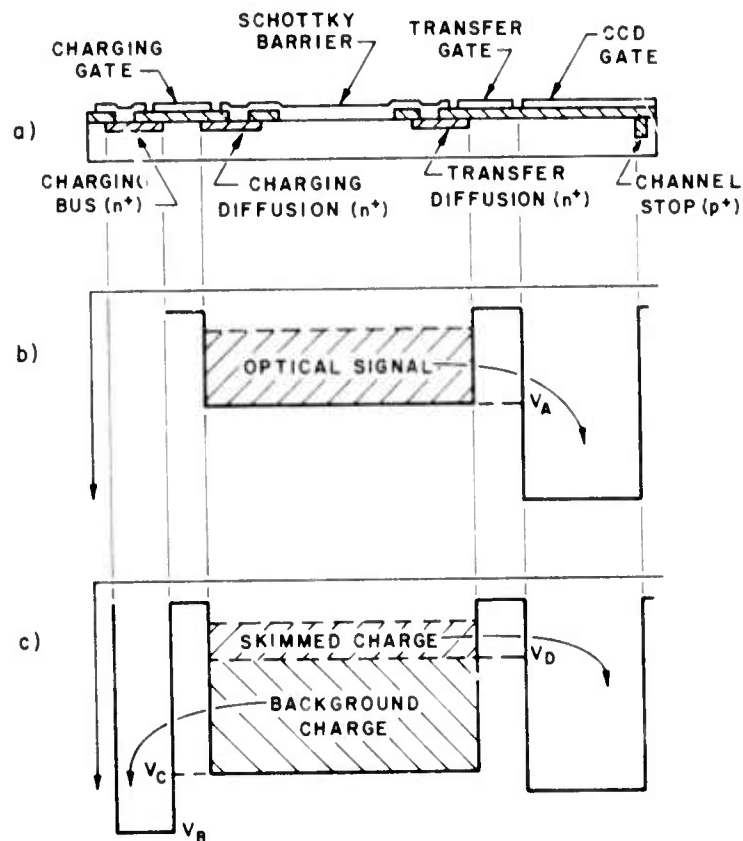


Figure 3. Electron potential energy profile of IR-CCD during operation. (a) Cross section of device. (b) Potential profile during operation in the vidicon mode. (c) Potential profile during operation in the thermal imaging mode. (Some details were omitted to aid clarity.)

wider than the other shift register gates for just this reason. The charging gate on the left of the detectors overlaps the individual charging diffusions and can couple them all at once to the charging bus diffusion. A channel stop diffusion at the right terminates the shift-register channel as shown in the illustration. The shift-register gates are connected to three phase busses to the right of the channel (not shown in Fig. 2). Strips of channel stop, also

not shown in the illustrations, are included between the detectors. They run from under the charging gate to under the transfer gate to prevent coupling between adjacent detectors or between adjacent charging and transfer diffusions. Such coupling could occur because of the inverted surface at the interface of the p-silicon and its oxide. The structure shown can be operated in two different modes: the high contrast mode or *vidicon mode*, and the background subtraction or *skimming mode*. A device designed for use in the high contrast mode does not require the charging gate or the charging diffusions. If these structures were included in the device, the charging gate can simply be biased negatively and ignored. The three-phase clock voltages are applied to the shift-register gates. At some time in the cycle, when the phase-1 shift register gates are on and the other two phases are off, a positive pulse is applied to the transfer gate making the potential under that gate V_A as in Fig. 3(b). The floating transfer diffusion will settle at a potential equal to V_A . All excess charge flows across the transfer gate channel into the deeper CCD potential well. After the transfer pulse ends, the shift register clocks out the charge packets. The next time, and each subsequent time, the transfer pulse is applied, the detectors are reset to the same potential, V_A , and the charges removed are stored in the phase-1 wells. These charges represent the photocurrent and dark current that accumulated at the detectors during the integration time and made up the video signal when read out. This mode of operation is somewhat different from that used in interline devices with photogates [1], where all minority carriers are removed from the detectors during the transfer time. It is more closely related to the mode of operation of a vidicon, since the detectors are reset to the same potential each frame, with the charge removed to do this making up the video signal. Hence, the designation, *vidicon mode*. An imager designed for use in this mode should have detectors whose charge storage capacity is about the same as a shift-register well.

During the transfer process, it is important for the phase-1 well to be large enough to hold the full detector charge without its surface potential rising above V_A . If necessary, phase-2 can be pulsed on during the transfer time to ease this requirement by sharing the transferred charge. Once the

transfer pulse is over, any single well can hold the entire charge packet because there is no longer the requirement that the surface potential at the well be greater than V_A .

When the device is operated in the vidicon mode as described above, the entire detector signal plus dark current must be carried out by the shift register. This is the usual method for sensing high-contrast images. For thermal images with only a few percent contrast, however, the dynamic range of the shift register would be better utilized if only the small fraction of charge containing the signal modulation were transferred out by the CCD and the large constant background charge containing no information were removed by an auxiliary drain. This can be accomplished with the help of the charging bus and the charging gate shown in Figs. 2 and 3. A large potential V_B is applied to the charging bus [Fig. 3(b)], which acts as an auxiliary drain for the constant background charge. A clock pulse is applied to the charging gate once per frame, setting the surface potential under it to V_C . This in turn sets the charging diffusions, Schottky-barrier gates, and transfer diffusions to V_C , since all excess electrons stored on these conductors will spill over the charging gate channel into the charging bus and be returned to the substrate. Thus, the initial level of the Schottky barrier is set by the charging gate pulse amplitude, not by the transfer gate pulse amplitude as in the vidicon mode described earlier. At the end of the integration period a small pulse is applied to the transfer gate which causes its surface potential to go to V_D [see Fig. 3(c)]. Now only the charge above V_D will drain into the CCD potential well and be read out. Presumably V_D is set to skim off all of the information-bearing charge but little or none of the constant background charge. This background charge is removed shortly thereafter when the charging pulse comes on and sets the Schottky barrier to V_C . It is assumed that the light falling on the detectors is sufficient to discharge each of them below V_D . In actual operation, V_C would be adjusted to ensure this condition. If this condition is satisfied, all of the photogenerated charge above transfer threshold is coupled to the CCD register. There is no capacitive division. The CCD capacitance need not be large compared with anything else. After the transfer pulse

is over, the charges are passed along the CCD register, and a video signal with enhanced contrast is coupled out. While the charges are being transferred out, the transfer gate is clocked off, so that there is no picture smear.

B. SCHOTTKY-BARRIER RESPONSE AND DARK CURRENT

The uniformity of response of Schottky-barrier detectors would be lost if the dark current were significant and variable among detectors in the array. A large dark current, even if uniform, would fill the shift-register wells. Dark current is therefore of fundamental concern to us.

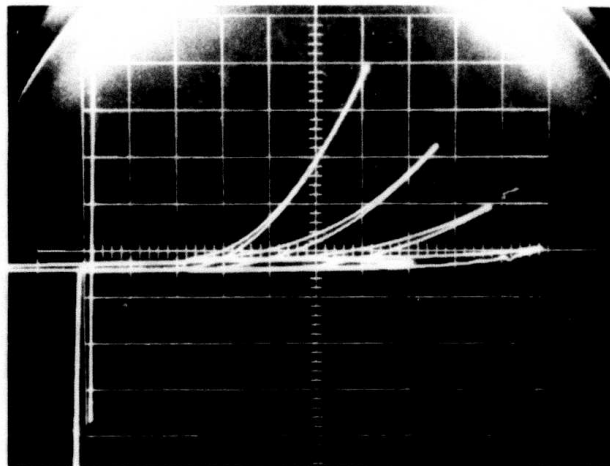
The theoretical dark current of an infrared-sensitive Schottky-barrier detector is due almost entirely to internal thermionic emission of carriers from the metal over the barrier into the semiconductor. The current density for this process is given by [9]

$$J = AT^2 \exp - \left(\frac{qV_b}{kT} \right) \quad (1)$$

where A is about $100 \text{ A/cm}^2 (\text{°K})^2$, V_b is the barrier height, q is the electronic charge, k is Boltzmann's constant, and T is the temperature. With V_b equal to 0.35 V for a palladium silicide-silicon barrier operated at 77°K , the current density is $7.7 \times 10^{-18} \text{ A/cm}^2$. At 300°K it would be 11.9 A/cm^2 . This must be compared with the charge storage capability of the CCD. The area of the Schottky barrier in our design is 4.5 mils^2 while the area of the CCD gate is 2.5 mils^2 . The capacitance of the gate oxide is $0.1 \text{ pF/mil}^2 = 10^{-13} \text{ F/mil}^2$. Thus, the capacitance of our gate is $0.25 \times 10^{-12} \text{ F}$. The charge that would cause the surface potential under the CCD gate oxide to change by 1 V is $0.25 \times 10^{-12} \text{ F} \times 1 \text{ V} = 0.25 \times 10^{-12} \text{ C}$. If the frame time is 1/30 second, the dark current at the Schottky barrier needed to produce this charge is $0.25 \times 10^{-12} \text{ C} / (1/30) \text{ sec} = 7.5 \times 10^{-12} \text{ A}$. Thus, the current corresponds to a current density at the Schottky barrier of $7.5 \times 10^{-12} \text{ A} / 4.5 \text{ mils}^2 = 7.5 \times 10^{-12} \text{ A} / 2.8 \times 10^{-5} \text{ cm}^2 = 2.7 \times 10^{-7} \text{ A/cm}^2$. Taking a 1-V swing at the CCD

9. S. Sze, *Physics of Semiconductor Devices* (Wiley-Interscience, New York, 1969).

interface as the maximum tolerable dark signal, we have 0.3×10^{-6} A/cm² as the maximum tolerable, dark-current density at the Schottky barrier. Thus, it is clear that our device cannot possibly operate at room temperature. At 77°K, the calculated dark current is below the maximum tolerable amount by a factor of more than 10^{10} . In practice, however, the margin can be considerably less because of field concentration at the edge of the device. This mechanism is difficult to account for analytically as it probably involves barrier-lowering, field emission, and avalanche multiplication as well as other effects, all occurring simultaneously in an uncertain geometry. The result is that the reverse current can increase rapidly with bias, depending on the substrate doping. This is shown in Fig. 4 for a test device made on a 10^{15} /cm³ doped p:Si wafer. In the figure, the reverse current averaged over the area is on the order of 30 mA/cm² at 5 V. The four barriers shown have areas of 5.8×10^{-4} cm², 2×10^{-4} cm², 0.9×10^{-4} cm², and 0.2×10^{-4} cm². A technique that has been successfully used to eliminate edge leakage in experimental devices is the inclusion of a diffused guard ring [10].



Horizontal scale: 1 V/div

Vertical scale: 0.01 mA/div

Figure 4. I-V curves of a set of palladium-silicide Schottky barriers at 77°K, showing the edge effect in the reverse characteristic.

10. J. M. Andrews and M. P. Lepselter, *Solid State Electronics* 13, 1011 (1970).

The original Schottky barrier is shown in Fig. 1(a); the same structure is shown in Fig. 1(b) except that a diffused guard ring has been added. Since the diffusion extends a few micrometers into the silicon wafer and does not end abruptly, there is much less field concentration here than at the sharp, abrupt edge of the metal-silicon interface shown in Fig. 1(a). Thus, the reverse breakdown voltage of the p-n junction can be quite high, and the presence of the guard ring eliminates the edge effects of the metal. While an IR-CCD with a diffused guard ring might eliminate the dark current, it was decided not to incorporate this idea into our design because of the large fraction of the area that would be made unavailable for infrared detection. This decision was vindicated since IR-CCDs were made without dark-current problems.

Another important source of dark current in a Schottky-barrier device involves surface inversion [11]. If the surface under the oxide is inverted, as it is in an n-channel (p-substrate) MOS device, the dark current measured at the Schottky barrier can include the dark current of the p-n junction associated with the inversion layer. The junction can cover a much larger area than the Schottky barrier itself. Still worse, parasitic channels can couple the detectors. This type of leakage can be pinched off with a channel stop diffusion or with a field plate biased to bring the surface beneath it into accumulation. In our IR-CCD, the Schottky barriers are surrounded on two sides by channel stop diffusion and on the other two sides by field plates, thus effectively eliminating this mechanism of dark current. In the test devices used to obtain the curves in Fig. 4, this mechanism may well have been responsible for the observed leakage.

The starting material for our Schottky-barrier test devices was (100)-oriented p-type silicon doped to $10^{15}/\text{cm}^3$. A thermal oxide was grown, and holes were opened in the oxide ranging in diameter from 2 mils to 10 mils. Palladium was evaporated in a sodium-free vacuum system while the silicon wafer was heated to permit the reaction forming palladium silicide. The unreacted palladium was removed with an etch, and gold was evaporated and defined to form contacts to the silicide. The chips were mounted with epoxy in IC flatpacks, each over a hole to permit rear illumination. Several diode

11. A. Y. C. Yu and E. H. Snow, J. Appl. Phys. 39, 3008 (1968).

contacts were bonded in each flatpack. The devices were tested for spectral sensitivity and dark current at 77°K. A typical relative spectral response curve is shown in Fig. 5. The peak at 0.9 μm is caused by absorption of light in the silicon substrate and collection of the minority-carrier photoelectrons

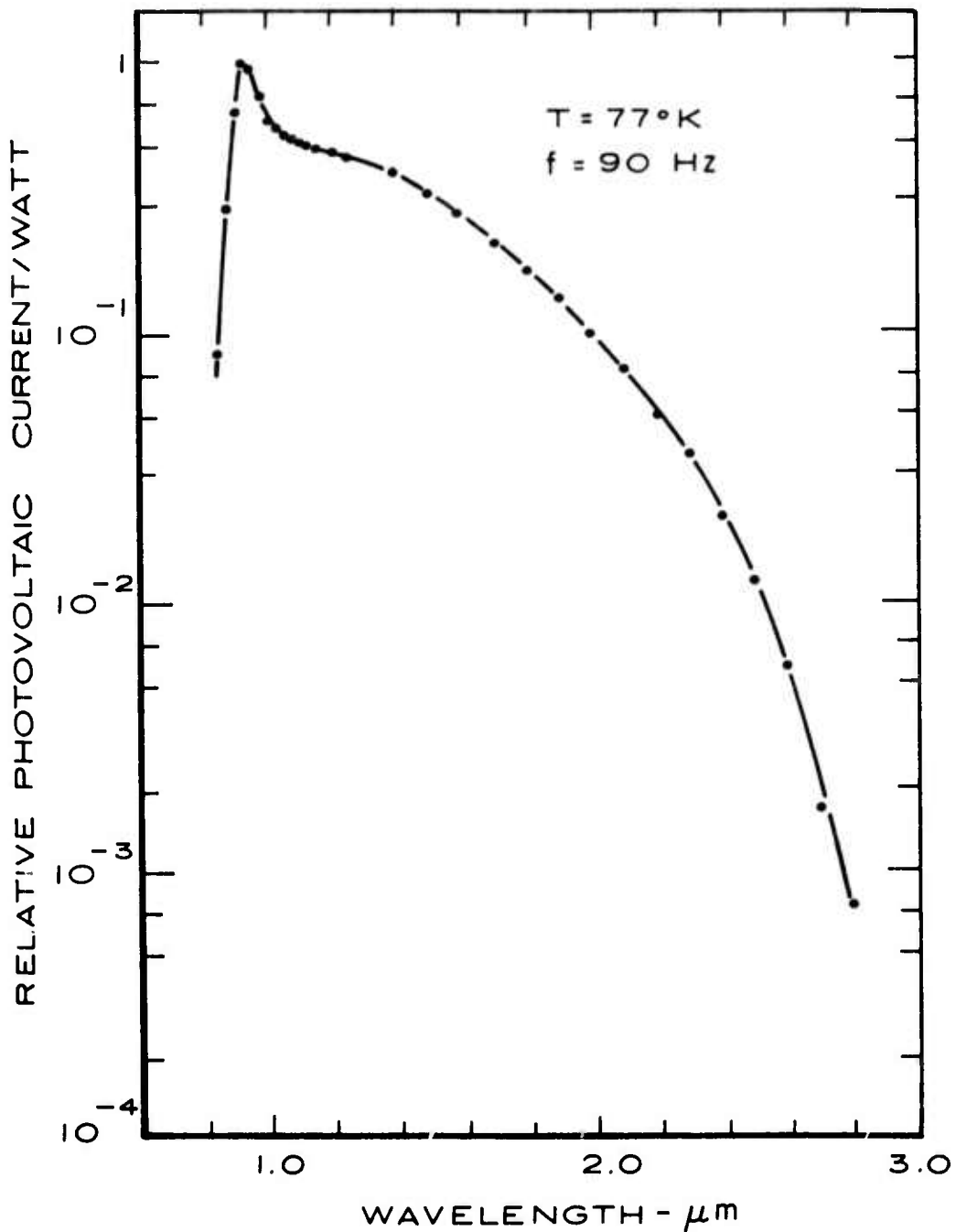


Figure 5. Relative spectral response of Schottky-barrier detector. The material was palladium-silicide on p-type silicon at 77°K. The data are uncorrected for the Pyrex dewar.

by the barrier. The response beyond $1.1 \mu\text{m}$ is clearly due to absorption in the metal film and photoemission of holes from the metal to the silicon. Its quantum efficiency is down from that of the peak silicon by a factor of 2 near the silicon band edge to 10^3 at $2.8 \mu\text{m}$. The best quantum efficiency seen here for the barrier in the IR mode is about 1%.

C. SHIFT-REGISTER DESIGN AND MASK LAYOUT

Charge-coupled semiconductor devices [1] consist of closely spaced MOS capacitors pulsed into deep depletion by the clock phase voltages. For times much shorter than that required to form an inversion layer of minority carriers by thermal generation, potential wells will be formed at the silicon surface. The minority-carrier charge representing the information will be stored or confined in these potential wells. The propagation of the information is accomplished by clock pulses applied to the electrodes of the successive MOS capacitors (i.e., charge-coupled elements), which results in a motion, or spilling, of charges from the potential wells that are becoming shallower to the potential wells that are becoming deeper. Such propagation of signal into the successive minima of the surface potential produces a shift-register for analog signals having signal transfer efficiency approaching unity. The simplest structure that accomplishes this is shown in Fig. 6(a).

If the charge-coupled structures are formed with symmetrical potential wells, at least three clock phases are required to determine the directionality of the signal flow. One interesting feature of the three-phase system is that it may be used for a bidirectional charge-coupled channel in which the flow of information may be reversed by reversing the timing of the two phase clocks.

Two-phase operation is also possible but it requires the charge-coupled structures to be formed so that the potential wells induced by the phase voltage pulses are deeper in the direction of the signal flow. In this case, as one phase voltage is lowered, the resulting potential barriers force a unidirectional signal flow. This can be accomplished with the structure shown in Fig. 6(b), if adjacent pairs of aluminum and polysilicon electrodes are connected together and alternate pairs are connected to the two clock phases. The signal charges reside under the polysilicon gates where the oxide is

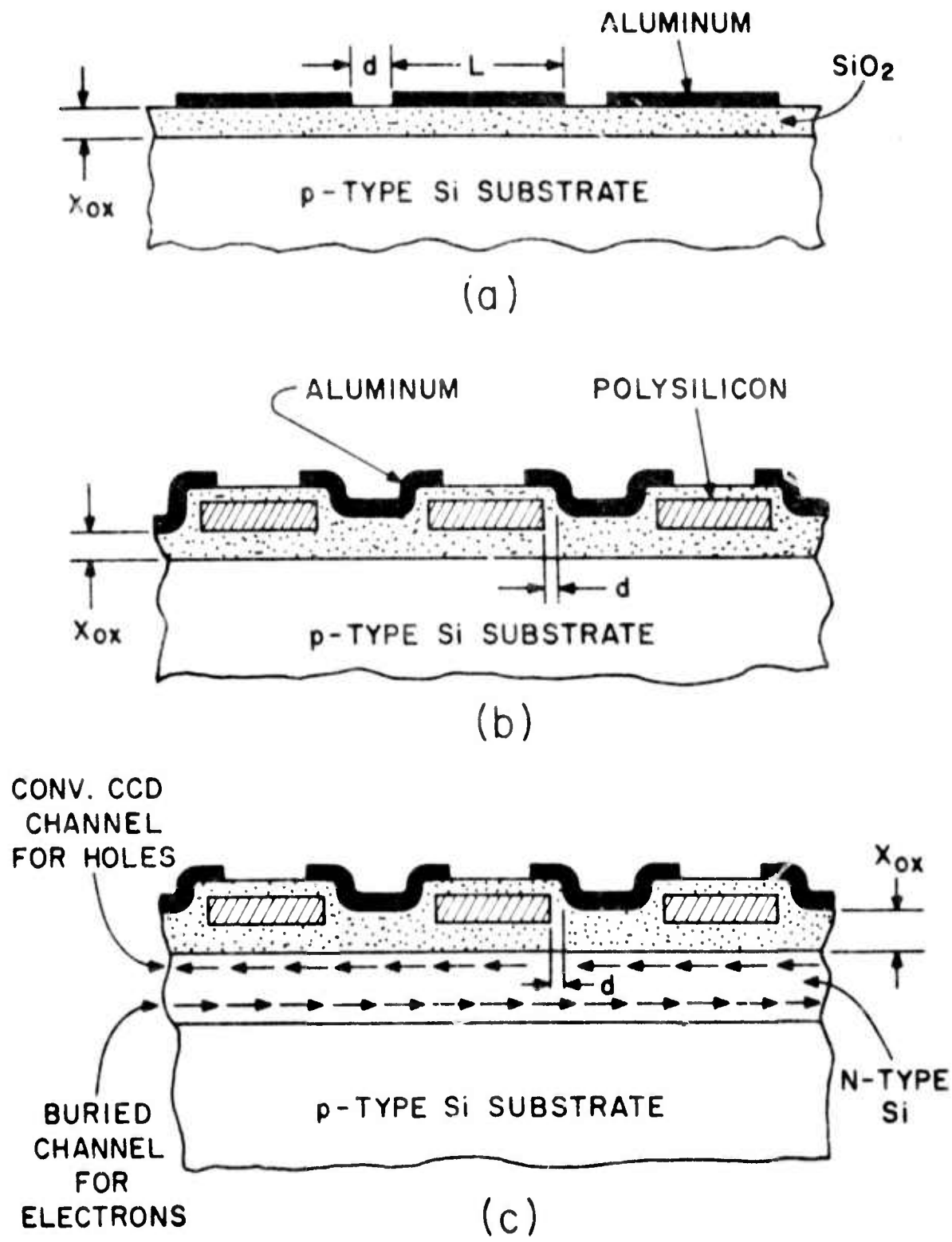


Figure 6. Three types of charge-couple structures: (a) single-metal CCDs, (b) sealed-channel CCDs in the form of polysilicon gates overlapped by aluminum gates, and (c) buried-channel CCDs.

thinner and the potential well deeper, and transfer upon clocking to the adjacent pair. It is possible to operate this device with a single clock phase if a proper dc voltage is applied to one of the phases.

In CCD operation the signal charge must be confined to a narrow potential well called the channel. This channel should provide a deep, abrupt potential well that changes surface potential in response to the clock pulse voltages. The region outside the channel should be insensitive to clock voltage changes and should be in accumulation.

Three general methods for channel confinement have been investigated at RCA Laboratories: (1) two thicknesses of oxide or thick field oxide, (2) guard ring diffusion or "channel stops," and (3) electrostatic guard rings in the form of polysilicon layers.

The two-oxide method operates by creating a deeper potential well under the thin oxide than under the thick oxide. It works best on low-resistivity substrates. A problem that occurs sometimes, however, involves metal continuity over the oxide step.

Our choice for channel confinement for CCDs was diffused channel stops. This approach is applicable to high-resistivity substrates and also provides for the simplest processing for large-area CCDs. Ideally, the diffused channel stops should be very abrupt and relatively low doped (10^{17} to $10^{18}/\text{cm}^3$).

The important difference between the first two methods of channel confinement and the polysilicon electrostatic guard rings, also referred to as polysilicon field shield, is that in the latter case the surface potential at the channel stop can be determined by an externally controlled potential. Thus, the regions between the CCD channels can be accumulated or held at any other surface potential. This capability may be useful in the operation of the CCD but at the cost of greater fabrication complexity.

The following three charge-coupled structures are available for the construction of CCD arrays: (1) single metal CCDs, (2) sealed-channel two-phase or multi-phase CCDs, and (3) buried-channel CCDs. The cross-sectional views for these three charge-coupled structures are illustrated in Fig. 6. The comparative merits and trade-offs of the three above-mentioned charge-coupled structures are discussed below.

Single-metal-layer three-phase charge-coupled devices made in a p-MOS or an n-MOS process require the minimum number of processing steps. The most

conventional process and the one used to make the first charge-coupled circuits at RCA is the thick-oxide p-MOS process. The major limitation of this process is the etching of the separation between the gates; it should be no larger than about 2.0 μm to control the surface potential in the resulting gap in the channel oxide. The operation of n-MOS CCDs, on the other hand, can be less sensitive to the interelectrode spacings because of the presence of positive charge in the channel oxide. CCDs in the form of n-channel structures using single metallization, diffusion guard rings for the channel confinement, and only a *single thickness of oxide* are the simplest to fabricate. We therefore adopted this approach.

The sealed-channel polysilicon-aluminum structures developed at RCA Laboratories [12] and shown in Fig. 6(b) are the most compact structures that can be fabricated with more or less conventional layout rules. The self-aligning-gate construction of these devices allows fabrication of charge-coupled structures with gate separation comparable to the thickness of the channel oxides as well as having the channel oxide always covered by one of the metallizations. Another important advantage of the silicon-gate process is that it provides a very simple method for the construction of two-phase CCDs. Charge transfer efficiencies of 99.99% per stage have been obtained in the operation of such p-channel two-phase CCDs operating at clock rates up to 2 MHz. This we believe is the highest charge transfer efficiency reported thus far in the operation of surface channel CCD structures. We chose not to use this method at this time because our 64×1 array did not need the extra bit of transfer efficiency to warrant the additional complexity of fabrication.

The buried-channel CCD [13] represents a charge-coupled structure in which the potential minimum for the charge signal is located inside the silicon substrate about 0.5 to 1.0 μm below the SiO_2 -Si interface. The buried channel structure is illustrated in Fig. 6(c). The completely depleted n-type layer forms a parabolic potential variation which, for a wide range of gate voltages, results in a potential minimum for electrons near the center of the buried-channel layer. This layer is initially depleted and is maintained in depletion by charge transfer action. Since the carriers are a distance from the surface,

12. W. F. Kosonocky and J. E. Carnes, *Two-Phase Charge-Coupled Devices*, Final Report, Contract No. NAS1-10983, Feb. 1972.

13. R. H. Walden et al., *Bell System Tech. J.* 51, 1635 (1972).

they avoid surface state trapping, and thus the bias charge (or fat zero) required for efficient surface channel operation is not required here. However, this is not an advantage for thermal imaging where a large background is present anyway. Again, the advantage for us, if any, does not warrant the complexity.

With the choice of a single-level metallization type structure and diffused channel confinement, the fabrication procedure is as follows. A $10^{15}/\text{cm}^3$ doped (100) silicon wafer is subjected to a p-type diffusion and an n-type diffusion, each defined by a thermal oxide left after a photolithographic step. The gate oxide is grown, and contact holes are opened. Palladium is then evaporated onto the wafer in a vacuum system that received special care to avoid sodium contamination. Any sodium would get into the oxide in ionic form and cause the device characteristics to drift. While the palladium is being evaporated, the wafer is heated, causing a palladium silicide to be formed in a chemical reaction. The wafer is then removed from the evaporator, and the remaining metallic palladium is etched off. It is returned to the vacuum system, where it receives a thin evaporated film of titanium followed by a film of aluminum. The titanium layer is required because aluminum can react with palladium silicide. The aluminum is defined photolithographically with an etch that stops at the titanium. The titanium is then etched down to the gate oxide with an etch that does not attack aluminum. A protective SiO_2 layer is next deposited over everything, and holes are opened for the bonding connections. The wafers are scribed and diced, and the chips are mounted with epoxy in integrated-circuit holders with holes cut to permit rear illumination. The final step is to bond leads from the bonding pads on the chips to the holder. A summary of the fabrication procedure and mask levels is shown in Table 1. If this were a visible-sensing CCD, it would be necessary to thin the chips to permit rear illumination. Fortunately, this step is not necessary for us since silicon is transparent to infrared light beyond $1.1 \mu\text{m}$.

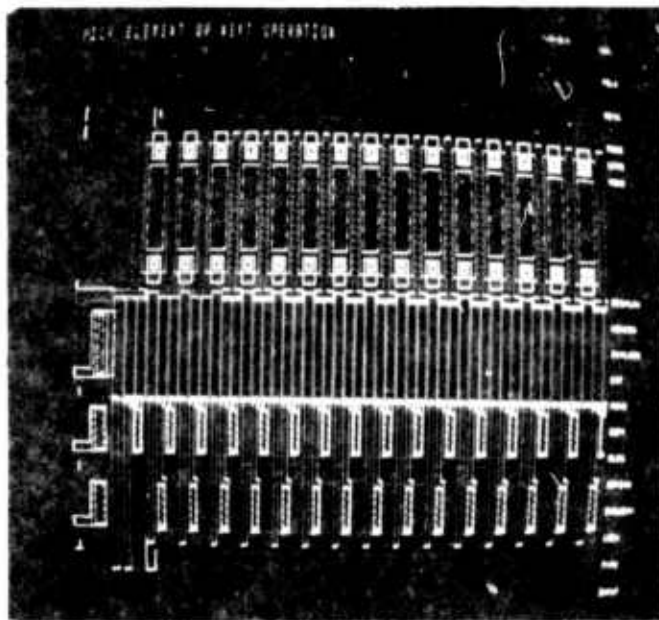
Our design is a 64×1 linear CCD with gates 0.52 mil long in the direction of charge transfer and 0.08-mil gaps. The repetition length is thus 1.8 mils per bit, and the channel is 5.0 mils wide. The Schottky-barrier contact holes are rectangles 5.0 mils by 0.9 mil and are spaced on 1.8-mil centers along the CCD register so that each detector can load into a phase-1 CCD gate when the transfer gate is clocked. There is a source diffusion with loading gates at one end of the shift register and a resettable floating diffusion connected

Table 1. Procedural Steps in Fabrication of Schottky-barrier Infrared CCDs

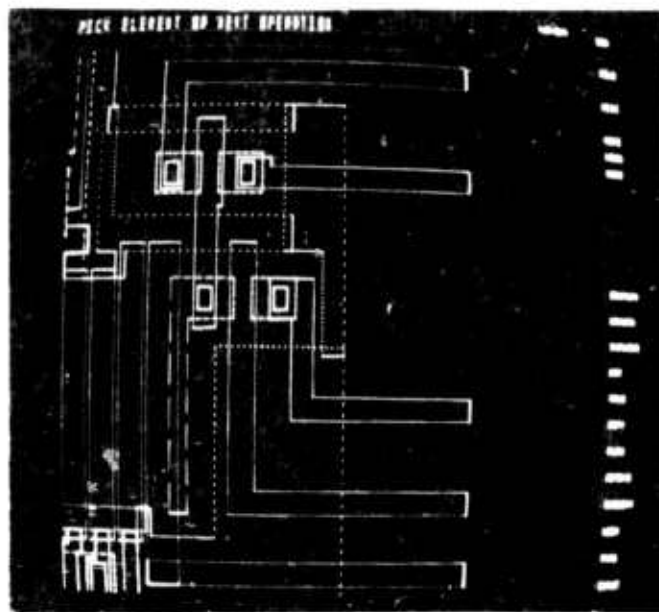
<u>Operation Performed by</u>	<u>Fabrication Steps</u>
INTEGRATED-CIRCUIT TECHNOLOGY CENTER, David Sarnoff Research Center, Princeton, NJ	1. Diffuse channel stop (Mask 1)
	2. Diffuse source and drain (Mask 2)
	3. Etch contact holes (Mask 3)
METALLIZATION LABORATORY, Solid-State Technology Center, Somerville, NJ	4. Clean wafer
	5. Evaporate and drive in palladium
	6. Remove excess palladium
	7. Evaporate titanium and aluminum
INTEGRATED-CIRCUIT TECHNOLOGY CENTER, David Sarnoff Research Center, Princeton, NJ	8. Etch pattern in aluminum (Mask 4)
	9. Etch titanium using aluminum as mask
	10. Deposit SiO ₂ overcoat
	11. Etch bonding holes and scribe lines in SiO ₂ (Mask 5)
	12. Scribe and cleave wafer
	13. Mount chip in package and bond leads

to an on-chip MOS transistor at the other end. Numerous other devices are on the chip, including alignment marks, photolab marks, level numbers, devices for measuring metal resistivity, diffusion resistivity, diffusion lateral spread, channel stop threshold, MOSFET characteristics, etc.

The masks were drawn, programmed, and punched on computer cards, and examined on a computer-generated CRT display. There, dimensions could be checked and programming errors could be easily spotted. Photographs of the CRT display are shown in Fig. 7. Several mask levels are shown superimposed with different kinds of lines to represent the different mask levels. It was possible to zoom in to measure coordinates, and to change the sections and levels displayed very quickly. When we were satisfied that no errors remained, the punched-card program was converted to a tape, and a large flat-bed ink-plot was generated from the tape with a different color for each mask level. We scrutinized this plot for errors and proceeded to order masks to be generated from the computer tape.



(a)



(b)

Figure 7. Computer-generated CRT displays of sections of the chip. Four of the mask levels are shown as different kinds of lines. (a) The beginning of the CCD array. The Schottky barriers can be seen along the top row. The shift register is the center row. (b) A close-up view of the CCD output stages. The top device is the MOS output transistor. The similar device in the center is the floating diffusion with its reset gate and drain.

D. DEVICE FABRICATION

The device fabrication procedure was given in Table 1. Figure 8 shows photomicrographs of the two ends of a completed device on a wafer containing about 50 chips. The vertical white rectangles in a row along the top are the Schottky-barrier metallizations, each overlapping the contact holes to the substrate and to the setting and transfer diffusions. The charging gate (27) and the transfer gate (28) control the channels to the charging bus (contacted by 24) and the phase-1 gates (7), respectively. The bonding pad for the phase-1 busbar (7) cannot be seen because it is near the center of the CCD. Phases 2 (3 and 9) and 3 (2 and 10) are double-end connected because they require a diffused crossunder which is more resistive than a metallization. Two separate gates are provided at the beginning (5 and 6) of the shift register and at the end (12 and 13). A source diffusion (contacted by 1) is provided to permit electrical input to the shift register while a floating diffusion with a reset gate (14) and drain (15) is provided at the output. The floating diffusion is connected to an on-chip MOS transistor whose source and drain diffusions are brought out to pads 16 and 19. Contact to the substrate is made at pads 20 and 23, each of which contacts a channel-stop diffusion.

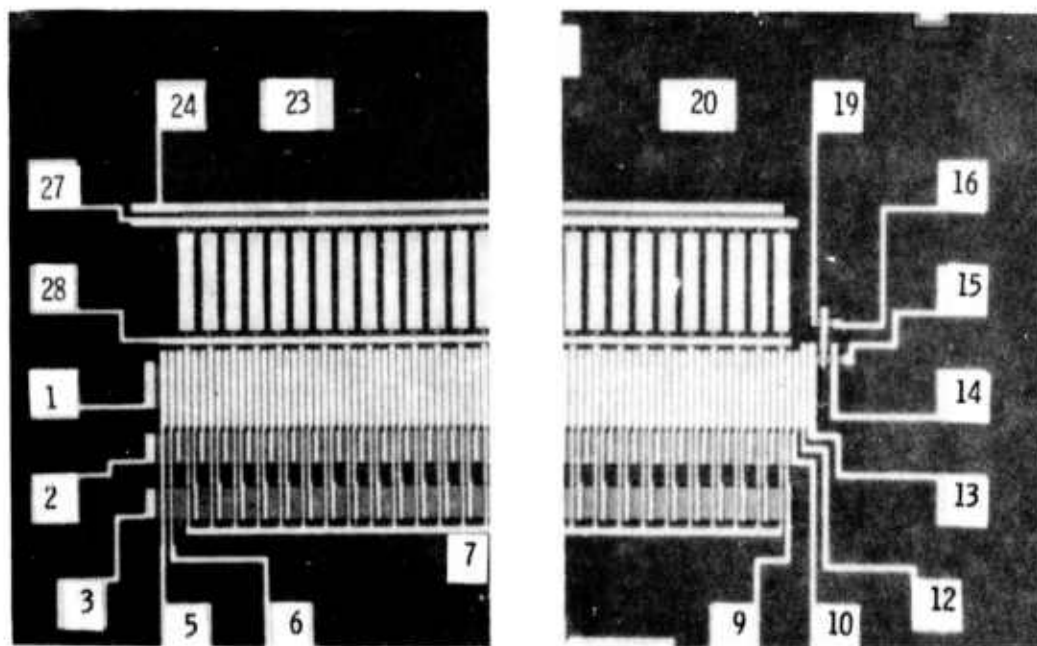


Figure 8. Photomicrographs of the two ends of the CCD chip.

The output stage is seen more clearly in the enlargement in Fig. 9. The "L"-shaped floating diffusion is seen to be connected through a contact hole to the gate of the MOS transistor. It is overlapped by the reset gate (14) which controls the channel to the drain (15). The channel stop diffusion surrounding these elements could be seen under the microscope but does not show well in this photograph.

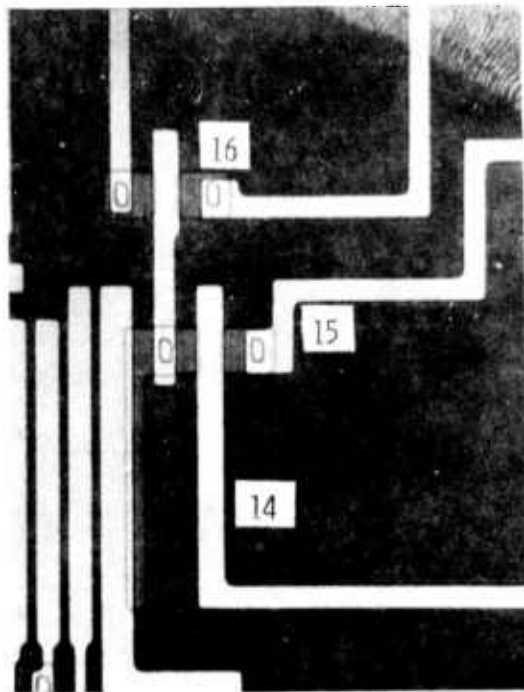
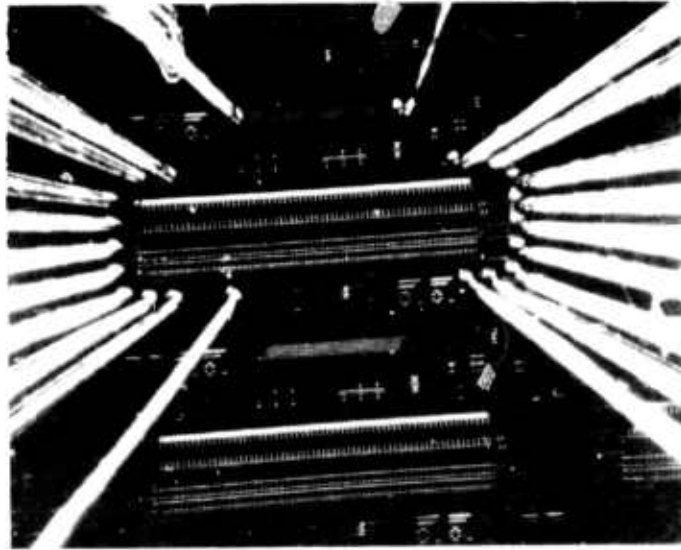
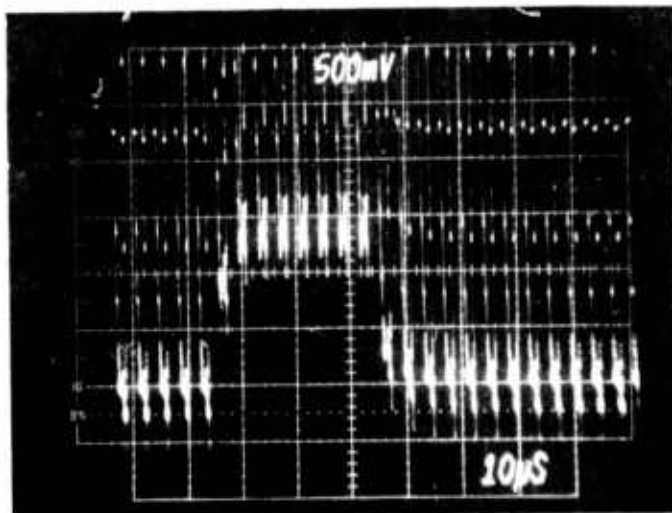


Figure 9. Output section of the CCD chip showing the L shaped floating diffusion, the MOS transistor (16), the reset gate (14), and the drain (15).

A probe card was made to order for testing the chips before the wafer was diced. Figure 10(a) shows a circuit being tested in the probe-card station as seen through the low-power binocular microscope on the station. Several chips were tested for open-circuits, short-circuits, and diode characteristics. When all of these tests proved satisfactory, it was decided to operate the chips as CCD shift registers with electrical input directly on the probe-card station and to select chips on the basis of CCD performance. About three-fourths of the chips with no obvious visible defects operated well as shift



(a)



(b)

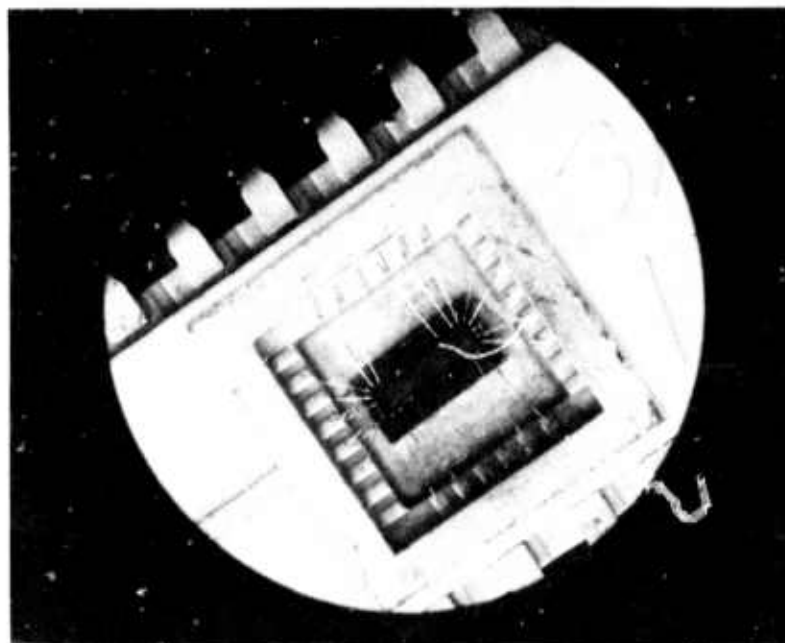
Figure 10. (a) Photomicrograph of the probe-card station showing one circuit on a wafer being tested. (b) Output signal from a chip operated on the probe-card station with an 8-bit input.

registers. The output signal from a typical good chip with an electrical input of eight "1's" is shown in Fig. 10(b). It consists of eight "1's" with the leading "1" degraded by one-third, all delayed by 64 clock periods from the input. The details of this electrical test are discussed later. While the clock noise pattern was particularly complicated because of crosstalk from the several unshielded leads carrying clock waveforms, it was nevertheless possible to sort out the chips on the wafers and mark the bad ones on the basis of this test. Since most of the shift registers on the wafers made with Pd worked as well as the devices on wafers made with aluminum only, nothing more was done with the Al-only control wafers. Al-only control wafers were not deemed necessary in subsequent runs.

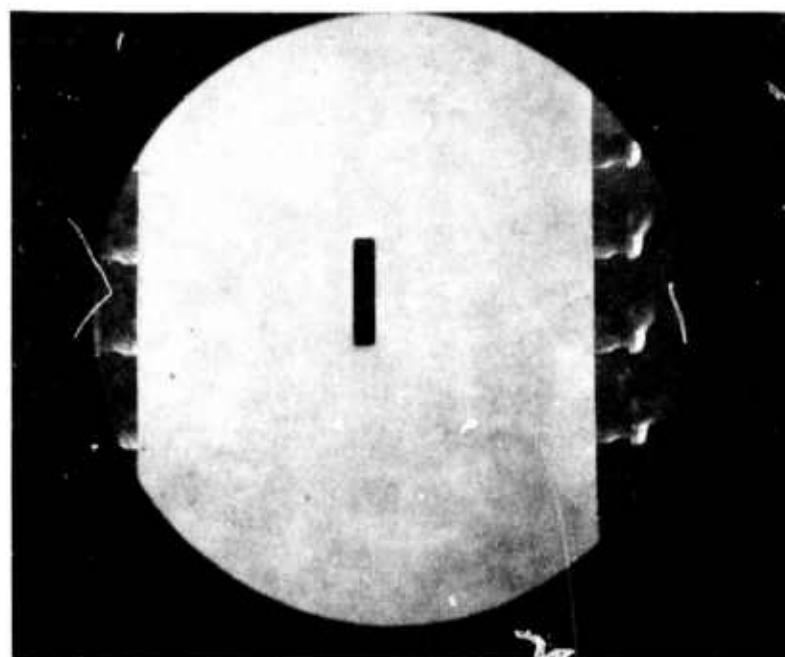
A 28-pin gold-plated, ceramic dual-in-line holder was selected for the chips. After the wafers were scribed and diced, tested chips were mounted and bonded to the holders which had been previously prepared with 0.120-in. by 0.030-in. rectangular holes ultrasonically ground in the centers of the 0.200-in.-square chip mounting areas. These holes are required for rear illumination with infrared light. A bonded chip is shown in Fig. 11(a); the back of the package is shown in Fig. 11(b) with the same magnification. To affix the chip with the detector array directly over the hole, we viewed the chip from the top, as in Fig. 11(a), with a low-power microscope equipped with an infrared image converter in place of the eyepiece. The image converter has an S-1 photocathode that is sensitive to light transmitted by silicon. With illumination from below the holder, we could see the bright rectangular hole in the ceramic masked by the aluminum metallization pattern of the device. All bonded chips were positioned in this manner.

E. OPERATION OF THE CCD WITH ELECTRICAL INPUT

A circuit diagram of the IR-CCD chip is shown in Fig. 12. The extra gates, G_2 and G_3 , were included to make possible other input and output schemes, and are connected in sequence with the three phases, while G_4 receives a small positive bias, and the reset gate is pulsed. The substrate is biased negatively by a few volts so that the gates always keep the surface inverted. For operation with electrical input, the transfer gate receives a negative bias, isolating the shift register from the detectors. The three-phase, overlapping clock



(a)



(b)

Figure 11. (a) Photograph of a bonded chip.
(b) Rear view of holder.

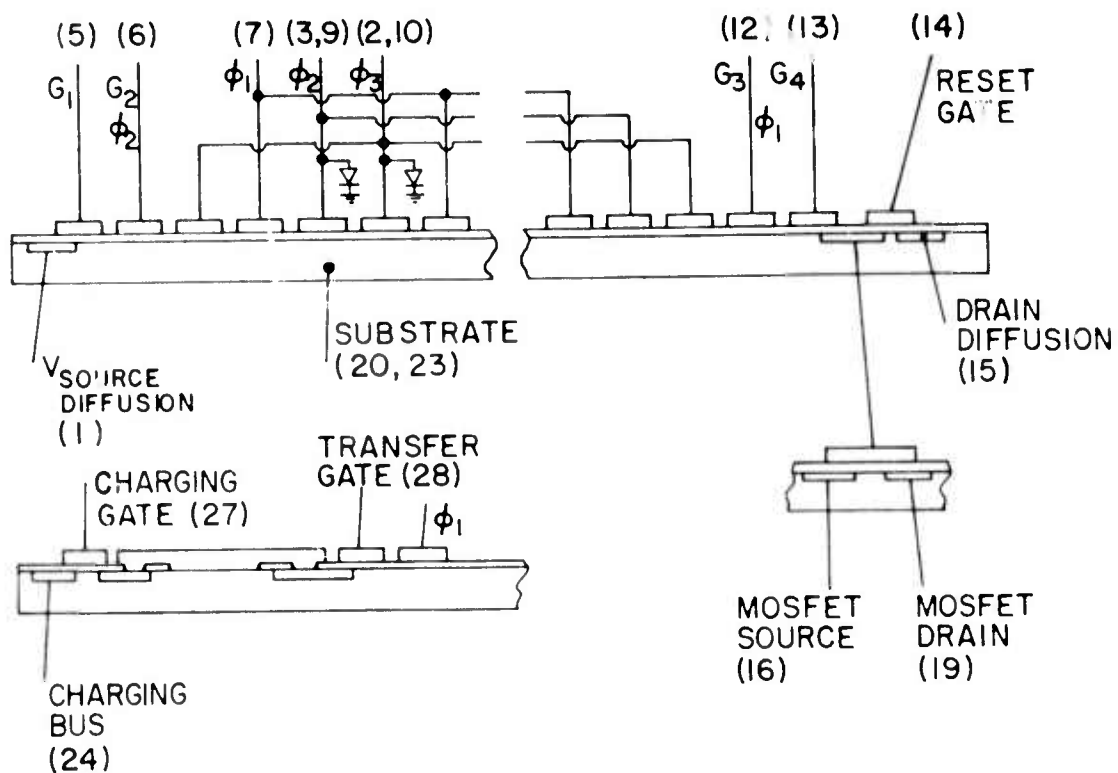


Figure 12. Circuit diagram of the IR-CCD chip.

waveforms run continuously. A word generator circuit runs in synchronism with the clocks and produces a settable number of positive pulses (such as 4) each time it counts a settable number of clock pulses (such as 128). The word is applied to G_1 and is expected at the output 64 clock periods later. Figure 13 shows such an output word with 1/10 of the leading pulse missing. Since there were 192 transfers (64×3), the average transfer loss was about 5×10^{-4} per transfer. To get this fairly good transfer efficiency with a surface channel CCD, it is necessary to introduce a bias level or "fat zero." For our chip running at 250 kHz, the optimum bias level was experimentally determined to be $0.3 \mu\text{A}$. The output signal is taken from the MOS transistor whose gate follows the potential of the floating diffusion. The MOS transistor can be wired as a source-follower or as a common-source amplifier, depending on which polarity of output signal is desired.

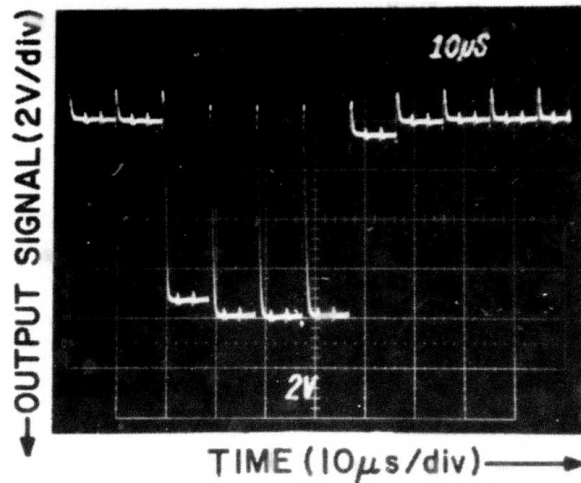


Figure 13. Output word for an 4-bit electrical input.

F. VISIBLE LIGHT IMAGING

Visible light (using the term to mean light absorbed by silicon as opposed to longer wavelength infrared) can be detected and imaged directly by the CCD shift register. The image can be incident on the top of the wafer through the gaps between the electrodes or on the back of the wafer. In the latter case, the wafer should be thinned or few of the minority carriers created by the light will be collected in the CCD wells. Our chips were not thinned since we were not concerned with detection of visible light.

In either case, image detection by the shift register requires one or two of the phases to be held on for a period of time while the other(s) are held off. This "integration time" should be much longer than the time required to read out the line after the clock waveforms begin running again to avoid smear. In our case the latter time is 64 (the number of bits) $\div 1/4 \times 10^6 \text{ s}^{-1}$ (the clock rate), or about $1/4 \text{ ms}$. Thus, for integration times more than a few milliseconds, there should be no smear. The bias level required for good transfer efficiency can be introduced by weak uniform illumination of the shift register or by an electrical input pulsed off during the integration time. The former is generally more convenient for optical measurements. Figure 14(a) shows the output signal corresponding to a small light spot imaged

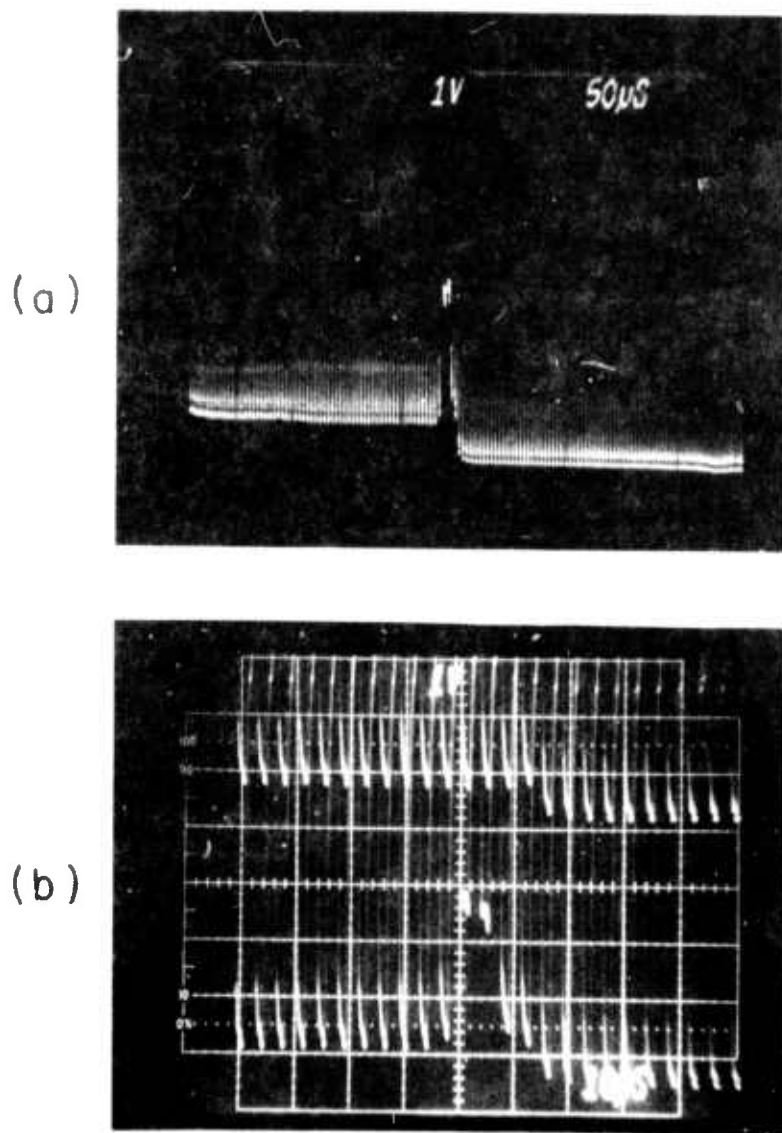


Figure 14. (a) Video signal for a spot of visible light shining on the beginning of the shift register. (b) Expanded view of the video signal without the light spot (top) and with the light spot (bottom).

through a microscope onto the beginning of the shift register. The spot illuminated about two bits, and little spreading of the signal can be seen even though the signal was transferred through the entire shift register to reach the output. The bottom trace in Fig. 14(b) is a magnified view of the output while the top trace was taken without the light spot. The weak uniform illumination can be seen in all three traces.

G. TESTING OF SCHOTTKY-BARRIER DETECTORS ON CCD CHIPS

The Schottky barriers on the IR-CCD chips were tested for dark current. Since the chips had no provision for direct connection to the detector metallizations, the circuit in Fig. 15 was used for the dark-current measurement. The transfer gate was tied to a negative voltage to isolate the detectors from the shift register while the setting gate was tied to a positive voltage to connect the setting diffusion to all the detectors at once. Data for three typical samples at 77°K are shown in Fig. 16. At room temperature, the reverse currents were many orders of magnitude higher, as expected. While most of the samples tested within the range shown in the illustration, a few had much higher dark current. It was not possible to tell from *this* test whether a few or all the detectors were contributing to the higher dark current.

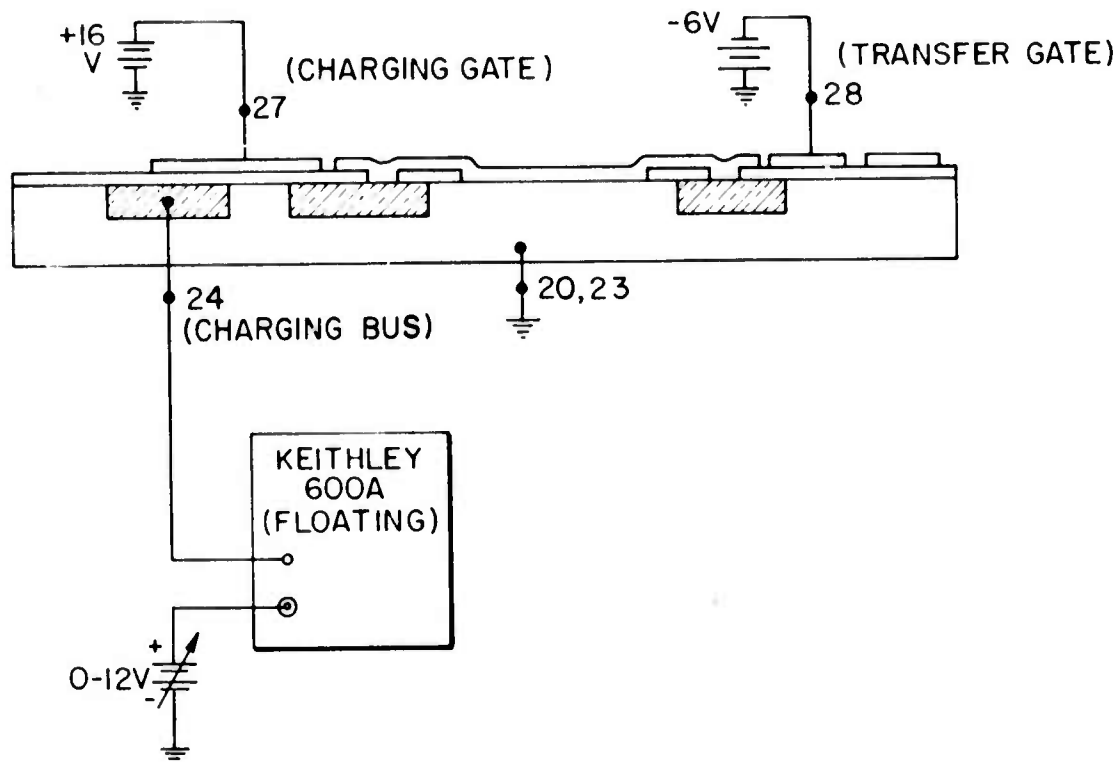


Figure 15. Circuit for measuring Schottky-barrier dark current.

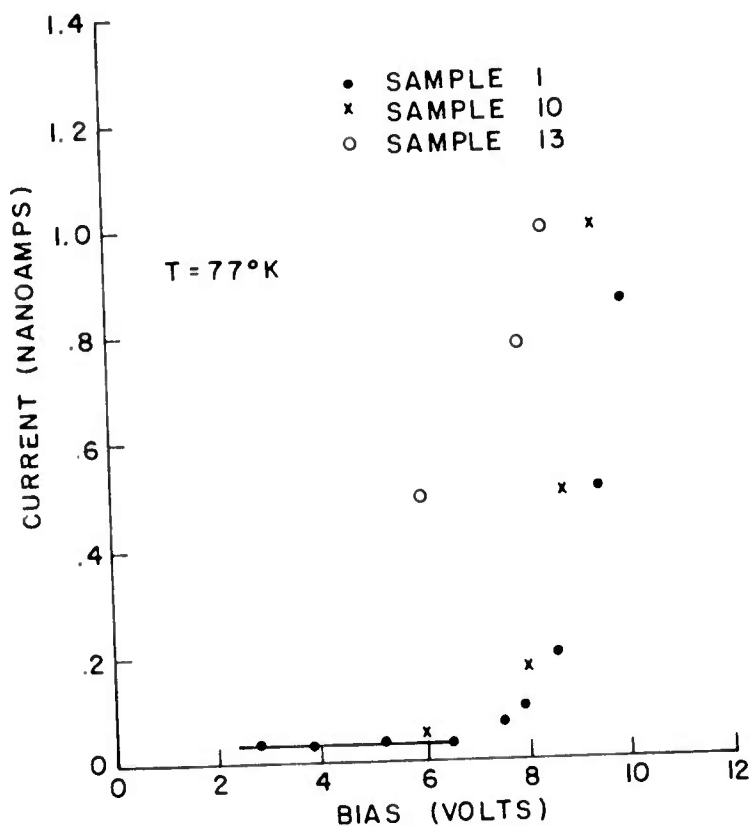


Figure 16. Dark-current characteristics of the three CCD samples.

It is apparent from Fig. 15 that an MOS transistor is formed by the setting diffusion, the setting gate, and the diffusion contacting each detector. These elements correspond to the drain, the gate, and the source, respectively. While a connection to the contacting diffusions is not available, at room temperature the detectors are essentially short-circuits. Thus, these elements can be tested as an MOS transistor with the source connected to the substrate. The collector characteristics are shown in Fig. 17, showing a transconductance of $650 \mu\text{mhos}$.

H. DETECTION OF INFRARED IMAGES IN THE VIDICON MODE

For infrared imaging, the IR-CCD chip must be operated at reduced temperature and illuminated through the back of the substrate. A special socket, with a hole to permit viewing of the window in the chip holder, was wired and

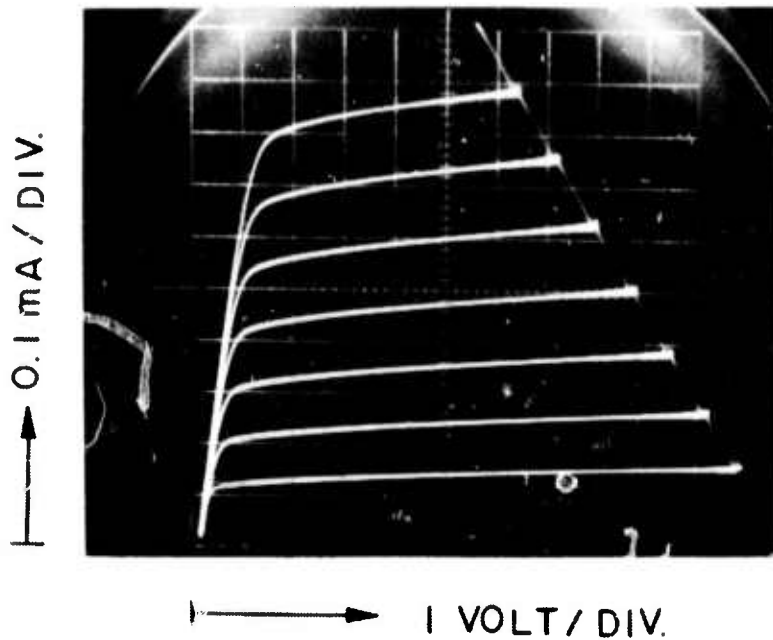


Figure 17. I-V characteristics of setting circuit of IR-CCD chip run as an MOS transistor. The bias is 0.2 V/step; the transconductance (g_m) is 650 μ hos. The largest trace is for zero bias.

mounted at the end of a plastic rod so that it could be positioned in a quartz optical dewar containing liquid nitrogen. A weak tungsten lamp illuminated an adjustable slit that was imaged on the IR-CCD chip with a special germanium lens. The lens also served to block any light whose wavelength was less than 1.7 μ m. A polished germanium wafer, 0.010 in. thick, was tested on a spectrophotometer to confirm the above cutoff wavelength and was used to block light that could be absorbed by silicon. A diagram of the optical path is shown in Fig. 18.

The auxiliary pulse requirements for infrared imaging were discussed above. The setting pulse is required only in the low-contrast mode. In the vidicon mode, the Schottky barriers are set to the required reverse bias when the transfer pulse is applied and the signal loaded into the wells of the shift register. The voltage to which the Schottky barriers are set is determined by the height of the transfer pulse so long as the shift register well not filled. Since the barriers are set to the same potential after each frame, the charge removed, and thus, the signal in the CCD well, is just the amount by which the

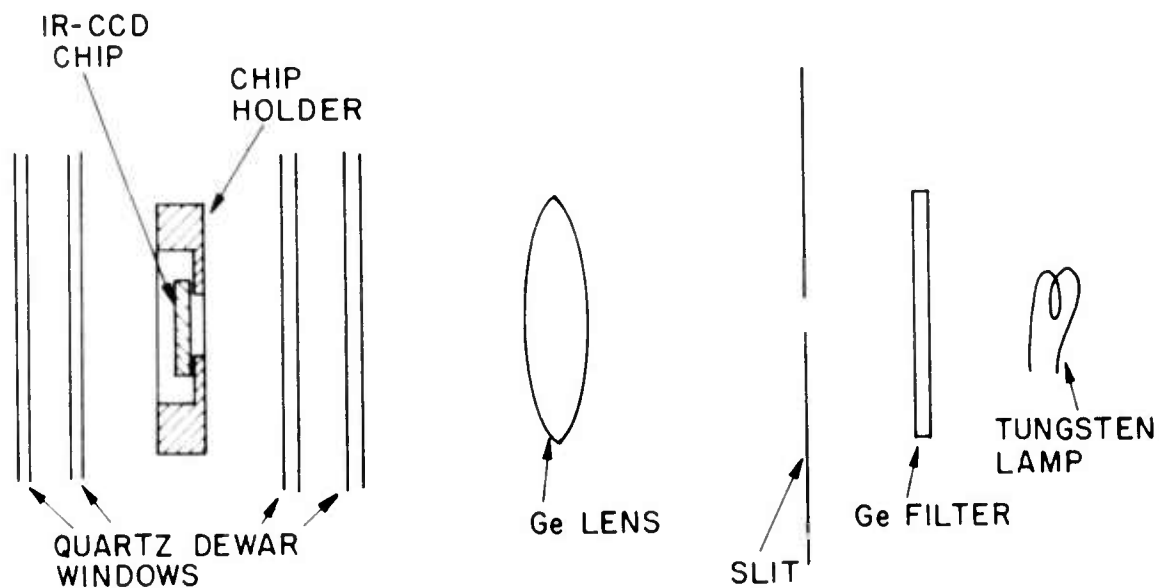


Figure 18. IR optical path.

Schottky barrier was discharged by photoemission and by dark-current mechanisms during the time period between transfer pulses. Hence, this time is the integration time for infrared detection. The shift register runs continuously during the integration time, with the first 64 bits after the transfer pulse ends comprising the video signal; only during the transfer pulse does the shift register not run. Hence, the transfer pulse width is the integration time for shift register light detection. Any doubt whether the video signal was caused by absorption at the shift register or absorption at the Schottky barriers can be resolved by varying the two integration times, one at a time, and observing which affected the signal in question. The video signal corresponding to uniform infrared illumination (filtered by the germanium wafer) is shown as the second trace in Fig. 19. The top trace is without the illumination. The transfer pulse was only 1.5 V because the dark current rose quickly with Schottky-barrier voltage in this sample. For some samples, it was possible to set the transfer pulse as high as 15 V before running into excessive dark current. The ability to use high transfer pulses is desirable since it corresponds to high signal-handling capacity. Figure 20 shows the video signal for imaging with a narrow slit and a wide slit in different locations. The signal with the narrow slit was 2 bits. Making the slit still smaller did not improve

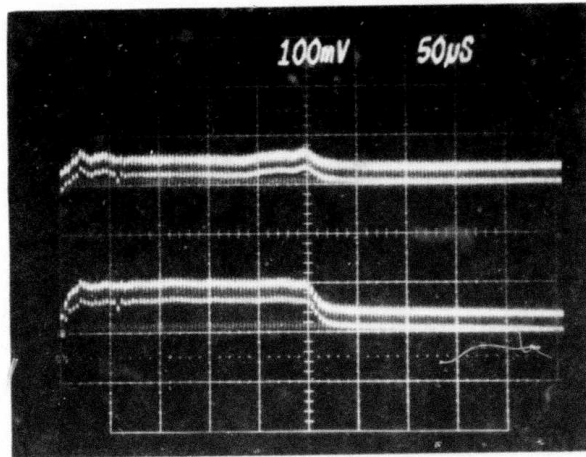


Figure 19. Video signal with uniform infrared illumination; top - without illumination, bottom - with illumination.

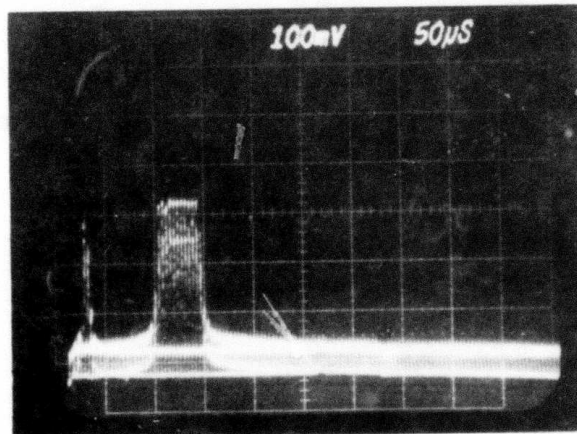


Figure 20. Video signal for infrared imaging with a narrow slit and a wide slit. The first trace was taken with the slit smaller than 0.1 mm; the second trace was taken with the slit repositioned and set to 1.0 mm.

the resolution beyond this. The limitation was probably in the focussing as the shift register had sufficiently good transfer efficiency to deliver a single recognizable bit. For this chip, a transfer pulse as high as 15 V could be used. The optical system was focussed using the video signal of a narrow slit. The slit could then be moved laterally to scan the signal across the oscilloscope screen. A photograph of the video signals with the narrow slit in four positions is shown in Fig. 21. A soldering iron tip, invisible to the human eye, easily saturated the video signal. A hotplate at 110°C could be detected with a 30-ms integration time.

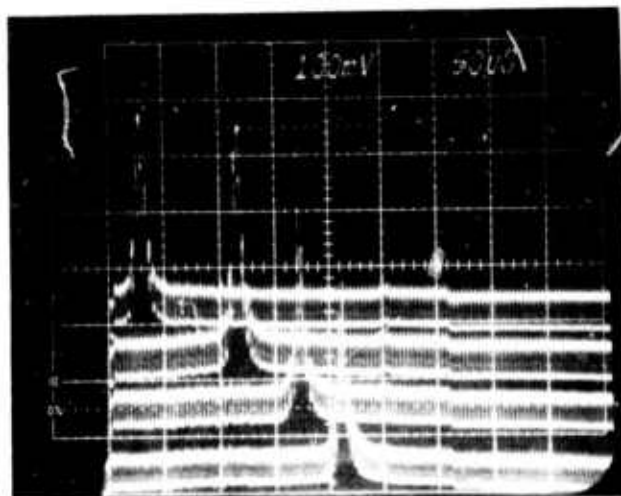


Figure 21. Video signal corresponding to a narrow slit in four positions.

It should be noted that, unlike visible charge-coupled imagers, this IR-CCD is immune to smear and blooming. Smear occurs when imaging is performed by the shift register, and an unusually bright spot creates a significant number of carriers in a shift-register well during the short time between two consecutive clock pulses. Since our chip will not be allowed to image at the shift register, this smear mechanism does not apply. This is true of all CCD's of the "interline" type. Blooming occurs when a bright spot causes a well to become overfilled with minority carriers which then transfer to adjacent wells. Again this is not possible at our shift register because we do not permit imaging there. A charge-coupled imager with separate p-n junction detectors or photogate detectors could conceivably bloom but

Schottky barriers are majority-carrier devices. No minority carriers are even generated, so there is no blooming mechanism.

I. DEVICE UNIFORMITY

Although Schottky-barrier detectors offer the advantage of uniformity good enough for thermal imaging, this advantage would be lost if nonuniformities were introduced by the transfer process. We must, therefore, consider the consequences of the various nonuniformities likely to occur during fabrication of the charge-coupled imager. Possible nonuniformities include those associated with substrate doping, oxide thickness, oxide charge, accuracy of definition in the photolithographic process, and the effect of gap charging.

A variation in doping across the array will not have any significant effect on detector responsivity, but will result in a variation of detector capacitance. If the device is operated in the vidicon mode, with the detectors recharged by the shift-register wells, small differences in detector capacitances should not show up in the video signal. Of course, if dark current due to edge effects were a factor, doping variation would result in dark-current variation. Variations in oxide thickness or oxide charge would cause variation of the surface potential under the transfer gate and, thus, would result in a variation of the level to which the detectors are set. Still, in the vidicon mode of operation, each detector is reset to its same potential at the end of each frame. The charge removed is independent of the capacitance and of the transfer level so long as the detectors are not discharged to zero. Thus, in the vidicon mode, the transfer process should not introduce any additional nonuniformities. The uniformity with which the contact holes can be defined and etched will clearly affect the uniformity of response. However, work at Air Force Cambridge Research Laboratories suggests that this will not be a problem [8].

In charge-coupled devices with gaps between metal electrodes, the exposed oxide in the gaps can become charged, causing the transfer efficiency to deteriorate. Device performance is then degraded because of the many transfer losses cascaded. We would not expect this to be a likely source of nonuniformity in the transfer process since only one transfer is involved in getting the charge from the detectors to the wells, while 200 transfers under gaps

take place in the shift register. A negative charge on the oxide in the transfer gap could produce a bump in the potential profile between the transfer gate and the adjacent shift register well. This would have the effect of creating a small change in the transfer level, which we have seen does not matter in the vidicon mode, even if it were nonuniform. Serious gap charging could interfere with the transfer process, but this condition is not likely to be present in a device in which the shift register is operating well. Thus, gap-charging does not appear to be a source of nonuniformity.

The uniformity obtained experimentally in the vidicon mode is shown in Fig. 22. The video signal, measured downward, is shown for seven levels of approximately uniform, germanium-filtered, tungsten illumination. Local nonuniformities of a few percent can be seen on the signals with small illumination. Slow variations across the signal are most likely due to grading of illumination. Much larger variations can be seen at high levels of illumination, just as expected from the above discussion. The difference in uniformity between the signals corresponding to the saturated and unsaturated conditions vividly demonstrates the point being made here.

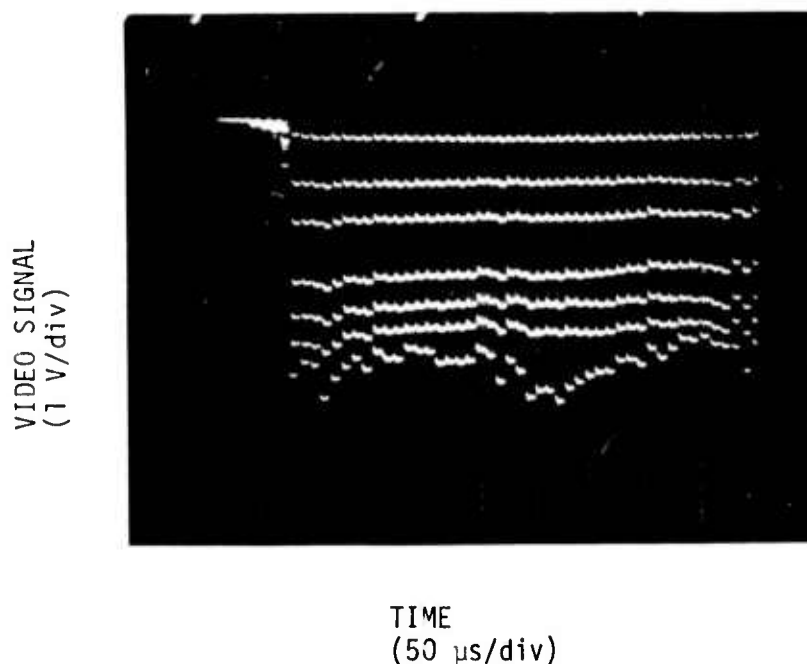


Figure 22. Response of a typical IR-CCD in the vidicon mode to several levels of approximately uniform infrared illumination.

J. OPERATION IN THE BACKGROUND-SUPPRESSION (SKIMMING) MODE

In the vidicon mode of operation all of the optical signal is necessarily transferred into the CCD for read-out because, as shown in Fig. 3(b), the surface potential under the transfer gate is used to set the Schottky-barrier potential and simultaneously remove the optical signal. In the background-suppression mode of operation, however, the initial Schottky-barrier potential is set at the beginning of the integration period by the surface potential under the charging gate or the charging bus potential, whichever is smaller. The charge, which is transferred into the CCD, is determined by the surface potential under the transfer gate which is turned on at the end of the integration period when phase-1 is high, as in Fig. 3(c). The voltage on the transfer gate is set so that just the "top" of the optical signal containing the signal modulation is skimmed off. The uniform background charge remains behind and is drained into the charging bus when the charging gate is turned on the start the next integration period. In order for the skimming technique to be beneficial, the charge storage capacity of each detector must be several times that of a shift register gate. If the shift register can hold the entire detector signal, there is no reason to have it do otherwise. Indeed the skimming mode might be expected to introduce nonuniformities in the video signal because of variations in the threshold voltages of the transfer gate and the charging gate. In the vidicon mode these differences are not observed because the same gate (the transfer gate) is used initially to set the Schottky-barrier potential and to remove the charge. Variations in detector capacitance can be expected to show up in the skimmed video signal as well, even in the absence of threshold variations. The devices were operated in the background suppression mode with scenes consisting of bright slits and a uniform background. For fixed optical input, increasing the potential applied to the charging gate did reduce the video signal, eventually removing the slit peaks as expected. However, since the storage capacity of the detectors in our device was smaller than the shift register well capacity, the true value of this technique could not be demonstrated. The operation in this mode was displayed more clearly with the charging circuit used to load charge in the dark. In these measurements, the charging bus was used to set the charging level with the charging gate used as a transmission gate. The relative magnitudes of the charging and

transfer levels were reversed compared with those in Fig. 3. That illustration shows the CCD signal being reduced through use of the charging circuit. Here, with no illumination, that circuit is being used to create a signal. The lower the charging bus potential the more charge is loaded. Figure 23 shows three different output signals using this mode of operation for three different charging bus potentials. The nonuniformities displayed here result from differences in the threshold voltages and detector capacitances, and contrast vividly with the uniformities displayed in Fig. 22 for the same device. Thus, while the skimming mode has been demonstrated, much better control of device uniformity will be required for practical use in this mode.

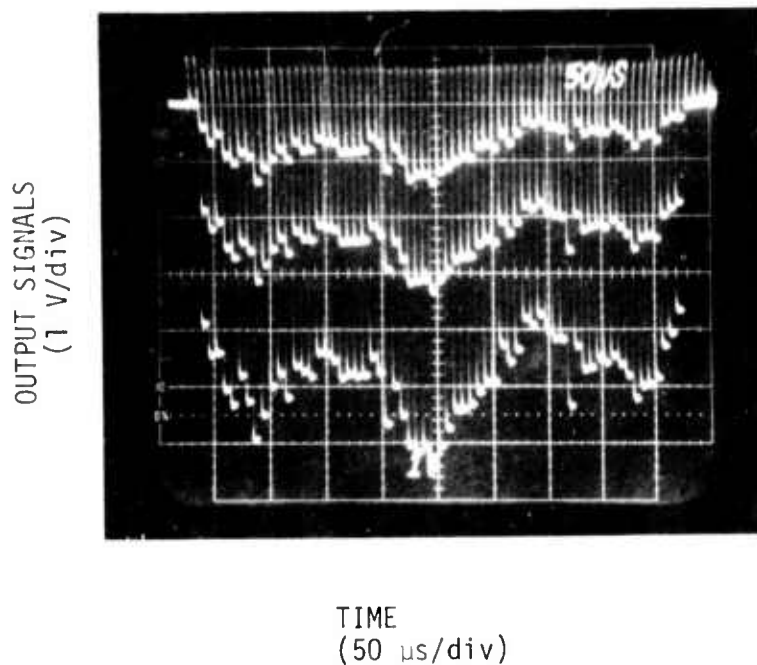


Figure 23. Output signals from shift register with charge loaded into the unilluminated detector from the setting diffusion. The largest output signal corresponds to the lowest setting potential. The transfer level was the same for all three cases. The device was the same one used for Fig. 22.

VIII. CONCLUSION

The uniformity of response observed in the vidicon mode is seen as the most important result of this work. Since variations of only a few percent were measured for devices routinely processed, still better uniformity should be obtainable with special care in mask-making and processing. Recent calculations have shown that a CCD with Schottky-barrier detectors operating in the 3- to 5- μm window in the vidicon mode is capable of resolving temperature differences better than 1°K. Thus, thermal imaging is possible even without background-subtraction, a process which, as we have seen, is *not* immune to the various nonuniformities introduced in processing. Frame comparison can be used to reduce the fixed-pattern noise, with storage accomplished with the sensor, but there is now a reasonable expectation that it will not be necessary. A quantitative evaluation of the capability of this device is presently in progress.

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