CHARGE-COUPLED SCANNED IR IMAGING SENSORS

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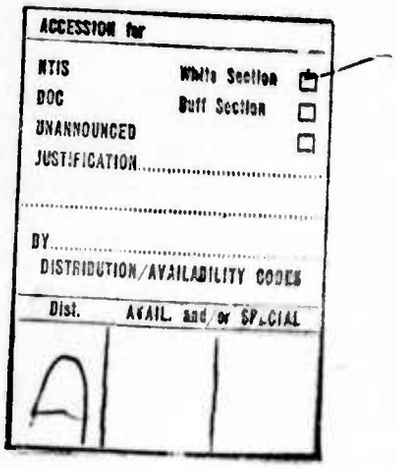

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A charge-coupled imager sensitive to infrared light as far out as 3 μm has been fabricated and operated. It consists of a linear array of 64 Pd:p-Si Schottky-barrier detectors adjacent to a three-phase charge-coupled shift register. The design has a single level of metallization with gaps. A single transmission gate, when pulsed on, coupled each detector to its associated shift register gate, thereby setting each barrier to a reverse bias determined by the potential applied to the transmission gate. Inci-

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20. dent infrared light discharges the individual detectors during the detector exposure time. The charges transferred into the CCD shift register the next time the transmission gate is pulsed are transferred out sequentially by the charge-coupled shift register to produce the video signal. The output is obtained from a floating diffusion connected to an on-chip MOSFET. The shift register had transfer losses as low as 5×10^{-4} per transfer as measured with an electrical input. Visible images were sensed directly by illumination of the shift register through the gaps as well as through the unthinned substrate. Infrared images ($1.1\ \mu m < \lambda < 3.0\ \mu m$) were sensed by the Schottky-barrier detectors illuminated through the (transparent) substrate. The two imaging modes could be easily distinguished by their spectral sensitivities as well as by their response to changes in integration time, since the integration time for IR detection at the Schottky barrier and the integration time for intrinsic silicon absorption at the shift register can be adjusted independently. All IR measurements were made at liquid-nitrogen temperature. A scheme for observing low-contrast, thermal scenes without requiring the charge-coupled shift register to carry the entire background signal has been implemented in the design of this chip. The investigation of optical detectors which are possible alternatives to palladium silicide Schottky barriers has been confined to the study of PbS-Si heterojunctions. It has been demonstrated that PbS films chemically deposited upon Si can be delineated to give elements of the size and packing density required. Delineated PbS samples have been shown to have dark-current and photoresponse characteristics suitable for the device. Uniformity of dark-current characteristics was examined using a set of 10 heterojunctions formed on a single chip of 10 ohm·cm n-type Si. The average dark CD at 77°K was 4.6×10^{-10} A/cm^2. The average deviation was 1.1×10^{-10} A/cm^2. Low-temperature heat treatment in air produces a decrease in the dark current and an increase in the photoresponsivity of cooled heterojunctions. The largest PbS peak photovoltaic responsivity observed to date is 4.5×10^{-3} A/W at 2.9 μm.

PREFACE

This Semiannual Technical Report was prepared by RCA Laboratories, Princeton, NJ, under Contract No. F19628-73-C-0282 and ARPA Order No. 2444. It describes work performed from 29 December 1973 to 30 June 1974, in the Process and Applied Materials Research Laboratory and in the Materials Research Laboratory. E. S. Kohn and M. L. Schultz are the principal investigators; the respective Project Supervisors are K. H. Zaininger and H. Kressel. Other members of the Technical Staff who participated in the research are: R. V. D'Aiello, S. O. Graham, and G. Fryszman. Sven Roosild and Freeman Shepherd are the AFCRL Contract Monitors.

The manuscript of this report was submitted by the authors on 15 July 1974. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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I. INTRODUCTION

The objective of this contract is the development of charge-coupled imaging arrays sensitive to infrared light. Two approaches are receiving our attention. The first is the use of Schottky barriers as optical detectors, and the second approach is the use of lead-sulfide films as the photo-responsive elements. Schottky-barrier detectors are easier to fabricate as the technology existed prior to this work, and they have the advantage of excellent uniformity which is essential for thermal detectors. Lead-sulfide detectors offer the possibility of greater sensitivity as well as the possibility of reduced cooling requirements. The development of the technology for integrating PbS detectors with silicon-integrated circuits was therefore made a part of this program.

Our first design was a 64 x 1 array of Pd:p-Si Schottky-barrier detectors read out by a three-phase charge-coupled shift register. Infrared imaging has been demonstrated with chips of this design. A scheme for viewing low-contrast, thermal scenes without requiring the shift register to carry the large background signal has been incorporated into the design of this chip. We accomplished this while retaining the capability of viewing high-contrast, near-infrared scenes such as those containing jet or rocket plumes. Current objectives of this work include improved operation of the existing chips, accurate determination of the detector uniformity, and demonstration of the low-contrast mode of operation. Another important current objective is the design of a second chip which will have the capability of using lead-sulfide detectors or Schottky-barrier detectors. It will have a gapless design with overlapping layers of polysilicon and metal for improved shift-register performance and stability. This linear array should provide the information we need to design a two-dimensional array, the ultimate objective.

II. DEVICE FABRICATION

Prior to this reporting period, the 64 x 1 Schottky-barrier CCD was designed, and masks were programmed and ordered. They were delivered, and the fabrication steps were scheduled. Fabrication of IR CCD's began at the beginning of this period. The channel-stop diffusions and the source-drain diffusions were done in the Integrated Circuit Technology Center at Princeton, as was the gate oxide growth and the contact hole preparation. The wafers were then sent to RCA Somerville where the palladium was evaporated, reacted, and etched, and the titanium and aluminum were evaporated. On two control wafers, only Al was used. The wafers were then returned to Princeton for the metal definition step. Figure 1 shows photomicrographs of the two ends of a completed device on a wafer containing about 50 chips. The vertical white rectangles in a row along the top (1) are the Schottky-barrier metallizations, each overlapping the contact holes to the substrate and to the setting and transfer diffusions. The setting gate (2) and the transfer gate (3) control the channels to the setting diffusion (contacted by 4) and the phase-one gates (5), respectively. The bonding pad for the phase-one bus bar (5) cannot be seen because it is near the center of the CCD. Phases two (6 and 7) and three (8 and 9) are double-end connected because they require a diffused crossunder which is more resistive than a metallization. Two separate gates are provided at the beginning (10 and 11) of the shift register and at the end (12 and 13).

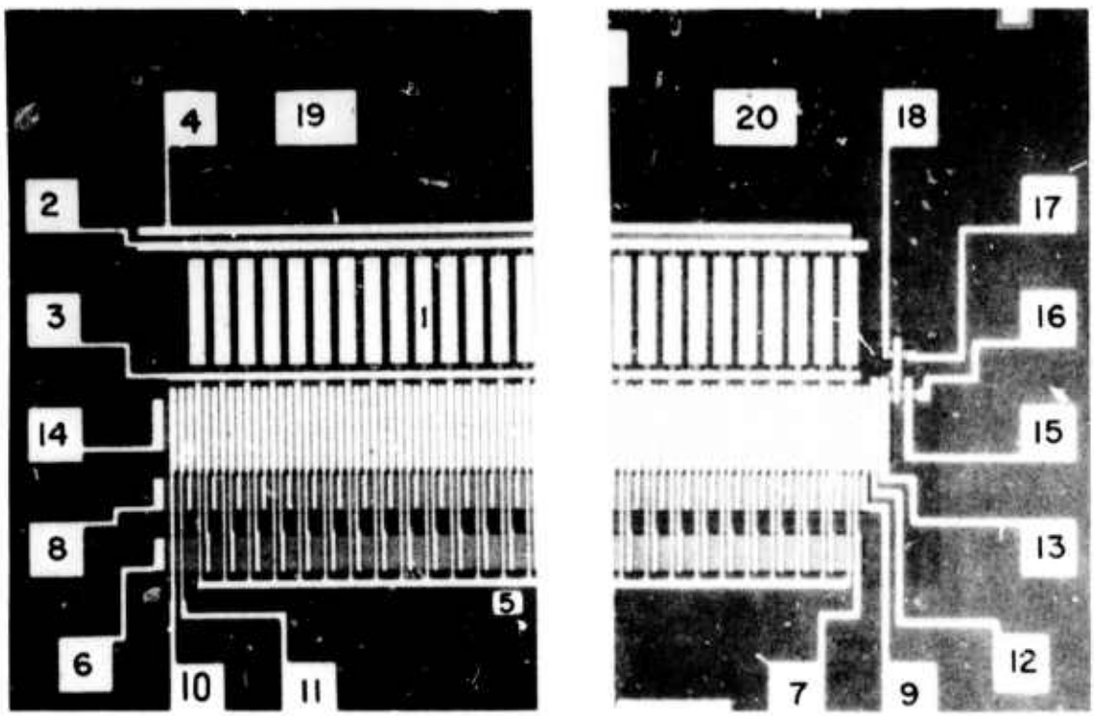


Figure 1. Photomicrographs of the two ends of the CCD chip.

A source diffusion (contacted by 14) is provided to permit electrical input to the shift register while a floating diffusion with a reset gate (15) and drain (16) is provided at the output. The floating diffusion is connected to an on-chip MOS transistor whose source and drain diffusions are brought out to pads 17 and 18. Contact to the substrate is made at pads 19 and 20, each of which contacts a channel-stop diffusion.

The output stage is seen more clearly in the enlargement in Fig. 2. The "L"-shaped floating diffusion (21) is seen to be connected through a contact hole to the gate of the MOS transistor (22). It is overlapped by the reset gate (23) which controls the channel to the drain (24). The channel stop diffusion surrounding these elements could be seen under the microscope but does not show well in this photograph.

A probe card was made to order for testing the chips before the wafer was cleaved. Figure 3(a) shows a circuit being tested in the probe-card station as seen through the low-power binocular microscope on the station. Several chips were tested for open-circuits, short-circuits, and diode

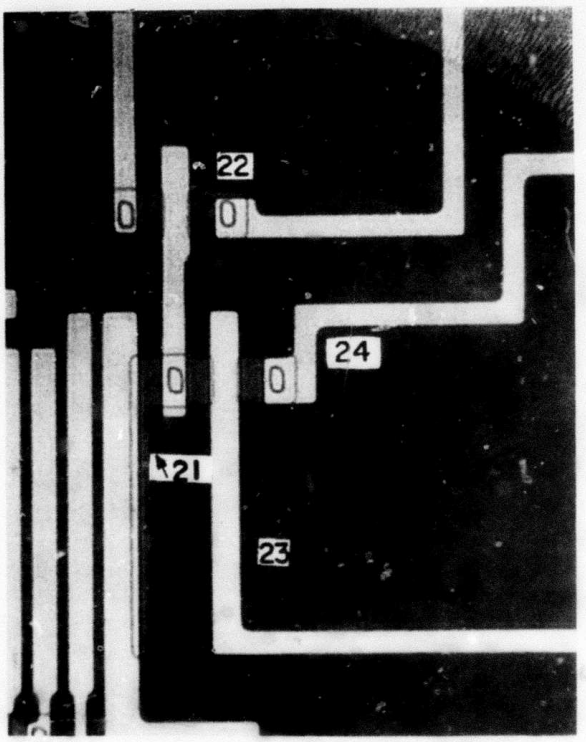
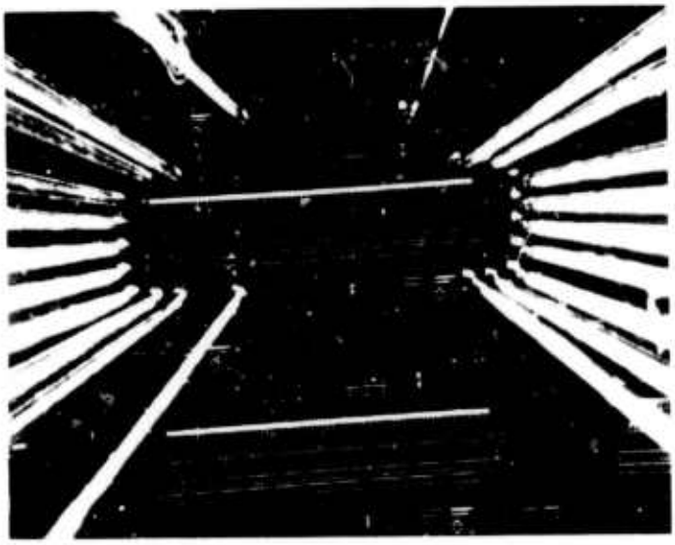
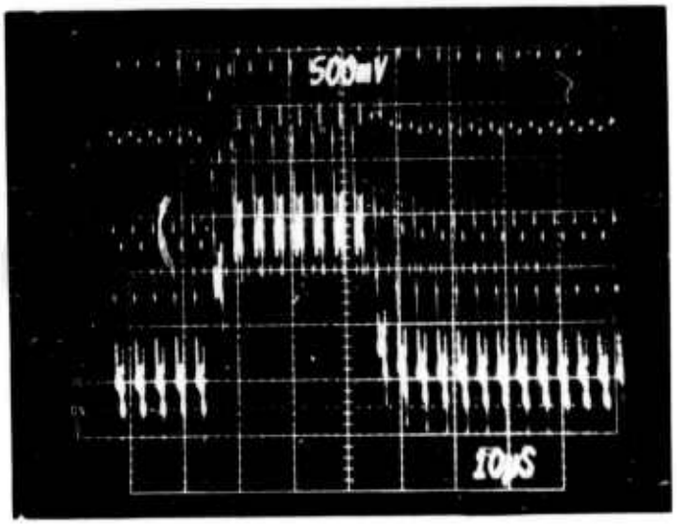


Figure 2. Output region of the CCD chip showing the floating diffusion (21), the MOS transistor (22), the reset gate (23), and the drain (24).



(a)

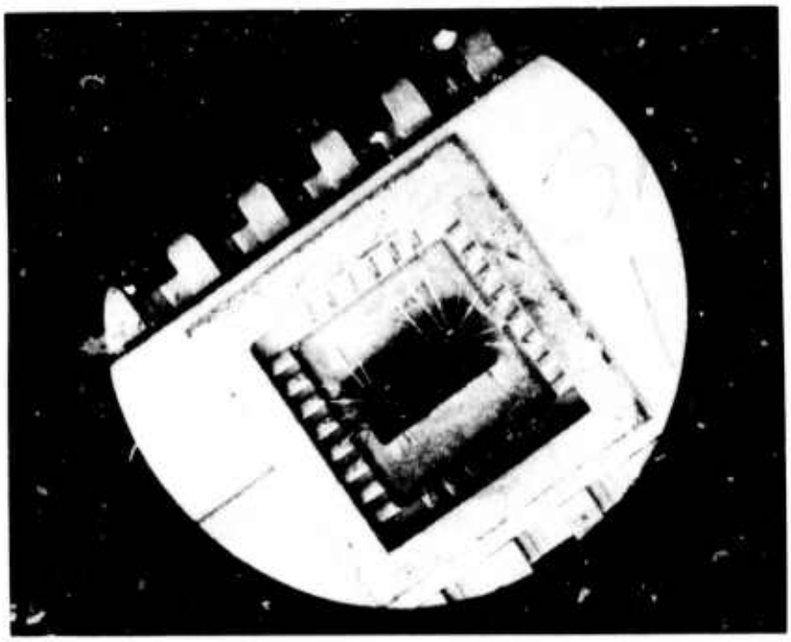


(b)

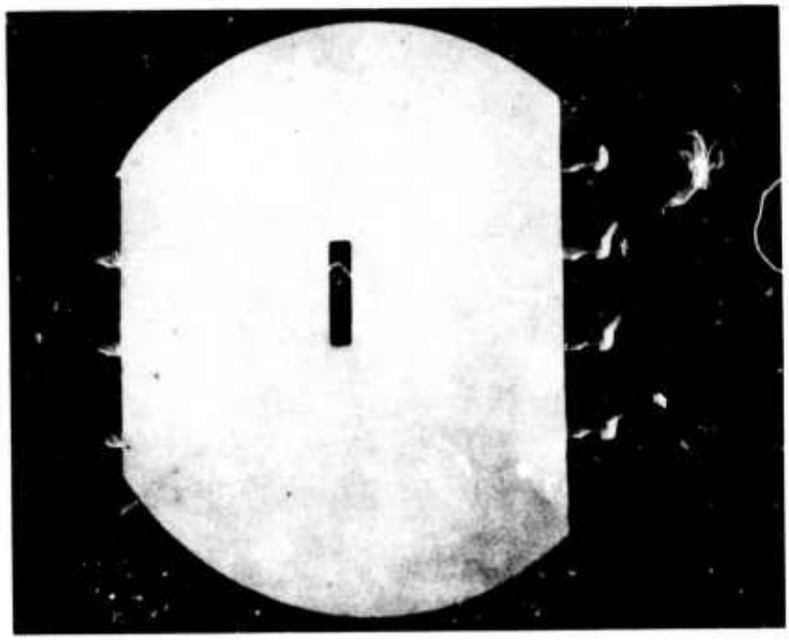
Figure 3. (a) Photograph through the microscope of the probe-card station showing one circuit on a wafer being tested.
(b) Output signal from a chip operated on the probe-card station with an 8-bit input.

characteristics. When all of these tests proved satisfactory, it was decided to operate the chips as CCD shift registers with electrical input directly on the probe-card station and to select chips on the basis of CCD performance. About three-fourths of the chips with no obvious visible defects operated well as shift registers. The output signal from a typical good chip with an electrical input of eight "1's" is shown in Fig. 3(b). It consists of eight "1's" with the leading "1" degraded by one-third, all delayed by 64 clock periods from the input. The details of this electrical test are discussed later. While the clock noise pattern was particularly complicated because of crosstalk from the several unshielded leads carrying clock waveforms, it was nevertheless possible to sort out the chips on the wafers and mark the bad ones on the basis of this test. Since most of the shift registers on the wafers made with Pd worked as well as the devices on wafers made with Al only, nothing more was done with the Al-only control wafers.

A 28-pin gold-plated, ceramic dual-in-line holder was selected for the chips. After the wafers were scribed and cleaved, tested chips were mounted and bonded to the holders which had been previously prepared with 0.120- by 0.030-in. rectangular holes ultrasonically ground in the centers of the 0.200-in.-square chip mounting areas. These holes are required for rear illumination with infrared light. A bonded chip is shown in Fig. 4(a); the back of the package is shown in Fig. 4(b) with the same magnification. In order to affix the chip with the detector array directly over the hole, we viewed the chip from the top, as in Fig. 4(a), with a low-power microscope equipped with an infrared image converter in place of the eyepiece. The image converter has an S-1 photocathode that is sensitive to light transmitted by silicon. With illumination from below the holder, we could see the bright rectangular hole in the ceramic masked by the aluminum metallization pattern of the device. All bonded chips were positioned in this manner.



(a)



(b)

Figure 4. (a) Photograph of a bonded chip.
(b) View of back of holder.

III. OPERATION OF THE CCD WITH ELECTRICAL INPUT

A circuit diagram of the IR-CCD chip, with pin numbers indicated, is shown in Fig. 5. The three phase gates must be provided with overlapping pulse trains as discussed in the last report [1]. The fall time of the pulses should be at least 70 nsec to provide sufficient transfer time. The extra gates labeled G_2, G_3, and G_4 are connected in sequence with the chains of 64 gates. The reset gate receives about 5 V dc and the drain diffusion 15 V dc. The substrate is biased negatively by a few volts so that the gates always keep the surface inverted. The input signal is applied to G_1 while the bias charge level is controlled by the potential applied to the source diffusion. For operation with electrical input (or visible optical input), the transfer gate is set at about 6 V negative, isolating the CCD from the Schottky-barrier detectors. The output signal is taken from the MOS transistor whose gate follows the potential of the floating diffusion. The MOS transistor can be wired as a source-follower or as a common source-amplifier, depending on which polarity of output signal is desired. For electrical operation, the three-phase clock waveforms must run continuously. A word generator circuit runs in synchronism with the clocks and produces a settable number of positive pulses (such as 8) each time it counts a settable number of clock pulses (such as 128). The word (8 pulses) is expected at the output 64-clock periods later since it must go through 64 bits on the chip. This is easily seen on an oscilloscope triggered on the first input pulse. Figure 6 shows such an output word with 1/10 of the leading pulse missing. Since there were 192 transfers (64 x 3), the average transfer loss was about 5×10^{-4} per transfer. The output signal in Fig. 6 is about 2.5 V superimposed on several volts of clock noise. The clock noise can be removed with either a low-pass filter or with a sample-and-hold circuit. In order to get this fairly good transfer efficiency, it is necessary to introduce a bias level or "fat zero". This means that each well in the shift register is filled to a small fraction of its capacity in the absence of any "signal". For our chip running at the above clock rate, the optimum bias level was experimentally determined to be 0.3 μA.

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1. E. S. Kohn and M. L. Schultz, Charge-Coupled Scanned IR Imaging Sensors, Semiannual Technical Report, AFCRL-TR-74-0056, Contract No. F19628-73-C-0282, 14 January 1974.

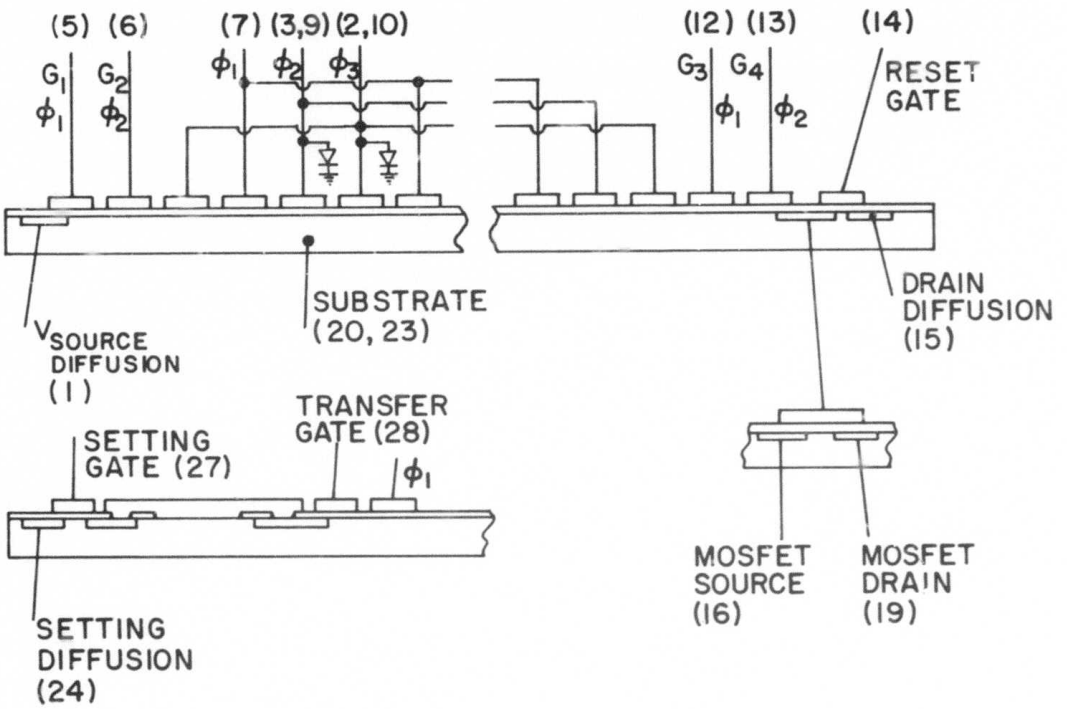

Figure 5. Circuit diagram of the IR-CCD chip.

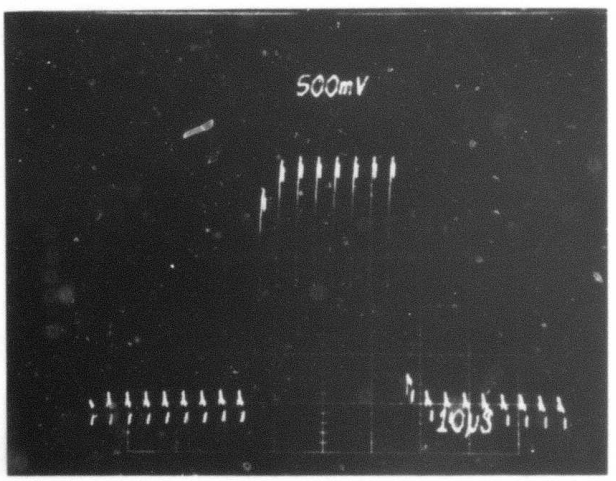

Figure 6. Output gate for an 8-bit electrical input.

IV. VISIBLE LIGHT IMAGING

Visible light (using the term to mean light absorbed by silicon as opposed to longer wavelength infrared) can be detected and imaged directly by the CCD shift register. The image can be incident on the top of the wafer through the gaps between the electrodes or on the back of the wafer. In the latter case, the wafer should be thinned or few of the minority carriers created by the light will be collected in the CCD wells. Our chips were not thinned since we were not concerned with detection of visible light.

In either case, image detection by the shift register requires one or two of the phases to be held on for a period of time while the other(s) are held off. This "integration time" should be much longer than the time required to read out the line after the clock waveforms begin running again in order to avoid smear. In our case the latter time is ~ (the number of bits) $\div 1/4 \times 10^6$ sec^{-1} (the clock rate), or about 1/4 msec. Thus, for integration times more than a few milliseconds, there should be no smear. The bias level required for good transfer efficiency can be introduced by weak uniform illumination of the shift register or by an electrical input pulsed off during the integration time. The former is generally more convenient for optical measurements. Figure 7(a) shows the output signal corresponding to a small light spot imaged through a microscope onto the beginning of the shift register. The spot illuminated about two bits, and little spreading of the signal can be seen even though the signal was transferred through the entire shift register to reach the output. The bottom trace in Fig. 7(b) is a magnified view of the output while the top trace is without the light spot. The weak uniform illumination can be seen in all three traces.

(a)

(b)

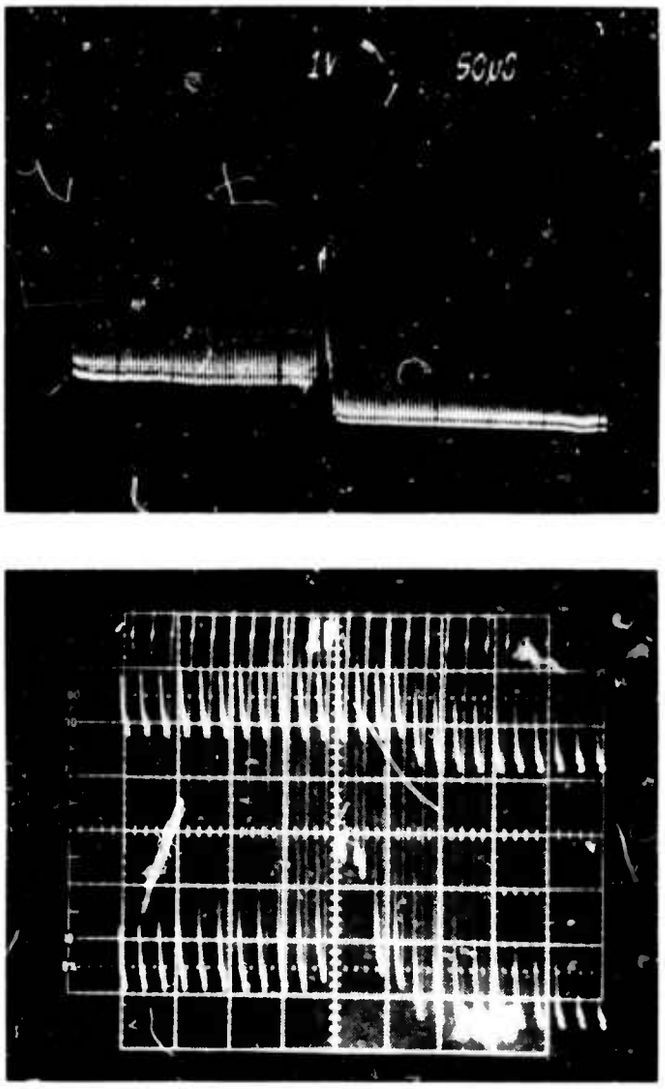

Figure 7. (a) Video signal for a spot of visible light shining on the beginning of the shift register.
(b) Expanded view of the video signal without the light spot (top) and with the light spot (bottom).

V. TESTING OF SCHOTTKY-BARRIER DETECTORS ON CCD CHIPS

The Schottky barriers on the IR-CCD chips were tested for dark current and relative spectral response. Since the chips had no provision for direct connection to the detector metallizations, the circuit in Fig. 8 was used for the dark-current measurement. The transfer gate was tied to a negative voltage to isolate the detectors from the shift register while the setting gate was tied to a positive voltage to connect the setting diffusion to all the detectors at once. Thus, the setting diffusion provided contact to all 64 detectors at once. Data for three typical samples at 77°K is shown in Fig. 9. At room temperature, the reverse currents were many orders of magnitude higher, as expected. While most of the samples tested within the range shown in the illustration, a few had much higher dark current. It was not possible to tell from this test whether a few or all the detectors were contributing to the dark current.

The circuit for measuring the relative spectral response of the detectors is shown in Fig. 10. The setting and transfer gates are biased as in the previous circuit. The sample is immersed in liquid nitrogen, and chopped monochromatic light is imaged onto the detectors through the substrate. The

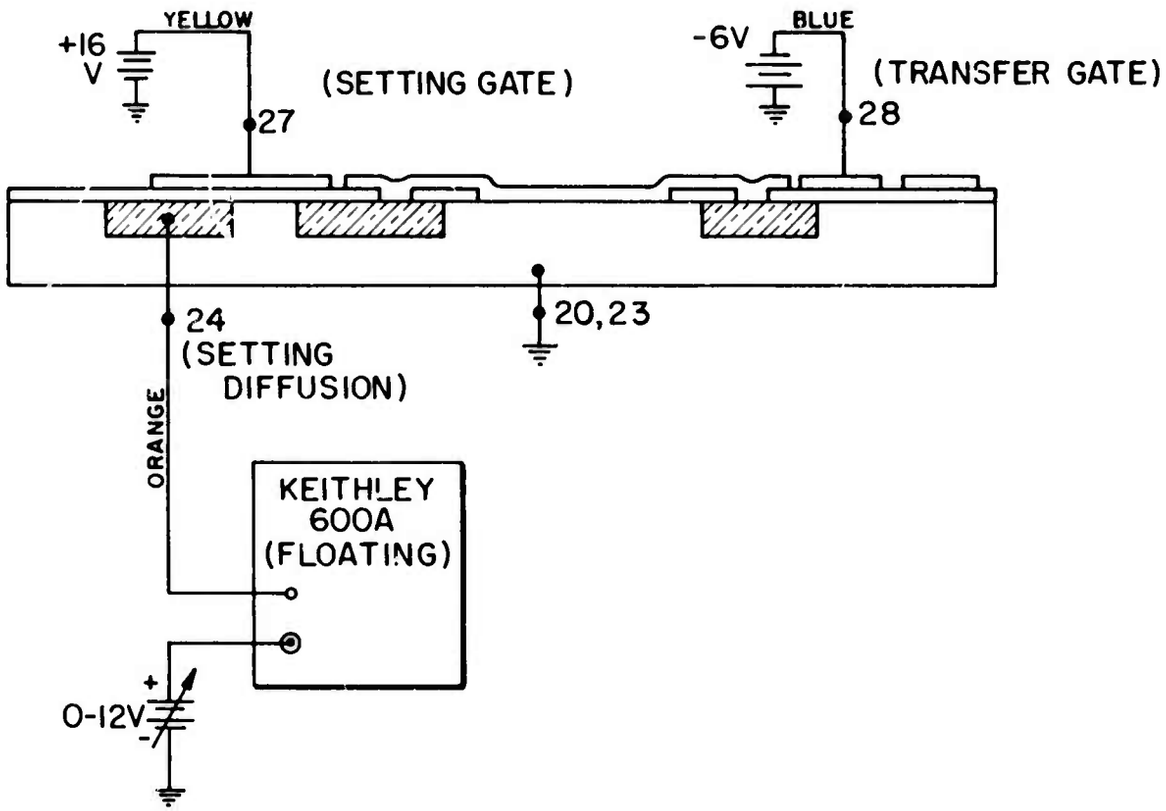

Figure 8. Circuit for measuring Schottky-barrier dark current.

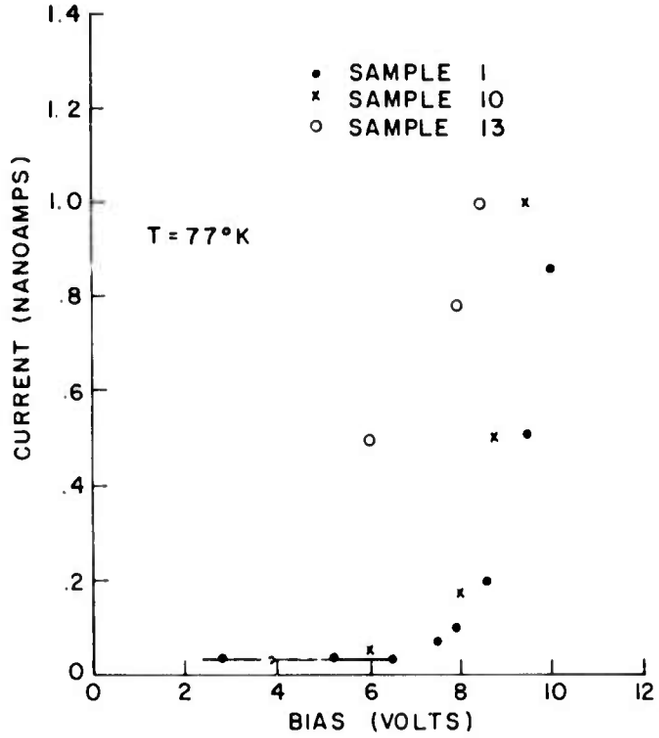

Figure 9. Dark-current characteristics of the three CCD samples.

photovoltaic signal is taken from the setting diffusion and is applied to a lock-in amplifier referenced to the chopper wheel. In this mode of operation, the diffusions become forward-biased, but not sufficiently to conduct. The relative spectral response of two IR-CCD arrays is shown in Fig. 11 and is compared with previous data on a test wafer.

The curves, which are individually normalized to their peaks, are very similar in shape, the only significant difference being the relative magnitude of the intrinsic silicon absorption peaks at 0.9 μm. This occurred because in the IR-CCD chips the diffusions as well as the Schottky barriers collected electrons created by intrinsic absorption in the silicon, while the old test wafer had no diffusions. Thus, in the IR-CCD samples, the area over which intrinsic photoelectrons could be collected was considerably larger than the Schottky-barrier area while in the old test wafer, the two were the same.

It is apparent from Fig. 8 that an MOS transistor is formed by the setting diffusion, the setting gate, and the diffusion contacting each detector. These elements correspond to the drain, the gate, and the source, respectively. While a connection to the contacting diffusions is not available, at room temperature the detectors are essentially short-circuits. Thus, these elements can be tested as an MOS transistor with the source connected to the substrate. The collector characteristics are shown in Fig. 12, showing a transconductance of 650 μmhos.

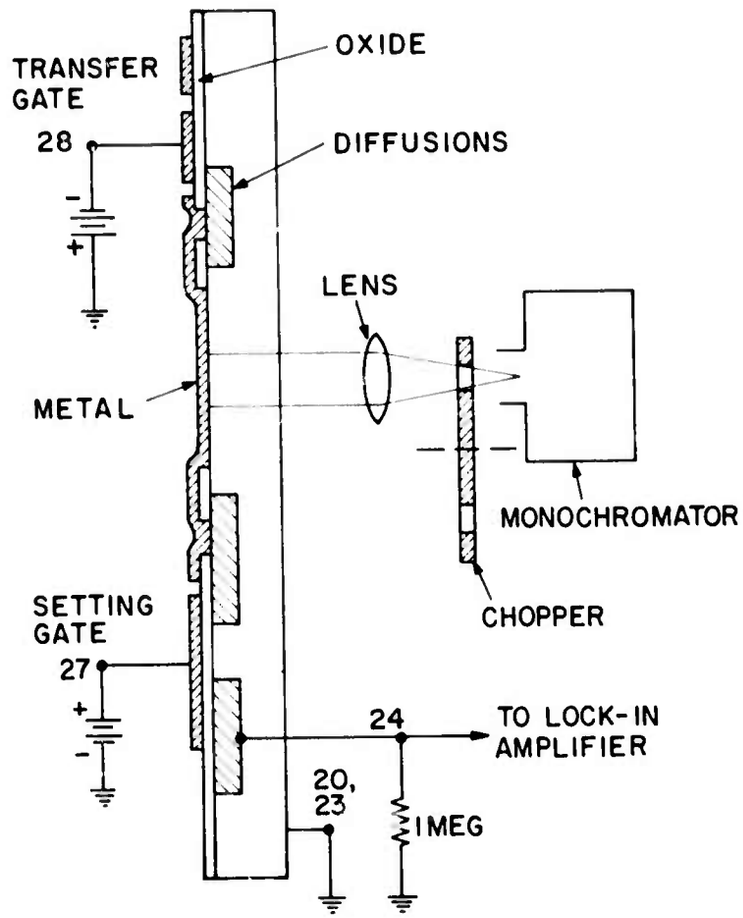

Figure 10. Circuit for measuring relative spectral response of detectors on IR-CCD chips.

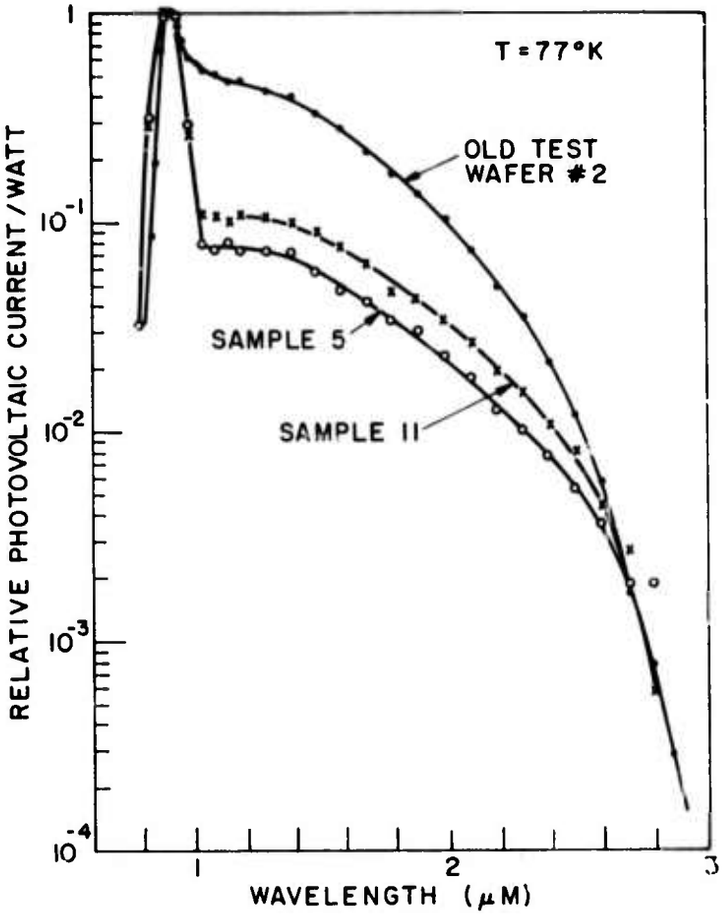

Figure 11. Relative spectral response.

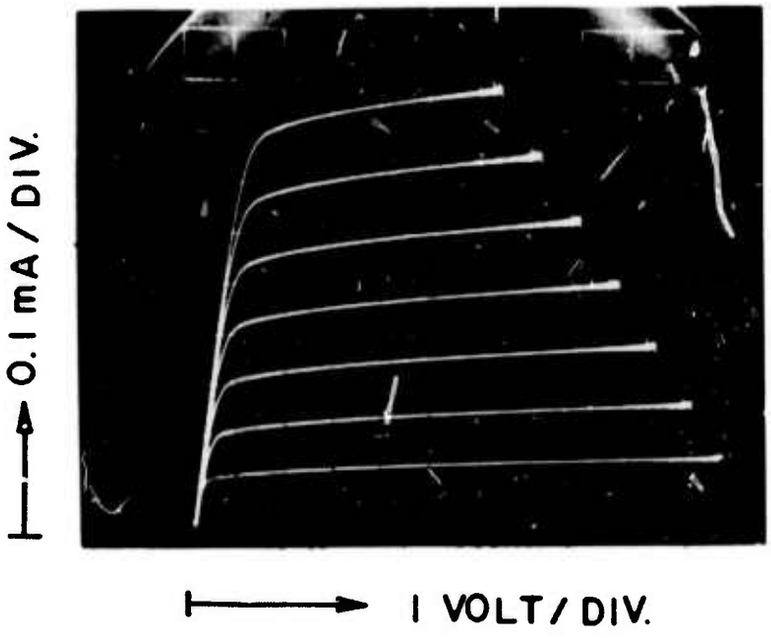

Figure 12. Characteristics of setting circuit of IR-CCD chip run as an MOS transistor. The bias is 0.2 V/step; the transconductance (g_m) is 650 μmhos. The largest trace is for zero bias.

VI. DETECTION OF INFRARED IMAGES

For infrared imaging, the IR-CCD chip must be operated at reduced temperature and illuminated through the back of the substrate. A special socket, with a hole to permit viewing of the window in the chip holder, was wired and mounted at the end of a plastic rod so that it could be positioned in a quartz optical dewar containing liquid nitrogen. A weak tungsten lamp illuminated an adjustable slit which was imaged on the IR-CCD chip with a special germanium lens. The lens also served to block any light whose wavelength was less than 1.7 μm. A polished germanium wafer 0.010 in. thick was tested on a spectrophotometer to confirm the above cutoff wavelength and was used to make doubly sure that no light passed that could be absorbed by silicon. A diagram of the optical path is shown in Fig. 13.

The auxiliary pulse requirements for infrared imaging were discussed in detail in the previous report [1]. The timing diagram is given in Fig. 14. The setting pulse is required only in the low-contrast mode. In the high-contrast mode, the Schottky barriers are set to the required reverse bias when the transfer pulse is applied and the signal loaded into the wells of the shift register. The voltage to which the Schottky barriers are set is determined by the height of the transfer pulse so long as the shift register well is not filled. Since the barriers are set to the same potential after each frame, the charge is removed, and, thus, the signal in the CCD well is just the amount by which the Schottky barrier was discharged by photoemission and by dark-current mechanisms during the time period between transfer pulses. Hence, this time is the integration time for infrared detection. The shift register runs continuously during the integration time with the first 64 bits after the transfer pulse ends comprising the video signal. The only time when the shift register is not running is during the transfer pulse. Hence, the transfer pulse width is the integration time for visible light detection. Thus, any doubt as to whether the video signal was caused by absorption at the shift register or absorption at the Schottky barriers could be resolved by our varying the two integration times, one at a time, and observing which affected the signal in question. The video signal corresponding to uniform infrared illumination (filtered by the germanium wafer) is shown as the second trace in Fig. 15. The top trace is without the illumination. The transfer pulse was only 1.5 V because the dark current rose quickly with Schottky-barrier voltage in this sample. For some samples, it was possible to set the transfer pulse as high as 15 V before running into excessive dark current. The ability to use high transfer pulses is desirable since it corresponds to high signal-handling capacity. Figure 16 shows the video signal for imaging with a narrow slit and a wide slit in different locations. The signal with the narrow slit was 2 bits. Making the slit still smaller did not improve the resolution beyond this. The limitation was probably in the focussing as the shift register had sufficiently good transfer efficiency to deliver a single recognizable bit. For this chip, a transfer pulse as high as 15 V could be used. The optical system was focussed using the video signal of a narrow slit. The slit could then be moved laterally to scan the signal across the oscilloscope screen. A photograph of the video signals with the narrow slit in four positions is shown in Fig. 17. A soldering iron tip, invisible to the human eye, easily saturated the video signal.

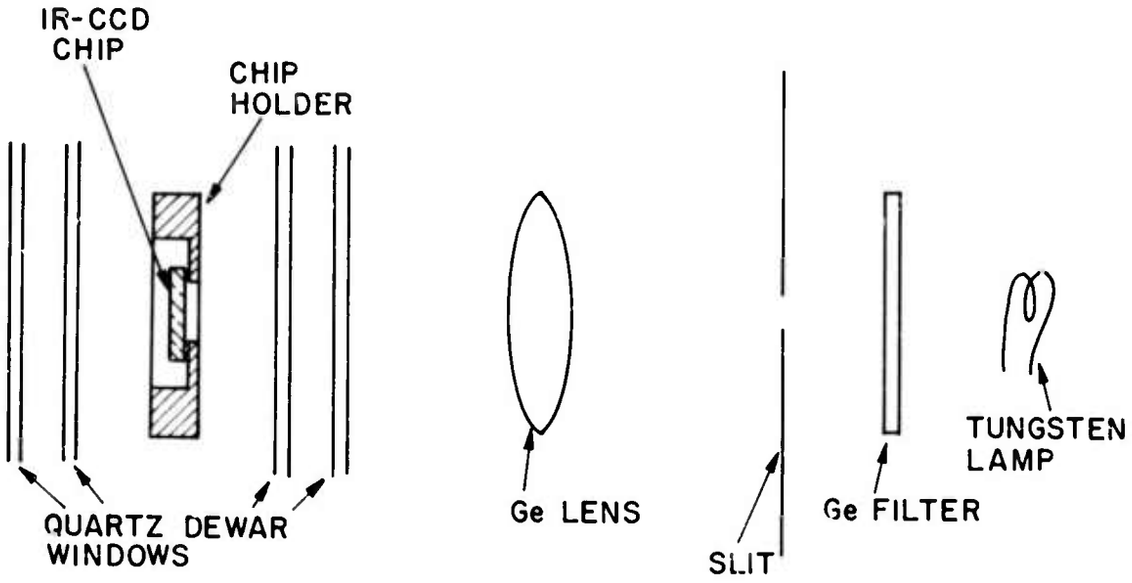

Figure 13. IR optical path.

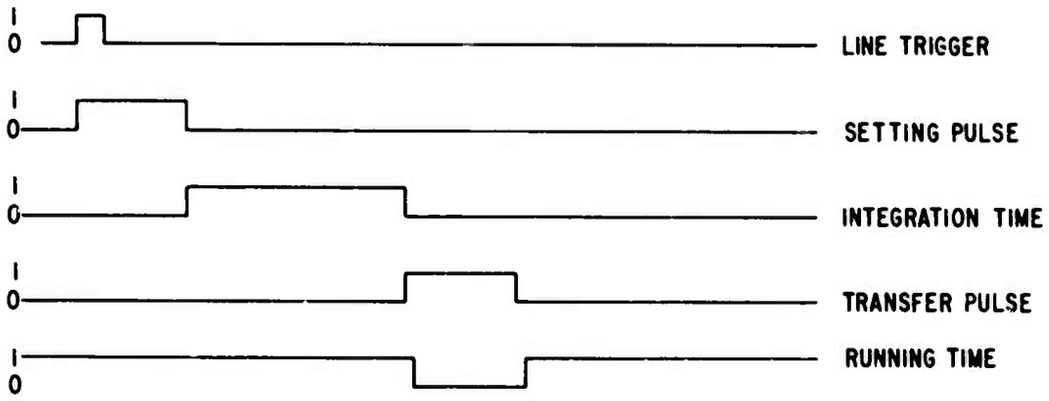

Figure 14. Pulse timing diagram.

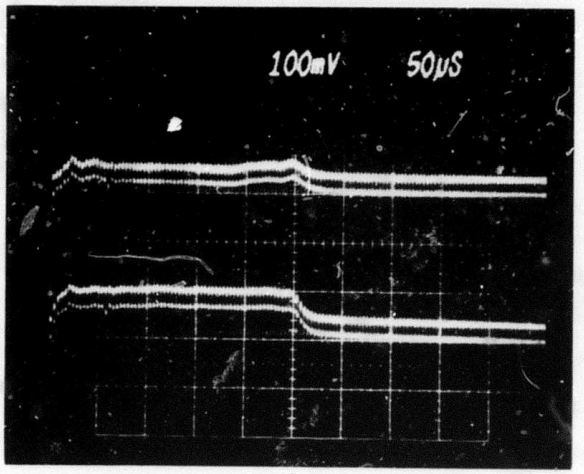

Figure 15. Video signal with uniform infrared illumination; top - without illumination, bottom - with illumination.

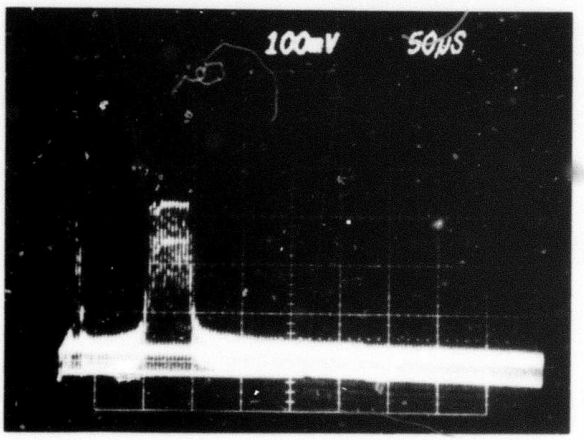

Figure 16. Video signal for infrared imaging with a narrow and a wide slit. The first trace was taken with the slit smaller than 0.1 mm; the second was taken with the slit repositioned and set to 1.0 mm.

It should be noted that unlike visible charge-coupled imagers, this IR CCD is immune to smear and blooming. Smear occurs when imaging is performed by the shift register, and an unusually bright spot creates a significant number of carriers in a shift register well during the short time between two consecutive clock pulses. Since our chip will not be allowed to image at the shift register, this smear mechanism does not apply. Blooming occurs when a bright spot causes a well to become overfilled with minority carriers which then transfer to adjacent wells. Again this is not possible at our shift register because we do not permit imaging there. A charge-coupled imager with separate p-n junction detectors or photogate detectors could conceivably bloom but Schottky barriers are majority-carrier devices. No minority carriers are even generated, so there is no blooming mechanism.

The detectors in our chips appear to be uniform within about 10% across a chip. This is a preliminary number and will be evaluated more carefully in future work. The open gaps between the transfer gate and the phase-one electrodes may be at least partially responsible for the variations.

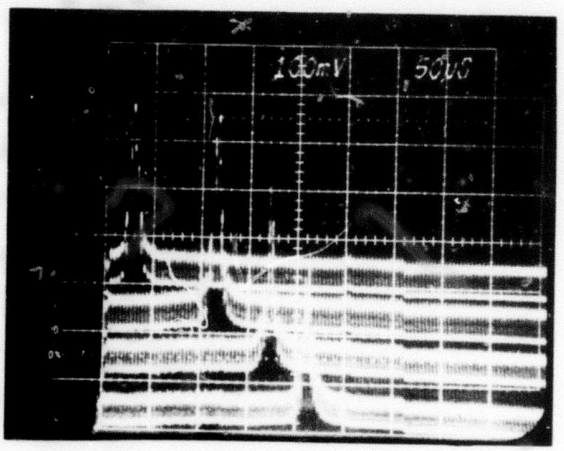

Figure 17. Video signal corresponding to a narrow slit in four positions.

VII. LEAD SULFIDE - SILICON HETEROJUNCTIONS

Results summarized in the first Technical Report [1] issued under the present contract have indicated the potential usefulness of PbS-Si heterojunctions as the optical detectors for the IR CCD. The possibility of obtaining very low dark currents at reverse biases up to at least 10 V at reduced temperatures was demonstrated. Photovoltaic response was observed at wavelengths as long as about 3.5 μm. In view of the possibilities offered by the heterojunction approach to the use of PbS as the photosensitive material to obtain response at wavelengths beyond the Si threshold, the decision was made, at the start of the present report period, to terminate the investigation of PbS photoconductive films. The principal objectives during this report period were: (a) to demonstrate that PbS films on Si could be delineated by photoresist masking, followed by chemical etching to produce heterojunction detector elements of the size and density required for the device, and (b) to determine whether or not the heterojunction properties important to the operation of the device were degraded by the masking and etching procedures. It has been demonstrated that the delineation can be carried out and that the properties of heterojunctions so delineated are suitable for the device. Some progress has been made, also, in devising heat treatment procedures that lead to improvement of the photoresponsivity of low dark-current PbS-Si heterojunctions in the PbS wavelength range (1.2 μm to 3.6 μm).

The procedures used for the chemical deposition of polycrystalline PbS films and for their delineation have been described [1]. In order to determine the resolution capabilities of the masking and etching procedures, a photoresist pattern having areas of approximately the size and shape required for the detector elements and also having gaps of several widths, the smallest being 0.1 mil, between adjacent areas was laid down on a PbS film deposited over Si. The dimensions of the delineated areas and the widths of the gaps in the etched film indicate that undercutting to the extent of about 0.05 mil occurs. The edges of the PbS regions are somewhat irregular because of the granularity of the polycrystalline PbS. Some of the 0.1-mil gaps were bridged by PbS projections on the order of 0.1 to 0.2 mil wide. There were virtually no such bridges across gaps having widths of 0.2 mil or more. A photograph of a portion of a delineated PbS film is given as Fig. 18. The dimensions of the large rectangles are 1.2 mils x 7.5 mils and their separation is 0.5 mil.

The heterojunctions prepared for the investigation of dark-current and photoresponse characteristics consisted either of 80-mil-diameter circles of PbS on Si or of 80-mil-diameter circles of PbS deposited over SiO_2 film on Si containing 40-mil-diameter holes in the oxide. In both cases, the PbS circles were delineated by photoresist masking and etching. Some samples of approximately the same areas but not having been so delineated were prepared for comparison. In all cases, contact to the PbS was made by Ag paste and a fine wire.

The earlier work [1] has indicated that the magnitude of the reverse-bias dark-current density (CD) of cooled PbS-Si heterojunctions depends strongly upon the resistivity of the n-type Si used in preparation of the heterojunctions. One sample each on 10 ohm·cm and on 0.1 ohm·cm <100> Si had been studied. The former had a CD on the order of 10^{-10} A/cm^2 for bias in excess

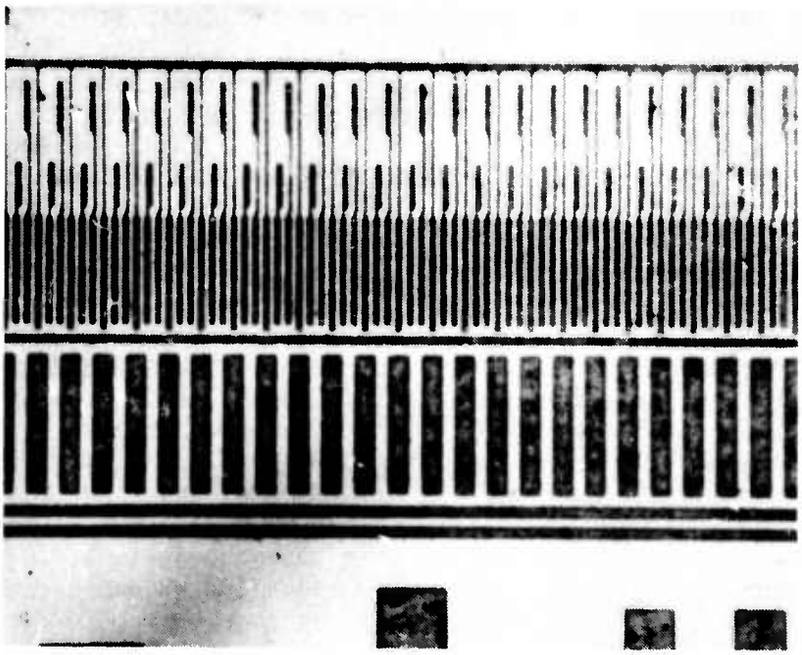

Figure 18. Photomicrograph of a portion of a delineated PbS film on Si.

of 10 V. The latter reached the upper limit of acceptable CD for the device (3×10^{-8} A/cm^2) at 0.3 V.

In order to obtain additional information on the effect of the resistivity of the Si upon the heterojunction properties, sample S20D was prepared on 1 ohm·cm n-type Si. The CD's at several temperatures are given as functions of bias in Fig. 19. At room temperature, the CD is about 1 to 2×10^{-4} A/cm^2. This is about an order of magnitude larger than for 10 ohm·cm Si. Breakdown is in excess of 20 V. As the sample is cooled, the CD at a fixed low bias decreases but, at the same time, the increase of CD with bias at a given temperature becomes more rapid. Consequently, the curve for a given temperature may cross that for a higher temperature. At 177°K, the CD reaches 3×10^{-8} A/cm^2 at 2.3 V while at 90°K this occurs at 2.0 V. Such bias values are too small for satisfactory operation of the device.

A set of curves for a recent sample on 10 ohm·cm Si, S21A3c, is given in Fig. 20 for comparison. These data refer to the sample after it had been given a low-temperature heat treatment in air (see below). The same trend of behavior with temperature occurs for this sample as for S20D but to a very much lesser extent. Even at 90°K, the rapid rise of CD with bias sets in only above ~12 V. Below this bias, the CD's are less than 10^{-10} A/cm^2. CD values in the low 10^{-10} A/cm^2 region or smaller are difficult to determine accurately since external leakage currents may be comparable with the sample currents.

It would appear that Si having resistivity as low as 1 ohm·cm is not suitable for the device. The range of resistivity between 1 and 10 ohm·cm has not yet been explored.

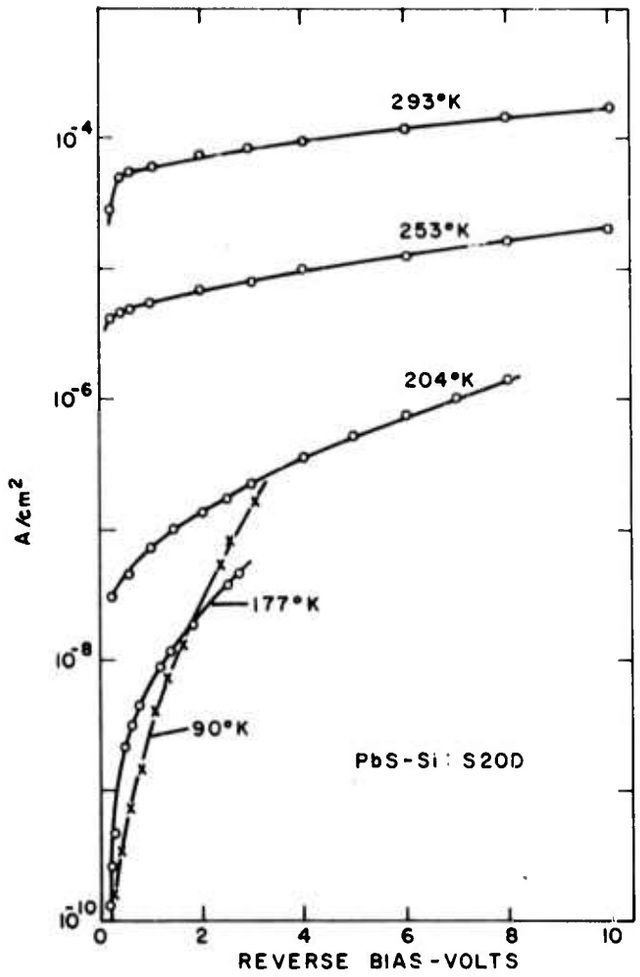

Figure 19. Dependence of dark-current density upon reverse-bias voltage at several temperatures for PbS-Si heterojunction S20D on 1 ohm·cm n-type Si.

To date, 20 heterojunction samples prepared on 10-ohm·cm Si and delineated by photoresist masking and etching have been measured. All but one of these had, either in the "as-prepared" condition or after heat treatment, small enough CD's ($<3 \times 10^{-8}$ A/cm^2), when cooled, for device use at reverse-bias voltages large enough for satisfactory operation. In most cases, operation at biases at least as great as 10 V would have been possible.

A first estimate of the uniformity of junction dark-current characteristics of samples subjected simultaneously to the same processing conditions was obtained from a study of three heterojunctions: S21A3a, b, and c, that were prepared on a single chip of Si. The reverse-bias currents were measured with the chip mounted on a dipstick that had sufficient leads to permit measurement of the three samples in a single cooldown. The chip was enclosed in a can that excluded stray radiation. The upper family of curves in Fig. 21 gives the dependence of CD upon bias voltage for the three samples in the "as-prepared" condition. The measurements were made at a comparatively high

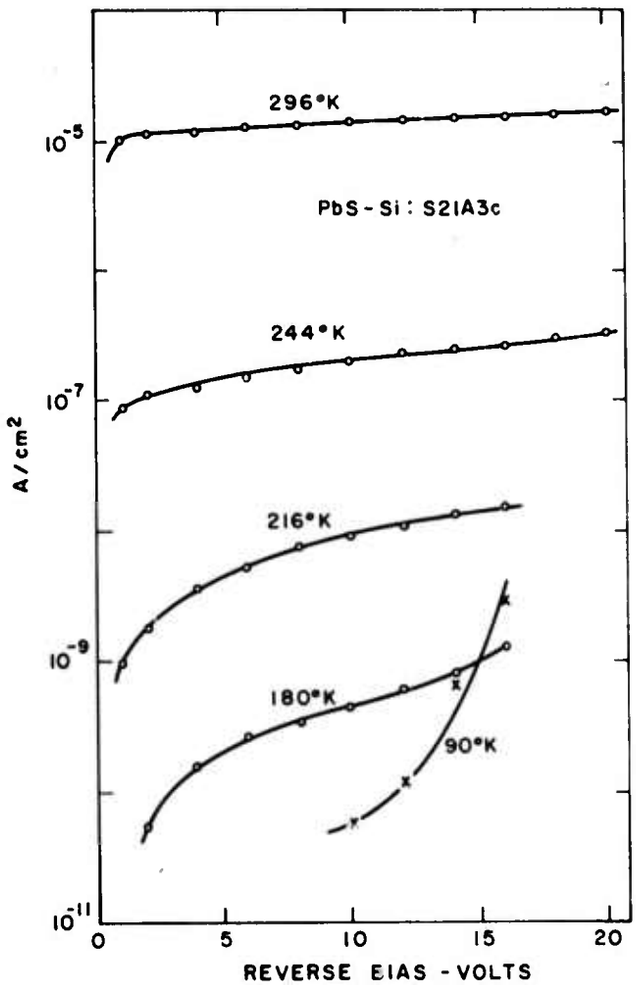

Figure 20. Dependence of dark-current density upon reverse-bias voltage at several temperatures for heat-treated PbS-Si heterojunction S21A3c on 10 ohm·cm n-type Si.

temperature so that the currents would be large enough (near 10^{-11} A) for accurate measurement. At 10-V reverse bias, the CD's were 2.3, 1.9, and 2.0 x 10^{-9} A/cm^2 for samples S21A3a, b, and c, respectively. The average deviation from the average value is less than 10%. The spread in CD's did not increase significantly at lower temperatures although the results are less precise since the currents were smaller.

A second study of uniformity of dark-current characteristics was made using sample S23C which consisted of two rows, each containing seven 40-mil-diameter heterojunctions on 100-mil centers. This array was mounted on a dipstick having sufficient leads for the measurement of 10 diodes; these were chosen at random from among the 14. At 77°K, the CD's at 10-V bias of the ten samples, in the "as-prepared" condition, ranged from a low of 2.3 x 10^{-10} A/cm^2 to a high of 6.3 x 10^{-10} A/cm^2. The average value was

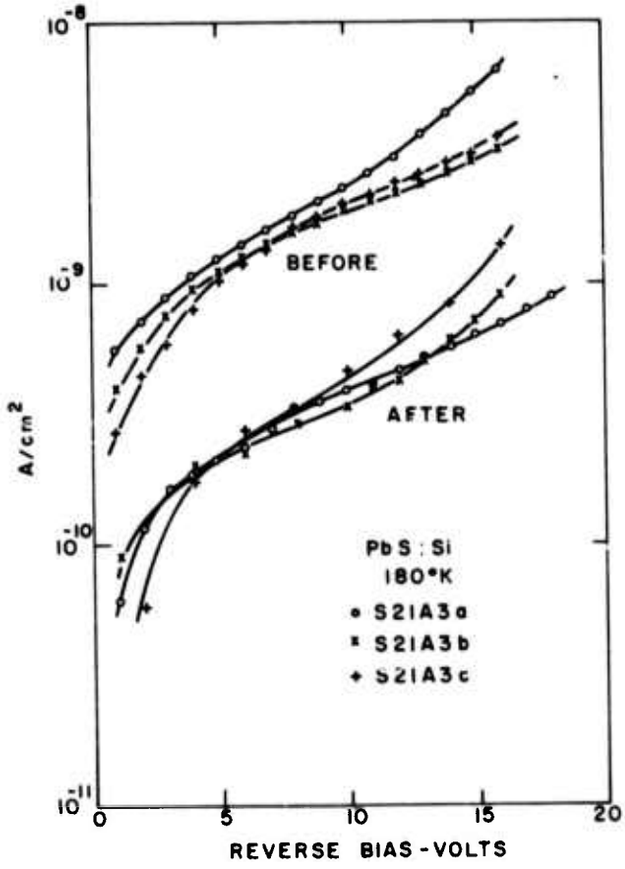

Figure 21. Dependence of dark-current density upon reverse-bias voltage at 180°K for three PbS-Si heterojunctions on 10 ohm·cm n-type Si before and after heat treatment.

4.6×10^{-10} A/cm^2 and the average deviation from the average was 1.1×10^{-10} A/cm^2. There seemed to be no correlation between CD and position of the diode in the array.

Earlier work had shown that a photoconductive PbS film, which had been delineated by photoresist masking and etching, behaved differently upon heat treatment from those which had not been in contact with photoresist [1]. This difference in behavior prompted the investigation of the effects of heat treatment upon the properties of delineated heterojunction samples. The set of samples S21A3a, b, and c, which by now had been transferred to the demountable dewar, was used. Heating was in air at temperatures up to 90°C for a total time of 3 hours. The subsequent dark-current measurements were made with the samples still in the dewar. The dependence of CD upon bias at 180°K is given as the lower family of curves in Fig. 21. The values of CD at 10-V bias were now 3.9, 3.5, and 4.4×10^{-10} A/cm^2. The heat treatment has reduced the average CD at 10 V by a factor of about five. Although the shapes of the curves have changed somewhat, the average deviation from the average CD at 10 V is still less than 10%. It should be noted that the measurements of CD for the three samples after heat treatment could not be made in a single cooldown since the dewar is provided with only a single set of leads. After

completion of the measurements on a given sample, the dewar had to be warmed and opened; the sample lead had to be shifted, and the dewar had to be repumped and recooled before measurements on the next sample could be made. These results, together with others, indicate that the heterojunction properties are not extensively altered by repeated exposure to the atmosphere or to vacuum environment. This was not the case with at least some high-resistivity PbS photoconductive films [1].

A similar heat treatment of another sample, S21A2, raised the voltage at which the CD became 3×10^{-8} A/cm^2 from 2.6 to 14.5 V when the sample temperature was 90°K. Not all of the samples of the group of 20 have been heat-treated. The samples S21A3 have, after heat treatment, CD's small enough for device operation at temperatures as high as about 220°K.

The type of heat treatment that causes a reduction of the dark currents in cooled PbS-Si heterojunctions also produces changes in the magnitude of the photoresponse in the PbS wavelength range. This effect was first clearly recognized near the end of the present report period and consequently has not yet been extensively investigated. It has thus far been observed for two samples. Some features of the photoresponse behavior of earlier heterojunction samples can be accounted for in terms of heat treatment effects that were not clearly recognized at the time.

The changes in responsivity resulting from heat treatment will be summarized for sample S21A3c. Curves 1 and 2 of Fig. 22 give the absolute photovoltaic responsivity of the sample before treatment at room temperature and at ~140°K, respectively. Curves 3 and 4 represent the corresponding responsivities after the air bake given during the dark-current studies described above. The effect upon the room-temperature responsivity is small. The low-temperature responsivity, on the other hand, has increased by an average factor of about 16 over the PbS wavelength range following the heat treatment. The shape of the curves is relatively unchanged except for a slight enhancement of the long wavelength edge. The sign of the temperature coefficient of responsivity has reversed. This substantial change in the low-temperature responsivity must be due to a change in the current, of carriers excited in the PbS, which flows toward the junction. Since it is not likely that the probability of optical excitation of carriers has been altered by the heat treatment, the transport properties of the layer must have been changed.

Curve 5 of Fig. 22 gives the responsivity of cooled sample S20A6 which had been prepared on low-resistivity Si. Its peak responsivity is a factor of ten larger than that of S21A3c. It had, prior to measurement of its photoresponse, been given a much more severe heat treatment than S21A3c had received. Its response had not been measured prior to this treatment. It is not known at present whether its higher responsivity is due to this difference in heat treatment conditions or whether it is a consequence of the difference in resistivity of the Si. At any rate, this sample demonstrates that it is possible to obtain comparable responsivities in the Si and in the PbS wavelength ranges even though the PbS layer is thin and consequently has

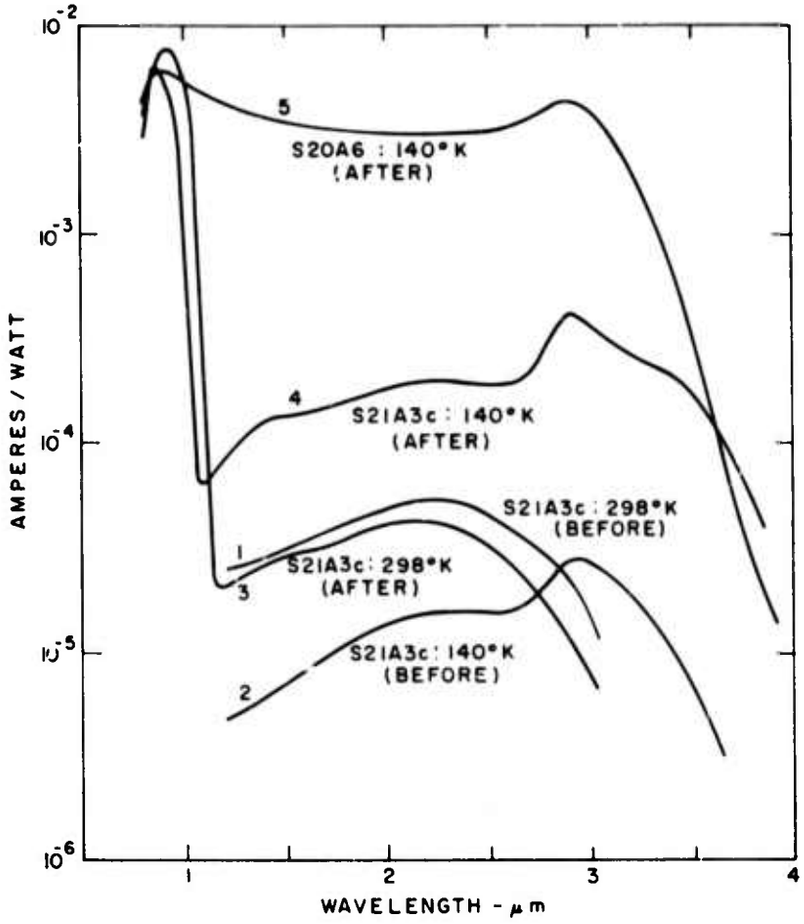

Figure 22. Photovoltaic absolute spectral responsivity curves of PbS-Si heterojunction S21A3c at 298°K and at 140°K before and after heat treatment. A response curve at 140°K for PbS-Si heterojunction S20A6 on ~0.1 ohm·cm n-type Si after a heat treatment is given for comparison.

relatively low absorption. It may be possible to improve the responsivity, in the PbS range, of low dark-current samples by suitable modification of the heat treatment conditions.

VIII. PLANS FOR THE NEXT PERIOD

A new mask set is being designed which will permit fabrication of IR CCD's with both Schottky-barrier detectors and PbS n-Si heterojunction detectors. It will be a linear array with aluminum and polysilicon gates to avoid gaps. This should result in improved transfer efficiency, better stability, and possibly better detection uniformity. Continued work with chips of the present design will be directed at more accurate measurement of detector uniformity, and demonstration of the mode of operation needed for imaging of low-contrast thermal scenes.

ABSTRACT OF PAPER PRESENTED AT THE DEVICE RESEARCH CONFERENCE, JUNE 1974, SANTA BARBARA, CALIFORNIA

An Infrared Sensitive, Charge-Coupled Imager*

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Princeton, New Jersey 08540

A charge-coupled imager sensitive to infrared light as far out as 3 μm has been fabricated and operated. It consists of a linear array of 64 Pd p-Si Schottky-barrier detectors adjacent to a three-phase charge-coupled shift register. We believe this to be the first time Schottky-barrier detectors have been used with a CCD. The design has a single level of metallization with gaps. A single transmission gate, when pulsed on, couples each detector to its associated shift register, thereby setting each barrier to a reverse bias determined by the potential applied to the transmission gate. Incident infrared light discharges the individual detectors during the detector exposure time. The charges transferred into the CCD shift register the next time the transmission gate is pulsed are transferred out sequentially by the charge-coupled shift register to produce the video signal. The output is obtained from a floating diffusion connected to an on-chip MOSFET.

The shift register has transfer losses as low as 5×10^{-4} per transfer as measured with an electrical input. Visible images could be sensed directly by illumination of the shift register through the gaps as well as through the unthinned substrate. Infrared images ($1.1\ \mu m < \lambda < 3.0\ \mu m$) were sensed by the Schottky-barrier detectors illuminated through the (transparent) substrate. The two imaging modes could be easily distinguished by their spectral sensitivities as well as by their response to changes in integration time, since the integration time for IR detection at the Schottky barrier and the integration time for intrinsic silicon absorption at the shift register can be adjusted independently. All IR measurements were made at liquid-nitrogen temperature. A scheme for observing low-contrast, thermal scenes without requiring the charge-coupled shift register to carry the entire background signal has been implemented in the design of this chip.

The results obtained with this imager and the problems of IR-CCD imagers will be discussed.

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*This work is being supported by the Defense Advanced Research Projects Agency and monitored by Air Force Cambridge Research Laboratories, Hanscom AFB, Massachusetts 01730.

REFERENCES

1. E. S. Kohn and M. L. Schultz, Charge-Coupled Scanned IR Imaging Sensors, Semiannual Technical Report, AFCRL-TR-74-0056, Contract No. F19628-73-C-0282, 14 January 1974.

SPECIAL NOTE ON ENERGY CONSERVATION

At the RCA David Sarnoff Research Center in Princeton, NJ, an Energy Conservation Committee has been working on the task of conserving energy since June 1973. By curtailing air conditioning during the warm season, by reducing interior lighting levels (more than 900 fluorescent tubes have been removed from offices and corridors) and eliminating exterior decorative lighting, and by shutting down nonessential machinery and equipment at night and on weekends, we have reduced our consumption of electrical energy substantially. In addition, throughout the heating season we achieved significant fuel savings by reducing interior temperatures to 68°F in all areas of the David Sarnoff Research Center during working hours and to 62 to 63°F during nights and weekends.

The payoff of energy conservation efforts at the Center has increased with each succeeding quarter. Total energy usage - in oil, gas, and electricity - for the last three months of 1973 was 22% less than for the same period in 1972; and, for the first quarter of 1974, this total was 27% less than that for the corresponding period in 1973. During the most recent quarter, combined oil and gas consumption was down by 28% and electricity by 20%, compared with the first quarter of 1973. For the heating season of October 1973 through March 1974, oil and gas savings totaled 49.2 billion BTU or 26% in comparison with usage in the heating season of a year ago. Data from the National Weather Service station at Trenton, NJ, indicates that these two heating seasons were quite comparable in terms of heating degree days, 4034 for 1973-4 and 4165 for 1972-3.

Likewise, our Industrial Relations Department has placed detailed Central New Jersey maps on strategically located bulletin boards to permit employees to identify home locations of other employees and to arrange for voluntary mutually agreeable car-pooling to and from work. Based upon our interpretation of statistics obtained from these maps, about 60 car-pooling arrangements have been consummated to date. The effects of this program are evident from the 10 to 15% reduction in the number of employee cars in our parking lots; as a result, the energy savings in reduced use of gasoline should be sizable.