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# MULTICS SECURITY EVALUATION VULNERABILITY ANALYSIS

ELECTRONIC SYSTEMS DIVISION

**JUNE 1974** 

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## 19. KEY WORDS

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## 20. ABSTRACT

certifiably secure and cannot be used in an open use multi-level system. However, the Multics security design principles are significantly better than other contemporary systems. Thus, Multics as implemented today, can be used in a benign Secret/Top Secret environment. In addition, Multics forms a base from which a certifiably secure open use multi-level system can be developed.

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This is Volume II of a 4 volume report prepared for the Air Force Data Services Center (AFDSC) by the information Systems Technology Applications Office, Deputy for Command and Management Systems, Electronic Systems Division (ESD/MCI). The entire report represents an evaluation and recommendation of the Honeywell Multics system carried out under Air Force Project 6917 from March 1972 to June 1973. Work proceeding after June 1973 is briefly summarized. Work described in this volume was performed by personnel at ESD/MCI with support from the MITRE Corporation. Computer facilities at the Rome Air Development Center and the Massachusetts Institute of Technology were used in the evaluation effort.

## PREFACE

# TABLE OF CONTENTS

| S  | ection   | Page   |
|----|--|--|
| 1  | INTRODUCTION   | 5  |
|    | 1.1 Status of Multi-level Security 1.2 Requirement for Multics Security Evaluation 1.3 Technical Requirements for Multi-level  | 5<br>5                                       |
|    | Security<br>1.3.1 Insecurity of Current Systems<br>1.3.2 Reference Monitor Concept<br>1.3.3 Hypothesis: Multics is "Secureable"<br>1.4 Sites Used  | 6<br>6<br>7                                  |
| 11 | I PULTICS SECURITY CONTROLS  | 8  |
|    |  | 9  |
|    | 2.1 Hardware Security Controls<br>2.1.1 Segmentation Hardware<br>2.1.2 Master Mode   | 9<br>9<br>10                                 |
|    | 2.2 Software Security Controls<br>2.2.1 Protection Rings<br>2.2.2 Access Control Lists<br>2.2.3 Protected Access Identification<br>2.2.4 Master Mode Conventions   | 12<br>12<br>13<br>15<br>15                   |
|    | 2.3 Procedural Security Controls<br>2.3.1 Enciphered Passwords<br>2.3.2 Login Audit Trail<br>2.3.3 Software Maintenance Procedures   | 15<br>15<br>16<br>16                         |
| 11 | I VULNERABILITY ANALYSIS   | 17   |
|    | 3.1 Approach Plan  | 17   |
|    | 3.2 Hardware Vulnerabilities<br>3.2.1 Random Failures<br>3.2.2 Execute Instruction Access Check Bypass<br>3.2.3 Preview of 6180 Hardware Vulnerabilities   | 17<br>17<br>20<br>22                         |
|    | <ul> <li>3.3 Software Vulnerabilities</li> <li>3.3.1 Insufficient Argument Validation</li> <li>3.3.2 Master Mode Transfer</li> <li>3.3.3 Unlocked Stack Base</li> <li>3.3.4 Preview of 6180 Software Vulnerabilities</li> <li>3.3.4.1 No Call Limiter Vulnerability</li> <li>3.3.4.2 SLT-KST Dual SDW Vulnerability</li> <li>3.3.4.3 Additional Vulnerabilities</li> </ul> | 22<br>22<br>25<br>30<br>36<br>37<br>37<br>38 |

# Section

| 3.4     | Procedural Vulnerabilities                              |            |
|---------|---|------------|
| 3       | .4.1 Dump and Patch Utilities                           | 38         |
|         | 3.4.1.1 Use of insufficient Argument                    | 38         |
|         | Valldation  | 39         |
|         | 3.4.1.2 Use of Unlocked Stack Base                      | 42         |
|         | 3.4.1.3 Generation of New SDW's                         | 42         |
| 3       | .4.2 Forging the Non-Forgeable                          |            |
|         | User identification                                     | 44         |
| 2       | .4.3 Accessing the Password File                        | 47         |
|         | 3.4.3.1 Minimal Value of the Password File              | 47         |
| 2       | 3.4.3.2 The Multics Password File                       | 47         |
| 3       | .4.4 Modifying Audit Trails<br>.4.5 Trap Door Insertion | 48         |
|         | 3.4.5.1 Classes of Trap Doors                           | 50         |
|         | 3.4.5.2 Example of a Trap Door in Multics               | 50         |
| 3       | .4.6 Preview of 6180 Procedural                         | 53         |
|         | Vulnerabilities   |            |
|         |   | 55         |
| 3.5     | Manpower and Computer Costs                             | 55         |
| IV CON  | CLUSIONS  | 58         |
| 4.1     | Multics is not Now Secure                               | 58         |
| 4.2     | Multics as a Base for a Secure System                   | 59         |
| 4       | .2.1 A System for a Benign Environment                  | 59         |
| •.      | .2.2 Long Term Open Secure System                       | 60         |
| Referen | nces  | 61         |
| Append  | l x   |            |
| A       | Subverter Listing                                       | <b>C</b> 1 |
|         |   | 64         |
| В       | Unlocked Stack Base Listing                             | 99         |
| С       | Trap Door in check\$device_name Listing                 | 115        |
| D       | Nump Utility Listing                                    | 131        |
| E       | Patch Utility Listing                                   | 138        |
| F       | Set Dates Utility Listing                               |            |
|         |   | 144        |
| Glossar | 'Y  | 149        |

Page

## LIST OF FIGURES

#### Figure Page 1 Segmentation Hardware 11 SDW Format 2 12 3 **Directory Hierarchy** 14 Execute Instruction Pypass 4 21 5 Insufficient Argument Validation 24 Master Mode Source Code 6 28 7 Master Mode Interpreted Object Code 28 Store With Master Mode Transfer 8 29 9 Unlocked Stack Base (Step 1) 34 Unlocked Stack Base (Step 2) 10 35 11 Dump/Patch Utility Using Insufficient Argument Validation 41 12 Dump/Patch Utility Using Unlocked Stack Base 43 13 Trap Door in check\$device\_name 54

## LIST OF TABLES

# TablePage1Subverter Test Attempts192Base Register Pairing313Cost Estimates57

## NOTATION

References in parentheses (2) are to footnotes. References in angle brackets (AND73) are to other documents listed at the end of this report.

4

#### SECTION I

#### INTRODUCTION

## 1.1 Status of Multi-Level Security

A major problem with computing systems in the military today is the lack of effective multi-level security controls. The term multi-level security controls means, in the most general case, those controls needed to several levels of classified material from process unclassified through compartmented top secret in 2 multi-processing multi-user computer system with simultaneous access to the system by users with differing levels of clearances. The lack of such effective controls in all of today's computer operating systems has led the military to operate computers in a closed environment in which systems are dedicated to the highest level of classified material and all users are required to be cleared to that level. Systems may be changed from level to level, but only after going through very time consuming clearing operations on all devices in the system. Such dedicated systems result in extremely inefficient equipment and manpower utilization and have often resulted in the acquisition of much more hardware than would otherwise be necessary. In addition, many operationai requirements cannot be met by dedicated systems because of the lack of information sharing. It has been estimated by the Electronic Systems Division (ESD) sponsored Computer Security Technology Panel (AND73) that these additional costs may amount to \$100,000,000 per year for the Air Force alone.

# 1.2 Requirement for Multics Security Evaluation

This evaluation of the security of the Multics system was performed under Project 6917, Program Flement to meet the requirements of the Air Force Data 64708F Services Center (AFDSC). AFDSC must provide responsive interactive time-shared computer services to users within Pentagon the at all classification levels from unclassified to top secret. AFDSC in particular did not wish to incur the expense of multiple computer systems nor the expense of encryption devices for remote terminals which would otherwise be processing only unclassified material. In a separate study completed in February 1972, the Information Systems Technology Applications Office, Electronic Systems Division (ESD/MCI) identified the Honeywell Multics system as a candidate to meet both

AFDSC's multi-level security requirements and highly responsive advanced interactive time-sharing requirements.

1.3 Technical Requirements for Multi-Level Security

The ESD-sponsored Computer Security Technology Planning Study (AND73) outlined the security weaknesses of present day computer systems and proposed a development plan to provide solutions based on current technology. A brief summary of the findings of the panel follows.

## 1.3.1 Insecurity of Current Systems

The internal controls of current computers repeatedly have been shown insecure through numerous penetration exercises on such systems as GCOS (AND71), WWMCCS GCOS (ING73, JTSA73), and IBP OS/360/370 (GCU172). This insecurity is a fundamental weakness of contemporary operating systems and cannot be corrected by "patches", "flx-ups", or "add-ons" to those systems. fundamental reimplementation using an Rather, a Integrated hardware/software design which considers security as a fundamental requirement is necessary. In particular, steps must be taken to ensure the correctness of the security related portions of the operating system. It is not sufficient to use a team of experts to "test" the security controls of a system. Such a "tiger team" can only show the existence of vulnerabilities but cannot prove their non-existence.

Unfortunately, the managers of successfully penetrated computer systems are very reluctant to permit release of the details of the penetrations. Thus, most reports of penetrations have severe (and often unjustified) distribution restrictions leaving very few documents in the public domain. Concealment of such penetrations does nothing to deter a sophisticated penetrator and can in fact impede technical interchange and delay the development of a proper solution. A system which contains vulnerabilities cannot be protected by keeping those vulnerabilities secret. It can only be protected by the constraining of physical access to the system.

## 1.3.2 Reference Monitor Concept

The FSD Computer Security Technology Panel introduced the concept of a "reference monitor". This reference monitor is that hardware/software combination which must monitor <u>all</u> references by any program to any

6

data anywhere in the system to ensure that the security rules are followed. Three conditions must be met to ensure the security of a system based on a reference monitor.

a. The monitor must be tamper proof.

b. The monitor must be invoked for <u>every</u> reference to data anywhere in the system.

c. The monitor must be small enough to be proven correct.

The stated design goals of contemporary systems such as GCOS or OS/360 are to meet the first requirement (albeit unsuccessfully). The second requirement is generally not met by contemporary systems since they usually include "bypasses" to permit special software to operate or must suspend the reference monitor to provide addressability for the operating system in exercising its service functions. The best known of these is the bypass in OS/360 for the IBM supplied service aid, IMASPZAP (SUPERZAP). (IBM70) Finally and most important, current operating systems are so large, so complex, and so monolithic that one cannot begin to attempt a formal proof or certification of their correct implementation.

1.3.3 Hypothesis: Multics is "Secureable"

The computer security technology panel identified the general class of descriptor driven processors (1) as extremely useful to the implementation of a reference monitor. Multics, as the most sophisticated of the descriptor-driven systems currently available, was hypothesized to be a potentially secureable system; that is, the Multics design was sufficiently well-organized and oriented towards security that the concept of a reference monitor could be implemented for Multics without fundamental changes to the facilities seen by Multics users. In particular, the Multics ring mechanism could protect the monitor from malicious or inadvertent tampering, and the Multics segmentation could

(1) Descriptor driven processors use some form of address translation through hardware interpretation of descriptor words or registers. Such systems include the Burroughs 6700, the Digital Equipment Corp. PPP-11/45, the Data General Nova 840, the DEC KI-10, the HIS 6180, the IBP 370/158 and 168, and several others not listed here.

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enforce monitor mediation on <u>every</u> reference to data. However, the question of certifiability had not as yet been addressed in Multics. Therefore the Multics vulnerability analysis described herein was undertaken to:

a. Examine Multics for potential vulnerabilities.

b. Identify whether a reference monitor was practical for Multics.

c. Identify potential interim enhancements to Multics to provide security in a benign (restricted access) environment.

d. Determine the scope and dimension of a certification effort.

1.4 Sites Used

The vulnerability analysis described herein was carried out on the HIS 645 Multics Systems installed at the Massachusetts Institute of Technology and at the Rome Air Development Center. As the HIS 6180, the new Multics processor, was not available at the time of this study. This report will describe results of analysis of the HIS 645 only. Since the completion of the analysis, work has started on an evaluation of the security controls of Multics on the HIS 6180. Preliminary results of the work on the HIS 6180 are very briefly summarized in this report, to provide an understanding of the value of the evaluation of the HIS 645 in the context of the new hardware environment.

#### SECTION II

2

#### MULTICS SECURITY CONTROLS

This section provides a brief overview of the basic Multics security controls to provide necessary background for the discussion of the vulnerability analysis. However, a rather thorough knowledge of the Multics implementation is assumed throughout the rest of this document. More complete background material may be found in Lipner (LIP74), Saltzer (SAL73), Organick (ORG72), and the Multics Programmers' Manual (MPM73).

The basic security controls of Multics fall into three major areas: hardware controls, software controls, and procedural controls. This overview will touch briefly on each of these areas.

2.1 Hardware Security Controls

2.1.1 Segmentation Hardware

The most fundamental security controls in the HIS 645 Multics are found in the segmentation hardware. The basic instruction set of the 645 can directly address up to 256K (2) distinct segments (3) at any one time, each segment being up to 256K words long. (4) Segments are broken up into 1K word pages (5) which can be moved between primary and secondary storage by software, creating a very large virtual memory. However, we will not treat paging throughout most of this evaluation as it is transparent to security. Paging must be implemented

(2) 1K = 1024 units.

(3) Current software table sizes restrict a process to about 1000 segments. However, by increasing these table sizes, the full hardware potential may be used.

(4) The 645 software restricted segments to 64K words for efficiency reasons.

(5) The 645 hardware also supports 64 word pages which were not used. The 6180 supports only a single page size which can be varied by field modification from 64 words to 4096 words. Initially, a size of 1024 words is being used. The supervisors on both the 645 and 6180 use unpaged segments of length 0 mod 64. correctly in a secure system. However, bugs in page control are generally difficult to exploit in a penetration, because the user has little or no control over paging operations.

Segments are accessed by the 645 CPU through segment descriptor words (SDW's) that are stored in the descriptor segment (DSEG). (See Figure 1.) To access segment N, the 645 CPU uses a processor register, the descriptor segment base register (DBR), to find the DSFG. It then accesses the Nth SDW in the DSEG to obtain the address of the segment and the access rights currently in force on that segment for the current user.

Each SDW contains the absolute address of the page table for the segment and the access control information. (See Figure 2.) The last 6 bits of the SDW determine the access rights to the segment - read, execute, write, etc. (6) Using these access control bits, the supervisor can protect the descriptor segment from unauthorized modification by denying access in the SDW for the descriptor segment.

2.1.2 Master Mode

To protect against unauthorized modification of the DBR the processor operates in one of two states master mode and slave mode. In master mode any instruction may be executed and access control checks are inhibited. (7) In slave mode, certain instructions including those which modify the DBP are inhibited. Master mode procedure segments are controlled by the class field in the SDW. Slave mode procedures may transfer to master mode procedure only through word zero of the master mode procedure to prevent unrestricted invocation of privileged programs. It is then the responsibility of the master mode software to protect itself from malicious calls by placing suitable protective routines beginning at location zero.

(6) A more detailed description of the SDN format may be found in the 645 processor manual <AGE71>.

(7) The counterpart of master mode on the HIS 6180 called privileged mode does not inhibit access control checking.









## Figure 2. SDW Format

## 2.2 Software Security Controls

The most outstanding feature of the Multics security controls is that they operate on a basis of "form" rather than the classical basis of "content". That is to say, the Multics controls are based on operations on a uniform population of well defined objects, as opposed to the classical controls which rely on anticipating all possible types of accesses and make security essentially a battle of wits.

2.2.1 Protection Rings

The primary software security control on the 645 Multics system is the ring mechanism. It was originally postulated as desirable to extend the traditional master/slave mode relationship of conventional machines to permit layering within the supervisor and within user code (see Graham (GPA68>). Fight concentric rings of protection, numbered 0 - 7, are defined with higher numbered rings having less privilege than lower numbered rings, and with ring 0 containing the "hardcore" supervisor. (8) Unfortunately, the 645 CPU does not implement protection rings in hardware. (9) Therefore, the eight protection rings are implemented by providing eight descriptor segments for each process (user), one descriptor segment per ring. Special fault codes are placed in those SDW's which can be used for cross-ring transfers so that ring 0 software can intervene and accomplish the descriptor segment swap between the calling and called rings.

## 2.2.2 Access Control Lists

Segments in Multics are stored in a hierarchy directories. A directory is a special type of segment of that is not directly accessible to the user and provides a place to store names and other information about subordinate segments and directories. Each segment and directory has an access control list (ACL) in its parent directory entry controlling who may read (r), write (w), or execute (e) the segment or obtain status (s) of, modify (m) entries in, or append (a) entries to a directory. For example in Figure 3, the user Jones. Druid has read permission to segment ALPHA and has null access to segment However, Jones. Druid has modify permission to BETA. directory DELTA, so he can give himself access to segment Jones Druid cannot give himself write access to BETA. segment ALPHA, because he does not have modify permission to directory GAMMA. In turn, the right to modify the access control lists of GAMMA and DELTA is controlled by the access control list of directory EPSILON, stored in the parent of EPSILON. Access control security checks for segments are enforced by the ring 0 software by setting the appropriate bits in the SDW at the time that a user attempts to add a segment to his address space.

(8) The original design called for 64 rings, but this was reduced to 8 in 1971.

(9) One of the primary enhancements of the HIS 6180 is the addition of ring hardware (SCHR72) and a consequent elimination of the need for master mode procedures in the user ring.





**Directory Hierarchy** 

## 2.2.3 Protected Access Identification

In order to do access checking, the ring O software must have a protected, non-forgeable identification of a user to compare with the ACL entries. This ID is established when a user signs on to Multics and is stored in the process data segment (PDS) which is accessible only in ring O or in master mode, so that the user may not tamper with the data stored in the PDS.

## 2.2.4 Master Mode Conventions

By convention, to protect master mode software, the original design specified that master mode procedures were not to be used outside ring 0. If the master mode procedure ran in the user ring, the master mode procedure itself would be forced to play the endless game of wits of the classical supervisor call. The master mode procedure would have to include code to check for all possible combinations of input arguments, rather than relying on a fundamental set of argument independent security controls. As an aid (or perhaps hindrance) to playing the game of wits, each master mode procedure must have a master mode pseudo-operation code assembled into location 0. The master mode pseudo-operation generates code to test an index register for a value corresponding to an entry point in the segment. If the index register is invalid, the master mode pseudo-operation code saves the registers for debugging and brings the system down.

2.3 Procedural Security Controls

## 2.3.1 Enclphered Passwords

When a user logs in to Multics, he types a password as his primary authentication. Of course, the access control list of the password file denies access to regular users of the system. In addition, as a protection against loss of a system dump which could contain the password file, all passwords are stored in a "non-invertible" cipher form. When a user types his password, it is enciphered and compared with the stored enciphered version for validity. Clear text passwords are stored nowhere in the system.

## 2.3.2 Login Audit Trail

Each login and logout is carefully audited to check for attempts to guess valid user passwords. In addition, each user is informed of the date, time and terminal identification (if any) of last login to detect past compromises of the user's access rights. Further, the user is told the number of times his password has been given incorrectly since its last correct use.

## 2.3.3 Software Haintenance Procedures

The maintenance of the Multics software is carried out online on a dial-up Multics facility. A systems programmer prepares and nominally debugs his software for installation. He then submits his software to a library installer who copies and recompiles the source in a protected directory. The library installer then checks out the new software prior to installing it in the system source and object libraries. Ring 0 software is stored on a system tape that is reloaded into the system each time it is brought up. However, new system tapes are generated from online copies of the ring O software. The system libraries are protected against modification by the standard ACL mechanism. In addition, the library installers periodically check the date/time las: modified of all segments in the library in an attempt to detect unauthorized modifications.

## SECTION III

## VULNERABILITY ANALYSIS

## 3.1 Approach Plan

It was hypothesized that although the fundamental design characteristics of Multics were sound, the implementation was carried out on an ad hoc basis and had security weaknesses in each of the three areas of security controls described in Section II - hardware, software, and procedures.

The analysis was to be carried out on a very limited basis with a less than one-half man month per month level of effort. Due to the manpower restrictions, a goal of one vulnerability per security control area was set. The procedure followed was to postulate a weakness in a general area, verify the weakness in the system, experiment with the weakness on the Rome Air Development Center (RADC) installation, and finally, using the resulting debugged penetration approach, exploit the weakness on the MIT installation.

An attempt was to be made to operate with the same type of ground rules under which a real agent would operate. That is, with each penetration, an attempt would be made to extract or modify sensitive system data without detection by the system maintenance or administrative personnel.

Several exploitations were successfully investigated. These included changing access fields in SDW's, changing protected identities in the PDS, inserting trap doors into the system libraries, and accessing the system password file.

3.2 Hardware Vulnerabilities

3.2.1 Random Failures

One area of significant concern in a system processing multi-level classified material is that of random hardware failures. As described in Section 2.1.1, the fundamental security of the system is dependent on the correct operation of the segmentation hardware. If this hardware is prone to error, potential security vulnerabilities become a significant problem. To attempt a gross measure of the rate of security sensitive component failure, a procedure called the "subverter" was written to sample the security sensitive hardware on a frequent basis, testing for component failures which could compromise the security controls. The subverter was run in the background of an interactive process. Once each minute, the subverter received a timer interrupt and performed one test from the list described below. Assuming the test did not successfully violate security rules, the subverter would for one minute before trying the next test. A listing of the subverter may be found in Appendix A.

The subverter was run for 1100 hours in a one year period on the MIT 645 system. The number of times each test was attempted is shown in Table 1. During the 1100 operating hours, no security sensitive hardware component failures were detected, indicating good reliability for the 645 security hardware. However, two interesting anomalies were discovered in the tests. First, one undocumented instruction (octal 471) was discovered on the 645. Experimentation indicated that the new instruction had no obvious impact on security, but merely seemed to store some internal register of no particular interest. The second anomaly was a design described in Section 3.2.2.

## TABLE 1

# Subverter Test Attempts

# 1100 Cperating Hours

## Test Name

C1 .....

# Attempts

| 2. Sterr Associative Memory   |      |  |
|---|------|--|
| 2. Store Control Unit   | 3526 |  |
| 3. Load Timer Register  | 3466 |  |
| 4. Load Decenter  | 3444 |  |
| 4. Load Descriptor Base Register  | 3422 |  |
| TO COLE DESCEIDEOF Baco Desta   |      |  |
| TH MANNELL I/II PASAAT  | 3403 |  |
| /. Delay Until Internet Standt  | 3378 |  |
| The second remove contraction Martin a  | 3359 |  |
|   | 3344 |  |
| 9. Set Memory Controller Mask Register<br>10. Set Memory Controller Mask Register   | 3328 |  |
| 10. Set Memory Controller Hask Register<br>11. Load Alarm Clock                     | 3309 |  |
|   | 3289 |  |
| 12. Load Associative Hemory   | 3259 |  |
| 13. Store Associative Memory  |      |  |
| ATT NESLOPE CONTROL HALA  | 3236 |  |
| 12. NO Read Permission  | 3219 |  |
| 10. NO Write Permission   | 3148 |  |
| 17. XED - No Read Permission  | 3131 |  |
| 18. XED - No Write Permission   | 3113 |  |
| 19. Tally Ward With Permission  | 3098 |  |
| 19. Taily Word Without Write Permission<br>20. Bounds Fault (Church Vite Permission |      |  |
|   | 3083 |  |
| 41. Bounds Fault Saur   | 2398 |  |
| 22. Illegal Opcodes   | 2368 |  |
|   | 2108 |  |
|   |      |  |

Tests 1-14 are tests of master mode instructions. Tests 15 and 16 attempt simple violation of read and write permission as set on segment ACL's. Tests 17 and 18 are identical to 15 and 16 except that the faulting instructions are reached from an Execute Double instruction rather than normal instruction flow. Test 19 attempts to increment a tally word that is in a segment without write permission. Tests 20 and 21 take out of supervisor to grow new page tables for them. Test 22 attempts execution of all the instructions marked illegal

## 3.2.2 Execute Instruction Access Check Bypass

While experimenting with the hardware subverter, a sequence of code (10) was observed which would cause the hardware of the 645 to bypass access checking. Specifically, the execute instruction in certain cases described below would permit the executed instruction to access a segment for reading or writing without the corresponding permissions in the SDW.

This vulnerability occurred when the execute instruction was in certain restricted locations of a segment with at least read-execute (re) permission. (See Figure 4.) The execute instruction then referenced an object instruction in word zero of a second segment with at least R permission. The object instruction indirected through an ITS pointer in the first segment to access a word for reading or writing in a third segment. The third segment was required to be "active"; that is, to have an SDW pointing to a valid page table for the segment. If all these conditions were met <u>precisely</u>, the access control fields in the SDW of the third segment would be ignored and the object instruction permitted to complete without access checks.

The exact layout of instructions and indirect words was crucial. For example, if the object instruction used a base register rather than indirecting through the segment containing the execute instruction (i.e., staq apl0 rather than staq 0,\*), then the access checks were done properly. Unfortunately, a complete schematic of the 045 was not available to determine the exact cause of the bypass. In informal communications with Honeywell, it was indicated that the error was introduced in a field medification to the 645 at MIT and was then made to all processors at all other sites.

This hardware bug represents a violation of one of the most fundamental rules of the Multics design the checking of <u>every</u> reference to a segment by the hardware. This bug was not caused by fundamental design problems. Rather, it was caused by carelessness by the hardware engineering personnel.

(10) The subverter was designed to test sequences of code in which single failures could lead to security problems. Some of these sequences exercised relatively complex and infrequently used instruction modifications which experience had shown were prone to error.





Figure 4. Execute Instruction Bypass

No attempt was made to make a complete search for additional hardware design burs, as this would have required logic diagrams for the S45. It was sufficient for this effort to demonstrate one vulnerability in this area.

# 3.2.3 Preview of 6180 Hardware Vulnerabilities

While no detailed look has been taken at the issue of hardware vulnerabilities on the 6180, the very first login of an ESD analyst to the 6180 inadvertently discovered a hardware vulnerability that crashed the system. The vulnerability was found in the Tally Word Without Write Permission test of the subverter. In this test, when the 6180 processor encountered the tally word without write permission, it signalled a "trouble" fault rather than an "access violation" fault. The "trouble" fault is normally signalled only when a fault occurs during the signalling of a fault. Upon encountering a "trouble" fault, the software normally brings the system down.

It should be noted that the HIS 6180 contains very new and complex hardware that, as of this nublication, has not been completely "shaken down". Thus, Honeywell still quite reasonably expects to find hardware problems. However, the inadequacy of "testing" for security vulnerabilities applies equally well to hardware as to software. Simply "shaking down" the hardware cannot find all the possible vulnerabilities.

3.3 Software Vulnerabilities

Although the approach plan for the vulnerability analysis only called for locating one example of each class of vulnerability, three software vulnerabilities were identified as shown below. Again, the search was neither exhaustive nor systematic.

3.3.1 Insufficient Argument Validation

Because the 645 Multics system must simulate protection rings in software, there is no direct hardware validation of arguments passed in a subroutine call from a less privileged ring to a more privileged ring. Some form of validation is required, because a malicious user could call a ring 0 routine that stores information through a user supplied pointer. If the malicious user supplied a pointer to data to which ring 0 had write permission but to which the user ring did not, ring 0 could be "tricked" into causing a security violation.

To provide validation, the 645 software ring crossing mechanism requires all gate segments (11) to declare to the "gatekeeper" the following information:

- 1. number of arguments expected
- 2. data type of each arguments
- 3. access requirements for each argumentread only or read/write.

This information is stored by convention in specified locations within the gate segment. (12) The "gatekeeper" invokes an argument validation routine that inspects the argument list being passed to the gate to ensure that the declared requirements are met. If any test fails, the argument validator aborts the call and signals the condition "gate\_error" in the calling ring.

In February 1973, a vulnerability was identified in the argument validator that would permit the "fooling" of ring 0 programs. The argument validator's algorithm to validate read or read/write permission was as follows: First copy the argument list into ring 0 to prevent modification of the argument list by a process running on another CPU in the system while the first process is in ring 0 and has completed argument validation. Next, force indirection through each argument pointer to obtain the segment in the calling ring's descriptor segment to check for read or write permission.

The vulnerability is as follows: (See figure 5.) An argument pointer supplied by the user is constructed to contain an IDC modifier (increment address, decrement tally, and continue) that causes the first reference through the indirect chain to address a valid argument. This first reference is the one made by the

(11) A gate segment is a segment used to cross rings. It is identified by R2 and R3 of its ring brackets R1, R2, R3 being different. See Organick (ORG72) for a detailed description of ring brackets.

(12) For the convenience of authors of gates, a special "gate language" and "gate compiler" are provided to generate properly formatted gates. Using this language, the author of the gate can declare the data type and access requirement of each argument.





argument validator. The reference through the IPC modifier increments the address field of the taily word causing it to point to a different indirect word which in turn points to a different ITS pointer which points to an argument which is writable in ring 0 only. The second reference through this modified indirect chain is made by the ring 0 program which proceeds to write data where it shouldn't. (13)

This vulnerability resulted from violation of a basic rule of the Multics design - that all arguments to a more privileged ring be validated. The problem was not in the fundamental design - the concept of a software argument validator is sound given the lack of ring hardware. The problem was an ad hoc implementation of that argument validator which overlooked a class of argument pointers.

Independently, a change was made to the PIT system which fixed this vulnerability in February 1973. The presence and exploitability of the vulnerability were verified on the PADC Multics which had not been updated to the version running at MIT. The method of correction chosen by MIT was rather "brute force." The argument validator was changed to require the modifier in the second word of each argument pointer always to be zero. This requirement solves the specific problem of the IDC modifier, but not the general problem of argument validation.

#### 3.5.2 Master Mode Transfer

As described in Sections 2.1.2 and 2.2.4, the 545 CPU has a master mode in which privileged instructions may be executed and in which access checking is inhibited although address translation through segment and page tables is retained. (14) The original design of the fultics protection rings called for master mode code to be

(13) Depending on the actual number of references made, the malicious user need only vary the number of indirect words pointing to legal and illegal arguments. We have assumed for simplicity here that the validator and the ring 0 program make only one reference each.

(14) The 645 also has an absolute mode in which all addresses are absolute core addresses rather than being translated by the segmentation bardware. This mode is used only to initialize the system.

0

restricted to ring 0 by convention. (15) This convention caused the fault handling mechanism to be excessively expensive due to the necessity of switching from the user ring into ring 0 and out again using the full software ring crossing mechanism. It was therefore proposed and implemented that the <u>signaller</u>, the module responsible for processing faults to be signalled to the user, (16) be permitted to run in the user ring to speed up fault processing. The signaller is a master mode procedure, hecause it must execute the RCU (<u>Restore Control Unit</u>) instruction to restart a process after a fault.

The decision to move the signaller to the user ring was not felt to be a security problem by the system designers, because master mode procedures could only be entered at word zero. The signaller would be assembled with the master mode pseudo-operation code at word zero to protect it from any malicious attempt by a user to execute an arbitrary sequence of instructions within the procedure. It was also proposed, although never implemented, that the code of master mode procedures in the user ring be specially audited. However as we shall see in Section 3.4.4, auditing does not guarantee victory penetrator. Auditing cannot be used to make up for fundamental security weaknesses.

It was postulated in the ESD/MCI vulnerability analysis that master mode procedures in the user ring represent a fundamental violation of the Multics security concept. Violating this concept moves the security controls from the basic hardware/software mechanism to the cleverness of the systems programmer who, being human, makes mistakes and commits oversights. The master mode rules for "sufficient" security checks. In fact, upon close examination of the signaller, this hypothesis was

(15) This convention is enforced on the 6180. Privileged mode (the 6180 analogy to the 645 master mode) only has effect in ring 0. Outside ring 0, the hardware ignores the privileged mode bit.

(16) The signaller processed such faults as "zerodivide" and access violation which are signalled to the user. Page faults and segment faults which the user never sees are processed elsewhere in ring 0. The master mode pseudo-operation code was designed only to protect master mode procedures from random calls within ring 0. It was not designed to withstand the attack of a malicious user, but only to operate in the relatively benign environment of ring 0.

The master mode program shown in Figure 6 assembles into the interpreted object code shown in Figure 7. The master mode procedure can only be entered at location zero. (17) By convention, the n entry points to the procedure are numbered from 0 to n-1. The number of the desired entry point must be in index register zero at the time of the call. The first two instructions in the master mode sequence check to ensure that index register zero is in bounds. If it is, the transfer on no carry (tnc) instruction indirects through the transfer vector to the proper entry. If index register zero is out of bounds, the processor registers are saved for debugging and control is transferred to "mxerror," a routine to crash the system because of an unrecoverable error.

This transfer to mxerror is the most obvious vulnerauility. By moving the signaller into the user ring, the designers allowed a user to arbitrarily crash the system by transferring to signaller10 with a bad value in index register zero. This vulnerability is not too serious, since it does not compromise information and could be repaired by changing mxerror to handle the error, rather than crashing the system.

However, there is a much nore subtle and dangerous vulnerability here. The tra 1p112,\* instruction that is used to call mxerror believes that the lp register points to the linkage section of the signaller, which it should if the call were legitimate. However, a malicious user may set the 1p register to point wherever he wishes, permitting him to transfer to an arbitrary location while the CPU is still in master mode. The key is the transfer in master mode, because this permits a transfer to an arbitrary location within another master mode procedure without access checking and without the restriction of entering at word zero. Thus, the penetrator need only find a convenient store instruction to be able to write into his own descriptor segment, for example. Figure a shows the use of a sta bplu instruction to change the contents of an SDW illegally.

(17) This restriction is enforced by hardware described in Section 2.1.2.



name master\_test mastermode entry a entry b code ... code ... end

a:

b:

Figure 6. Master Mode Source Code

Cmp xU 2, du "call in bounds? transfer\_vector,0 "Yes, go to entry tnc "Illegal call here stb splu "save registers sreg sp|10 eapap arglist "set up call stcd sp|24 "1p]12 points to mxerror tra 1p|12,\* a: code . . . b: code . . . transfer\_vector: tra а tra Ь end

Figure 7. Master Mode Interpreted Object Code

28



Figure 8. Store with Master Mode Transfer

29

There is one major difficulty in exploiting this vulnerability. The instruction to which control is transferred must be chosen with extreme care. The instructions immediately following the store must provide some orderly means of returning control to the malicious user without doing uncontrolled damage to the system. If a crucial data base is garbled, the system will crash leaving a core dump which could incriminate the penetrator.

This vulnerability was identified by ESD/HCI in June 1972. An attempt to use the vulnerability led to a system crash for the following reason: Due to an obsolete listing of the signaller, the transfer was made to an LDBR (Load Descriptor Base Register) instruction instead of the expected store instruction. The DBR was loaded with a garbled value, and the system promptly crashed. The system maintenance personnel, being unaware of the presence of an active penetration, attributed the crash to a disk read error.

The Master Mode Transfer vulnerahility resulted from a violation of the fundamental rule that master mode code shall not he executed outside ring 0. The violation was not made maliciously by the system implementors. Rather it occurs because of the interaction of two seemingly independent events: the ability to transfer via the 1p without the system being able to check the validity of the 1p setting, and the ability for that transfer to be to master mode code. The separation of these events made the recognition of the problem unlikely during implementation.

3.3.3 Unlocked Stack Base

The G45 CPU has eight 18-bit registers that are used for inter-segment references. Control bits are associated with each register to allow it to be paired with another register as a word number-segment number pair. In addition, each register has a lock bit, settable only in master mode, which protects its contents from modification. By convention, the eight registers are named and paired as shown in Table 2.

## TABLE 2

# Base Register Pairing

| lumber | llame | Use              | Pairing        |
|--------|-------|------------------|----------------|
| 0      | ap    | argument pointer | paired with ab |
| 1      | ab    | argument base    | unpaired       |
| 2      | bp    | unassigned       | paired with bb |
| 3      | bb    | unassigned       | unpaired       |
| 4      | lp    | linkage pointer  | paired with 1b |
| 5      | 16    | linkage base     | unpaired       |
| 6      | sp    | stack pointer    | paired with sh |
| 7      | sh    | stack base       | unpaired       |
|        |       |                  |                |

During the early design of the Hultics operating system, it was felt that the ring 0 code could be simplified if the stack base (sb) register were locked, that is, could only be modified in master mode. The sh contained the segment number of the user stack which was guaranteed to be writeable. If the sb were locked, then the ring 0 fault and interrupt handlers could have convenient areas in which to store stack frames. After Hultics had been released to users at MIT, it was realized that locking the stack base unnecessarily constrained language designers. Some languages would be extremely difficult to implement without the capability of quickly and easily switching between stack segments. Therefore, the system was modified to no longer lock the stack base.

When the stack base was unlocked, it was realized that there was code scattered throughout ring 0 which assumed that the sb always pointed to the stack. Therefore, ring 0 was "audited" for all code which depended on the locked stack base. However, the audit was never completed and the few dependencies identified were in general not repaired until much later.

As part of the vulnerability analysis, it was hypothesized that such an audit for unlocked stack base problems was presumably incomplete. The ring 0 code is so large that a subtle dependency on the sh register could



easily slip by an auditor's notice. This, in fact proved to be true as shown below:

Section 3.3.2 showed that the master mode pseudo-operation code believed the value in the 1p register and transferred through it. Figure 7 shows that the master mode pseudo-operation code also depends on the sb pointing to a writeable stack segment. When an illegal master mode call is made, the registers are saved on the stack prior to calling "mxerror" to crash the system. This code was designed prior to the unlocking of the stack base and was not detected in the system audit. The malicious user need only set the sp-sb pair to point anywhere to perform an illegal store of the registers with master mode privileges.

The exploitation of the unlocked stack base vulnerability was a two step procedure. The master mode pseudo-operation code stored all the processor registers in an area over 20 words long. This area was far too large for use in a system penetration in which at most one or two words are modified to give the agent the privileges However, storing a large number of words he requires. could be very useful to install a "trap door" in the system -- that is a sequence of code which when properly invoked provides the penetrator with the needed tools to subvert the system. Such a "trap door" must be well hidden to avoid accidental discovery by the system maintenance personnel.

It was noted that the linkage segments of several of the ring 0 master mode procedures were preserved as separate segments rather than being combined in a single linkage segment. Further, these linkage segments were themselves master mode procedures. Thus, segments such as signaller, fim, and emergency\_shutdown corresponding master mode linkare segments had signaller.link, fim.link, and emergency\_shutdown.link. Linkage segments contain a great deal of information used only by the binder and therefore contain a great deal of extraneous information in ring 0. For this reason, a master mode linkage segment is an ideal place to conceal a "trap door." There is a master mode procedure called emergency\_shutdown that is used to place the system in a consistent state in the event of a crash. Since emergency\_shutdown is used only at the time of a system crash, its linkage segment, emergency\_shutdown.link, was chosen to be used for the "trap door".
The first step of the exploitation of the unlocked stack base is shown in Figure 9. (18) The signaller is entered at location 0 with an invalid index register 0. The stack pointer is set to point to an area of extraneous storage in emergency\_shutdown.link. The An register contains a two instruction "trap door" which when executed in master mode can load or store any 36-bit word in the system. The index registers could be used to hold a longer "trap door"; however, in this case the xed bpl0, tra bpl2 sequence is sufficient. The base registers, index registers, and AQ register are stored into emergency\_shutdown.link, thus laying the "trap door". Finally a transfer is made indirect through lpl12 which has been pre-set as a return pointer. (19)

Step two of the exploitation of the unlocked stack base is shown in Figure 10. The calling program sets the hp register to point to the desired instruction pair and transfers to word zero of the signaller with an invalid value in index register 0. The signaller saves its registers on the user's stack frame since the sp has not been changed. It then transfers indirect through Ip112 which has been set to point to the "trap door" in emergency\_shutdown.link. The first instruction of the "trap door" is an execute double (XED) which permits the user (penetration agent) to specify any two arbitrary instructions to be executed in master mode. In this example, the instruction pair loads the ? register from a word in the stack frame (20) and then stores indirect through a pointer in the stack to an SD!' in the descriptor segment. The second instruction in the "trap door" transfers back to the calling program, and the penetrator may go about his business.

(18) Listings of the code used to exploit this vulnerability are found in Appendix B.

(19) This transfer uses the Master Fode Transfer vulnerability to return. This is done primarily for convenience. The fundamental vulnerability is the storing through the sp register. Without the Master Hode Transfer, exploitation of the Unlocked Stack Base would have been more difficult, although far from impossible.

(20) It should be noted that only step one changed the value of the sp. In step two, it is very useful to leave the sp pointing to a valid stack frame.



33



# **Setup Conditions**

| AQ register   | := xed bp   0; tra bp   2  |
|---------------|--|
| Index 0       | :1   |
| sp<br>Ip   12 | <pre>: = address (unused storage in emergency_shutdown.link) : = address (return location)</pre> |

Figure 9. Unlocked Stack Base (Step 1)





The "trap door" inserted In emergency\_shutdown.link remained in the system until the system was reinitialized. (21) At initialization time, a fresh copy of all ring zero segments is read in from the system tape erasing the "trap door". Since system Initializations least once per day, occur at the penetrator must execute step one before each of his working sessions. Step two is then executed each time he wishes to access or modify some word in the system.

The unlocked stack base vulnerability was identified in June 1972 with the Master Mode Transfer Vulnerability. It was developed and used at the RADC site in September 1972 without a single system crash. In October 1972, the code was transferred to the MIT site. Due to lack of good telecommunications between the two sites, the code was manually retyped into the MIT system. A typing mistake was made that caused the word to be stored into the SDW to always be zero (See Figure 10). When an attempt was made to set slave access-data in the SDW of the descriptor segment itself, (22) the SDU of the descriptor segment was set to zero causing the system to crash at the next LDBR instruction or segment initiation. The bug was recognized and corrected immediately, but later in the day, a second crash occurred when the SDW for the ring zero segment fim (the fault intercept module) was patched to slave access-write permit-data rather than slave access-write permit-slave procedure. In more straightforward terms, the SDN was set to read-write rather than read-write-execute. Therefore, when the system next attempted to execute the fim it took a no-execute permission fault and tried to execute the fim, thus entering an infinite loop crashing the system.

3.3.4 Preview of 6180 Software Vulnerabilities

The 6180 hardware implementation of rings renders invalid the attacks described here on the 645. This is not to say, however, that the 6180 l'ultics is free of vulnerabilities. A cursory examination of the 6180 software has revealed the existence of several software vulnerabilities, any one of which can be used to access

(21) See Section 3.4.5 for more lasting "trap doors".

(22) The attempt here was to dump the contents of the descriptor segment on the terminal. The user does not normally have read permission to his own descriptor segment.

any information in the system. These vulnerabilities were identified with comparable levels of effort to those shown in Section 3.5.

#### 3.3.4.1 No Call Limiter Vulnerability

The first vulnerability is the No Call Limiter vulnerability. This vulnerability was caused by the call limiter not being set on gate segments, allowing the user to transfer to any instruction within the gate rather than to just an entry transfer vector. This vulnerability gives the penetrator the same capabilities as the Master Mode Transfer vulnerability.

## 3.3.4.2 SLT-KST Dual SDW Vulnerability

The second vulnerability is the SLT-KST Dual SDW vulnerability. When a user process was created on the 645, separate descriptor segments were created for each ring, with the ring O SDW's being copied from the segment loading table (SLT). The ring 0 descriptor segment was essentially a copy of the SLT for ring O segments. The ring 4 descriptor segment zeroed out most SDW's for ring 0 segments. Non-ring 0 SDW's were added to both the ring 0 and ring 4 descriptor segments from the Known Segment Table (KST) during segment initiation. Upon conversion to the 6180, the separate descriptor segments for each ring were merged into one descriptor segment containing ring brackets in each SDW (IPC73). The ring 0 SDW's were still taken from the SLT and the non-ring O SDW's from the KST as on the 645.

The system contains several gates from ring 4 into ring 0 of varying levels of privilege. The least privileged gate is called hcs\_ and may be used by all users in ring 4. The most privileged gate is called hphcs\_ and may only be called by system administration personnel. The gate hphcs\_ contains routines to shut the system down, access any segment in the system, and patch ring 0 data bases. If a user attempts to call hphcs in the normal fashion, hphcs\_ is entered into the KST, an SDN is assigned, and access rights are determined from the access control list stored in hphcs\_'s parent directory. Since most users would not be on the access control list of hphcs\_, access would be denied. Ring 0 gates, however, also have a second segment number assigned from the segment loading table (SLT). This duplication posed no problem on the 645, since SLT SDW's were valid only in the ring 0 descriptor segment. However on the 6180, the KST SDW for hphcs\_ would be null access ring brackets 0,0,5,

but the SLT SDW would read-execute (re) access, ring brackets 0,0,5. Therefore, the penetrator need only transfer to the appropriate absolute segment number rather than using dynamic linking to gain access to any hphcs\_ capability. This vulnerability was considerably easier to use than any of the others and was carried through identification, confirmation, and exploitation in less than 5 man-hours total (See Section 3.5).

## 3.3.4.3 Additional Vulnerabilities

The above mentioned 6180 vulnerabilities have been identified and repaired by Honeywell. The capabilities of the SLT-KST Dual SDW vulnerability were demonstrated to Honeywell on 14 September 1973 in the form of an illegal message to the operator's console at the 6180 site in the Honeywell plant in Phoenix, Arizona. Honeywell did not identify the cause of the vulnerability until March 1974 and installed a fix in Hultics System 23.6. As of the time of this publication, additional vulnerabilities have been identified but at this time have not been developed into a demonstration.

3.4 Procedural Vulnerabilities

This section describes the exploitation by a remote user of several classes of procedural vulnerabilities. No attempt was made to penetrate physical security, as there were many admitted vulnerabilities in this area. In particular, the machine room was not secure and communications lines were not encrypted. Rather, this section looks at the areas of auditing, system configuration control, (23) passwords, and "privileged" users.

3.4.1 Dump and Patch Utilities

To provide support to the system maintenance personnel, the Multics system includes commands to dump or patch any word in the entire virtual memory. These

(23) System configuration control is a term derived from Air Force procurement procedures and refers to the control and management of the hardware and software being used in a system with particular attention to the software update tasks. It is not to be confused with the Fultics dynamic reconfiguration capability which permits the system to add and delete processors and memories while the system is running. utilities are used to make online repairs while the system Clearly these commands are very continues to run. dangerous, since they can bypass all security controls to access otherwise protected information, and if misused, can cause the system to crash by garbling critical data bases. To protect the system, these commands are implemented by special privileged gates into ring zero. The access control lists on these gates restrict their use to system maintenance personnel by name as authenticated by the login procedure. Thus an ordinary user nominally cannot access these utilities. To further protect the system, the patch utility records on the system operator's console every patch that is made. Thus, if an unexpected or unauthorized patch is made, the system operator can take immediate action by shutring the system down if necessary.

Clearly dump and patch utilities would be of great use to a system penetrator, since they can be used to facilitate his job. Procedural controls on the system dump and patch routines prevent the penetrator from using them by the ACL restrictions and the audit trail. However by using the software vulnerabilities described in section 3.3, these procedural controls may be bypassed and the penetration agent can implement his own dump and patch utilities as described below.

Dump and patch utilities were implemented on Multics using the Unlocked Stack Pase and Insufficient Argument Validation vulnerabilities. These two vulnerabilities demonstrated two basically different strategies for accessing protected segments. These two strategies developed from the fact that the Unlocked Stack Pase vulnerability operates in ring 4 master mode, while the Insufficient Argument Validation vulnerability operates in ring 0 slave mode. In addition, there was a requirement that a minimal amount of time be spent with the processor in an anomalous state - ring 4 master mode ring 0 illegal code. or When the processor is in an anomalous state, unexpected interrupts or events could cause the penetrator to be exposed in a system crash.

3.4.1.1 Use of Insufficient Argument Validation

As was mentioned above, the HIS 645 implementation of Multics simulates protection rings by providing one descriptor segment for each ring. Patch and dump utilities can be implemented using the Insufficient Argument Validation vulnerability by realizing that the ring zero descriptor segment will have entries for segments which are not accessible from ring 4. Conceptually, one could copy an SDW for some segment from the ring 0 descriptor segment to the ring 4 descriptor segment and be guaranteed at least as much access as available in ring 0. Since the segment number of a segment is the same in all rings, this approach is very easy to implement.

The exact algorithm is shown in flow chart form in Figure 11. In block 2 of the flow chart, the ring 4 SDW is read from the ring 4 descriptor segment (wdseg) using the insufficient Argument Validation Next the ring O SDW is read from the ring vulnerability. O descriptor segment (dseg). The ring O SPN must now he checked for validity, since the segment may not be accessible even in ring 0. (24) An invalid Shy is represented by all 36 bits being zero. One danger present here is that if the segment in question is deactivated, (25) the SDW being checked may be invalidated while it is This event could conceivably have being manipulated. disastrous results, but as we shall see in Section 3.4.2, the patch routine need only be used on segments which are never deactivated. The dump routine can do no harm if it accidentally uses an invalid SDW, as it always only reads using the SDW, conceivably reading garbage but nothing else. Further, deactivation of the segment is highly unlikely since the segment is in "use" by the dump/patch routine.

If the ring 0 SDN is invalid, an error code is returned in block 5 of the flow chart and the routine terminates. Otherwise, the ring 0 SDN is stored into the ring 4 descriptor segment (wdseg) with read-execute-write access by turning on the SDN bits for slave access, write permission, slave procedure. (See Figure 2). Now the dump or patch can be performed without using the vulnerability to load or store each 36 bit word

(24) As an additional precaution, ring 0 slave mode programs run under the same access rules as all other programs. A valid SDW entry is made for a segment in any ring only if the user is on the ACL for the segment. We shall see in Section 3.4.2 how to get around this "security feature".

(25) A segment is deactivated when its page table is removed from core. Segment deactivation is performed on a least recently used basis, since not all page tables may be kept in core at one time.







heing moved. Finally in block 8, the ring 4 SDW is restored to its original value, so that a later unrelated system crash could not reveal the modified SDW in a dump. It should be noted that while blocks 2, 3, 6, and 8 all use the vulnerability, the bulk of the time is spent in block 7 actually performing the dump or patch in perfectly normal ring 4 slave mode code.

3.4.1.2 Use of Unlocked Stack Base

The Unlocked Stack Base vulnerability operates in a very different environment from the Insufficient Argument Validation vulnerability. Rather running in ring 0, the Unlocked than Stack Base vulnerability runs in ring 4 in master mode. In the ring O descriptor segment, the segment dseg is the ring O descriptor segment and wdseg is the ring 4 descriptor segment. (26) However, in the ring 4 descriptor segment, the segment dser is the ring 4 descriptor segment and wdseg has a zeroed SDN. Therefore, a slightly different strategy must be used to implement dump and patch utilities as shown in the flow chart in Figure 12. (27) The primary difference here is in blocks 3 and 5 of Figure 12 in which the ring 4 SDU for the segment is used rather than the ring 0 SDW. Thus the number of segments which can be dumped or patched is reduced from those accessible in ring 0 to those accessible in ring 4 master mode. We shall see in Section 3.4.2 that this reduction is not crucial, since ring 4 master mode has sufficient access to provide "interesting" segments to dump or patch.

3.4.1.3 Generation of New SDU's

Two strategies for implementation of dumn and patch utilities were shown above. In addition, a third strategy exists which was rejected due to its inherent dangers. In this third strategy, the penetrator selects an unused segment number and constructs an SPL occupying that segment number in the ring 4 descriptor

(26) Actually wdseg is the descriptor segment for whichever ring (1-7) was active at the time of the entry to ring 0. No conflict occurs since wdseg is <u>always</u> the descriptor segment for the ring on behalf of which ring 0 is operating.

(27) This strategy is also used with the Execute Instruction Access Check Bypass vulnerability which runs in ring 4.





segment using any of the vulnerabilities. This totally new SDW could then be used to access some part of the Hultics hierarchy. However, two major problems are associated with this strategy which caused its rejection. First the absolute core address of the page table of the segment must be stored in the SDW address field. There is no easy way for a penetrator to obtain the absolute address of the page table for a segment not already in his descriptor segment short of duplicating the entire segment fault mechanism which runs to many hundreds or thousands of lines of code. Second, if the processor took a segment page fault on this new SDW, the ring 0 software would or malfunction, because the segment would not be recorded in the Known Segment Table (KST). This malfunction could easily lead to a system crash and the disclosure of the penetrator's activities. Therefore, the strategy of generating new SDW's was rejected.

3.4.2 Forging the Non-Forgeable User Identification

In Section 2.2.3 the need for a protected, non-forgeable identification of every user was identified. This non-forgeable ID must be compared with access control list entries to determine whether a user may access some segment. This identification is established when the user logs into Multics and is authenticated by the user password. (28) If this user identification can be forged in any way, then the entire login audit mechanism can be rendered worthless.

The user identification in Multics is stored in a per-process segment called the process data segment (PUS). The PDS resides in ring 0 and contains many constants used in ring U and the ring O procedure stack. The user identification is stored in the PDS as a character string representing the user's name and a character string representing the user's project. The PDS must be accessible to any ring J procedure within a user's process and must be accessible to ring 4 master mode procedures (such as the signaller). Therefore, as shown in Sections 3.4.1.1 and 3.4.1.2, the dump and patch utilities can dump and patch portions of the PDS, thus forging the non-forgeable user identification. Appendix E shows the actual user commands needed to forge the user

(28) Clearly more sophisticated authentication schemes than a single user chosen password could be used on Hultics (see Richardson <RIC73>). However, such schemes are outside the scope of this paper.

#### identification.

This capability provides the penetrator with "ultimace weapon". The agent can now undetectably an masquerade as any user of the system including the system administrator or security officer, immediately assuming that user's access privileges. The agent has hypassed and rendered ineffective the entire login authentication mechanism with all its attendant auditing machinery. The user whom the agent is impersonating can login and operate without interference. Even the "who table" that lists all users currently logged into the system records the agent with his correct identification rather than the forgery. Thus to access any segment in the system, the agent need determine who has access and change his user only identification as easily as a legitimate user can change his working directory.

It was not obvious at the time of the analysis that changing the user identification would work. Several potential problems were forseen that could lead to system crashes or could reveal the penetrator's presence. However, none of these proved to be a serious barrier to masquerading.

First, a user process occasionally sends a to the operator's console from ring 0 to report message some type of unusual fault such as a disk parity error. These messages are prefaced by the user's name and project taken from the PDS. It was feared that a random parity error could "blow the cover" of the penetrator by printing his modified identification on the operator's console. However, the PDS in fact contains two copies of the (29) user identification - one formatted for printing and one formatted for comparison with access control list entries. Ring 0 software keeps these strictly separated, so the penetrator need only change the access control identification.

Second, when the penetrator changes his user identification, he may lose access to his own programs, data and directories. The solution here is to assure that the access control lists of the needed segments and directories grant appropriate access to the user as whom the penetrator is masquerading.

(29) This danger exists only if the operator or system security officer is carefully correlating parity error messages with the names of currently logged in users.

Finally, one finds that although penetrator can set the access control lists of his ring 4 segments appropriately, he cannot in any easy way modify the access control lists of certain per process supervisor segments including the process data segment (PDS), the process initialization table (PIT), the known segment table (KST), and the stack and combined linkage segments for ring 1, 2, and 3. The stack and combined linkage segments for ring 1, 2, and 3 can be avoided by not calling any ring 1, 2, or 3 programs while masquerading. However, the PDS, PIT, and KST are all ring 0 data bases that must be accessible at all times with read and write permission. This requirement could pose the penetrator a very serious problem; but, because of the very fact that these segments must always be accessible in ring 0, the system has already solved this problem. While the PIT, PDS, and KST are paged segments, (30) they are all used during segment fault handling. In order to avoid recursive segment faults, the PIT, PDS, and KST are never deactivated. (31) Deactivation, as mentioned above, is the process by which a segment's page table is removed from core and a segment fault is placed in its SDW. The access control bits are set in an SDV only at segment fault time. (32) Since the system never deactivates the PIT, PDS, and KST, under normal conditions, the SDW's are not modified for the life of the process. Since the process of changing user identification does not change the ring O SDW's of the PIT, PDS, and KST either, the penetrator retains access to these critical segments without any special action whatsoever.

(30) In fact the first page of the PDS is wired down so that it may be used by page control. The rest of the PDS, however, is not wired.

(31) In Multics jargon, their "entry hold switches" are set.

(32) In fact, a segment fault is also set in an SDW when the access control list of the corresponding segment is changed. This is done to ensure that access changes are reflected immediately, and is effected by setting faults in all descriptor segments that have active SDW's for the segment. This additional case is not a problem, because the access control lists of the PIT, PDS, and KST are

#### 3.4.3 Accessing the Password File

Une of the classic penetrations of an operating system has been unauthorized access to the password file. This type of attack on a system has become so embedded in the folklore of computer security that it even appears in the definition of a security "breach" in DOD 5200.28-M (DOD73). In fact, however, accessing the password file internal to the system proves to be of minimal value to a penetrator as shown below. For completeness, the Multics password file was accessed as part of this analysis.

3.4.3.1 Minimal Value of the Password File

It is asserted that accessing the system password file is of minimal value to a penetrator for several reasons. First, the password file is generally the most highly protected file in a computer system. If the penetrator has succeeded in breaking down the internal controls to access the password file, he can almost undoubtedly access every other file in the system. Why bother with the password file?

Second, the password file is often kept enciphered. A great deal of effort may be required to invert such a cipher, if indeed the cipher is invertible at all.

Finally, the login path to a system is generally the most carefully audited to attempt to catch unauthorized password use. The penetrator greatly risks detection if he uses an unauthorized password. It should be noted that an unauthorized password obtained outside the system may be very useful to a penetrator, if he does not already have access to the system. However, that is an issue of physical security which is outside the scope of this paper.

3.4.3.2 The Multics Password File

The Multics password file is stored in a segment called the person name table (PNT). The PNT contains an entry for each user on the system including that user's password and various pieces of auditing information. Passwords are chosen by the user and may be changed at any time. (33) Passwords are scrambled by an

(33) There is a major problem that user chosen passwords



allegedly non-invertible enciphering routine for protection in case the PNT appears in a system dump. Only enciphered passwords are stored in the system. The password check at login time is accomplished by the equivalent of the following PL/1 code:

if scramble\_(typed\_password) = pnt.user.password
 then call ok\_to\_login;
 else call reject\_login;

For the rest of this section, it will be assumed that the enciphering routine is non-invertible. In a separate volume (DOW74>, Downey demonstrates the invertibility of the Multics password scrambler used at the time of the vulnerability analysis. (34)

following access control list:

rw \*.SysAdmin.\* null \*.\*.\*

Thus by modifying one's user identification to the SysAdmin project as in Section 3.4.2, one can immediately gain unrestricted access to the PNT. Since the passwords are enciphered, they cannot be read out of the PNT directly. However, the penetrator can extract a copy of the PNT for cryptanalysis. The penetrator can also change a user's password to the enciphered version of a known password. Of course, this action would lead to almost immediate discovery, since the user would no longer be able to login.

3.4.4 Modifying Audit Trails

Audit trails are frequently put into computer systems for the purpose of detecting breaches of security. For example, a record of last login time printed when a user logged in could detect the unauthorized use of a user's password and identification. However, we have seen that a penetrator using vulnerabilities in the operating

are often easy to guess. That problem, however, will not be addressed here. Hultics provides a random password generator, but its use is not mandatory.

(34) FSD/MCL has provided a "better" password scrambler that is now used in Multics, since enciphering the password file is useful in case it should appear in a system dump.

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system code can access information and bypass many such audits. Sometimes it is not convenient for the penetrator to bypass an audit. If the audit trail is kept online, it may be much easier to allow the audit to take place and then go back and modify the audit trail to remove or modify the evidence of wrong doing. One simple example of modification of audit trails was selected for this vulnerability demonstration.

Every segment in Multics carries with it audit information on the date time last used (DTU) and date time last modified (DTM). These dates are maintained by an audit mechanism at a very low level in the system, and it is almost impossible for a penetrator to bypass this mechanism. (35) An obvious approach would be to attempt to patch the DTU and DTM that are stored in the parent directory of the segment in question. However, directories are implemented as rather complex hash tables and are therefore very difficult to patch.

Once again, however, a solution exists within the system. A routine called set\_dates is provided among the various subroutine calls into ring 0 which is used when a segment is retrieved from a backup tape to set the segment's DTU and DTM to the values at the time the segment was backed up. The routine is supposed to be callable only from a highly privileged gate into ring 0 that is restricted to system maintenance personnel. However, since a penetrator can change his user identification, this restriction proves to be no barrier. To access a segment without updating DTU or DTM:

- 1. Change user ID to access segment.
- 2. Remember old DTU and DTM.
- 3. Use or modify the segment.
- 4. Change user 1D to system maintenance.
- 5. Reset DTU and DTM to old values.
- 6. Change user ID back to original.

in fact due to yet another system bug, the procedure is even easier. The module set\_dates is callable, not only from the highly privileged gate into ring 0, but also from the normal user gate into ring 0. (36) Therefore, step 4

(35) Section 3.4.5 shows a motivation to bypass DTU and DTM.

(36) The user gate into ring 0 contains set\_dates, so that users may perform reloads from private hackup tapes.

in the above algorithm can be omitted if desired. A listing of the utility that changes DTU and DTM may be found in Appendix F.

It should be noted that one complication exists in step 5 - resetting DTU and DTM. The system does not update the dates in the directory entry immediately, but primarily at segment deactivation time. (37) Therefore, step 5 must be delayed until the segment has been deactivated - a delay of up to several minutes. Otherwise the penetrator could reset the dates, only to have them updated again a moment later.

3.4.5 Trap Door Insertion

Up to this point, we have seen how a penetrator can exploit existing weaknesses in the security controls of an operating system to gain unauthorized access to protected information. However, when the penetrator exploits existing weaknesses, he runs the constant risk that the system maintenance personnel will find and correct the weakness he happens to be using. The penetrator would then have to begin again looking for weaknesses. To avoid such a problem and to perpetuate access into the system, the penetrator can install "trap doors" in the system which permit him access, but are virtually undetectable.

3.4.5.1 Classes of Trap Poors

Trap doors come in many forms and can be inserted in many places throughout the operational life of a system from the time of design up to the time the system is replaced. Trap doors may be inserted at the facility at which the system is produced. Clearly if one of the system programmers is an agent, he can insert a trap door in the code he writes. However, if the production site is a (perhaps on-line) facility to which the penetrator can gain access, the penetrator can exploit existing vulnerabilities to insert trap doors into system software while the programmer is still working on it or while it is in quality assurance.

As a practical example, it should be noted that the software for WWMCCS is currently developed using uncleared personnel on a relatively open time sharing system at Honeywell's plant in Phoenix, Arizona.

(37) Pates may be updated at other times as well.

The software is monitored and distributed from an open time sharing system at the Joint Technical Support Agency (JTSA) at Reston, Virginia. Both of these sites are potentially vulnerable to penetration and trap door insertion.

Trap doors can be inserted during the distribution phase. If updates are sent via insecure communications - either US Mail or insecure telecommunications, the penetrator can intercept the update and subtly modify it. The penetrator could also generate his own updates and distribute them using forged stationery.

Finally, trap doors can be inserted during the installation and operation of the system at the user's site. Here again, the penetrator uses existing vulnerabilities to gain access to stored copies of the system and make subtle modifications.

Clearly when a trap door is inserted, it must be well hidden to avoid detection by system maintenance personnel. Trap doors can best be hidden in changes to the binary code of a compiled routine. Such a change is completely invisible on system listings and can be detected only by comparing bit by hit the object code and the compiler listing. However, object code trap doors are vulnerable to recompilations of the module in question.

Therefore the system maintenance personnel could regularly recompile all modules of the system to eliminate object code trap doors. However, this precaution could play directly into the hands of the penetrator who has also made changes in the source code of the system. Source code changes are more visible than object code changes, since they appear in system listings. However, subtle changes can be made in relatively complex algorithms that will escape all but the closest scrutiny. Of course, the penetrator must be sure to change all extant copies of a module to avoid discovery by a simple comparison program.

Two classes of trap doors which are themselves source or object trap doors are particularly insidious and merit discussion here. These are the teletype key string trigger trap door and the compiler trap door.

It has often been hypothesized that a carefully written closed subsystem such as a query system or limited data management system without programming capabilities be made invulnerable to security may penetration. The teletype key string trigger is just one example of a trap door that provides the penetrator with a vulnerability in even the most limited subsystem. To create such a trap door, the agent modifies the supervisor teletype modules at the development site such that if the user types normally, no anomaly occurs, but if the user types a special key string, a dump/patch utility is triggered into operation to allow the penetrator unlimited The key string would of course have to be some access. very unlikely combination to avoid accidental discovery. The teletype key string trap door is somewhat more complex than the trap door described below in Section 3.4.5.2. However, it is quite straightforward to develop and insert with relatively nominal effort.

It was noted above that while object code trap doors are invisible, they are vulnerable to recompilations. The compiler (or assembler) trap door is inserted to permit object code trap doors to survive even complete recompilation of the entire system. a In Multics, most of the ring 0 supervisor is written in PL/1. A penetrator could insert a trap door in the PL/1 compiler to note when it is compiling a ring 0 module. Then the compiler would insert an object code trap door in the ring U module without listing the code in the listing. Since the PL/I compiler is itself written in PL/I, the trap door can maintain itself, even when the compiler is recompiled. (38) Compiler trap doors are significantly more complex than the other trap doors described here, because they require a detailed knowledge of the compiler design. However, they are quite practical to implement at a cost of perhaps five times the level shown in Section 3.5. It should be noted that even costs several hundred times larger than those shown here would be considered nominal to a foreign agent.

There is also a variant on the compiler trap door called the initialization trap door. Here, the system initialization code is modified by the penetrator to insert other trap doors as the system is brought up. Such trap doors can be relatively invulnerable to

(38) This type of trap door does not require a higher level language. Entirely analogous trap doors could be placed in an assembler. detection and recompilation, because system initialization is usually a very complex and poorly understood procedure.

## 3.4.5.2 Example of a Trap Door in Multics

To demonstrate the feasibility of inserting and distributing trap doors, the following object code change was made to check\*device\_name to provide a generalized dump or patch facility. Figure 13 shows a PL/I program that performs essentially the same function as the trap door actually inserted in the object code. The listing of the actual trap door and its calling program is in Appendix C. Checksdevice\_name is normally called with three arguments, the third being a fixed hinary error code. The trap door is inserted at the point at which check\$device\_name would have returned. The trap door looks at the 72 bits immediately following the error code that was passed by the caller. If those 72 hits match a predefined 72 bit password, then the fixed hinary word to which ptrl points is copied into the fixed binary word to which ptr2 points. Since check&device\_name is a ring 0 procedure, this copy is carried out using the ring 0 descriptor segment and allows the caller to read or write any word in ring 0. Dump and patch utilities can use this trap door exactly like the Insufficient Argument Validation vulnerability. The 72 bit key is used to that the vulnerability is not invoked by accident ensure by some unsuspecting user.

The actual insertion of the trap door was done by the following steps:

1. Change user identification to project SysLib.

2. Make patch in object archive copy of checkSdevice\_name in >ldd>hard>object.

3. Reset DTP on object archive.

4. Make patch in bound archive copy of check\$device\_name in >ldd>hard>bound\_components.

5. Reset DTM on hound archive.

6. Reset user identification.

This procedure ensured that the object patch was in all library copies of the segment. The DTN was reset as in Section 3.4.4, because the dates on library segments are

declare overlay fixed binary (35) based;

/\* Start of regular code \*/

•••;

/\* Here check\$device\_name would normally return \*/

if key = bit\_string\_constant\_password
 then ptr2 -> overlay = ptr1 -> overlay;

return;

end check\$device\_name;

Figure 13. Trapdoor in check\$device\_name

checked regularly for unauthorized modification. These operations did not immediately install the trap door. Actual installation occurred at the time of the next system tape generation.

A trap door of this type was first placed in the Multics system at MIT in the procedure del\_dir\_tree. However, it was noted that del\_dir\_tree was going to be modified and recompiled in the installation of Hultics system 18.0. Therefore, the trap door described above was inserted in checkSdevice\_name just before the installation of 18.0 to avoid the recompilation problem. Honeywell was briefed in the spring of 1973 on the results of this vulnerability analysis. At that time, Honeywell recompiled checkSdevice\_name, so that the trap door would not be distributed to other sites.

3.4.6 Preview of 6180 Procedural Vulnerabilities

To actually demonstrate the feasibility of trap door distribution, a change which could have included a trap door was inserted in the Multics software that was transferred from the 645 to the 6180 at MIT and from there to all 6180 installations in the field.

3.5 Manpower and Computer Costs

Table III outlines the approximate costs in man-hours and computer charges for each vulnerability analysis task. The skill level required to perform the penetrations was that of a recent computer graduate of any major university with a moderate knowledge Multics design documented in the <u>Multics</u> of Programmers' Manual (HPM73) and Organick (ORG72), plus nine months experience as a Multics programmer. In addition, the penetrator was aided by access to the system listings (which are in the public domain) and access to an operational Multics system on which to debug penetrations. In this example, the RADC system was used to test penetrations prior to their use at MIT, since a system crash at HIT would reveal the intentions of penetrations. (39) the

Costs are broken down into identification, confirmation, and exploitation. Identification is that

(39) It should be noted that while the MIT system was crashed twice due to typographical errors during the penetration, the RADC system was never crashed.

part of the effort needed to identify a particular vulnerability. It generally involves examination of system listings, although it sometimes involves computer work. Confirmation is that effort needed to confirm the existence of a vulnerability by using it in some manner, however crude, to access information without authorization. Exploitation is that effort needed to develop and debug command procedures to make use of the vulnerabilities convenient. Wherever possible, these command procedures follow standard Multics command conventions.

All figures in the table are conservative estimates as actual accounting information was not kept during the vulnerability analysis. However, costs did not exceed the figures given and in all probability were somewhat lower.

The costs of implementing the subverter and inverting the password scrambler are not included, because those tasks were not directly related to penetrating the system (See Downey (DOW74>). The Master Mode Transfer vulnerability has no exploitation cost shown, because that vulnerability was not carried beyond confirmation. TABLE 3

Cost Estimates

| Iask   | Manhrs              | Hanhrs CPU \$ | Confirmation<br>Manhrs CPU 5 | CPU S  |     | Exploitation<br>Manhrs CPU \$ |            | <u>Manhrs CFU \$</u> |
|--|---------------------|---------------|------------------------------|--------|-----|-------------------------------|------------|----------------------|
| Execute Instruction<br>Access Check Bypass     | 60                  | \$150         | 5                            | \$ 30  | 80  | \$100                         | 75         | \$ 280               |
| Insufficient Argument<br>Validation            | 1                   | •             | 5                            | \$ 30  | 24  | \$ 300                        | 30         | \$330                |
| Master Mode Transfer                           | 0.5                 | ,<br>,        | 2                            | \$ 20  | :   | 1                             | 2.5        | 2.5 \$ 20            |
| Unlocked Stack Base                            | 0.5                 | n \$          | 20                           | \$ 50  | 80  | \$500                         | 88.5       | 88.5 \$550           |
| Forging User ID                                | \$                  | n \$          | 5                            | \$ 30  | 5   | \$ 90                         | 15         | \$120                |
| check\$device_name<br>Trap door                | 5                   | о <b>\$</b>   | ø                            | \$ 50  | s   | \$ 30                         | 13         | \$ 80                |
| Access Password File<br>(Does not include decl | l \$<br>ciphering.) | ° (;          | 5                            | \$ 30  | 24  | \$150                         | 30         | \$180                |
| Totai  | 73                  | \$150         | 38                           | \$ 240 | 146 | 146 \$1170                    | 257 \$1560 | \$1560               |

57

## SECTION IV

## CONCLUSIONS

The initial implementation of Multics is an instance of an uncertified system. For any uncertified system:

a. The system cannot be depended upon to protect against deliberate attack.

b. System "fixes" or restrictions (e.g., query only systems) cannot provide any significant improvement in protection. Trap door insertion and distribution has been demonstrated with minimal effort and fewer tools (no phone taps) than any industrious foreign agent would have.

However, Multics is significantly better than other conventional systems due to the structuring of the supervisor and the use of segmentation and ring hardware. Thus, unlike other systems, Multics can form a base for the development of a truly secure system.

4.1 Multics is not Now Secure

The primary conclusion one Can reach from this vulnerability analysis is that Multics is not currently a secure system. A relatively low level of effort rave examples of vulnerabilities in hardware security, software security, and procedural security. While all the reported vulnerabilities were found in the HIS 645 system and happen to be fixed by the nature of the changes in the HIS 6180 hardware, other vulnerabilities exist in the HIS 6180. (40) No attempt was made to find more than one vulnerabilities exist in the HIS 645 Multics that have not heen identified. Some major areas not even examined are 1/0, process management, and administrative interfaces. Further, an initial cursory examination of the HIS 6180 Multics easily turned up vulnerabilities.

We have seen the impact of implementation errors or omissions in the hardware vulnerability. In the

(40) In all fairness, the HIS 6180 does provide significant improvements by the addition of ring hardware. However, ring hardware by itself does not make the system secure. Only certification as a well-defined closed process can do that.

software vulnerabilities, we have seen the major security impact of apparently unimportant ad hoc designs. We have seen that the development site and distribution paths are particularly attractive for penetration. Finally, we have seen that the procedural controls over such areas as passwords and auditing are no more than "security blankets" as long as the fundamental hardware and software controls do not work.

4.2 Multics as a Base for a Secure System

While we have seen that Multics is not now a secure system, it is in some sense significantly "more secure" than other commercial systems and forms a base from which a secure system can be developed. (See Lipner (LIP74).) The requirements of security formed part of the basic guiding principles during the design and implementation of Multics. Unlike systems such as 0S/360 or GCOS in which security functions are scattered throughout the entire supervisor, Multics is well structured to support the identification of the security and non-security related functions. Further Multics possesses the segmentation and ring hardware which have been identified (SMI74) as crucial to the implementation of a reference monitor.

### 4.2.1 A System for a Benign Environment

We have concluded that AFDSC cannot run an open multi-level secure system on Multics at this time. As we have seen above, a malicious user can penetrate the system at will with relatively minimal effort. However, Hultics does provide AFDSC with a basis for a <u>benign</u> multi-level system in which all users are determined to be trustworthy to some degree. For example, with certain enhancements, Multics could serve AFDSC in a two-level security mode with both Secret and Top Secret cleared users simultaneously accessing the system. Such a system, of course, would depend on the administrative determination that since <u>all</u> users are cleared at least to Secret, there would be no malicious users attempting to penetrate the security controls.

A number of enhancements are required to bring fultics up to a two-level capability. First and most important, all segments, directories, and processes in the system should be labeled with classification levels and categories. This labeling permits the classification check to be combined with the ACL check and to be represented in the descriptor segment. Second, an earnest review of the Multics operating system is needed to identify vulnerabilities. Such a review is meaningful in Multics, because of its well structured operating system design. A similar review would be a literally endless task in a system such as OS/360 or GCOS. A review of Multics should include an identification of security sensitive modules, an examination of all gates and references in ring 0, and a check of all intersegment be useful but not essential. These are some sort of "high and some sort of protection from user written applications programs that may contain "Trojan Horses".

# 4.2.2 Long Term Open Secure System

In the long term, it is felt that Multics can be developed into an open secure multi-level system by restructuring the operating system to include a security kernel. Such restructuring is essential since malicious users cannot he ruled out in an open system. The procedures for designing and implementing such a kernel are detailed elsewhere. (AND 73, BL 73-1, BL 73-2, LIP73, PR173, SCH73, SCH173, WAL74> To briefly summarize, the access controls of the kernel must always be involted (segmentation hardware); must be tamperproof hardware); and must be small enough and simple enough to he certified correct (a small ring 0). Certifiability is the critical requirement in the development of a multi-level secure system. ESD/MCI is currently proceeding with a development plan to develop such a certifiably secure version of Multics (FSD73).

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### APPENDIX A

## Subverter Listing

This appendix contains listings of the three program modules which make up the hardware subverter described in Section 3.2.1. The three procedure segments which follow are called subverter, coded in PL/1; access\_violations\_, coded in PL/1; and subv, coded in assembler. Subverter is the driving routine which sets up timers, manages free storage, and calls individual tests. Access\_violations\_ contains several entry points to implement specific tests. Subv contains entry points to implement those tests which must be done in assembler.

The internal procedure check\_zero within subverter is used to watch word zero of the procedure segment for unexpected modification. This procedure was used in part to detect the Execute Instruction Access Check Bypass vulnerability.

The errors flagged in the listing of subv are all warnings of obsolete 645 instructions, because the attached listing was produced on the 6180.

hcs\_sinitiate entry (char (\*), char (\*), char (\*), fixed bin (1), fixed bin (2), pir, fixed bin), /\* establishes default condition handler \*/ /\* resets alara clocks \*/
hcs\_smake\_seg entry (char (\*), char (\*), flxed bin (5), ptr, flxed bin),
/\* create a segment \*/ -ioa\_fioa\_siream entry options (variable), /\* prints on lo streams \*/
ioa\_siream entry options (variable), /\* prints on user\_eutput \*/
cv\_dec\_check\_ entry (cher (\*), fixed bin) returns (fixed bin (35)),
/\* string to numeric conversion points to failure blocks "/ points to statistics segment entry to do the testing #/ data\_time\_entry (fixed bin (71), cner (\*)). defauit\_handler\_sset entry (entry). timer\_meneger\_ssiera\_cell\_inhibit entry (fixed bin (71), bit (2), entry). does a cam instruction "/ /\* get pointer to arguments prints error messages "/ /\* sets alara clocks \*/ cu\_sarg\_ptr entry (fixed bin, ptr, fixed bin, fixed bin), COMPILATION LISTING OF SEGMENT subverter Compiled by: Multics PL/I Compiler, Version II of 30 August 1973. \*/ :: • • fimer\_manager\_fresst\_alars\_call entry (entry). access\_vielations\_siegel\_bounds\_fault, access\_vielations\_siilegaf\_bounds\_fault) com\_err\_ entry options (veriable), loa\_\$loa\_stream entry options (veriable), loa\_ entry options (veriable), access\_violations\_\$ilisgal\_opcodes. clock\_ entry returns (fixed bin (71)); user\_info\_fnomedir entry (cher (\*)). access\_violations\_\$xed\_fatchs access\_violations\_\$xed\_store. access\_violations\_Sfatch. access\_violations\_satore . access\_violations\_sid, subverterstimer ext entry. Cospiled on: 04/10/74 1845.8 edf Med sp pointer int static. df\_string cher (24). wdir cher (163). CODE TAXED BADA subvaldbr. subv sadbr. Subvector, subvise Ic. subvalaci, SCOV STRACE. . S IDSVOUS subvelas. subv scale. subvaldt, SUDV\$20 .. SUBV STCL. Subvisio u, entry (ptr). "IT Xed bin to pointer. deciare deciare Opt ions: map procedure; subverter: -NMS UN. 0 N 0 0 10 16 10 19 22 53 30 52 26 53 8 1000 1000 38 69 244 5 44 . 6 20 븱 12 2 4 15 17 21 2 28 1 51 25 23 22

|--|

```
call con_err_ (8. "subverter",
"Test "a was in progress. Call subvertersreset to clear segment and resume.",
                        /* default interval = 68 seconds */
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    •
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               Lf test_In_progress = 22 /* illegal opcode test */ then sext_code = next_code
test_in_progress = 0;
                                                                                             call fiser_mnager_$reset_alara_ca!! (subverterStimer);
                                                                                                                                                                                                                                                                                                                                                                                                                               /* segment aiready exists
                                                                                                                                                                    cali com_err_ (error_table_$bedep1, "subverter", arg);
                                                                                                                                                                                                                                                                                                                                                       /* 64% segment length */
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           /* start in 1 second */
                                                                                                                                                                                                                  cali user_info_Shomedir (wdir);
cali hcs_Seske_seg (wdir, "subvert_statistics", "", 01011b, sp. code);
if sp = nuli () then
                                                                                                                                                                                                                                                                                                                              /* segment is new */
last_failure_block, end_of_seveent = 100000.000000005
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              cell timer_sensers.selers_cell_inhibit (1, "11"b, subverterstimer);
                                                                                                                                                                                                                                                                              cell com_err_ (code, "subvertar", "subvert_statistics");
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      fest_nees (fest_in_progress)) ;
                                                                                                                                  intervel = cv_dec_check_ (arg, code);
1f code ^= 0 then
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             fime_of_test_test = clock__();
do i = 1 to rumber_of_tests;
tast_test_time (i) = time_of_test_;
                                 call cu_serg_ptr (1, argp, arg1, code);
If code = 0 then
                                                                                                                                                                                                                                                                                                                                                                                                                                        If test_in_progress "= 8 then
/* End of include file fallurs_block.incl.pl1 */
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                                                                      -- stop Then
                                                                                                                                                                                  return
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                                                                                                                                                                                                                                                                                                                 if code = 0 then
                     interval = 60;
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67

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ref\_label = next\_setup; call default\_newdier\_sset (fault\_hendier); call get\_failura\_block (cur\_test); number\_of\_attempts (cur\_test) = number\_of\_attempts (cur\_fest) + 1; time = cloct\_\_(); cail subvsidt (fp); co to screan\_bloody\_aurder; go to screas\_bloody\_surder! go to screan\_bloody\_murder! go to scream\_bloody\_murder; go to scream\_bloody\_murder; go to scream\_bloody\_aurder; go to screen\_bloody\_murder; go to scream bloody\_murder! go to scream\_bloody\_surder! celi subvșidbr (tp); call subv\$cloc (fp) } cell subv\$sdbr (fp); cell subvarace (fp); call subv \$sacs (fp); call subvisces (fp); call subvision (10); ge to finish\_setup; call check\_zero (); call subvsdis (fp); 5-bver 1 8781 8871 entry () : c (1) 1 c (2)1 c (3): C (4) c (5)1 c (5)1 c (8)1 c (9) c (7)8 1221 12001 333 1111 166 120 55 -241 152 193 ŝ 23 3 163 193 169 191 191 182 183 194 105 105 105 5 137 191 162
cali access\_vloiations\_Siliegal\_bounds\_fault (fp); call access\_vieletions\_siegal\_beunds\_fault (fp); go to scream\_bleedy\_murder; call access\_violations\_\$xed\_fatch (fp) } go to scream\_bloody\_murder; call access\_violations\_Sxed\_store (fp) ; cell access\_violations\_Statch (19); go to scream\_bleedy\_murder; call access\_violations\_satore (fp); go to screas\_bloody\_aurder; call access\_violations\_Sid (19)1 cali subvštaic (tp); go ło scream\_bloody\_surder; go to screas\_b'oody\_surder; cell subvissen (fp); go to scress\_bloody\_surder; call subv§rcu (fp); go to screat\_bloody\_surder; go te screas\_bloody\_aurder! ge to scream bloody\_surder! go to scream\_bloody\_murder! call subvisient (fp)] call subvision (fp); c (21) I c (15) 1 c (20) : c (10) : c (11) : c (12) 1 c (13) 1 C (14) 1 c (16) t c (17)-1 C (18) 1 c (19) 1 202 202 202 202 542 202 62.22.22.22 215 225 191 616161 66161 199 122 230 242 208 223 224 240 -217 210 219

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tp -> naxt_block() while (rei (p)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           ř
                                                                                                                                                                                                                                                                                                                                                                                                      cell loa_ ("'//'-Display of subverter statistics.'/");
if test_in_progress "= 8 then cell loa_ ("Test "R"="8 in progress.", test_neees (test_in_pregress));
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 nueber_of_strespts (1), nueber_of_feliuros (1));
do te = pointer (sp. failure_block_ptr (1)) repeat (peinter (sp. next_bleck)) while (rei (1p)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  "bd", fest_nees (1), cua_test_time (1)/36808888868.808.
                                                                                                                                                                                                                                                                                                                                                                                                                                               ("Total testing fise = ".2f hours.", cua_total_fime/3608000880.8e0)
                                                                                                                                                                                                                                                         call timer_senager_selers_cell_invibit (time, "11"b, subverterstimer);
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              = pointer (sp. failure_block_ptr (i)) repeat (pointer (sp.
                                                                                                                                                                                                                                                                                                                                          call user_infe_ghomedir (wdir);
call hcs_sinitiate (wdir, "subvert_statistics", "", 0, 0, sp. cede);
if sp = null () then ge to no_seg!
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         block_size (22) fixed bin init ((22) 32) int static.
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          call date_fime_ (time_of_fallure, dt_string);
call iom_ ("---fallure at "e.", dt_string) }
                                                                                                                                                                                                                                                                                                                                                                                                                                                                            ("Iast Name "-"-Iast Ikas Attantis
                                              call access_violations_sillegal_opcodes (fp);
go to screas_bloody_aurder;
                                                                                                                                                                                                                       if cur_fest = mex_fest then cur_fest = 15
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           = 1 to number_of_tests1
cell los_ ("-30s -0.21 -00
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          296
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   298
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                299
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             300
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       302
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    303
                                                                                                                                                                                                                                                                                                                                 272
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              299
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   293
                                                                                                                                                                                                            263
                                                                                                                                                                                                                            1222
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                     282
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   283
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        902
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   200
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         162
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       262
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        297
                                                                                          552
                                                                                                                   296
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| <pre>f (1) _= 0 then f [1] _= 0 then f [2] _= 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 =</pre> |  | all free failure block (cur test ) i | t_in_progress = 0; /* No sore worries about | A NG WOLL LUG WOLL LUG COUNTING | T CONS_NEED = CONVE (1) THEN | If cond_name = conds (1) then | L = 1 to n_condsi /* 1000 through the condition name array |  | U_DOUNDE_MTT , 1118 981 000000 1 | ut bounds err". "illegel opcode") [ | 35_competibulity", "undefined_acc", "accessvigiation", "peunds_reuri.on | with remeting the "undefined act" "active "active". "Bounds foul of | r (32) int static init ("Lilegs! precedure", "635/645_competibility" |  | ntinue bit (1) siloned. /* bit to indicate to continue search for handler |  | fixed bin int static init (8). | LIVA DAVI | 1 L xed | and bla | The char ("). | A mana char (e). |  |  |  | 10_DTF) /* pointer to software delined inte | de neinter to |  | ofr. A pointer to sechine conditions in ring a |  | MC DTF. /* DJLTTeF TO SAVED BECHINE CONGLIAONS V | All release to sever marking read that |  |  | precedure to catch interrupts | 18 moradus to catch internots | (ac ptr + cond_ness, wc ptr , into ptr + conti mest | procedure (at ptr. cond name, at ptr. into ptr. | the same the same same the same the same |  | aut bandlari |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 2 |  |  |  |  |  |  | at failure black a last failure black + |  |  |  |  |  | and the second |  |  | PLOTER NUCER BOLL BROLLIN | te is is in the first the state that the second field to be set | and a fight and analysis and heart share and an an |  | f p "= pointer (sp, fallure bicck pir (12) then ip =2 heat block = 44 | f o "s bointer (so, faliure block ofr (1)) then to -> next_block = 5; | the self for for failing black at (1) |  |  |  |  |  |  |  | D a Di | D = D] | D = DI | v a lind a painter to the block lust before the one to be |  |  |  |  |  |  |  |  | D = DOLT OF 180, 1811UTE_DIOCK_DIT 11/1 FEVEL NUMBER NUMER 18/ 18/ N - INAL PUTER NUMER | D = DOLMER (SD. 781, UPEDIOCK_DIT (L) / TEDEST (DEADIST 150, D -7 1944, DISCA) MILLE NY | a z asietar (eo. fallura block ofr (j)) repeat (seinfar (sp. p -> next_bleck)) while (rel (P) | <pre></pre> | a set of the set of the start of the second testates for a start highly will (rei (a) |  |  |  |  | -> failure block version. fo -> fyde = Ui /* 2000 The gave / | -> failure block version. fo -> fyde = 01 /* 2000 700 0373 / | and the black terelon. To an trop a D1 / tere the data | and the plant conclass for a function the data |  |  |  |  |  | AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA | A ANTA TO THE SDECE TOD BY UNDERDED TALINTE BIECK | A ANTAK TA TTAA SDACA TAATUKA AATUKA AATUKA AATUKA AATUKA ATUKAAAAA TAATUKA ATAKA AATUKA ATAKA | verse free an unneeded failure block | A star as the start of the start of the start of the start start start | the state of the s |  |  |  | 60 7 B 1 U 10 B 10 G K 2 | ee failure block! | ee faiture blocks | as failure blocks | an faiture black | deal of a state of a state | deals and the and | deal deal of the set |  |  |  |  |  |  |  |  |  |  |  |  |  |
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/\* This is a procedure to check for clobbering of bound subverter If compara\_word Ta word\_zero then call exec\_com (">udd>Qruid>Karger>subverter\_preero /\* Me can't handle this condition \*/ /\* So maybe semeone else con... \*/ Call setaci (">udd>d>pak>scbverter", "rems", "Karger.Druid.e"); call seteci (">udd>d>pak>subverter", "re", "Karger.Oruid.e"); word\_20 ro bit (36) aligned based (peinter (lapure\_ptr. 0)). impure\_ptr pointer based (addr (label\_var)). 1 lapure basad (lapure\_pfr) aligned, 2 lock\_word bit (36) a)igned, 2 compare\_word bit (36) aligned; tabel\_var tabel, exec\_com entry options (variable). setect entry options (veriable); label\_var = dumay\_label; if lock\_word ^= "d"b then CORPARA\_WORD = WORD\_ZARA; LOCK\_WARD = "0"5; continue = "1"b; -----\*\* return returns 100 dect are deci are :pue 120 proct - Due - 20 CI OCK\_ZOFOI diany\_labels ip s 365 365 369 369 378 371 372 376 375 11.0 191 -----300 1000 •

INCLUDE FILES USED IN THIS COMPILATION.

NAME subvert\_statistics.incl.pl1 failure\_block.incl.pl1 NU4 86 R LINE 71

PATHMAHE > user\_dir\_dir > Druid>Karger>cempiler\_peei>subver1\_stafistics.inci.pl1 > user\_dir\_dir > Druid>Karger>cempiler\_peei>tailure\_block.inci.pl1

|                                    | ATTRIBUTES AND REFERENCES | externel dcl 7 ref 215  | external del 7 ref 235 | externel dol 7 ret 245                | external doi 7 ret 258                  | externel dol 7 ret 248                           | externel dcl 7 ref 228         | externel dci 7 ref 225              | ci 7 ref 230<br>ci 56 set ref 76 61  | 1 841 741                | 1.8  | ernel dcl 7 ref 115 139 | 10 4/ 8/ 11 10/ 10 | Tar.  | ed del 346 ret 342 399 | Tal array     |         | rel 3 del 1-7 sat ref 1 | 2 dcl 1-7 807 rof 148 148 | 257 264    | 265 265 342 391 | dol 7 701 61    | orternal OCI 7 Tel 697 | u dci 98 sat ref 209 298 | icked unstigned del 1 | •                              | al del art rei | 555 233 335          | 50 set ref 146 150 155 168 165 | 26 912 112 112 601 501 319 32 | ernel del 7 ret | ernal dol 7 ref 89 | 50 set ref 117 118 det des des des des des des | ci 299 re | 326 329 333 335 |                  |                    |  |
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|                                    | DATA TYPE                 | entry   | entry                  | entry                                 | entry                                   | entry  | entry                          | ant r v                             | entry                                | fixed bin(17.8)          | 11<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1 | TING DINITA             | TIXed bin(17.0)    | entry | b1f (36)               | Char (32)     | PT4 (1) | 10                      | b10(71.                   | bin(17.8   |                 | entry           | entry                  | entry                    |                       | c fixed bin(35.6               | entry          | fixed bin(17.8)      | sounter                        |                               |                 |                    | TIXed bin(17.0)                                | 3         |                 | fixed bin(17.0)  | pointer            |  |
| W ILATION.                         | LOC STORAGE CLASS         | 374 constant  |                        | dan .                                 | N                                       | fault<br>000406 constant                         | sself 6 constant               |                                     | N                                    | Dased<br>Dates automatic |  |                         | Desig t automatic  |       | pesed                  | nate constant |         | 000322 constant         |                           | D = \$ = 0 |                 | adding constant |                        |                          |                       | Desed<br>Desed avternet static | constant       |                      | contro sufferentic             |                               |                 | 000304 constant    | D00100 automatic                               |           | D97989197       | 000100 automatic | Desed<br>Dereveter |  |
| WAYES DECLARED IN THIS CONFILATION | IDENTIFIER OFFSET         | WANES DECLARED BY DECLARE STATEMENT.<br>accase_violat long_sfatch 00037 | access_violaf lons_Sid | accass_vlataf lens_sillegaf_be unds_f | access_violat lons_\$11 te gat_op codes | access_violat tons_stags t_bounds_fault<br>00040 | access_violat ions_\$store 000 | access_violations_\$xed_fetch 00044 | access_violat ions_\$xed_store 00048 |                          | arg1   |                         |                    |       | compera_word           |               | cends   | DIT                     | cum_test_time 20          | cur test   |                 |                 | CV_DBC_CRBCM_          | er sset                  |                       | paert 1                        |                | failure_block_ptr 14 |                                | tp                            |                 |                    |  | -4        | 1               | 4<br>0 (         | Lapure_pir         |  |

000276 Internal static flxed bin(35.8) 000238 constant 000226 constant entry Isbel variable fixed bin(17.0) fixed bin(71.0) fixed bin(17.9) fixed bin(17,0) fixed bin(17.0) fixed bin(17.0) fixed bin(17.0) Isbel veriable fixed bin(17.8) fixed bin(17.0) fixed bin(17.8) fixed bin(17.8) fixed bin(71.0) fixed bin(71.0) fixed bin(71.8) fixed bin(17,0) fixed bin(17,0) polnter 090912 internet static char(32) b1t (36) pointer Polnter peinter entry entry entry entry entry entry mtry utry entry Intry entry Intry entry entry entry 000272 Internal static 003956 constant 000428 constant 000428 constant 000428 internal static autometto 941080178 parameter 888178 automotic 080102 automatic constant constant Beside constant BB3%6 constant BB8356 constant ----censtent censtant constant censtant 00312 constant 000314 constant censtant censtant censtant constant constant constant constant constant **peseq** peseq Desed peseq peseq. 99594 **beseq** besed 0.... besed Desed Desed Desed 000206 003655 1 50200 24600 000366 99799 4200 0 22 0 0 0 100376 1100\_01\_10100 2 1100\_01\_1051\_1051 4 1100\_\_000000\_\_0010\_11 1(1.8) 0(10) finer\_menger\_Sreset\_alars\_call 16 ÷ 1 1 0 wi lest\_failure\_block number\_of\_attendts number\_of\_failures number\_of\_fests user\_Infe\_Sho sedir test\_in\_progress 100\_\$100\_\$171 an 141\_fest\_fiee reverterst last seg\_version sefaci next\_block eck\_word abel\_ver 1021\_\_\_\_\_.10805 ref\_label next\_code subvacies subvelaci Subv8race Interval Nax\_fest subv Sanca U TESSADIS 5155Vdr Sub V Saan 10887478 L conds version K otr -TYPe 1100 4

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| statt stics  |   | peseq   | 517 LCT LT 0   | •  | 1 dcl 1-7  |  |
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| NAMES DECLARED BY EXPLICIT CONTEXT<br>C  | 0 MTEXT.<br>000000  | constant  | ledel  |  | dc1 146 ref 144 146<br>  | 1 150 155 160 165 170 175 100<br>2 210 215 226 225 238 235 240 |
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| check zere   | 002677  | constant  | entry  |  | dc1 378  | ref 134 262 378  |
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| dumey_ isbe!   | 040200  | Constant  | 19081  |  | rrai del 16  | 1 126 126 342  |
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|  | 61616   | constant  |  |  | 192 197 202 207 212<br>95 955  | 217 222 227 232 237 242 247                                    |
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| tesecscetterane  | 928388  | constant  | entry  |  | autornal del 125 r   |  |
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| 121  |   |   | bul i tin  | funct Len  | ernel ref 287  | <b>363 329 329</b>   |
| STORAGE REQUIRENENTS FOR THIS  | IS PROGRAM .  |   |  |  |  |  |
| Calect Text<br>Stert 0aject Text<br>Length 5548 3857   | Link<br>3542<br>422   | Syabot<br>4164<br>342   | Defs Ste<br>3057<br>463  | atic<br>3952<br>412  |  |  |
| External precedure subverter v<br>Internal precedure pal_fallure<br>Internal precedure fault_hand<br>Internal precedure check_zero   | - uses 280<br>are_block u<br>dier uses  | subverter uses 280 words of autematic storage<br>get_fallure_block uses 74 words of autematic storage<br>fault_handler uses 75 words of avfommatic storage<br>check_zero shares stack frame of axternal procedure | eutrematic storage<br>rds of autrematic :<br>of antomatic stor<br>of auternal pro- | age<br>1 c storage<br>forage<br>procedure subverter  |  |  |
| THE FOLLOWING EXTERNAL OPERATORS ARE USED BY<br>cp_cs call_ext_out_desc call<br>set_csa tra_isbel_ver ext_<br>rpd_ieep_2_i3_bp   | AL OPERATORS ARE U<br>call_exf_eut_desc<br>fra_fabef_ver                        | 1.  | 6 RAN .  | call_int_this<br>int_entry   | caliint_ether<br>int_entry_desc  | return<br>rpd_1000_1_10_bp                                     |
| THE FOLLOWING EXIERNAL ENTRIES ARE<br>access_violations_sfotch acces<br>access_violations_stitegal_opcodes<br>access_violations_store acce<br>access_violations_store acce | IES ARE CALLED BY<br>access_violati<br>ppcndes<br>access_violati<br>cu_sarg_ptr | BY THIS<br>etions_si<br>ations_sx   | RDGRAN.<br>d_fetch   | access_violafions_\$ilf<br>access_violafions_\$ieg<br>access_violafions_\$reg<br>cv_dec_check_ | access_violafions_\$iifegal_bounds_fault<br>access_violafions_\$iegad_bounds_fault<br>access_violafions_\$iegad_bounds_fault<br>cv_dec_check\$xed_sforecleck |  |

default\_hendter\_sset azec\_com Lea\_ Lea\_ subviscioc subvisidi THE FOLLOWING EXTERNAL VARIABLES ARE USED BY THIS PROGRAM. Beter\_table\_fbackpt

rcs\_Sinitiate hcs\_Semice\_teg setaci subvisiaci subvisiaci subvisider subvisader filme\_senager\_seiarm\_coli\_inhibit user\_infe\_shemedir

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|       |          | 2      | 8        |        | 1.1.1   |           |            |         | 3      |          |         |        |         |          |          | 2       | 202      | 274      |        |        |        |          |        |          |        |          |       |        |
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|       |          |        |          |        |         |           | 1.16       |         |        |          |         |        |         |          |          |         |          |          |        |        |        |          |        |          |        |          |       |        |
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| LINE  | 22       | 82     | 40       |        |         | 120       | 134        | 141     | 152    |          |         | 101    | 682     | 222      | 241      | 297     | 26.0     |          | 192    | 290    | 306    | 194      |        | 225      | - 652  |          |       | 5      |
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of threaded list of failure blocks "/ Identifies fest in pregress if mechine crashes "/ /\* rel pointer to nexr failurs block of this type of files of lest fest fixed bin(71). cum fortal fime fixed bin(71). rueber of tests fixed bin. a number of attempts fixed bin. 3 number of failures fixed bin. 5 failure biock pfr fixed bin. 5 failure biock bfr fixed bin(17) unal. /\* rei peinter to start of the test of failure • 2 of segment /\* ret peinter to test failurs bleck used humber of current tust in progress \*/ /\* index of test in test array \*/ /\* rel pointer te end /\* should never enter here \*/ Lf no test in pregress Text opcode number \*/ /\* 1 \* Tabler number \* 1 \*/ /+ 0060 to use fixed bin unai 19 July 1972 89 88 +/ 1+ Den 11eb • COMPILATION LISTING OF SEGNEMT access\_violetions\_ Ceeplied by: Muirics PL/I Compiler, Version II of 38 August 1973. Cesplied on: 84/18/74 1843.9 odt Med hts\_struncate\_seg entry (ptr, fixed bin, fixed bin), scratch\_p ptr int static init (nuil ()), • • 19 JULY 1972 /\* To be high\_code fixed bin int static init (184), end\_of\_segment fixed bin(17) unal, last\_failure\_block fixed bin(17) unal, /\* start of include file subvert\_statistics.incl.pl1 last\_test\_time fixed bin(71), CUR\_fest\_time fixed bin(71); 1 subvert\_statistics besed(sp) aligned, Initially coded by 2 Lt. Paul Karger Modified 21 July 72 8820 by P. Karger next\_code fixed bin(17) unet. of Include file failure\_bleck.incl.pl1 • Initiality coded by 2 Lt. Paul Karger 2 time\_of\_failure fixed bin(71). 2 mext\_block fixed bin(17) unal. 2 scu\_data(5) fixed bin(17) unal. next\_block fixed pin(17) unel, scu\_date(5) flxed bin; cur\_test fixed bin(17) unst. /\* End of include file failure\_block.incl.pl1 test\_in\_pregress fixed bin. \*allure\_block based(1p) all gned. /\* End of subvert\_statistics.incl.pl1 \*/ 1 11 2 version fixed bin, 2 type fixed bin, ac case\_violations\_I Terster dec lare Cottonst asp N NNNN deciare precedere! dectare ..... /\* Stert • -\* \*\* . 2 56 5 \* 3 .... 5 12 3 \* 5 16 5 0 NN NNNN NNNNNNNN

|   | <pre>code s (0:104) fixed bin int static init (0, 3, 5, 6, 10, 11, 12, 14, 15, 24, 25, 25, 28, 47, 55, 60<br/>72, 74, 75, 76, 80, 89, 90, 91, 92, 124, 136, 138, 139, 148, 152, 280, 294, 252, 259, 259, 259,<br/>260, 262, 253, 254, 266, 267, 268, 270, 271, 272, 274, 276, 278, 282, 284, 296, 294, 306,<br/>308, 309, 310, 311, 314, 315, 316, 318, 321, 322, 323, 324, 328, 239, 337, 338, 389,<br/>349, 409, 410, 428, 444, 457, 458, 459, 460, 472, 476, 504),<br/>394, 409, 410, 428, 444, 457, 458, 459, 460, 472, 476, 504),<br/>304, pot refure s (cher (168)),<br/>clock</pre>   |
|---|--|
|   |  |
|   | entry options (veriable).<br>add1 entry (char (*), char (*), fixed bin (5), die (8:2) fixed  |
|   | cu siever get entry (fixed bin).<br>Neme p ptr int static init (nuit ()).<br>reme p ptr int static init (nuit ()).<br>reed p ptr int static init (nuit ()).  |
|   | spectration in the second seco |
| ootseretchse                              |  |
| 001<br>001<br>001<br>001<br>001<br>0100   | if scratch_p = nuli () then call hcz_\$eeke_seg ("", "subverter_temp_3_", "", Biiiith scratch_p,<br>code);<br>cell hcs_\$fruncate_seg (scratch_p, 0, code);<br>dure;   |
|   | call hcs_\$mmia_seg ("", "subverter_fowp_4,", "", 011116, rewe_p, code);   |
| gat_no_acc_seg:<br>procedur<br>if<br>end; | :<br>dure;<br>if no_acc_p = null () then call hcs_Smake_seg ("", "subverter_teep_1_", "", 00.00%, ne_scc_p, cede)  |
| get_read_seg :                            |  |

| procedure;<br>if read p  | = null ()   |   |
|--|---|---|
| 2  | cell hos.<br>read_p ->  | <pre>p_2_r, "", 01111b, read_p, code);<br/>create pointer to word 7 */<br/>"101110"b;</pre>   |
|  | ្វដ្ឋី  | /* put in id modifier to its pointer /<br>/* fill in the taily in the indirect word °/<br>/* get validation level °/  |
|  | rings (*) = ];<br>call hcs_sacl_addt (get_pdir_ ();             | "subverter_taep_2_", "", 81888b, rings, code) }<br>/* reset the acl */  |
| • 10 •   |   |   |
| <pre>fstchi fstchi entry (fp) ; entry (fp) ; l = no_scc_p -&gt; i l = no_scc_p -&gt; i time i scu_data (1) = l; return;</pre>  | acc_seg;<br>> array (0);<br>ure = clock_ ();<br>= 1;            | <pre>/* attempts to read data from execute anly procedure */ /* metp sure we have a pointer to the segment */ /* should never get here */ /* should never get here */ /* sould never we got */ /* save whatever we got */</pre> |
| store!<br>antry (fp);<br>cali get_no_acc_B<br>no_acc_D -> array<br>time_of_fallure =<br>return;  | acc_seg;<br>array (0) = 17;<br>ure = clock_ ();                 | /* attampt to write data into execute only segment */<br>/* try to store */<br>/* failed */   |
| х<br>аd<br>14а<br>14а<br>14а<br>14а<br>14а<br>1<br>18а<br>1<br>0<br>1<br>18а<br>1<br>0<br>1<br>1<br>18а<br>1<br>0<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1 | scc_seg;<br>1_fmfcher (na_acc_p, i);<br>we = clock_ ();<br>= l; | /* try to fatch with xed instruction */<br>/* go into sim code */<br>/* should not return */  |
| 111<br>112 xe d_store:<br>113 xe d_store:<br>114 entry (fp);<br>114 cell get_no_ac<br>116 time.of_feilur<br>117 return;<br>118   | acc_seg;<br>d_storer (no_acc_p);<br>ure = clock_ ();            | /* try to store with an wed instruction */<br>/* go into alm */<br>/* should not return */  |
| 11:<br>entry (fp);<br>ca:1 get_rea<br>ca:1 sursid<br>time_of_fail<br>return;   | d_seg;<br>_inst (read_p);<br>ure = ciock_ ();                   | <pre>/* try to store using an indirect and taily modifier */ /* get a read only segment with data initialized */ /* go into als code */ /* should never return */</pre>   |
| le ge 1_bounds_fault 1   |   |   |

```
/* Indicate found non-zero first fies */
entry (fp);
call get_rewa_segi
call subvglegel_p1 (rewa_p);
if rewa_p -> bitstring = "0"b then signal condition (bounds_fault_ok);
do i = 0 to 65535;
                                                                         tise_of_fallure = clock_ () 1
scu_date (1) = 11
scu_date (2) = rewa_p -> array (1)1
                                                                                                                                                                                                                                                                                                            cell get_scretch_seg!
If next_cede = high_code then next_cede = 0;
else next_cede = next_cede • 1;
cell subw Stry_op (cedes (next_cede), scretch_p);
time_of_siture = clock_ ();
scu_dete (1) = cedes (next_cede);
                                                   If rews_p -> array (1) ~= 0 then
                                                                                                                                                                                                                              call subvisitegal_bf (rewa_p. 1)1
fiae_of_faijure = clock_ ()1
scu_data (1) = 11
                                                                                                           return:
                                                                                                                                        scu_date (1) = -11
scu_date (2) = 81
                                                                                                                                                                                                                     call get_ress_sep!
                                                                                                                       tpue
                                                                 100
                                                                                                                                                                                                 Il legel_bounds_fault1
entry (fp) 1
                                                                                                                                                                                                                                                                                         Li lagal_opcodes!
                                                                                                                                                                                                                                                                                                                                                                             return!
                                                                                                                                                                   return!
                                                                                                                                                                                                                                                                  Intu ter
                                                                                                                                                                                                                                                                                                   entry (10) 1
                                                                                                                                  = pue
                                                                                                                                                                                                                                                                                                                                                                                         10 4
1221
                                                                                                                                                                 144
                                                                                                                                                                                                                                                                                                  151
                                                                                                                                                                                                                                                                                                                       191158
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INCLUDE FILES USED IN THIS COMPILATION.

LIME

NAME subvert\_statistics.incl.pl1 failure\_block.incl.pl1 NUMBER 1

PATHMANE > user\_dir\_dir > 0ruid>Karger>complier\_pool>subver%\_ctatistics.incl.pii > user\_dir\_dir > 0ruid>Karger>complier\_pool>faliwre\_biec% .incl.pii

NAVES DECLARED IN THIS COMPILATION.

S Isvel Ievel 10/01 181 fixed bin(35.8) fixed bin(17.8) fixed bin(17,0) fixed bin(17.8) fixed bin(35.8) (8.71)nid bexi? fixed bin(17,8) bit (2359295) fixed bin(6.8) fixed bin(71.0) fixed bin(71.0) fixed bin(17.6) fixed bin(71.8) fixed bin(17.8) structure fixed bin(17,0) fixed bin(17.0) DATA TYPE condit Lon Pointer Polner pointer Pointer Pointer Pointer V L L L Pointer entry NAMES DECLARED BY DECLARE STATEMENT AND NEVER REFERENCED. 000100 stack reference 000210 censtant 000012 Internal static 098164 Internal static Internal static Internal static LUC STORAGE CLASS Internal static automattc Daname ter 088112 automatic 000113 automotic ALTOBATIC Constant Constant const nt Constant Constany 000110 automatic constant Constant censtant constant constant constant Constant 00000 constant 09260 Deseq besed Desed pesed besed peseq besed Desed Deseq Deseq besed besed 000100 000232 9 62 6 8 0 0 0 0 2 3 0 92000 4 02 0 0 0 000170 912000 991904 11111 000222 12000 010000 DECLARE STATEMENT. 4 22 0 0 0 OFFSET ( 1 7 7 ) 1(18) ŝ N 20 9 -13 hes\_struncets\_seg feijure\_bjocu\_ptr lest\_feijure\_bjock lest\_test\_tise mext\_bjock stavstillessi bi stavstessi bi stavstry\_ss stavstry\_ss NAMES DECLARED bounds faul 1\_ok CU\_SIAVA1\_941 Bubväxed\_ster er hcs\_seci\_edd 7186\_61\_fa11416 cum\_fotal\_fire end\_of\_segment fellure\_block Cea\_err\_\_ Cue\_fest\_fim subveld\_inst LOE NT IF IER bitstring \_DGLF\_ high\_cese Text\_code ad at ch b 1-306 M BCU\_data 1891 20 CLOCK ALLAY 0.000 10000 9 Code rings ī 9 8

83

ATTRIEUTES AND REFERENCES

dci 8 set ref 52 54 59 66 73 88 Initial errey dci 8 set ref 168 162 external dci 8 ref 78 oct 8 ref 86 98 91 95 99 183 187 186 112 116 128 dci 8 ref 86 98 91 95 99 183 187 186 112 116 128 124 128 136 137 138 142 143 147 151 152 159 161 external dc! 8 ref 98 99 187 116 124 136 191 161 del 2-10 807 ref 98 99 187 116 124 136 151 2-15 801 Fof 91 186 137 138 142 154 dc1 8 set ref 89 91 186 188 133 134 137 138 198 ref 8 158 158 159 159 159 168 162 19491 2 pecked unailgnad dci 1-7 sat ref 198 199 199 168 162 Initial dci 8 set raf 89 98 186 115 %6 66 Initial doi 8 set ref 121 180 134 138 158 59 Brrav doi 8 set ref 79 88 set ref 123 71 73 74 76 75 79 array dci 8 set ret 89 96 136 138 77 1-7 BOT FOI 168 52 52 54 level 3 packed unaligned dci 2 packed unaligned dci 1-7 2 packed unsitgned dci 2-10 fevel 3 dcl 1-7 fevel 3 dcl 1-7externel dol 8 ref 88 externel dol 8 ref 52 59 66 73 externel dol 8 ref 54 array level 3 dcl 1-7 level 2 dcl 1-7 level 2 dcl 1-7 level 2 packed uneilgned dcl 1-7 2 packed unaligned dci 1-7 1 dcl 2-10 external dol 8 ref 88 88 123 701 104 Initial del 8 ret 158 150 181 169 externel dci 8 ret externel dci 8 ret 24 75 dci 8 set rei 78 79 level 3 dcl 1-7 ž 2222 ÿ 1.0 dci 8 rei 132 dci 8 rei 132 dol 8 set ref Initial del a . . 1-2 Initial del 8 Inittal del 8 external dol a 1-7 dc1 1-7 i n array level i og ş ş del Initial del ş 143 152 162 ş R axternal externel SKTOP1 externel externe! externet PLAY Ievel I a va I **XOLLO** 16491 Brray PLIAY I aval

> fixed bin(71.0) fixed bin(17,8) fixed bin(17.8) (11,10 bin(17.8) fixed bin(17.0)

Desed Deseq Deseq Deseq Desed Desed Deseq

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214

number\_of\_attempts number\_of\_fai lures subvert\_statistics fest\_in\_progress

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number:

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Structure

| 14215<br>148_61_1451_1651  | 12  | Â           | besed   |           |  | 1  |   | -            |   |            |         |
|--|---|-------------|---|-----------|--|--|---|--------------|---|------------|---------|
| 1 ype  | -   | 5 4         |   | 10        |  |  | >   | N            |   |            |         |
| wersten  | 4   | ŏŏ          | Desed   |           | xed bin(17.8)  | 17.0)  |   |              |   |            |         |
|  | EAPLICIT CONTEX   | Τ.          |   |           |  |  |   |              |   |            |         |
| a_vielaf lone_   |   |             | constant  | ent       | Irv  |  | ax 1.   | arnal d      | del 2 mat 2                               |            |         |
|  | 0   |             | constant  | C         | entry  |  | 4 10  |              | 16 Per                                    |            |         |
|  |   |             | censtant  | ŝ         | entry  |  | Int   |              | 101 39                                    | 97 105     | 114 64  |
|  |   |             | Constant  | 0         | entry  |  | T'ut  |              | 12 53                                     | 5          |         |
| est acratch a es   |   |             |   |           |  |  | 104   |              | 101 95                                    | 130 149 56 |         |
| 10   |   |             | Constant  |           |  |  |   |              | 2 12                                      |            |         |
| Tingel_serves_feet1  |   | -           | constant  | C.        | entry.   |  |   | arternal del |   |            |         |
| iliegel_epcodes  |   | -           | constant  | Ce        | entry  |  | - X -   |              |   | 155        |         |
| legal bounds fault   | 0   |             | constant  | C.        | entry  |  | A XO  |              | 120 1                                     |            |         |
|  |   |             | constant  | en.       | entry  |  | ext.  | ITAN de      | 1 95 Fe                                   |            |         |
|  |   | 000211 CC   | constant<br>constant  | 55        | entry<br>entry   |  | er te   | externel do  |   |            |         |
| NAMES DECLARED BY  | CONTEXT OR IMPLI  | CAT TON-    |   |           |  |  |   | 1            |   |            |         |
|  |   |             |   | P.I.I     |  |  |   |              |   |            |         |
| ped nt er  |   |             |   | 22        | Put Itto fun   | funct Len  |   |              | 1 92 99 71                                |            |         |
|  |   |             |   | 12        |  | function   | Int   |              |   |            |         |
| ers sin a anose syreous  |   |             |   | 2         |  | ue Tab   | TO T  |              |   |            |         |
|  | ANA CTUI MAL C  |             |   |           |  |  |   |              |   |            |         |
| 0.01 .00   | Text Link   |             | Sy abo I  | Oafs      | Static   |  |   |              |   |            |         |
| Langth 2106  | 1122 234  |             | 2612  | 233       | 1366   |  |   |              |   |            |         |
|  |   |             |   |           |  |  |   |              |   |            |         |
| Externel precedure<br>Internel precedure<br>Internel precedure<br>Internel precedure | access_violations_ uses 296 words<br>9e1_scratch_seg shares stack frame<br>9a1_rewa_seg shares stack frame of<br>9a1_rewa_seg shares stack frame of<br>9a1_rewa_seg shares stack frame of |             | nt, uses 296 mords<br>wheres stack frame<br>ares stack frame of<br>shares stack frame of<br>shares stack frame of |           | 01 actosatic<br>01 actosatic<br>01 actoration<br>01 actoration<br>01 actoration<br>01 actoration | Pic storege<br>al procedure<br>procedure<br>procedure<br>procedure | storage<br>procedure access_visiations_<br>ocedure access_vialations_<br>procedure access_vialations_ |              | ÷   |            |         |
| THE EQLLONING EXTER  | EXTERNAL OPERATORS A  | DE USED     | AV THT' DOCEAN  | Panc a tu |  |  |   |              |   |            |         |
|  | cell_ext_eut_d  | 1-0050      |   | _out      | return   |  | s i gn  | j eug        | ext                                       | t_entry    |         |
|  |   |             |   |           |  |  |   |              |   |            |         |
| 2 8  | EXTERNAL ENTRIES ARE CULSIC   |             | V THIS  | PROGRAM.  | 100  | get_pdir   |   | È            | cs_Baci_add                               |            |         |
| subveleget bf  | 202   | subvstry_op |   |           | 18.AQ.78   | d_fetchei  | 4   | •            | To Lo |            |         |
| NO EXTERNAL VARIABLES  | ES ARE USED BY  | THIS PR     | PROGRAM.  |           |  |  |   |              |   |            |         |
| LINE LJC   | LINE LOC  | 1 1 10      | 10.1  |           | 8  |  | :   |              |   |            |         |
| 1000   | 2 000056  | 1 1 1 1 1   | 000065  | L L ME    |  |  |   |              |   |            | L OC    |
| 1 00011  |   | 95          | 000121  | 000       |  |  | 5/0000  |              |   | 00 00      | 1010    |
| 11000  | 9 1 0 9 0 1 5   | 106         | 000157  | 107       | 80 1 70  |  | 1010707   |              |   |            | 146     |
| 12000  |   | 116         | 000227  | 117       | 00 0 2 41  | 120  |   |              |   |            |         |
| 124 888261   | 125 000273  | 128         | 000274  | 130       | 000303   | 131  | 00 0 30 4   | 132          | 51500                                     |            | 26.26   |
|  | 55000   | 137         | 000345  | 138       | 000355   | 1 39   | 0   | 141          |   |            | 992 990 |
|  |   |             |   |           |  |  |   |              |   |            |         |

| 25.000 251  | - | - | -         | - |  |
|-------------|---|---|-----------|---|--|
| 151 000420  |   |   |           |   |  |
| 158 889487  |   |   | 67 000734 |   |  |
| 149 000406  |   |   |           |   |  |
|             |   |   | 64 800664 |   |  |
|             |   |   | 68 888663 |   |  |
| 143 88937 3 |   |   |           |   |  |

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| 2/11/74     1725.5     odf Ned     1973       2/11/74     1725.5     odf Ned     111       2/11/74     1725.5     odf Ned     111       2/11/74     111     odf Ned     0001       2/11/74     111     odf Ned     0011       2/11/74     111     0017     0017       2/11/74     111     0017     0017       2/11/74     111     0017     0017       2/11/74     111     0017     0017       2/11/74     111     17     0017       2/11/14     11     0017     0017       2/11/14     11     11     0017       2/11/14     2/11     0017     0017       2/11/14     2/11     0017     0017       2/11/14     2/11     0017     0017       2/11/14 <th></th> <th></th> <th></th> <th>01</th> <th>Ner</th> <th></th> <th>b</th> <th>gisters</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th>sode_succeeded-*, Lc Sheuld never get here</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th>The subdid user Basic Diffe</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> |  |        |           | 01      | Ner     |          |       |      |     |        |     |   |      |           |           |            |       |           |           |           | b | gisters   |               |            |           |          |          |            | sode_succeeded-*, Lc Sheuld never get here |              |             |           |             |             |              | The subdid user Basic Diffe |   |                           |             |             |             |              |              |               |
|--|--|--------|-----------|---------|---------|----------|-------|------|-----|--------|-----|---|------|-----------|-----------|------------|-------|-----------|-----------|-----------|---|-----------|---------------|------------|-----------|----------|----------|------------|--|--------------|-------------|-----------|-------------|-------------|--------------|-----------------------------|---|---------------------------|-------------|-------------|-------------|--------------|--------------|---------------|
| 0.4/11/7, 0.1d_01     0.1d_01       0.11/7, 0.1d_01     0.1d_01       0.11/7, 0.1d_01     0.1d_01       0.11/7, 0.1d_01     0.1d_01       0.11/7, 0.126, 0.1d_01     0.1d_01       0.11/7, 0.126, 0.1d_01     0.1d_01       0.11/7, 0.126, 0.1d_01     0.1d_01       0.0021     0.1d_01       0.00224     0.1d_01       0.00250     1.1       0.00250     1.1       0.00250     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.0017     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.00160     1.1       0.1     1.1<  | 973<br>973   | - BLDV | - 100al - | y 11149 | y xed_f | Y Ked_ST | TOT A | ×    |     |        | • • | 0 | TE A | E .       |           | -          |       |           | antry nou |           |   | ses pases | tenpd control | 54V0       |           |          |          |            |  | e.ves        |             |           |             |             |              |                             | 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 |                           |             |             |             |              |              | 110 BER107    |
| 1     1 <td></td> <td>,</td> <td></td> <td></td> <td>80</td> <td></td> <td></td> <td></td> <td></td> <td>5</td> <td></td> <td>144</td> <td>101</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>  |  |        |           |         |         |          |       |      |     |        |     |   |      |           |           |            |       |           |           |           |   |           |               |            |           |          | ,        |            |  | 80           |             |           |             |             | 5            |                             | 144                                     | 101                       |             |             |             |              |              |               |
|  | 1/74 1826.<br>old_objec<br>version 4.4<br>3/74 1728. | 1111   | 9200      | 0031    | 021     | 9922     | +208  | 0000 | 100 | 0 2000 |     |   |      | 8 2 0 0 0 | 0 0 1 0 0 | <br>0 2100 | 00130 | 0 9 7 8 0 | 00150     | 2 8 8 8 9 |   |           | 22            | 22 3521 20 | 20 5521 8 | a 1265 a | 0 3331 0 | 0e 1052 22 | 10 23/6 64<br>51 7100 64                   | 0022 3521 20 | 0 1269 0200 | 1255 0010 | 7722 2521 9 | 0032 2501 0 | 0000 6570 00 | 10 0012 1110                | 00 1001 CC00                            | 00515555500<br>0050655100 | 0 1255 0100 | 7722 2521 0 | 7700 3331 0 | 0032 2501 00 | 0000 6370 00 | 01 21 7100 04 |

|      |      |       |      |      | 0    | Bester sode succesded *. I c |   |   |      |       |      |      |      |      |   |      |      | Saster_seda_s uccesseded- *, Lo |   |    |         |        |       |       |       |       |      | antar mode succession-s |    |   |       |        |        |       |        |        |      | astar anda succession- |   |     |       |        |       |      |       |        |        | acter and succession |    |   |        |      |      |        |      |       | 9     |      |   |   |
|------|------|-------|------|------|------|------------------------------|---|---|------|-------|------|------|------|------|---|------|------|---------------------------------|---|----|---------|--------|-------|-------|-------|-------|------|-------------------------|----|---|-------|--------|--------|-------|--------|--------|------|------------------------|---|-----|-------|--------|-------|------|-------|--------|--------|----------------------|----|---|--------|------|------|--------|------|-------|-------|------|---|---|
|      |      |       |      |      | L    | tre                          |   |   |      | 0 405 |      |      |      |      |   |      |      | 24                              |   |    | 8 84 8  |        |       |       |       |       | chec |                         |    |   | 5846  |        |        |       |        |        | die  |                        |   |     |       |        |       |      |       |        |        |                      |    |   | Save   |      |      |        |      |       |       |      |   |   |
| Ider |      |       |      |      |      |                              |   |   | 1    |       |      |      |      |      |   |      |      |                                 |   |    | c1 0 C1 |        |       |       |       |       |      |                         |    |   | 9188  |        |        |       |        |        |      |                        |   |     | Laca1 |        |       |      |       |        |        |                      |    |   | S BC B |      |      |        |      |       |       |      |   |   |
| 7    |      |       |      |      |      | 7                            | 3 | 1 |      |       |      |      |      |      |   |      | 3    | 1                               | 3 | 54 | 9       |        |       |       |       |       | 51   | 2                       | 12 | 1 | 16    |        |        |       |        |        | 3    | 15                     |   | R S | 3     | 8      |       |      |       |        | 61     | 12                   | 15 | 3 | 5      |      |      |        |      |       | \$    | 13   | 5 | 0 |
|      |      |       |      |      |      |                              |   |   |      |       |      | -    | 0    |      |   |      |      | 1                               |   |    |         |        |       |       |       |       |      |                         |    |   | 5.8   |        |        |       |        |        |      | 1                      |   |     | 2.0   |        |       |      |       |        |        |                      |    |   |        |      |      | 00     |      |       |       |      |   |   |
| 1269 | 3521 | 2521  | 1000 | 2581 | 2320 | 7100                         |   |   | 1674 | 1965  | 1269 | 3521 | 2521 | 1111 |   | 1043 | 1548 | 1100                            |   |    | 3521    | 6521   | 3521  | 2521  | 1555  | 2992  | 0150 | 7100                    |    |   | 3521  | 6521   | 5521   | 2521  | 1225   | 2501   | 6168 | 7100                   |   |     | 1251  | 103    | 14.91 | 1030 | 1225  | 1852   | 23.30  | 7108                 |    |   | - 60   | 5    | 10   | 2521   | 10   | 10    | 10    |      | 4 |   |
|      | 301  | ~ ~ ~ | 222  |      | 8    | 100                          |   |   |      |       |      |      | 777  | 777  |   |      |      |                                 |   |    | 22000   | 00020  | 00700 | 77722 | 77700 | 22000 |      | 10100                   |    |   | 10022 | 00020  | 00700  | 77722 | 77788  | 00032  |      | 12000                  |   |     | 22000 |        |       | 2222 |       | 0.32   |        |                      |    |   | 8822   | 0200 | 0100 | 77722  | 7700 | 55.00 | 00000 | 0051 |   |   |
|      |      |       |      |      |      |                              |   |   |      |       |      |      |      |      |   |      | •    |                                 |   |    |         | •      |       |       |       |       |      |                         |    |   | 9     |        |        |       |        |        |      |                        |   |     |       |        |       |      |       |        |        |                      |    |   |        |      |      | 2      |      |       |       |      |   |   |
|      | •    | •     | •    | •    | •    | •                            |   |   | 1    | •     |      | •    |      | -    | • |      |      |                                 |   |    |         | •      | •     | •     | •     | •     | •    |                         |    |   | •     |        |        |       |        | •      |      |                        | • |     |       |        |       |      |       |        |        |                      | •  |   | •      |      |      |        | •    | •     | -     |      |   |   |
|      |      |       |      |      |      | =                            |   |   |      |       |      |      | •    |      |   |      |      |                                 |   |    | 5       | 150000 | 3     | 3     | 8     | -     | 3    | . 🖷                     |    |   | 10000 | 199999 | 200000 | 20000 | 430000 | 300065 |      | 00000                  |   |     | 92999 | 179988 |       |      | 17996 | 276669 | 010000 | 770000               |    |   | 100    | 100  | 100  | 000103 | 100  | 130   | 100   |      |   |   |

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|      |       |      |      |      |      |      |       | 1    | ucceeded- * , i c |   |        |      |      |       |      |      |      |        | 1 Barbar dates |    |            |      |         |      |      |      |      |      |      | ucce e ded- * , I c |   |    |       |      |      |        |      |     |     |     | uccae ded- *, I c |   |         |        |      |     |      |     |     |      | vccse ded= * , L c     |     |   |              |     |     |      |     | Get pointer te greusent 1 | rgument 1 is a pointer |   |
|------|-------|------|------|------|------|------|-------|------|-------------------|---|--------|------|------|-------|------|------|------|--------|----------------|----|------------|------|---------|------|------|------|------|------|------|---------------------|---|----|-------|------|------|--------|------|-----|-----|-----|-------------------|---|---------|--------|------|-----|------|-----|-----|------|------------------------|-----|---|--------------|-----|-----|------|-----|---------------------------|------------------------|---|
|      |       |      |      |      |      |      | e     |      | sester_sode_s     |   |        |      |      |       |      |      |      | 0      | actes some     |    |            |      |         |      |      |      |      |      |      | 1 0000 Letter       |   |    |       |      |      |        |      |     |     |     | 8 000 Laisa       |   |         |        |      |     |      |     |     |      | 19191 - 9008 - 1915 BE |     |   | dedi         |     |     |      |     | 2                         | p 10.                  |   |
|      | 8 A B |      |      |      |      |      | - Jan |      |                   |   | S AV B |      |      |       |      |      |      | 1 act  | 414            |    |            |      |         |      |      |      |      |      |      |                     |   |    | 8 BVB |      |      |        |      |     |     |     |                   |   | Sava.   |        |      |     |      |     |     | 3    |                        |     |   | BO DE SUCCES | 419 |     | sted |     | d q de e                  | e ep p                 |   |
|      | Seict |      |      |      |      |      |       |      |                   |   | 1aclt  |      |      |       |      |      |      |        |                |    |            |      |         |      |      |      |      |      |      |                     |   |    |       |      |      |        |      |     |     |     |                   |   | 1 D C I |        |      |     |      |     |     |      |                        |     |   | Rester.      |     |     |      |     |                           |                        |   |
| 69   | 20    |      |      |      |      |      | 11    |      | 22                | 2 | 75     |      |      |       |      |      |      | 76     | 11             | 78 | : <b>R</b> |      | 8       |      |      |      |      |      |      | 8                   | 2 | \$ | 3     |      |      |        |      |     | -   | 3 5 | 8                 | 8 | R       |        |      |     |      |     | 8   | : 8  | XS                     | 2 3 | 8 | 8            | 25  | 8   | 8    | 100 | 101                       | 102                    |   |
|      |       | 0    | a    | •    | 0    | •    | 8     | e    |                   |   | 20     |      | 0    |       |      |      |      | 00     | -              |    |            |      |         |      | 0    | :    | 00   |      |      |                     |   |    |       |      |      |        | 00   |     |     | 1   |                   |   | 20      |        |      | 00  | 00   | 00  | 00  |      |                        |     |   |              |     |     | 00   |     | 20                        |                        |   |
|      | 1255  | 6521 | 3521 | 1747 | 1252 | 2561 | 4510  | 7100 |                   |   | 3521   | 6521 | 3524 | 26.94 | 1242 | 1222 | 2561 | 4538   | 7100           |    |            | 1621 |         | 1360 | 1262 | 1000 | 2501 | 2570 |      |                     |   |    | 1255  | 1255 | 1251 | 2521   | 1221 | 195 | 571 | 100 |                   |   | 125     | 125    | 1251 | 125 | 1331 | 501 | 130 | 100  |                        |     |   |              | 145 | 531 | 571  |     | 521                       | 170                    |   |
| - 16 | 22 88 | 64   | 0    | ũ.   |      | in.  | ē     | 141  |                   |   |        | 50   | 00   |       | 3    | 8    | 25   |        | 10             |    |            | -    |         |      | 22   | 2    | 25   |      |      | 4                   |   | -  | N     |      | 2    | N      | 2    | 2   | 9   |     |                   |   | N       | 20 6   | -    | 22  | 2    | 25  | 2   | -    |                        |     |   |              | 0   | ~   |      |     | 202                       | 2                      | 1 |
|      |       |      | G    |      | •    | •    | 5     | 000  | >                 |   |        |      |      |       | - 1  |      | 9    |        | ۲              |    |            |      |         |      | 111  | •    | •    |      | 9999 |                     |   |    |       |      |      | 777    |      |     | -   |     |                   |   | :       |        | 001  | 117 | 777  | 000 |     | 0000 |                        |     |   |              | 8   | 8   |      |     | 000                       | 2                      |   |
|      | •     |      |      |      |      |      |       |      |                   |   | 9      |      |      |       |      |      |      |        |                |    |            |      |         |      |      |      |      |      |      |                     |   |    |       |      |      | ~      |      |     |     |     |                   |   |         | N      |      |     |      |     |     |      |                        |     |   |              | 9   | •   |      |     | <b>.</b>                  | v                      |   |
|      |       | _    |      |      |      |      |       |      |                   |   | *      | -    | -    |       | •    | •    | •    | •      | -              |    |            |      |         | •    |      | •    | -    | -    |      | •                   |   | 1  |       | -    | •    |        | •    | -   |     |     |                   |   |         |        |      |     |      |     |     |      |                        |     |   |              |     |     |      |     |                           |                        |   |
|      |       | 1100 | 1100 |      |      | 1100 | 1110  | 1110 |                   |   |        | 100  | 100  |       |      |      |      | 000126 | 10.0           |    |            |      | 22.2000 |      |      |      | 100  | 100  |      |                     |   | 1  | 53    | 5    | 5    | 241800 | 5    |     |     | 3   | •                 |   |         | 151000 | 100  | 10  | 100  | 100 | 100 | 100  |                        |     |   | 000160       | 10  | 100 | 1    |     |                           |                        |   |
|      |       |      |      |      |      |      |       |      |                   |   |        |      |      |       |      |      |      | -      |                |    |            |      |         |      |      |      |      | -    |      |                     |   |    |       |      |      |        |      |     | _   |     |                   |   |         |        |      |     |      |     |     |      |                        |     |   |              |     |     |      |     |                           |                        |   |

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| Raad the clock    | ore high          | Iom bits -       | Zero z2 |             |      |      | Lucresort DV 1 |       |     |            |           |                    |     |        | Increasnt loop counter by 1 | 4 7    |   |    |     |         |   |              |      |      |      |      |         |    |   | 11151 810 18 8 911 | execute the xed instruction |          |     |       |       |       |       |          |     |      |           |         |       |
|-------------------|-------------------|------------------|---------|-------------|------|------|----------------|-------|-----|------------|-----------|--------------------|-----|--------|-----------------------------|--------|---|----|-----|---------|---|--------------|------|------|------|------|---------|----|---|--------------------|-----------------------------|----------|-----|-------|-------|-------|-------|----------|-----|------|-----------|---------|-------|
| tave infost[cloce | pittee of feilure | I TON OF OFT TIM |         | •           | 5.2  |      |                | • 🗰   |     |            | 9151ers+2 | 0915846_8rea+ 6, 2 |     |        | 1.2                         |        |   |    |     |         |   |              |      |      |      |      |         |    | - · · · · · · · · · · · · · · · · · · · | 00101              | etch                        |          |     |       |       |       |       |          |     |      | sed store |         |       |
|                   | at a              | 519              | eax 2   | Dases_Icopi |      | 810  |                | † mil |     | regs_iacp1 |           | 519                |     |        | eax?                        | C 40x2 | 1 |    |     |         | 7 | vad fatchers |      |      |      |      |         |    |   |                    | Xex                         | 210<br>2 |     |       |       |       |       |          |     |      | U         | L L L L |       |
| 103               | 105               | 106              | 101     | 109         | 110  | 111  |                | 114   | 115 | 117        | 110       | 119                | 021 |        | 121                         | 21     | 3 | 10 | 851 | 128     | 2 | 10           |      |      |      |      |         | 19 | 均                                       |                    | 20                          | 53       | 141 |       | 2     |       |       |          | 144 | 541  |           | 140     |       |
|                   | 00                |                  | 00      |             | 12   | 2    |                | 00    |     |            | 12        | 21                 |     | 00     | 12                          |        |   |    |     |         |   |              | 20   | 00   |      |      |         |    | 20                                      |                    | 49 G<br>67 G                |          |     | 20    | 0     |       | 00    |          |     | 30   | 0         |         |       |
| 11                | 7551              | 20               | 6220    |             | 36   | 90   | 1020           | 1     |     |            | 36        | 3                  | 28  | 6191   | 22                          | 21     |   |    |     | 1952    |   |              | 25   | 52   | 25   | N 1  | 1052    |    | 3521                                    | N N                | 7160                        |          |     |       |       | 10    | 10.1  | 3331     | 1 1 | 111  |           | 1731    | 73    |
| 020               | 2 00002           | 000              | 000000  |             | 500  | 0000 |                | 100   |     |            | 9000      | 1000               |     | 90054  |                             |        |   |    |     | 2 00026 |   |              | 500  |      |      |      | 20035 9 |    | 28488                                   |                    | 192900                      | 64.288   |     | 00022 | 60020 | 00100 | 77722 | 2 777 00 |     | 0000 | 0266      | 02000   | 00010 |
|                   |                   |                  |         |             |      |      |                |       |     |            |           |                    |     |        |                             |        |   |    |     |         |   |              |      |      |      | •    |         |    |   |                    |                             |          |     |       |       |       | •     |          |     |      |           |         |       |
| 916               | 000166            | 9110             | 1100    | 9.017       | 0017 |      | 421000         | 1100  |     |            |           |                    |     | 000203 |                             |        |   |    |     | 000211  |   | 212888       | 0.21 | 1200 | 1200 | 1288 | 12000   |    | 000220                                  |                    | 000222                      | 7788     |     |       | 288   |       | 200   | 052000   |     | 200  | 903       | 000235  | 005   |

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|        |     |               |     |    |     |  |       |       |   |     |            |      |      |     |                  | get peinter to second arg | store result in it |        |        |       |    |            |                |   |                 |        |   |                 |       |      |     |            |       |     |     |                |       |       |     |       | ast psinter to and 1 |      |       |        | the beunda  |        |       |       |     |        |              |        | reference last page |
|--------|-----|---------------|-----|----|-----|--|-------|-------|---|-----|------------|------|------|-----|------------------|---------------------------|--------------------|--------|--------|-------|----|------------|----------------|---|-----------------|--------|---|-----------------|-------|------|-----|------------|-------|-----|-----|----------------|-------|-------|-----|-------|----------------------|------|-------|--------|-------------|--------|-------|-------|-----|--------|--------------|--------|---------------------|
|        |     |               |     |    |     |  |       | 2010° |   |     |            |      |      |     |                  | -                         | 00100              |        |        |       |    |            | xed_fetch_petr |   |                 |        |   |                 | 17.64 | 010  |     |            |       |     |     |                |       |       |     |       |                      |      |       | 25575  | pounds pair |        |       |       |     |        |              | 2010.1 | 0010+Z              |
|        |     | 1d_inst! save |     |    |     |  |       |       |   |     |            |      |      |     | fetch_succeeded! | 9000                      | 519                | ことうちゃん |        |       |    | xed_fetch: | Dex            |   | xed_tetch_pairt |        |   | xed store cairs |       | 048  |     | xed_store! | Dex   |     |     | tegal_bft save |       |       |     |       |                      |      |       |        |             | return |       |       |     |        | 1 Ted Spunda | 81     | 90                  |
| 149    | 120 | 151           |     |    |     |  | <br>X | 2     |   | 2   | R          |      | -    | 151 | 156              | 139                       | 31                 | 161    |        |       | 16 | 3          | 5              | 5 | 8               | 101    |   | 170             | 171   | 172  | 173 | 21         | 22    | 112 | 178 | 179            |       |       |     |       | 1 40                 | 1.81 | 2     |        | 1           | 1.65   |       |       | 106 | 187    |              |        | R                   |
| 00     |     | 20            | 00  | 00 | 00  |  |       |       |   |     |            |      |      |     |                  |                           |                    |        |        |       |    |            |                |   |                 |        |   |                 |       |      |     |            | D     |     |     | 20             |       |       |     |       |                      |      |       |        |             |        |       |       |     | 20     |              | -1 0   |                     |
| 6101   |     | 3521          | 25  | 25 | NS  |  |       | N     |   |     | 21         | 2    |      |     |                  | 52                        | 20                 | 3      | 0731   | 10    |    |            | 7170           |   | 2               | 1922   |   |                 | 36    | 1951 |     | į          | LICO  |     |     | 3521           | 2     | 2 4   |     | 2 4   |                      | 10   | 12    | 0      |             | 73     | 73    | 10    |     | 8110   |              | 2361   | 90                  |
| 024    |     | 0022          | 8   |    | 22  |  |       |       |   |     |            |      | 924  |     |                  | 10                        |                    | 320    | 010    | 124   |    | 1          | 292            |   |                 |        |   |                 | 21    |      |     |            | -     |     |     |                |       |       |     |       |                      |      |       | -      | 9           | 02     | 10    | 1     |     | 808    |              |        | 0                   |
| 6 00   |     | 6 00          | •   | 0  | -   |  |       | 8     | • |     | <b>a</b> ( | 9 (  | 0    |     |                  | 80                        | -                  | 90     | 6 00(  | 00    |    |            |                |   |                 |        | 3 |                 |       | -    |     |            |       |     |     | 999            |       |       | - P |       |                      |      | 0     | •      | 000         | •      | 6 00  | 0     | -   | 000    | 00           | 00 2   | 0                   |
|        |     |               |     |    |     |  |       |       | ( | B ( |            |      | •    |     |                  |                           |                    |        |        |       |    |            | •              |   | 4               | 0 (    |   |                 |       |      |     |            |       |     |     |                |       |       |     |       |                      |      |       |        |             |        |       |       |     |        |              | • •    |                     |
| 000237 |     | 24            | 288 | 8  | 200 |  |       |       |   |     |            | <288 | 6220 |     | 45200            | 99254                     | 0 0 2 5 5          | 95298  | 000257 | 99269 |    | -          | 19288          |   | 9288            | 292999 |   |                 | 10264 | 65   |     | 000266     | 99788 |     |     | 267            | 8.288 | 1/200 |     | 14690 | 0275                 | 9226 | 00277 | 00.300 | 10200       | 00302  | 20203 | 48284 |     | 587888 |              | 90760  | 10200               |
|        |     |               |     |    |     |  |       |       |   |     |            |      |      |     |                  |                           |                    |        |        |       |    |            |                |   |                 |        |   |                 |       |      |     |            |       |     |     |                |       |       |     |       |                      |      |       |        |             |        |       |       |     |        |              |        |                     |

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|  | this time reference beyond MK  | shuld fault<br>get painter to return point<br>store the value as get illegalit |  | pcede<br>eft 9 bits<br>arg 8 instruct<br>arg 2                     | arg 2 is a pointer to segment<br>store the instruction in the segment<br>new execute the instruction |
|--|--|--|--|--|--|
|  | ants stat  | shuid fault<br>get peinter<br>store the v                                      |  |  | 878 2 18<br>84918 779<br>298 84916   |
|  | 8912,*<br>8910,*<br>0<br>180080  | bounds_pair<br>apit.*  |  | ap 12. *<br>59 18<br>87 9. 6<br>87 9. 6                            |  |
|  | 44000  | anone<br>ata   |  | 1 40 0000 0 0 0000 0 0 0 0 0 0 0 0 0 0 0                           | ret urn  |
| 1 4 0 1 0 0 1 1 1<br>9 0 1 0 0 1 1 1         |  |  | arg_81<br>try_001  |  |  |
| 222  | ****   | 200  | 488  | 207<br>208<br>209<br>210<br>211                                    | 212<br>213<br>213<br>213<br>213<br>213<br>213<br>213<br>213<br>213                                   |
| 000  |  | 0 000  |  |  | N88 N88  |
| 1521   | 2521<br>3521<br>3521<br>3521<br>3521<br>3521<br>3521<br>3521   | 1952   |  | 3521<br>2561<br>2361<br>7360<br>8760<br>8760<br>8760               | 7561<br>7561<br>7161<br>1731<br>1731<br>1731<br>6101   |
|  | 77722  |  | SI INSEN   | ENNESSA  | 110 800 800  |
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|      |                    | 00000       | <br>  |         |      |      |      |     |     |     |     |     |     |  |
|------|--------------------|-------------|-------|---------|------|------|------|-----|-----|-----|-----|-----|-----|--|
|      | * 1 ***            | S UDV E     | *2    | 3.      | ;    | 5,   | •    | 5.0 | •   | .6  | 10. | 11. | 12. |  |
|      |                    |             |       | 15.     | 16.  | 17.  | 18.  | 19. | 28. | 21. |     |     |     |  |
|      | arg_0              | E VDV E     | 205.  | 230.    |      |      |      |     |     |     |     |     |     |  |
|      | 3050 Q             | I AQD E     | 52.   | 97.     | 110. |      |      |     |     |     |     |     |     |  |
| 171  | deo j sese q       | E AQN E     | 109.  | 114.    |      |      |      |     |     |     |     |     |     |  |
| 386  | b eunds_pair       | I AQDS      | 184.  | 198.    | 199. |      |      |     |     |     |     |     |     |  |
| -    |                    | S UDVE      |       | 28.     |      |      |      |     |     |     |     |     |     |  |
| 2    | c 1 ec             | - 107 5     | 13.   | 50.     |      |      |      |     |     |     |     |     |     |  |
|      | cleck.             | I AGO S     | 10%.  |         |      |      |      |     |     |     |     |     |     |  |
| 20   | centret            | I AQD S     | 26.   | 99,     | 126. |      |      |     |     |     |     |     |     |  |
| 9    | 918                | 1 100       | 14.   | 55.     |      |      |      |     |     |     |     |     |     |  |
| 254  | fetch_succeeded    | 1 AGD 8     | 139.  | 158.    |      |      |      |     |     |     |     |     |     |  |
| 240  | 1 d_ inst          | S UDV 2     |       | 151-    |      |      |      |     |     |     |     |     |     |  |
| 31.0 | 1 1 1 99 1 D 1     | 1 107 5     | ;     | 193.    |      |      |      |     |     |     |     |     |     |  |
| 128  | Isci               | B ubv 1     | 18.   |         |      |      |      |     |     |     |     |     |     |  |
| 130  | 1                  | 5 ubv 2     | .61   | 60.     |      |      |      |     |     |     |     |     |     |  |
|      | 1 dbr              | a ubv a     |       | 100     |      |      |      |     |     |     |     |     |     |  |
| 0    | 1.41               | S ubv 1     |       | 16.     |      |      |      |     |     |     |     |     |     |  |
| 267  | ieasi bi           | a ubw       | -     | . 7 .   |      |      |      |     |     |     |     |     |     |  |
| -    | at older time      | 1 101       | 23.   |         |      |      |      |     |     |     |     |     |     |  |
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|      |                    |             | .1.   | 92.     | :    |      |      | 194 |     |     |     |     |     |  |
| 150  | 200                | 1 107 8     | 21.   | 99.     |      |      |      |     |     |     |     |     |     |  |
| 3    | 10010101           | 1 1978      | 25.   | 98.     | 118. |      |      |     |     |     |     |     |     |  |
| 177  | 1.000              | 1 1478      | 117.5 | 123.    |      |      |      |     |     |     |     |     |     |  |
| 20   | 1 202              | 1 1475      |       | .0.     |      |      |      |     |     |     |     |     |     |  |
| 140  |                    | 1 AQD 5     | 28.   | .60     |      |      |      |     |     |     |     |     |     |  |
| 5    | 5 8 V0_87 00       | S UDV E     | 24.   | 111.    | 119. | 127. | 128. |     |     |     |     |     |     |  |
| 10   | scu                | s uby t     |       | 32.     |      |      |      |     |     |     |     |     |     |  |
| •    | s dor              | 1 147 5     | 12.   | 45.     |      |      |      |     |     |     |     |     |     |  |
| 10.3 | 5 BCB              | 1 1008      | 16.   | 65.     |      |      |      |     |     |     |     |     |     |  |
| 11.0 | saic               | subv :      | 17.   | 78.     |      |      |      |     |     |     |     |     |     |  |
|      | svs. Infe          | S vbv S     | 104.  |         |      |      |      |     |     |     |     |     |     |  |
| ~    | 1 180 Of 1811476   | S ubv I     | 22 .  | 105.    |      |      |      |     |     |     |     |     |     |  |
| 331  | Try op             | s ubv s     |       | 2.86.   |      |      |      |     |     |     |     |     |     |  |
| 261  | xed fetch          | E UDV E     | 134.  |         |      |      |      |     |     |     |     |     |     |  |
| 212  | xed fet cher       | 1 Adv 2     |       | 132.    |      |      |      |     |     |     |     |     |     |  |
| 292  | xed fetch peir     | subvi       | 164.  | 156.    |      |      |      |     |     |     |     |     |     |  |
| 265  | xed store          | a units     |       | - 34.   |      |      |      |     |     |     |     |     |     |  |
| 224  |                    | a ubvi      |       | 4 4 2 4 |      |      |      |     |     |     |     |     |     |  |
| 9.6  |                    |             |       |         |      |      |      |     |     |     |     |     |     |  |
| - 07 | Lied_oform_nex     | SUDV 1      | 179.  | 175.    |      |      |      |     |     |     |     |     |     |  |

FATAL ERRORS ENCOUNTERED

## APPENDIX B

## Unlocked Stack Base Listing

This appendix contains listings of the four modules which make up the code needed to exploit the Unlocked Stack Base Vulnerability described in Section 3.3.3. The first two procedures, di and dia, implement step one of the vulnerability – inserting code into emergency\_shutdown.link (referred to in the listings as esd.link.) The last two procedures, fi and fia, implement step two of the vulnerability – actually using the inserted code to read or write any 36 bit quantity in the system. Figure 9 in the main text corresponds to di and dia. Figure 10 corresponds to fi and fia. As in Appendix A, obsolete 645 instructions are flagged by the assembler.

call ring0\_get\_Ssegptr ("", "emergency\_snutdown.iing", w/p. code); /\* get segment number of emergency\_shutdewn.iink /\* offset within emergency\_shutdown.iinh at which to patch \*/ call dic (sp. addrei (mvp. mvoffset)); /\* call ale program fe finish \*/ do I = mvoffset to mvoffset+11, mvoffset+14 to mvoffset+23; /\* zero evi all but 2 instruction patch \*/ call fi (addrei (mvp. 1), """b); /\* eiher words were filled from registers \*/ call ring0\_get\_ssegptr ("", "signaller", sp. code); /\* get segment number of signaller If code "= 0 then ring0\_get\_ssepptr entry (char (\*), char (\*), ptr, fixed pin), COMPILATION LISTIMG OF SEGMENT di Compiled by: Muitics PL/I Compiler, Version II of 38 August 1973. Compiled on: 84/18/74 1838.9 edt Med 4 /\* Procedure to place trapdoor in emergency\_shutdown.iink \*/ dia entry (ptr. ptr). Rvoffset fixed bin int static init (296), code fixed bin, commerr\_ entry outions (variable), i fixed bin, fi entry (pir, bit (36) aligned), call commert (code, "di"); go to error! if code "= 0 then returns AVD PTT 100 deciare so otr. Opt Lons ? BED + pue pr ec; 110-10 110 --91 86 8 7 7 7 8 21 -15 22 23 \* 20220

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LINE LOC 23 000132 del 6 set ret 26 27 27 Initial del 6 ret 25 25 25 26 26 26 del 6 set ret 22 25 25 27 27 external del 6 ret 15 22 53 ring1\_0+1\_6+0 011 22 ATTRIBUTES AND REFERENCES Internal ref 25 25 27 27 dc1 6 set ref 15 16 18 external dcl 6 ref 18 external dcl 6 ref 25 external dcl 6 ref 27 externel dol 1 ref 1 dol 18 ref 18 73 LINE LOC 22 000101 doi 6 set ref 15 25 rpd\_1000\_1\_10\_bp LINE LOC 78 000100 29 000217 builtin function fixed bin(17.8) fixed bin(17.8) fixed bin(17.8) ext\_entry 51 a 71 c 30 b 12 LINE LOC 18 800 861 28 800 200 DATA TYPE 2 pointer pointer entry Isbel entry ALTLA entry entry THE FOLLOWIN EXTERNAL OPERATORS ARE USED BY THIS PROGRAM. THE FGLLOWING EXTERNAL ENTRIES ARE CALLED BY THIS PROGRAM. 8101 8 98 228 3 LOC STORAGE CLASS External precedure di uses 118 words of automatic 000102 automatic 000014 constant 000020 constant 000026 constant L0C 000057 000161 Deelo 3 automatic 000104 automatic 000100 automatic 000012 constant 000020 constant 000061 constant NO EXTERNAL VARIABLES ARE USED BY THIS PROGRAM. constant Symbol 312 127 return NAYES DECLARED IN THIS COMPILATION. LINE 16 27 NAME DECLARED' BY CONTEXT OR IMPLICATION. STORAGE REQUIRENENTS FOR THIS PROGRAM. NAMES DECLARED BY DECLARE STATEMENT. NAMES DECLANED BY EXPLICIT CONTEXT. L1nk 278 22 elb call\_ext\_out\_oasc call\_ext\_out L 0C 3000 25 000150 OFFSE 1 St St Tex ? 220 ring8\_get\_6 se go fr 0 b] ac 1 454 LINE LJC 1 000017 25 000134 IDENT IF LER -110-002 COB\_BFF\_ 8vo 1 1 sat Langth a ddr a l PL OL Start Cod 419 9 10

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"so tradoor isn't interrupted "here's the trapdoor! "signation does the ipila." "pointer to return point "ptr to signaller "save stack ptr "ptr to esd.link into sp "so trandoor can return "transfer to signation "pointer to esd. Link "Instructions in AQ Trestore stack ptr return\_pointer.do\_it\_etr return\_pointer-18 SEGMENT > user\_dir\_dir>Druid>Karger>compiler\_pool>dia.aim 04/11/74 1824.7 edf Thu 11st oid\_object oid\_call symbols ALM Version 4.4. September 1973 02/13/74 1728.8 edf Med return\_tast 40\_11\_ptr.º do\_17\_ptr ap12.\* xed\_inst 0018. \* ----\*\* 1 0° \* .... - N L L • 10 Imieit CL7 181 ..... ----CMO Dex. return\_insta xed\_inst 1 . 1 p HOM B .... えいいんないのの . -... 0 0 0 0 0 0 00860 77742 77720 06032 ASSEMBLY LISTING OF S ASSEMBLED ONI OPTIONS USED: ASSEMBLED DVI ASSEMBLER CREATED: 0 . N . . • ..... NN N ø . -. .... . . --. . . -..... ...... Ü

NO LITERALS

MANE DEFINITIONS FOR ENTRY POINTS AND SEGUEFS

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|---|---|-------------|----------|-----------------|
| 2 |   | 200000      |          |                 |
| 2 | * | 000012      | 000001   |                 |
| 4 | : | 003 144     | 191 191  |                 |
| - |   | 110000      | 0 0000 0 |                 |
| * | ; | 000000      | 2 00000  |                 |
| - | : | 014 163     | 171 155  | sy shot _ table |
| - | : | 142 157     | 154 137  |                 |
| - | : | 164 141     | 142 154  |                 |
| 2 | : | 145 000     | 000 000  |                 |
| 7 |   | 000016      | 0 00000  |                 |
| 5 | : | 000037      | 200200   |                 |
| - | : | 010 162     | -        | Tat. Inr        |
| 3 | : | 137 164     | 145 170  |                 |
| - | : | 10. 000     | •        |                 |
| 2 | : | 000023      |          |                 |
| 2 | : | 010 162     | 145 154  | rei_link        |
| 2 | : | 137 154     | 151 156  |                 |
| 1 | : | 153 000     | 888 888  |                 |
| - |   | 0 0 0 0 3 0 |          |                 |
| - | : | 912 162     | 145 154  | rel_symbol      |
| 3 | : | 137 163     | 551 147  |                 |
| 1 | : | 142 157     | 154 000  |                 |
| 2 | : | 000000      | 0 00000  |                 |
| - |   | 2           |          |                 |

NO EXTERMAL 4 ANFS

TO TRAP POINT ER WORDS

TYPE PAIR BLJCKS

INTERNAL EXPRESSION NORDS

## LINKAGE INFORMATION

| 00 00 00 | 0032 0 | 00 00 00 | 0 0000 | 0000 | 0000 00600 | 0010 0000 | 000 0000 | 7770 0000 | 0033 00 | 7766 3 | 20 2000 | 29 0000 | 7773 71 | 0 0000 | 0 0000 |
|----------|--------|----------|--------|------|------------|-----------|----------|-----------|---------|--------|---------|---------|---------|--------|--------|
| •        | •      |          | •      | •    | •          | 2 0       | 2 0      | -         |         |        |         |         |         |        |        |

(entry\_sequence)
SYMBUL INFORMATION

SYNBOL TABLE HEADER

| 0010 | 2000 | 1010 | 0042 | 0145 | 167671 | 0156 | 0335 | 0000 | 0000 | 0000 | 2000 | 1410 | 1100 | 5415 | 1411 | 9151 | 5115 | 5605 | 2314 | 4515 | 6204 | 6736 | 41.04 | ž    | ž    | 0 40040 | ě.   | 919919 | 948848 | 0 10010 |
|------|------|------|------|------|--------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-------|------|------|---------|------|--------|--------|---------|
| 000  | 100  | 000  | 100  | 000  | 141711 | 0000 | 1741 | 0000 | 0000 | 0000 | 9000 | 0000 | 1000 | 4120 | 3710 | 4012 | 631  | 4006 | 1015 | 6016 | 4214 | 6107 | 4415  | 1001 | 100  | 100     |      | 010010 | 60     | 010010  |
|      |      | -    | •    |      |        |      |      |      |      |      |      |      |      | •    |      |      |      |      |      |      | •    |      |       | 6    |      |         |      |        |        |         |
|      | 18   | 200  | 200  | 100  | 500    | 900  | 1001 | 010  | 1011 | 210  | 610  | 4100 |      | 9700 |      | 8200 | 1200 | 122  | 0023 | 4200 | 6290 | 9200 | 1200  | 0200 | 1500 | 0032    | 8833 | 1203   | 1935   | 9298    |
|      |      |      | 643  |      | ÷      | •    | ē    | ē    |      |      | ë    | š    | ž    |      | ē    | ē    |      | :    | :    | :    | :    | :    | 5     | 8    | :    | :       | -    |        | ŝ      | 8       |

MULTICS ASSEMBLY CRUSS REFERENCE LISTING

| Value | S y mbo l      | Source file |        | Line number |     |
|-------|----------------|-------------|--------|-------------|-----|
|       | * TexT         | d i a t     | 2.     |             |     |
| 0     | 118            | diat        | •<br>• |             |     |
| 52    | do_lt_ptr      | dist        | 5      |             | 15. |
| 53    | return_inst    | Gial        | 6,     |             |     |
| 05    | return_pointer | dial        | 5      |             |     |
| 20    | xed_inst       | dist        | 5      | 24.         |     |

NO FATAL EREDRS

pat segment mumber of emergency\_shutdown.ilm lf code "= 8 then go to error: 1f fix then call fia (sp. addrei (mvp. uveffset+12), fixp. merd); /\* call! aim pregrem to finish \*/ eise call fla8gia (sp. addrei {mvp. avoffset+12), fixp. mord)} /\* pointer to word to be read/written \*/ call ringl\_get\_tregotr ("", "signaller", sp. cede); /\* get segment number of signaller \*/ If cede "= 8 then /\* Entry to read out 36 bits \*/ call ringl\_get\_stegptr ("", "emergency\_shutdown.link", m/p, code)} /\* ring0\_get\_\$segpt entry (char (\*), char (\*), ptr, fixed pin), aveffset fixed bir int static init (296), COMPILATION LISTING OF SEGNENT fl Compiled by: Muitics PL/I Compiler, Version II of 30 August 1973. Compiled on: 84/10/74, 1848.9 edf Med fis entry (ptr. ptr. ptr. bif (36) aligned). cemerr\_ entry cotions (variable). fistgia entry (ptr. ptr. bif (36) aligned). call con\_err\_ (code, "fi"); return; word bit (36) all gred. fix bif (1) aligned; fix = "1"b; entry (fixp, word); 4 /\* Entry to store 36 bits \*/ code fixed bin. proc (fixp, word)] 19.0. = X11 fixp ptr. 3 dec lare Options: mep . 25. ptr. pue t b s C01 001 918 1 1 1 1 58 122220 26 22 30 30 N#04 10 212 1 5 -2

107

L OC 000074 000074 

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 30 ¥83 ring8\_get\_\$soget ATTRIBUTES AND REFERENCES 5 dc1 28 Fe( 28 28 dc1 32 Fe( 32 37 externel dc1 1 Fef 1 externel dc1 23 Fef 23 Internal ref 38 38 39 LINE LOC 20 000040 39 000201 NE LOC 26 000037 38 000154 3 builtin function fixed bin(17,0) Tixed bin(17.0) ext\_entry 1143914 51011c 314 12 LOC 010 031 DATA TYPE pointer peinter pointer bit ( 36 ) b11(1) I e q e I entry entry 1 = Q = I entry entry entry entry L INE 23 37 6 THE FOLLOWING EXTERNAL OPERATORS ARE USED BY THIS PROGRAM. Cali\_ext\_out\_desc cell\_ext\_gut return THE FOLLOWING EXTERNAL ENTRIES ARE CALLED BY THIS PROGRAM. External procedure fi uses 114 words of automatic storage Dets 224 99 LOC STORAGE CLASS LOC 808838 888116 000102 automatic 000012 constant 88864 5 constant 888876 constant 888821 constant 888832 constant 000104 automatic 000105 automatic 00010 sutomatic parameter parameter NO EXTERNAL VARIABLES ARE USED BY THIS PROGRAM. constant 000016 constant 000014 constant 000020 constant 326 130 Symbol NAVES DECLARED IN THIS COMPILATION. LINE 20 36 NAME DECLARED BY CONTEXT OR IMPLICATION. STORAGE REQUINCENENTS FOR THIS PROGRAM NAMES DECLARED BY DECLARE STATEMENT. NAMES DECLARED BY EXPLICIT CONTEXT. Link 304 22 110 L OC 0000 26 0001 15 OFF SE T LINE 34 Tex† 0 224 00] 001 0 rings\_set\_sage tr 100 02 0 000 02 0 **IDENTIFIER** \_\_\_\_\_\_\_ COM\_BFF\_ Evol feet -LINE 1125912 Cossed Length addre. **TOTN** Start P LON epec 11xp XI. 110 2 8 108

|   |                       |               |           |                |              |           |                   |      | 1104           | : 8                           |           |            |    |         |                      |          |        |   |     |                    |    |       |    |            |           |            |                  |       |         | Ink         |                         |   |
|---|-----------------------|---------------|-----------|----------------|--------------|-----------|-------------------|------|----------------|-------------------------------|-----------|------------|----|---------|----------------------|----------|--------|---|-----|--------------------|----|-------|----|------------|-----------|------------|------------------|-------|---------|-------------|-------------------------|---|
|   |                       | 36 6118       |           |                | stered       |           | 81 er e           |      | - In esd.      |                               |           | 1102       |    | 1000    | petch                | tra bolz |        |   |     | 1 36 bits          |    |       |    |            | argument  |            |                  |       |         | n esd. iint | a 10116                 | • |
|   |                       | store         |           |                | 8            |           | TO KNOTO TO STOTE |      | L. "           |                               | signelier | to signal! |    | t s.pex | and 16 bits to patch | 4005 TTa |        |   |     | "antry to read out |    |       |    |            |           |            | to where to read |       |         | trapdoor in | "signalier does fra ipt |   |
|   |                       | 0 t           |           |                | bits to      |           |                   |      | PIL TO Trapdoo | 10 10                         |           | 5          |    | deer    | 10                   | 5        | -et un |   |     | y to 7             |    |       |    |            | to output |            | to whe           |       |         | to tre      | 11147                   |   |
|   |                       | Tentry        |           |                | -36          |           | LIC               | 1    |                | - 110                         | 1 ta      | "transf    |    | Trap    |                      | Tree     | pue    |   |     | "antr              |    |       |    |            | -te       |            | "otr             |       |         | - 110       | 116 1 S.                |   |
| oid_cail symbols<br>September 1973<br>edf Med |                       | · fixp. wordp |           |                |              |           |                   |      |                |                               |           |            |    |         |                      |          |        |   |     |                    |    |       |    |            |           |            |                  |       |         |             |                         |   |
|   |                       | 471 · 0       |           | · •            | •            |           | •                 | •    | - 1            | 619                           | •         | •          |    |         | •                    |          |        |   |     |                    |    |       |    |            | 1         | • •        |                  | •     |         | (           | ra_p-10                 |   |
|   | ***                   |               |           | 60<br>60<br>60 | 101d         | 9 1 0     | 8014s*            | 0100 |                | 160.01                        | 100       |            |    | 5       | L xo.                | 110      |        |   |     |                    |    |       |    | ap 18.     | 10740     | 8016. *    | 1 XD             | 2014s | 5010. * | tr.         |                         |   |
|   | A LUCA                |               |           | 4 <b>4</b>     | stą<br>eepbp | 00        | 10                | 4    |                | đđ                            | a .       |            |    | tiald   |                      | Intibit  | こしつまし  |   |     | ~                  |    |       |    | 9          | 0         | <b>a</b> c |                  |       |         | •           | 0                       |   |
| syabols<br>1973                               |                       |               |           | 38             |              | 9 9 9 9 9 |                   |      |                | eebp                          |           | 1          |    | E       |                      | E        |        |   |     |                    |    |       |    | e app o    | 5100p     |            | Cipbp            |       |         | 1912        |                         |   |
|   |                       |               |           |                |              |           |                   |      |                |                               |           |            |    | 4       | 1015 00              |          |        |   |     |                    |    |       |    |            |           |            |                  |       |         |             |                         |   |
| September                                     |                       | 1101          |           |                |              |           |                   |      |                |                               |           |            |    |         |                      |          |        |   |     | 91.01              |    |       |    |            |           |            |                  |       |         |             |                         |   |
|   |                       |               |           | •••            | 22           | 33        | 4                 | 54   | 15             | 39                            | 2 2       | 21         | 88 | 8       | 8 0                  | N        | 8      | 8 | 6 8 | R                  |    |       |    | <b>P</b> 1 | 31        | 5 16       | *                | A     | 聘業      | 61          | F 3                     |   |
| old_object<br>ersion 3.4.                     |                       | 5             |           |                | 9 0<br>N     | 20        | 50                |      |                |                               |           | 28         |    |         |                      |          |        | - |     |                    | :: |       | :: | 20         |           | 5          |                  | •     |         |             |                         |   |
| 0 5   | 00000<br>0000<br>0000 | 1521          | 25112     | 195            | 112          | 129       | 12                |      | =              | 2                             |           | 1          |    |         | 263                  |          | 731    | - | ł,  | 123                |    | 1251  |    |            |           |            |                  |       |         |             |                         |   |
| ALN 4   |                       | 2             |           | 223            | 22           |           | *                 |      | 12             | 19 1<br>1<br>1<br>1<br>1<br>1 |           | •          |    |         | 52 7                 | •        |        | • |     |                    |    | 12 29 |    |            |           |            | -                |       | -2 4    | 0 M         | 9.87                    | 1 |
|   |                       |               |           | 333            |              |           |                   |      |                |                               |           | •          |    |         |                      |          |        | 2 |     | 2 2                |    | 7774  | ·  | 23         |           |            | 9                |       |         |             |                         |   |
| AT 69   |                       |               | • • • • • |                |              |           |                   |      | •              |                               |           | •          |    |         | •                    | •        |        | • |     |                    |    | NN    |    |            |           |            |                  |       |         |             | 100                     | 1 |
| 540   |                       |               | ::::      |                | •            | • •       | •                 |      |                | •                             |           | •          |    |         |                      |          |        |   |     |                    |    |       |    |            |           |            |                  | = :   |         |             |                         | ) |
| LEG   |                       |               |           |                | 1            | 2100      | 110               | 919  | 110            |                               | 22        | R.         |    |         |                      |          | 2.2    |   |     |                    |    | 5     |    | 12         |           | 24         |                  | 33    |         | 13          |                         |   |
| OPT LONS<br>ASSEMBLI                          | :::                   | ::            |           |                |              |           |                   |      |                |                               |           | i          |    |         |                      |          |        |   |     | 22                 | 8  |       |    |            | 28        | 2          | 2 2              | 23    | 25      |             |                         |   |
| P S S   |                       |               |           | U              |              | 90        |                   |      | 90             | 9 4                           |           |            |    |         |                      |          |        |   |     |                    |    |       |    |            |           |            |                  |       |         |             |                         |   |

| "transfer to signatier | "trapdoor ked's these<br>"toad thru ptr<br>"store in output argument   | "and returns here |
|------------------------|--|-------------------|
| -1.<br>                | 11 x0. *   |                   |
| 0 sert                 | 104_510_11_500_1100_11000000 |                   |
| 319                    | \$3338   | <b>x</b>          |
|                        | 802  |                   |
| 7101 20                | 2363 20<br>7563 20   | 1619              |
| 00000                  |  | 00010 1 00010 0   |
| ::                     |  |                   |
|                        | 450000   | 090026            |

NO LITERALS

NAME DEFINITIONS FOR ENTRY POINTS AND SECOEFS

| 000000     2000000     0000000     151     151       0000000     5000000     0000000     1500000     1500000       00000000     1000000     1000000     1000000     1500000       00000000     1000000     1000000     1000000     100000       00000000     1000000     1000000     1000000     100000       00000000     1000000     1000000     1000000     100000       00000000     1000000     1000000     1000000     1000000       000000000     1000000     1000000     1000000     1000000       00000000000     10000000     1000000     1000000     1000000       000000000000000000000000000000000000   | 0000000     0000000     0000000       0000000     0000000     000000       0000000     0000000     000000       0000000     0000000     000000       0000000     0000000     000000       0000000     0000000     000000       0000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     0000000       000000     000000     0000000       000000     0000000     0000000       000000     0000000     0000000       0000000     0000000     0000000       0000000     0000000     0000000       0000000     0000000     0000000       0000000     0000000     0000000       00000000     0000000     0000000       00000000     0000000       00000000     0000000       00000000     0000000       00000000     0000000       000000000     0000000       00000000     0000000   | 0100     151     141     151     141       100     141     151     141     141       100     141     151     141     141       100     141     151     141     141       100     141     151     141     141       100     141     151     141     151       111     141     154     137     154     137       111     142     154     154     154       111     142     154     154     154       111     142     154     154     154       111     142     154     154     154       111     145     154     154     154       111     145     154     154     154       111     145     154     154     154       111     151     154     154     154       111     151     154     154     154       111     151     154     154     154       111     151     154     154     154       111     151     154     154     154       111     151     154     154     154       1111   |             | 000    | -     |            |
|--|--|---|-------------|--------|-------|------------|
| 000000     000000     000000     000000       000000     000000     000000     000000       000000     000000     000000     000000       000000     000000     000000     000000       000000     000000     000000     000000       000000     000000     000000     000000       000000     000000     000000     000000       000000     0000000     000000       000000     0000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     000000     000000       000000     0000000     000000       000000     0000000     0000000       000000     0000000     000000       000000     0000000     000000       000000     0000000     000000       0000000     0000000     000000       0000000     0000000     0000000       0000000     0000000     0000000 <t< td=""><td>000000       151       141       151       141         000012       000001       000001       111       151       141         000112       000112       000000       000000       000000       111         000112       000114       151       171       155       141       141         000112       000114       171       155       171       155       171       156         00017       00011       00011       142       157       154       137       142       152       154       171       155       154       171       155       154       155       154       155       154       156       166       156</td><td>000000     50     00001     151     141       000010     50     000010     151     141       000017     50     000010     000000       000017     50     000010     000000       000017     50     000010     000000       000017     142     154     137       000017     50     010     142     154       000017     50     011     142     154       000017     50     144     147     155       00017     50     144     147     155       00017     50     144     145     156       00017     50     145     155     154       000100     145     154     156       00110     145     154     156       00110     145     154     156       00110     151     155     154       001115     50     156     156       001115     50     151     156       001115     50     151     156       001115     50     157     156       001115     50     156     156       001115     50     157     156       0</td><td>20</td><td>020000</td><td>00</td><td></td></t<>   | 000000       151       141       151       141         000012       000001       000001       111       151       141         000112       000112       000000       000000       000000       111         000112       000114       151       171       155       141       141         000112       000114       171       155       171       155       171       156         00017       00011       00011       142       157       154       137       142       152       154       171       155       154       171       155       154       155       154       155       154       156       166       156   | 000000     50     00001     151     141       000010     50     000010     151     141       000017     50     000010     000000       000017     50     000010     000000       000017     50     000010     000000       000017     142     154     137       000017     50     010     142     154       000017     50     011     142     154       000017     50     144     147     155       00017     50     144     147     155       00017     50     144     145     156       00017     50     145     155     154       000100     145     154     156       00110     145     154     156       00110     145     154     156       00110     151     155     154       001115     50     156     156       001115     50     151     156       001115     50     151     156       001115     50     157     156       001115     50     156     156       001115     50     157     156       0   | 20          | 020000 | 00    |            |
| 00005     5     000001     151     141       151     151     151     151     151       151     151     151     151     151       151     171     155     171     155       151     171     155     171     155       151     171     152     157     154       151     151     151     152     157       151     151     151     152     155       151     151     145     156       151     151     145     156       151     151     145     156       151     151     154     156       151     151     156     156       151     151     156     156       151     151     156     156       151     151     156     156       151     151     156     156       151     151     156     156       151     151     156     156       151     151     156     156       151     151     156     156       151     151     156     156       151     156     156 <t< td=""><td>000001       11       15       11       15         00011       15       11       15       11         1       15       11       15       11         1       15       11       15       11         1       15       11       15       11       15         1       1       15       11       15       11       15         1       1       15       15       15       17       15         1       1       15       15       15       17       15         1       1       15       15       15       16       16         1       1       15       15       15       16       16       16         1       1       15       15       15       16       &lt;</td><td>000000       140       151       141         000000       151       151       141         000000       171       154       137         000000       171       154       137         000000       171       154       137         000000       141       142       154         000000       144       142       154         000007       144       142       154         000007       144       142       154         145       145       154       154         000007       145       145       156         000007       145       145       156         000007       145       145       156         000008       145       154       156         000008       145       154       156         000108       145       154       156         000108       157       154       156         000108       157       154       156         0001108       157       154       156         0001110       50       151       156         0001111       50       157       &lt;</td><td>64 99</td><td>-</td><td>15</td><td></td></t<>  | 000001       11       15       11       15         00011       15       11       15       11         1       15       11       15       11         1       15       11       15       11         1       15       11       15       11       15         1       1       15       11       15       11       15         1       1       15       15       15       17       15         1       1       15       15       15       17       15         1       1       15       15       15       16       16         1       1       15       15       15       16       16       16         1       1       15       15       15       16       <  | 000000       140       151       141         000000       151       151       141         000000       171       154       137         000000       171       154       137         000000       171       154       137         000000       141       142       154         000000       144       142       154         000007       144       142       154         000007       144       142       154         145       145       154       154         000007       145       145       156         000007       145       145       156         000007       145       145       156         000008       145       154       156         000008       145       154       156         000108       145       154       156         000108       157       154       156         000108       157       154       156         0001108       157       154       156         0001110       50       151       156         0001111       50       157       <  | 64 99       | -      | 15    |            |
| 00001     00001     00000       0001     00000     00000       11     15     14       11     15     14       11     15     14       11     15     15       11     15     15       11     15     15       11     14     15       11     14     15       11     14     15       11     14     15       11     14     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15       11     15     15   | 710000     151     141       710000     151     141       710000     151     151       711     154     155       711     154     155       711     154     155       711     154     155       711     154     154       711     154     154       711     154     154       711     154     154       711     154     154       711     154     154       711     154     154       714     154     154       715     154     154       714     154     154       714     154     154       714     154     154       714     154     154       714     154     154       714     154     154       714     155     155       714     155     156       714     155     156       714     155     156       714     155     156       714     155     156       714     155     156       714     155     156       714     155     156 <td>711       151       141         711       151       141         711       151       141         711       151       171         711       151       171         711       151       171         711       151       171         711       151       151         711       151       155         711       142       151         711       142       151         711       142       151         711       145       145         711       145       145         711       145       145         711       145       145         711       145       170         711       145       171         711       145       171         711       151       155         711       151       155         711       151       155         711       151       155         711       151       155         711       155       155         711       155       155         711       155       1</td> <td>63</td> <td>980808</td> <td>0</td> <td></td>   | 711       151       141         711       151       141         711       151       141         711       151       171         711       151       171         711       151       171         711       151       171         711       151       151         711       151       155         711       142       151         711       142       151         711       142       151         711       145       145         711       145       145         711       145       145         711       145       145         711       145       170         711       145       171         711       145       171         711       151       155         711       151       155         711       151       155         711       151       155         711       151       155         711       155       155         711       155       155         711       155       1   | 63          | 980808 | 0     |            |
| 00007     500014     00000     151     141       00072     1     154     157     54     137       00072     1     1     1     155     137       00072     1     1     1     1     155     137       00077     1     1     1     1     1     1       00077     1     1     1     1     1     1       00077     1     1     1     1     1     1       00077     1     1     1     1     1     1       00077     1     1     1     1     1     1       00077     5     00071     000000     000     000       00017     5     000017     000000     000     000       00110     1     1     1     1     1       00111     5     1     1     1     1       001110     5     1     1     1     1       001110     5     1     1     1     1       001110     5     1     1     1     1       001110     5     0     000     000     000       001111     5     0  | 00007     5     000010     050002     5     5     000000       7     1     1     1     1     1     5     5     0       7     1     1     1     1     1     5     5     0     0       7     1     1     1     1     1     5     1     5     1       7     1     1     1     1     1     1     5     1     5       7     1     1     1     1     1     1     5     1       7     1     1     1     1     1     5     1       7     1     1     1     1     1     5     1       7     1     1     1     1     1     1     1       7     1     1     1     1     1     1     1       7     1     1     1     1     1     1     1       7     1     1     1     1     1     1     1       7     1     1     1     1     1     1     1       7     1     1     1     1     1     1     1       1   | 00007     50     00014     00000       71     50     00000     50     50       00072     14     151     154     135       00072     14     141     152     137       00077     14     142     154     137       00077     14     142     154     137       00075     14     142     154     147       00077     14     142     154     157       00077     14     145     154     154       00077     14     145     154     154       00077     14     145     154     154       00077     14     145     154     154       000700     147     145     154     170       00110     14     145     154     170       00110     14     151     155     171       00110     157     151     155     171       001110     157     154     155     171       001113     137     151     155     171       001113     137     155     155     171       001113     137     155     155       001113     137  |             |        | 00    |            |
| 00071     5     00000     030002     5     5     00000       11     15     137     15     137       11     12     15     137       11     14     14     15       11     14     14     15       11     14     14     15       11     14     14     15       11     14     14     15       11     14     14     15       11     14     14     15       11     14     14     16       11     14     14     16       11     14     14     16       11     14     14     16       11     14     16     16       11     14     16     16       11     14     16     16       11     14     16     16       11     14     16     16       11     16     16     16       11     16     15     16       11     16     16     16       11     16     15     16       11     16     15     16       11     16     16  | 00071     5     00000     030002       111     15     137       111     142     154     137       111     142     154     137       111     142     154     137       111     142     154     137       111     142     154     137       111     142     154     137       111     142     154     137       111     145     114     145       111     141     145     154       111     141     145     154       111     141     145     154       111     141     145     154       111     141     145     154       111     141     155     156       111     151     155     156       111     151     155     156       111     151     155     156       111     151     155     156       111     151     155     156       111     151     156     156       111     151     156     156       111     151     156     156       111     151     156  | 000071       50       00000       000002       5       57       171       155       137         00077       10       147       154       137       154       137         00077       10       147       154       137       154       137         00077       10       147       154       154       147       154       154         00077       15       154       147       147       154       154       154         00077       5       0000       000       000       000       000       000         000101       5       154       154       154       154       154       154         0001012       5       000000       0000       000       000       000       000         000110       5       157       154       155       155       156       171       156         0001110       5       00003       0000       000       000       000       171       155         0001110       5       157       155       155       156       171       156         0001113       5       157       155       155   |             | 20     | 5     | 110        |
| 00071     3     01     15     15     5     37       00073     1     1     15     15     15       00075     1     1     1     15     15       00075     1     1     1     1     1       00075     1     1     1     1     1       00075     1     1     1     1     1       00077     1     1     1     1     1       00077     1     1     1     1     1       00076     1     1     1     1     1       1     1     1     1     1     1       00007     1     1     1     1     1       00017     1     1     1     1     1       00018     1     1     1     1     1       00118     1     1     1     1     1       00118     1     1     1     1     1       00118     1     1     1     1     1       00118     1     1     1     1     1       00118     1     1     1     1     1       00111     1     1 <t< td=""><td>00071       34       171       155       5       9       171       155       5       9       171       155       5       9       171       155       5       171       155       5       171       155       5       171       155       171       155       171       155       171       155       171       151       171       <td< td=""><td>700071     300002     571     155     171     155       700073     142     142     154     137     142     154       700075     145     142     154     137     154     137       700076     145     142     154     154     154       700077     155     155     152     154     154       7000077     155     155     155     155     154       7000007     157     154     154     156       700101     15     154     155     154       700101     15     154     155     155       70110     157     154     155     156       70111     15     155     155     155       70111     15     155     155     155       70111     157     155     155     156       70111     157     155     155     156       70111     15     155     155     156       70111     157     155     155     156       70111     157     157     156     156       70111     15     155     156     156       701113     157     157</td><td></td><td>000014</td><td>8</td><td></td></td<></td></t<>  | 00071       34       171       155       5       9       171       155       5       9       171       155       5       9       171       155       5       171       155       5       171       155       5       171       155       171       155       171       155       171       155       171       151       171 <td< td=""><td>700071     300002     571     155     171     155       700073     142     142     154     137     142     154       700075     145     142     154     137     154     137       700076     145     142     154     154     154       700077     155     155     152     154     154       7000077     155     155     155     155     154       7000007     157     154     154     156       700101     15     154     155     154       700101     15     154     155     155       70110     157     154     155     156       70111     15     155     155     155       70111     15     155     155     155       70111     157     155     155     156       70111     157     155     155     156       70111     15     155     155     156       70111     157     155     155     156       70111     157     157     156     156       70111     15     155     156     156       701113     157     157</td><td></td><td>000014</td><td>8</td><td></td></td<>   | 700071     300002     571     155     171     155       700073     142     142     154     137     142     154       700075     145     142     154     137     154     137       700076     145     142     154     154     154       700077     155     155     152     154     154       7000077     155     155     155     155     154       7000007     157     154     154     156       700101     15     154     155     154       700101     15     154     155     155       70110     157     154     155     156       70111     15     155     155     155       70111     15     155     155     155       70111     157     155     155     156       70111     157     155     155     156       70111     15     155     155     156       70111     157     155     155     156       70111     157     157     156     156       70111     15     155     156     156       701113     157     157  |             | 000014 | 8     |            |
| 00072     01     171     155     137       00073     14     142     154     137       00075     14     142     154     137       00075     15     100     000     000       00077     5     00021     000000       00010     14     145     154       00010     137     145     170       00010     137     145     156       00110     137     154     151       00110     137     154     156       00110     137     154     156       00110     137     154     156       00110     137     154     156       00110     137     156     156       00111     5     0000     00       00111     5     154     155       00111     5     157     155       00111     5     156     160       00111     5     154     155       00111     5     154     155       00111     5     155     155       00111     5     154     155       00111     5     155     155       001111     5   | 00072       01       171       155       137         00075       14       142       154       137         00075       15       145       154       137         00075       15       145       154       137         00075       15       145       154       154         00075       15       00000       000       000         00017       15       145       170       161         00111       137       145       170       156         001105       16       151       155       156         001105       16       151       155       156         001105       15       151       156       161         001105       15       151       156       161         001105       157       151       156       161         001105       157       156       156       161         001115       157       156       156       161         001115       157       156       156       161         001115       157       156       156       161         001115       157       15  | 01072     01     17     15     137       01073     14     14     14     15       01075     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     14     14       14     14     14     15     16       14     14     15     15     15       14     15     15     15     16       15     15     15     15     16       16     15     15     15     16       16     15     15     15     16       16     15  | -           |        | 0000  |            |
| 00073     147     154     137       00075     145     142     154       145     145     162     154       145     145     154     154       145     145     154     154       145     145     154     154       146     147     145     154       141     141     145     154       141     141     145     170       141     144     145     170       141     145     154     154       141     154     154     154       141     154     154     156       141     154     154     156       141     154     154     156       141     154     154     156       141     154     156     156       141     154     156     156       141     157     155     156       145     154     156     156       145     156     156     156       145     156     156     156       145     156     156     156       145     156     156     156       145     156 <td< td=""><td># 00073     1 + 1     1 + 2     1 5 + 1     1 + 2</td><td>00073       142       154       137         000075       154       142       154         000077       149       142       154         000077       149       142       154         000077       149       145       154         000077       149       157       154         000077       149       154       154         000107       141       145       170         001112       141       145       170         001110       141       145       154         001110       141       151       156         001110       157       151       156         001111       157       151       156         001111       59       100       171       156         001111       59       152       155       156         001111       59       157       156       156         001111       59       157       156       156         001111       59       157       156       161         001111       59       157       156       156         001111       50       157<td></td><td>14 16</td><td>71 15</td><td>Vabol</td></td></td<>   | # 00073     1 + 1     1 + 2     1 5 + 1     1 + 2  | 00073       142       154       137         000075       154       142       154         000077       149       142       154         000077       149       142       154         000077       149       145       154         000077       149       157       154         000077       149       154       154         000107       141       145       170         001112       141       145       170         001110       141       145       154         001110       141       151       156         001110       157       151       156         001111       157       151       156         001111       59       100       171       156         001111       59       152       155       156         001111       59       157       156       156         001111       59       157       156       156         001111       59       157       156       161         001111       59       157       156       156         001111       50       157 <td></td> <td>14 16</td> <td>71 15</td> <td>Vabol</td>  |             | 14 16  | 71 15 | Vabol      |
| 00075       145       142       154         000075       145       000       000       000         5       00021       000001       000       000         00010       117       145       154       170         000111       117       145       170       100         000112       117       145       170       100         000112       117       145       170       100         000116       15       145       155       170         00110       137       145       155       170         100110       137       151       156       111nk         100111       15       151       155       151         00111       15       151       155       151         00111       15       151       155       151         00111       15       151       155       151         001113       137       155       155       151         001113       137       155       155       151         001113       137       155       155       151         001113       157       155   | 00075       145       142       154         000077       5       0002       000       000         000177       5       00001       000       000         000117       5       00001       145       154         000111       117       145       154       170         001112       117       145       145       154         001105       147       145       154       170         001105       147       145       154       154         001107       157       155       145       155         001112       157       155       145       155         001112       137       155       145       155         001112       137       155       145       155         001112       147       155       145       155         001113       147       155       155       161_stynbo         001113       147       155       155       161_stynbo         001113       147       155       155       161_stynbo         001113       147       155       155       155         001113       157<  | 00075       145       142       154         000075       145       000       000       000         000017       5       000011       000       000       000         000010       10       145       154       145       170         000101       10       145       145       154       145       170         000101       10       145       145       170       145       170         000101       10       145       145       151       156       170         000105       10       145       145       151       156       170         000105       10       151       151       155       171       155         000105       10       151       155       145       156       171       155         000111       10       151       151       155       171       155       171       155         0001113       137       151       155       171       155       171       155         0001113       137       151       155       155       161       161       161       161       161       165       161 <td></td> <td>15</td> <td>54 13</td> <td></td>   |             | 15     | 54 13 |            |
| 00075       5       000010       000000         00017       5       000010       000000         000100       117       145       155         000100       117       145       155         000100       117       145       155         000100       117       145       155         000100       117       145       155         000100       137       151       155         00110       137       151       155         00110       15       151       155         00110       15       151       155         00111       5       00033       0000         00111       5       00033       0000         00111       5       152       155         00111       5       157       155         00111       5       157       155         00111       5       157       155         00111       5       157       155         001113       5       157       155         001113       5       157       155         001115       6       00001       156   | 00075       5       000000       000000         00017       5       000010       000000         00010       0       010100       000000         00010       0       000000       000000         00010       0       17       145       170         00010       0       17       145       170         00010       0       17       145       170         00010       0       145       154       170         00110       0       137       151       155         00110       0       157       151       156         00111       5       00033       00000       000         00111       5       00033       00000       000         00111       5       157       151       155         00111       5       157       155       154         001113       5       157       155       155         001113       5       157       155       155         001113       5       157       155       155         001113       5       157       155       155         001113  | 00075       5       00071       00000         00017       5       00011       00000         00010       117       145       155         00010       117       145       170         00010       117       145       170         00010       117       145       155         00010       117       145       156         00010       137       151       155         00010       137       151       155         00010       137       151       156         000110       137       151       156         000110       137       151       155         000111       5       00033       0000         000111       5       152       155         000111       5       157       151       155         000111       5       157       154       155         000111       5       157       155       171         000111       5       157       155       171         000111       5       157       155       171         000111       5       157       156 <t< td=""><td></td><td>11</td><td>51 24</td><td></td></t<>   |             | 11     | 51 24 |            |
| 000075       50       00000       00000       7       15       7       1   | 000075       50       000000       7010002         000100       10       145       175       7010002         000101       10       145       170       145       170         000101       10       145       170       145       170         000102       10       145       155       701       145       170         000103       10       145       151       155       701       161       1110         000105       137       151       155       155       155       701       110         000105       00       137       151       156       755       755       755         000105       00       152       145       155       755       755       755         000112       0       0       157       155       755       755       755         001113       30       137       155       755       755       755       755         001113       30       142       157       155       755       755         001115       80       00000       156       754       000       157         001115 <t< td=""><td>000077       50       000000       7         000101       10       145       154         000101       11       145       170         000101       11       145       170         000101       11       145       170         000101       11       145       170         000102       145       145       170         000103       10       151       155       161         000110       15       151       155       161         000111       5       00033       0000       000         000111       5       157       151       156         000111       5       153       171       155         000111       5       157       151       156         000111       5       157       156       171         000111       5       157       155       161         000111       5       157       156       171         000111       5       157       156       171         000111       5       157       156       171         000111       5       157       156</td></t<> <td>000075 00 1</td> <td>8</td> <td>00 00</td> <td></td>   | 000077       50       000000       7         000101       10       145       154         000101       11       145       170         000101       11       145       170         000101       11       145       170         000101       11       145       170         000102       145       145       170         000103       10       151       155       161         000110       15       151       155       161         000111       5       00033       0000       000         000111       5       157       151       156         000111       5       153       171       155         000111       5       157       151       156         000111       5       157       156       171         000111       5       157       155       161         000111       5       157       156       171         000111       5       157       156       171         000111       5       157       156       171         000111       5       157       156  | 000075 00 1 | 8      | 00 00 |            |
| 000100     10     15     15     15       000100     10     145     170     145     170       000102     10     145     170     000     000       000102     10     145     155     155     160       000105     10     137     151     156     160       000105     10     137     151     156     160       000105     10     151     156     160     160       000107     15     151     156     151     156       000107     10     157     151     156       000107     0     137     151     156       000112     0     1012     152     155     155       000113     137     163     171     155       000113     137     163     171     155       000113     142     157     155     151       000114     142     157     155     155       000113     142     157     155       000114     142     157     156       000115     0     156     156       000116     157     155     156       001115     0   | 000100       00       000100       00       00000       00 <td>000100       10       145       154       701         000101       10       145       170       145       701         000102       10       145       170       000       000       000         000102       10       145       170       000       000       000       000         000105       10       145       151       151       155       151       156         000107       00       137       151       155       151       156       171       155         0001110       50       00033       00000       000       000       000       171       155       171       1</td> <td>00076 50</td> <td>200</td> <td>00000</td> <td></td> | 000100       10       145       154       701         000101       10       145       170       145       701         000102       10       145       170       000       000       000         000102       10       145       170       000       000       000       000         000105       10       145       151       151       155       151       156         000107       00       137       151       155       151       156       171       155         0001110       50       00033       00000       000       000       000       171       155       171       1  | 00076 50    | 200    | 00000 |            |
| 000100     10     145     154     170       000102     10     145     170     145     170       000102     10     144     000     000     000       000105     10     100     145     154       000105     10     137     145     155       000105     10     137     151     156       000107     10     137     151     156       000107     10     137     151     156       000107     10     137     151     156       000117     10     100     000     000       000112     0     127     155     155       000113     137     155     155     161       000113     137     155     155     161       000113     137     155     155     161       000114     142     157     155     161       000115     0     157     155     161       001113     142     157     155     161       001115     0     156     155     161       001115     0     156     155     161   | 000110     10     145     154     17       000112     11     145     170     145     170       000113     50     1000     000     000     000       000105     10     151     155     151     156       000105     10     151     151     156     151       000107     10     151     151     156     151       000117     10     151     156     151     156       000112     151     152     145     156       001112     10     121     155     145       001112     10     137     155     145       001112     10     137     155     145       001113     10     152     145     155       001113     10     152     145     155       001113     10     152     145     155       001113     10     156     155     160       001113     10     156     155     160       001113     10     156     156     160       001113     10     156     156     160       001114     10     156     156     160    <  | 00110     10     145     154     17       001101     10     117     145     170     170       001102     10     145     154     170     170       001105     10     100     000     000     000       001105     10     137     154     151     156       0001105     10     137     151     156       0001105     10     137     151     156       0001105     10     137     151     156       0001105     10     137     151     156       0001105     10     125     151     156       000111     50     0003     00000     171       0001113     30     137     155     161       0001113     30     137     155     161       000111     50     01000     166     171       000111     50     00000     160     161       000111     50     156     155     161       000111     50     160     171     155       000111     50     160     160     161       000111     50     160     160     161       001111  | 000077 50   | 003    | 000   |            |
| 00111        | 00111       1 <td>00111       1<td>000100 no 0</td><td>16</td><td>515</td><td></td></td>   | 00111       1 <td>000100 no 0</td> <td>16</td> <td>515</td> <td></td>   | 000100 no 0 | 16     | 515   |            |
| 000102 00 104 000 000 000<br>000105 30 010 145 154 154 154 155<br>000105 30 010 142 145 154 154 156<br>000110 50 157 154 151 156<br>000110 50 150 300000<br>000111 50 152 145 154 155<br>000113 30 137 153 171 155<br>000113 30 137 153 171 155<br>000114 80 142 157 154 000<br>000114 80 145 157 154 000   | 000102 00 104 000 000 000<br>000105 30 010 145 154 151 156<br>000107 30 137 145 151 156<br>000107 50 157 151 156<br>000117 50 150 000 000<br>000112 50 152 145 154 155<br>000113 30 137 153 171 155<br>000113 30 137 153 171 155<br>000114 80 142 157 154 000<br>000114 80 142 157 155 155<br>000114 80 148 155<br>000114 80 148 157 155 155   | 00112 00 100 000 000<br>00113 55 00020 000 000<br>00110 55 010 145 154 151 156<br>00110 50 137 154 151 156<br>00111 50 137 154 154 154 154<br>00113 50 137 152 145 154<br>00113 50 137 153 171 155<br>00114 50 157 154 000<br>00115 50 157 154 000<br>00115 50 010 160 000<br>00115 50 012 157 154 000<br>00114 00 157 155 000<br>00115 50 010 20000  | 000101 10 1 | 37 164 | 11 50 |            |
| 000103 5a 00000 00000<br>000105 2a 01 142 145 154<br>000106 aa 137 154 151 156<br>000107 aa 137 154 151 156<br>000112 aa 012 152 145 154<br>000113 2a 137 163 171 155<br>000114 aa 142 157 154 000<br>000114 aa 142 157 154 000<br>000114 aa 142 157 154 000<br>000114 aa 142 157 154 000<br>000115 aa 012 157 154 000   | 000103 5a 00020 00000<br>000105 2a 01 142 145 156<br>000106 3a 01 142 145 156<br>000107 5a 030 000 000<br>000112 5a 09033 00000<br>000112 5a 012 152 145 155<br>000112 5a 012 152 145 155<br>000113 5a 137 163 171 155<br>000114 5a 142 157 154 000<br>000114 5a 142 157 154 000<br>000114 5a 142 157 154 000<br>000114 5a 142 157 156 000<br>000114 5a 142 157 155 155<br>000114 5a 142 157 155 155<br>000114 5a 142 157 155 155<br>000114 5a 142 157 155 155<br>000115 5a 012 155 155<br>000115 5a 012 155 155<br>000115 5a 012 155 155<br>000115 5a 012 155<br>000115 5a 015<br>000115 5a 015<br>000115 5a 015<br>000115 5a 015<br>000000  | 001103       5.9       000026       000000         001105       1.9       1.5       1.5       1.5       1.5         001105       1.9       1.3       1.5       1.5       1.5       1.5         001107       1.9       1.5       1.5       1.5       1.5       1.5       1.5         001110       5.9       000033       000000       000       000       000       000         001113       5.9       012       1.5       1.4       1.5       1.5       1.1       1.5         0001113       5.9       012       1.5       1.7       1.5       0.0       1.7       1.5         0001113       5.9       012       1.5       1.7       1.5       0.0       1.4       1.5         0001113       5.9       010011       1.5       1.5       0.0  | •           |        | 00 00 |            |
| A00105         10         11         145         154         151         160         137         145         154         151         156         160         110k         151         155         151         156         151         155         151         155         151         155         151         156         151         156         151         155         151         156         151         156         151         156         151         156         151         156         151         156         151         151         152         151 </td <td>A00105         Jac         B10         L5         145         154         Fol_link           000107         00         137         154         151         155         Fol_link           900107         00         137         154         151         156         Fol_link           900107         00         137         154         151         156         Fol_gayebo           900110         50         100033         000000         000         000         156           900112         50         137         152         154         155         Fol_gayebo           900113         30         137         153         171         155         Fol_gayebo           900113         30         157         154         000         156         Fol_gayebo           800113         30         157         154         000         156         Fol_gayebo           800113         30         163         171         155         Fol_gayebo           800113         30         163         171         155         Fol_gayebo           800114         40         160         170         156         Fol_gayebo</td> <td>A00105         Jac         B10         Let         145         154         151         156         160         161         160         161&lt;</td> <td></td> <td></td> <td>0000</td> <td></td> | A00105         Jac         B10         L5         145         154         Fol_link           000107         00         137         154         151         155         Fol_link           900107         00         137         154         151         156         Fol_link           900107         00         137         154         151         156         Fol_gayebo           900110         50         100033         000000         000         000         156           900112         50         137         152         154         155         Fol_gayebo           900113         30         137         153         171         155         Fol_gayebo           900113         30         157         154         000         156         Fol_gayebo           800113         30         157         154         000         156         Fol_gayebo           800113         30         163         171         155         Fol_gayebo           800113         30         163         171         155         Fol_gayebo           800114         40         160         170         156         Fol_gayebo   | A00105         Jac         B10         Let         145         154         151         156         160         161         160         161< |             |        | 0000  |            |
| 000106 00 137 154 151 156<br>900107 00 153 000 00<br>900112 00 012 152 145 154<br>000113 00 137 153 171 155<br>000115 00 137 154 000<br>000115 00 10001 00000  | 000106 00 137 154 151 156<br>900107 00 153 00 000 000<br>900112 00 012 152 145 154<br>000113 00 132 153 145 154<br>000115 00 012 153 171 155<br>000115 00 142 157 154 000<br>000115 00 198 157 154 000<br>000115 00 00001 00000  | 000106 00 137 154 151 156<br>900107 00 153 000 000<br>900112 00 012 152 145 154<br>000113 30 137 163 171 155<br>000115 00 138 163 171 155<br>000115 00 142 157 154 000<br>000115 00 00000 00000   | A00105 20 0 | 10 162 | 1 54  |            |
| 900107 be 153 000 000 000<br>000112 be 012 152 145 154 rel_symbo<br>000113 be 012 153 145 154 rel_symbo<br>000114 be 147 154 000<br>000114 be 142 157 154 000<br>000115 be 00000 200000  | 900107 be 153 000 000 000<br>000112 be 012 152 145 154<br>000113 be 012 152 145 154<br>000113 be 137 163 171 155<br>000114 be 145 157 154 000<br>000114 be 145 157 154 000<br>000115 be 00000 00000  | 900107 be 153 00 00 00 00 00 00 00 00 00 00 00 00 00  | 000106 00 1 | 1 2    | 51.1  |            |
| 000110 50 00033 00000<br>000112 00 012 152 145 154<br>000113 30 137 163 171 155<br>000114 00 142 157 154 000<br>000114 00 142 157 154 000<br>000115 00 000001 00000  | 000110 50 00033 00000<br>000112 00 012 152 145 154 rol_symbo<br>000113 30 137 163 171 155<br>000114 00 142 157 154 000<br>000114 00 142 157 154 000<br>000115 00 00000 00000<br>000115 00 00000 00000  | 000110 50 00033 00000<br>000112 00 012 152 145 154<br>000113 30 137 163 171 155<br>000114 00 142 157 154 000<br>000115 00 00000 00000<br>000115 00 00000 00000  | 07 00       | 3 .    | 0     |            |
| 000112 00 012 152 145 154 Fel_symbo<br>000113 00 137 153 171 155<br>000114 00 142 157 154 000<br>000115 00 000001 000000<br>XTERMAL VAMES  | 000112 00 012 152 145 154 Fol_symbo<br>000113 30 137 163 171 155<br>000114 00 142 157 154 000<br>000115 00 00000 000000<br>XTERMAL VAMES   | 000112 00 012 152 145 154 Fel_0<br>000113 00 137 163 171 155<br>000114 00 142 157 154 000<br>000115 00 00000 00000<br>XTERMAL VAMES   |             |        |       |            |
| 000113 30 137 163 171 155<br>000114 80 142 157 154 000<br>000115 80 000001 200000<br>XTERMAL VANES   | 20 137 163 171 155<br>20 142 157 154 000<br>20 88001 20000   | 000113 30 137 163 171 155<br>000114 80 142 157 154 000<br>000115 80 000001 200000<br>XTERMAL VAMES  | 12 00 0     | 2 15   | 45.1  | addana 1 a |
| 000114 80 142 157 154 00<br>000115 80 800001 20000<br>XTERNAL 4AMES  | 000114 80 142 157 154 00<br>000115 80 880001 00000<br>XTERNAL VANES  | 000114 80 142 157 154 00<br>000115 80 000001 00000<br>XTERNAL YANES   | 13 38 1     | 7 16   | 71 15 |            |
| 000115 00 000001 00000<br>Xtermal vanes  | 000115 00 000001 00000<br>Xternal vanes  | 000115 80 000019 00000<br>Xternal Vanes   | 14 88 1     | 2 15   | 54 90 |            |
| XTERMAL V  | XTERNAL 1  | XTERNAL 1   | 15 88       | =      |       |            |
|  |  |   | XTERMAL 4   |        |       |            |

G 2 111

NO 16

TYPE PAIR BLICKS

INTERNAL EXPRECISION NORDS

LINKAGE INFORMATION

STHOOL INFORTATION

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STHBOL TABLE HEADER

| 100000 | : | 000000 | 0010   |
|--------|---|--------|--------|
| 800001 | - | 240000 | 0000   |
|        | : | 000000 | 0100   |
| -      | : | 240000 | 1000   |
| -      | : | 00000  | 1014   |
| 200002 |   | 141711 | 067671 |
| -      |   | 000000 | 10154  |
| -      | : | 720061 | 63764  |
| -      | : | 000000 | 0000   |
| -      | : | 000000 | 60000  |
| -      | : | 000000 | 00000  |
| -      | : | 000122 | 0000   |
| -      | : | 000000 | 00147  |
| =      | : | 240000 | 1000   |
| =      | : | 003141 | 15415  |
| =      | : | 037101 | 11411  |
| -      | : | 040126 | 14516  |
| -      | : | 163151 | 15715  |
|        | : | 190810 | 05606  |
|        | : | 024040 | 12314  |
| 423880 | : | 160164 | 14515  |
|        | : | 142145 | 16204  |
|        | : | 061071 | 86706  |
|        | : | 146151 | 14184  |
|        | : | 810018 | 49640  |
|        | : | 010010 | 1040   |
|        | : | 010010 | 10010  |
|        | : | 010010 | 10010  |
|        | : | 040040 | 10018  |
|        | : | 0+00+0 | 10010  |
|        |   | 040040 | 10010  |

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|                 |  | NLTICS                                | ASSEMB  | CROSS | MULTICS ASSEMBLY CROSS REFERENCE LISTING                    | LISTIA | 9                                     |  |                   |       |  |
|-----------------|--|---------------------------------------|---|-------|---|--------|---------------------------------------|--|-------------------|-------|--|
| AE I No         |  | Symbol                                |   |       | Source file   | 1110   | Line                                  | Line pueber                            |                   |       |  |
|                 | 00000000000000000000000000000000000000 | 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 | • text<br>1 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 |       | 1191<br>1191<br>1191<br>1191<br>1191<br>1191<br>1191<br>119 |        | 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 | ************************************** | 26.<br>25.<br>25. | 4 6 F |  |
| NO FATAL ERRORS | ERRO RS                                | ľ                                     |   |       |   |        |                                       |  |                   |       |  |

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#### APPENDIX C

### Trap door in check\$device\_name Listing

This appendix contains listings of the trap door inserted in check\$device\_name in Section 3.4.5.2 and the modules needed to call the trap door. two Check\$device\_name is actually one entry point in the procedure check\$device\_index. The patches are shown in the assembly language listing of the code produced by the PL/I compilation of check\$device\_index. Most of the patches were placed in the entry sequence to check\$device\_index, taking advantage of the fact that PL/1 entry sequences contain the ASCII representation of the entry name for debugging purposes. Since the debugger cannot run in ring J, this is essentially free patching space. Additional patches were placed at each return point from check\$device\_name, so that the trap door would be executed whenever check\$device\_name returned to its caller.

Ag is a PL/1 procedure which calls the trap door to either read or write any 36-bit word accessible in ring 0. Ag uses zdata, an assembly language routine, to define a structure in the linkage section which contains machine instructions with which to communicate with the trap door.

The trap door algorithm is as follows:

1. Set the bp register to point to the argument rcode. Rcode has been bound to zdata\$code in the procedure call from 2g and must lie on an odd word boundary.

2. Compare the double word at up[1 with the key string in the trap door to see if this is a legitimate user calling. If the keys do not match, then just return. If the keys do match, then we know who this is and must proceed.

5. Do an execute double (XED) on the two instruction at up[3. This allows the caller to provide any instructions desired.

4. The two instructions provided by zdata at bp[3 and bp[5 are ldq bp[5 and stq bp[7. Bp[5 and bp[7 contain pointers to the locations from which to read and to which to write, respectively. These pointers are set in zg.

5. Finally, the trap door simply returns upon completion of the KED pair.

```
/* permdevice-index information accessed */
/* by the "devx" presented in the GIN calls */
/* megment number of the CCT for this user */
/* - only accessed by one process */
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   •
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              /* absolute address of base of DCW segment
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         aame of phraisel chaquel and $200 °/
#200 number of this device */
LFT channel number of this device */
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          start of device description */
                                                                                                                                                                                                                                                                                                                                                                                                                                                            device configuration table "/
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    -
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                /* pointer to safety DCW pair */
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              /* status channel used by GIN
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             ON 12 direct channel ./
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            /. BER VALE STAN NID "/
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     /* Channel Assignment Table for the SIOG Interface Nodule */
CONFILATION LISTIME OF SEGNENT CHOCK
COMPLIED by: Multice PL/I COMPLIAT, Version of 5 Uctober 1972.
Complied opt 92/21/74 1115.3 edt Thu
                                                                                                                                                                                                                                                                                                                                                                                                                                                            ::::::::::
                                                                                                                                                                                                                                                                                                                                                                                                                    /* Declaration for the Device Configuration Table */
                                                                                  checksdevige_index! proc (devi, dp. cctp. roode);
                                                                                                                                                                                                                                                                                       error_table_9918_so_cet ert firsd bin,
error_table_640v_st_sessed ert firse bin,
error_table_944v_st_sessed ert firse bin,
                                                                                                                                                                                                                                                                                                                                                                                     /* BEGIN IFCLODE ...... 404 ..... */
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     /* BEGIN ISCLUDE ...... C44 ..... ******
                                                                                                                                                                                                                                                                                                                                                                                                                                                   1 dct_999 ext aligned.
2 nder 21sed bin (17),
2 desc (300 /* dev_nan_max */ ).
3 dest_nam char (32),
                                                                                                                                                                                                                                                        del loss_check art antry!
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     /* BBD INCLUDE ..... det ..... */
                                                                                                                                                                                                                     Scl code fixed bin(17);
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       phicho fixed bin (3),
phichn fired bin (3),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       2 aba_base fixed bin (28).
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         direct_chan bis (1))
                                                                                                                                   49 918, "/
cets 919,
roode fired bin (17),
cotno fired bin (18);
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     dol 1 cat_gage art aligned.
                                                                                                                     deva Sixed bin (12).
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       phis nem char (32)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       stat base bit (3),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         (3 cctno bit (18),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      2 event fixed bis,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       2 devteb (200).
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       2 safep ptr.
                                                                                                                                   :
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       -
                                                                                                                    4.31
                                                                                                                                                                                                                                                                                                                                                                                                                                                    461
                                                                                                                                                                                                                                                                                       401
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      ----
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        20
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       80.01
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22 Inder pointing to sidest item in status queue "/ /\* inder pelating to houd of free status queue \*/ /\* status queue \*/ /\* fedesher to change sur\_jongth of est\_see in /\* hardeers header if you shange this • index peinting to and of Status guese "/ effet of dev list vithis dev segment. Sero is interpreted as deywiist not of status stats overflov come "/ /\* "devtab" entry declaraties size of dev list in dev's "/ /\* pointor to devisab entry of on if direct channel ./ OF 12 status lost "/ ret allocated "/ /. Guess again "/ 2 • • \* :: • : • • • : 2 • : • :

1 694\_94877 54204 (49) 9119704. (2 00440 bit (10); 2 604\_041 bit (10); 2 664\_144\_140 bit (10); 2 854\_144\_140 bit (10); /\* 28D ZPC50DW ..... 684 ..... \* \* 2 8444\_4 (512) £1204 bis (71); States\_lost bit (1), Gir\_shas bit (1)) unailgned! 3 padt Bit (1)) unsligned, 3 dev\_list\_ien bit (12), 2 OVERELOW ELXed MAD (18). 3 60V\_Fel\_s44 bit (18). 2 Freest fixed bin (101, stersatest bit (1), J dis\_chan bit (1). stat.s bit (10), end\_z bit (10). \$1011 pad bit (1). .... del de ptel ---1 -----

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/* device name */
                              dp = addr(cat_seg8,devtab (devt)) / sea 1f devtce accigned to this Progess */
sell ioam_check(ievt.code) / sea 1f devtce accigned to this Progess */
if sode "= 1 then do]
reode = error_table_fdev_nt_seend) /* it is not, so repert arror */
cdtp = null;
                                                                                                                                                                                                                                                                                        gcode = 0;
do detx = 1 to det_meg6,ndev/
14 det_seg8,desc (detx).dev_nam = devnam then return;
                                                                                                    econe = dp => dev_entry.cctno/
if cctno = 0 them do/
rcode = errer_table_sgim_po_cct/
cctp = null/
                                                                                                                                                                                                                                                                                                                                                                rcode = errer_table_0gip_badarg/
return:
                                                                                                                                                                                                                    devide name! onsry (devnam, dotx, rcode);
                                                                                                                                                                                                                                                                       /* setup and search the DCT for match "/
                                                                                                                                                        gnd)
gctp = baseptr (sctno)j
geturnj
                                                                                                                                                                                                                                                                                                                                            /* no matches, set complaint */
                                                                                                                                                                                                                                        devasa clar (*)6
CCLr Eined bin (17);
                                                                                                                                              reteral
                     10 - .....
                                                                                    returns
                                                                                             (pue
                                                                                                                                                                                                                                                                                                                                                                                                         (pue
                                                                                                                                                                                                                                        401
00000000
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VARIABLES DECLARED IN THIS CONFLLATION.

Etrec bin(34,0) fixed bin(]7.0] atructure tixed bin( 18.0) ELX66 Bin(17,01 ##### P##(32.0) bin()\*.01 to. () atd bezt \$4n(]2.01 [1244 b4n(]7.0) 10.17.01 b11(79,0) DATA TTPE structure structure structure char (32) cher (32) POLACer 948450 514(18) 5111 P44 132 b14(98) OLAter 01111 844 101 PEC 101110 326 98 b14(1) Sixed ) 11×04 CTX04 to a la Tree 3 × 8 4 1110 atty b1t ( **ntry** DALT. 11 ostono external static ostono external static external static external static link reference external static external static automatic external static externul static external static externel statio externel statio SETAMOTOR SETERAL STATIC external statio externel statio axternal static OP0034 axternal statia static static suternal static external static external static external static external statio sxternal static external static external static VARATABLUS DECLARED BT STPLECTT CONTEXTS Chegkedevice\_inder 000022 link reference device\_name 000016 link reference LOC STORAGE CLASS VARIABLES DECLARED BY DECLARE STATEMENT. PEFABOLOF Parameter Paranoter PETABOLOF Parameter Tenterna. axternal oxternal. external besed 1004 basad ..... besed ----..... 99840 ...... 000143 950000 010000 250000 920000 920000 000036 errer\_table\_\$sin\_no\_ect errer\_table\_ster\_stand error\_table\_sgin\_badere dev\_11st\_1es dev\_11st\_1es dev\_re1\_add dev\_re1\_add dese Lroct\_ghan status\_lost 1008 Dheck statue\_lost IDEWTIFIES lev\_ontgy stat\_bage 4 ba., base lot ..... Ir. chas Physes Physes Physes Foode Aotzaste 1:00 44444 4 4 8 6 H P.Safe tel. sctae 00130 sctne 7084 cota 240 2 119

ATTEUTES AND REFERENCES

level 2 usationed dc1 93 level 2 usationed dc1 93 srrar level 3 unaigned dc1 93 srrar level 3 ulageed dc1 31 level 1 aligned dc1 93 srrar level 3 aligned dc1 78 ref 131 srrar level 3 aligned dc1 78 ref 131 srrar level 3 aligned dc1 93 srrar level 3 unaigned dc1 93 srrar level 3 aligned dc1 93 srrar level 3 aligned dc1 93 srrar level 2 unaigned dc1 78 level 2 aligned dck 78 level 4 aligned dck 78 dcl 8 ref 111 112 417 srrr level 3 unsidened dcl 78 level 2 unsidened dcl 93 ref 111 dcl 8 ref 108 116 417 dcl 10 ref 105 106 dc1 10701 1 11400 401 31 401 125 ref 130 131 132 errar 10701 3 unaligned 101 16 reg 107

level 2 Aligned del 78 level 2 Aligned del 78 strar 1evel 3 aligned del 31 strereret 4 traducible ref 108 level 2 Aligned del 31 ref 130 level 2 Aligned del 78 95783 1evel 3 unaligned del 78 bret 2 unaligned del 93 erret 1evel 3 unaligned del 78 evel 2 aligned dol 78 level 3 unsidened dc1 78 level 3 aligned dc1 31 level 3 aligned dc1 31 ref 103 107 913 139 136 level 3 unslamed 4c1 78 usaligned dc1 93 pauligned del 93 aligned del 7 101 16 reg 313 Tudet ALL . 1evel 18221 10101 IT'SAY 1040 12937 FF67

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external irreducible ref external irreducible ref

FAREABLES DECLARED BY CONTEXT OR INFLICATION. 6442 basepte 8411

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bulltain function bulltain function bulltain function

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Internal ref 104 Internal ref 117 Internal ref 108 194

|                       |             |                        |              |             |            |              |            |             |            |               |        |               |               |               |            |   | 132          |             | 191340       | a3182                                   | -         | 2,41      | -          | #\$   103 .*    | ep176.*       | -            | 0.41        |              |      |       | 2           |        | ap176.*     |             |             |              | 10        |               | -            |  |
|-----------------------|-------------|------------------------|--------------|-------------|------------|--------------|------------|-------------|------------|---------------|--------|---------------|---------------|---------------|------------|---|--------------|-------------|--------------|---|-----------|-----------|------------|-----------------|---------------|--------------|-------------|--------------|------|-------|-------------|--------|-------------|-------------|-------------|--------------|-----------|---------------|--------------|--|
|                       |             | GZXIJ                  | TIXED        | TIND        | TXXD       | TIND         | TIXED      | TIND        | Ladax      |               | Chec . | -             | -             |               |            |   | 98K7         |             | 8            |   |           | 144       | *          | sts             | 144           |              | 14          | 67658        | 1    | atobe |             | Btaq   | aapp        | stopp       | -           | 44428        | at a ba   |               | stabb        |  |
| MA625<br>000012006016 | 00001300001 | 00000000000            | 100000000000 | 00000000033 | 0660000010 | 000000000000 | 7777777777 | 77777055543 | Lvebsdevi  | ekteriet.inde |        | 91 691 181 39 | 37 181 154 14 | 45 170 800 00 | 0000000000 | 000000000000000000000000000000000000000 | C0160 6279 0 | 0118 6260 0 | 00042 8729 2 | 000000000000000000000000000000000000000 | 1488 8879 | 0003 8360 | 1958 05100 | 6 00146 6501 20 | 2 1361 2361 2 | 00001 2360 0 | 0000 6280 0 | 00094 8701 2 |      |       | 0 1422 2340 | 9579 2 | 2 1258 9110 | 0102 2521 0 | 0 1258 5810 | 00104 8521 0 | 7730 3530 | 777727 3520 0 | 00110 2521 0 |  |
| DESCRIPTOR I          | 000001 AA   | COF8TARTS<br>000002 58 |              |             | as 200000  | 3e 500000    | 000001 88  | 000010 ME   | TOTA PROCE | Thy TO Ch     | 25000  |               |               | 1000          | 0004       | 0000 98                                 |              | 2000        | 0003         | 0003                                    |           | 2000      | 000        | 000032 88       |               |              | 2000        | 0003         | 0003 | 0.000 |             |        |             | 50000       | 90000       | 1+000        | 5000      | 10000         | 1000023 88   |  |

| 2.17.20 1 1.5.24.24.24.25 | - |      |     | 1000<br>1000<br>1000<br>1000<br>1000<br>1000<br>1000<br>100 | 891102.*<br>5911 00<br>6.46 00<br>891409 59<br>5913 591276697<br>4215531276697 | 000030<br>Fettra<br>187 |
|---------------------------|---|------|-----|---|--|-------------------------|
| TATABUT                   |   | 1111 | 505 |   |  |                         |
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STATERAST 1 OF LIES 105

0000021 = 0000031 008000 = 00001200001#

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|            |                   |            |         | -                 |      |      |      |       |                     |   |     |      |             |         |
|------------|-------------------|------------|---------|-------------------|------|------|------|-------|---------------------|---|-----|------|-------------|---------|
| 106        | 101               |            |         |                   |      |      | :    |       | 417                 |   | 122 |      |             |         |
| 1218       |                   | :          | 0000    |                   |      |      |      |       | 121                 |   |     |      |             |         |
|            |                   |            | 10 4    |                   |      |      |      | -     |                     |   |     |      |             |         |
|            |                   |            |         |                   |      |      |      | 111   |                     |   |     |      |             |         |
| 1          | -                 |            |         |                   |      |      |      | E .   | -                   |   |     |      |             |         |
| 18         |                   |            | - 01    |                   |      | 103  |      | - 010 |                     |   |     |      |             |         |
| TAPENDAT I | 05970<br>71728570 |            | - 01000 | FOLUTA<br>STATERT |      |      |      |       | Fettra<br>37A75KEPT |   |     |      |             |         |
| 111        |                   |            |         |                   |      |      |      |       | 111                 |   | 1   |      |             |         |
|            |                   |            |         |                   |      |      |      |       |                     |   |     |      |             |         |
|            |                   |            |         |                   |      |      |      |       |                     |   |     |      |             |         |
|            |                   |            |         |                   |      |      |      |       |                     |   |     |      |             |         |
|            |                   |            |         |                   |      |      |      |       |                     |   |     |      |             |         |
|            |                   |            |         |                   |      |      |      |       |                     |   |     |      | 36,*        | 00 00   |
|            |                   |            | 100     | -                 |      | · le | 108  |       | -                   | 8.400                                   |     |      |             |         |
|            |                   |            | -       | -                 | 1111 |      |      | 78    |                     | 1.14                                    |     |      |             |         |
|            |                   |            |         |                   |      |      |      |       |                     |   |     |      |             |         |
| 11         |                   |            |         |                   |      |      | A    |       |                     |   |     | E3:  |             |         |
| 33         |                   |            |         | 178               | Îss  | 111  |      |       | 128                 |   |     | :::  | :::         |         |
| -0         |                   | 000        |         | 0                 | 0000 |      | 000  |       | 0                   | 000000                                  | 0 0 |      |             | 00100   |
| 00         | 000               | <b>nnn</b> | 94      | •                 |      | 0    | ***  | 94    | •                   | -0                                      | -   |      |             |         |
| 101        | 2-0               | 999        | 197     | 5                 | 8823 | 101  | 0.00 | 1955  | 310                 |   |     |      |             |         |
| 0.00       |                   |            | no      | -                 |      | 01   | 404  | 00    | -                   |   | 0 - |      | 00000       |         |
| 000        | *000              | 000        | 773     | 063               | -000 | 8    | 000  | 771   |                     | 000000                                  | 0 0 |      | 00000       | 00000   |
| 00         | 000               | 000        | 777     | 0                 | 0000 | 00   | 000  | 77    | 0                   | 000000                                  |     |      | 000         |         |
| -          | •                 |            |         |                   |      |      |      |       |                     |   |     |      |             |         |
|            | :::               | 111        |         |                   | :::: | -    |      |       |                     | ::::::                                  |     |      |             |         |
|            |                   |            | ::      | 967               |      | -    |      | 00    | 0                   | 740000F                                 | : : |      | - 1919 1919 | 10000 F |
| 003        | 000               | 0.00       |         | •                 | 0000 |      | 000  | 000   | 001                 |   |     | 0000 | 00000       | 000000  |
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|        |          |            |          |        |     |      |      |      |      |         |        |                 |     |     |     |     | •    |     |         |     |       |    |       |          |         |          |      |         | 000174 |          |        |   |            |         |       |                     |          | 710000                 |         |
|--------|----------|------------|----------|--------|-----|------|------|------|------|---------|--------|-----------------|-----|-----|-----|-----|------|-----|---------|-----|-------|----|-------|----------|---------|----------|------|---------|--------|----------|--------|---|------------|---------|-------|---------------------|----------|------------------------|---------|
|        |          |            |          |        |     |      |      |      |      |         |        |                 |     |     |     |     |      |     |         |     |       |    |       |          |         |          |      |         | 6.10   |          |        |   |            |         |       |                     |          |                        |         |
|        |          |            |          |        |     |      |      |      |      |         |        |                 |     |     |     |     |      |     |         |     |       |    |       |          |         |          |      |         | 174    |          |        |   |            |         |       |                     |          |                        |         |
|        |          | C          |          |        |     |      |      |      |      |         |        |                 |     |     |     |     |      |     |         |     |       |    |       |          |         |          |      |         | 001000 |          |        |   |            |         |       |                     | 000174   |                        |         |
|        | 129      | 130        |          |        |     |      |      |      |      |         |        | 134             |     |     |     |     |      |     |         |     |       |    |       |          |         |          |      |         |        |          |        |   | 977        |         |       |                     |          | 140                    |         |
|        | 1233     | asz1       |          |        |     |      |      |      |      |         |        | HEX'S           |     |     |     |     |      |     |         |     |       |    |       |          |         |          |      |         |        |          |        |   |            |         |       | 1.7 2.0             |          |                        |         |
|        | Io       |            |          |        |     |      |      |      |      |         |        | 10              |     |     |     |     |      |     |         |     |       |    |       |          |         |          |      |         |        | 4        |        |   | -          |         |       | 01 1.1              |          | 11 10                  |         |
|        | #*       | -          |          |        |     |      |      |      |      |         |        | -               |     |     |     |     |      |     |         |     |       |    |       |          |         |          |      |         |        | -        |        | • | *          |         |       | -                   |          | -                      |         |
|        | STATEMER | 327232728  |          |        |     |      |      |      |      | 000 140 | 126000 | STATEREST STATE |     |     |     |     |      |     |         |     |       |    |       |          |         | 69 69    |      |         |        |          | 008483 |   |            |         |       | STATEMENT STATEMENT | return   | STATEMENT<br>STATEMENT |         |
| 00110e | ap   102 | sp   36. * | - 10 I O |        |     |      |      |      |      | 2010    | 20,1c  |                 |     |     |     |     |      |     |         |     | 10100 |    |       | 001 88   | sp176.* | 49   392 | 2.10 | 801 808 |        | ap 178.* | -22.50 |   | ap   36. * | 10120.* | 2     |                     | ap   409 |                        |         |
|        | sta      | espip      |          |        | 140 |      | 14.  |      |      | 022     | tal    | 1400            |     |     |     |     |      |     |         |     | 4455  |    | teblp | 1116     | eapp    | tably    | tas  | tra     |        | 101      | tra    |   | eaply      | ą       | 314   |                     | tra      |                        | -       |
| 00     | 30       | 20         | 20       | 00     | 01  | 20   | 20   |      |      | 5       | 8      | 00              | Q Q | 10  | 90  | 0   |      |     | 5       | 20  | 12    | 00 | 00    | 00       | 50      | 00       | 10   | 00      |        | 20       |        |   | 20         | 00      | 20    |                     | 00       | 0                      | 100 T   |
| 1561   | 1051     | 1701       | 3        |        | -   | 7561 | 90   | -    |      |         | ñ      | 174             | 320 | 760 | 042 |     |      |     | 7260    | 10  | 54    | 53 | -     |          | 2       | -        | -    | -       |        | 115      | 100    |   | 701        | 191     | 261   | 1                   | 101      | 101 0                  | TAODON: |
| 144    | 146      | -          | 36       | 25     | 5   | 96   | 16   | 5    | 1    |         |        | 18              | -   | 1   | 00  | 9   | -    | 0   | 0       | -   | 9     | -  | -     |          |         | 0        | ~    | -       |        | 9        | -      |   | *          |         | 5     |                     |          |                        |         |
| 00     | 00       | 000        | 00       | 8      | 000 | 0    | 0    | 0    | 00   |         | 2      | Ö               | ŏ   | 00  | ă   | 00  | 000  | 000 | 0000    | 0   | 0     | 51 |       | <u> </u> | 21      | 900      | 000  | •       |        | 0011     | 177    |   | 1000       | -       | an 19 |                     |          | 0063                   |         |
| •      | •        | •          |          |        |     |      | •    | -    |      |         |        | •               |     |     |     | •   |      |     |         |     |       |    |       |          |         | D        |      | •       |        | •        | -      |   | •          |         |       |                     | >        | 0                      | DURI    |
| •      |          |            |          |        | •   |      |      | •    |      |         | •      | -               |     |     |     |     |      | -   |         |     |       | -  |       |          |         |          |      |         |        |          |        |   |            |         |       |                     |          |                        | 0       |
| 000333 | 000134   | 56000      |          | r t 00 | 001 |      | 9018 | 1500 | 9100 |         | 2      | 001             | 100 | 100 | 100 | 100 | 2500 | 013 | 000 155 | 500 | 50    |    |       |          |         |          |      |         |        | 1000     | 1100   |   | 115000     | 100     | 1100  |                     | -        | 000175                 | te att  |

1. 2114 /\* .....y to read out 36 bits \*/
/\* structure passed to ring 8 \*/
/\* standard system arrer code \*/
/\* 72 oit key to prevent accidental use \*/
/\* 2 instructions to be XED\*ed by ring 8 \*/
/\* pir to read 36 bits; pir to stere 36 bits /\* Entry to patch 36 bits \*/ /\* call ring 8 \*/ db pfr. word bit (36) aligned; Mcs\_Schack\_device entry (cher (\*), fixed bin (17), fixed bin), dcfx fixed bin (17) init (0); COMPILATION LISTING OF SEGMENT 29 Compiled "yr muitics PL/I Compiler, Version II of 30 August 1973. Compiled ont 04/10/74 1843.4 edf Med . piri = dpi pir2 = addr (word); cali hcs\_Scheck\_device ("", dcfx, code); 1 zdatascode syt static aligned. 2 code fixed bin aligned. 2 key bit (72) aligned. 2 inst (2) bit (35) aligned. 2 inst (2) bir (35) aligned. entry (dp. word); ptr1 = addr (word); ptr2 = dp; go to comoni proc (do, word); returns Opt Lons 1 and 14 composit 291 dcl z 11 AND SH 213 ø σ -----2 

| ARE DIR GELARE STATEMENT.<br>ARE DIR GELARE STATEMENT:<br>BIBLE STATEM   | ICENTIFIER                           | OFFSET         | n<br>n   | STORAGE CLASS |         | DAT A TYPE   |                                 | ATTRIB   | ATTRIBUTES AND REFERENCES | REFERENC | CES    |     |
|--|--------------------------------------|----------------|----------|---------------|---------|--------------|---------------------------------|----------|---------------------------|----------|--------|-----|
| Control     00002  | MANES DECLARED OF                    | DECLARS STATSM |          |               |         |              |                                 |          |                           |          |        |     |
| Antic Stratt     Trant Stratt     T  |                                      |                | ABBA 2   |               |         | Lead biality |                                 |          | 401.3                     |          | 4      |     |
| Control  |                                      |                |          |               |         |              |                                 |          |                           |          | 4      |     |
| Control     Double control     Contro  |                                      |                |          |               | - 6     |              |                                 |          |                           |          | •      |     |
| 3     00012  | hes Scherk dayles                    |                | 4 10000  |               |         |              |                                 |          |                           |          |        |     |
| AED BY EARLICTI CONTEXT a TETLE DITTER<br>10 00012 etternal static Ditter<br>10 00012 etternal between betwee   |                                      |                |          |               |         |              |                                 |          | •                         |          |        |     |
| AE:0 BY EAPLICIT CONTEXT     100012 enternal static built?     100012 enternal static built?     100012 enternal static built3       AE:0 BY EAPLICIT CONTEXT     000112 enternal static built3     00112 enternal static built3     00112 enternal static built3       AE:0 BY EAPLICIT CONTEXT     000112 enternal static built3     00112 enternal static built3     00111 enternal       AE:0 BY EAPLICIT CONTEXT     000112 enternal static built3     00112 enternal static built3     00111 enternal       AE:0 BY EAPLICIT CONTEXT     000112 enternal static built3     00111 enternal     00111 enternal       AE:0 BY EAPLICIT CONTEXT     000112 enternal static built3     00111 enternal     00111 enternal       AE:0 BY EAPLICIT ON INPLICATION     00112 enternal     00111 enternal     00111 enternal       AE:0 BY EAPLICIT ON INPLICATION     00112 enternal     00111 enternal     00111 enternal       AU     001000     00112 enternal     00111 enternal     00111 enternal       AU     ENTERNAL ONE ENTERNAL     00111 hunctien     00111 enternal     00111 enternal       AU     1010     1010     1010     1010     1010       AU     1010     1010     1010     1010     1010       AU     1010     1010     1010     1010     1010       AU     1010     1010     1010     1010     1010 <td></td> <td></td> <td>7 18898</td> <td></td> <td></td> <td>107111</td> <td></td> <td>ABLLB</td> <td></td> <td></td> <td></td> <td></td>   |                                      |                | 7 18898  |               |         | 107111       |                                 | ABLLB    |                           |          |        |     |
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| 0b) ect     Text     Link     Symbol     Defa     Static       322     72     14     162     72     155     52     155       722     72     16     125     52     155     155     155       722     72     16     126     72     155     155     155       722     72     16     175     States     156     72     155       755     15     126     07     THIS     PROGRAM.     ext_onfry     ext_onfry       Uf_desc     76400     07     115     PROGRAM.     ext_onfry     ext_onfry       Uf_desc     76400     07     115     PROGRAM.     ext_onfry     ext_onfry       Uf_desc     76100     1715     PROGRAM.     ext_onfry     ext_onfry       156     ExtERMAL ENTRIES ARE CALLED OF THIS PROGRAM.     ext_onfry     ext_onfry     ext_onfry       166     ExtERMAL VARIABLES ARE USED OF THIS PROGRAM.     ext_onfry     ext_onfry     ext_onfry       166     ExtERMAL VARIABLES ARE USED OF THIS PROGRAM.     13     ext_onfry     ext_onfry       166     178     00001     113     ext_onfry     ext_onfry       166     12     00015     12     ext_onfry   | STORAGE REQUIRENEN                   |                | OGRAN .  |               |         |              |                                 |          |                           |          |        |     |
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| THE EXTERNAL OPERATORS ARE USED BY THIS PROGRAM.<br>U1_dence return ext_entry<br>THE EXTERNAL ENTRIES ARE CALLED BY THIS PROGRAM.<br>Ldevice<br>THE EXTERNAL ENTRIES ARE CALLED BY THIS PROGRAM.<br>THE EXTERNAL ENTRIES ARE USED BY THIS PROGRAM.<br>THE EXTERNAL PROFILES ARE USED BY THIS PROFRAM.<br>THE EXTERNAL PROFILES ARE USED BY THIS PROFRAM.<br>THE EXTERNAL PROFILES ARE USED BY THIS PROFRAM.<br>THE ARE ARE ARE ARE ARE ARE ARE ARE ARE AR  | External precedure                   | 29 4865 52 86  | rds ef   | eutematic s   |         |              |                                 |          |                           |          |        |     |
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|  | 10 00050                             |                |          |               |         |              |                                 |          |                           |          |        |     |

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ASSEMBLY LISTING OF SEGMENT > UPOT dir dir Druld>Karger>compiler\_pool>zdata.alm ASSEMBLED ON: 04/11/74 1826.1 ddf Thu OPTIONS USED: 11st old\_object old\_call symbols ASSEMBLED BY: ALM Version 4.4. September 1973 ASSEMBLER CREATED: 02/13/74 1720.8 ddf Med

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|   | "aske code addressable<br>"Instructions below must be even<br>"So pad here with 8<br>"system errer code<br>"system errer code<br>"22 bit way to compere in ring<br>"22 bit way to compere in ring<br>"32 for accidental invouriton<br>"36 for accidental invouriton" |
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NO LITERALS

NAME DEFINITIONS FOR ENTRY POINTS AND SEGDEFS

|          | •       |         | M AN Se    | EXTERNAL |
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|          | •       | 5000    |            |          |
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|          | 171 155 | 137 163 |            | 12000    |
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|          | 00000   |         |            | 200020   |

TTERNAL MANES

NO TRAP POINTER WORDS

TYPE PAIR BUCKS

INTERNAL EXPRESSION NORDS

LINKAGE INFORMATION

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SYMBOL INFORMATION

STMBOL TABLE HEADER

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MULTICS ASSEMBLY CROSS REFERENCE LISTING

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| Dueber    | 2. 6.<br>3. 13.            |
|-----------|----------------------------|
| Line      |                            |
|           |                            |
| Source    | zdata:<br>zdata:<br>zdata: |
| S y abe i | ceda<br>Lapure<br>Key      |
| Value     | 193                        |

NO FATAL ERRORS

#### APPENDIX D

## Dump Utility Listing

This appendix is a listing of a dump utility program designed to use the trap door shown in Section 3.4.5 and Appendix C. The program, zd, is a modified version of the installed Multics command, ring\_zero\_dump, documented in the <u>MPM Systems Programmers' Supplement</u> (SPS75). Zd will dump any segment whose SDW in ring zero is not equal to zero. In addition, zd will not dump the ring zero descriptor segment, because the algorithm used would result in the ring 4 descriptor segment being completely replaced by the ring U descriptor segment which could potentially crash the system. Zd will also not dump master procedures, since modifying their SDW's could also crash the system.

\* /\* initsm = 0 if we haven't initiated a segment • = "-nm" ! targ = "-nmme" then do! /\* user specified a segment number \*/
xt\_arg = 3;
11 cu\_sarg\_pfr (nmxt\_arg-1, tp, tc, code); /\* pick up the ascil for the segment name
code \_= 1 then do; ~ lerror\_table\_sneerg, error\_table\_gseginoun) fixed bin ext. Icqde, outi, i, ic, first, initsu, the\_same, next\_erg, offset, left, pg\_size, bound) fixed bine plot up the first ang (neme/number) cv\_ect\_check\_ entry (cher (\*), fixed bin) returns (fixed bin (35)). (com\_err\_, log\_) entry options (væriæbje). ring@get\_ssegptr entry (cher (\*), cher (\*), ptr, fixed bin). hcs\_sterminate\_nensee entry (ptr, fixed bin). hcs\_sinitiate entry (cher (\*), cher (\*), tixed bin, fixed bin, ptr, fixed bin). (2962f, 29) entry (ptr, bit (36) eligned). tell user he gave bad args "/ -.(""" get pointer to dota orea ľ đ This procedure prints out specified locations of d segment in octal format. It checks first to see if the segment has a counterpart in ring 3 and if not checks the given mage "/ 02 2 1 1 1 cu\_terg\_pir ext entry (fixed bin, pir, fixed bin, fixed bin), condition ext entry. expend\_peth\_ext entry (ptr. fixed bin. ptr. ptr. fixed bin); Compiled by: Nuitics PL/I Compiler, Version II of 38 August 1973. e C ę 2 \* "H", ""60 if cede = error\_isble\_Snearg | tc = 8 then do; call los\_ ("rzd segno/neme first count"); bdete (1925) bit (36) aligned based (eddr (deta)), overlay (811eft-1) bit (36) aligned based, (fp. datep. segptr) ptr. dirname char (158), an fixed bin, dreg\_word bit (36) aligned based (addr (daeg)), If targ = "-na" 1 targ = "-name" then do! count fixed bin (35), f (3) char (16) aligned static init (""6e call com\_err\_ (code, "rzd"); call cu\_sarg\_ptr (1, tp, tc, code) ; Cempiled on1 84/18/74 1842.6 edt Hed CONFILATION LISTING OF SEGNENT 20 targ char (tc) beact (tp). save\_acc bit(36) aligned, detep = sedr (dete); next\_erg = 31 date (1824) fixed bin, 1013181 dseg aligned. padi bit (19) unal. brd bit (8) unal. size bit (1) unal. pad2 bit (2) unal. acc bit (6) unals Letura: mane char (32), inites = 01 La Co stagetr ptri Options! map - Due proct 1 6u 12 21 u 1 -NNNN . 2 di • / 1 U 25 -----\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* \*\*\* \*\* 7 2 2 3 245 2 2 9 5 3 5 25

9

**b**-

, î î

|  | end;<br>go to get_name;<br>end; | <pre>naxt_arg = 2;<br/>l = cv_oct_check_ (farg, code);<br/>l = cv_oct_check_ (farg, code);<br/>l = cv_oct_check_ (farg, code);<br/>l = cv_oct_check_ (farg, code);<br/>l = cv_oct_check_ (farg, code);<br/>segptr = nul! ();<br/>call ring0_ort_sreptr ("", targ, segptr, code); /* get pointer te nul!(), seys den't have it yet */<br/>l = segptr = nul! () then do;<br/>l = segment */<br/>l = segment */<br/>l = code == 0 then go te alssing;<br/>l = code == 0 then go te alssing;<br/>l = code == 0 then go te alssing;<br/>l = code == 1 then l = code == error_table_srephonen then go te alssing;<br/>l = code == 1 then l = code == error_table_srephonen then go te alssing;<br/>l = code == 1;<br/>end;<br/>end;<br/>end;<br/>end;<br/>end;<br/>end;<br/>end;<br/>end</pre> | <pre>else segetr = bemeptr (1); /* get peinter to base ef segment */ 1f baseme (segptr) = "a"b</pre> | <pre>first = cv_ect_check_ (targ, code);<br/>if code == 8 then de;<br/>cali loa_ ("-RBed first word "a-B", targ);<br/>return;<br/>end;<br/>cali cu_Berg_Dfr (next_arg+1; tp; tc; code); /* get count of words to duep */<br/>if code = arren_rebla_Shoarg 1 tc = 8 then count = 1; else de;<br/>count = cv_ect_check(targ; code); /* convert count value */<br/>if code == 8 then de;<br/>count = cv_ect_check(targ; code); /* bed value */<br/>count = cv_ect_check(targ; code); /* bed value */<br/>end;<br/>end;<br/>end;<br/>end;<br/>end;<br/>end;<br/>end;<br/>end;</pre> |  |
|--|---------------------------------|--|--|---|--|
|--|---------------------------------|--|--|---|--|

| <pre>call zg(pfr(Mdsegpfr, baseno(se</pre> |
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| The set of |                    |          |                   |                 |  |
|---|--------------------|----------|-------------------|-----------------|--|
|   | OFFSE T            |          | LOC STORAGE CLASS | DATA TYPE       | ATTRIBUTES AND DEFERENCES  |
| MAMES DECLARED BY DEC   | DECLARE STATEMENT. | F NEWT.  |                   |                 |  |
| BCC   | 0(30)              | 002206   | 6 automatic       | P.1 + 1 + 1     |  |
| bolata  |                    |          | Desed             | 101 101         | level 2 packed unaligned doi 20 apt raf 110 114                  |
| Puol.   | 0(19)              | 0 002206 | 1.5               | NI+ (2)         | array dcl 7 set ret 126  |
| ponog   |                    |          |                   | *14-44 P1-14 P1 | level 2 packed unsilgned dol 30 set ref 118                      |
| code  |                    | 000100   |                   | fixed bin(17-0) | dc1 7 8ef ref 118 120 120  |
|   |                    |          |                   |                 | 20 81 83 84 85 85 85 85 81 85 87 85 86 87 88 89                  |
| count   |                    | 120000   | -                 | entry           | external dc1 7 raf 54 72   |
|   |                    | * TEANA  | SUTOBOTIC         | TAXed bin(35.0) | JCI 7 887 FBI 84 94 95 128 128 128 124 124 184 147 147           |
| cu_serg_bt  |                    | 000002   |                   |                 | 148  |
| cv_act_chack  |                    | 00000    |                   | ALLA            | externel dcl 7 ref 63 52 81 93                                   |
| dete  |                    | 000115   | autometic .       | entry series of | external dol 7 ref 61 87 95                                      |
|   |                    |          |                   | 10"/ LINTO DAXI | Brray dol 7 8et ref 61 126 131 131 131 131 135 135 135           |
| datap   |                    | 002120   | automatic         | animine.        | 152 155 159 150 150  |
| dirname   |                    | 602124   | -                 | Char (164)      | OCI 7 801 701 41   |
|   |                    | 002206   | -                 | #11 LOT 191     | unsitghed doi 7 set ret 66 66 68                                 |
| D TON . BOOD  |                    |          | _                 | bit (14)        | INVEL 1 DECIDE CCI 30 Set ref 184 105 111 116                    |
| and the second  |                    | 002176   |                   | cher (32)       | Unalized del 7 ant 105 111 116                                   |
| arrer_table_5 seguroun  |                    | 020020   | externel static   |                 | del 7 raf 44 82 94   |
| atmand asth   |                    | 000030   | externel static   |                 | del 7 rat 60   |
|   |                    | 4 50000  |                   | _               | external del 7 rat 64  |
| first   |                    |          | Internal static   |                 | initial array dol 7 sat raf 156                                  |
| hcs_Siniflats   |                    |          | 211000100         | Tixed Dir(17.8) | dc1 7 set ref 83 87 128 124 126 131 154                          |
| hcs_Stareinat a_nonase  |                    |          |                   | entry           | externel dcl 7 ref 68  |
|   |                    | 24000    | constant          | entry           | externel dcl 7 ret 161   |
|   |                    |          | 011080170         | TAXed bin(17,0) | CCI 7 807 F01 61 73 127 131 131 131 131 135 135                  |
| Inites  |                    | 000105   | autosatic         | fixed bin(17.01 | 144 140 152 152 156 156 156                                      |
|   |                    | 000036   |                   |                 | external del 7 raf 46 ao or ras 444 ao                           |
| 1.01  |                    |          |                   |                 | 165 FET TET TIT DAT 15 65 10 10 10 10 10 10 10 10 10 10 10 10 10 |
|   |                    |          | 01108811C         | fixed bin(17,8) | du! 7 807 rof 124 125 126 126 189 130 143 143 150                |
| next_erg  |                    | 008107   | Butomatic         | fixed bin(17.8) |  |
|   |                    | 000110   |                   | fixed bin(17.6) | del 7 and and 100 to 10 01 95                                    |
| ver lav   |                    | 000101   | Butomatic         | fixed bin(17.0) | dc1 7 Bat pat 123 131 149 149                                    |
| adl   |                    |          |                   | bit (36)        | Brrav dol 7 sat rat 126 126                                      |
| 2040  | 0(28)              | 902200   | 51100011C         | 161) 170        | level 2 packed unaligned dcl 30                                  |
|   |                    | 000112   |                   | (2) 110         | level 2 packed unailgned dol 38                                  |
| 'Inglaget_ssagptr   |                    | 0 40000  |                   | (8./11)UTO 0111 | dcl 7 set ref 117 117 118  |
| Save_acc  |                    | 102200   |                   |                 | external dol 7 ref 64 102  |
| 1100et  |                    | 882122   |                   |                 | dci 37 set ref 115 159   |
|   |                    |          |                   | Jan Tana        | GC1 7 807 F01 63 64 65 68 73 76 184 184 115 115                  |
|   | 0(27)              | 002200   | automatic         | bit (1.         | lavel 2 Decked testioned det 20                                  |
| 10  |                    |          | based             | cher            | unsiloned dol 7 set rat 68 68 64 64 67 227                       |
|   |                    |          | 84108811C         | Tixed plut17.0) | dci 7 set ref 43 44 50 50 52 61 61 64 64 64 64 64 64 64 64 84 89 |
|   |                    |          |                   |                 | 87 87 89 89 93 94 95 95 97 97 134 135 135 151 152                |
| The seen  |                    | 000106   | automitic         | fixed bin(17.8) | dcl 7 set ref 128 121 121 129 132 140                            |
|   |                    |          | 841 0881 1 C      | pointer         | dci 7 set ref 43 50 58 52 61 64 66 81 87 89 92 85                |
| wdse gptr<br>za   |                    | 0 12200  | cutomotic         | peinter         |  |
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| ant entry external doi 7 ref 116 159 | R REFERENCEO.<br>ant entry externel dol 7<br>efic fixed bin(17.0) dol 7 | ant       1abe!       dc!       97       120         ant       1abe!       dc!       139       rof       135       139         ant       1abe!       dc!       139       rof       135       139         ant       1abe!       dc!       139       rof       135       139         ant       1abe!       dc!       137       rof       57       53         ant       1abe!       dc!       137       rof       57       53         ant       1abe!       dc!       127       124       56       56         ant       1abe!       dc!       126       127       140         ant       ant       ant       ant       127       140         ant       ant       ant       ant       ant       127       140         ant       ant | Multin function     Internal ref 41 66 66 66 106 115 115 115 115 115 115 115 115 115 11  | LOC LINE LOC |
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| 10012100 010100                      | Y DECLARE STATEMENT AND NEVER R<br>300000 constant<br>autometi          | <pre>r ExPLICIT CONTEXT.<br/>008736 constant<br/>001463 constant<br/>0013%1 constant<br/>001277 constant<br/>001277 constant<br/>0012%5 constant<br/>0013%2 constant<br/>0013%2 constant</pre>   | CONTEXT OR IMPLICATION<br>IS FOR THES PROGRAM.<br>Text Link<br>0 1656<br>1516 56<br>1516 56<br>2d uses 1254 mords of<br>2d uses 1254 mords of<br>2d uses 1254 mords of<br>2d uses 254 mords of<br>2d uses 254 mords of<br>2d uses 1254 mords of<br>2d uses 254 mords of<br>2d uses 255 mords of 2555 mords of 255 mords of   | LINE LOC LINE<br>51 000225<br>51 000225<br>52 000273<br>56 000273<br>56 000273<br>56 000273  |
|                                      | NAMES DECLARE D BY<br>condition   | MANES DECLARED BY<br>MANES DECLARED BY<br>CHOCK_INIT<br>different<br>get_beund<br>get_neme<br>ise<br>ise<br>fer<br>skip<br>skip  | STORACE REQUIRENTS<br>STORACE REQUIRENTS<br>STORAC | LIME LJC<br>1 000113<br>50 00012<br>67 000415<br>77 000415   |

| 101124<br>101172<br>101172<br>101276<br>101276<br>101276<br>101272<br>1001272<br>1001272<br>1001272<br>1001272   |
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| 114 00110<br>120 001222<br>136 001222<br>136 001222<br>136 001335<br>136 001335  |
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| 111 901062<br>116 001152<br>126 001204<br>134 001320<br>134 001350<br>1451 001361<br>161 001361  |
| 110 0010 56<br>117 0011 56<br>125 0012 83<br>133 0012 85<br>140 0013 62<br>150 0013 63<br>159 0013 63<br>159 0013 63   |
| 4 201 001 001 00<br>1 10 10 10<br>1 |

## APPENDIX E

# Patch Utility Listing

This appendix is a listing of a patch utility corresponding to the dump utility in Appendix D. The utility, zp, is based on the installed Multics command, patch\_ring\_zero, documented in the <u>MPM System Programmers</u><sup>1</sup> Supplement (SPS73). Zp uses the same algorithm as zd in Appendix D and operates under the same restrictions. A sample of its use is shown below. Lines typed by the user are underlined.

> Zp pds 660 123171163101 144155151156 660 104162165151 to 123171163101 661 144040040040 to 144155151156 Type "yes" if patches are correct: yes

As seen above, the command requests the user to confirm the patch before actually performing the patch. The patch shown above changes the user's project identification from Druid to SysAdmin.

/\* pick up the first ang (name/number) \*/ /\* didn't sive number \*/ cail ringl\_et\_sseptr ("", targ, sagptr, code); /\* so assues ring 8 name \*/ If segptr = null () then do! /\* get pointer to deta area \*/ /\* segment number given \*/ /\* This procedure allews privileged users to patch lecations in ring 0. If necessary the descriptor segment is patched to give access to patch a non-write /\* get segment number \*/ current antry (char (?)) returns (fixed bin (35)). current char (?), returns (fixed bin) returns (fixed bin (35)). rings\_get\_geneget entry (char (°), cher (°), ptr. fixed bin). (los\_freed\_ft entry (ptr. fixed bin, fixed bin). los\_freed\_ft entry (ptr. fixed bin, fixed bin). (so, zosat) entry (ptr. fixed bin, fixed bin). buffer char (16) aligned. curser\_ptr ext entry (ptr. fixed bin, ptr. fixed bin). call cu\_sarg\_ptr (1, 1p, tc, code); /\* plot up 11 code = errer\_febie\_\$nearg 1 tc = 0 then de; call lea\_ ("prz name/segne effset value1 ... vel ueg"); Compiled by: Multics PL/I Compiler, Version II of 30 August 1973. Compiled on: 84/10/74 1843.6 edf Med (arrer\_table\_\$neerg: error\_table\_\$segmoun) fixed bin ext; (code: i, fc, first: sw) fixed bin; (sdup: segptr) ptr stafic; get\_process\_id\_ext entry returns (bit (36) bitgind), processid bit (36) all gned, detal (8: 99) fixed bin static, data (8: 99) fixed bin (35), overlay (8:count-1) bit (36) all gned based, count fixed bin static. call lea\_ (""e not found.", torg) ! 1 = cv\_oct\_check\_ (forg. code); 1f code ^= 8 then do; eise segntr = baseptr (1) ; COAPILATION LISTING OF SEGNENT ZD 1() | nul | () | targ char (tc) based (tp). detep = eddr (dete); count = 8; seve\_acc fixed bin(35) 5 itp, datas, datas) ptr. dirname chier (168), ----1 sd# based all gned. 2 pad bit (30) unal: 2 acc bit (6) unal; teruter ename cher (32). le treges tialer end: wdsegptr ptr. Opt Lons : map t pue PC. tuerd 15 20 8 102 get \*\*\*\*\*\*\* \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* 25 35 -\* -

```
cail cuisergiptr (2, tp, tc, code); /* pick up second ang (first word to duap ) */
if code = error_table_snoarg ! tc = 0 then go to mass;
first = cv_oct_ (targ);
segotr = ptr (segotr, first);
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         /* read in the answer "/
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 /* get next argument */
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          ì
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  /* convert i th arg
                                                                                                                                                                                                                                                                                                             If substr (datap -> sdw.acc. 4. 3) = "100"b then do!
call tos. ("pt Mester procedure. SOM = "4", date (8));
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              "w to "w", firstel, data (1), datas (1));
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  cell cu_sarg_pr (1, tp, tc, code) ;
if code = error_table_fnoarg i tc = 0 then go to endergi
data1 (1-3) = cv_oct_ (targ);
/* com
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       cell loa_gnni ("Type ""yea" If patches are correct! ");
cell los_gread_ptr (addr (buffer); 15; 1); /* read
If 1 = 4 then go to reset;
If substr (buffor; 1: 3) ~* "yea" then go to reset;
                                                                  stdwp = pfr (beseptr (0), besend (segptr));
cail ring0_get_staegptr("", "wdseg", wdsegptr, code);
                                                                                                                                64 /* Now check the access on the segment about to be patched */
65 detep = addr (deta)]
67 detato = addr (deta)]
                                                                                                                                                                                                                                                                                                                                                                                             call zg(pfr(wdsegptr,baseno(ssgpfr)), seve_acc);
call zg&zf(pfr(wdsegptr, baseno(segptr)), defa(0));
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               113 resett call zg$zf(pfr((#dsegpfr), baseno(segptr)), save_acc);
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       datap -> overiey = segptr -> overiey;
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  segntr -> overiay = dataip -> overiay;
                                                                                                                                                                                                                                                                                                                                                                                 dafap -> sdw.acc = "118010"b;
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              111 /* Now reset access (in dsey) if necessary */
                                                                                                                                                                                                                                                 1 ( .. 0 .. MOS
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       If count = 0 then go to messi
                                                                                                                                                                                        detaip = addr (detai);
ceii zg (zdwp, deta (0));
i' deta (0) = 0 then do;
                                                                                                                                                                                                                                                                                                                                                                                                                                             /* Now pick off the arguments */
                                                                                                                                                                                                                                           call 100_ ("p1
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             Carl 100_ (**60
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        do 1 = 0 to count-11
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      count = 1 - 34
                                                                                                                                                                                                                                                              return:
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           187 /* Now do the patches "/
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      10001 01 00
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     1 = 1 + 1 = 1
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| IDENT LF IER   | OFFSE T                       | 100  | OFFSET LUC STORAGE CLASS DATA TYPE                             | DATA TYPE  | ATTRIGUTES AND NEFERENC   |
| NAMES DEGLARE D BY DECLARE STATEMENT.<br>acc 0(30)<br>buffer 00025<br>code<br>count<br>count<br>count<br>count<br>00025<br>00010<br>00010<br>00010<br>00025<br>00010<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00025<br>00 | C DECLARE STATI               | MENT -<br>000250<br>000100<br>000100<br>000150 | based<br>automatic<br>automatic<br>internal static<br>constant | (ENT. based bif(6)<br>000256 automatic char(15)<br>000100 automatic fixed bin(17,0)<br>000150 internal static fixed bin(17,0)<br>000264 constant antry | level 2 packed unaligne<br>dcl 7 set raf 99 99 181<br>dcl 7 sot raf 40 41 45<br>dcl 7 set raf 38 98 92<br>external dcl 7 raf 48 |

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| NAMES DECLANED BY DECLARE | SIA JERENI .        |                   | MI # (61          |
|---------------------------|---------------------|-------------------|-------------------|
| BCC .                     |                     |                   |                   |
| Del ter                   | 9700                |                   |                   |
| code                      | 000100              | Ψ.                | + 1 1 1 UT 0      |
| ceunt                     | 0 97 0 0 0 7 0 0    | internal static   | D10(17.0          |
| cu sera ptr               | 00020+              | constant          | entry             |
| cr act                    | 000164              | constant          | entry             |
| cv.ect.check              | 000166              | constant          |                   |
|                           | 000100              | automatic         | bin(35.           |
|                           | 10000               | Internet static   | fixed bin(17.0)   |
|                           | 9 52 0 0 0          | autometic         | pointer           |
|                           | 000254              | autometic         | pointer           |
| arrer table troops        | 300162              | externel static   | fixed bin(17.0)   |
|                           | 000103              | -                 | D10(17            |
|                           | 000101              | automotic         | bln(17            |
|                           | 000177              | constant          | entry             |
|                           | 0.17                | constant          | entry             |
| Les Greed of              | 000176              | constant          | entry             |
|                           |                     | based             | b11 (36)          |
| rinas set ssaptr          | 000770              | constant          |                   |
| Save acc                  | 4 92550             | suforet LC        | 11×00 010(35.8)   |
|                           | 0 10 0 0 0          | Intervel static   | peinter           |
| segnir                    | 2 10 0 0 0          | Internet static   | pointer           |
| tare                      |                     | peseq             |                   |
| 16                        | 000785              | automatic         | fixed bin(17.8)   |
|                           | 0.0000              |                   | aduter            |
|                           |                     |                   | Del ster          |
|                           | 000200              |                   |                   |
| 2952 f                    |                     | constant          | entry             |
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| HANES UCHANED OF UCHANE   |                     | automitic         | cher (168)        |
|                           |                     | automatic         | char (32)         |
| errer_table_5 segmoun     |                     |                   | 10.7.1.1.1. bents |
|                           | 00000               |                   |                   |
|                           | 00000               | Constant          | entry             |
|                           |                     | besed             | DI1 (30)          |
| corese id                 |                     | automatic         | b11 (35)          |
|                           |                     | Desed             | structure         |
| HT.                       |                     | automatic         | fixed bin(17,0)   |
|                           | T CONTEXT.          |                   |                   |
| UCULARE U OF              | 000035              | constant          | [sbe]             |
|                           | 000555              |                   | 1.0001            |
|                           | 060132              |                   | Isbel             |
|                           | 000270              |                   | label             |

 

 ACT 7
 Tot 750
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 ACT 7
8 57 56 56 8 ned dci 31 set ref 76 78 31 61 86 87 
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 ettermel dci 7 ref 61 79
Internal ref 37 66 67 99 99 Internal ref 68 79 88 88 113 113 Internal ref 54 68 15 25 ievel 2 packed unailgned dci 31 dci 7 dcl 92,ref 87 96 dcl 85 ref 85 89 dcl 42 ref 42 57 92 dcl 113 ref 128 181 113 external dcl 1 ref 1 ievel 1 pecked dcl 31 dcl 7 del 7 externel del 7 externel del 7 unaligned dci 7 unaligned dci 7

> builtin function builtin function builtin function entry 000072 constant NAMES DECLARED BY CONTEXT OR IMPLICATION. besend 10001 addr 8 142

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## APPENDIX F

# Set Dates Utility Listing

This appendix is a listing of the set dates utility described in Section 3.4.4. The get entry point takes a pathname as an argument and remembers the dates on the segment at that time. The set entry point takes no arguments and sets the dates on the segment to the values at the time of the call to the get entry point. Set remembers the pathname as well as the dates and may be called repeatedly to handle the deactivation problem discussed in Section 3.4.4.

2 (type bit (2), numers bit (16), nrp bit (18), dtm bit (36), dtu bit (36), mede bit (5), pedding bit (13), records bit (18), dtd bit (36), dtem bit (36), acct bit (36), curien bit (12), bitent bit (24), did bit (4), mdid bit (4), cepysm bit (1), pud2 bit (9), nbs (8:2) bit (6), uid bi; (36) . /\* get relative pathnese from command line 2 call hcs\_sstatus\_long (dir. entry. 1. bp. null (). code); /\* -ead out dates en segment If code T= 8 them go to arror; 2 save dates in internal static cu\_Struct to entry (fixed bin, ptr, fixed bin, fixed bin), expand\_path\_entry (ptr, fixed bin, ptr, ptr, fixed bin), com\_err\_entry epitons (variable), hcs\_Status\_long entry (cher (?), cher (?), fixed bin (1), ptr, ptr, fixed bin), hcs\_Stet\_detes entry (cher (?), cher (?), ptr, fixed bin); (argp. arg!, addr (dir), addr (antry), coda); COMPILATION LISTING OF SEGNENT get Complied by: Muitics PL/I Compiler, Varsian II of 38 August 1973. Compiled on: 04/10/74 1841.1 odt Med \* (dies. did. diu. dis) bit (36) unsilgned; /\* Entry point to gai the dates from a segment \*/ call cu\_Sarg ptr (1, argo, argi, cada); if code ~= 0 than dir char (168) int static init (" "), antry char (32) int static init (" "), "get". arg) ; 1("1 m5" time aligned internal static. arg char (argi) based (argp). cell commerty (code, call cos\_err\_ (code, fime.dtem = branch.dtem; time.dtd = branch.dtd; time.dtu = branch.dtu; tille.die = branch.dim; bp = addr (branch); cell expend\_peth\_ if code ^= 0 then branch aligned, ergi fixed bin. code fixed bin, return: return: ergp ptr. 100 8 bp ptr: entry: \* pce t pue Ų qui N pr oci 1-0---get t -----10 1 12 2 \* 5 9 22.23 2222 26 \*\*\*\*\*\* 2 27 39 ie 2

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57 /\* Entry to sai the dates on a segment to the values at the time of the <u>sai</u> call \*/ 58 cell hcs\_sset\_dates (dir, entry, addr (time), code); /\* sat the dates \*/ 60 if code \*\* 0 then go to erri; 61 end;

NAMES DECLARED IN THIS COMPILATION.

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builtin function builtin function TIXed BIN(17.8) ILKed bin(17.0) Static 360 102 polnter structure structure DATA TYPE Ar (160) (32) 179 char (32 (33) bit (36) pointer b11 (24) 011 (13) (11) + 79 (1 (12) 3 11 (1) 3 entry entry ntry Char Internet static internet static Internet static Internul static internal static 100072 Internal static Sec. JOBOLS Internal static LOC STORAGE CLASS automotic ut emt le autometic utomitic sut om tic 00016 0 automatic 00016 6 automatic 000103 automatic 000196 automatic automit.c 000106 sutempte 000106 automatic autometic autemette 100186 autometic automatic sut one tic 5 automatic eutemette 00010 constant 00010 constant 000013 constant 000221 constant out centle automette automitic outomatic outomatic 000104 constant constant 100110 constant 10106 constant 1182 constant Symbol pesed NAMES DECLARED BY CONTEXT OR INPLICATION. Mar 90100 000106 000106 890192 4 0100 9 979 80 000106 000106 000072 0.10 6 000100 8 STORAGE REQUEREVENTS FOR THIS PROGRAM. 000012 10000 200 11001 010010 3 NAMES DEGLARED BY DEGLARE STATEMENT. 112 350 112 NAMES DECLARED BY EXPLICIT CONTEXT WILL DECLARED BY EXPLICIT CONTEXT 10(04) 3(1.0) 10(110) 3(85) 7(12) 10(0.0) 0170 10(09) OFFSE T 11 - 9 4 Text expend\_path\_ hcs\_6set\_dates hcs\_8status\_1 eng 0b) ec 1 ces\_err\_ cepysh cu\_serg\_ptr IDENT IF IER pedding recerds reach 5100 bitcht 25 190 100 ŝ 101 8 2 100 É 147

ATTRIBUTES AND REFERENCES

3 55 97 57 2 Internet ref 37 37 37 37 44 59 59 Internet ref 45 45 ĩ 1 30 31 31 37 26 40 6 fot 33 46 d unaligned dci 29 6 fot 30 3 101 5 52 mailgned dci 25 unaligned dcl 14 set ref 40 dcl 14 set ref 30 37 40 40 dcl 14 set ref 30 37 40 40 dcl 14 set ref 30 37 40 valigned del ki 25 set ref del 14 set pecket unally al Igned Penel is Dec Mellened 045719 una | 19n 87 79 5 5 packed unally 1105 external del 1 ref 1 external del 54 ref poch a 3c1 14 set rel 10461 2 98649 061 14 861 70 packe 1 packs ievel 2 pecto 2 packs suternal del 1 25 Packs pecke PACKE External del ----2 pack pect 109 Ų exterse axterse n11201 R terna 5 10A0 S ISVOI In1110 ----1010 ----1020 1020 ..... 1020 Versi -----1020 10/01 1020 I evel

External procedure get uses 148 words of automatic storage

260

632

Length

Start

5

162 136

ext\_entry THE FOLLOWING EXTERNAL OPERATORS ARE USED BY THIS PROGRAM. Call\_ext\_out\_desc call\_ext\_out return

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hcs\_sast\_dates

NO EXTERNAL VAPIABLES ARE USED BY THES PROGRAM.

|      | 7       | 112000 | 1.1     |
|------|---------|--------|---------|
| 100  | 190000  | 102000 | \$62000 |
| LINE | 37      | ;      | 3       |
| ğ    |         | 1200   | 12200   |
|      |         | 3      |         |
| 106  | 14000   | M1000  | 02200   |
|      |         | ;      |         |
| LOC  | 100037  | 241000 | 112000  |
| LINE | 31      | :      | 25      |
| Loc  | 02 0000 | 1+1000 | 51 2000 |
|      |         | 42     |         |
| 50   | 2 10 01 | 90700  | 1 20    |
| TINE |         | ;      |         |

#### GLOSSARY

Access

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"The ability and the means to approach, communicate with (input to or receive output from), or otherwise make use of any material or component in an ADP System." <DOD73>

Access Control List (ACL)

"An access control list (ACL) describes the access attributes associated with a particular segment. The ACL is a list of user identifications and respective access attributes. It is kept in the directory that catalogs the segment." (HIS73)

Active Segment Table (AST)

The AST contains an entry for every active segment in the system. A segment is "active" if its page table is in core. The AST is managed with least recently used algorithm.

Argument Validation

On calls to inner-ring (more privileged) procedures, argument validation is performed to ensure that the caller indeed had access to the arguments that have been passed to ensure that the called, more privileged procedure does not unwittingly access the arguments improperly.

Arrest

"The discovery of user activity not necessary to the normal processing of data which might lead to a violation of system security and force termination of the activity." (DOD73)

## Breach

"The successful and repeatable defeat of security controls which or without an arrest, which if carried to consummation, could result in a penetration of the system. Examples of breaches are: a. Operation of user code in master mode; b. Unauthorized acquisition of 1.D. password or file access passwords; and

c. Accession to a file without using prescribed operating system mechanisms." (D0D73)

# Call Limiter

The call limiter is a hardware feature of the HIS 6180 which restricts calls to a mate semment to a specified block of instructions (normally a transfer vector) at the base of the segment.

Date Time Last Modified (DTM)

The date time last modified of each segment is stored in its parent directory.

Date Time Last Used (DTU)

The date time last used of each segment is stored in its parent directory.

Deactivation

Deactivation is the process of removing a segments page table from core.

Descriptor Base Register (DBR)

The descriptor base register points to the page table of the descriptor segment of the process currently executing on the CPU.

Descriptor Segment (DSEG)

The descriptor segment is a table of segment descriptor words which identifies to the CPU to which

| Repr | oduced fr<br>available | om    | 0 |
|------|------------------------|-------|---|
| 0031 | available              | copy. |   |

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segments, the process currently has access.

## Directory

"A directory is a segment that contains information about other segments such as access a/tributes, number of records, names, and bit count."

#### emergency\_shutdown

"This mastermode module provides a system reentry point which can be used after a system crash to attempt to bring the system to a graceful stopping point." (SPS73)

#### Fault Intercept Module (fim)

The fim is a ring 0 module which is called to bandle most faults. It copies the saved machine state into an easily accessible location and calls the appropriate fault bandler (usually the signaller).

Gate Segment

A gate segment contains one or more entry point user on inward calls. A gate entry point is the only entry in a inner ring that may be called from an outer ring. Argument validation must be performed for all calls into gate segments.

General Comprehensive Operating Supervisor (GCOS)

GCOS is the operating system for the Honeywell 600/6000 line of computers. It is very similar to other conventional operating systems and has no outstanding security features.

HIS 645

The Honeywell 645 is the computer originally designed to run Multics. It is a modification of the HIS 635 adding paging and segmentation hardware.

> Reproduced from best available copy.

#### HIS 6180

The Honeywell 6180 is a follow-on design to the HIS 645. The HIS 6180 uses the advanced circuit technology of the HIS 6080 and adds paging and segmentation hardware. The primary difference between the HIS 6180 and the HIS 645 (aside from performance improvements) is the addition of protection ring hardware.

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hcs\_

The gate segment hcs\_ provides entry into ring 0 for most user programs for such functions as creating and deleting segments, modifying ACL's, etc.

#### hphcs\_

The gate segment hphcs\_ provides entry into ring 0 for such functions as shutting the system down, hardware reconfiguration, etc. Its access is restricted to system administration personnel.

ITS Pointer

An ITS (Indirect To Segment) Pointer is a 72-bit pointer containing a segment number, word number, bit offset, and indirect modifier. A Multics PL/I aligned pointer variable is stored as an ITS pointer.

Known Segment Table (KST)

The KST is a per-process table which associates segment numbers with segment names. Details of its organization and use may be found in Organick. (ORG72)

Linkage Segment

"The linkage segment contains certain vital symbolic data, descriptive information, pointers, and instructions that are needed for the linking of procedures in each process." (OPG72)



### Master Mode

When the HIS 645 processor is in master mode (as opposed to slave mode), any processor instruction may be executed and access control checking is inhibited.

Multics

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Multics, the Multiplexed Information and Computing Service, is the operating system for the HIS  $\overline{6}45$  and HIS 6180 computers.

## HultI-Level Security Mode

"A mode of operation under an operating system (supervisor or executive program) which provides a capability permitting various levels and categories or compartments of material to be concurrently stored and processed in an ADP system. In a remotely accessed resource-sharing system, the material can be selectively accessed and manipulated from variously controlled terminals by personnel having different security clearances and access approvals. This mode of operation can accomodate the concurrent processing and storage of (a) two or more levels of classified data, or (b) one or more levels of classified data with unclassified data depending upon the constraints placed on the systems by the Designated Approving Authority." (DOD73)

### 0S/360

OS/360 is the operating system for the IBM 360 line of computers. It is very similar to other conventional operating systems and has no outstanding security features.

Page

Segments may be broken up into 1024 word blocks called pages which may be stored in non-contiguous locations of memory.

#### Penetration

"The successful and repeatable extraction and identification of recognizable information from a protected data file or data set without any attendant arrests." <DOD73>

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### Process

"A process is a locus of control within an instruction sequence. That is, a process is that abstract entity which moves through the instructions of a procedure as the procedure is executed by a processor." (DEN66)

### Process Data Segment (PDS)

The PDS is a per-process segment which contains various information about the process including the user identification and the ring 0 stack. The PDS is accessible only in ring 0 or in master mode.

## Process Initization Table (PIT)

The PIT is a per-process segment which contains additional information about the process. The PIT is readable in ring 4 and writable only in ring 0.

#### Protection Rings

Protection rings form an extension to the traditional master/slave mode relationship in which there are eight hierarchical levels of protection numbered 0 - 7. A given ring 11 may access rings 11 through 7 but may only call specific gate segments in rings 0 to N-1.

Reference Monitor

The reference monitor is that hardware/software combination which must monitor <u>all</u> references by any program to any data anywhere in the system to ensure the security rules are followed.

a. The monitor must be tamper proof.

b. The monitor must be invoked for every

reference to data anywhere in the system. c. The monitor must be small enough to be proven correct.

#### Segment

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A segment is the logical atomic unit of information in Multics. Segments have names and unique protection attributes and may contain up to 256K words. Segments are directly implemented by the HIS 645 and HIS 6180 hardware.

Segment Descriptor Word (SDW)

An sdw is a single entry in a Descriptor Segment. The SDW contains the absolute address of the page table of a segment (if one exists) or an indication that the page table does not exist. The SDW also contains the access control information for the segment.

## Segment Loading Table (SLT)

The SLT contains a list of segments to be used at the time the system is brought up. All segments in the SLT come from the system tape.

signaller

"signaller is the hardcore ring privileged procedure responsible for signalling all fault and interrupt-produced errors." (SPS73)

Slave Hode

When the HIS 645 processor is in slave mode, certain processor instructions are inhibited and access control checking is enforced. The processor may enter master mode from slave mode only by signalling a fault of some kind.

# Stack Base Register

The stack base register contains the segment number of the stack currently in use. In the original design of Multics, the stack base was locked so that interrupt handlers were guaranteed that it always pointed to a writable segment. This restriction was later removed allowing the user to change the stack base arbitrarily.

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#### subverter

The subverter is a procedure designed to test the reliability of security hardware by periodically attempting illegal accesses.

## Trap door

Trap doors are unnoticed pieces of code which may be inserted into a system by a penetrator. The trap door would remain dormant within the software until triggered by the agent. Trap doors inserted into the code implementing the reference monitor could bypass any and all security restrictions on the systems. Trap doors can potentially be inserted at any time during software development and use.

#### WWMCCS

WWMCCS, the World Wide Military Command and Control System, is designed to provide unified command and control functions for the Joint Chiefs of Staff. As part of the WWMCCS contract for procurement of a large number of HIS 6000 computers, a set of software modifications were made to GCOS, primarily in the area of security. The WWMCCS GCOS security system was found to be no more effective than the unmodified GCOS security, due to the inherent weeknesses of GCOS itself.