SPECIAL HARDWARE FOR ARL ANALYSIS OF ACOUSTIC DATA ACQUISITION CAPSULE (ACODAC) DATA

Richard O. Grohman, et al

Texas University at Austin

Prepared for:

Office of Naval Research

14 March 1974

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1 REPORT NUMBER ARL-TM-74-12	2. GOVT ACCESSION NO.	3 RECIPIENT'S CATALOG NUMBER AD/A-000 295
4. TITLE (and Subtitle) SPECIAL HARDWARE FOR ARL ANALYSIS OF ACODAC DATA		5 TYPE OF REPORT & PERIOD COVERED 6 PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Richard O. Grohman, Larry L. Mellenbruch, Felix J. Sawicki		8. CONTRACT OR GRANT NUMBER(s) N00014-70-A-0166
9 PERFORMING ORGANIZATION NAME AND ADDRESS Applied Research Laboratories The University of Texas at Austin Austin, Texas 78712		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Task 0016 292-134
11. CONTROLLING OFFICE NAME AND ADDRESS OFFICEOF NAVAL RESEARCH Department of the Navy Arlington, Virginia 22217		12. REPORT DATE 14 March 1974 13. NUMBER OF PAGES 82
14. MONITORING AGENCY NAME & ADDRESS(If different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

ONR SCIENTIFIC OFFICER
Tel: (202) 692-4411

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

IRIG C time code reader
phase lock loop frequency multiplier
low pass active filter

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report provides functional, operational, and maintenance information for six specially fabricated pieces of hardware used in the analysis of Acoustic Data Acquisition capsule information. This special equipment was designed to decode time, overload, and calibration information from the analog acoustic data, as well as provide synchronization between units in the data analysis system. (U)

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

ARL-TM-74-12
14 March 1974

SPECIAL HARDWARE FOR ARL ANALYSIS OF ACODAC DATA

Richard O. Grohman
Larry L. Mellenbruch
Felix J. Sowic[illegible]

This Research Sponsored by
OFFICE OF NAVAL RESEARCH
Contract N00014-70-A-0166, Task 0016
292-131

APPLIED RESEARCH LABORATORIES
THE UNIVERSITY OF TEXAS AT AUSTIN
AUSTIN, TEXAS 78712

ABSTRACT

This report provides functional, operational, and maintenance information for six specially fabricated pieces of hardware used in the analysis of Acoustic Data Acquisition capsule information. This special equipment was designed to decode time, overload, and calibration information from the analog acoustic data, as well as provide synchronization between units in the data analysis system.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

1.0 INTRODUCTION

This report contains the functional and operational description of specially fabricated hardware used in the analysis of data from the Acoustic Data Acquisition Capsule (ACODAC). (1,2) The data recorded on analog magnetic tape, consists of six channels of acoustic information from a hydrophone array and one channel with the time, data channel gains, and unit identification in a coded sequence. The ACODAC system provides both overload indications and periodic calibration signals to determine the influence of the data acquisition equipment on the information. Analysis of the data is primarily performed by a CDC 3200 computer. However, a real time analyzer (RTA) is integrated into the system for ambient noise and continuous wave (cw) analysis.

The special hardware is used to decode information from the magnetic tape, and to provide time and frequency references for digitization and RTA operation. The flow charts, Figs. 1 and 2, show a block diagram of the precomputer functions, with heavy lines indicating the equipment described in this report. That equipment consists of the following items.

(1) a time code reader that provides a time and channel gain visual reference for the operator and digitally for the computer;
(2) a phase lock frequency multiplier that aids in reducing tape recorder induced jitter;
(3) a filter for the data channels to compensate the spectrum of some types of data during digitization;
(4) an overload and calibration signal detector to inform the computer and the operator of the presence of such conditions;
(5) a RTA reset counter to synchronize the loading of information into the analyzer; and
(6) a pulse delay circuit to synchronize A/D sampling of the RTA spectrum information.

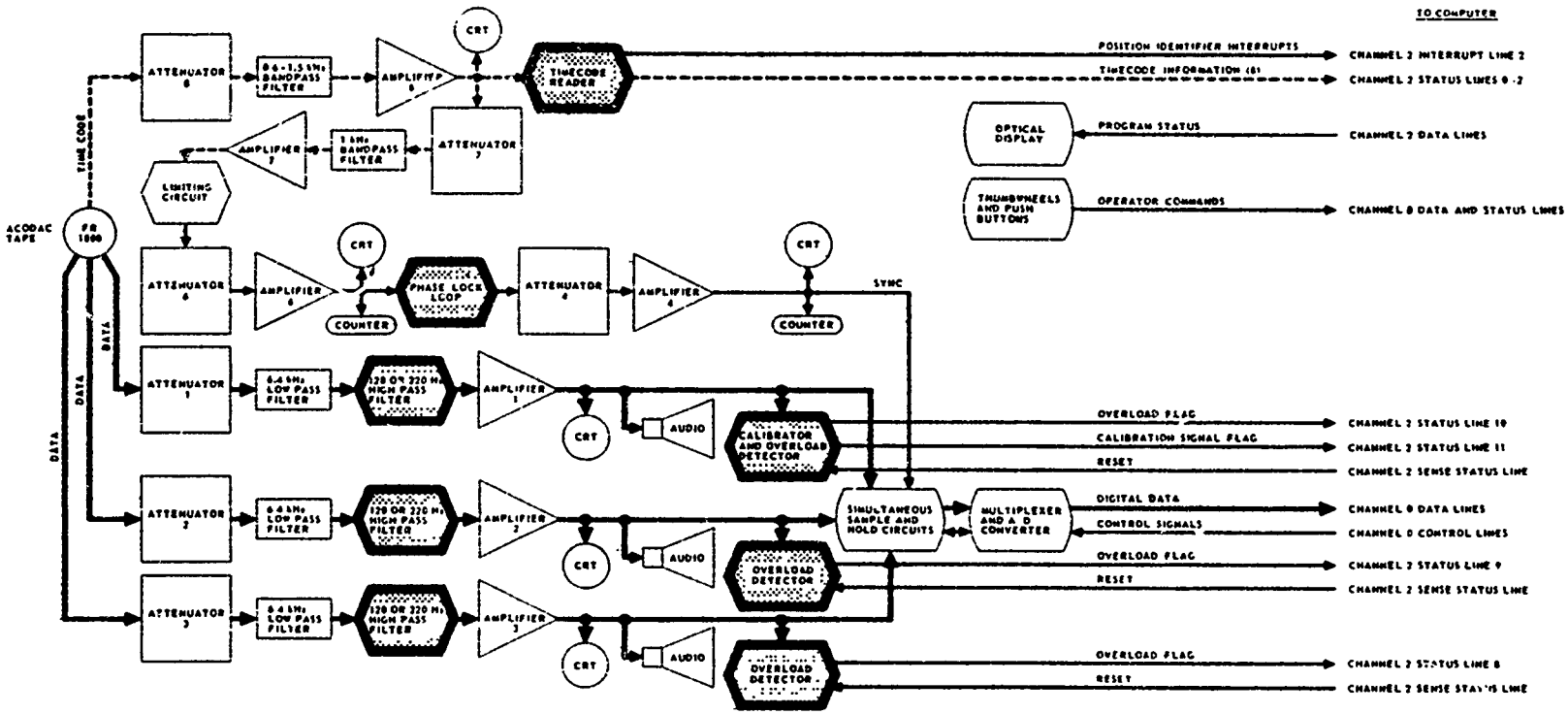


FIGURE 1
ANALOG EQUIPMENT CONFIGURATION FOR DIGITIZATION OF ACODAC DATA

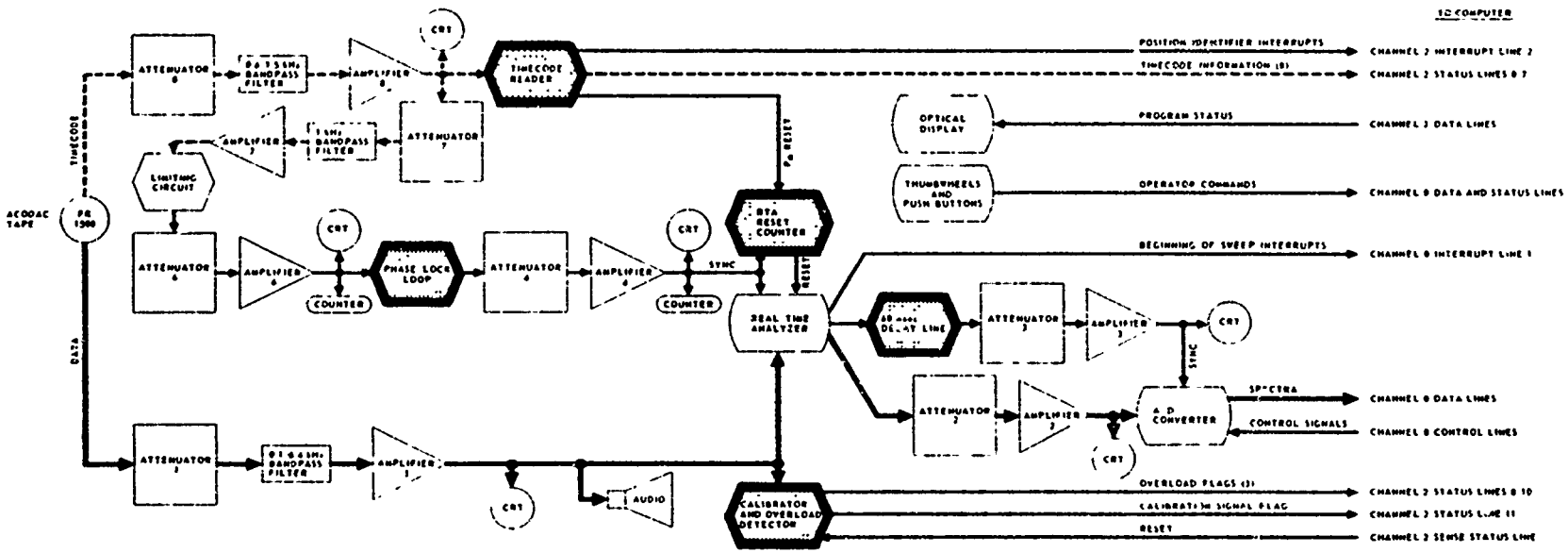


FIGURE 2
ANALOG EQUIPMENT CONFIGURATION FOR ANALYSIS OF ACODAC DATA VIA RTA

Each succeeding chapter, therefore, provides a description of one of those special pieces of hardware, a brief discussion of its operation, and an explanation of its pertinent controls and adjustments.

2.0 TIME CODE READER

2.1 Introduction

2.1.1 Background

The ARL time code reader (TCR) was built to analyze ACODAC (acoustic data acquisition capsule) data. One channel of the ACODAC analog data tape contains a modified form of IRIG-C time code which is used to synchronize the data recorded on the other channels. Hence, a time code reader capable of outputting time data and timing interrupts to the ARL computer system was required to synchronize the analysis of acoustic data on ACODAC tapes. The location of the TCR in the data analysis system is shown in Fig. 3.

The decision to build a time code reader "in-house," as opposed to purchasing a modified version of one of the commercially available units, was based on several considerations. First of all, there was a problem with scheduling and delivery. The analysis of the ACODAC data tapes required a TCR in 4 to 6 weeks after the contract had been awarded. Quotes obtained by the ARL purchasing department from several prominent TCR manufacturers provided for delivery times of 60 to 120 days. It was decided that a TCR could be designed and fabricated in-house in approximately 6 weeks using devices which were on hand, thereby precluding the usual delivery problems.

In addition to the foregoing problems, there was the requirement that the TCR be capable of reading a nonstandard IRIG-C code and additional bits of ACODAC system information from unused portions of the IRIG-C time frame. All of the TCR manufacturers contacted were willing to build these special capabilities into their TCR's. However, it was thought that the characteristics of the time code recorded on future ACODAC tapes might be changed. In that event, the TCR would have to be modified to accommodate the changes in the characteristics of the time code. Such a modification would obviously be easier to perform on an "in-house" TCR than on a purchased unit.

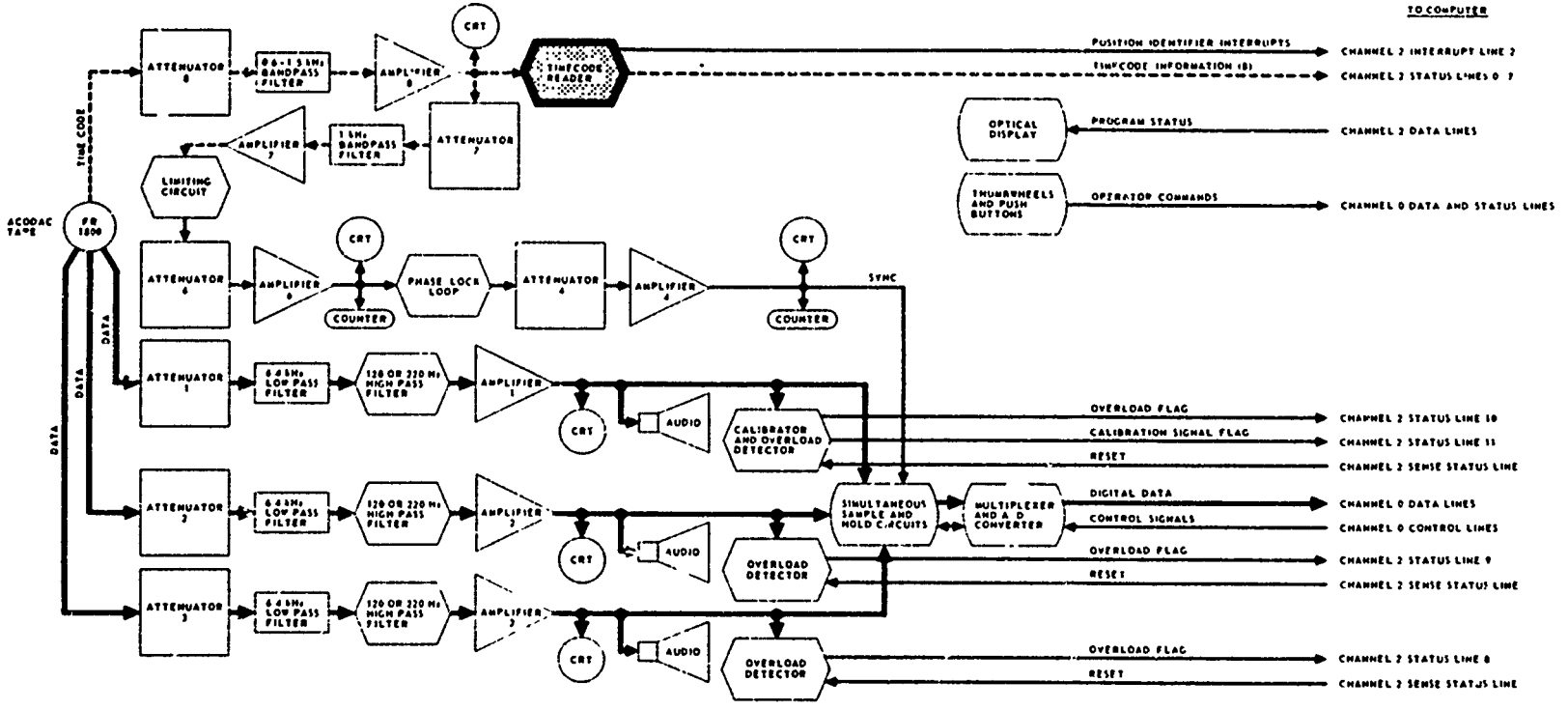


FIGURE 3
ANALOG EQUIPMENT CONFIGURATION FOR DIGITIZATION OF ACODAC DATA

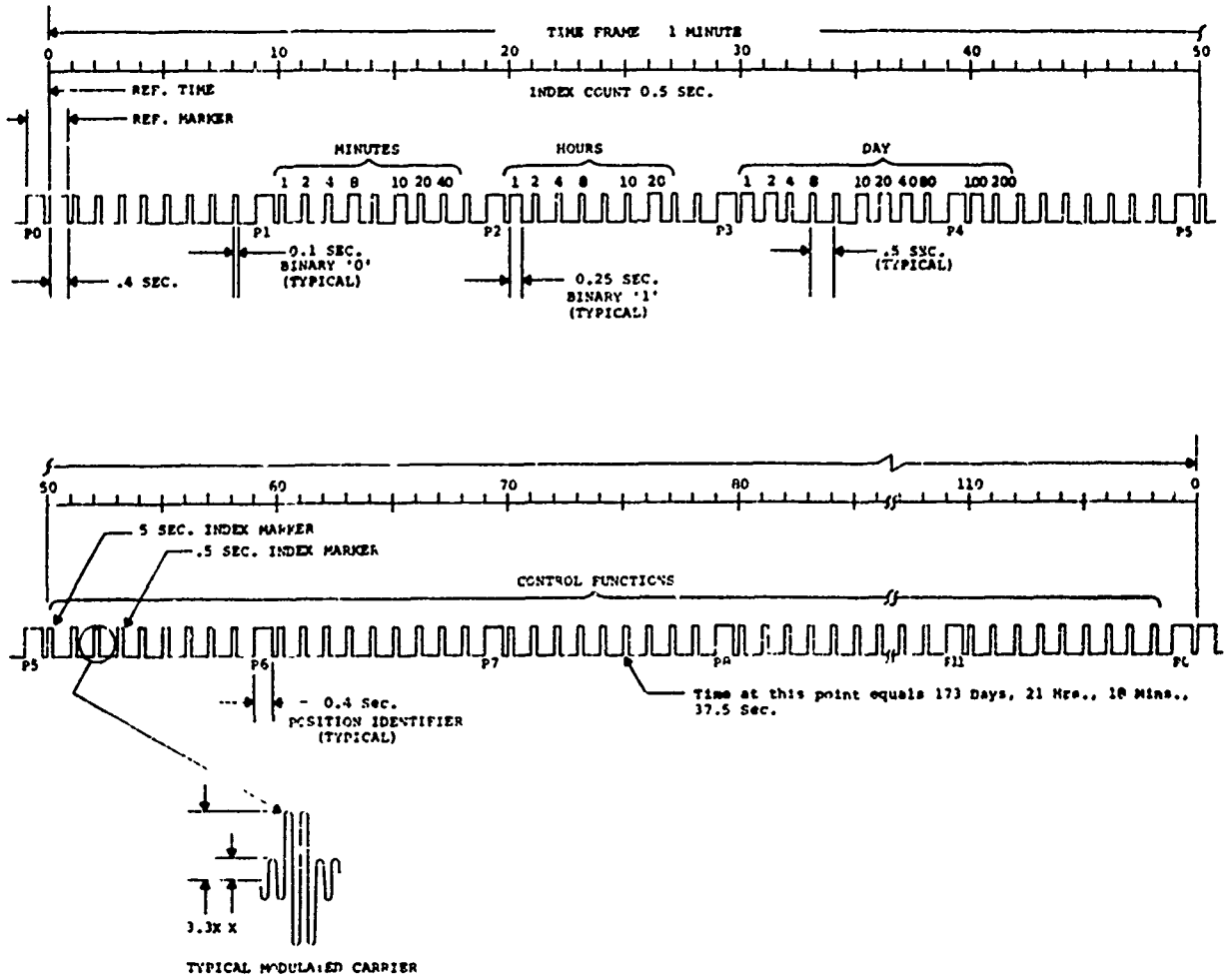
2.1.2 General Description

The ARL time code reader is designed to read and display IRIG standard time code—Format C (Fig. 4), which has been encoded on either a 100 Hz or 50 Hz carrier frequency. Although a carrier frequency of 100 Hz is the "standard" for IRIG-C time code, the ACODAC data (for which the TCR was specifically designed) uses a 50 Hz carrier. (Carrier frequency of 50 or 100 Hz is selectable with a switch on the front panel of the TCR.)

The ARL-TCR also reads and displays ACODAC system identification and channel gain states data which has been encoded in "unused" portions of the basic IRIG-C time frame by the ACODAC time code generators and recorders.

A continuously variable range of playback speeds from 1 to 160 times the original speed of recording can be accommodated by the TCR. The time decoding technique used in the ARL-TCR eliminates the need for a "playback speed" selector switch. The TCR will also accommodate inputs from tapes played either forward or reverse; however, the option to read forward or reverse must be indicated via the DIRECTION selector switch on the front panel of the TCR. See Fig. 5.

An overall block diagram of the TCR is shown in Fig. 6. An amplitude modulated sine wave signal containing IRIG-C time data is input to the analog "front end" of the TCR. It is converted to two digital pulse trains (see Fig. 7) which are output to the digital section of the reader. The digital section decodes the time information contained in these pulse trains and displays the results as days, hours, and minutes. In addition, the aforementioned ACODAC system data is decoded and displayed on the front panel of the TCR via binary lamps. All of the displayed data are made available for output to external equipment (specifically the ARL CDC 3200 computer system) via a multipin connector at the rear of the TCR chassis.



Element identification

a On time reference point for all Elements is the leading edge

b Index Marker — 0.1 seconds
(Binary zero or uncoded Element)

c. Code Digit — 0.25 seconds.
(Binary one)

d Position Identifier 1 per 5 seconds — 0.4 seconds
(Refers to the leading edge of the succeeding Element)

e Reference Marker 1 per minute — Two consecutive Position Identifiers.
(The 'on time' point, to which the Code Word refers, is the leading edge of the second Position Identifier)

FIGURE 4
IRIG STANDARD TIME CODE – FORMAT "C"

ARL - UT
AS-74-356
LLM - DR
3 -25 -74

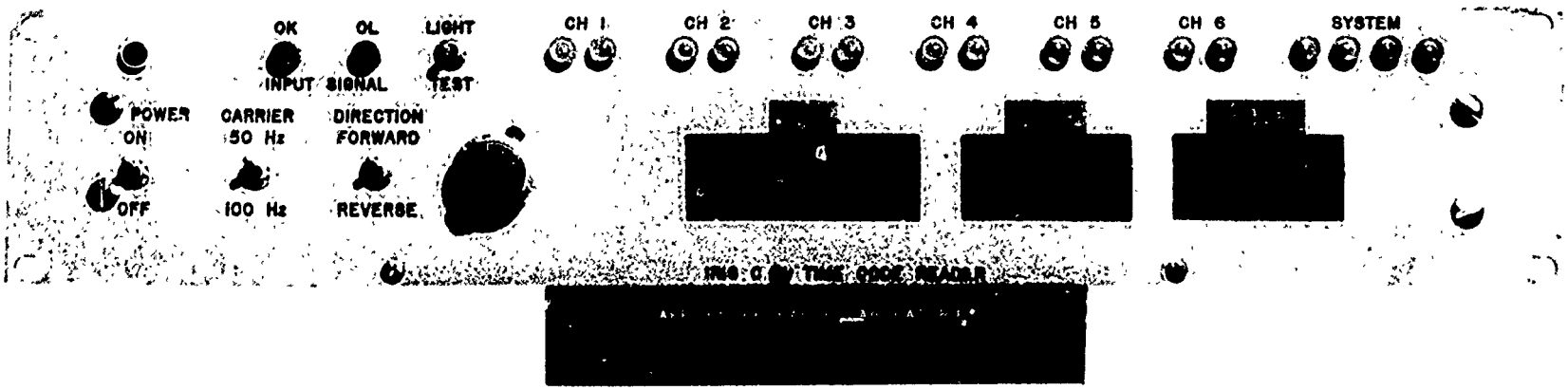
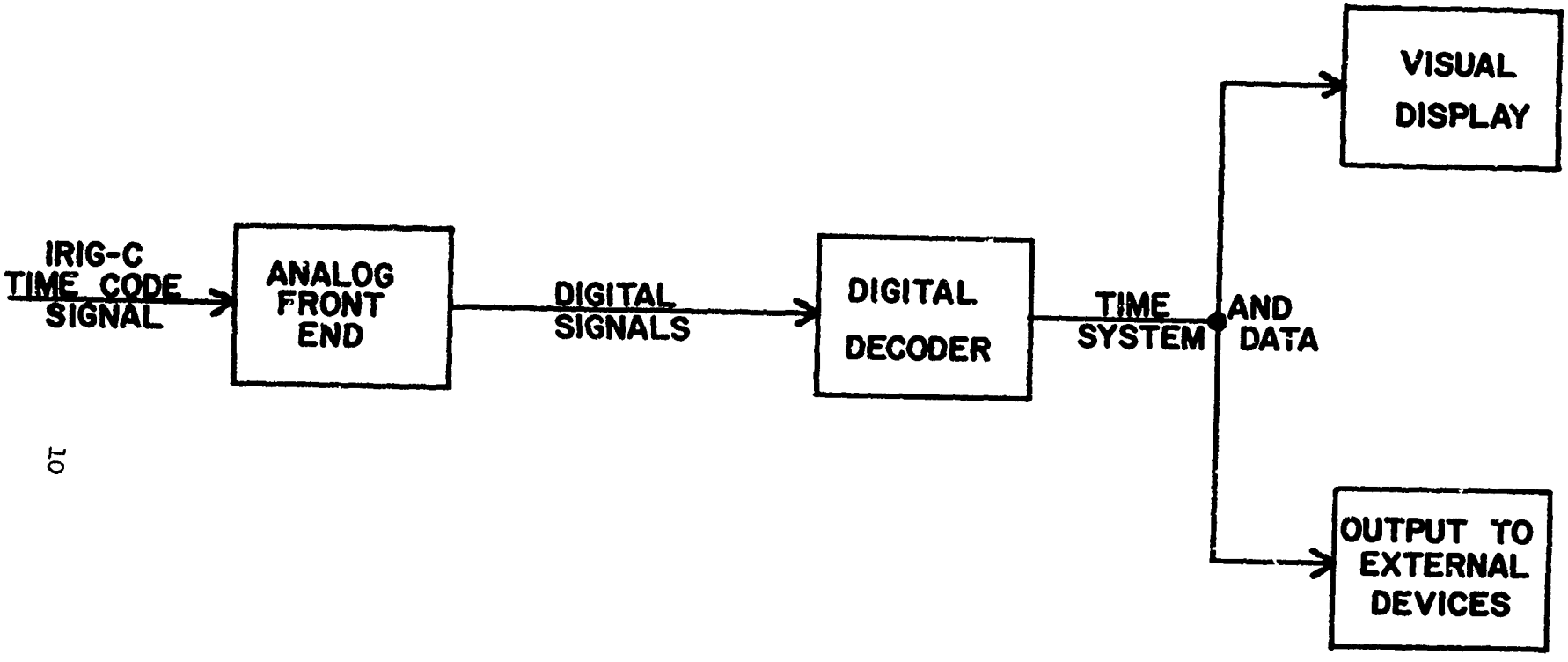


FIGURE 5
TIME CODE READER – FRONT PANEL VIEW



ARL - UT
AS-74-357
LLM - DR
3 - 25 - 74

FIGURE 6
ARL TIME CODE READER – BLOCK DIAGRAM

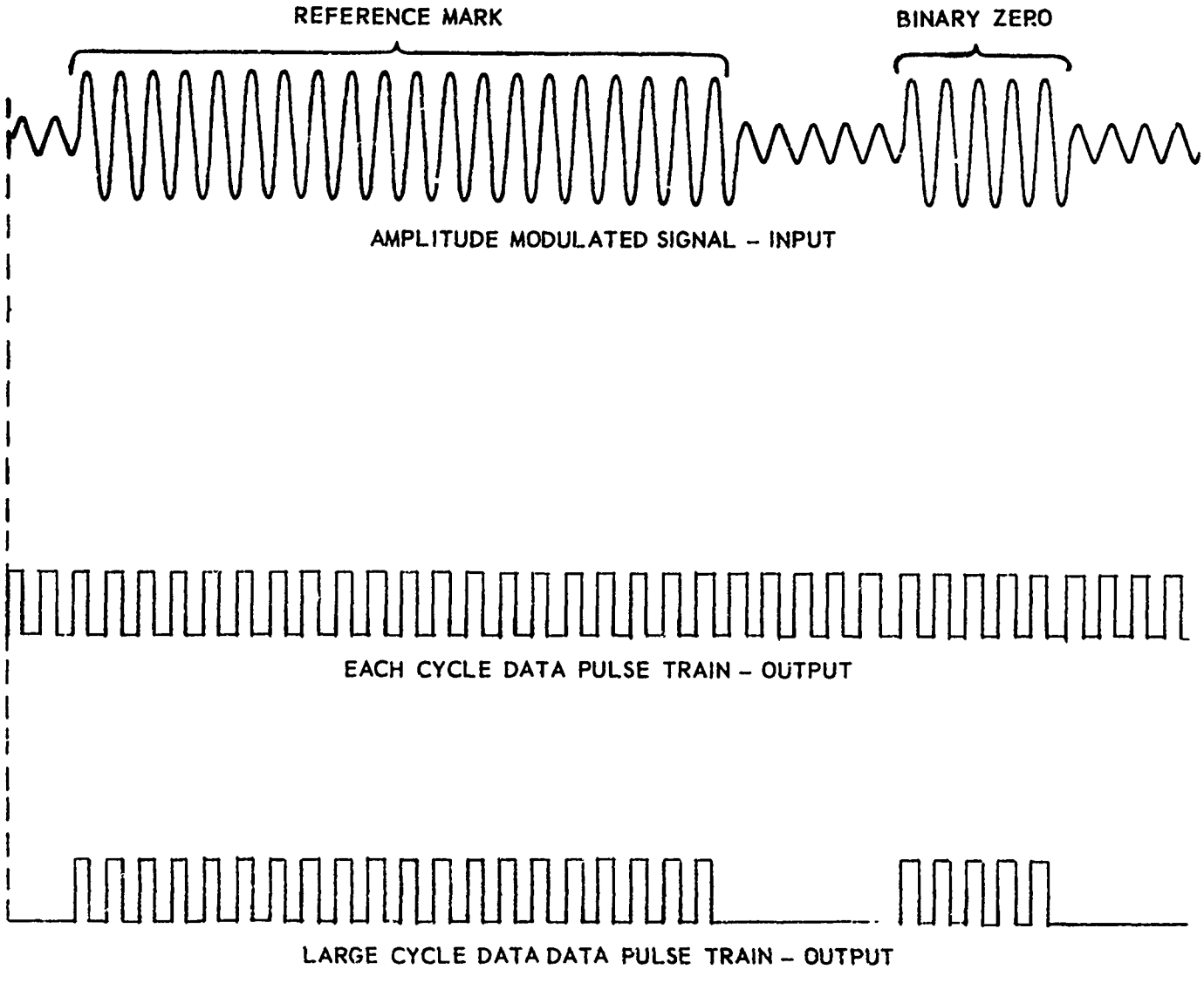


FIGURE 7
CODE STRIPPER INPUT AND OUTPUT SIGNALS

ARL - UT
AS-74-358
LLM - DR
3 - 25 - 74

2.1.3 Modified IRIG-C Time Code

IRIG-C is one of the standard time code formats devised by the Interrange Instrumentation Group. It consists of a sine wave carrier signal which has been amplitude modulated by a level shift signal. Figure 4 illustrates all of the more pertinent characterisitcs of the IRIG-C time code. Basically, it is a serial code generated as a continuous series of time frames. The frame length is 1 min and remains constant from one frame to the next. Changes occur only in the time information which is coded into the frame.

Each time frame consists of a series of 120 gated pulses each of which has a modulated amplitude ≧3.3 times the carrier amplitude. The cw pulses correspond to coded elements of recorded time, and the period from leading edge to leading edge of each pulse is called the index count and is 0.5 sec for IRIG-C. Every tenth pulse is called a position identifier (PI), or mark, and these pulses are used for synchronization during playback and decoding. The start of a new time frame is designated as the leading edge of the first pulse following the twelfth PI of the previous time frame. Thus the beginning of each time frame is characterized by two PI's which occur during two successive index counts. These two adjacent PI's are designated as a reference marker (RM).

The recorded time duration of each gated pulse (coded element) determines whether it is a position identifier or a "0" or "1" weighted binary element. These time durations are listed in the data block of Fig. 4. The identity (i.e., minutes, tens of minutes, etc.) of each bit of coded information is determined solely by the location of that particular coded element within the time frame. IRIG-C time information is encoded in that part of the time frame between position identifiers P1 and P5.

The IRIG-C time code format used on the ACODAC recordings is a version of the standard IRIG-C with two modifications. As noted above,

it is based on a 50 Hz carrier frequency as opposed to the standard 100 Hz carrier. Also, some ACODAC system information is contained between position identifiers P5 and P7. The same information is repeated between P7 and P9. Specifically, bits 1 through 4 and 6 through 9 after P5 and bits 1 through 4 after P6 contain the gain states of the six data amplifiers of each ACODAC unit (2 bits per amplifier channel). Bits 6 through 9 after P6 contain a binary system identification number, which is the serial number of the ACODAC unit from which the data tape was acquired.

2.2 Theory of Operation

The amplitude modulated sine wave is input to the analog section of the TCR. If the signal meets certain requirements, the time information is "stripped" from the signal and is output to the digital section via two pulse trains as indicated in Fig. 7.

The digital section of the TCR then decodes the data which is essentially contained in the large cycle (LC) pulse train. Each group of LC pulses comprises a coded element, i.e., a "0", a "1", or a position identifier. Applying the coded element time durations from Fig. 4 to 50 Hz and 100 Hz carrier frequencies produces the equivalent numbers of cycles tabulated in Fig. 8. During each index count (0.5 sec), at least one coded element must appear. Thus the basic decoding is accomplished by determining both when an LC pulse group occurs and the total number of LC pulses in the group. The number of pulses indicates the occurrence of a "0", "1", or "PI" and, by detecting two PI's in succession, the occurrence of a reference marker (RM) is ascertained. The RM signifies the beginning of the 1 min "time frame," and the PI's segment the time frame into 12 "sub-frames," each having a recorded time duration of 5 sec. The TCR utilizes the occurrence of the RM's, PI's, and the individual coded elements to sequence the data read and store operations.

CARRIER FREQUENCY	50 HZ	100 HZ
INDEX COUNT	25 CYCLES	50 CYCLES
"0"	5 CYCLES	10 CYCLES
"1"	12.5 CYCLES	25 CYCLES
POSITION IDENTIFIER	20 CYCLES	40 CYCLES

FIGURE 8
IRIG-C DATA IN TERMS OF CYCLES
OF THE CARRIER FREQUENCY

The results of the digital decoding of the input data are stored in output registers; these are updated when the PI occurs that follows the sub-frame in which the data was contained. Both the displays and the external outputs are driven by these registers.

2.3 Functional Description

2.3.1 Analog Section

2.3.1.1 Signal Level Sense

The time code is received in analog form on board No. 1 shown in Fig. 9. Operational amplifier A1 is configured as a noninverting unity gain buffer amplifier, providing a 100 kΩ input impedance. The time code information is then presented to operational amplifiers A4 and A5, which are configured as comparators.

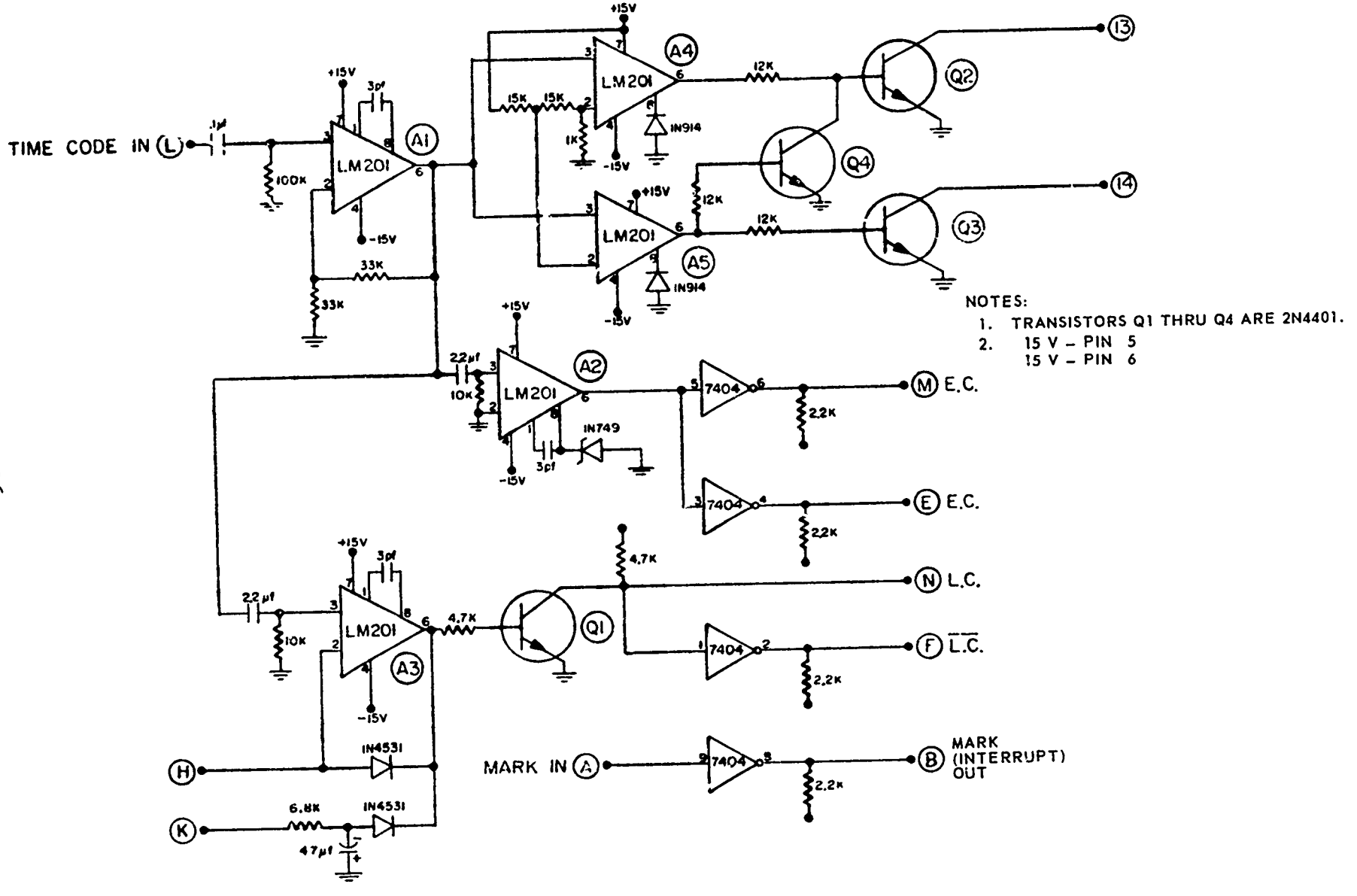
Amplifier A4 is triggered when the buffered input signal is greater than 0.5 V peak. This indicates sufficient amplitude for the time code stripper operation. Transistor Q2 detects the output of A4 and activates a green OK lamp on the front panel when the input signal is adequate.

Amplifier A5 is triggered on signals greater than 7.5 V peak to indicate an overload situation. The transistor Q3 detects the overload signal from the amplifier A5 and activates a red OL lamp on the front panel.

Time code information that satisfies the level sense circuitry will be within the dynamic range of the code stripper.

2.3.1.2 Code Stripper

The code stripper provides each cycle (EC) and large cycle (LC) information for the digital part of the reader. The EC information is obtained by operational amplifier A2 which is configured as a zero crossing detector. The zener diode connected to pin 7 limits the output of the amplifier to TTL levels.



NOTES:

1. TRANSISTORS Q1 THRU Q4 ARE 2N4401.
2. 15 V – PIN 5
   15 V – PIN 6

FIGURE 9
ANALOG SECTION – CIRCUIT

ARL - UT
AS-74-391
LLM - DR
3 - 25 - 74

The 7404 hex inverter gates provide an inverted and buffered output to both the digital circuitry for processing and the back panel for monitoring.

The LC information is obtained by the operational amplifier A3, which is configured as a negative peak detector. If, upon observing the input signal, the positive part of the modulation appears to be most favorable for detection, the time code reader input should be inverted. The peak detector operation is accomplished by the comparison of the input voltage on pin 3 with the voltage on pin 2. If the voltage on pin 3 is greater than the voltage on pin 2, the output (pin 6) of A3 goes to +15 V, and the diodes CR2 and CR3 block any current flow to C_7. If, however, the voltage on pin 3 is less than the voltage on pin 2, the output goes to -15 V. This provides, by way of the diodes, a negative voltage on C_7 and pin 2 that is slightly less than pin 3, thereby making the output once again go to +15 V. A negative charge thus is left on C_7 which corresponds to the most negative voltage applied by the input signal to pin 3. The charge on C_7 decays through the resistor network R7, R8, and R9 at a rate that is very slow compared to the modulation period of the time code. When the output of A_3 is positive, the voltage on pin 2 is established by the stored voltage on C_7 and the divider network R7, R8, and R9. Hence, during the next negative cycle provided by the input signal, the voltage on pin 2 is slightly less negative than that on C_7 and represents a threshold level.

During operation, the charge on C_7 is maintained at the negative peak level of the input signal. The threshold voltage on pin 2 is set by the variable resistor R8. Input cycles that are not more negative than the threshold are not recorded as large cycle information. Input cycles that become more negative than the threshold cause the amplifier A3 to change state, thus indicating a large cycle.

The most desirable setting for the threshold will vary according to the quality of the time code information. In general, the threshold may be set at 90% of the peak negative voltage on C_7. However, if the information is subject to dropouts or ripple with modulation greater than 10% of the peak signal, errors will occur. The threshold should then be adjusted to a less negative voltage to permit identifying large cycles with variations in amplitude. A proper threshold setting may be found if the dropouts or ripple do not modulate the signal as much as the time code itself.

Once the large cycle information has been identified by the detector circuit, the output of A3 is converted to TTL logic levels by transistor Q1 and routed to the digital circuitry by pin N. As with EC information (above), a buffered output is provided to the rear panel for monitoring.

2.3.2 Digital Section

Figure 10 is a simplified block diagram of the digital decoder and displays. Note that the blocks are indicated as dashed lines in the schematics (Figs. 11, 12, and 13).

2.3.2.1 LC Reset Circuit

The EC and LC signals from the analog section are input to the LC reset circuit. This circuit detects the end of each group of LC pulses. Subsequently it outputs 2 separate pulse signals to the LC counter and decoder. Each of these signals consists of a single pulse having a duration of 2 μsec. The first of these to occur is the data latch pulse which is output 1 cycle of the carrier after the end of the LC pulse group. Then the LCR (LC reset) pulse occurs 2 carrier cycles later.

The LC reset circuit also produces the LC1 signal. This is a relatively very short pulse with a fixed duration of 4 μsec and it is triggered by the leading edge of each LC pulse. Thus it is simply an abbreviated LC pulse.

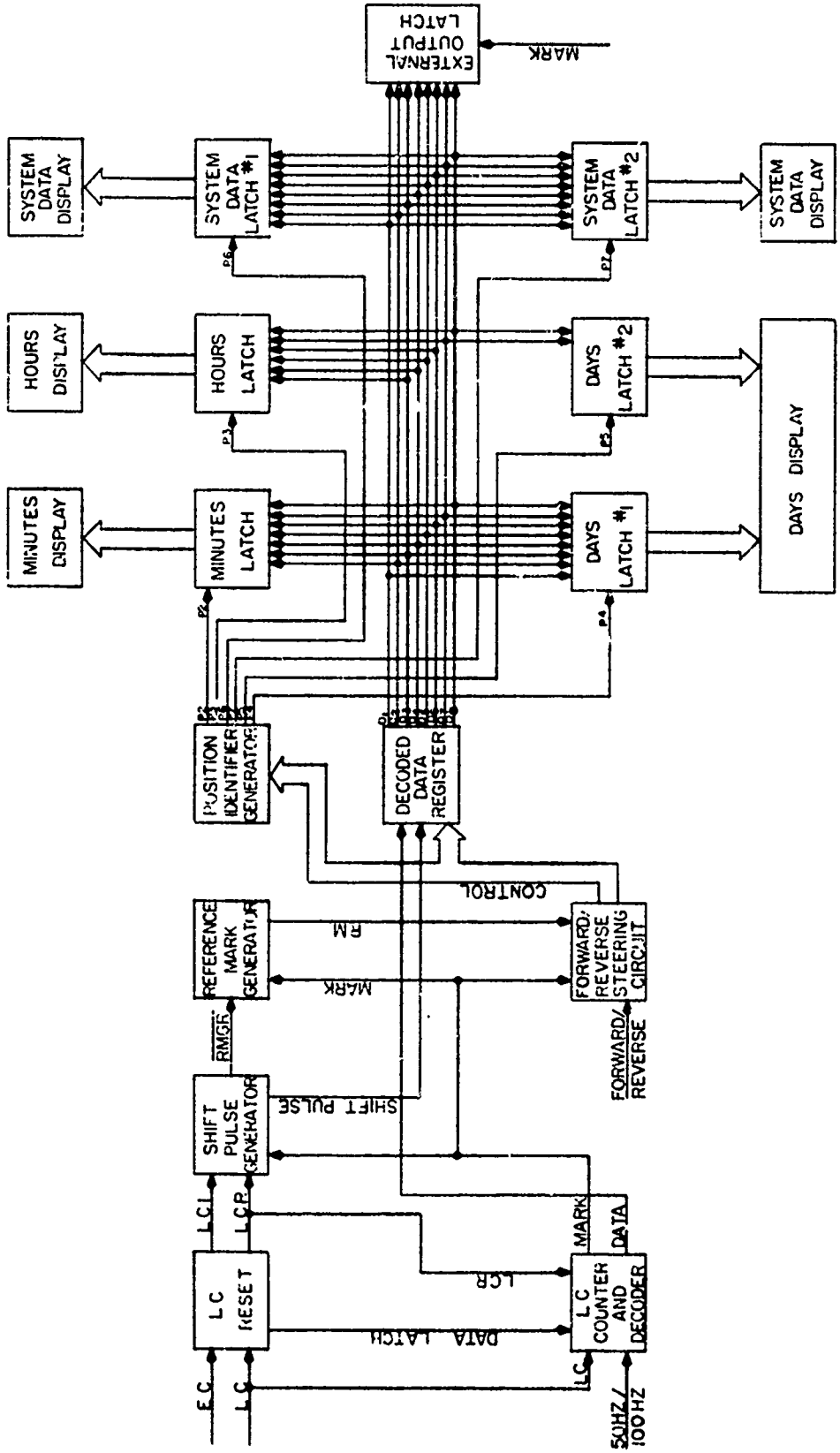


FIGURE 10
DIGITAL DECODER AND DISPLAYS – BLOCK DIAGRAM

ARL - UT
AS-74-393
LLM - DR
3 - 25 - 74

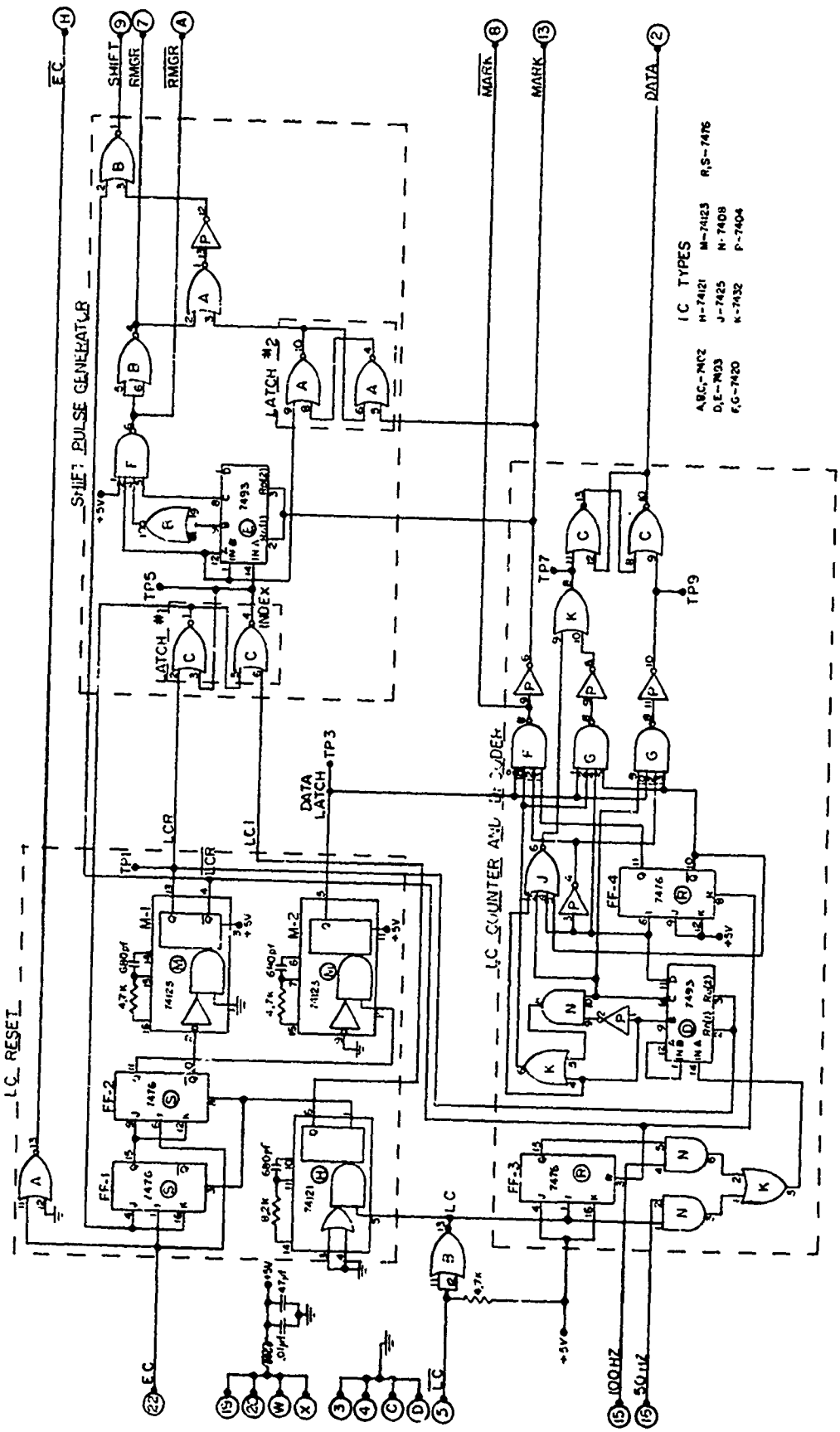


FIGURE 11
LC RESET, COUNTER, DECODER,
AND SHIFT PULSE GENERATOR – CIRCUIT

ARL - UT
AS-74-395
LLM - DR
3 - 25 - 74

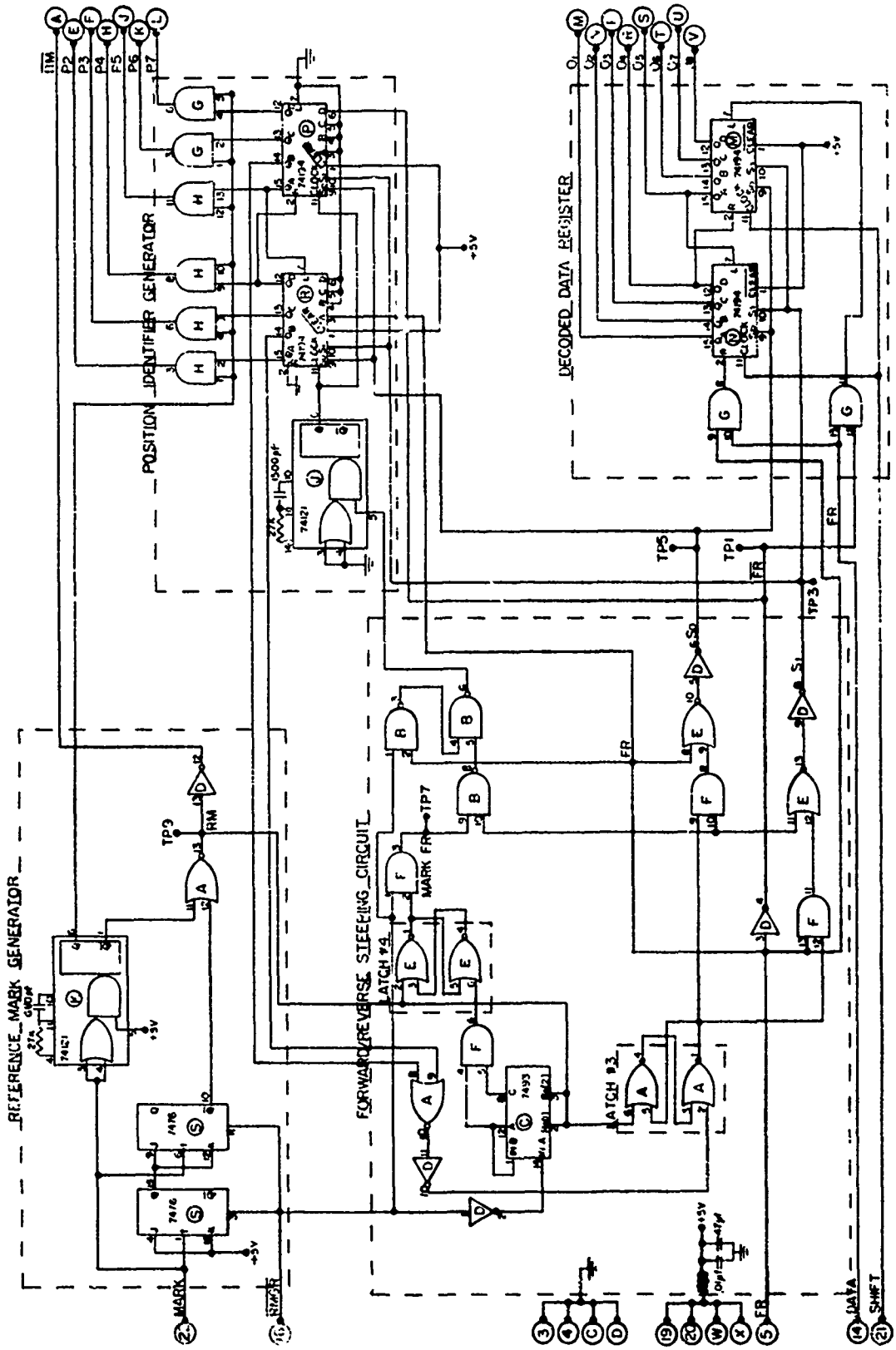


FIGURE 12
RM AND PI GENERATOR AND DECODED DATA REGISTER – CIRCUIT

ARL - UT
AS-74-396
LLM - DR
3 - 25 - 74

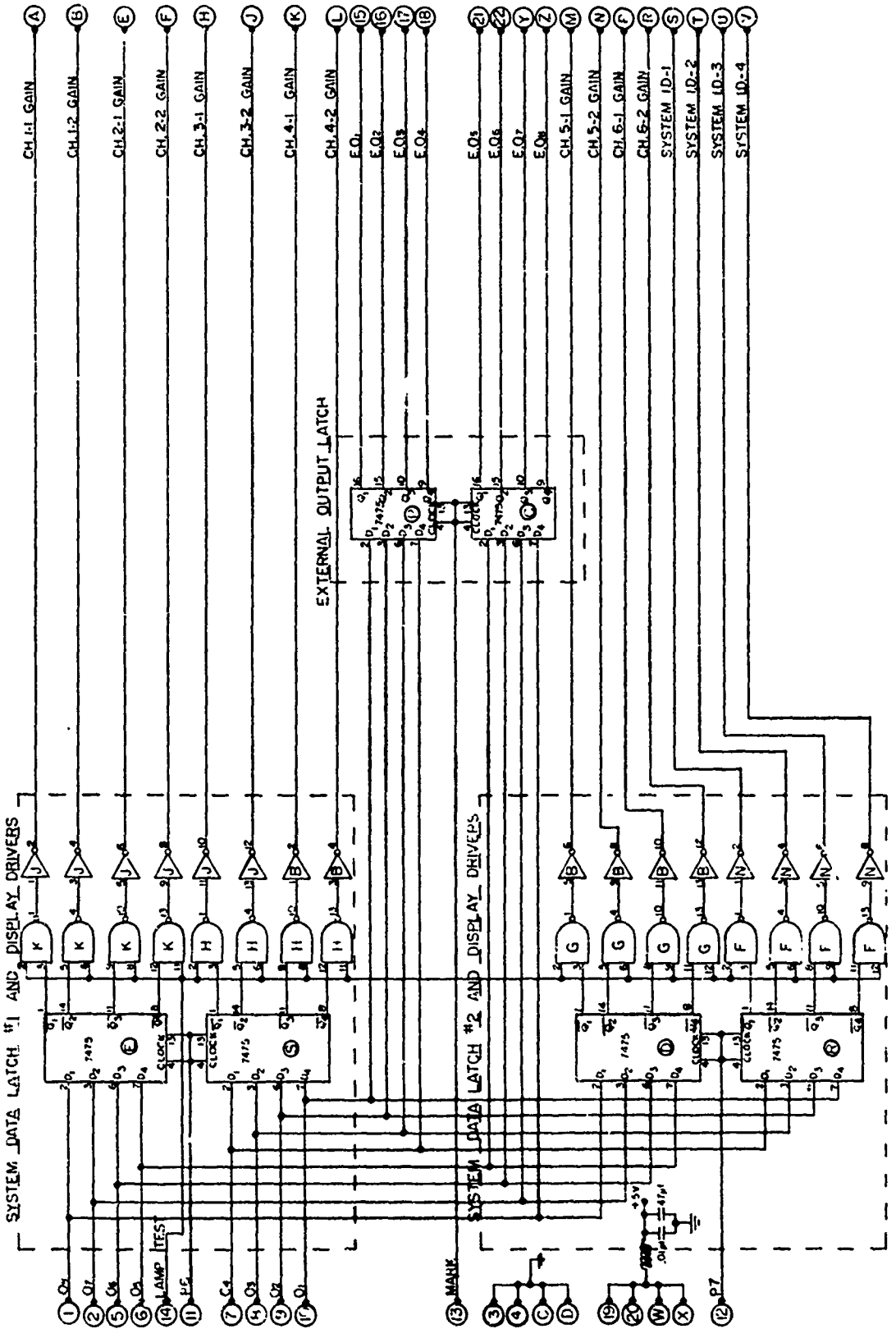


FIGURE 13
DATA LATCHES AND DISPLAY DRIVERS - CIRCUIT

ARL - UT
AS-74-397
LLM - DR
3 - 25 - 74

2.3.2.2 LC Counter and Decoder

The LC signal from the analog section is also input to the LC counter and decoder along with 50 Hz and 100 Hz carrier select signals from the switch on the front panel. This circuit counts all of the pulses in each LC pulse group if the 50 Hz carrier option has been selected. If the 100 Hz carrier option is selected, a flip-flop first performs a binary division on the LC pulse train and thus counts only one-half of the LC pulses in each group. This is the only circuit provision necessary to accommodate time codes based on the two different carrier frequencies. Subsequently, the digital decoder performs all of the logical functions based on a 50 Hz carrier.

The LC counting is performed by a 5-bit binary counter, the outputs of which are fed to an array of digital logic gates. These gates are configured such that they will detect any of three different groups of LC counts. The "0" gating will produce an output for a 4, 5, 6, or 7 LC count; the "1" gating will produce an output for an LC count of 10 through 17 inclusive; and the PI or MARK gating will produce an output for an LC count of 18 through 23 inclusive. The ideal numbers are 5 LC counts for a 0, 12 1/2 LC counts for a 1, and 20 LC counts for a PI or MARK (refer to Fig. 8). Thus the LC counter gating will accommodate a wide error margin in the code.

The final stage of the PI or MARK gating is logically AND-ed with the data latch pulse from the LC reset circuit, thereby producing a MARK pulse each time a position identifier is detected. This MARK pulse is used extensively throughout the remainder of the digital decoder for timing and synchronization and is also made available as an output so that the ARL computer (or any other external device) can use it for the same purposes.

The final stages of both the 0 and 1 gating are also AND-ed with the data latch pulse, and the resultant pulses are input to an R-S latch. The latch is configured so that its output will flip to

a high level anytime a 1 pulse is input to it, and will conversely flip to a low level for a 0 input pulse. Thus the data bit is stored in the R-S latch until the next data latch pulse occurs. The R-S latch output is fed to the decoded data register as the DATA signal.

After either a MARK pulse has been produced or the data have been stored as described above, the LC counter is reset to zero. This is done by the aforementioned LCR pulse which occurs two carrier cycles after the data latch. Then the LC counter and decoder is ready to count and decode the next group of LC pulses.

2.3.2.3 Shift Pulse Generator

There are three inputs to the shift pulse generator. They are the LCR and LC1 signals from the LC reset circuit and the MARK pulse from the LC counter and decoder. Using the LCR and LC1 signals, the beginning of each group of LC pulses is detected, thereby establishing an index signal. The index is input to a 3-bit binary counter which is reset to zero by the MARK pulse. The outputs of the index counter are gated so that the occurrence of the 5th index count after the previous MARK is detected. The output gating of the shift pulse generator is then configured to produce a shift pulse at the beginning of each group of LC pulses except for the 5th LC group after the previous MARK. The reason for skipping this 5th shift pulse will be discussed in the section on the decoded data register.

2.3.2.4 Reference MARK Generator

The reference MARK generator detects the occurrence of two adjacent position identifiers or MARKS. This is accomplished by inputting the MARK signal to a 2-counter. Reset of the 2-counter is performed by the $\overline{\text{RMGR}}$ (reference mark generator reset) signal from the shift pulse generator. Since the $\overline{\text{RMGR}}$ occurs during the 5th LC group after the previous MARK, the counter will reach a count of two only when the MARKS occur in adjacent LC groups. Upon detection of two adjacent MARKS, the reference MARK generator outputs an RM (reference MARK) pulse signal.

2.3.2.5 Decoded Data Register

This register accepts and stores all of the significant data which occur between two successive PI's, i.e., during each subframe. At the end of the subframe, the acquired data bits are all available on parallel output lines to the output data latches.

The modified IRIG-C time code which the ARL-TCR is designed to read has no significant data in the 5th coded element (LC pulse group) of each subframe. Therefore each subframe contains only 8 significant data bits. The data from the LC counter and decoder is shifted into the decoded data register by the shift pulses from the shift pulse generator. Although the LC counter and decoder identifies all of the coded elements within a subframe, the shift pulse for the 5th data bit after each PI is inhibited by the shift pulse generator. Thus the 5th coded element in each subframe is ignored.

The decoded data register is comprised of an 8-bit serial-in, parallel-out bidirectional shift register and two data input gates. These gates are driven by the forward/reverse (F/R) steering circuit and direct the data to the right serial or left serial input of the shift register for forward or reverse data acquisition respectively. The F/R steering circuit also provides clocking and initial loading of the register so that the data is right-shifted for forward data acquisition and left-shifted for reverse data acquisition. These functions are performed by the F/R steering circuit in order that the parallel data bit outputs (O_1 through O_8) available at the end of each subframe are in the same order regardless of whether the time code is being read in the forward or reverse direction.

2.3.2.6 Position Identifier Generator

The PI generator sequentially produces 6 successive PI pulses with a fixed length of 10 μsec, each on a separate signal line.

These PI pulses occur in time coincidence with the MARK pulses that follow the subframes containing time code or ACODAC data. Thus, the PI pulses produced for the forward direction of data acquisition are P2, P3, P4, P5, P6, and P7, and are fed to the data output latches. There they are used to update the data in each output latch once per time frame. This will be explained in more detail in the section on the data output latches.

When the reverse direction of data acquisition is selected, the PI pulses required to update the data output latches must be coincident with P6, P5, P4, P3, P2, and P1, in that order. Therefore, in the reverse read mode, the PI pulse on the signal line labeled P7 is actually P6 and it is the first PI pulse to occur in that mode. Similarly, P6 is replaced by P5 and so on, such that the last PI pulse to occur in the reverse mode is P1 and it appears on the signal line labeled P2.

The PI generator consists primarily of an 8-bit, parallel-in, parallel-out bidirectional shift register together with a set of output gates which logically AND the shift register outputs with a MARK pulse. Only the 6 centermost outputs of the shift register are used since only 6 PI pulses are required. The right and left serial inputs to the shift register are grounded (set to zero). Initially, the shift register is loaded with a 1 in the first bit and zeroes in the other bits. Then, each time the shift register is clocked, the 1 will move to the next bit in the register and all of the other bits will be zeroes. Thus the 1 output is sequenced through the shift register, and the outputs, in conjunction with the AND-ed MARK pulse, provide the 6 sequential PI pulses.

The clocking and initial loading of the shift register is performed by control inputs from the F/R steering circuit. Essentially the shift register is clocked by MARK pulses selected by the F/R steering circuit to provide the PI pulse outputs in the proper order.

In the forward direction of data acquisition, the register is right shifted, and in the reverse direction it is left shifted. Thus the output sequence of the PI pulses is reversed for the two different directions.

2.3.2.7 Forward/Reverse Steering Circuit

An input from the forward/reverse direction switch on the front panel of the TCR informs the forward/reverse (F/R) steering circuit of the direction in which the time code is to be read. Then this circuit provides the necessary controls for the decoded data register and PI generator such that the proper information is obtained from time codes read in either the forward or reverse direction.

The data input control furnished to the decoded data register is simply a pair of complimentary signals (FR and $\overline{FR}$) which only change states when the position of the F/R switch is changed.

The RM pulse and the MARK pulse are both input to the F/R steering circuit. There they are used in conjunction with the input from the F/R switch to produce the signals necessary to control the direction in which the shift registers of the decoded data register and the PI generator are shifted. The F/R circuit also provides for the parallel load of the shift register in the PI generator.

The pulses used to clock the shift register in the PI generator are selected by the F/R steering circuit. This is accomplished by counting MARK pulses after the occurrence of the RM pulse. In the forward direction of data acquisition, the first MARK pulse is thus ignored and the succeeding MARK pulses are then output to the PI generator to clock its shift pulse. Similarly, in the reverse direction of data acquisition, the first 5 MARK pulses are ignored, thereby providing the proper sequence of clock pulses to the PI generator.

2.3.2.8 Data Output Latches

The parallel data lines from the decoded data register are fed to the data inputs of the output data latches. Although each of the latches has a maximum capacity of 8 bits, only the data lines required for each individual latch are input to it.

There are a total of seven output data latches, six of which are configured so that each stores the decoded data from one of the six subframes that contain time code or ACODAC information. Specifically the latches are designated: the minutes latch, the hours latch, the days latch No. 1 (units and tens of days), the days latch No. 2 (hundreds of days), the system data latch No. 1 (gain states of the first four data amplifiers in the ACODAC), and the system data latch No. 2 (gain states of the two remaining data amplifiers plus the system identification number). The data stored in each of these six latches is updated by the appropriate PI pulse. Thus the information which is decoded during each subframe is set into the output data latch by the PI at the beginning of the next subframe. In this way, all of these latches are updated once during each time frame.

The outputs of each of the six latches discussed above are fed directly to their associated displays. Consequently the displays are updated at the same time as the associated output data latches.

New data is clocked into the 7th output data latch (designated the external output latch) by each MARK pulse. Thus it is updated at the beginning of every subframe, and the eight data bits which it stores are the 1st through 4th and 6th through 9th coded elements of the previous subframe.

The eight output bits from this latch, along with the MARK for timing purposes, are fed to any external device via a connector on the rear of the TCR chassis. The specific external device to which these

outputs are fed during analysis of the ACODAC tapes is the CDC 3200 computer system at ARL.

2.3.3 Displays

2.3.3.1 Time Displays

Display of the time information is accomplished via three modules which are commercially produced by ESE of Inglewood, California. The minutes data and hours data are each displayed via a Model ES-922, 2-digit display module. The day's data is displayed via a Model ES-923, 3-digit display module. It should be noted that the wiring of the ES-923 module has been modified to allow a common latch clock for digits 1 and 2 and a separate latch clock for digit 3. Specification sheets which include schematics of the modules types of display are provided in Figs. 14 and 15. The modules contain a planar 7-segment incandescent display tube for each decimal digit; each tube is mounted on a printed circuit card along with a BCD-to-7 segment decoder-driver integrated circuit for each tube. In addition, the output data latch (the 7475 integrated circuits) associated with each of these displays is mounted on the same printed circuit card; this can be seen in the schematics. A lamp test for the display tubes of the modules is activated by momentary action of the lamp test switch on the TCR front panel.

2.3.3.2 ACODAC System Data Display

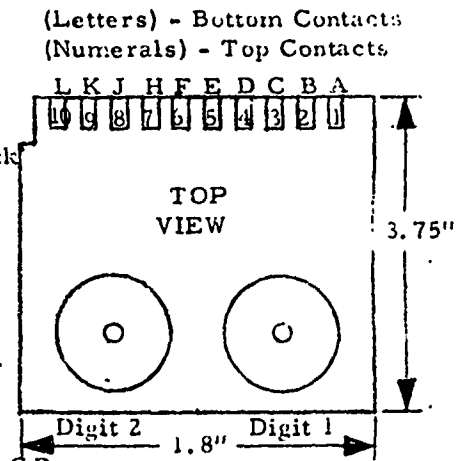
Display of the ACODAC system data contained between position identifiers P5 and P7 of the time code is accomplished via an array of 16 small incandescent panel-type lamps. Each lamp corresponds to one of the decoded data bits and its binary state is indicated as a 1 when lit and a 0 when not lit.

These lamps are each driven by an open collector type of integrated circuit inverter which is capable of sinking 40 mA of current. The inverters are in turn driven by an array of gates on the outputs of

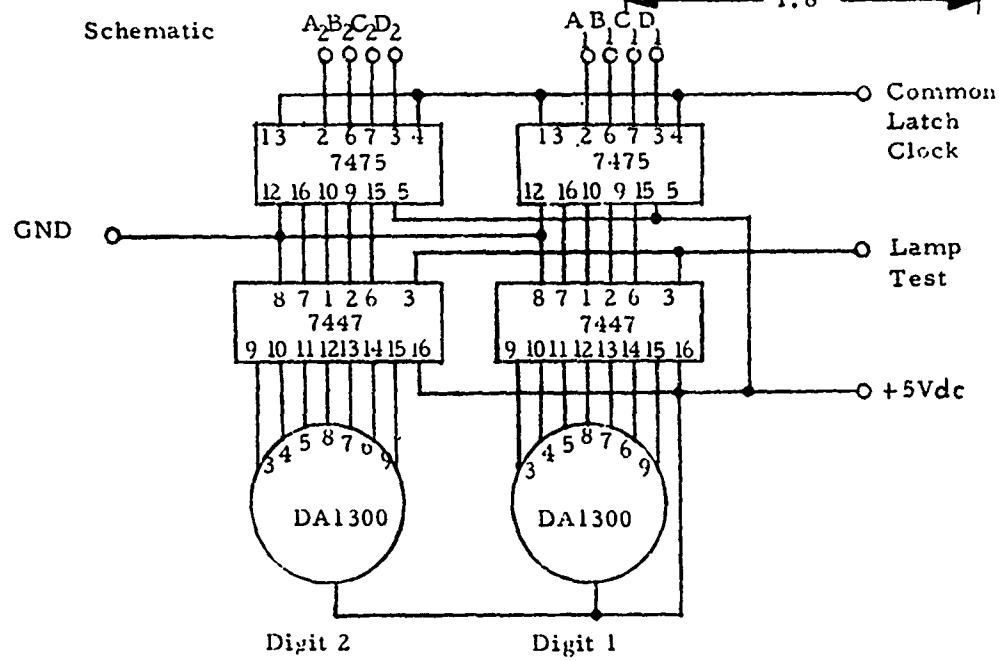
The ESE Model ES-922 is a 2 digit incandescent display module which operates from a single +5 Vdc supply.

Connector Contacts

Top Side		Bottom Side	
Contact	Function	Contact	Function
1	Ground	A	Lamp Test
2	+ 5Vdc	B	Common Latch Clock
3	B1	C	A1
4	C1	D	D1
5	B2	E	A2
6	C2	F	D2
7	-	H	-
8	-	J	-
9	-	K	-
10	-	L	-



Schematic



Electrical Specifications

Supply current drain will be typically 375 mA at +5Vdc. Complete data sheets on IC's and display tubes will be furnished upon request.

FIGURE 14
ESE MODEL ES-922 DISPLAY MODULE – SCHEMATIC

ARL - UT
AS-74-403
LLM - DR
3 - 25 - 74

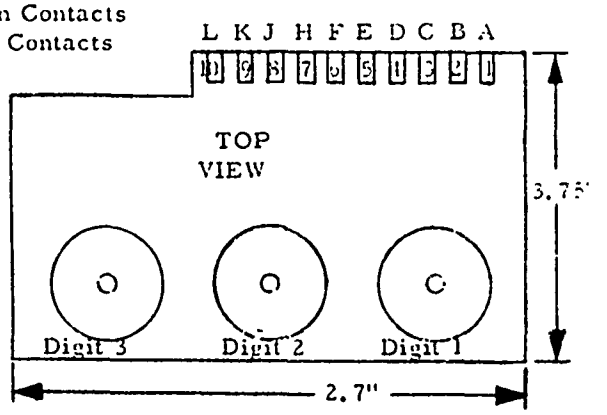
The ESE Model ES-923 is a 3 digit incandescent display module which operates from a single +5Vdc supply.

Mechanical

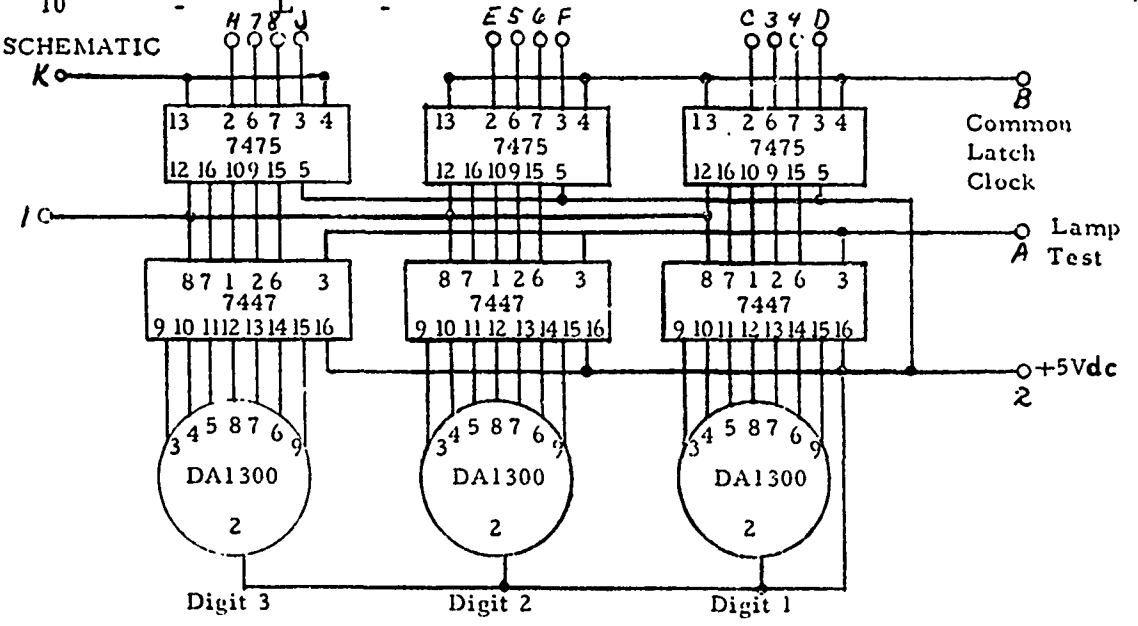
(Letters) Bottom Contacts
(Numerals) Top Contacts

CONNECTOR CONTACTS

Top Side Contact	Top Side Function	Bottom Side Contact	Bottom Side Function
1	Ground	A	Lamp Test
2	5Vdc	B	Common Latch Clock
3	B1	C	A1
4	C1	D	D1
5	B2	E	A2
6	C2	F	D2
7	B3	H	A3
8	C3	J	D3
9	-	K	-
10	-	L	-



SCHEMATIC



Electrical Specifications

Supply current drain will be typically 550 mA at + 5Vdc. Complete data sheets on IC's and display tubes will be provided upon request.

FIGURE 15
ESE MODEL ES-923 DISPLAY MODULE – SCHEMATIC

ARL - UT
AS -74-404
LLM - DR
3 -25 - 74

system data latches No. 1 and No. 2. The gates allow the display lamps to be tested simultaneously with the digital display modules by activating the LAMP TEST switch as described above.

Although the lamps are designed for 7.5 V operation, they are activated by only about 4.5 V in this application. The resulting brightness is still quite good, and the service life of the bulbs should be greatly extended.

2.3.4 Power Supply

The dc power required by the TCR circuits and displays is provided by a triple output power supply produced by Powertec, Inc., of Chatsworth, California. It is a model 2R-70T unit with outputs of 5 V at 6 A and ±15 V at 1.3 A each. The supply is also equipped with overvoltage protectors on each of its outputs. Schematics, specifications, and application data for the supply and overvoltage protectors are located in the manufacturers data in Appendix A.

2.4 Operation

2.4.1 Equipment Layout and Construction

The TCR is packaged entirely on a single 17.0 in. wide by 18.5 in. deep chassis behind a 3.5 in. high panel for mounting in a standard 19 in. wide rack. All of the input/output connectors are located at the rear of the chassis, and all of the controls and displays are located on the front panel. Except for the dc power supply and the display boards, all of the circuitry is contained on four circuit boards, each measuring 4.5 in. x 7.0 in. Board No. 1 contains the analog input section. Boards No. 2, 3, and 4 contain the digital decoder section.

Figure 16 is the chassis wiring diagram for the entire time code reader.

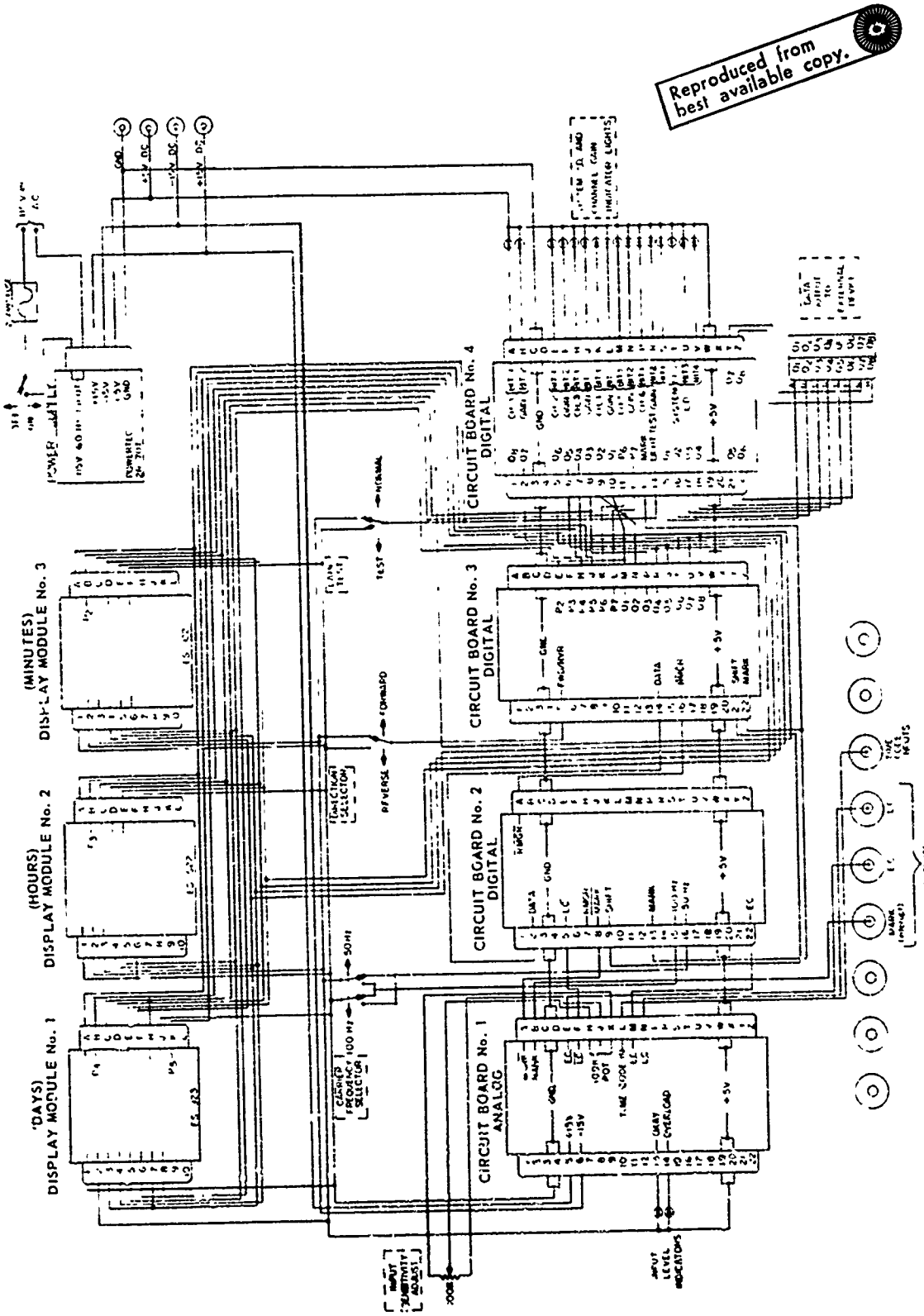


FIGURE 16
MAIN CHASSIS WIRING DIAGRAM

ARL : UT
AS-74-399
LLM : DR
3 - 25 - 74

2.4.2 Inputs/Outputs

All inputs to and outputs from the TCR are accomplished via connectors at the rear of the chassis (see Fig. 17).

2.4.2.1 Inputs

There are only two inputs to the ARL time code reader. A standard jack at the rear of the chassis provides an input for 115 V, ac, 60-cycle, single phase power required by the TCR.

The time coded signal is input to the TCR via a BNC type connector at the rear of the chassis. This signal must be an IRIG-C time coded signal based on either a 50 Hz or 100 Hz carrier. The playback speed of the tape must be maintained between a minimum of 1 times and a maximum of 160 times the recording speed of the tape. The amplitude modulation must be such that the ratio of modulated to unmodulated signal is at least 1.1.

2.4.2.2 Outputs

The time code reader outputs the following signals on BNC type connectors.

2.4.2.2.1 EC

The square wave corresponding to the carrier of the input time coded signal (uncommitted standard TTL output gate).

2.4.2.2.2 LC

The gated pulse train which corresponds to the large modulated cycles of the carrier (uncommitted standard TTL output gate).

2.4.2.2.3 MARK (interrupt)

The pulse signal which is produced each time a position identifier element is detected in the time code. This is used by the ARL CDC 3200 computer system for synchronization of the data analysis (uncommitted standard TTL output gate).

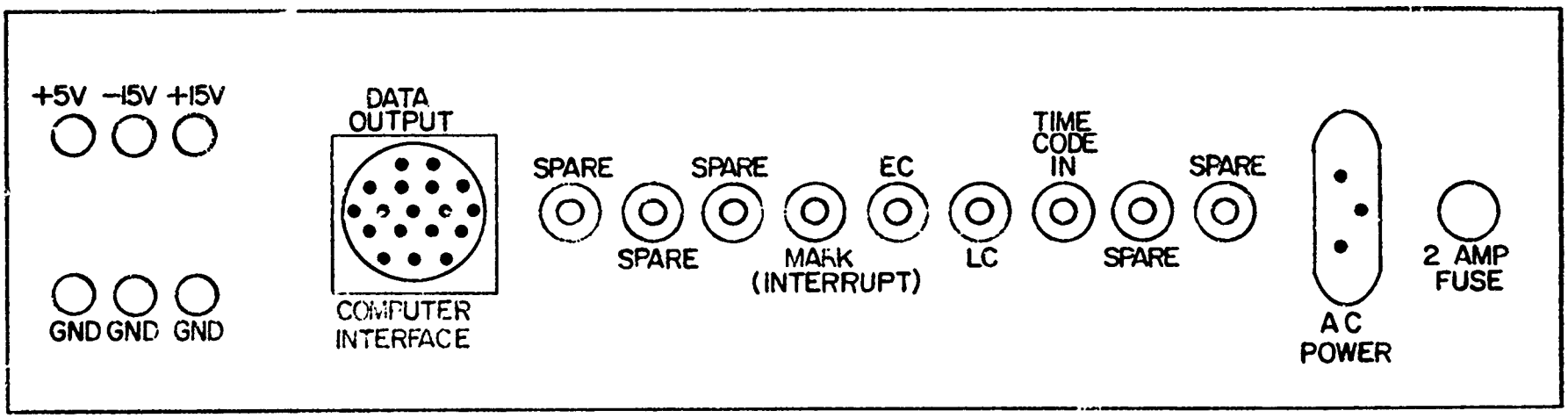


FIGURE 17
TIME CODE READER – REAR PANEL LAYOUT

ARL - UT
AS-74-360
LLM - DR
3 - 25 - 74

2.4.2.2.4 Reference MARK (RM)

Indicates the double position identifiers separating the minute intervals.

2.4.2.2.5 Data Output/Computer Interface

The eight digital data outputs (see wiring diagram for connector pin designations - Fig. 18) for use by an external device, such as the ARL computer system. These outputs are updated at the occurrence of each position identifier (MARK), and each data bit corresponds to one of the eight significant coded elements contained in the subframe prior to the position identifier (uncommitted standard TTL output gate).

2.4.3 Controls

All of the controls for the TCR are located on its front panel (see Fig. 5). The function of each is described below.

2.4.3.1 POWER, ON-OFF

Applies ac power to the TCR.

2.4.3.2 CARRIER, 50 Hz to 100 Hz

Provides the choice of reading IRIG-C time code based on either a 50 Hz or 100 Hz carrier.

2.4.3.3 DIRECTION, FORWARD-REVERSE

Provides the choice of reading the input IRIG-C time code in either the forward or reverse direction, referenced to the direction in which it was originally recorded.

2.4.3.4 LIGHT TEST

Activates all of the display circuits such that every lamp and every segment of the digital displays should light up to indicate its condition when this switch is momentarily depressed.

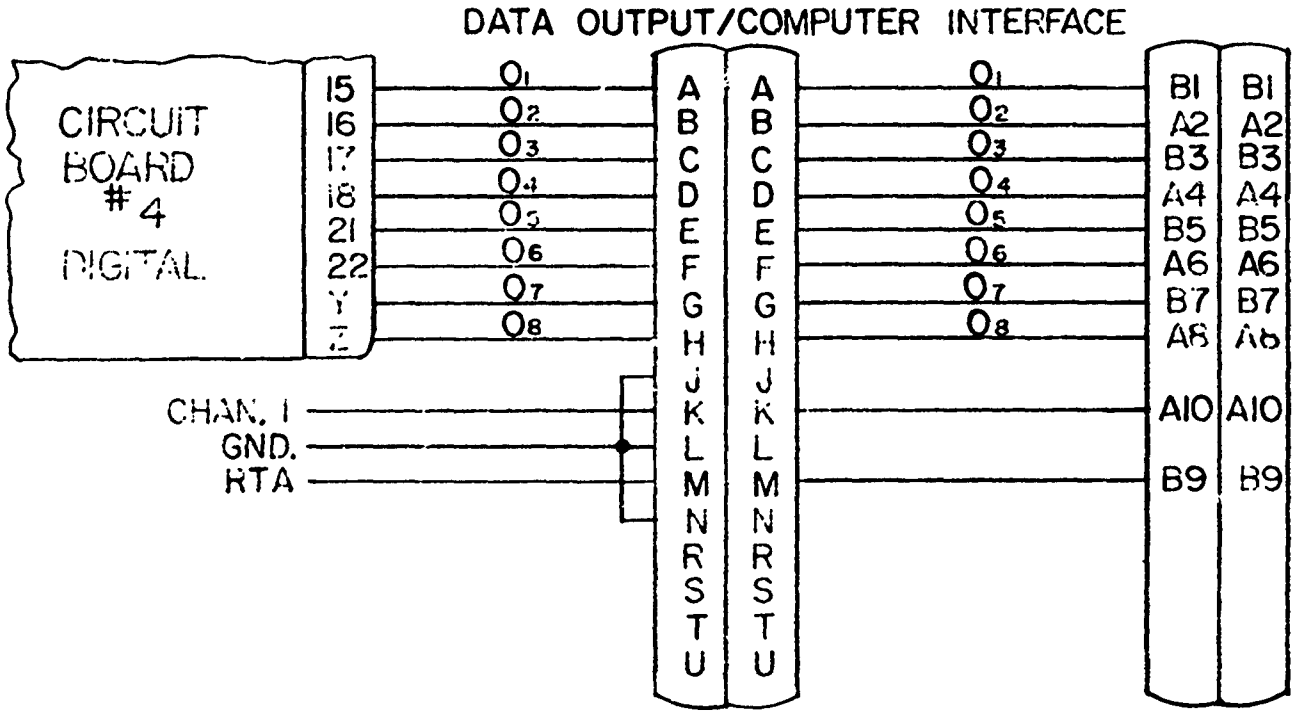


FIGURE 18
WIRING DIAGRAM FOR DIGITAL OUTPUT INTERFACE PLUG

ARL-UT
AS-74-361
LLM-RFO
3-25-74

2.4.3.5 Input Sensitivity

Permits adjustment of the input sensitivity to the TCR according to the discussion of paragraph 2.3.1.2.

3.0 PHASE LOCKED LOOP FREQUENCY MULTIPLIER

3.1 Introduction

3.1.1 Background

To compensate for fluctuations in tape recorder speed (record and playback), the reference signal used in digitizing analog signals recorded on tape needs to be synchronized to the tape speed. If the fluctuations in tape speed are not compensated for, the signals reproduced from the tape will vary in frequency due to those fluctuations. This will reduce the resolution of any frequency analysis performed on these signals. Thus, a phase locked loop frequency multiplier (PLFM) is employed which is synchronized to a reference signal on the tape. The PLFM will provide any desired harmonic of the reference signal required for digitizing and will compensate for the tape speed fluctuations. Figures 19 and 20 are graphs of the results of computing the power spectrum of a 100 Hz calibration signal produced from one of the ACODAC tapes. The signal was first digitized using 12 kHz as the sampling frequency. The graph of the power spectrum computed from these data is shown in Fig. 19. The tape was then redigitized, using as the sampling frequency the 12th harmonic of the time code signal. The power spectrum computed from these data is shown in Fig. 20. The improvement in the resolution of the computed power spectrum can easily be seen.

The ACODAC analog tapes have a 50 Hz signal that is used to encode time information which is used for a reference signal. Since the signals are reproduced at 20 times the recording speed, this time code signal used as an input to the PLFM has a nominal frequency of 1 kHz. The location of the PLFM in the data analysis system is shown in Fig. 21.

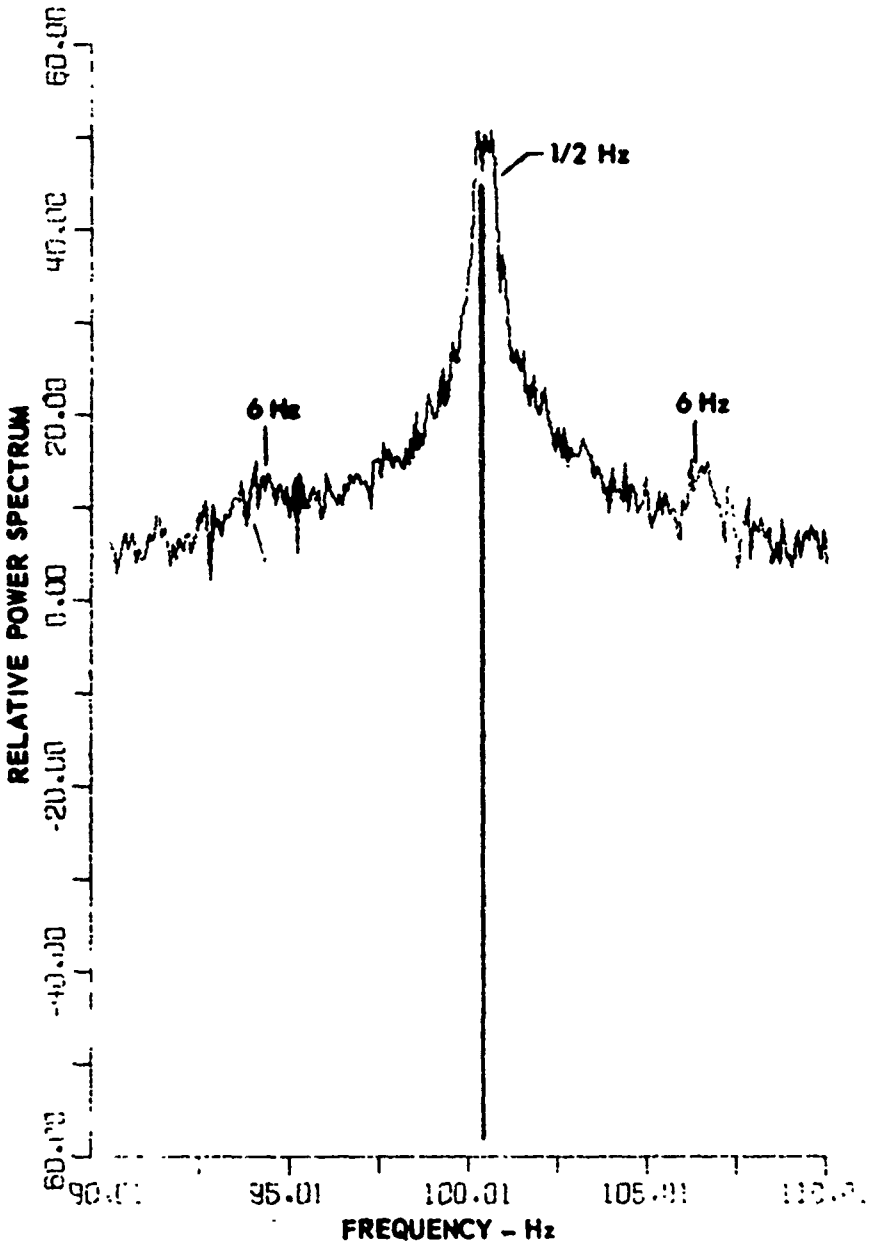


FIGURE 19
GRAPH OF THE POWER SPECTRUM OF
100 Hz CALIBRATION SIGNAL USING
A REFERENCE OSCILLATOR

ARL - UT
AS-74-362
LLM - DR
3 - 25 - 74

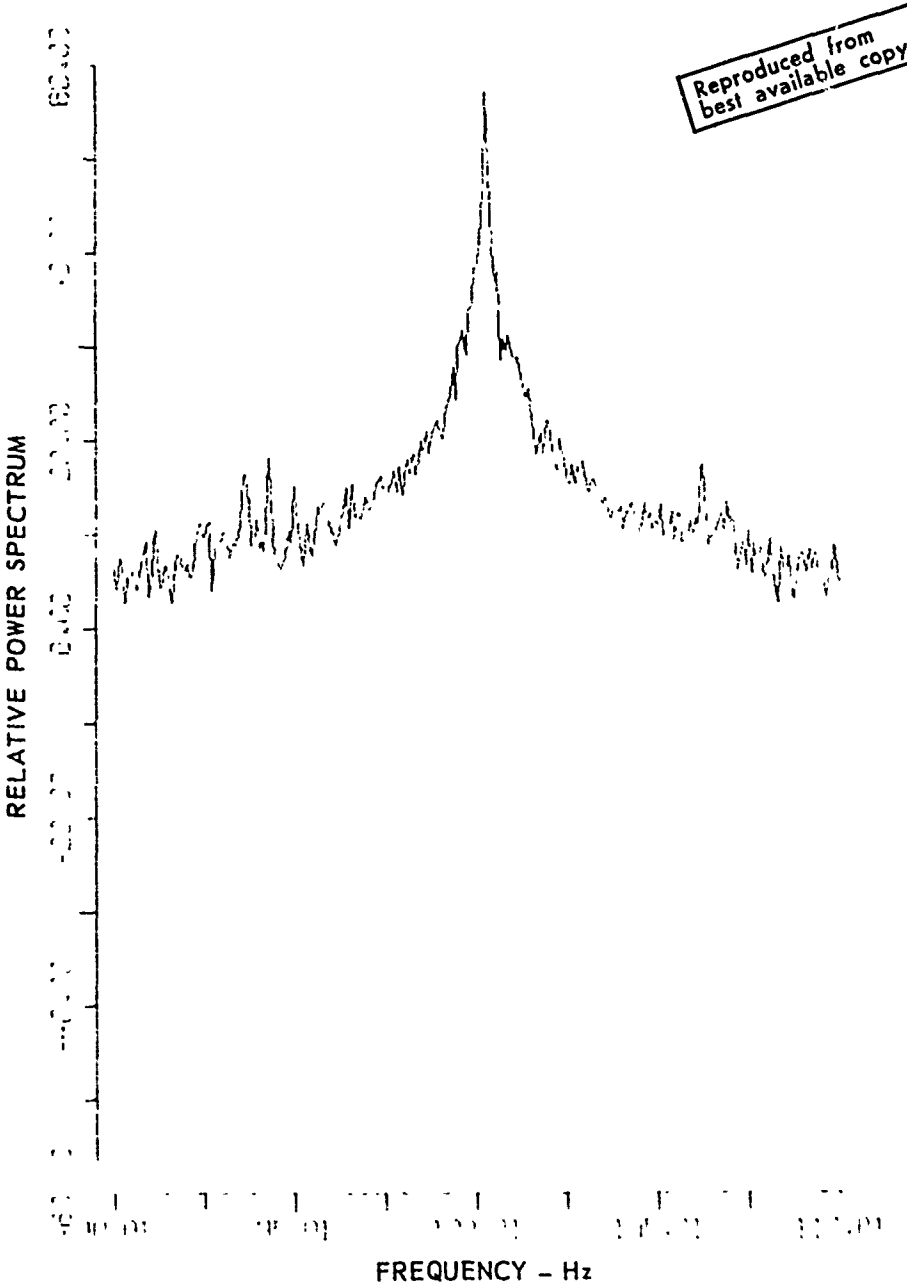


FIGURE 20
GRAPH OF THE POWER SPECTRUM OF 100 Hz
CALIBRATION SIGNAL USING THE PHASE
LOCKED LOOP FREQUENCY MULTIPLIER

ARL - UT
AS-74-363
LLM - DR
3 - 25 - 74

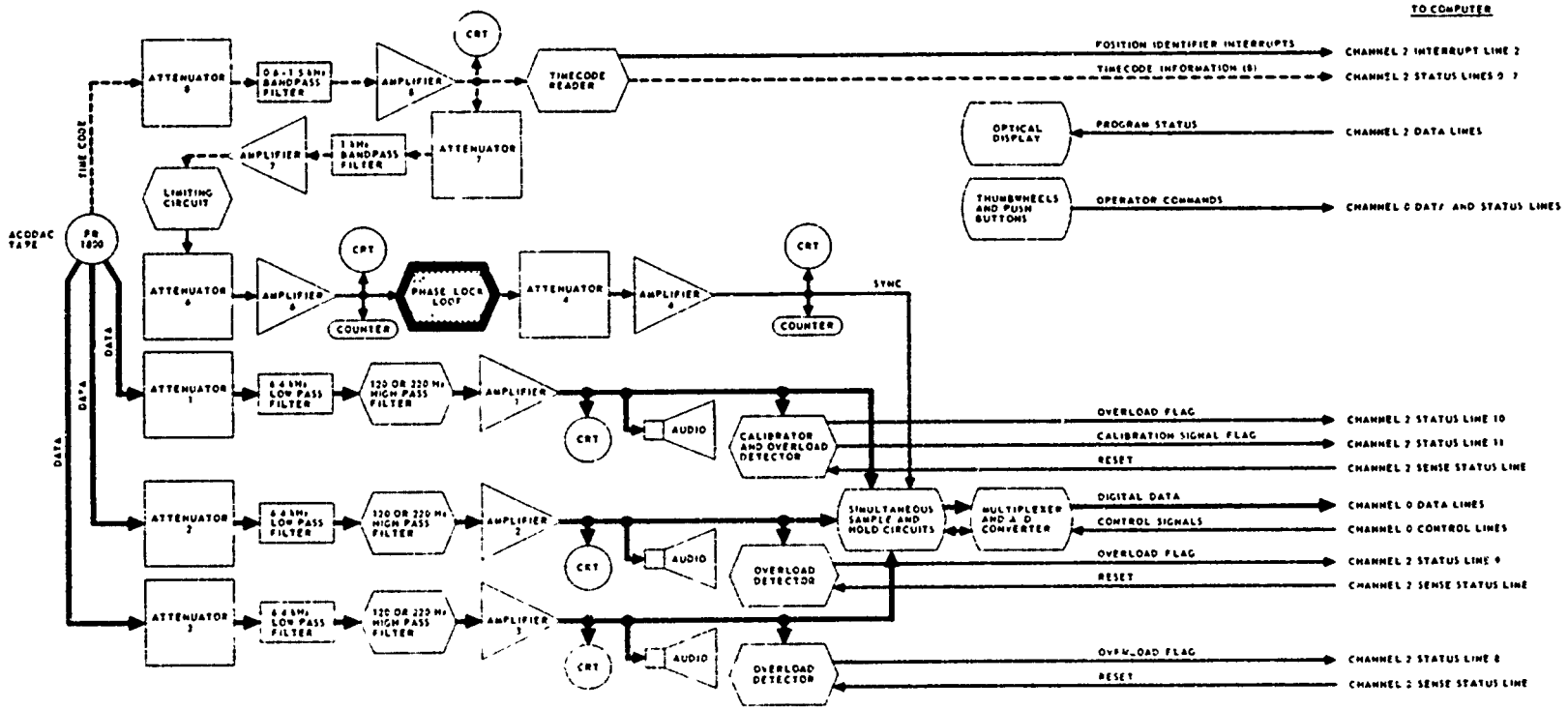


FIGURE 21
ANALOG EQUIPMENT CONFIGURATION FOR DIGITIZATION OF ACODAC DATA

3.1.2 General Description

The output frequency of the phase locked loop frequency multiplier (PLFM) is an integral multiple of the input reference frequency

$$f_o = N_o f_R \quad .$$

3.2 Theory of Operation

A block diagram of the PLFM is shown in Fig. 22. The output frequency (f_o) is divided by a binary counter to produce the frequency f_o/N. This frequency is compared with the reference frequency f_R in a phase detector; if the two frequencies are not identical, an error signal is produced. The error signal is then filtered and used to correct f_o until $f_o/N=f_R$.

3.3 Functional Description

The input, output, and power supply leads should be connected according to the markings on the case. The desired multiplier factor (N) in binary form is selected by using the eight toggle switches on the front panel of the PLFM. The convention used for the switches is down for 1 and up for 0, with the least significant digit being the switch farthest to the right.

Since the phase detector triggers off the trailing edges of the input signal, the fall times of the input signal should be kept as short as possible to reduce the time uncertainty to a minimum. The PLFM should be operated within the limits described below.

(1) 10 kHz $\leqq f_o \leqq$ 36 kHz
(2) $1 \leqq N \leqq 128$
(3) reference signal $\geqq$ 50 V p-p
(4) 9 V $\leqq$ power supply $\leqq$ 15 V at 200 mA

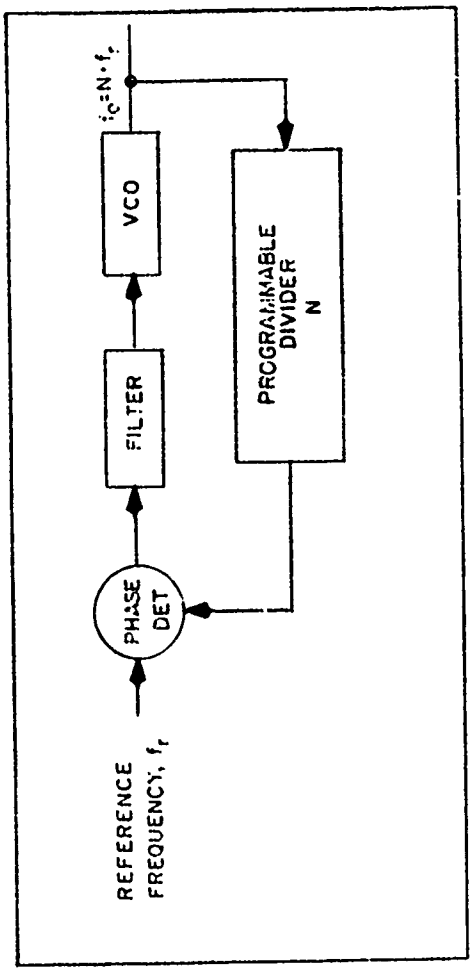


FIGURE 22
BLOCK DIAGRAM OF PHASE LOCKED LOOP
FREQUENCY MULTIPLIER (PLFM)

ARL - UT
AS-74-364
LLM - DR
3 - 25 - 74

3.4 Circuit Description

The circuit schematic is shown in Fig. 23. Its components and their operations are described in the following paragraphs. For a more detailed analysis of this type of circuit or certainly before attempting any modification of this circuit, it would be advisable to refer to the Motorola phase locked loop handbook. (3)

3.4.1 Phase Detector and Low Pass Filter

The phase detector and the active elements of the low pass filter are contained in the Motorola IC, MC 4044. A transistor (2N4401) and a diode (IN 914) have been added to the input to protect the phase detector from signals larger than 5 V. The active filter has a loop bandwidth (f_{BW}) of 8 Hz and a damping factor (δ) of 0.6.

3.4.2 Voltage Controlled Oscillator (VCO)

A Motorola MC 4024 IC is used for the VCO. The ratio of maximum frequency to minimum frequency for this VCO is approximately 3.5 to 1. The frequency range of the VCO in its present configuration is 10 kHz to 36 kHz, but this range can be raised or lowered by decreasing or increasing the size of the capacitor between pins 3 and 4.

3.4.3 Programmable Counter

The programmable counter consists of two Motorola MC 4018 IC's and will divide the VCO output by any number selected from 1 to 128.

3.4.4 Voltage Regulator

The low pass filter and the VCO obtain their power via a separate voltage regulator (Motorola IC MC 1723G) because of their extreme sensitivity to noise on their power supply. Any noise picked up in this way will be manifested as "jitter" on the output frequency.

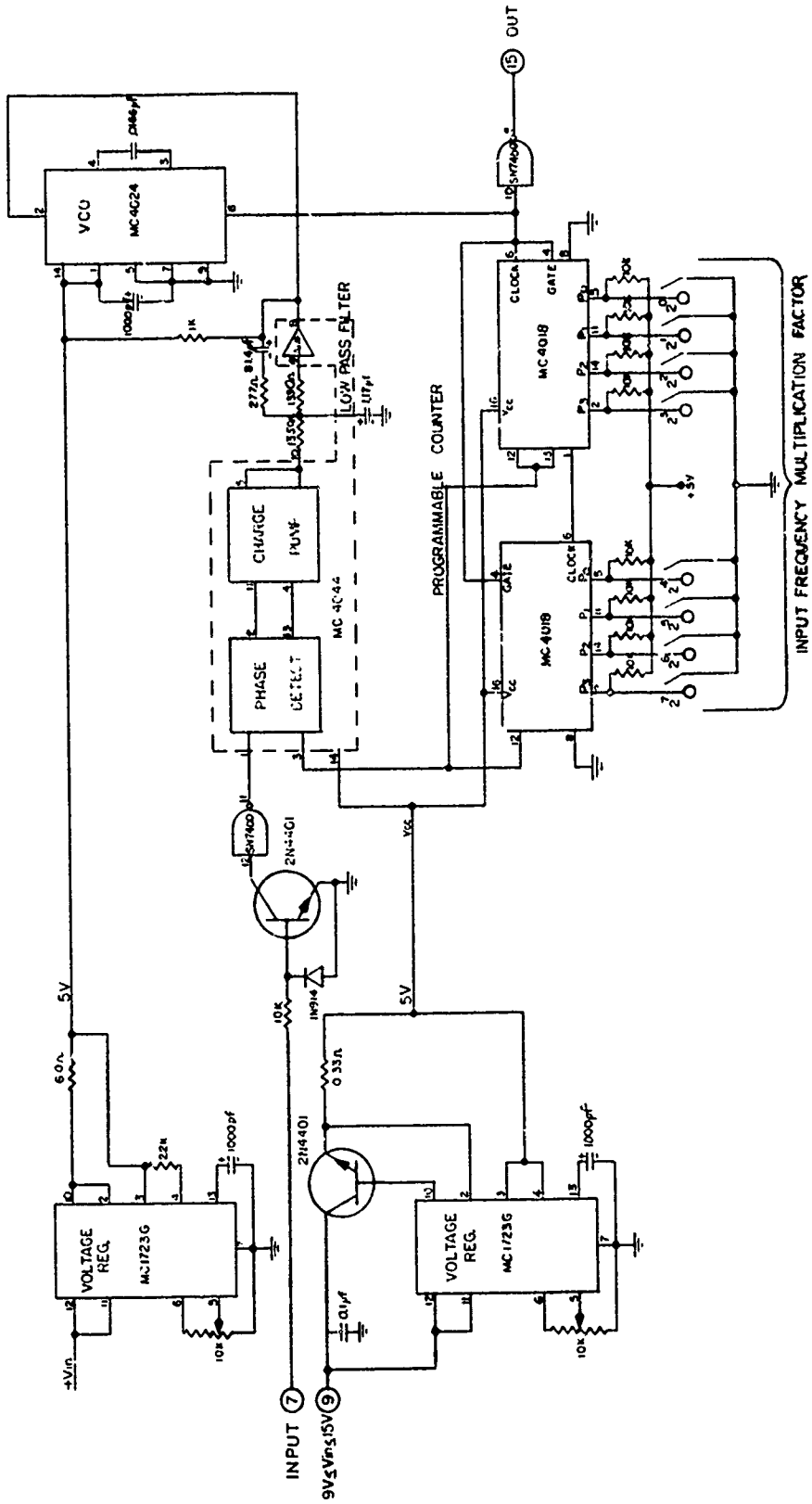


FIGURE 23
SCHEMATIC OF PHASE LOCKED LOOP FREQUENCY MULTIPLIER (PLFM)

ARL - UT
AS-74-398
PLLM - DR
3 - 25 - 74

4.0 HIGH PASS FILTERS

4.1 Introduction

4.1.1 Background

Because of the presence of extraneous, low frequency, large amplitude signals on the ACODAC tapes, the analog signals must be high pass filtered before they are digitized. These undesired signals are due to system noise in the electronics and cable strumming on the ACODAC hydrophone array. If these signals are not eliminated, their large amplitudes will seriously reduce the dynamic range of the spectral analysis of the desired signals. Since some of the noise signals were present on some tapes and not on others, it was desirable to have a high pass filter whose cutoff frequency (-3 dB) could be alternately set to 125 Hz or 220 Hz. This could allow the bandwidth of the system to be as large as the varying noise conditions permitted. The location of the high pass filters in the data analysis system is shown in Fig. 24.

4.1.2 General Description

The assembly consists of 3 separate 4-pole active Butterworth high pass filters. In keeping with the requirement noted above, the cutoff frequency (-3 dB) of each filter can be independently set to either 125 Hz or 220 Hz by means of a toggle switch on the front panel.

4.2 Theory of Operation

Shown in Fig. 25 is the general circuit configuration for an individual 2-pole filter section. Each of the high pass filters uses two of these sections in series. The transfer function for each 2-pole filter section in terms of filter parameters is

$$E_2/E_1 = S^2/(S^2+2\delta\omega_o S+\omega_o{}^2) \quad ,$$

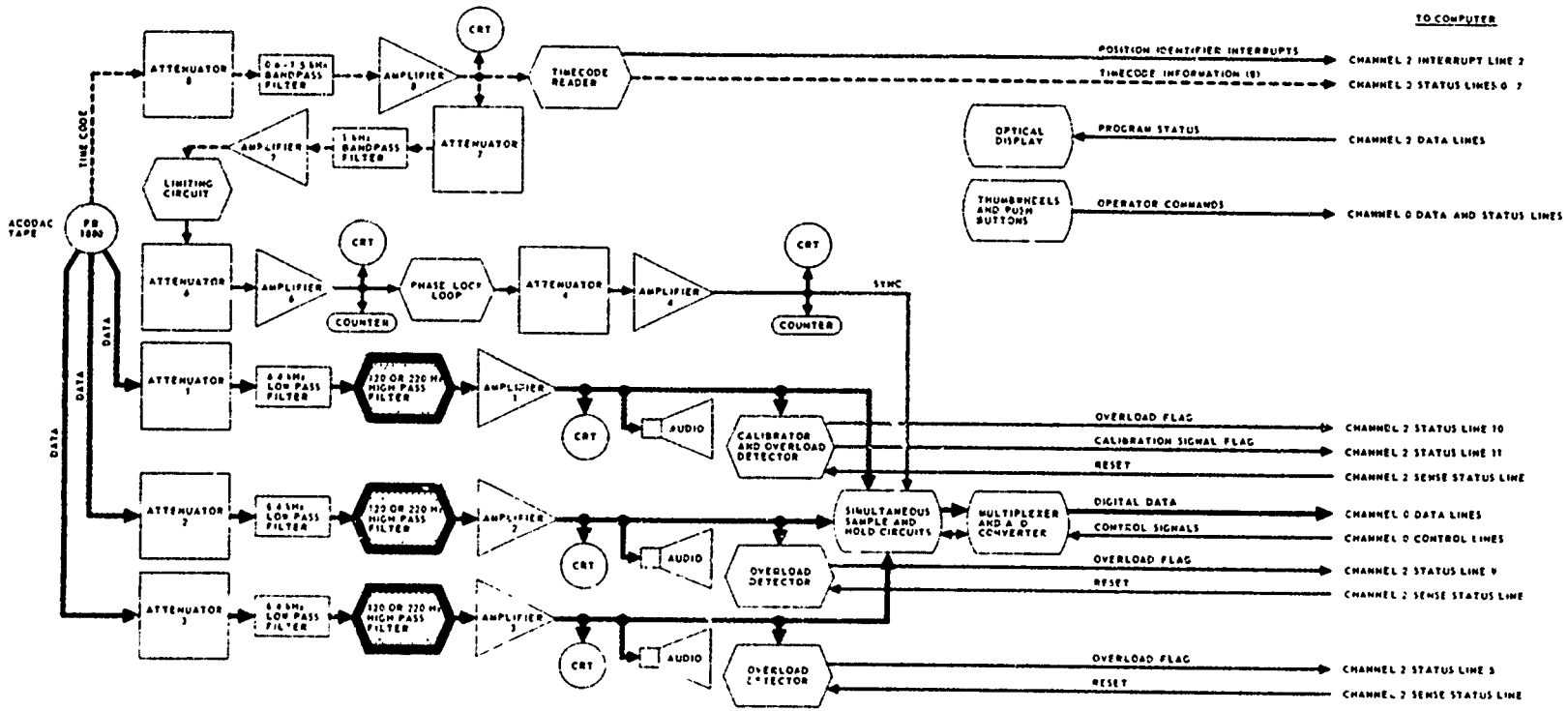


FIGURE 24
ANALOG EQUIPMENT CONFIGURATION FOR DIGITIZATION OF ACODAC DATA

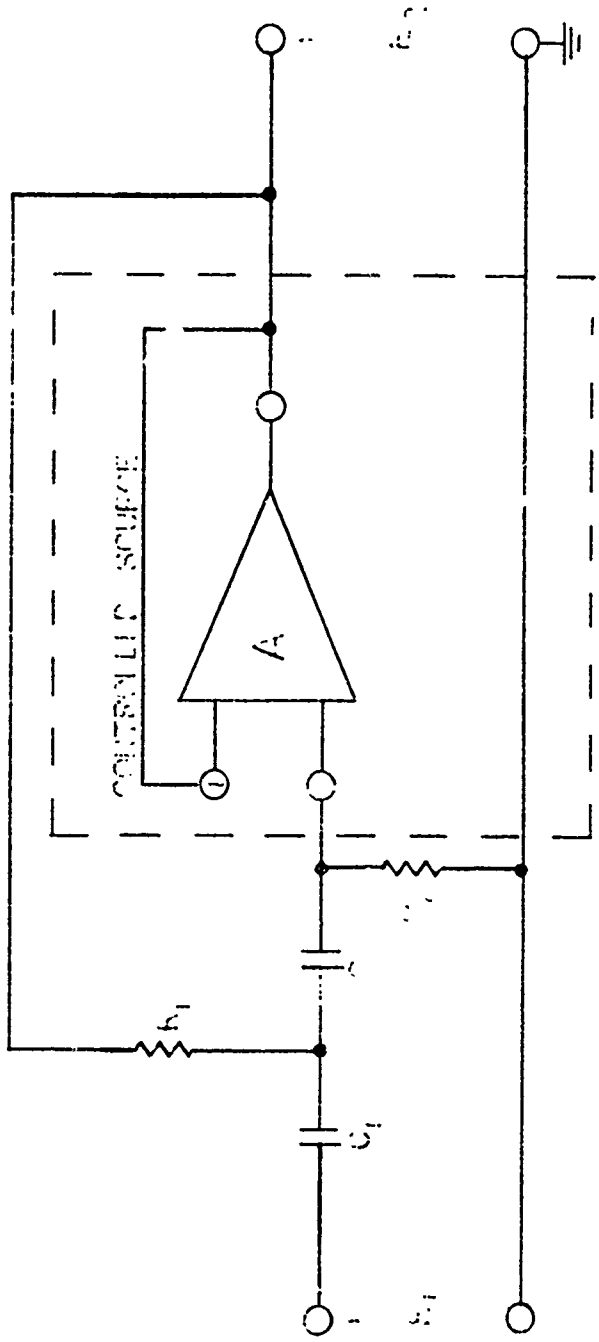


FIGURE 25
SCHEMATIC OF 2-POLE CONTROLLED SOURCE HIGH PASS FILTER SECTION

ARL - UT
AS-74-365
LLM - DR
3 - 25 - 74

where

E_2 is the output voltage for the 2-pole section,

E_1 is the input voltage,

δ is the damping factor, and

ω_o is the undamped frequency of oscillation.

In order to obtain a Butterworth response the coefficients from the fourth ordered Butterworth polynomial are used in the transfer function of the filter. The fourth ordered Butterworth polynomial in factored form is $(S^2+0.76536S+1)(S^2+1.84776S+1)$. Therefore, the overall transfer function for both 2-pole sections cascaded will be

$$\frac{E_{out}}{E_{in}} = \frac{S_4}{\left(S^2+0.76536\omega_c S+\omega_c{}^2\right)\left(S^2+1.84776\omega_c S+\omega_c{}^2\right)} \quad ,$$

where ω_c is the -3 dB point of the resulting 4-pole filter. The damping factors for the two filter sections derived from the last equation are

$$\delta_1 = 0.76536/2 \quad , \text{ and}$$

$$\delta_2 = 1.84776/2 \quad .$$

It is important that the first 2-pole section S in the series have the larger of the two damping factors (δ_2); otherwise the filter will saturate at relatively low input levels at some frequencies.

4.3 Functional Description

The design procedure is shown below for the calculation of the component values which will be used for each 2-pole section (see Fig. 25).

(1) C_1 is chosen as some convenient value. In this case

$$C_1 = 0.02\ \mu F \quad .$$

(2) The damping factors, δ_1 and δ_2, for the two filter sections are obtained from the fourth ordered Butterworth polynomial which is

$$(S^2 + 0.76536\ S + 1)(S^2 + 1.84776\ S + 1) \quad .$$

The damping factors derived from this polynomial are

$$2\delta_1 = 1.84776 \text{ and}$$

$$2\delta_2 = 0.76536 \quad .$$

(3) $C_2 = C_1$

(4) $R_1 = \frac{\delta}{2\pi C_1 f_c}$, where f_c is the desired -3 dB point.

(5) $R_2 = \frac{1}{2\delta\pi C_1 f_c}$

(6) This procedure is repeated for the design of the second section with the substitution 2δ=0.76536.

A schematic of the resulting filter is shown in Fig. 26 and frequency response curves are shown in Fig. 27. It can be seen from the design equations that only the resistor values need be changed to alter the cutoff frequencies. In order to have the capability of selecting either a 125 Hz or 220 Hz cutoff frequency (-3 dB), resistor values have been calculated for both cases, and the sets of resistors may be alternately switched into the circuit using toggle switches.

When a toggle switch is in the up position, the cutoff frequency for the corresponding filter is 125 Hz; when down, the cutoff frequency is 220 Hz. The high pass filter assembly requires dc input power of ±15 V at 75 mA. The input voltages should be limited to 20 V p-p to avoid saturating the amplifiers. The impedance presented to the input of the filters should be no larger than 10 kΩ, whereas the terminating impedance should be greater than 50 kΩ.

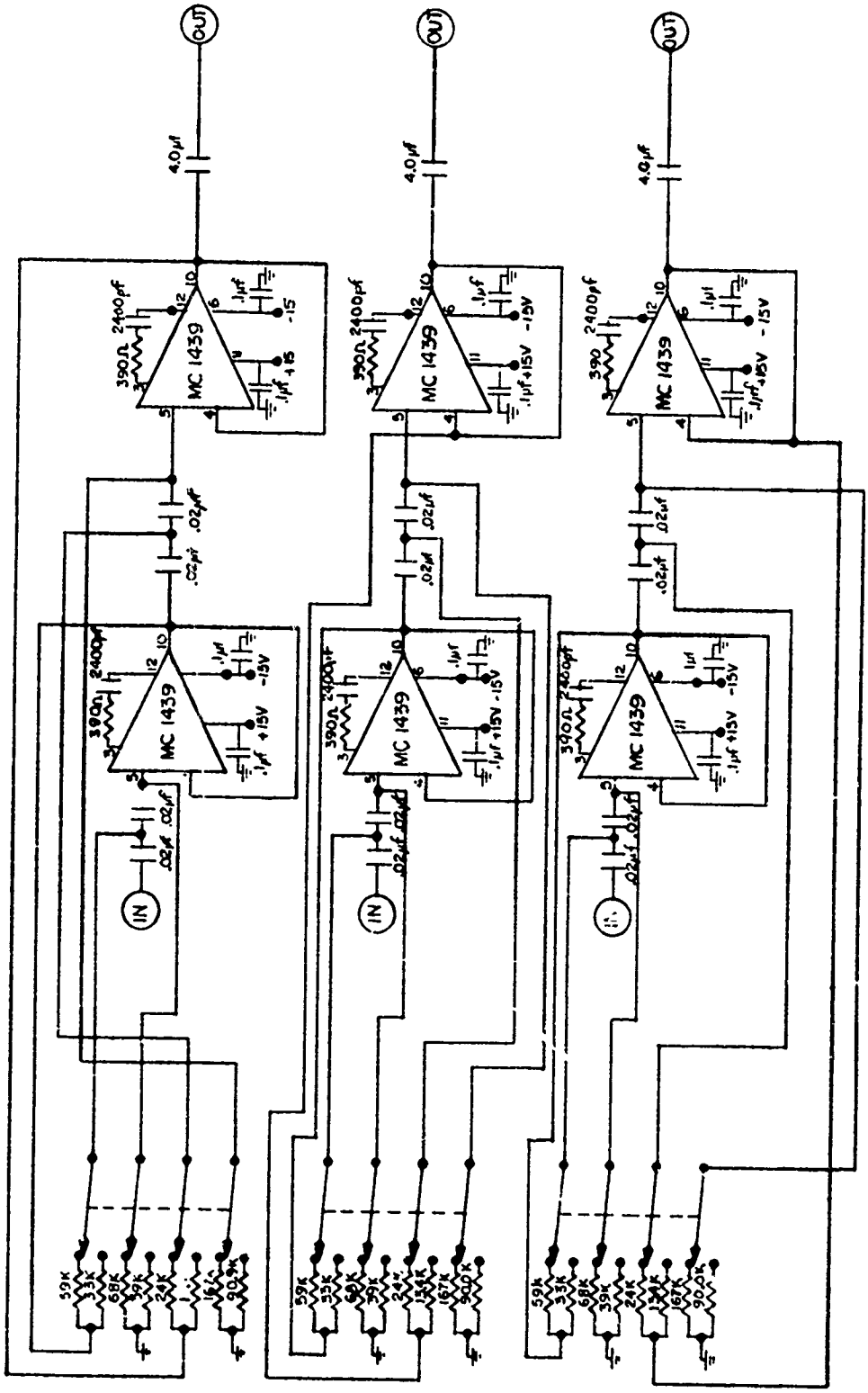
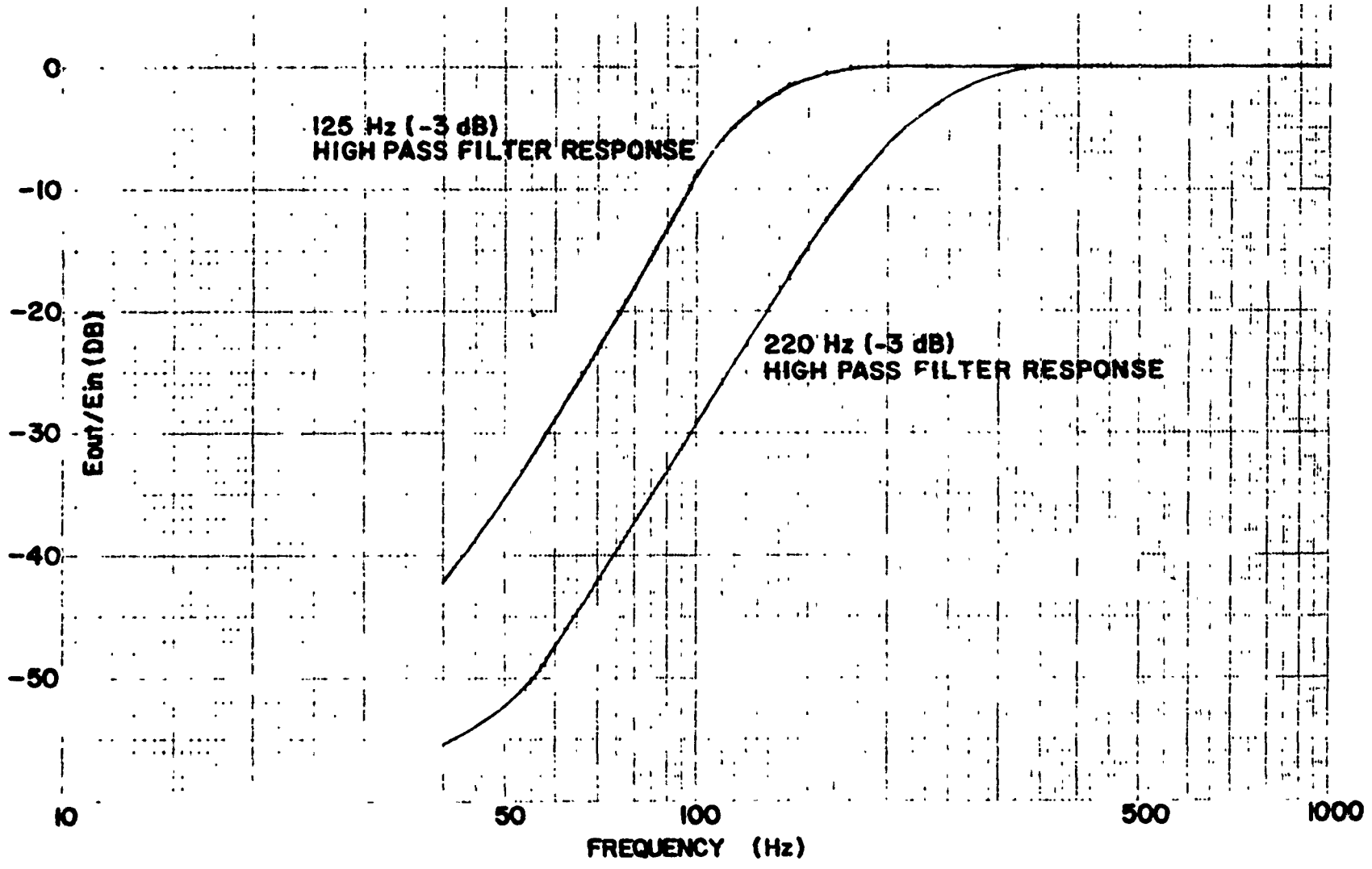


FIGURE 26
4-POLE BUTTERWORTH HIGH PASS FILTERS – CIRCUIT

ARL - UT
AS-74-392
LLM - DR
3 - 25 - 74



ARL - UT
AS:74-366
LLM - DR
3-25-74

FIGURE 27
FREQUENCY RESPONSE CURVES FOR HIGH PASS FILTERS

5.0 OVERLOAD AND CALIBRATION DETECTORS FOR ACODAC DATA ANALYSIS

5.1 Problems from Recording Extreme Amplitudes

5.1.1 Background

The acoustic data acquisition capsule (ACODAC) uses analog magnetic tape to record six channels of analog acoustic information from a hydrophone array. Should the amplitude of information fail to satisfy established maximum and minimum levels for recording purposes, the gain in the preamplifiers can be reset at any 10 dB increment from +10 dB to +40 dB. Although the information level is monitored continuously, the desired gain change is delayed until the following minute interval from the time code reader. This sequence ensures a minute of analog information at a fixed preamplifier gain setting that is coded with the time code information. For reduction purposes the time code channel can be read to determine the gain setting of any information channel during the previous minute.

5.1.2 Overload and Calibration Tone Generation

Abrupt changes in the acoustic level, such as from impulses, may exceed the recording capabilities of the system before sufficient gain correction can be made. Such data is not reliable and should not be used. The ACODAC (Ref. 2) electronics senses the excessive levels and denotes it as overload information by interrupting the data channel and inserting two simultaneous tones of 75 Hz and 200 Hz. The period of the overload indication is the greater of 9.75 carrier frequency cycles or the duration of the overload itself.

A calibration signal of two simultaneous tones of 50 Hz and 200 Hz is applied to all of the data channels once every six hours. This calibration sequence provides an indication of recording conditions.

5.1.3 Overload and Calibration Tone Detection

Overload detectors were designed to identify the overload tones and indicate them to the computer that is digitizing the analog information. A visual indicator was also provided for operator editing of the tape. Since the analog to digital converter has the capability of digitizing three analog channels simultaneously, three identical overload detectors were fabricated.

One of the detector channels was configured to identify the presence of a calibration tone. The calibration tone is recognized by its long duration of 200 Hz information. The location of the overload and calibration tone detectors in the data analysis system is shown in Fig. 28.

5.2 Theory of Operation

Each data channel is monitored for signals produced by the ACODAC system. Upon detection of the two simultaneous overload tones or the calibration tone, an electronic latch is tripped to provide a signal for the computer and to illuminate an indicator on the front panel. The computer interrogates the system once every time code minute. If the tripped latch indication is present during the interrogation, the event is recorded, and the computer automatically resets the latch.

A manual reset is provided on the front panel enabling an operator to monitor a tape and reset the event latches manually.

5.3 Functional Description

5.3.1 Overload Detector Circuit

The overload detector circuit contains two tone decoders (NE 567) for each data channel (see Fig. 29). The free running frequency of the tone decoder is set by the resistors and capacitors connected to pin 5 and pin 6 on the decoder. The free running frequencies should be set

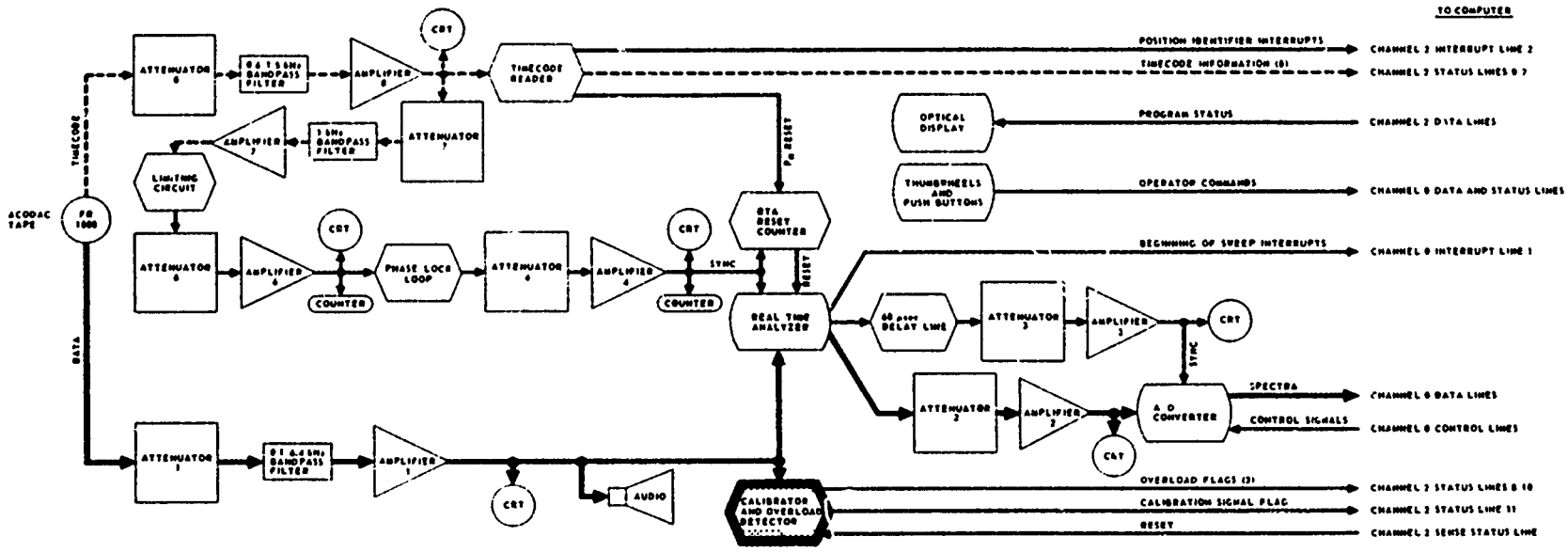


FIGURE 28
ANALOG EQUIPMENT CONFIGURATION FOR ANALYSIS OF ACODAC DATA VIA RTA

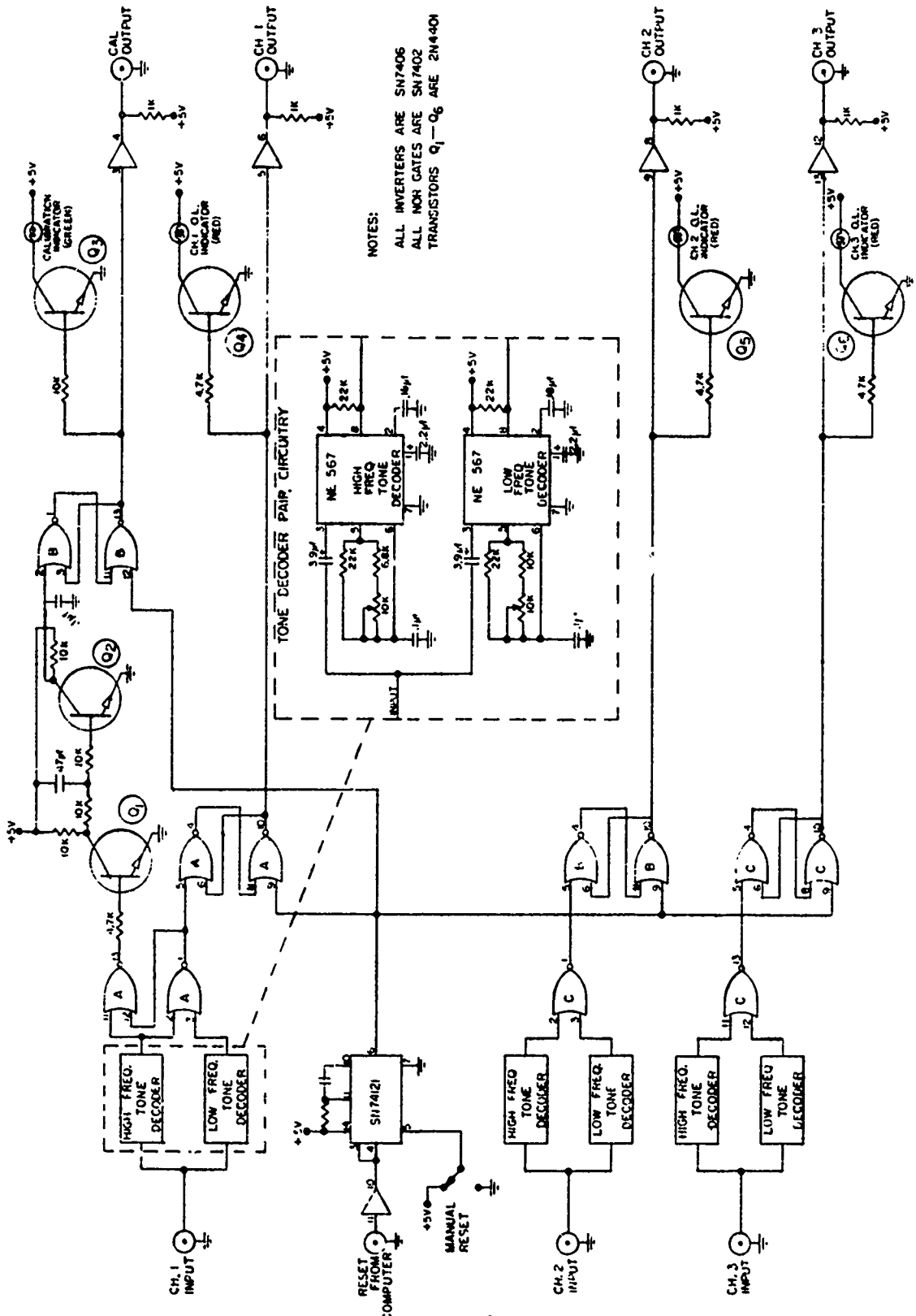


FIGURE 29
OVERLOAD DETECTOR CIRCUIT

ARL - UT
AS-74-394
LLM - DR
3 - 25 - 74

equal to the 75 Hz and the 200 Hz overload tones in the playback mode. Hence, if the data were to be played back at 20 times the recorded speed, the free running frequency of the low frequency decoder would be set at 1500 Hz, and the frequency of the high frequency decoder at 4000 Hz. The tone decoders are designed to detect 15 successive cycles of incoming information within a bandwidth that is 10% of the center frequency. A 2-input NOR gate is the monitor of the outputs of the decoders; it senses when simultaneous overload tones have been detected. When simultaneous tones are received, a latch consisting of two NOR gates is tripped. The output of the latch drives a transistor, which turns on a red front panel lamp and an inverter, which in turn acts as a buffer to the computer.

5.3.2 Reset

A reset may be accomplished either mechanically by the computer or manually by an operator. The computer reset signal passes through an inverter to a SN74121 monostable that generates a pulse to all of the latches. An operator may reset the system by pressing a momentary pushbutton on the front panel that triggers the reset monostable.

5.3.3 Calibration

The calibration tone indicator identifies the presence of a persisting 200 Hz frequency. Since the calibration tone is presented to all data channels simultaneously, only one channel needs to be monitored. Any of the high frequency overload tone detectors will determine the presence of the 200 Hz frequency; therefore, the channel 1 decoder is monitored for convenience. A NOR gate is used to determine the presence of the 200 Hz tone but not the 75 Hz and 200 Hz overload tones. The output of this NOR gate is buffered and integrated to ensure the presence of a calibration tone and not random 200 Hz information. Upon confirmation of a calibration tone, a two NOR gate latch is tripped. The latch drives an inverted and buffered output on the computer and a green indicator lamp appears on the front panel.

6.0 PULSE DELAY CIRCUIT

6.1 Introduction

The signal from the RTA to the analog to digital converter for the computer consists of commutated analog information with undesirable ringing at the commutation transitions. The sampling command for the A/D is generated simultaneously with the commutation command. Thus when the A/D samples during the ringing, it obtains poor quality information. Therefore, a delay circuit has been fabricated to command the A/D to sample the commutated information at a time when the ringing ceases. The location of the delay circuit in the data analysis system is shown in Fig. 30.

6.2 Theory of Operation

A circuit has been designed to trigger on the commutator transition command and to provide a 6 μsec output pulse after a 70 μsec delay time.

6.3 Functional Description

The pulses marking the commutation transition are fed into an inverter that in turn triggers a SN74121 monostable shown in Fig. 31. The monostable time period of approximately 70 μsec is established by the external capacitor and a resistor that is internal to the integrated circuit. This monostable establishes the delay necessary for the ringing of the analog transition to cease.

The output of the first monostable triggers a second monostable that generates a short pulse (6 μsec) that is buffered by an inverter and transmitted to the computer.

The power supply requirements of this circuit are 50 mA at +5 Vdc. The input and output are TTL compatible.

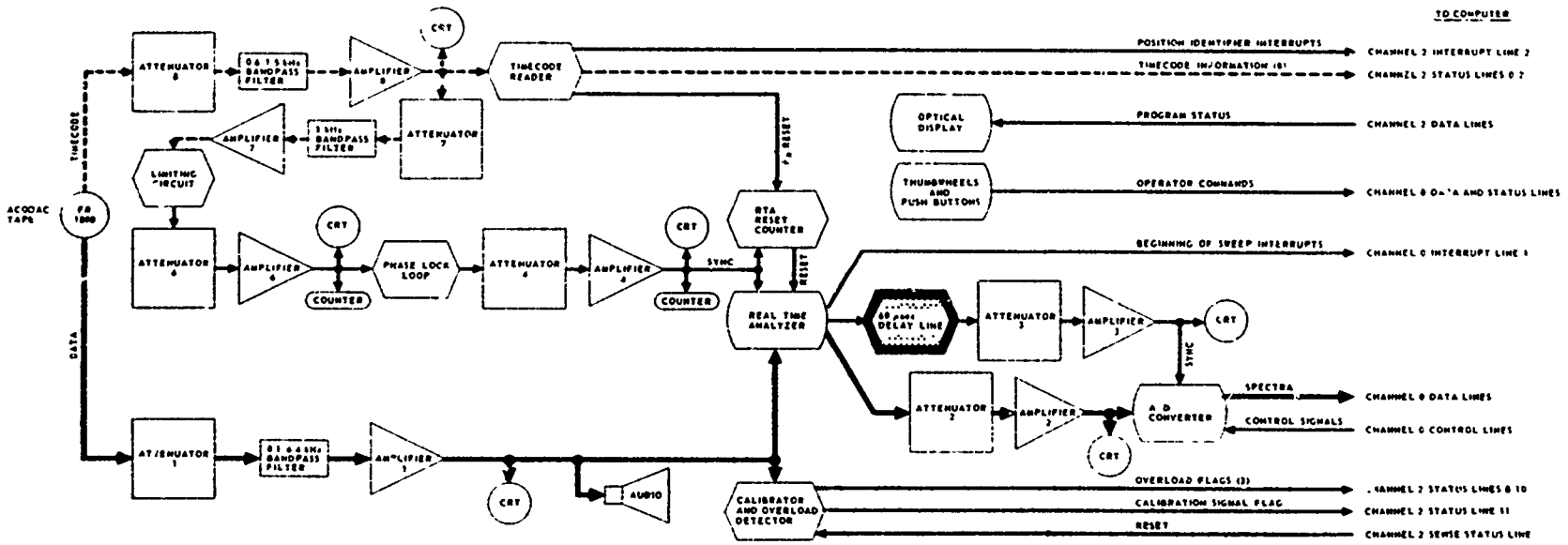


FIGURE 30
ANALOG EQUIPMENT CONFIGURATION FOR ANALYSIS OF ACODAC DATA VIA RTA

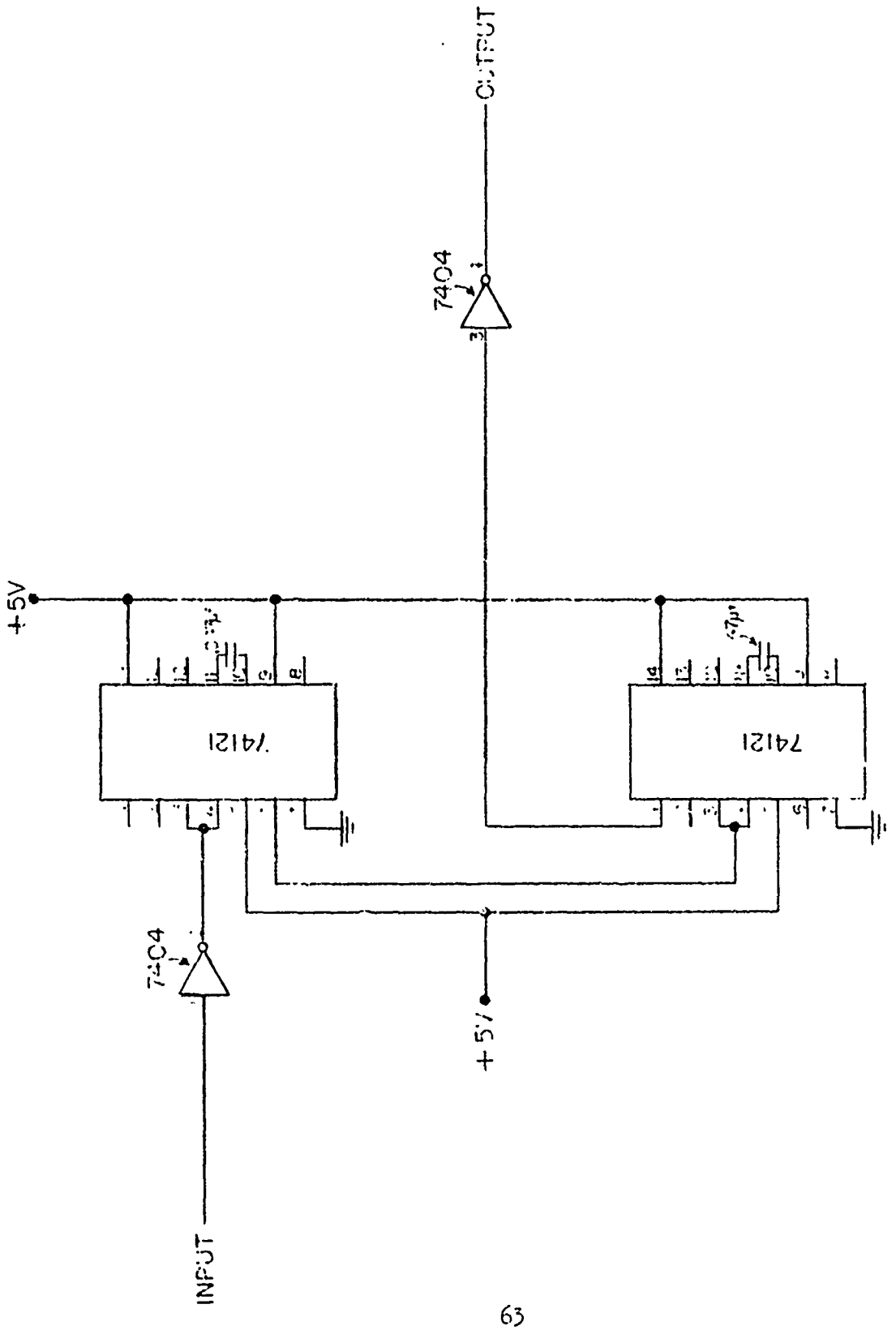


FIGURE 31
PULSE DELAY CIRCUIT

ARL - UT
AS-74-367
LLM - DR
3 - 25 - 74

7.0 REAL TIME ANALYZER (RTA) RESET COUNTER

7.1 Introduction

A 1/3 octave band analysis of the ACODAC data is performed via a real time ANALYZER. A pulse counter circuit is necessary to determine when the analyzer memory is filled with new information. When the 1500 samples required to fill the memory are received, a pulse is sent to command the analyzer to process the new information. The analog information is subject to gain changes at the minute marks of the time code reader; thus the counter is reset by the time code minute mark to prevent the loading of the memory with information from two adjacent minutes with different gain settings. The location of the RTA reset counter in the ANALYSIS SYSTEM is shown in Fig. 32.

7.2 Theory of Operation

A counter circuit is preset to 1500 counts which represents the number of samples required to fill the RTA memory. Each sample command for the analyzer memory also shifts the downcounter. When the counter has been shifted down 1500 times, a pulse is produced that presets the counter to 1500 and the counter commands the RTA to process the new information in the memory.

A minute mark from the time code reader will reset the counter without producing an output pulse. Thus the memory continues to take new information until 1500 samples after the minute mark have been loaded. This prevents the RTA memory from containing information from more than one ACODAC minute interval.

7.3 Functional Description

The sample clock is inverted by a NAND gate which drives a SN74193 up-down binary counter as shown in Fig. 33. This is the first of three counters programmed to count down from 1500. When the countdown is completed, a pulse is generated at pin 13 of the last counter. The pulse triggers a SN74121 monostable whose output goes

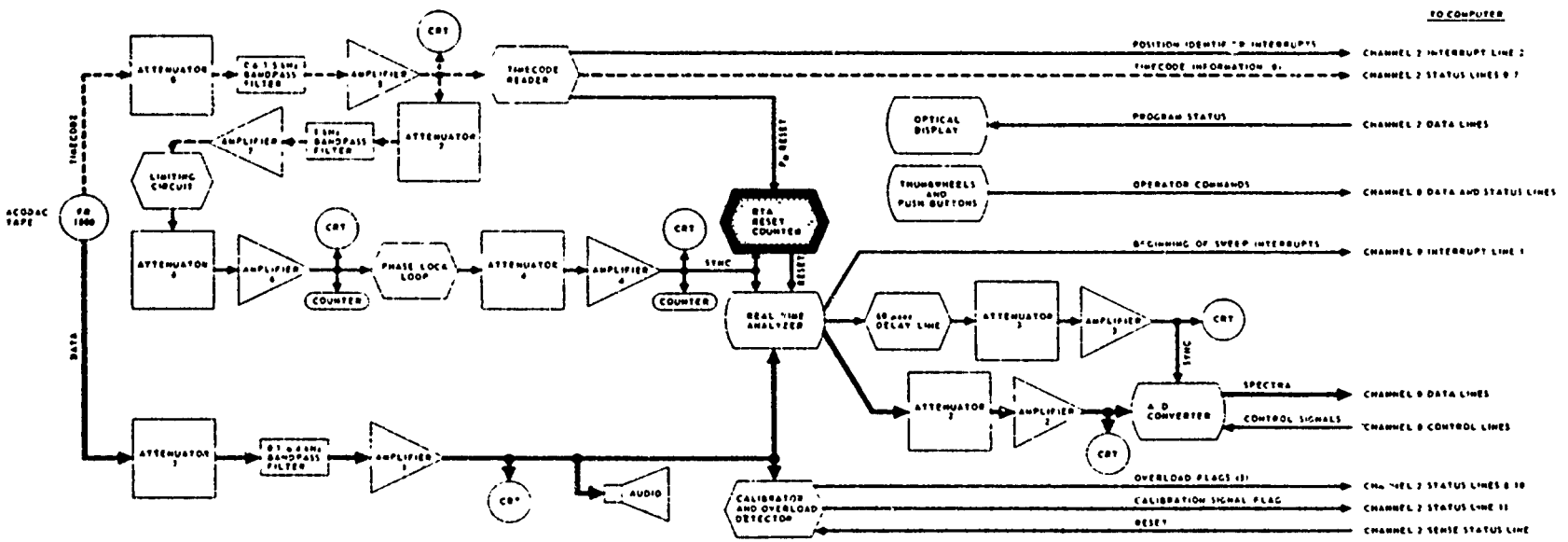


FIGURE 32
ANALOG EQUIPMENT CONFIGURATION FOR ANALYSIS OF ACODAC DATA VIA RTA

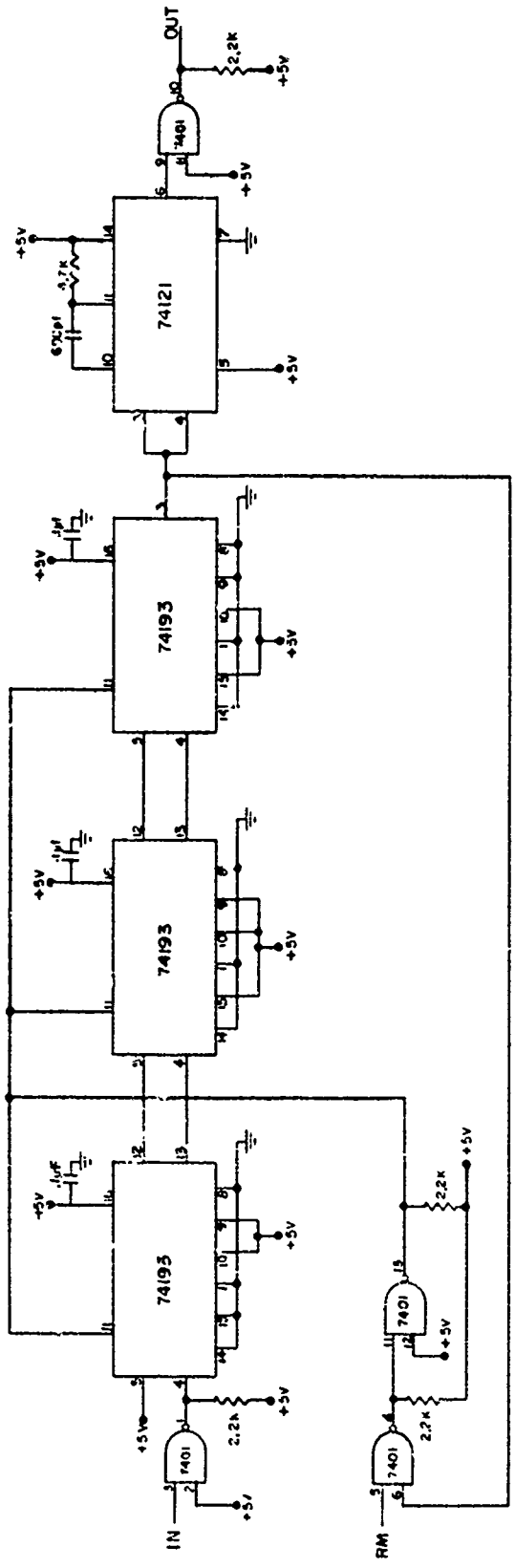


FIGURE 33
PULSE COUNTER CIRCUIT

ARL - UT
AS-74-390
LLM - DR
3 - 25 - 74

to the RTA via a NAND gate buffer. The output of the counter also goes to a NAND gate with the minute mark reset; this gate detects either the minute mark or the completed count and presets the counters through a NAND inverter. Since the minute mark reset does not go to the monostable, no output pulse is generated during this preset command.

The counters can be reprogrammed for different sampling criteria by selecting the proper preset loads in the inputs A, B, C, and D to the SN74193's.

The power requirements for this circuit are 160 mA at +5 Vdc. The inputs and outputs are TTL compatible.

8.0 SUMMARY

This report provides a description of special hardware that was fabricated to permit analysis of ACODAC data. Discussion of the hardware provides an explanation of the problems and the solutions. Flow charts are presented to show the relationship of the devices with other system functions. A description of the hardware with circuit diagrams is provided to assist in operation and maintenance.

APPENDIX A

MANUFACTURER'S DATA FOR PROCURED EQUIPMENT

POWERTEC
AN AIRTRONICS SUBSIDIARY
9168 DESOTO AVENUE
CHATSWORTH CALIFORNIA 91311
(213) 882-0004 TWX 910-494-2092

APPLICATION DATA
OEM SERIES
TRIPLE OUTPUT
DC POWER SUPPLY

MODEL 2R-70T

SPECIFICATIONS

AC INPUT: 105 to 125VAC, 47 to 63Hz (Derate Unit 15% for 50Hz operation). For wider range or 400Hz operation, consult the factory.

DC OUTPUT RATINGS:

OUTPUT	OUTPUT (1) VOLTAGE	MAX. OUTPUT CURRENT	XFMR (2) TERMINALS
A1	12 V 15 V	1.5 A 1.3 A	12 V 15 V
A2	12 V 15 V	1.5 A 1.3 A	12 V 15 V
A3	5 V	6 A	N.A

(1). Adj. range ± 5%

(2). See outline drawing

REGULATION: Line ± 0.25%, Load ± 0.25%

OUTPUT RIPPLE: 1 mV RMS, 3 mV p to p

TRANSIENT RESPONSE: 50μ sec. for 50% load change.

OVERLOAD PROTECTION: Unit is protected from overload & short circuit using the current foldback method.

INPUT FUSING: 2A input fusing is recommended for power supply protection.

COOLING: Convection cooled. Moving air is desirable when mounted in a contined area. Do not restrict airflow through baseplate for maximum ratings.

OPERATING TEMPERATURE: See table below

PERCENT OF FULL RATED LOAD AT AMBIENT TEMPERATURE			
+40°C	+50°C	+60°C	+71°C
100%	75%	50%	35%

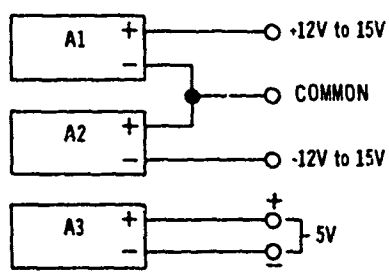
CONSTRUCTION: All aluminum, anodized

WEIGHT: 8.2 Pounds

CONNECTIONS FOR VARIOUS VOLTAGES

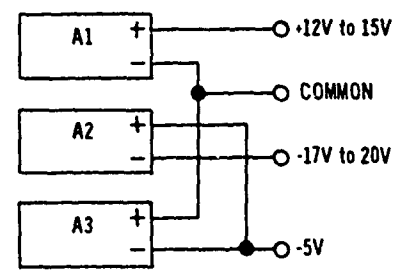
BASIC CONFIGURATION

OUTPUTS
A1) +12V to 15V
A2) -12V to 15V
A3) 5V floating



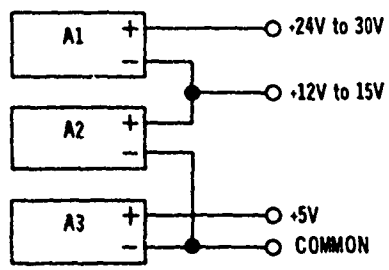
OPTIONAL

OUTPUTS
1) -5V
2) +12V to 15V
3) -17V to 20V



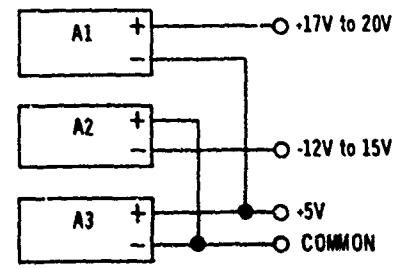
OPTIONAL

OUTPUTS
1) +24V to 30V
2) +12V to 15V
3) +5V



OPTIONAL

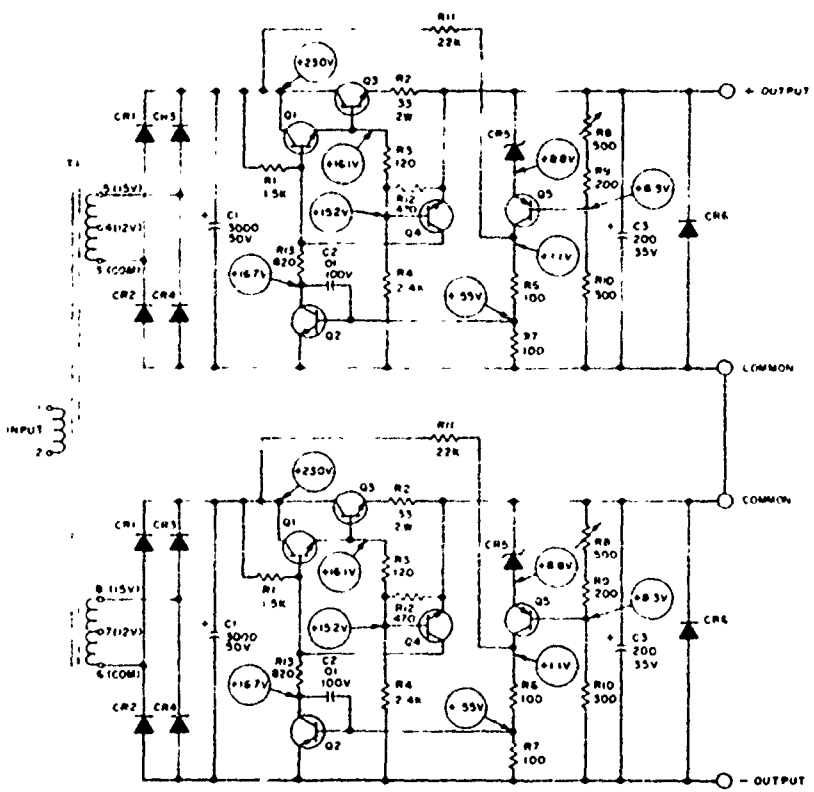
OUTPUTS
1) +17V to 20V
2) -12V to 15V
3) +5V



Preceding page blank

15092-002

REF DES (A1 & A2)	POWERTEC P/N	COM'L EQUIV	DESCRIPTION
C1	32-13007-012	STM39C350AA33	5000 MFD, 50V
C2	31-13005-003	NPC-EL	.01MFD 100V
C3	32-13008-004	IEC-PCZ200PR35	200MFD, 35V
CR1-4	11-13010-001	SEMTECH-35IE	—
CR5	12-13013-008	1N4755A	—
CR6	11-13009-001	SEMTECH-51-2	—
R1	20-13004-077	RC20GF152J	1.5k, 1/2W, 5%
R2	24-13016-007	IRC 8WH	33Ω, 2W, 10%
R3	20-13004-051	RC20GF121J	120Ω 1/2W 5%
R4	20-13004-082	RC20GF242J	2.4k 1/2W 5%
R6,7	20-13004-049	RC20GF101J	100Ω, 1/2W, 5%
R8	25-13016-001	CTS-111	500Ω
R9	20-13004-058	RC20GF201J	200Ω, 1/2W 5%
R10	20-13004-060	RC20GF301J	300Ω, 1/2W 5%
R11	20-13004-105	RC20GF223J	22k 1/2W, 5%
R12	20-13004-045	RC20GF471J	470Ω 1/2W, 5%
R13	20-13004-071	RC20GF821J	820Ω, 1/2W 5%
Q1,2,4	10-13018-001	2N2219A	—
Q3	10-13002-003	2N3055	—
Q5	10-13021-001	2N2905A	—
A1,2	55-12795-001	—	PCB 2R15V-24V
T1	40-13965-001	—	—



1. OPTION ON R8 25-13016-005 (CTS-IRC-111, 500Ω)
2. TEST VOLTAGES ARE TAKEN AT FULL RATED LOAD CURRENT, 115VAC INPUT. OUTPUT VOLTAGE ADJUSTED TO 15.0 VOLTS
3. TEST VOLTAGES ARE REFERENCED TO COMMON OUTPUT FOR + SUPPLY (A1) TEST VOLTAGES ARE REFERENCED TO NEGATIVE OUTPUT FOR - SUPPLY (A2)

A	SEE ECN 06135	7-9-76

13984

POWERTEC DIVISION

OEM SERIES
15D-13A

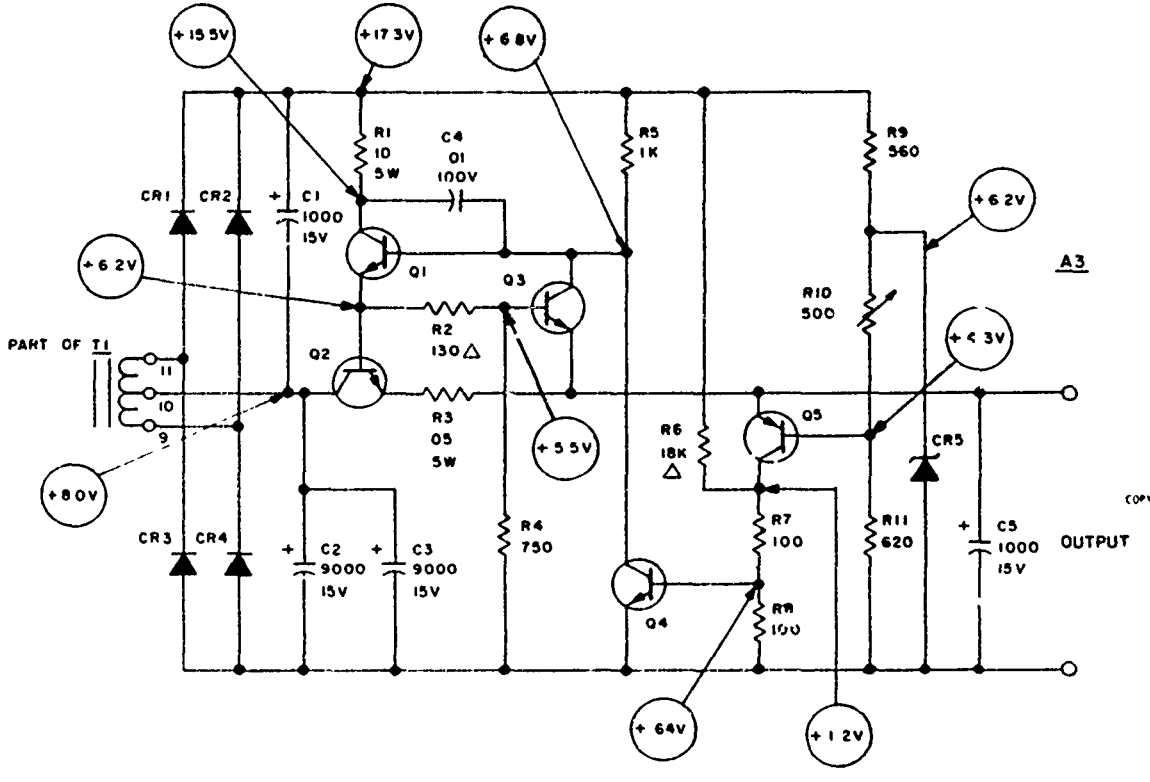
SIZE	CAGE NO.	DRAWING NO.	REV
D	24429	13984	—

SHEET 1 OF 1

74

SYM	POWERTEC P/N	COM'L EQUIV	DESC
C1,5	32-13006-003	CZ1000PN15	1000 MFD, 15V
C2,3	32-13008-001	STM23C15AA93	9,000 MFD, 15V
C4	31-13005-003	NPC-EL	01 MFD, 100V
CR1,2	11-13009-001	SI-2	—
CR3,4	11-13012-001	IN1200	—
CR5	12-13013-008	IN4735A	—
R1	22-13049-002	PW5-10Ω,10%	10Ω, 5W, 10%
R7,8	20-13004-049	RC20GF101J	100Ω, 1/2W, 5%
R3	22-13280-001	KS500	.05Ω, 5W, 5%
R4	20-13004-070	RC20GF751J	750Ω, 1/2W, 5%
R5	20-13004-073	RC20GF102J	1K, 1/2W, 5%
R6 △	20-13004-103	RC20GF183J	18K, 1/2W, 5%
R9	20-13004-067	RC20GF561J	560Ω, 1/2W, 5%
R10	23-13016-001	CTS-111	500Ω
R11	20-13004-068	RC20GF621J	620Ω, 1/2W, 5%
Q1,2	10-13002-003	2N3055	—
Q3,4	10-13018-001	2N2219A	—
Q5	10-13021-001	2N2905A	—
P.C.B	55-12891-001	—	—
T1	40-13967-001	—	—
R2 △	20-13004-052	RC20GF13[illegible]J	130Ω, 1/2W, 5%

A	SEE ECN 011057	10-6-71	
B	SEE ECN 011128	11-10-71	



COPY 15033

3 TEST VOLTAGES ARE TAKEN AT FULL RATED LOAD CURRENT, 115 VAC INPUT OUTPUT VOLTAGE ADJUSTED TO 5.0 VOLTS

2 ALL VOLTAGES ARE REFERENCED TO NEGATIVE OUTPUT

1 Δ INDICATES NOMINAL VALUE

NOTE UNLESS OTHERWISE SPECIFIED

POWERTEC DIVISION
A RITRON'S INCORPORATED
9168 DESOTO AVE CHATSWORTH CALIF 91311

TITLE
OEM SERIES
5V — 6A

C LEEDY 7/7/71

SIZE	CAGE CODE	DRAWING NO.	REV
C	24429	15033	--

SHEET 1 OF 1

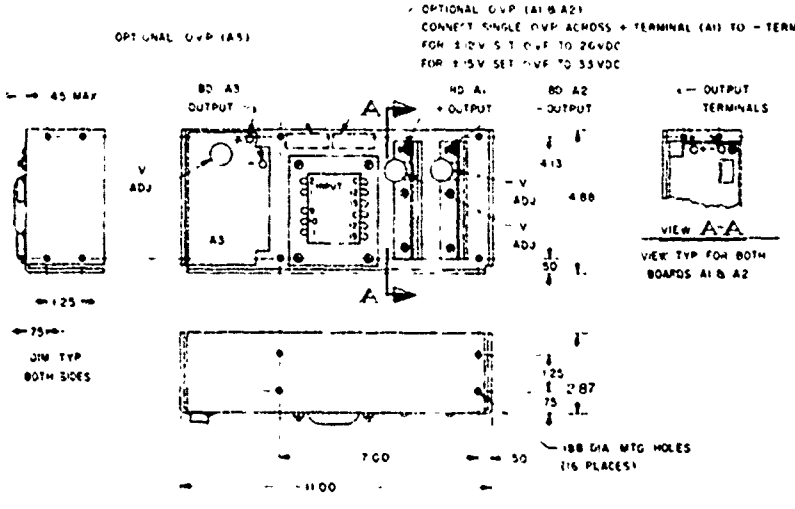
TROUBLESHOOTING GUIDE

Check voltage test points shown on schematic 13984 for ease of failure determination
(Applies to A1 or A2)

FAILURE INDICATION:	CHECK:
1. High input current, blows fuses.	C1 shorted
	CR1-CR4 shorted
2. Poor regulation, high output ripple.	C1 open
	CR1-CR4 open
	Q3 shorted
	possible output overload
3. High output voltage and ripple, poor regulation.	Q1, Q3 shorted
	Q2 open
4. Low output voltage with excessive ripple.	C3 leaky
	CR1-CR4 open
	Q4 shorted
	possible output overload
5. Excessive unit heating.	improper input frequency or voltage
	possible output overload
	inadequate ventilation
	improper transformer tap connection (See schematic)

Check voltage test points shown on schematic 15033 for ease of failure determination.
(Applies to A3)

FAILURE INDICATION:	CHECK:
1. High input current, blows fuses	C1 C3 shorted
	CR1-CR4 shorted
2. Poor regulation, high output ripple.	C1-C3 open
	CR1-CR4 open
	Q2 shorted
	possible output overload
3. High output voltage and ripple, poor regulation.	Q1, Q2 shorted
	Q4 open
4. Low output voltage with excessive ripple.	C5 leaky
	CR1-CR4 open
	Q3 shorted
	possible output overload
5. Excessive unit heating.	improper input frequency or voltage
	possible output overload
	inadquate ventilation
	improper transformer tap connection (See schematic)



POWERTEC AIRTRONICS INC
9168 DESOTO AVENUE
CHATSWORTH CALIFORNIA 91311
(213) 882 0004 TWX 910 494 2092

APPLICATION DATA
O.E.M. SERIES

OVERVOLTAGE PROTECTION

SPECIFICATIONS:

VOLTAGE ADJUSTMENT RANGE: 6.5 – 33.0 VDC

MAXIMUM CURRENT: 12 AMPS Intermittent
8 AMPS Continuous

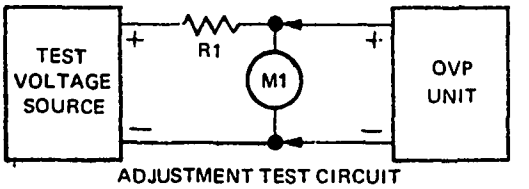
ADJUSTMENT PROCEDURE:

The OVP unit should be adjusted to trigger at the suggested voltage as indicated in Figure 1

POWER SUPPLY OUTPUT VOLTAGE	SUGGESTED OVP TRIGGER VOLTAGE	R1	MI
5 VDC	6.5 VDC	68Ω 1 w	ACCURATE TO WITHIN 1% OF SUGGESTED OVP TRIGGER VOLTAGE
6	7.8	82Ω 1 w	
12	14	150Ω 2 w	
15	17	200Ω 2 w	
18	21	250Ω 5 w	
20	24	250Ω 5 w	
24	28	300Ω 5 w	

FIGURE 1

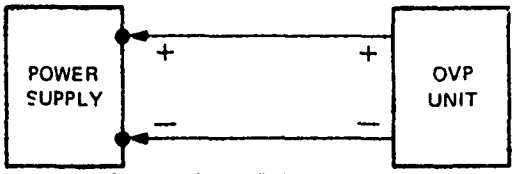
1. Connect test circuit as shown in Figure 2.
2. Energize and adjust the test voltage source to the suggested OVP trigger voltage.
3. Slowly rotate the adjustment potentiometer (R5) from its maximum clockwise position until the OVP unit triggers as indicated by a zero reading on M1. Leave R5 in this position.
4. The unit is now properly adjusted and ready for installation.



ADJUSTMENT TEST CIRCUIT
FIGURE 2

INSTALLATION PROCEDURE:

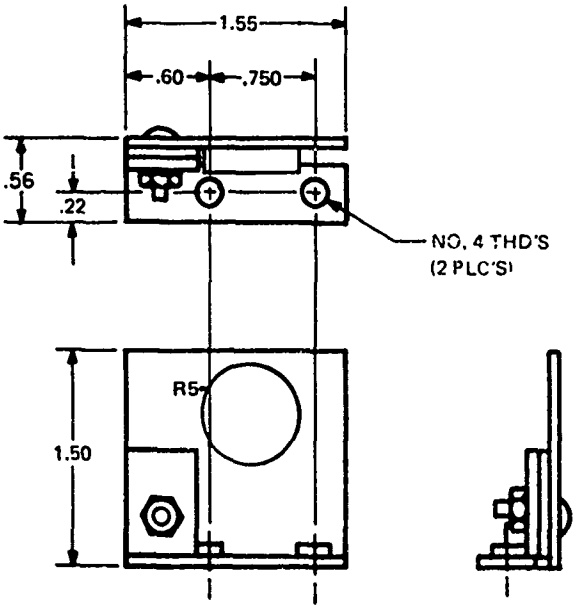
Connect the OVP unit in parallel with the power supply as indicated in Figure 3



OVP INSTALLATION DIAGRAM
FIGURE 3

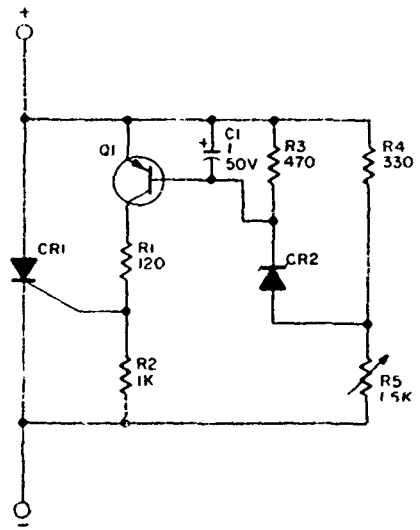
TROUBLESHOOTING GUIDE

FAILURE INDICATION	CHECK
1. UNIT REMAINS SHORTED AFTER AN OVERVOLTAGE CONDITION IS CORRECTED.	SCR1 SHORTED Q1 SHORTED CR2 SHORTED
2. UNIT REMAINS SHORTED AFTER ALL VOLTAGE IS REMOVED.	SCR1 SHORTED
3. UNIT TRIGGERS ERRATICALLY ON NOISE SPIKES OR TRANSIENTS	C1 OPEN
4. UNIT FAILS TO TRIGGER.	SCR1 OPEN Q1 OPEN CR2 OPEN R5 OPEN C1 SHORTED



15471-002

SYM	POWERTEC P/N	[illegible]	DESC
C1	32-13006-001	PCZIPA5[illegible]	1MFD 50V
CR1	13-13015-001	2N4441	—
CR2	12-13025-007	1N752A	—
R1	20-13004-051	RC20GF[illegible]	120Ω 1/2W,[illegible]
R2	20-13004-073	RC20GF10[illegible]	1K,1/2W,5%
R3	20-13004-065	RC20GF47[illegible]	470Ω,1/2W,5%
R4	20-13004-061	RC20GF331J	330Ω [illegible]W,5%
R5	23-13016-002	CTS-111	1.5K
Q1	10-11020-001	2N2907A	—
BRACKET	50-12836	—	—
PCB	55-12789	—	—



13207

NOTE UNLESS OTHERWISE SPECIFIED

POWERTEC DIVISION

OEM OVP
ADJ. 6.5 TO 30VDC
12 AMPS MAX.

C	24429	13207

M PIERCE 10 26-70

SHT 1 OF 1

LIST OF REFERENCES

1. Scott C. Daubin, Henri O. Beteaux, David S. Bitterman, Jr., Paul R. Boutin, Peter E. Kallic, "The ACODAC System," Woods Hole Oceanographic Institution Technical Report No. 72-87, Woods Hole Oceanographic Institution, Woods Hole, Massachusetts (November 1972).

2. ACODAC Operations and Maintenance Manual, Texas Instruments Incorporated Services Group (March 1973).

3. Phase Locked Loop Data Book, 2nd edition, Motorola Incorporated (August 1973).

DEPARTMENT OF THE NAVY
OFFICE OF NAVAL RESEARCH
875 NORTH RANDOLPH STREET
SUITE 1425
ARLINGTON VA 22203-1995

IN REPLY REFER TO:

5510/1
Ser 321OA/011/06
31 Jan 06

MEMORANDUM FOR DISTRIBUTION LIST

Subj: DECLASSIFICATION OF LONG RANGE ACOUSTIC PROPAGATION PROJECT (LRAPP) DOCUMENTS

Ref: (a) SECNAVINST 5510.36

Encl: (1) List of DECLASSIFIED LRAPP Documents

1. In accordance with reference (a), a declassification review has been conducted on a number of classified LRAPP documents.

2. The LRAPP documents listed in enclosure (1) have been downgraded to UNCLASSIFIED and have been approved for public release. These documents should be remarked as follows:

   Classification changed to UNCLASSIFIED by authority of the Chief of Naval Operations (N772) letter N772A/6U875630, 20 January 2006.

   DISTRIBUTION STATEMENT A: Approved for Public Release; Distribution is unlimited.

3. Questions may be directed to the undersigned on (703) 696-4619, DSN 426-4619.

BRIAN LINK
By direction

Subj: DECLASSIFICATION OF LONG RANGE ACOUSTIC PROPAGATION PROJECT (LRAPP) DOCUMENTS

DISTRIBUTION LIST:

NAVOCEANO (Code N121LC – Jaime Ratliff)
NRL Washington (Code 5596.3 – Mary Templeman)
PEO LMW Det San Diego (PMS 181)
DTIC-OCQ (Larry Downing)
ARL, U of Texas
Blue Sea Corporation (Dr.Roy Gaul)
ONR 32B (CAPT Paul Stewart)
ONR 321OA (Dr. Ellen Livingston)
APL, U of Washington
APL, Johns Hopkins University
ARL, Penn State University
MPL of Scripps Institution of Oceanography
WHOI
NAVSEA
NAVAIR
NUWC
SAIC

Declassified LRAPP Documents

Report Number	Personal Author	Title	Publication Source (Originator)	Pub. Date	Current Availability	Class.
WHOI73-59	Tollios, C. D.	THE ACODAC DATA PROCESSING SYSTEM	Woods Hole Oceanographic Institution	730901	AD0773114; ND	U
Unavailable	Russell, J. J.	DOCUMENTATION FOR COMPUTER PROGRAM SUMMARY: A COMPUTER PROGRAM TO SUMMARIZE SOUND SPEED PROFILE DATA	Naval Undersea Center	731001	AD0918907	U
MC001Vol2	Unavailable	CHURCH ANCHOR DATA ANALYSIS PLAN VOL 2 (U)	Maury Center for Ocean Science	731001	ND	U
73-9M7-VERAY-R2	Jones, C. H.	LRAPP VERTICAL ARRAY- PHASE III	Westinghouse Research Laboratories	731105	ADA001130; ND	U
55	Weinstein, M. S., et al.	SUS QUALITY ASSESSMENT	Underwater Systems, Inc.	731201	AD 785875 ND	U
ARL-TM-73-42	Mitchell, S. K., et al.	QUALITY CONTROL ANALYSIS OF SUS PROCESSING FROM ACODAC DATA	University of Texas, Applied Research Laboratories	731220	ADB000243 ND	U
Unavailable	Daubin, S. C.	CHURCH GABBRO TECHNICAL NOTE: CONTINUOUS CURRENT PROFILES	University of Miami, Rosenstiel School of Marine and Atmospheric Science	740101	AD0775333	U
Unavailable	Bitterman, D. S.	ACODAC AMBIENT NOISE SYSTEM	Woods Hole Oceanographic Institution	740101	ADA009440	U
ONR MC-002 VOL. 2; XONICS 885	Unavailable	LONG RANGE ACOUSTIC PROPAGATION PROJECT (LRAPP). SQUARE DEAL DATA ANALYSIS PLAN (U) VOLUME 2 - ANNEXES	Maury Center for Ocean Science; Xonics, Inc.	740101	ND	U
ARL-TM-74-12	Groman, R. O., et al.	SPECIAL HARDWARE FOR ARL ANALYSIS OF ACODAC DATA	University of Texas, Applied Research Laboratories	740314	ADA000295; ND	U
Unavailable	Unavailable	ASEPS NEAR FIELD TRANSMISSION LOSS MODIFICATION, P-2205	Ocean Data Systems, Inc.	740401	ADA096583	U
Report 001; MSAG-1	Unavailable	MEASUREMENT SYSTEMS ADVISORY GROUP	Office of Naval Research	740401	ADA096586; ND	U
ACR-196	Gregory, J. B.	PROJECT PACIFIC SEA SPIDER, TECHNOLOGY USED IN DEVELOPING A DEEP-OCEAN ULTRASTABLE PLATFORM	Office of Naval Research	740412	AD0529945; ND	U
Unavailable	Gottwald, J. T.	ANNUAL REPORT FOR 1 MAY 1973 - 30 APRIL 1974	Tracor, Inc.	740524	AD0920210	U
Unavailable	Unavailable	ACOUSTIC MODEL SUPPORT ACTIVITIES, P-2220	Ocean Data Systems, Inc.	740530	ADA096584	U
HCI-CMC-18540	Daubin, S. C.	TRANSMISSION LOSS OF LOW FREQUENCY UNDERWATER SOUND IN THE CAYMAN TROUGH (CHURCH GABBRO TECHNICAL NOTE)	University of Miami, Rosenstiel School of Marine and Atmospheric Science	740601	ADC000424; ND	U
HCI-CMC-18343	Daubin, S. C.	AMBIENT NOISE IN THE NORTHWEST CARIBBEAN SEA (CHURCH GABBRO TECHNICAL NOTE) (U)	University of Miami, Rosenstiel School of Marine and Atmospheric Science	740601	ND	U
Unavailable	Barnes, A., et al.	DISCRETE SHIPPING MODEL	Planning Systems, Inc.	740604	ND	U