AFRL-RV-PS-
TR-2022-0007

FUNDAMENTAL RESEARCH INTO RADIATION EFFECTS IN CRYOGENIC ELECTRONICS TECHNOLOGIES

Thomas Daniel Loveless

University of Tennessee at Chattanooga
615 McCallie Ave.
Chattanooga, TN 37403

06 Nov 2021

Final Report

AIR FORCE RESEARCH LABORATORY
Space Vehicles Directorate
3550 Aberdeen Ave SE
AIR FORCE MATERIEL COMMAND
KIRTLAND AIR FORCE BASE, NM 87117-5776

NOTICE AND SIGNATURE PAGE

Using Government drawings, specifications, or other data included in this document for any purpose other than Government procurement does not in any way obligate the U.S. Government. The fact that the Government formulated or supplied the drawings, specifications, or other data does not license the holder or any other person or corporation; or convey any rights or permission to manufacture, use, or sell any patented invention that may relate to them.

This report is the result of contracted fundamental research which is exempt from public affairs security and policy review in accordance with AFI 61-201, paragraph 2.3.5.1. This report is available to the general public, including foreign nationals. Copies may be obtained from the Defense Technical Information Center (DTIC) (http://www.dtic.mil).

AFRL-RV-PS-TR-2022-0007 HAS BEEN REVIEWED AND IS APPROVED FOR PUBLICATION IN ACCORDANCE WITH ASSIGNED DISTRIBUTION STATEMENT.

//SIGNED//

CHRISTIAN MORATH
Program Manager

//SIGNED//

VINCE COWAN
Tech Advisor, Space Component Technology Branch

//SIGNED//

JOHN BEAUCHEMIN
Chief Engineer, Spacecraft Technology Division
Space Vehicles Directorate

This report is published in the interest of scientific and technical information exchange, and its publication does not constitute the Government's approval or disapproval of its ideas or findings.

Approved for public release; distribution is unlimited

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	**2. REPORT TYPE**	**3. DATES COVERED** *(From - To)*
06-11-2021	Final Report	06 Nov 2019 - 06 Nov 2021

4. TITLE AND SUBTITLE
Fundamental Research Into Radiation Effects in Cryogenic Electronics Technologies

5a. CONTRACT NUMBER
FA9453-20-2-0002

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
C6601F

6. AUTHOR(S)
Thomas Daniel Loveless

5d. PROJECT NUMBER
4846

5e. TASK NUMBER
EF133273

5f. WORK UNIT NUMBER
V1HU

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
University of Tennessee at Chattanooga
615 McCallie Ave.
Chattanooga, TN 37403

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Research Laboratory
Space Vehicles Directorate
3550 Aberdeen Avenue SE
Kirtland AFB, NM 87117-5776

10. SPONSOR/MONITOR'S ACRONYM(S)
AFRL/RVSU

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
AFRL-RV-PS-TR-2022-0007

12. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
Fundamental Research into Radiation Effects in Cryogenic Electronics Technologies

14. ABSTRACT
The overall goal of this fundamental research project was to expand the state-of-the-art understanding of radiation interactions in relevant cryogenic CMOS technologies at and below 180 nm feature sizes. This goal was accomplished through the innovative design of test chips for radiation characterization in a commercially available CMOS technology relevant to the focal plane array (FPA) and read-out-integrated circuit (ROIC) cryogenic electronics communities, and the development of a modeling strategy analysis of radiation effects degradation mechanisms, and for prediction of the natural space radiation effects response. Results have been presented to the radiation effects community in the form of journal and conference submissions, through technical interchange meetings, and through the release of technology characterization vehicle (TCV) and circuit test vehicle (CTV) design files. Full manuscripts are included as appendices.

15. SUBJECT TERMS
Radiation effects, cryogenic electronics, radiation mitigation

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**			**19b. TELEPHONE NUMBER** *(include area code)*
Unclassified	Unclassified	Unclassified	Unlimited	38	

(This Page Intentionally Left Blank)

TABLE OF CONTENTS

LIST OF FIGURES

Page

LIST OF TABLES

Page

(This Page Intentionally Left Blank)

1. SUMMARY

The overall goal of this fundamental research project was to expand the state-of-the-art understanding of radiation interactions in relevant cryogenic CMOS technologies at and below 180 nm feature sizes. The Reliable Electronics and Systems (RES) laboratory at the University of Tennessee at Chattanooga (UTC) accomplished this goal through the innovative design of test chips for radiation characterization in a commercially available CMOS technology relevant to the focal plane array (FPA) and read-out-integrated circuit (ROIC) cryogenic electronics communities, and the development of a modeling strategy analysis of radiation effects degradation mechanisms and for prediction of the natural space radiation effects response. Results have been presented to the radiation effects community in the form of journal and conference submissions, through technical interchange meetings, and through the release of technology characterization vehicle (TCV) and circuit test vehicle (CTV) design files ready for fabrication in the commercial SkyWater 90 nm bulk CMOS foundry. Full manuscripts and presentations are included as appendices.

2. INTRODUCTION

The unrelenting progress in microelectronic capabilities has enabled significant changes in commercial terrestrial applications, space systems, and command and control on the battlefield, with imaging, high-speed communication, and networking performing a critical role. Therefore, the performance, reliability, and radiation hardness of the electronics components are critical. Silicon-On-Insulator (SOI) CMOS has a long history of use in radiation-hardened electronics due to the reduced collection volumes for single-event and transient dose radiation [1]-[12]. Total ionizing dose (TID) effects are likewise partially mitigated by the thinner oxides present in advanced technology nodes. Currently, partially-depleted (PDSOI) realizations, in which the silicon thickness and doping are such that the maximum depletion region does not extend to the underlying buried oxide (BOX), and fully-depleted SOI (FDSOI) implementations, in which the silicon thickness and doping extend to the BOX, are the current mainstream production processes [2].

Moreover, these technologies offer significant advantages in RF CMOS applications due to decreased noise and increased speed compared to their bulk counterparts. Nevertheless, bulk CMOS still holds substantial market value, with high-reliability processes in mature technology generations. However, while necessary for maintaining improving trends in commercial performance, it may pose a significant risk to high-reliability applications. Figure 1 shows the ratio of radiation-induced leakage current to pre-irradiation leakage current versus technology node [13]. The onset of FDSOI, FinFET, ultra-thin body (UTBB), and Nanowire structures disrupt the improving performance trend with scaling, potentially due to the doping profiles and device architecture required to maintain performance [13]-[15]. To meet this knowledge gap, this effort resulted in innovative technology, radiation characterization, and new radiation damage analysis techniques.

Few works have been reported in the study of the radiation response mechanisms and associated mitigation approaches in mature CMOS technologies at cryogenic temperatures. These technologies are designed with commercial terrestrial performance specifications in mind and often result in significant vulnerabilities for space systems. A basic understanding of radiation and reliability effects is essential forthe continued innovation of space-appropriate microelectronics systems. Insufficient radiation effects dataat cryogenic temperatures increases the development cost of high-performance space electronics and

broadens the gap between terrestrial and space electronics systems due to substantial test requirements before hardening devices and systems. The Skywater 90 nm bulk CMOS process (S90) was identified as a technology target for the program due to SkyWater's mature and trusted manufacturing ecosystem[1]. In addition, the foundry has been optimized for peak performance in imaging and infrared applications in cryogenic environments. The technology node also coincides with peak RF performance in bulk CMOS and allows for a high level of customized mixed-signal solutions.

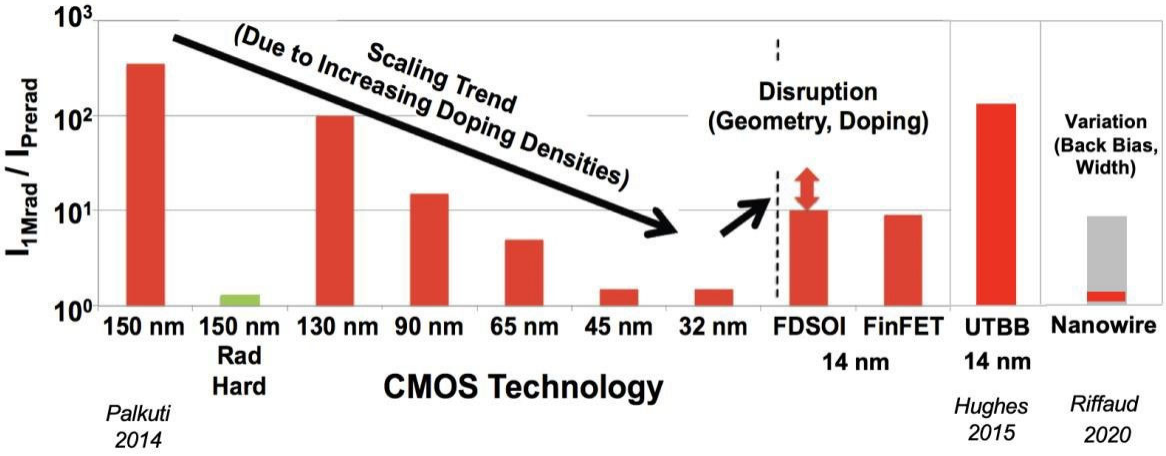


Figure 1. Ratio of post-rad (1 Mrad(SiO_2) to pre-rad leakage current versus CMOS technology

Innovative approaches to gathering robust radiation effects data sets are required to enable the design of radiation hardened applications with minimal performance penalties. Available data is often of limited use to the circuit designer due to the specific constraints and requirements imposed on the measured data and the application-specific design. As such, new radiation technology characterization vehicles (TCV) and innovative experimental strategies are required to develop a comprehensive radiation effects data set for general use in a technology. Such a technology agnostic approach is easily portable between technologies and allows for technology comparisons.

The goal of this program to expand the state-of-the-art in the understanding of radiation effects in nanoelectronics for cryogenic applications through innovative testing and design. This research has resulted in a new technology portable built-in self-test architecture for on-chip measurement of radiation effects and noise in cryogenic circuit technologies. Findings will aid in the development of novel tools and techniques for radiation effects modeling and simulation for circuit operating in cryogenic and RF domains, and innovation in the development of hardening techniques for high-speed digital and analog circuits. All of these accomplishments will enhance the state-of-the-art in high-reliability components and systems available to commercial and military space missions.

3. METHODS, ASSUMPTIONS, AND PROCUDURES

The UTC RES group developed and implemented a standardized approach to gathering radiation performance data from the SkyWater S90 process at temperature. This methodology allows for the

[1] *Note that the SkyWater S90 process is derived from Cypress Semiconductor's C9 memory process*

transition of radiation effects response mechanisms to practical application in rad-hard circuit design and implementation, including a complete cell library and Process Design Kit (PDK). Figure 2 illustrates the iterative methodology for the (i) evaluation and adaptation to a selected technology, (ii) design of early radiation vulnerability models, (iii) design and development of a technology characterization vehicle (TCV) and circuit test vehicle (CTV) suitable for characterization of radiation response metrics, (iv) fabrication of the TCV/CTV and characterization the radiation response to update radiation response models, early development of a radiation-hardened PDK, and for (v) development of library test vehicle (LTV) and circuit macros for a product demonstration vehicle (PDV). The 21-month technical portion of the program resulted in a completed TCV/CTV that is ready for fabrication. The completed test vehicles will be fabricated through SkyWaters multi-project-wafer (MPW) program in December 2021 and May 2022 through synergistic DoD support.

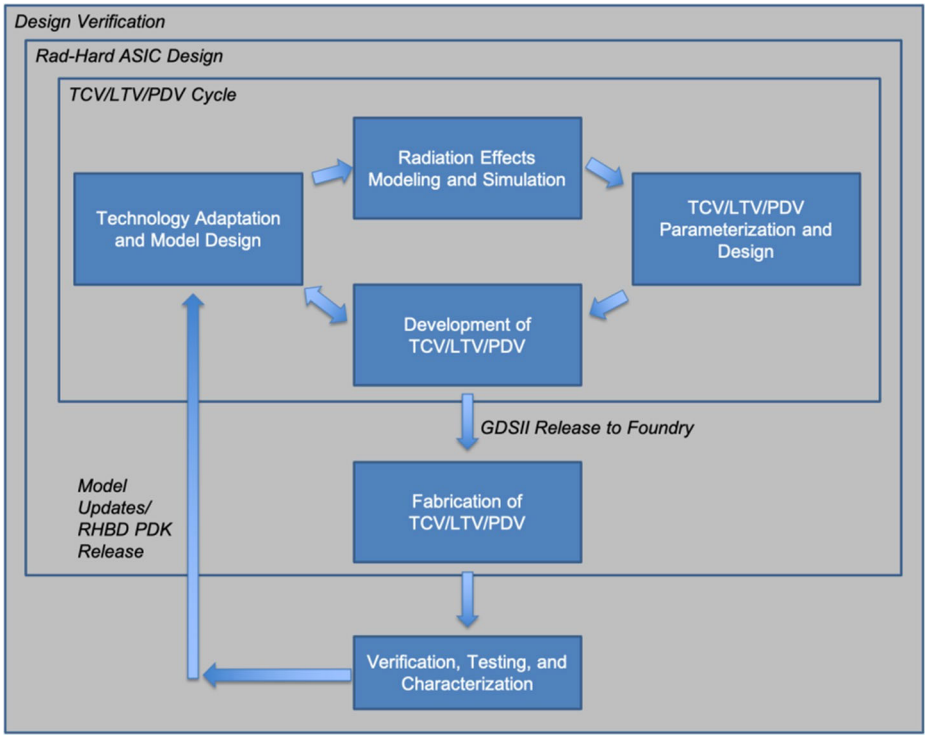


Figure 2. Development cycle for TCV/CTV, LTV, and PDV and corresponding chip release, modelupdates, and PDK release points

One full development cycle shown in Figure 2 was completed including the (i) development of early radiation response models, and (ii) the design of a TCV/CTV development and demonstration plan. Early radiation response models were implemented for predicting the single-event transient (SET) response and total-ionizing dose (TID) response of devices and circuits in the S90 process.

Transient Modeling: A commonly used analytical model to approximate the induced transient current waveform is the double-exponential function, described by the piecewise linear function in Equation (1) [16], where τ_1 and τ_2 are the rising and falling time constants associate with drift and diffusion charge collection processes, respectfully, I_{Peak} is the maximum current, t_{d1} and t_{d2} are the times associated with the onset of the event and the onset of recovery, respectfully. The integral of Equation (1) represents the total

collected charge. The time constants were estimated from the physical technology dimensions obtained from the PDK, such as the diffusion heights and well and substrate depths, and typical carrier mobilities and lifetimes. As seen in Section 4: RESULTS, the resulting transient pulse widths are reported as a range of anticipated values that have the propensity to propagate through logic. This approach allowed us to bound the maximum possible values while sacrificing physical accuracy. We observed through simulation that the SET pulse widths have an upper bound limited by the intrinsic parasitic capacitances.

$$I(t) = \begin{cases} 0; & t < t_{d1} \\ I_{Peak}\left(1 - e^{-\left(t - t_{d1}/\tau_1\right)}\right); & t_{d1} < t < t_{d2} \\ I_{Peak}\left(e^{-\left(t - t_{d2}/\tau_2\right)} - e^{-\left(t - t_{d1}/\tau_1\right)}\right); & t > t_{d2} \end{cases} \quad (1)$$

Total Ionizing Dose Modeling: The parameters of the SPICE-level transistor-model (BSIM) are useful in characterizing the operation of a device. The degraded response can be captured at the transistor level by changing these parameters. Transistor-level compact models were built to incorporate the principal TID-induced effects, *i.e.*, the decrease in and the slope of the drain current. The model parameters of the BSIM model [10] of the *nfet* and *pfet* transistors that affect the above-mentioned behaviors were identified and estimated degradation factors were applied. These parameters can be measured from the designed TCV/CTV and used to calibrate models in the future. These TID-aware compact models can be used to design AMS circuits to determine the effects of TID on circuit performance parameters [17].

Parametric Analysis: The general approach to the parameterized TCV/CTV is to model any given sensitive parameter of transistor *i* dispersed on the chip as a random variable θ_i given by (2)

$$\theta_i = \mu_{\theta,i} + \sigma_{\theta,i}(d_i) \cdot p(d_i, \phi),\ \theta_i \in \{\theta_1, \ldots \theta_M\} \quad (2)$$

where $\mu_{\theta,i}$ and $\sigma_{\theta i,di}$ are the mean and standard deviation of the ith transistor at location d_i on die ϕ, and p is the corresponding stochastic process that can take the form of an appropriate statistical distribution [18]. In this way, each parameter can be modeled using a generic approach that enables large-scale transparent simulations rather than through parametric sampling approaches through embedded behavioral compact models (though compact models will be used to inform initial stochastic models and determination of the stochastic parameter p in the absence of data). Moreover, this approach will allow for the use of Bayesian inference to derive posterior probabilities improved with measured data [19][20]. Though, initial models can be created without the need for data, thus mitigating risk associated with device procurement and experimental measurement. Data obtained from measurement of devices on the TCV/CTV will be used to improve the device-level stochastic reliability models in the future.

The general floorplan of the finished TCV/CTV is shown in Figure 3 and consists of structures for electrical calibration, total-ionizing dose (TID) leakage measurements, parasitic bipolar measurements, variability analysis, reliability analysis, noise analysis, parametric analysis of latch up vulnerabilities, andsingle-event characteristic response. The Cadence Virtuoso environment was used to realize the physicaldesign of the TCV/CTV. Details are provided in Section 4: Results and Discussion.

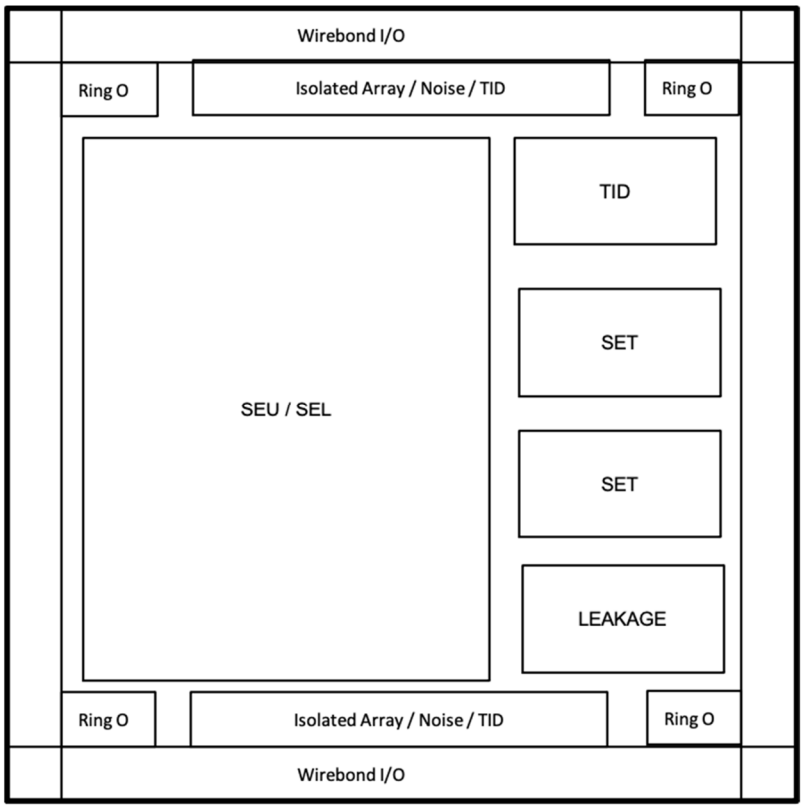


Figure 3. General floorplan for radiation effects TCV/CTV

4. RESULTS AND DISCUSSION

The designed radiation test coupon consists of two primary modules, the TCV and CTV. The first, the technology characterization vehicle (TCV), is designed to facilitate the extraction of key technology parameters that are of particular importance to radiation-effects engineers. Basic MOS devices and diodes (and associated variants) are included, for example, for electrical calibration of device models, calibration points for 2- and 3-dimensional (2D/3D) technology-computer-aided-design (TCAD) models, TID leakage measurements, parasitic bipolar measurements, and SEE charge collection measurements. The second module, the circuit test vehicle (CTV), includes but is not limited to, structures for the measurement of basic radiation-induced circuit-level effects, the evaluation of on-chip built-in-self-test (BIST) structures for radiation effects analysis, and the direct comparison of radiation measurement technologies and radiation-hardened-by-design (RHBD) circuits, including read-out-integrated circuit (ROIC) building blocks. Moreover, the CMOS bulk S90 coupon has been developed for the extraction of technology-specific features. Table 1 outlines the contents of the TCV and CTV.

Table 1. Overview of the UTC RES Test-Structure Coupon

TCV (Technology Characterization Vehicle)	CTV (Circuit Test Vehicle)
Purpose: MOSFET and Diode Parameter Extraction, Model Calibration, Total-Ionizing Dose (TID) Measurements.	*Purpose:* Measurement of Total-Ionizing Dose (TID) and Single-Event Effects (SEE), Evaluation of Built-In-Self-Test Circuits, Evaluation of Radiation-Hardening-by-Design Solutions
• Active device PROBE structures for electrical calibration of models, TID measurements, and measurement of the parasitic bipolar • Transistor device arrays in a BOND-pad configuration for measurement of intra- and inter-device variability and accelerated radiation degradation • Arrays of digital library elements for measurement of TID in the standard cell library	• Built-in-self-test (BIST) circuits for the on-chip measurement of TID, SEE, and noise performance • Read-out-integrated circuit (ROIC) building blocks for measurement of TID and SEE effects • Ring-oscillators for electrical calibration and measurement of intra- and inter-die variability

Technology Characterization Vehicle (TCV): The TCV consists of isolated device arrays (accessed via probe pads as well as embedded within the bond-pad arrangement) placed in several locations throughout the die. Figure 4 illustrates the layout of a 12-pad PROBE array that consists of 4 isolated transistors. The PROBE pad array uses a pitch of 90 um for compatibility with SkyWater's automated wafer probe measurement capability. The device arrays leverage the bond-pad structure (see Figure 5). The isolated devices and arrays are used for electrical calibration and corner analysis and to measure intra-die and inter-die variability, in addition to radiation and reliability degradation.

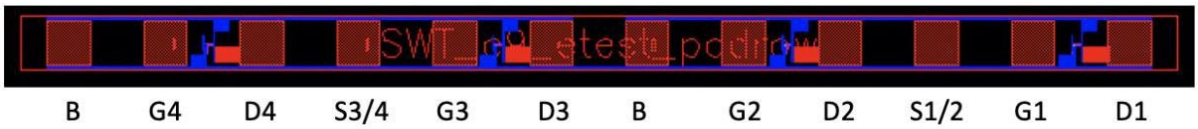


Figure 4. Layout of a 12-pad PROBE array consisting of 4 isolated transistors

Table 2 details the specific devices in the TCV. The elements consist of transistor variations offered within the process as well as custom transistor modifications to improve the TID radiation response. Specifically, these isolated arrays allow for determination of the influence of MOSFET design parameters on TID and noise responses, as well as providing radiation and reliability model calibration points. Design parameters include: Width (W), Length (L), oxide thickness, surface versus buried channel, and channel doping. Both isolated pMOS and nMOS devices are used, as well as logic configurations derived from SkyWater's standard cell library. Additionally, input/output (I/O) cells from SkyWater's standard cell library are provided for electrical evaluation of standard I/O designs and for single-event latch up (SEL) screening. The TCV will be included in a tapeout scheduled for December 202, funded through DoD support on SkyWater's RTS enhancement program. The 12-pad PROBE arrays are arranaged in two 2 x 24 matrices, occupying two 2 mm x 2 mm chiplets, as seen in Figure 5. The chiplets occupies 50% of a standard MPW tile and will be accompanied by test structures for random telegraph signal (RTS) noise test structures for the RTS enhancement program.

Table 2. TCV Elements

Item	Element	Description	Variants	Purpose
1	nshort	Nominal low-voltage (1.2 V) nMOS device.	Gate lengths = min (100 nm), 350 nm, 1600 nm and 10 um) Gate widths = min (280 nm), 1.5 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
2	pshort	Nominal low-voltage (1.2 V) pMOS device.	Gate lengths = min (100 nm), 350 nm, 1600 nm and 10 um) Gate widths = min (280 nm), 1.5 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
3	nshort_l	Low-leakage (high V_{TH}) low-voltage (1.2 V) nMOS device.	Gate lengths = min (100 nm), 350 nm, 1600 nm and 10 um) Gate widths = min (280 nm), 1.5 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
4	pshort_l	Low-leakage (high V_{TH}) low-voltage (1.2 V) pMOS device.	Gate lengths = min (100 nm), 350 nm, 1600 nm and 10 um) Gate widths = min (280 nm), 1.5 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
5	nthick	Thick-oxide high voltage (3.3 V) surface-channel nMOS	Gate lengths = min (350 nm), 500 nm, 800 nm and 10 um) Gate widths = min (420 nm), 1.2 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise

Table 2. TCV Elements (continued)

Item	Element	Description	Variants	Purpose
6	pthick	Thick-oxide high voltage (3.3 V) surface-channel pMOS	Gate lengths = min (350 nm), 500 nm, 800 nm and 10 um) Gate widths = min (420 nm), 1.2 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
7	nthick_bc	Thick-oxide high voltage (3.3 V) buried-channel nMOS	Gate lengths = min (350 nm), 500 nm, 800 nm and 10 um) Gate widths = min (420 nm), 1.2 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
8	pthick_bc	Thick-oxide high voltage (3.3 V) buried-channel pMOS	Gate lengths = min (350 nm), 500 nm, 800 nm and 10 um) Gate widths = min (420 nm), 1.2 um, and 10 um)	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
9-16	Deep N-Well	Elements 1-8 repeated with a deep N-Well option	W/L variations in 1-8	electrical calibration, TID leakage, parasitic bipolar, random telegraph signal noise
17	IO	I/O devices	library cells, level-shifters	electrical calibration, single-event latchup (SEL) measurements

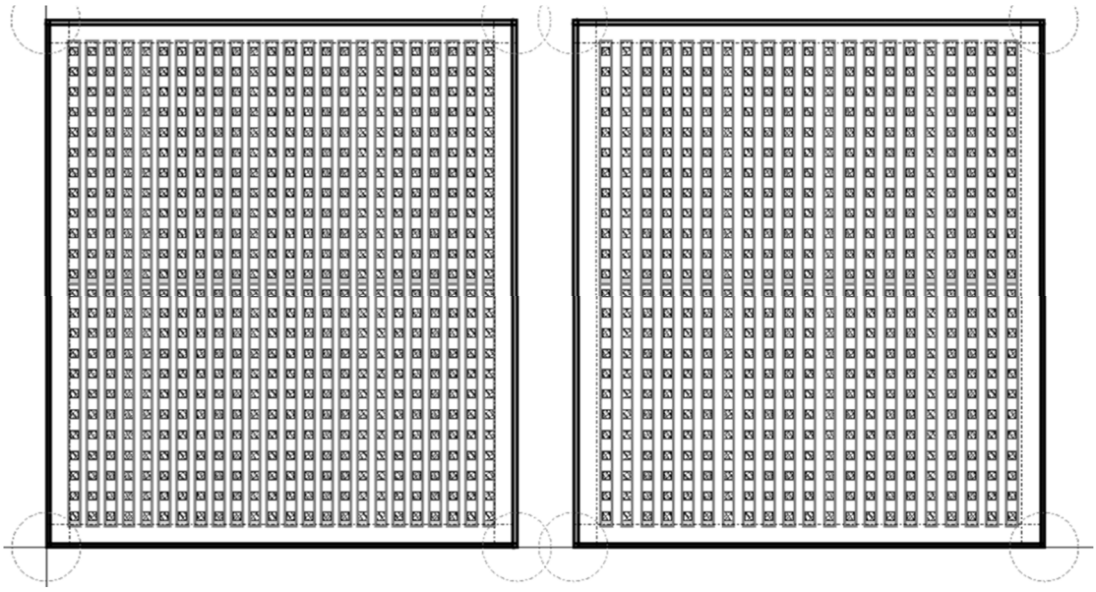


Figure 5. Top-level layout of the two 2 mm x 2 mm chiplets containing the TCV

Circuit Test Vehicle (CTV): The CTV consists of ring oscillators (RO) placed in several locations around the chip in order to measure degradation in AC parameters and to provide additional intra- and inter-die variability. Circuits, including shift registers and logic chains are provided for the on-chip measurement of single-event effects (SEE) such as single-event upsets (SEU) and single-event transients (SET). Several building blocks for read-out integrated circuits (ROIC) have been designed for characterizing radiation vulnerabilities in ROIC sampling circuits. Figure 6 shows an image of the top-level layout of a 64-pin chiplet sized to be approximately 2 mm x 2 mm. The chiplet contains the CTV modules in Table 3 and will be included in a SkyWater MPW scheduled for May 2022, funded through DoD support on SkyWater's RTS enhancement program. The chiplet occupies 25% of one standard MPW tile and can be duplicated if space is available.

Table 3. CTV Elements

Item	Element	Description	Variants	Purpose
18	RO	Ring oscillators	min NMOS, matched-drive PMOS inverter loop, 1001x	delay measurements, AC model calibration, SET measurements, variability analysis
19	SHIFTREG	Shift registers	Standard cell library DFF (4 variations), DICE and NAND-DICE	SEU measurements
20	CREST	Circuit for radiation effects self test of standard cell logic	Standard cell library logic elements (inverters, NAND, NOR)	On-Chip SEU measurements
21	INVSTRING	Inverter chains	Standard low-voltage devices from standard cell library	On-Chip SET measurements
22	AUTOSET	UTC autonomous pulse width capture circuit	min dim, 2x, 10x library cell inverter chains	On-Chip SET pulse width characterization
23	ROIC	Standard analog building blocks for read-out integrated circuits (ROIC)	ROIC front-end elements	Evaluation of radiation vulnerabilities in ROIC front-end elements

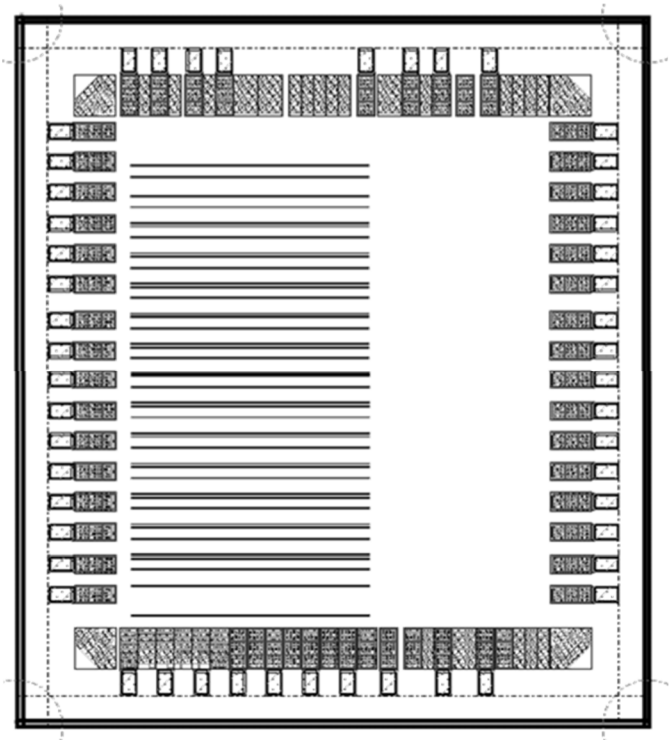


Figure 6. Top-level layout of a 2 mm x 2 mm 64-pin chiplet

Three key features of the implemented test coupon are the (1) single event transient (SET) characterization capabilities, (2) single-event upset (SEU) evaluation using a Circuit for Radiation-Effects Self-Test (CREST) approach, and the (3) ROIC standard cell array. The following sub-sections describe details regarding the features.

Single Event Transient Characterization: The single event transient (SET) characterization of is critical in the understanding of the impacts of technology node on the radiation performance of structures, as well as our development of TCAD models and single event compact models. The SET characterization circuits have been designed and validated through parasitic extraction, process corners, temperatures down to 70 K, and layout verification tools in order to measure SETs, propagate them across a 2 mm x 2 mm silicon die, and extract pulses in the range of 30 ps to approximately 3 ns.

SET simulations were conducted using the Cadence Virtuoso toolkit and the Spectre circuit simulator. A sensitivity analysis was conducted to evaluated the minimum SET pulse widths that are capable of propagating through a logic chain consisting of 10 cells (reflective of typical logic depths). Table 4 shows the minimum values of SET that have the propensity to propagate indefinitely through logic chainsbuilt with different standard cell inverters. These transients will have the capability of being latched input memory or compete with legitimate signals propagating through a circuit. Table 4 also shows the maximum expected pulse widths expected following exposure to ionizing radiation (up to a linear energy transfer or LET of 80 MeV-cm^2/mg). The SET pulse was injected by creating a current source model for injecting charge within the circuit. The integral of the current is total deposited charge, and LET is approximated by assuming linear charge deposition across the ion path length to a depth of 1 um.

Table 4. Estimates for the Expected Minimum and Maximun SET Pulse Widths in the SkyWater S90 Process

Inverter Type	Minimum SET Pulse Width(ps)	Maximum SET Pulse Width(ps)	Inverter Type	Minimum SET Pulse Width(ps)	Maximum SET Pulse Width(ps)
Inv 0	91.784	823.294	Inv 0	82.493	878.515
Inv 1	65.492	752.618	Inv 1	89.127	812.975
Inv 2	49.386	678.607	Inv 2	61.65	754.915
Inv 3	41.258	638.48	Inv 3	72.22	717.927

*Note: SETs were generated for simulated ion strikes (up to an LET of 80 MeV-cm^2/mg) on nMOS (left)and pMOS (right) transistors.

On-chip measurement of SETs is accomplished by creating arrays of inverter chains that feed a common built-in self-test (BIST) measurement circuit for quantizing the SET time widths into a digital code. We designed a time-to-digital converter based on the Vernier delay chain concept shown in Figure 7. An incoming SET pulse goes through a trigger generator that creates rising signal edges representing the onset of the pulse (Start) and end of the pulse (Stop). The signal edges propagate through the parallel delay chains that feed a sequence of data registers. The delay chains, however, are designed to have different delay times (t_2 and t_1, respectively) so that the Stop signal edge will eventually "catch up" in timing to the Start signal edge. When the signals align, the data registers will be unable to latch the triggers anymore, thus indicating the pulse width in digital units with resolution t_2-t_1.

UTC's on-chip SET measurement circuit is illustrated in Figure 8. The design includes a digitally-controlled variable delay chain. The variable chain allows for adjustments in the resolution as well as maximum measurable pulse during experimentation. Table 5 indicates the four options for resolution and maximum measurable pulse width at 70 K.

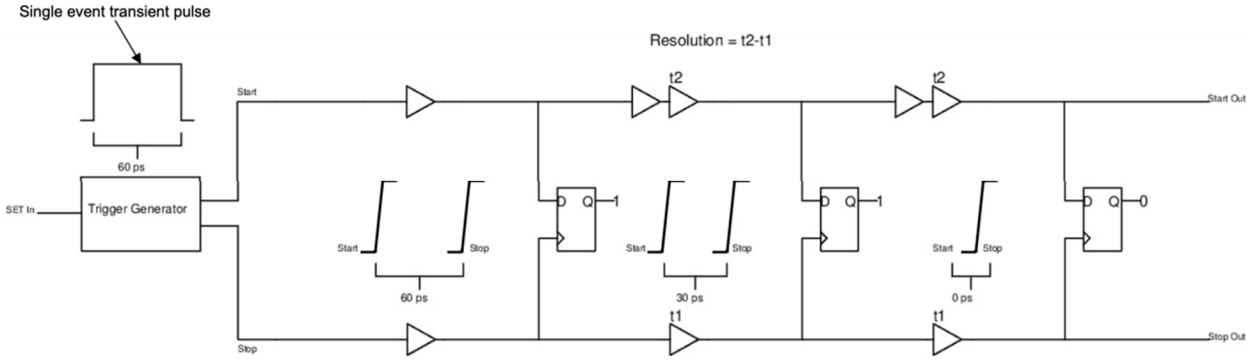


Figure 7. Vernier delay chain concept for a time-to-digital converter for on-chipSET measurement

Table 5. Measurement Resolution and Range Options for UTC's Autonomous SET Capture Circuit

Resolution(ps)	Minimum SET Pulse Width(ps)	Maximum SET Pulse Width(ps)
20	38	1024
40	38	1680
60	38	2443
80	38	2867

Single Event Upset Characterization: As part of the test coupon for the SkyWater S90 fabrication run, various Circuits for Radiation Effects Self-Test (CREST) designs were developed to test different variants of flip-flops and test the effects of combinational logic SETs on error rates. There are 6 flip-flop variants included in the CREST test circuits to test the effects of various layout techniques in S90. Designs include a baseline D flip-flop (DFF), and three other SkyWater standard cell flip-flops, and two DICE variants designed by UTC. DICE variations include an inverter-based and NAND-based designs. Each flip-flop variant contains chains of between 1000 and 2000 flip-flops built in units of 256. A pseudo random test pattern is input in the chain. The output of the shift register is compared to the data input to detect errors, as seen in Figure 8. By testing these various flip-flop circuits with the CREST design, a comparison of various circuit hardening techniques and layout variations is possible from a single test chip.

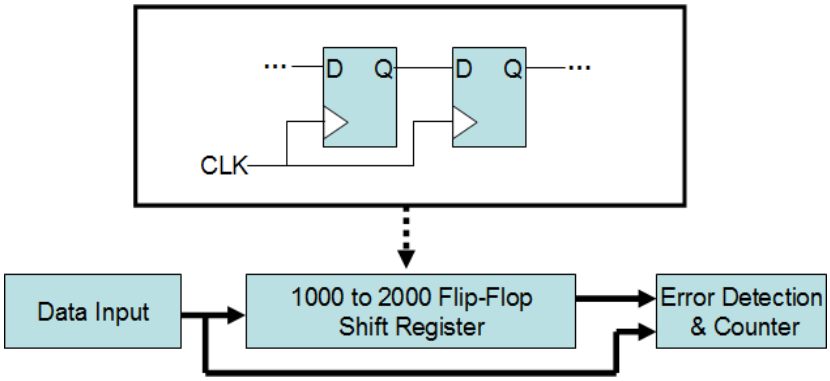


Figure 8. Basic CREST setup for the 6 different flip-flop variations

ROIC Characterization: One additional element of the CTV is the addition of analog building blocks critical for evaluation of noise and radiation vulnerabilities in focal plane arrays (FPA) and read-out-integrated circuit (ROIC) front-end electronics. Analog FPA designs generally include on-chip ROICs for photocurrent detection and conversion into analog voltages (Figure 9). These voltages, which are proportional to the collected charge in the FPA are then sampled and quantized for signal processing. A common ROIC front-end (Figure 10) includes a switched-capacitor sampling circuit and a source-follower amplifier (buffer) for distributing the pixel voltages to an analog multiplexor prior to processing. Switched capacitors are notoriously vulnerable to radiation effects. In addition, the source follower amplifier has been seen to generate RTS noise which obfuscates the FPA data. The CTV contains 4 x 4 unit cells of the circuit shown in Figure 10 that can be used for evaluation of RTS as well as SEU. These unit cells can be

arrayed to fill a 256 x 256 analog memory array, based on space permitted. The large device matrix will allow for intra- and inter-die variability analysis, as described in Section III.

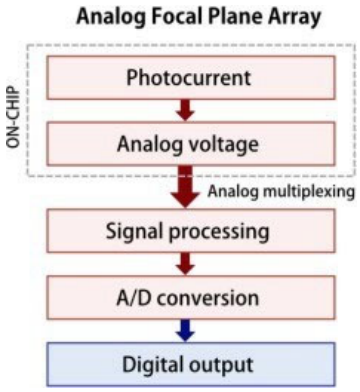


Figure 9. Typical building blocks in an analog FPA and ROIC design

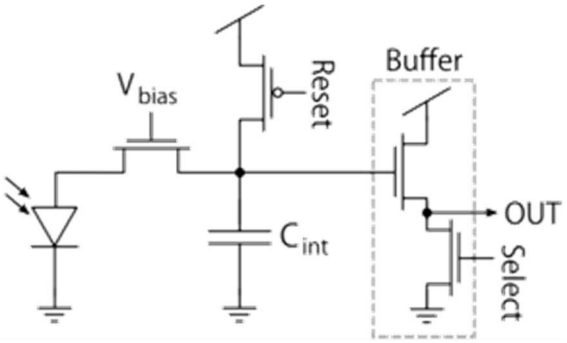


Figure 10. Simplified FPA pixel sampling circuit including a switched capacitor sampling circuit andsource-follower amplifier

5. CONCLUSIONS

The UTC RES program has developed innovative test chip designs for radiation and noise characterization in the SkyWater S90 process. The test chip designs include transistor-level and circuit-level approaches for at temperature characterization of total ionizing dose (TID), single-event upsets (SEU), single event transients (SET), single-event latch up (SEL) and random telegraph signal (RTS) noise. The test chip design will be fabricated in two parts in December 2021 and May 2022 through DoD funding and collobaration with SkyWater's RTS enhancement program. Measurement results will be disseminated to the Defense Industrial Base and DoD focal plane array (FPA) and read-out-integrated circuit (ROIC) cryogenic electronics communities. Results are expected to aid in the development of a modeling strategy for radiation effects degradation analysis and for prediction of the natural space radiation effects response. Designs have been presented to the radiation effects community in the form of journal and conference submissions, through technical interchange meetings, and through the release of technology characterization vehicle (TCV) and circuit test vehicle (CTV) design files ready for fabrication in the commercial SkyWater 90 nm bulk CMOS foundry. Full manuscripts and presentations are included as appendices.

6. REFERENCES

[1] M. J. Gadlage, J. R. Ahlbin, V. Ramachandran, P. Gouker, C. A. Dinkins, B. L. Bhuva, B. Narasimham, R. D. Schrimpf, M. W. McCurdy, M. L. Alles, R. A. Reed, M. H. Mendenhall, L. W. Massengill, R. L. Schuler, and D. McMorrow, "Temperature Dependence of Digital Single-Event Transients in Bulk and Fully-Depleted SOI Technologies," IEEE Trans. Nucl. Sci., **vol. 56**, no. 6, pp. 3115-3121, Dec. 2009.

[2] M. L. Alles, R. D. Schrimpf, R. A. Reed, L. W. Massengill, R. A. Weller, M. H. Mendenhall, D. R. Ball, K. M. Warren, T. D. Loveless, J. S. Kauppila, and B. D. Sierawski, "Radiation Hardness of FDSOI and FinFET technologies," proc. of the 2011 IEEE International SOI Conference, Tempe, AZ, Oct. 2011.

[3] T. D. Loveless, M. L. Alles, D. R. Ball, K. M. Warren, and L. W. Massengill, "Parametric Variability Affecting 45 nm SOI SRAM Single Event Upset Cross-Sections," IEEE Trans. Nucl. Sci., **vol. 57**, no. 6, pp. 3228-3233, Dec. 2010.

[4] T. Daniel Loveless, W. Timothy Holman, Bharat L. Bhuva, Lloyd W. Massengill, Jonathan R. Ahlbin, Nick M. Atkinson, En Xia Zhang, Nelson Gaspard, Pierre Maillard, Matthew J. Gadlage, Oluwole, A. Amusan, and Megan C. Casey, "Single-Event Effects Characterization of Analog, Digital, and Low-Power Electronics Designed in a Multiple-Tiered SOI Process," proc. of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Mar. 2011.

[5] D. Loveless, J. Kauppila, T. Haeffner, T. Holman, M. Alles, B. Bhuva, L. Massengill, S. Jagannathan, N. Gaspard, N. Atkinson, R. Blaine, J. Ahlbin, "Analysis of Single-Event Transients in a 45-nm SOI Technology for Rad-Hard Applications," proc. of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Las Vegas, NV, Mar. 2012.

[6] N. Rezzak, E. X. Zhang, D. R. Ball, M. L. Alles, T. D. Loveless, R. D. Schrimpf, and K. P. Rodbell, "Total-ionizing-dose radiation response of 32 nm partially and 45 nm fully-depleted SOI devices," proc. of the 2012 IEEE International SOI Conference, Napa, CA, USA, Oct. 2012.

[7] J. A. Maharrey, R. C. Quinn, T. D. Loveless, J. S. Kauppila, S. Jagannathan, N. M. Atkinson, N. J. Gaspard, E. X. Zhang, M. L. Alles, B. L. Bhuva, W. T. Holman, and L. W. Massengill, "Effect of Device Variants in 32 nm and 45 nm SOI on SET Pulse Distributions," IEEE Trans. Nucl. Sci., **vol. 60**, no. 6, pp. 4399-4404, Dec. 2013.

[8] J. S. Kauppila, T. D. Loveless, R. C. Quinn, J. A. Maharrey, M. L. Alles, M. McCurdy, R. A. Reed, B. L. Bhuva, L. W. Massengill, K. Lilja, "Utilizing Device Stacking for Are Efficient Hardened SOI Flip-Flop Designs," proc. of the 2014 IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, pp. SE. 4.1-SE. 4.7, June 2014.

[9] J. Kauppila, J. Maharrey, R. Quinn, D. Loveless, T. Haeffner, J. Rowe, D. Ball, M. Alles, and L. Massengill, "Single-Event Measurements and Modeling in 32 nm SOI CMOS," presented at the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), St. Louis, MO, Mar. 2015.

[10] R. C. Quinn, J. S. Kauppila, T. D. Loveless, J. A. Maharrey, J. D. Rowe, M. L. Alles, B. L. Bhuva, R. A. Reed, W. T. Holman, M. Bounasser, K. Lilja, and L. W. Massengill, "Heavy-Ion SEU Test Data for 32 nm SOI Flip-Flops," 2015 Nuclear Space and Radiation Effects Conference (NSREC) Data Workshop, Boston, MA, July 2015.

[11] J. A. Maharrey, J. S. Kauppila, R. C. Quinn, T. D. Loveless, E. X. Zhang, W. T. Holman, B. L. Bhuva, and L. W. Massengill, "Heavy-Ion Induced SETs in 32nm SOI Inverter Chains," 2015 Nuclear Space and Radiation Effects Conference (NSREC) Data Workshop, Boston, MA, July 2015.

[12] T. D. Loveless, S. Jagannathan, E. X. Zhang, D. Fleetwood, J. Kauppila, L. W. Massengill, "Combined Effects of Total Ionizing Dose and Temperature on a K-band Quadrature LC-Tank VCO in a 32 nm CMOS SOI Technology," IEEE Trans. Nucl. Sci., **vol. 64**, no. 1, pp. 204-211, Jan. 2017.

[13] L. Palkuti, M. Alles, and H. Hughes, "The Role of Radiation Effects in SOI Technology Development*," 2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Millbrae, CA, USA, pp. 1-2, 2014.

[14] H. Hughes, P. McMarr, M. Alles, E. Zhang, C. Arutt, B. Doris, D. Liu, R. Southwick, and P. Oldiges, "Total Ionizing Dose Radiation Effects on 14 nm FinFET and SOI UTBB Technologies," 2015 IEEE Radiation Effects Data Workshop (REDW), pp. 1-6, 2015.

[15] J. Riffaud, M. Gaillardin, C. Marcandella, N. Richard, O. Duhamel, M. Martinez, M. Raine, P. Paillet, T. Lagutere, F. Andrieu, S. Barraud , M. Vinet, and O. Faynot, "TID Response of Nanowire Field-Effect Transistors: Impact of the Back-Gate Bias," *IEEE Trans. Nucl. Sci.*, **vol. 67**, no. 10, pp. 2172-2178, Oct. 2020.

[16] R. C. Baumann, "Soft errors in advanced semiconductor devices-part I: The three radiation sources," IEEE Trans. Device Mater. Rel., **vol. 1**, no. 1, pp. 17–22, 2001.

[17] S. Jagannathan, T. D. Loveless, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, T. D. Haeffner, J. S. Kauppila, N. Mahatme, B. L. Bhuva, M. L. Alles, W. T. Holman, A. F. Witulski, and L. W. Massengill, "Sensitivity of High-Frequency RF Circuits to Total Ionizing Dose Degradation," *IEEE Trans. Nucl. Sci.*, **vol. 60**, no. 6, pp. 4498-4504, Dec. 2013.

[18] A. Zjajo (2014). Stochastic Process Variation in Deep-Submicron CMOS. Springer Netherlands.

[19] A. Vehtari and J. Ojanen, "A survey of Bayesian predictive methods for model assessment, selection, and comparison," Statistics Surveys**, vol. 6**, pp. 142-228, Oct. 2012.

[20] D. Spiegelhalter and K. Rice, "Bayesian Statistics," Scholarpedia, **vol. 4**, no. 8, pp. 5230, 2009.

APPENDIX

PUBLICATIONS AND PRESENTATIONS

Page

A-1. Cryogenic Radiation Effects Test Coupon in SkyWater 90nm - Publication

Cryogenic Radiation Effects Test Coupon in SkyWater 90nm

Ryan Young, Spencer Westfall, David Deberry

University of Tennessee Chattanooga
Chattanooga, TN USA
bhl553@mocs.utc.edu

Daniel Loveless

University of Tennessee Chattanooga
Chattanooga, TN USA
Daniel-Loveless@utc.edu

***Abstract*—A test coupon for cryogenic radiation effects in the SkyWater 90nm technology is presented. Both a circuit test vehicle (CTV) and technology characterization vehicle (TCV) are presented within the test coupon.**

Keywords—Built-In-Self-Test, Cryogenic Electronics, Radiation Effects, Single-Event Effects, Total Ionizing Dose

I. Introduction

A common challenge for design of commercial products into DoD applications is lack of access to technology parameters and test devices that are designed to perform in extreme environments (radiation, temperature) outside of what is commercially available. This test coupon is designed to provide both characterization parameters and novel test circuits that can be shared with the radiation effects community, allowing for collaboration of information for utilization in DoD applications using commercially available parts. This test coupon is designed to classify the radiation susceptibility of the SkyWater 90nm bulk CMOS technology (S90) in cryogenic, or otherwise extreme environments.

The test coupon is designed on a single chip, but is split into two modules, the technology characterization vehicle (TCV) and circuit test vehicle (CTV). The TCV is used for measurement of electrical parameters and circuit calibration, total-ionizing dose (TID) effects, and noise. The CTV includes several circuit test structures for the measurement of single event effects (SEE). These structures include combinational logic for capture and measurement of single event transients (SET), and a built in self-test (BIST) architecture for analyzing single event upsets (SEU) in latch and flip-flop designs. All control circuits and elements are designed to be radiation-hardened and are equipped with guarding mechanisms to ensure that detected errors originate in the desired area, and not inside of the control systems.

II. TCV Design

It's vitally important to be able to calibrate and determine baseline characteristics of the technology as well as measure die-to-die variability. This information will be used to help determine the susceptibility of the technology to radiation and to put together base data for later experiments used in generating useful statistics from collected experimental data.

The TCV consists of isolated device arrays placed in several locations throughout the die. The arrays are used to measure intra-die and inter-die variability, in addition to radiation and reliability degradation. The arrays consist of transistor variations offered within the process as well as custom transistor modifications to improve the TID radiation response. Specifically, these isolated arrays will allow for determination of the influence of MOSFET design parameters such as Width, Length, gate type, and oxide thickness on TID and noise responses, as well as providing radiation and reliability model calibration points. Both isolated pFETs and nFETs are used as well as NAND and NOR logic gates. Additionally, ring oscillators will be placed in several locations around the chip in order to measure degradation in AC parameters and to provide additional intra- and inter-die data.

III. CTV Design

The CTV includes several different structures to interrogate the susceptibility of the S90 process to SEEs. Both SEU and SET structures are capable of "self test", that is capture and quantization of transient and upset phenomena independently and at speed. The only outside influence is a communication line used to offload data from the measurement circuits.

An SET target design was developed that achieves a large total sensitive area of inverter and other logic chains, that will maintain pulse distortion benefits of short inverter chains, this was accomplished by using many short inverter chains and performing a logical OR of all networks [1]. The SET target consists of four different logic types. three inverter sizes, SkyWater 1x, 2x, and 3x, and SkyWater 1x NAND gates. Each logic target is placed in a column, with 24 gates per row, 64 rows per column, and 16 columns (4 per type), for a total of 25,476 total gates, as seen in Figure 1.

Preliminary simulation data suggests that combining a 5-stage OR network, such as that presented in [1], skewed the signal on the falling edges of the network in the S90 process; to compensate for the skew, an edge detection circuit was

placed at the end of each row to propagate a delayed pulse corresponding the rising and falling edges of the radiation-induced transients. These "start" and "stop" pulses can propagate through arbitrarily long logic chains with minimal skew by taking advantage of differential common-mode rejection. Transients occurring within these logic chains are measured using a radiation-hardened Vernier-delay chain with a minimum pulse width of 30 ps, and a 31 ps resolution at room temperature.

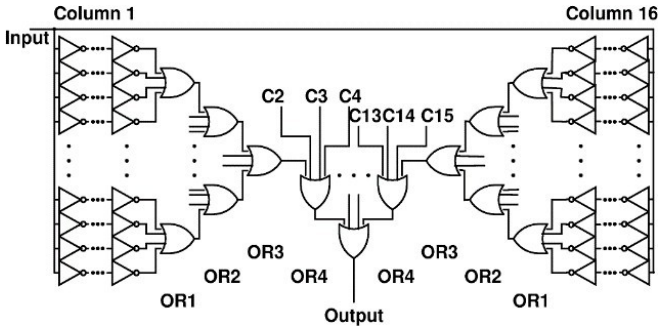


Figure 1. Schematic representing two columns of inverters, columns 1 and 16, and the five levels of the OR-gate network that connect all 1024 inverter chains. The target has a total of 24576 inverters and 341 four-input OR-gates [1]

SEU are evaluated using BIST techniques using circuits called circuit for radiation self-test (CREST) and combinational-logic circuit for radiation self-test (C-CREST) [4]. Each CREST device leverages the same basic architecture shown in Figure 2. A radiation hardened and triple modular redundant 7-bit repeating random pattern generator (RPG) provides data for shift registers designed with various D flip flops (DFF). The outputs of the RPG and the shift registers are compared by an on-chip error detection and counter to determine if an upset occurrs. Our CTV includes 6 different DFF designs with varying radiation tolerance. Specifically, the SkyWater standard 1x and 4x DFFs, a 1x DFF with improved well and substrate contacting, the SkyWater standard 1x reset DFF, the University of Tennessee Chattanooga (UTC) DICE latch, and the UTC NAND DICE latch are provided. The CREST variants can be measured simultaneously and operate with a clock frequency of 400 MHz.

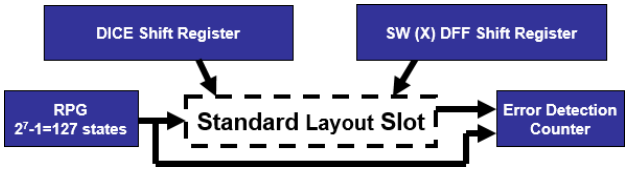


Figure 2. Schematic for CREST devices, representing random data generation, a shift register structure, and error detection.

One combinational logic for CREST (C-CREST) device is also provided to test for the combination of both latch and logic errors when used together [2]. The structure is different from the CREST device where the data source is implemented from off chip, and the shift register is lengthened to 576 bits opposed to 127 bits. Combinational logic cells include buffers, XOR gates, multiplexors, and counters, which are all common logic circuits used in readout integrated circuits (ROIC), and will be useful in collecting data for ROIC purposes.

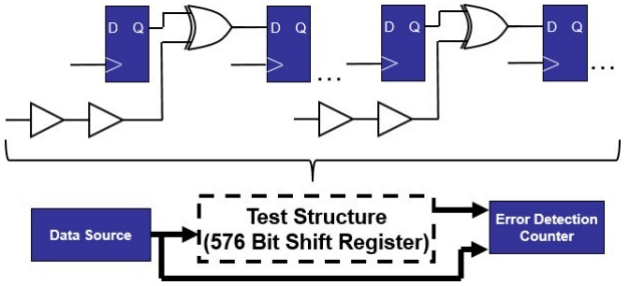
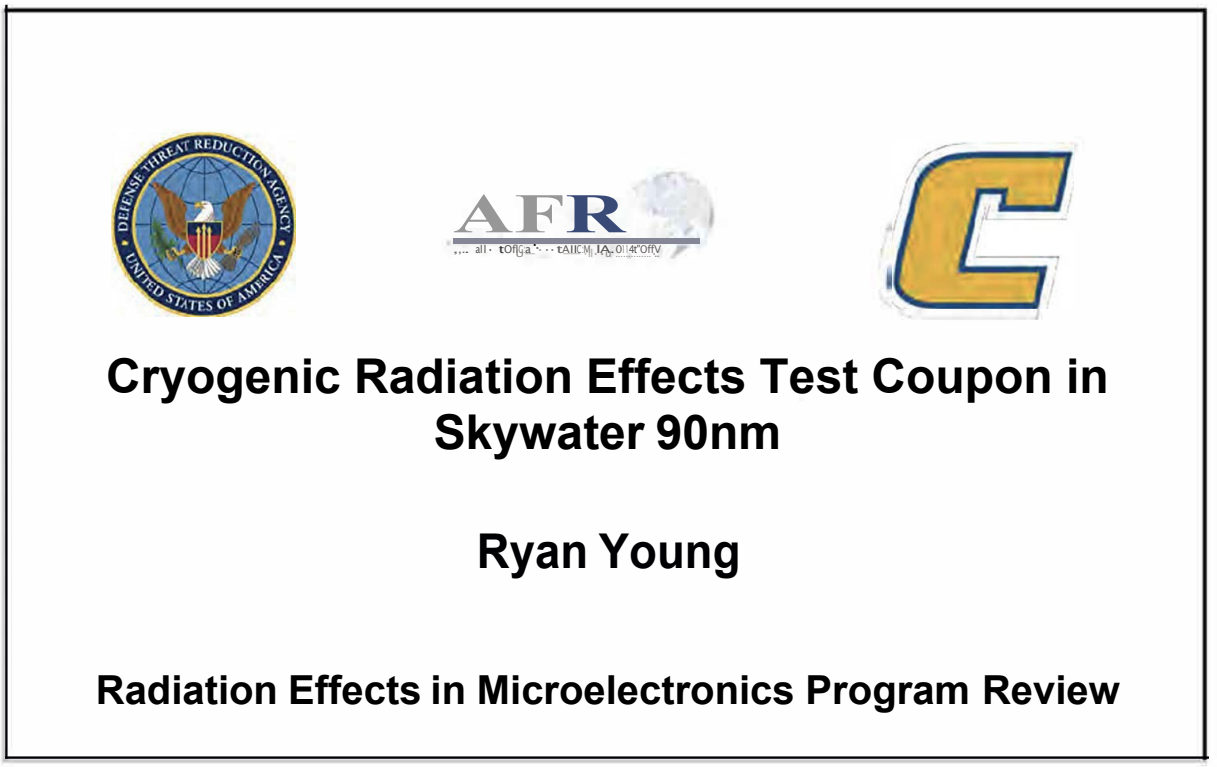


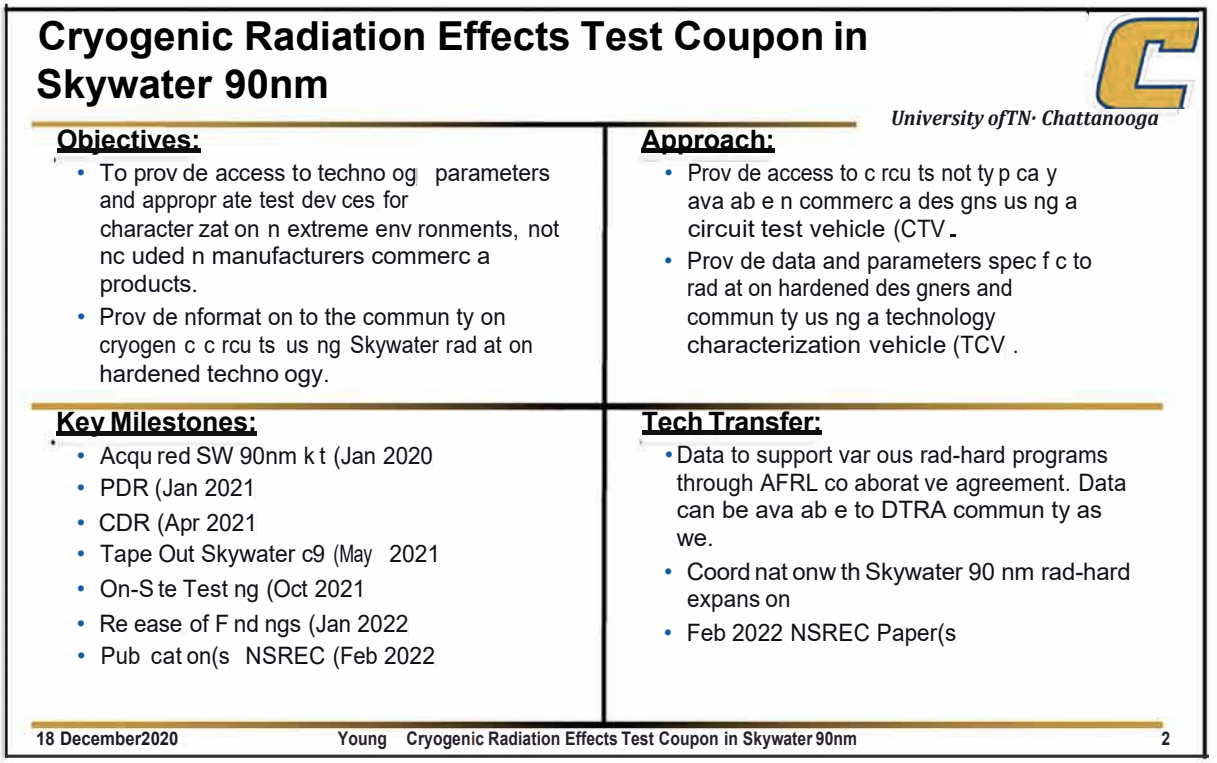
Figure 3. Schematic of C-CREST structure for SEU BIST capabtility.

REFERENCES

[1] T. D. Loveless, *et al.*, *IEEE TNS*, Dec. 2012
[2] J.R. Ahlbin, *el at, IEEE TNS,* Dec. 2008
[3] P.E. Dodd, *et al, IEEE TNS*, June 2003
[4] A. Balasubramanian, *et al, IEEE TNS,* Dec. 2008.

A-2. Cryogenic Radiation Effects Test Coupon in Skywater 90nm - Presentation





Objective and Timeline

University ofTN· Chattanooga

Provide access to parameters important for extreme environments (radiation, temperature)

Timeline:

- Acquired SW 90nm ktt (Jan 2020)
- PDR (Jan 2021 J
- COR (Apr 2021)
- ape Out Skywater c9 (May 2021)
- On-Site esling (Oct 2021)
- Release o Findings (Jan 2022)
- Publication NSREC (Feb 2022)

Technology Characterization Vehicle

University ofTN· Chattanooga

TCV (Technology Characterization Vehicle)

Basic test structures for:

- Electrical calibration
- Total-ionizing dose leakage measurements
- Parasitic bipolar measurements
- Variability Analysis
- Reliability Analysis
- Noise Analysis (Random Telegraph)

- **Ring Oscillators**
- **Isolated MOSFETs** *(finger, oxide variants)*
- **Isolated NANO logic gate configurations** *(width variants)*
- **Isolated NOR logic gate configurations** *(width variants)*

Circuit Test Vehicle (CTV)

University of TN - Chattanooga

CTV (Circuit Test Vehicle)

Standard and novel test circuits for:
- Delay measurements
- Electrical and radiation effects calibration
- SET measurements
- Built-in self-testing for single event evaluation of latch and flip/flop designs
- Single event measurements of analog and mixed-signal circuits
- Evaluation of BIST approaches

- R ng osc ators (dev ce var ants, d e check)
- I/O ce s (ESD, eve -sh ft ng nterfaces, standard brary ce s)
- Iso ated sh ft reg ster des gns
- CREST (C rcu t for Rad at on Effects Se f Test)
- C-CREST (Comb nat ona Log c C rcu t for Rad at on Effects Se f Test)
- Comb nat ona og c
- SET pu se w dth measurement c rcu ts
- Read Out Integrated C rcu ts (ROIC)

Device Arrays

Universityof TN· Chattanooga

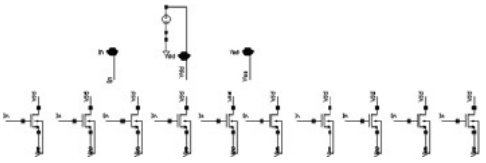
Uses

- MOSFET Influence on TIO and SET Responses
- TIO
- Leakage Current
- Noise
- Electrical Reponses (Model Verifciation)

Device Types

Isolated MOSFETS
- PINFETS Short Oxlde
  - 1 2 3 Finger Variants
  - Folded
- PINFETS Thick Oxlde
  - 1 2 3 Finger Variants
  - Folded

Isolated Logic Cells
- NAND
  - 1 2 3 Finger Variants
  - Folded
- NOR
  - 1 2 3 Finger Variants
  - Folded



Paralel placed nFETSschematic

laolabkt nFET cell (100)

SET Targets

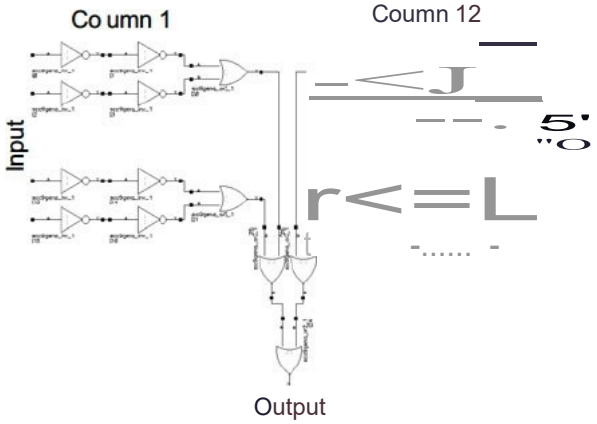
Universityof TN· Chattanooga

Parameters

12 Columns (4 per type)
24 nverters per chain
64 Chains per column
18 432 Total inverters
3 Total target types
1x Standard inverter Used
Scaled to 2x and 3x
OR Network staged
Chain-> Chain per Column
Column -> Column
Output to SET measurement circuit

Inverter Chains (Skywater Standard Cells)

- Minimum Sized (1x 1160nm/ 800nm)
  - NominalVt
- 2x nverters
  - NominalVt
  - Folded
- 3x nverters
  - NominalVt
  - Folded

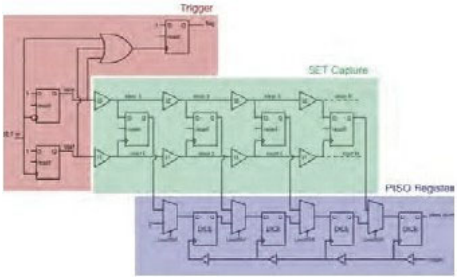


Visualization only, not drawn to scale or for accuracy.

SET Pulse Width Measurements

Universityof TN· Chattanooga

- **SET Pulse Width Measurement Circuit:**
  - Vanderbilt Autonomous Vernier Chain
    - {~16ps .. + **N x** 16ps .. + 160ps}
- **Capable of evaluating pulses as small as ~16 ps, with pulses over 32ps being measured in ~32ps blocks stages.**



Vanderbilt Autonomous Pulse Capture Circuit (VUAUTO) (Image la.ken from *Exploiting Parallelism and IHterogenelty In • Radiation Effects Te.st Vehicletor Efficient Sing,.Event Charactwtzatlon of NanoscaM Circuits. J•.s. KauppHla.J*

Output of the PISO register will be representative of the measured SET pulse.

Single Event Upset (SEU) Measurements

University of TN - Chattanooga

CREST (Circuit for Radiation Effects Self Test):

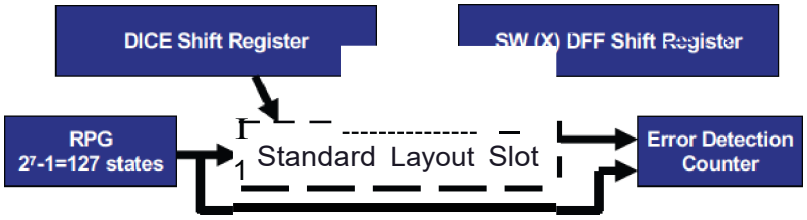
Bu t n se f test ng scheme for s ng e event eva uat on of atd'l and f p/f op des gns

7 Flip/Flop variants included in UTC-SW90 design:

- LJTC Desgned DICE FF topoogy
- Skywater Standard DFF 1/4x
- Skywater Standard DFF 1x Heavy Contact
- Skywater Reset DFF 1/4x

Designed for up to 1016 cells per variant

All cell arrays can simultaneously be evaluated on-chip and at-speed (**400 MHz)**



Single Events in Combinational Logic

University of TN - Chattanooga

C -CREST {Combination Logic Circuit for Radiation Effects Sett Test)

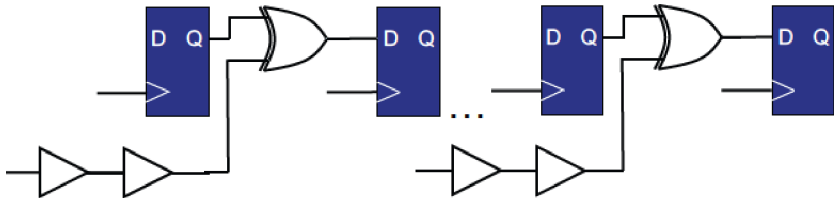
Built-in sel -testing scheme or single event evaluation o latch and lip/ lop designs with combinational logic elements to distinguish between latch and combinational log1ic errors

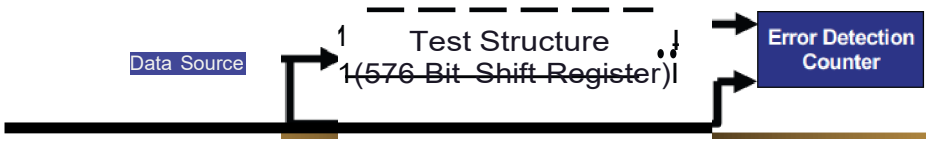
Combinetional logic to include bu ers XOR gates multiplexors and counters (Common logic circuit,sin RO C design)

Designed for 576 cells

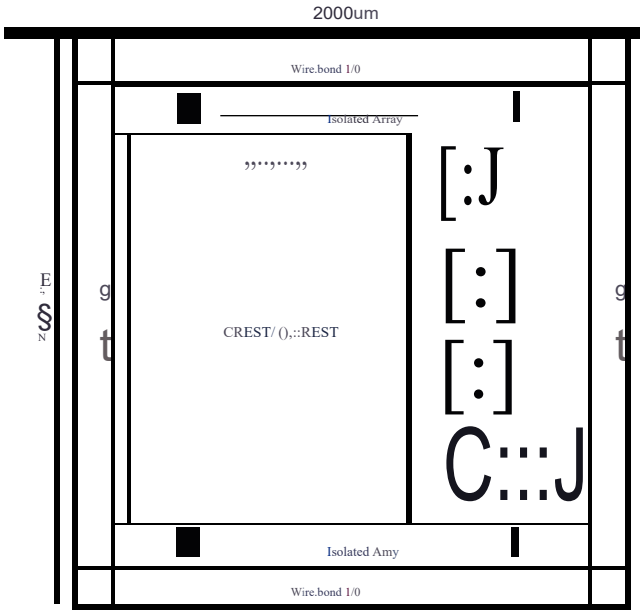
All cell arrays can slmultaneousl,y be evaluated on-chip and at-speed {S **,OO MHz}**

Used to evaluate tlile coni.lbutlon of transients to upsets





Floor Plan



University of TN· Chattanooga

- Chip Parameters
  - 1/0 :3.3V
  - Core Votage: 1.2V
  - Pn Number: 119
- Included Devices
  - asET Targets
  - 1S ET I'v'ieasurement C rcut
  - Iso ated MOSFETS
  - 4 R ngOsc ators
  - 7 CREST Dev ces
  - 1 C CREST Dev ce
  - *Analog ROIC sub circuits (Tentatively)*

Future Work

University ofTN· Chattanooga

- Finish Design (Current ~ Jan 2021)
- Conduct Simulation Campaign (Jan 2021)
- Preliminary Design Review (Jan 2021)
- Critical Design Review (April 2021
- Tape Out Skywater c9 Technology (May 2021)
- Release of Findings (Jan 2022)
- Publication at NSREC (Feb 2022)
- Reproduce Chip in Skywater Skywater 90 nm rad-hard expansion (~Late 2021 - 2022)

LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

AMS	Analog and Mixed-Signal
BIST	Built-in Self-Test
BOX	Buried Oxide
CMOS	Complementary Metal Oxide Semiconductor
CREST	Circuit for Radiation Effects Self Test
CTV	Circuit Test Vehicle
DFF	D Flip-Flop
DICE	Dual Interlocked Cell
DoD	Department of Defense
FDSOI	Fully Depleted Silicon on Insulator
FET	Field Effect Transistor
FPA	Focal Plane Array
IO (I/O)	Input and Output
LET	Linear Energy Transfer
LTV	Library Test Vehicle
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPW	Multi-Project Wafer
nFET	n-type Field Effect Transistor
nMOS	n-type Metal Oxide Semiconductor
PDSOI	Partially Depleted Silicon on Insulator
PDK	Process Design Kit

PDV	Product Demonstration Vehicle
pFET	p-type Field Effect Transistor
pMOS	p-type Metal Oxide Semiconductor
Rad	Radiation (or unit of radiation)
RHBD	Radiation Hardened (or Hardening) by Design
RES	Reliable Electronics and Systems
RF	Radio Frequency
ROIC	Read-Out Integrated Circuit
SEE	Single-Event Effects
SEL	Single-Event Latchup
SET	Single-Event Transient
SEU	Single-Event Upset
SOI	Silicon on Insulator
TCAD	Technology Computer-Aided Design
TCV	Technology Characterization Vehicle
TID	Total Ionizing Dose
UTBB	Ultra Thin Body and BOX
UTC	University of Tennessee at Chattanooga
V_{TH}	Threshold Voltage

DISTRIBUTION LIST

DTIC/OCP 8725 John J. Kingman Rd, Suite 0944 Ft Belvoir, VA 22060-6218	1 cy
AFRL/RVIL Kirtland AFB, NM 87117-5776	1 cy
Official Record Copy AFRL/RVS/Christian Morath	1 cy

(This Page Intentionally Left Blank)