Single Step Bonding of Thick Anodized Aluminum Oxide Templates to Silicon Wafers for Enhanced System-on-a-Chip Performance

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**Abstract**

Vertically-aligned nanostructures are of interest for novel system-on-a-chip applications including sensing and energy storage. Templated synthesis of such structures has been previously demonstrated via anodized aluminum oxide (AAO). However, the performance of AAO-on-Si devices has been limited by current methods of obtaining well-adhered, thick AAO templates on Si substrates. Thicker AAO templates allow for longer nanostructures of active material, which is expected to increase performance of devices reliant on the surface area or volume of the active material. In this study, Al-Si eutectic bonding is used to achieve thick AAO-on-Si, with templates up to 90 μm thick bonded to the wafer. Carbon nanotubes (CNTs) are grown in the AAO templates bonded to Si to create proof-of-concept on-chip electrochemical double layer capacitors (EDLC) devices. Our devices show a promising value of 0.44 mF $cm^{-2}$, much higher than previous AAO capacitors on Si chips. The structure of the CNT/AAO/Al/Si stack is examined using SEM and TEM, and the device performance is tested through cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS), and galvanostatic charge-discharge (GCD) measurements.

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**Keywords**

Anodized aluminum oxide; carbon nanotubes; ionic liquid; supercapacitor; system-on-a-chip

## 1. Introduction

Systems-on-a-chip (SOCs) are of great interest in remote sensing, with applications in structural health monitoring, gas sensing, and implantable biological sensing [1]–[3]. Ideal remote sensing SOC devices would be operable as-deployed over long periods of time without active maintenance such as battery replacement or manual data collection. These devices would require on-chip energy harvesting and storage in addition to their sensing and transmitting modules. Recently, a fully integrated SOC energy storing and harvesting module was demonstrated using thin-film microsupercapacitors (MSCs) integrated with on-chip transistors [4].

Anodized aluminum oxide [5] (AAO) is a hard nanotemplate consisting of an ordered array of cylindrical channels within an $Al_xO_y$ matrix perpendicular to the Al substrate. The channels are open on the surface, but the base of the pore is covered by a thin oxide layer often referred to as the barrier oxide layer. Electrical contact to nanostructures in the pores can be made by removing this barrier layer through either a modification to the anodization potential [6] or wet etching [7]. AAO has been used to create vertically-aligned nanostructures for sensing, energy harvesting, and energy storage applications [2], [8]–[12] making it a material of great interest for SOCs. Previous work has shown that AAO can be patterned through conventional lithographic techniques, further demonstrating its applicability for SOC devices [13]. However,

the performance of devices based on AAO is limited by the thickness of the AAO template [14]; thicker templates allow for greater volumes or surface areas of active materials per footprint area on the chip. Integrating thick AAO templates with Si substrates has had limited success, with most AAO-Si work being performed on thin films only a few μm thick. In this work, we present a new and simple approach for bonding very thick (>50 μm) AAO templates to Si wafers. These thick AAO-on-Si templates are then used to create electrochemical double layer capacitors (EDLCs) which greatly outperform previous AAO capacitors formed on Si wafers.

One commonly used method of obtaining AAO on Si is by directly depositing Al on the wafer through one of several vacuum deposition techniques. The deposited metal film is subsequently anodized to form an AAO layer on the wafer. Vacuum deposition processes are well-suited for thin-films, but deposition rates on the order of 1 nm $s^{-1}$ greatly limit this approach for AAO applications requiring thick films such as high-performance SOCs [15]–[17]. Rabin et al. reported the thickest AAO from this method we are aware of, depositing 12 μm of Al to yield approximately 17 μm of AAO if the entire film were consumed [18]. However, the film thickness varied by as much as 50% across the wafer and delamination of the film after anodization was often observed. Delamination of vacuum-deposited Al films has previously been addressed through both precise control of the anodizing process and by depositing additional adhesion layers between the Al and Si [18]–[20]. These methods allow for well-adhered AAO films on Si, but they do not address the issue of limited film thickness which limits overall device performance.

The second method of obtaining AAO on Si is a template transfer process in which the AAO template is freed from the residual Al through chemical etching and subsequently attached to the Si [21]–[23]. The brittle AAO templates are easily fractured in this method, which makes

the process unfavorable for large-scale production. Jang et al. [24] attempted to solve the problems associated with the brittleness of the templates by creating thicker AAO, removing the underlying Al as normal, and using vacuum deposited gold as a bonding layer between the AAO and substrate. To our knowledge this is the only report of thick (>20 μm) AAO templates on Si which could be used for high performance SOCs. However, this technique relies on chemical etching steps to remove the residual Al from the AAO, vacuum deposition of bonding materials, high pressure (5 MPa) heat treatments, and ion etching to remove the barrier layer, all of which are avoided in the present study.

In this work, eutectic bonding of Al and Si is demonstrated as a single-step method of bonding thick AAO films to Si wafers. Al-Si eutectics [25] are commonly used in contacting solar cells and older generation CMOS devices, and they have also been used as a braze material between Al surfaces [26]–[29]. Using these eutectics to produce thick (>20 μm) AAO templates on Si would enable a new generation of integrated SOCs due to the versatility of AAO as a nanotemplate. As proof of concept, 250 μm thick Al films were anodized to produce 55 μm thick AAO templates. The Al films with the AAO template on top were then bonded to Si, and carbon nanotubes (CNTs) were deposited in the AAO via chemical vapor deposition (CVD). CNT/AAO/Al/Si stacks were then used as electrodes in bulk scale pouch-cell type EDLCs to study their applications for on-chip microsupercapacitors [30], [31]. AAO-based EDLCs have shown as much as 223 mF $cm^{-2}$ under optimized conditions [32], but these devices have never been demonstrated for on-chip applications. On-chip electrostatic metal-insulator-metal capacitors made using AAO-on-Si [33] have only reported values as high as 0.002 mF $cm^{-2}$. The AAO-on-Si devices in the present study show a promising capacitance of 0.44 mF $cm^{-2}$, comparable to other carbon-based on-chip EDLCs.

## 2. **Methods**

### *2.1 Anodization*

Unless otherwise stated, chemicals were obtained from Sigma-Aldrich and used as-received. Discs of Al (99.999%, Goodfellow) 2.5 cm in diameter were punched out of 250 µm thick sheeting. The pieces were degreased by sonication in soapy water, acetone, and ethanol. The Al was anodized via the two-step method [34] in 0.3 M oxalic acid at 15°C and 40 V. The first anodization lasted for more than 16 h. The resulting disordered AAO layer was then removed through etching for 2 h in a 1.8% wt. chromic acid/6% wt. phosphoric acid solution heated to at least 60°C. The second anodization was carried out using the same conditions for 10 h to achieve a final AAO thickness of 55 µm, depicted in Fig. 1a. Longer anodization times were also used to create thicker AAO layers of 90 µm, which were successfully bonded to Si. At the end of the second anodization, the voltage was dropped linearly to 0 V by 1 V $s^{-1}$ to achieve barrier layer thinning at the AAO pore bottom shown schematically in Fig. 1b (detail in Fig. S1). This enables the CNTs to make direct electrical connection to the Al current collector in the EDLC devices. The Al discs were anodized in a custom-built sample holder which kept the anodized area constant for all samples at a 1.9 cm diameter circle (2.85 $cm^2$).

### *2.2 Carbon Nanotube Deposition and AAO/Si Bonding Post-Anodization*

After both anodization steps, there is approximately 130 µm of Al below the AAO to react in the eutectic bonding process. Si squares 2.5 cm × 2.5 cm were cleaved from 300 mm wafers to act as carrier wafers for the thick AAO films. Before CVD, the Si was washed through sonication in acetone and ethanol. No pre-bonding etching was performed on the native oxide on the Al or Si. The anodized Al was bonded to the Si during the growth of the CNTs in the AAO pores shown in Fig. 1c. A homebuilt CVD chamber (2-inch diameter tube furnace, Lindberg

Blue M from Thermo Scientific) was used to deposit CNTs in the pores of the AAO by decomposing $C_2H_2$ (21 sccm) in Ar (284 sccm) and $H_2$ (10 sccm) at 650°C for 6 h. In order to keep the AAO/Al film from deforming and to maintain contact with the Si wafer, an $Al_2O_3$ washer of approximately 60 g was used to weigh down the AAO. The washer pressed only on the un-anodized rim of the AAO/Al film while leaving the AAO template open to the reaction gas during CNT growth. After CVD, the CNT/AAO/Al/Si stacks were etched with Ar plasma using a Unaxis SLR RIE/ICP etch system. The plasma was generated at 90 W and the samples were etched for 2 min under 20 sccm Ar at 20 mTorr pressure with a power of 250 W. This etch step was important to remove the amorphous carbon film deposited on top of the AAO template during CVD and fully open the CNTs as seen in Fig. 1d.

*2.3 Pouch Cell Supercapacitors*

Symmetrical pouch cell devices were made using two CNT/AAO/Al/Si electrodes separated by glass fiber filter paper (0.7 μm pore size, 0.46 mm thick, MilliporeSigma) sealed in a Mylar pouch. A hole was drilled through the backside of the Si using a modified drill press to allow for electrical connection between the Al current collector and Al metal tabs extending out of the EDLCs. The final device is depicted in Fig. 1e. After sealing three sides of the Mylar pouch, the unsealed pouch was transferred to a vacuum oven and dried overnight at 50°C. The unsealed devices were then transferred to an MBraun glovebox antechamber and held under vacuum for more than 1 h to cool before being transferred into the Ar atmosphere. The separator was wetted with 0.5 mL of neat 1-ethyl-3-methylimidazolium tetrafluoroborate (EMIM-BF4, ≥99%) as the electrolyte. The hollow CNTs create very large and controllable surface areas that can be tuned by changing the pore size or pore length of the AAO via the anodization conditions.

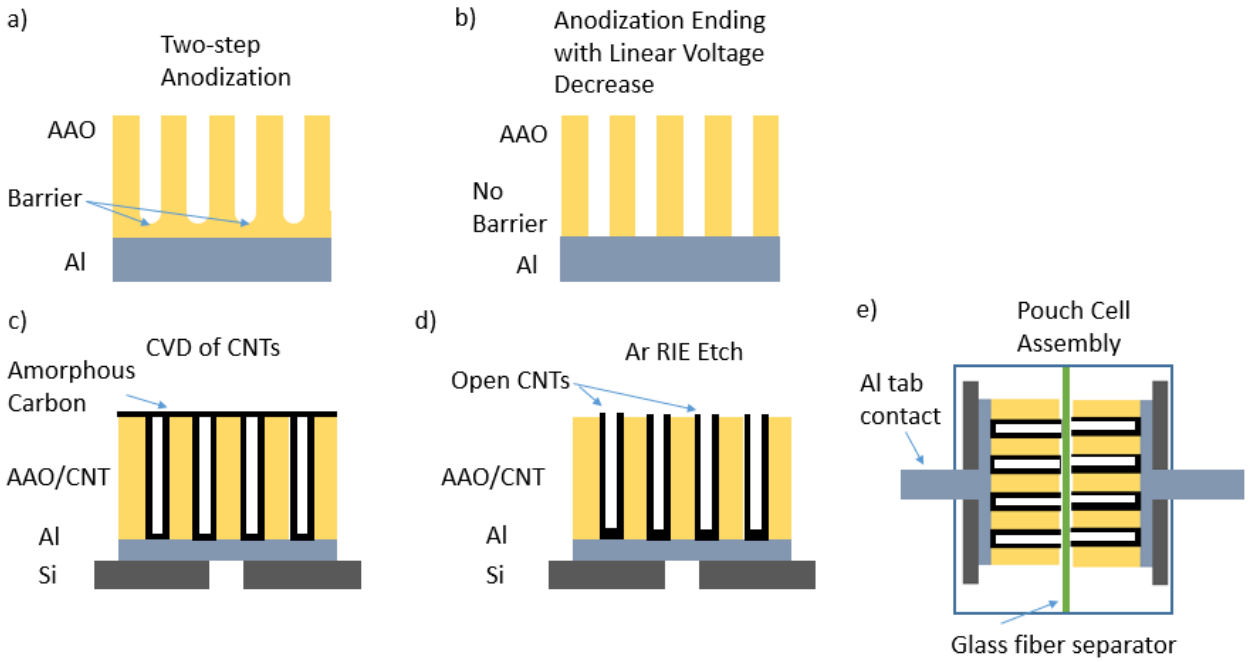


*Figure 1: Schematic showing the fabrication steps of a single CNT/AAO/Al/Si stack electrode including a) anodization, b) barrier layer removal through linear voltage decrease at the end of anodization, c) CVD of CNTs within AAO, d) RIE-ICP etching of amorphous carbon on the AAO surface, and e) pouch cell configuration.*

### *2.4 Electrochemical Testing*

The devices were tested through cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS), and galvanostatic charge-discharge (GCD) in order to measure capacitance, internal resistance, and cycling stability. Impedance analysis and cyclic voltammetry testing was performed on a VersaSTAT 3 potentiostat (Princeton Applied Research) and cycle stability testing was performed using an Arbin BT-2000 battery cell testing station.

### *2.5 Structure Characterization*

The microstructure of the AAO templates and structure of the CNTs were examined under SEM using a FEI Nova 430 FE-SEM. CNT/AAO/Al/Si composites and CNTs freed from the AAO template were examined using a FEI Tecnai F20 S/TEM. Plan-view TEM samples of the

AAO/CNT composite were made from cleaved cross-sections using a FEI Helios Nanolab 600 Dualbeam FIB/SEM. SEM and TEM images were analyzed using ImageJ software.

## 3. Results and discussion

SEM was performed on cross sections of a series of different anodization times to determine the growth rate of the AAO. Cross-sectional SEM allowed for the derivation of an empirical formula for AAO thickness given in Eq. (1) below. AAO thickness in μm is given as $t$ and charge passed during the anodization is given as $Q$ in units of coulombs. Eq. (1) was used to determine the thickness of the AAO in the EDLC under study (55.4 ± 1.4 μm thick), not directly imaged via SEM.

$$t = 0.134Q\,\frac{\mu m}{C} - 1.91\ \mu m \qquad (1)$$

AAO was successfully bonded onto Si wafers for AAO thicknesses between 20 and 130 μm seen in Fig. S2. The effect of the 650°C bonding treatment/CVD process on the pore structure was first explored. Harsher heat treatments of 1200°C have been shown to decrease pore ordering and increase pore diameter which is unwanted for controllable device performance [35].

Fig. 2a shows the top view of a representative AAO film with no heat treatment. The average pore diameter, $D_p$, based on 512 pores is 51 ± 11 nm. The average interpore spacing, $D_{int}$, is 92 ± 19 nm giving an average AAO wall thickness of 41 nm. The measured pore density is $9.9\times10^{9}$ $cm^{-2}$. These measurements are in the expected range for oxalic anodization at 40 V [36].

Fig. 2b shows the top surface of the AAO template which was bonded to the Si wafer after anodization. The bonding procedure was performed at 650°C for 6 h, the same as the CVD

process used to deposit CNTs but in this case without flowing $C_2H_2$ or $H_2$. The pores are unchanged from the as-anodized sample, with an average $D_p$ of 52 ± 8.5 nm over 2000 pores and an average $D_{int}$ of 90 ± 14 nm, giving a resulting AAO wall thickness of 38 nm. These measurements are well within the measurement error of the non-heat-treated AAO, indicating no or minimal pore widening.

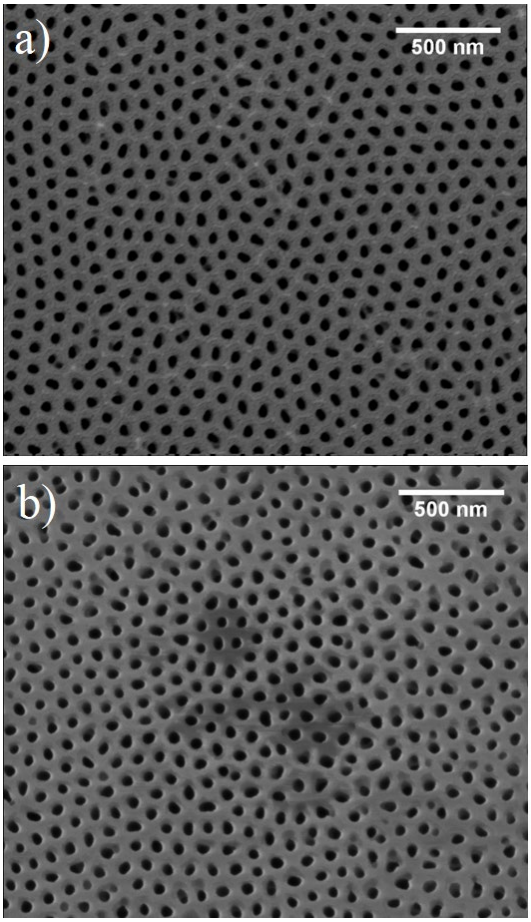


*Fig. 2: Top-down view of the AAO pores a) as-prepared and b) after bonding to Si at 650°C for 6 h under flowing Ar.*

The structure of the composite AAO/Al/Si stack after bonding for 6 h at 650°C under Ar is shown in Fig. 3a. This sample was anodized for 24 h and did not undergo any barrier layer thinning techniques. The result is a 90 µm thick AAO template, the thickest ever AAO reported on a Si wafer to our knowledge. The composite sample was cleaved to view the cross section, and the ductile Al is easily distinguishable between the brittle AAO and Si layers. Fig. 3b shows that the interior of the pore structure is unaffected by the heat treatment. Pores are straight with no aberrations. At the base of the pore is the barrier oxide layer, shown in Fig. 3c, which prevents electrical contact between the Al current collector and any materials deposited in the

AAO pores. The barrier oxide is unaffected by the bonding process, but it is effectively removed through a linear voltage decrease at the end of the 2nd anodization step (Fig. S1). This method allows CNTs to make direct electrical contact to the Al current collector in the pouch cell EDLC device.

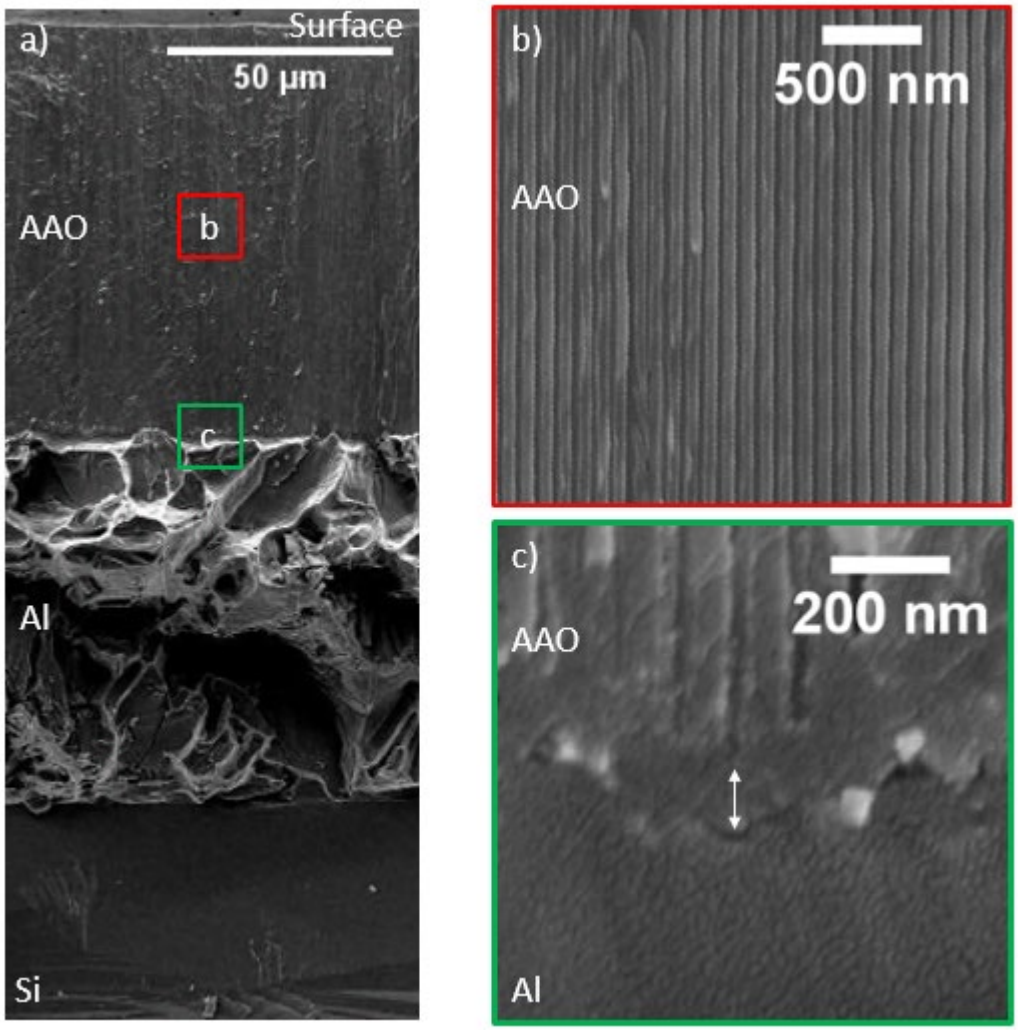


*Fig. 3: a) Cross section of the bonded stack showing AAO (top), Al (middle), and Si (bottom). Areas of interest are outlined and shown in higher magnification, demonstrating b) that the pore wall structure of the AAO is maintained after bonding and c) that the barrier oxide, highlighted with white arrow, is intact. For EDLC devices, the barrier layer for CNT/AAO/Al/Si electrodes is removed through a linear voltage decrease at the end of the second anodization step.*

Fig. 4 shows the interface between the Al and Si layers after annealing at 650°C for 6 h under Ar flow. There are three common microstructural features seen at the interface. In Fig. 4a,

Si is shown redepositing at the interface, forming Si islands similar to those seen in Al metallized contact holes in integrated circuits [37]. Due to the low solubility limit of Si in Al, slow cooling of the bonded structure can easily precipitate Si from the eutectic composition of 12.2% at. to the solid solubility limit of <1.2% at. at room temperature. Faster cooling rates can decrease the size of precipitates and could be explored to eliminate these plateaus [38]. Fig. 4a also shows large, hemispherical pits into the Si. These pits are the result of the liquid eutectic reaction between Al and Si and are commonly seen in Al contacted solar cells annealed above the eutectic point [26], [39]. Since the Al and Si used in this study was extremely pure, there are large concentration gradients for interdiffusion of Si and Al. However, the diffusion of Si is much faster into Al than vice versa, and this mismatch of diffusion coefficients (a.k.a. the Kirkendall effect) is thought to exacerbate the eutectic pitting seen in Fig. 4a. Replacing the pure Al with AlSi alloys could be explored to reduce the interdiffusion and eliminate such pitting. AlSi alloys have been used in the semiconductor industry at approximately 0.7% Si to combat similar pitting defects, and anodization of similar purity alloys has been shown to have minimal effect on the AAO structure [28], [40].

In Fig. 4b, a different microstructure is seen (note the difference in scale bars). The bonding interface is much more planar compared to Fig. 4a and there are small voids on the Al side of the interface. Voids may have been caused by mass transport during the bonding process, and the roughness of the rolled Al used in this study could also play a role in forming this structure. Roughness values obtained from profilometry are on the order of $R_a \sim 100$ nm for the Al, which is similar to the height of the voids seen in Fig. 4b. Due to this roughness, the Al and Si may not have been in as intimate contact as other regions leading to void formation. To provide more intimate contact between the Al and Si layers, the Al could be polished before

anodization through either chemical [41] or electrochemical [42] methods. These polishing methods were not employed in the present study but are known to decrease surface roughness by a factor of ~10. Additionally, deformation of the AAO/Al film may occur during the CNT deposition and lead to decreased bonding. Chang et al.[43] found that this deformation can be prevented through a hydrothermal treatment performed before heating. The hydrothermal treatment removes the anion contaminated inner layer of the AAO which the authors deemed responsible for the film deformation. Such a method may also be explored to improve the bonding character of the Al/Si interface. Overall, the Al film in the present study showed excellent bonding characteristics using the eutectic bonding process, with no signs of delamination and high structural integrity.

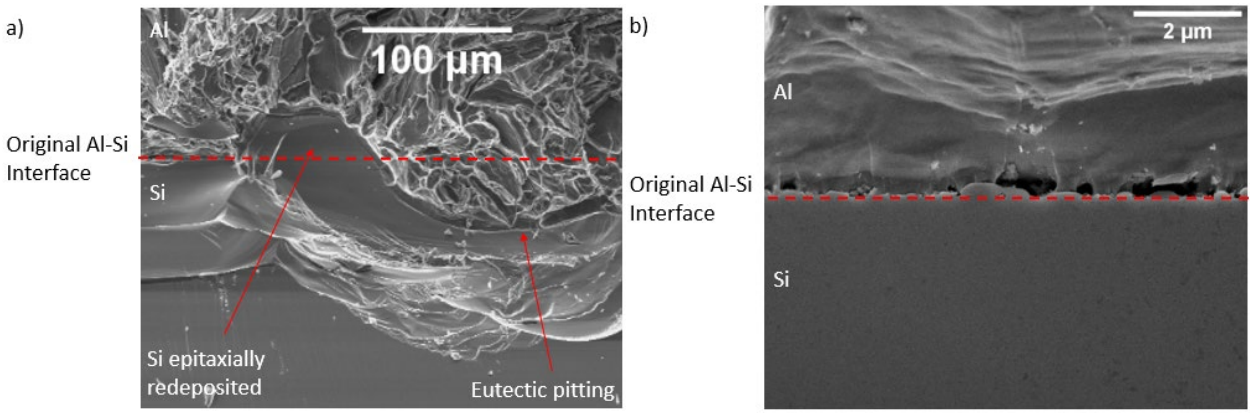


*Fig. 4: Resulting Al-Si interface after annealing at 650°C for 6 h. Dashed red line indicates the proposed original position of the interface. At lower magnifications a), islands of epitaxially regrown Si and Al-Si eutectic pits are seen along the interface. Higher magnification of some regions b) show the presence of voids which are believed to be caused by surface roughness of the Al leading to non-intimate contact during bonding, but which may also be the result of mass transfer during the bonding process.*

CNTs were grown inside the AAO by decomposition of $C_2H_2$ mixed with $H_2$ and Ar in a CVD tube furnace. Similar CVD methods have previously been used to grow CNTs in AAO, with the carbon being deposited through the full length of the AAO channel. In this way, controlling the AAO thickness effectively controls the length of deposited CNTs [44], [45]. Fig. 5 shows the resulting nanostructure from the single-step CNT deposition/Al-Si eutectic bonding.

Fig. 5a shows the top view of the AAO template filled with CNTs after an ICP-RIE etching step. The nanotubes are conformally grown in the template with an average pore diameter after growth of $D_p = 33 \pm 13$ nm. With an initial $D_p$ of 51 nm, the CNT wall thickness is determined to be 9 nm. Fig. 5b shows a cross section of the midpoint of the AAO template with CNTs inside, indicating that CNTs grow throughout the length of the entire template. Some tubes were pulled out of the template when it was fractured for SEM analysis, but the top view indicates that all AAO pores are lined with CNTs. Fig. 5c shows plan-view TEM of the CNTs within the AAO template. The CNTs can be seen as bright rings with slightly darker walls. Closest to the CNT outer walls is the "softened layer" of the AAO, which contains incorporated anions from the anodization and is less dense than pure $Al_2O_3$. The inner wall or "hard layer" of the AAO is clearly delineated as a sharp hexagon of relatively pure alumina [46]. Fig. 5d shows TEM of CNTs freed from the AAO template. Raman and TEM analysis in the literature has shown that low temperature CVD growth of CNTs in AAO produces mostly amorphous carbon with some degree of crystallinity[44], [47], [48]. Higher magnification images of our CNTs (not shown) show no signs of graphitic layers in the CNTs, indicating a high amorphous content. TEM images were used to corroborate the CNT wall thickness obtained from SEM. 10 measurements each of 15 distinct CNTs gave an average wall thickness of $9.4 \pm 2.8$ nm, in good agreement with the SEM analysis. The agreement between SEM and TEM analysis also indicates that tubes are formed evenly along the entire AAO pore and do not taper in either direction.

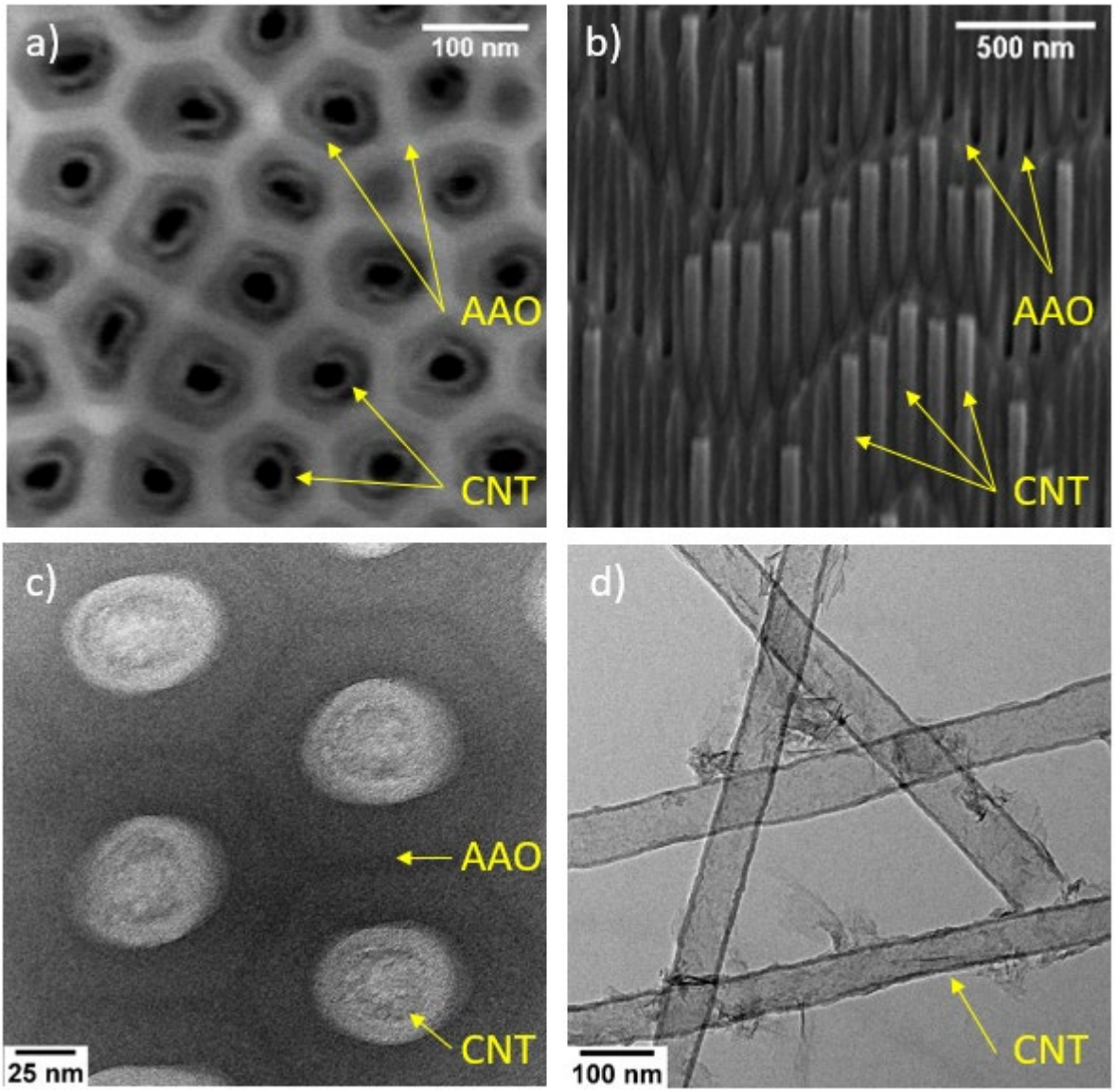


*Fig. 5: SEM images of CNTs deposited in the pores of AAO in a) top down view and b) side view. TEM of CNTs c) in AAO pores and d) freed from the AAO template.*

Pouch cell performance was measured through CV, GCD, and EIS. Using the anodization data and Eq. (1), the thickness of the AAO in the cells was determined to be 55 µm. Fig. 6 shows the Nyquist plot of the EIS scans for the device. The ohmic resistance taken as the high-frequency limit of the real part of the impedance is 5.4 Ω $cm^2$ showing that there is good electrical connection to the CNTs and that the barrier layer has been effectively removed. The slope of the impedance at low frequencies should be vertical (90°) for a purely capacitive

response [49]. The pouch cell gives a phase of 83° over the frequency window 1 – 0.1 Hz, indicating near ideal capacitive behavior. Higher frequency regions above 40 Hz show a phase angle close to 45°, which is expected due to the ordered porous structure of the electrode [50].

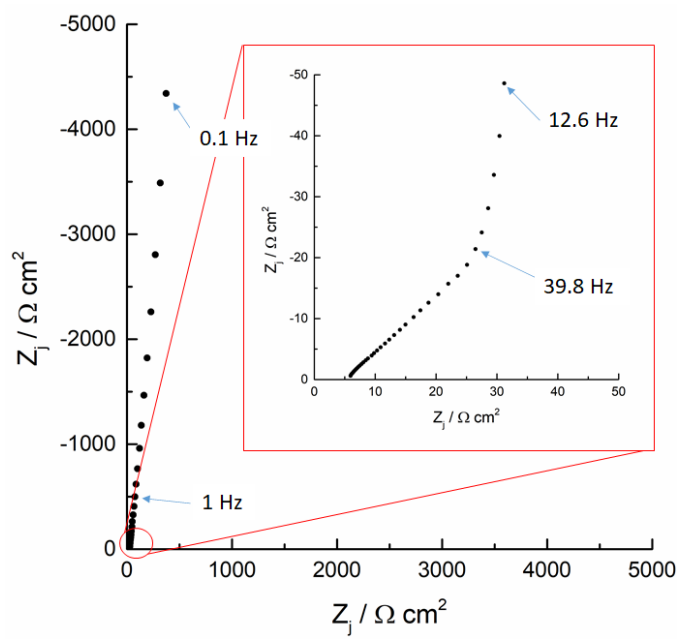


*Fig. 6: Nyquist plot of the pouch cell device from 100 kHz to 100 mHz. Inset highlights the high frequency region from 100 kHz to 12 Hz with a knee frequency at 39.8 Hz.*

Fig. 7 shows the CV response of the 55 µm thick AAO cell. The CV curve shows no peaks or valleys related to redox reactions [51]. The shape is nearly rectangular, ideal for such an EDLC device, and the current transient at the switching potential is sharp. Specific capacitance was calculated using Eq. (2),

$$C = \frac{\int_{V_1}^{V_2} di\, dV}{Av\Delta V} \qquad (2)$$

where $\int di\, dV$ is the integrated current with respect to voltage, $V_1$ and $V_2$ are the switching voltages in the CV scan, $A$ is the footprint area, $v$ is the sweep rate, and $\Delta V$ is the voltage window. The capacitance calculated from the CV curves is shown in Fig. 7b, decreasing from

0.44 mF $cm^{-2}$ at 10 mV $s^{-1}$ to 0.36 mF $cm^{-2}$ at 500 mV $s^{-1}$. The capacitance decreased only 18% over more than an order of magnitude increase in sweep rate, indicating that similar devices are suitable for the high power, short duration pulses expected for SOC charging. On-chip, carbon-based EDLCs have previously been demonstrated by pyrolyzing photoresist on Si wafers. These devices have shown capacitances between 1.5 and 6 mF $cm^{-2}$ using aqueous electrolytes[52], [53]. Greater capacitance has been shown in on-chip devices combining pseudocapacitive materials such as $RuO_2$ or $MnO_2$[54], [55] which may be an approach to further improving these devices.

Based on the density and radius of the pores and the thickness of the AAO template, the surface area of the CNTs per Si footprint is calculated to be 613 $cm^2$ $cm^{-2}$. Normalizing the total capacitance measured with CV (1.26 mF) to the internal area of the CNTs gives a value of 0.73 ± 0.29 μF $cm^{-2}$. Standard deviation was determined through propagation of error [56] in pore size, template length, potentiostat sensitivity, etc. Commonly, a value of 20 μF $cm^{-2}$ is used to discuss double layer capacitance[57]. It is important to note that this value is determined for an ideal system of a mercury drop electrode in an aqueous electrolyte. The specific capacitance can be changed drastically based on the electrode and electrolyte used, and our results are comparable to similar systems. Ahn et al.[9] fabricated CNT/AAO capacitors with *no* Si substrate and measured a capacitances of 2.7 and 3.1 μF $cm^{-2}$ in 0.5 M $H_2SO_4$ of two devices using different anodization conditions. Zhan et al.[58] also made AAO/CNT capacitors with *no* Si substrate and measured a capacitance of 2.4 μF $cm^{-2}$ in 1 mM ferrocyanide and 0.1 M KCl electrolyte. Balducci et al. reported a capacitance of 1.3 μF $cm^{-2}$ based on GCD at 10 mA $cm^{-2}$ for activated carbon capacitors in neat ionic liquid [59]. Shim et al. simulated single walled carbon nanotubes in

ionic liquid [60] and reported capacitance values of 1-3 μF $cm^{-2}$. Our value of specific capacitance is then very close to previously reported data.

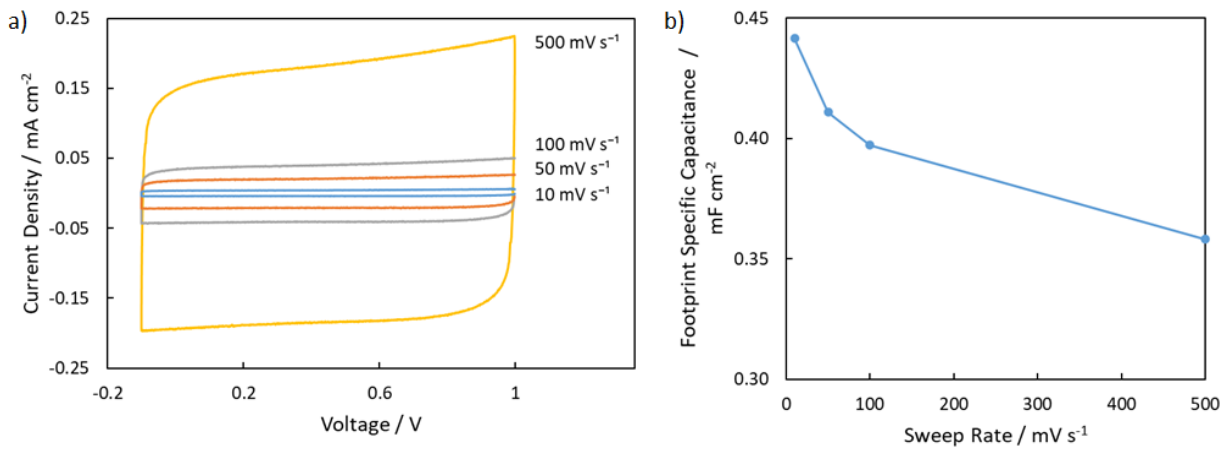


*Fig. 7: a) CV response at sweep rates between 10 and 500 mV $s^{-1}$ and b) corresponding capacitance of the pouch cell device.*

Fig. 8a shows the GCD measurements for the cell cycled 1000 times at 17.5 μA $cm^{-2}$ and another 1000 times at 1.75 μA $cm^{-2}$ between -0.1 and 1.0 V. The 55 μm cell suffered minimal fade in discharge energy over the first 1000 cycles at 17.5 μA $cm^{-2}$, falling by just 1%. The fade was slightly more drastic at lower charge rates, falling by 10% of the first cycle after all 2000 cycles. The charging efficiency given in Fig. 8b was much better for the higher charge rate, with an average of 87% compared to an average of 69% efficiency for the 1.75 μA $cm^{-2}$ rate. Fig. 8c shows a single GCD cycle at each current density over the actual cycle time and Fig. 8d shows the same scans plotted against normalized cycle time. Both show a triangular response expected from a capacitor device. The triangular shape is somewhat more distorted at lower current density, indicating imperfect capacitive behavior. The lower charge rate cycle shows a change in slope near 0.7 V during charging. This slope change is not mirrored in the discharge curve, suggesting the presence of a parasitic irreversible reaction at the electrode surface. In comparison, the high rate cycle does not show a significant change in slope at high potentials,

indicating that the kinetics of the reaction are relatively slow. At slow rates, a non-negligible portion of the charging current is siphoned into the parasitic reaction and cannot be retrieved during discharge, decreasing discharge efficiency as seen in Fig. 8b. At higher charge rates, this slow reaction has less effect on the charge efficiency. The greater fade at lower charge rates is further evidence that some impurities on the electrode surface were consumed during cycling. We believe that this parasitic reaction is most likely the result of surface functional groups on the CNT walls generated during the somewhat low temperature of the CVD reaction[61], [62]. Further study into reducing such parasitic reactions might explore removing these surface groups through appropriate anneals or chemical reactions. The GCD results indicate that thick AAO films are suitable for large current transients which might be expected from intermittent energy harvesting sources on self-sustaining SOCs [4].

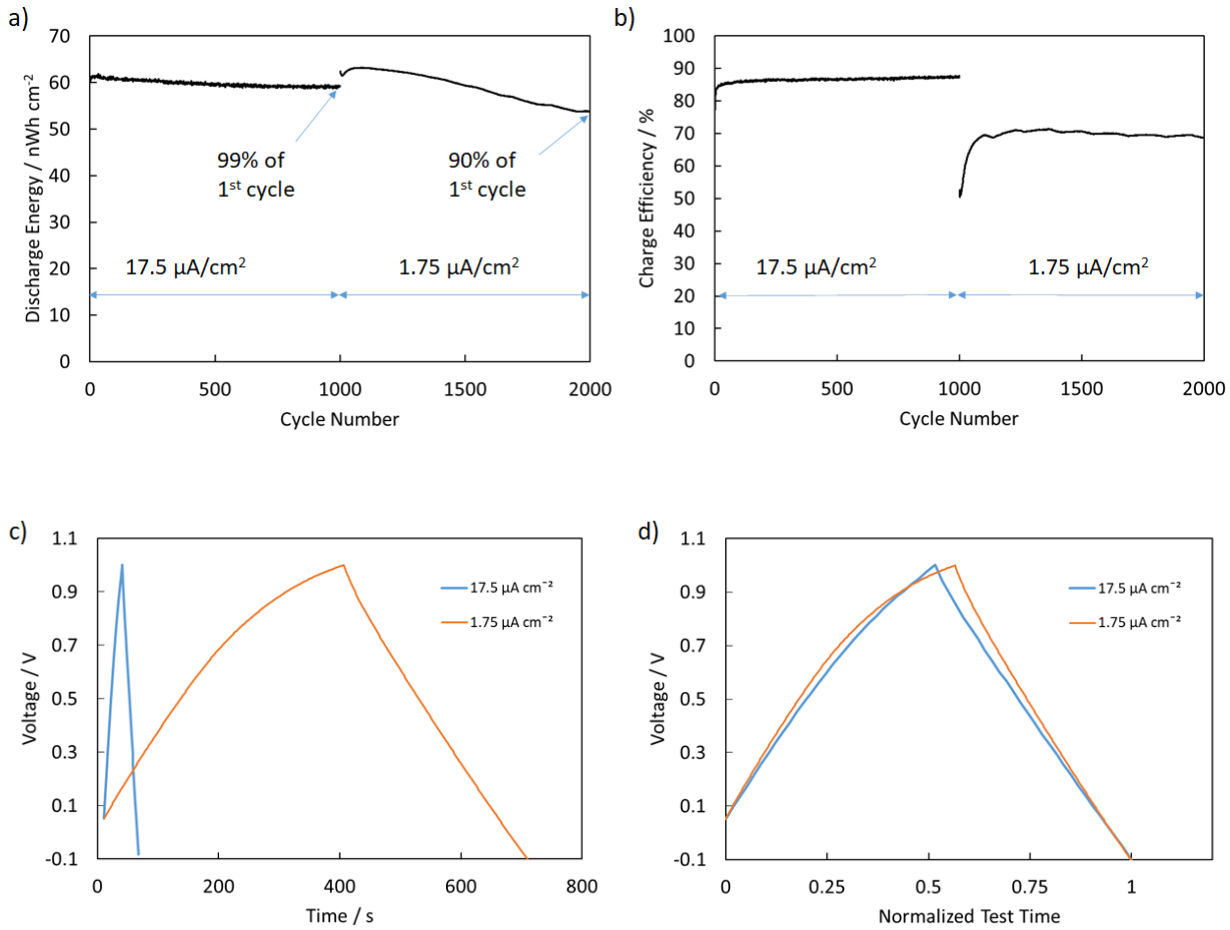


*Fig. 8: GCD of the pouch cell device of 1000 cycles each at 17.5 and 1.75 µA cm$^{-2}$. a) Discharge energy from 1 to -0.1 V and b) charging efficiency based on charge and discharge energy. c) An individual GCD scan at each current density and d) individual GCD curves based on normalized cycle time.*

## Conclusions

Thick AAO templates were bonded to Si wafers using a simple single step eutectic bonding method which had no impact on the AAO structure. The bonding interface between the Si and Al displays some defects including Si islands, eutectic pits, and void content, but the AAO/Al/Si stack is physically robust with the AAO firmly attached to the Si. Importantly, electrical connection can be made to materials deposited in the AAO pores via the underlying Al. CNTs deposited in bonded AAO templates were used to create pouch cell EDLCs with a

capacitance as high as 0.44 mF $cm^{-2}$, more than two orders of magnitude higher than previously reported electrostatic AAO-on-Si capacitors. The eutectic bonding approach enables the fabrication of very thick AAO films on Si that can drastically increase the active loading of vertically-aligned 1-D nanostructures and opens the door for enhanced performance in SOC devices.

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**Appendix A. Supplementary data**

Supplementary data has been included as a separate file.

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