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TECHNICAL REPORT

Basic Single-Event and Total-Ionizing Dose Mechanisms in Ge/InGaAs-based CMOS Transistors with ALD High-k Dielectric

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14. ABSTRACT

Objective of this work was to determine, using theory and experiments, the basic mechanisms of single-event and total ionizing dose effects in InGaAs and Ge/Si heterostructure MOSFETs with high-k dielectrics/metal gate. We established understanding of radiation-induced charge transport and collection mechanisms on the structure and composition of nanoelectronic Ge and InGaAs FETs on Si, and, on the nature of the ionizing species by modeling/designing devices, fabricating MOS test structures, and testing their electrical behavior under radiation exposure.

15. SUBJECT TERMS

High-k dielectrics/metal gate Ge and InGaAs based heterostructure transistors. Radiation-induced charge transport and collection mechanisms. Basic mechanisms of total ionizing dose effects and single-event effects.

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PI Name: Krishna Saraswat
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Project Title: Basic Single-Event and Total-Ionizing Dose Mechanisms in Ge/InGaAs-based CMOS Transistors with ALD High-k Dielectric

What are the major goals of the project?

List the major goals of the project as stated in the approved application or as approved by the agency. If the application lists milestones/target dates for important activities or phases of the project, identify these dates and show actual completion dates or the percentage of completion. Generally, the goals will not change from one reporting period to the next. However, if the awarding agency approved changes to the goals during the reporting period, list the revised goals and objectives. Also explain any significant changes in approach or methods from the agency approved application or plan.

OBJECTIVE. Ultra high speed, ultra low-power FETs based on Ge PMOS and InGaAs NMOS with a high-κ dielectric gate will play a key role in future generation terrestrial, space and electronic warfare (EW) systems. While the device technology development is moving forward at a rapid pace, little is understood about the performance of these technologies in hostile environments. The basic research program, HDTRA1-14-1-0036, is a joint collaborative research program between Stanford, Notre Dame, and the Naval Research Laboratory. The objective of this joint program is *to determine, using theory and experiments, the basic mechanisms of total ionizing dose effects and single-event effects in Ge and InGaAs based heterostructure transistors with integrated high-κ dielectrics/metal gate.* We will also establish a fundamental understanding of how the radiation-induced charge transport and collection mechanisms are modified by the tuning of the heterostructure composition and the electrical quality of the interface, and, finally, the nature of the ionizing species. We will accomplish these objectives by iteratively modeling and designing the device structures, synthesizing such structures, fabricating MOS-capacitors and 3D MOSFET/FinFET test structures, and testing their electrical behavior under radiation exposure. Specifically, we will utilize vacuum ultraviolet, and gamma-ray exposure to systematically study total ionizing dose (TID) effects and an ultrafast laser to inject charge into precise locations in the device to study single event effects (SEEs). Location and density controlled defect generation within the high-κ and the channel regions of the structures, accomplished using ultra-low energy ion implantation, will be used in conjunction with systematic TID studies to elucidate the role of defects and interstitial species within the novel materials stacks.

At the end of the proposed two year option period, the specific outcome of this program will be:

(i) establish the experimental and theoretical knowledge base of the primary events associated with response of high-κ gated *3D* Ge PMOS and InGaAs NMOS transistors to radiation,

(ii) establish a solid, experimentally-validated theoretical foundation that quantitatively captures the non-equilibrium transport of ionization-induced carriers in advanced 3D Ge PMOS and InGaAs NMOS transistors,

(iii) extend the calibrated theoretical model to circuit level assessment of 3D Ge PMOS and InGaAs NMOS nanoscale transistors technology for a range of ultra-low power digital and analog applications.

Summary of Goals:

Time	Tasks
	•
Year 1	• Bandstructure modeling using k.p perturbation theory and InP/InxGa1-xAs -heterostructure redesign varying x from 0.53 to 0.70 to understand tradeoff between performance and radiation immunity (PSU) • Bandstructure modeling using virtual crystal approximation within the framework of the nonlocal empirical pseudopotential method and GeSn and Si/Ge -heterostructure redesign to understand tradeoff between performance and radiation immunity (Stanford). • Optimization of selective heteroepitaxial growth of Ge and GeSn on Si (Stanford) • Ungated and gated Hall transport measurements on InP/InxGa1-xAs, Ge and Si/Ge heterostructures (Stanford, PSU) • Fabrication and characterization of MOS capacitors with various high-k gate stacks on InP/In.53Ga.47As epitaxially grown on both InP and silicon substrates (PSU) and with various high-k gate stacks with and without fluorination on Ge and Si/Ge-heterostructures epitaxially grown on Si substrate (Stanford) • TID (Co-60) Characterization of MOS-Capacitor Test Structures (Metal/high-k/[Ge and InGaAs]) (NRL) (critical parameters include flat band voltage shift and interface state density, Dit, as a function of energetic location)
Year 2	• Fabrication and characterization of MOSFETs with various high-k gate stacks on InP/In.53Ga.47As heterostructure epitaxially grown on Si substrate (PSU) and with various high-k gate stacks with and without fluorination on Ge, and Si/Ge-heterostructures epitaxially grown on Si substrate. (Stanford) • Fabrication and characterization of MOS capacitors with various high-k gate stacks GeSn-heterostructures epitaxially grown on Si substrate. (Stanford) • TID (Co-60) Characterization of Ge and In.53Ga.47As MOSFET characteristics pre and post radiation (leakage, threshold voltage, transconductance, on-current) and compare with parametric shifts obtained using MOSCAPs in Year 1 (NRL) • Develop high-speed packaging/bonding and initiate L-SEE testing of MOSFETs using pulsed laser
Year 3	• Fabrication and characterization of ultrathin body nanoscale MOSFETs with optimized high-k gate stacks on InP/InxGa1-xAs heterostructure grown on Si substrate (PSU) and on Ge, GeSn, and Si/Ge-heterostructure grown on Si substrate (Stanford). • Characterization of MOS capacitors and MOSFETs pre and post radiation, modeling of LET in heterostructures, single transient event simulation in SRAM and Logic circuits (PSU) • Continue TID / SEE testing, with systematic introduction of displacement damage using low-energy ion implantation.

	• Neutron testing (Penn State Breazeale Reactor) on Stanford fabricated Si/Ge heterostucture FETs with optimized gate stack and on Penn State fabricated InP/InGaAs heterostructure FETs with optimized gate stack • Include Heavy Ion testing and correlate with laser SEE testing (done at heavy ion facility, TBD).
Option Year 1	• Transport measurements on redesigned and radiation tolerant n-channel InGaAs (Notre Dame) and p-channel Ge-heterostructures (Stanford) • TID (total ionizing dose) and DD (displacement damage) measurements on n- and p-channel InGaAs and Ge MOSCAPs with new *in-situ* gate dielectric (NRL) • Fabrication and Characterization of n-channel InGaAs (Notre Dame) and p-channel Ge (Stanford) MOSFETs with varying gate length/source drain spacing • Pulsed Laser and Heavy-ion induced time resolved, charge collection measurements (NRL) • Characterization and data analysis of irradiated n-channel InGaAs and p-channel Ge MOSFETs (NRL, Stanford and Notre Dame) • Device-level modeling and comparison with experiments (NRL, Stanford and Notre Dame)
Option Year 2 (not executed)	• Redesign and transport measurement on n-channel InGaAs (Notre Dame) and p-channel Ge MOSFETs (Stanford). • Fabrication and Characterization of advanced nanoscale 3D n-channel InGaAs (Notre Dame) and p-channel Ge MOSFETs (Stanford) • Pulsed Laser and Heavy-ion time resolved, charge collection measurements (NRL) • Characterization and data analysis of irradiated n-channel InGaAs and p-channel Ge MOSFETs (NRL, Stanford and Notre Dame) • Device level modeling and comparison with experiments (NRL, Stanford and Notre Dame) • Logic level abstraction and assessing soft error vulnerability using calibrated device level radiation response models (Notre Dame) • Final report (Stanford, Notre Dame and NRL)

What was accomplished under these goals?

For this reporting period describe: 1) major activities; 2) specific objectives; 3) significant results, including major findings, developments, or conclusions (both positive and negative); and 4) key outcomes or other achievements. Include a discussion of stated goals not met. As the project progresses, the emphasis in reporting in this section should shift from reporting activities to reporting accomplishments.

Year 1

Task 1: Band structure modeling and heterostructure redesign:

1.1 $In_xGa_{1-x}As$

Higher on state current (I_{ON}) and transconductance (g_m) with increasing indium percentage (In%) have been demonstrated in planar $In_xGa_{1-x}As$ HEMTs [1]. However in Fin-FET structures, the benefit of increasing indium percentage is not as straightforward, due to the additional quantum confinement imposed by fin patterning and the lack of conduction along the entire height of the fin. We have studied in detail, electron transport and electron density per fin in $In_xGa_{1-x}As$ Fin-FET structures. Fig. 1.1 shows the $In_xGa_{1-x}As$ Fin-FET structures that were studied with varied Indium percentages. The Fin-FET structures were fabricated using Molecular Beam Epitaxy (MBE) to grow varied $In_xGa_{1-x}As$ layers on InP substrates. Common to all devices structures was an $In_{0.52}Al_{0.48}As$ buffer layer on which was grown the varied $In_xGa_{1-x}As$ layers. To provide lower contact resistance n++cap layers were used to enable raised source and drain regions InP cap was used for to define the source drain regions. To define the raised source/drain regions, these n++ cap regions were etched with a citric acid based wet etch, which is selective to InP.

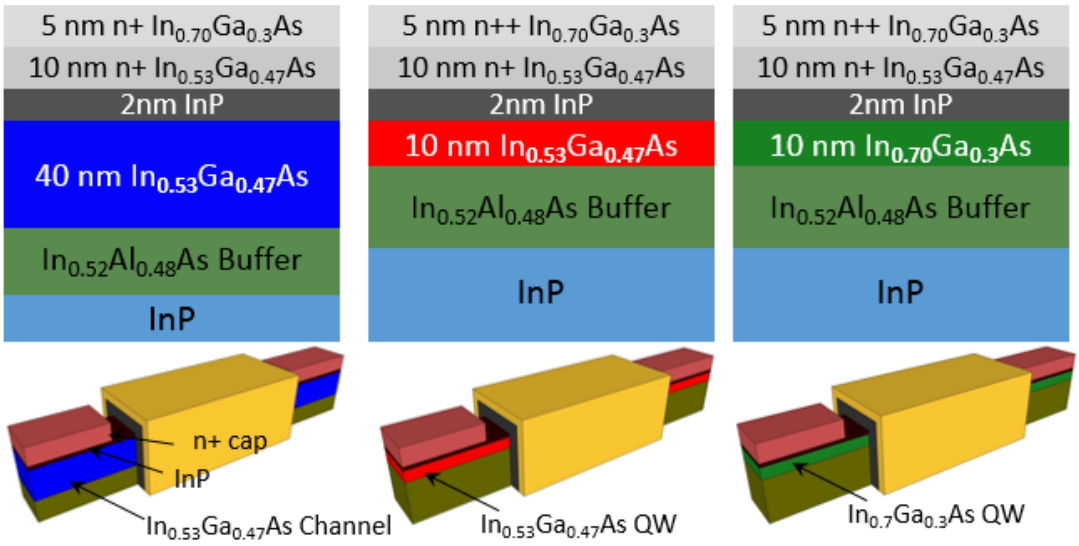
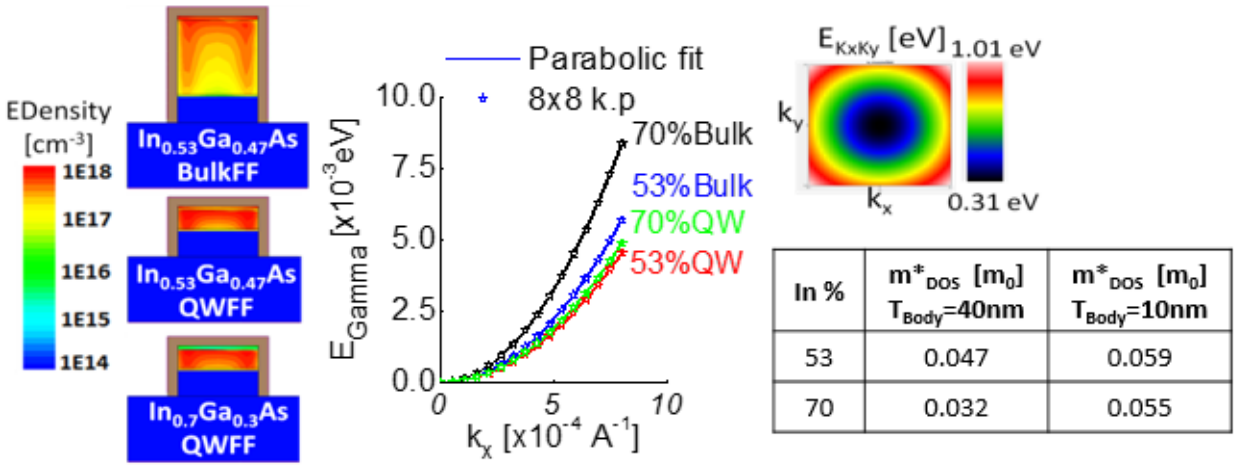


Fig. 1.1: Schematics of the $In_xGa_{1-x}As$ Fin-FET structures. $In_{0.53}Ga_{0.47}As$ and $In_{0.70}Ga_{0.3}As$ thin body (T_{body}=10nm) and thick body (T_{body}=40nm)

Fin-FET structures were studied using 8x8 k.p band structure (Fig 1.2) Parabolic fit of the 8x8 k.p band structure gives the effective electron mass, m_e^*. Increasing the In% leads to a decrease in m^*_{DOS} for thick body (bulk) and thin body (QW) $In_xGa_{1-x}As$ structures resulting in higher mobility.



In %	m^*_{DOS} [m_0] T_{Body}=40nm	m^*_{DOS} [m_0] T_{Body}=10nm
53	0.047	0.059
70	0.032	0.055

Fig. 1.2: (a) Electron density profile in Fin x-section showing surface conduction for $In_{0.53}Ga_{0.47}As$ Bulk Fin-FETs vs. volume conduction for QW. (b) Parabolic fit of 8x8 k.p band structure gives lower effective electron mass, m_e* for $In_{0.70}Ga_{0.3}As$ QW and $In_{0.53}Ga_{0.47}As$ QW

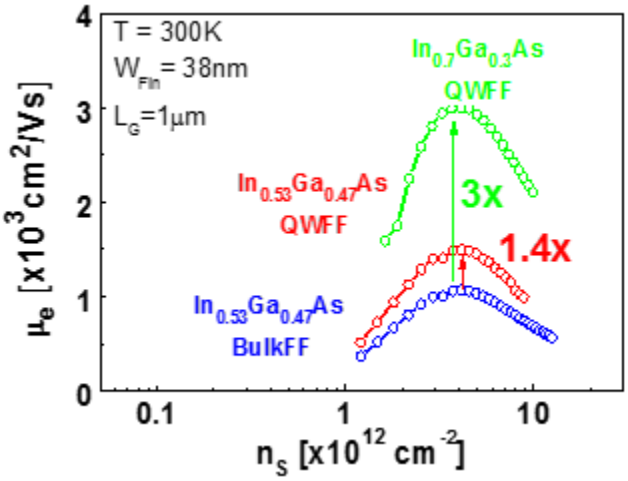


Fig. 1.3 Effective mobility extracted from $In_xGa_{1-x}As$ Fin-FETs with varied In percentages.

Experimental effective field mobility was extracted from split CV measurements on W_{Fin}=38 $In_xGa_{1-x}As$ Fin-FETs with varied In% (Fig 1.3). The experimental effective field mobility shows that increasing In% leads to an increase in the effective mobility of Fin-FET structures. $In_{0.7}Ga_{0.3}As$ QW Fin-FETs show the highest experimental effective mobility near 3000 cm^2/Vs, 3X greater than the effective mobility for $In_{0.53}Ga_{0.47}As$ Bulk Fin-FETs.

References:

[1] D. H. Kim et al, "50-nm E-mode In0.7Ga0.3As PHEMTs on 100-mm InP substrate with f_{max} > 1 THz" 2010 IEEE International Electron Devices Meeting (IEDM), 2010

1.2 Ge/GeSn

It has been found that local (LDA) and semi-local generalized gradient approximation (GGA) tend to severely underestimate energy gaps in Ge and Sn. These standard approximations for

exchange-correlation delocalize the electron density over the entire crystal such that each electron experiences an average of the coulombic potential. For highly correlated materials, the large coulombic repulsion between localized electrons might not be well represented by a functional such as the LDA or GGA. As a result, LDA/GGA fails to capture the orbital dependence of the coulomb interactions. A way to avoid this problem is to add a localized term to the density functional. This approach is known as LDA/GGA+*U*. The electronic structure of Ge, Sn and GeSn are calculated using density functional theory (DFT) as implemented in the Vienna Ab Initio Simulation Package (VASP). Next, the DFT- GGA+*U* method is extended for calculating the properties of substitutional GeSn alloy.

The electronic properties Ge had been modeled in our previous work in detail. In this work the electronic properties GeSn alloy were examined through first principles and empirical methods. Electronic band structure and effective masses in relaxed and strained germanium-tin (GeSn) alloys is calculated using virtual crystal approximation (VCA) within the framework of the nonlocal empirical pseudopotential method (NL-EPM). Application of corrections to the virtual crystal potential in order to account for the large lattice mismatch between Ge and Sn was shown to reproduce band gaps in agreement with experiments. The calculated electronic band structures of the relaxed GeSn alloy with 3% and 6% Sn are shown in Figure 1.4. Figure 1.5 shows band gap at high symmetry points in the brillouin zone for GeSn alloys using VCA corrected for alloy compositional and structural disorder.

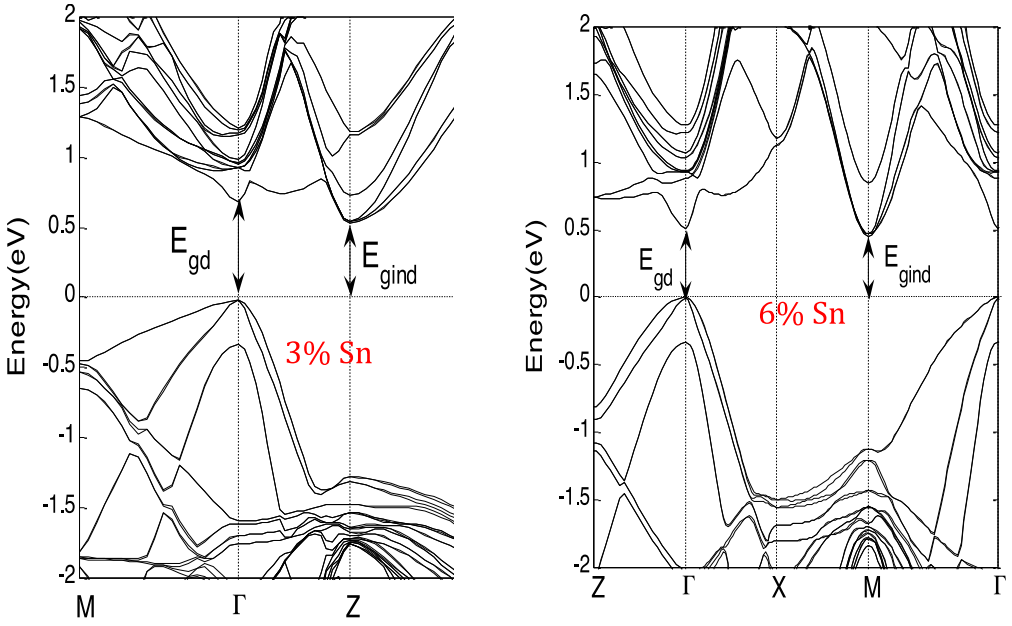


Figure 1.4: Band structure of GeSn showing the direct and the indirect band gaps for 3% and 6% Sn.

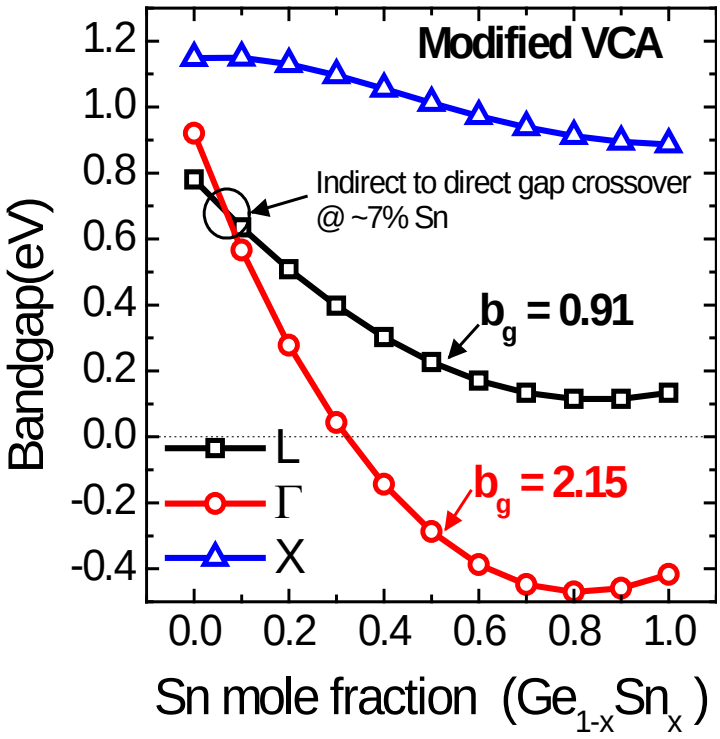


Fig. 1.5. Bandgap at critical points for GeSn alloys using VCA corrected for alloy compositional and structural disorder.

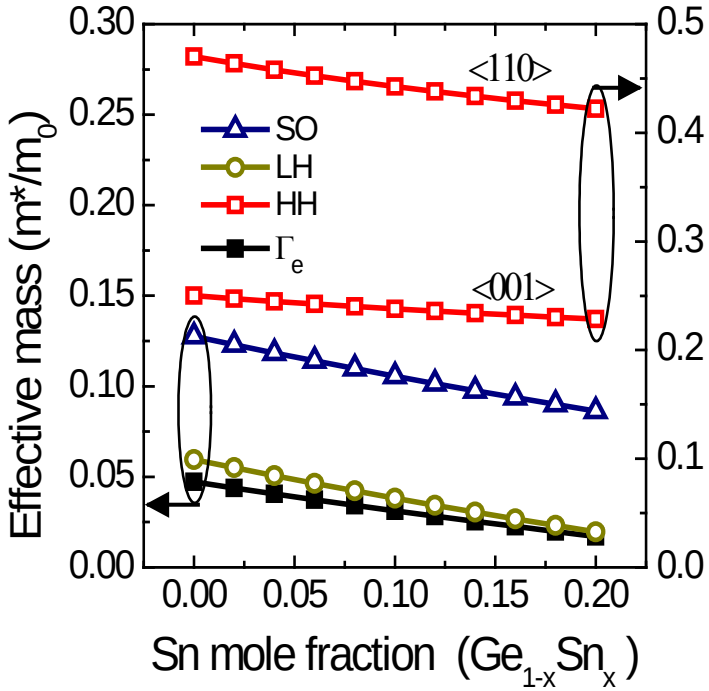


Fig. 1.6. Calculated electron and hole effective masses at Γ point as a function of Sn composition in GeSn

From k.p perturbation theory one can arrive at the conclusion that the effective mass of light hole and Γ electrons is proportional to the direct energy gap. A similar trend is observed in our simulation results. As the Sn content in GeSn increases, effective masses at Γ point decreases for both electrons and holes as shown in Figure 1.6. Interestingly, electron effective masses in GeSn at the satellite L and Δ conduction valley minima are found to be practically unchanged from those in Ge.

Population of valleys with low effective mass in the transport direction results in increase in the source injection velocity V_{inj} and the ballistic drive current of the device. As shown in Figure 1.7, for direct gap GeSn (Sn > 7%) increased population of Γ valley boosts V_{inj}. For both direct gap (10% Sn) and indirect gap (6% Sn) GeSn, increase in L-Δ energy gap inhibits Δ valley occupancy at large gate voltages and prevents the V_{inj} degradation seen in Ge. Thus, improvement over Ge nMOSFETs in terms of electron V_{inj} (or equivalently, ballistic drive current) can be expected for GeSn channel nMOSFETs throughout the operating gate voltage range.

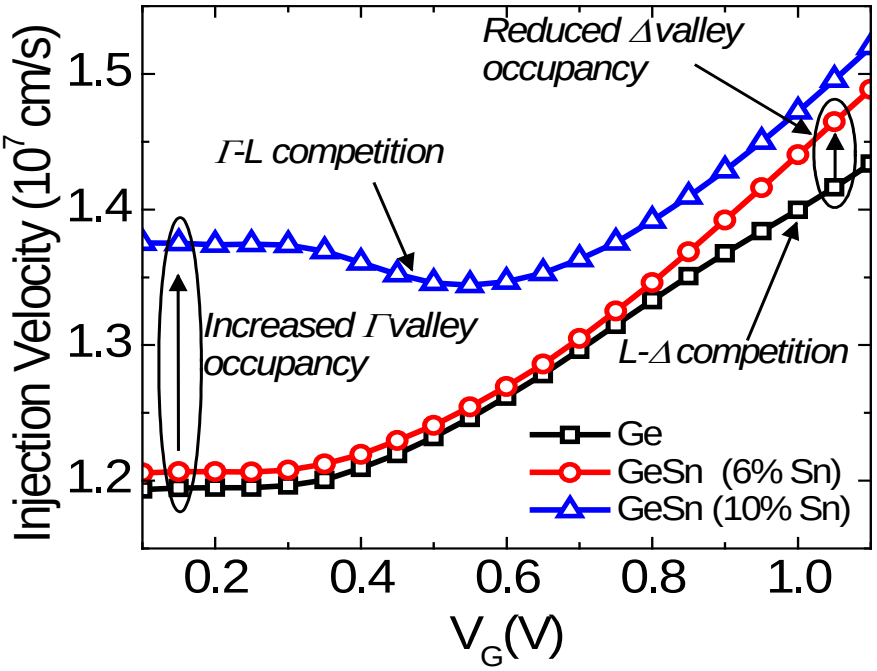


Fig. 1.7. Comparison of source injection velocity (V_{inj}) double gate nMOSFETs with Ge, unstrained GeSn (6%Sn, 10%Sn) channel

In our proposed CMOS design, the p-channel transistors are compressively strained and composed of GeSn (4% Sn) as the channel and boron-doped GeSn (8% Sn) as the S/D stressors. Likewise, the tensile-strained nMOSFETs are formed by a Ge channel and phosphorus-doped $Si_{0.3}Ge_{0.7}$ S/D. Both n and pMOSFETs utilize a common buffer layer which is lattice matched to Ge. Process simulations of the standard gate-last process flow with *in-situ* doped epitaxial re-growth of S/D regions and fin dimension expected in a 7 nm technology node reveals the average longitudinal stress in pMOSFET (nMOSFET) to be -1 GPa (+1 GPa). The drive current (I_D) in the ballistic limit for the proposed CMOS design is compared with strained-Si CMOS in Fig. 1.8 (b) and (c). Results shown here take into account the effect of parasitic source/drain resistance in the FinFET. The channel to S/D spreading resistance, doped S/D sheet resistance and contact resistance are

lumped into a single parameter – source resistance R_S. Note that total source/drain parasitic resistance, $R_{ext} = 2R_S$.

The transistor off-current is a critical design metric. In small band gap materials Ge and GeSn, drain band-to-band-tunneling (BTBT) leakage is an important concern. Additionally, the stress-induced band gap shrinkage in Ge and GeSn may exacerbate this problem. However, for the fin dimensions in the 7 nm technology node, strong quantum confinement effect in the channel causes an increase in the effective channel band gap 'E_G'. For a channel stress of ±1GPa and 6 nm fin width, a net increase in E_G as compared with unstrained, bulk material is observed as shown in Fig. 1.9(a). This increase in E_G is essential in reducing the BTBT leakage. Note that quantum confinement and channel stress have opposite effect on E_G. The increase in E_G due to confinement partly offsets the stress-induced reduction in the E_G.

For the Ge/GeSn CMOS, the simulated I_D-V_G characteristics shown in Fig. 1.9(b) indicate that the BTBT-limited I_{OFF} stays below the ITRS requirement for both high performance (100nA/μm) and low standby power (10nA/μm) technology at a supply voltage of 0.7V. Continued scaling beyond 7 nm entails further reduction in fin width. The resulting enhancement of the confinement effect provides the additional E_G bandwidth for incorporating larger stress in the channel, boosting the I_{ON} at the same I_{OFF}. Thus, the design proposed here illuminates a clear path for further technology scaling.

Note that several combinations of S/D and channel materials may be contemplated depending upon the application requirements and practical constraints and the CMOS solution presented here represents an exemplary demonstration of the band gap and stress engineering capabilities of group IV elements – Si, Ge and Sn. Furthermore, a practical realization of the Ge/GeSn CMOS design is contingent upon a successful implementation of several underlying technologies. In addition to the daunting process complexities involved in FinFET fabrication at the 7 nm technology node, the use of Ge and GeSn as channel materials introduces unique challenges which need to be addressed to preserve the feasibility of the proposed design. The low solid solubility (< 1%) of Sn in Ge, SiGe and the resulting metastability of supersaturated solid solutions of Sn with Ge and SiGe raises concerns over the synthesis and subsequent processing of Sn-based group IV alloys. A comprehensive study of the effect of strain and Sn composition on the maximum allowable thermal budget can greatly help in designing processes for GeSn device fabrication.

The presence of large number of density of trap states at the high-κ/semiconductor interface is known to degrade subthreshold behavior, cause threshold voltage instability and reduce the device drive current. The results presented in Task 3 represent a significant progress in achieving superior quality high-κ/Ge and high-κ/GeSn interfaces. Extending these methods to non-planar devices and arbitrary surface orientations forms an important module in Ge, GeSn FinFET fabrication. Lastly, the mitigation of parasitic source/drain resistance is necessary to obtain high drive current and a large S/D resistance may potentially erode the benefits of replacing strained-Si with Ge and GeSn as channel materials. Low-temperature (< 450 ºC) epitaxial growth methods that achieve selective area deposition of highly doped SiGe and GeSn are critical modules in the scaled FinFET CMOS technology. Nevertheless, these challenges in low-temperature, selective epitaxy of SiGe:P and GeSn:B provide interesting avenues for further research.

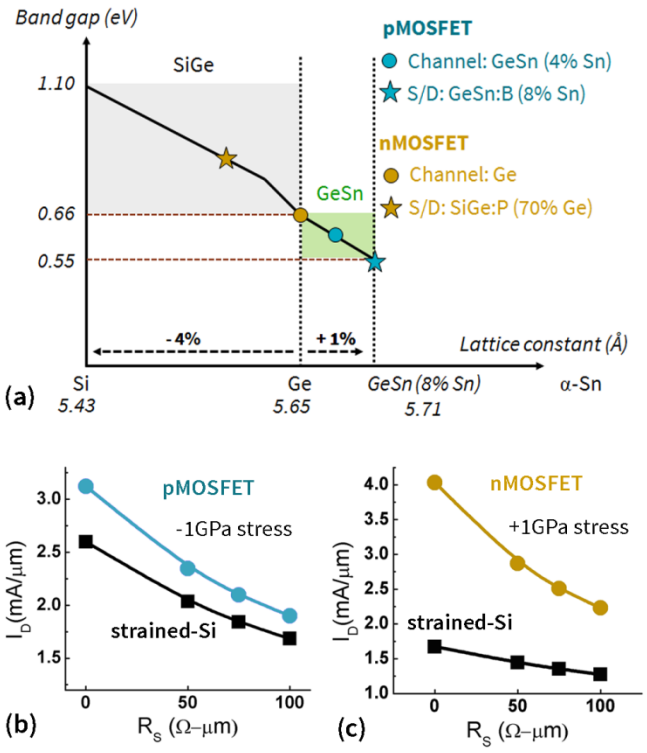


Fig. 1.8 (a) Band gap versus lattice constant for the group IV materials: Si, SiGe, Ge and GeSn. Practical constraints limit the maximum concentration of Sn to 8%. The plot also shows the material choices for the CMOS design under consideration. Simulations comparing the ballistic saturation I_D for (b) strained-Si and GeSn (4% Sn) pMOSFET, (c) strained-Si and Ge nMOSFET as a function of the parasitic source resistance R_S.

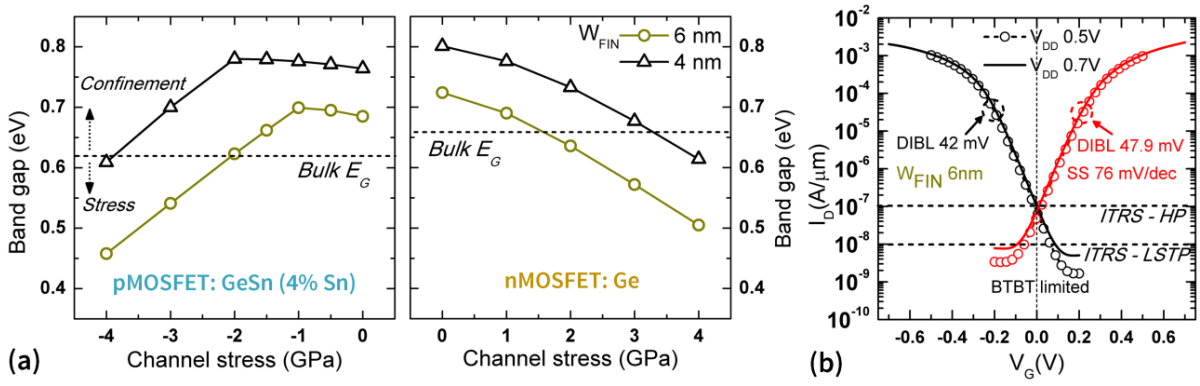


Fig. 1.9 (a) Effect of channel stress and fin width (W_{FIN}) on channel band gap (EG) for GeSn (4% Sn) pMOSFET and Ge nMOSFET. Band gap of unstrained, bulk material is shown as 'Bulk E_G'. At large stress, a net reduction in EG compared with bulk is observed. (b) Calculated I_D-V_G characteristics of 7 nm FinFET CMOS with W_{FIN} = 6nm showing that I_{OFF} meets ITRS requirements.

Task 2: Fabrication and Characterization, $In_xGa_{1-x}As$:

The integration of high-k dielectrics on $In_xGa_{1-x}As$ is essential for $In_xGa_{1-x}As$ MOSEFTs. We have demonstrated the successful integration of HfO_2 onto $In_xGa_{1-x}As$ using N_2 plasma combined with trimethylaluminum (TMA). The TMA/N_2 plasma treatment is done in-situ using a Kurt J. Lesker Co. ALD-150LX reactor equipped with a load-lock chamber and a remote 13.56 MHz RF inductively coupled plasma (ICP) source. Both the plasma treatment and subsequent HfO_2 growth are done at a temperature of 250C. HfO_2 with 3.5 nm thickness was deposited using alternate cycles of tetrakis(dimethylamino)hafnium [Hf(NME2)4] and H_2O precursors. Following HfO_2 deposition, the samples underwent an in-situ forming gas anneal (FGA) in the ALD process chamber. The FGA was done at 350C with an H_2/Ar ambient (40 sccm of H_2 and 110 sccm of Ar). Gate pads were deposited by thermal evaporation of Ni.

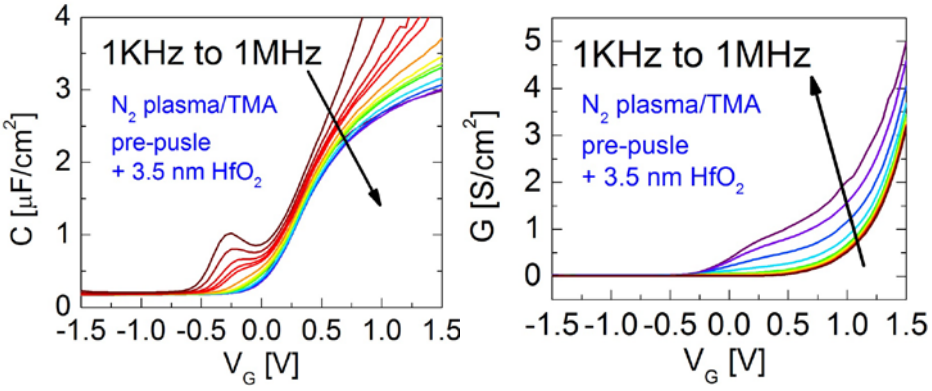


Fig 2.1 CV and GV characteristics of 3.5 nm of HfO_2 on InGaAs

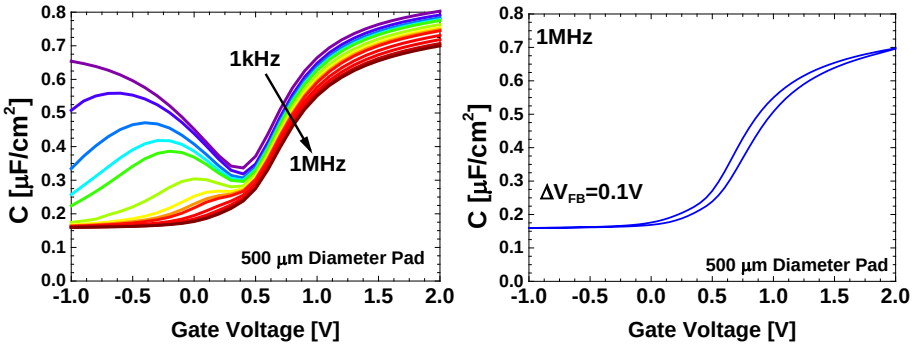


Fig 2.2 Frequency dependent CV and 1 MHz CV hysteresis characteristics for 10 nm of HfO_2 on $In_{0.53}Ga_{0.47}As$

Fig 2.1 shows CV and GV characteristics of 3.5 nm of HfO_2 gate stack on InGaAs using the TMA/N_2 plasma. The plasma process results in a very good interface with low interfacial states (D_{it}). At high gate biases in accumulation gate leakage begins to dominate low frequency CV and GV characteristics. To enable Total Ionizing Dose (TID) measurements large diameter gate pads are required. This required an increase in HfO_2 thickness from 3.5 nm to 10 nm to help suppress leakage currents in the dielectric. Fig 2.2 shows the both frequency dependent and high frequency hysteresis CV characteristics of 10 nm of HfO_2 on $In_{0.53}Ga_{0.47}As$. The thicker gate oxide results in

less oxide capacitance to fill and overcome interface states, thus resulting in degraded frequency dispersion performance in the depletion region. However the high frequency (1 MHz) performance of the thicker gate oxide is still very good with a ΔV_{FB} of 0.1V.

Task 3: Fabrication and Characterization, Ge:

3.1 Lateral Overgrowth (LAT-OGV) of Germanium for Monolithic Integration of

3.1.1 Germanium-on-Insulator on Silicon

A technique to locally grow germanium on insulator (GOI) structure on silicon (Si) platform has been developed (Fig. 3.1). On (001) Si wafer, silicon dioxide (SiO_2) is thermally grown and patterned to define growth window for germanium (Ge). Crystalline Ge is grown via selective hetero epitaxy, using SiO_2 as growth mask. Lateral overgrowth (LAT-OGV) of Ge crystal covers SiO_2 surface, and neighboring Ge crystals coalesce with each other. Chemical mechanical polishing (CMP) is done to planarize the GOI surface. Thus, crystalline Ge sitting on insulator for GOI applications is achieved (Fig. 3.2).

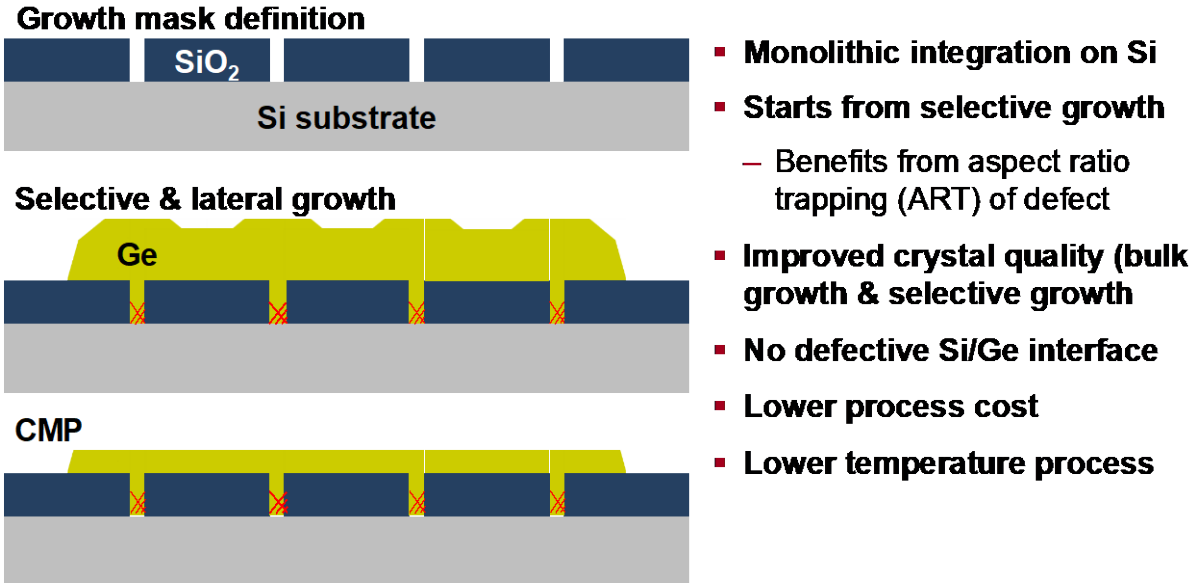


Fig. 3.1: Schematics of the lateral overgrowth process.

The influence of growth conditions on LAT-OGV is studied. An optimal recipe for LAT-OVG is designed by using different process conditions during different steps of the growth. Initial Ge seed layer growth is done at a low temperature (400 ^oC), which provides better coverage. Hydrogen annealing is done at a high temperature (825 ^oC) after the seed layer growth. This cycle is repeated several times for a better quality seed layer deposition. On this seed Ge layer, selective Ge growth is done to fill the growth window, with high HCl gas flow used to minimize nucleation on the oxide. During the lateral growth phase, growth conditions are optimized to eliminate any void at the intersection of the two growth fronts. After coalescence, the HCl gas is turned off since nucleation suppression is no longer needed. After the initial valleys are filled by dominant <100> growth, CMP is done for further planarization. High quality crystalline Ge on SiO_2 is observed by cross sectional TEM (Fig. 3.2). Low threading dislocation density (TDD) of $1\sim3\times10^6$ /cm^2 is measured from plan view TEM (Fig. 3.3). Raman spectroscopy is used to evaluate the strain level. Just like the bulk epi growth, 0.20 % of residual biaxial tensile strain is observed.

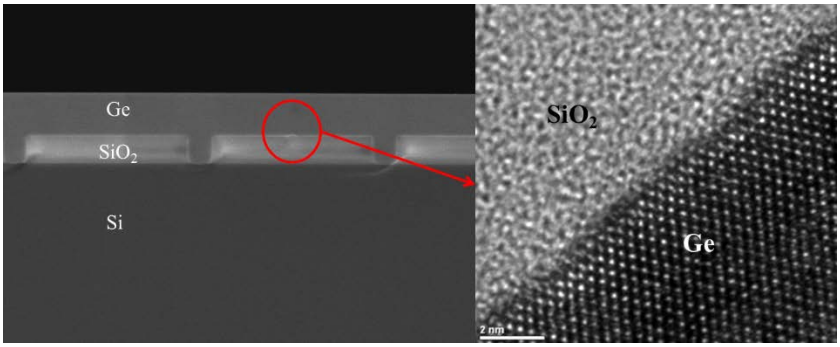


Fig. 3.2: Cross sectional SEM and TEM

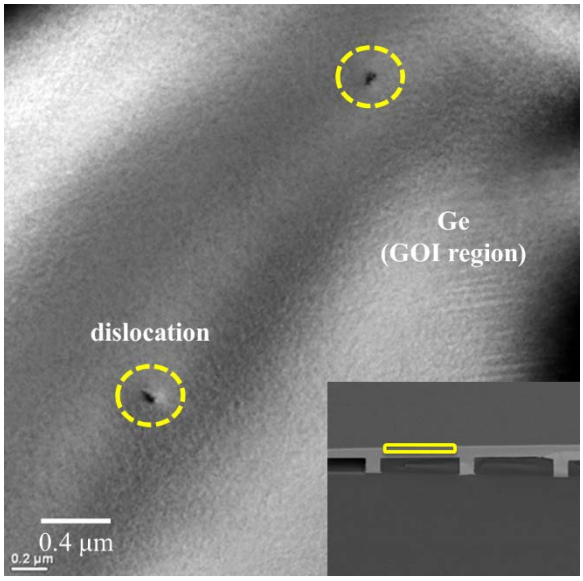


Fig. 3.3: Plan view TEM for analysis of threading dislocation density.

Time-resolved photoluminescence is used to measure minority carrier lifetime in LAT-OVG GOI. Results using time-correlated single-photon counting technique are shown in Table 3.1. Compared to the un-patterned epi-growth with the same thickness (600 nm), LAT-OVG GOI shows more than 7x improvement in minority carrier lifetime. Since threading dislocations act as acceptor-like traps and limit minority carrier lifetime, lower threading dislocation density is believed to be the main reason for this improvement.

Table 3.1. Minority carrier lifetime from time-resolved photoluminescence from 500nm and 1.5 μm un-patterned epi-Ge and 600nm thick GOI on 900nm SiO_2 from LAT-OVG.

	Epi Ge on Si	LAT-OVG GOI
Threading dislocation density(/cm^2)	3×10^8	$1\sim3 \times 10^6$
Lifetime (ns)	0.478	3.534

3.1.2 Heteroepitaxial Growth of GeSn

The first set of GeSn samples were fabricated using MBE. However, CVD-grown GeSn was chosen as the preferred platform for subsequent work. This migration was largely motivated by the lack of adequate material supply from MBE and the need to develop the device technology compatible with large-area wafer processing. As opposed to MBE that relies on small (2" or 3" diameter wafers) Ge or GaAs substrate for GeSn epitaxy, CVD growth process is compatible with industry standard 8" or 12" Si wafers. The CVD growth was done in collaboration with Applied Materials.

A 30 nm thick GeSn (7% Sn) is grown epitaxially on strain relaxed Ge-on-Si (001) buffer layers using reduced-pressure CVD. Digermane (Ge_2H_6) and tin tetrachloride ($SnCl_4$) are used as CVD precursors. The growth temperature during GeSn CVD is kept below 350 ºC. The Ge buffer layer thickness is ~3.7 μm. Schematic of the material stack used for fabrication of GeSn pMOSFETs shown in Fig. 3.4 (**a)**. The GeSn growth method adopted produces high quality crystalline GeSn as confirmed by the cross sectional TEM image of Fig. 3.4(**b)**. From (004) high resolution x-ray diffraction (HRXRD) omega-2theta scan of Fig. 3.4(**c)**, the out of plane lattice constant of Ge and GeSn layers is determined to be 5.652Å and 5.759Å respectively. CVD grown Ge on Si is slightly tensile strained due to the thermal mismatch between Ge and Si. The residual strain in Ge buffer layer is biaxial tensile and estimated to be 0.139%.

Due to its larger lattice constant than Ge thin epitaxial layers of GeSn are fully compressively strained with respect to the Ge buffer layer. This is confirmed by the (224) asymmetric 2D reciprocal space map (RSM) shown in Fig. 3.4(d). Both Ge and GeSn peaks lie along the same in plane reciprocal lattice vector indicating that GeSn is fully strained with respect to the underlying Ge buffer. The biaxial compressive strain in the GeSn layer is calculated to be 1.02% with respect to fully relaxed GeSn (7% Sn). Ge buffer on Si (without the GeSn layer) forms the control sample (Ge control).

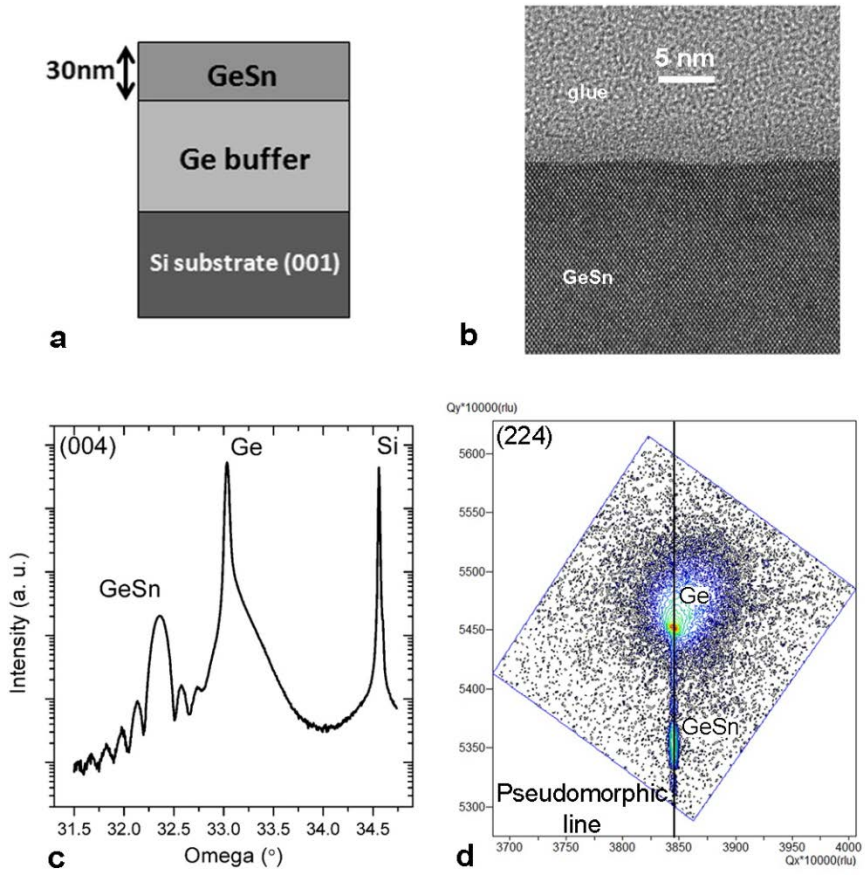


Figure. 3.4 (a) Schematic of the material stack used for pMOSFET fabrication **(b)** High resolution TEM image of the top GeSn layer **(c)** (004) HRXRD scan for extracting out-of-plane lattice constant and strain in Ge and GeSn layers. The Sn content in the GeSn layer is 7% **(d)** (224) RSM showing GeSn fully strained with respect to Ge buffer.

3.1.3 Ozone oxidation for Ge and GeSn surface passivation

In our earlier work a novel ozone oxidation process was developed for surface passivation of Ge MOS gate. Sulfur passivation of Ge surface was done in 5% $(NH_4)_2S$ solution at room temperature. This was followed by high-k dielectrics deposition step, firstly ~1nm ALD Al_2O_3 was deposited using trimethylaluminum (TMA) and ozone precursors. Subsequently an oxidation in ozone was performed in situ at 400°C, through the 1st Al_2O_3 layer to form a GeO_x interfacial layer (IL) between Ge and Al_2O_3, followed by a deposition of several nm ALD Al_2O_3. Combination of this ozone oxidation and sulfur treatment leads to a high quality gate stack on Ge with unpinned Fermi level and record-low Dit (1e11/cm^{2}eV) at both conduction and valence band edges. ~25meV flat band hysteresis is achieved, suggesting a very low border trap density.

We have extended this low-temperature ozone oxidation method for the formation of an interface passivation layer of GeO*x* and GeSnO*x* between a high-κ material and GeSn. This is achieved by depositing □1 nm of ALD Al_2O_3, followed by *in situ* O_3 oxidation at 400°C. The resulting gate stack containing an interlayer of GeSnO*x* on GeSn (6 at.% Sn) is shown in Figure 3.5(a). This surface passivation scheme has been shown to achieve interface trap density in the

10^{11} cm^{-2} over the entire range of energies in the bandgap. Moreover, if GeSn is capped with a thin layer (□2 nm) of Ge, controlled ozone oxidation results in an interlayer of GeO*x* on GeSn. This helps in further reduction of interface traps, as shown in Figure 3.5b–c.

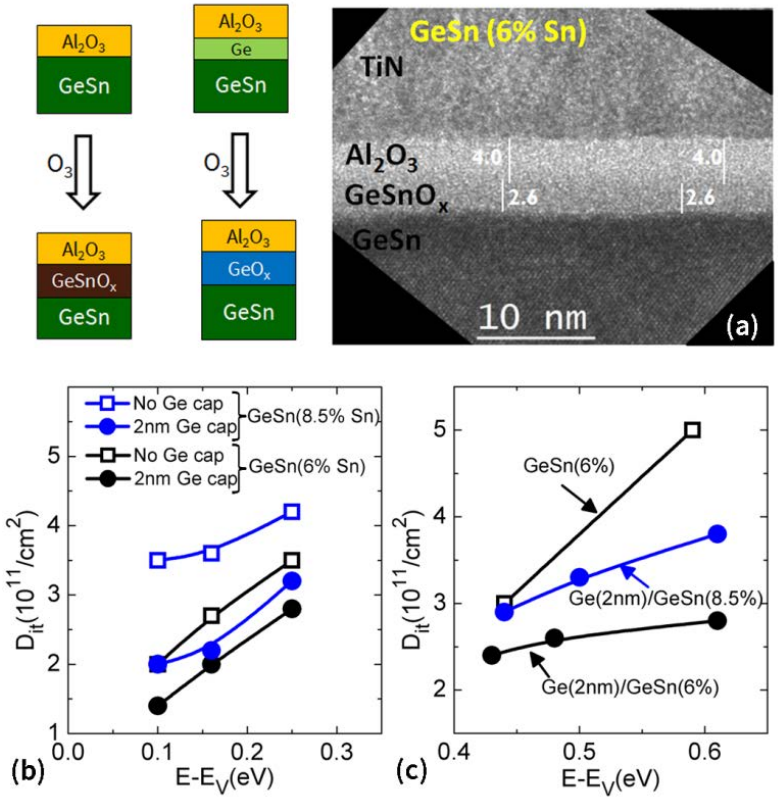


Fig. 3.5: (a) Ozone oxidation for formation of interface passivation layer of $GeSnO_x$ or GeO_x. TEM image showing ~2.6nm thick $GeSnO_x$ on GeSn (6% Sn). D_{it} near the (b) valence band edge and (c) conduction band edge for samples with 6% Sn and 8.5% Sn stays in the low-10^{11} cm^{-2} range. Some of the samples also have a thin (~ 2nm) Ge cap. Controlled oxidation of thin Ge cap to form IL of GeO_x is identified as the optimal route for GeSn surface passivation.

3.1.4 Fluorine Passivation of Gate Dielectric for Ge MOS Devices

Fluorine passivation was applied to the interface between Ge and Al_2O_3 gate oxide in a Ge p- and n-MOS capacitors to reduce the interface defects density. If F passivation is effective, it will result in increased carrier mobility in the MOSFET channel region. The F passivation is done by CF_4 plasma exposure, where F atom diffuse through the gate oxide to the interface. Id-Vg and split CV measurement was done to characterize the effective mobility.

Figure 3.6 shows the fabrication process flow for F passivation of Ge p- and n- MOSCAPs. Fabrication begins with the same epitaxially grown 2.0 μm thick Ge on Si substrate. A 12nm thick layer of Al_2O_3 is deposited on top of Ge surface in an ALD system at 250 °C. For F passivation of Ge/Al_2O_3 interface, the sample is exposed to CF_4 plasma with a flow of 500sccm at 40W in a PECVD system. During this process, F atom diffuse through the Al_2O_3 layer passivating the defect at the Ge/Al_2O_3 interface. Adjusting the sample's exposure time to the CF_4 plasma from no exposure to 40 minute exposure controls the degree of F passivation. Then the

samples are deposited with 20nm thick TiN and 50nm thick W as a gate metal. MOSCAP pattern was then defined by lithography and plasma etching.

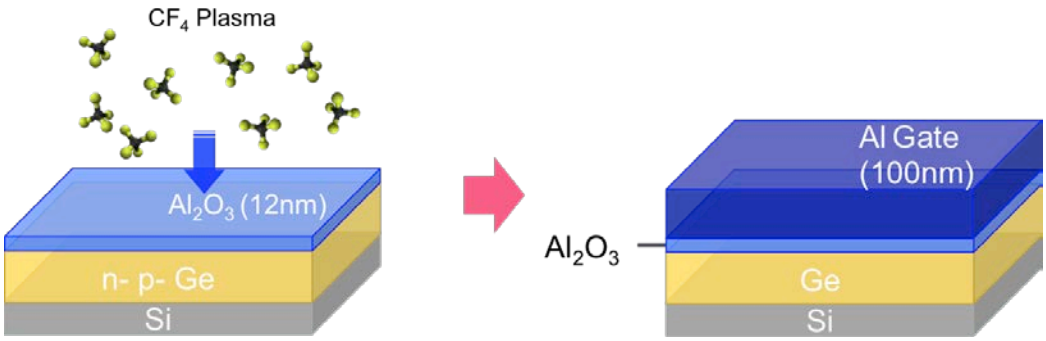


Figure 3.6: Process diagram for Ge p- and n- MOSCAPs.

The measured CV characteristics for Ge p- and n-MOSCAPs according to different CF_4 plasma exposure are shown Figure 3.7 (a) and (b), respectively. Here, main indication that it is the defects that are being passivated is the fact that CV bumps that are associated with the defects are decreasing as the fluorination time is increased. Although not completely eliminated, it can be observed that with increased fluorination time, these bumps begin to shrink. In addition, for both MOSCAPs the slope between the accumulation and inversion seems to increase with F incorporation, also suggesting defect reduction. Interface defect density extracted by conductance method for Ge p-MOSCAPs improved from $5x10^{12}$ /cm^2 (0 min exposure) to $7x10^{11}$ /cm^2 (40min exposure) and for Ge n-MOSCAPs it decreased from $9x10^{12}$ /cm^2 (0 min exposure) to $3x10^{12}$ /cm^2 (40min exposure). It can be expected that with better Ge gate stack such as $Ge/GeO_2/Al_2O_3$ with O_3 annealing, F passivation will give additional boost in giving more ideal CV profile. However, this reduction of interface defects comes at the expense of increased negative fixed charge in the oxide, indicated by positive flat band voltage (V_{fb}) for Ge p- and n-MOSCAPs. It is thought that these fixed oxide charges are created during the CF_4 plasma treatment. Such results are expected to increase the effective mobility in a Ge p- and n-MOSFETs, which will be investigated in our future work.

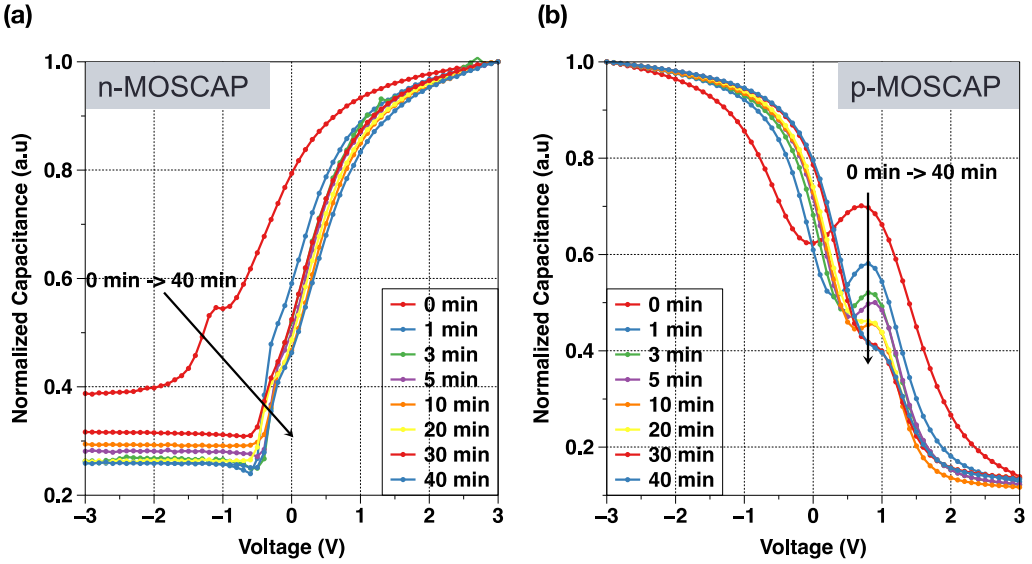


Figure 3.7 Current-Voltage response of fluorinated Ge (a) n- and (b) p- MOSCAPs.

Task 4: Radiation Testing I:

Total Ionizing Dose (TID) measurements were performed on InGaAs MOSCAPs by NRL researchers using 10keV X-Ray with dose rate 1000 krad (SiO_2) /s. Fig 4.1 shows the high frequency (1 MHz) capacitance-voltage (CV) response for 10 nm of HfO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAPs, which were irradiated with varied doses of X-ray radiation under +0.9V and -0.9V of applied bias on the gate. For both treatment combinations of applied bias during irradiation, there is a negative flat band voltage (V_{FB}) shift with increasing X-ray dose. Post X-ray exposure the devices were allowed a room temperature (RT) anneal for 24 to 48 hours. For each applied bias treatment combination, the V_{FB} did not recover after the room temperature anneal. Typically ion-induced fixed charge will anneal out or recover as a function of time. The lack of such a recovery is indicative of a permanent degradation mechanism.

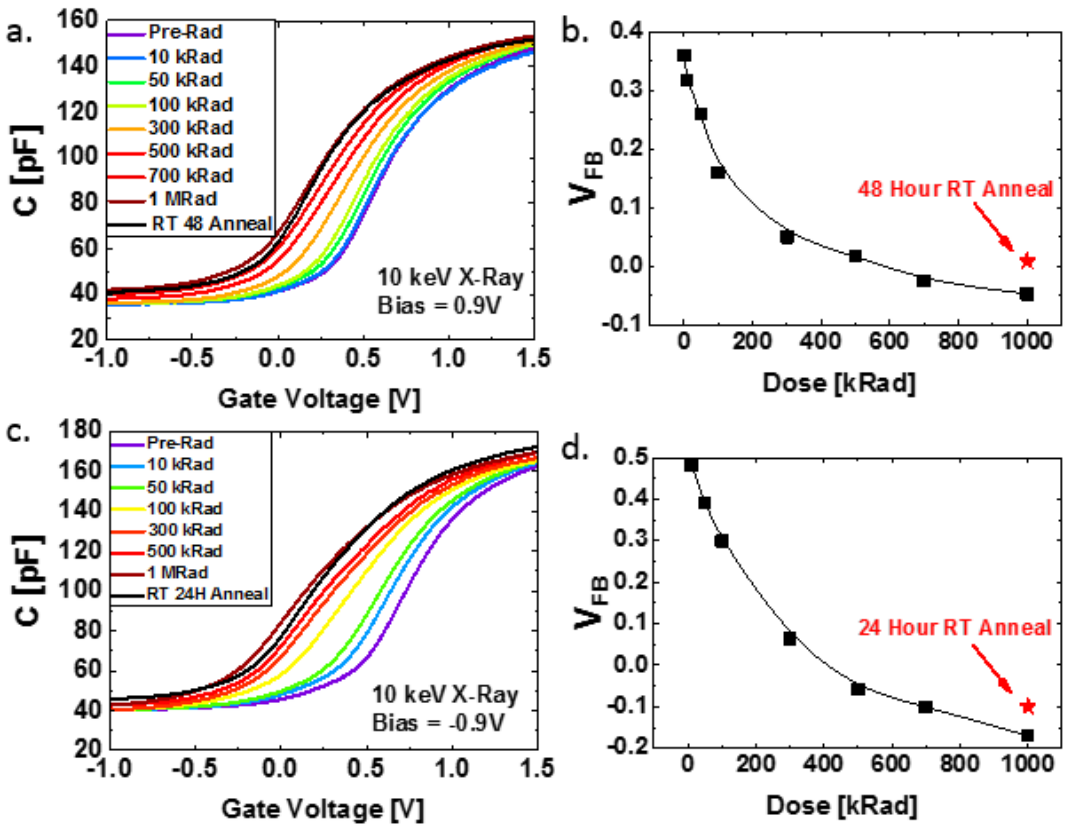


Fig 4.1 High Frequency CV (1 MHz) and ΔV_{FB} characteristics of a 10 nm HfO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAP as a function of 10 keV X-Ray dose for +0.9V (a&b) and -0.9V (c&d) bias.

To further study the effect of the 10 keV X-Ray on the 10 nm $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs, Terman analysis was performed on the high frequency CV characteristics to extract both the experimental band bending and D_{it}.

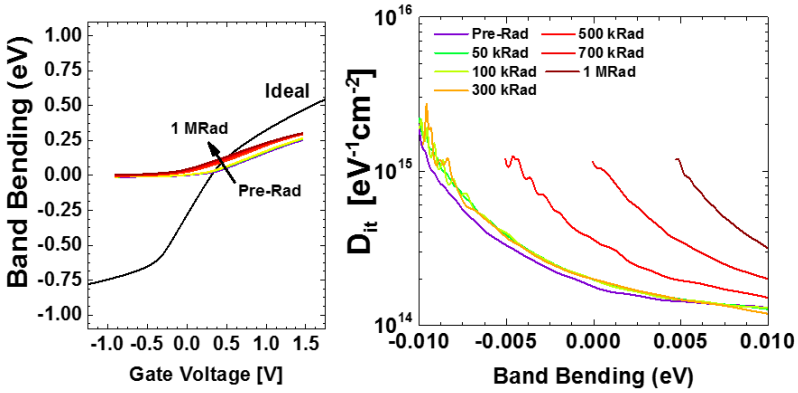


Fig 4.2 Terman Analysis of the High Frequency CV characteristics 10 nm HfO_2 on $In_{0.53}Ga_{0.47}As$ MOSCAP as a function of 10 keV X-Ray dose.

As shown in Fig. 4.2 (a) the degradation in band bending as a function of X-ray dose suggests that the high-κ semiconductor interface is being degraded by the X-ray radiation. A similar trend is observed for the D_{it} response versus band bending (Fig. 4.2 (b) where at 1 MRad the D_{it} is sufficiently high enough to prevent the band bending from moving past the flat band condition (Band Bending =0.0 eV). Work is ongoing to determine the physical cause of the high-κ semiconductor interface degradation with increasing radiation dose.

MOS capacitors on bulk Ge substrate have been fabricated at Stanford using ALD of Al_2O_3 as the gate dielectric and tungsten gate electrode. They are currently undergoing radiation testing at NRL.

Year 2

Task 1: Fabrication and characterization of FINFETs with various high-k gate stacks on $In_{0.53}Ga_{0.47}As$ heterostructure epitaxially grown on InP substrate (PSU) and with various high-k gate stacks with and without fluorination on Ge, and Si/Ge-heterostructures epitaxially grown on Si substrate. (Stanford)

FINFETs with various high-k gate stacks on $In_{0.53}Ga_{0.47}As$

Fig. 1.1 shows the structure of the 10nm QW $In_{0.53}Ga_{0.47}As$ structure utilized for the fabrication of the Fin-FET test structures. The Fin-FET structures were fabricated on carefully designed multi-layer epitaxial of on semi-insulating InP substrates using Molecular Beam Epitaxy (MBE) grown. N++cap layers are used to enable raised source and drain regions, allowing for improved contact resistance. Mo/Pt source drain contacts are deposited on the n++ cap regions These n++ cap regions is later etched with citric acid based wet etch selective to InP to define the raised source/drain regions.

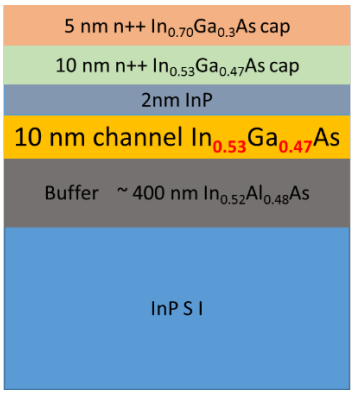


Fig. 1.1: Schematic of the 10nm thick $In_{0.53}Ga_{0.47}As$ Quantum-Well (QW) structure grown on semi-insulating Indium Phosphide (InP) substrate. The top 15nm thick InGaAs cap layer provides low resistance access to the QW via source-drain regions. InP is used as an etch-stop layer to remove the sacrificial cap layer over channel region.

The integration of high quality high-κ dielectrics directly on $In_xGa_{1-x}As$ is essential for high performance III-V FINFETs. We have demonstrated the successful integration of ALD HfO_2 onto $In_xGa_{1-x}As$ using N_2 plasma combined with trimethylaluminum (TMA). The TMA/N_2 plasma treatment is done *in-situ* using a Kurt J. Lesker ALD-150LX reactor equipped with a load-lock chamber and a remote 13.56 MHz RF inductively coupled plasma (ICP) source. Both the plasma treatment and subsequent HfO_2 growth are done at a temperature of 250C. HfO_2 with 3.5 nm thickness was deposited using alternate cycles of tetrakis (dimethylamino) hafnium [$Hf(NME_2)_4$] and H_2O precursors. Following HfO_2 deposition, the samples underwent an *in-situ* forming gas anneal (FGA) in the ALD process chamber. The FGA was done at 350C with an H_2/Ar ambient (40 sccm of H_2 and 110 sccm of Ar). Gate electrodes were deposited by thermal evaporation of Nickel. The C-V and G-V characteristics of 3.5 nm of HfO_2 on $In_{.53}Ga_{.47}As$ is presented in Fig 1.2. The plasma process yields a high quality electrical interface with low interface states density (D_{it}). At high gate biases, in strong accumulation, gate leakage starts to dominate low frequency C-V and G-V characteristics.

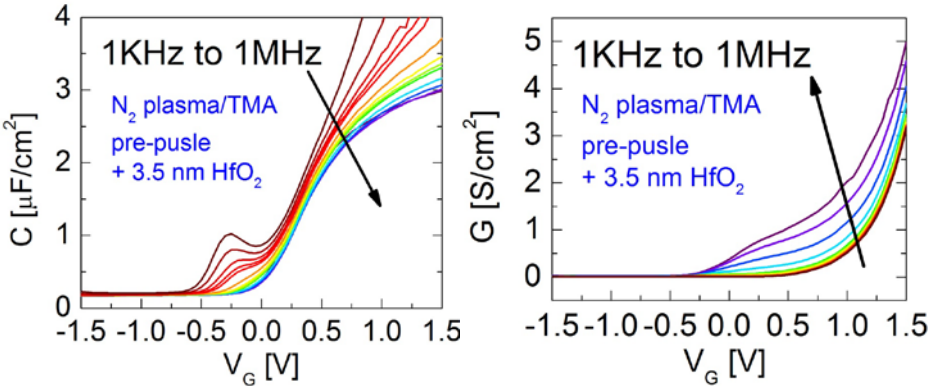


Fig 1.2 C-V and G-V characteristics of 3.5 nm thick HfO_2 dielectric on $In_{.53}Ga_{.47}As$ channel

The FinFET process flow is shown in Fig 1.3. The first step in fabricating the FinFETs is the deposition of Mo/Pt contacts to patterned source-drain regions. This is followed by the citric acid

gate recess wet etch step to remove the sacrificial n++ cap layer over the channel. The third step is the fin patterning and etch. The fin etch is done using a 900W Inductively Coupled Plasma (ICP) plasma etch using Cl/N_2 etch chemistry. Following the fin etch the high-κ dielectric is deposited in a conformal fashion around the fin utilizing the optimized ALD process as previously described. Ni gate electrode is deposited using thermal deposition. Fig 1.3 shows the SEM Micrograph and I_DV_G of L_G= 1µm 10nm QW $In_{0.53}Ga_{0.47}As$ FinFET.

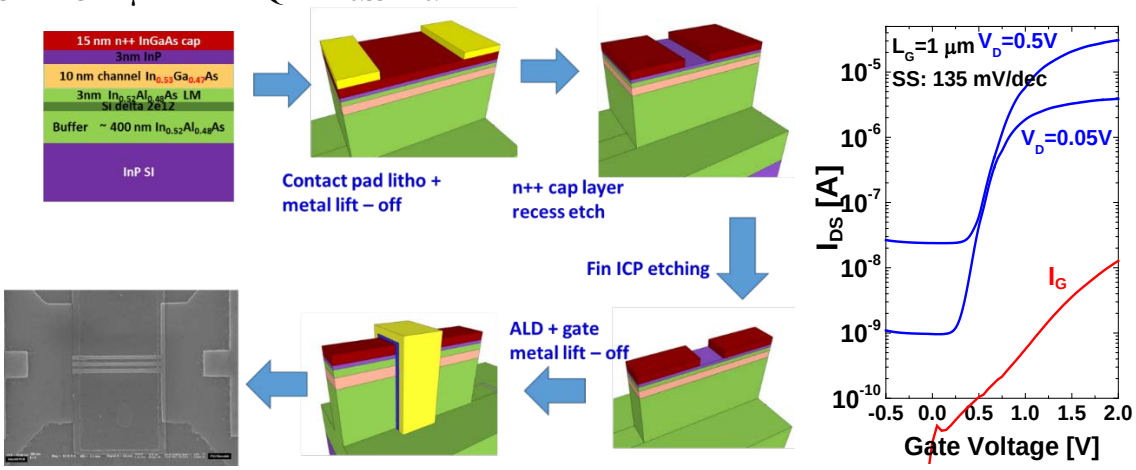


Fig 1.3 (a) $In_{0.53}Ga_{0.47}As$ Quantum-Well FinFET process flow with SEM micrograph; (b) Experimental transfer characteristics of $In_{0.53}Ga_{0.47}As$ QW FinFET

Ge MOSFETs with Fluorine Passivated Channel Region

By improving the gate oxide interface with Ge substrate in Ge MOSFET, one can obtain better performance in terms of carrier mobility, which gives better on-current in a I_d-V_g measurement. Figure 1.4 respectively shows the I_d-V_g curves for Ge p- and n- MOSFETs. As previously discussed in section 5.3.4, the threshold voltage (V_t) shifts positively for F treated samples, due to increased bulk oxide charge during the CF_4 plasma treatment. But, both samples show an increase in on-current with improvement in sub-threshold (SS) voltage. This suggests that the interface scattering is less for F treated samples. For quantification, carrier mobility for both samples was extracted by split-CV method and is shown in Figure 1.5. Here, there was ~40% improvement in terms of peak hole mobility for Ge p-MOSFET and ~20% improvement in peak electron mobility for Ge n-MOSFET. However, the mobility enhancement is smaller at higher charge density, which needs to be addressed in future works.

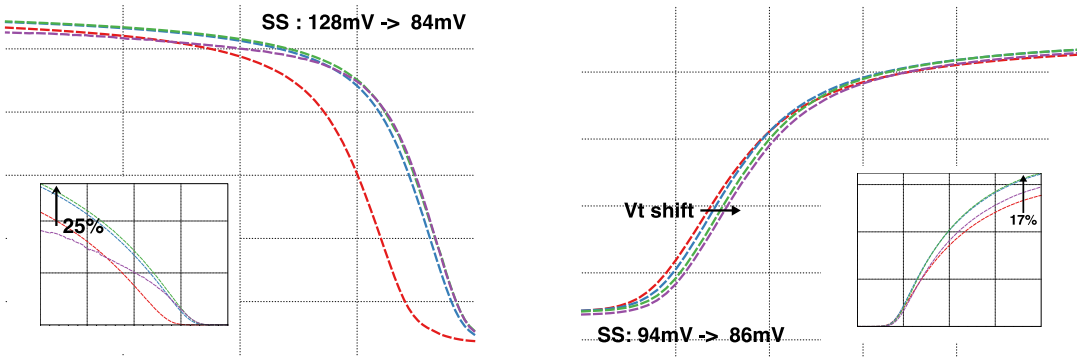


Figure 1.4: I_d-V_g measurement of Ge p- and n- MOSFET with F passivation in the channel interface. For both cases, increase of on current with shift threshold voltage (V_t) is observed.

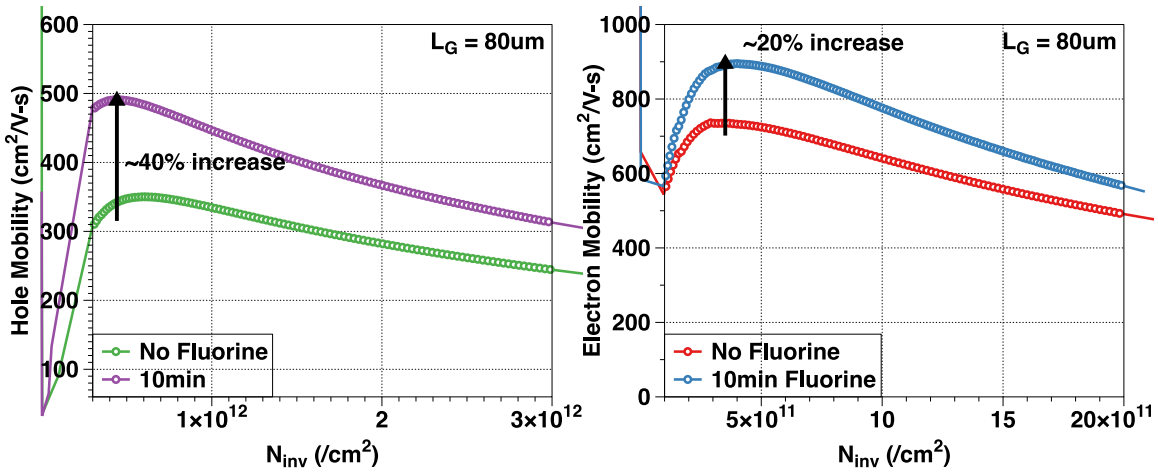


Figure 1.5: Hole and Electron mobility measurement from Ge p- and n- MOSFET. Mobility improvement is present for both Ge p- and n- MOSFETs.

Germanium Integration on Silicon

High performance Ge multigate MOSFETs require high crystal quality Ge. After the lateral overgrowth of Ge on insulator (GOI) through holes etched in SiO_2 and CMP, followed by selectively removing the SiO_2 growth mask by wet etching, monolithically integrated high crystal quality Ge on nothing (GON) on Si can be achieved.

Figure 1.6. shows the schematic process flow for the GON membrane. On the polished surface of lateral overgrowth GOI after CMP (Figure 1.6. (a)), etch holes are defined by optical lithography and dry etching, to ensure faster lateral wet etching (Figure 1.6. (b)). Through the etching holes, SiO_2 is wet etched by 6:1 buffered oxide etch (BOE) (Figure 1.6. (c)). Figure 1.7 shows SEM images of the resulting GON membrane.

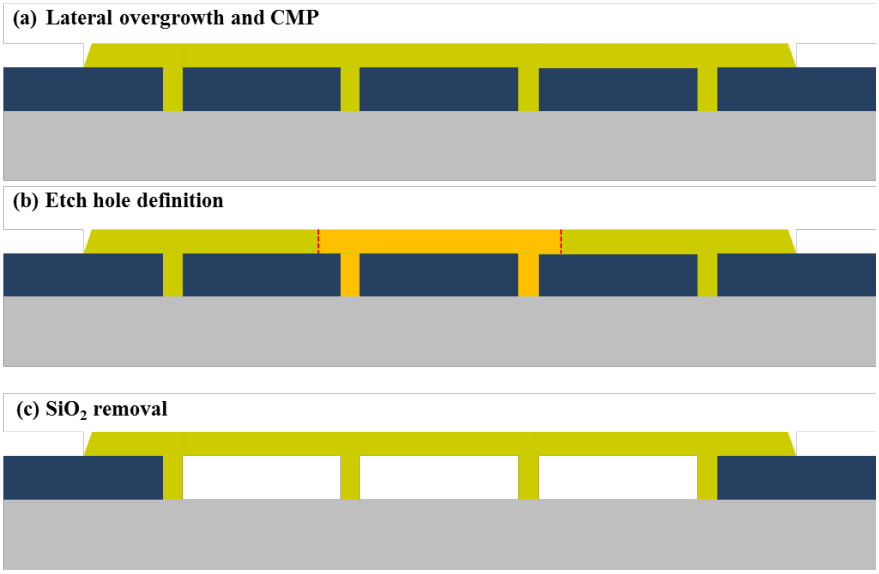


Figure 1.6. Wet etching of SiO_2 for GON. (a) Lateral overgrowth GOI after CMP. (b) Etch hole definition by optical lithography and dry etching. (c) Wet etching of SiO_2 using 6:1 BOE.

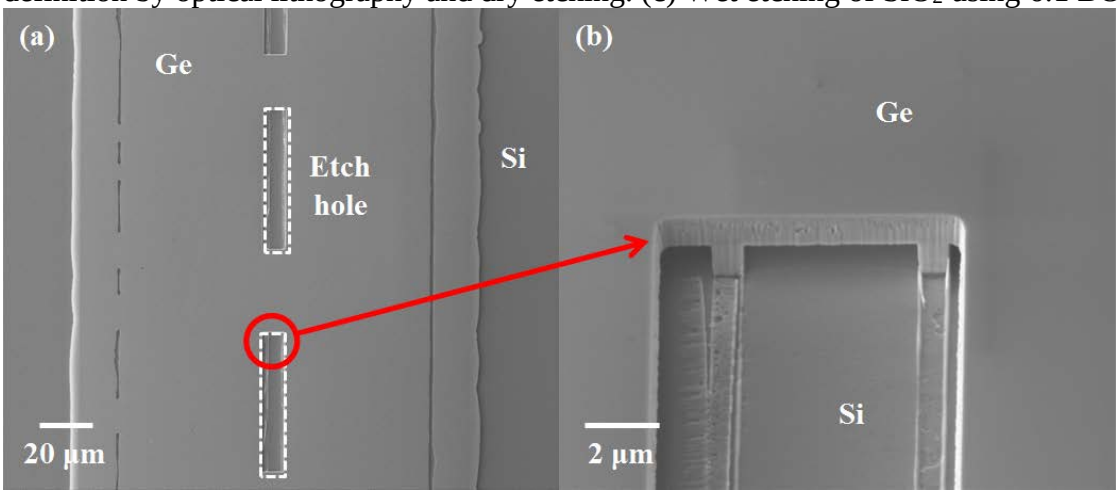


Figure 1.7: GON membrane on Si from lateral overgrowth and wet etching through etch holes.. Alternatively, GON membrane can be achieved by defining a mesa followed by the wet etching. Starting from the lateral overgrowth GOI (Figure 1.8. (a)), instead of defining etch holes, Ge mesa is defined by dry etching (Figure 1.8. (b)). SiO_2 growth mask is then removed by wet etching, using 6:1 BOE (Figure 1.8. (c)). The resulting GON membrane is shown in Figure 1.9.

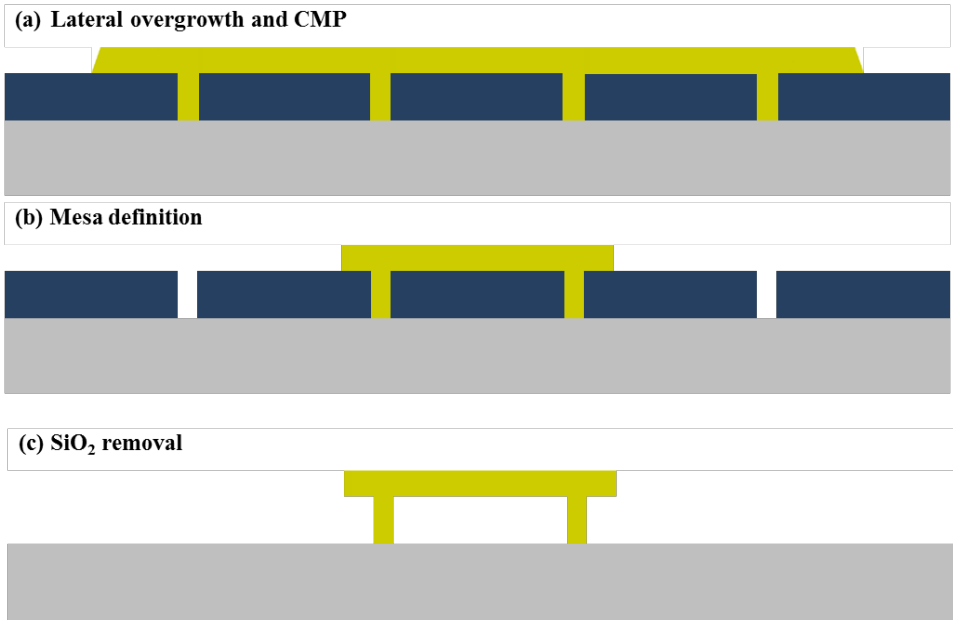


Figure 1.8. Wet etching of SiO_2 for GON. (a) Lateral overgrowth GOI after CMP. (b) Etch hole definition by optical lithography and dry etching. (c) Wet etching of SiO_2 using 6:1 BOE.

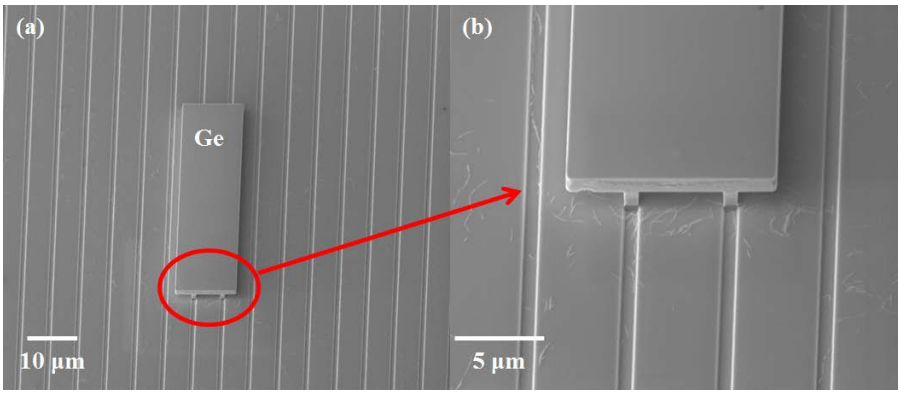


Figure 1.9. GON membrane on Si from lateral overgrowth and wet etching after mesa definition. By using the GON from lateral overgrowth GOI, monolithic integration of highly strained Ge based MOSFETs can be integrated on Si. This work is currently in progress. FinFETs and double/surround gate MOSFETs are now being fabricated on both GOI and GON structures.

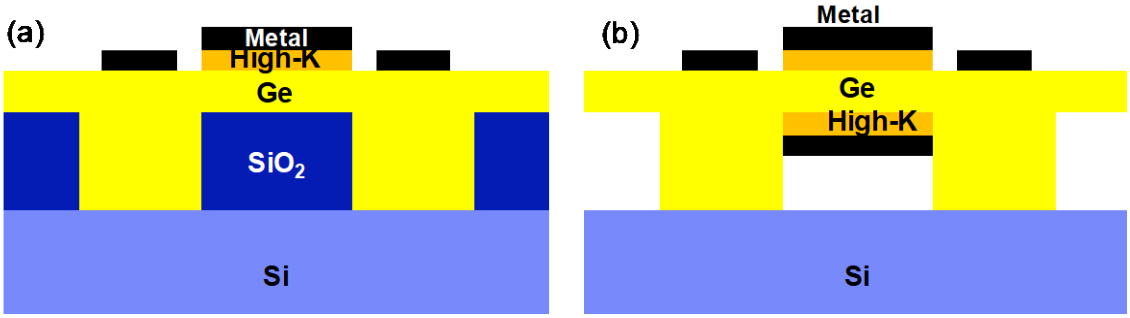


Fig. 1.10: Ge-based (a) single gate thin body transistor (b) double gate or surround gate transistor.

Task 2: Fabrication and characterization of MOS capacitors with various high-k gate stacks GeSn-heterostructures epitaxially grown on Si substrate. (Stanford)

Fabrication of Germanium-Tin-on-Insulator Substrates

In this work, a selective etch between GeSn and Ge is used to enable fabrication of germanium-on-insulator (GeOI) and germanium-tin-on-insulator (GSOI) substrates. Fig. 2.1 shows the key steps in the process flow. The fabrication process begins with formation of relaxed-Ge buffer on a Si-carrier wafer (donor wafer), followed by deposition of a layer of GeSn and a second layer of Ge using CVD. The top Ge is then passivated using the GeO_x/Al_2O_3 surface passivation scheme detailed in chapter 4. This wafer is directly bonded to a Si handle wafer with thermally grown SiO_2, resulting in the stack shown in Fig. 2.1(b). Prior to bonding, the Si/SiO_2 handle wafer is cleaned using SC-1 solution, followed by a 30s clean in 1:50 HF:DI-H_2O solution. After bonding, the composite wafer is furnace-annealed at 300ºC for 3 hours. There exists a strong adhesion between the SiO_2 and Al_2O_3 surfaces due to the following bonding reaction that occurs at the Al_2O_3/SiO_2 interface:

$$\text{Al-OH} + \text{Si-OH} \longrightarrow \text{Al-O-Si} + H_2O \qquad (2.1)$$

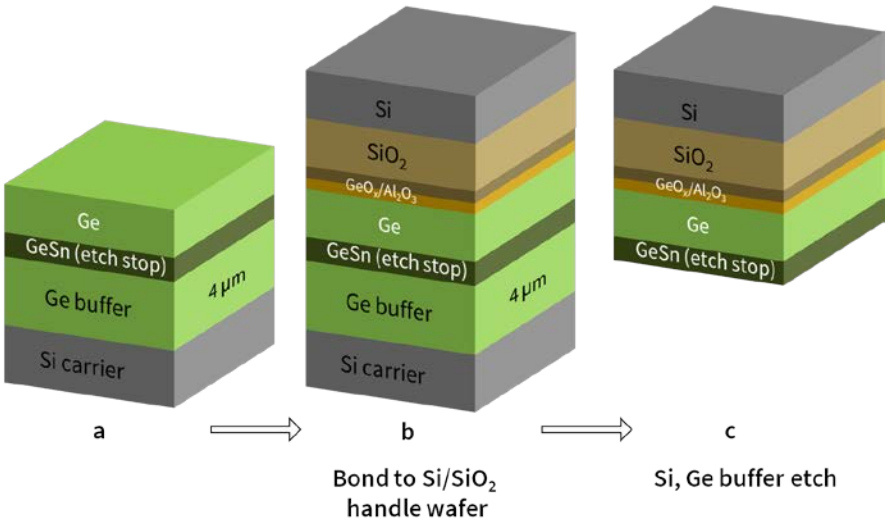


Fig. 2.1 Key steps in fabrication of GeOI and GSOI substrates

Next, the Si-carrier (donor wafer) is thinned down to ~30μm using a SF_6-based dry etch. The remaining Si-carrier is etched in tetra-methyl-ammonium-hydroxyl (TMAH) solution. This solution etched Si without affecting the Ge-buffer layer. In principle, the Si donor wafer can be recycled through the use of wafer splitting techniques such as Smart-Cut or controlled wafer spalling. The Ge-buffer is then thinned using aluminum etchant. The final etch is done using the selective dry etch between Ge and GeSn resulting in the stack shown in Fig. 2.1(c). In the process, the Ge and GeSn layers from the starting wafer are effectively transferred onto the Si/SiO_2 handle wafer.

Fig. 2.2 shows the cross-section TEM image of a GSOI substrate fabricated using this process flow. The thickness of the Ge and GeSn layers chosen here is 220 nm and 10 nm, respectively. Note that there is no fundamental constraint on the choice of the material/thickness of the semiconductor layer to be transferred. For simplicity, only a single layer of 220 nm thick Ge is shown here. The present approach is also applicable for transfer of any number of stacked semiconductor layers from the carrier wafer to the Si/SiO_2 handle wafer. From the TEM images, it is clear that the transferred layers retain their high crystal quality. In this particular case, the use of GeO_x helps achieve high quality back interface passivation by reducing the density of electrically active traps at the Ge/Al_2O_3 interface.

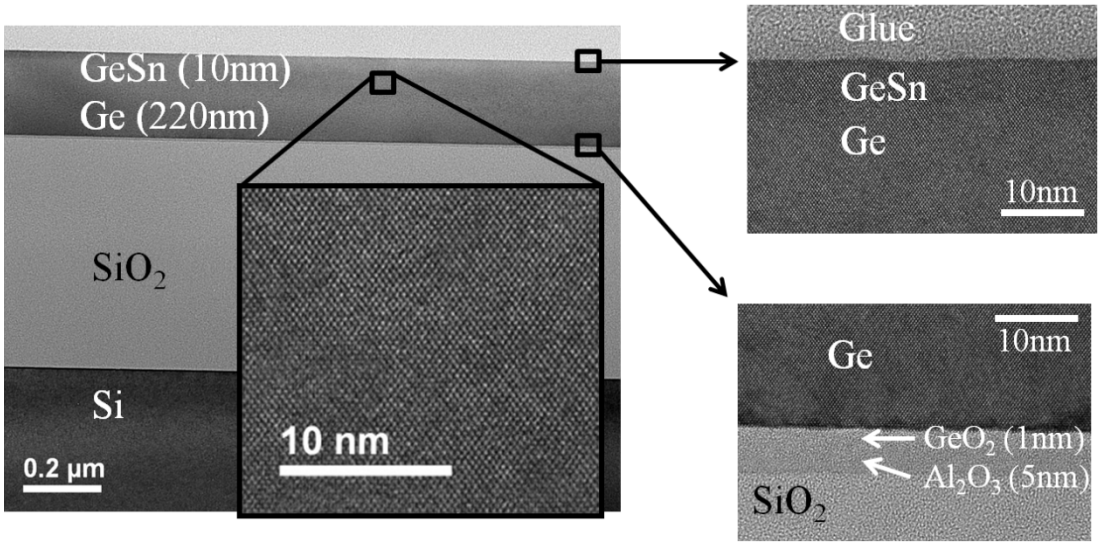


Fig. 2.2: TEM cross-sections of (a) GSOI with a high resolution inset, (b) top and (c) bottom interface. Excellent crystal quality, high uniformity of the transferred layers and good interfacial quality are observed.

Thickness uniformity of the semiconductor layer across the wafer is a key figure of merit for semiconductor-on-insulator substrates. A tight control over the semiconductor layer thickness variation is necessary in order to reduce the variability in device performance. Due to the high etch selectivity between GeSn and Ge substrates, the thin GeSn layer acts as an effective etch stop during the final etch and results in excellent thickness uniformity of the transferred layers. The thickness uniformity that can be obtained using this method is as good as that of the epitaxial method employed for growth of the GeSn and Ge layers.

High-k gate Stack on Ge

We have demonstrated successful integration of high-k dielectric Al_2O_3 on to Ge with very low D_{it} down to 1e11/cm^{2}eV. Process flow is shown in Fig. 2.3(a) and the device cross section in Fig. 2.3(b). After cyclic HF/H_2O cleaning, sulfur passivation of Ge surface was done in 5% $(NH_4)_2S$ solution at room temperature. A monolayer of sulfur is formed on the surface of Ge, which further eliminates native oxide and protects the Ge surface while transferring to ALD chamber. This was followed by high-k dielectrics deposition step. For ALD Al_2O_3 onto Ge, O_3 precursor was found to be with much lower D_{it} compared to H_2O precursor. So firstly ~1nm ALD Al_2O_3 was deposited using trimethylaluminum (TMA) and ozone precursors. Subsequently, an oxidation in ozone was performed in situ at 400°C, through the 1st Al_2O_3 layer to form a GeO_x interfacial layer (IL) between Ge and Al_2O_3, followed by a deposition of several nm ALD Al_2O_3. In total, 10nm Al_2O_3 with 1nm GeO_2 beneath it was formed on Ge as dielectric layer. Gate pads was formed by sputtering TiN/W under shadow masks. Back contact was formed by sputtering Ti/Al. Finally, a forming gas anneal was done at 350°C for 15 minutes.

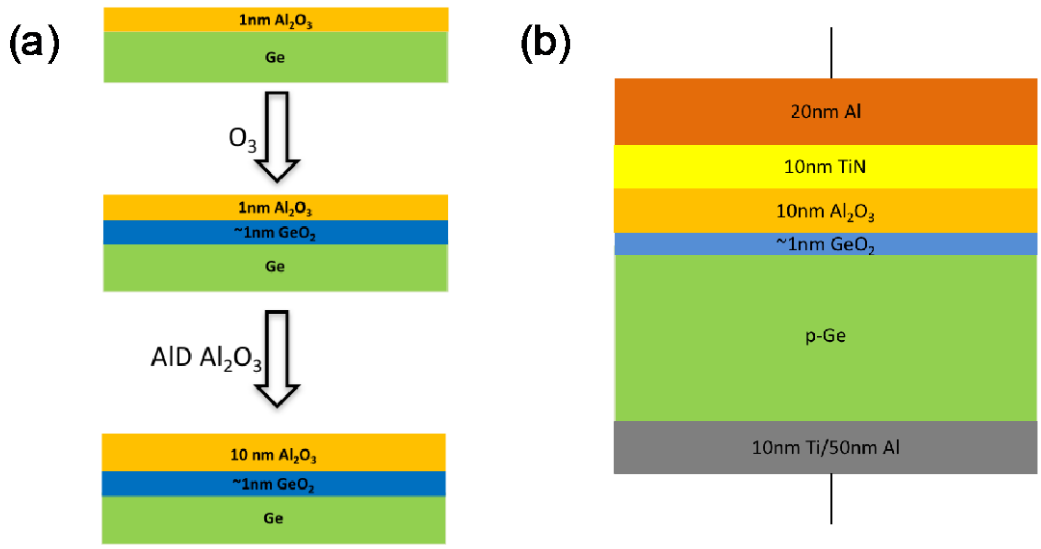


Fig 2.3 (a) Schematic for ozone oxidation (b) Schematic for Ge gate stack

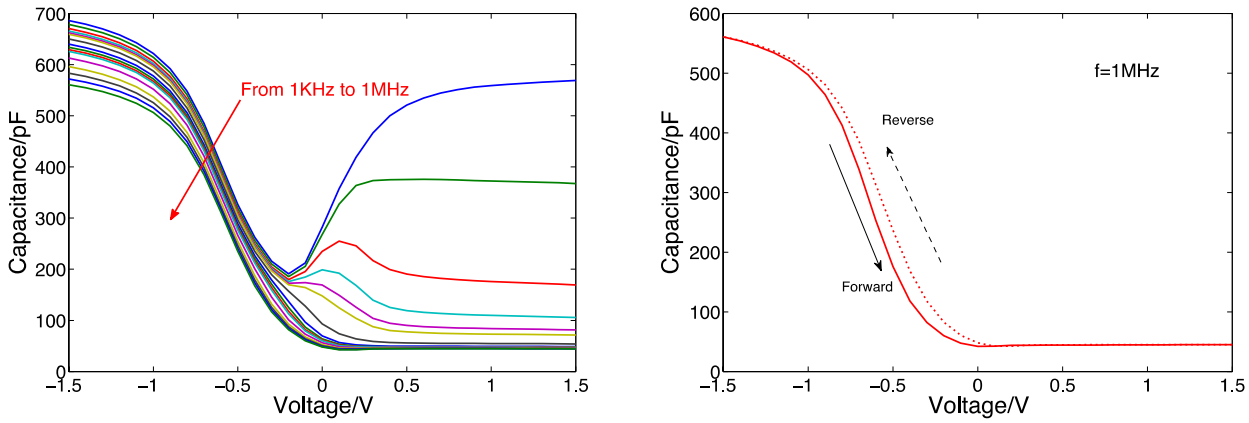


Fig 2.4 Frequency dependent CV characteristics and 1 MHz CV hysteresis characteristics of 10 nm of Al_2O_3 on Ge

Fig 2.4 shows requency dependent CV characteristics and 1 MHz CV hysteresis characteristics of 10 nm of Al_2O_3 on Ge. Fig 2.5 shows D_{it} distributions across the Ge band gap without ozone oxidation or sulfur passivation, with ozone oxidation but without Sulfur passivation, and with ozone oxidation and sulfur passivation. Combination of the ozone oxidation and sulfur treatment leads to a high quality gate stack on Ge with unpinned Fermi level and record-low D_{it} ($1e11/cm^2eV$) at both conduction and valence band edges. ~25meV flat band hysteresis is achieved, suggesting a very low border trap density.

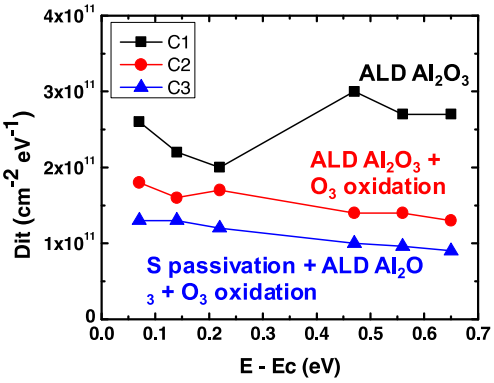
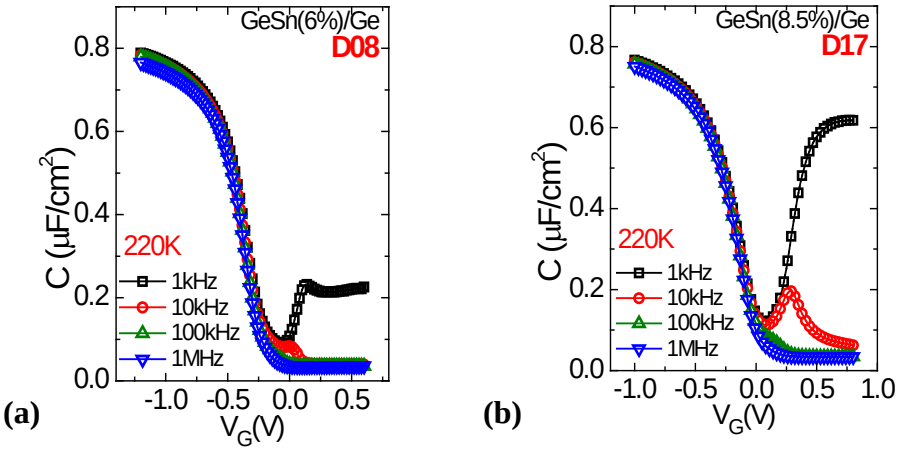


Fig 2.5 D_{it} distributions across the Ge band gap, where C1: without ozone oxidation or sulfur passivation, C2: with ozone oxidation but without sulfur passivation, C3: with ozone oxidation and sulfur passivation.

High-k gate Stack on GeSn

Using the $GeSnO_x$ (or GeO_x) formation method described in the previous section, MOS capacitors are fabricated on the following GeSn samples:

- D08: GeSn (6% Sn), no Ge cap on GeSn
- D09: GeSn (6% Sn), 5 nm Ge cap on GeSn
- D10: GeSn (6% Sn), 2 nm Ge cap on GeSn
- D17: GeSn (8.5% Sn), no Ge cap on GeSn
- D19: GeSn (8.5% Sn), 2 nm Ge cap on GeSn



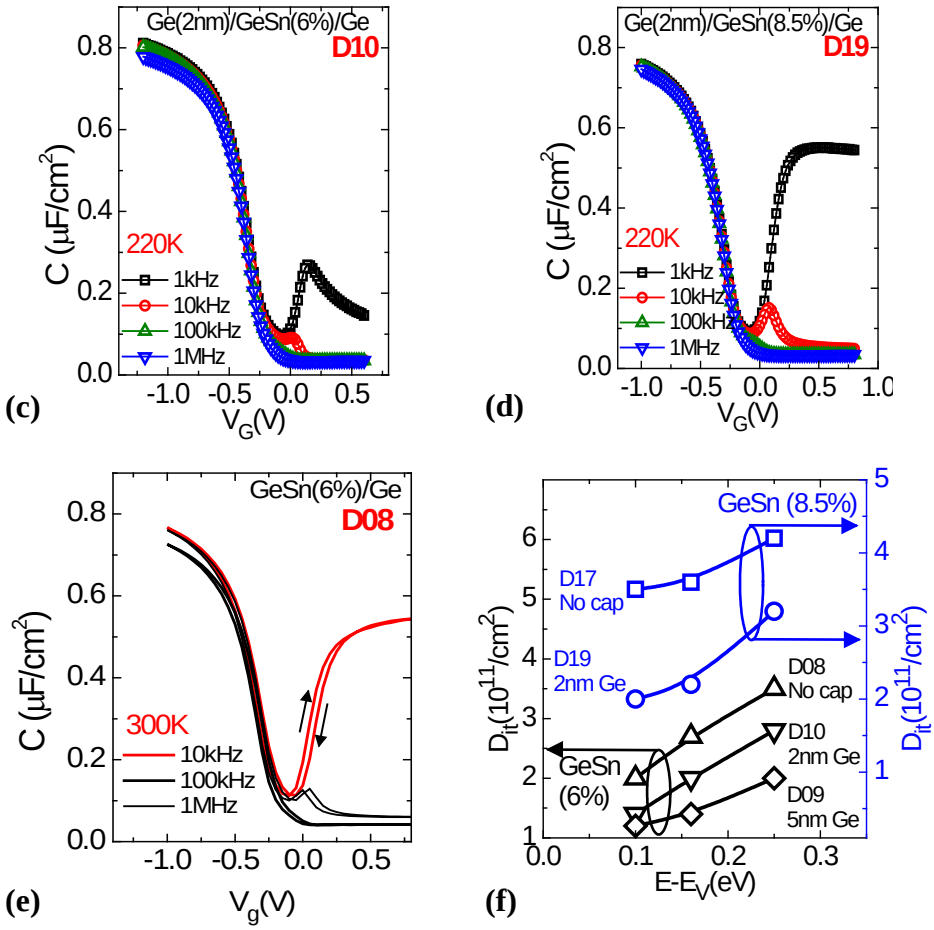


Fig. 2.6. p-MOSCAP C-V characteristics at 220 K for MOS capacitors on GeSn with (a) 6% Sn, no Ge cap, (b) 8.5% Sn and no Ge cap, (c) 6% Sn, 2 nm Ge cap and (d) 8.5% Sn, 2 nm Ge cap, (e) Hysteresis in C-V characteristics for p-MOSCAPs on GeSn (6% Sn), no Ge cap (f) D_{it} near the valence band.

Fig. 2.6. (a)-(d) show the C-V characteristics of MOS capacitors fabricated on these GeSn samples. Note that the undoped as-grown CVD Ge and GeSn tend to be slightly p-type with hole concentration of ~ 10^{16}/cm^3. The MOS capacitors show negligible frequency dispersion in both depletion and accumulation. In addition, the steep transition from accumulation to inversion as well as the low flat band hysteresis of less than 50mV. Fig. 2.6(e) attest to the high quality of the oxide/semiconductor interface.

Low temperature conductance method for measuring the D_{it}, when applied to p-MOSCAPs, reveals the trap distribution in the lower half of the band gap (towards the valence band). As shown in Fig. 2.6(f), the D_{it} near the valence band stays in the 10^{11}/cm^2 regime for all the samples. There is only a slight increase in trap density as the Sn% in the GeSn is increased from 6% to 8.5%. A thin Ge cap helps reduce the trap density for both 6% and 8.5% GeSn. Also, note that the extracted D_{it} increases as the trap energy approaches mid-gap. This is most likely an artefact of the conductance measurement on MOS capacitors. The small band gap of GeSn makes it particularly susceptible to the "weak inversion" phenomenon, causing an overestimation of the conductance response (and hence the D_{it}) near the mid-gap.

Task 3: TID (Co-60) Characterization of Ge and $In_{.53}Ga_{.47}As$ MOSFET characteristics pre and post radiation (leakage, threshold voltage, transconductance, on-current) and compare with parametric shifts obtained using MOSCAPs in Year 1 (NRL)

TID testing of the 10nm QW $In_{0.53}Ga_{0.47}As$ FinFETs has been limited by the Mo/Pt contacts. During wire bonding the Mo/Pt contact adhesion with the InGaAs substrate fails (Figure 3.1). This adhesion issue is attributed to the high stress in the Pt layer. The contacts are being re-engineered to remove the high stressed Pt form the contact pad.

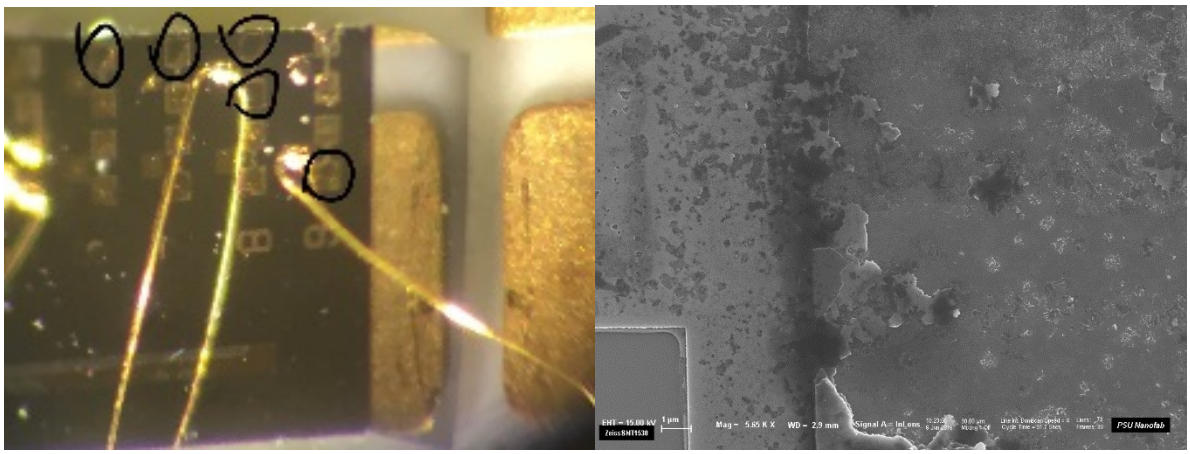


Fig 3.1 Picture of wire bond failure on $In_{0.53}Ga_{0.47}As$ QW FinFETs and SEM Micrograph bond site failure

Total Ionizing Dose (TID) experiments were performed on Ge MOSCAPs. One sample set had tungsten gates and the other had platinum gates. Both sample types had very good gate leakage currents in the 10 pA range. These devices were subjected to X-ray radiation using an Aracor 10 keV source with a dose rate 1000 rad (SiO_2)/s. The devices were biased at V_G = 1V during radiation. The Ge MOSCAPs with the Pt gate did not survive TID testing. Most of the devices blew after 10 to 50 krad. The reason for this is currently under investigation. The TID results for Ge MOSCAPs with W gate are shown in Fig 3.2. The curves corresponding to increasing dose levels. The data shows a negative shift in flat band voltage (V_{FB}) over the dose levels studied indicative of net hole trapping in the oxide or at interface states between the oxide/Ge interface. The change in V_{FB} as a function of dose (relative to prerad data) is shown in Fig 3.3 by the downward triangular symbols. A change in V_{FB} of ~ -0.366V is observed compared to ΔV_{FB} of -0.92V observed during the first year. Almost a factor of 3X improvement in ΔV_{FB} is observed. This is attributed to improved process control and different forming gas anneal (FMA) conditions. Reducing the FGA temperature from 400C to 350C and increasing anneal time from 5 minutes to 15 minutes reduced D_{IT}. This result is significant and currently under further investigation to directly correlate ΔV_{FB} with FMA conditions. This provides a potential path forward to optimize FMA process for Ge MOSFETs.

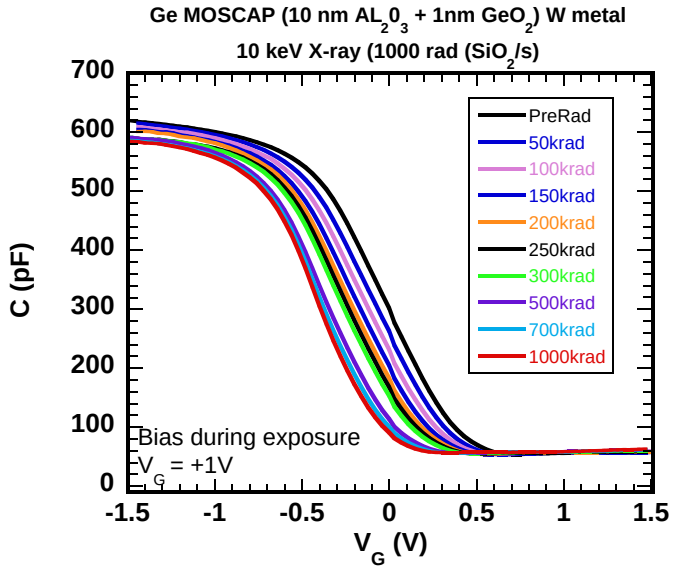


Fig 3.2 High frequency capacitance (100 kHz) as a function of gate voltage for increasing dose levels up to 1 Mrad. The gate was biased at 1V during exposure.

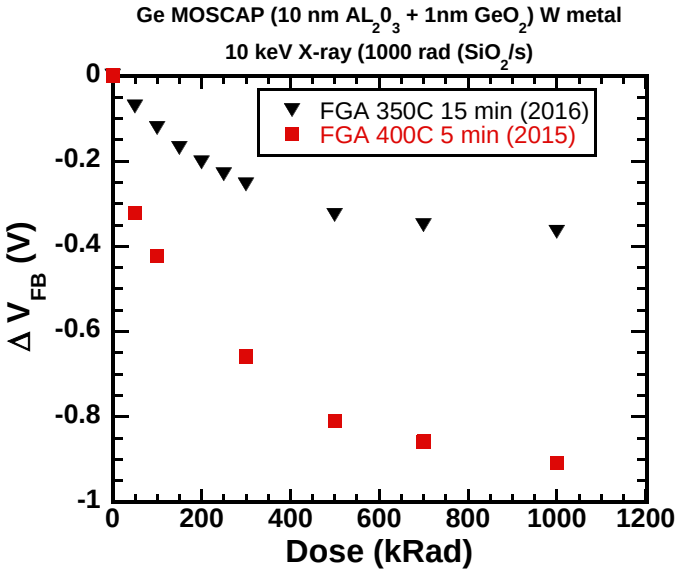


Fig 3.3 Change in V_{FB} as a function of dose measured on Ge MOSCAPs. Samples had different forming gas anneal temperature and time.

Task 4: Develop high-speed packaging/bonding and initiate L-SEE testing of MOSFETs using pulsed laser

In order to perform ion- or laser-induced charge collection measurements on MOSFET structures, the devices need to be mounted and wirebonded in high frequency boards. These boards have been designed and procured as shown in Figures 4.1 and 4.2. The packages have a total 8 transmission lines which have an impedance of 50 ohms to match the input impedance of our high bandwidth 16 GHz Tektronix oscilloscope. Several different transistors on a given sample can be wirebonded in a single HF board depending on whether all terminals are wirebonded or just the gate and drain (source grounded). Electrical connection from the HF

board is accomplished using end launch SMA connectors (27 GHz) purchased through Southwest Microwave (part# 292-07A-5). These connectors are removable and can be used on other HF boards.

A high frequency microwave probe setup was used to measure the scattering parameters (S-parameters) of the boards out to 40 GHz with limitations coming from the probes. The setup is shown in Figure 4.3 and the s-parameter results are shown in Figure 4.4. Since the S parameters matrix for this test describes a 2-port network the generic descriptions below apply:

S11 is the input port voltage (reflection coefficient)
S12 is the reverse voltage gain (transmission coefficient)
S21 is the forward voltage gain (transmission coefficient)
S22 is the output port voltage (reflection coefficient)

The results show that S12 is nearly identical as S21 as expected. There is minimal degradation in the forward and reverse transmission signals over the frequency range of interest (up to 26 GHz).

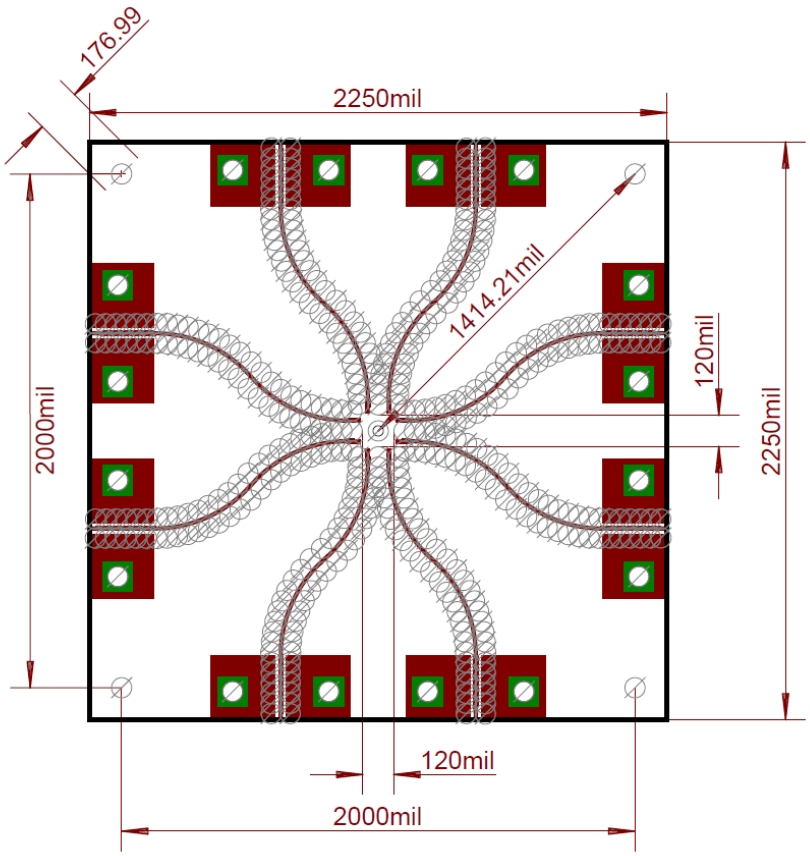


Fig 4.1 Schematic diagram of the high frequency package designed to perform high frequency ion- and/or laser-induced charge collection measurements. The dimensions of the board are shown in the figure.

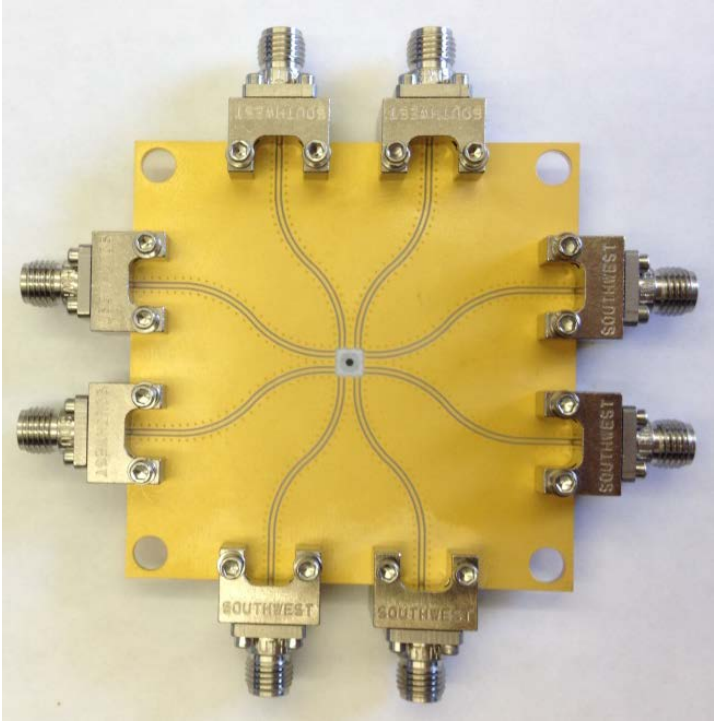


Fig 4.2 Picture of the high frequency package specially made to perform high frequency ion- and/or laser-induced charge collection measurements. The end launch connectors are also shown in the photo which can be removed and used on another board.

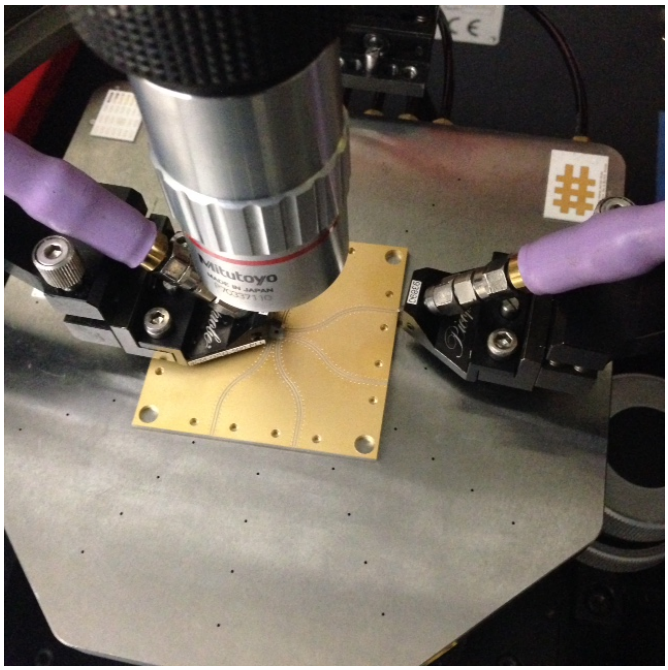


Fig 4.3 Photo showing setup used for determining S-parameters of HF boards.

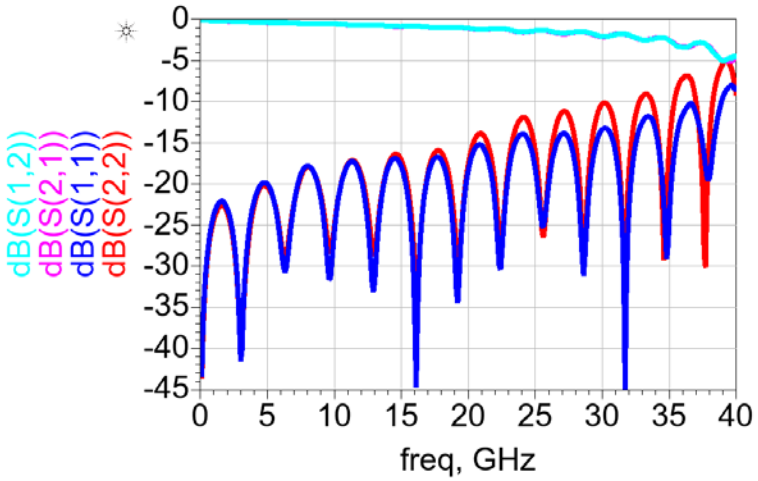


Fig 4.4 Plot of s-parameters, in decibels, as a function of frequency.

Year 3

1. Soft Error Evaluation for InGaAs and Ge Complementary FinFETs

With relentless scaling of transistor dimensions, the single cell soft error rate (SER) reduces with each technology node [1]. InGaAs and Ge complementary FinFET technology is promising for next generation NMOS/PMOS FETs, due to their superior transport properties [2] over silicon, but their soft error performance is unexplored to date. Previous work investigated the SER in InAs nFinFET assuming symmetrical NMOS and PMOS current and exposed the vulnerability of InAs FinFET compared with Si FinFET [3]. In this work done in collaboration with Prof. Suman Datta of Notre Dame University, we evaluate the soft error rates in InGaAs n-channel and Ge p-channel FinFETs for complementary logic application. Many technical assumptions were made based on the technology developed earlier in both the groups.

Model Calibration: The FinFET structures studied in this work are shown in Fig. 1.1. All the devices are integrated on Si substrate. Metamorphic buffer layers are employed for InGaAs and Ge FinFETs to accommodate the lattice mismatch between the substrate and the channel. The transport properties are calibrated against experimental data [4-6], as shown in Fig. 1.2. The calibrated transport parameters are used to project the device performance at 14 nm node, as shown in Fig. 1.3. Devices are work function adjusted to match the respective IOFF at 100 nA/μm. It is to be noted that an acceptor interface trap density of 1013 cm-2eV-1 is included to match the Ge FinFET model to experimental data. A look up table (LUT) based Verilog A model is then constructed for all the devices for circuit level analysis [3].

Single Event Transients: Fig. 1.4 shows Si planar MOSFET and FinFET transfer curves and transient currents. The ION of planar device is smaller than FinFET, but the transient current is 10x higher than FinFET. This is due to the smaller footprint of FinFET, which reduces the charge collection from the substrate. While the critical charge is similar in both, the collected charge within the FinFET is significantly smaller than the planar architecture, thereby greatly improving the soft error rate in the FinFET [1].

Ion induced drain current transients are shown in Fig. 1.5 for different FinFETs. The transient current is larger in InGaAs than Si FinFET, due to higher electron mobility, while the transient current in Ge FinFET is 50% lower than that in Si FinFET. Fig. 1.6 shows the hole current density in Ge and Si FinFET. The arrows indicate that both the source and drain collect holes in

Ge FinFET, while, in Si FinFETs, the source injects holes, which are collected by the drain. This is related to the quantum-well structure of Ge FinFET. The source electron current is counterbalanced by the hole current in Ge FinFET, while the source hole current reinforces the electron current in Si FinFET. Fig. 1.7 shows the conduction band energy at pre-strike and transient peak. The source-to-channel barrier reduces, suggesting bipolar amplification in these devices [3], [7]. Interestingly, the barrier collapses for InGaAs FinFET, turning on the device completely [7]. However, the barrier remains significant, 0.23 eV, for Ge FinFET, leaving the channel partially formed and, therefore, both the source and drain junctions collect holes [8].
Soft Error Evaluation: Fig. 1.8 shows the threshold linear energy transfer (LETTH) and the critical charge Qcrit required to upset an SRAM cell with ion strikes at different FinFETs. The Ge FinFET requires the largest LETTH, due to the low charge collection efficiency and high InGaAs FinFET restoring current. For InGaAs FinFET, the charge collection efficiency is high and the LETTH is the smallest. However, it shows a superlinear relationship with VDD, and correlates well with the restoring Ge FinFET drive current dependence on VDD. The Qcrit is also consistent with the drive current of the restoring device. Fig. 1.9 benchmarks the Qcrit of InGaAs, Ge and Si FinFET at VDD=0.5 V. It is to be noted that this value is smaller than the measured Si FinFET data, likely due to the under-estimation of additional parasitic capacitance in the simulation. The transient propagation in a combinational logic chain is shown in Fig. 1.10. A threshold LET exists for the transient that cannot be electrically masked. Fig. 1.11 shows the LET vs. pulse width and the threshold LET for different VDD. The LETTH dependence on VDD is qualitatively similar to the SRAM case. To evaluate the SER, heavy ion differential flux is shown in Fig. 1.12. The LET in Si is higher than that in both InGaAs and Ge, largely due to the smaller mass density of Si. Fig. 1.13 shows the relative SER of SRAM and combinational logic. InGaAs FinFET dominates the SER and is the most vulnerable to radiation. Ge FinFET has an improved SER compared with Si FinFET. Therefore, SER in InGaAs and Ge FinFET complementary technology is higher (worse) than Si.
Conclusion: The soft error in InGaAs and Ge complementary FinFET technology is evaluated. The soft error is dominated by ion strike at the InGaAs FinFET because of its high charge collection efficiency, low ionization energy, and high mass density. Ge FinFET has a low charge collection efficiency and shows an improved SER over Si FinFET. Moreover, poor dielectric/Ge interface degrades drive current at low VDD, increasing the susceptibility to soft error. Therefore, special consideration has to be given for InGaAs and Ge complementary FinFET technology for their application in radiation sensitive environment.
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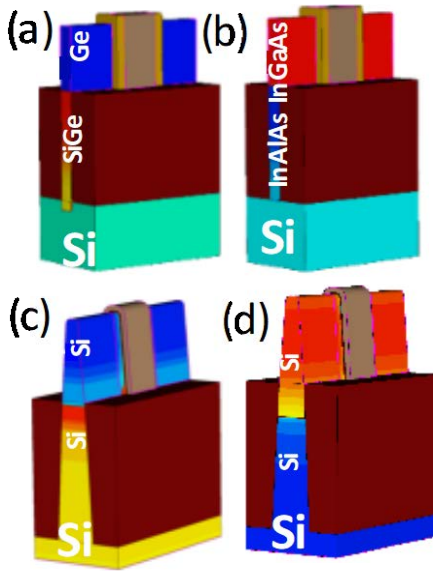


Fig. 1.1: Schematic of (a) Ge pFinFET, (b)InGaAs nFinFET,(c) Si pFinFET and (d) Si nFinFET. All the devices have Si substrate.

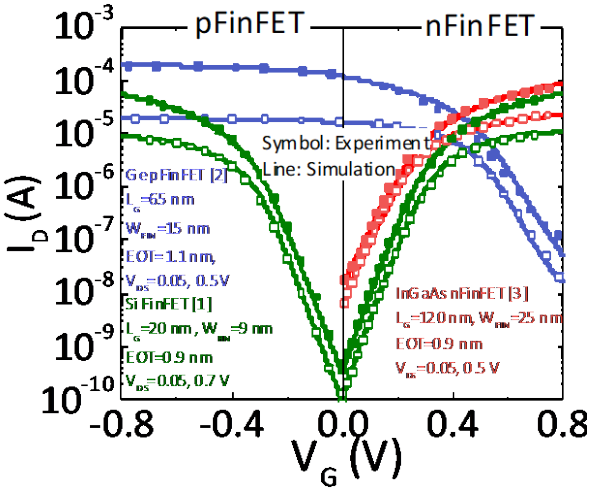


Fig. 1.2: Calibration of model with Si FinFET [4], Ge pFinFET [5], InGaAs nFinFET [6].

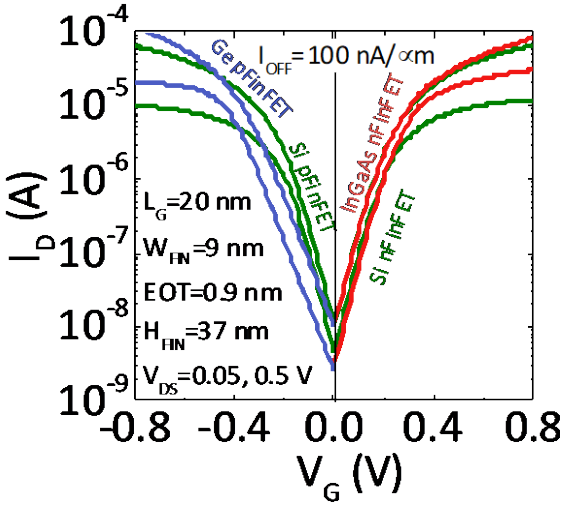


Fig. 1.3: $I_D V_G$ of FinFETs projected to 14 nm node. OFF current is 100 nA/μm. Fin pitch is100 nm.

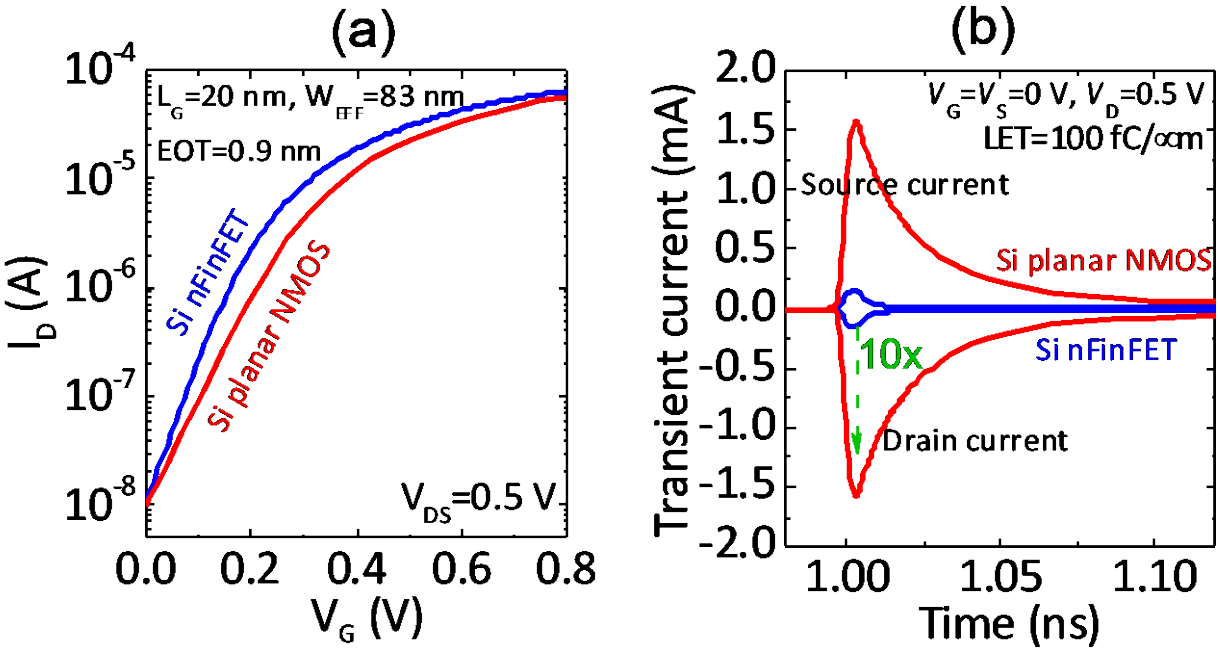


Fig. 1.4: Comparison of (a) transfer curves and (b) ion induced transient current between Si planar NMOS and nFinFET

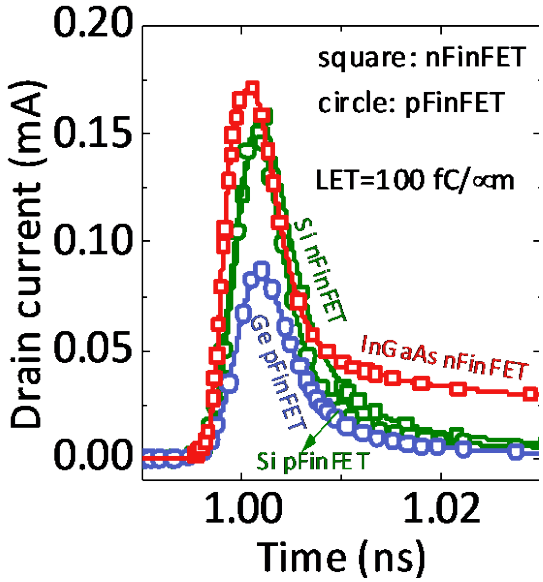


Fig. 1.5: Comparison of ion induced drain transient current for InGaAs/Ge and Si FinFET.

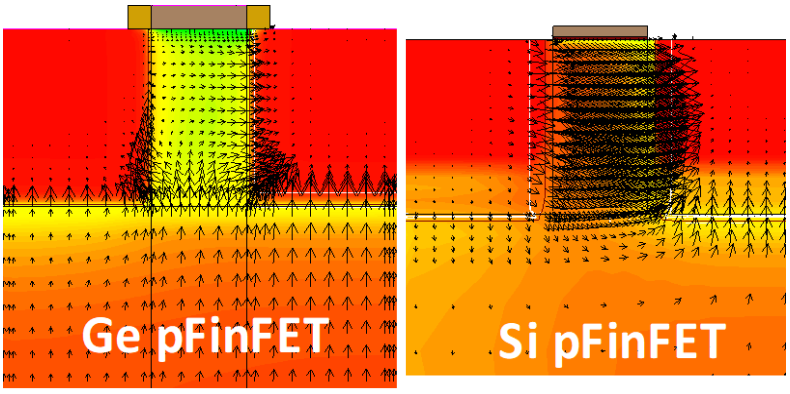


Fig. 1.6: Hole current density (arrow) for Ge and Si pFinFET.

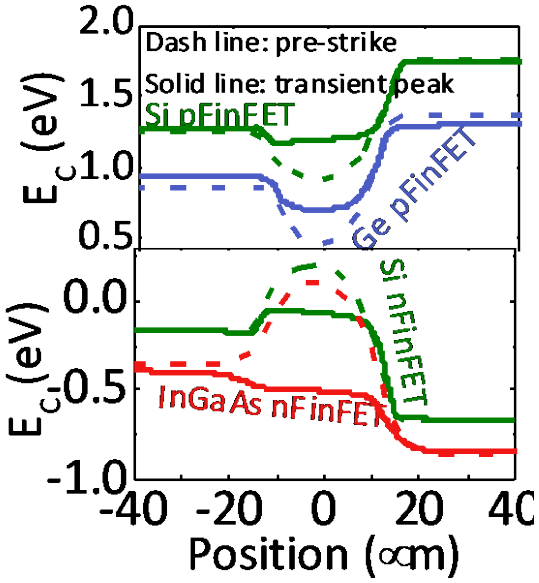


Fig. 1.7: Conduction band diagram at pre-strike and peak of the transient. Source-to-channel barrier reduces for all devices.

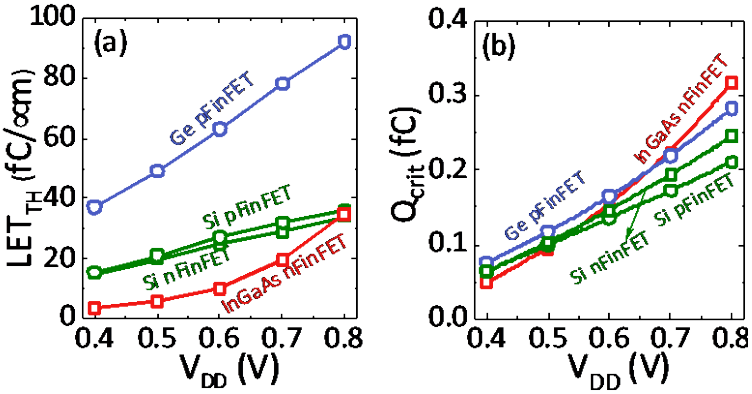


Fig. 1.8: (a) Threshold LET and (b) critical charge required to upset a 6T SRAM as a function of V_{DD}. Critical charge is consistent with drive current of restoring device. The threshold LET_{TH} is consistent with charge collection efficiency.

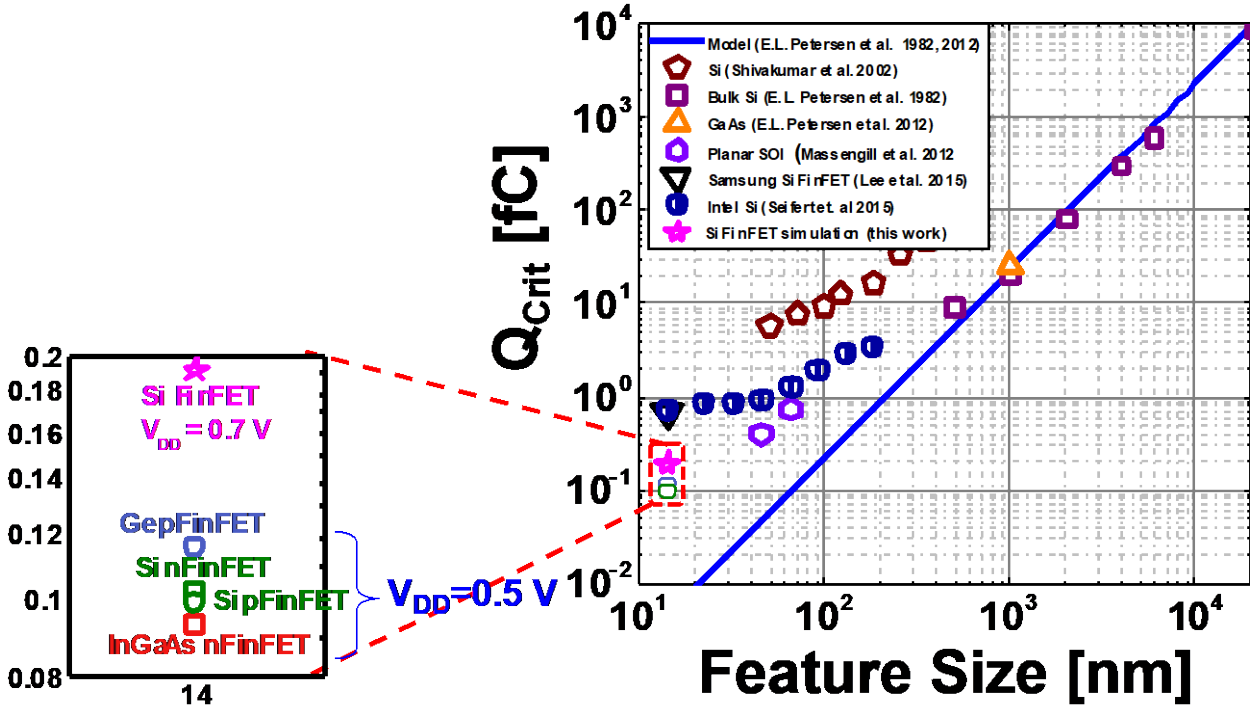


Fig. 1.9: Critical charge comparison for InGaAs, Ge and Si FinFET. V_{DD}=0.5 V data is shown here.

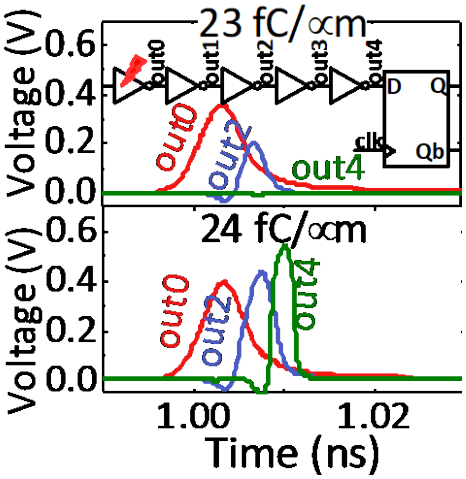


Fig. 1.10: Electrical masking of transient propagation through combinational logic.

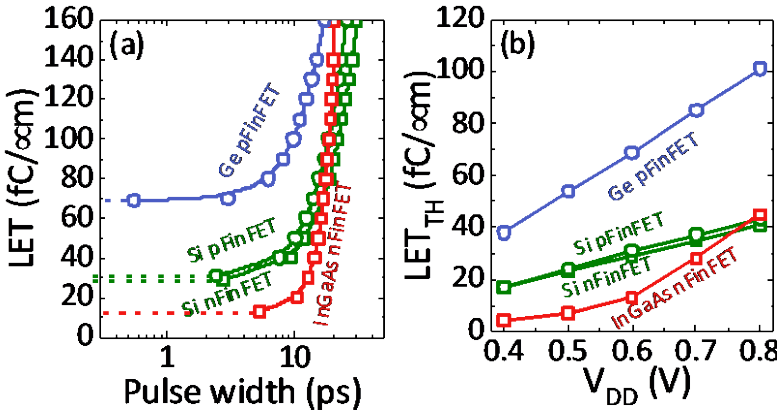


Fig. 1.11: (a) LET vs. pulse width and (b) Extracted critical LET. Pulse width is the width at $V_{DD}/2$ for V_{out4}. Dashed line indicates LET_{TH}.

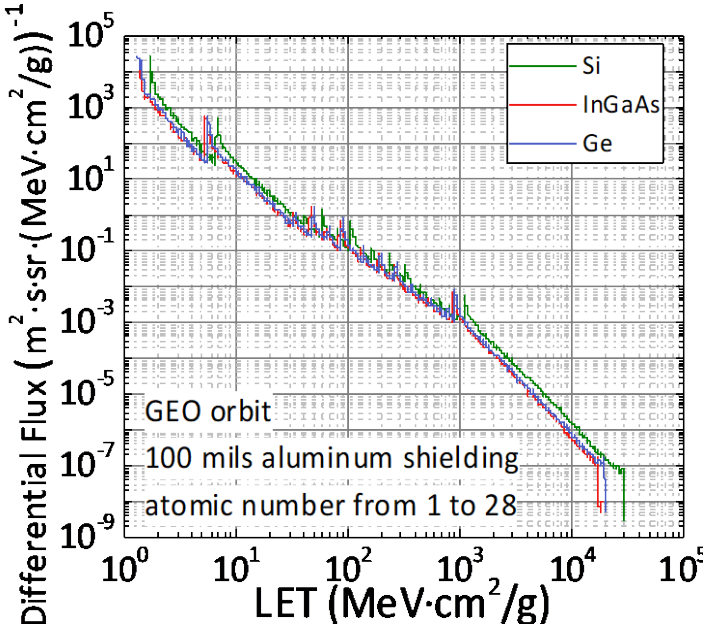


Fig. 1.12: Heavy ion differential flux vs. LET for InGaAs, Ge and Si material.

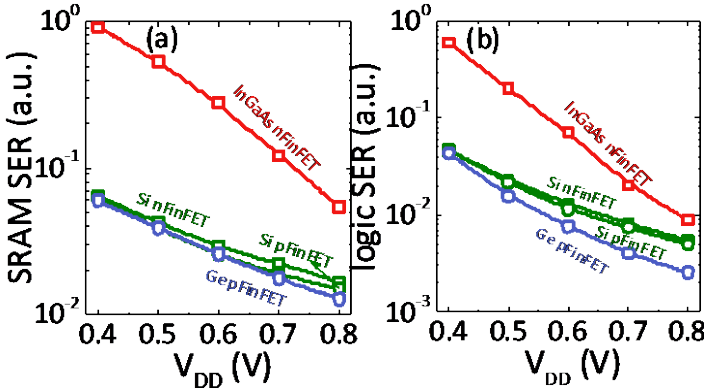


Fig. 1.13: Relative SER of (a) SRAM and (b) combinational logic for ion strike at InGaAs, Ge and Si FinFET.

2. InGaAs MOSFET Technology Development (Notre Dame)

InGaAs nFinFETs with various numbers of quantum-well channel have been developed at University of Notre Dame. Figure 2.1 shows several critical process steps during fabricating single quantum-well InGaAs FinFET. Source/Drain contacts are first formed via lift-off of sputtered Mo/Pt to form low resistivity contact to n+ InGaAs. A course mesa isolation etch is then performed for device and contact isolation. To form the quantum well channel, citric acid based wet etch is used to selectively etch away the n+ cap layers and form the gate recess. (Citric acid is very selective between the InGaAs and InP etch stop) Fins are then patterned and etched using a Cl_2–based RIE etch. 3.5nm ALD HfO_2 is deposited before gate metal lithography, where thermal Nickel gate electrode is formed via a lift-off process. A forming gas anneal at 350 °C completes the QW FinFET process.

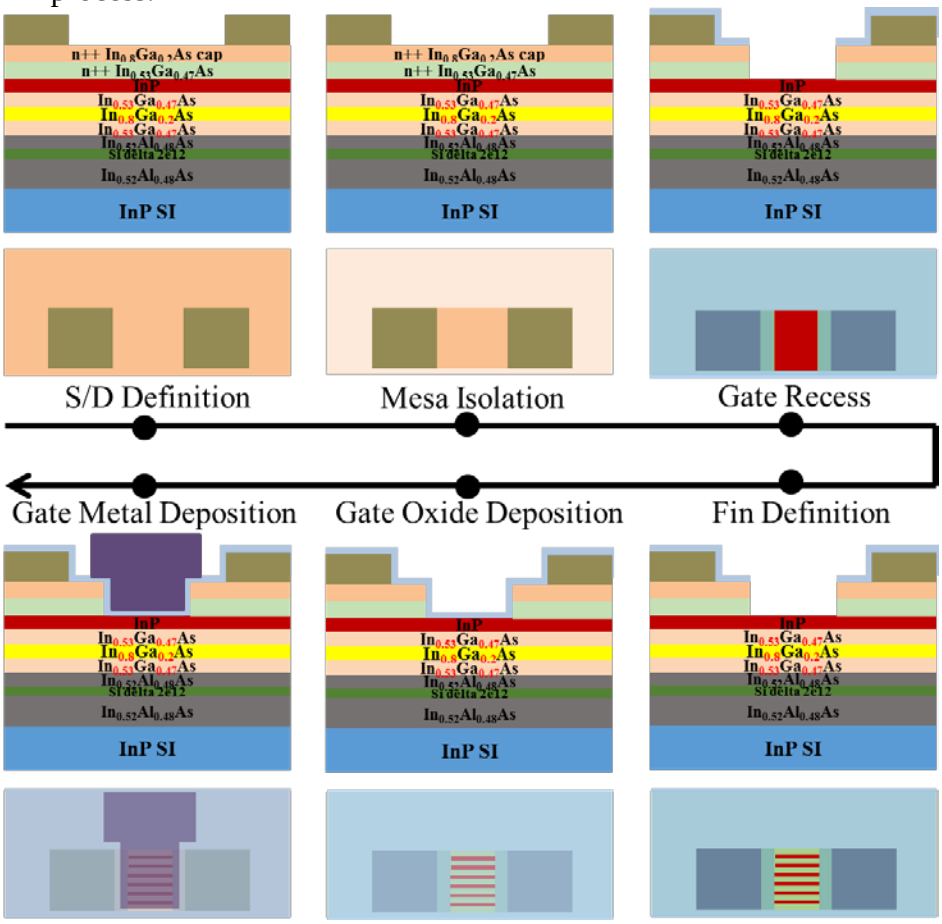


Figure 2.1. Critical process steps in fabricating InGaAs quantum-well FinFET. Here single quantum device is shown for an example.

Electron mobility has been measured through Hall measurement for InGaAs FinFETs with different numbers of quantum-wells. The results are shown in Figure 2.2. It shows that single quantum-well device has the highest Hall mobility, while the triple quantum-well device has the lowest electron mobility. This is probably related with the strain relaxation as the number of quantum-well increases. Further decomposition of mobility into different scattering mechanisms show that the mobility in single quantum-well device is limited by the interface roughness scattering and the polar optical phonon scattering, as shown in Figure 2.3. Therefore, if these scattering could be controlled, the electron mobility could be further enhanced.

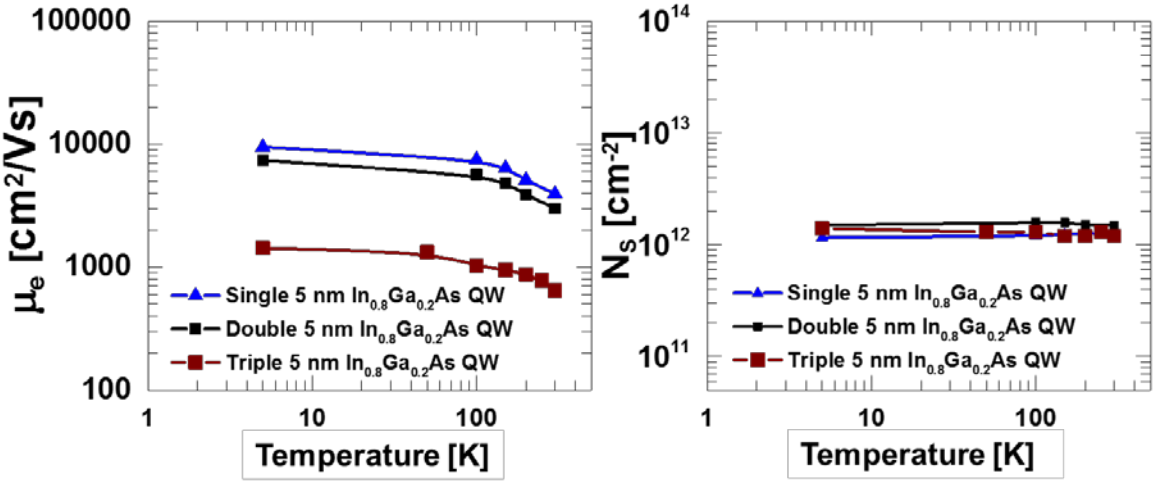


Figure 2.2. Electron mobility and electron density as a function of temperature for single, double, and triple InGaAs quantum-well FinFETs.

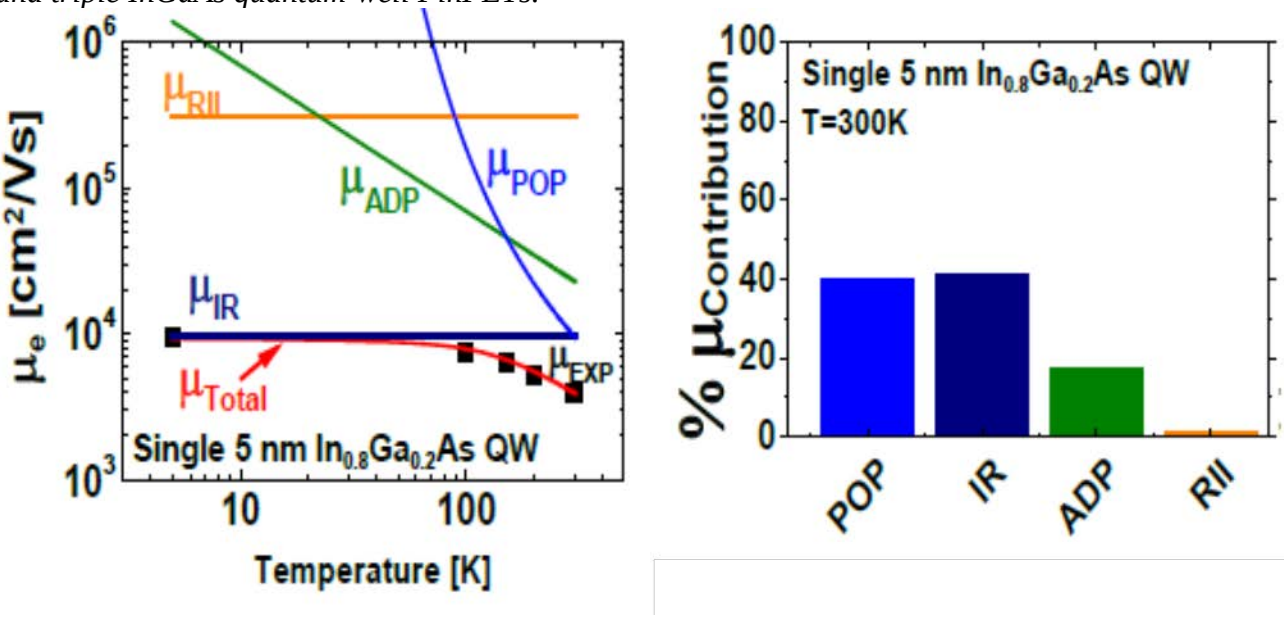
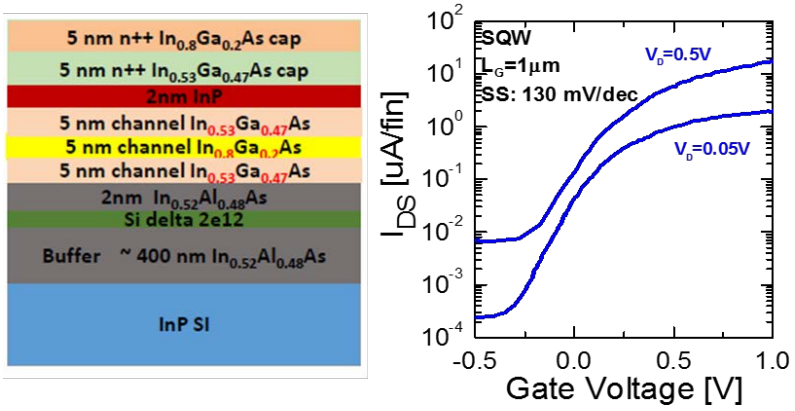
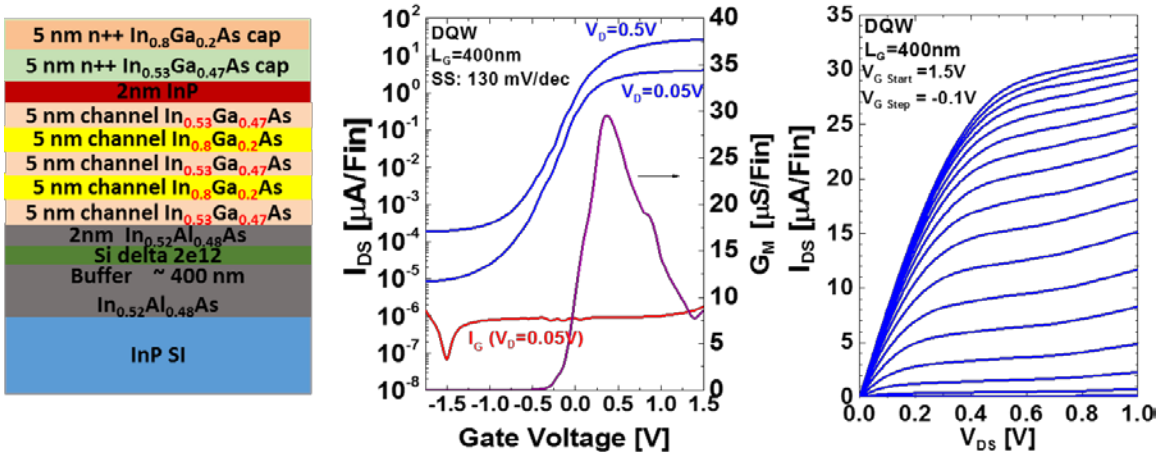
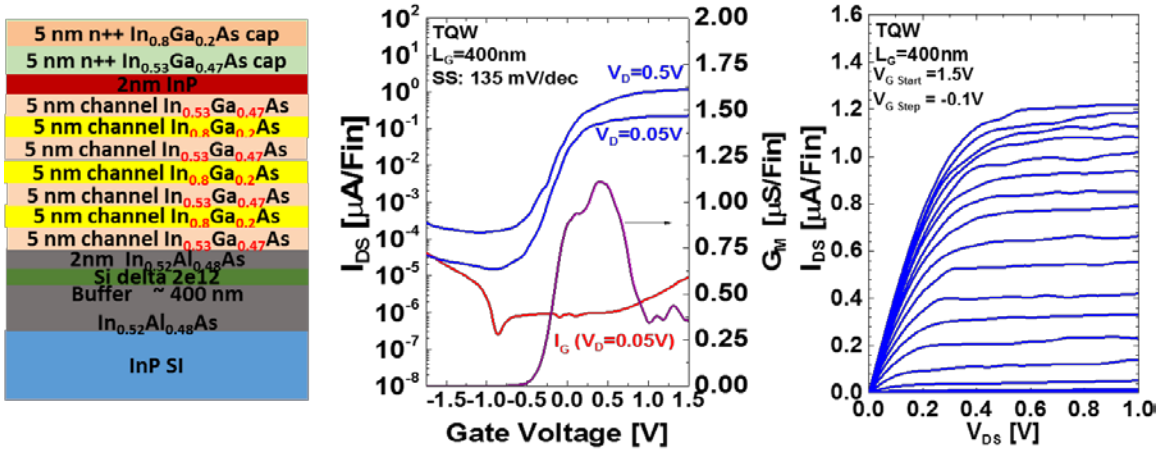


Figure 2.3. Electron mobility due to different scattering mechanisms. It shows that the polar optical phonon and interface roughness limit the electron mobility.

Device characteristics for single, double, and triple quantum-well InGaAs FinFETs are shown in Figure 2.4. Well controlled I_D-V_G and I_D-V_D characteristics are shown for all the devices. Double quantum-well FinFET has the best performance, due to large electron mobility and density. Triple well FinFET shows degraded performance, consistent with the results obtained from Hall measurement. This suggests that double quantum-well FinFETs could be beneficial for future scaling. Pulsed laser testing will be performed on these devices.







Device	$I_{D,LIN}$ [μA/fin]/[μA/μm] (Vg-Vt=1V)	$I_{D,SAT}$ [μA/fin]/[μA/μm] (Vg-Vt=1V)	SS [mV/dec]	$G_{m,\ PEAK}$ [μS/fin]/[μS/μm]
SQW FF	2.25/11.95	16/85.1	130	19.2/102.1

DQW FF	3.6/17.3	19.8/95.2	130	29.7/142.8
TQW FF	0.21/4.83	1.6/7.1	135	1.1/48.3

Figure 2.4. Device characteristics of single, double, and triple quantum-well InGaAs FinFET.

3. Ge MOSFET Technology Development (Stanford)

Experimental work on Ge bulk pMOSFET has been pursued at Stanford University. In order to realize high performance Ge pMOSFETs for testing the electrical behaviors of the devices under radiation exposure, high quality MOS interface on Ge is of paramount importance. Here, we have developed the integration of high-k dielectric (Al_2O_3 and HfO_2) on Ge with GeO_2 as an interlayer (IL) formed by in-situ O_3 treatment. 1st ALD capping with high-k dielectric allows us to control the amount of GeO_2 formed by the in-situ O_3 oxidation in between the high-k dielectric and Ge substrates, which is beneficial in term of the scalability of the proposed gate stack. The lowest interface state density (D_{it}) achieved is 10^{11} $eV^{-1}cm^{-2}$.

3.1 Formation of High-k Gate Stack on Ge with GeO_2 formed by in-situ O_3 treatment

The approach to achieve high quality Ge MOS interface is to insert GeO_2 as IL underneath high-k dielectric. O_3 is more reactive than O_2 so that it forms significant amount of Ge oxides quickly if directly exposed. Therefore, 1st ALD capping with high-k dielectric serves as a diffusion barrier such that the amount of GeO_2 formed can be well controllable.

Figure 3.1 shows the SEM image and the process flow of the proposed high-k gate stack on Ge with GeO_2 interface. Firstly, n-Ge is cyclically cleaned using diluted HCl aqueous solution and 2% HF. Then, the substrate is immediately loaded in ALD chamber in which 1st Al_2O_3 deposition takes place with 10 cycles of TMA precursor and O_3 as oxidant at 400 ℃. As a result, ~1nm Al_2O_3 is deposited. Subsequently, ozone flows into the chamber at 400 ℃ at 9 Torr for 10 min to form GeO_2 below the 1st Al_2O_3. In order to suppress gate leakage, 2nd Al_2O_3 deposition is conducted at 350 ℃ with 90 cycles of TMA precursor and O_3 as oxidant. After that, post deposition annealing (PDA) is performed at 400 ℃ in N_2 ambient for 30 min to anneal out defects and charges in the dielectric. Finally, for the formation of gate electrode, 15nm reactive TiN and 60nm W are deposited by physical vapor deposition (PVD).

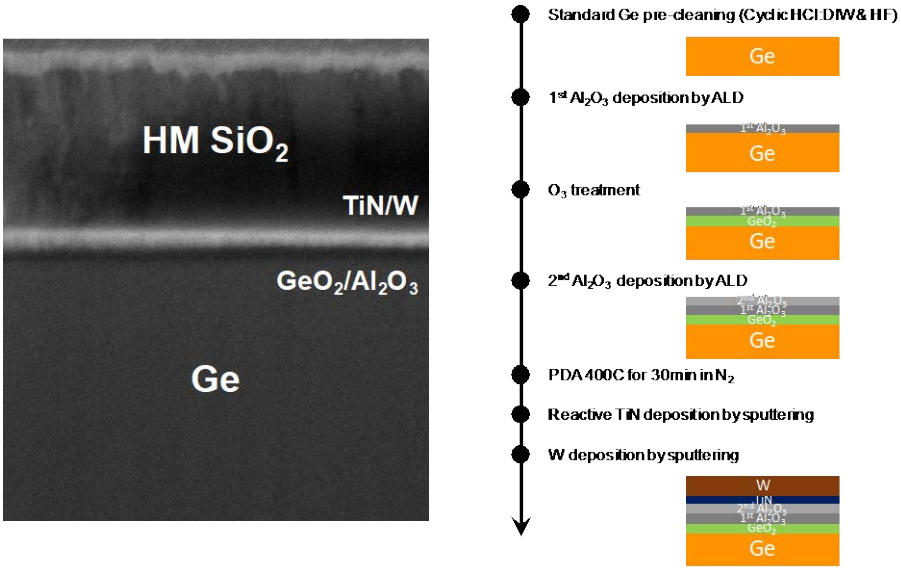


Figure 3.1. SEM image and process flow of high-k gate stack on Ge with GeO_2 interface.

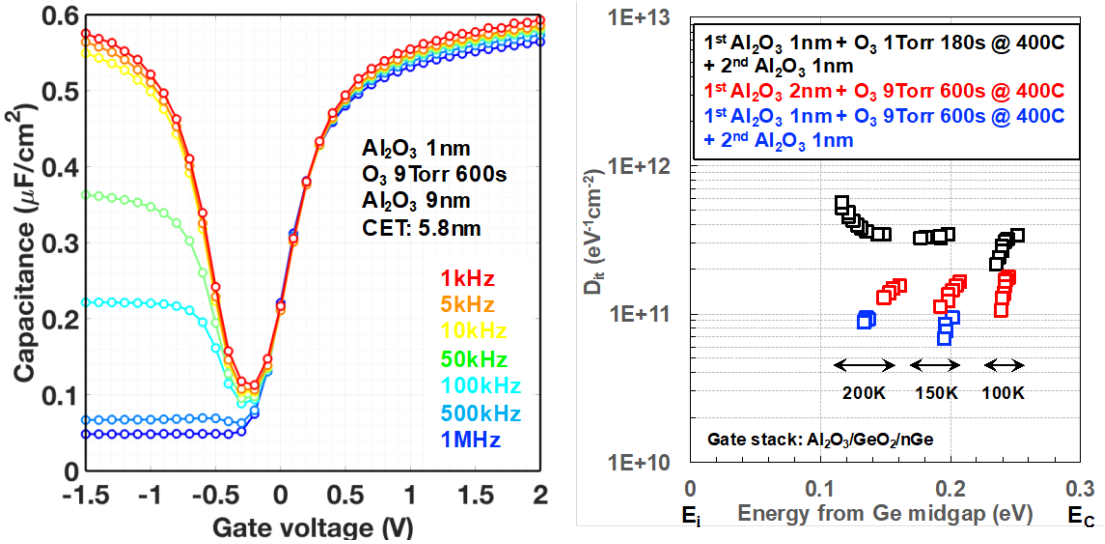


Figure 3.2. C-V characteristics of the proposed high-k gate stack and its interfacial quality quantified by D_{it}.

Figure 3.2 shows the C-V characteristics of the high-k gate stack and the evaluated D_{it} by low temperature conduction measurement. The evaluation of D_{it} was conducted at low temperature to suppress minority carrier response for semiconductor materials like Ge that have small bandgap where weak inversion response leads to a substantial overestimation of D_{it} [1]. As shown in figure 3.2, virtually no frequency dispersion of capacitance in the depletion region and well-modulated surface potential were observed, which is indicative of high quality Ge interface and in order to quantify D_{it}, conductance across the gate stack as a function of frequency was measured at various temperatures (100/150/200K) to be able to analyze the energy distribution of D_{it}. The lowest D_{it} achieved is 10^{11} $eV^{-1}cm^{-2}$.

3.2 Introduction of HfO_2 in Place of 2nd ALD Al_2O_3 dielectric

The proposed gate stack can have variations where 2nd ALD Al_2O_3 can be replaced by higher-k dielectric among which HfO_2 can be introduced to scale equivalent oxide thickness (EOT). It is critical to integrate small EOT gate stack in Ge MOSFETs for future experiments as channel length of devices shrinks.
In fact, the 1st ALD Al_2O_3 layer plays an important role in that it serves as a capping layer for GeO desorption as well as a diffusion barrier that prevents HfO_2 from intermixing with GeO_2. The advantage of having higher-k dielectric is two-fold. Firstly, a physically thicker dielectric can be deposited while maintaining the same electrical thickness, which reduces gate leakage current caused by tunneling which is a dominating factor in aggressively scaled gate oxides. Second, it is less susceptible to plasma damage during gate electrode deposition where energetic Ar species is ion-bombarding thin layers of high-k with a certain penetration depth.
Figure 3.3 shows the C-V characteristics of the high-k gate stack with 2nd Al_2O_3 replaced by HfO_2. The CV curve presents no frequency dispersion of capacitance in the depletion region and well-modulated surface potential as the previous gate stack, which is indicative of high quality Ge interface. It can be inferred that Ge interface is well passivated by the 1st ALD Al_2O_3 with GeO_2 formed by ozone oxidation. To further scale EOT, IL and high-k thickness should be carefully engineered.

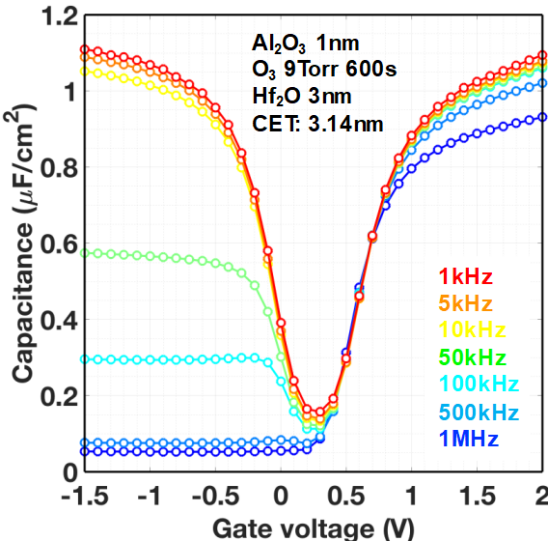


Figure 3.3. C-V characteristics of the gate stack with HfO_2 dielectric.

However, there are two features that are different from the GeO_2/Al_2O_3 gate stack. First of all, there is frequency dispersion in the accumulation region, which is a sign of the high series resistance effect at high frequency. Due to the inferior band offset of HfO_2 compared to Al_2O_3 [2], there is more lateral voltage drop across the gate electrode which can modeled with RLC components in a complex form at high frequency. At high frequency the impedance of L component becomes significant, resulting in larger voltage drop laterally, which manifests as lower capacitance in the accumulation region as denoted by the blue line in figure 3.3. Secondly, the flat band voltage is right-shifted meaning there are more negative charges present in the HfO_2. These negative charges are oxygen vacancies that are intrinsic defects in HfO_2 [3]. Further investigation is required to minimize the defects in the bulk of HfO_2.

3.3 Development of Ge Bulk pMOSFETs with the High-k Gate Stack

For the electrical characterization of devices with the high-k gate stack, Ge bulk pMOSFETs were fabricated with self-aligned metal source/drain (S/D). Figure 3.4 shows the process flow of gate-first self-aligned metal S/D Ge bulk pMOSFETs. First and foremost, the surface of n-Ge is

cyclically cleaned using diluted HCl aqueous solution and 2% HF. Then, the substrate is immediately mounted in ALD chamber in which 1st Al_2O_3 deposition takes place with 10 cycles of TMA precursor and O_3 as oxidant at 400 ℃. As a result, ~1nm Al_2O_3 is deposited. Subsequently, ozone flows into the chamber at 400 ℃ at 9 Torr for 10 min to form GeO_2 below the 1st ALD Al_2O_3. In order to suppress gate leakage, 2nd Al_2O_3 deposition is conducted at 350 ℃ with 90 cycles of TMA precursor and O_3 as oxidant, followed by post deposition annealing (PDA) at 400 ℃ in N_2 ambient for 30 min to anneal out defects and charges in the dielectric. For the formation of gate electrode, 15nm reactive TiN and 60nm W are deposited by physical vapor deposition (PVD). The gate electrode is patterned by using CF_4 + CHF_3 + Ar chemistry. After that, the gate stack in the S/D regions is wet-etched by 2% HF, exposing the surface of Ge. 10nm Ni is deposited by e-beam evaporation followed by rapid thermal annealing (RTA) at 150 ℃ for 1 min to drive Ni into Ge. The remaining unreacted Ni is washed off in HCl aqueous solution and then RTA is performed to stabilize nickel-germanide (NiGe) metal S/D. Metal 1 (M1) S/D/Gate pad is formed by depositing 10nm Ti/100nm Al and the substrate is covered by 300nm high density plasma (HDP) SiO_2 at 90 ℃. In order to make it conducive to wire-bonding for high frequency testing setup, metal 2 layer (M2) with via is processed with 10nm Ti/40nm Pt/120nm Au.

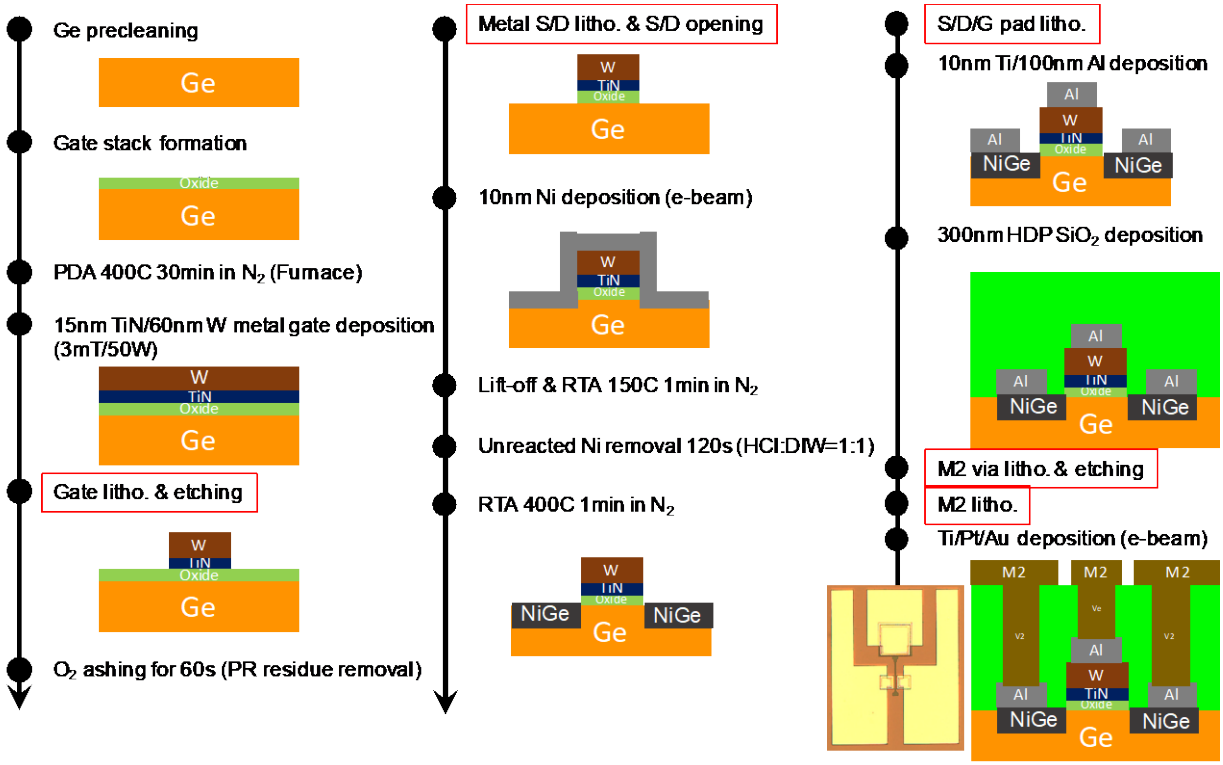


Figure 3.4. Process flow of gate-first self-aligned metal S/D Ge bulk pMOSFETs.

3.4 Electrical Characteristics of the Fabricated Ge Bulk pMOSFETs

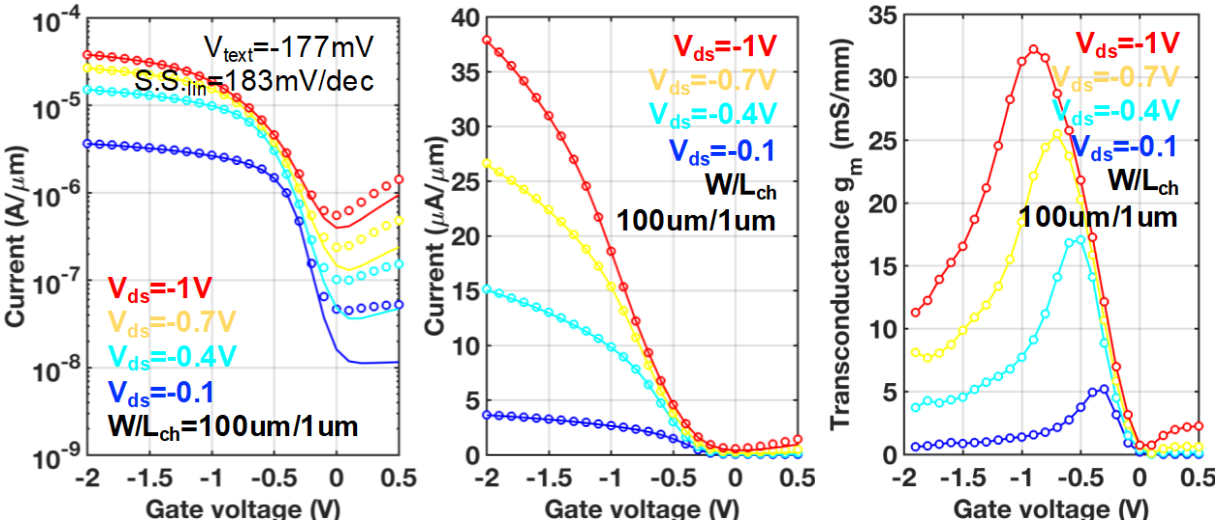


Figure 3.5. I_D-V_G characteristics and transconductance of the Ge devices. (Circles are I_{drain} and solid lines are I_{source}) The difference between them is due to junction leakage, which can be improved by ion implantation S/D. The transconductance of $L_{ch} = 1\mu m$ Ge bulk pMOSFETs amounts to 32.22 mS/mm.

I-V characteristics of the Ge bulk pMOSFETs were measured. Figure 3.5 and 3.6 show the well-tempered I_D-V_G and I_D-V_D characteristics with the thin GeO_2/Al_2O_3 gate stack whose capacitive equivalent thickness (CET) is 2.26nm. There is a slight discrepancy between I_{drain} (circles) and I_{source} (solid lines) because of the poor junction properties of metal S/D. The transconductance of $L_{ch} = 1\mu m$ Ge bulk pMOSFETs is 32.22 mS/mm.

Here, it should be pointed out that the D_{it} extraction by subthreshold slope in figure 3.5 is not an accurate method because junction leakage current is incorporated in the subthreshold current degrading the subthreshold slope. As a consequence, the method overestimates D_{it}. However, the method could be used to a certain extent for evaluating D_{it} if the subthreshold current is measured at low temperature where the junction leakage is well suppressed.

The hole mobiltiy of Ge bulk pMOSFETs at room temperature with thick (CET=5.98nm) and thin (CET=2.26nm) gate oxides is plotted in red and blue, respectively in figure 3.7 together with Si universal hole mobiltiy [4]. The peak mobilities of the thick and the thin gate oxides amount to 382 cm^2/Vsec and 274 cm^2/Vsec, respectively which is 1.8X and 1.3X improvement over that of Si. On top of that, the hole mobility enhancement factor is plotted in figure 3.7 which is defined as

$$mobility\ enhancement\ factor = \frac{\mu_{Ge}}{\mu_{Si}}$$

It is worth noting that the enhancement is kept high at not only low carrier concentration, but also high carrier concentration.

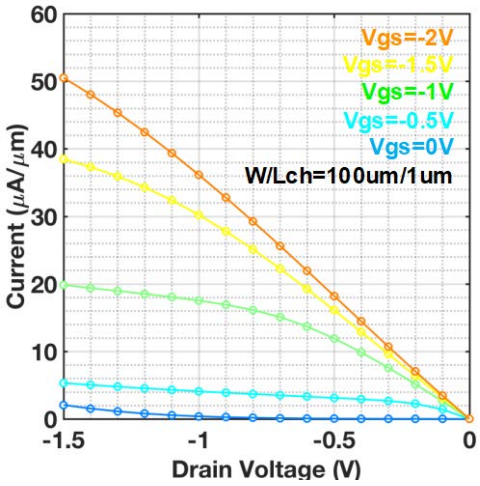


Figure 3.6. I_D-V_D characteristics of the $L_{ch} = 1\mu m$ Ge devices. (Circles are I_{drain} and solid lines are I_{source})

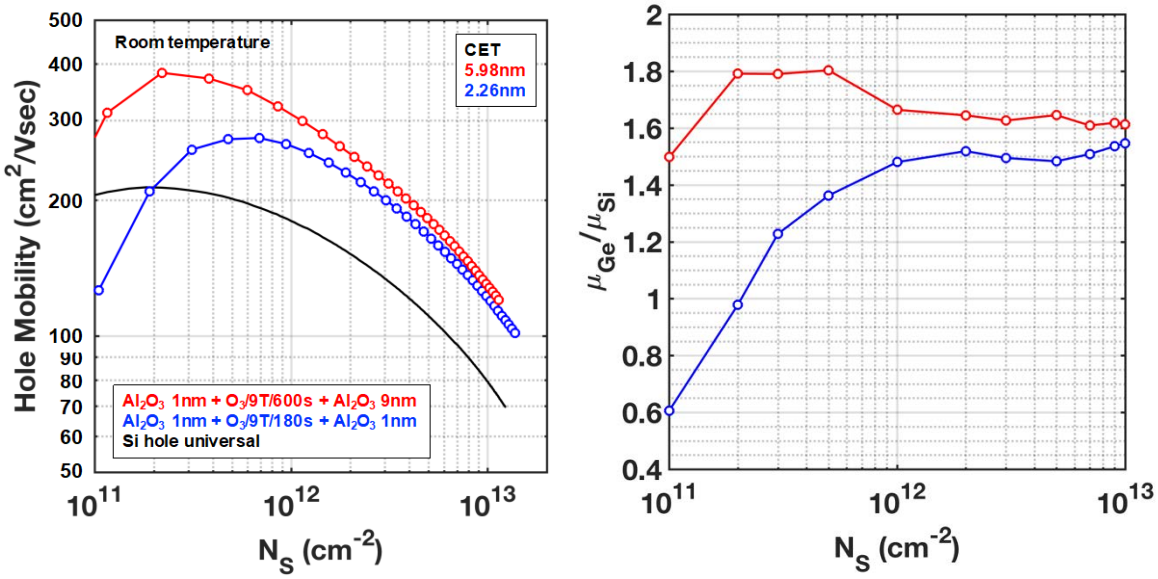


Figure 3.7. Hole mobility of Ge bulk pMOSFETs at room temperature as a function of surface carrier concentration with two different gate oxide thicknesses (CET=5.98nm in red and CET=2.26nm in blue) together with Si universal hole mobility. The peak mobility enhancement of the thick and the thin gate oxides is 1.8X and 1.3X, respectively over that of Si. The enhancement is kept high at both the low and high field regimes.

Reference

[1] Koen Martens et al., "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates.," IEEE TED 55(2) 2008

[2] E. Simoen et al., "The assessment of border traps in high-mobility channel materials.," ECS Trans. 69(5) 2015

[3] J. L. Gavartin et al., "Negative oxygen vacancies in HfO2 as charge traps in high-k stacks," APL 89 2006

[4] S. Takagi et al., "On the universality of inversion layer mobility in Si MOSFET's: Part I – Effects of substrate impurity concentration," IEEE TED 1994;41(12):2357–62.

4. Radiation Testing (NRL)

In order to perform ion- or laser-induced charge collection measurements on MOSFET structures, the devices need to be mounted and wirebonded in high frequency boards. These boards have been designed and procured. The packages have a total 8 transmission lines which have an impedance of 50 ohms to match the input impedance of our high bandwidth 16 GHz Tektronix oscilloscope. Several different transistors on a given sample can be wirebonded in a single HF board depending on whether all terminals are wirebonded or just the gate and drain (source grounded). Electrical connection from the HF board is accomplished using end launch sma connectors (27 GHz) purchased through Southwest Microwave (part# 292-07A-5). These connectors are removable and can be used on other HF boards.

Several devices were prepared for testing but there were many problems in mounting them in the package and wire bonding. Those problems have been resolved and testing will be done in the near future.

Option Year 1

Heavy-ion induced Single Event Transient Testing

The devices investigated in this study are Ge bulk pMOSFETs with self-aligned metal source/drain (S/D). A cross section of the device is shown in Figure 1. The gate oxide is GeO_2/Al_2O_3 gate stack whose capacitive equivalent thickness (CET) is 2.26nm. More specific details of these devices were presented in the previous section. The gate width is 30 μm, gate length is 2 μm. The gate finger is centered between the source drain contacts. I_{DS}-V_{GS} characteristics are shown in Figure 2. The transconductance is 32.22 mS/mm @ W/L_{ch}=100um/1um.

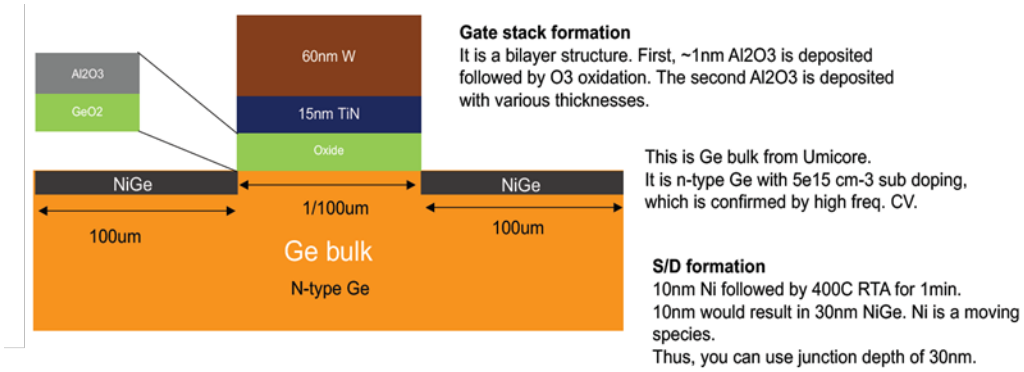


Figure 1. Schematic diagram illustrating the cross-section of a Ge bulk pMOSFET.

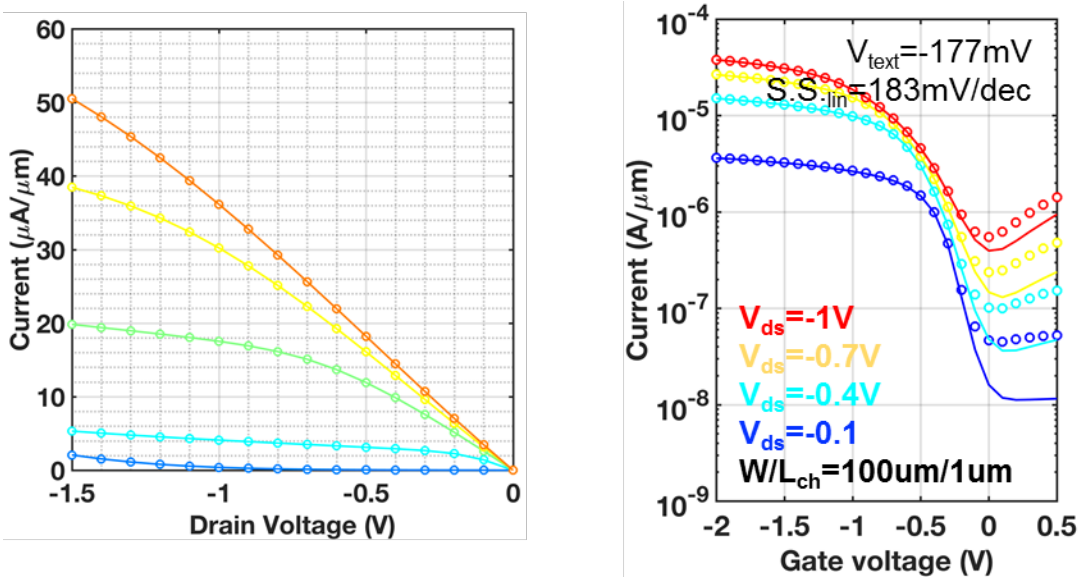


Figure 2. I_{DS}-V_{DS} characteristics for Ge bulk pMOSFETs.

Heavy ion induced single-event transient measurements were performed on Ge bulk pMOSFETs using xenon particles at the Grand Accélérateur National d'Ions Lourds (GANIL). The incident energy at the surface of the device under test (DUT) is 4.3 MeV/amu, and the calculated linear energy transfer (LET) in Ge is 46.21 MeV cm^2/mg using Monte Carlo SRIM simulation. A beam flux of $5x10^6$ ions/cm^2/s was utilized. The device under test (DUT) are mounted in specially designed high-frequency (50 GHz) microwave packages, which have been qualified out to 26 GHz. All connections were made using high frequency (40 GHz) cables and the signals are brought off-chip by the impedance-matched microstrip transmission lines. The gate, drain, and source terminals are wire-bonded to microstrip transmission lines of the package and the substrate grounded. Transients on the gate, drain, and source are measured through 26 GHz bias tees using a Tektronix TDS8200 70 GHz digital sampling oscilloscope with a 50 ohm input impedance. The high-speed bias tees allow the dc bias to be decoupled from the ac transient signal. The oscilloscope was setup to trigger from channel 1 on the drain transients and the trigger level was set to 2.4 mV. This experimental setup allows us to monitor transients generated from single ion strikes. Approximately 400 transients were recorded at each bias condition. The DUT is biased through bias tees at various gate biases, with gate voltages varied from -1.5V (strongly-on) to 1V (strongly-off). The drain voltage was held fixed at -1V for these experiments.

During broad beam heavy ion testing, a distribution of transients are observed which is associated with ion strike location. Drains transients generated from an ion striking on the source side of the gate will be different from generated drain transients for an ion striking on the drain side of the gate. Figure 3 illustrates an example of the drain, gate and source transient captured simultaneously. The exact position where these transients are generated is unknown. There is a rapid rise in current on the drain due to holes collected at the drain. Electrons are collected at the source causing a negative current pulse. For this gate bias, a negative gate transient is generated. The sum of the current generated from these terminals should be equal to zero.

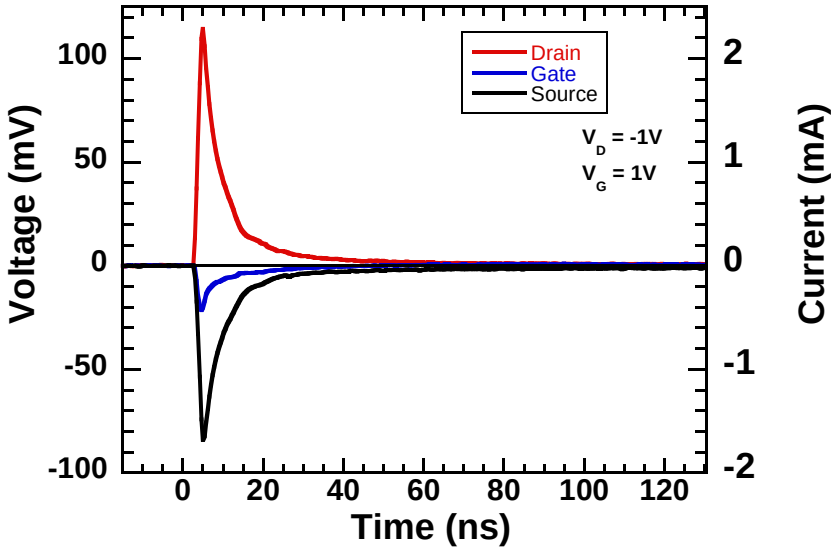


Figure 3. Example of the drain, gate and source transients captured simultaneously for a V_D = -1V and V_G = 1V.

Figure 4 represents the distribution in drain collected charge for V_D = -1V and V_G = 1V. The transients on the right in Figure 4 correspond to different collected charge values which are provided in the legend. These transients vary in amplitude. The collected charge is calculated by integrating the transient over 200 ns temporal windows for the present data set). The transient peak or maximum amplitude for each gate bias is shown in Figure 5. There is almost no gate bias dependence for drain transients but slight dependence for source and gate transients for V_G ranging from 0 to 1V. The maximum collected charge was extracted from each distribution of transient events and plotted as a function of gate bias in Figure 6. Similar to the maximum amplitude, there is essentially no gate bias dependence for the drain collected charge but a slight dependence for source and gate transients for V_G ranging from 0 to 1V.

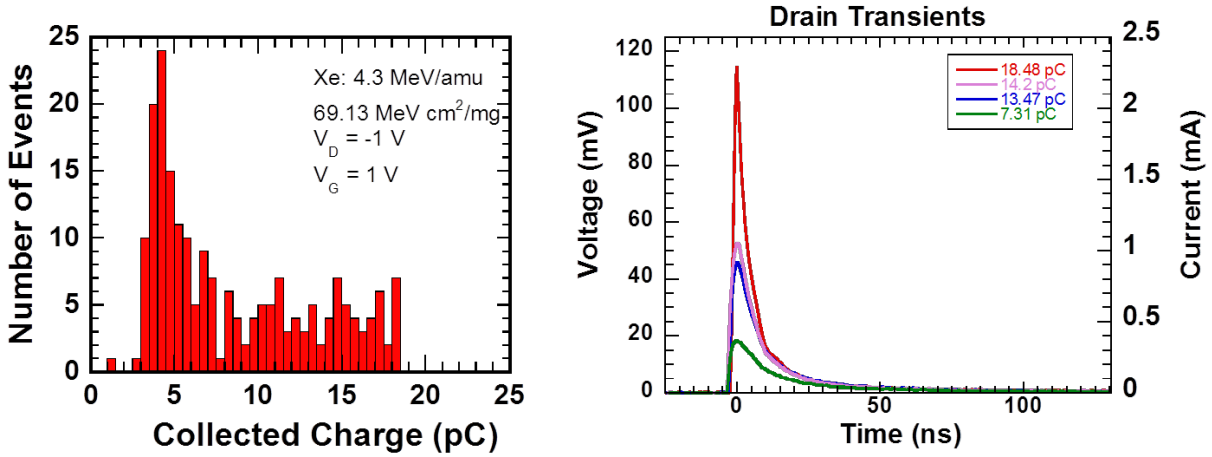


Figure 4. Histogram representing the distribution in drain collected charge for V_D = -1V and V_G = 1V. The transients on the right correspond to different collected charge values which are provided in the legend.

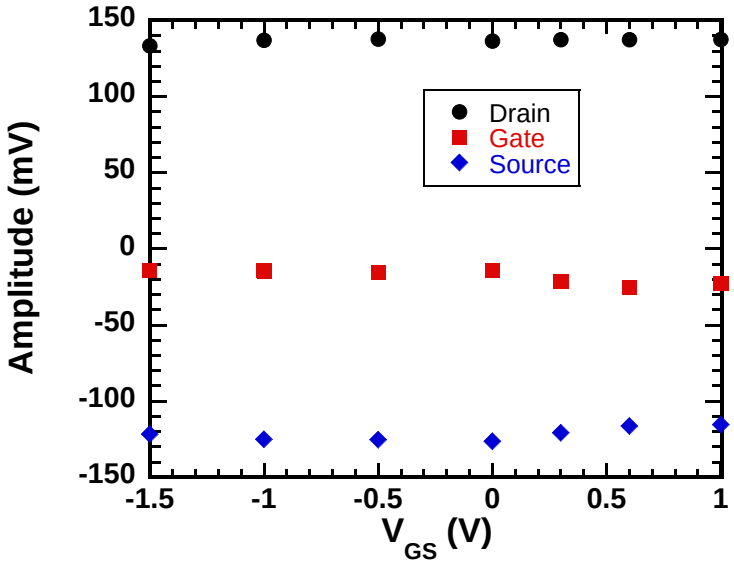


Figure 5. The maximum amplitude as a function of gate bias.

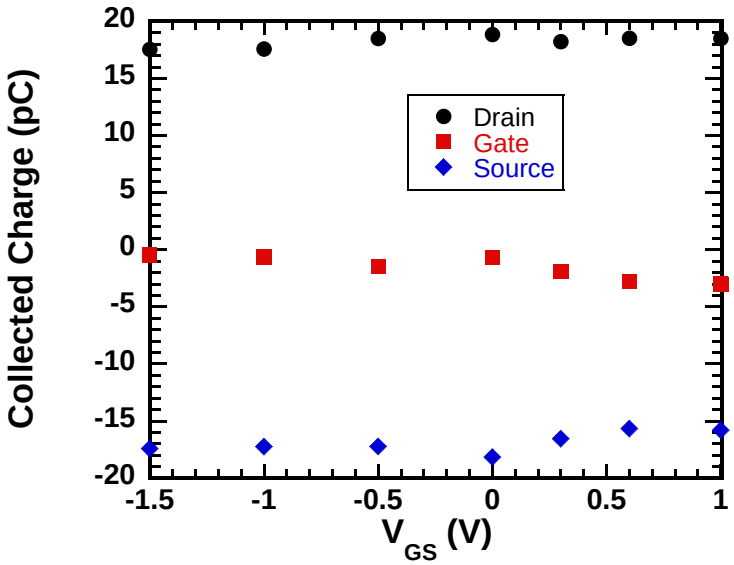


Figure 6. The maximum collected charge as a function of gate bias.

The full distribution of collected charge values for the drain, gate and source at each gate bias are summarized using dot plots as illustrated in Figure 7. The maximum or mean collected charge for the drain or source is relatively independent of gate bias. However, the mean collected charge for the gate changes from positive to negative as the gate bias changes from -1.5V to 1V. Also, for a gate bias of -1.5V, the collected charge ranges from negative to positive values. This data suggests the peak of the gate transients are changing sign. For V_G = -1.5V, the drain, source and gate transients which resulted in a negative gate collected charge are shown in Figure 8. Indeed, the gate transient is negative. The gate transient does go positive around 30 ns before decaying to 0. For the same gate bias but for a positive gate collected charge value, the corresponding drain, source and gate transients are shown in Figure 9. The gate transient is positive and so the gate transients change sign for V_G = -1.5V. The reason for this change in sign of the gate transients is explained using TCAD simulations. There is also a bipolar behavior observed for the drain

transient and the source transient is very broad compared to the source transient in Figure 8. The ion strike location that generated these transients is not known so TCAD simulations can be used to suggest which side of the gate the ion strike occurred.

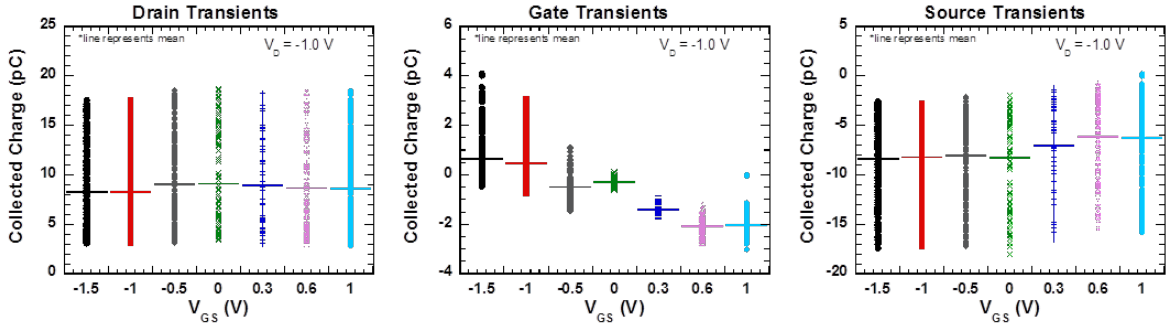


Figure 7. Dot plots representing the distribution of collected charge values for a given gate bias condition for the drain, gate and source. The horizontal lines represent the mean values.

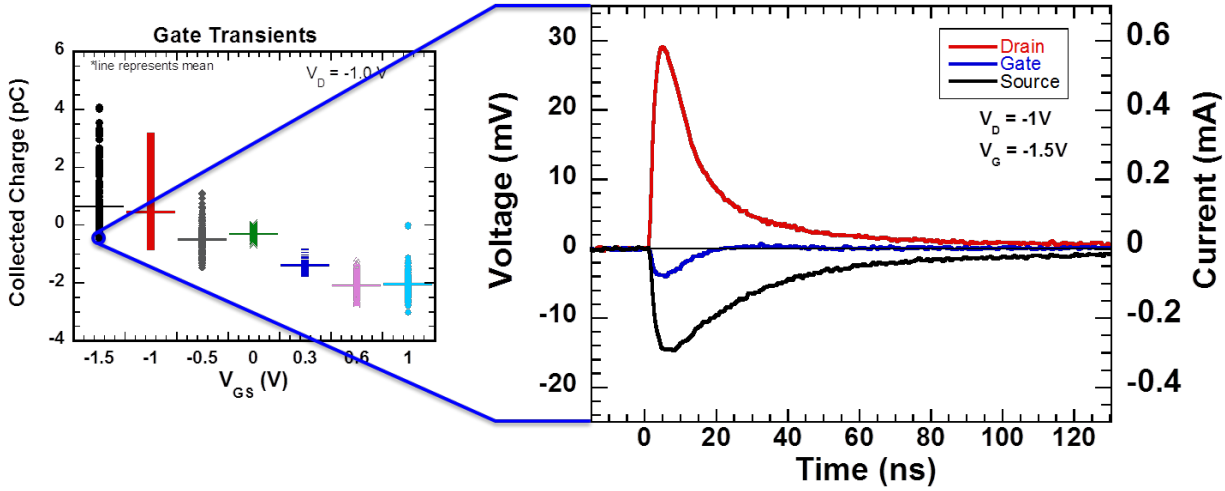


Figure 8. For a negative collected charge value on the gate, the corresponding drain and source transients are compared. These transients were recorded for a bias condition of V_D = -1V and V_G = -1.5V.

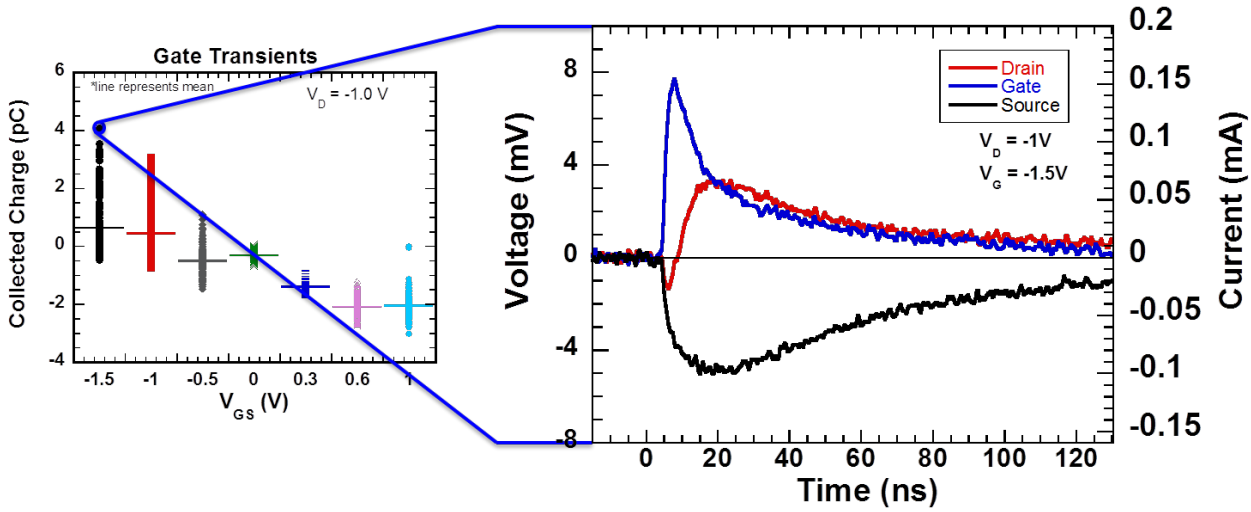


Figure 9. For a positive collected charge value on the gate, the corresponding drain and source transients are compared. These transients were recorded for a bias condition of V_D = -1V and V_G = -1.5V.

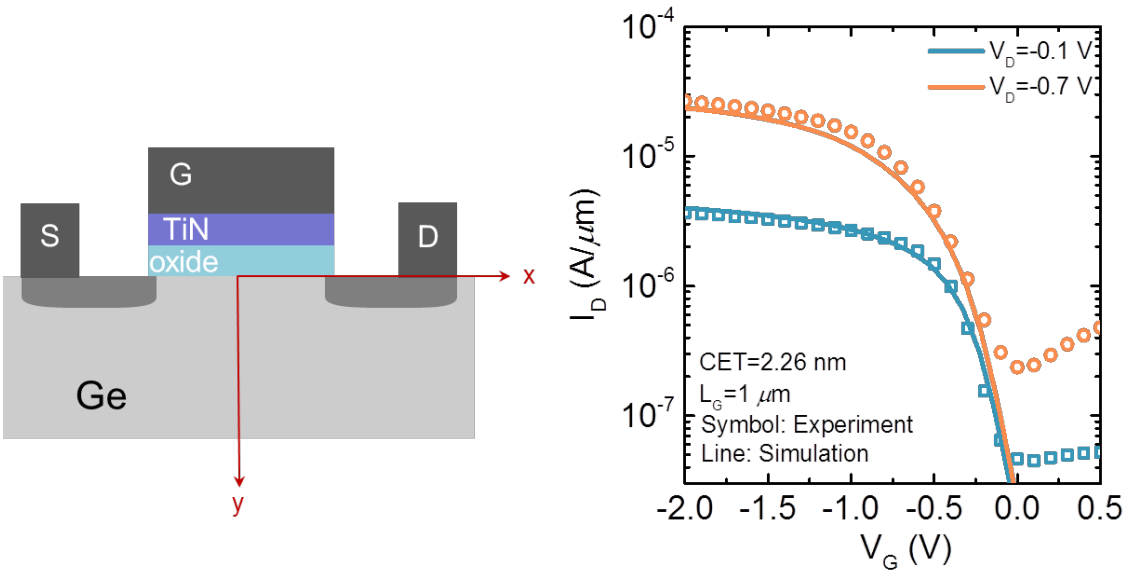


Figure 10. A cross section of the device and a comparison of I_D-V_G characteristic for measured and simulation.

Two-dimensional (2D) Sentaurus TCAD modeling is employed to study the charge deposition, carrier transport, and transient response. A 2D model was calibrated to the measured I-V characteristics illustrated in Figure 10. Figure 11 are the band diagrams corresponding to inversion, depletion and accumulation conditions. Figure 12 are the simulated transients as a function of gate bias for an ion strike on the drain side of the gate. No gate bias dependence is observed for the source or drain transients for a drain side strike. The gate transients exhibit a bipolar behavior and are associated with displacement current. The gate transients do not change much with gate bias. These simulations were repeated assuming the ion strike was on the source side of the gate. The results are shown in Figure 13. A weak gate bias dependence is observed for the source and drain transients. Gate transient are also generated for an ion strike on the source side and the displacement gate current increases with an increase in gate bias. For inversion, an ion strike on the source side typically generates a negative transient current (positive voltage signal) consistent with the experimental data.

Figure 14 shows the time evolution of the valence band energy along the X-direction in accumulation (V_G = 1V) for an ion strike on the drain side (left plot) and the source side (right plot). The gate finger is centered at x = 0 μm. The curve labeled 1 ps corresponds to the pre-strike condition because the ion strike is centered at time t = 1 ns. Prior to the ion strike, there is a barrier between the source and the drain for hole transport. At time t = 1.2 ns, an ion strike on the drain side causes this barrier to fully collapse essentially causing a temporary channel formation so that holes are injected from the source to the drain. This barrier slowly begins to recover even after 8 ns. However, for an ion strike on the source side, at t = 1.2 ns there is still ~ a 70 meV barrier so fewer holes are injected from the source to the drain. Therefore, the transient current is smaller for an ion strike on the source side transient than the drain side. The source and drain transients are much broader for an ion strike on the source side than they are for a drain side strike due to the longer transit times. This broadening of the source and drain transients are observed in the

experimental data. It could be assumed that the transients in Figure 8 originated from a drain side strike and a source side strike for the data in Figure 9.

For other device technologies studied in the past, such as GaAs and Sb-based MOSFETs, the collected charge (shape and amplitude of the transients) usually changes with gate bias in contrast to the current data set. The data in Figure 15 represents the hole current density after an ion strike at the peak of the transient current. The red arrows are the hole current density vectors. For both inversion and accumulation, a significant hole current flow occurs in the channel and deep into the Ge substrate. The gate control over the channel is temporarily lost and significant current flows from source to drain freely which explains why the collected charge is relatively independent of the gate bias.

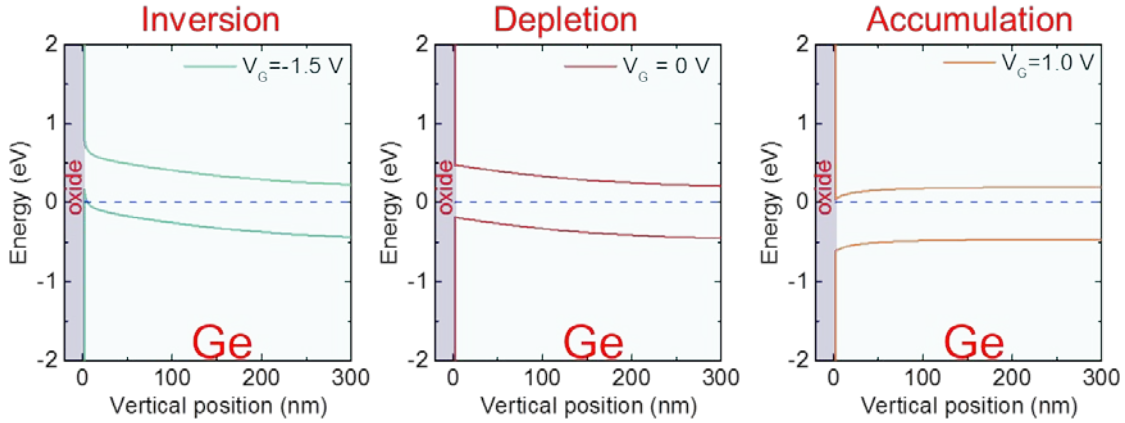


Figure 11. Band diagrams corresponding to inversion, depletion and accumulation.

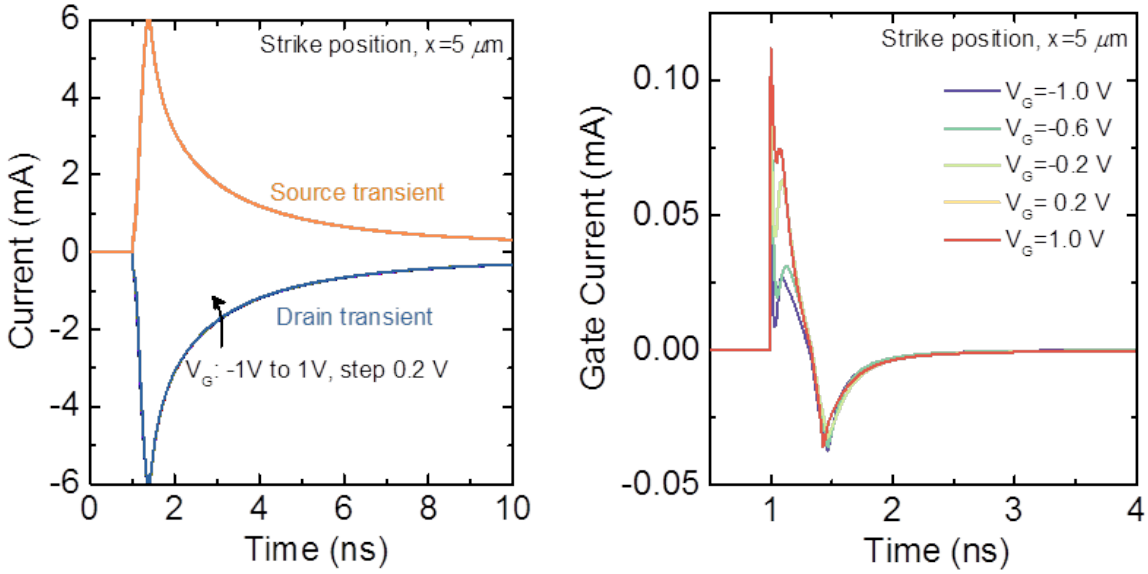


Figure 12. Simulated transients as a function of gate bias assuming the ion strike was on the drain side of the gate.

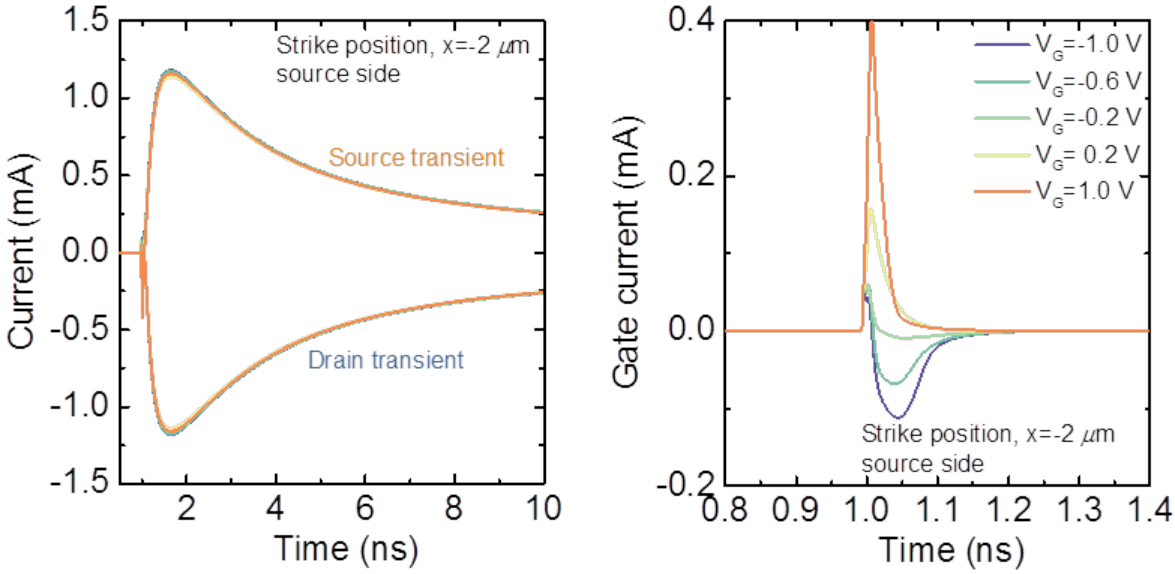


Figure 13. Simulated transients as a function of gate bias assuming the ion strike was on the source side of the gate.

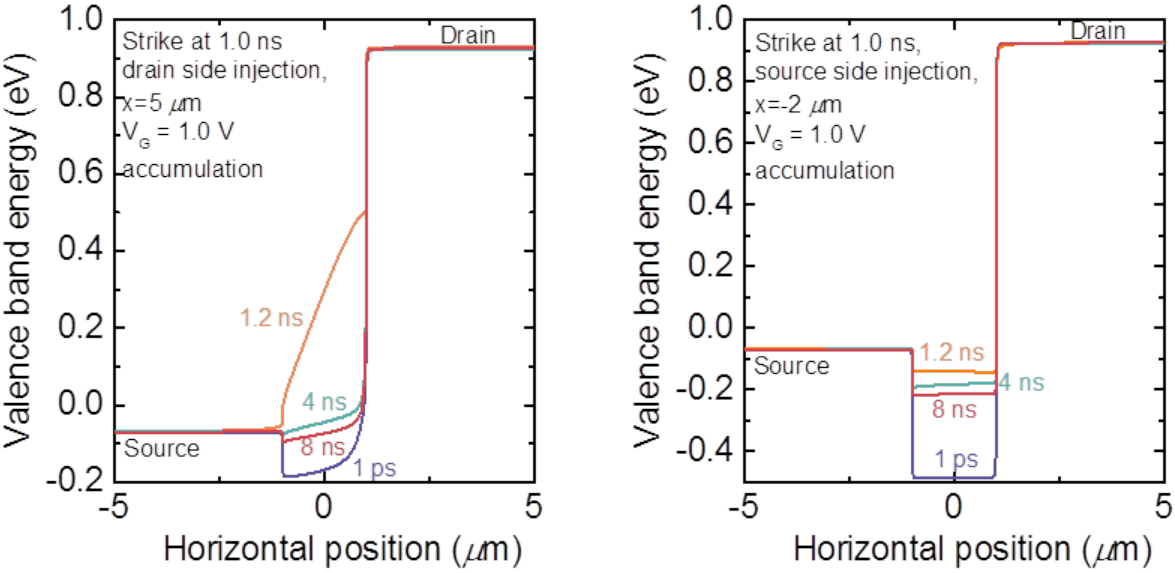


Figure 14. Valence band energy as a function of horizontal position for an ion strike on the drain side (left plot) and an ion strike on the source side (right plot). The center of the gate finger is located at x = 0 μm.

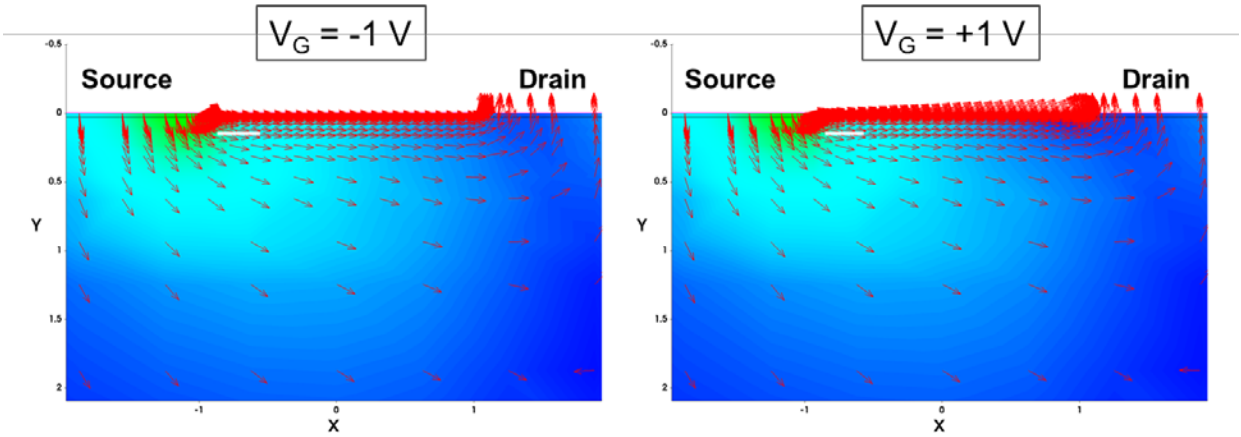


Figure 15. Hole current density as a function of position. The red arrows are the density vectors.

The charge collection response for the Ge pMOSFETS was compared to Sb-based pMOSFETs that have an identical device geometry. These devices were irradiated with Xe particles having an LET in Ge and Sb of 46.2 and 39.55 MeV cm^2/mg, respectively. The peak of the transient for the Ge pMOSFET is significantly larger than the Sb-based pMOSFET. The LET was slightly larger for the Ge MOSFET but this difference cannot account for the increase in peak height. Integration of the transients result in a collected charge of 18.77 pC for the Ge MOSFET compared to 0.829 pC for the Sb pMOSFET, a 23X improvement in the collected charge for the Sb-based technology. The primary difference in these technologies is that the Ge is a bulk structure and the Sb is a quantum well structure where the channel thickness is only 10nm so the active volume is very minimal. Industry is very interested in using Ge for pMOSFET and InGaAs for the nMOSFET. After comparison to Sb-based technology, the Ge transient have a much larger transient peak and full-width-half-maximum, which leads to more collected charge. If we want to develop a radiation hardened technology using alternate channel materials, we either need to use the Sb-based materials or improve the radiation response of Ge. For this reason, we will be investigating Ge gate-all-around nanowire FET.

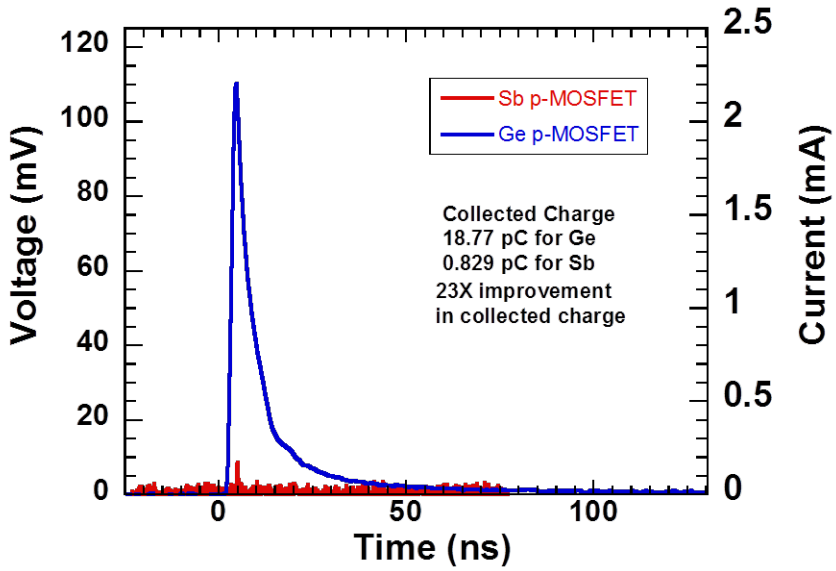


Figure 16. Comparison of the transient response for Ge pMOSFETS is compared to Sb pMOSFETs that have identical device geometry. The heavy ion LET for the Ge and Sb MOSFETs were 46.2 and 39.55 MeV cm^2/mg, respectively.

The SET cross section was calculated for each gate bias by dividing the number of events by the particle fluence and plotted in Figure 17. The SET cross section slightly increases with increasing gate bias. The SET cross section is significantly larger than the device cross section (the active area includes the source and drain contact regions) of 1800 μm^2. This suggests that ion strikes outside of the device contact region can generate transient events. Transient simulations were performed assuming that an ion strike occurred at various distances from the gate as shown in Figure 18 by the closed circles. It is observed that transients are generated at these locations and the transient current decreases for an increase in distance from the gate. The simulations are consistent with the experimental observations. The SET cross section being significantly larger than the physical area of the transistor means this particular device geometry is more sensitive to SETs. In order to improve the SET response, a reduction in the SET cross section is required. To improve the SET cross section, we need to isolate the transistor from the surrounding Ge bulk, e.g., FinFET or surround gate nanowire FET. In order to improve the SET cross section and the charge collection response as previously mentioned, development of Ge nanowire FETs has been underway. Heavy ion and laser-induced transient measurements will be performed in option year 2.

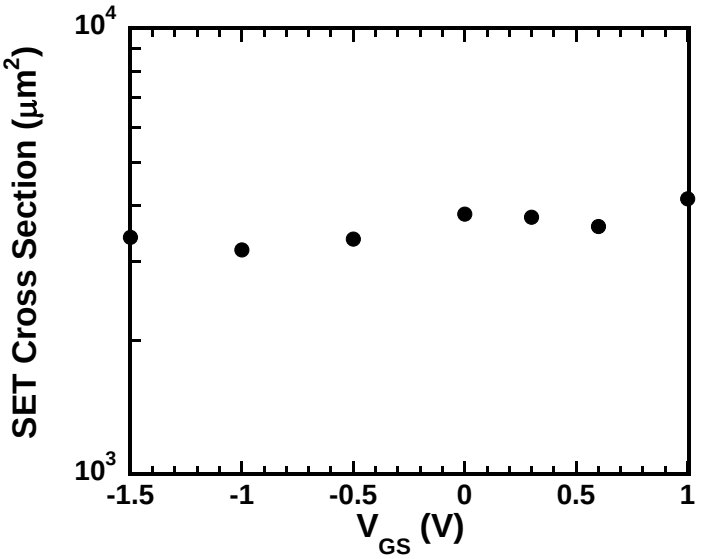


Figure 17. SET cross section as a function of gate bias.

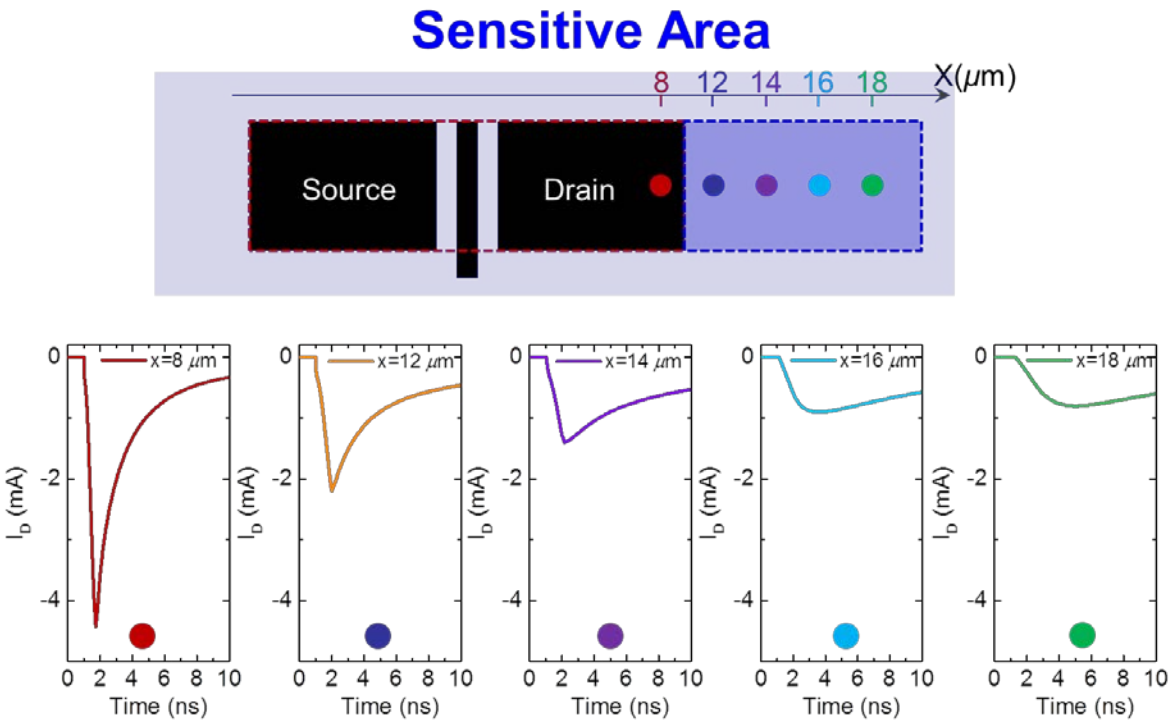


Figure 18. Transient simulations for ion strikes at different locations away from the drain contact.

Ge MOSFET Technology Development: High mobility vertically stacked Ge gate all around (GAA) device structure

Ge gate-all-around (GAA) FETs are very attractive because of their ability to provide high current drive per unit area. Several techniques have been investigated for incorporating Ge on the Si platform such as Smart Cut process [1], direct wafer bonding [2], aspect ratio trapping and lateral Ge overgrowth on SiO_2 [3,4], and Ge condensation [5]. Among these latter two are most appealing techniques because of their excellent compatibility with the incumbent Si CMOS technology, low defect count and the ease of controlling the thickness of GOI layer. We have already demonstrated the aspect ratio trapping and lateral Ge overgrowth on SiO_2 during our previous effort. In this program we are working on Ge condensation technique for vertically stacked horizontal Ge GAAFETs (Fig. 19).

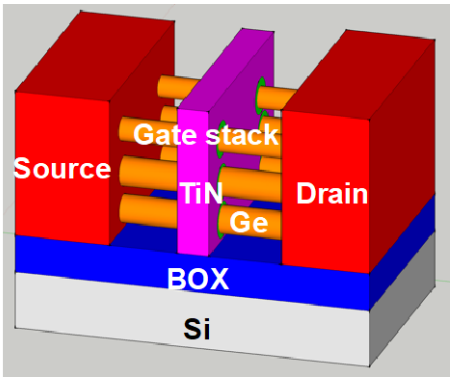


Fig. 19: Vertically stacked horizontal channel Ge gate-all-around (GAA) FET.

We propose a novel method to fabricate highly scalable 3D multi-stacked SiGe/Ge GAA structure by Ge condensation. The technique enables Ge to be incorporated on the Si platform where high mobility channel material is needed with the ease of controlling critical dimension (CD) of GAA. SiGe/Ge nanosheet (NS) or nanowire (NW) configuration can be made by properly choosing epitaxial SiGe thickness and linewidth by lithography. It should be pointed out that Ge is condensed in channel while source and drain remain Si-rich SiGe due to Si sandwiched by SiGe layers, which offers compatibility with the incumbent Si CMOS contact technology.

Ge condensation is composed of epitaxial growth of SiGe layers on SOI substrates and successive thermal oxidation. As thermal oxidation proceeds, Ge atoms diffuse toward BOX and are segregated at the SiO_2/SiGe interface whereas Si atoms are selectively oxidized because of the larger negative Gibbs free energy of forming SiO_2 compared to GeO_2. When all the Si atoms are dry-oxidized, high quality pure GOI is formed (Fig. 20).

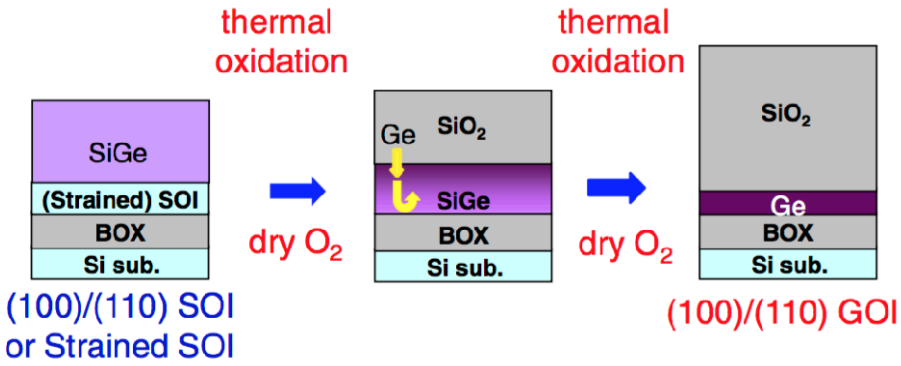


Fig. 20: Ge channel formation by Ge condensation technique.

Looking ahead to 5nm node and beyond, the ultimate GAA device architecture is highly desirable to achieve maximum gate controllability, which can potentially be realized by Ge condensation. By having a sequence of SiGe epitaxial growth with Si capping layer, patterning, and successive thermal oxidation, vertically stacked horizontal Ge GAAFETs can be fabricated, which enables higher drive current in a limited footprint. The conceptual process flow of Ge GAA is outlined in Fig. 21.

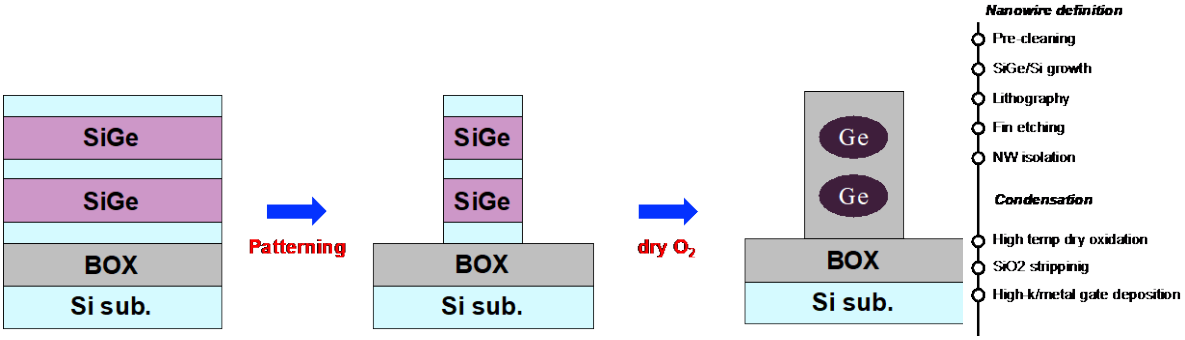


Fig. 21: Vertically stacked horizontal Ge GAA by Ge condensation technique.

During the first 6 months of the option year 1 of this project, we experimented with this technology and demonstrated vertically stacked Ge nanosheets. During the last 6 months we have optimized this structure.

There have been reports on vertically stacked GAA [6] Ge NWs where either Ge is directly grown on Si [7] or strain relaxed buffers (SRB) are used to grow high quality strained Ge. [8,9,10]. However, the proposed method is a simpler approach to fabricate 3D multi-stacked Ge GAA structure without the need of SRB. Also, by the virtue of Ge condensation, high temperature oxidation results in high quality SiGe and Ge as well as the channel being compressively, which is promising for pMOSFETs. [5]

The key process steps are delineated in Fig. 22. SiGe/Si multilayer channel is epitaxially grown on (100) n-Si, which determines the number of SiGe channels horizontally stacked. In our experiment, $Si_{0.70}Ge_{0.30}$ is grown below its critical thickness as shown in Fig. 3.9. Narrow fin is defined and SiGe channel is released by TMAH. Ge condensation is performed at various temperatures to achieve Ge-rich SiGe or pure Ge. It is worth noting that source and drain are Si-rich SiGe even after Ge condensation because Si sandwiched by SiGe is not removed in S/D.

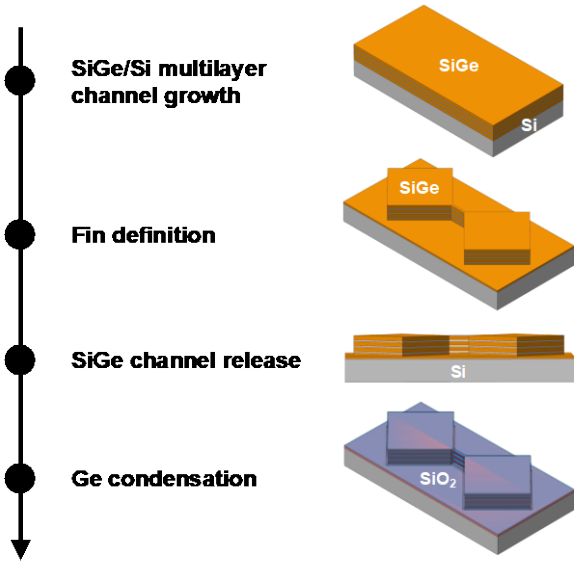
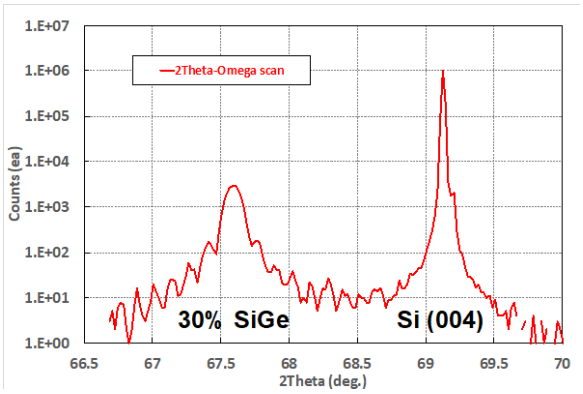


Fig. 22: Process flow of 3D multi-stacked Ge gate-all-around (GAA) structure fabricated by Ge condensation.

Fig. 23 shows that high quality pseudomorphic $Si_{0.70}Ge_{0.30}$ layer below critical thickness is grown on Si substrate, which is corroborated by XRD. The grown $Si_{0.70}Ge_{0.30}$ is compressively strained and complaint to Si substrate.



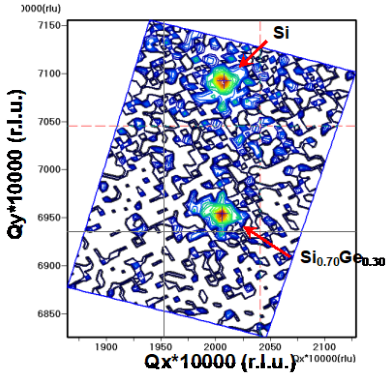


Fig. 23: X-ray diffraction (XRD) data confirming that high quality pseudomorphic Si0.70Ge0.30 is grown (interference fringes) and compliant to Si substrate without relaxation.

Raman spectroscopy is used to evaluate Ge composition during Ge condensation. As shown in Fig. 24 the evolution of Ge-Ge and Si-Ge peaks in SiGe is recorded as Ge condensation progresses. From the blue curve (bottom) to the red one (top), one can observe that Ge-Ge signal becomes stronger nearing 300 cm^{-1} whereas Si-Ge signal vanishes as the SiGe layers are being condensed to pure Ge.

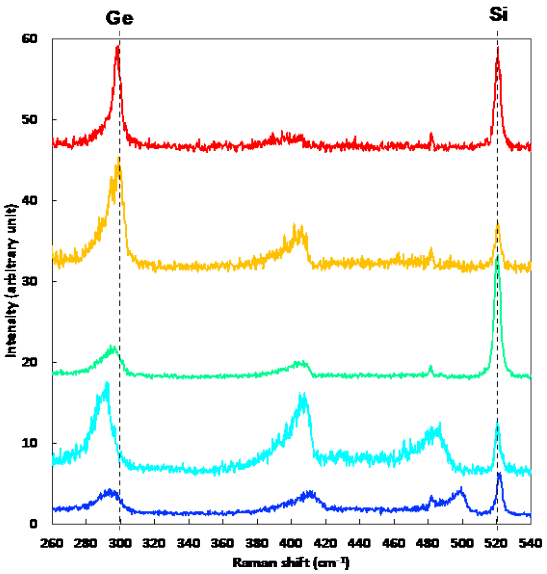


Fig. 24: Raman spectroscopy data showing the evolution of Ge-Ge and Si-Ge peaks in SiGe as Ge condensation proceeds.

Fig. 25 shows the resultant 3D multi-stacked Ge GAA structure. The method is highly scalable in terms of the number of SiGe/Ge GAA stacked. It is worth noting that various shapes of GAA structure such as NS and NW can be made by properly choosing the epitaxial SiGe thickness from the beginning and linewidth by lithography.

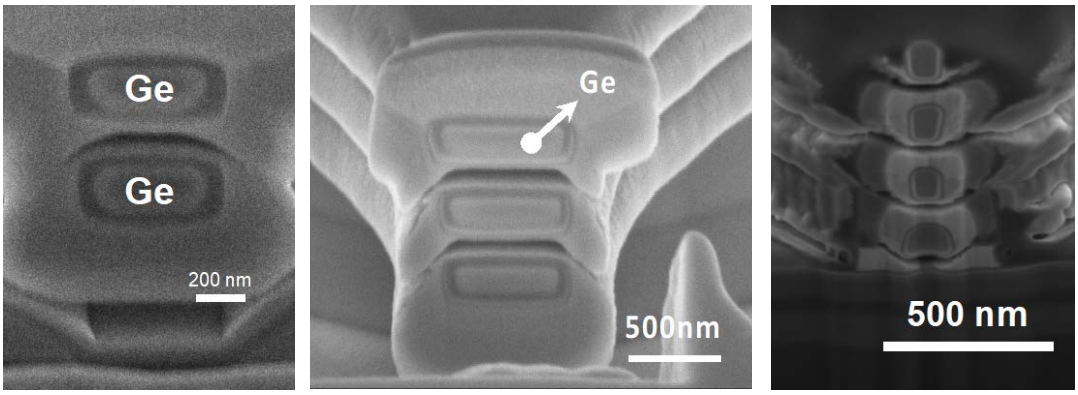


Fig. 25: SEM images of various shapes of GAA structure fabricated by Ge condensation. Ge composition ranging from 30% (initial Ge content) to 100% can be achieved.

It should be highlighted that GAA channel becomes compressively strained as Ge condensation progresses because S/D remains Si-rich SiGe (30%) while Si atoms are being rejected by high temperature oxidation and replaced by Ge atoms in the channel whose lattice

constant is bigger than that of Si. As a result, Ge channel is compressively strained by rigid body of $Si_{0.70}Ge_{0.30}$ in S/D which is also compressively strained by Si substrate.

Fig. 26 is an example of 4 suspended $Si_{0.25}Ge_{0.75}$ NWs. By STEM along the axis of NW length (the red dotted line), Ge composition is measured to be 75% in the channel whereas 30% Ge is found in S/D as can be seen in Fig. 26. This allows the proposed structure to have great compatibility with the incumbent Si CMOS contact technology because source and drain remain Si-rich SiGe.

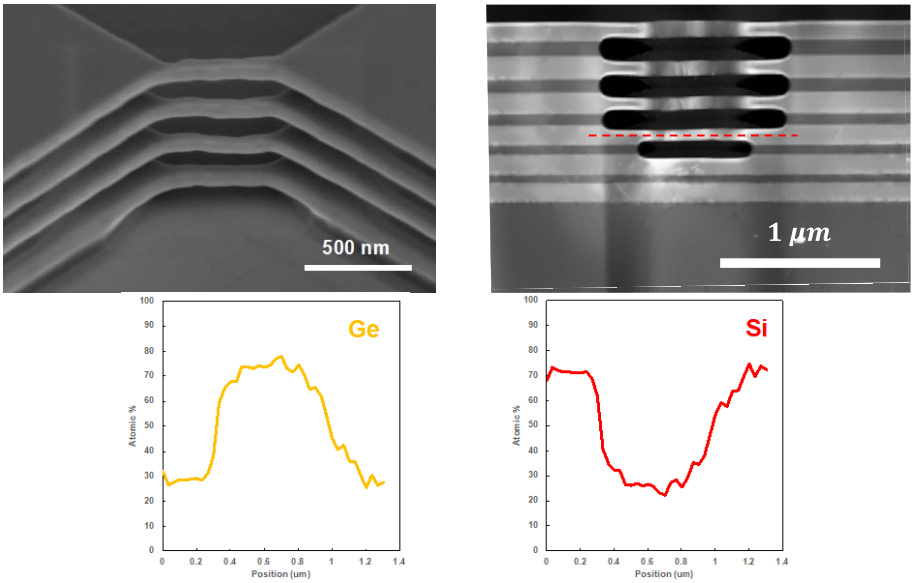


Fig. 26: SEM and TEM images of 4 suspended $Si_{0.25}Ge_{0.75}$ NWs and Ge composition along the axis of GAA length by STEM.

Strain analysis of the suspended NW is performed by convergent beam electron diffraction in 4D-STEM (Fig. 27). It is found that the $Si_{0.25}Ge_{0.75}$ NW retains ~1.2% compressive strain at the center of NW and there is a slight decrease of the strain towards S/D. It is plausible that the region with smaller strain acts as a buffer to accommodate higher amount of compressive strain in the middle of NW. Thus, the center of the channel is kept highly strained. The high amount of compressive strain is beneficial to boost hole mobility of Ge in the proposed GAA device architecture. We will demonstrate electrical characteristics of devices in the future.

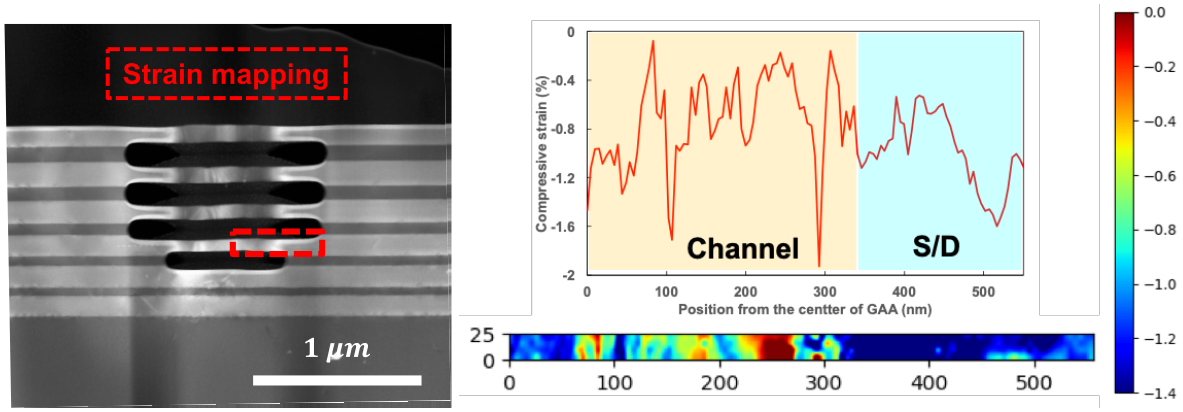


Fig. 27: 4D-STEM strain analysis by convergent beam electron diffraction (CBED). It is observed that the peak of compressive strain is located at the middle of NW and there is a slight decrease of the strain towards S/D.

In summary we have proposed a new technique for fabricating a pure Ge Gate All Around (Ge GAA) MOSFET in a 3-D multi-stack multi-finger device architecture on bulk material. This method is highly scalable vertically, easy to fabricate, and compatible with current silicon CMOS technology. It also eliminates the need for expensive fine lithography because Ge condensation allows making small diameter nanowire by oxidation which is a slow/controllable process. A small dimension nanowire is desirable for better electrostatic control over a channel and high gate controllability.

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