March 16, 2020

ATTN: Defense Technical Information Center

Re: Contract N00014-16-1-2990; Development of a 600 MHz, 0.3 MW Power Combining System Using RF LDMOS Power Transistors

Subject: Submission of Final Technical Report

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This submission is made in accordance with the data item 31. REPORTS of this contract. Distribution has been made as directed in the contract and as shown below.

Sincerely,

Jin Joo Choi
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Kwangwoon University
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Abstract

The objective of the project is to develop all solid-state, compact RF power combining system which generates HPM (high power microwave) coherent radiation with sub-megawatts level high peak power at UHF frequency band (400 ~ 600 MHz).

The SSPA based power combiner system consists of 4 major parts: (1) high-efficiency, 1 kW and 2 kW LDMOS solid-state-power-amplifiers (SSPA), (2) high-power capable 160 ports, cavity power combiner with high combining efficiency, (3) 40-way equal-amplitude, equal-phase power divider, and (4) water-cooled RF load.

We have designed and tested a 1 kW SSPA and a 2 kW SSPA module. The 1 kW RF LDMOS power transistor used in this work is the push-pull type transistor commercially available from NXP. Two RF output signals amplified from the push-pull type transistors were combined through a matched strip line balun. All the input and output impedance transformers were obtained and optimized for maximum output power from analytic theory and numerical simulations using 3-dimensional EM simulator (HFSS) and non-linear circuit simulator (ADS), followed by input/output impedance measurements of cold-test PCB circuits using a calibrated vector network analyzer. RF test on the 1 kW SSPA showed output power of > 1 kW, gain of > 16 dB, and DC/RF conversion efficiency of > 60 %. Two of the 1 kW SSPAs were combined through a Gysel power combiner in order to make a 2 kW unit module for the use in the cavity power combiner. Experiments showed output power of > 2 kW, gain of > 15 dB, and drain efficiency of > 50 % where insertion losses from both circulator and Gysel combiner were included.

A cavity power combiner was designed to be resonant at 460 MHz with a TM_{010} mode. The designed cavity is a cylindrical cavity with diameter = 50 cm and height = 25 cm. In order to meet a critical coupling condition (equivalently, maximum combining efficiency), analytic equations were set to predict cavity Q and initial cavity coupling parameters. HFSS was used to perform numerical simulations and optimize cavity parameters and coupling antennas. The cavity combiner has 160 input ports (magnetic loop antennas) and one output port (6-1/8" coaxial transmission line). Cold-test measurements showed that measured power combining efficiency of both 40-way and 80-way power combiner was more than 97 %, which agreed well with HFSS simulation result.

In order to maintain a high combining efficiency in the cavity combiner, equal phase and equal amplitude of all the input drive signals should be guaranteed at the entrance of the cavity combiner. A 40-way radial power divider was designed by using analytic theory and 3-D EM simulator. The divider consists of 10-way radial power divider and 2 stage cascaded Wilkinson power dividers. Measurements showed -16.3 dB with an amplitude variation of within 0.5 dB and isolation of -31 dB between output ports, indicating a good power/phase balance and an excellent RF isolation.

A water-cooled RF dummy load was designed and fabricated. Dielectric properties of the coolant (tap water and tap-water mixed with solium molybdate) were measured in order to accurately design a matching transformer between the air-filled 6-/18" coaxial transmission line and water-cooled RF load. Measurements showed a return loss of < - 16 dB, which was in good agreement with HFSS simulation results.

Following extensive efforts on fabricating 80 identical 2 kW SSPA modules and installing them on the cavity power combiner, a power combiner system was constructed and successfully tested. The RF power combiner produced a peak RF output power of 100 kW at 464 MHz with 1.2 % bandwidth for the case of forty 2kW SSPA modules and 200 kW at 467 MHz with 2 % bandwidth for the case of eighty 2 kW SSPA modules. Measured power combining efficiency was found to be more than 95 % for both cases. Simulation predicts that power combining efficiency remains > 95 % even if 160 SSPA modules are combined through the cavity power combiner. The unique characteristics of the innovative power combiner system are its compactness and extremely low power loss, making it possible to obtain an unmatchable power combining efficiency.

Acknowledgement

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I would like to acknowledge many graduate students and undergraduate students of High Power Microwave Engineering Laboratory. I thank Dr. Kwangho Jang, Dr. Boki Kim, Joo-Young Park, Sooyeon Park, Yelim Heo, Hyong-Min Seo, Hyun-Tae Park, Cheol-Heon Lee, Hyun-Jin Kim and Hyun-Jun Kim for their dedicated efforts on this successful completion of this project.

Chapter 1. Introduction

Many military high-power-microwave (HPM) systems demand MW and GW-level high output power and highly efficient RF sources in the UHF frequency range (30MHz to 1 GHz). Vacuum-tube based HPM sources, such as relativistic magnetron, reltron, backward-wave-oscillator (BWO), virtual-cathode-oscillator (Vircator), and relativistic klystron amplifier (RKA) demonstrated excellent performances in generating power from sub MW to tenths of GW with DC-RF energy conversion efficiency ranging from a few to 30 percent [1].

Recently, the rapid advancements of commercial RF high-power transistors such as silicon LDMOS (Laterally Diffused Metal Oxide Semiconductor) FET and GaN HEMT (High Electron Mobility Transistor) enabled to replace the conventional vacuum tubes in some applications for radar, electronic warfare, high gradient accelerator, communications, and industrial RF heating system. Solid-state power amplifier (SSPA) has many benefits over the vacuum tube such as low supply voltage, small size, long lifetime, high reliability and low cost. Table 1 summarizes pros and cons of solid-state transistor and vacuum power tube available in the UHF frequency range.

Table 1. Comparison of solid-state transistor and vacuum power tube

	Vacuum tube	SSPA
supply voltage	high voltage (10,000 ~ 100,000 V)	low voltage (50 V)
X-ray	Needs to shield	No X-ray
magnet	Needs for beam focusing	No magnet
Vacuum pump/power supply	Needs for ultra high vacuum	No vacuum system
RF power	MW ~ GW	kW per packaged transistor
DC-RF conversion efficiency	> 60 %	> 60 %
System size/weight	Bulky/heavy	Compact/light
Cost	high	medium
reliability	good	very reliable

Despite many advantages of solid-state devices, the individual transistor produces a maximum kW-level output power, which is considerably low compared with MW-level power of

the vacuum tube. Therefore, power combining is the only solution to obtain a MW-level or, higher power HPM source.

One of the key parameters in designing the power combiner is the high combining efficiency with low RF loss in the combiner. As shown in Figure 1, there are two types of power combiners: binary combiner and spatial combiner. Typical 3 dB, 2-way power combining techniques such as Wilkinson power combiner and branch-line coupler suffer from significant power loss when a number of transistors are combined in cascade. The power loss increases as the number of transistors increases, according to α^k where $k = log_2 N$, α is the loss per stage, and N is the number of transistors. The combining efficiency drops to 80 % and 63% when the number of device elements is 10 and 100, respectively, where the loss per stage is assumed to be 0.3 dB (typical). Therefore, the binary combining technique is not suitable for combining a large number of transistors due to large RF insertion loss.

A spatial power combiner is one of the promising candidates as a high efficiency, solid-state based power source. As shown in Figure 1(b), the spatial power combiner combines output powers from a number of transistors with the use of simultaneous multiple input signals in an enclosed metallic cavity or distributed waveguide structure. It works the same as a phased array antenna combining RF power in a free space. Differently from the binary combiner, the combining efficiency of the spatial power combiner remains constant independent of the number of transistors. Over the past decade, significant progress has been made in spatial power combining of low power MMIC devices for enhancing combiner's efficiency in University of California, Santa Barbara and University of Michigan [2]. Combined power from 10s W to 10s kW was reported in S, X, Ku, Ka frequency bands. A coaxial-type spatial power combiner with peak output power of 75 kW at 352MHz is currently in operation with a low duty cycle at the European Synchrotron Radiation Facility (ESRF) in France [3]. Innovative research work demands the development of RF power combiner with a high combining efficiency capable of MW-level high output power with a high duty cycle.

During the past 3 years, High Power Microwave Engineering Laboratory, Kwangwoon University developed all solid-state, compact power combining system with peak output power of 0.2 MW operating at 467 MHz. The unique characteristics of an innovative power combiner is its compactness and extremely low power loss, making it possible to obtain an unmatchable power combining efficiency of more than 95 %. This final report is composed of 11 Chapters. Design works including SSPA, power combiner/divider, and RF diagnostic-related devices are described in Chapter 3, 4, 5, 6, 7, 8, and 9. Experimental results and analysis on 40-way and 80-way power combiner systems are described in detail in Chapter 10 and 11.

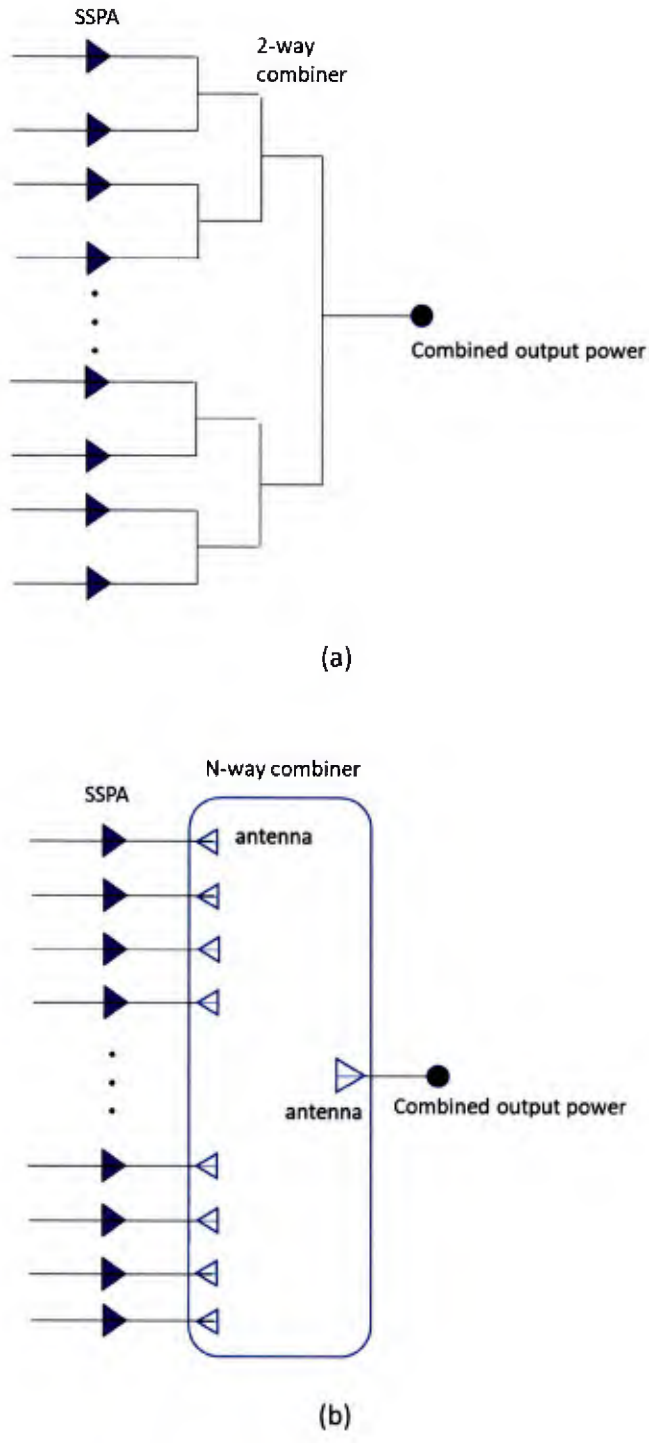


Figure 1. Two types of power combiners: (a) binary combiner and (b) spatial combiner

Chapter 2. Overview of power combiner system

2.1 Design specification

The SSPA based power combiner system consists of 4 major parts: (1) high-efficiency, 1 kW and 2 kW LDMOS solid-state-power-amplifiers (SSPA), (2) high-power capable 160 ports, cavity power combiner with high combining efficiency, (3) 40-way equal-amplitude, equal-phase power divider, and (4) water-cooled RF load. Research goals of the SSPA based power combiner system are as follows:

- Design of 1 kW, 460 MHz LDMOS SSPA with high gain and high efficiency
- Design and test of 2 kW SSPA module
- Design and fabrication of a 160-way cavity power combiner with high combining efficiency of > 95%.
- Design and fabrication of N-way power divider with low loss
- Experimental investigation and analysis of power combiner system operating at 200 kW peak power with variable duty cycle
- Thermal analysis on SSPA module and RF components
- Building RF diagnostics and control units
- Design and fabrication of high power RF dummy load

The specification of the power combiner system is as follows.

EM specification:

- Center frequency 460 MHz
- Bandwidth 1 ~ 2 %
- Output power 0.2 MW (peak power)
- Operation mode Pulsed
- Duty cycle Variable (0.1 % to 30 %)

Device specification:

- Solid state device 1 kW RF LDMOS power transistor (NXP)
- Drain bias voltage 50 V
- Gate bias voltage 2.5 V
- SSA gain 16 dB
- SSA drain efficiency > 60 %
- Combiner type Cylindrical cavity (TM_{010} mode)
- Combining elements 40 (1 x 40), 80 (2 x 40), 120 (3 x 40), 160 (4 x 40)

- Divider — Microstrip line radial and Wilkinson dividers
- Combining efficiency — > 95 %
- Divider loss — < 0.5 dB
- Total system efficiency — > 50 %
- RF output — Coaxial transmission line (6-1/8")
- System size — 120 cm x 220 cm x 170 cm (not including a rack)

2.2 Power budget

We need to amplify RF signal through multi-stage solid state amplifiers from a dBm level low power signal source. Since our target power level is 200 kW (83 dBm), we need to fill with cascaded multi-stage gain amplifiers between the signal source and the cavity power combiner. A power and gain budget plan of each amplifier stage should be carefully made for a required total power gain.

A basic RF unit module connected to the power combiner is the SSPA with output power of 2 kW. The cavity power combiner combines RF power from eighty 2 kW SSPA modules, which require a total drive power of 8 kW. Each 2 kW SSPA module requires an input RF signal of 100 W. Considering a signal generator's power, RF power losses in divider, combiner, circulator, and line losses, we arranged multi-stage gain amplifiers in order to drive the eighty 2 kW SSPA modules. Power budget required at each amplifier stage is shown in Figure 2.

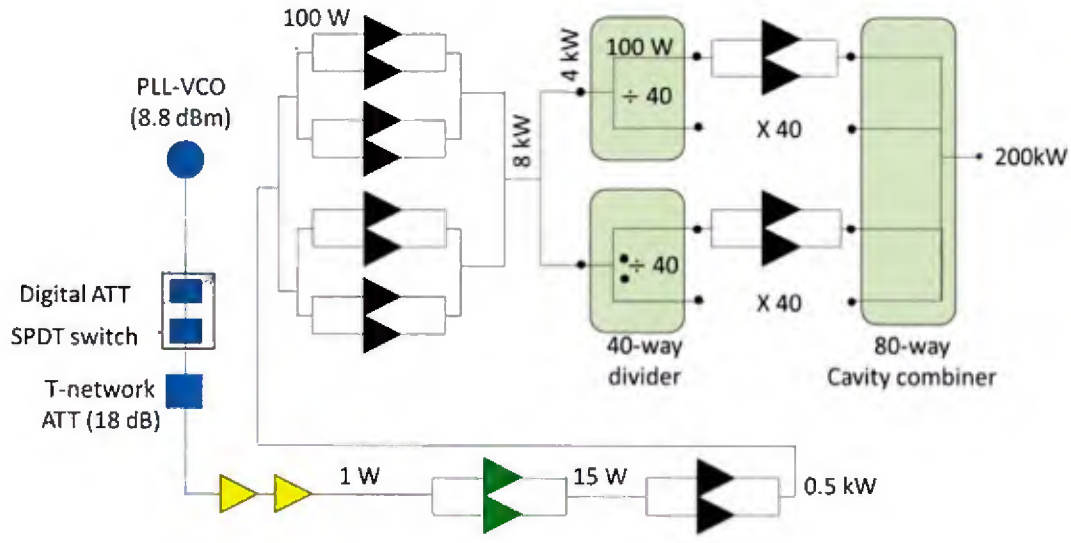


Figure 2. Power budget required at each amplifier stage

2.3 System layout

A CAD drawing for the power combiner system is shown in Figure 3. Key components of the power combiner system are

- 2 kW SSPA modules (x 80)
- Cavity power combiner
- Power divider (x 2)
- Drive amplifier (5 stage)
- PLL-VCO
- RF digital switch
- 5-bit RF attenuator
- 60 dB directional coupler
- High power RF load
- Computer with programmable control/monitoring software (VEE, Discovery2)

AC electrical power required for the power combiner system operating at duty cycle = 30 % is 220VAC, 150 kW. Cooling water (inlet temperature = 10 degree C, flow rate = 10 lpm) should be supplied.

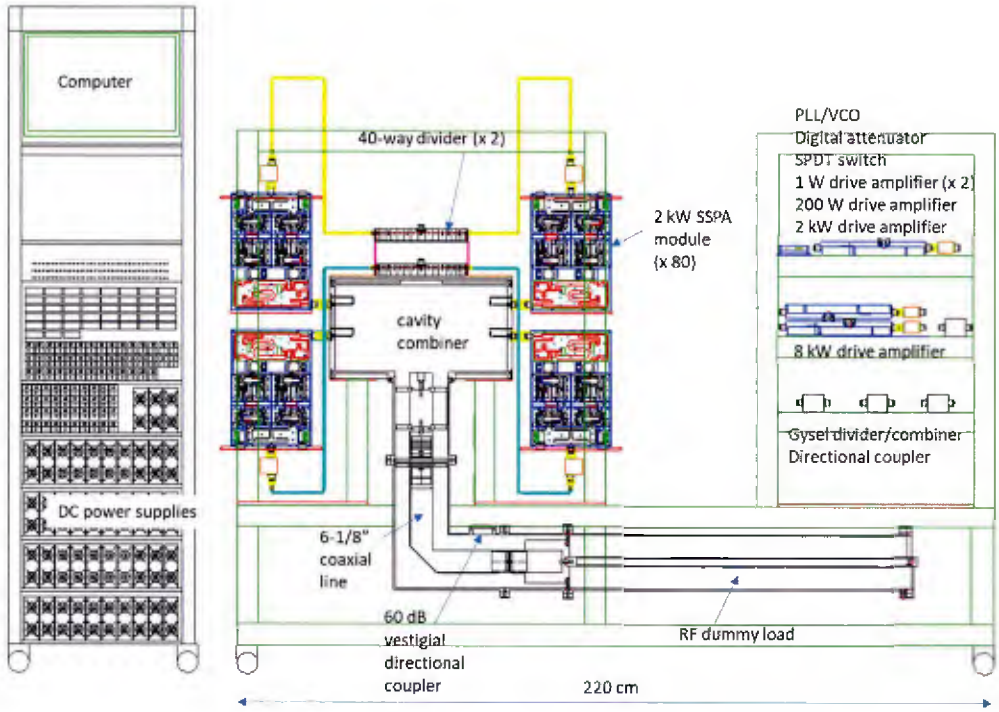


Figure 3. CAD drawing for the power combiner system

Chapter 3. 1 kW solid-state power amplifier (SSPA)

The RF power transistors applicable for the present project should have high output power (> 1 kW), high gain (> 16 dB), high efficiency (> 60 %), and most importantly high reliability. Although GaN chip meets the requirements, we chose the RF power LDMOS transistor manufactured by NXP (formerly Free Scale Inc.) because of low cost (< 0.2 $/W). LDMOS transistor works well up to 4 GHz. However, power amplifier operating at more than 4 GHz needs GaN transistor because power and gain of LDMOS FETs drop drastically above 4 GHz.

3.1 Design and numerical simulation

The NXP 1 kW transistor (MRFE6VP61K25HR6: 1.8 – 600 MHz, 1,250 W CW) is the push-pull, high ruggedness N-channel enhancement-mode lateral MOSFET designed for use in high VSWR industrial, broadcast, aerospace and radio mobile applications [4]. The NXP LDMOS FET is known to be very robust to external high load reflection (maximum VSWR = 65). Any transistor can be damaged and failed by harsh operating conditions, such as high junction temperature due to insufficient cooling and high surge voltage or current on drain and gate terminals. The NXP datasheet shows that a nominal RF performance of the transistor is output power = 1 kW (CW), gain = 18 dB, drain efficiency = 58 % at 500 MHz where drain voltage = 50 V, quiescent current = 100 mA (deep class AB), and source and load impedance are 0.29 + j 1.47 ohm and 1.79 + j 1.80 ohm respectively, at 500 MHz.

The design procedure of the 1 kW SSPA is the followings. All the design parameters were obtained from rf analytic theory and numerical simulations using 3-dimensional EM simulator (HFSS [5]) and non-linear circuit simulator (ADS [6]). Based on the circuit parameters obtained from the theory and numerical simulations, RF cold-test circuits were fabricated using our in-house fabrication etching equipment. Cold-test measurements on rf frequency responses such as rf return losses and circuit impedances were performed and thoroughly examined by the use of a high precision calibrated vector-network-analyzer (VNA). A final circuit layout was employed on a gold-plated printed-circuit-board (PCB) with grounded via holes for better rf performance and reliable fabrication.

We have designed a 1 kW SSPA through an extensive numerical analysis using ADS and HFSS simulation tools. The first step in designing SSPA is to find source and load impedances through the source and load pull simulations at the frequency we are interested in, or 460 MHz. Figure 4 shows the ADS layout for DC I-V curve and DC I-V curves for various gate voltage. Gate voltage was set at 2.21 V for the quiescent current of 100 mA. Figure 5 plots simulation results of load pull and source pull, showing constant power contours and constant efficiency contours on real and imaginary reflection coefficients. Simulations predicted output power = 60.73 dBm, and efficiency = 70.7 % at normalized source impedance = 0.297 + j0.149 and normalized load impedance = 0.661 – j0.332. As seen in Figure 5, the impedance for maximum power is different from the impedance for maximum efficiency. It should be noted that, differently from the NXP

data sheet, the source and load impedances were selected for obtaining maximum output power, instead of maximum efficiency. Electrical parameters were drain voltage = 50 V, drain current = 34 A, and gate voltage = 2.21 V. Note that the impedances are very low like other LDMOS transistors. This requires a circuit designer to take a careful and thoughtful design work on impedance matching transformers as well as DC bias lines so that the amplifier can operate at high efficiency free from unwanted spurious oscillations.

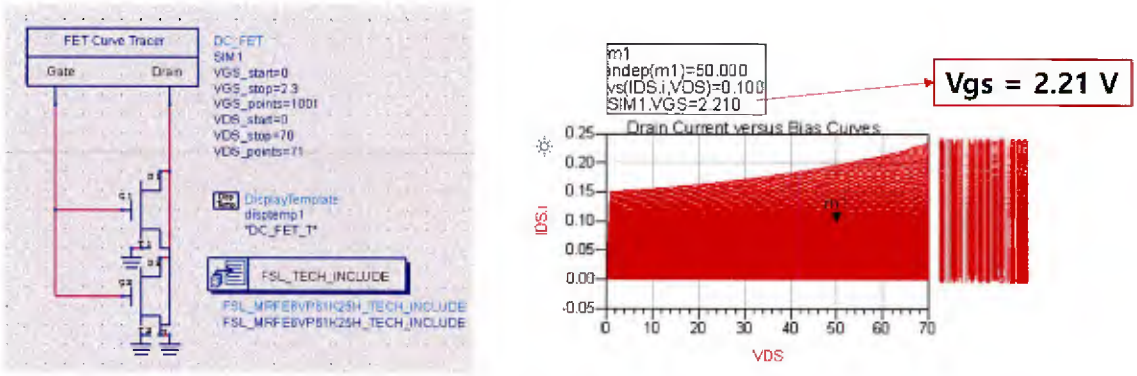
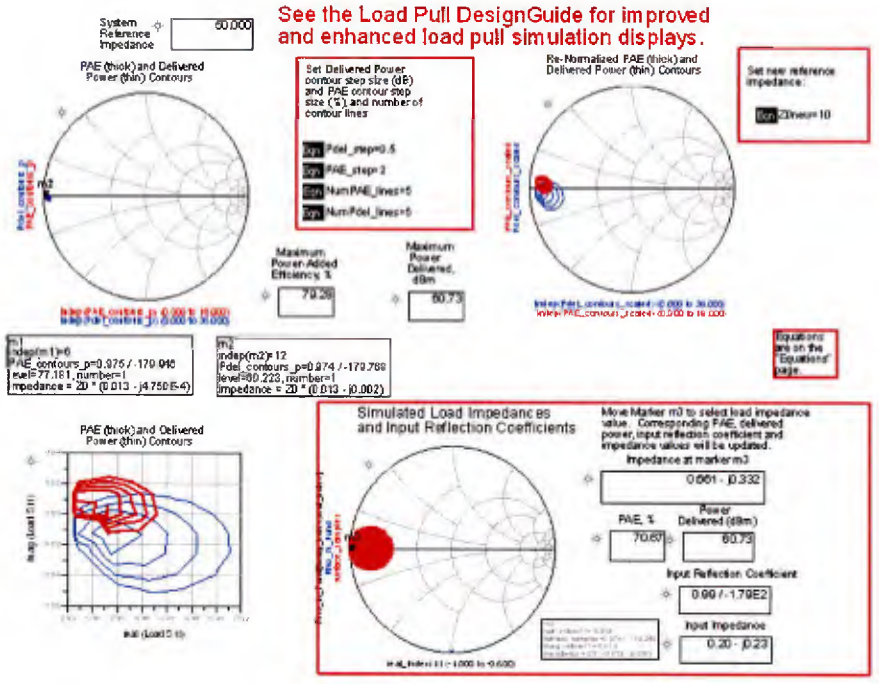
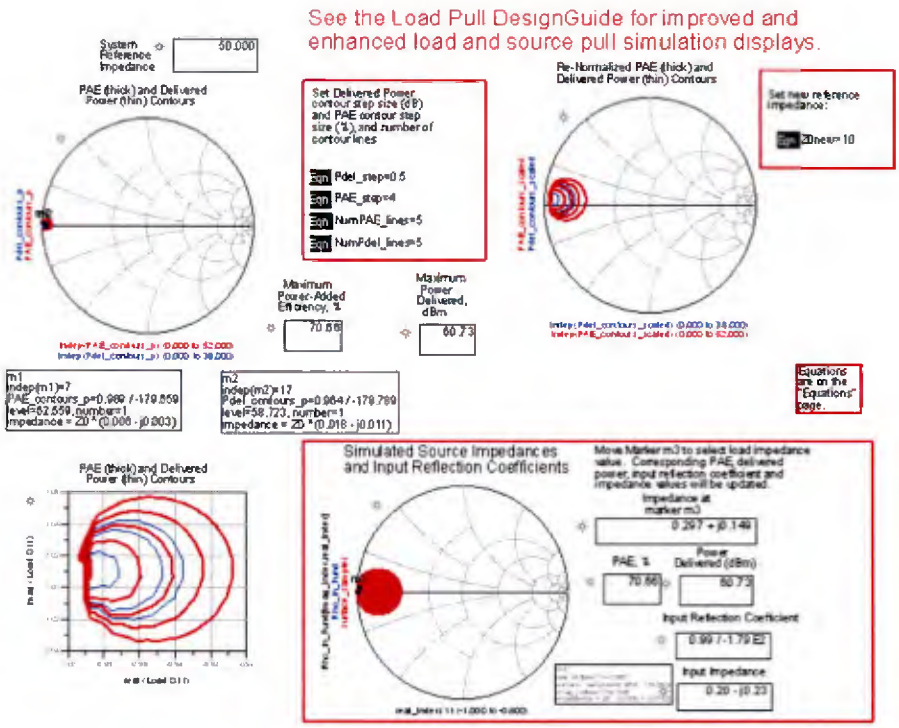


Figure 4. ADS model and DC I-V curve for various gate voltage



(a)



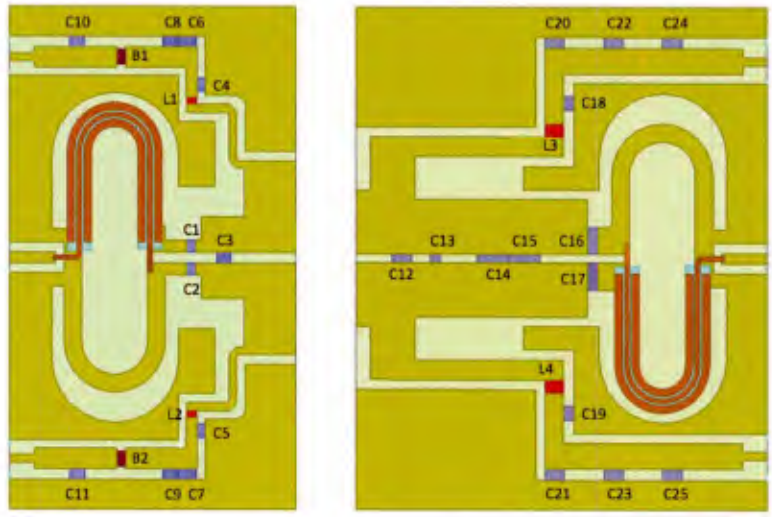
(b)

Figure 5. Plots of constant power contours and constant efficiency contours on real and imaginary reflection coefficients for (a) load pull and (b) source pull.

The next step in designing the 1 kW SSPA is to implement a circuit layout on a dielectric circuit board. There are many ways of designing the microstrip line patterns including drain and gate bias lines. Figure 6 shows the layout on a hybrid microwave integrated circuit (MIC) that we have designed for matching the source and load impedances obtained from the source and load pull simulations. Table 2 shows values of inductors and capacitors in Figure 6.

The input and output baluns play an important role of dividing the incoming signal into the push-pull transistor without reflection and combining two amplified output powers. The most general type of the impedance transformer (balun) is a quarter-wavelength coaxial transmission line with a characteristic impedance of 25 ohms. This coaxial balun requires an accurate cutting to a quarter-wavelength, bending and soldering on the hybrid microwave integrated circuit board. Since we need 320 pairs of baluns for the power combining system, reliability and repeatability of the balun fabrication are critical issue. An innovative design of the impedance transformer was embedded in our hybrid MIC. The designed impedance transformer is a strip line with a

characteristic impedance of 25 ohms, supporting a TEM mode propagation. Figure 6 shows input and output strip-line baluns.



(a) (b)

Figure 6. Layout on a hybrid microwave integrated circuit (MIC) that we have designed for matching the source and load impedances: (a) input matching transformer and (b) output matching transformer

Table 2. Values of inductors and capacitors in Figure 6

Part	Description
B1, B2	47 ohm, 100 MHz Short Ferrite Bead
C1, C2	10 pF
C3	27 pF
C4, C5	1000 pF
C6, C7	220 nF
C8, C9	0.1 uF
C10, C11	47 uF
C12	15 pF
C13	22 pF
C14, C15	8.2 pF
C16, C17, C18, C19	220 pF
C20, C21, C22, C23, C24, C25	470 uF
L1, L2	18.5 nH
L3, L4	12 nH

Harmonic balance simulations were performed to predict amplifier non-linear characteristics such as saturated output power, gain, efficiency, bandwidth, voltage/current waveforms, harmonics, intermodulation etc. NXP provides a non-linear circuit model of the 1 kW LDMOS transistor for ADS harmonic balance simulations. Figure 7 depicts the ADS circuit layout for the 1 kW SSPA. Since ADS uses equivalent circuit models of RF circuit components, the simulation accuracy is not as good as HFSS simulation. In particular, the strip-line balun cannot be accurately modeled in ADS. Therefore, we used HFSS to model and obtain scattering parameters (or, impedances) of the input and output impedance matching transformers (including stripline baluns, matching capacitors, inductors, and stepped microstrip lines). This way, we are confident that the simulated results from the full 3-D simulations by HFSS are as accurate as possible. HFSS predicted that the impedances of the input and output transformers are 1.44 + j16.5 ohm and 1.41 – j6.8 ohm, respectively, at 467 MHz. The scattering matrices were imported into the ADS model to perform non-linear harmonic balance simulations along with the LDMOS FET.

Harmonic balance simulation results of the 1 kW SSPA are in Figure 8, showing output power from drive curve, frequency bandwidth, efficiency, gain, and spectral amplitude. As shown in Figure 8, the saturated output power, power-added efficiency (PAE), and gain are 62 dBm, 70 %, and 16 dB, respectively at 467 MHz. The 3 dB bandwidth was 80 MHz (440 MHz - 520 MHz, 17 %). Second harmonic and third harmonic power are - 33 dBc @ 934 MHz and - 65 dBc at 1,401 MHz, respectively, compared with the fundamental frequency's power 62 dBm. It should be noted that the amplifier was optimized for maximum power (instead of maximum efficiency). The predicted output power at saturation is higher than that predicted from the NXP's reference circuit. Note that NXP's reference circuits' balun is made from 25 ohm coaxial cables. Table 3 shows the summary of ADS simulation results.

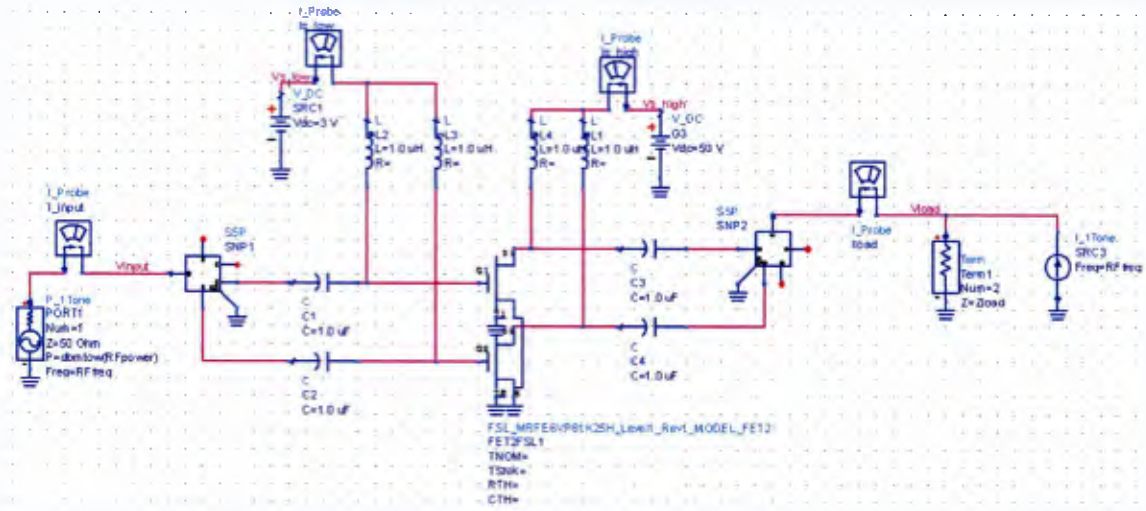
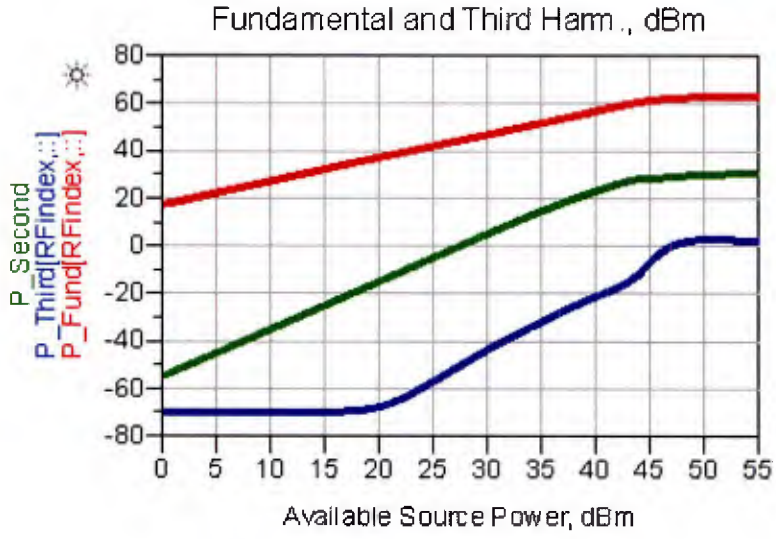


Figure 7. ADS model for harmonic balance simulation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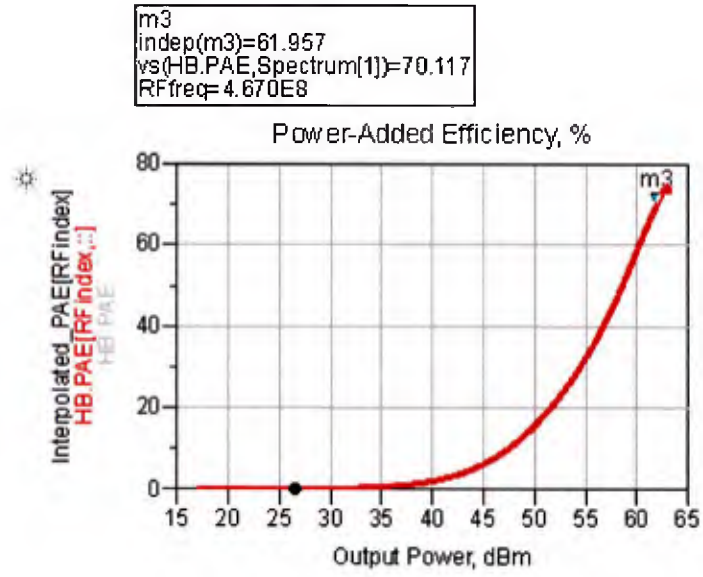
15
20
25
30
35
40
45
50
55
Available Source Power, dBm

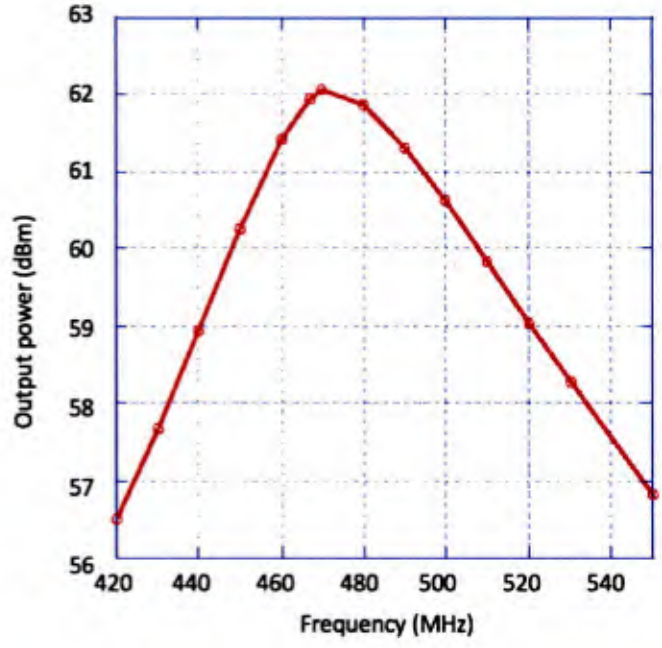
(a)


m3
indep(m3)=61.957
vs(HB.PAE,Spectrum[1])=70.117
RFfreq=4.670E8
Power-Added Efficiency, %
Interpolated_PAE[RFindex]
HB.PAE[RFindex,::]
HB.PAE
m3
80
60
40
20
0
15
20
25
30
35
40
45
50
55
60
65
Output Power, dBm

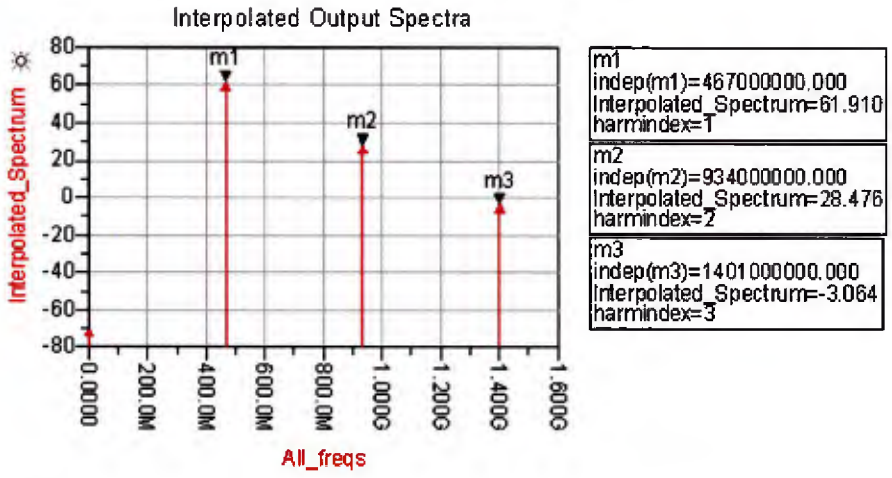
(b)


m2
indep(m2)=61.957
vs(HB.Gain_Transducer.Spectrum[1])=15.957
RFfreq=4.670E8
Gain and Gain Compression
Interpolated_Gain[RFindex]
HB.Gain_Transducer[RFindex,::]
HB.Gain_Transducer
Interpolated_Gain_Compr[RFindex]
Gain_Compression[RFindex,::]
Gain_Compression
m2
18
16
14
12
10
8
10
8
6
4
2
0
15 20 25 30 35 40 45 50 55 60 65
Output Power, dBm

(c)


Output power (dBm)
63
62
61
60
59
58
57
56
420 440 460 480 500 520 540
Frequency (MHz)

(d)



(e)

Figure 8. ADS harmonic balance simulation results: (a) drive curve, (b) efficiency, (c) gain, (d) bandwidth, and (e) harmonic power at saturation

Table 3. Summary of ADS harmonic balance simulation results (f = 467 MHz)

Parameter	Specifications	remark
Drain voltage	50 V	
Gate voltage	2.21 V	
Drain current	34 A	
PAE	70 %	
Output power	62 dBm	1.58 kW
Saturated gain	16 dB	
3 dB bandwidth	80 MHz (440 – 520 MHz)	17 %
Source impedance at fundamental frequency	1.44 + j16.5 Ω	HFSS simulation
Load impedance at fundamental frequency	1.41 - j6.8 Ω	HFSS simulaiton
Harmonic termination: - Source impedance (2^{nd}) - Source impedance (3^{rd}) - Load impedance (2^{nd}) - Load impedance (3^{rd})	 0.89 + j30.45 Ω 5.75 + j22.48 Ω 0.28 + j4.98 Ω 0.08 + j 4.42 Ω	Predicted from HFSS simulation
Circuit board of matching transformer: - Model - Thickness - Dielectric constant	 Rogers TC 350 0.762 mm 3.5	
Strip line balun: - Model - Thickness - Dielectric constant	 Taconic CER-10 0.64 mm 10	

3.2 Fabrication and test of 1 kW SSPA

Input and output hybrid microwave integrated circuits were fabricated. All the circuit components such as microstrip lines/pads, impedance matching capacitors, capacitors/inductors for rejecting AC noises from DC power supplies, and DC block capacitor were selected based on the simulated results for optimum amplifier performance operating at deep class AB. They were soldered on the gold-plated PCB with grounded via holes for ensuring good thermal dissipation and grounding RF signals along RF path.

The strip line balun was fabricated by etching the center conductor (copper) on a grounded dielectric substrate and then covering it with an equal thickness of the grounded

dielectric substrate on the backside. The substrate dielectric material was chosen to be high dielectric constant (Taconic CER10: dielectric permittivity = 10, loss tangent = 0.035, thickness = 0.64 mm) so that the length of the balun becomes short and thus the balun takes less space in the hybrid MIC. The total number of strip line baluns amounted to 320 for the 200 kW, 80-way power combiner system. Since all fabrication process is done in a gold-plated PCB processing line, fabrication repeatability of the 320 baluns is fully guaranteed. Fabricated strip line baluns are shown in Figure 9(a) and 9(b). Strip line width is selected so that the characteristic impedance becomes 25 ohm. Balun is typically configured so that both signal line and ground line are equal-length 25 ohm coaxial cable (as seen in Figure 10(a). In order to facilitate fabrication, we configured that the combined signal passes through the 25 ohm strip line and the ground path is made to be a copper line (as seen in Figure 10(b)). We have cold-tested the fabricated strip line balun using VNA. Figure 10 shows output baluns for 3 cases: (a) 25 ohm coaxial cable (a-1 and a-2 are the setup for impedance at signal line and impedance at ground line, respectively), (b) 25 ohm strip line (b-1 and b-2 are the setup for impedance at signal line and impedance at ground line, respectively), and (c) 25 ohm strip line with grounded copper line (c-1 and c-2 are the setup for impedance at signal line and impedance at ground line, respectively). Case (c) is the case that we have tuned the grounded copper line so that the impedance and phase became the same as case (b). Table 4 summarized the measurement results of Figure 10. Measurements show that complex input impedances of the output strip line balun are 2.92 + j31.98 ohms (signal path) and 3.26 + j 32.39 ohms (ground line). The transmission-phase measurements show -147 degrees (signal path) and 31 degrees (ground line). The phase difference between two output ports is measured to be 31-(-147) = 178 degrees, which is supposed to be 180 degrees for combining power from the push-pull transistor in an ideal balun. Figures 11(a) and 11(b) show fabricated hybrid microwave integrated circuits employed with input and output strip line. Figure 12 shows measurement setup and measured load impedances in a push-pull amplifier configuration: (a) signal path of the transformer and (b) ground path of the transformer. Note that the isolated port is terminated with a conjugated value of a transistor load impedance. As shown in Figure 12(a), measured load impedances (signal path) were 3.083 + j9.029 ohms at fundamental frequency = 500 MHz, 4 + j32.510 ohms at second harmonic, and 7.351 + j45.775 ohms at third harmonic. The phase difference between two ports (signal path and ground copper) was found to be 179 degrees, which is very close to the theoretical value (180 degrees) in the push-pull amplifier configuration.

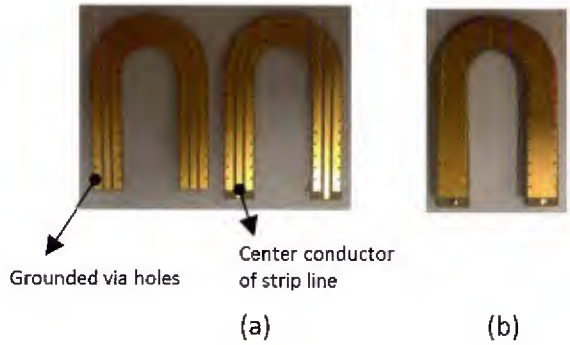


Figure 9. (a) Strip-lines before putting together and (b) assembled strip-line balun

(a-1) (a-2) (b-1) (b-2) (c-1) (c-2)

Figure 10. Output baluns for 3 cases: (a) 25 ohm coaxial cable (a-1 and a-2 are the setup for impedance at signal line and ground line), (b) 25 ohm strip line (b-1 and b-2 are the setup for impedance at signal line and ground line), and (c) 25 ohm strip line with grounded copper line (c-1 and c-2 are the setup for impedance at signal line and ground line)

Table 4. Measured impedances of output balun for various tuning cases

	(a-1)	(a-2)	(b-1)	(b-2)	(c-1)	(c-2)
Measured impedance (ohm)	7.5+ j29.88	8.12+ j30.18	3.17+ j32.2	3.23+ j31.88	2.92+ j31.98	3.26+ j32.39
Phase delay (degree)	-95.34	84.82	-149.19	30.75	-147.07	30.47
remark	25 ohm coaxial cable Impedance measured at signal line	25 ohm coaxial cable Impedance measured at ground line	Strip line Impedance measured at signal line	Strip line Impedance measured at ground line	Strip line & copper line Impedance measured at signal line	Strip line & copper line Impedance measured at ground line

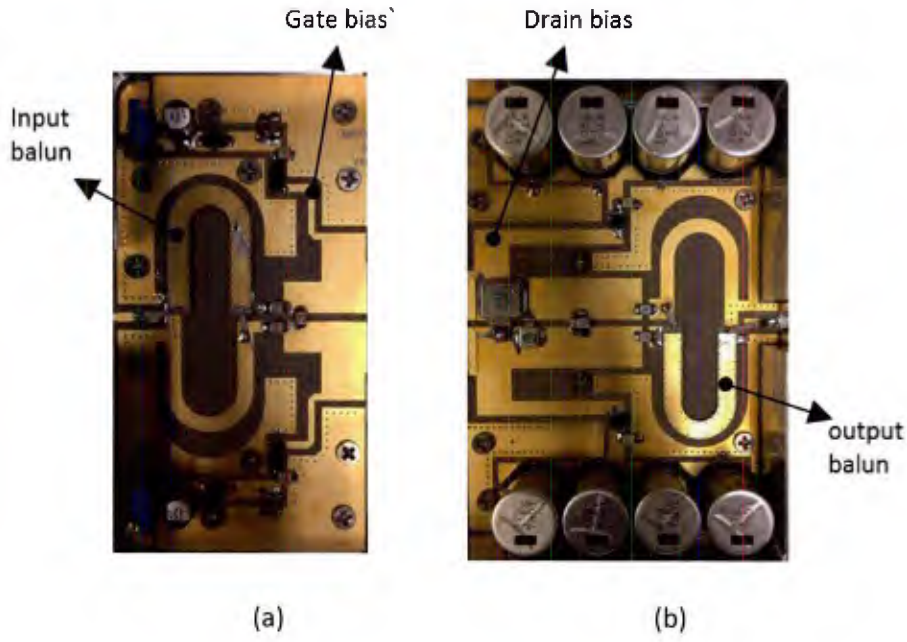
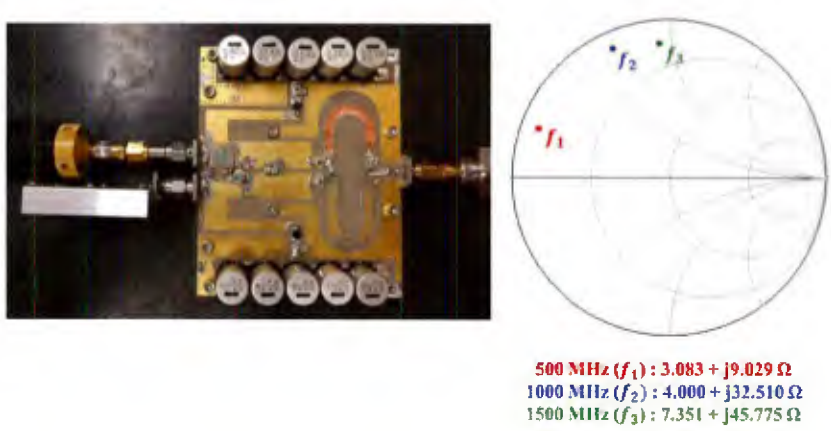
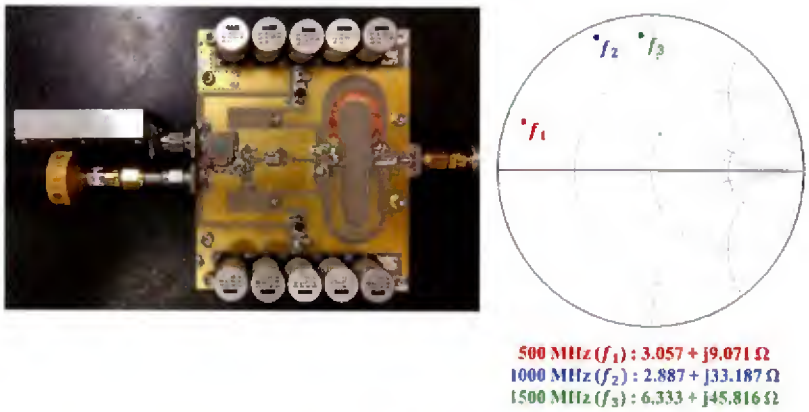


Figure 11. (a) Input impedance matching circuit including a strip-line balun and a gate bias line and (b) output matching circuit including a strip-line balun and a drain bias line.



(a)



(b)

Figure 12. Measurement setup and measured load impedances in a push-pull amplifier configuration: (a) signal path of the transformer and (b) ground path of the transformer

A 1 kW SSPA consists of (1) an input impedance matching circuit and a gate bias line, (2) 1 kW RF power LDMOS, (3) an output impedance matching circuit and a drain bias line, and (4) a high power circulator. Figure 13 shows a photo of the prototype 1 kW SSPA. The high power circulator (UIY DC3538A470T570, 2 kW forward power (peak)) is placed right after the output balun in order to protect the sensitive transistor from any unwanted reflected signal. We have observed unstable DC oscillations as well as rf-driven oscillations in an initial RF test. All the oscillations caused by the DC power lines were suppressed by properly inserting series inductors and high-capacitance capacitors (470 micro-Farads) on the gate and drain bias lines. We could successfully operate the zero-drive stable SSPA without spurious oscillations.

Figure 14 shows experimental results on amplifier output power, drain efficiency and gain as functions of drive frequencies. Experiments show an output power of more than 1.5kW (1.8 kW max), maximum drain efficiency close to 83 % and saturated gain of 18 dB at 460 ~ 485 MHz (BW = 5%) where drain voltage is 50 V, quiescent current is 100 mA and duty cycle is 0.5 % (100 microsecond, 50 Hz). The measured output power and DC-RF conversion efficiency are fully satisfied for the project goals. The frequency bandwidth (460 – 475 MHz) corresponding to 1.5 kW or more was measured to be much wider than that of the TM_{010} cavity (described later in Chapter 5). Table 5 summarizes experimental results of the 1 kW SSPA.

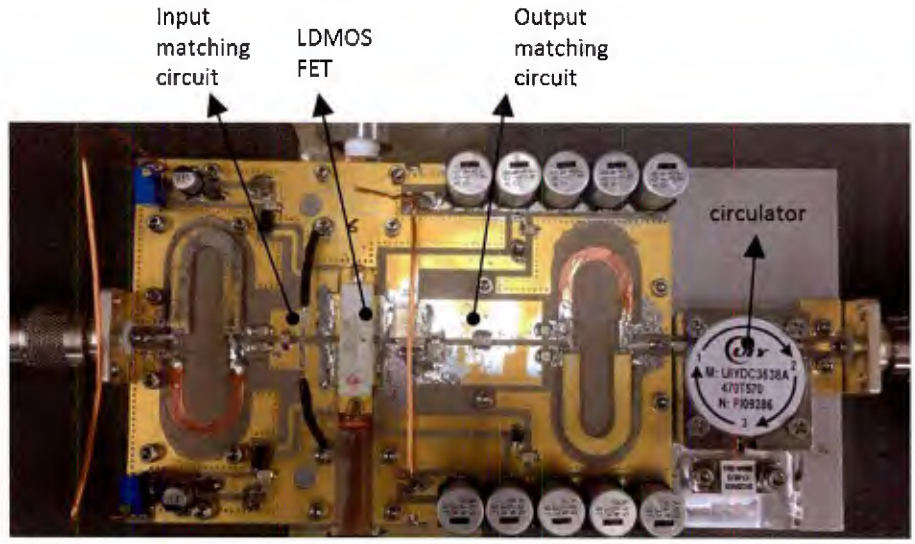


Figure 13. Photo of the prototype 1 kW SSPA

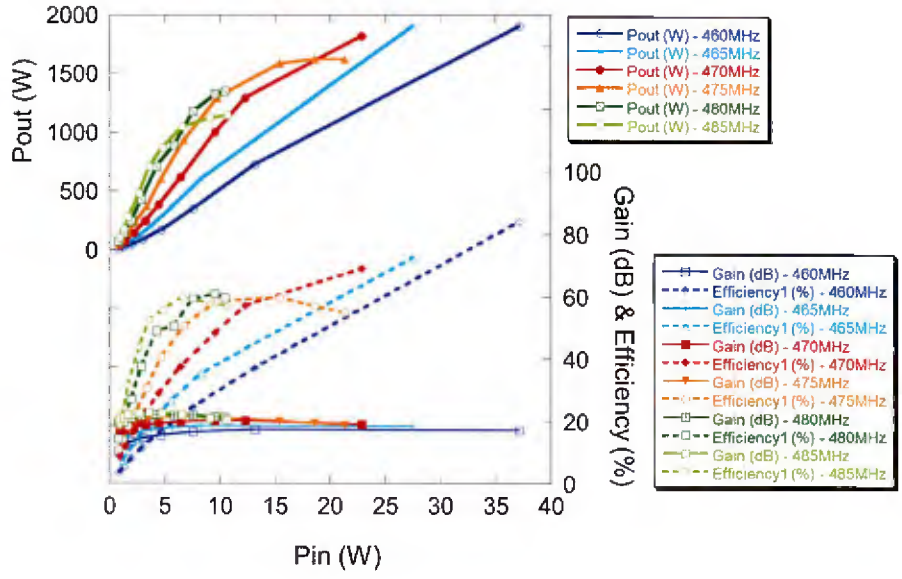


Figure 14. Experimental result on amplifier output power, drain efficiency and gain as functions of drive frequencies

Table 5. Experimental results of the 1 kW SSPA

FET	MRFE6VP61K25HR6	NXP
Frequency	460~485 MHz	
Output power	> 1.5 kW	Max: 1.8 kW @ 460~ 465 MHz
Drain efficiency	> 70 %	Max: 83 % @ 460 MHz
Saturated gain	18 dB	
Duty cycle	0.5 %	100 microsecond, 50 Hz
Operating conditions	V_{DS} = 50 V V_{GS} = 2.5 V	

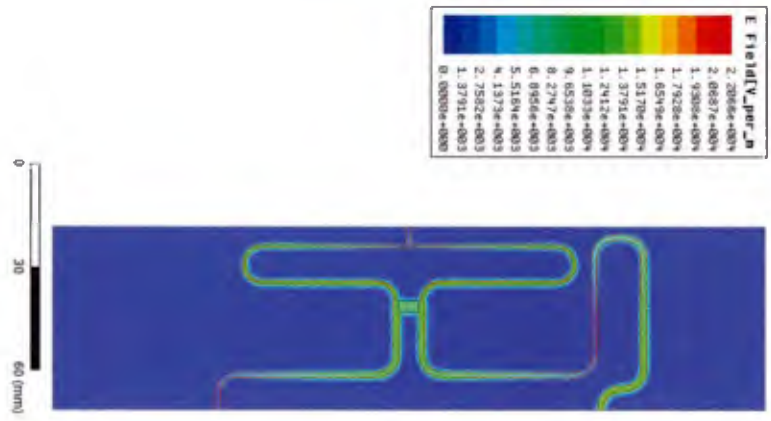
Chapter 4. 2 kW SSPA module

4.1 Wilkinson power divider and Gysel power combiner

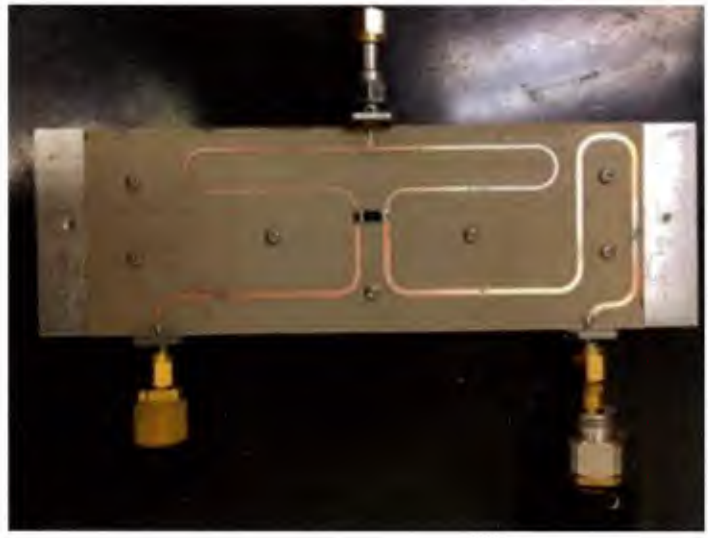
A 2 kW SSPA module will be used as a unit-module for the power array of the cavity power combining system. The eighty 2 kW unit-modules will be assembled and combined in the cavity power combining system. Two of the 1 kW SSPA which was previously described in Chapter 3 are combined through a 3 dB power combiner to get 2 kW RF power. Both Wilkinson and Gysel combiners were designed. It was concluded that, although RF characteristics were same for both combiners, Gysel combiner was superior to Wilkinson combiner because of its high power handling capability.

The SSPA module was configured as a balanced amplifier. The two signals at input have 90 degree out of phase and the two signals at output have 90 degree out of phase in an opposite way so that the two amplified RF signals combine in phase at output port. It should be noted that, in the balanced amplifier configuration, the two signals reflected from two transistors cancel each other and dissipate in the 100 ohm isolation resistor of the Wilkinson power divider. As shown later in Section 4.3, temperature of the 100 ohm resistor increased due to the dissipated power of the reflected signal when the amplifier operated at high duty cycle.

Input power is divided with 3 dB through the conventional 3-dB Wilkinson power divider with a 100 ohm isolation resistor. The 3 dB Wilkinson power divider was designed for equal power and equal phase on two output ports by using ADS and HFSS simulation codes. Figure 15 shows (a) HFSS simulation result and (b) a photo of the fabricated Wilkinson power divider. Figure 16 shows scattering matrices measured from VNA. As shown in Figure 16, RF cold-tests of the Wilkinson power divider showed a power division of -3.2 dB which is in a good agreement with HFSS simulations. Phase difference between two output ports was found to be 90 degrees as expected.

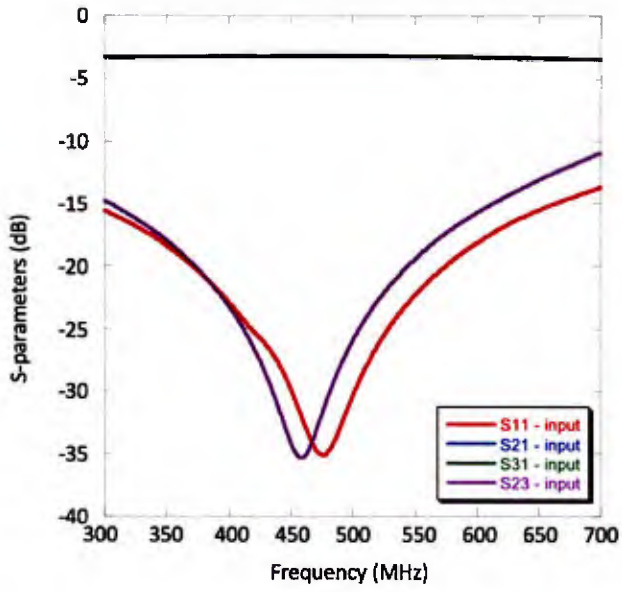


(a)

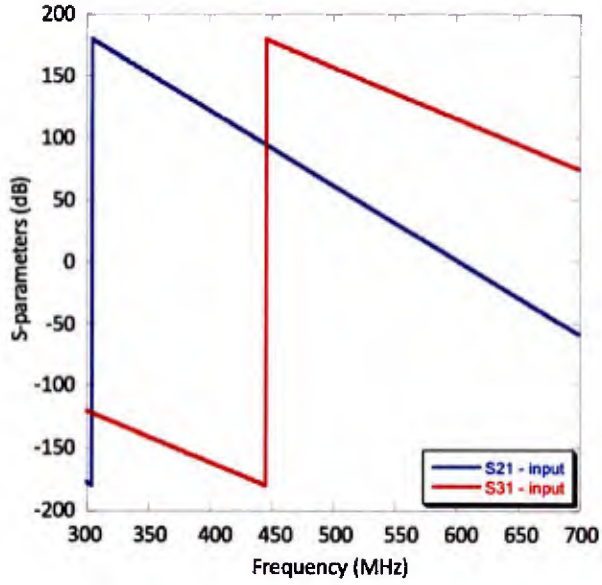


(b)

Figure 15. 3-dB Wilkinson power divider: (a) HFSS simulation result and (b) fabricated Wilkinson divider



(a)



(b)

Figure 16. RF cold-test results of the Wilkinson power divider

The Gysel combiner is a 3-dB equal amplitude and equal phase power combiner which is the same characteristic as the well-known 3-dB Wilkinson combiner. Figure 17 shows layout of the Gysel combiner with dimensions and resistor values. Differently from the 3-dB Wilkinson power combiner, 50 ohm resistors are terminated directly to a ground pad as shown in Figure 17. High power 50 ohm resistor can be mounted and be efficiently cooled on the metallic plate. Figure 18 shows HFSS model of the Gysel combiner. Based on the HFSS simulation results, the Gysel combiner was fabricated on PCB where the dielectric circuit board is Rogers AD250C (thickness = 1.524 mm , dielectric constant = 2.52, loss tangent =0.0013). Note that the thicker dielectric circuit board was chosen for this Gysel combiner in order to reduce electric field stress. Scattering matrices are plotted on Figure 19. As shown in Figure 19, return loss is less than -20 dB and phase difference is 90 degrees.

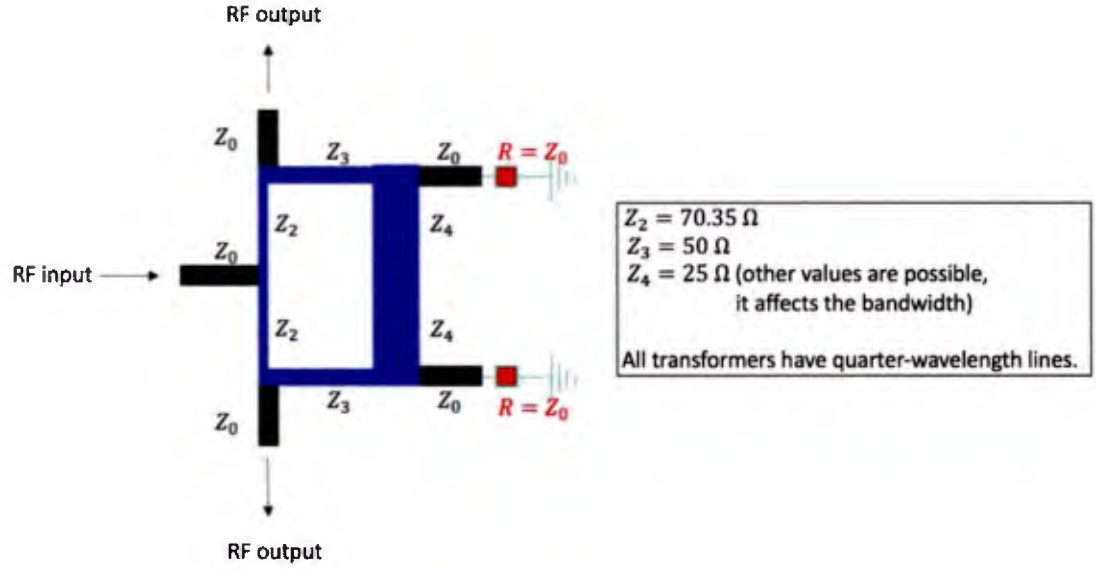
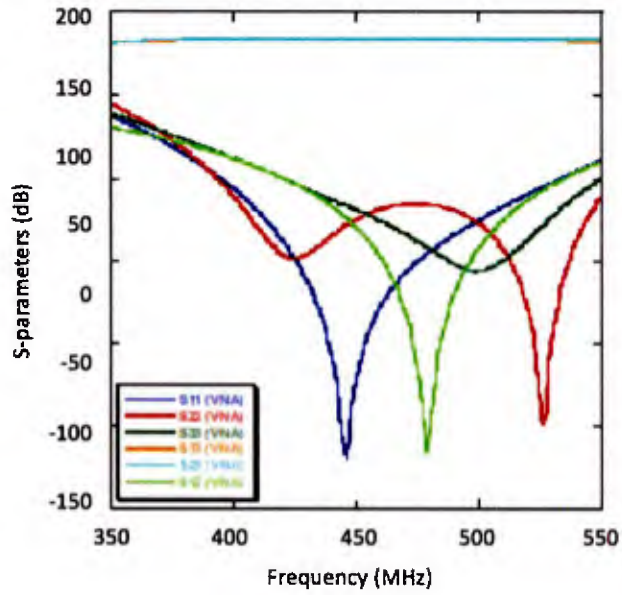
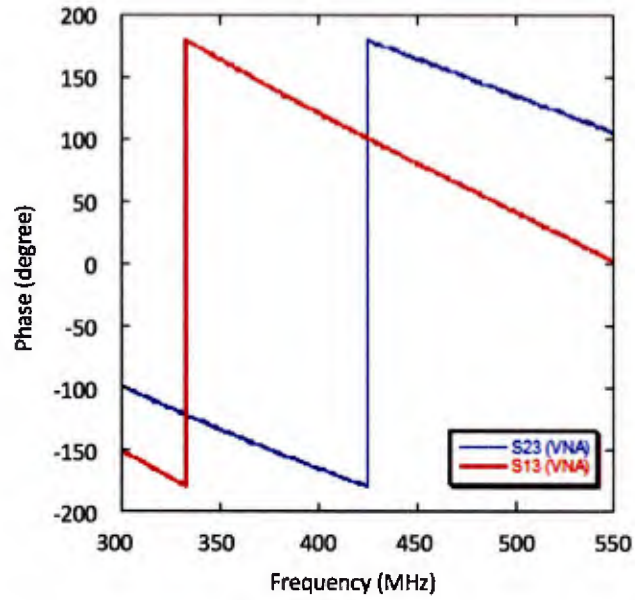


Figure 17. Layout of the Gysel combiner with dimensions and resistor values

Figure 18. HFSS model of the Gysel combiner



(a)



(b)

Figure 19. Simulation results: (a) scattering parameter and (b) phase difference as functions of frequency

4.2 Fabrication and test of 2 kW SSPA module

Figure 20 shows a photo of the assembled 2 kW SSPA module. In order to test the module with a high duty cycle (up to CW), a forced liquid cooling is needed. The two LDMOS power transistors were soldered directly on a copper carrier in order to have a good thermal contact between transistor and copper carrier. The cooling channel was designed for a coolant flow-rate of 10 lpm or more, so that 2 kW heat can be efficiently removed from the power transistors.

Experimental setup for testing the 2 kW SSPA module is shown in Figure 21. A CW signal is generated from Hittite signal generator (HMC284MS8G). An RF switch (described in Section 8.3) is used to obtain a pulse train with predefined PW and PRF (controlled by an external TTL pulse). The RF pulse is injected into two cascaded 1 W SSPA, followed by a 200 W drive amplifier (described in Section 9.2). The output signal of the 200 W drive amplifier is injected into the 2 kW SSPA module through Type-N connector. All measurement data were taken on a computer-controlled VEE program. A drive curve of the 2 kW SSPA module is shown in Figure 22(a). Measured output power, efficiency, and gain were 2,844 W, 66 %, and 14 dB at input power of 104 W and duty cycle = 0.5 %, respectively. Output power variation as a function of input frequency was plotted on Figure 22(b). RF power did not change significantly through the frequency sweep, showing a broadband characteristic of the amplifier. As will be shown later in Chapter 11, the bandwidth of the RF power combiner system is limited by the cavity quality factor (Q), not by the SSPA.

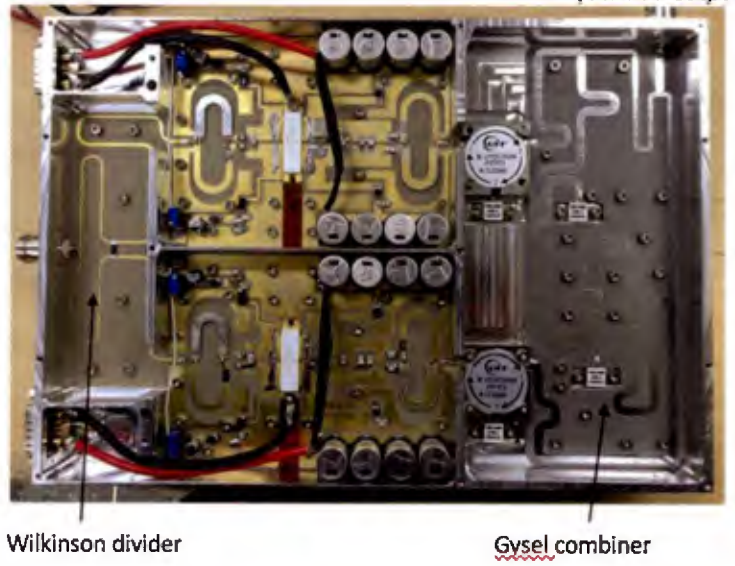


Figure 20. Photo of the assembled 2 kW SSPA module

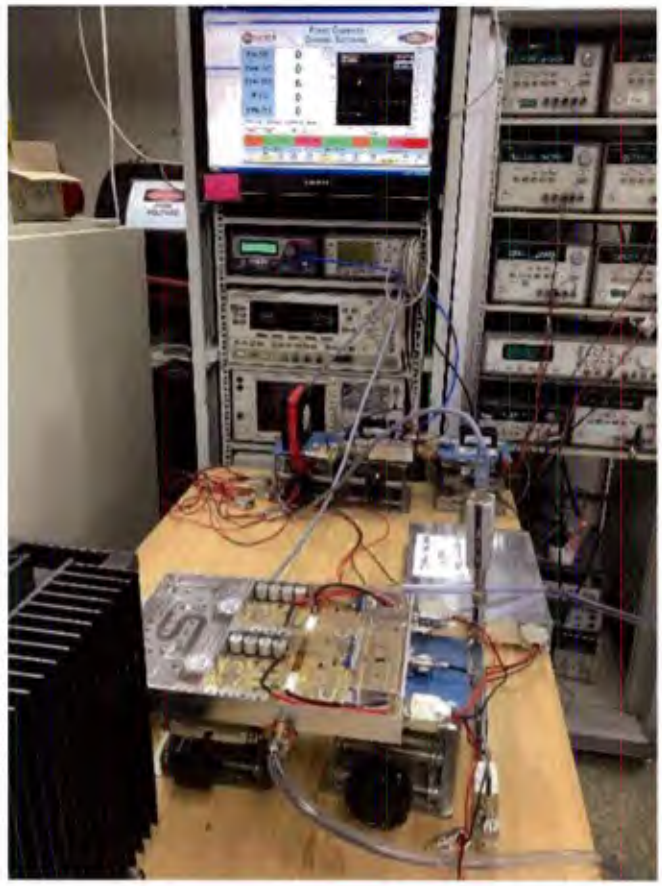
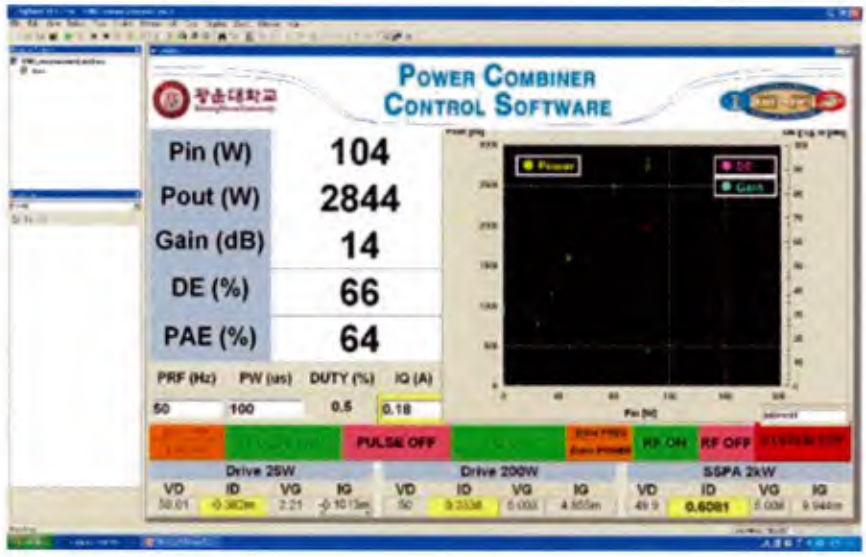
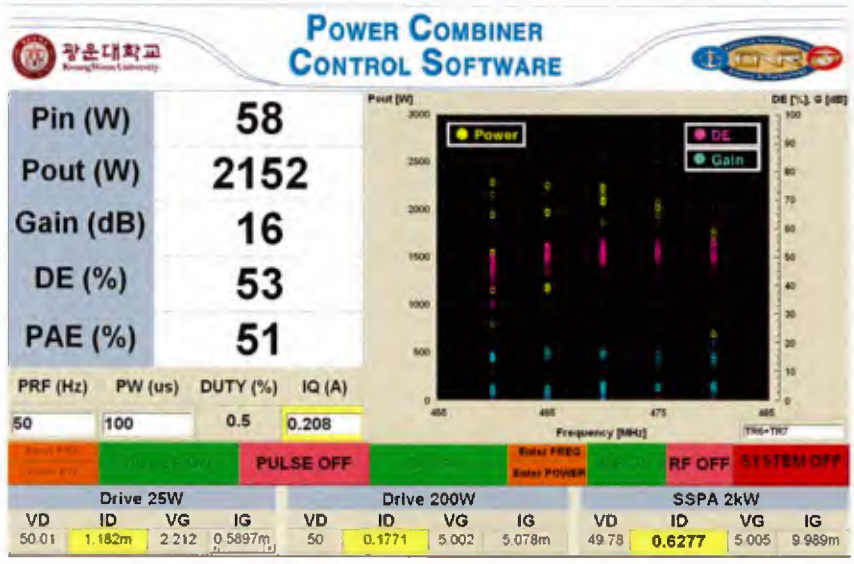


Figure 21. Experimental setup for testing 2 kW SSPA module



(a)



(b)

Figure 22. Experimental results: (a) drive curve and (b) frequency bandwidth

4.3 Thermal analysis and high duty operation

ICEPAK [7] was used to do thermal analysis of the 2 kW SSPA module. The most critical point of concern is the temperature rise of the LDMOS transistor when the SSPA module operates at high duty cycle. Mounting the LDMOS transistor on the copper carrier should be carefully designed. Four cases of mounting the transistor were investigated: (1) thermal compound (Jetart), silver epoxy (EPO-TEK), Pb-based solder, and ideal contact with CPC bonding material. Simulation results were summarized in Table 6 where the cooling water temperature at inlet is 7 degree C and flow rate is set 10 lpm. As shown in Table 6, for the case of Pb-based solder, the temperature on the transistor rises to 168 degree C when it operates at CW mode. Figure 23 shows the ICEPAK model of the module and temperature distribution for Pb-based solder assuming that the SSPA module operates at CW mode. The temperature is below the threshold limit of transistor's junction temperature (typically < 170 degree C for reliable operation). Note that neither thermal compound nor silver epoxy can be used for this application due to too high temperature, potentially causing burn-out of the transistor. Figure 24 shows temperature rise as functions of duty cycles for two cases: (a) with cooling water and (b) without external cooling water (ambient temperature = room temperature (17 degree C)). It is interesting to note that, as shown in Figure 24(b), the temperature of the 2 kW SSPA module reaches 150 degree C at 20 % duty cycle, which is well below the threshold limit. In other words, simulation predicts that the SSPA module can operate at 20 % duty cycle even without external cooling water. However, as will be pointed as later, although the transistor is safe to run at high duty cycle, other RF components such as isolation resistor and strip line balun get very hot, limiting a high average power operation.

Table 6. Summary of ICEPAK simulation results of four cases of mounting the transistor

	Thermal Compound (Jetart)	Silver Epoxy (EPO-TEK)	Solder	Ideal contact (CPC)
Thermal Conductivity (W/m-K)	4.5	2.5	56.9	270
TR Temperature (°C) at 7 °C inlet	237	292	168	163
Water Velocity (lpm)	10	10	10	10

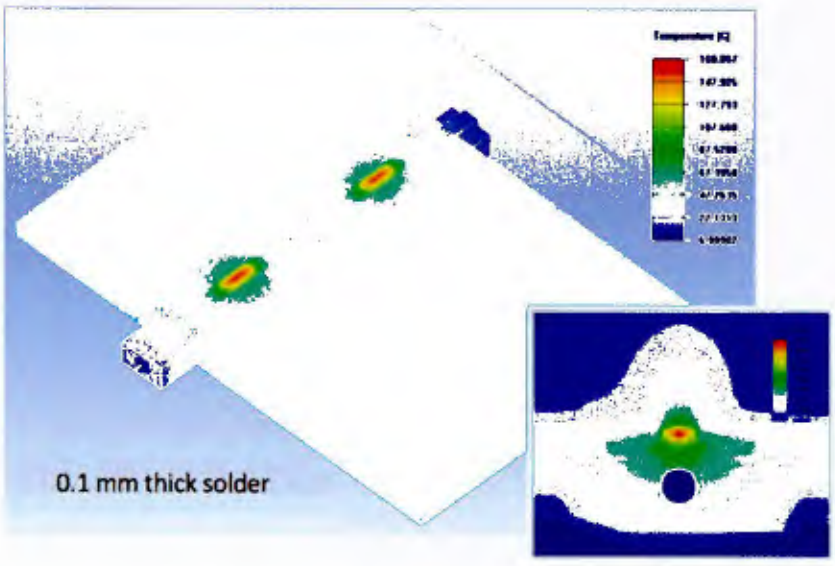
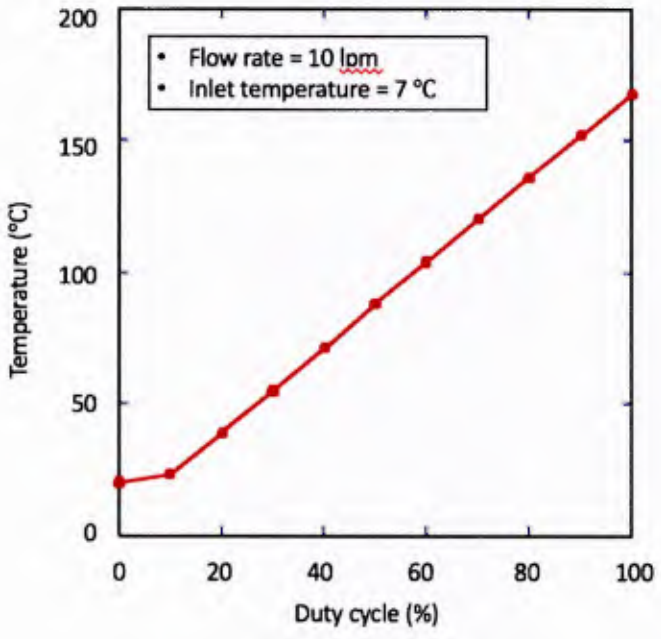
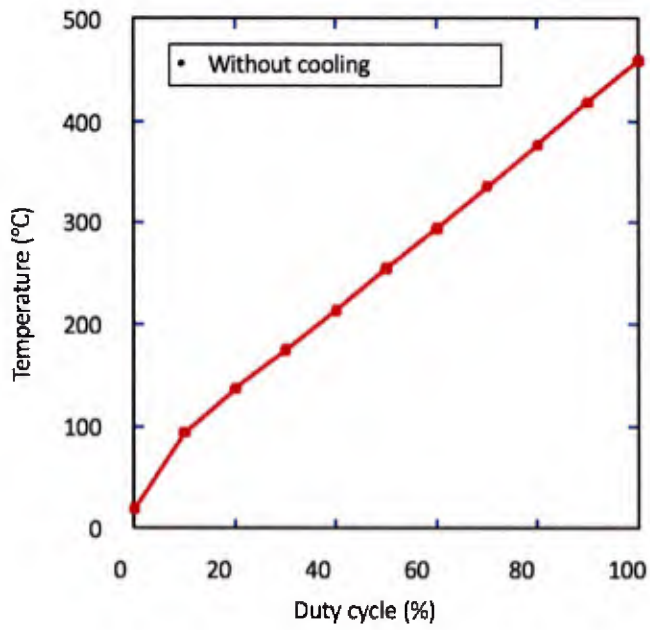


Figure 23. ICEPAK model of the module and temperature distribution for Pb-based solder assuming that the SSPA module operates at CW mode



(a)

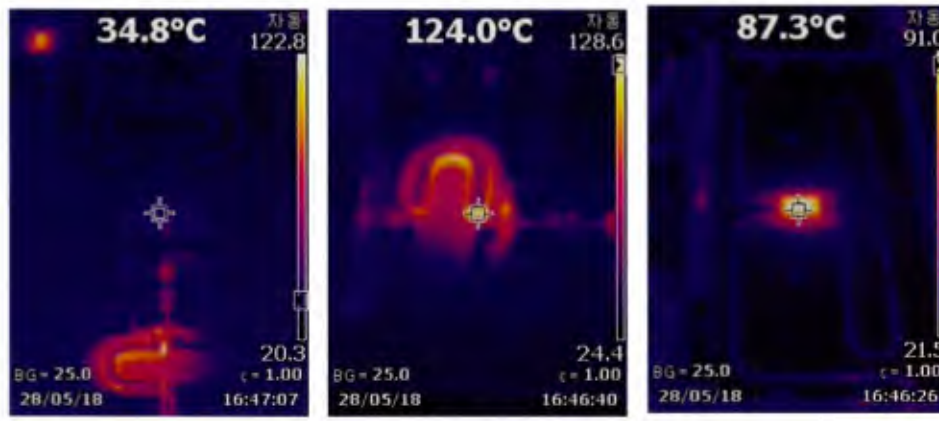


(b)

Figure 24. Temperature rise as functions of duty cycles for two cases: (a) with cooling water and (b) without external cooling water (ambient temperature = room temperature (17 degree C)).

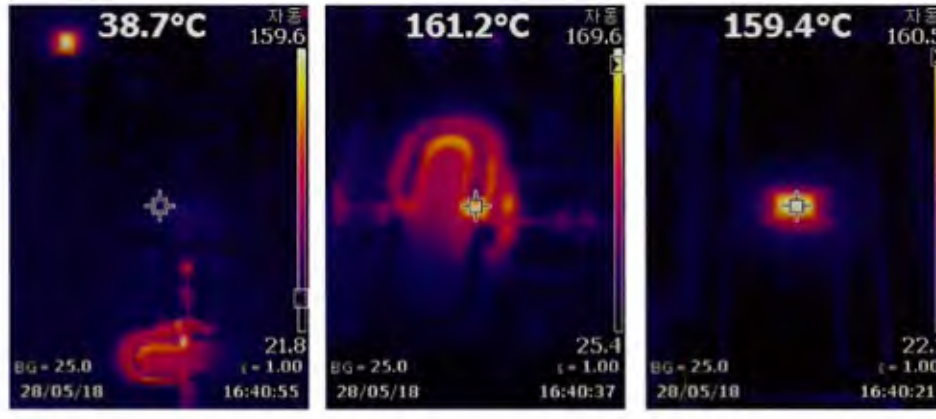
We have measured temperature distribution of the 2 kW SSPA module by the use of IR camera (FLIR-E6390). Thermal images were taken at two enhanced duty cycles = 20 % and 40 %. Thermal images were taken at LDMOS transistor, output balun, and 100 ohm isolation resistor of the Wilkinson power divider. Figure 25 and Figure 26 show the thermal image for duty cycle = 20 % and 40 %, respectively. As shown in Figure 27, highest temperature rise was observed to ~ 160 degree C at output balun and 100 ohm isolation resistor at 40 % duty cycle. This is close to the melting temperature of the Pb-based soldering material (185 degree C). It is expected that the temperature will be reduced if the whole PCB is soldered directly on a copper plate cooled by a coolant.

Figure 28 shows the power, efficiency, and gain of the 2 kW SSPA module as functions of duty cycle (from 0.1 % to 35 %) where frequency = 464 MHz, drain voltage = 50 V, temperature of cooling water = 11 degree C). The RF output power and efficiency stay nearly constant throughout all duty cycles. It is observed that amplifier gain drops slightly as the duty cycle increases dur to thermal power dissipation in the transistor.



(a) (b) (c)

Figure 25. Thermal image of the power amplifier (20 % duty cycle: PRF = 1 kHz, PW = 200 microseconds): (a) LDMOS transistor, (b) output balun, (c) 100 ohm isolation resistor of Wilkinson power divider



(a) (b) (c)

Figure 26. Thermal image of the power amplifier (40 % duty cycle: PRF = 1 kHz, PW = 400 microseconds): (a) LDMOS transistor, (b) output balun, and (c) 100 ohm isolation resistor of Wilkinson power divider

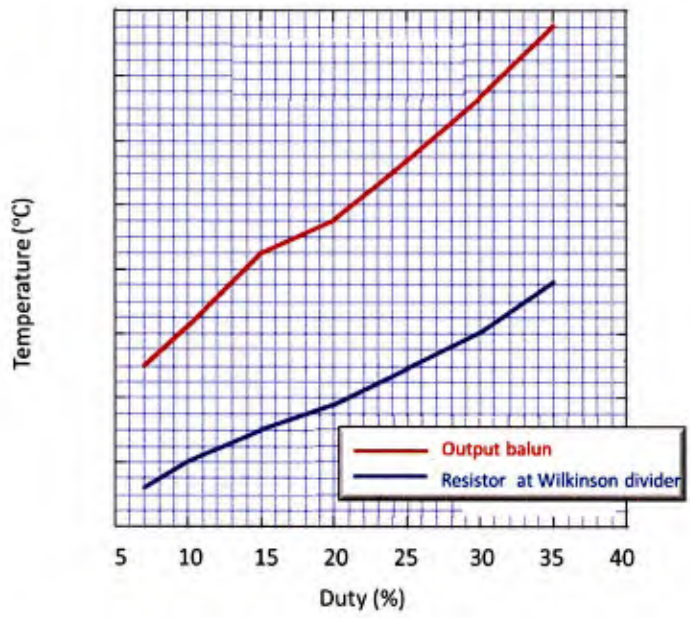


Figure 27. Measured temperature rise on output balun and 100 ohm resistor of the Wilkinson power divider as functions of duty cycle.

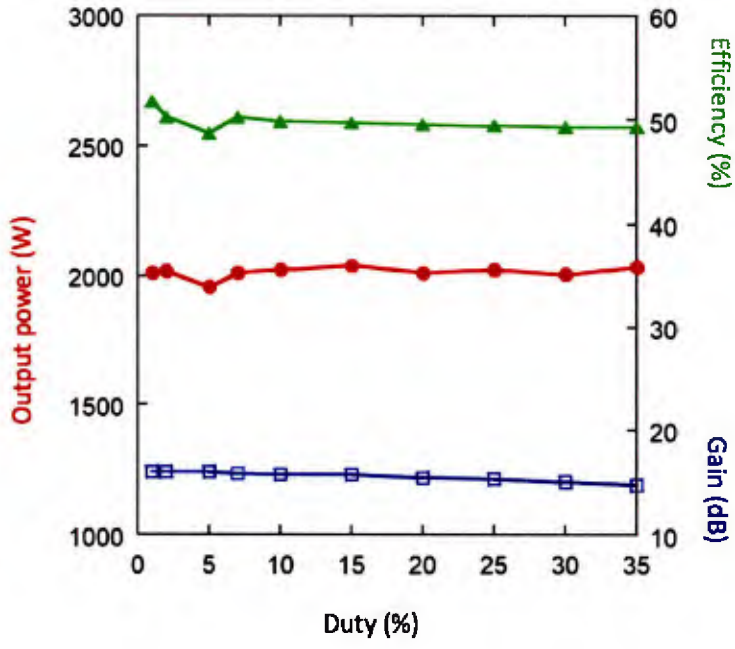


Figure 28. RF output power, efficiency, and gain as functions of duty cycle.

Chapter 5. N-way power combiner

Since the output power of the SSPA unit module is limited to 2 kW, the only available solution for achieving high output power is to combine the output power of individual modules. One of the key issues in a power combiner design is the combining efficiency, which is defined as the ratio of combined output power to the sum of output powers of individual SSPA modules. A conventional cascaded two-way (binary) combiner is not suitable for meeting our requirement of a 200 kW combined output power due to a large power loss in the combiner. Designing a highly efficient power combiner is the most important theme for this project. We have investigated two types of power combiner with high combining efficiency and high-power handling capability: (1) transmission line-type combiner and (2) cylindrical cavity combiner.

5.1 Transmission-line type power combiner

We investigated a compact, highly efficient 40-way transmission line-type power combiner. As shown in Figure 29, there are 40 input ports equally spaced along the azimuthal angle and one output port located in the center of the cylindrically symmetric cavity. The 40 RF input electromagnetic waves travel along the radial direction (inward) of the cavity as a propagating wave, differently from a cavity resonance behavior with a relatively high Q. The propagating wave is a TEM wave in the azimuthally symmetric cylindrical cavity. Both input and output transitions were designed for impedance matching at 470 MHz. The 40 input signals from the 2 kW SSPA modules are coupled into the cavity through inductive coupling probes. The inductive (magnetic) coupling scheme is suitable for a high power application because electric field is zero at the coupling junction. Output power extraction is made through the inductive coupling as well. This coupling scheme has advantages over electric coupling in high power transmission without break-down and easy cooling on the center conductor of the coaxial transmission line. The resultant combined power of 80 kW is extracted through a 3-1/8" coaxial transmission line centered in the cavity.

A four-step impedance transformer was designed so that the 40 input signals can be combined without reflection or mismatches. Figure 30 shows power combining efficiency as functions of frequencies. Simulations predicted a maximum efficiency = 98 % at 470 MHz and bandwidth = 40 % (400 ~ 600 MHz: frequency band with combining efficiency of more than 90 %). It is interesting to note that the frequency bandwidth was much wider compared with the cavity combiner described in Section 5.2. This is because the transmission line-type combiner has a lower Q than that of the cavity combiner (note that bandwidth is inversely proportional to cavity quality factor.). A disadvantage is that the number of input ports is restricted to 40 due to the limited diameter of the cavity (60 cm). The combiner becomes too large if all 160 input ports (for > 300 kW output power) are placed on the transmission line-type combiner. Considering that one needs 4 of the transmission line-type power combiners in order to get 300 kW, the total combining efficiency when combining 4 transmission line-type power combiners will be degraded

to be even lower than 98 %. Other than the advantage of the large bandwidth, it is concluded that the cavity power combiner is more suitable than the transmission line-type combiner from the viewpoint of overall combining efficiency, low fabrication cost, size and weight. Design and experimental investigation on the cylindrical cavity power combiner are the main theme in this project.

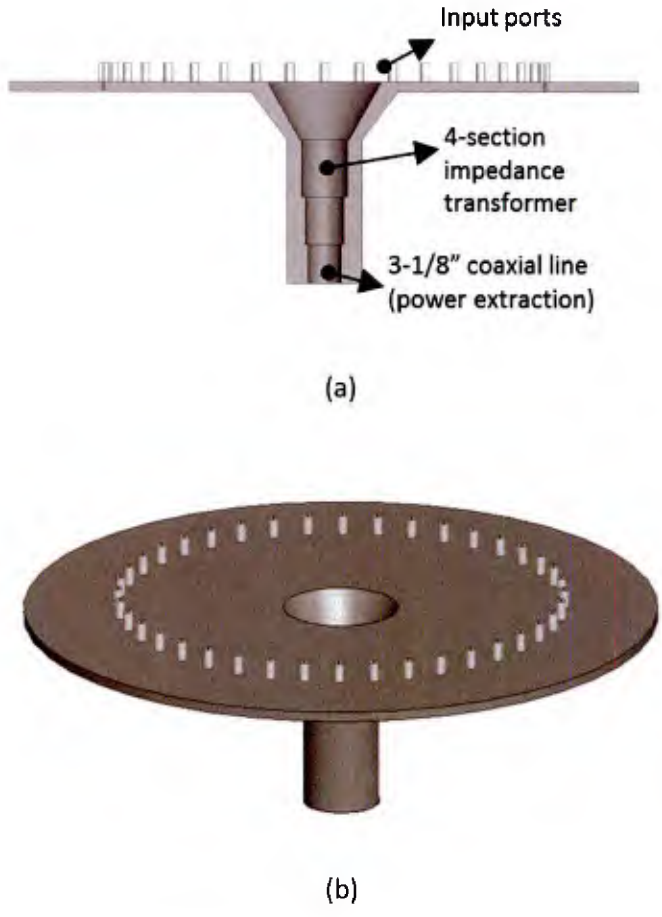


Figure 29. Transmission line-type combiner with 40 input ports: (a) cut-way view and (b) 3-D view

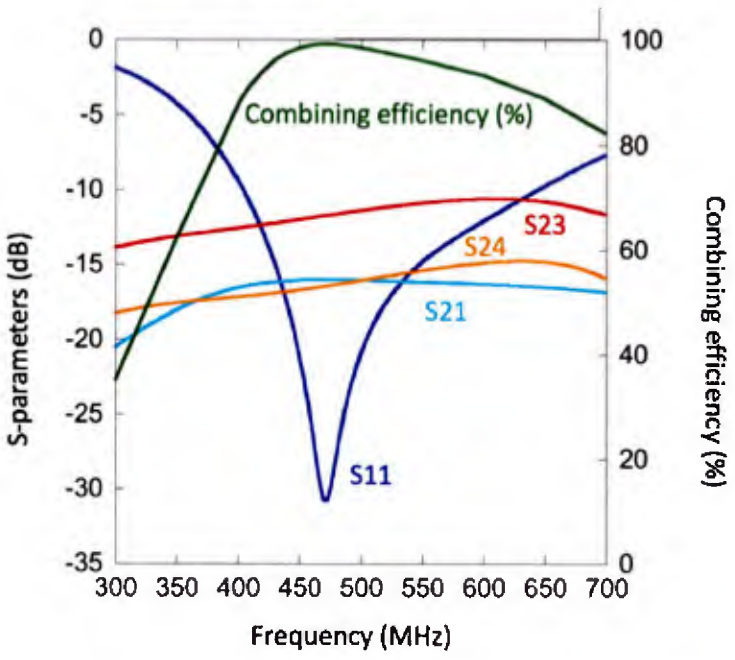


Figure 30. Power combining efficiency as functions of frequencies

5.2 Theoretical study of cavity power combiner

A cavity power combiner is a cylindrical cavity. The resonant mode in interest for our cavity combiner is a TM_{010} mode. Resonant frequency of a cylindrical cavity is given by [8]

$$f_r = \frac{c}{\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{\chi_{mn}}{2\pi a}\right)^2 + \left(\frac{p}{2\ell}\right)^2} \tag{1}$$

where χ_{mn} is the m-th root of Bessel equation, $J_n(x) = 0\ (TM)\ and\ J_n'(x) = 0\ (TE)$ (χ_{mn} = 2.4048, 1.8412, 3.054 for TM01, TE11, TE21 mode, respectively), a is cavity radius, ℓ is cavity length, c is speed of light and p is axial mode index. An ohmic Q (defined as 'resonant frequency' times 'stored energy' divided by 'ohmic power dissipation in the cavity') of TM_{010} mode is given by [8]

$$Q_{ohmic} = \frac{\chi_{01}\eta_0}{2\left(1 + \frac{a}{\ell}\right)R_s} \tag{2}$$

where $R_s = 1/\sigma\delta$ is a surface impedance, σ is conductivity, and $\delta = 1/\sqrt{\pi f \mu \sigma}$ is skin depth. A resonant frequency and ohmic Q of the TM_{010} mode calculated from Eqn. (1) and Eqn. (2) are 459 MHz and 42,000, respectively where radius = 25 cm, length = 25 cm, and conductivity (AL6061) = 2.5E7 [S/m]. Figure 31 shows mode spectrum of TM_{010}, TE_{111}, TM_{011}, and TE_{211} as a function of cavity height where cavity radius is set to be 25 cm. As shown in Figure 31, a cavity height of 25 cm is chosen so that other competing modes such as TE_{111}, TM_{011}, and TE_{211} are not resonant near 460 ~ 470 MHz.

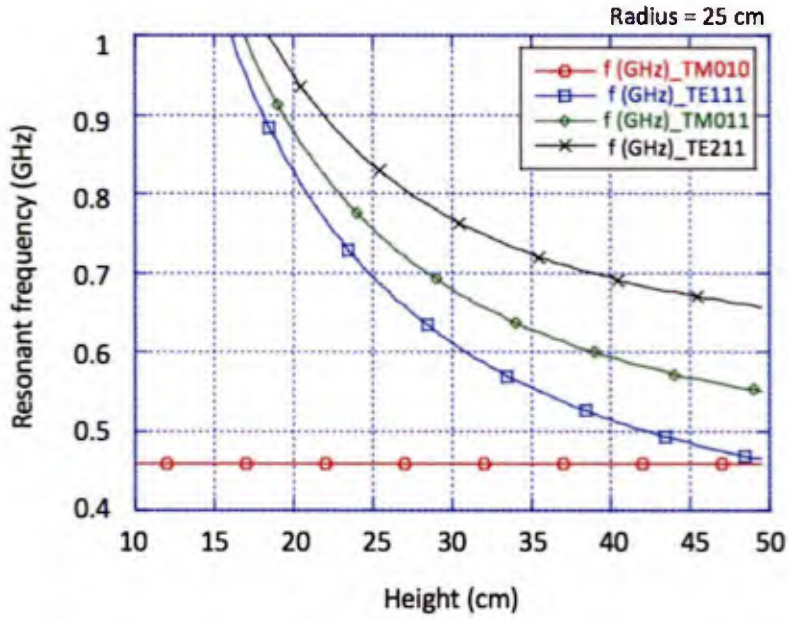
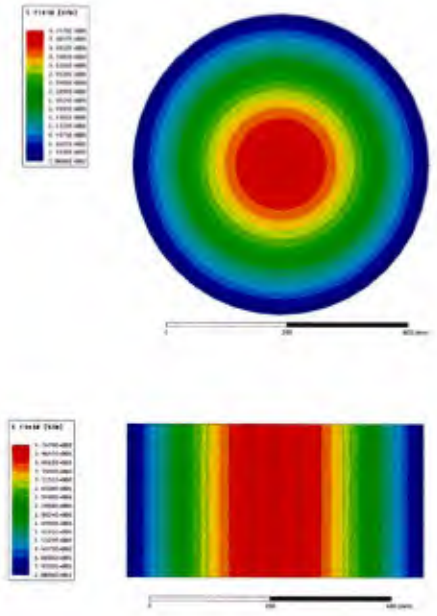
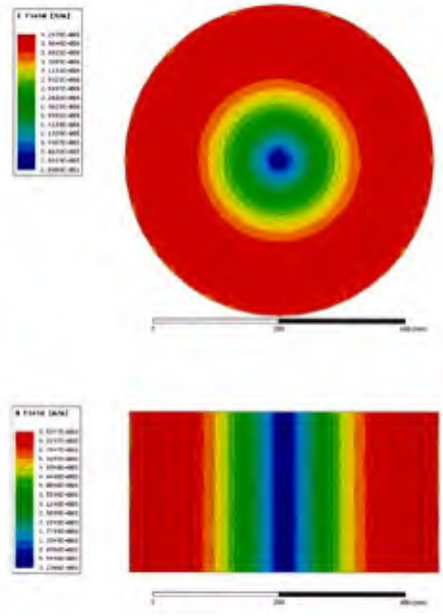


Figure 31. Mode spectrum near the operating TM_{010} mode (cavity radius = 25 cm)

Figure 32 shows HFSS simulation results of the T TM_{010} mode: (a) electric field distribution, and (b) magnetic field distribution. Simulated resonant frequency and ohmic Q were found to be 460 MHz and 27,000, respectively. The simulated resonant frequency is slightly different from the calculated one (459 MHz) due to the numerical error in modeling the circle. The difference between calculated Q (42,000) and simulated ohmic Q (27,000) is due to the approximated expression for skin depth in Eqn. (2). The simulated ohmic Q was used for the following cavity combiner design. Note that the magnetic field intensity is high near the cavity sidewall. We will place loop antennas on the cavity sidewall in order to magnetically couple RF power into the cavity (described in detail later in this section).



(a)



(b)

Figure 32. HFSS simulation results of TM_{010} mode at 460 MHz: (a) electric field distribution and (b) magnetic field distribution

Theoretical design work on a cavity combiner has been performed for any arbitrary number of input port, N. Figure 33 shows an equivalent circuit layout of the cavity combiner including N input ports (on which N SSPA modules are mounted) and one output port (for extracting combined RF power). A condition for critical coupling is given by [9]

$$\beta_{out} = 1 + N \cdot \beta_{in} \tag{3}$$

where β_{in} is the coupling coefficient of one input port, β_{out} is the coupling coefficient of the output port, and N is the number of the input port. Coupling coefficient, β is defined as Q_{ohmic}/Q_{ext}. Under this critical coupling condition (Eqn. (3)), RF power injected from N SSPA modules is maximally combined in a TM_{010} mode cavity and is extracted through the single output port (transmission line) with minimal ohmic loss of RF power in the cavity.

A cavity has a finite Q (quality factor) which is the measure of RF power loss in the cavity. RF power loss consists of two categories: ohmic power loss (the power loss due to a finite conductivity of the cavity wall) and external power loss (the power loss through coupling structures (antennas, input and output ports)). Loaded Q (or, total Q) is related to ohmic Q and external Q by

$$\frac{1}{Q_{load}} = \frac{1}{Q_{ohmic}} + \frac{1}{Q_{ext}^{out}} + \frac{1}{Q_{ext}^{in}/N} \tag{4}$$

where Q_{load} and Q_{ohmic} are loaded Q and ohmic Q, Q_{ext}^{out} is external Q of the output port, and Q_{ext}^{in} is external Q of one of N input ports. Using the definition of coupling coefficient ($\beta = Q_{ohmic}/Q_{ext}$), the loaded Q is rewritten as

$$Q_{load} = \frac{Q_{ohmic}}{1 + \beta_{out} + N \cdot \beta_{in}} \tag{5}$$

One can solve the two linear equations (Eqn. (4) and Eqn. (5)) to get the input and output coupling coefficients as

$$\beta_{in} = \frac{\frac{Q_{ohmic}}{Q_{load}} - 2}{2N} \tag{6}$$

$$\beta_{out} = \frac{Q_{ohmic}}{2Q_{load}} \tag{7}$$

Noting the loaded $Q = f_0/BW$ (where f_0 is the cavity resonant frequency of TM_{010} mode, BW is the 3-dB frequency bandwidth), one can determine the two coupling coefficients using Eqn. (6) and Eqn. (7). Here, f_0 and BW are initial parameters determined by a designer. The ohmic Q is related to a cavity material (aluminum AL6061 for our cavity). A cavity combining efficiency and ohmic power dissipated in the cavity are predicted by

$$\eta = 1 - 1/\beta_{out} \tag{8}$$

$$P_{ohmic} = P_{out}/\beta_{out} \tag{9}$$

where P_{ohmic} is the ohmic power dissipated in the cavity and P_{out} is the output combined power. As seen in Eqn. (7) and (8), the combining efficiency increases as the ohmic Q increases (or, ohmic power dissipation decreases), as expected. Figure 34 plots the coupling coefficients, β_{in} (Eqn. (6)) and β_{out} (Eqn. (7)) required for a given bandwidth for the cases of input ports = 40, 80, 120 and 160. Here, the ohmic Q is assumed to be 27,000 and frequency to be 460 MHz, as predicted from HFSS simulation.

The design procedure of the cavity combiner is as follows:

(1) Set a resonant frequency of TM_{010} mode, BW, ohmic Q, and the number of input port (N)
(2) Calculate β_{in} (Eqn. (6)) and β_{out} (Eqn. (7)) for the given f_0, Q_{load} (= 1/BW), Q_{ohmic}, and N
(3) Using HFSS simulation code, an output coupling port is designed so that one can get β_{out} (or, external Q).
(4) Similarly, the input coupling port (or, loop antenna) is designed so that one can get β_{in}. Note that simulation should be performed by using a single antenna.
(5) Perform a full-model HFSS simulation with N input antennas and one output port. Obtain N+1 by N+1 scattering matrix elements. Check that the reflection coefficient measured at the output port becomes zero (reflected power = 0).

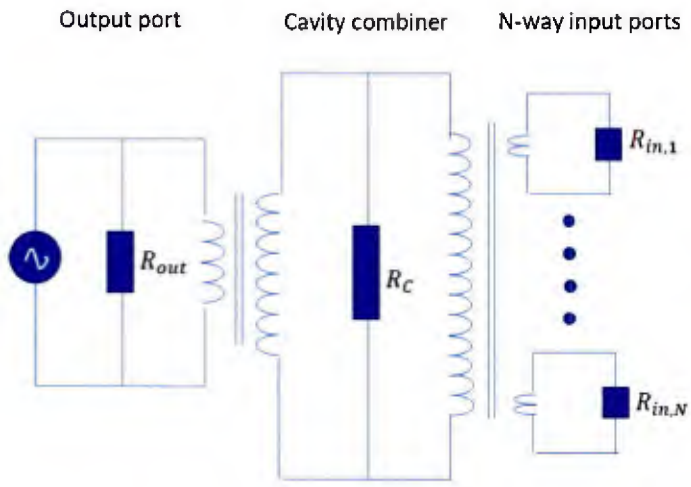


Figure 33. Equivalent circuit layout of the cavity combiner including N input ports (on which N SSPA modules are mounted) and one output port (for extracting combined power)

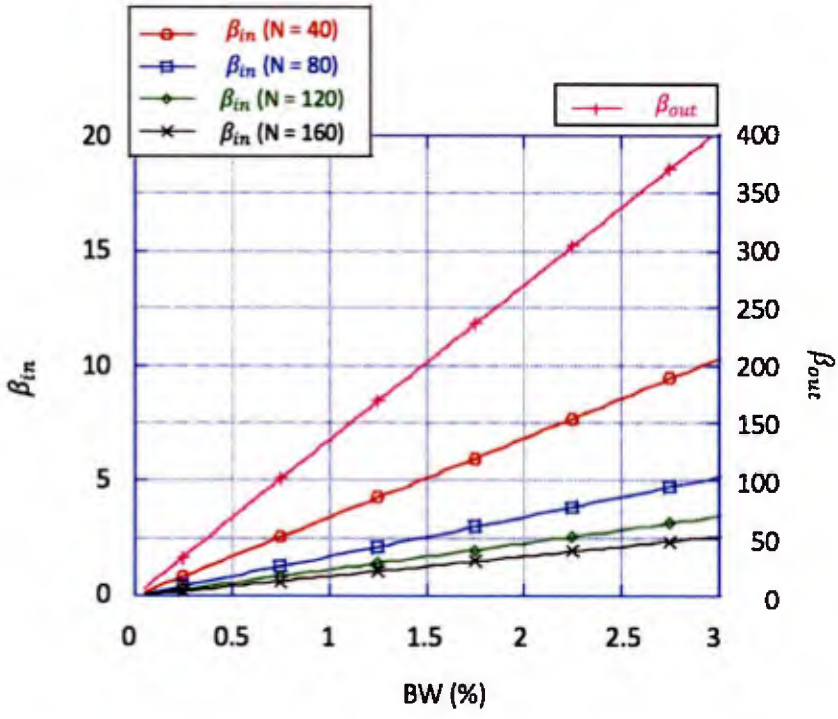
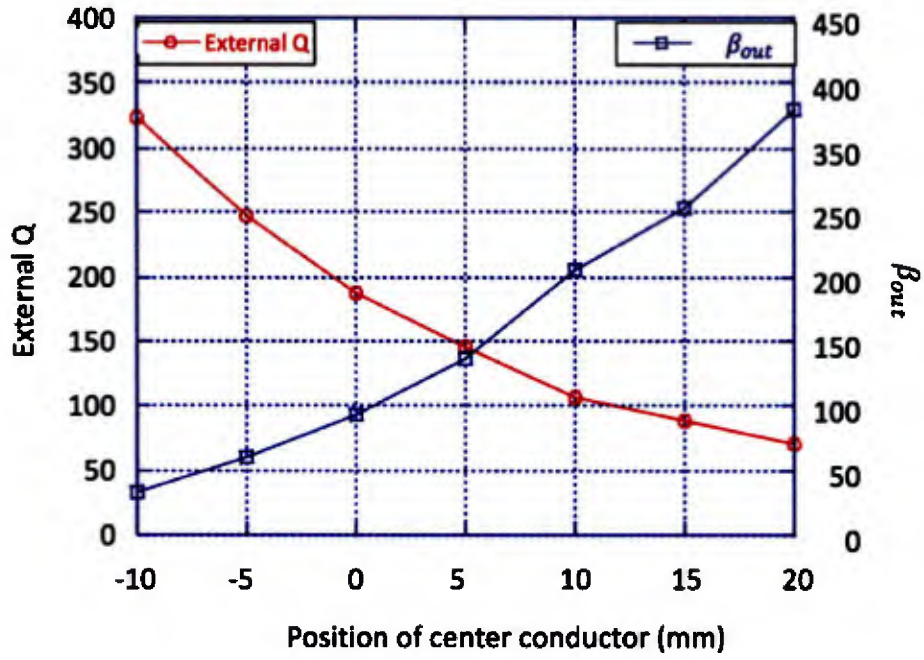


Figure 34. Coupling coefficients, $\beta_{in}$and β_{out} required for a given bandwidth for the cases of input ports = 40, 80, 120 and 160. Here, the ohmic Q is assumed to be 27,000 and resonant frequency = 460 MHz.

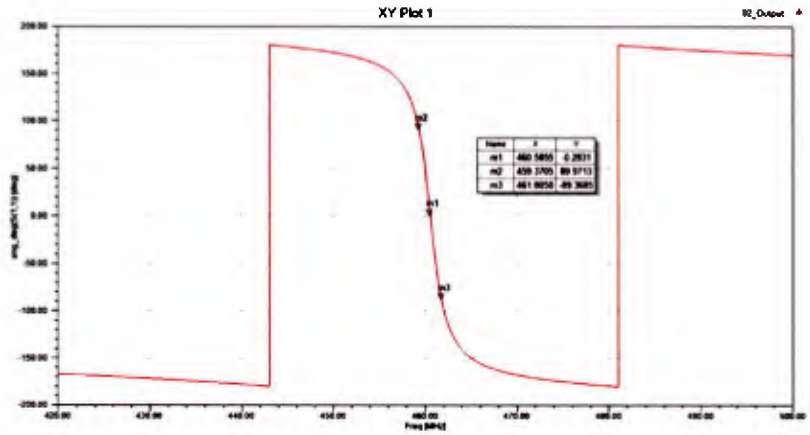
We designed a 40-way cavity power combiner where there are 40 input ports and one output port. The aforementioned 2 kW SSPA modules will be mounted on each input port. Initial design parameters ($\beta_{in}$and β_{out}) of both input port (the coupling antenna for injecting 40 RF signals) and output port (the port extracting a combined RF power) are found from the analytic equations mentioned above. As shown in Figure 34, the output and input coupling coefficient should be β_{out} = 203 and β_{in} = 5.1 under the given condition of N = 40 and BW = 1.5 %. Recall that β_{in} is the coupling coefficient for a single input antenna. Maximum power combining can be achieved when 40 x β_{in} +1 is equal to output coupling coefficient, β_{out}.

Based on the initial design parameters, first of all, an output coupling port is designed by utilizing the 3-D simulation code, HFSS. Cavity length and radius are 25 cm and 25 cm, respectively. Output port should have β_{out} = 203 or Q_{ext}^{out} =133 in order to meet the condition for critical coupling. Output combined power is extracted through a 6-1/8" coaxial transmission line. A 3-1/8" coaxial transmission line was first considered. However, the 3-1/8" line was excluded because of too high electric stress near the center conductor (20 kV/cm). Extensive numerical simulations using HFSS were performed using the 6-1/8" coaxial transmission line for output port. The external power coupling (or external Q of the output port) is sensitive to the location of the center conductor of the 6-1/8" coaxial transmission line. Figure 35 shows (a) simulation model, (b) Q_{ext}^{out} and β_{out} obtained by varying the location of the center conductor, (c) phase variation versus frequency at detuned short position (position of center conductor = 0 mm), (d) electric field, and (e) magnetic field. Here, the external Q was obtained from 'resonant frequency' divided by 'bandwidth' (where the bandwidth is the frequency bandwidth corresponding to + 90 degree and - 90 degree phase shift). As seen in Figure 35(b), output coupling coefficient, β_{out} = 203 was obtained when the center conductor is inserted in the cavity by 6 mm (inward by 6 mm from the cavity surface).

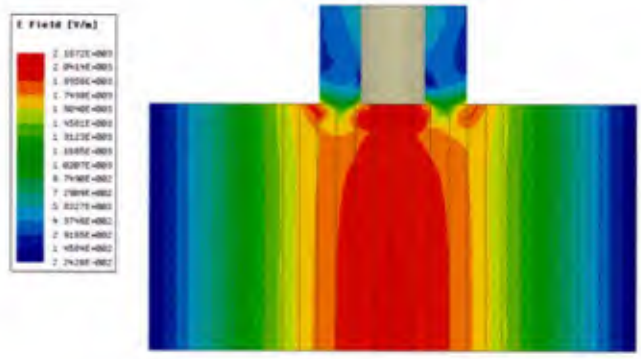
(a)


External Q
β_{out}
External Q
β_{out}
Position of center conductor (mm)
400
350
300
250
200
150
100
50
0
450
400
350
250
200
150
100
50
0
-10
-5
0
5
10
15
20

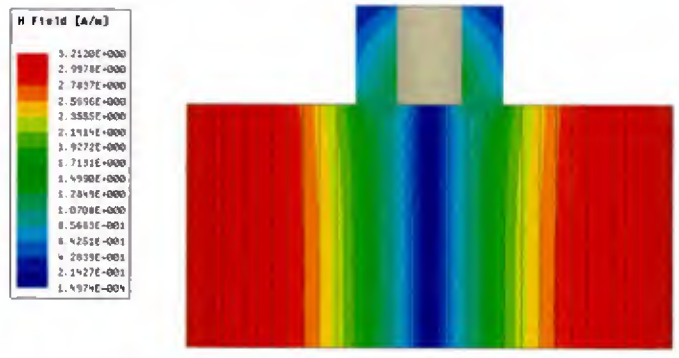
(b)


XY Plot 1

(c)



(d)



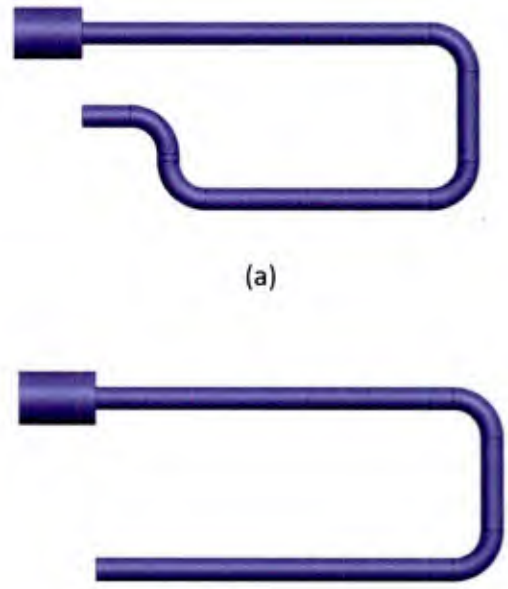
(e)

Figure 35. HFSS simulation results: (a) simulation model, (b) external Q and beta_out obtained by varying the location of the center conductor, (c) phase variation versus frequency at detuned short position (position of center conductor = 0 mm), (d) electric field, and (e) magnetic field. (Here, a perfect conductor was assumed.)

Similar to the design work on the output port, input coupling structure was designed by using 3-D HFSS simulations based on the initial design parameters. HFSS simulations were performed to design and optimize the dimension of a single input antenna through iterative simulations until we get β_{in} = 5.1 (or, $Q_{ext}^{in} = Q_{ohmic}/\beta_{in}$= 5,300). Input power coupling takes place through a loop antenna, which is mounted on a commercially available N-type connector. Figure 36 shows two types of loop antennas we have designed: (a) type I and (b) type II. Both are a magnetically coupled antenna and equally good for the use of input coupler. Type II is preferred because of easy fabrication. The amount of external magnetic coupling loss (or, external Q) is determined by loop location, loop orientation with respect to the rf magnetic axis, and area

surrounded by the loop. The coupling strength is proportional to the area enclosed by the loop where magnetic field intensity of TM_{010} mode is strong in the cavity. The loop antenna is oriented perpendicular to the rf magnetic field of TM_{010} mode.

Figure 37 shows the simulation model, a loop antenna and phase of S_{11} versus frequency. External Q of the single input antenna was found to be 5,300, resulting in β_{in} = 5.1. Here, the conductor was assumed to be a perfect conductor.



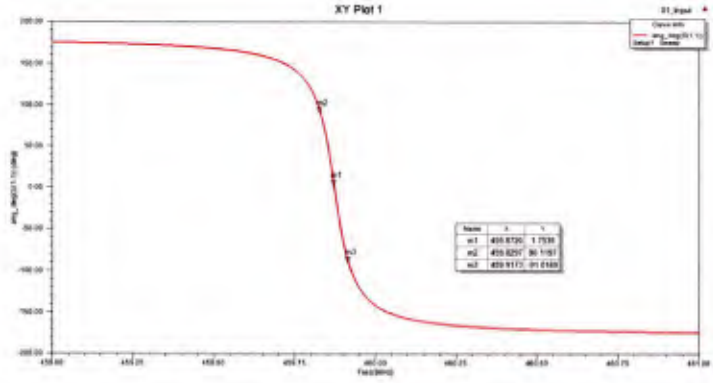
(a)

(b)

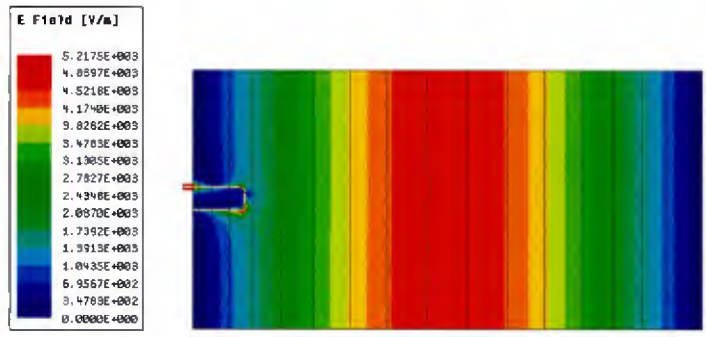
Figure 36. Two types of loop antennas we have designed: (a) type I and (b) type II.

(a)

(b)


XY Plot 1

(c)


E Field [V/m]
5.2175E+003
4.8697E+003
4.5218E+003
4.1740E+003
3.8262E+003
3.4783E+003
3.1305E+003
2.7827E+003
2.4348E+003
2.0870E+003
1.7392E+003
1.3913E+003
1.0435E+003
6.9567E+002
3.4783E+002
0.0000E+000

(d)

(e)

Figure 37. (a) Simulation model, (b) loop antenna, (c) S_{11} phase versus frequency, (d) electric field, and (e) magnetic field

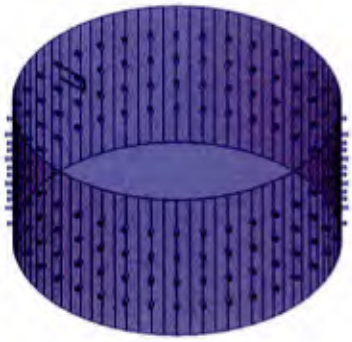
In order to cross-check the ohmic Q and external Q of the cavity, HFSS simulation was performed with AL6061 conductivity = 2.5E7 [S/m]. Figure 38(a) and Figure 38(b) show the HFSS model with a single loop antenna and an impedance locus at a detuned short position. Both ohmic Q and external Q were obtained by the use of the impedance measurement technique described in detail in Reference 10 and 11. Ohmic Q and external Q and loaded Q are obtained from

$$Q_{ohmic} = \frac{f_r}{f_2 - f_1} \tag{10}$$

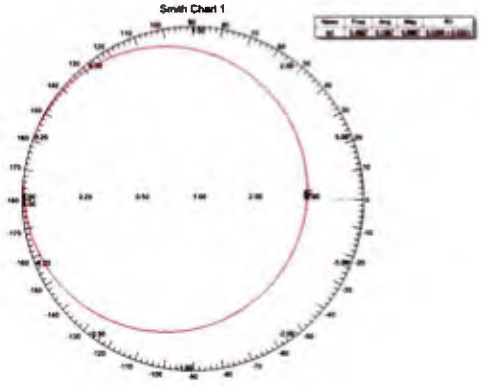
$$Q_{ext} = \frac{f_r}{f_4 - f_3} \tag{11}$$

$$Q_{Load} = \frac{f_r}{f_6 - f_5} \tag{12}$$

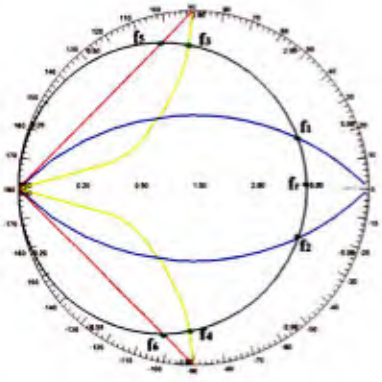
where f_1, f_2, f_3, f_4, f_5, and f_6 are defined in Figure 38(c). As shown in Figure 38(c), the frequencies are those intersecting with the cavity impedance locus at detuned short position. Ohmic Q and external Q were found to be 5,400 and 27,000, respectively at 456 MHz. The ohmic Q and external Q were in good agreement with the previous HFSS simulated results (ohmic Q = 27,000, external Q = 5,300). The resonant frequency shift from 460 MHz is due to the effect of the 40 antenna ports modeled in this simulation. Table 7 summarizes the simulation results.



(a)



(b)



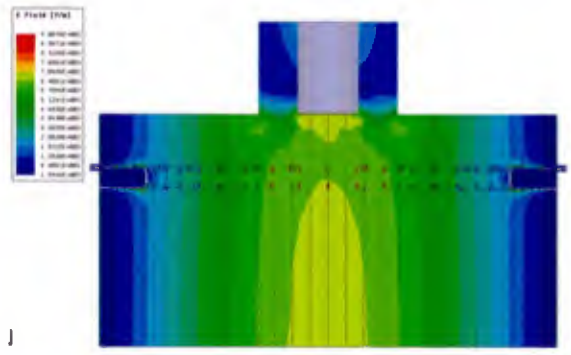
(c)

Figure 38. (a) HFSS model with a single loop antenna, (b) an impedance locus at a detuned short position, (c) admittance locus for impedance measurement technique

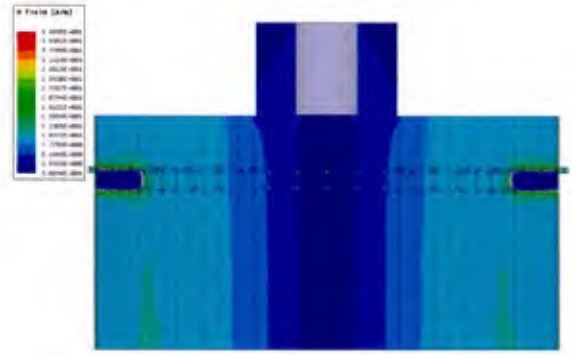
Table 7. Summary of HFSS simulation results where the conductivity of cavity is 2.5E7 [S/m] (ideal conductivity of AL6061)

Parameter	Specifications
Frequency	456 MHz
S_{11}	-3.6 dB
Unloaded Q	27,000
External Q	5,400
Loaded Q	4,500
β_{in}	5

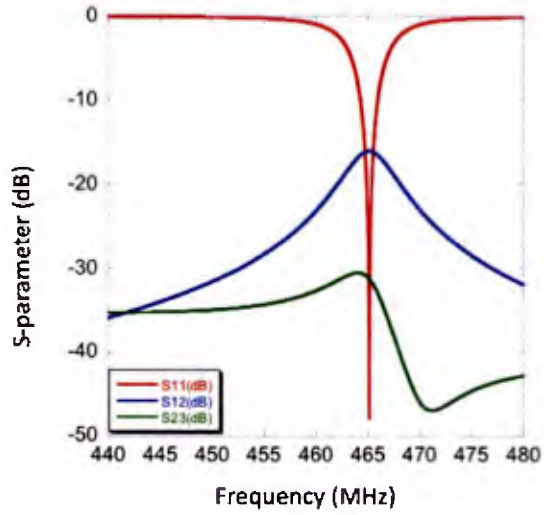
Now, a full-model simulation with all 40 loop antennas (all 40 antennas are identical) and an output port (6-1/8" coaxial transmission line) was performed. Figure 39 shows HFSS simulation results of the 40-way power combiner: (a) electric field, b) magnetic field, (c) scattering parameters (port 1 denotes output port, port 2 and 3 are two input ports among 40 input ports), and (d) isolation between two input ports. Table 8 shows the summary of HFSS simulation results. Note that uniform magnetic field strength is observed along the cavity axis near the wall. Good field uniformity is required for maximizing power combining efficiency. As shown in Figure 39(c), return loss seen from the output port is S_{11} = - 48 dB, suggesting that the 40-way cavity combiner works as a 40-way power divider (or, combiner). The center conductor of the 6-1/8" output transmission line was placed at - 1.4 mm (outward from the cavity surface). It should be noted that the center conductor was tuned for low return loss. As seen in Fig. 39(c), a critical coupling occurred at a center frequency of 465 MHz, resulting in a high combining efficiency of 99.34 %. Here, 40 input ports were assumed to be injected with 1 W each (with equal phase) and output power was calculated from HFSS field calculator. S_{21} = - 16.09 dB denotes that only 0.09 dB loss occurs during power division (or combination). Such a high combining efficiency meets the design goal of the 40-way cavity power combiner. The 3-dB bandwidth was predicted to be 1 %, which is slightly narrower than the initial analytic bandwidth (1.5 %). Isolation (or cross-coupling) between input ports was S23 = 31 dB. The high isolation is not affecting on adjacent power amplifiers at all. Simulations also predicted a maximum field stress of 3 kV/cm is observed at the center conductor of the 6-1/8" coaxial line when all input ports are injected with 2 kW each. This field stress is well below than the air break-down limit (30 kV/cm).



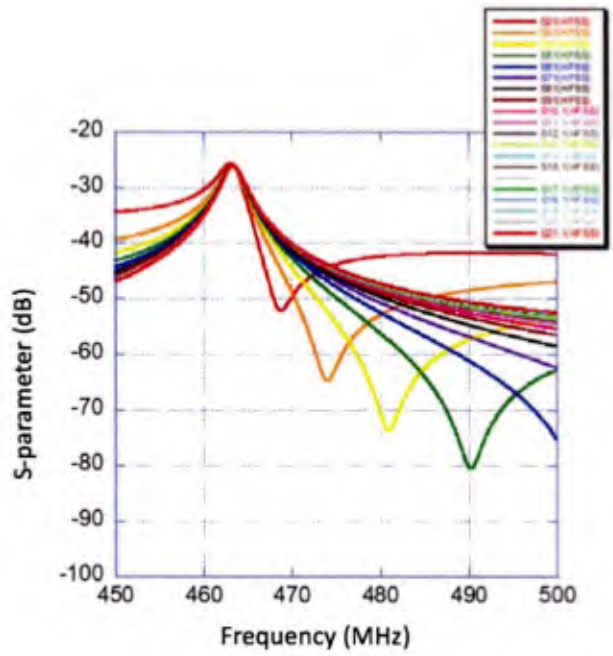
(a)



(b)


0
-10
-20
-30
-40
-50
S-parameter (dB)
S11(dB)
S12(dB)
S23(dB)
440 445 450 455 460 465 470 475 480
Frequency (MHz)

(c)



(d)

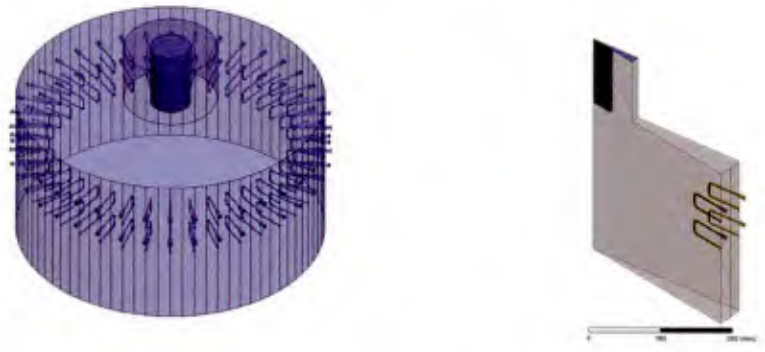
Figure 39. HFSS simulation results of the 40-way power combiner: (a) electric field, (b) magnetic field, (c) scattering parameters, and (d) isolation between input ports

Table 8. Summary of full model HFSS simulation results

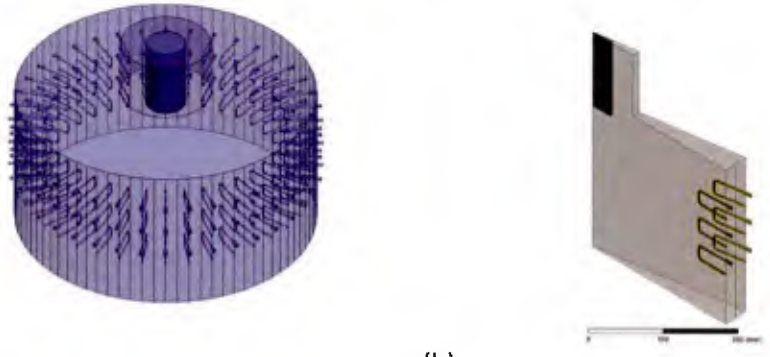
S_{11}(Resonance)	-47.86 dB
S_{21}(Combining)	-16.09 dB
S_{23}(Isolation)	-31.20 dB
Combining efficiency	99.34 %

Similar to the design work of the 40-way power combiner, we have designed power combiner for N= 80, 120, and 160. The design procedure is the same as the 40-way power combiner. Due to the limited memory capacity of the PC (Intel Core i7-3770 CPU @3.4 GHz, RAM = 32 GB), symmetry boundary conditions (perfect H boundary condition) had to be applied to save simulation space, memory and run-time. Figure 40 shows the full model and symmetry model of 80-way, 120-way and 160-way power combiners. Table 9 shows simulation results of the three power combiners. As shown in Table 9, one can tune for optimal power combining efficiency by adjusting the location of center conductor of the 6-1/8" coaxial line. Note that, instead of tuning input antenna, we tuned the output port for facilitating tuning job for critical coupling of the

cavity for any number of input ports. It is anticipated that the power combining efficiency is more than 99 %, no matter how many SSPA modules are mounted on the cavity.



(a)



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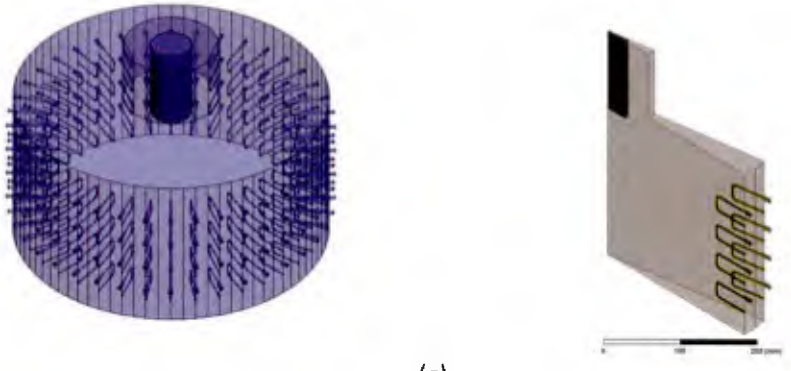


(c)

Figure 40. HFSS full model and symmetry model: (a) 80-way, (b) 120-way, and (c) 160-way power combiners

Table 9. Simulation results of N = 80, 120, and 160 power combiners, along with N = 40 power combiner

Number of antenna	Center pin height (mm)	Resonance frequency (MHz)	S_{11} (dB)	Bandwidth (%)	Combining Efficiency (%)
40	- 1.4	466.76	- 42.05	1.0	99.28
80	6.3	469.00	- 47.81	2.1	99.50
120	22.0	470.87	- 58.22	3.1	99.45
160	28.0	474.20	- 49.14	4.1	99.25

The general expression for a combined power with N input ports is given by

$$P_{out} = \frac{1}{N}\left(\sum_{i=1}^{N} P_{in}^{i}\right)^{2} \tag{13}$$

where P_{in}^{i} is an individual power of input ports. Here, we assumed perfect matching on all ports and infinite isolation between input ports. Also, we neglected insertion loss associated with ohmic power dissipation in the combiner. Power combining efficiency of the cavity power combiner decreases gradually as any number of transistors fails during the operation. Assuming that all input powers are identical, power combining efficiency is expressed as

$$\eta_{comb} \equiv \frac{P_{out}^{N-m}}{P_{out}^{N}} = \left(1 - \frac{m}{N}\right)^{2} \tag{14}$$

where m is the number of failed transistors, P_{out}^{N} is the combined power of all N transistors and the combined power of (N-m) working transistors. Figure 41 shows the calculated combining efficiency versus the number of failed input sources. The effect on degradation of power combining efficiency due to amplifier failure was investigated using the HFSS simulation code. Figure 42 shows the HFSS simulated power combining efficiency versus the number of failed amplifiers. As expected, the power combining efficiency was gradually degraded as the number of failed amplifiers increases. The difference between the calculated and simulated combining efficiency is originated from the fact that we assumed ideal combiner in the calculation. Such a graceful degradation observed in this multi-way power combining system is advantageous over conventional HPM vacuum tubes such as klystron and magnetron. Table 10 shows a comparison between the transmission-line type power combiner and cavity power combiner.

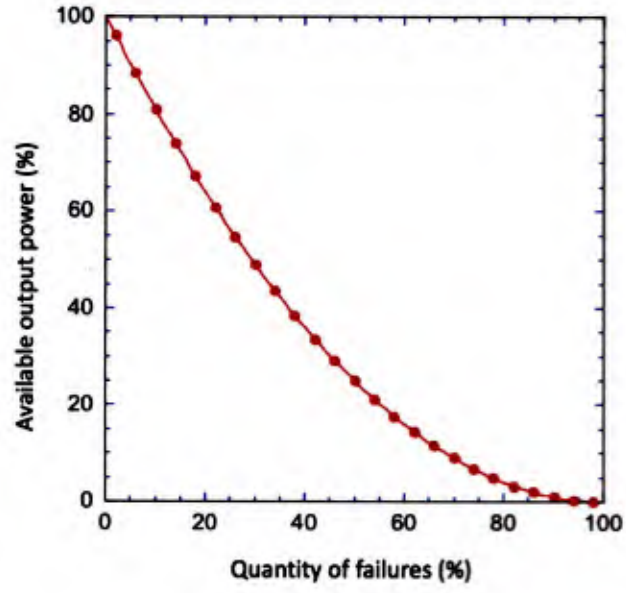


Figure 41. Calculated combining efficiency versus the number of failed input sources

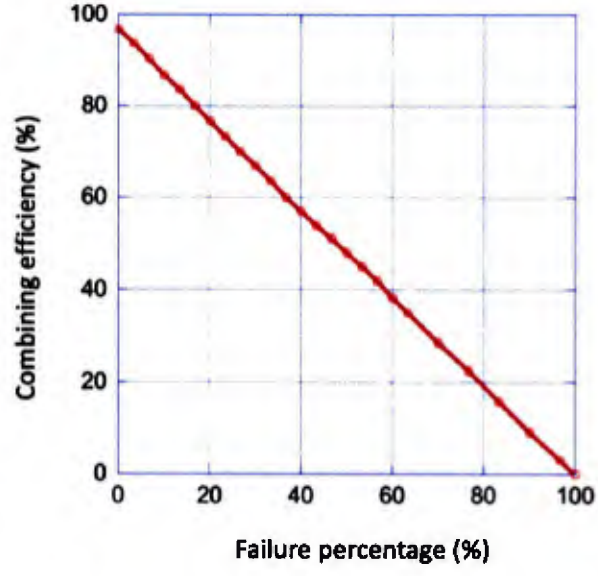


Figure 42. Power combining efficiency obtained from HFSS simulations versus the number of failed amplifiers

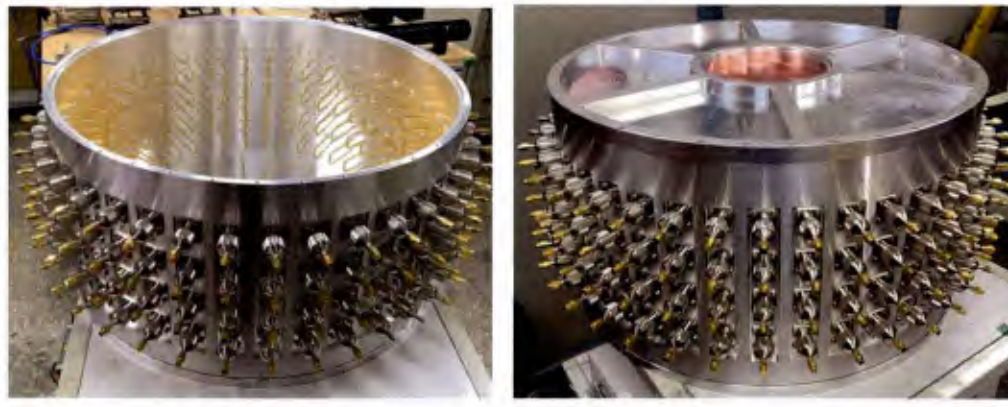
Table 10. Comparison between the transmission-line type power combiner and cavity power combiner

	Transmission-Line	Cavity
Efficiency	> 90 %	> 95 %
Bandwidth	> 50 % (Related to impedance matching)	< 5 %
Power Handling	Moderate	Good
Number of inputs	Limited by size	> hundreds
Size	Large	Compact
Effect on Failure	Sensitive	Insensitive

5.3 Fabrication and cold-test of cavity power combiner

Figure 43 shows a photo of the fabricated power combiner. There are 4 rows of loop antennas mounted on the cavity sidewall. Each row has azimuthally equally spaced 40 loop antennas. The fabricated cavity can operate with 160 SSPA modules in maximum. The fabricated cavity parameters are summarized in Table 11.

Cavity external and ohmic Qs for a single loop antenna were measured. Figure 44 shows the measured resonant frequency and impedance locus compared with HFSS simulated result. Resonant frequency was measured by two port transmission coefficient (S_{21}). The measured resonant frequency was 457 MHz, which is 1 MHz higher compared with the simulated frequency, 456 MHz. The simulation results give more over-coupled (lower impedance) than the measurement. This is because the conductivity of ideal AL6061 (2.5E7 [S/m]) was used in the simulation. Using the impedance measurement technique, we measured unloaded (ohmic) Q = 20,000 and external Q = 5,200 at a resonant frequency = 457 MHz. We could get the same unloaded Q as the measured value (20,000) when the conductivity was set at 1.4E7 [S/m], which is 56 % of the ideal conductivity. Figure 45 shows measured isolation between input ports. As shown in Figure 45, isolation of more than 26 dB was observed between any pair of two input ports, which agrees well with HFSS simulation results earlier shown in Figure 39(d). Table 12 shows comparison between measured and HFSS simulation results.

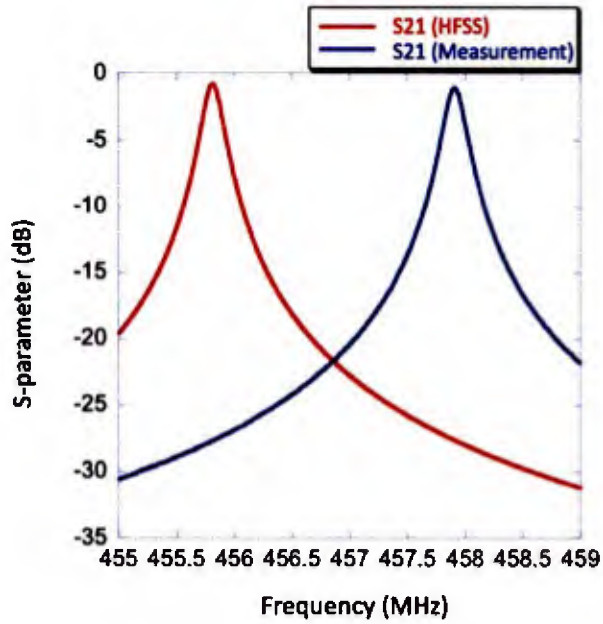


(a) (b)

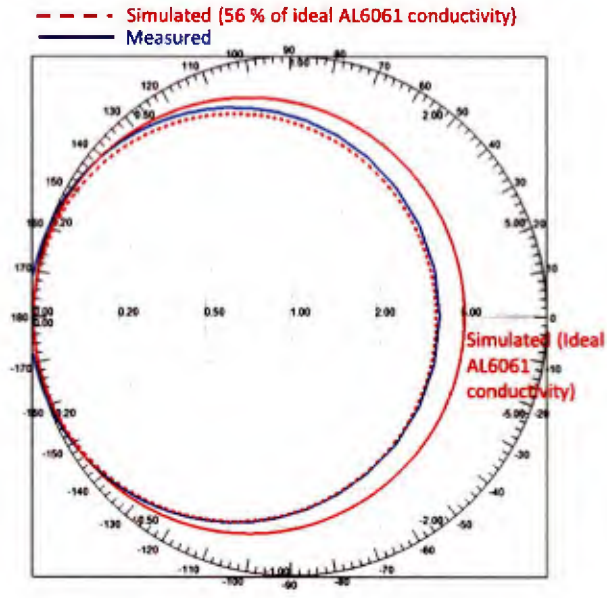
Figure 43. Fabricated power combiner showing (a) 160 loop antennas inside and (b) outside view of the cavity with 160 N-type connectors

Table 11. Parameters of cavity combiner

Parameter	Specifications
Number of input ports	160 (any number of input ports can be selected)
Input connector	Type-N (female)
Output connector	6-1/8" coaxial transmission line
Material	Aluminum 6061
Diameter	500 mm
Length	250 mm



(a)



(b)

Figure 44. (a) Measured resonant frequency (S_{21}) and (b) impedance locus compared with HFSS simulated result (S_{11})

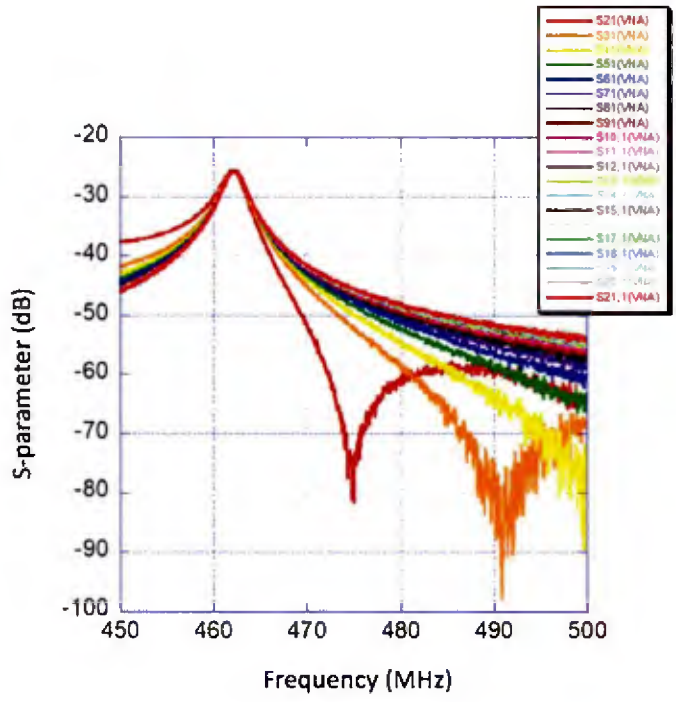


Figure 45. Measured isolation between input ports

Table 12. Comparison between measured and HFSS simulation results

	HFSS (ideal conductivity= 2.5E7 [S/m])	HFSS (ideal conductivity= 1.4E7 [S/m])	VNA
Frequency (MHz)	456	456	457
S_{11} (dB)	- 3.6	- 4.3	- 4.3
Unloaded Q	27,000	20,000	20,000
External Q	5,400	5,200	5,200
Loaded Q	4,500	4,500	4,500
β_{in} (N=1)	5	3.9	3.9

Cold-test of 40-way power combiner

A 40-way power combiner was cold-tested to measure combining efficiency, return loss and isolation between input ports. Figure 46 shows a photo of the test setup. 40 loop antennas and one 6-1/8" output line were installed. The 40-way divider (described in Chapter 6) was used to divide equal phase and equal amplitude to all 40 input ports. We adjusted the center conductor of the 6-1/8" coaxial transmission line to see the effect on coupling strength. Figure 47 shows measured scattering parameters by changing the center conductor's location (zero denotes the reference surface of the cavity). As shown in Figure 47, the transmission loss was - 1.03 dB at 464 MHz when the center conductor was placed at - 1.6 mm outward from the cavity surface. Compared with - 1.4 mm predicted from HFSS simulation, this measured result (- 1.6 mm) showed an excellent agreement. Considering power divider loss (0.5 dB) and interconnecting cable loss (0.4 dB), the cavity combiner loss is 0.13 dB. This corresponds to the measured power combining efficiency of 97 %, which agrees well with the simulated value of 99 %. Figure 48 depicts measured scattering parameters as functions of frequency for the center conductor location = - 1.6 mm.

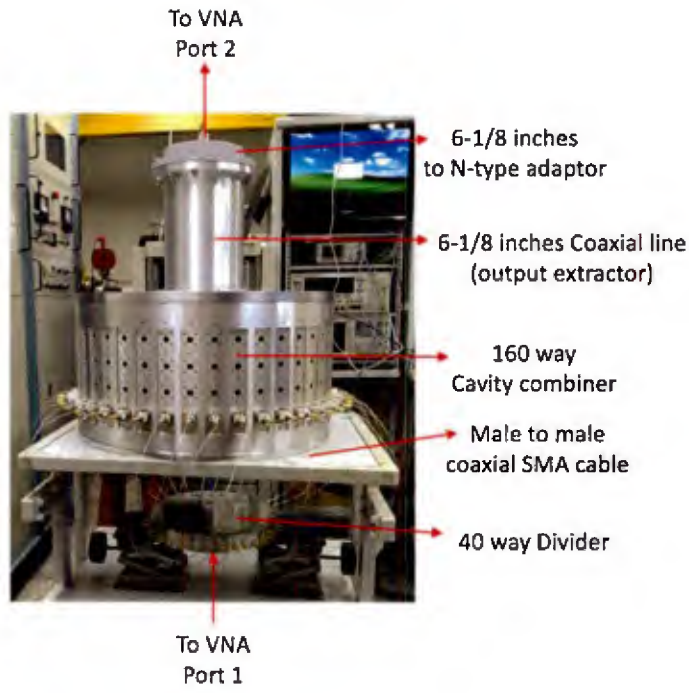
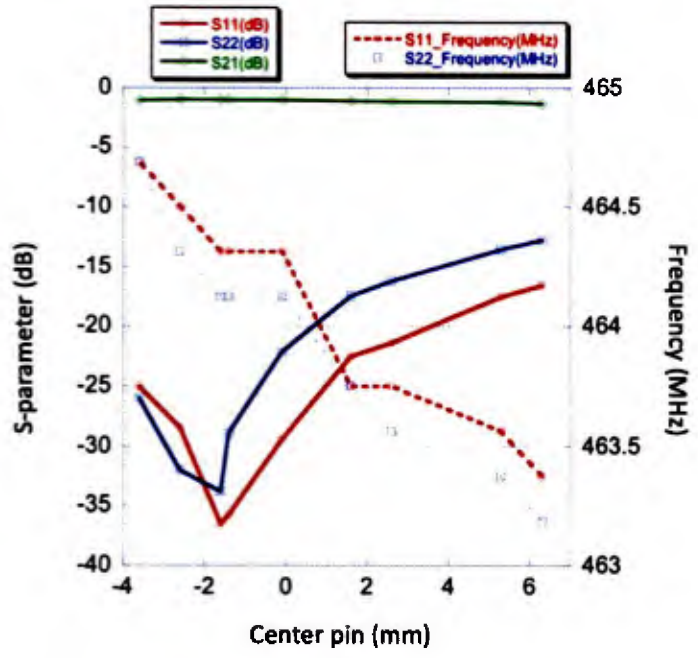
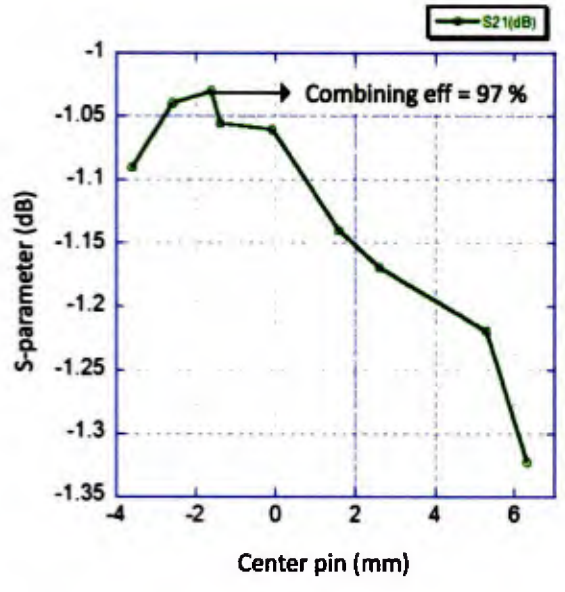


Figure 46. Photo of the 40-way power combiner test setup



(a)



(b)

Figure 47. Measured scattering parameters by changing the center conductor's location (here, zero denotes the reference surface of the cavity)

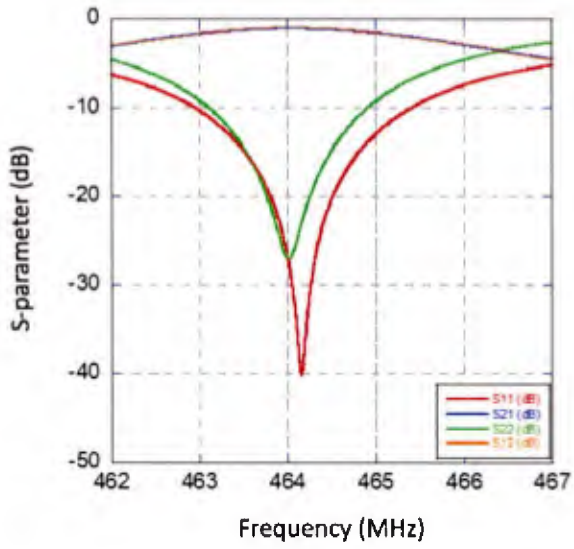


Figure 48. Measured scattering parameters as functions of frequencies for the center conductor location = - 1.6 mm

Cold-test of 80-way power combiner

Cold-tests of the 80-way power combiner were also performed using VNA in order to measure power combining efficiency. 80 identical loop antennas were installed in the cavity. Figure 49 shows a schematic layout. One Wilkinson power divider and two 40-way power dividers were used to inject equal phase and equal amplitude to 80 input ports. Figure 50 shows return losses measured from 6-1/8" port by varying the position of center conductor of the 6-1/8" coaxial transmission line. A strong resonance peak was observed at 467 MHz. Measurements shows return loss of – 14 dB at the predicted optimal position of the center conductor = + 6.3 mm. As shown in Figure 50, the return loss decreases as the conductor moves inward from the cavity surface. A good return loss of -33 dB was observed at +13.5 mm. Cold-test showed that the conductor should be placed more inward, compared with the HFSS simulated results (+ 6.3 mm). RF losses measured from a calibrated VNA were 0.29 dB in Wilkinson divider, 0.58 dB in first blue cable, 0.4 dB in 40-way divider, 0.37 dB in the second SR-250 cable, and 0.61 dB in second blue cable, resulting in 2.25 dB in total. The measured S_{21} was 2.33 dB. Taking all losses into account in the S_{21} measurements, the combining loss in the cavity was found to be 2.33 dB – 2.25 dB = 0.08 dB. This corresponds to a combining efficiency of 97 %, which agrees well with the HFSS simulated result (99 %). Note that the combining efficiency of the 80-way power combiner was not degraded compared with 40-way power combiner, as expected from the HFSS simulation results earlier shown in Table 9.

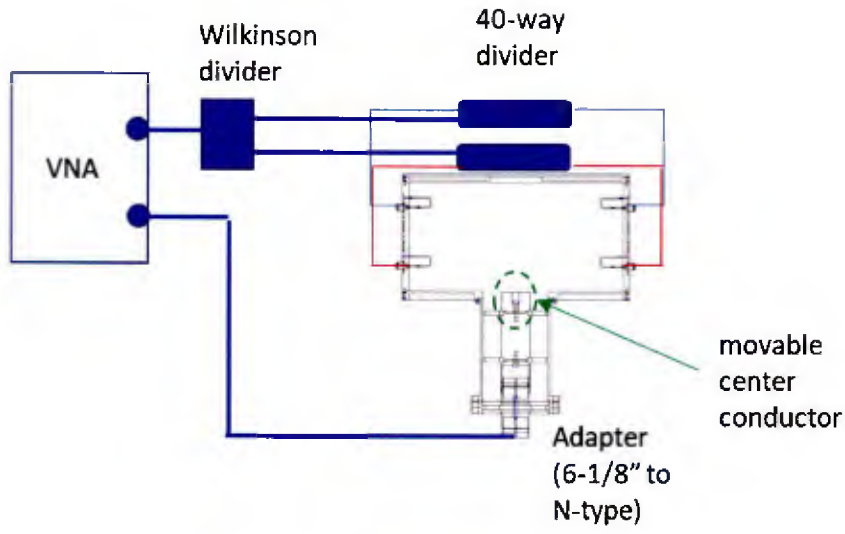


Figure 49. Schematic layout for 80-way power combiner cold-test

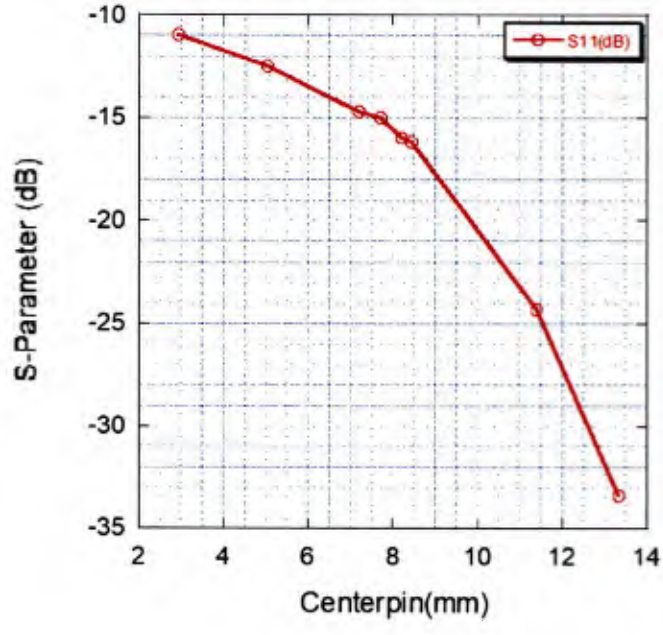


Figure 50. Return loss measured from 6-1/8" port by varying the position of center conductor of the 6-1/8" coaxial transmission line

Chapter 6. 40-way power divider

6.1 Design of power divider with equal amplitude and phase

The 80 SSPA modules require RF input drive signals. In order to maintain a high combining efficiency in the cavity combiner, equal phase and equal amplitude should be guaranteed at all the input drive signals. Two identical 40-way power dividers are utilized for dividing the 8 kW RF power into eighty 100 W RF power branches.

The 40-way radial power divider was designed by using analytic theory and 3-D EM simulator, HFSS. As shown in Figure 51, the divider consists of a 10-way radial power divider and 2 stage Wilkinson dividers. The dielectric circuit board is AD250 (dielectric thickness = 0.8 mm, dielectric constant = 2.5, loss tangent = 0.0016). The length of 10 equal microstrip transmission lines is a quarter wavelength at center frequency = 467 MHz. The characteristic impedance of the 10 equal microstrip transmission lines should be 50 ohm x $\sqrt{10}$ = 158 ohm. The transmission line width calculated from ADS line calculator is 0.15 mm. Note that the width becomes thinner as the number of dividing lines increases. Line width resolution and power handling capability will limit the maximum number of the dividing ports. Figure 52 shows the HFSS model of 10-way radial divider. The height of the center conductor of the Type-N connector was tuned in order to have a better matching condition. As shown in Figure 53, the simulated return loss of the 10-way radial power divider seen at the Type-N connector was -30 dB at center conductor height = 5 mm, which was improved by 6 dB compared with that before tuning.

A 3-dB Wilkinson power divider was designed. The length of the dividing branch is a quarter wavelength and the width is chosen so that the characteristic impedance becomes 50 ohm x $\sqrt{2}$ = 71 ohm. The Wilkinson divider located at the output end has isolation resistors in order to prevent cross-coupling between output ports.

Simulations on the full model of the 40-way divider were carried out where port 1 stands for input port, and the output ports are from port 2 to port 41. Figure 54 shows the plot of electric field of the 40-way power divider obtained from HFSS Simulation. All the 40 output ports have equal phase as expected. Figure 55 shows HFSS simulated scattering parameters of the 40-way power divider. Simulation predicts return loss = 15 dB, isolation = 23 - 32 dB, and power division ratio = 16.1 dB at 467 MHz. The simulated power division ratio is very close to ideal value (16 dB) for power division by 40.

Figure 51. 40-way power divider consisting of a 10-way radial power divider and 2 stage 3-dB Wilkinson dividers.

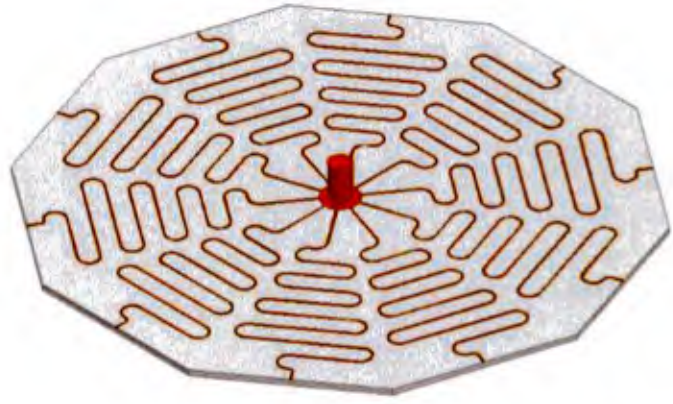


Figure 52. HFSS model of 10-way radial power divider (center conductor height = 5 mm)

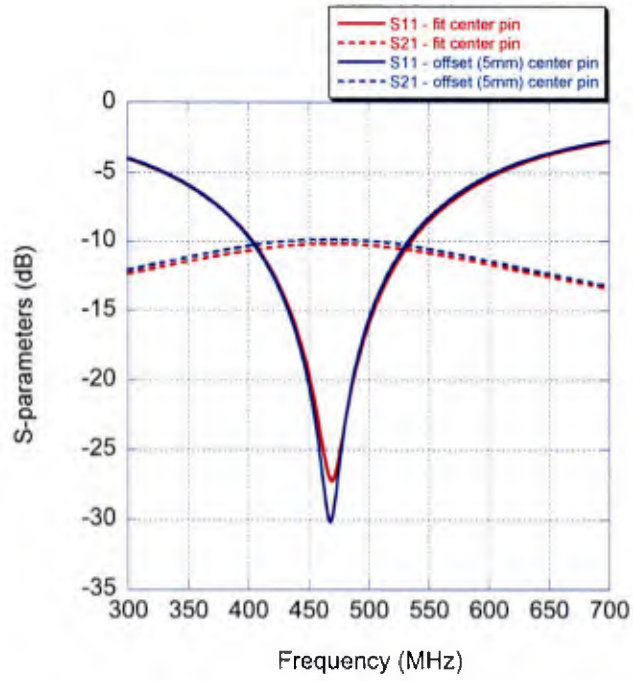


Figure 53. Return loss of 10-way radial divider seen at the Type-N connector

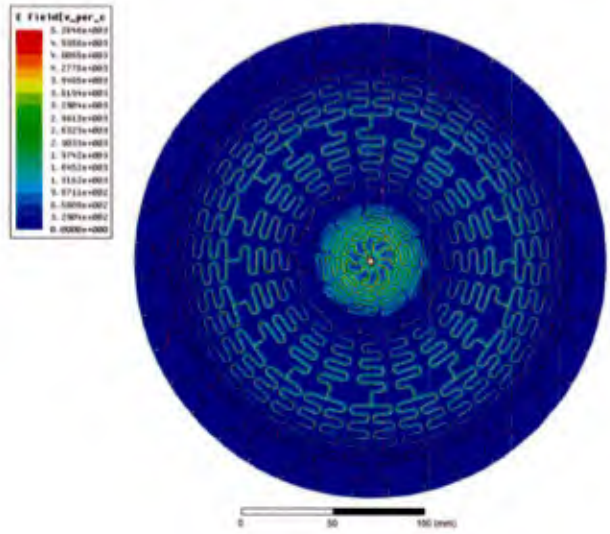


Figure 54. Plot of electric field of the 40-way power divider obtained from HFSS Simulation

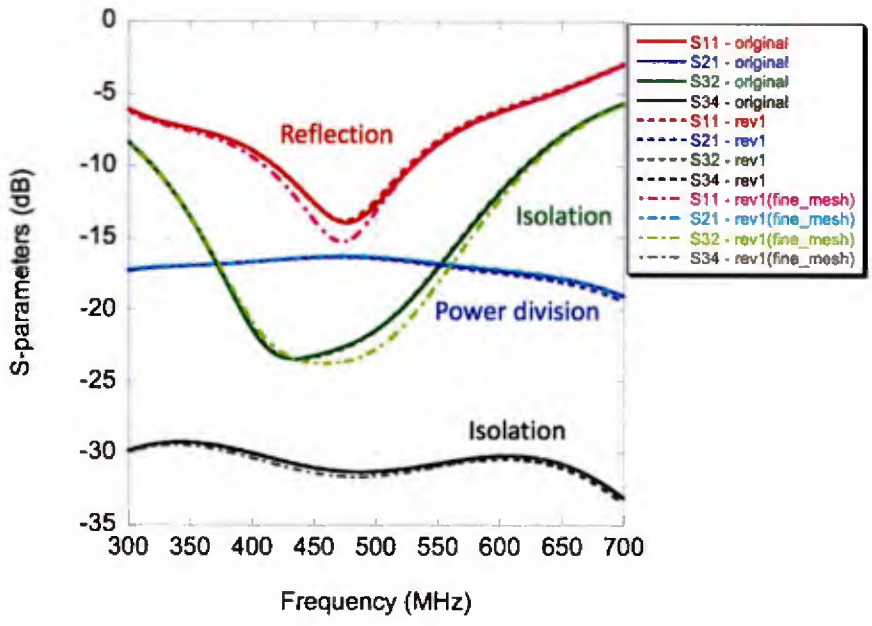


Figure 55. HFSS simulated scattering parameters of the 40-way power divider

6.2 Fabrication and cold-test of 40-way power divider

Based on the design and simulation result described in Section 6.1, a 40-way power divider was fabricated. Figure 56 shows a photo of the fabricated 40-way power divider. RF input connector is the standard Type-N coaxial connector and the 40 output connectors are the standard SMA coaxial connectors. Scattering matrices for transmission and isolation are measured using a calibrated VNA. Figure 57 shows measured power division and return loss compared with the HFSS simulation results. As shown in Figure 57, the dividing factor is – 16.2 dB (ideal value = -16 dB for the case of no loss) and the return loss is less than -25 dB. The measured return loss (-25 dB) was tuned by changing the height of the center conductor of the Type-N connector and found to be better the simulated result (-15 dB).

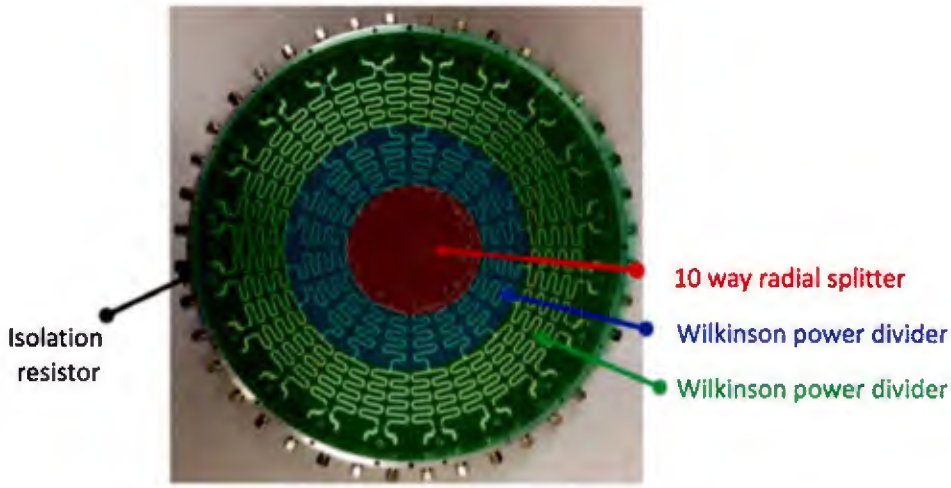


Figure 56. Fabricated 40-way radial power divider

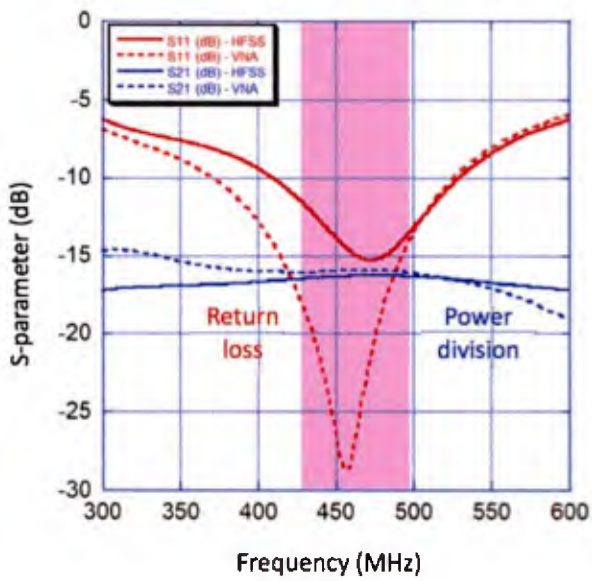


Figure 57. Measured scattering parameters of 40-way power divider

The 40-way power divider was tested at various high duty cycle to see if any thermal runaway takes place due to temperature rise in the dielectric-filled printed circuit board. Here, the input power was set at 8 kW in peak (the RF power driven by four 2 kW SSPA modules described

in Secion 9.3). Figure 58 depicts the temperature (taken by the use of the infrared camera) as functions of duty cycles. The highest temperature was observed on the thin microstrip transmission line of the 10 raidal divider. It increases fairly linearly along the duty cycle, reaching 53 degree C at duty cycle = 20 % (corresponding to average power = 1.6 kW). Figure 59 shows (a) Photo taken at room temperature before RF injection, and (b) thermal image taken at duty cycle = 20 %. The PCB should hold up to a maximum temperature of 350 degree C.

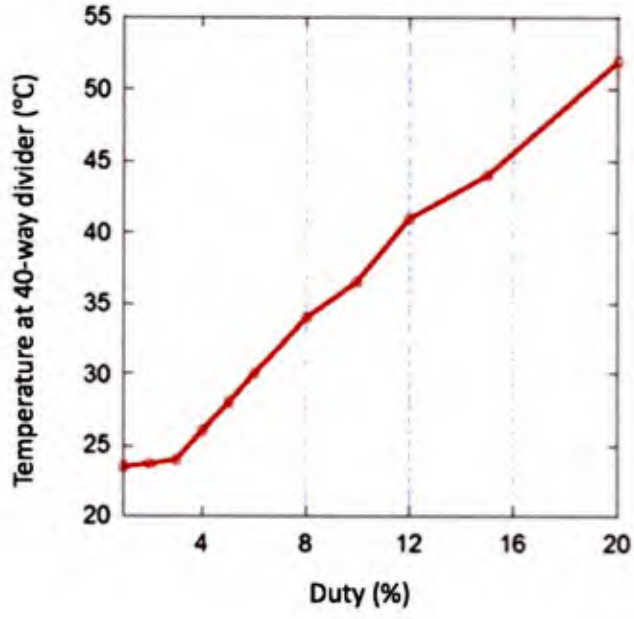
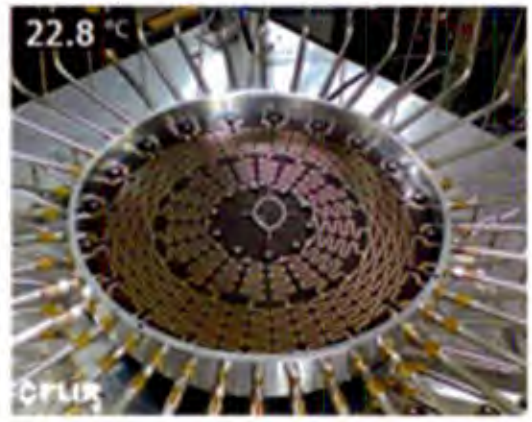
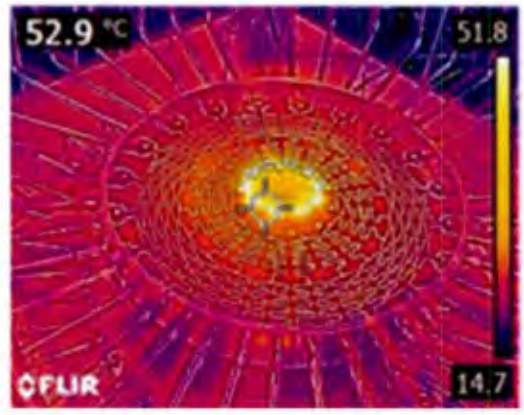


Figure 58. Temperature rise seen on the thin microstrip transmission line of the 10 raidal divider as functions of duty cycle.



(a)



(b)

Figure 59. (a) Photo taken at room temperature before RF injection, (b) thermal image with RF taken at duty cycle = 20 %

Chapter 7. RF water load

The high power (200 kW) RF generated from the cavity combiner has to be absorbed in a RF terminator. We have designed and fabricated a water-cooled RF load for the use of our 80-way power combiner system.

7.1 Measurement of dielectric properties of cooling water

There are many coolants used in high power RF systems to dissipate RF power. Both glycol and Ethylene-glycol water [12] were used in hundreds kW and UHF dummy loads because glycol has a high dielectric loss tangent. Since glycol has an ecological problem, a water mixed with sodium-molybdate can be a substitute coolant.

When RF power enters into a lossy dielectric medium, the amount of time-average RF power dissipated in a volume v is given by [13]

$$P_{dissipation} = \frac{\omega}{2}\int_v \varepsilon''\left|\vec{E}\right|^2 dv = \frac{1}{2}\omega\varepsilon_o\varepsilon_r' \cdot \tan\delta_e \cdot \int_v \left|\vec{E}\right|^2 dv \tag{15}$$

where ε_r' is relative dielectric constant, $\tan\delta_e$ is loss tangent, and E is electric field in the lossy dielectric. Note that, in order to have a high dissipation power, one needs a coolant medium with both high dielectric constant and high loss tangent. The attenuation rate [dB/m] along the axial distance in the lossy dielectric medium is written as [13]

$$\alpha_d = \frac{\omega\varepsilon''\eta}{2} = 9.1 \times 10^{-8} \cdot f \cdot \tan\delta \cdot \sqrt{\varepsilon_r} \quad [dB/m] \tag{16}$$

where f is the operating frequency. This equation provides us an initial design parameter of the length of the lossy dielectric medium, or how long the RF load should be for given frequency, dielectric constant, and loss tangent of the lossy dielectric.

We have measured complex dielectric permittivity of two types of coolants: a tap-water (the simplest coolant) and a water mixed with sodium-molybdate by the use of a probe measurement technique. The basic equation and measurement technique is described in Reference 14. An equivalent circuit of a transmission line terminated with a lossy dielectric material is shown in Figure 60. The load admittance is expressed by sum of three terms: (1) internal admittance (relating to the capacitance (Ci) due to the fringing field in the dielectric region of the coaxial probe), (2) the admittance (relating to the capacitance (C) due to the

fringing field in the dielectric material) and (3) the radiation conductance (G) in the dielectric material. Here, the sample is assumed to be thick enough so that all the radiation is dissipated in the dielectric material. The total admittance is rewritten as

$$Y_L(\omega, \varepsilon) = j\omega C_i + j\omega C_0 \varepsilon_r + jB\omega^3 \varepsilon_3^2 + A\omega^4 \varepsilon_3^{2.5} \tag{17}$$

where the four constants (Ci, C0, A, B) are obtained from 4 known materials. The four materials are air (ε_{r1} = 1.0006), distilled water (ε_{r2} = 78 - j4.2), methanol (ε_{r3} = 32.7 – j7), and acetone (ε_{r4} = 20.7 – j0.828) at 1 GHz. From the measured reflection coefficient, input impedance and input admittance for 4 materials, one can have 4 sets of linear equations. Thus, one can obtain 4 unknown constants (Ci, C0, A, B) from the 4 sets of equations. The 4 linear equations with variables of complex numbers are solved by using MATLAB. Using Eqn. (17) above with given 4 known constants, one can now measure dielectric permittivity, which is ε_r in Eqn. (17) by measuring Y_L with a tap-water and a water mixed with molybdate. The real and imaginary values of ε_r represent dielectric constant and loss tangent, respectively.

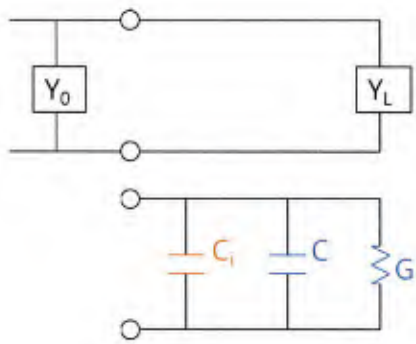


Figure 60. An equivalent circuit of a transmission line terminated with a lossy dielectric material

Figure 61 shows the experimental setup for measuring dielectric properties using VNA. An open-ended coaxial cable is submerged in a 1 liter glass beaker filled with a lossy dielectric material (e.g. tap-water or tap-water mixed with sodium-molybdate). One port calibration of VNA was done and then the calibrated port was extended to the open ended coaxial cable by the use of 'port extension' option of VNA. Figure 62 shows the temperature dependence on dielectric constant and loss tangent of a tap-water at 1 GHz. The dielectric constant decreases linearly as the tap-water's temperature increases from 82 at 10 degree C to 28 at 90 degree C. However, the loss tangent decreases initially and increase gradually with temperature near 40 ~ 60 degree C. This increase of loss tangent is due to the increase of conductive loss of the tap-water, which was previously also observed in other literature [15]. As shown in Figure 62, the

tap-water's temperature should be kept near 10 degree C (where both dielectric constant and loss tangent are high) in order to achieve a high dissipation rate of the RF power.

Similarly, we have measured dielectric properties of a distilled water (1 liter) mixed with sodium-molybdate (Na2MoO4, 10 g) as a function of temperature. As shown in Figure 63, the dielectric constant appears to be similar to that of the tap-water. However, differently from the tap-water, the loss tangent increases with temperature. Note that the lowest value of the loss tangent is 0.2 at 10 degree C, which is higher than that for the case of a tap-water. Dielectric properties of the distilled water-molybdate mixture were measured by changing the fraction of molybdate in a 1 liter distilled water where temperature is 27.3 degree C. As shown in Figure 64, the loss tangent becomes higher as the amount of molybdate increases from 0.2 (10 grams) to 0.63 (60 grams). This indicates that the length of the RF load can be designed to be short if the distilled water-molybdate mixture is used as a coolant. However, one disadvantage would be that one needs a recirculating cooling system with a large cooling capacity. Table 13 shows a summary of the measured data.

Figure 61. Photo showing a probe measurement technique using VNA

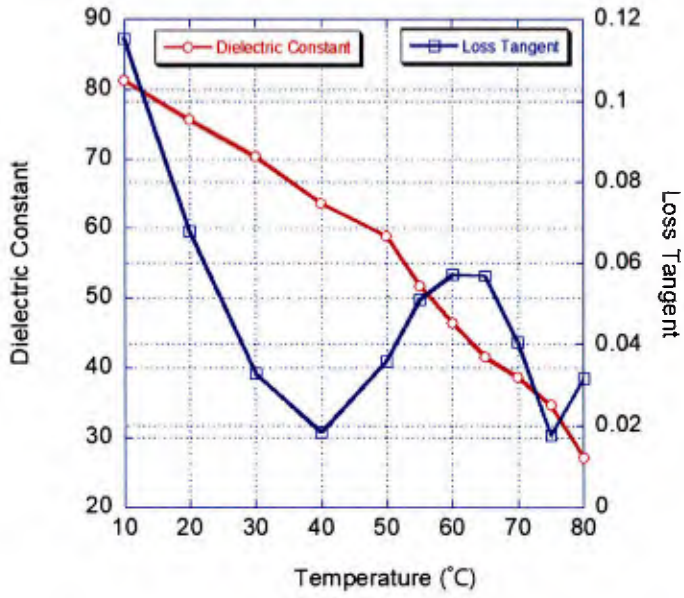


Figure 62. Temperature dependence on dielectric constant and loss tangent of a tap-water

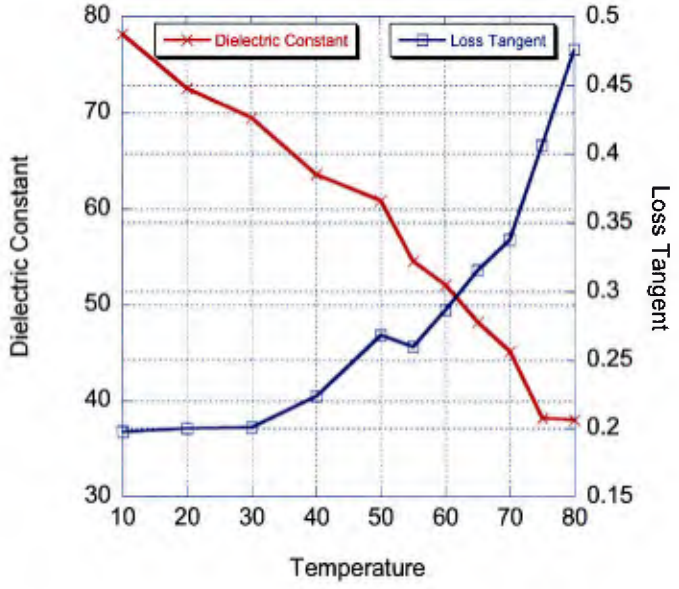


Figure 63. Temperature dependence on dielectric constant and loss tangent of a distilled water mixed with molybdate

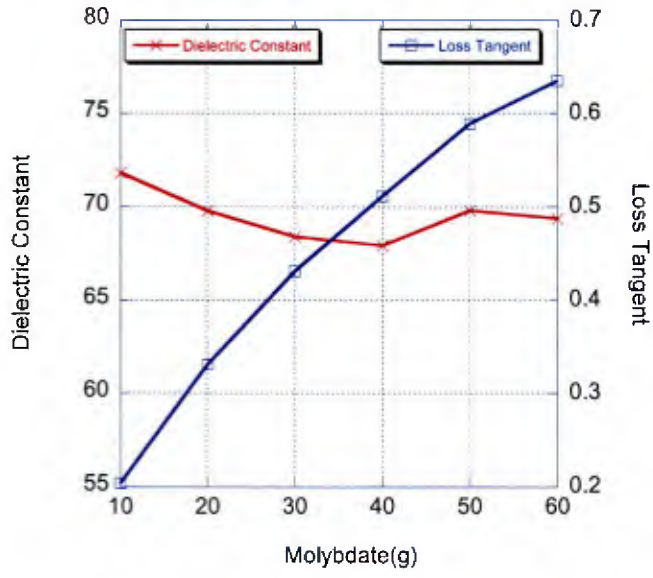


Figure 64. Dielectric constant and loss tangent of the distilled water-molybdate mixture as a function of the fraction of molybdate (temperature = 27.3 degree C, water volume = 1 liter)

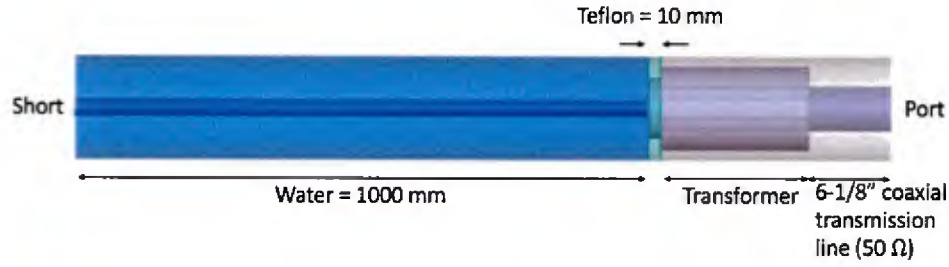
Table 13. Summary of the measured data (temperature: 10 – 80 degree C, molybdate = 10 g, water = 1 liter)

	Dielectric constant	Loss tangent
Tap water	80 ~ 27	0.1 ~ 0.01
Distilled water with Molybdate	79 ~ 38	0.2 ~ 0.47

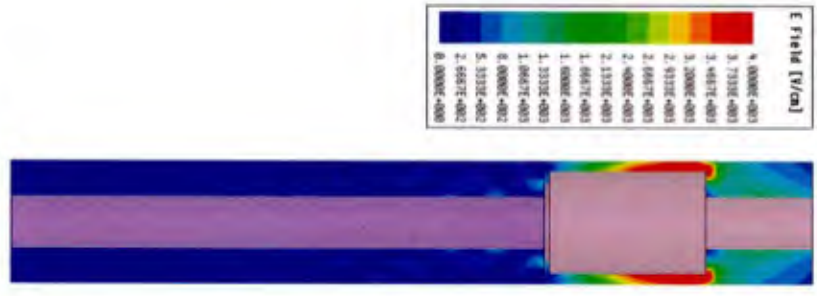
7.2 Design of RF water load

RF load is composed of air-filled 6-/18" coaxial line, impedance matching line, and RF-absorbing coolant. An impedance matching transformer is inserted between the 6-1/8" coaxial transmission line and the RF load so that all the RF power from the 6-1/8" coaxial transmission line dissipates without reflection. HFSS simulation was used to design the RF water load. The dielectric properties (dielectric constant and loss tangent) of the coolant measured in Section 7.1 were used in the HFSS simulations.

Figure 65 shows HFSS simulation model of the RF load, electric field and 3-D CAD drawing. Dielectric constant and loss tangent were set at 81 and 0.12 in the HFSS simulation, which are the measured values at 10 degree C for tap-water described in Section 7.1. The transformer is a quarter-wavelength impedance matching section placed between the 50 ohm air-filled 6-1/8" coaxial transmission line and the coolant-filled coaxial line. The inner conductor of the RF load was chosen to be 21 mm in diameter so that the characteristic impedance became high, making the broadband matching condition. A viton O-ring sealed Teflon plate (1 cm thick) was inserted to prevent water leak. Figure 66 shows the simulation results on return loss for different transformer lengths. The transformer's inner and outer diameters are 151 mm and 254 mm, respectively. The length in the figure's legend represents the length with respect to a reference length = 129 mm. As shown in Figure 66, a low return loss was found to be < - 20 dB over the frequency band (445 – 470 MHz) at transformer's length = 129 mm – 10 mm = 119 mm. When 200 kW RF power is injected into the load, a maximum electric stress of 4 kV/cm is seen at the edge of the transformer, which is well below the air-breakdown limit.



(a)



(b)

(c)

Figure 65. (a) HFSS simulation model of the RF load, (b) electric field, (c) 3-D CAD drawing

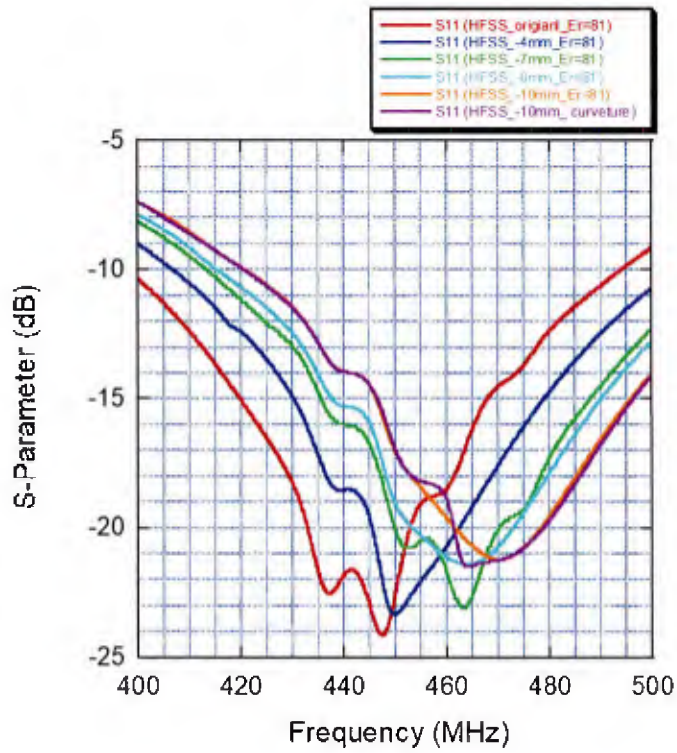


Figure 66. Simulation results on return loss for different transformer lengths

7.3 Fabrication and cold-test of RF water load

RF water load was fabricated based on the design parameters obtained from HFSS simulations. Figure 67 shows a photo of the fabricated RF water load. Inner and outer conductors and transformer are made of copper in order to minimize RF ohmic loss. The inlet water is injected through the center conductor and runs all the way to the end of the center conductor and is split via 6 holes. The outlet water exits through the side wall of the outer conductor.

Figure 68 shows the measured return loss of tap-water and tap-water mixed molybdate as a function of frequency, compared with HFSS simulation result. The measured return loss was found to be < - 17 dB in our operating frequency range (460 ~ 480 MHz), which agrees well compared with HFSS simulation results. The small ripple seen in the measured data is due to RF resonance between the short end of the RF load and the Teflon. It is interesting to notice that the ripple height for the case of tap-water molybdate mixture is a lot less than that of tap-water. This observation is expected from the fact that the tap-water molybdate mixture has a higher loss tangent than that of tap-water by a factor of 10 as shown in Section 7.1.

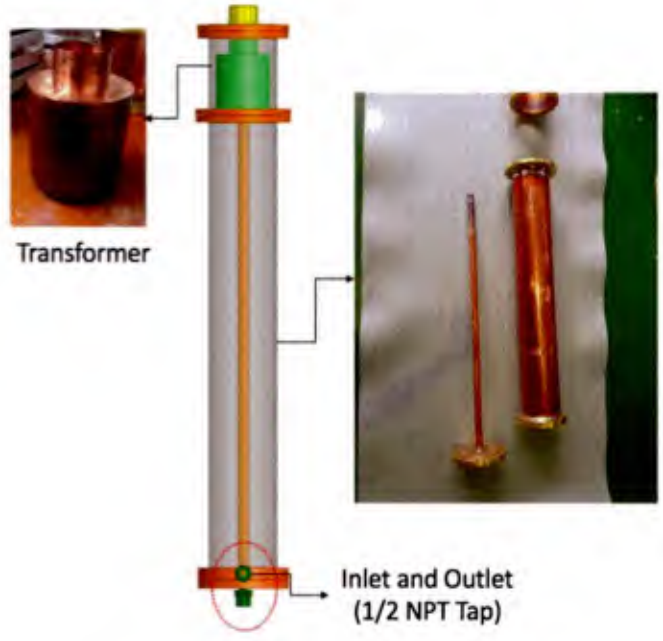


Figure 67. Photo of fabricated RF water load

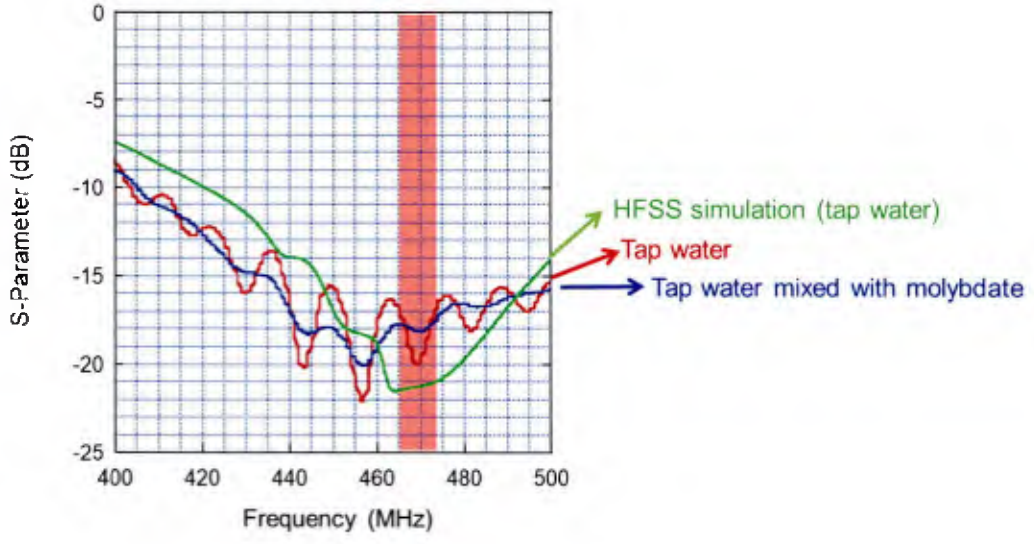


Figure 68. Measured return loss of tap-water and tap-water mixed molybdate as a function of frequency, compared with HFSS simulation result

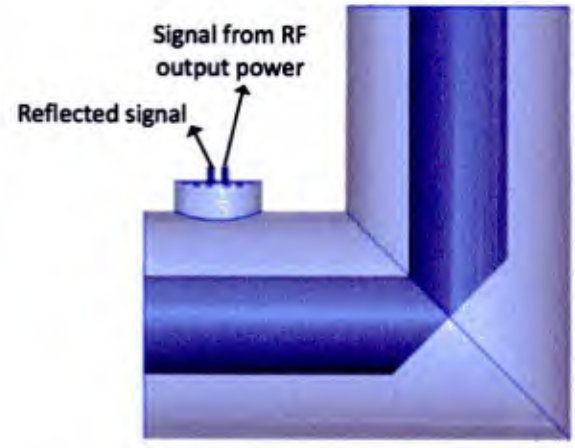
Chapter 8. Diagnostics and control circuits

8.1 Vestigial loop coupler

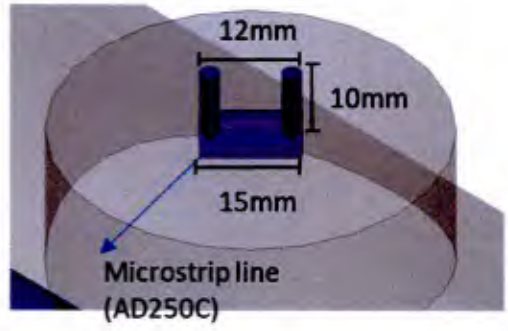
The 6-1/8" coaxial transmission line is the main transmission line carrying the full RF power (200 kW). Instead of direct measurement of the high peak power, a directional coupler is utilized to sample a small amount RF signal from the main transmission line. Vestigial loop couplers have been widely used for decades in many applications for particle accelerators and high power vacuum tubes. Figure 69 shows the vestigial loop coupler. The loop coupler is a short circular waveguide section in which the cutoff frequency of the RF wave is well below cutoff. The evanescent wave decays rapidly in the short circular waveguide and is coupled through a loop antenna. The coupling loop antenna is a microstrip line patterned on a dielectric circuit board. The loop antenna patterned on a dielectric laminate (AD250C) is suspended on a short circular waveguide and connected to two SMA connectors: one for forward power coupling and the other for reflected power coupling. Like other directional coupler, this vestigial loop coupler should have a high directivity for a given coupling factor. The directivity depends on the orientation of the loop antenna with respect to the axial direction of the main transmission line. The coupling strength is determined by the length of the short circular waveguide.

We have designed a vestigial coupler with coupling factor = 60 dB and directivity > 20 dB. Circular cavity size, loop dimension and its orientation were optimized using HFSS simulations. Simulation model, electric field distribution, and simulation results are plotted in Figure 70. The microstrip line loop is tilted by 45 degree with respect to the axial direction of the 6-1/8" coaxial transmission line. As shown in Figure 70(b), the forward coupling factor is 61 dB (the backward coupling is the same as of forward coupling due to the symmetrical structure). Directivity is found to be > 20 dB, meaning that only 1 % of the forward RF power is back-coupled into the reflected port. Since the RF load has a return loss of -17 dB (described in Section 7.3), the power reflected from the RF load is coupled to the forward power coupling port, resulting in an error of 0.02 % (17 dB + 20 dB = 37 dB). This is sufficiently low error enough to ignore in forward RF power measurement.

Based on the design obtained from the HFSS simulations, a 60 dB vestigial loop coupler was fabricated. Figure 71 shows a photo of the vestigial coupler assembled on the 6-1/8" coaxial transmission line. As shown in Figure 72, measurements show S_{21} (forward power coupling) = - 60 dB, which is in good agreement with the HFSS predicted value (- 61 dB). Directivity couldn't be measured accurately because of limited dynamic range of our VNA. However, the directivity is estimated to be better than 20 dB.

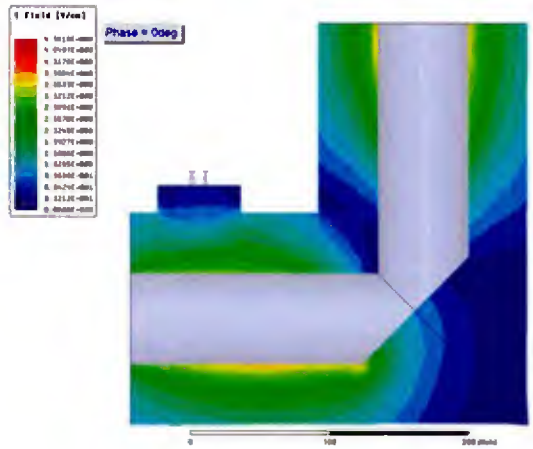


(a)

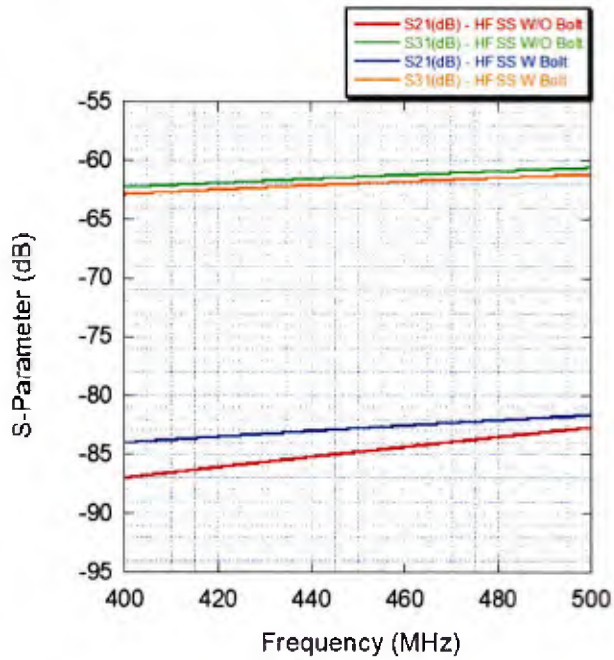


(b)

Figure 69. Vestigial loop coupler: (a) coupler mounted on 6-1/8" coaxial transmission line and (b) dimension of the coupling probe



(a)



(b)

Figure 70. (a) electric field distribution, (b) simulation results of scattering parameters

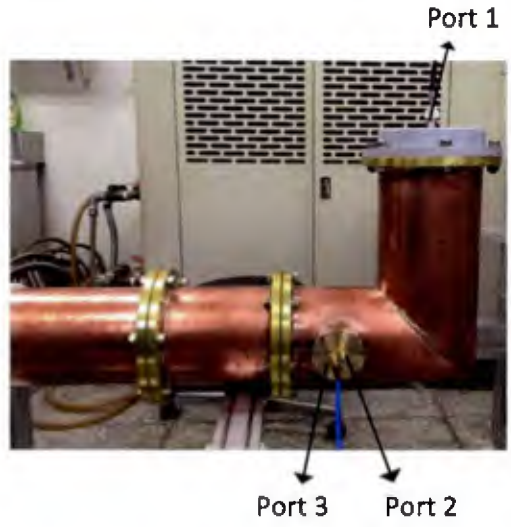


Figure 71. Photo of the vestigial coupler assembled on the 6-1/8" coaxial transmission line.

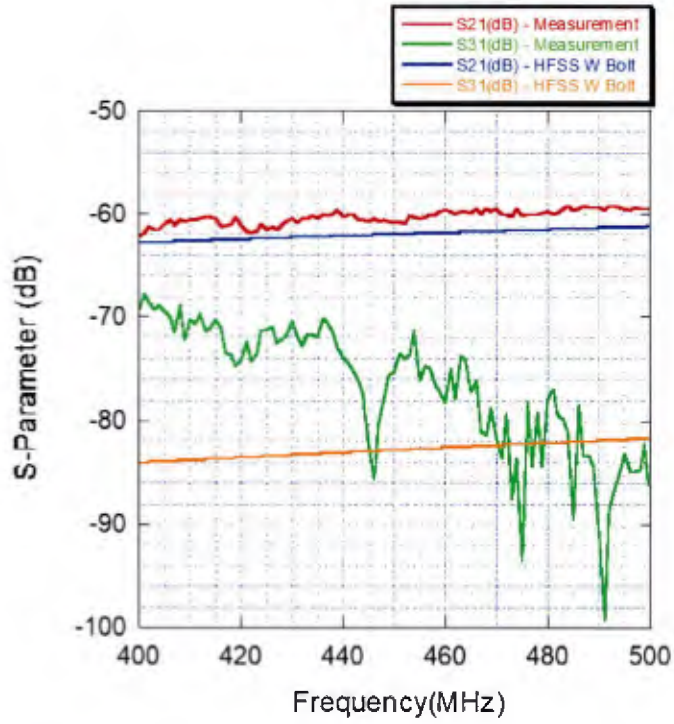


Figure 72. Measured coupling factor and directivity, compared with HFSS simulation results

8.2 Coupled line directional coupler/RF detector

A coupled line coupler was designed in order to sample a small fraction of RF power at the output port of the 8 kW drive amplifier module. A PCB (printed circuit board) is used to patten the microstrip lines. RF coupling takes place by locating two microstrip lines in close proximity. There are two important factors to take into account when designing the coupler. One is the directivity of the coupler. The directivity is a measure of how good the forward and backward waves are isolated. The directivity has to be more than at least 30 dB. The other issue is to design the coupler not to exceed the air-dielectric breakdown limit (30 kV/cm).

ADS and HFSS simulation tools were utilized to design the coupler. A relatively thick board (AD250: dielectric thickness = 0.8 mm, dielectric constant = 2.5, loss tangent = 0.0016) was selected. A coupling factor is set at 60 dB. If a 10 kW RF signal travels in the main microstrip line, a coupled RF power would be 10 dBm, which is low enough for a RF detector's diode. Figure 73 shows the HFSS model of coupled line directional coupler. We designed three coupled lines: (1) 60 dB coupler for measuring a forward power, (2) 60 dB coupler connected with RF Schottky diode, and (3) 30 dB coupler for measuring a reflected power. Note that 60 dB coupling is made by using two identical 30 dB coupled lines in series. The first 60 dB coupler is connected to a peak power sensor/meter. The second 60 dB coupler with the Schottky diode generates an analog output voltage, which is proportional to the RF power. Figure 74 shows HFSS simulation results of the 12 ports microstrip line directional coupler. The coupling factor is found to be 54.35 dB at 467 MHz. The total directivity is 20+24 dB = 44 dB. HFSS predicts the highest field stress of 13 kV/cm near the gap between the main line and coupled line when the input power was assumed to be 10 kW. This is lower than the air-breakdown threshold (30 kV/cm).

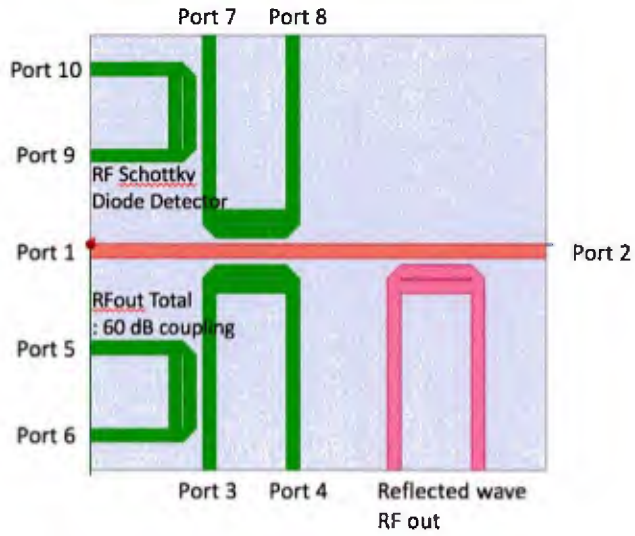


Figure 73. HFSS model of coupled line directional coupler

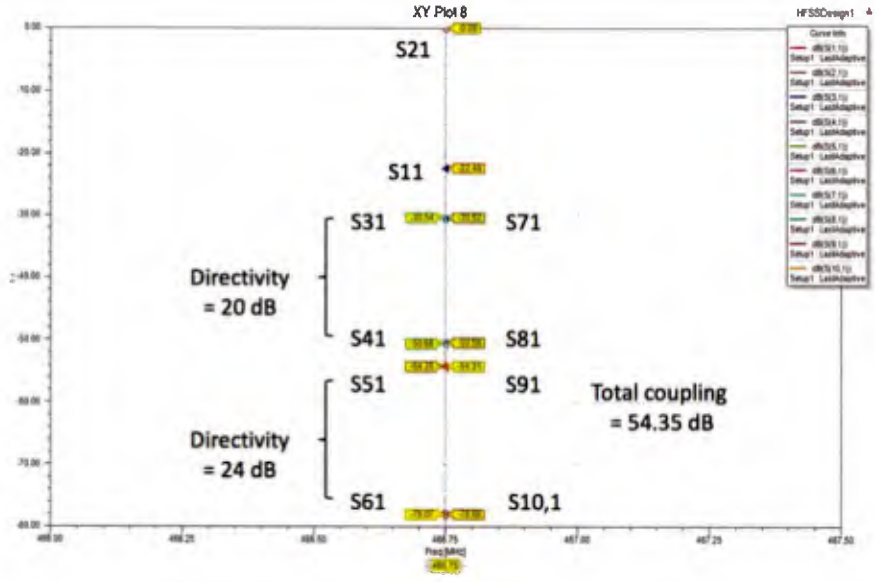


Figure 74. HFSS simulation results of coupled line directional coupler

A coupled line directional coupler was fabricated on the AD250 PCB. A photo of the fabricated coupler is shown in Figure 75. The coupling factor measured by using a calibrated VNA is - 70 dB. The measured directivity is 15 dB + 15 dB = 30 dB. Compared with simulated results of 44 dB, the measured directivity is 14 dB worse. However, this 30 dB directivity is high enough to make the forward and backward signals apart. Figure 76 shows the power measured at port 5 (using the coupling factor of - 70 dB) versus the RF power directly measured by a commercial high power attenuator (Weinschel 82-30-34: 30 dB, 1kW average, 10 kW peak) and Agilent's power sensor/meter (E9325A /E4417A). As shown in Figure 76, the power measured from the directional coupler is in good agreement with the directly measured RF power. This indicates that the coupling factor of the coupled line coupler is -70 dB, being consistent with the previous measurement using the calibrated VNA.

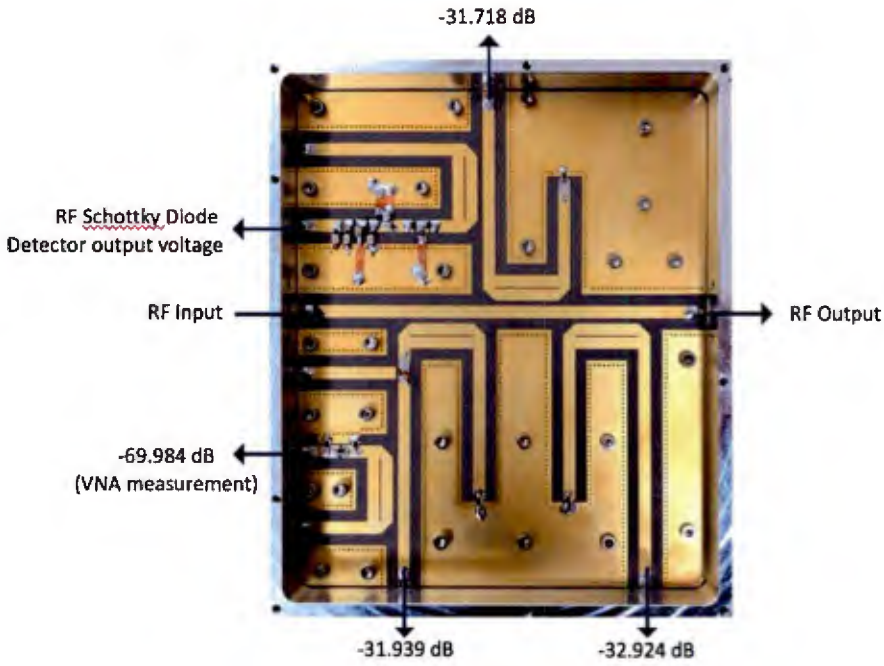


Figure 75. Photo of the fabricated coupler

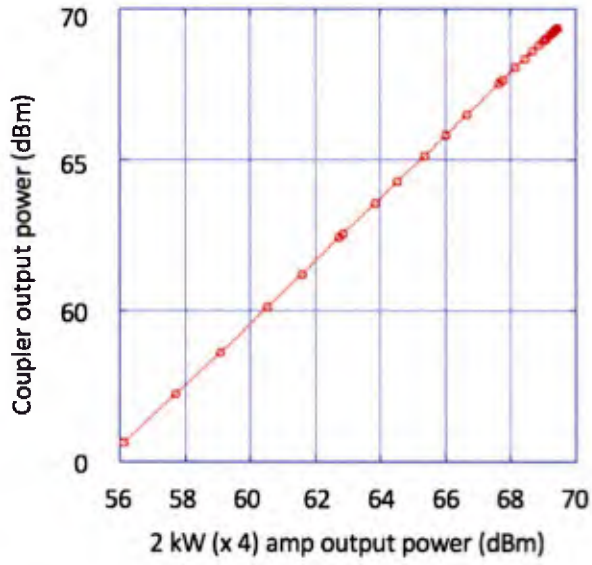
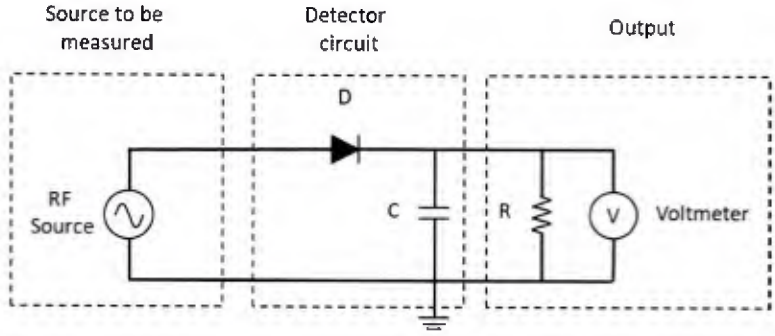
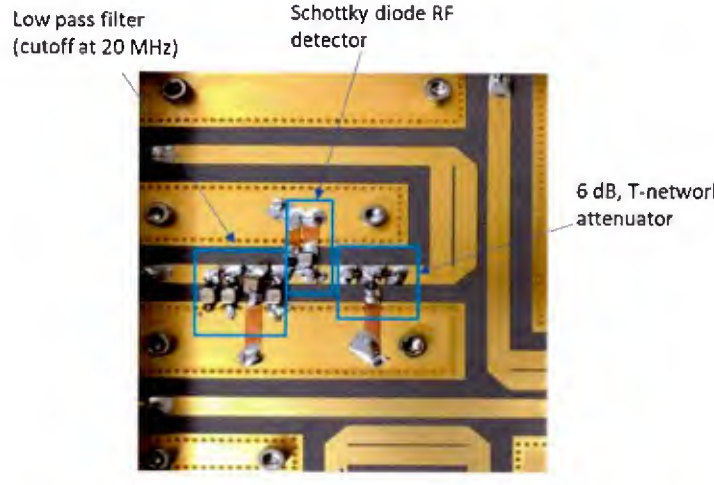


Figure 76. Power measured at port 5 where the horizontal axis stands for the RF power directly measured by high power attenuator and power sensor/meter

The RF detector circuit is shown in Figure 77. As shown in Figure 77, 6 dB T-equivalent matched attenuator is placed directly before the Schottky diode (Infineon BAT63-02V) in order to reduce the sampled power and protect the sensitive diode. Since the diode is a non-linear device, spurious harmonic frequency components are produced. A low-pass filter with a cutoff frequency of 20 MHz was designed and inserted right after the Schottky diode in order to filter all the unwanted AC noises out. Figure 78 shows the DC voltage response from the Schottky diode. As shown in Figure 78, a square-law region is seen in the low RF power and gradually rolls off and reaches a linear region, as expected from a typical diode characteristic curve. The square-law region is the region where we would like to operate the Schottky diode in experiments.



(a)



(b)

Figure 77. (a) Schottky diode's circuit, (b) RF detector circuit using the Schottky diode

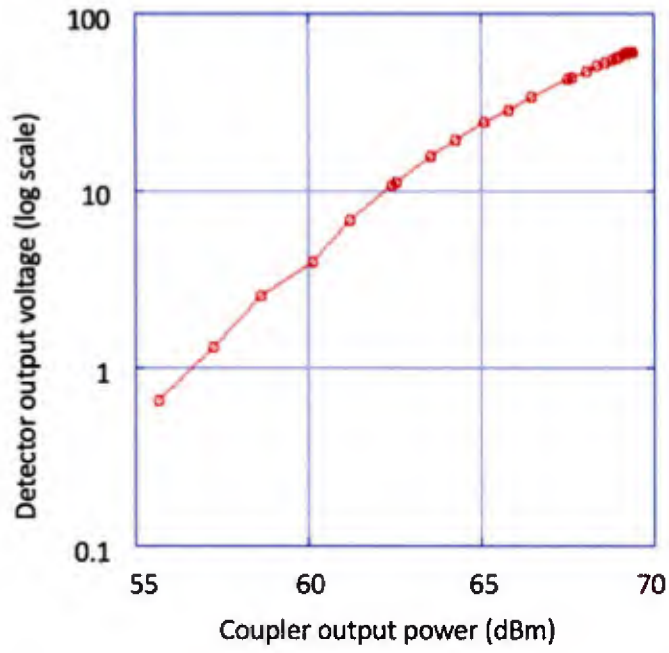


Figure 78. DC voltage response from the Schottky diode

8.3 RF switch

The RF power combiner was designed to operate with a variable duty cycle. The duty cycle is defined as product of 'pulse width' (PW) and 'pulse repetition rate' (PRF). There are two ways of changing duty cycle: (1) changing PW and (2) changing PRF.

A RF switch is required in order to control and vary the PW and PRF. Instead of using a mechanical switch, we chose a digitally controlled SPDT (Single-Pole Double-Throw) switch. Since the rise-time and fall-time of RF pulse are dominated by the RF switch characteristics, the switch should be selected carefully. The electrical properties of the SPDT non-reflective switch chip (Hittite HMC284MS8G) are summarized in Table 14. It has high isolation (> 45 dB) and low insertion loss (0.5 ~ 1 dB) usable from DC to 3.5 GHz.

Table 14. Summary of the Hittite HMC284MS8G electrical properties

Parameter	Specifications
Frequency	DC – 3.5 GHz
Isolation	> 45 dB
Return loss	25 dB (ON-state), 13 dB (OFF-state)
Switching speed	40 nsec
Control voltage	5 V

Figure 79 shows the fabricated RF switch. The switch requires two logic control signals (High and Low) in order to switch the input RF to RF output path 1 or RF output path 2. A dual inverter chip (Texas Instrument SN74LVC2G04DCKR) was used to provide the two logic control signals. As shown in Figure 80, a primary pulse signal (with a predefined PW and PRF at a computer-controlled Digilent's Discovery2 AD convertor) is applied to PIN 1. The same pulse as the primary pulse appears on PIN 4 whereas an inverted pulse appears on PIN 6 as shown in Figure 80.

Figure 81 shows a RF pulse waveform measured from a digital oscilloscope. The RF envelop signal was obtained by using a Krystal's RF detector (D101). Both 0.5 % and 10 % duty cycle were tested. As shown in Figure 81, a CW 467 MHz RF signal converts into a pulse waveform (PW = 1 milliseconds, PRF = 100 Hz) when it passes through the RF switch. The pulse with and PRF were measured to be the same as the primary pulse generated from the computer- controlled AD converter as expected. Pulse rise-time was measured to be 27.2 nsec.

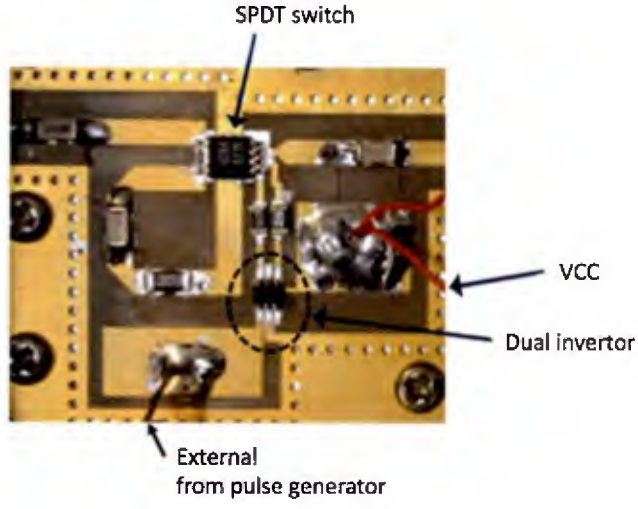


Figure 79. SPDT switch with a dual inverter

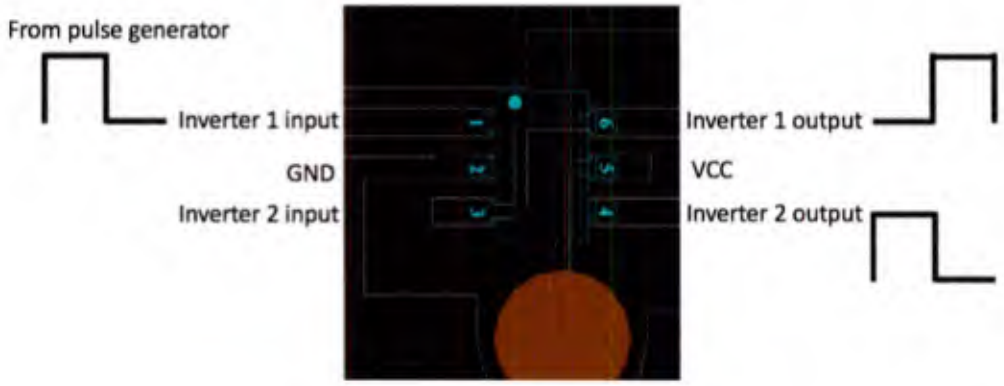


Figure 80. Operation of a dual invertor circuit

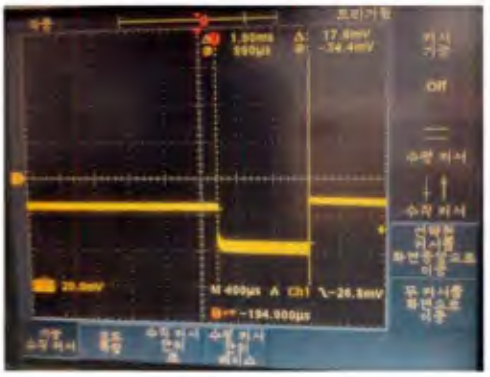


Figure 81. RF pulse envelop measured from a digital oscilloscope (PW = 1 milliseconds, PRF = 100 Hz)

8.4 Digital attenuator

A 5-bit digital attenuator was used in order to make the RF output power variable. The attenuator was directly placed right after a stable phase-locked CW RF source (Analog Devices ADF4355-2BCPZ). The attenuator chip (Hittite HMC539LP3) is a switched line attenuator. It has 5 SPDT switched lines in the chip so that each switched line can have 0.25 dB, 0.5 dB, 1 dB, 2 dB, and 4 dB attenuation. Figure 82 shows a CAD drawing of the 5 bit digital attenuator along with the aforementioned RF switch. Attenuation value is adjusted by 5 TTL logic signals (V1, V2, V3, V4, V5), externally controlled by the computer-controlled Digilent's AD convertor. The voltage of the 5 logic signals is all 3.25 V.

Figure 83 shows the packaged module including both the digital attenuator and RF switch. Using a calibrated VNA, attenuation values as functions of RF frequencies (20 MHz to 3 GHz) for various logic signal settings were measured. As shown in Figure 84, the range of attenuation is about 7 dB. The detailed attenuation values at 467 MHz which is the frequency we are interested in are plotted in Figure 85. As seen in Figure 85, the attenuation varies from 0.93 dB to a maximum 8.96 dB, depending the 5 logic signals.

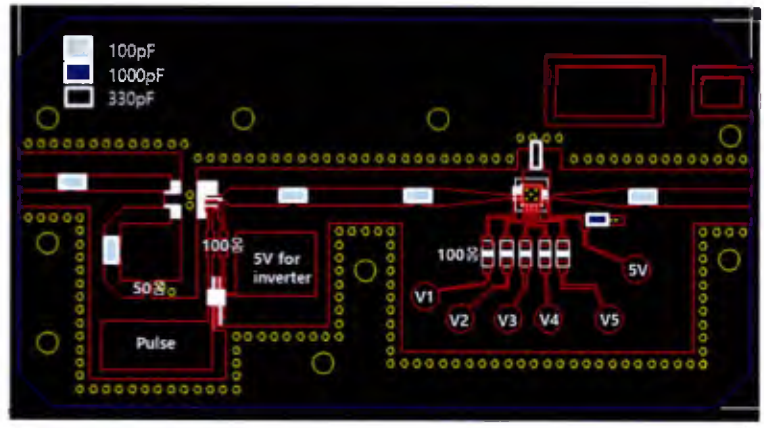


Figure 82. CAD drawing of the 5-bit digital attenuator along with the RF switch

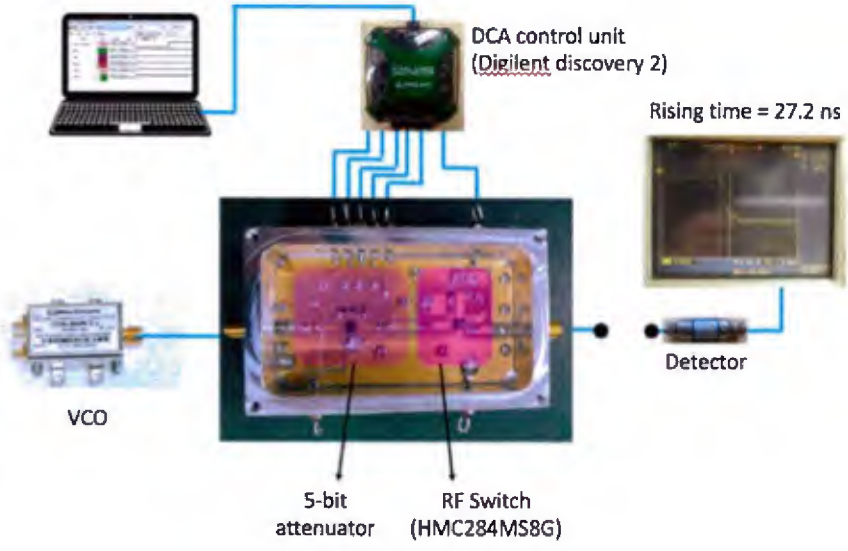


Figure 83. Packaged module including both digital attenuator and RF switch

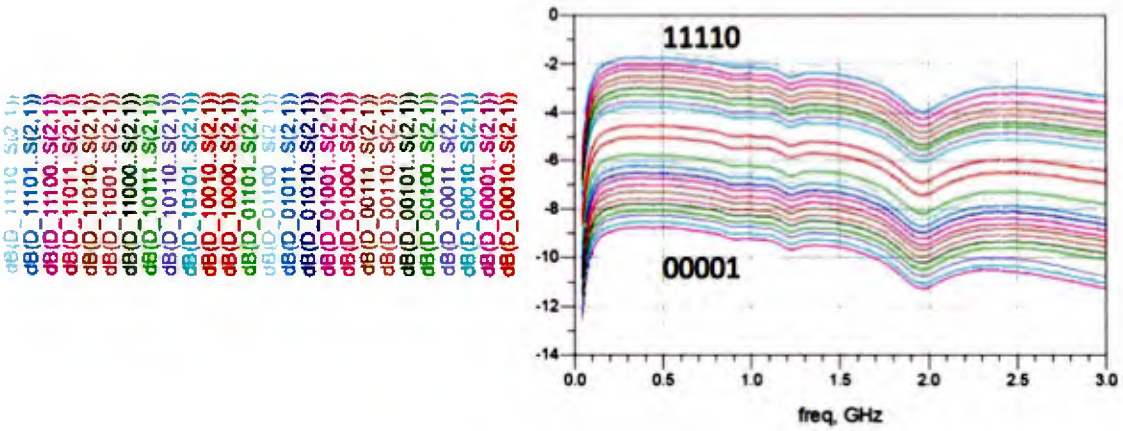


Figure 84. Attenuation values as functions of RF frequencies (20 MHz to 3 GHz) for various logic signal settings

D	E	F
logic(12345)	power(dBm)	ATT(dB)
00000	1.24	8.96
00001	1.53	8.67
00010	1.76	8.44
00011	2.05	8.15
00100	2.26	7.94
00101	2.56	7.64
00110	2.79	7.41
00111	3.1	7.1
01000	3.24	6.96
01001	3.53	6.67
01010	3.76	6.44
01011	4.06	6.14
01100	4.27	5.93
01101	4.57	5.63
01110	4.81	5.39
01111	5.12	5.08
10000	5.24	4.96
10001	5.55	4.65
10010	5.78	4.42
10011	6.09	4.11
10100	6.3	3.9
10101	6.61	3.59
10110	6.84	3.36
10111	7.16	3.04
11000	7.29	2.91
11001	7.61	2.59
11010	7.84	2.36
11011	8.16	2.04
11100	8.39	1.81
11101	8.71	1.49
11110	8.95	1.25
11111	9.27	0.93

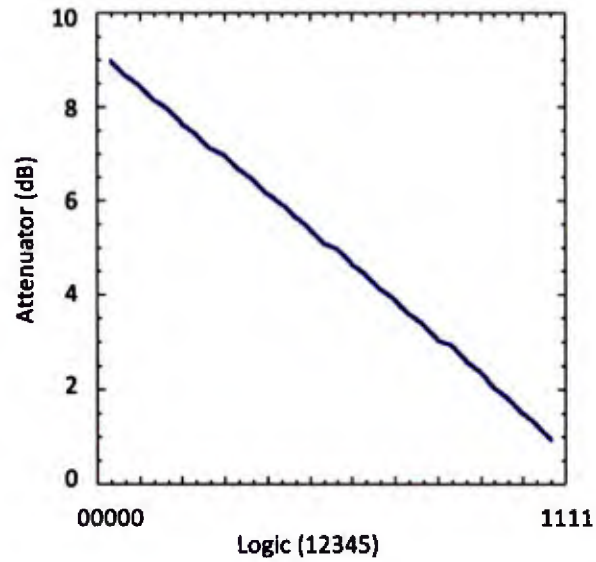


Figure 85. Detailed attenuation values at 467 MHz for 5 bit digital logic signals

Chapter 9. Drive amplifier

As mentioned earlier in power budget of the power combiner system in Chapter 2, we need a multi-stage gain amplifier to drive eighty 2 kW SSPA modules. The drive amplifier is composed of (1) 1 W high gain SSPA, (2) 200 W SSPA, (3) 2 kW SSPA module, and (4) 8 kW SSPA drive amplifier. The 2 kW SSPA module which we developed for the 80-way cavity power combiner was used here for a drive amplifier.

9.1 1 W SSPA

The phase-locked signal power generated from Analog Devices PLL is 8.8 dBm. A Mini-circuit 1 W SSPA (ZHL-1A-S+) is used as a first stage drive amplifier. Figure 86 shows a photo of the 1 W SSPA. Table 15 summarizes the amplifier characteristics provided by Mini-Circuit Inc. Two 1 W SSPAs are connected in series to get an output power of 1 W. Figure 87 shows a measured drive curve, or a plot of output power versus input power for one amplifier and two cascaded amplifiers. Since the signal level of the phase-locked signal source is less than 15 dBm, one SSPA is not enough to produce 1 W output power. Two 1 W SSPAs were connected in series to get total gain of 32 dB (= 16 dB x 2).

Figure 86. Photo of Mini-circuit's 1 W SSPA

Table 15. RF characteristics of Mini-Circuit's SSPA (ZHL-1A-S+) provided by Mini-Circuit Inc.

Parameter	Specifications
Frequency (MHz)	2 ~ 500
Gain (dB)	16 ±1.0
Maximum power output (dBm)	28 (1 dB Compr.)
IP3 (dBm)	38

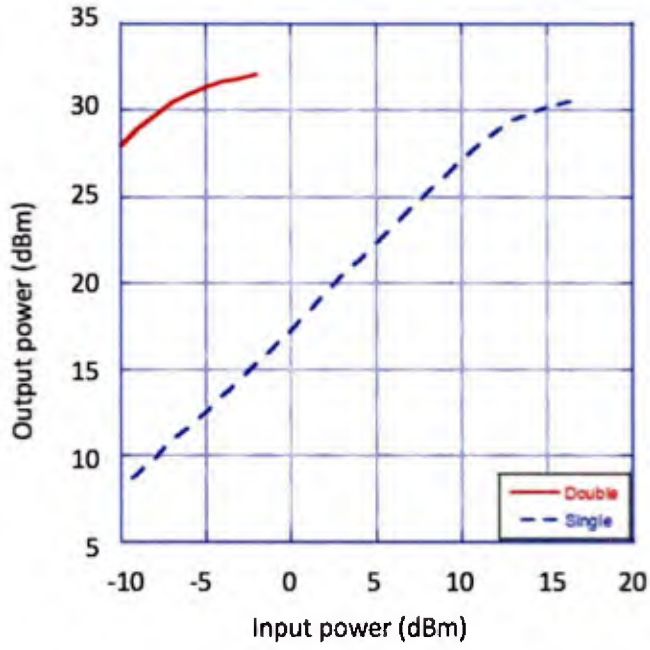


Figure 87. Plot of measured output power versus input power for one amplifier and two cascaded amplifiers (input power denotes the Hittite's signal power.)

9.2 200 W drive amplifier

The second drive amplifier for producing 200 W output power is constructed. Two 100 W LDMOS transistors (NXP MRFE6VP100H) are combined to produce a 200 W RF power. Table 16 shows a list of electrical parameters of the 100 W LDMOS FET. NXP provides the circuit layout of the 100 W LDMOS FET as a reference circuit. Figure 88 shows the fabricated 200 W SSPA. The transistor was directly soldered on a copper carrier where a cooling water runs through a drilled hole. The power divider at the input port is a conventional 3-dB Wilkinson power divider. Power combining of the two 100 W signals was done through the 3-dB Wilkinson power divider. Both input and output connectors are the Type-N connector. A circulator is placed at output

end of the 100 W SSPA before the Wilkinson power combiner, in order to protect transistors from unwanted reflected power. Figure 89 shows a drive curve (output power versus input power) for 460 MHz, 470 MHz, and 480 MHz. As shown in Figure 89, output power was measured to be more than 200 W for all frequencies when 1 W input power was injected.

Table 16. Electrical parameters of the 100 W LDMOS FET (MRFE6VP100H)

Parameter	Specifications
Frequency	1.8 ~ 2000 MHz
Output power	100 W (typical)
Power gain	25 ~ 27 dB
Drain efficiency	70 % tTypical)
Drain-Source Breakdown voltage	141 V
Gate Quiescent Voltage	2.1 ~ 3.1 V

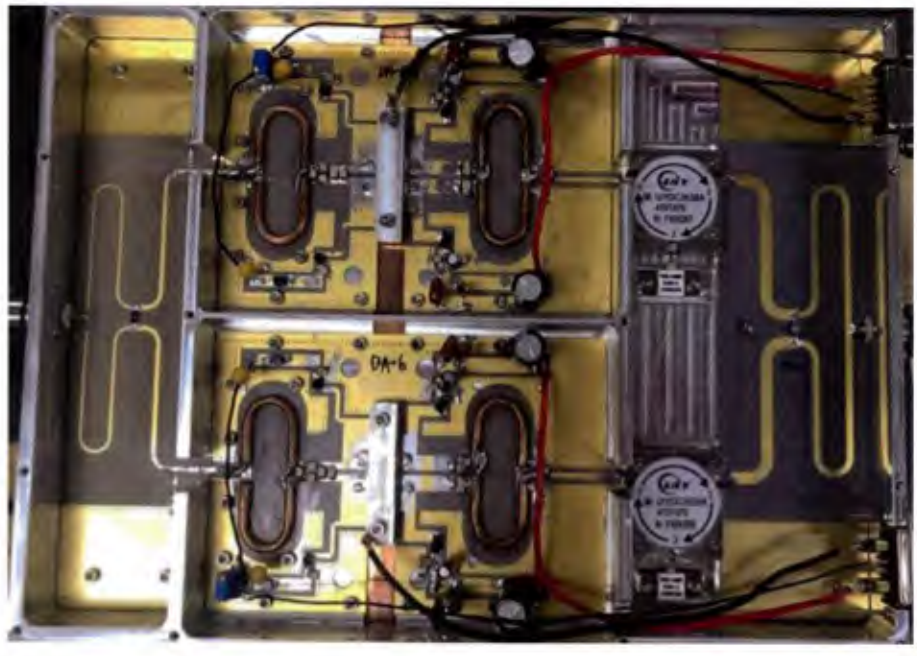


Figure 88. Photo of the fabricated 200 W SSPA

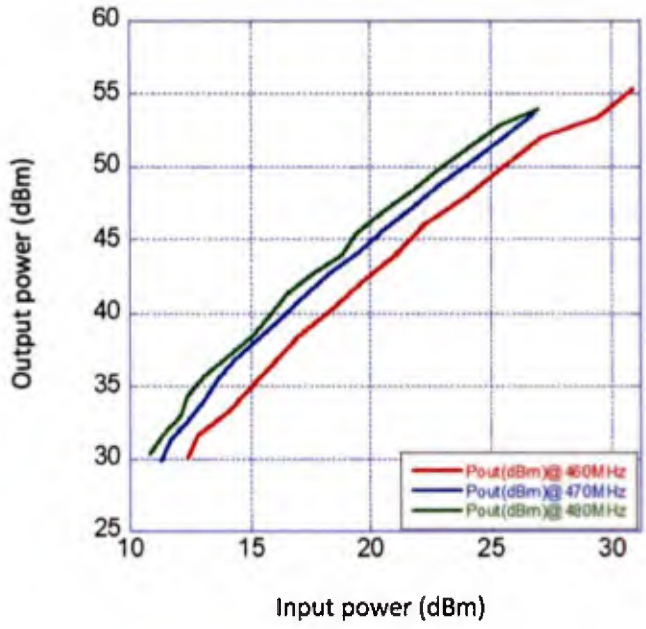
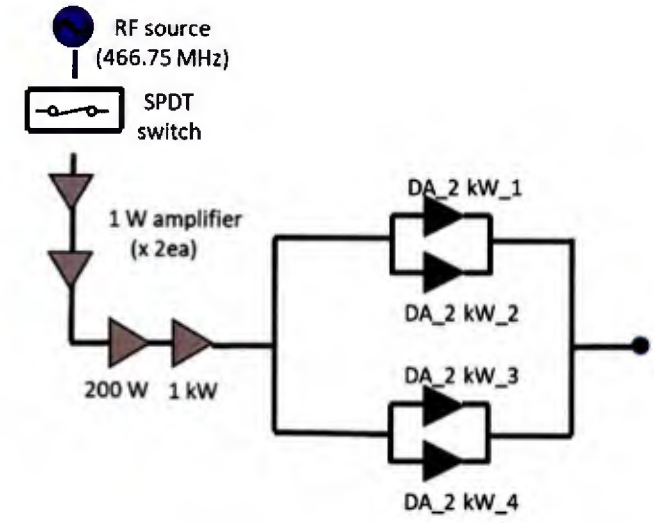


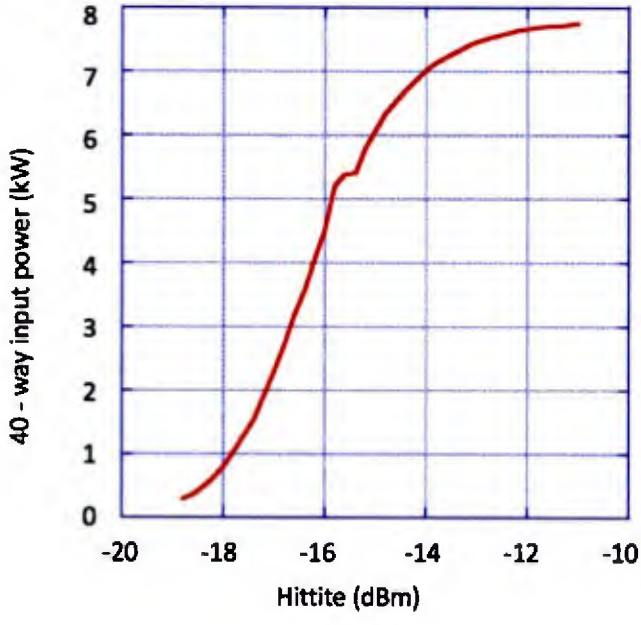
Figure 89. Drive curve (output power versus input power) of the 200 W SSPA for 460 MHz, 470 MHz, and 480 MHz

9.3 8 kW SSPA drive amplifier

The 200 W drive amplifier drives a 2 kW SSPA module (which is the same SSPA module as the amplifier used for the 80-way power combiner (described in Chapter 4)). The output power of the 2 kW SSPA module is injected to 8 kW SSPA drive amplifier. The 8 kW drive amplifier consists of four 2 kW SSPA modules. A schematic layout of the 8 kW drive amplifier is shown in Figure 2. As shown in Figure 2, two modules are combined to get 4 kW output power through the first Gysel combiner and then the two 4 kW signals are again combined in the second Gysel combiner to get a total 8 kW RF output power. Figure 90 shows (a) experimental layout and (b) RF output power as a function of input power. As seen in Figure 90, we need to operate the 2 kW SSPA modules near a saturation region to get full power of 8 kW. As will be explained later in Chapter 11, a drive power of more than 8 kW would be necessary if one wants to produce 200 kW output power from the 80-way power combiner system operating at high duty cycle (> 10 %). For the case of low duty operation, the 8 kW drive power is enough to saturate the combiner system because the 2 kW SSPA modules have high gain more than 16 dB at low duty cycle.



(a)



(b)

Figure 90. (a) Experimental layout, (b) RF output power of 8 kW SSPA drive amplifier as a function of input power

Chapter 10. Experiments on 40-way power combiner

10.1 Experimental layout

Prior to the full test of 80-way power combiner system, we configured a 40-way power combiner to investigate the cavity combiner performance. Figure 91 shows the experimental layout with a power budget. As seen in Figure 91, the 40-way power combiner system consists of (1) 4 stage high gain drive amplifiers, (2) a low-loss 40-way power divider, (3) forty 2 kW LDMOS RF power amplifier modules, (4) a cavity power combiner, (5) directional coupler, and (6) high power dummy load. Figure 92 shows a CAD of the 40-way power combiner system.

An RF source (Hittite) of - 11 dBm at 464 MHz (Hittite signal source) is injected to two high-gain 1 W drive amplifiers, which are in connection with a 200 W drive amplifier. The 200 W SSPA drives 4 kW SSPA (2 x 2 kW SSPA modules). The 4 kW output power generated from the high-power drive amplifier is splitted into the 40 output ports through the equal amplitude/phase 40-way power divider. The key point in this power divider is to keep equal amplitude and equal phase on all of the 40 output ports. Each output power is injected into two push-pull LDMOS power transistors producing an output power of 2 kW. The 40 SSPA modules (2 kW output power per module) are mounted on the cylindrical cavity sidewall in order to combine RF power in the cavity. The combined power is extracted through a 6-1/8" coaxial transmission line, which is terminated with a water-cooled high power dummy load. The RF dummy load used in the 40-way power combiner experiments is Bird's coaxial RF load as shown in Figure 93. The returnn loss of the the Bird dummy load is – 20 dB at 464 MHz. An accurate RF power is measured through a calibrated 60 dB directional coupler (Dielectric Inc.) as shown in Figure 94. The both forward and reflected coupling factor is 60.4 dB. Note that the 60 dB coupler and RF water load which we designed and fabricated (described in Chapter 7 and 8) was used only for 80-way power combiner experiement discussed later in Chapter 11. The attenuation setting is 60.4 dB (directional coupler) + adpator loss (0.1 dB) + cable loss (0.7 dB) + fixed attenuator (39.6 dB), which gives a total attenuation 101 dB. The attenuated RF signal is injected to Agilent peak power sensor/meter to measure RF power in 6-1/8" coaxial transmission line. RF pulse width and PRF (or duty cycle) are adjusted by using a SPDT switch, controlled by an external pulse generator.

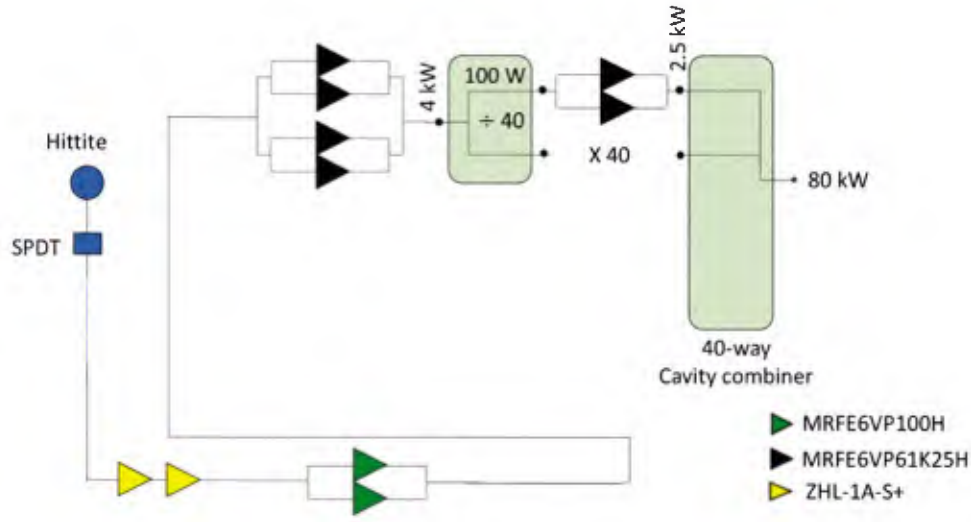


Figure 91. Experimental layout with a power budget for a 40-way power combiner experiments

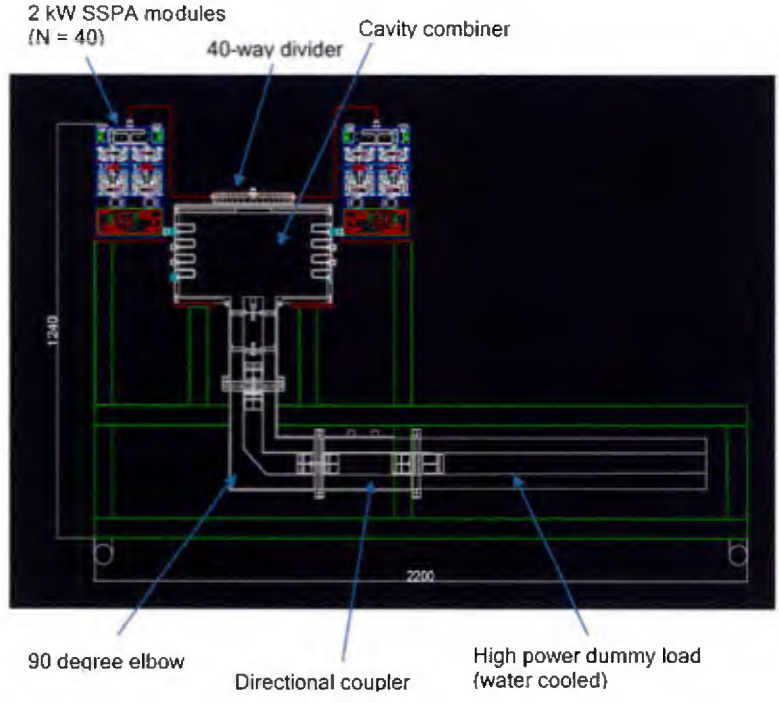


Figure 92. CAD drawing for a 40-way power combiner system

Figure 93. RF dummy load used in the 40-way power combiner (Bird Inc.)

Figure 94. 60 dB coupler (Dielectric Inc.)

10.2 Experimental results

First experiments

Based on the previous work of the 2 kW LDMOS SSPA module which we have described in Chapter 4, we constructed forty SSPA modules. In order to keep temperature of the LDMOS FET low enough below 170 degree C, the LDMOS transistors are solded directly on the copper plate. The copper plate has a water channel just beneath the FET so that the heat generated by the FET is effectvely removed. Figure 95 shows a photo of a typical 2 kW SSPA module including a Wilkinson divider, RF input/output matching circuits, and Gysel power combiner. As shown in Chapter 3, the experimental result of 1 kW SSPA showed an output power of more than 1 kW with drain efficiency of 60 %. Using the 3 dB Gysel binary power combiner, we combined two 1 kW SSPAs to get an output power of 2 kW. Note that high power circulators (manufactured by UIY Inc.) were placed at each end of the two 1 kW SSPAs in order to protect transistors from unwanted reflected rf power and isolate signals from each other.

Figure 96 shows the experimental setup for testing each of the 40 SSPA modules. Figure 97 shows individually tested output powers of the forty SSPA modules for three input powers; 50 W, 75 W, and 100 W. As shown in Figure 97, there are some power variations from 2 kW to 2.7 kW. It should be noted that we tuned input and output matching circuits for maxmium power rather than maximum efficiency, as described in details earlier in Chapter 3. All the following experiments on the 40-way combiner were performed in a duty cycle of 0.5 % (PRF = 50 Hz, PW = 100 microseconds) unless otherwise stated. The output power increases with better flatness in power as the input power increases to 100 W. This is because all SSPA modules approach a saturated power when they are overdriven.

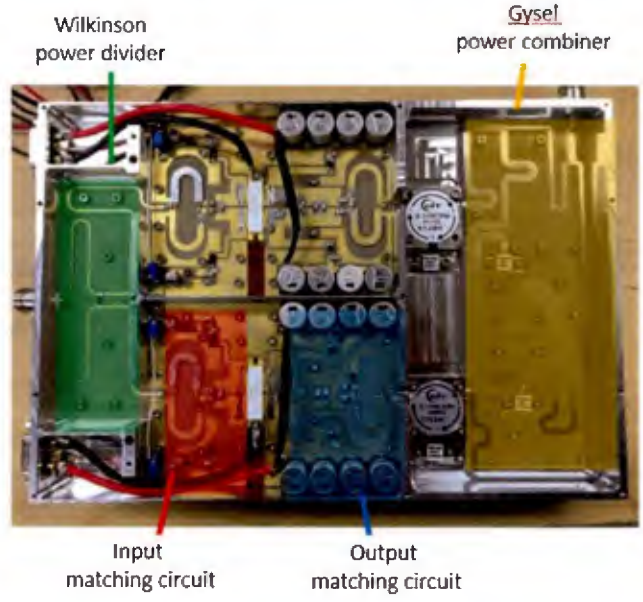


Figure 95. Photo of a typical 2 kW SSPA module

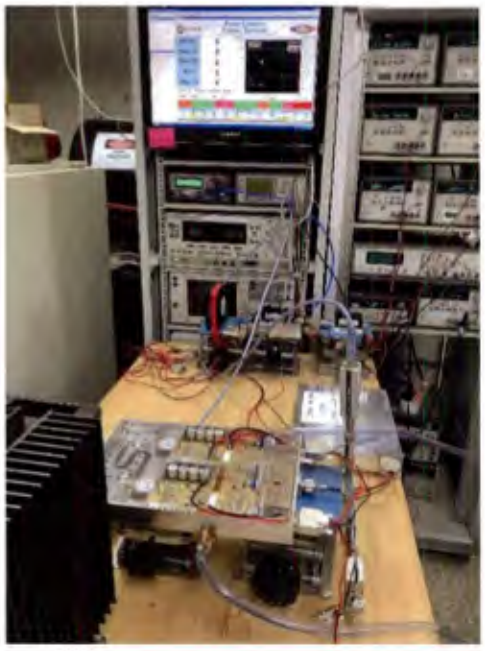


Figure 96. Experimental setup for measuring Individually tested output powers of 2 kW SSPA modules

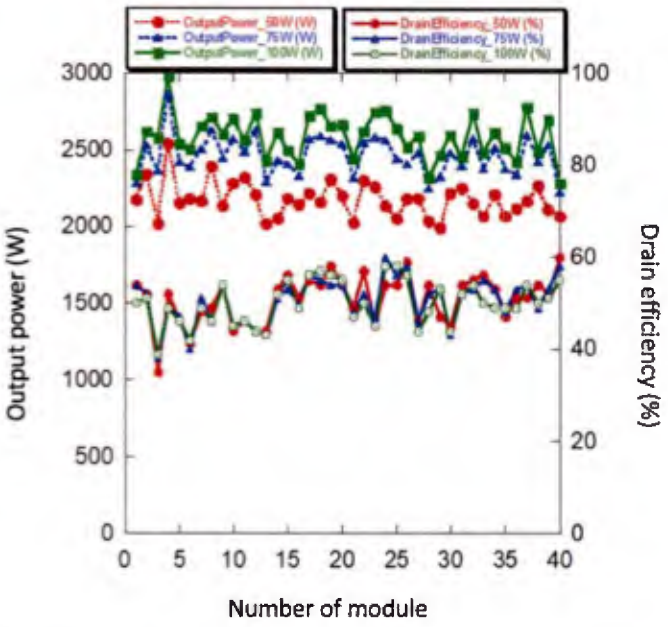


Figure 97. Individually tested output powers of the forty SSPA modules

As described in Chapter 5, the center conductor of the 6-1/8" coaxial transmission (RF output extraction port) has to be accurately positioned in order to meet a critical condition of the cavity. The coupling coefficient for critical coupling is obtained by adjusting an external coupling value (or, an external Q of the cavity). We have adjusted the position of the center conductor of the 6-1/8" coaxial transmission line for maximum coupling for the case of 40 loop antennas installed in the cavity. As shown earlier in Chapte 4, the measured return loss was -30 dB at 464 MHz, indiciating that the cavity is near a critical coupling condidtion. Figure 98 shows the in-situ measurement of the RF output power of individual SSPA module where all other SSPA modules were mounted on the cavity combiner. It should be noted that the RF power was somewhat lower than the earlier measurement shown in Figure 97. The reason was found to be due to non-perfect isolation between the SSPA modules. In other words, a small amount RF power reflected from the input end of the SSPA module is coupled through the 40-way divider, resulting in affecting the input impedance of the nearby SSPA modules. In order to eliminate the problem, we had to add additional isolators on every input channel of the all SSPA modules. As described in the following section, UIY 300 W isolators were placed on each of the SSPA entrance in the second experiment.

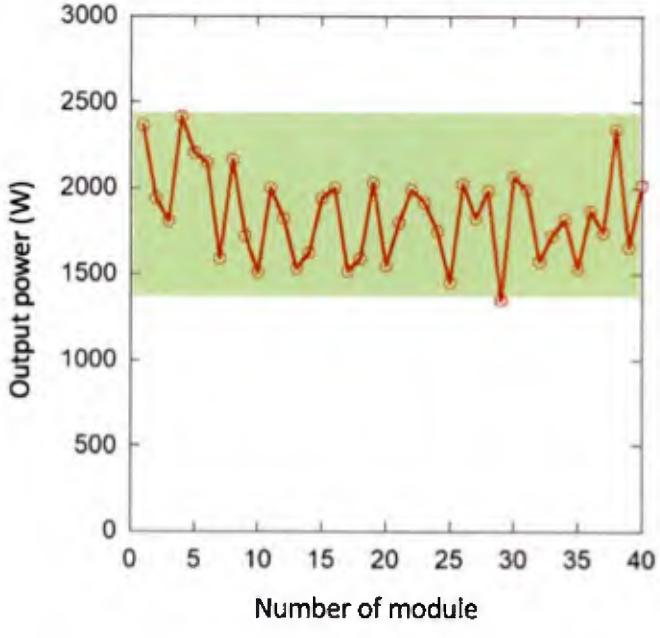


Figure 98. In-situ measurement of the RF output power of individual SSPA module (where all other SSPA modules were mounted on the cavity combiner)

After careful testing of the all 40 SSPA modules and installing the 40 loop antennas, we assembed SSPA modules on the TM_{010} cylidrical cavity combiner. Figure 99 depicts the view of the assembed experimental setup. Experiments of the 40-way power combining system were conducted with forty 2 kW SSPA modules. Figure 100 shows a result of the power combiner test, showing a maximum output power of 80 kW (79 dBm) at 464 MHz where PRF is 50 Hz and pulse length is 100 microseconds (equivalent to duty cycle = 0.5 %). The error bar in the power measurements comes from the signal fluctuation on the 60 dB directional coupler. The actual S-parameter of the directional coupler in Figure 100 should be -60 dB + the value on the Y-axis. This corresponds to a combining efficiency of 97 %. A DC-RF power conversion efficiency of the overall power combiner system was near 50 %. The saturated gain was 81 dB (input RF signal power = - 2 dBm). Such a high combining efficiency was realized by a low ohmic power loss of the cavity and a careful design for a critical coupling condition at RF input and output ports. Input RF source frequency was swept from 461 MHz to 467 MHz to measure instantaneous 3 dB bandwidth. Here, the input RF power was set at a constant value for all input frequencies. The 3 dB bandwidth was measured to be 1.2 %, which was limited by the cavity Q-factor. It should be noted that the bandwidth can be increased if one uses a cavity frequency tuner placed at the cavity wall. It is interesting to see that the frequency response (or, BW) of the power combiner followed very closely the cavity cold-test result of S_{21} (without SSPA) measured by the calibrated VNA.

Figure 99. Photo of the assembed experimental setup of the 40-way power combiner

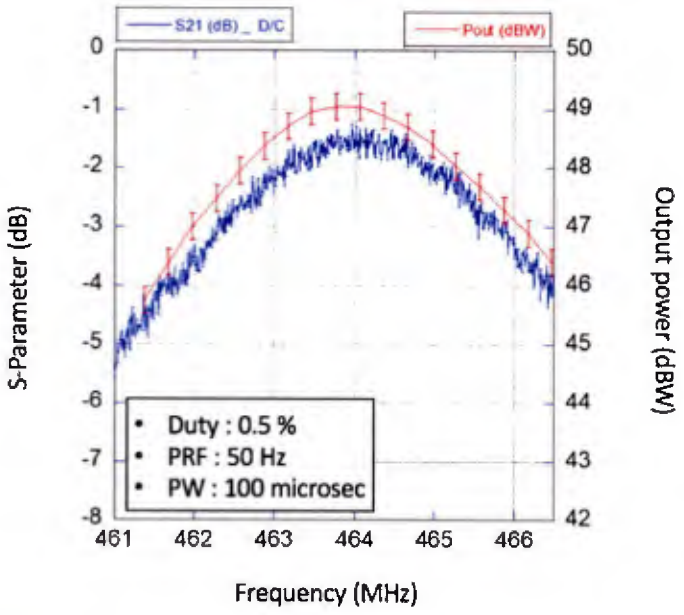


Figure 100. Test result of the power combiner, showing a maximum output power of 80 kW at 464 MHz

Additional experiments were carries out to see the effects of gate bias voltage and drain bias voltage on the RF combined power. All other conditions except bias voltages are the same as before. Figure 101 shows the RF combined power as functions of gate bias voltage. As shown in Figure 101, as the gate bias voltage decreases from 5.1 V to 4.3 V (where drain voltage was set at 50 V), the output power drops from 79 kW to 70 kW. This is somewhat expected from the fact that the conduction angle of the transistor drain-source channel is reduced (approaching Class B, and thus closing the conduction channel). Recall that the original design of the transistor (described in Chapter 3) was to operate at Class AB. The drain bias voltage was raised from 50 V (nominal operating voltage) to 60 V to see how the RF power changed. Figure 102 shows RF combined power as functions of drain bias voltage where the gate bias was set at 5 V. As shown in Figure 102, the RF combined power increased by 10 kW, producing 89 kW. Table 17 summarizes experimental results of the 40-way power combiner.

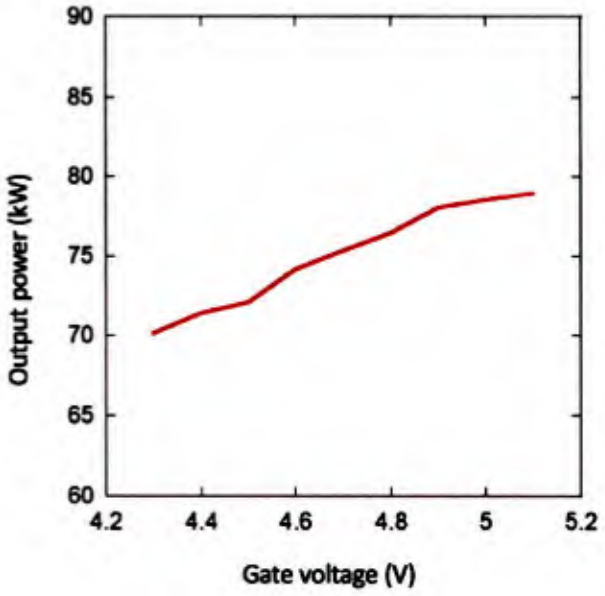


Figure 101. RF combined power as functions of gate bias voltage

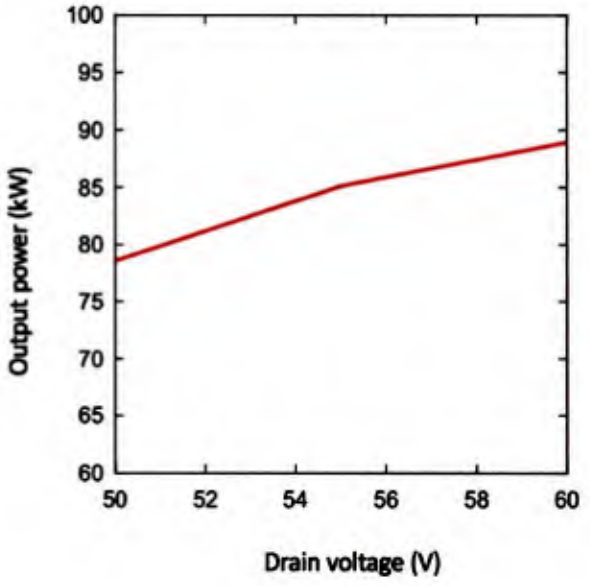


Figure 102. RF combined power as functions of drain bias voltage

Table 17. Experimental results of the 40-way power combiner system

Parameter	Specifications	Remarks
Transistor	NXP 1 kW LDMOS FET (MRFE6VP61K25HR6)	Total number of transistors = 160
Frequency	464 MHz	1.2 % bandwidth
RF output power of 2 kW SSPA module	2.0 ~ 2.6 kW	
Drain efficiency of 2 kW SSPA module	55 ~ 65 %	
Saturated gain of 2 kW SSPA module	15 ~ 16 dB	
Combiner	TM_{010} mode cylindrical cavity	
Combined output power	79 kW (79 dBm) at 50 V (89 kW at drain voltage = 60 V)	
DC – to – RF power conversion efficiency of power combiner system	50 %	
Combining efficiency	> 95 %	
System gain	90 dB	- 4 stage drive amplifiers - Hittite RF source power = -11 dBm
Duty cycle	0.5 % (PRF = 50 Hz, PW = 100 µsec)	Individual SSPA module was tested up to 20 % duty
Operating conditions (nominal)	$V_{DS} = 50$ V $V_{GS} = 2.5$ V	
RF transmission line	6-1/8" coaxial transmission line	Maximum CW power = 80 kW at 1 GHz

Second experiments

We performed second experiments on the 40-way power combiner. In this case, we modified 3 major setups: (1) installtion of UIY isolator (UIY 14550A400T500NF, forward power = 300 W, isolation = 20 dB) to isolate between 2 kW SSPA modules, (2) tuning impedances on input and output impedance matching circuits, and (3) using the in-house designed RF water load and directional coupler (described in Chapter 7 and 8). We also changed the configuration o fdrive amplifiers as follows: Hittite (- 11 dBm), 1 W SSPA, 1 W SSPA, 200 W SSPA, 2 KW SSPA, 8 KW SSPA.

We have tuned the input and output impedances of the SSPA modules for higher power and efficiency and less fluctuation in power among the 40 SSPA modules. In-situ measurements on the 40 SSPA modules were carried, in which case all other 39 modules were mounted on the cavity power combiner while one module was tested. Figure 103 shows the output power versus individual SSPA module. As shown in Figure 103, the output power ranges from 2.2 kW to 2.7 kW. The summed power of all 40 SSPAs output power was 100.6 kW. Note that the summed power (100.6 kW) is higher than the power in the first experimental setup.

Figure 104 shows the photo of the second experimental setup of the 40-way power combiner. A drive curve is shown in Figure 105. Operating conditions are drain voltage = 50 V, PRF = 50 Hz, PW = 100 micsroseconds. The combined output power reaches 95 kW (+- 4 kW) at input drive power of 3.8 kW at 464 MHz. The combining efficiency was found to be 95 kW/100.6 kW = 95 % where the summed power of all 40 individually measured powers is 100.6 kW. The measured combining efficiency (95 %) is consistent with the that (97 %) obtained in cold-test measurement with the cavity combiner by itself described in Chapter 4. HFSS field calculator was used to predict a combined power. It predicts 100.6 kW, which is nearly the same as the individually summed power. This indicates that the cavity power combiner combines RF power efficiently regardless the little imbalance in both power and phase. The total gain of the combiner system was 91 dB. The DC-RF conversion efficiency was measured to be ~ 50 %.

Input drive frequency was swept to measure the 3-dB bandwidth. Figure 106 shows the output power vesus drive frequency. As shown in Figure 106, the 3-dB bandwidth was measured to be 461.3 MHz ~ 467 MHz (1.2 %). The measured freqeuncy response is in good agreement with HFSS simulated results. Table 18 summarizes the experimental results of the 40-way power combiner.

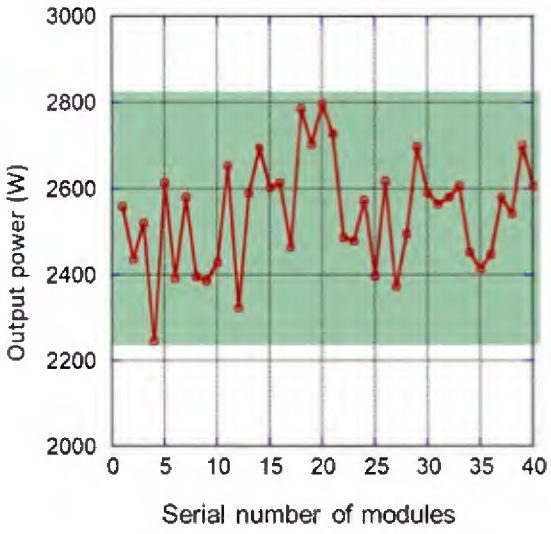


Figure 103. In-situ measurement of the SSPA modules after tuning both input and output impedances of the matching circuits for higher output power

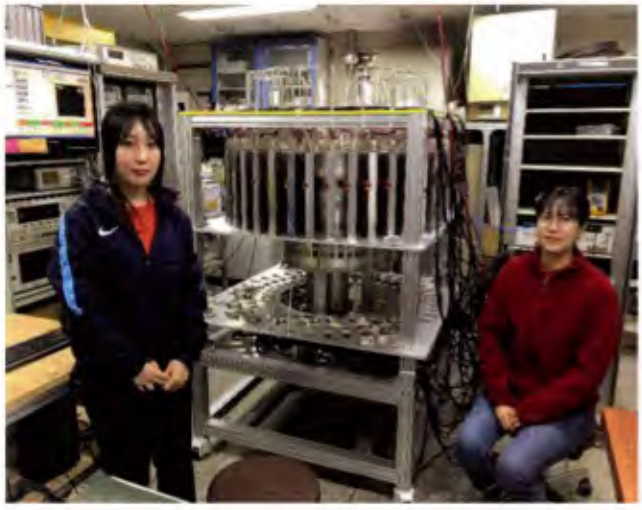


Figure 104. Photo of the second experimental setup of the 40-way power combiner

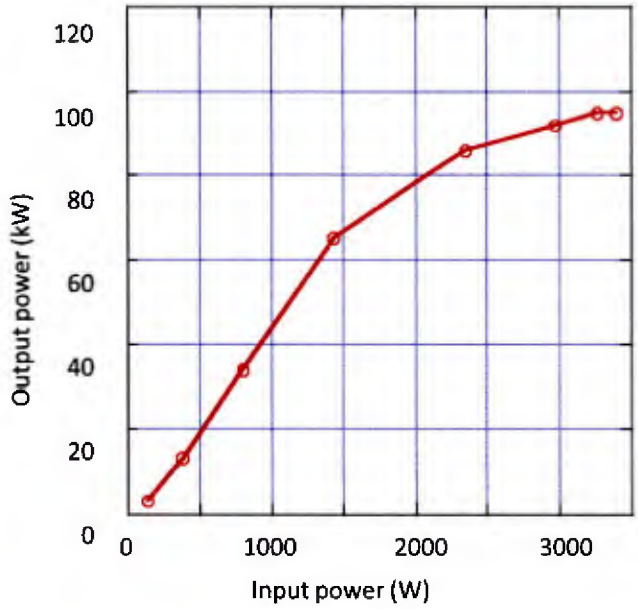


Figure 105. Drive curve (frequency = 464 MHz)

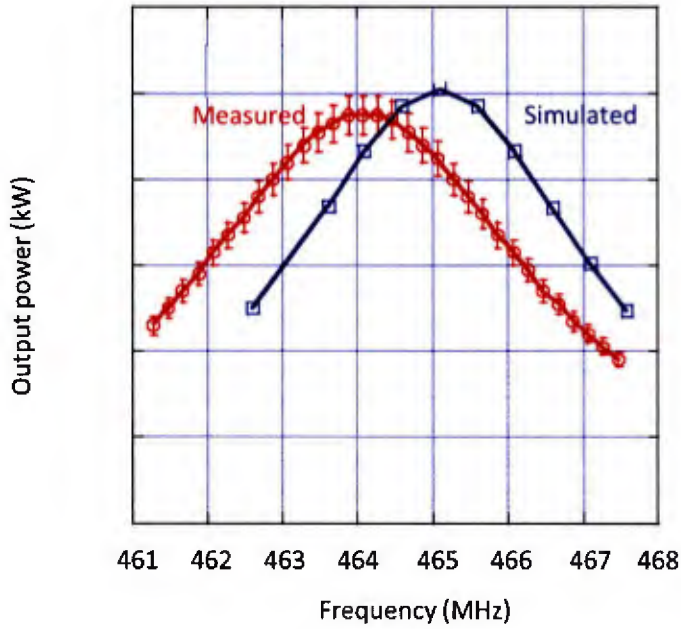


Figure 106. Output power versus RF frequency

Table 18. Summary of the experimental results of the 40-way power combiner

Parameter	Measured result
RF output power	95 kW (± 4 kW)
3 dB bandwidth	461.3 MHz ~ 467 MHz (1.2 %)
Total gain	91 dB (with 4 drive stages)
DC to RF conversion	> 50 %
Combining efficiency	~ 95 %
Operating condition	PRF = 50 Hz, PW = 100 μsec

Chapter 11. Experiments on 80-way power combiner

11.1 Experimental layout

As a continuing effort on achieving even higher combined power, we have designed, fabricated and carried out extensive experimental investigation on an 80-way power combiner.

Differently from the 40-way power combiner experiments described in Chapter 10, the 80-way power combiner will need more input power for the eighty 2 kW SSPA modules (40 SSPA modules were added in this experiment. Two additional drive amplifiers (two 2 kW SSPA modules) was fabricated. The total output power from the drive amplifier is now 8 kW. Detailed description on 8 kW drive amplifier is in Section 9.3. Figure 107 shows a layout for power budget of the 80-way power combiner experiments.

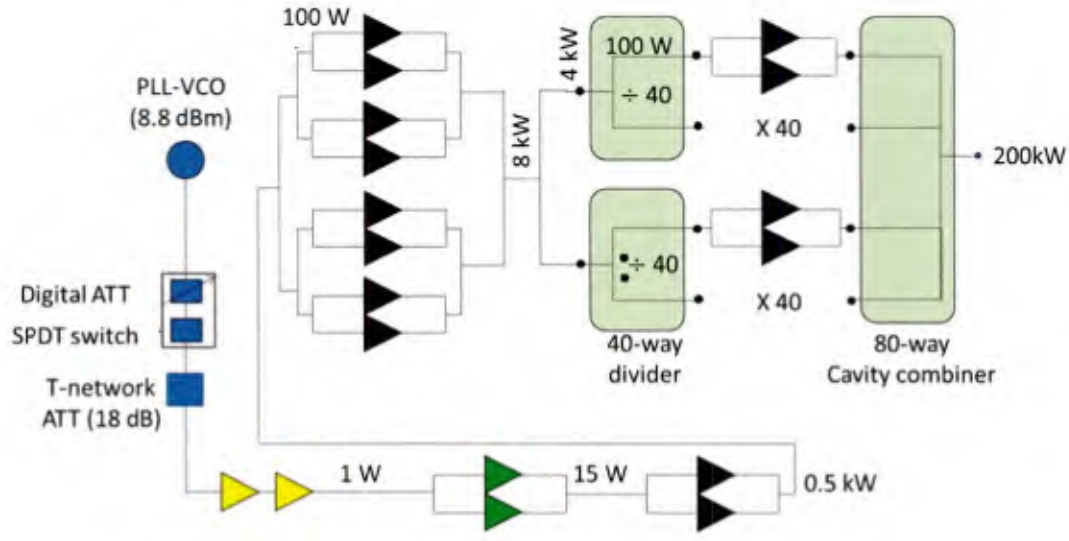


Figure 107. Layout and power budget of the 80-way power combiner experiments

Figure 108 shows a CAD drawing of the 80-way power combiner system. As shown in Figure 108, the 80-way power combiner system consists of (1) 5 stage high gain drive amplifiers, (2) two low-loss 40-way power dividers, (3) eighty 2 kW LDMOS RF power amplifier modules, (4) a cavity power combiner (installed with 80 loop antennas), (5) directional coupler, and (6) high power dummy load. An 467 MHz RF source (Hittite HMC284MS8G, or Analog Devices ADF4355-2BCPZ) is injected to two cascaded 1 W high-gain drive amplifiers (mini-circuit ZHL-1A-S+), which output signal drives a 200 W SSPA. The RF output signal of the 200 W SSPA is divided through an

equal phase and equal amplitude Gysel power divider. The equally splitted RF powers are injected to a 2 kW SSPA module. The 2 kW output power is injected to four 2 kW SSPA modules. The 8 kW output power from the four 2 kW SSPA modules are splitted into two 40-way power divider with equal amplitude and equal phase. The output power divided from the power divider is 100 W, which is injected into each 2 kW SSPA module (one of 80 SSPA modules mounted on the cavity combiner) as an input signal. In order to insure good isolation between SSPA modules, isolators (UIY 14550A400T500NF, forward power = 300 W, isolation = 20 dB) were placed directly before the input ends of the SSPA modules.

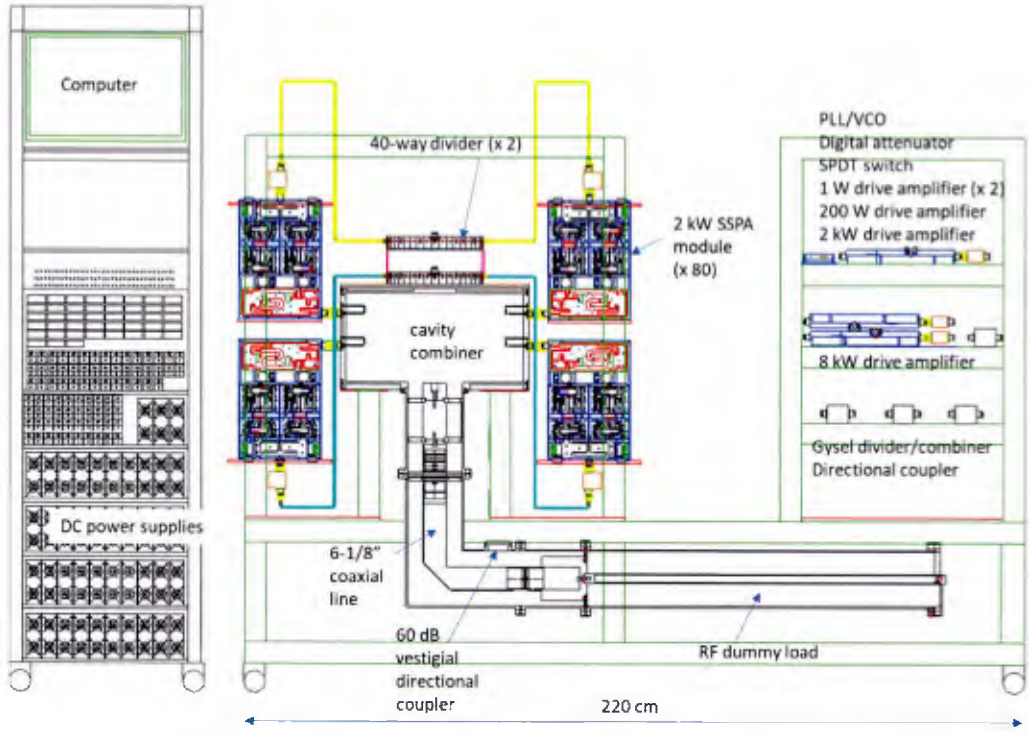


Figure 108. The 80-way power combiner system

All 80 SSPA modules were installed on the side wall of the cavity combiner. The length of all 80 coaxial transmission lines (SRT technology: SR250) is equal so that no phase difference will take place among them. As shown in Figure 109, the 80 loop antennas were installed. The loop antenna is the same type as those used in experiemnts of the 40-way power combiner. The combined RF power is extracted through 6-1/8" coaxial transmission line. As mentioned earlier in Chapter 4, the center conductor of the 6-1/8" coaxial transmission line was adjusted so that a maximum power (under a critical coupling condition) can be extracted through the line. The critical coupling condition can be met by either adjusting size and/or orientation of loop antenna or

adjusting the height of the center conductor of the 6-1/8" output line, or both. We could achieve a critical coupling condition only by adjusting the center conductor of the 6-1/8" coaxial line (without changing the loop antenna dimension or adjusting its orientation). Cold-test measurement showed that, under the critical conupling condition, the RF loss in the cavity combiner was only 0.08 dB (corresponding to the combining efficiency of 97 %). This high combining efficiency was attributed to extensive and careful design work done by HFSS simulation and analytic calculations.

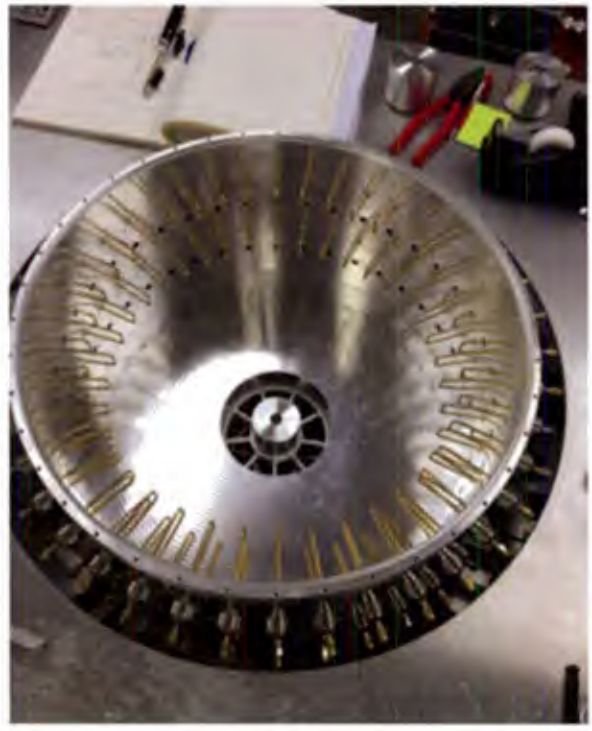


Figure 109. Cavity power combiner showing 80 loop antennas

The combined RF power passes through a 90 degree bend. A small fraction of the power is sampled through the vestigial directional coupler (described in Section 8.1) to monitor signal spectrum and measure true RF power in the 6-1/8" coaxial line. The RF high power is dumped in the water-cooled RF load (described in Chapter 7). All RF compoents (incuding coaxial cables, attenuators, couplers) were measured by using a calibrated VNA. The power sensor and meter are Agilent's E4417A/E9325A. The spectral shape of the combined RF signal (including spectral width, harmonic frequencies) was analyzed by using Agilent Spectrum Analyzer (E4440A). Pulse rise-time and fall-time of the pulsed RF signal were measured by a Krystal detector (model D101) and a fast digital oscilloscope. The phase detector (Analog Devices 8302 EVAL BD) was used to measure AM-

PM conversion (degree versus dBW), which is the measure of phase change as a function of RF output power.

CW RF source converts into a pulsed RF signal through a RF switch. RF pulsing (producing a pulse train with predetermined pulse with and PRF) was contolled by a digital SPDT switch (described in Secion 8.3). Duty cycle can be variable from 0 to CW by properly choosing pulse width and PRF. Control signal was provided by an analog TTL signal generated by the Digilent's Discovery2 ADC module connected with a notebook computer. RF power was adjusted by using a variable attenuator (mechanical attenuator) or changing the digital attenuation factor of the 5-bit digital attenuator. The 5 control signals were supplied by the Digilent's Discovery2 ADC module connected with a notebook computer.

We have configured the Agilent VEE program to control power supllies and monitor input and output RF powers. Instruments were connected to a computer via GPIB cables. The programmable VEE software facilitates us to contol and monitor the power combiner system. It displays power and efficiency and status of power supplies (voltage and curent) in real time.

11.2 Experimental results

Experiments on the 80-way power combiner were performed in two cases: (a) low duty cycle, and (b) high duty cycle. Hittite RF source (manually variable power from -40 dBm to 25 dBm) was used as a signal source in a low duty experiment. A stable Analog Devices PLL/VCO frequency synthesizer (fixed power at 8.8 dBm) was used in a high duty experiment.

11.2.1 Low duty experiment

FIRST TRIAL

All the low duty experiments were carried out with parameters: duty cycle = 0.1 %, PRF = 10 Hz, PW = 100 microseconds. There was no need of cooling SSPA modules. ANSYS thermal analysis (described in detail in Section 4.3) predicts that 0.1 % duty cycle does not cause significant thermal loading on the SSPA modules. The first experimental setup is shown in Figure 110. As shown in Figure 110, the first 40-way power divider is connected to 40 SSPA modules (serial numbers: 1 to 40) and the second 40-way power divider is connected to the other 40 SSPA modules (serial numbers: 41 to 80).

An 80-way power combining experiment was performed. A photo of the 80-way power combnier system is depected in Figure 111. The center pin (conductor) height of the 6-1/8" coaxial line was set so that a maximum output power should be extracted with a critical coupling condition (described in Section 5.3). RF ouptut power was sampled through a 60 dB directional coupler. Figure 112 shows combined power as a function of input power at 467 MHz where the input power is the power measured at the output port of the 200 W drive amplifier. As shown in Figure

112, the output power increases linearly at a linear region and get saturated when a drive power reaches 50 W as seen in a typical RF ampifier. The saturated RF power was measured to be 155 kW, which is 25 kW less than the expected power (180 kW).

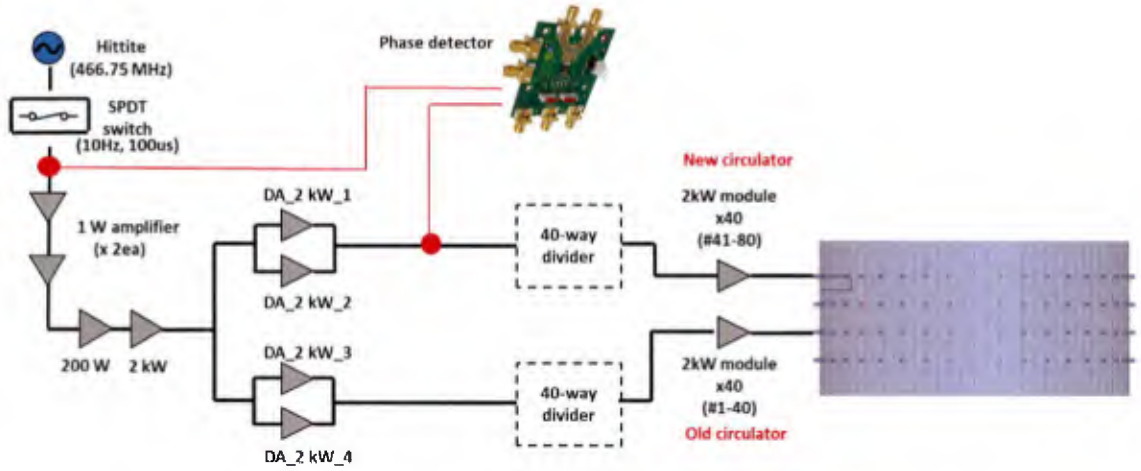


Figure 110. First setup for experiments on 80-way power combiner.

Figure 111. Photo of 80-way power combiner system, operating at low duty cycle (duty cycle = 0.1 %, PRF = 10 Hz, PW = 100 microseconds)

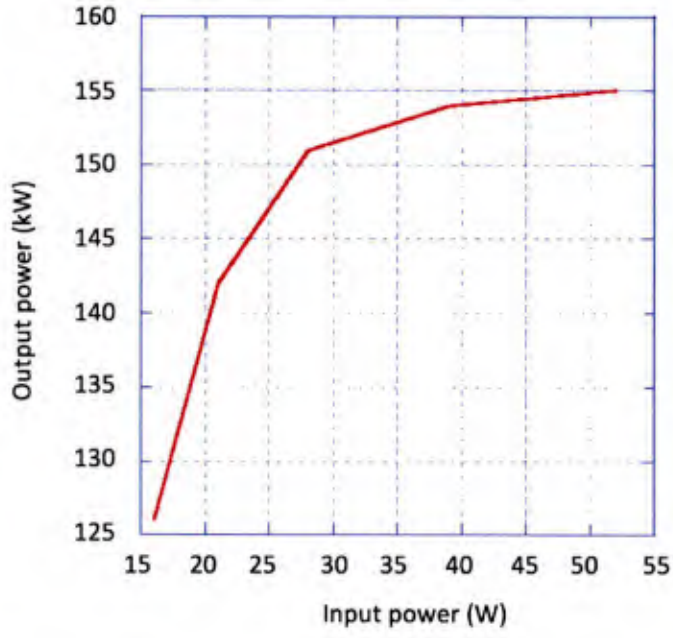


Figure 112. Combined power as a function of input power (here, the input power is the power measured at the output port of the 200 W drive amplifier.)

Analysis has been done in order to understand the degradation of output power and combining efficiency. It was realized that phase coherence is very important for efficient power combining experiments. Individual RF signal injected into all 80 SSPA modules should have phase coherence so that maximum power combining takes place in the TM_{010} cavity. We have measured relative phases at two drive output ends using a phase detector, as shown in Figure 110. The measured phase difference between two drive amplifier output ends was 30 degrees. This is quite astonishing results. The two output ends are supposed to be equal phase because all the RF components and connectors are identical. The reason for the 30 degrees phase discrepancy might be caused by different characteristics of the LDMOS transistor operating near saturation.

The other phase discrepancy was found in UIY circulators. We installed two different models. The first 40 SSPA modules (serial numbers: 1 to 40) have UIY circulators of model UIYDC3538A470T570 and the second 40 SSPA modules (serial numbers: 41 to 80) have UIY circulators of model UIYDC3538A450T550. The S_{21} phases of the two models were measured using a calibrated VNA. The phase difference was found to be 10 degrees.

HFSS field calculator was utilized to predict the effect of a combined output power by phase difference. All the 80 SSPA powers entered in the field calculator were measured powers.

Table 19 shows the results of HFSS field calculator. As shown in Table 19, phase difference was entered in the field calculator by 40 degrees (30 degrees from the drive amplifier and 10 degrees from circulator). The calculated combined power was 159 kW, which is in good agreement with the experimentally measured RF power of 155 kW. It was confirmed that the power degradation was caused by the phase imbalance.

Table 19. Combined power as functions of phase difference

$\Delta Phase$ (degrees)	$P_{combined}$ (kW)
40	159
50	148
60	135

SECOND TRIAL

Based on the first trial experiments, we had to modify two things in order to keep phase coherence on all 80 SSPA modules output ends before they are coupled in the cavity combiner: (1) reconfiguring the drive amplifier and (2) replacing UIY circulators with new model UIY circulators. One simple way of keeping phase coherence of the drive amplifier is that two output ports of the drive amplifiers are combined and divided into two output ports. All UIY circulators located at output ports of NXP LDMOS transistors were replaced with new model UIY circulators (UIYDC3538A450T550). Figure 113 shows the modified experimental layout. One disadvantage is power loss due to the combiner and divider's insertion loss (typically 0.3 dB loss each). As shown in Section 9.3, the measured output power of 8 kW drive amplifier modules was 7.7 kW at saturation. This 7.7 kW will be divided by 3 dB through a Gysel divider and two 40-way dividers before injecting into the eighty 2 kW SSPA modules.

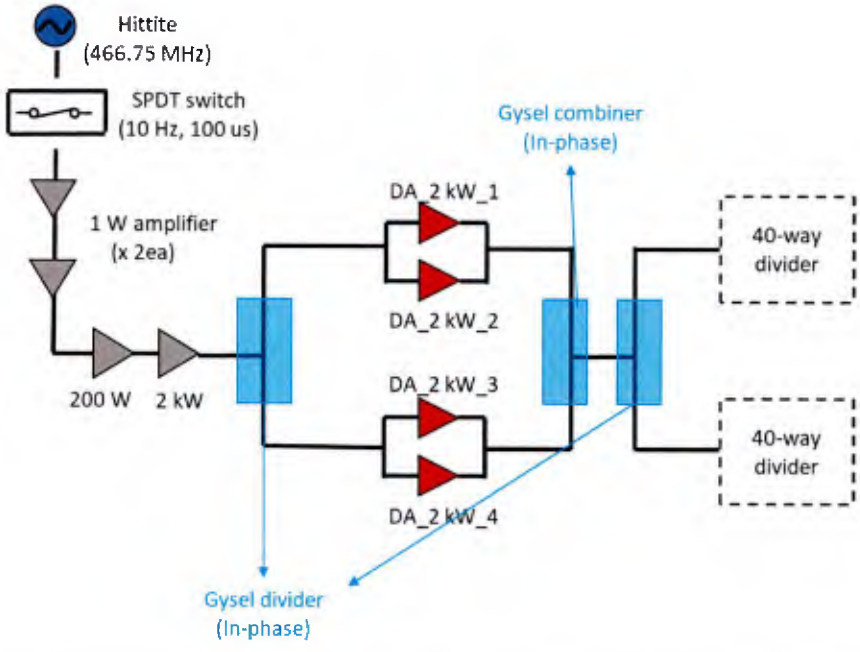


Figure 113. Experimental layout for keeping phase coherence on all 80 SSPA modules.

Output powers of the eighty 2 kW SSPA modules were measured to ensure that all SSPAs operate without any failure or power degradation. All other 79 SSPA modules were mounted on the cavity combiner while each individual SSPA was tested. Figure 114 shows measured output power of all 80 SSPA modules. Note that we have tuned all 80 SSPA modules for higher output power. As shown in Figure 114, RF power ranges between minimum 2 kW and maximum 2.8 kW. The algebraic summed power of all individual power is 187 kW. It should be noted that power variation does not cause a significant degradation of combining efficiency, which was verified by HFSS field calculator. Taking into account the power imbalance of the 80 SSPAs, we use HFSS calculator to predict combined output power and combiner efficiency. Entering the individually measured RF power of the 80 SSPAs into the HFSS field calculator, we obtained the combined power of 182 kW. This HFSS calculated RF power is 5 kW less than the summed power of all 80 individual RF powers, indicating that the power imbalance is not an important factor in such a cavity power combiner. The discrepancy is due to the non-equal SSPA power (power imbalance) as seen in Figure 114.

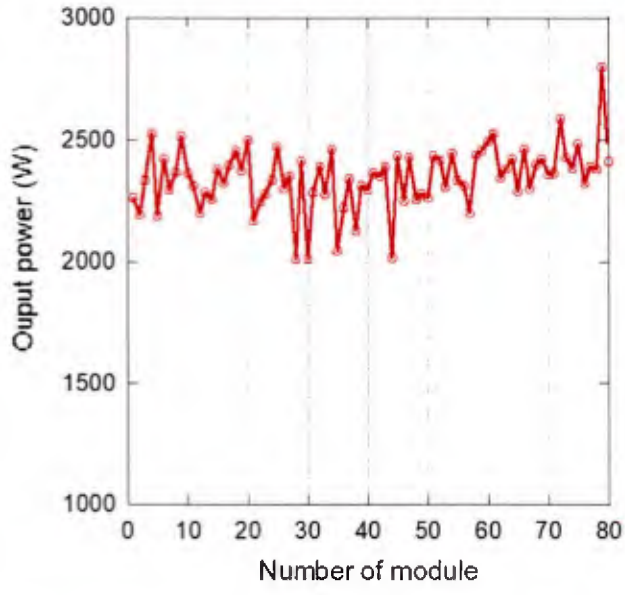
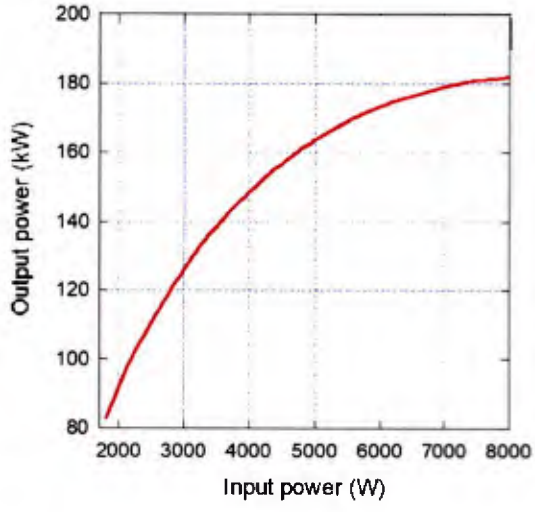


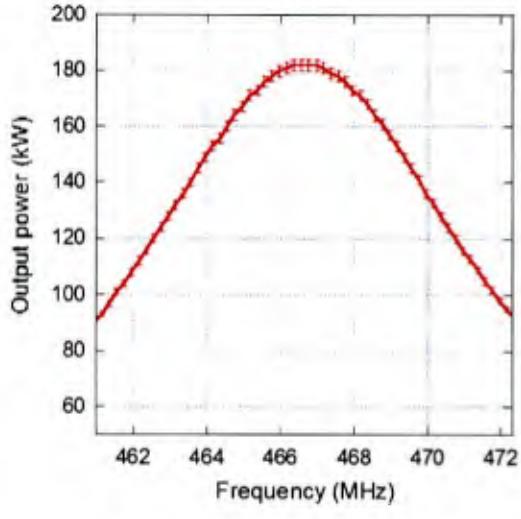
Figure 114. In-situ power measurement of the 80 SSPA modules.

A low duty experiment (PW = 100 miscrosecond, PRF = 50 Hz, duty cycle = 0.5 %) was performed. A drive curve (combined RF output power verse RF input power) is depicted in Figure 115(a). Here, the input power is the power combined from four 2 kW drive amplifiers. The input power was monitored by the use of the microstrip line diretional coupler. The output power was measured from the signal samapled from the vestigial directional coupler, followed by two fixed attenuators (in order to further attenuate the signal before the Agilent's sensitive RF detector). As shown in Figure 115(a), the combined output power increases linearly as the input power rises. The output power starts to roll off as the input power reaches near 8 kW. The saturated RF power was measured to be 183 kW at 467 MHz. A power combining efficiency defined as the measured combined power divided by the summed power of all individual SSPA output power. The summed power, measured combined power, and HFSS field calculated power are 187 kW, 179 kW, and 182 kW, respectively. From the equaiton above, we calculated the power combining efficiency. The power combining efficiency was found to be 96 %. If one uses the HFSS field calculated power (182 kW) (instead of the summed power (187 kW)) as a reference value, the combining efficiency becomes 98 %. To my best knowledge, this is the highest power and efficiency achieved from a single cavity power combiner ever reported. It should be pointed out that this unprecedented high combining efficiency of more than 95 % was achieved from the the cavity combiner, where the number of input signals were 80. As mentioned earlier in Chapter 5, HFSS predicts that the combining efficiency will remain as high as 95 % even with 160 SSPAs combined in the cavity combiner. Such an efficient cavity power combiner can be applied to the higher number of input signals than 160.

Figure 115(b) shows frequency bandwidth. The 3 dB bandwidth was measured to be 11 MHz (461 ~ 472 MHz), or 2.4 % which is twice wider than that of the 40-way power combiner. The bandwidth increase was due to the low external Q of the cavity lowered by the 80 loop antennas. The error bar in Figure 115(b) was from the amount of error found in measuring the coupling factor of the 60 dB directional coupler using the calibrated VNA.



(a)



(b)

Figure 115. (a) Drive curve, (b) freqeuncy bandwidth of the 80-way power combiner

11.2.2 High duty experiment

Experiments on high duty operation was carried out to investigate the effects of thermal stress of the RF components. Although the LDMOS FET power transistor is rugged enough for CW operation, there exist other limiting factors to increasing the duty cycle. We have analyzed thermal loads of all RF passive and active components used in the 80-way power combiner system. Figure 116 shows the summary of the thermal loading values of RF components. As shown in Figure 116, the lowest value of maximum duty cycle is 30 % (circulator of LDMOS output, Diconix 50 ohm load resistor (Diconix 17-0573) at circulator, and UIY circulator of 2 kW SSPA module input), indicating that thermal handling capability limits the maximum duty cycle of 30 %. The 6-1/8" coaxial transmission line has a maximum CW power handling capability of 80 kW (corresponding to 40 % duty cycle) at which the center conductor reaches to 100 degree C. The output coaxial connector of the 2 kW SSPA module is the Type-N connector. This Type-N connector has a typical CW power rating of 1 kW at 1 GHz. The power rating of any transmission line or connector decreases as RF frequency increases (maximum power rating $\propto 1/\sqrt{f}$) due to skin effects of the metallic conductor.

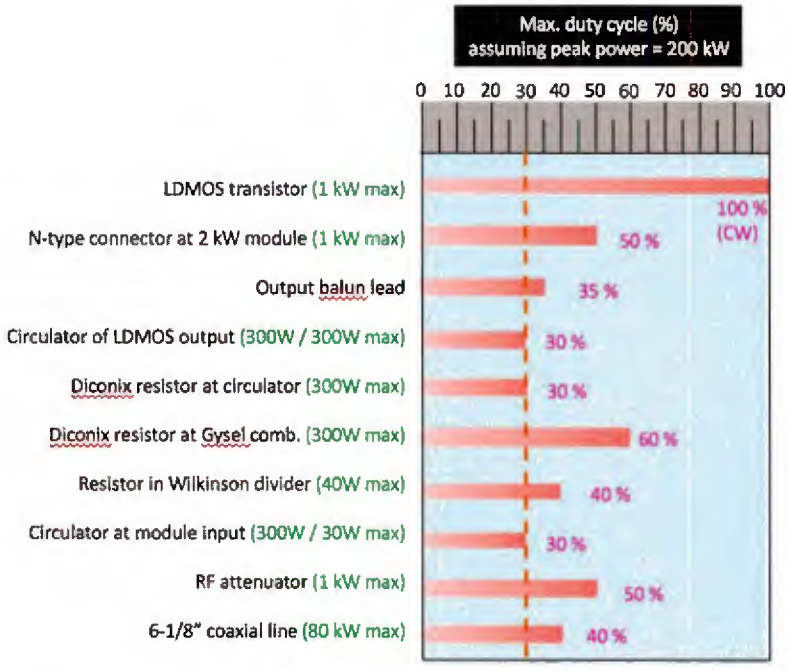


Figure 116. Summary of thermal loading values of RF components

Figure 117 shows the experimental layout for testing the power combiner system operating at high duty cycle. Three major changes in experimental setup were made. One is the

replacement of the RF signal source. Instead of the Hittite signal source, a phase-lock-looped RF synthesizer (Analog Devices ADF4355-2BCPZ: Fractional-N synthesizer 50 MHz – 4.4 GHz) was used as a signal source. This will provide us a stable RF signal source with an extremely low phase noise. RF power generated from the RF synthesizer was measured to 8.8 dBm at 467 MHz, which is 18 dB higher than what we need for source power. As shown in Figure 118, we inserted a 18 dB fixed T-network attenuator between RF switch and 5-bit variable attenuator. We could have taken one 1 W SSPA out instead of the 18 dB attenuator. However, We decided to leave two 1 W SSPAs as it was because one might need higher drive power for a future high duty experiment.

The second is the installation of cooling pipes on all 80 SSPA modules. Cooling the SSPA modules was necessary for operating the SSPAs at a high duty cycle of more than 20 % (as predicted from ANSYS ICEPAK simulations (shown in Section 4.3)). The coolant used in this experiment is a tap-water.

And, the third is the use of MEANWELL DC power supplies (MEAMWELL RSP-2000-48: 48 V, 42 A). As shown in Figure 119, we installed 10 power supplies in the instrument rack so that the high duty operation can be done. The electric power available in our lab limits the maximum duty on the 80-way power combiner experiments. Although the power combiner system is designed for operating up to 30 % duty cycle, we were forced to run the system with a maximum duty cycle of 5 % due to the limited AC power capacity available in our lab. Assuming peak RF power = 200 kW (average RF power = 10 kW), duty cycle = 5 % and DC-RF power conversion efficiency = 50 %, the total average current supplied to 80 SSPA modules is calculated to be 400 A where DC voltage is assumed to be 50 V. Therefore, 10 DC power supplies are sufficient to provide DC power to the 80 SSPA drain bias lines. Each power supply provides DC power to 8 SSPA modules.

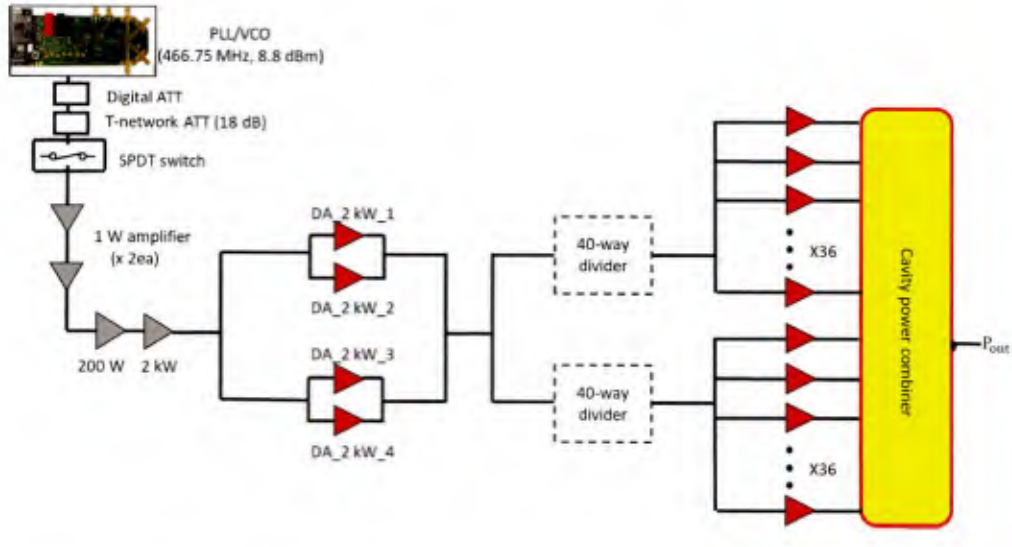


Figure 117. Experimental layout for testing the power combiner system with high duty cycle

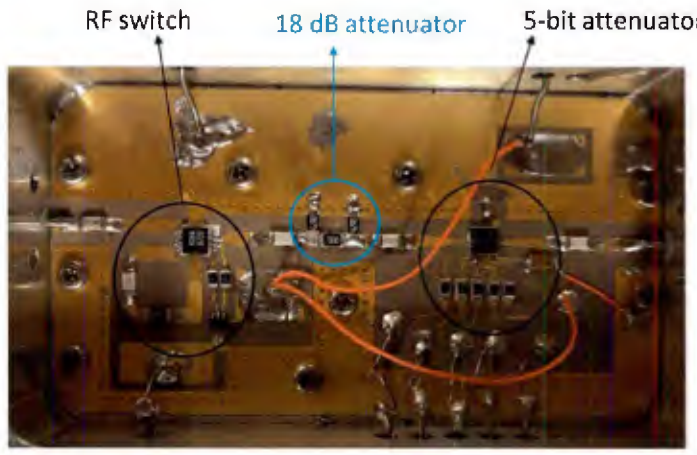


Figure 118. Photo of modified RF switch and attenuator module inserted with a18 dB T-network fixed attenuator

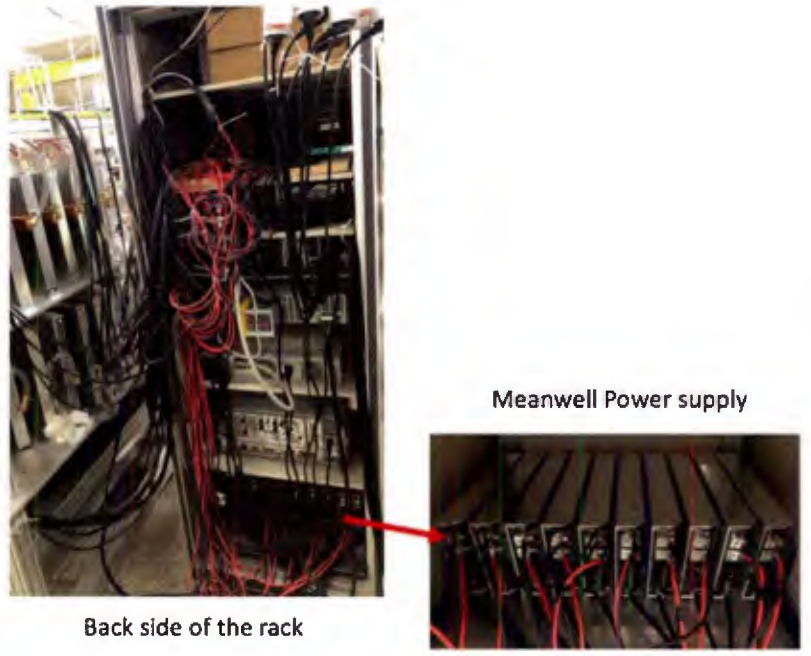


Figure 119. Photo showing the backside of the rack and 10 power supplies

Figure 120 shows the photo of the assembled 80-way power combiner system operating at high duty cycle. As described in Section 4.3, we showed that each individual 2 kW SSPA

module was tested up to 30 % without any failure. Coolant (inlet tap-water temperature = 18 degree C) was flowing to all 80 SSPA modules and RF dummy load in order to dissipate RF ohmic power.

High duty operation was performed with variable PRF and PW. Table 20 summarizes the operation conditions (PW, PRF, attenuator digital logic) for each duty cycle. Figure 121 shows the output power as functions of duty cycle varying from 0.1 % to 5 % where the drive frequency is 467 MHz. As shown in Figure 121, the RF power decreases as the duty cycle increases. The peak power and average power at 5 % duty cycle are 170 kW and 8.5 kW, respectively. The output power of 5 % duty cycle slightly dropped by 0.3 dB compared with the 0.1 % low duty operation. The power drop by 10 kW was expected from the earlier tests on the SSPA module (described in Section 4.3). As described in Section 4.3, the gain of the 2 kW SSPA gradually dropped as the duty cycle increased. It should be noted that the power drop can be cured by increasing input power as shown in Figure 28 in Section 4.3. It is evident that the gain drop was the cause of the power drop. The high output power (52.6 dBW, 180 kW) can be achieved by injecting higher drive power more than 8 kW. Unfortunately, the maximum drive RF power is 8 kW in the present experimental setup. It should be noted that the power combining efficiency remains 95 % for duty cycle variation from 0.1 % to 5 %, suggesting that the high combining efficiency was not affected by the duty cycle at all.

Figure 122 shows RF combined power as functions of the input frequency sweeping from 460 MHz to 475 MHz where the duty cycle was set at 5 %. A maximum power, 52.3 dBW (170 kW) was observed at 467 MHz. The 3 dB bandwidth was 2.4 % (462 MHz – 473 MHz), which is the same as the bandwidth seen at low duty operation.

Additional experiments were performed with higher drain voltages in order to investigate the drain voltage dependence on the amplifier output power. The MEANWELL power supply (nominal voltage = 50 V) can supply voltage up to 55 V. Table 21 shows the measured RF output powers for 50 V, 53 V, and 55 V for two duty cycles (0.1 % and 1 %) where the input source frequency is 467 MHz. A maximum power was found to be ~ 200 kW at drain bias voltage = 55 V. Noting that the NXP LDMOS FET (drain-source breakdown voltage = 133 V minimum) is rugged enough to operate at higher drain voltage = 60 V (or, peak voltage = 60 x 2 = 120 V for Class AB operation), it is expected to have RF output power of more than 200 kW when the amplifier operates at drain voltage = 60 V.

Figure 120. Photo of 80-way power combiner system operating at high duty cycle

Table 20. summary of operation condition for high duty cycle

Duty cycle (%)	PRF (Hz)	PW (microseconds)	RF output power (dBW/kW)	5-bit digital attenuator logic
0.1	10	100	52.58/181.1	10110
1.0	100	100	52.57/180.7	10110
2.0	200	100	52.52/178.6	10110
3.0	300	100	52.45/175.8	10110
4.0	400	100	52.39/173.4	10110
5.0	500	100	52.30/169.8	10110

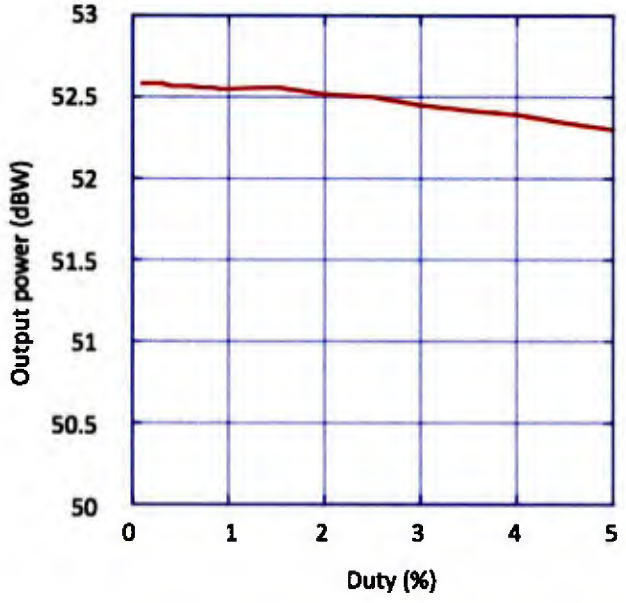


Figure 121. RF output power as functions of duty cycle varying from 0.1 % to 5 %

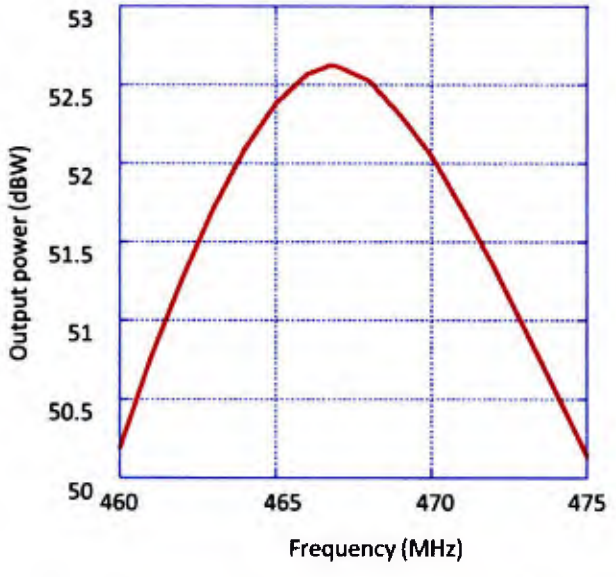


Figure 122. RF combined power as functions of the input frequency sweeping from 460 MHz to 475 MHz where the duty cycle is 5 %

Table 21. Measured RF output powers for drain voltage = 50 V, 53 V, and 55 V for two duty cycles (0.1 % and 1 %) where the input source frequency is 467 MHz

Drain voltage (V)	50		53		55	
Duty (%)	0.1	1.0	0.1	1.0	0.1	1.0
Input power (kW)	8.4	8.3	8.3	8.2	8.4	8.2
Output power (kW)	176	175	189	191	197	196

Spectral purity was analyzed using the Agilent's frequency spectrum analyzer. First of all, a phase noise of the PLL signal source was measured in a CW mode. A phase noise of -124 dBc/Hz was measured at 100 kHz offset from carrier frequency of 467 MHz. Figure 123 shows a photo of screen shots of the displayed spectral shape at 6 locations where the duty cycle is 5 %. As seen in the Figure 123, The spectral width became remarkably widened right after the SPDT switch (position 1 in Figure 123). The increased spectral width is presumably caused by the pulse-to-pulse phase noise (or signal jittering in a time domain) occurring in the SPDT switch. In other words, a phase coherence does not maintain between pulses in the pulse train. It is interesting to notice the spectral width does not grow anymore since the position 1. Asymmetric spectral shape was seen at position 6 in Figure 123. The asymmetric spectral shape is due to non-uniform RF power during the pulse width. We have observed a slight RF power drop within the intra-pulse during a 100 microseconds pulse width. Harmonic frequency contents were measured as well. Figure 124 shows spectral amplitudes at fundamental frequency (467 MHz), second harmonic frequency (934 MHz), and third harmonic frequency (1401 MHz). The second and third harmonic amplitudes are 34 dBc and 40 dBc, respectively, lower than that of the fundamental frequency. As seen in Section 3.2, ADS HB simulation predicted 33 dBc and 65 dBc for the second and third harmonics, respectively.

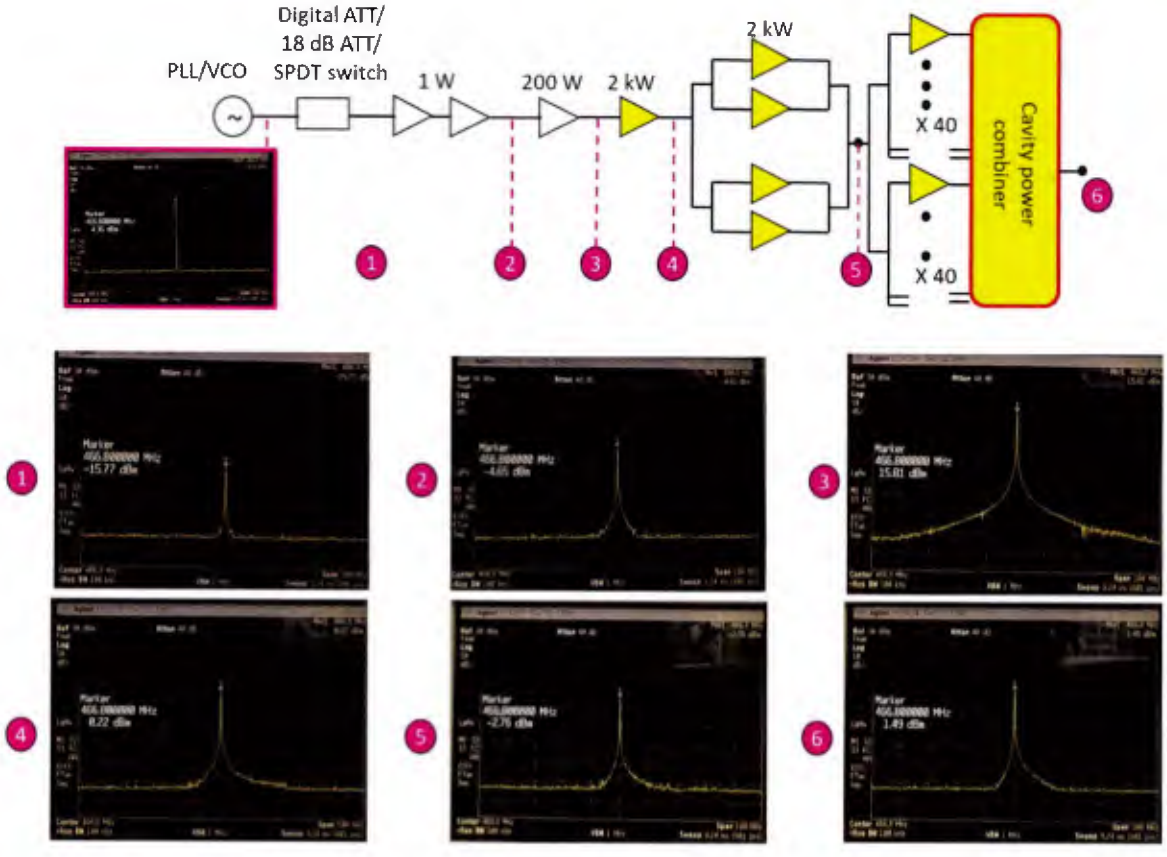


Figure 123. Screen shots of the displayed spectral shape at 6 locations

Figure 124. Spectral amplitudes at fundamental frequency (467 MHz), second harmonic frequency (934 MHz), and third harmonic frequency (1401 MHz).

Lastly, an AM-PM conversion loss was measured using a phase detector. The RF phase of the output signal varies along with the output power in any non-linear active devices including both solid state transistors and vacuum power tubes (TWTs, kylstrons, gyrotrons etc.). The AM-PM conversion loss tells us the measure of non-linear characteristic of the amplifier operating near the saturation regime. The phase detector was used to detect phase difference between the input line from the signal source (as a reference point) and the 6-1/8" coaxial transmission line (the point where 170 kW RF power is observed). The output analog signal from the phase detector is proportional to the phase difference (30 mV per 10 degrees). One can get the phase value by measuring the analog voltage displayed on a digital oscilloscope. Figure 125 shows the measured phase change as functions of RF output power. Phase change increases linearly at the beginning and increases rapidly near the power saturation region. The maximum phase change is observed to be 48 degrees at 52.7 dBW output power. Table 22 shows a summary of the experimental results of the 80-way RF power combiner system.

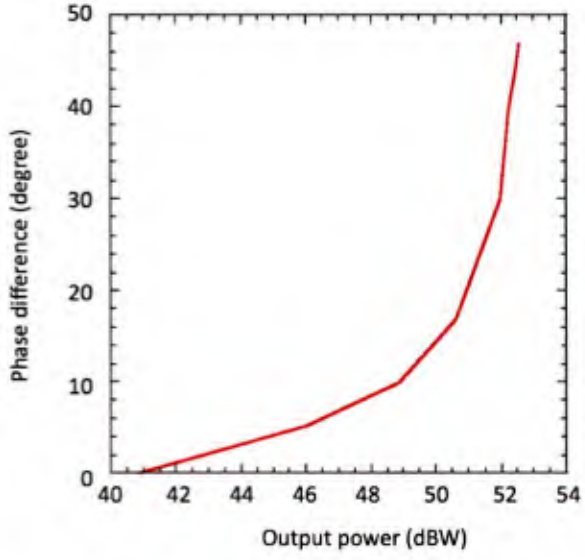


Figure 125. Measured phase change as functions of RF output power

Table 22. Experimental results of the 80-way power combiner system

Parameter	Specifications	Remarks
Transistor	NXP 1 kW LDMOS FET (MRFE6VP61K25HR6)	Total number of transistors = 160
Frequency	467 MHz	2.4 % bandwidth (1.2 % for 40-way combiner)
RF output power of 2 kW SSPA module	2.3 ~ 2.6 kW	
Drain efficiency of 2 kW SSPA module	55 ~ 65 %	
Saturated gain of 2 kW SSPA module	15 ~ 16 dB	- 16 dB at low duty (0.1 %) - 15 dB at 30 % duty cycle
Combiner	TM_{010} mode cylindrical cavity	
Combined output power (peak power)	183 kW (82.6 dBm) at 50 V (200 kW at drain voltage = 55 V)	
DC to RF power conversion efficiency of power combiner system	> 50 %	> 60 % for SSPA
Combining efficiency	> 95 %	Equally high combining efficiency for 40-way power combiner
System gain	92 dB	- Without 18 dB attenuator - PLL/VCO power: 8.8 dBm
Duty cycle	0.5 ~ 5 % (PRF = 50 ~ 2000 Hz, PW = 100 ~ 1000 μsec)	- Individual SSPA module was tested up to 30 % duty - Duty cycle was limited up to 5 % by AC power capacity in our laboratory
Operating conditions (nominal)	$V_{DS} = 50$ V $V_{GS} = 2.5$ V	
Harmonics	34 dBc (2^{nd} harmonic) 40 dBc (3^{rd} harmonic)	at saturation
AM-PM	48 degrees at saturation	
System size	120 cm x 220 cm x 170 cm	not including a rack
RF output port	6-1/8" coaxial transmission line	- Maximum CW power = 80 kW at 1 GHz - Maximum peak power = 3 MW

Conclusion

In this project, an all solid-state, compact RF power combining system with a cavity power combiner was proposed and developed. Both 40-way and 80-way combining systems demonstrated RF output power of 100 kW (peak) at 464 MHz and 200 kW (peak) at 467 MHz, respectively with a combining efficiency of more than 95 %.

The major accomplishments in developing the SSPA based power combiner system include (1) design of high-efficiency, 1 kW and 2 kW LDMOS solid-state-power-amplifiers (SSPA), (2) fabrication and RF test of one hundred sixty 1 kW SSPAs and eighty 2 kW SSPA modules with a high duty cycle (30 %), (3) theoretical study and development of a 160-way cavity power combiner for high combining efficiency and high-power handling capability, (4) design and test of a 40-way equal-amplitude, equal-phase power divider, (5) design and fabrication of a high power water-cooled RF load, and (6) RF system integration and reliable operation of the power combiner system with a variable duty cycle (PW, PRF).

The RF power transistor used for power combiner was the NXP 1 kW RF LDMOS push-pull type transistor. Source-pull and load-pull impedances were extracted from an extensive numerical analysis using non-linear circuit simulator (ADS) and 3D electromagnetic field simulation tool (HFSS). Following circuit optimization for maximum output power, two of the 1 kW SSPAs were combined through a Gysel power combiner in order to make a 2 kW SSPA module. Eighty identical SSPA modules were fabricated. All 80 SSPA modules were tested with RF power ranging from 2 kW to 2.8 kW and DC-RF conversion efficiency of more than 60 %.

An RF power combining technique is the most challenging and critical work in this project. We have designed and developed a cavity-type power combiner operating at TM_{010} mode in a cylindrical cavity. The unique characteristics of the innovative power combiner system are its compactness and extremely low power loss, making it possible to obtain an unmatchable power combining efficiency. The cavity combiner was designed to combine 160 input RF sources in maximum. The work included thorough examination on cavity coupling theory and extensive numerical simulation for optimizing cavity and coupling. Cold-test measurements for cavity Q and power combining efficiency for both 40-way and 80-way power combiners were performed by using a calibrated VNA. Cold-test measurements showed that measured power combining efficiency of 40-way and 80-way power combiner was more than 97 %, which was in good agreement with HFSS simulation results.

A power combiner system was constructed and was successfully tested. The system consists of eighty 2 kW SSPA modules, cavity power combiner, 40-way power equal amplitude/phase RF power divider, 60 dB vestigial directional coupler, matched RF load, and 5 stage drive amplifiers. RF amplifier was designed to operate at variable duty cycle by controlling PW and PRF through a SPDT RF switch and to operate at adjustable output power by controlling a 5-bit digital RF attenuator. Experiments showed that the RF power combiner produced a peak

RF output power of 100 kW at 464 MHz with 1.2 % bandwidth for the case of forty 2 kW SSPA modules and 200 kW at 467 MHz with 2.4 % bandwidth for the case of eighty 2 kW SSPA modules. Most remarkably, the measured power combining efficiency was found to be more than 95 % for both cases. Simulations predicted that power combining efficiency remained > 95 % when 160 SSPA modules were combined through the cavity power combiner. To our best knowledge, this is the highest combining efficiency reported ever for such large number of power amplifiers.

The present work on the high power multi-way power combiner system that we have performed and achieved under this ONR contract is truly believed to have impacts on our HPM community. The developed highly efficient power combining system operating with a variable duty cycle revealed a high efficiency power combining technology and extended the limit of all transistor-based radiation source. It will advance MW-level HPM technology and its application for future industrial heating and military EW/radar system in higher frequency bands covering microwave and millimeter waves (GHz to THz).

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