**Project Report**
**LSP-293**

# Digital Material Architecture: FY19 Advanced Materials & Processes Line-Supported Program

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21 April 2020

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Massachusetts Institute of Technology
Lincoln Laboratory

# Digital Material Architecture: FY19 Advanced Materials & Processes Line-Supported Program

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# 1. PROBLEM STATEMENT

Smart materials, which can respond to their environment or external input by changing properties or shape, are an active area of research. Versatility of these materials has been limited by their lack of "programmability." Current smart materials generally react along predefined paths, by changing their shape between two or more known configurations via folding, or actuation caused by internal or external stimuli. We propose a new class of smart material that will not be limited to single or few configurations but be truly arbitrary in its shape-changing abilities. Conceptually, this material would consist of repeating units or "cells," with each "cell" having a digital microcontroller and affiliated microhydraulic actuators. Upon reprogramming, the cells could individually change shape and potentially relative location, giving a macroscopic shape change to the overall material. Instructions to the cells would be sent using digital addressing principles that are used to make modern digital computers so versatile. In general, the shape of these digital materials could be changed arbitrarily, but in reality the limitations of the internal and external cell architecture will translate into limitations for the digital material.

Figure 1 shows a relatively simple architecture of a 1D digital material, or a digital string. The cells have one controller and four actuators that locally change the curvature and length of the string. This allows the string to take an arbitrary shape within the limits of maximum local curvature allowed by the actuators. The 1D example is simple because cells don't have to move or twist past each other, and there are no constraints on stretching or folding within a string. The situation quickly becomes much more complex for 2D and 3D digital material. In 2D and 3D materials, no conceptually simple cellular or extracellular architecture seems to exist, and the list of potential configurations that could form a structural basis multiply greatly.

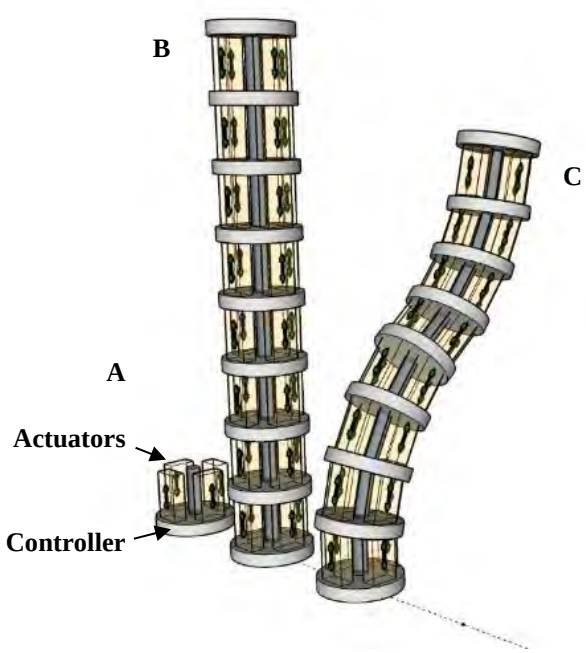


*Figure 1. Example of a digital material string (1D) . (A) Shows a single "cell" unit of the 1D digital material. It consists of a central core, four linear actuators, and a base controller. String cells can be stacked in to form a string material; without actuation the string is straight as shown in (B). When actuators are actuated by the controller of the digital string changes local curvature or length, as shown in (C). The result is a 1D string material that can arbitrarily change curvature in the two orthogonal directions, as well as change length. Because the cellular neighbors in the arrangement of this digital material are fixed, this is a "solid" architecture. More complex "liquid" architectures where digital cells change their neighbors are possible but in case of 1D strings, they are not required.*

# 2. INTRODUCTION

Smart materials can be loosely defined as materials that change properties due to some external stimulus. The vast majority of smart materials are analog in nature, in that they accept an analog stimulus. Examples of such materials include piezoelectric materials, shape memory alloys, and electro-active polymers, which respond to analog stimuli such as electric field, temperature, and humidity. However a much more limited set of "materials" exist where the stimuli are digital in nature. This subset of smart materials is sometimes referred to as programmable matter, or digital material. Perhaps the best example of programmable matter is biological cells modified or programmed with synthetic biology techniques. These cells accept a DNA or specific chemical activator that can be thought of as being binary and multidimensional in nature. Non-biological examples of digital material also exist but are significantly behind synthetic biology in their development. Examples include Claytronics, and Modular Robotics. Just as in the biological counterpart, the non-biological digital material consist of repeated units called cells or modules that interact with each other to form a larger system. Thus far, the size of these cells tend to be quite large, over 1 $cm^3$, and thus the granularity of digital materials is very coarse. Many nanotechnology concepts also envision a digital material composed of much smaller units, but these concepts are so far in the realm of science fiction.

At MIT Lincoln Laboratory, we have developed an actuator concept based on manipulating surface tension forces, called microhydraulics. Microhydraulic actuators are small, digital, high force, and efficient—this makes them ideal candidates for consideration as enablers of digital materials. If realized, digital material based on microhydraulics could revolutionize robotic medicine, make small reconfigurable robotic systems, or lead to self-foldable displays, solar panels, and visors. In this study, we considered different architectures for realizing digital material based on microhydraulics. This includes geometric architecture but also electronic architecture.

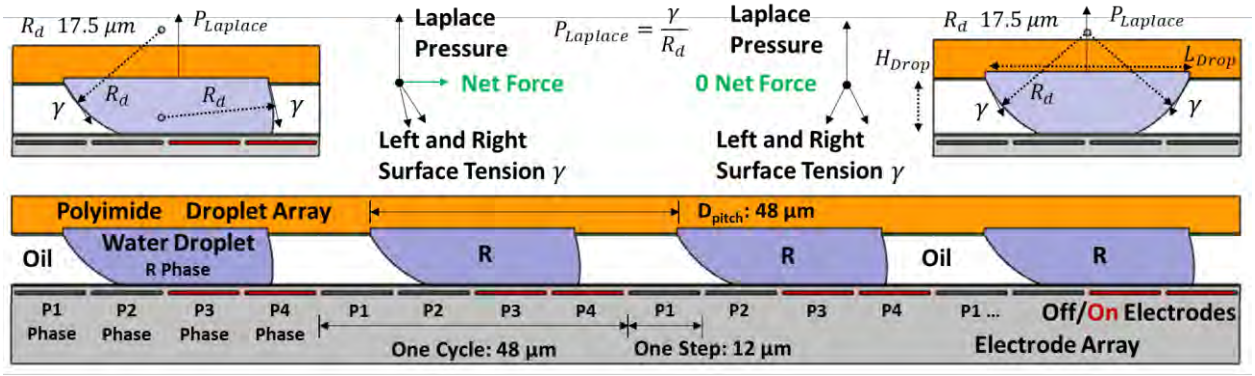


*Figure 2. Functional 2D cross-section of a single layer linear microhydraulic actuator, drawn to scale, with the water droplets deformed by voltages on electrodes (P3,P4), relative to the water droplet voltage R. Upper right shows the droplet profile with the electrodes off. In this condition, the net forces on the array are zero. When the droplets are deformed by the electrodes, shown in the upper left, a net horizontal force is produced, and the droplet array moves to align the drops to the energized electrodes. The energized electrodes are cycled with two on at any particular time, going through four states, (P1,P2), (P2,P3), (P3,P4) shown in figure, and finally (P4,P1), at which point the cycle starts again at (P1,P2). The droplet array physically follows the energized states to result in actuator motion.*

A quick overview of a 2D microhydraulic actuator is provided in Figure 2. Multilayer and 3D versions of microhydraulic actuators also have been made and are shown in Figure 3. Multilayer actuators can be stalked in series configuration as shown in Figure 3 where each layer moves in the same direction as the one below it, or in parallel which each layer moves in the direction opposite from the one below it. Series configuration multiplies speed, and parallel configuration multiplies force or torque.

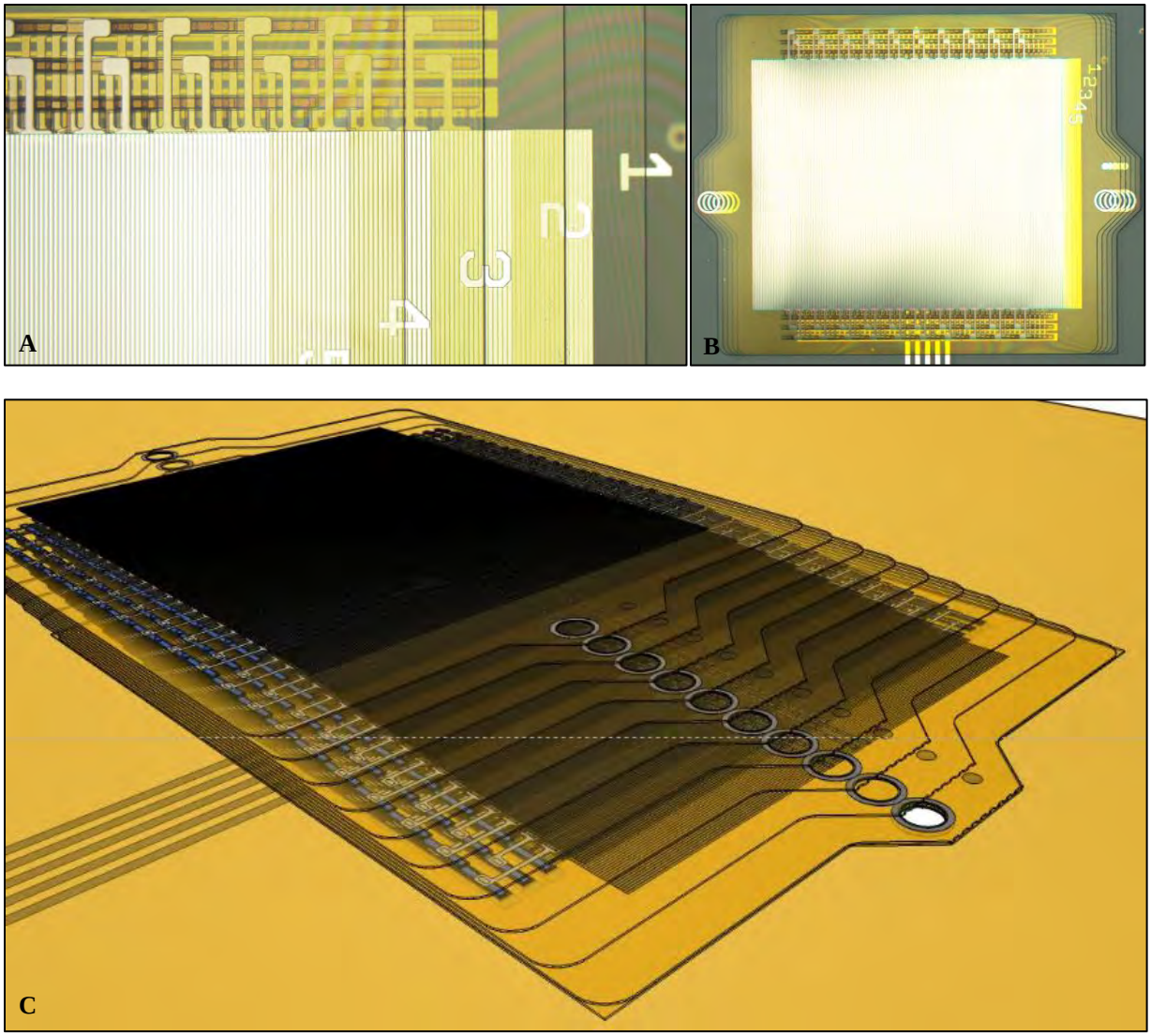


*Figure 3. 3D multilayer microhydraulic actuator, shown here in linear series configuration for greater speed. A,B (high and low magnification respectively) show implemented actuator during actuation with 5 layers in series. C shows 3D simulated image of a 10-layer linear series actuator for clarity.*

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# 3. PHYSICAL IMPLEMENTATION

The physical implementation of digital material depends on the level of complexity desired. Although we considered physical architectures for sheets of digital material that can fold and transform in an arbitrary way with origami inspired geometry, the decision was made early in the study to focus on the simplest physical architecture: that of a 1D string of digital material. Figure 1 shows a notional version of such an architecture, however we have simplified it further with only radius of curvature control along 1 axis. This simplest physical implementation is shown in Figure 4, and includes the cell and system views. The cell view shows the actuators, the backbone, the power and data buses, as well as the electronics package. These details and how they will be implemented are of course critical to the architecture. We envision that two linear parallel microhydraulic actuators will work in this architecture to provide the actuation. They will be controlled by an electronic package in each cell, which will be provided with both the data buses and the power buses. The backbone of the system will provide the mechanical rigidity for the system and connect each cell to the adjacent cells.

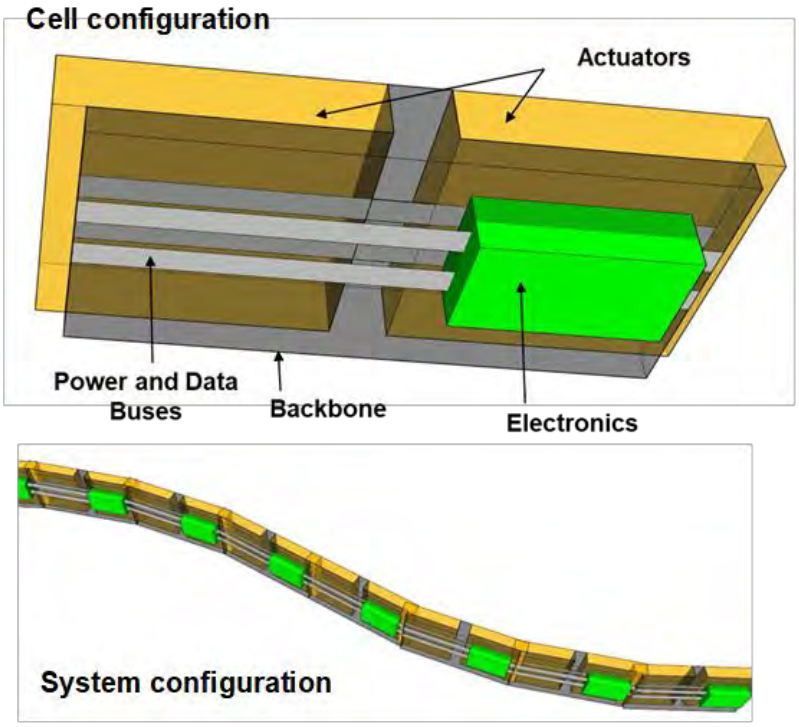


*Figure 4. Physical architecture of a simple 1D string digital material. Top view shows the cell architecture with 2 actuators, a backbone for stability and an electronics module. The buses provide data and power for the electronics module and are shared by cells along the material. The bottom view shows the system configuration with multiple cells connected along the backbone. Each cell would be addressed along the data bus and obtain instructions and power from a central module.*

The system architecture that we considered consists of a linear configuration of cells connected end-to-end on a flexible backbone. The cells are connected with data, power buses, and actuators that can induce a curvature in each cell. The data and power buses are controlled by a ‘master’ node that has a CPU, memory, and a power supply.

# 4. ELECTRICAL IMPLEMENTATION

Since the actuator design is already being explored in other programs, this study focused on the details of electronic architecture required for digital materials. There are a number of considerations when designing the electronic architecture, the primary one is how and if to do energy recovery. Microhydraulic actuators are capacitive in nature, and each phase once charged stores energy in the electric field; if the phase is turned off by simply shorting it to ground, this energy is lost and there is significant lowering of overall actuator efficiency. However the energy can be recovered and reused for subsequent steps. The two ways of recovering capacitive energy are multistep discharging and inductive discharging. Multistep discharging discharges the capacitor in steps—if, for instance, there is capacitor with a voltage V, we can discharge it in two steps: first to V/2 then to 0. This way loses only half of the energy stored. If you use four steps of V/4 to discharge, only one-fourth of the energy is lost. The second technique is to discharge the capacitor through an inductor, the inductor stores the energy in the magnetic field, which can then be recovered. Both techniques have their advantages and disadvantages. Multistep discharge requires multiple voltage sources at a fraction of the actuator voltage, and even more importantly, ways to switch those sources in and out. The inductive technique requires inductors which tend to be large, potentially defeating the aim of making a small cell.

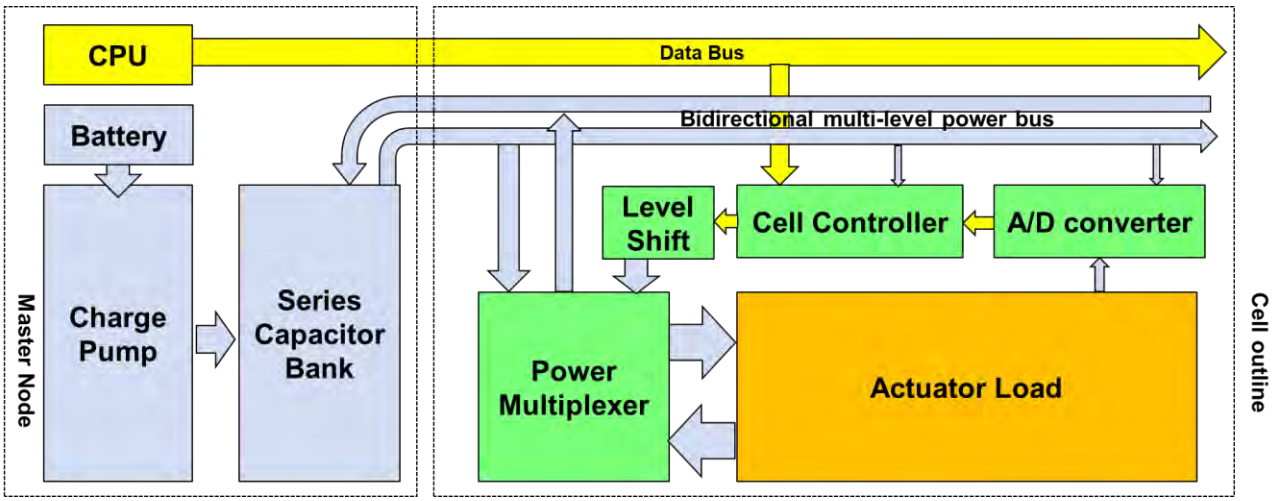


*Figure 5. Electrical configuration for a multistep discharge digital material architecture. Low-voltage digital lines are marked in yellow, power and analog lines are marked in gray. Cell electrical components are in green, and the actuator is orange. The dotted line demarks the cell boundary.*

Figure 5 shows an electrical architecture for multistep discharge based digital material. The master node has the battery, CPU, a charge pump, and a series capacitor bank. The battery provides a low voltage, $V_{batt}$. The charge pump multiplies the battery voltage by N-stages generating $V_{batt}$*N voltage, but also all the multiples of $V_{batt}$ from 1 to N. The voltages are fed into a series capacitor bank which stores the energy for use by the cells. All the voltage levels are passed to the cells through a multi-level power bus, which contains N power levels and ground. The general concept is that the actuator phases are charged and discharged in a multistep fashion by connecting them sequentially to the appropriate power levels in the power bus. This is accomplished through a power multiplexer controlled by the cell controller through a level shifter. The complexity of this design is mostly in the level shifter that is required to generate the appropriate gate voltages for the power multiplexer. This shifter has to be designed given the gate breakdown and puncture voltages of the specific implementation technology. The advantages of this design is that all the large electrical components such as the charge pump, CPU, and capacitor bank are confined to one central location and don't scale linearly with the number of cells. The electrical components inside the cell are all based on scalable transistors, and thus can be fabricated in a compact ASIC. This allows for scaling the cell without any capacitors or inductors in the cell itself, while still recovering energy from the capacitive actuator.

In this short study we did not have the resources to implement this architecture. For the cell to be compact, an ASIC encompassing the green components in Figure 5 would have to be designed. Since we wanted to implement some hardware in this study, we decided to use an inductive energy recovery architecture, implemented on a circuit board. This architecture is less compact, but more easily implemented in the time and budget constraints of this study. The next section of this report will outline the design of a four-phase microhydraulic actuator driver with inductive energy recovery, as implemented on an 8x4 cm circuit board. This circuit is probably 10,000x more area than an ASIC with the appropriate cell components for an architecture shown in Figure 5.

In addition to energy recovery, how the actuator is timed is another important consideration. The microhydraulic actuator is basically a stepping actuator, and just like a stepper motor, each step has to be externally timed by the cell controller. Timing of course should be programmable by the user, however some limits exist. For example, the actuator has a limit in force, so if the resistance to motion is too high the actuator will not move. This should be detected by the cell, and can be done by some encoder mechanism that feeds back into the cell controller. In this implementation, such an encoder is shown as an A/D converter, but it could also be implemented in an analog fashion as a current mirror with an integration capacitor, connected to a comparator. The comparator would trigger the end of the charging cycle for any phase when its charge (measured on the integration capacitor) reached a completion threshold.

# 5. MICROHYDRAULIC DRIVER CIRCUIT WITH INDUCTIVE ENERGY RECOVERY - DETAILED IMPLEMENTATION

Figure 6 shows the exact design of a microhydraulic actuator driver circuit with inductive energy recovery. The power is provided by three 3.3V batteries and is boosted to -40V, -20V, and 20V by a charge pump. The capacitive driver charges and discharges each phase with the use of an inductor, recovering the energy from the capacitive actuator. The timing for the drivers is provided by the signal generation block, which generates the master frequency and the appropriate phase-shift between the four phases of the actuator. The driver is unidirectional and does not have an encoder. Appendix A details each sub-circuit design.

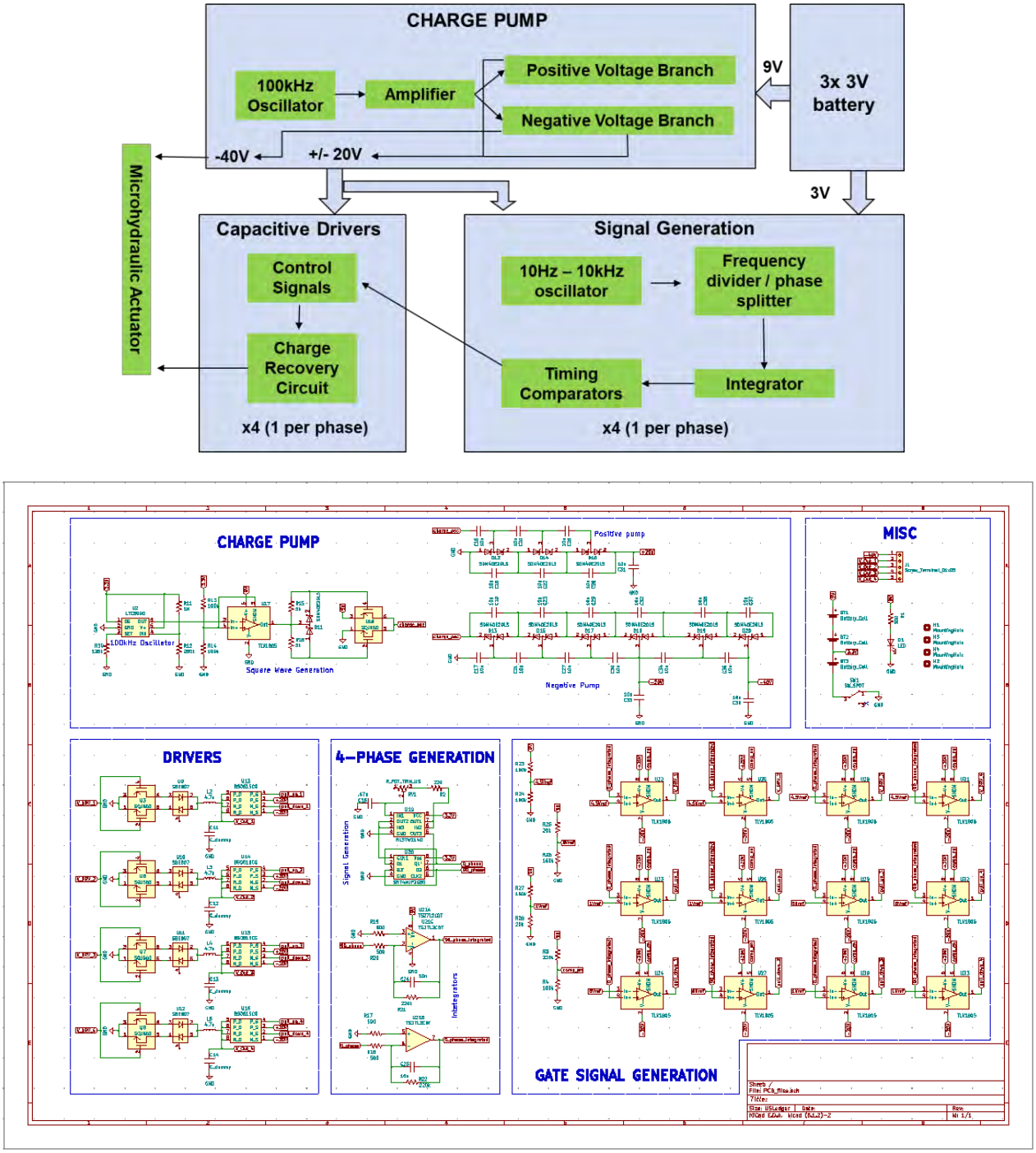


*Figure 8. (Top) Sub-section diagrams for the circuit implementation. (Bottom) The details of each sub circuit as laid out on the board.*

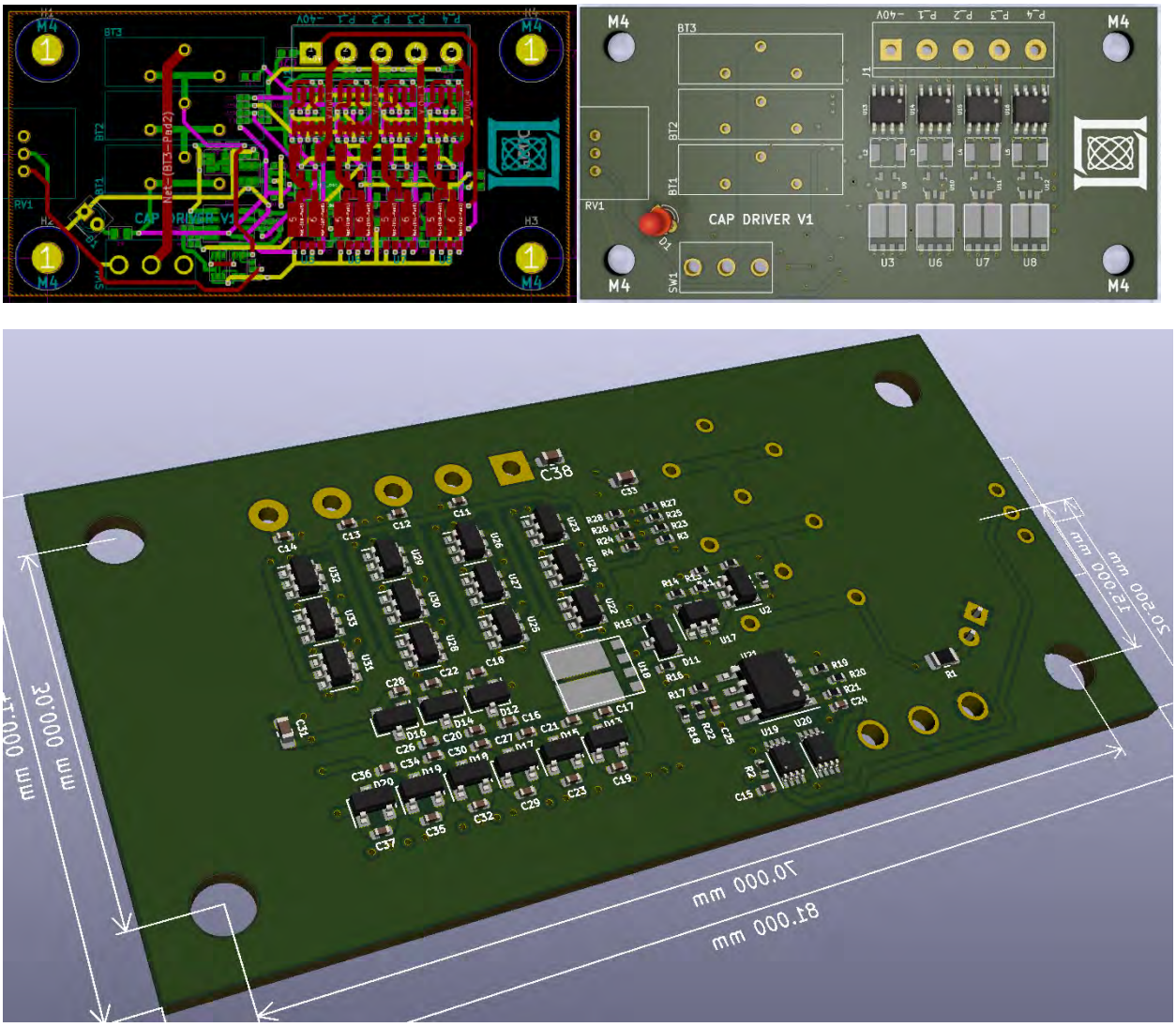


*Figure 7. Board layout for the microhydraulic driver circuit with inductive energy recovery. The board is an 8x4 cm double-sided board with batteries, frequency control knob, and all the electronics required to produce a variable frequency microhydraulic actuation.*

The physical layout of the board is shown in Figure 7. It is double-sided and significantly bigger than the target cell size for digital material. However, it contains many of the components that are required for an electronic architecture of a digital material. Both components that would be in the master node, such as the battery and charge pump, as well as components that would be in the cell, such as timing generation and energy recovery circuit, are in the board.

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# 6. CONCLUSIONS

Digital material is a very interesting technology direction. The realization of a digital material system requires the proper architecture of all the components. In this study, we have investigated an architecture for a 1D string of cells, controlled by a master node. The physical architecture of the digital material would consist of a supporting backbone with power and data buses, an electronics module for driving the actuator, and the actuator itself. The electronics module would consist of a controller, a power driver or multiplexer, and optionally an encoder. The cell could recover capacitive energy by multistep charging and discharging of the actuator phases. The electronics module consists only of digital logic and power transistors, so it can be integrated in a DMOS/CMOS technology into a compact ASIC chip. It is possible that given the limited functional requirements of such a chip, it could be made at a 1x1 mm scale. This would enable a digital material string of approximately 2 mm in diameter.

In addition to the ASIC to make these systems technically feasible, the microhydraulic actuator technology needs to mature. Packaging and reliability development needs to take place to make the actuators a system-ready technology. Also rapid manufacturing of microhydraulic layers would need to be developed in order to fabricate the many actuators required for a digital material. Lastly, custom manufacturing techniques would need to be developed for assembling a digital material system; these could probably in large part borrow from pick-and-place methods used for circuit board manufacturing.

Another important consideration when deciding on how to move forward with this technology is the end use cases. While the overall concept is broad in potential applications, the architecture outlined here is just of a 1D digital material string. Even such a string could have potentially revolutionary applications. For example in the microrobotics area, a robotic snake could be designed and implemented with a very small diameter for ISR applications. 1D digital material could also form legs of small microrobotic systems, for insect like robots. In another area, medical robotics, thin narrow systems such as endoscopes are routinely used in diagnostics and surgery. 1D digital material systems could provide a new and much more capable way of designing endoscopic diagnostic and surgical tools. Finally, 1D digital material systems could function as deployment components for microsystems that need to unpackage themselves.

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# APPENDIX A

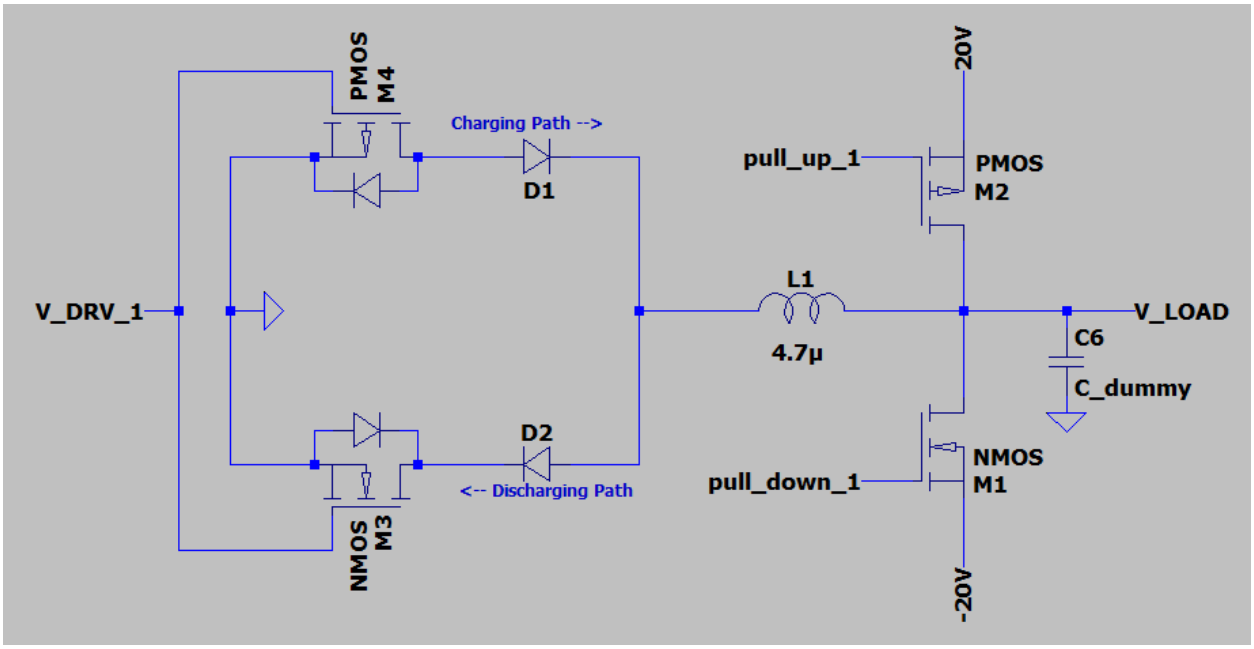
Sub circuit descriptions for the microhydraulic actuator driver circuit with inductive energy recovery.

This system is split into 4 individual sub-circuits. They are as follows:

- Charge Pump/Voltage Multiplier
- 4-Phase Generator
- Gate signal Generator
- Capacitive Driver

The capacitive driver is the most important part of the system and will be the first section of this documentation. The charge pump serves an almost equally important but definitively less glamorous role and its documentation will follow the driver's. Lastly, the 4-phase generator and gate signal generator serve to integrate all 4 phases of this system and will be discussed last.

## Capacitive Driver

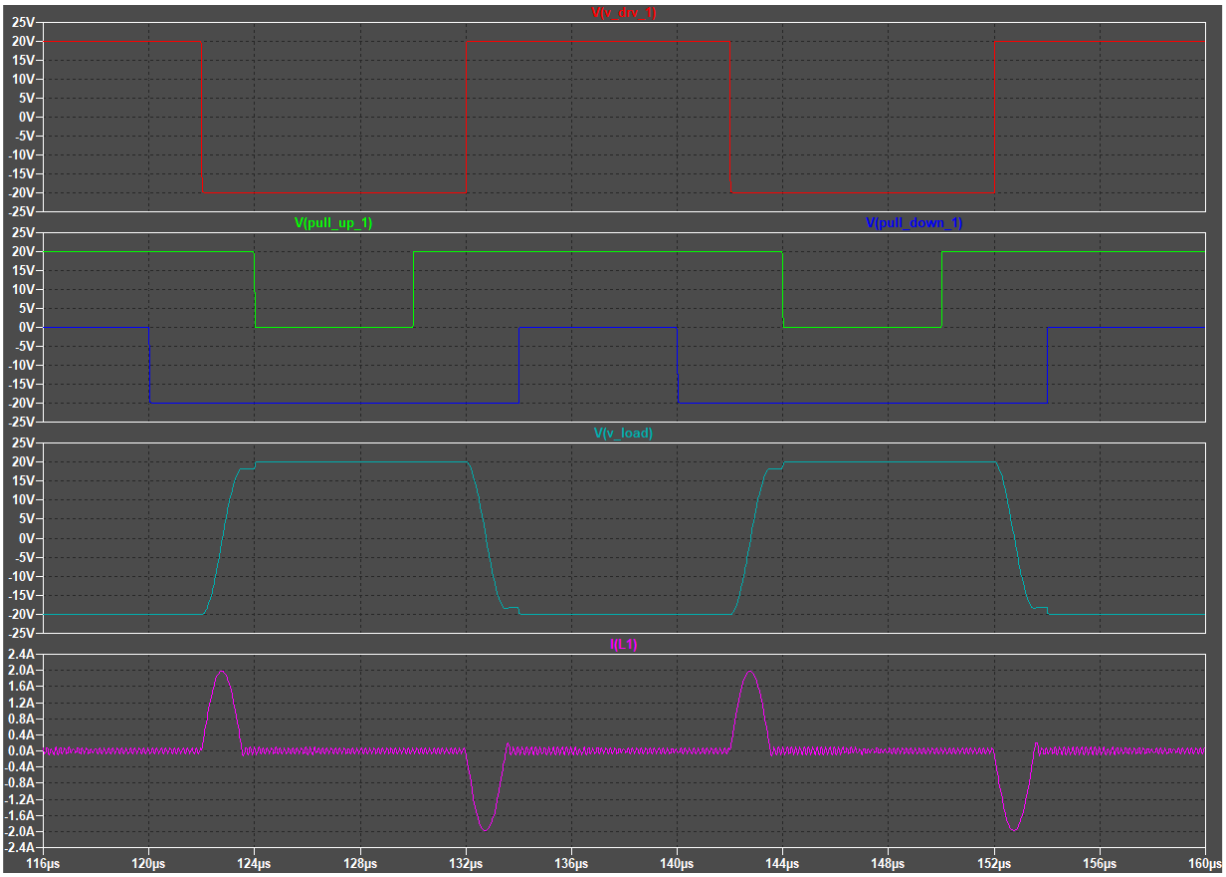


The schematic above is for a single phase of the capacitive drivers. In total, there are 4 of these capacitive drivers, each 90 degrees out of phase from one another. For the sake of simplicity, consider the circuit in its ideal sense. When V_DRV_1 goes high, NMOS M3 turns on and PMOS M4 turns off. The initial state of C_dummy is charged to +20V (C_dummy represents the capacitive load of the actuator). When M3 turns on, current drains out of this capacitance, through L1, D2, and M3 to ground. Inductor L1 charges. Inductor L1 stops charging when V_load = 0. The energy stored in L1 (equal to half of the total energy stored in C_dummy) begins draining, forcing the current to keep flowing from V_load through L1, D2, M3, to ground. When inductor L1 has drained all its stored energy, current ceases to flow, V_load equals a -20V, and diode D2 blocks current from flowing in the opposite direction. In this manner, the polarity of C_dummy is switched without losing any energy (ideally).

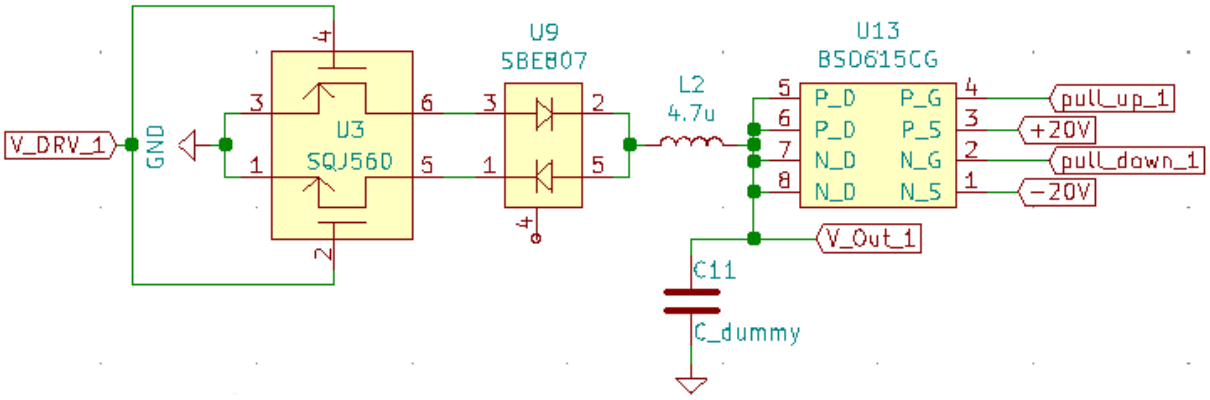
A similar process happens when V_DRV_1 goes low. At this point, the intial state of C_dummy is discharged to -20V, NMOS M3 turns off and PMOS M4 turns off. When M4 turns on, current flows from ground through M4, D1, L1 and into C_dummy. Inductor L1 charges and stops charging when V_load = 0. The energy stored in L1 then begins draining, again forcing the current to keep flowing from ground through M4, D1, L1, into C_dummy. When all the energy is drained out of L1, current ceases to flow, V_load = 20V, and diode D1 blocks current from flowing in the opposite direction. The polarity of C_dummy has again been switched without spending any energy (again, ideally).

In the non-ideal sense, however, switching the polarity of C_dummy will require spending some energy. M3 and M4 have non-zero on-resistances, L1 had a DC resistance component, and D1 and D2 have forward voltage drops. This has the effect of burning energy during switching events. So V_LOAD will not go from 20V to -20V or -20V to 20V, but rather 20V to >-20V or -20V to <20V, respectively. This necessitates the inclusion of PMOS M2 and NMOS M1.

During positive switching events (V_DRV_1 low and current flows into C_dummy) PMOS M2 turns on after the energy has finished draining from L1. This brings V_LOAD from some value <20V to 20V. During negative switching events (V_DRV_1 high and current flows out of C_dummy) NMOS M1 turns on after the energy has finished draining from L1. This brings V_load from some value >-20V to -20V. The timing of M1 and M2 is controlled by the gate signal generator (a separate system) and works in conjunction with the timing of V_DRV_1.




The timing of the switching can be more clearly seen in the above LTSpice simulation with real components. The inductor causes the load voltage to swing to slightly above -20V or slightly below +20V. Once the current through the inductors ceases, the pull up or pull down transistors turn on (depending on the state of the circuit). When V_DRV_1 is high, the output load voltage is low and vice versa.




Component selection is as follows: The driver NFET + PFET (previously M3 and M4, respectively) are an SQJ560 (NFET + PFET in a single package). The on resistance will affect the amount of charge that gets recovered from the load capacitance during switching events, so low on resistance was a top priority. Unfortunately, low on-resistance typically comes at the cost of high gate capacitance, so a compromise had to be made. The SQJ560 was chosen for its small physical size and low on resistance (within a given range of allowable gate capacitance).

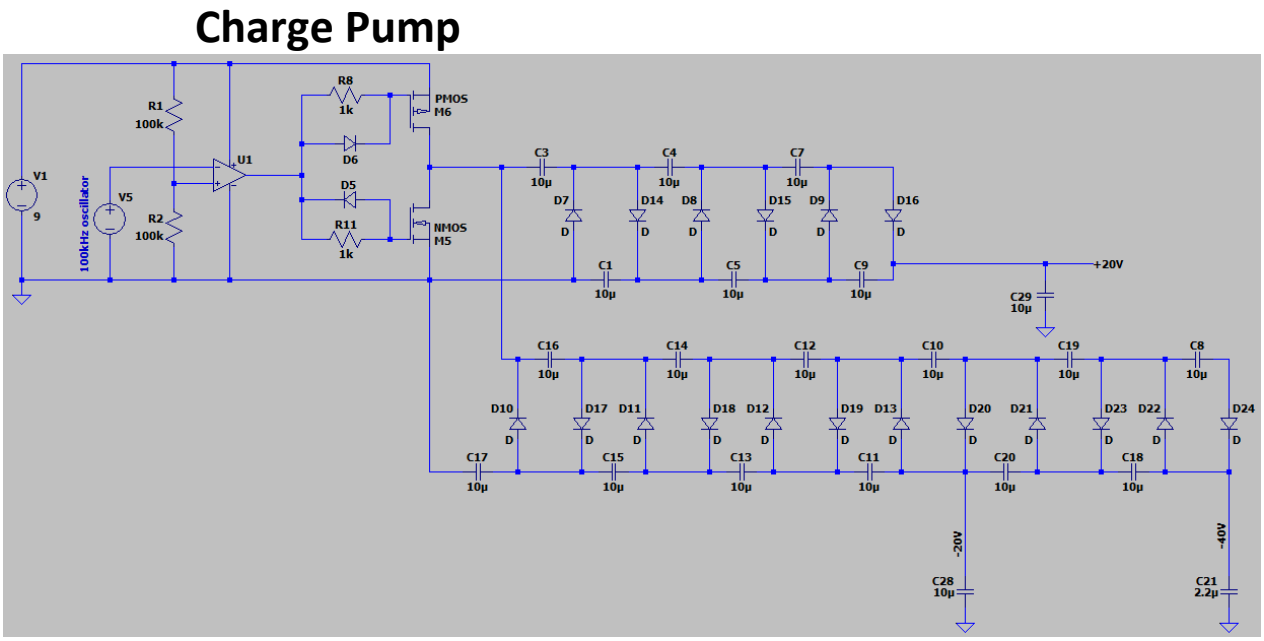
The blocking diodes (previously D1 and D2) are a SBE807 dual diode package. Again, the forward voltage drop of this diode directly effects the amount of charge that can be recovered from the load capacitance, so low forward voltage drop schottky diodes were used. SBE807s were chosen were chosen for their small size, low forward voltage drop, and peak current handling capability.

The on resistance of the pull up and pull down transistors does not affect the energy consumption of the circuit. Half the of the energy spent charging up the load capacitance will be dissipated during charging regardless of the resistance it is being charged through. Low gate capacitance and small physical size were prioritized when choosing these transistors. A BSO615CG was picked to fulfill these criteria.

| Capacitance | .5CV^2 | 2*(.5CV^2) | 1uH .014ohm | | | 3uH .035ohm | | | 5uH .034ohm | | | 10u .077ohm | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Positive Supply (mA) | Negative Supply (mA) | **Total Watts** | Positive Supply (mA) | Negative Supply (mA) | **Total Watts** | Positive Supply (mA) | Negative Supply (mA) | **Total Watts** | Positive Supply (mA) | Negative Supply (mA) | **Total Watts** |
| 0p | 0mW | 0mW | 0.067 | 0.049 | **0.004176** | 0.065 | 0.047 | **0.004032** | 0.05 | 0.045 | **0.00342** | 0.055 | 0.052 | **0.003852** |
| 10p | .026mW | .052mW | 0.067 | 0.051 | **0.004248** | 0.065 | 0.053 | **0.004248** | 0.05 | 0.05 | **0.0036** | 0.053 | 0.053 | **0.003816** |
| 100p | .26mW | .52mW | 0.07 | 0.052 | **0.004392** | 0.06 | 0.085 | **0.00522** | 0.051 | 0.083 | **0.004824** | 0.062 | 0.055 | **0.004212** |
| 1n | 2.6mW | 5.2mW | 0.082 | 0.081 | **0.005868** | 0.066 | 0.088 | **0.005544** | 0.059 | 0.088 | **0.005292** | 0.06 | 0.088 | **0.005328** |
| 10n | 26mW | 52mW | 0.227 | 0.472 | **0.025164** | 0.175 | 0.472 | **0.023292** | 0.168 | 0.475 | **0.023148** | 0.202 | 0.451 | **0.023508** |
| 100n | 260mW | 520mW | 1.395 | 4.25 | **0.20322** | 1.124 | 3.35 | **0.161064** | 1.065 | 2.81 | **0.1395** | 1.34 | 2.14 | **0.12528** |
| 1u | 2.6W | 5.2W | 26.1 | 35 | **2.1996** | 17 | 25.5 | **1.53** | 15.4 | 21 | **1.3104** | 13.5 | 16.1 | **1.0656** |
| 10u | 26W | 52W | 200 | 250 | **16.2** | 165 | 205 | **13.32** | 160 | 200 | **12.96** | 116 | 160 | **9.936** |

The Inductor was sized using both qualitative and quantitative methods. Quantitatively, the inductor must be able to store at least the energy stored in the load capacitance. A relationship between the

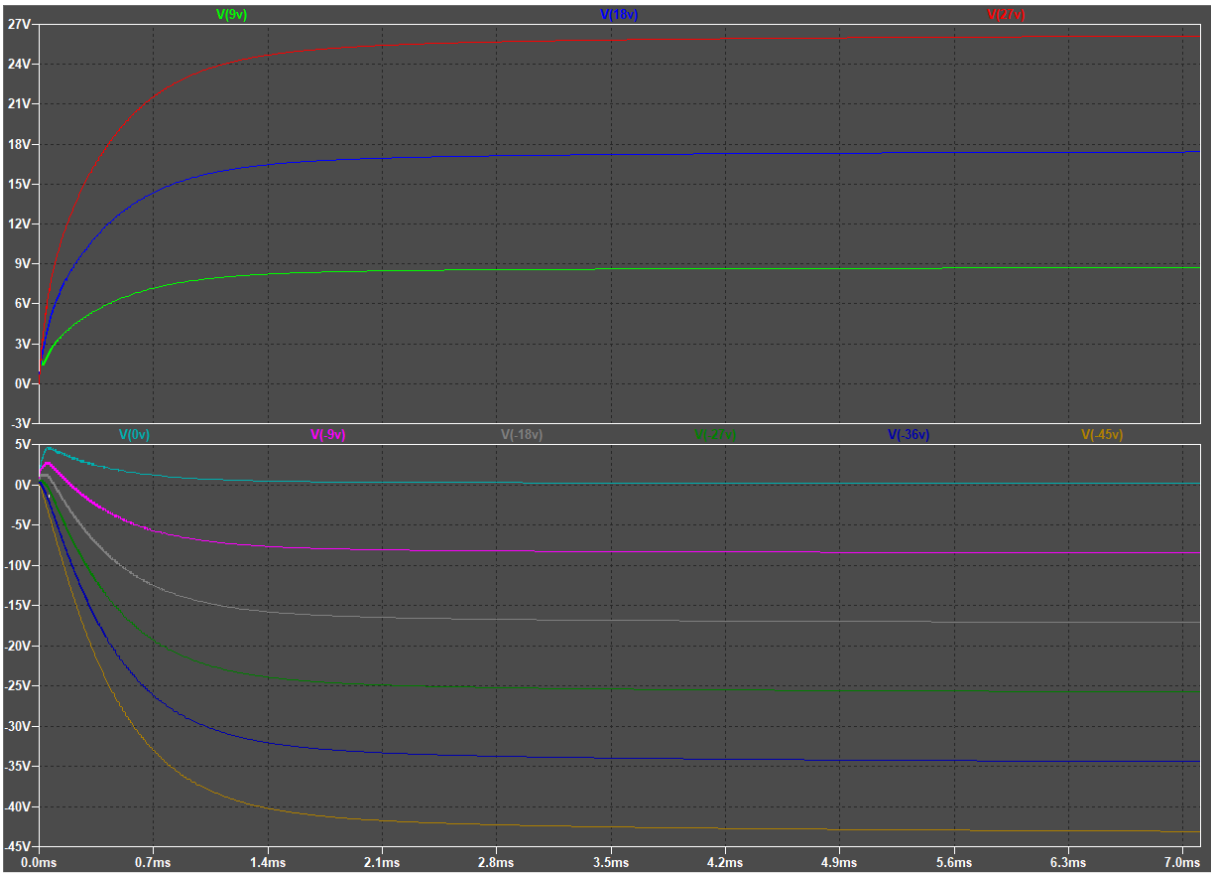
inductance and saturation current of the inductor can be found from this value. The inductance also effects the rate the voltage across the load capacitance will change during switching events. Because the load capacitance is variable and the inductance is not, the inductor must be suitable for a range of load capacitances. An inductor with an inductance of 4.7uH and a saturation current of 4A was chosen (BOURNS SRP4020TA).



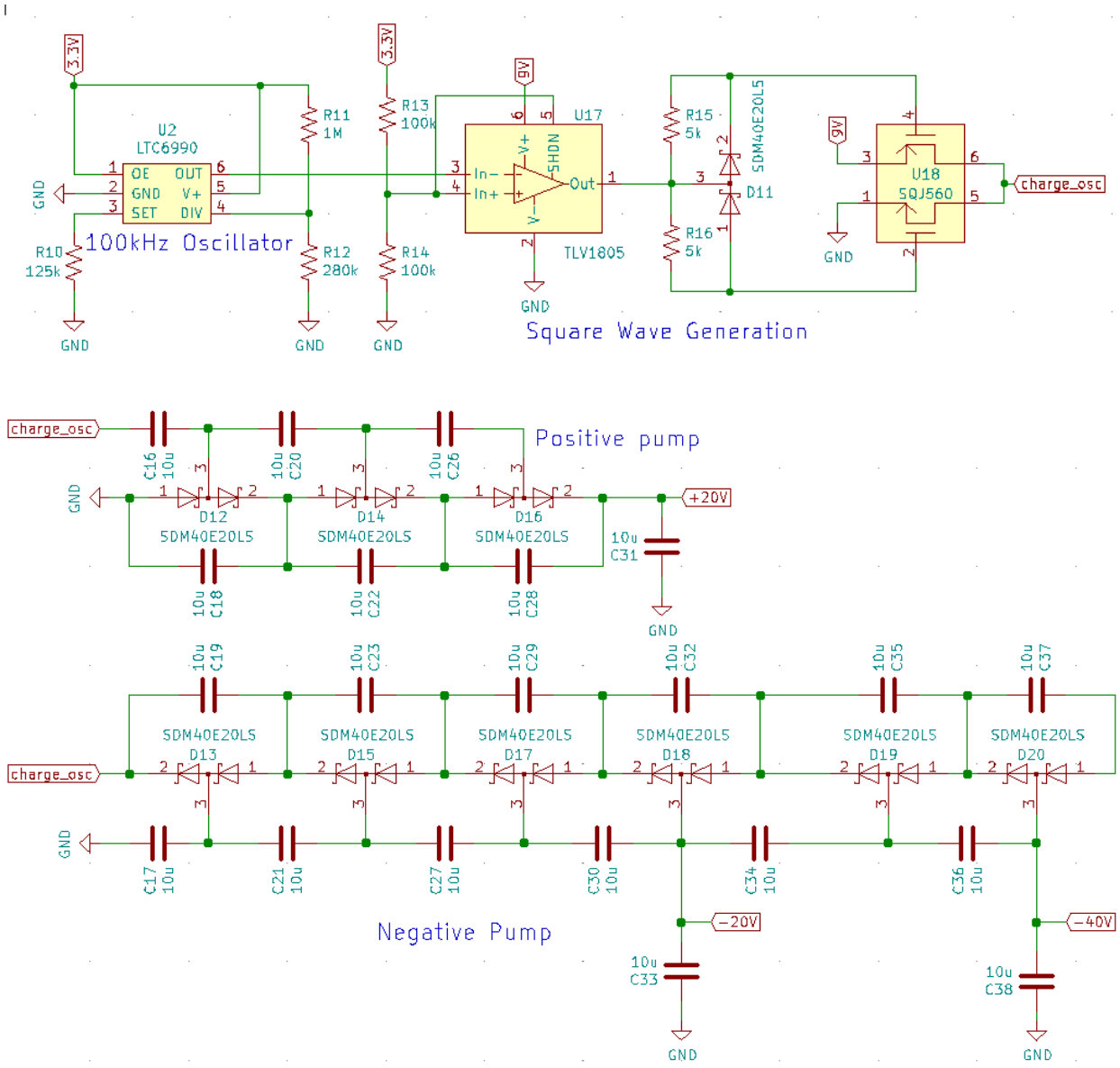

The charge pump can be effectively split into 2 components: The voltage multiplier and the square wave generator. The square wave generator consists of an IC oscillator, a comparator, and a CMOS inverter. The oscillator provides the initial signal. The comparator turns it into a clean square wave and provides a lower output impedance to drive the gates of the CMOS inverter. The CMOS inverter provides an output impedance low enough to drive the voltage multipliers.

There are two voltage multipliers that are driven by the same square wave, one to generate the positive voltage and another to generate the negative voltages. They are both Cockcroft–Walton topology multipliers. The positive multiplier is three stages, which ideally would result in an output voltage of 27V (3 times the input voltage of 9V). However, due to the chain of diodes with each a non-zero forward voltage, the no-load output voltage is closer to 25V. Loading from the driver circuitry will bring this value down further.

The negative voltage multiplier is the same type of topology as the positive voltage multiplier, just with more stages and two outputs (one for -20V and another for -40V). The voltages between stages can be seen in the following plot:




These voltages are taken without any output load. Smoothing capacitors are placed at each output node to ensure the (spikey) current draw of the drivers does not cause substantial voltage droop. The charge pump is not regulated and therefore the exact output voltages will depend on the (variable) load capacitance.

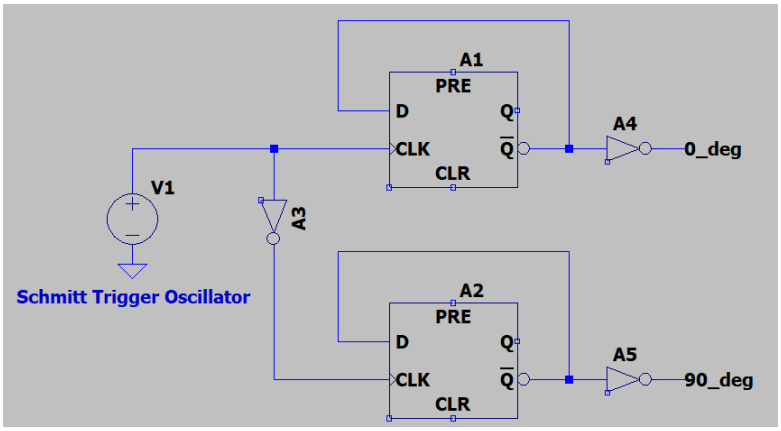



The final schematic for the charge pump can be seen above. An LTC6990 IC oscillator was chosen for both its small size and low power. It is set to oscillate at 100kHz to maximize the potential power output of the charge pump vs. switching losses. Higher frequencies will allow the charge pump to output more current, but it will also increase the switching loss. The frequency can be adjusted with R10, R11, and R12. A TLV1805 comparator was chosen as it has a push-pull output (as opposed to an open drain output) which will be better suited for driving the gates of the following inverter stage. R16, R15, and D11 are included between the output of the comparator and the gates of the inverter to produce dead time during switching. This is in an effort to eliminate shoot-through occurring in the inverter stage.

SQJ560 dual NFET+PFET IC was chosen for the inverter for the same reason it was chosen in the driver section (Low on resistance in conjunction with a reasonable gate capacitance).

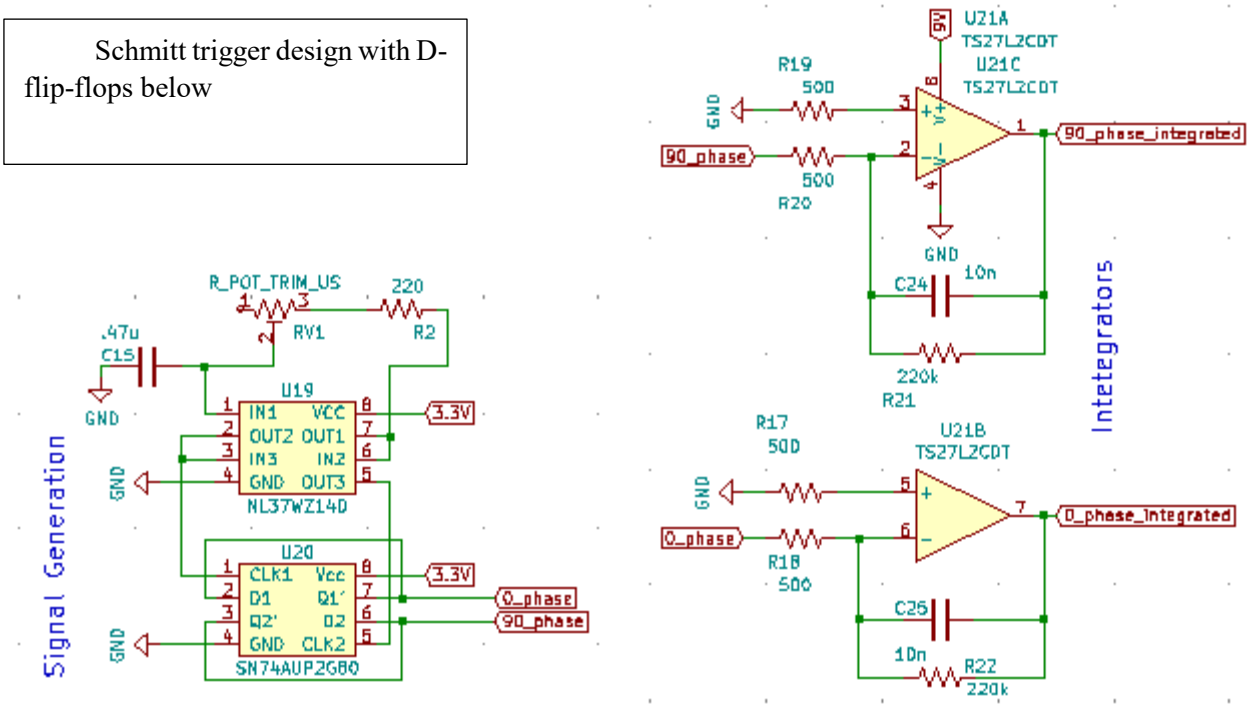
The efficiency of the charge pump is highly dependent on the IV characteristic of the diodes. SDM40E20LS diodes were chosen for their small package and low forward voltage. 10uF charge pump capacitors were chosen as they are the largest commonly available 0402 package 10V capacitors. 10uF and 2uF smoothing capacitors were chosen for the same reason but for 0603 package at 25V and 50V, respectively.

## Four Phase Generator




The four phase generator creates two square waves with a 90 degree phase difference. The other two phases are derived from these two phases as inverses. A Schmitt trigger oscillator operating at twice the desired frequency serves as the input to the circuit. The input signal gets split into two signals, and then one of those signal gets inverted. Those two signals get fed into the clock input of two separate D-flip-flops. Because the output state of a D-flip-flop in this configuration changes (flips) on the rising edge of the clock signal, two 50% duty cycle square waves that are 90 degrees out of phase with eachother and one half of the input frequency are produced. The signal is then buffered with an inverter. The operation of this circuit is more clear in the following picture:

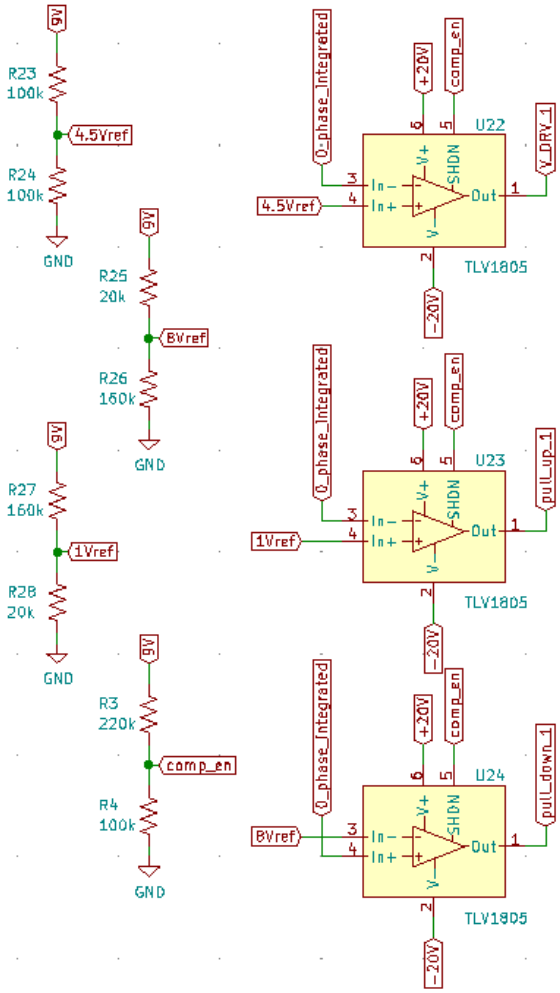
Schmitt trigger design with D-flip-flops below




The two signals that are 90 degrees out of phase with one another are then integrated in an opamp with an integration constant of .5uS. This turns the square wave into a waveform that is more trapezoidal, which becomes useful in the gate signal generation component of this system.

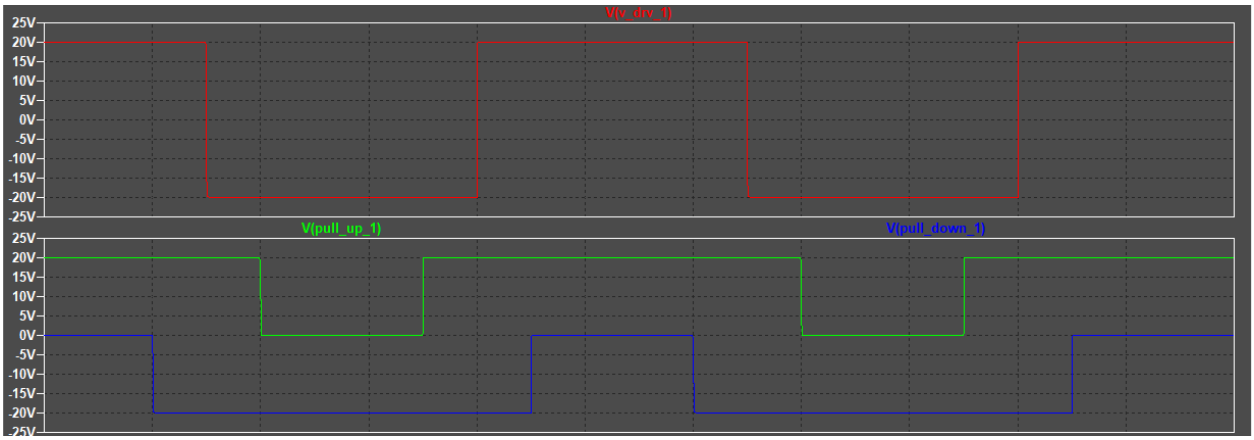
An NL37WZ14 triple schmitt inverter was chosen for the schmitt trigger oscillator as well as the two inverters used in the d-flip flop frequency divider/90 degree phase generator. This IC was used as it is low power and has three inverters in a single package. An SN74AUP2G80 was chosen for a similar reason as it is low power IC that contains two D-flip-flops (with only the necessary inputs and outputs) in a single package. TS27L2CDT opamp was used for integration as it, at these frequencies, will not require external stabilization, has two opamps in a single package, and is a low power device. An integration constant of 5uS was chosen as it allows the output of the integrators to remain a trapezoidal shape (as opposed to turning into a triangle wave at high frequencies).

# Gate Signal Generator

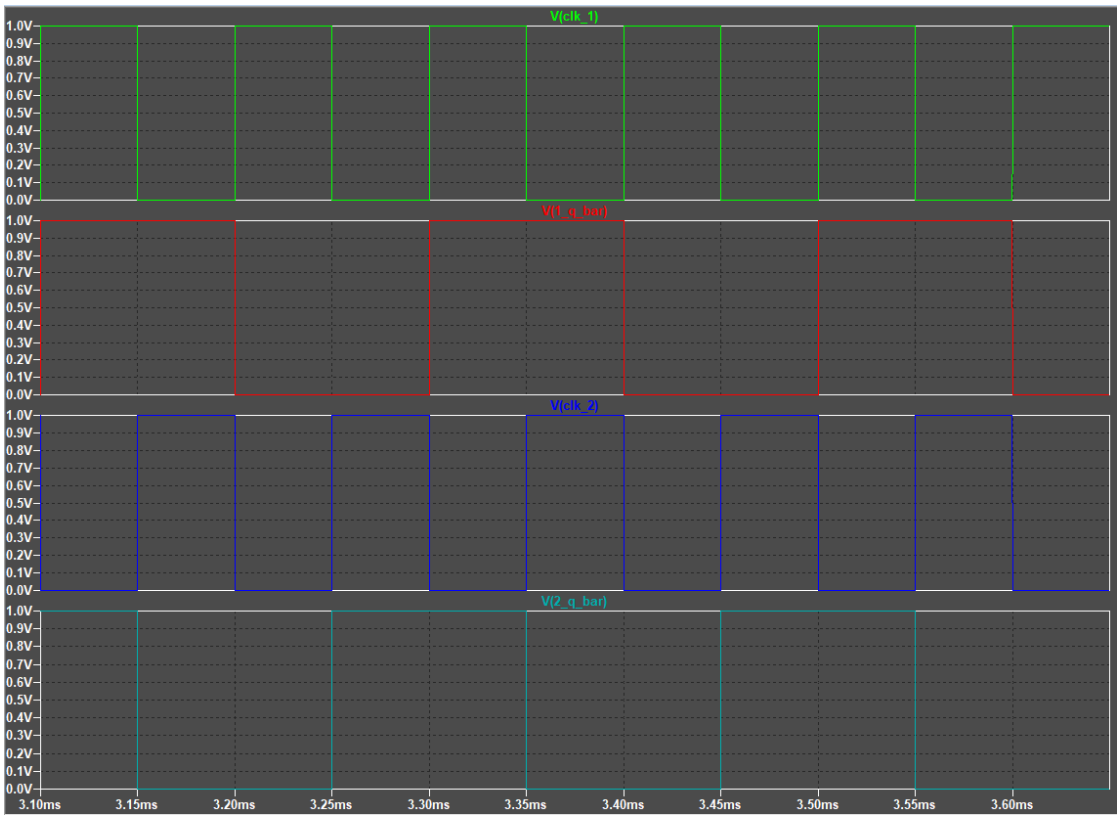



The gate signal generators for a single phase can be seen in the above picture. The two integrated 90 degree out of phase signals created in the previous stage (four stage generator) are fed into this group of comparators.

Each phase needs three signals to be generated: one for the pair of driver FETs (M3 and M4 in the capacitive driver section), one for the pull-up FET, and one for the pull-down FET. Three comparators are required to generate these signals from a single integrated signal created in the previous stage. The timing of each of these signals is dependant on the threshold of the comparator and the rise/fall rate of the integrated signal.




The output of the comparators for one phase can be seen in the above picture. TLV1805 comparators were chosen for the push-pull output which will provide an efficient low impedance node to drive MOSFET gates. Threshold levels were set in conjunction with the switching time (determined by the value of the inductor in the driver), the ramp rate (determined by the integration rate of the integrators), and the maximum desired phase frequency (5kHz).




In the above picture it can be seen that the two output signals are 90 degrees out of phase with each other and are half of the frequency of the input clock sequence. The two signals then get split into 4 signals, each 90 degrees out of phase with the next, in the signal generation circuit of this system.