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Major Goals: The goal of this ARO-funded research program was to develop the necessary infrastructure to enable a new class of modulators based on the hybrid silicon-graphene (HSG) material platform. Taking advantage of the high carrier mobility and the strong plasma dispersion effect of graphene combined with strong light confinement in compact Si-photonic devices, this program was aimed at developing a novel material and device platform, which can enable modulators with modulation speeds reaching 100 Gb/s and sub-100 fJ/bit energy consumption.

Accomplishments: During the past 12 months, we developed several approaches to overcome the relative high sheet resistance of undoped graphene. We integrate ion liquid assisted gating mechanism into our device and demonstrate reduced resistance through electric double layer structure. With electro-chemical doping, we significantly reduced the graphene resistance (~5 time), which enables high speed modulation above 25 GHz. To overcome the high loss of graphene and to achieve low-power modulation, we investigated two approaches for fabricating of ultra-high Q devices integrated with 1) graphene and 2) two-dimensional tungsten disulfide (WS2) as an alternative for giant electro-refractive modulation. We demonstrated ultra-high quality (Q) factor (~8M loaded Q) with a newly optimized etching recipe with flowable oxide (FOX) as negative resist mask. We also show integration of WS2 onto high Q cavity with a relative low reduction in Q factor (from 2M to 300k). We also developed a method for planarization of SiO2 on patterned SiN sample using our recently installed commercial CMP machine to make our platform suitable for 2D material integration. We developed a recipe that works effectively for oxide-stop-on-nitride, which allow us to have a sample with “flat” surface for crack-free 2D material integration.
More recently, we integrate ion liquid on microdisk resonators fabricated on SOI to demonstrate the feasibility of ion liquid assisted gating on integrated photonic devices. We also reoptimize our Flowable Oxide (FOx) planarization technique on SiN platform to achieve near perfect platform for crack-free graphene integrating while CMP approach is under aggressive development. A final approach would be using FOx as the initial seeding layer for PECVD oxide followed by CMP polishing to guarantee both flatness and smoothness. Finally, we optimized the design of ohmic contacts for our graphene/Si device to further reduce the contact resistance to achieve a better trade-off between resistance (speed) and insertion-loss.

Training Opportunities: Nothing to Report

Results Dissemination: The result of this research has been presented in several conferences and invited talks. Several manuscripts for publication in refereed journals are submitted or are in preparation.

Conference contributed presentations:
[1] T. Fan, H. Taghinejad, A. H. Hosseinnia, H. Moradinejad, A. A. Eftekhar, and A. Adibi, “A high-quality silicon nitride (SiN) platform integrated with two-dimensional (2D) materials”, Photonics West, San Francisco, CA, January 2019.
[2] T. Fan, A. H. Hosseinnia, H. Moradinejad, A. A. Eftekhar, and A. Adibi, “Hybrid h-BN/Graphene/h-BN Silicon Device for Electro-optic Modulation,” CLEO: QELS_Fundamental Science, JTh2A. 78
[3] T. Fan, A. H. Hosseinnia, H. Moradinejad, A. A. Eftekhar, and A. Adibi, “Hybrid graphene modulator on CMOS platform for integrated photonic applications,” Photonics West, San Francisco, CA, January 2018.

Invited talks:
[1] A. H. Hosseinnia, M. Sodagar, H. Moradinejad, T. Fan, A. A. Eftekhar, and A. Adibi “Hybrid Material Platforms for Reconfigurable Integrated Nanophotonics,” Invited for Presentation in Stegeman Symposium, Orlando, FL, March 2018.
[2] A. A. Eftekhar, A. H. Hosseinnia, H. Moradinejad, T. Fan, S. Taghavi, M. Sodagar, R. Dehghannasiri, and A. Adibi, “Hybrid Material Platforms for Low-power, High-speed, and Miniaturized Integrated Nanophotonic Devices and Systems,” Invited Keynote Talk for Presentation in Optics and Photonics Conference, Philadelphia, PA, September 2018.
[3] A. H. Hosseinnia, M. Sodagar, H. Moradinejad, T. Fan, A. A. Eftekhar, and A. Adibi, “Can Hybrid Materials Replace Silicon? Nano-photonics and the Optical Path to the Future,” Invited Seminar Presentation in Samsung, San Jose, CA, October 2018.
[4] A. H. Hosseinnia, T. Fan, H. Maoradinejad, M. Sodagar, S. Taghavi, A. A. Eftekhar, and A. Adibi, “Low-power High-speed Resonance-based Integrated Photonic Modulators,” Invited for Presentation in IEEE Photonic Conference, Reston, VA, October 2018.

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RPPR Final Report

as of 07-Jan-2020

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Compact, Low-Power, and High-Speed Graphene-Based Integrated Photonic Modulator Technology

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I. Introduction

This Final report summarizes achievements in Dr. Adibi's research group at Georgia Institute of Technology in the area of "Compact, Low-Power, and High-Speed Graphene-Based Integrated Photonic Modulator Technology", supported by award grant number W911NF-18-1-0142 since March 14th, 2018. Major achievements with detailed descriptions are listed in this report. The focus of this report is on the 12-month achievements of the program while some supportive results that have been reported in previous annual reports are briefly included.

This ARO-supported program started on March 14, 2018 and was directed toward developing a hybrid integrated photonic platform for realization of high-speed and low-power optical modulators based on integration of graphene with CMOS-compatible substrates.

Optical interconnects are poised to replace metallic wires in short-range communications networks at different levels, including board-to-board communications between different processing units in computer clusters, chip-to-chip communications on electronic board between different processors and memory units, and even intra-chip between different processing cores. With the ever-increasing need for higher computation power and higher data rates, the dissipated heat due to the interconnection network has become one of the main challenges and facing the advancement of the current processing systems. Optical interconnection is the most promising solution that can mitigate this challenge by enabling broadband and low-power communication networks. However, to realize such solution, especially for intra-chip interconnect networks, there is an urgent need for a new optical communication subsystem/device technology to achieve these data rates at very low power consumption to avoid any energy dilemma. One of the main building blocks of such systems is a high-speed and low-power optical modulator. Current modulation technologies such as directly-modulated lasers (e.g. VCSELs) and silicon photonic modulators based on carrier dispersion (e.g., PN-junction-based modulators) face several limitations in delivering the stringent system requirements of next-generation optical interconnects in terms of speed and power consumption. The goal of this ARO-funded research program was to develop the necessary infrastructure to enable a new class of modulators based on the hybrid silicon-graphene (HSG) material platform. Taking advantage of the high carrier mobility and the strong plasma dispersion effect of graphene combined with strong light confinement in compact Si-photonic devices, this program was aimed at developing a novel material and device platform, which can enable modulators with modulation speeds reaching 100 Gb/s and sub-100 fJ/bit energy consumption. These target modulator performance measures surpass the existing on-chip modulating solutions in terms of modulation speed while enabling five times less power consumption than the best-reported Si-photonic modulators for similar speeds.

During the previous period of this research, we developed two major graphene-based integrated nanophotonics material platforms with very high quality based on: 1) integration of single layer graphene with silicon on isolator (SOI) namely graphene-on-Si (GoS), and 2) integration of double-layer graphene on silicon nitride (SiN), namely graphene on SiN (GoN). While the first platform enables to achieve low-power modulator devices with specifications that considerably surpass those of Si-photonic modulators,

the second platform enables high-performance modulators in the SiN platform that lacks any modulation mechanism otherwise.

In realization of the proposed high-performance modulators several major challenges in different aspects of the process had to be addressed. The first challenge is to achieve high conductivity graphene by effective doping of the graphene to achieve low modulator resistance and high modulation speed. The second challenge is to overcome minimize of the optical loss of the graphene, to preserve the high Q of the modulator resonator for better modulation voltage efficiency. The last challenge is to achieve a reliable and high-yield fabrication process for graphene modulators, which requires planarizing the die/wafer surface before the graphene transfer process to minimize the probability of cracking of 2D materials during the device fabrication process.

To address the above-mentioned issues, we develop several approaches during the past 12 months. To overcome the relative high sheet resistance of undoped graphene, we integrate ion liquid assisted gating mechanism into our device and demonstrate reduced resistance through electric double layer structure. With electro-chemical doping, we significantly reduced the graphene resistance (~5 time), which enables high speed modulation above 25 GHz. To overcome the high loss of graphene and to achieve low-power modulation, we investigated two approaches for fabricating of ultra-high Q devices integrated with 1) graphene and 2) two-dimensional tungsten disulfide (WS2) as an alternative for giant electro-refractive modulation. We demonstrated ultra-high quality (Q) factor (~8M loaded Q) with a newly optimized etching recipe with flowable oxide (FOX) as negative resist mask. We also show integration of WS2 onto high Q cavity with a relative low reduction in Q factor (from 2M to 300k). We also developed a method for planarization of SiO_2 on patterned SiN sample using our recently installed commercial CMP machine to make our platform suitable for 2D material integration. We developed a recipe that works effectively for oxide-stop-on-nitride, which allow us to have a sample with “flat” surface for crack-free 2D material integration.

More recently, we integrate ion liquid on microdisk resonators fabricated on SOI to demonstrate the feasibility of ion liquid assisted gating on integrated photonic devices. We also reoptimize our Flowable Oxide (FOx) planarization technique on SiN platform to achieve near perfect platform for crack-free graphene integrating while CMP approach is under aggressive development. A final approach would be using FOx as the initial seeding layer for PECVD oxide followed by CMP polishing to guarantee both flatness and smoothness. Finally, we optimized the design of ohmic contacts for our graphene/Si device to further reduce the contact resistance to achieve a better trade-off between resistance (speed) and insertion-loss.

Our recent developments resolve several important challenges facing the development of high-speed and low power modulators in graphene and helps to further push graphene-based integrated photonic modulators as a viable solution for next-generation low-power, and high-speed interconnect solutions.

II. Research Accomplishments

In this section we briefly review our research progress in different areas. More details will be available upon request.

II.1. Ion liquid assisted gating mechanism for resistance reduction of graphene

Ionic liquids are highly polar binary salts with low melting temperatures. It is a dielectric material with high dielectric constant and could be used as gate dielectric material to electrostatically dope other materials. By applying few volts of potentials, it is possible to tune ionic liquids continuously through their phase diagram to provide efficient change of the doping level [1]. Ionic liquid has been widely used in Electric Double Layer (EDL) devices [2]. Such device is a powerful tool to tune interfacial band bending (perpendicular electric field) and the Fermi level of channel material over a wide range [3-5].

We use N,N-diethyl-N-methyl-N-(2-methoxyethyl)ammonium bis(trifluoromethanesulfonyl)imide (DEME-TFSI) as ionic liquid, which is a commonly-used ionic liquid dielectric with large electrochemical potential as well as a low glass transition temperature (182K) [6,7]. We will cover the graphene modulator with DEME-TFSI and apply voltage between the graphene layer and electrode in contact with ionic liquid to electro-chemically-dope the graphene and achieve super-low sheet resistance. Here we detail the develop fabrication process and the characterization results.

II.1.1. Fabrication process

To characterize the conductivity (i.e., sheet resistance) of the Graphene sample upon electro-chemical doping, we transfer a mono-layer graphene on the oxide substrate, integrate ohmic contacts with graphene, and cover it with ionic-liquid (Fig. 1 and Fig. 2). We start with a monolayer graphene on copper foil grown by chemical vapor deposition (CVD) method (ACS materials). We cut graphene/copper sample into piece of approximately one inch by one inch (~1" x 1") with a razor blade. Next, we tape the piece on a clean glass slide. Then we spin coat PMMA (A6 M_w ~950k from Micro Chem) at 3000 rpm for 60 sec. It gives us a protective layer on graphene with a thickness about 500 nm. We wait overnight (> 12 hours) for PMMA to dry. After PMMA becomes dry, we remove the tape, take the graphene/copper sample out of the glass slide, and tape it upside down on a new glass slide. We expose the slide to oxygen plasma for 5 min in a reactive ion etching (RIE) chamber to remove the backside graphene. After RIE, we remove the tape and put the graphene/copper sample in the Marble's reagent ($CuSO_4$/HCl/H_2O: 10 g/50 mL/50 mL) overnight to etch the backside copper substrate. After substrate being etched away, graphene film with protective layer is floating on the surface of Marble's reagent. We use a clean glass slide to fish it to DI water bath to remove the unwanted ions. Finally, we use our target substrate (hard substrate like silicon, metal, etc. or flexible substrate like PDMS, plastic, etc.) to fish the graphene film and let the water dry overnight. In this specific case we transfer graphene onto 280 nm

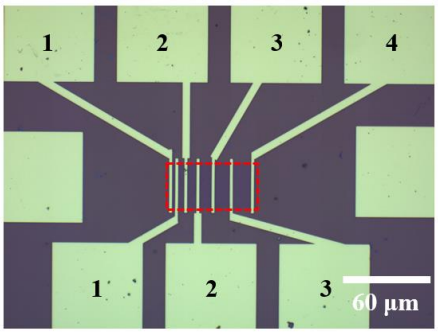

Fig. 1. Device for characterizing graphene sheet resistance. Region marked with red color is a single layer graphene sheet.

SiO_2/Si substrate. We bake the dry sample at 100 °C for 5 minutes and put it in an Acetone bath overnight to remove the PMMA layer.

After transferring graphene onto SiO_2, we do a first step electron beam lithography with PMMA to lift off contacts on top of graphene layer. The ohmic contact is based on the deposition of a metal stack of 1.5 nm titanium (Ti), 45 nm palladium (pd), and 15 nm gold (Au), which is shown to provide a low resistance ohmic contact. The graphene layer is then patterned through a second step of EBL with PMMA followed by a short oxygen plasma descum (in a RIE chamber). The final fabricated device is shown in Fig. 1 and Fig. 2.

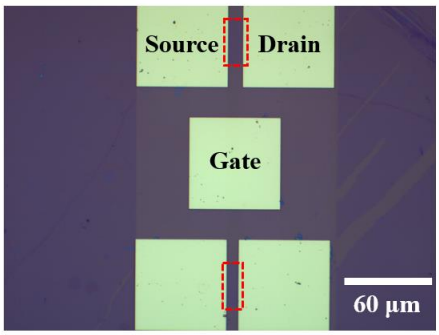

Fig. 2. Device for characterizing graphene sheet resistance with ion liquid assisted gating. Region marked with red color is a single layer graphene

Figure 1 is a device with finger electrodes on top of graphene. The size of the graphene sheet is 30 µm x 60 µm. The width of the finger electrodes is 2 µm. The distance between pad 1 on the top and pad 1 on the bottom (Pad 1-1) is 2 µm. Similarly Pad 2-1, 2-2, 3-2, 3-3, and 4-3 have distance of 4 µm, 6 µm, 8 µm, 10 µm, and 12 µm, respectively.

Figure 2 depicts a device with source, drain, and gate electrodes, specifically designed for ion liquid assisted gating experiments. We have a series of devices with distances between pads similar to the distances in the device shown in Fig. 1.

II.1.2. Characterizing initial graphene resistance

We apply DC voltage between contacts of the device in Fig. 1 and measure the current. Fig. 3. Shows the I-V curve measured from different pads- pad 1-1 (top left), 2-1 (top right), 2-2 (mid left), 3-2 (mid right), 3-3 (bottom left), and 4-3 (bottom right).

We substrate the resistance from each sub-figure in Fig. 3

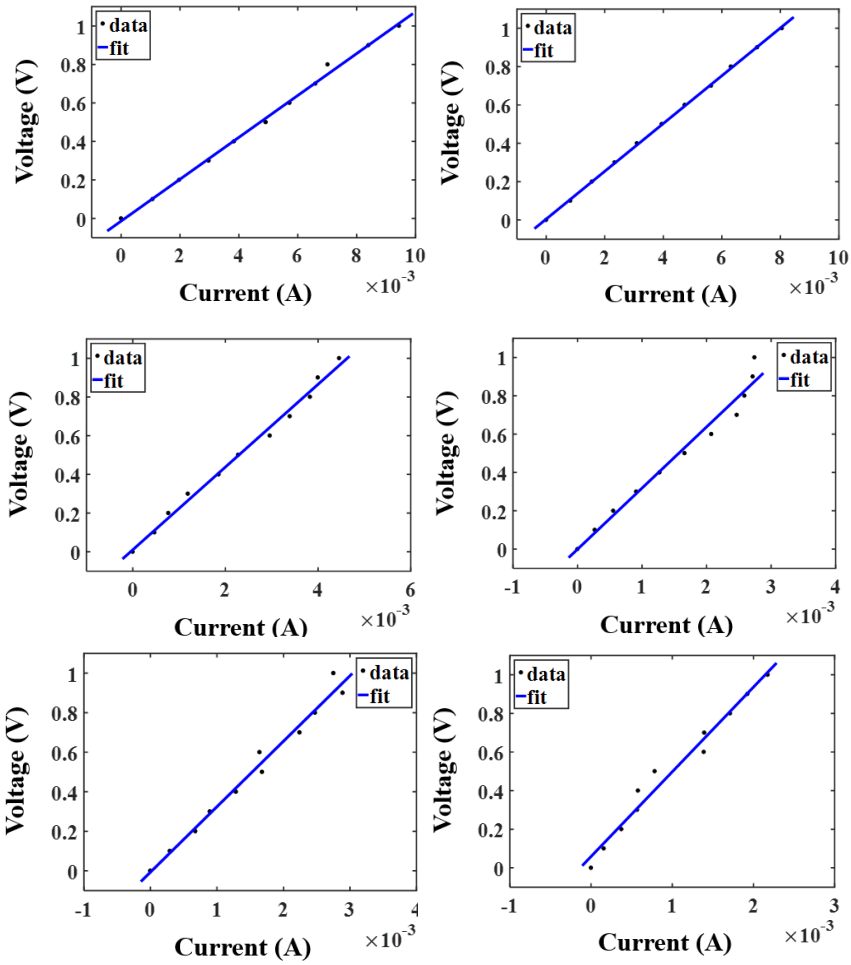

Fig. 3. I-V measurements between two consecutive finger-electrodes.

and plot the resistance versus the length of graphene between each pad, which leads us to Fig. 4. As it can be clearly seen from Fig. 4, the resistance has a linear relationship with the length of the graphene.

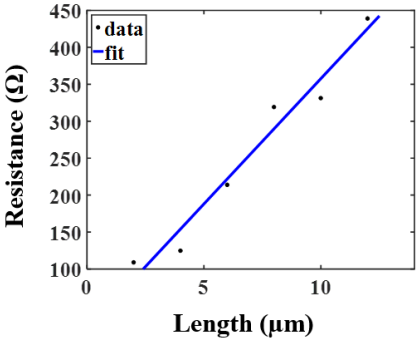

Fig. 4. Total resistance between two consecutive finger-electrodes vs. the length of the graphene between two consecutive finger-electrodes.

The total resistance of graphene (R_T) is determined by 2 parts, the sheet resistance (R_{SH}) and the contact resistance (R_{Sk}), as described by the equations below [8]

$$R_T = \frac{2R_{SK}L_T}{W} + \frac{R_{SH}L_X}{W},$$

$$L_T = \sqrt{\frac{\rho_c}{R_{SK}}},$$

where, W is the width of the graphene section, L_X is the gap between the contacts and L_T is the transfer length, which is defined as the distance over which the current drops to 1/e of the total current. From our measurements, we extract a sheet resistance R_{SH} = 33.93 X 30 = 1017.9 Ω/□, and a contact resistance of s R_{SK} = 18.52 ÷ 2 X 30 ÷ 0.5 = 555.6 Ω/□. Assuming L_T ~= 0.5 μm [8], the contact resistivity ρ_c = (2 X 0.25)^2 X 555.6 X (10^{-4})^2 = 1.3890e-06 Ω cm^2. The extracted sheet resistance and contact resistance are in-line with what has been previously reported for undoped (intentionally) CVD graphene.

II.1.3. Characterizing graphene resistance with Ion liquid assisted gating

We drop cast ion liquid on top of our device and wait it to dry for 12 hours. After 12 hour, the ion liquid gains more viscosity and does not move around on the surface of the sample. As seen from Fig. 5, a drop of ion liquid covers the surface of our devices. And we are probing into ion liquid to get contact with our devices. We measure a device with 4 μm graphene between contacts. Fig. 6 shows the I-V curve of the device. A resistance of ~300 Ω is extracted from Fig. 6. The resistance is twice as high as what we have measured before drop casting the ion liquid. One possible reason is that the mobility of graphene drops after applying ion liquid. After characterizing the source-drain current, we apply gate voltage with a third probe. Fig. 7 shows the source-drain current of the device versus the gate voltage. By applying gate voltage the s-d current is symmetric and the response is asymmetric in respect to changing the voltage polarity.

We extract the resistance response from Fig. 7. As shown in Fig. 8, by applying 4-V gate voltage, the total resistance of graphene is reduced to ~80 Ω.

From what has been presented in the previous section, we believe that the contact resistance is smaller than 50 ohm and sheet resistance may be the major issue here but have stayed with more conservative estimation.

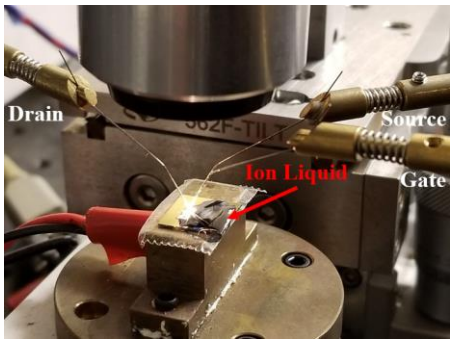

Fig. 5. Experimental setup for ion liquid assisted gating measurements of devices in fig. 2.

The previously measured Graphene/Si modulator devices based on compact Si microdisk resonators, device capacitance based on the required voltage to compensate for the initial doping of the graphene on Al_2O_3 substrate (~ 0.33 eV) and 20 um^2 area is 10 fF (corresponding to ~70 nm oxide dielectric layer). The measured capacitance of 10 fF matches better with the shift measurements as well (corresponding to a carrier concentration of $5x10^{12}/cm^2$ for an applied voltage of 15 V on the capacitive device). The 10 fF with a resistance of 150 ohm leads to a calculated 3 dB frequency response (1/(2πRC)) of 100 GHz. However, based on the model assuming the 15 nm Al_2O_3 and 12 nm BN the capacitance should be 36 fF. For the calculated capacitance of 36 fF this will reduce to 30 GHz. On a 30 GHz 3dB you can get a baud rate as high as 60 GS/s.

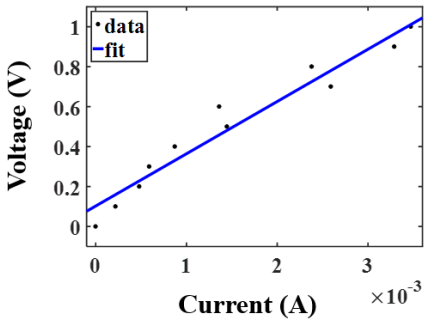

Fig. 6. I-V measurements between two electrodes (4 µm apart from each other) of Fig. 2 after drop casting ion liquid.

As we only have access to the top side of graphene, it is better to go with graphene/Si structure if we want to shoot for high speed. If we go with graphene/Si structure, we should include the Si side resistance, which is expected to be around or less than 75 ohms. Therefore the assumption of 150 ohm total resistance, 75 ohm single side graphene and 75 ohm Si is a reasonable estimate and could be improved in both graphene/Si and double-layer graphene structures.

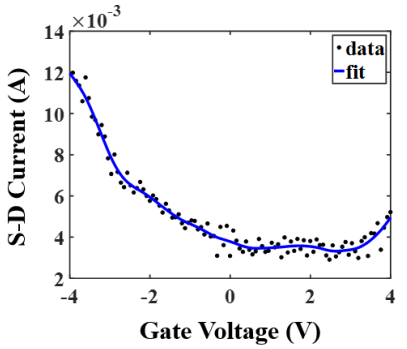

Fig. 7. Source-drain current measurement with ion liquid assisted gating. Current is measured from two electrodes (4 µm apart from each other) of Fig. 2.

For our Si/Graphene modulators, applying a 10 V voltage between the graphene and Si layers, results in ~ 250 pm shift in the resonance wavelength of the resonator(matches with 10 fF effective capacitance), which for the current device with ~ 1k quality factor results in a modulator with 2 dB insertion loss and 5 dB modulation depth. If the Q of the resonator was 4K that we have in similar devices and should be easily achievable, this could result in an insertion loss of 1 dB and modulation depth of 10 dB. Design based on 10 fF capacitor assumption and modifying the design should give us 1dB insertion loss, >10 dB modulation depth (equivalently 2dB insertion loss and > 25 dB modulation depth), > 50 GHz 3dB bandwidth (100 G baud rate), ~ 3.3 V modulation voltage, and ~ 75 fJ /bit. Design based on 36 fF capacitor assumption and modifying the design should give us 1dB insertion loss, >10 dB modulation depth (equivalently 2dB insertion loss and > 25 dB modulation depth), > 25 GHz 3dB bandwidth (50 G baud rate), ~ 5 V modulation voltage, and ~ 300 fJ /bit.

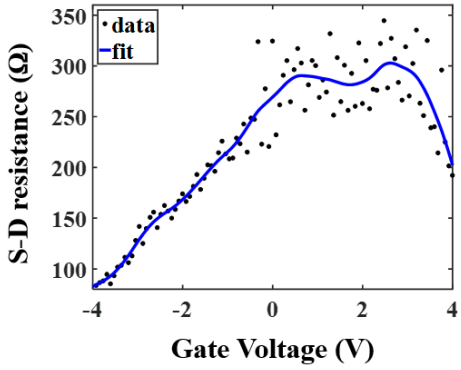

Fig. 8. Source-drain graphene total resistance with ion liquid assisted gating. Resistance is measured from two electrodes (4 µm apart from each other) of Fig. 2.

II.2. SiN resonator with ultra-high quality (Q) factor for low power modulation

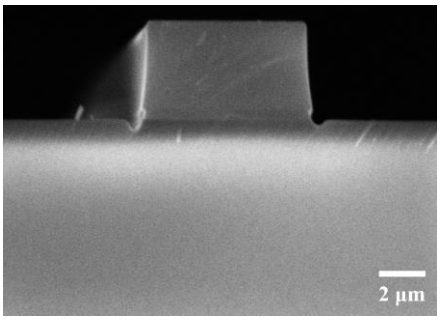

Fig. 9. SEM images showing cross-section of SiN waveguide etched with newly developed ICP recipe.

To be able to operate device with relatively low voltage, which leads to low power consumption, we want to have a device as sensitive as possible to the refractive index change of graphene. In this case, SiN material platform would be a good choice because of its low intrinsic loss. One of the main challenges in realization of graphene modulators is the significantly drop of the Q factor of the resonators upon integration of Graphene. To address this issue, one way is to bias graphene to the Pauli Block regime so that graphene will have nearly no loss. [9] On the other hand, increasing the intrinsic Q factor of the device is also important as we could get lower loss to begin with.

II.2.1. Fabrication process

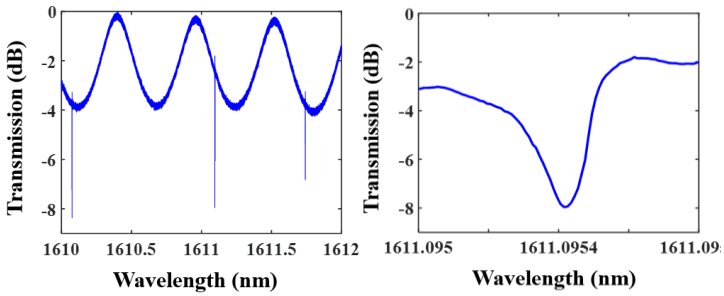

Fig. 10. Transmission spectrum of ultra-high-Q microring resonators. Zoomed in spectrum shows loaded Q factor of ~ 8M.

Previously we pattern SiN with ZEP 520A (positive resist) and RIE etching. Recently, we develop a new process using FOX (negative resist) and ICP-RIE etching. Figure 9 shows a cross-section SEM image of a SiN waveguide etched by new recipe. As we can see, we achieve nearly vertical sidewalls and it looks very smooth under SEM.

II.2.2. Characterizing ultra-high-Q cavity

We characterize the micro(thick)ring resonator we fabricate with a tunable laser at near-IR wavelength. Fig. 10 shows the transmission spectrum of the device. A loaded quality factor of ~8 M is extracted from the measurements. We also observe thermal broadening due to the heat generation from high field enhancement. To start our device fabrication with such a high Q device, we will be possibly to end up with a device that has a Q-factor as high as few thousand or above, which will lower down the requirements for modulation voltage. We are working towards optimizing the integration process to achieve higher Q-

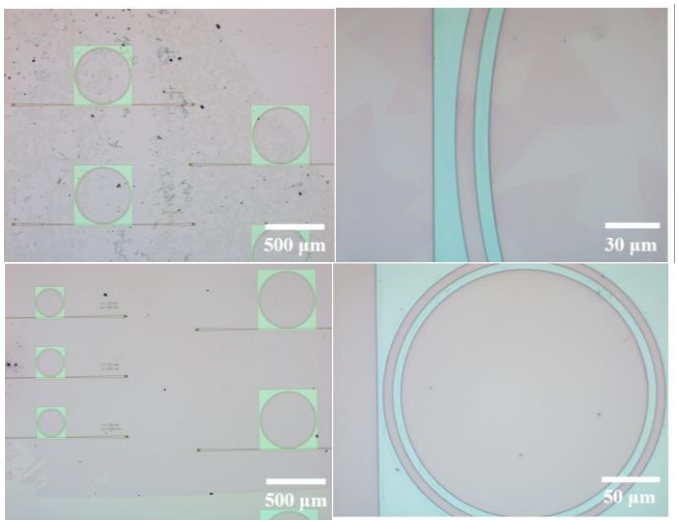

Fig. 11. Optical micro-images showing high-Q SiN microring resonators after triangular (top) & continuous (bottom) WS_2 films transfering.

factor after transferring graphene onto our devices.

II.3. WS2 as a substitute of graphene for low power modulation

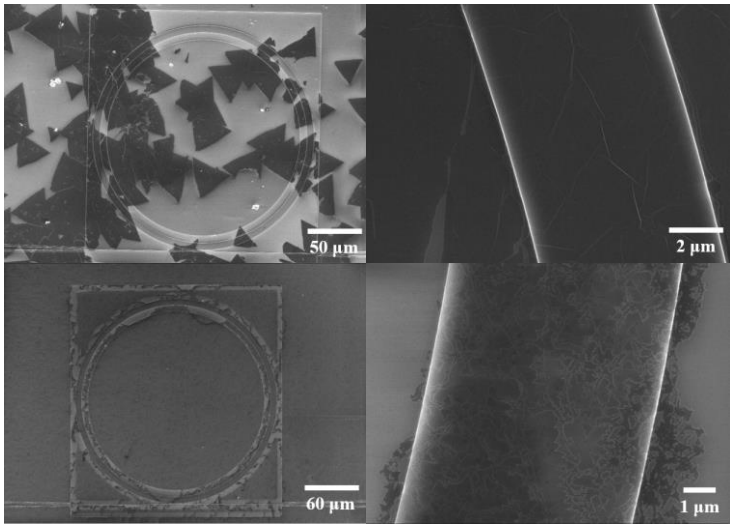

Fig. 12. SEM images showing high-Q SiN microring resonators after triangular (top) & continuous (bottom) WS_2 films transfering.

In the meantime, to be able to efficiently tune the resonance of our device without introducing too much loss into the system, we also look for other alternatives two-dimensional materials such as transitional metal dichalcogenide (TMDC) materials. We specifically use Tungsten disulfide (WS_2), which has been shown to have giant electro-refractive effect and very low optical loss at NIR wavelength. [10] To evaluate the loss that WS_2 brings into our resonator system, we transfer WS_2 onto our high-Q resonators.

II.3.1. Fabrication process

The resonators we use here is the common SiN resonators fabricated with our ZEP 520A resist. The loaded Q-factors of our resonators are around 2-3 M. We transfer WS_2 onto our device using a wet transfer method. Fig. 11 shows the optical microimages of the devices after WS_2 transfer. We use two type of WS_2-triangular shape and continuous film, both of which have been grown by CVD. Figure 12 shows SEM images of the device. We can see from SEM that WS_2 are well sitting on top of the waveguide. Further planarization on the substrate before transferring WS_2 will allow us to have WS_2 film extended out from the waveguide/resonator to enable ohmic contact to WS_2.

II.3.2. Characterizing WS_2 on high-Q cavity

We measure the transmission spectrum of the cavity before and after transferring WS_2. As can be seen from Fig. 13, before transferring WS_2 our device has a loaded Q-factor of ~2M while after transferring WS_2, our device has a loaded Q-factor of ~300k. As the fact that the whole device is covered with WS_2 and it has not been annealed in forming gas to remove organic residues, the loss reduction we get is very small. In the real application later, we only need a small portion of waveguide to be covered with WS_2 as its giant electro-refractive

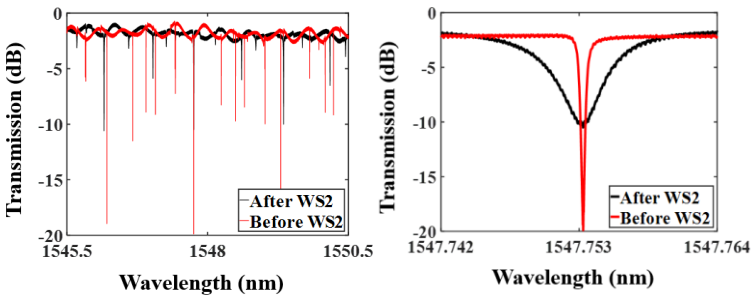

Fig. 13. Transmission spectrum of high-Q microring resonators before (red) & after (black) WS_2 layer-transfer. Zoomed in spectrum shows loaded Q factor of 2M before WS_2 layer-transfer & 300k after it.

effect to achieve efficient phase shift and lower loss. We are in the process of developing active devices with WS_2 to show low voltage tuning and later low power modulation.

Fig. 14. IPEC Westech Avanti 472

II.4. CMP for surface planarization

To solve the issue of the cracking as well as discontinuity of 2D materials after being transferred onto waveguide/resonator, we need to planarize the surface of our device. During the planarization, we should not introduce damage or extra surface roughness into the system, which will drop the Q-factor of our devices. We have developed a recipes for SiO_2 on SiN planarization using our new CMP system (Fig. 14), which enables platform suitable for crack-free 2D material integration. To planarize our sample, we first clad 660 nm PECVD SiO_2 onto our 400-nm-thick (with 15% over-etch into BOX layer beneath) SiN microresonators and waveguides which are fabricated by EBL and RIE with our common recipes as described above. We polish the 4-inch wafer sample with oxide polishing slurry (70 nm colloidal Silica, pH 11) for 23 min in total with moderate pressure (2-6 psi) and sample/pad rotation speed (30-60 rpm). After polishing, we clean the sample with DI water and followed by Acetone, Methanol, and IPA solvent cleaning. Figure 15 (left) is a photo of SiO_2-cladded SiN-on-oxide wafer after CMP. The oxide on the edge of the wafer is totally removed while majority of the sample is uniformly polished. Figure 15 (right) shows the profilometry data for a waveguide structure- a 12 nm step height has been reached after planarization (previously it is 400 nm). The profilometry data has proven the effectiveness of our CMP process.

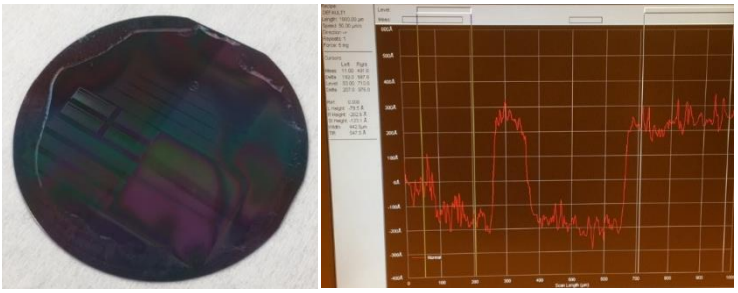

Fig. 15. A photo of a 400 nm SiN-on-oxide wafer (with PECVD SiO_2 cladding) after planarization with CMP (left). Profilometry data of a waveguide structure after planarization (right).

To further prove the effectiveness of our CMP process on making our SiN-on-oxide platform well suitable for integration with 2D materials, we take cross-sectional SEM images on the sample after planarization. As seen from Fig. 16, our SiO_2 cladding on top of SiN waveguide is totally removed- the 400 nm step height is filled up. Now with our CMP process, we can effectively planarize our sample to have a "flat" surface for 2D materials to sit on without cracking.

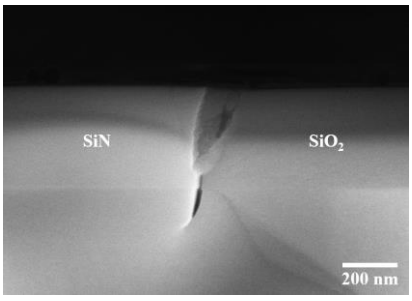

Fig. 16. Cross-sectional SEM image of a 400 nm SiN-on-oxide wafer (with PECVD SiO_2 cladding) after planarization with CMP.

II.5. Ion liquid integration on resonators

We fabricated microdisk resonators on SOI substrate and integrate ion liquid onto it to monitor the change of refractive index and quality factors. Also, we integrated back-gate electrode on the Si

pedestal so that we can apply bias voltage through S-electrode (probe)/ion liquid/Si/G-electrode stack. By monitoring the change of resonances, we can calculate the charge accumulated through the stacking structure.

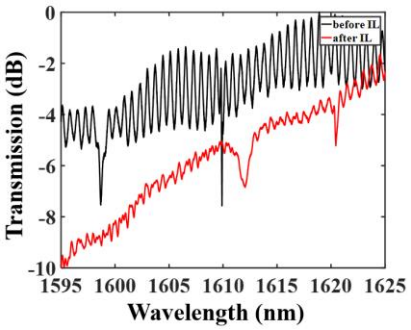

Fig. 17. Transmission spectrum before (black) and after (red) applying ion liquid a 3-um-radius microdisk resonator on SOI.

II.5.1 Fabrication process

The microdisk resonators have radius of 3 µm and height of 250 nm which corresponds to an FSR of 39 nm. The FSR is very big so that we can clearly see the change of resonance. From fig. 17, we can see that ion liquid adds extra loss to our resonators. Also, the resonances are red shifted, indicating a higher cladding refractive index. However, the loss is acceptable as the Q does not drop that much (~a factor of 2-3). The passive devices are fabricated by 2 steps of EBL and ICP dry etching (one for defining the device, one for defining the pedestal for contact). An extra step of EBL and lift-off is done to form Au/Ti contacts on the Si side. Finally, we dropcast ion liquid on to our device after mounting it onto the test bench.

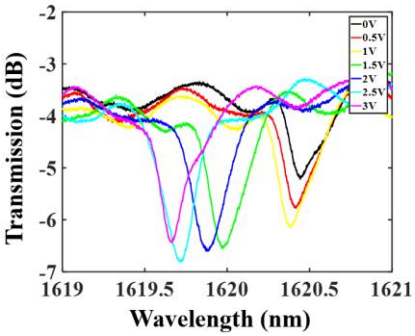

Fig. 18. Transmission spectrum of a 3-um-radius microdisk resonator on SOI with different gate voltage applied through S probe-ion liquid-Si- G probe.

II.5.2 Characterization process

Voltage is applied across S-electrode (probe)/ion liquid/Si/G-electrode stack while light is being coupled into the resonator and out of it through grating couplers. We change the gate voltage from 0 V to 3 V and monitor the shift of resonances. As shown from fig. 18, blue shift clearly happens, which means we are accumulating charges on the device. By comparing the experimental shifts with the simulation results, we arrive at the value of 0.0005/V for refractive index change vs. gate voltage, which corresponds to 1.5×10^{17} cm^{-3}/V charge accumulated calculated according to the free carrier plasma dispersion effect of Si. It shows that we could effectively accumulate charges on our integrated photonic devices without introducing too much insertion loss.

II.6. Double layer graphene on SiN modulator

II.6.1 Platform preparation

As an alternative to the CMP process, we optimized our flowable oxide (FOx) planarization process to facilitate the needs of planarized substrate for crack-free 2D material transfer. Also, FOx will be needed later in the CMP process to form the first seeding layer on top of waveguides for later deposition of PECVD

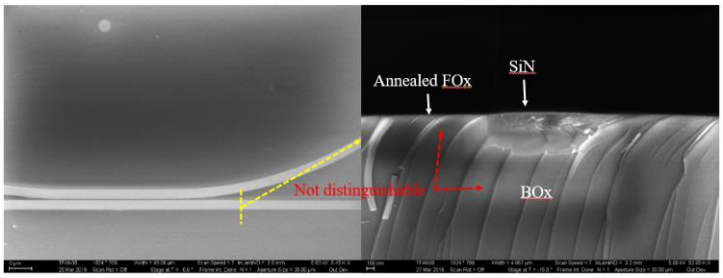

Fig. 19. Top view (left) and cross-sectional (right) SEM images of aa SiN waveguide after FOx planarization process.

oxide as it gives void-free conformal coating and will introduce little loss after annealing. Usually PECVD oxide and LPCVD oxide are directional, and they will leave voids next to the waveguide-Box intersections. Flowable oxide is a great material to overcome such issues as it could be spin coated on uneven structures and it will be converted to oxide after high temperature annealing.

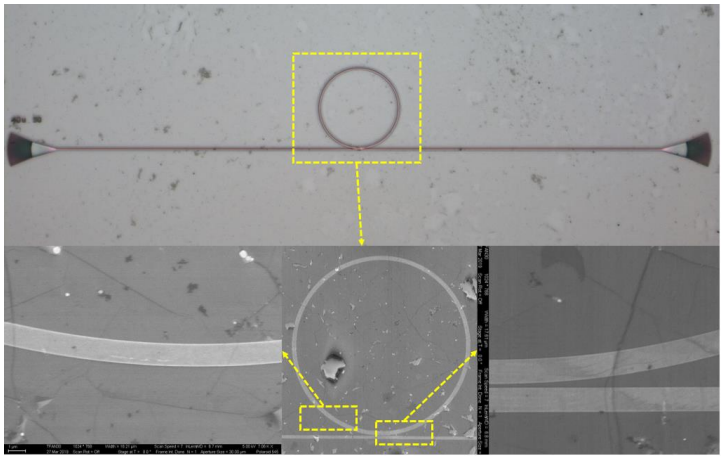

Fig. 20. SEM image (top) of a planarized microring resonator after graphene transfer; bottom SEM images are the zoomed-in pictures of the device shown in the top.

Before the planarization, we deposit 30 nm Al_2O_3 on to our SiN waveguide-resonator devices as the etch stop. We first spin coat FOx-16 on our SiN to form a layer with a thickness of 600-700 nm. Then FOx is annealed at 1150 ^oC in O2 ambient to be converted to SiO_2. After annealing process, the FOx layer will shrink for about a few 10s of nm and its refractive index will drop to close to oxide. Finally, we etch the sample in RIE chamber to thin down the FOx cladding all the way down to the etch stop. We repeat the above process for at least 3 times to ensure the sample is totally flattened. Figure 19 shows a SiN waveguide embedded in FOx layer, and there is no height difference between FOx and SiN. Also, the FOx cladding can not be distinguished from the Box after annealing, which means it is fully converted to oxide.

II.6.2 Graphene transfer and inspection

After planarization, we transfer graphene onto the device. Figure. 20 is a microring resonator after graphene transfer. Zoomed-in SEM images in fig. 20 shows graphene is crack-free in the region where we have waveguides. There are some cracks on the device which is a result from detachment of graphene. It shows that FOx after thinning down has a low adhesion compared to oxide substrate. This issue comes from the fact that dry etching will introduce roughness and defects on the surface. Later we will use CMP to treat the surface instead of using etched FOx directly, which will resolve the issue. And the density of cracks on the sample is not high- we have a pretty good yield even on the etched FOx sample.

After transferring graphene, we also pattern it and do the metallization. Figure 21 shows a microring resonator with electrode (Au/Pd/Ti) on top of graphene. Zoomed-in SEM images shows that the graphene maintains perfect after processing owe to the flatness of the substrate. The platform is well ready for double layer graphene integration. However, for the sake of yield, it would be better to combine this process with CMP to

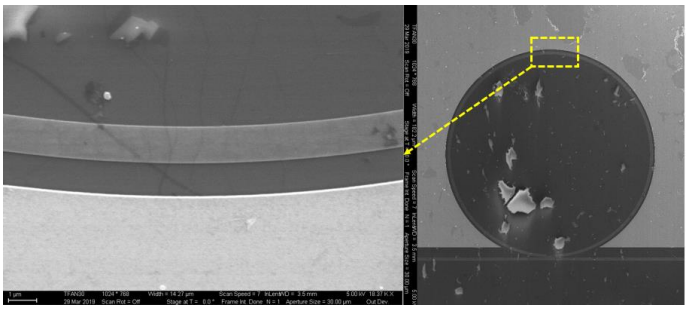

Fig. 21. SEM image (right) of a SIN microring resonator after graphene transfer and metal lift off; zoomed-in image (left) of the device in the right.

make sure the substrate not only flattened, but also polished to be very smooth. The CMP process is under development with our Avanti system. The most challenge now is the cleaning of the wafer after polishing as the residue polishing particles are boned to the wafer due to strong electrostatic force. Those particles will degrade the performance of the integrated photonic devices and cause problems for graphene transfer. We are working with a brush cleaner to develop recipes to do post cleaning of wafers after CMP.

II.7. Graphene/Si modulator

II.7.1 Fabrication process

Beside the graphene sheet resistance (which could be considerably reduced through ion gel assisted gating), the graphene ohmic contact resistance also affect in the maximum modulation speed of the modulator. The geometry of the graphene contacts and the distance between the metal-contacts and the modulator resonator are optimized based on a trade-off between the modular contact resistance and induced-loss in the resonators by the loss in metallic contacts. To do so, we use COMSOL simulation to evaluate the loss of the contacts introduced to our mode vs. the distance of it from the periphery of the microdisk. We adjust the distance to be 1 um so as to get lowest sheet resistance and contact resistance as possible.

We fabricate the passive Si microdisk resonator by 2 steps of EBL and ICP etching (one for the device, the other for the pedestal). Then we form contact (Al/Ti) on Si side by EBL and lift-off. And we do 30 nm Al_2O_3 depostion by ALD to form the gate dielectric. Graphene is then transferred onto the device and it is patterned by another step of EBL and short exposure to oxygen plasma. Finally, another contact (Au/Pd/Ti) is formed on graphene, and a final ALD oxide is deposited to passivate the surface.

Figure 21 shows the SEM of a device after reoptimizing the contacts. The yield of the fabrication is not high as we are moving contacts really close to the disk to introduce step height in a relatively small region-graphene is easier to be torn. However, we manage to get some good samples that looks good under SEM-graphene has less crack after all the fabrication.

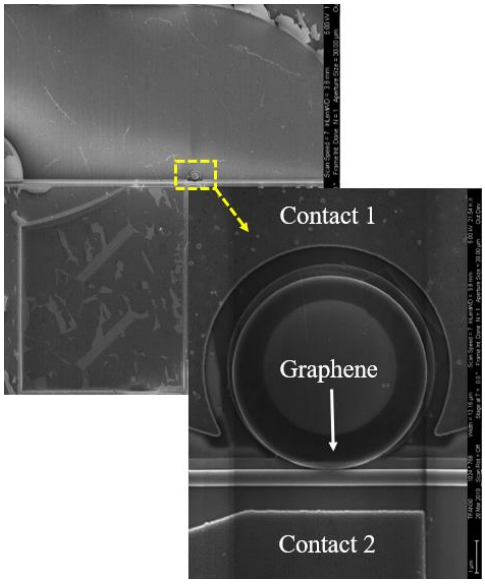

Fig. 21. SEM image of a graphene/Si microdisk modulator after reoptimizing the contacts.

II.7.2 Characterization results.

The characterization is done on our electro-optical test bench. We couple light into the modulator device through grating couplers on one end and collect the light out from the other end. We sweep the wavelength near the resonant wavelength of the device. On the electric end, we use electric probe to apply voltage through

graphene/Si capacitive junction. The voltage source we use is a Keithley SMU system which produce stable, accurate voltage supply.

Figure 22 shows the transmission spectrum of the graphene/Si microdisk modulator at positive and negative gate voltage. As seen from the figures, the resonance both blue-shifts, which matches with theory as graphene has similar dispersion effect with positive and negative charges. However, the shift is not symmetrical as graphene is not intrinsic (it is slightly p-doped due to the growth chemistry). The maximum shift we can get is 30pm/V which is good enough for us to conduct on-off modulation as the relatively high Q factors of the device (Q_0~3000-4000). The insertion loss of the device is slightly high as the contact is close to the microdisk. This could be compensated by EDFA.

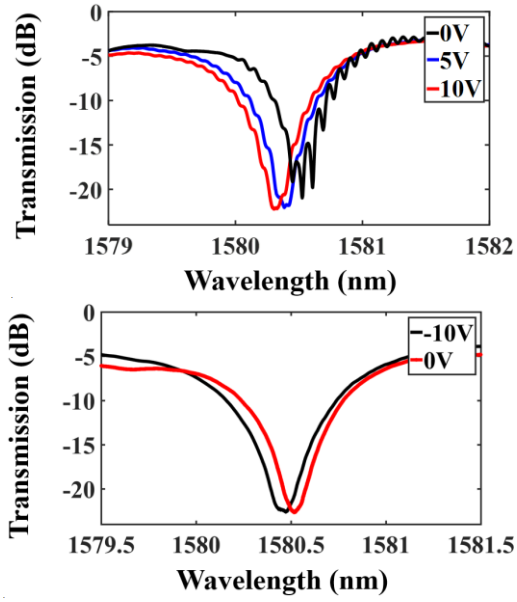

Fig. 22. Transmission spectrum of the device in fig. 21 when applying positive (top) and negative (bottom) voltage across the graphene/Si capacitive junction.

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IIII. Publications and Presentations

III.A Journal papers

[1] H. Moradinejad, T. Fan, A.A. Eftekhar, A. Adibi, "High-speed graphene modulators on passive SiN substrates," To be submitted to Optics. Express (2019).

[2] T. Fan, A.A. Eftekhar, H. Moradinejad, A. Adibi, "High-speed graphene modulators on SOI substrates," To be submitted to Optics. Express (2019).

III.B Conference presentations

[1] T. Fan, H. Taghinejad, A. H. Hosseinnia, H. Moradinejad, A. A. Eftekhar, and A. Adibi, “A high-quality silicon nitride (SiN) platform integrated with two-dimensional (2D) materials”, Photonics West, San Francisco, CA, January 2019.

[2] T. Fan, A. H. Hosseinnia, H. Moradinejad, A. A. Eftekhar, and A. Adibi, “Hybrid h-BN/Graphene/h-BN Silicon Device for Electro-optic Modulation,” CLEO: QELS_Fundamental Science, JTh2A. 78

[3] T. Fan, A. H. Hosseinnia, H. Moradinejad, A. A. Eftekhar, and A. Adibi, “Hybrid graphene modulator on CMOS platform for integrated photonic applications,” Photonics West, San Francisco, CA, January 2018.

III.C Invited Conference and seminar presentations

[1] A. H. Hosseinnia, M. Sodagar, H. Moradinejad, T. Fan, A. A. Eftekhar, and A. Adibi “Hybrid Material Platforms for Reconfigurable Integrated Nanophotonics,” Invited for Presentation in Stegeman Symposium, Orlando, FL, March 2018.

[2] A. A. Eftekhar, A. H. Hosseinnia, H. Moradinejad, T. Fan, S. Taghavi, M. Sodagar, R. Dehghannasiri, and A. Adibi, “Hybrid Material Platforms for Low-power, High-speed, and Miniaturized Integrated Nanophotonic Devices and Systems,” Invited Keynote Talk for Presentation in Optics and Photonics Conference, Philadelphia, PA, September 2018.

[3] A. H. Hosseinnia, M. Sodagar, H. Moradinejad, T. Fan, A. A. Eftekhar, and A. Adibi, “Can Hybrid Materials Replace Silicon? Nano-photonics and the Optical Path to the Future,” Invited Seminar Presentation in Samsung, San Jose, CA, October 2018.

[4] A. H. Hosseinnia, T. Fan, H. Maoradinejad, M. Sodagar, S. Taghavi, A. A. Eftekhar, and A. Adibi, “Low-power High-speed Resonance-based Integrated Photonic Modulators,” Invited for Presentation in IEEE Photonic Conference, Reston, VA, October 2018.