AFRL-RV-PS-
TR-2019-0158

RADIATION HARDENED MEMRISTIVE TECHNOLOGIES FOR SPACE-BASED NONVOLATILE MEMORY

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07 November 2019

Final Report

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
07-11-2019	Final Report	30-Jul-2015 - 07-Nov-2019

4. TITLE AND SUBTITLE

Radiation Hardened Memristive Technologies for Space-based Nonvolatile Memory

5a. CONTRACT NUMBER
FA9453-15-1-0080

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
63401F

6. AUTHOR(S)

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5d. PROJECT NUMBER
2181

5e. TASK NUMBER
EF126431

5f. WORK UNIT NUMBER
V0XP

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Arizona State University
ISTB4 Rm 561
781 E Terrace Rd
Tempe, AZ 85287-5804

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Research Laboratories
Space Vehicles Directorate
3550 Aberdeen Avenue, SE
Kirtland AFB, NM 87117-5776

10. SPONSOR/MONITOR'S ACRONYM(S)
AFRL/RVSV

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
AFRL-RV-PS-TR-2019-0158

12. DISTRIBUTION /
Approved for Public Release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT
We seek to demonstrate the viability of a commercially compatible resistive RAM (RRAM) as a non-volatile-memory technology for space electronics and to optimize RRAM array architectures and peripheral circuitry for space applications. Our studies have shown that the RRAM technology has high total ionizing dose (TID) and displacement damage (DD) tolerance. In this program we are seeking to demonstrate that compared to FLASH, RRAM has the potential for better programming cycle endurance, faster programming speed, lower power requirements, and much better scalability down to 100 nm feature sizes. Meeting these specifications would make RRAM a strong candidate for supplanting FLASH as the most widely used NVM technology. Summarizing the above listed advantages, the RRAM technology may show improved performance and likely greater radiation hardness compared to FLASH technology, bringing significant benefits to the next generation of space systems. In this program we are trying to move forward with a wafer level fabrication of a RRAM integrated circuit to that demonstrates these improvements.

15. SUBJECT TERMS
Solid state electrolyte, CMOS, Integrated Circuit, Total Ionizing Dose, Single Event Upset, Resistive Random Access Memory, Conductive Bridge Random Access Memory

16. SECURITY CLASSIFICATION OF: KTR complete boxes a-c			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
					Arthur Edwards
a. REPORT	b. ABSTRACT	c. THIS PAGE	SAR	92	19b. TELEPHONE NUMBER *(include area code)*
Unclassified	Unclassified	Unclassified			505-853-6042

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1. PROGRAM OVERVIEW

The goal of this program is to develop and transition innovative memory technologies supporting government and commercial spaceflight. We seek to demonstrate the viability of a commercially compatible resistive RAM (RRAM) as a non-volatile-memory technology for space electronics and to optimize RRAM array architectures and peripheral circuitry for space applications. RRAM memory elements are two terminal structures with resistance values set by voltage levels applied across device electrodes. Our studies during this program have shown that the RRAM technology has high total ionizing dose (TID) and displacement damage (DD) tolerance. We have shown that, when compared to FLASH, RRAM has much better total ionizing dose (TID) tolerance (> 1 MRad (Si) in RRAM vs. 100 krad(Si) in FLASH). Moreover, compared to FLASH, RRAM has better programming cycle endurance (10^6 cycles up to 10^{12} cycles in RRAM vs. 10^5 cycles in FLASH), much faster programming speed (~10 ns in RRAM and ~10 µs-100 µs in FLASH), lower programming voltage requirements (typically < 3V and as low as 0.2V in RRAM vs. >10V in FLASH) and much better scalability to sub 10 nm feature sizes, making RRAM a strong candidate for supplanting FLASH as the most widely used NVM technology. Summarizing the above listed advantages, the RRAM technology shows improved performance and likely greater radiation hardness compared to FLASH technology, bringing significant benefits to the next generation of space systems.

1.1. PROGRAM OBJECTIVES

The objective of the proposed research effort is to conduct research to demonstrate the feasibility of resistive random access memory (RRAM) for space electronics. RRAM is regarded as one of the most promising candidates for the non-volatile memory (NVM) applications beyond the scaling limit of FLASH. However, there are still two issues that are of concern to the space industry. They are:

1. the long term survivability of the RRAM technology in the hostile space environment,
2. the challenge to develop low power, high performance RRAM architectures that simultaneously meet density specifications (e.g., 128 Mb) while achieving sufficient reliability (e.g., endurance and retention) and radiation hardness?

By addressing these questions, the goal of this program is to demonstrate that RRAM will become the most viable low cost and high performance NVM technology beyond the FLASH and bring significant benefits to the next generation of space systems.

1.2. RESEARCH DESCRIPTION

The effort will be performed over a three-year period. The program focuses specifically on the following tasks:

Task 1 – RRAM Commercial Product Acquisition

During the first year of the program, the ASU team will work with CBRAM and OxRAM manufacturers to acquire commercial parts and test chips. Among the manufacturers vendors

targeted are Adesto Technologies (CBRAM), Panasonic (OxRAM), Sandia National Laboratories (OxRAM), Micron and IMEC (OxRAM).

Task 2 – Cumulative Radiation Damage Testing of Commercial Parts

Electrical testing will be performed after to ^{60}Co irradiations performed in the GammaCell220 irradiator at ASU. Displacement damage tests will utilize high energy protons and neutrons. Damage testing will be performed on commercial parts (e.g. Adesto 64Kbit CBRAM) and vendor supplied test chips to quantify the impact of ionizing and non-ionizing radiation on identified specifications.

Task 3 – Electrical and Temperature Stress Experiments on Commercial Parts

In this task, virgin commercial parts and vendor supplied test chips will be characterized to assess the response of identified specifications to electrical and temperature stress. Such tests will quantify reliability and yield for the targeted technologies and support the development of robust test protocols for wafer level and packaged part evaluations. For this task, the performance and reliability were evaluated by statistical measurements at the part and test chip level. The samples that we evaluated were:

1) Packaged parts: RRAM parts obtained from SanDisk, Adesto, IMEC, and other participating vendors, with the full write/read control logic and peripheral circuitry, will be tested to evaluate whole system performance and reliability with respect to identified electrical specifications.

2) Test chips: high density RRAM test chips provided by commercial vendors will be tested to evaluate individual cell performance and reliability with respect to identified electrical specifications.

Task 4 – Heavy Ion Testing/SEE Characterizations of Commercial Parts

Heavy ion testing on commercial parts and vendor supplied test chips will be performed to quantify the impact of transient radiation effects (e.g., single event upsets) on identified specifications. Tests will be performed using the ASU Ion Beam and the cyclotron at Lawrence Berkeley National Laboratory.

Task 5 – RRAM Device and Circuit Modeling

Throughout the program, NVM device and circuit development will be supported by modeling. Analysis of the physics of operation of both cation- and anion-based technologies will be performed with the numerical device simulator ATLAS, part of the SILVACO suite of simulation tools. This TCAD modeling effort will leverage new understandings of device operation that are products of an existing research relationship with AFRL.

Task 6 RRAM Architecture Assessment

For this task we will evaluate these two RRAM architectures to assess suitability for use in space environment. Assessments will be based on a detailed analysis of the response of identified specifications across targeted range of temperatures, total ionizing and displacement damage dose, and transient ion LETs and fluence.

Task 7 High Density RRAM Array Fabrication

At present Adesto's current generation 3 CBRAM is only a 1 Mb memory chip. Targeted memory densities for DoD space applications are currently 128 to 256 Mb. The commercial industry is interested in similar densities. For this task, ASU will design and fabricate arrays of both CBRAM and OxRAM variants that meet these density requirements. The ASU team will determine the dimensions necessary for the memory elements and design masks for array fabrication.

Task 8 Cumulative Radiation Damage Testing of High Density RRAM Arrays

Electrical testing will be performed after ^{60}Co irradiations performed in the GammaCell220 irradiator at ASU. Displacement damage tests will utilize high energy protons and/or neutrons. Damage testing will be performed on high density RRAM arrays to quantify the impact of ionizing and non-ionizing radiation on identified specifications.

Task 9 Electrical and Temperature Stress Experiments on High Density RRAM Arrays

High density RRAM arrays will be characterized to assess the response of identified specifications to electrical and temperature stress. Such tests will quantify reliability and yield. As with task 3, the performance and reliability will be evaluated by statistical measurements on the array.

Task 10 Heavy Ion Testing/SEE Characterizations of High Density RRAM Arrays

Heavy ion testing on high density RRAM arrays will be performed to quantify the impact of transient radiation effects (e.g., single event upsets) on identified specifications. As with task 4, tests will be performed using the ASU Ion Beam and the cyclotron at Lawrence Berkeley National Laboratory.

Task 11 Process Optimization for Density and Radiation Tolerance

In this task, we will develop, design, and evaluate new fabrication processes to increase memory density and enhance reliability and radiation tolerance of RRAM devices and circuits

Task 12 Design Optimization for Radiation Tolerance

In this task, we will develop, design, and evaluate memory peripheral circuitry, and RRAM array architectures using layout techniques and CMOS radiation-hardening-by-design methodologies. Through year 1, were have only completed work on Task 1-8. Program Results in Year 1

1.3. Summary of Year 1 Results

Tasks 1 – 4 were completed in the first year. At present the list of commercial RRAM chip makers includes: Fujitsu, 4DS memory, Sandisk, Crossbar, Panasonic and Adesto Technologies (source: https://www.rram-info.com/companies/rram-chip-makers). As yet our research shows that only Adesto and Panasonic have standalone products, both 512kb (Adesto's Mavriq CMRAM serial EEPROM and Panasonic's MN101L series) In year 1 we evaluated Panosonic and Adesto commercial parts for cumulative dose, heavy ion single event effect, and electrical/temperature stress response. All parts acquired were shown to meet tolerance levels for TID, DD, SEE, and stress. We would expect that RRAM devices from all manufacturers would meet targeted levels of tolerance for space applications. At issue is the impact of radiation on the underlying CMOS that control the RRAM and the density levels achieved. We are still investigating issues related to CMOS, however clearly at present, none of the chip manufacturers who have available product today are close to the 128Mb density we are looking to develop in this program..

1.4. Detailed Results in Year 1

1.4.1. RRAM Commercial Product Acquisition (Tasks 1)

1.4.1.1. Commercial RRAM Chip Acquisition

Two kinds of Mavriq serial memory chips (Figure 1 a) were acquired from Adesto. They are RM24C64 and RM25C64. Mavriq serial memory is based on the CBRAM resistive technology and is the new memory for the IoT and other energy-conscious applications. Both of them contain a memory array of 64 Kbit (8 KByte) which is EEPROM compatible serial memory. The page sizes are both 32 byte. RM24C64 is compatible with 2-wire I^2C interface which can work at 100 kHz and 400 kHz and it consumes only 60 nJ for byte write. While RM25C64 is compatible with SPI interface which can work at either 1.6 MHz or 5MHz for read.

AM13L-STK2 Evaluation Kit with MN101LR05D MCU was acquired from Panasonic Inc. MN101LR05D microcontroller unit contains an AM13L CPU core with LOAD-STORE architecture and it can work at 10 MHz frequency. Inside the microcontroller, there are 68 KB memory embedded with 64 KB ReRAM as ROM with 62 KB programmable area and 2 KB Data area. The programming voltage for RRAMs are 1.8 V to 3.6 V and it promises 1 K cycles for program area and 100 K cycles for Data area. Data rewritable in bytes without data erase.

OxRAM testing dies from Sandia National Lab was obtained in this project. The structure of the OxRAM is TiN/TaOx/TiN with both diagonal cross-point arrays and individual dog bone-structured devices. The devices showed quite unstable switching behaviors during our measurement. As shown in Figure 2 (a), devices on the diagonal cross-point arrays are all

exhibiting characteristics of constant resistance without any switching. While some of the devices from the individual dog bone structures showed switching characteristics but it is not stable. From Figure 2 (b), it is obvious that with the switching cycles increase, the on/off ratio of the devices are decreasing. There is one of the devices can switch multiple time and some parts of the cycles of this device is shown in Figure 2 (c), which presents a quite unstable switching. The initial switching is with appropriate on/off ratios. But when more cycles are swept, reset problem comes up. Even a larger voltage reset has been tried, but the larger voltage reset eventually caused unrecoverable hard breakdown of the devices. So, such device should not be used as our project candidate for further evaluations.

Figure 1. (a) Adesto Mavriq Serial Memory chips in Tube and (b) Panasonic AM13L-STK2 Evaluation Kit for MN101LR05D

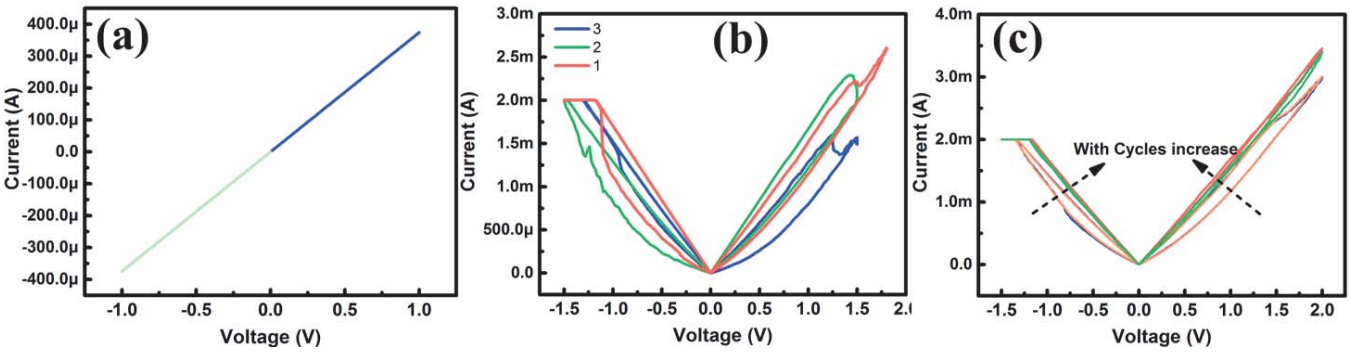


Figure 2. DC I-V characteristics of (a) diagonal cross-point devices, (b) individual dog bone structure devices and (c) part of the cycles of the individual devices. OxRAM testing dies from Sandia National Labs

1.4.1.2. Programming System Preparation

For the convenience of chip programming, SOIC to DIP sockets are prepared. Memory chips are put into sockets for programming and reading. Since both Adesto chips are EEPROM compatible, EZP2013 EEPROM USB high-speed Programmer are prepared (Figure 3 (a)). A programming software CH_2013B high-speed programmer (Figure 3 (b)) has been installed on the PC for controlling of programming circuits and data collection.

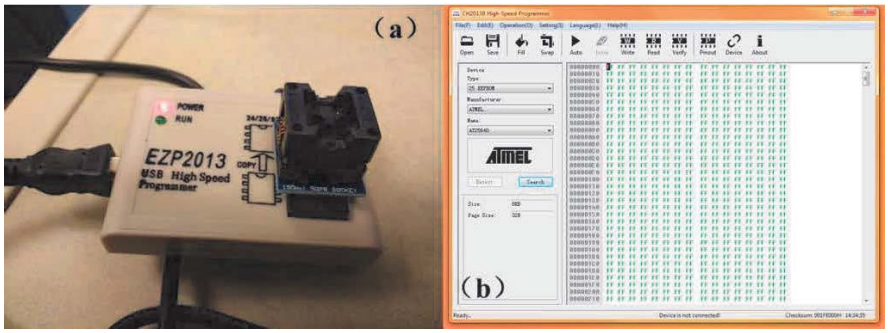


Figure 3. (a) EZP2013 USB high speed programmer with DIP sockets and (b) CH2013B high-speed Programmer software interface

To program the ReRAM inside the Panasonic MN101LR05D microcontroller, a DebugFactory Builder software is installed in the computer. As shown in Figure 4, the Evaluation Kit will be plugged into computer through USB port. The DFB software can download and operate C++ codes to control the microcontroller. To program and read the ReRAMs, we typically use the debug mode for the kit, and set up a RAM monitor to check each bit.

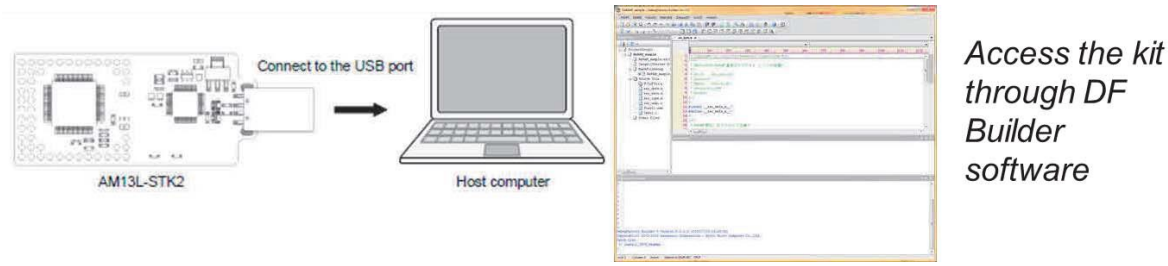


Figure 4. Illustration of the programming methods of ReRAM inside the Panasonic MN101LR05D microcontroller

1.4.2. Cumulative Radiation Damage Testing of Commercial Parts (Task2)

1.4.2.1. Electrical Programming of the chips

Atmel AT24C64 model and AT25640 model inside the CH2013B software have been used for programming RM24C64 and RM25C64 cells, respectively. The Read, Write, Erase and Verify operations of the memory chips are all fulfilled through the CH2013B programmer. The Address and memory contents are in hexadecimal notation with each row in the software representing a page inside the memory chip since both of them contain 32 Byte memory. Before radiation exposure, RM24C64 and RM25C64 chips are programmed with a repeating pattern of 00, AA, 55, FF and 00, 55, AA, FF respectively. The detailed programming information is shown in Table 1(a) and (b).

Table 1. Memory contents of (a) RM24C64 and (b) RM25C64 programmed before radiation

(a)

Address	Memory Content for RM25C64															
0000	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
• • • • • •																
07F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0800	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
• • • • • •																
0FF0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
1000	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
• • • • • •																
17F0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
1800	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
• • • • • •																
1FF0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

(b)

Address	Memory Content for RM24C64															
0000	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
• • • • • •																
07F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0800	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
• • • • • •																
0FF0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
1000	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
• • • • • •																
17F0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
1800	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
• • • • • •																
1FF0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

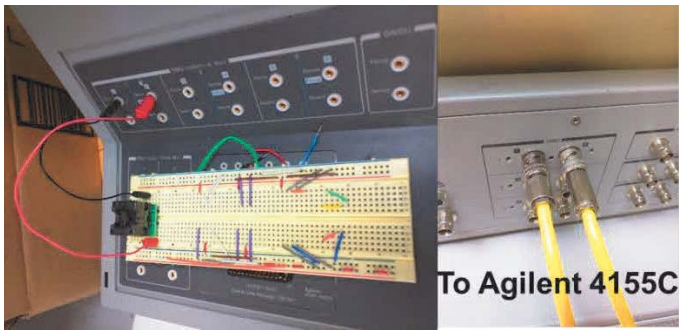


Figure 5. Testing setup for the stand-by current of the memory chips

Meanwhile, the standby current of both chips are measured to investigate the potential power consumption issue that could be induced by ionizing radiation. The standby current was measured by applying voltages from Agilent 4155C SMU1 to the Vcc pin and connecting the GND pin with grounded SMU2. The external connection was assisted with Agilent 16442A test fixture and breadboard (Figure 5). Sampling mode are employed on SMU1 with a total 10 second duration with once a second read rate. The final standby current is averaged on the 10 sampling current points.

1.4.2.2. Total Ionizing Dose Effects on the Commercial Memory Parts

Memory Tenability and Functionality Impacts

The two types of Adesto memory chips were exposed to Gamma ray with an incremental dose up to 5 Mrads (SiO_2) in a GammaCell220 irradiator. During the radiation, the chips were taken out of the irradiator chamber for contents check within 2 hours when the total doses were 600 krads, 2 Mrads, and 5 Mrads. No bit change has been observed during and after radiation for both chips. After 5 Mrads γ-ray irradiation, all memory cells were reversely programmed. For example, hexadecimal number 00 was programmed to FF, FF was programmed to 00, AA was programmed to 55, and 55 was programmed to AA. No failure has been detected during programming.

In addition, Panasonic ReRAM chip was also exposed to Gamma ray irradiation. But since the chip contains microcontroller embedded as well as the communication chips on board which are very vulnerable to the ionizing radiation, the chip stopped work after 600 krads irradiation.

Standby Current Impacts

The measured standby current before, during and after irradiation is shown in Figure 6. As seen from the results, the standby current of different chips under different biasing voltages only increased a little bit during and after the radiation comparing with the current before radiation (0 rad). However, the functionality of the chips were retained, so the tiny increase of supply current did not get influences on the functions.

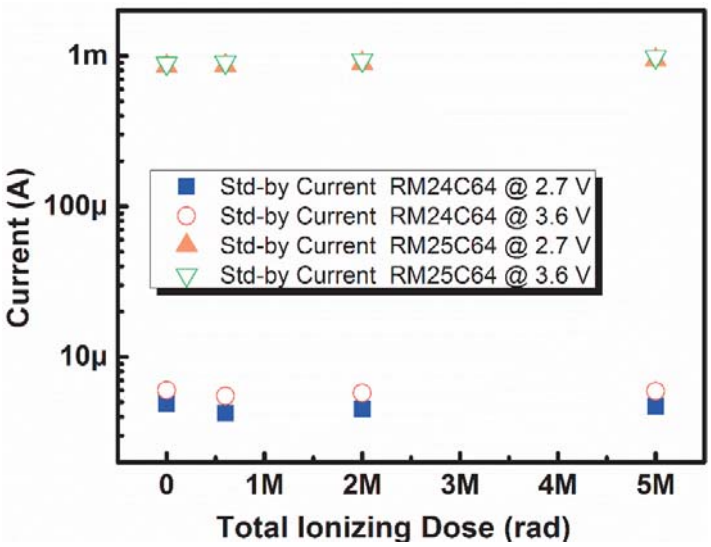


Figure 6. Standby Current of the Adesto's Mavriq Memory chips before and after certain doses of radiation

1.4.2.3. Non-Ionizing Radiation Effects on the Commercial Memory Parts

Neutron radiation was employed for the non-ionizing radiation testing of both Panasonic ReRAM chip and Adesto CBRAM chip at Cobham RAD Solutions. An in-situ read operation was performed during the radiation. The setup of the radiation testing is shown in Figure 7.

For the Panasonic part, the chip stopped working after 5 minutes inside the neutron radiation chamber with a fluence of 5.9×10^{10} cm^{-2} 14 MeV neutrons which is equivalent to 10^{11} $n\cdot cm^{-2}$ for 1 MeV(Si). Several upsets were observed for the internal RAM and most of the bit upsets were found for bit '1' rather than bit '0'. However, no bit upsets were observed in the ReRAM part even until the chip stopped working.

For the Adesto part, the chip RM24C64 was exposed to the neutron sources with a fluence of 2.2×10^{13} cm^{-2} 14 MeV neutron which is equivalent to 3.9×10^{13} cm^{-2} 1 MeV(Si) without any upsets. The chip was preprogrammed with a pattern same to Figure 4 (a). Pattern of the whole chip was checked every 2.5 minutes. No bit upsets were observed for the chip which exhibited very robust performance against the radiation.

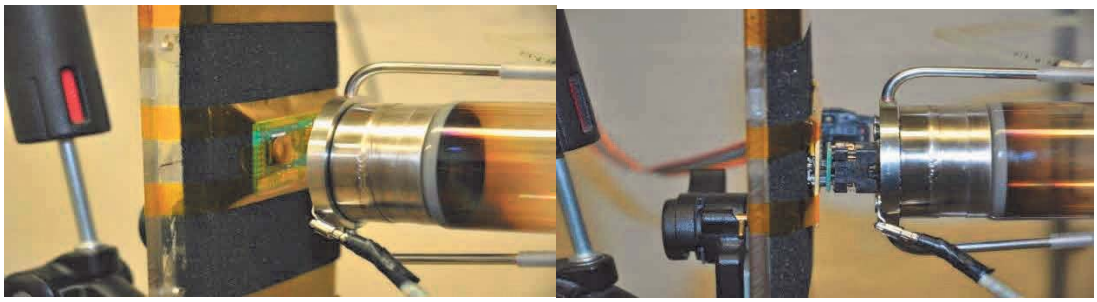


Figure 7. The in-situ testing setup of neutron radiation for Panasonic chip and Adesto chip

1.4.3. Temperature and Electrical Stress Experiments on Commercial Parts (Task 3)

1.4.3.1. Temperature Stress on Commercial Parts

Preparation of the Temperature Stress Experiments

To evaluate the temperature effects on the memories, both Adesto CBRAMs and Panasonic ReRAMs were preprogrammed at room temperature. For evaluation of high temperature effects, memories were put into oven at 90 ^{o}C. For evaluation of low temperature effects, memories were put into cryostat at -50 ^{o}C. The setup for temperature stress evaluations are shown in Figure 8 (a) and (b). The total stress time for low and high temperatures are 3 hours respectively. During the 3 hours' time, chips were taken out for information check when it is 1 hour, 2 hours and 3 hours from the beginning. The duration of each check is within 2 minutes and chips are put back immediately after evaluation.

For Adesto CBRAM memories, two RM24C64 and two RM25C64 chips were employed for temperature stress evaluation. One of each type chip is used for memory retention ability evaluation and another one of each type is used for programming ability evaluation. The memory

contents pattern for retention ability evaluation is same as shown in Figure 4 (a) while the reversed pattern of Figure 4 (a) is used for programming ability evaluation.

For ReRAM MN101LR05D microcontroller, memory addresses from 04000 to 13FFF are ReRAM memories and has been employed for the temperature stress. The ReRAM contents were preprogrammed according to the address. Memories from 04000 to 06FFF and from 10000 to 10FFF programmed to 00, from 07000 to 09FFF and from 11000 to 11FFF programmed to 55, from 0A000 to 0CFFF and from 12000 to 12FFF programmed to AA, from 0D000 to 0FFFF and from 13000 to 13 FFF programmed to FF. Among them, 10000 to 13FFF (16 KB) are used for programming evaluation and 04000 to 0FFFF (48 KB) are used for retention ability evaluation.

Memory Tenability and Functionality Impacts

No bit flip from ReRAM (MN101LR05D) and CBRAM (RM24C64 and RM25C64) has been observed during and after the 3-hour temperature stress for all the chips. Programming abilities for all the chips during and after the 3-hour temperature stress were checked. One of the RM24C64 chips and one of the RM25C64 chips and memory address from 10000 to 13FFF of the Panasonic RRAM chips are programmed with their reversed patterns twice during each check time and after all the stress. For example of RM24C64, the memory of address from 0000 to 07FF was reprogrammed from FF to 00 and from 00 to FF during one check time and then the chip is put back to chamber for further temperature stress. After the 3-hour stress, all chips are programmed with their reversed pattern. During this test, no bit error has been observed which means all the memories function well during and after the high and low temperature stress.

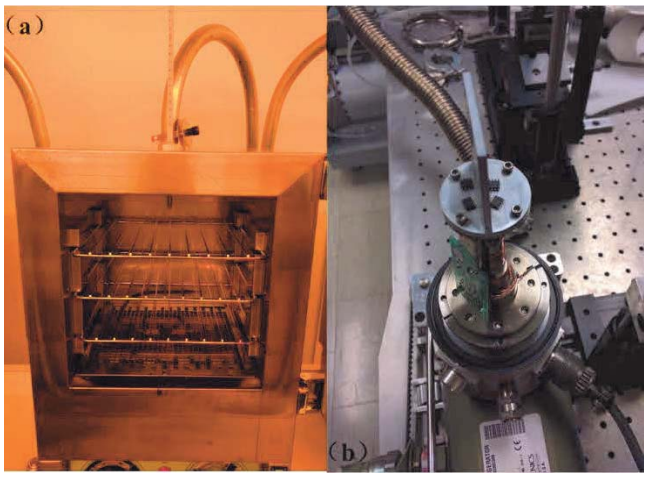


Figure 8. (a) Oven for high temperature evaluation and (b) cryostat for low temperature evaluation.

Standby Current (SBC) Impacts

The measured standby current before, during and after irradiation is shown in Figure 9 for RM24C64 and RM25C64 chips. As seen from the results, the standby current of different chips under different biasing voltages only varied a little bit during and after the temperature stress

comparing with the current before temperature stress (0 min). However, the functionality of the chips still retained, so the tiny variations of supply current did not impact the functionality.

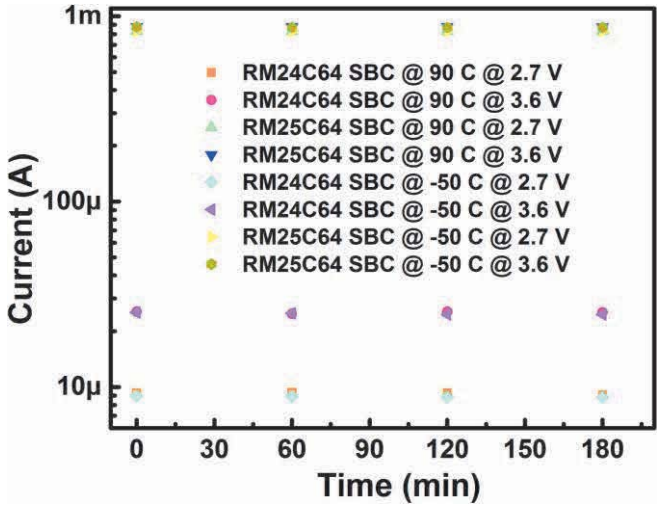


Figure 9. Standby Current of the Mavriq Memory chips before and during the temperature stress

1.4.3.2. Electrical Stress on bare die of Commercial Parts

Adesto Apollo CBRAM test dies were acquired for the stress testing. The typical specifications of the CBRAM devices were shown in Figure 10 (a) and 10 (b). The device with an area of 0.25 um×0.25 um were tested via a DC sweep from 0 to 1.0 V with a current compliance of 10 uA for set operation and a sweep from 0 to -1.0 V for reset operation. The threshold voltage for programming and erasing are estimated to be 0.5 V and -0.25 V, respectively. In Figure 10 (b), the resistance distribution of 100 DC cycles was shown for the demonstration of the functionality of the device. After that, device was programmed to LRS and HRS separately for stress testing. The stress conditions were -0.05 V 10^4 s for on state and 0.1 V 10^4 s for off state. No current upsets were observed for HRS during the stress. However, for LRS, though current degradation were observed within the first 2000 s, the on state has kept unchanged with current almost unchanging afterwards.

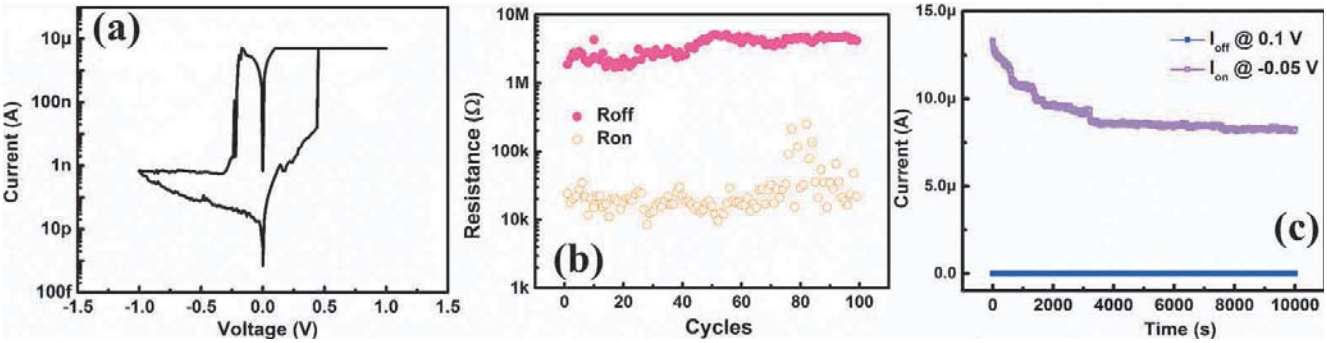


Figure 10. (a) Typical sweep, (b) the resistance distribution of 100 DC sweep cycles and (c) the LRS and HRS 10^4 s stress results of Adesto Apollo CBRAM device.

1.4.4. Heavy Ion Testing/SEE Characterizations of Commercial Parts (Task 4)

1.4.4.1. Part Preparation

As shown in Figure 11 (a), QFP080-P-1212F plastic package of the Panasonic MN101L chip was acid etched and the entire die surface was exposed for the heavy ion test. A collimator was made to expose only the RRAM portion of the microcontroller and Ultra-Tech ASAP-1® surface preparation machine was used to create a "window" in a kovar lid. The thickness of the kovar collimator was approximately 10 mils (254 um), which stops the majority of the test facility heavy ion energy spectrum from penetrating into the device sensitive regions such as the static random access memory (SRAM), logic circuits, and analog circuits [1]. As shown in Figure 11 (b), the Adesto CBRAM was interfaced using an ARM Cortex-M4-based 32-bit microcontroller with 64kB RAM and 256kB flash memory. A PC was used to send/receive commands to/from the microcontroller [2].

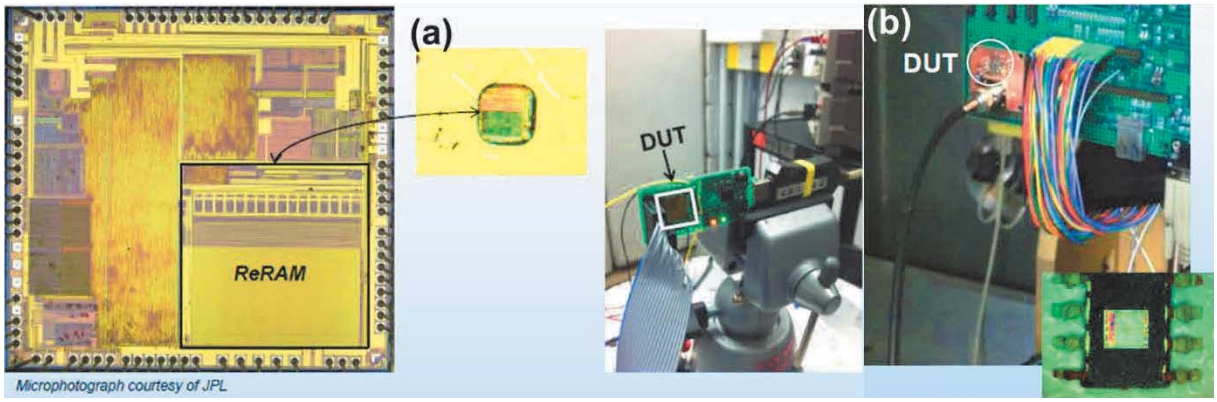


Figure 11. Testing setup of the heavy ion testing for (a) ReRAM parts and (b) for CBRAM parts

1.4.4.2. Testing Methodology

The Panasonic ReRAM was operated in the following test modes: static on, dynamic read, dynamic read/compare/write, and dynamic write. Different data patterns, including 00, FF, and checkerboard AA were evaluated. The light emitting diode (LED) indicator was actively monitored which shows the functionality of the microcontroller. The irradiation was carried out at the Texas A&M University (TAMU) Cyclotron SEE Test Facility (15 MeV/amu beam) and at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility (16 MeV/amu beam). The detailed linear energy threshold, energy and range is shown in Figure 12 (a). Four parts were irradiated during the two test campaigns [1].

(a)

Ion	Total Energy (MeV)	LET (MeV·cm²/mg)	Range in Si (µm)
TAMU			
Ne	253	3.1	225
Ar	453	11.2	124
Kr	768	33.1	88
Xe	1027	60.6	75
LBNL			
Cu	659	21.2	108
Kr	886	30.9	113

(b)

Ion	Total Energy (MeV)	LET (MeV·cm²/mg)	Range in Si (µm)
Ne	253	3.1	225
Ar	642	7.3	256
Kr	1225	25.0	165
Xe	1955	49.3	148

Figure 12. Heavy ion species, energy, LET, and range for (a) ReRAM parts and (b) for CBRAM parts

For the Adesto CBRAM, the device-under-test (DUT) is soldered onto a two-sided copper-plated socket and programmed with a repeating pattern: 00, FF, AA, 55, or counter. The test modes include: static on (standby), continuous read, and continuous write/read. The read mode included byte (random) read and sequential read. The write mode included byte write and page write. The supply current was monitored during irradiation. Four parts were tested at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility with a cocktail of 16 MeV/amu heavy ions. The detailed linear energy threshold, energy and range is shown in Figure 12 (b) [2].

1.4.4.3. Heavy ion testing results/ SEE Characteristics

For Panasonic ReRAM parts, no bit upset and no bit errors with the device operating in static mode, for heavy ions with LET as high as 70 MeV·cm2/mg. Read-back errors caused by single-even upsets (SEU) corrupted the data in address buffers and/or registers (see Figure 13 for memory space and error bit locations). However but the functionality recovers after device reset.

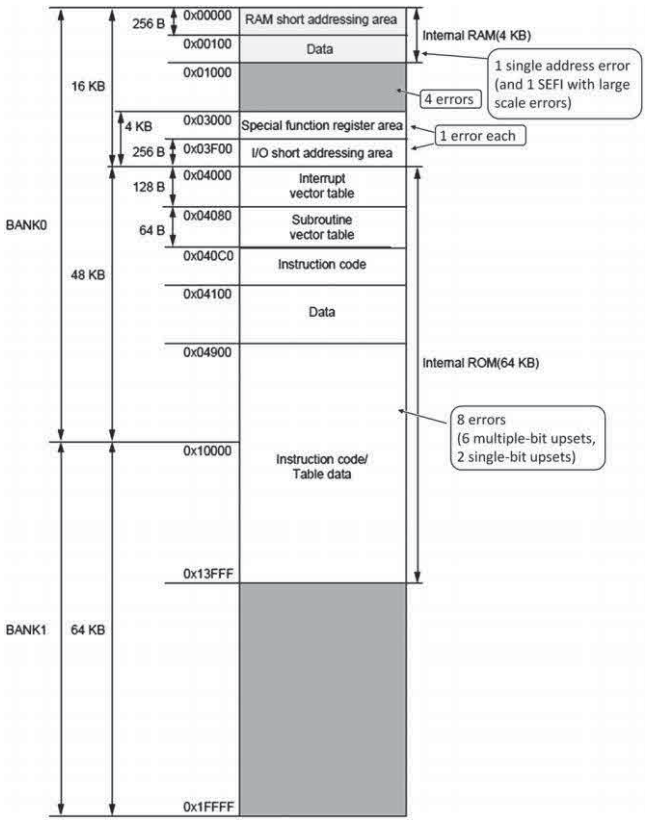


Figure 13. Address locations of various SEE modes in the MN101L memory space and error bits locations

While the single-event functional interrupt (SEFI) was the predominant SEE mode from the dynamic read and write test. The majority of SEFIs are caused microcontroller hang-ups together with the supply current dropping to the standby level. Nevertheless, a reset can always recover the functionality. Neglecting SEFI, 15 bit errors (addresses with errant bits) were observed. Among all the errors, four of these errors originated from the ReRAM portion of the memory space and the other errors originated from inaccessible memory areas of the microcontroller. For the four errors from the ReRAM memory space, they are unlikely to have originated from bit upsets in the memory cells but look like control circuit upsets caused incorrect reads or write commands. In addition, two parts lost functionality during the irradiation.

For Adesto CBRAM parts, during static or read-only test modes, no SEU was observed. While during write/read tests, the single-bit upsets (SBU) was observed. Most (if not all) bit upsets due to acknowledgement fails, indicative of control circuit errors and not array errors. SEFIs were observed in the static (standby) and dynamic test mode which caused stuck address, accumulating acknowledgement failures and read errors in continuous addresses. Those errors typically can be resolved by a reset. Lastly, there is no apparent pattern sensitivity for FF, 00, AA, and Counter.

1.4.5. RRAM Device and Circuit Modeling (Task 5)

1.4.5.1. Basic Analytical Model

The mobile metal ions in a solid electrolyte sit in potential wells separated by low barriers and the ions can readily diffuse from site to site. The application of an external voltage lowers the barriers in the direction of the electric field ε via a sinh(*azqε/2kT*) expression, where *a* is the effective barrier width (hopping distance) and *zq* is the total charge on the ion accounting for ionic strength. The ions will drift in the direction of the electric field. As usual, *T* is local temperature and *k* is Boltzmann's constant. The ions move through the solid electrolyte via a coordinated motion, in which the ion in the site closest to that vacated by a removed ion will move into this site and the ions upstream will do likewise, each filling the vacated site of the one downstream until the last vacated space closest to the anode is taken by an incoming ion. The ion current density created by the drift component J_d is the product of the charge density zqN_i, where N_i is cation concentration, and the drift velocity u_d. The drift velocity is determined via the thermal velocity u_{th} by

$$u_d = u_{th} exp\left(-\frac{E_o}{kT}\right) sinh\left(\frac{azq\varepsilon}{2kT}\right) \quad (1)$$

where E_o is the barrier height between sites at zero field, i.e., the barrier for diffusion only. This is the Mott-Gurney formalism. In disordered glassy materials, typical of our solid electrolytes, there is actually a distribution of barrier heights but we can use a single value for these and for hopping distance a in a simple analysis. Taking $u_{th} = (2kT/m_i)^{½}$, where m_i is the mass of the ion, u_{th} is 2.1 x 10^4 cms^{-1} for Ag+ and 2.8 x 10^4 cms^{-1} for Cu^{2+}. It can also be assumed that u_{th} is equivalent *aν*, where ν is hopping frequency (ion jump rate) between sites, in the order of 10^{12} s^{-1}. Considering the case of Ag+ in a chalcogenide glass with E_o = 0.2 eV, a = 10^{-8} cm, Eq. 1 gives us a drift velocity for ε = 10^6 V cm^{-1} of 1.9 cms^{-1}. So, the expression for ion drift current density J_d may be given as

$$J_d = zqN_i \left(\frac{2kT}{m_i}\right)^{½} exp\left(-\frac{E_o}{kT}\right) sinh\left(\frac{azq\varepsilon}{2kT}\right) = zqN_i a\nu\, exp\left(-\frac{E_o}{kT}\right) sinh\left(\frac{azq\varepsilon}{2kT}\right) \quad (2)$$

At relatively high electric field (>>2kT), this expression may be modified to

$$J_d = zqN_i a\nu\, exp\left(-\frac{E_o}{kT}\right) exp\left(\frac{azq\varepsilon}{2kT}\right) \quad (3)$$

This exponential relationship between field/applied voltage and ion current above is common in ion conductors.

To get a sense of the magnitude of current density for appropriate fields, we take reasonable values of concentration and barrier height in Eqs. 2 and 3for two cases, a high diffusivity and high ion concentration system ("fast" case), representative of Ag+ in a chalcogenide base glass, with E_o = 0.2 eV and N_i = 10^{22} cm^{-3}, and a lower diffusivity and lower concentration system ("slow" case), representative of Cu^{2+} in a low density (e.g., 2.08 g cm^{-3}) deposited oxide, with E_o = 0.6 eV and N_i = 10^{21} cm-3. In doing this, we see that for an electric field of 10^6 V cm^{-1} (1 V

across a 10 nm thick electrolyte), the current density in these systems differs by around seven orders of magnitude (1.9 x 10^4 A cm^{-2} for the high case vs. 1.3 x 10^{-3} A cm^{-2} for the low case) but increasing the field narrows the differential. Clearly, to get similar ion current density in the two systems, the field would have to be much larger in the low diffusivity/low concentration case; e.g., to achieve a current density of 1.6 x 10^4 A cm^{-2} in both systems, we would have to have fields of 10^5 V cm^{-1} in the fast case and 4.4 x 10^7 V cm^{-1} for the slow case. The latter is unreasonably large and will lead to breakdown in the material in question and so transport current density parity cannot be achieved in these two classes of materials.

The simple ion current analysis above assumes a constant field in the electrolyte but an incomplete filament of length h will reduce the effective gap between the electrodes and thereby increase the field by $\varepsilon = V_c/(L-h)$, so that the expression for current density becomes

$$J_d = J' exp\left(\frac{azqV_c}{2kT(L-h)}\right) \quad (4)$$

Therefore, the ion current density essentially increases as $exp(-1/h)$ as the filament growth proceeds. Current density is also proportional to filament growth rate, dh/dt, which leads to a non-linear differential equation,

$$\frac{dh}{dt} = \frac{N_i a\nu}{N_f} exp\left(-\frac{E_o}{kT}\right) exp\left(\frac{azqV_c}{2kT(L-h(t))}\right) \quad (5)$$

Plotting this for the fast case above and for three different values of voltage, V_c, (Figure. 14) we see that the growth rate is actually quite constant for much of the filament growth at low voltage but that it accelerates as the filament-anode gap nears closure, as expected. Higher cell voltage results in a more pronounced growth rate acceleration effect. Figure. 15 shows filament length vs. growth time for 1 V across a 10 nm thick fast electrolyte (Figure. 15(a)) and 2 V across a 3 nm thick slow electrolyte (Figure. 15(b)). We can see from these plots that bridging of the electrolyte, indicated by the black dashed lines in Figure. 15, occurs in 356 ns and 171 ms for the fast and slow cases respectively. The growth beyond the half-way point (where the filament is 5 nm long – red dashed lines in Figure. 15) is greatly accelerated in the slow system, indicating that the effect of the increasing field is much more pronounced in this case.

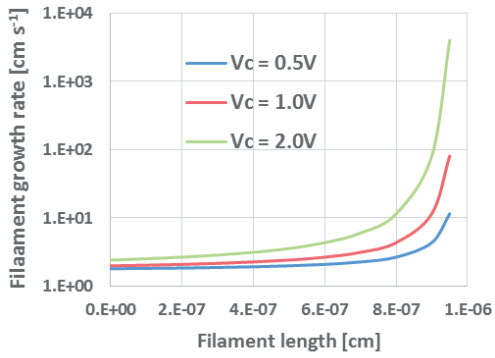


Figure 14. Filament growth rate vs. filament length for cell voltages of 0.5, 1.0, and 2.0 V

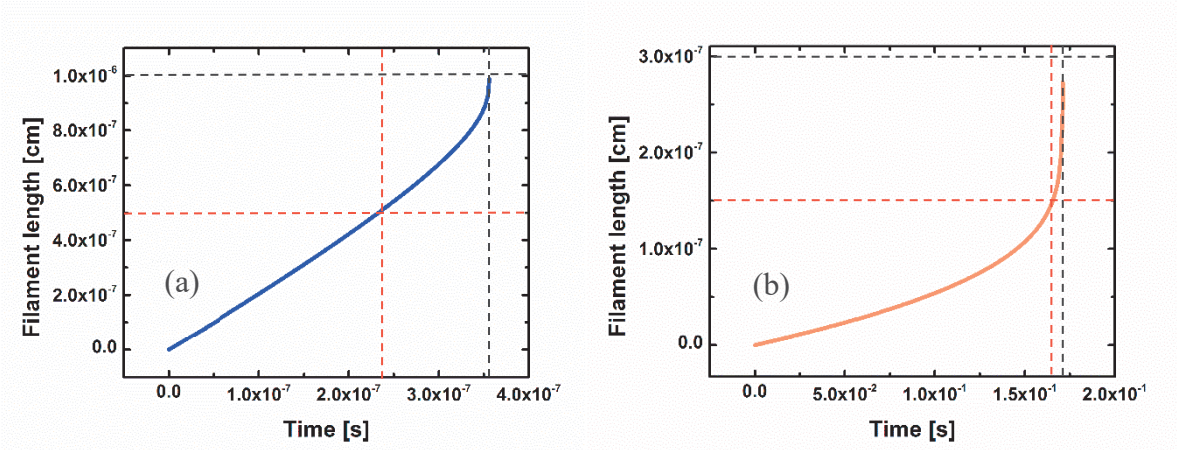


Figure 15. Filament length vs. growth time for (a) a cell voltage of 1.0 V across a 10 nm thick electrolyte for a "fast" material system and (b) a cell voltage of 2.0 V across a 3 nm thick electrolyte for a "slow" material system

The analytical model described above captures the relative dynamics of filament growth in a "fast" (e.g., Ag-ChG system) and a "slow" (e.g. Cu-SiO_2 system). It can also be used to support a qualitative interpretation of the ionizing radiation response of both systems. The "slow" response characteristics of Cu in SiO_2 may explain its suppression of ionizing radiation-induced photo-doping. More details regarding this and subsequent models discussed below can be found in our paper [3] recently published in the Journal of Semiconductor Science and Technology.

1.4.5.2. Compact modeling

In order to incorporate new devices such as CBRAM into the IC design framework and support circuit level modeling of radiation effects in this memory technology, compact models for these components must be developed with standard interfaces such a Verilog-a. Today one of the most widely accepted Verilog-a models for CBRAM is derived from the Mott-Gurney equation introduced above. In the model, the switching mechanism relies on the dynamics of filament formation and dissolution. The primary internal variables for the model are the filament height, h, and its radius, r. For simplicity, it is assumed that the filament has a cylindrical shape with uniform radius. Based on the Mott-Gurney ion transport model the filament's vertical and lateral growth/dissolutions rates are expressed as

$$\frac{dh}{dt} = C_h \exp\left(\frac{-E_o}{kT}\right)\sinh\left(\frac{azq(V_c/(L-h))}{2kT}\right) \tag{6}$$

and

$$\frac{dr}{dt} = C_r \exp\left(\frac{-E_o}{kT}\right)\sinh\left(\frac{azq\beta V_c}{kT}\right), \tag{7}$$

where β is the field parameter for lateral growth. The remaining parameters were defined previously, except for constants C_h and C_r, which can be derived from the physical model (e.g.,

$C_h = N_i av/N_f$) or obtained empirically from fits to experimental data. Based on the values of h and r computed from the time integrals of Eqs. 6 and 7, the resistance across the CBRAM device R_c can be expressed as the parallel combination of filament, R_f, and electrolyte resistance, R_e

$$R_c = \frac{1}{\frac{1}{R_f} + \frac{1}{R_e}}, \tag{8}$$

where $R_f = \frac{h}{\sigma_f \pi r^2}$ and $R_e = \frac{L}{\sigma_e (S - \pi r^2)}$. The parameter σ_f for R_f is the filament resistivity. The parameters σ_e and S for R_e are the electrolyte resistivity and device cross-sectional area, respectively. While $\sigma_e << \sigma_f$, precise values are difficult to derive from first principles due to their strong dependence on device processing. Thus resistivity parameters are generally used as free fitting parameters within specified extremes. When inserting into a compatible circuit simulation package, a Verilog-a model, once optimized, can be used to simulate the electrical characteristics of the CBRAM device. Figure. 16 shows how the circuit model simulation reproduces the electrical characteristics of a device fabricated with a germanium selenide electrolyte with silver as the active metal. For these simulations, $\sigma_f = 483\ \Omega^{-1}\text{cm}^{-1}$ and $\sigma_e = 4.76 \times 10^{-2}\ \Omega^{-1}\text{cm}^{-1}$. The figure clearly shows that when properly parameterized, the CBRAM compact model can provide an accurate representation of the device for the circuit simulator.

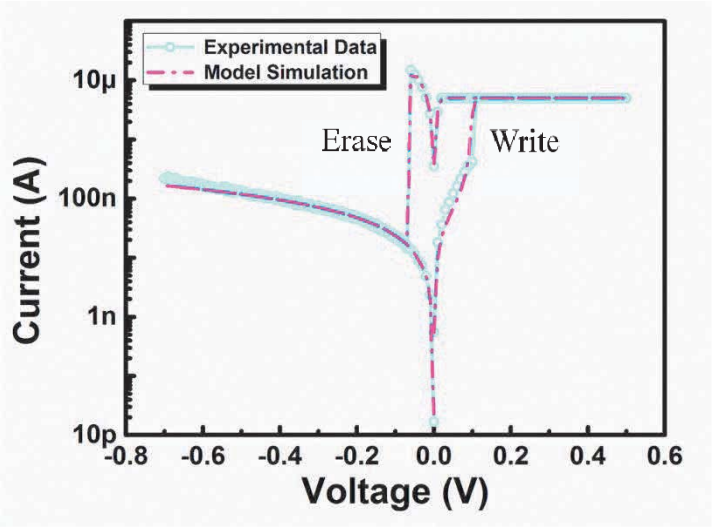


Figure 16. Circuit simulation results overlay on experimental data for DC switching characteristics of an Ag-Ge-Se CBRAM device.

1.4.5.3. Finite element device modeling

The precise physics of metallic filament growth and dissolution in solid electrolytes is still not fully understood. While nano-scale metrology has revealed much about the static characteristics of the filament and DFT calculations provide useful information regarding localized structure, a unified physics-based analytical model for device operation has not been developed. This type of

modeling is critical for expanding use of CBRAM in circuit applications, particular those used in harsh radiation environments. Although Monte Carlo methods have been shown to effectively model particular aspects of metal transport and filament formation, these statistical models are not easily mapped into the compact models necessary for circuit design. Compact models are built from closed form analytical functions that are best derived from device physics. The drift-diffusion, recombination-generation (R-G), and continuity equations that serve as the backbone of physical models for solid state devices (e.g., transistors) can be adapted to serve as excellent abstractions for processes governing CBRAM operation. For example, metal oxidation at the anode can be modeled as the recombination-generation (R-G) equation

$$G_{\mathrm{i}} = zG_n = R_M = \left[k_o exp\left(\frac{-E_{Ao}}{kT}\right)\right] N_M, \tag{9}$$

where G_i and G_n represent the generation rates ($cm^{-3}s^{-1}$) of metal ions and electrons respectively and R is the recombination rate ($cm^{-3}s^{-1}$) of neutral metal species. Also in Eq. 9, z is the number of charges on the generated ion, N_M is the neutral metal density (cm^{-3}), and k_o, and E_{Ao} are the oxidation rate constants. Similarly, metal reduction at the cathode and onto a growing filament can be modeled as

$$R_i = zR_n = G_M = \left[k_r exp\left(\frac{-E_{Ar}}{kT}\right)\right] (N_i)(zn), \tag{10}$$

where N_i is the ion density, n is the electron density, and k_r, and E_{Ar} are the reduction rate constants. Ion transport within the electrolyte is modeled using the drift-diffusion equation

$$F_i = -D_{\mathrm{i}}\left(\frac{zqN_i\nabla\varphi}{kT} + \nabla N_{\mathrm{i}}\right) \tag{11}$$

where D_i is the diffusion constant for metal ions and ϕ is the local potential. The spatial and time dependent change in species across the device can be thus modeled with the continuity equations:

$$\frac{dN_i}{dt} = -\nabla F_{\mathrm{i}} - R_{\mathrm{i}} + G_{\mathrm{i}} \tag{12}$$

for charged species, and

$$\frac{dN_M}{dt} = -R_M + G_M \tag{13}$$

for neutral species.

Unlike the free carriers in semiconductors, ion transport in the solid electrolyte is characterized by ionic hopping. As described earlier, according to the Mott-Gurney model, the hopping process is characterized by thermionic emission over an energy barrier, E_o, the barrier width, a, the hopping frequency, v, and the local electric field magnitude, $\mathcal{E}$. Again assuming a large electric field, these localized effects can be captured with a field dependent diffusion constant

$$D_i = f(\varepsilon) a \nu \exp\left(\frac{-E_o}{kT}\right) \tag{14}$$

where

$$f(\varepsilon) = \frac{kT}{zq} \frac{\exp(zqa\varepsilon/2kT)}{\varepsilon} . \tag{15}$$

When incorporated into a finite element device simulator that simultaneously solves standard carrier statistics along with Eqs. 9-15, a deterministic model for filament growth and radiation effects can be realized. Figure. 17 represents a conceptual illustration of the basic filament growth process commonly observed in CBRAM. The three primary mechanisms of growth are (1) oxidation at the active metal anode, (2) ion current in the electrolyte, and (3) ion reduction at the cathode and attached filament. Filament growth is exhibited as an increase in neutral metal species within the electrolyte. Figure. 18 plots the change in the neutral metal concentration, along the cutline indicated on Figure. 17, as a function of distance from anode (0 μm) to cathode (0.1 μm). For this transient simulation, a constant positive bias of 1V is applied on the anode while the cathode is grounded. The profiles represent concentrations at four different time steps (Δt, $1.5\Delta t$, $2\Delta t$ and $100\ \Delta t$) and demonstrate filament (neutral metal) growth initiating at the cathode and growing (increases in density) toward the anode over time. It should be noted that the speed and direction of filament formation is largely dependent on the selection of material, diffusion, and reaction rate constant parameters. For the simulation results presented above the modeled system is Ge-Se chalcogenide glass electrolyte with silver as the active metal.

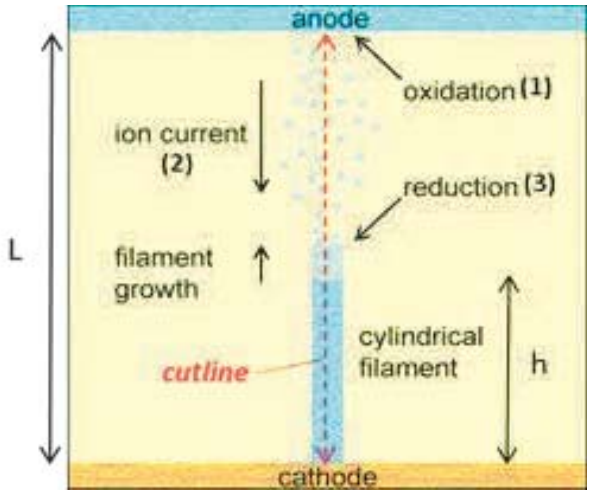


Figure 17. Conceptual illustration of filament growth in CBRAM

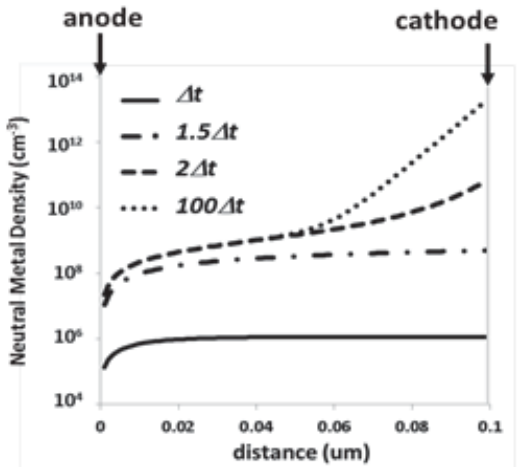


Figure 18. Finite element simulation results showing filament growth as an increase in neutral metal density

1.4.5.4. Model for neutron displacement damage effects

Eq. 14 elucidates a potential model that explains the neutron effects on CHG CBRAM. An explanation for the observed displacement damage effect could be the reduction of ion diffusivity through the electrolyte (Eq. 14). The Ag-$Ge_{30}Se_{70}$ material system is a disordered glass with a variety of evolving bond formations at room temperature. The localized variation in material structure creates potential barriers that the Ag^+ ions must hop over to migrate through the electrolyte as illustrated in Figure. 19. This is the core feature of Mott-Gurney transport. Prior to exposure a relatively low barrier (~0.2 eV for ChG) can typically be assumed (see left side Figure. 19). The inability to erase or further program the device after neutron exposure suggests that displacement damage may have greatly reduced the diffusivity of Ag^+ cations. Material changes that have occurred, that resulted in an increase in potential barrier height, preventing the cations from hopping to the next site (see right side Figure. 19). Localized Ag_2Se formation, recrystallization or a redistribution of the glassy structure may result in a deepening of the potential wells, E_o, occupied by the Ag^+, restricting the diffusivity of the ions. As Eq. 14 shows, an increase in E_o will reduce diffusivity, D_i, which will significantly reduce ion flux, i.e., transport. This will freeze the device into a fixed resistance state as the neutron data show.

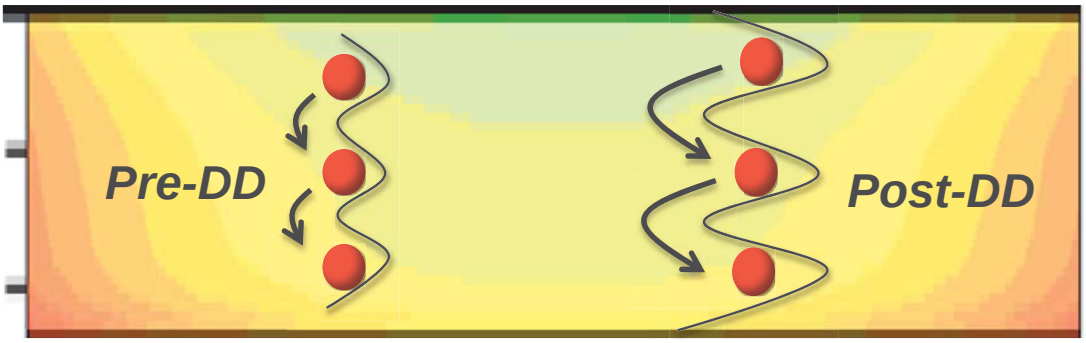


Figure 19. Conceptual illustration of effects of displacement damage

1.4.6. SEE Vulnerability for Two RRAM Architecture (1T1R and Crossbar) (Task 6)

The SEE vulnerability is associated with the RRAM array architectures. In general, there are two types of integrated RRAM array architectures. The first is the 1-transistor and 1-resistor (1T1R) array. In this configuration each RRAM device is in series with a transistor, as shown in Figure 20 (a). The use of selection transistors in the 1T1R enable the electrical isolation of RRAM devices from one to another. The second configuration is the crossbar array, which consists of rows and columns perpendicular to each other with RRAM cells sandwiched in between. Crossbar architecture consists of only RRAM devices without transistors in the array, as shown in Figure 20 (b). At the edge of the array, RRAM devices on the same word line (WL) or bit line (BL) share a common driver (e.g. CMOS inverter). A simple crossbar array suffers from a problem known as "sneak paths" that limits the array size, increases power consumption, and degrades write/read margins. Therefore, today's crossbar designs typically use stacked cell structures composed of 1-selector and 1-resistor (1S1R) in series. The Adesto's chip uses the 1T1R architecture, while the Panasonic's chip uses the crossbar architecture.

As mentioned above, single event upset (SEU) was experimentally observed during the dynamic read/write operation of both Adesto and Panasonic's chips, therefore it is necessary to perform device modeling and circuit simulations to further analyze the SEE susceptibility of the RRAM architectures. Our recent work [4] studied SEU in the 1T1R and crossbar architectures at the array level. It was demonstrated that 1) a single-bit upset could occur when a heavy ion strikes the drain of "OFF" transistors (with the blue color in Figure 20 (a)) along the selected bit line during SET operation in a 1T1R array; 2) multiple-bit upsets may occur when a heavy ion strikes the drain of an "OFF" transistor (either a PMOS or NMOS) on a driver at the edge of the crossbar array. The susceptible edge drivers in different locations from A to F are labeled different colors in Figure 20 (b).

In order to investigate the dependence of the numbers of upset cells on the incident ion linear energy transfer (LET), the PTM model for the 45nm bulk transistors is used to simulate the transistors in the drivers at the edge of the array. A physics-based RRAM SPICE model [5] that is fitted with IMEC HfOx RRAM and a radiation-induced photocurrent model are employed to perform the circuit simulations. Figure 20 (c) presents the single bit upset probability for HRS to LRS flipping as a function of the incident ion LET. The threshold LET is found to be 1.8 MeV*cm^2/mg from the SPICE simulations. Figure 20 (d) shows the multiple-bit upset simulation result for a 128 × 128 array when only one bit is written into the array. The multiple-bit upset in crossbar array is due to the voltage transient propagation along the word line or bit line, since there is no isolation in the crossbar array.

If we compare the 1T1R and the crossbar architectures, the crossbar array does not have transistor in the array (only at the edge), thus it has smaller sensitive area than the 1T1R array. On the other hand, the 1T1R only shows single-bit upset, the crossbar array may have multiple-bit upset, thus once the crossbar is struck, it would generate more bit errors. However, the threshold LET of the crossbar structure is much higher than that of the 1T1R structure. As the integral LET spectra for galactic cosmic rays is decreased exponentially with ion LET. As a result of all the aforementioned factors, our analysis shows that the crossbar architecture may present a better radiation hardness (SEE) as compared to the 1T1R architecture.

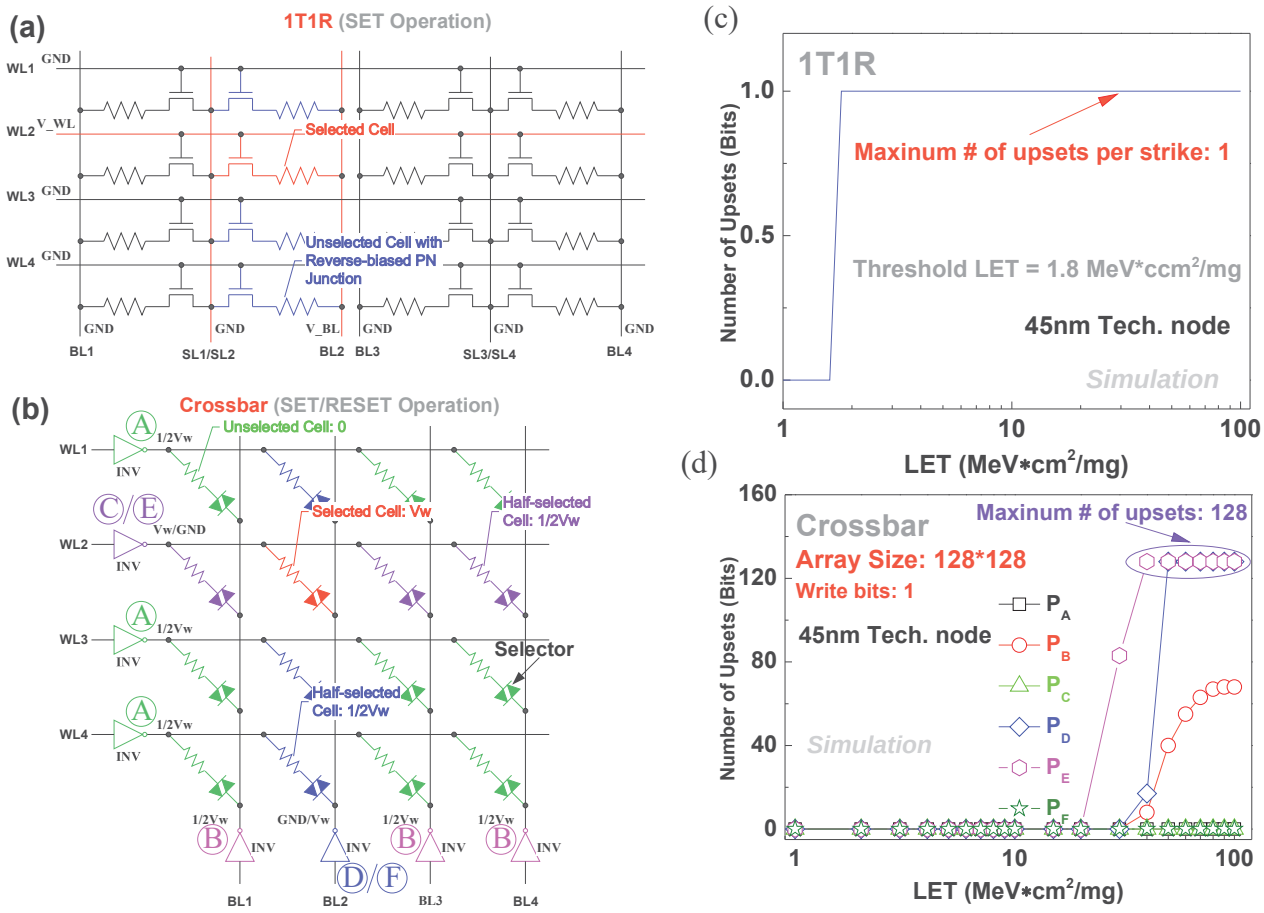


Figure 20. (a) Schematic of the 1T1R architecture (b) schematic of 1/2 bias scheme in the crossbar architecture (c) single bit upset from HRS to LRS due to SEE in 1T1R array (d) multiple bit upset from HRS to LRS or from LRS to HRS

1.4.7. Density Issues (Task 7)

MoAs the requirement for the future space electronic applications, it is necessary to achieve high density RRAM with both low power and high performance. There are many possible choices for array designs such as 1T1R and cross-bar array (X-bar) and so on. Here we would like to simply evaluate the feasibility of 1T1R array and X-bar array. For 1T1R array, it may cost an area of $6F^2$ (F stands for the feature size) for each bit and extra power supply is needed for turning the transistor on and off. So there should be some special considerations of leakage and power consumption of transistors. While for X-bar array, it will only cost an area of $4F^2$ for each bit and no extra power is needed. In addition, from the view of possible multiple-layer integration in the future, X-bar are quite feasible no matter simple stacking or 3D RRAM is to be utilizedm but for 1T1R array, as the limitation of the transistor fabrications, it could not sustain the multiple-layer integration.

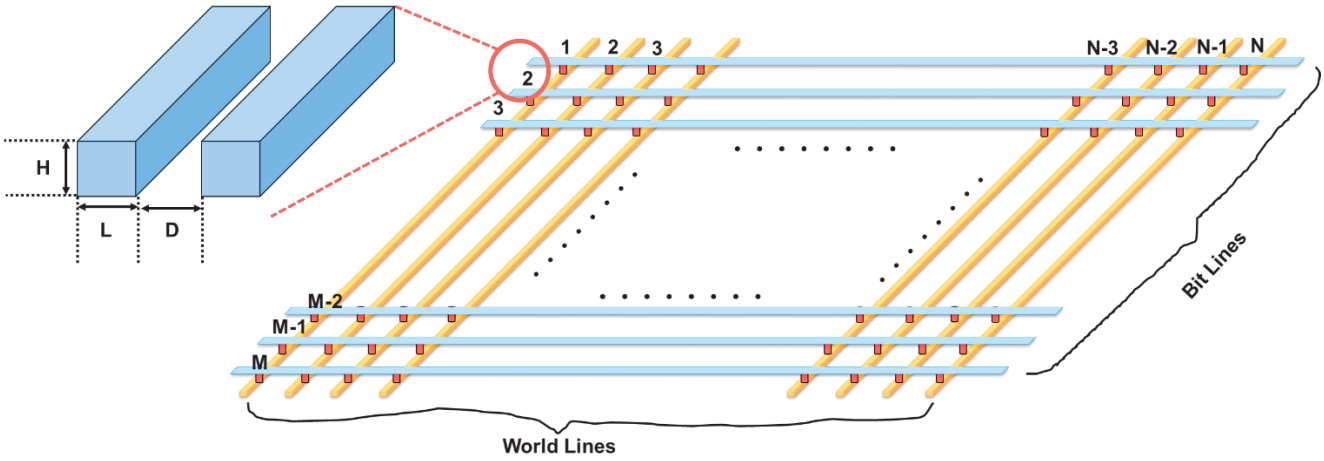


Figure 21. Schematic of the RRAM Cross-bar array

To further investigate the possibility of high-density RRAM array, minimum LRS and area cost will be evaluated. A schematic of M*N X-bar array is shown in Figure 21. The RRAM cells are located between every two crossing lines which represented as a pillar. As shown in the cross-section insert, L stands for both the width of the wire, D stands for the gap between the wires, and H stands for the height of the wire. According to the design rule used in the fab, L should be equal to D which might represent the technology node if fabricated via first metal layer. Meanwhile, the area ratio (H/L) shall be 2.

To consider the minimum LRS, a simple example is given. If a memory array with 64 Mb volume is to be built, an 8 kb world lines (vertical yellow) and an 8 kb lines (lateral blue) are needed. It is assumed that the signals all come from the left of the world lines (from decoder) and flow out from the bottom of the world lines (to sense amplifier). The worst-case cell is marked as N at the right up corner when it is in LRS and selected for operation. Firstly, to successfully complete the operation, a rule that at least 2/3 of the voltage applied from the decoder should drop on the selected cell has to be established. Next, the length of wire from decoder to the selected cell can be roughly estimated to be 2L*N where N is 8 kb mentioned before. Similarly, the length from the selected cell to sense amplifier is 2L*M. As M equals to N equals to 8 kb, the total length of the wire should be 4L*8 kb. Thus the total wire resistance along the path is roughly ρ_M*4L* 8kb/(2L*L) + R_{LRS}. In order to satisfy the rule established, a minimum of R_{LRS} of twice the total wire resistance is required.

On the other hand, the area cost is another factor that might limit the possibility of high density memory. It is assumed that driving circuits, decoder/encoder circuits, and sense amplifiers are all fabricated either underneath the first metal layer or separately on the other chips. So the minimum area of the X-bar can be simply calculated as $(2*(N+1)*L)^2$.

As shown in Figure 22, the results of minimum LRS and area cost of the X-bar arrays with the scaling of feature size are evaluated with the methods illustrated before.

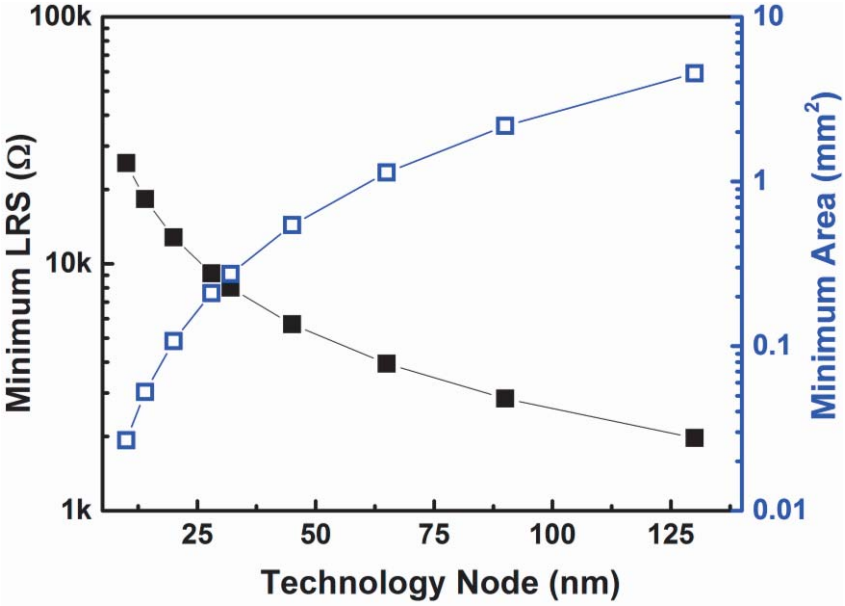


Figure 22. The minimum LRS requirement and area cost of the X-bar array with the scaling of the technology node

So, if the RRAM cells can satisfy the requirement mentioned here, it will be feasible to achieve the high density memory in the future. Of course, due to the requirement of RC latency and the capability of the cell selector to minimize of the sneak path, a 64Mb X-bar arrays may be partitioned into several sub-arrays with local decoder and driving circuits, for example, 16 sub-arrays with 2kb word lines and 2kb bit lines.

1.4.8. Cumulative Radiation Damage of High Density RRAM Arrays (Task 8)

In CBRAM a conductive filament is formed by controlling the migration of an electrochemically active metal, such as silver (Ag), through a solid electrolyte. As we have shown through the course of this research program, standard CBRAM technologies have a high tolerance to ionizing radiation, with TID exposure exceeding several Megarad of absorbed dose. Devices fabricated at ASU with Ag-$Ge_{30}Se_{70}$ electrolyte layers have demonstrated a suburb TID tolerance beyond 10 Mrad. This is likely do to the fact that these devices are fabricated with processing steps that include a photo-exposure cycle which introduces Ag into the film prior to TID exposure. We have also shown that Cu-SiO_2 devices have shown a tolerance to 7.1 Mrad (SiO2) [6]. These do not even require photo-doping for reasons we will discuss in thrust III. Commercially available Ag-GeS CBRAM is tolerant to a TID of 5 Mrad (Si).

In this section we present the results of neutron irradiations on Ag-$Ge_{30}Se_{70}$ devices. The solid electrolyte used is Ge30Se70 photo-doped with Ag. Testing was performed in situ using Cobham RAD Solutions' 14 MeV neutron generator. Packaged CBRAM devices were irradiated to a total neutron fluence of 3.19×10^{13} n/cm^2 (5.65×10^{13} n/cm^2 1 MeV neutron equivalent in Si) and periodically tested to evaluate their response. A die containing 32 individually accessible CBRAM cells was mounted and wire bonded into a ceramic dual in-line package (CDIP). A total of six cells were available for in situ testing. A ceramic lid was taped across the package opening

to protect the CBRAM from ambient light exposure. Prior to irradiation, a niobium foil was taped onto the lid for passive dosimetry, as shown in Figure 23.

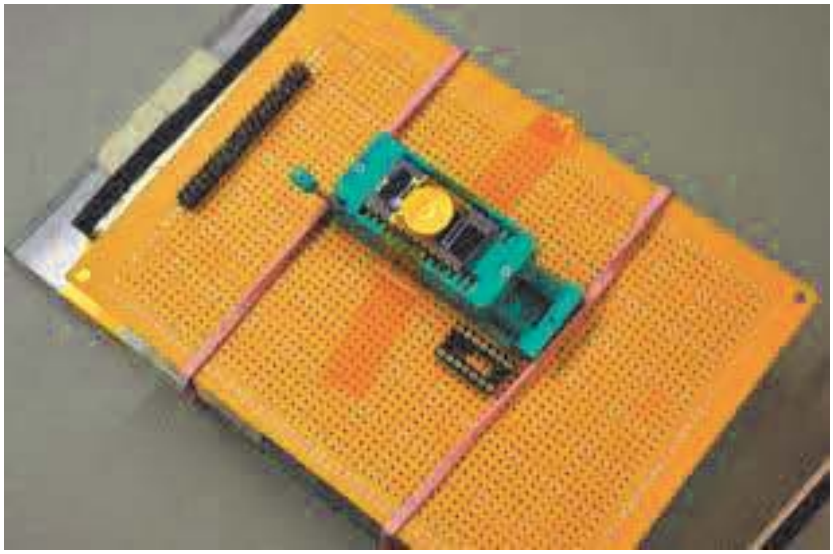


Figure 23. Test board used for securing and accessing the CBRAM during irradiation with dosimeter taped to front

An Aloka dosimeter mounted inside the radiation chamber was used for active dosimetry. The test board was mounted to a tripod and placed against the end of the neutron generator beam plate to ensure that the CBRAM received the highest possible neutron flux, as shown in Figure. 23. The CBRAM cells were accessible via ribbon cables that ran from the test board inside the chamber to a switch board outside of the chamber. The switch board allowed each CBRAM cell to be individually accessed and tested using an Agilent 4156A parameter analyzer. Prior to irradiation, each device was cycled five times using a DC staircase sweep to verify their functionality. The devices were swept between 0 V to 0.5 V then back to 0 V to program and 0 V to -0.8 V to 0 V to erase. A compliance current of 100 uA was used for five of the devices and a compliance current of 500 uA was used for the sixth device. The resistance states were determined by the current values at 20 mV. The devices were erased to a high resistance state during exposure. The devices were irradiated with a mean neutron flux of 2.18x109 n/cm2·s. During irradiation the anode and cathode terminals were biased to ground.

The HRS and LRS of the CBRAM cells was observed to converge with increasing 14 MeV neutron fluence. Figure 24 shows how the HRS and LRS was observed to decrease, with the HRS eventually shorting to the LRS. One of the devices exhibited a behavior where the LRS increased to converge with the HRS, as shown in Figure 25. All irradiated devices were not able to be switched at by the conclusion of the 3.19×10^{13} n/cm2 exposure. An erase sweep from 0 V to -3 V was applied to each device in an attempt to recover their HRS. The devices remained not switchable after performing the erase sweep, with no observable difference between the LRS and HRS. The behavior suggests displacement damage is occurring to the electrolyte layer, impeding the complete formation or dissolution of the filament. A possible explanation for this observed effects is that the neutrons, as we have seen possibly in protons previously, create new phase

structures in the ChG film which create deep binding sites for Ag rendering the ion unable to transport in the film, as discussed in the modeling section above.

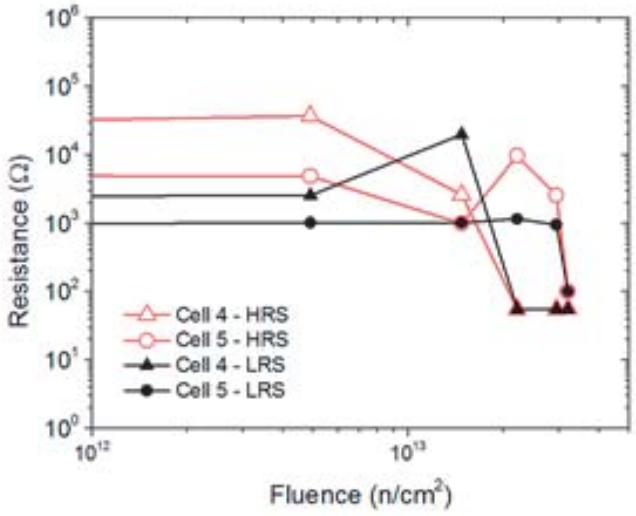


Figure 24. Mean HRS and LRS verses neutron fluence for CBRAM cells 4 and 5

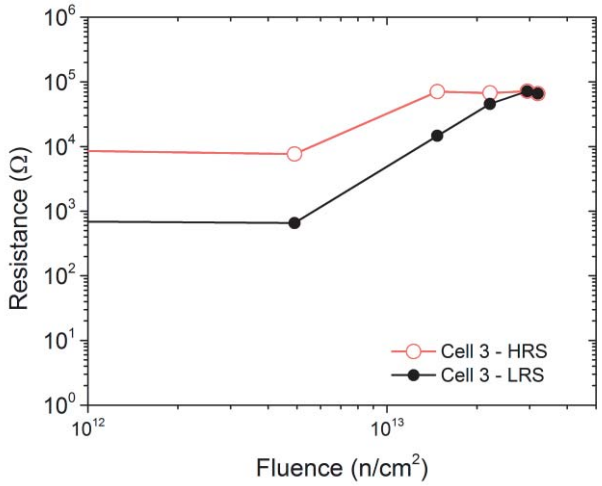


Figure 25. Mean HRS and LRS for CBRAM cell 3 verses neutron fluence

2. PROGRAM RESULTS IN YEAR 2

2.1. Summary of Year 3 results

Task 5 - CBRAM TCAD modeling was developed in Silvaco's Victory Device.

Task 6 - We have detemerminedit will be possible to meet the 128Mb density requirement by designing RRAM arrays in a cross-bar configuration integrated into the BEOL metal stack (Metal2, 3, or 4).

Task 7 - Back end of line (BEOL) implementation of CBRAM technology/PMC cells.

Task 8 - Analysis of combined total ionizing dose and displacement damage effects in CBRAM Cells ($Ge_{30}Se_{70}$RRAM).

Task 9 - We conducted electrical testing on Cu-SiO_2 RRAM arrays fabricated at both ASU and BRIDG. These results of these tests are discussed in year 3 section reporting.

Task 10 – Reported on system-level analysis of single event upset in RRAM architectures

2.2. Detailed Result in Year 2

2.2.1. RRAM Modeling (Task 5)

The following are the list of items currently being investigated:

- verify reactions, adding other reactions as needed
- reaction rates and activation energies
- species boundary conditions on the anode
- species properties (diffusion and activation energy)
- material parameters for electrolyte films.
- given 1D nature of the first pass at full TCAD simulation, we are trying to understand how and if it is necessary to added stochasticity to the model. This may be necessary to simulate fractal growth of filament
- geometric configuration in which metallic and semiconductor phases are separate but interleaved on a microscopic scale such that below a certain ratio of metal atoms to semiconductor atoms, the regions of metallic phase exist as disconnected +specks"

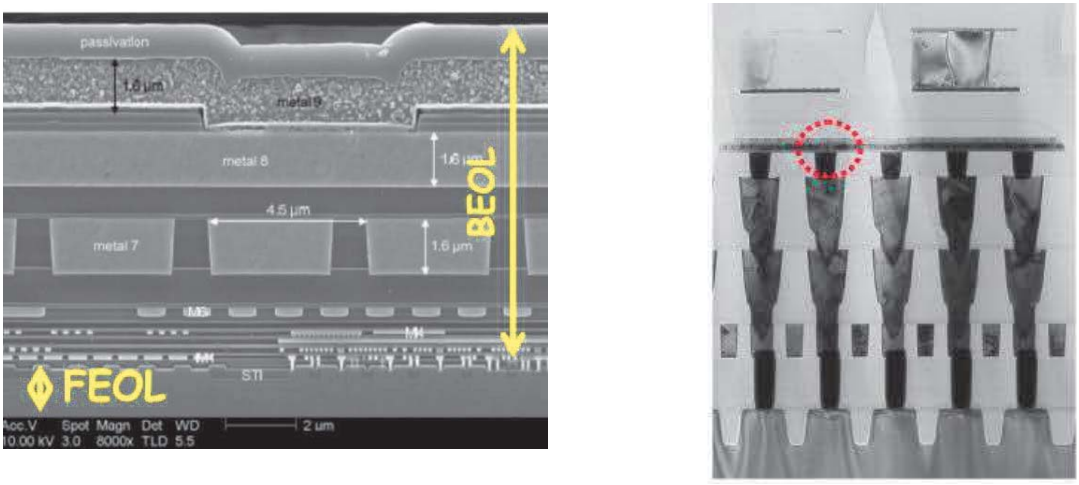
2.2.2. RRAM Architecture Assessment (Task 6)

To meet the 128Mb density requirement, the underlying CMOS technology node should be 180 nm or less. If a 180 nm technology is selected, based on the formula $Area = (2*(N+1)*L)^2$, where N is the number of word lines (assume 16k for a 256k memory) and L is slightly larger than the minimum feature size of 180nm, the total area of a 256 Mb chip will be less than 2 cm x 2 cm. Which is large but doable. We recommned moving forward with designing and building CMOS wafers in either the 180 nm or 130 nm nodes.

2.2.3. High Density RRAM Array Fabrication (Task 7)

CBRAM technology exploits the movement of cation through solid-electrolytes to provide non-volatile memory (NVM) cells. To be able to use such technology to manufacture a novel NVM radiation hardened memory there is a need to implement CBRAM memory cells in the back end of line (BEOL) of a CMOS circuit. The BEOL is the top layer of an IC, where metallization layers provide the interconnection between the transistors and the different parts of an IC.

Several IC manufacturers have demonstrated BEOL implementation of CBRAM technology, or RRAM technology in the last few years on an internal research basis. One company provides commercial products based on CBRAM technology (Adesto), illustrating the slow adoption but actual maturity that this novel technology is acquiring over the years. However, this technology is internally restricted to such companies and not directly available to AF designers and or applications. In addition, from a radiation effect perspective, if the CBRAM cells have demonstrated outstanding behavior during total dose and single event testing, the commercial ICs implemented with this NVM technology have also shown that the CMOS circuitry around such NVM cells would require some radiation-hardened by design (RHBD) to insure specifications typical of Air Force, DoD in general and space community needs for both the total dose effects and single event effects. The work conducted at ASU is an effort to develop a BEOL compatible process to support of radiation-hard RRAM IC with CBRAM devices. The BEOL region of the IC is shown in the cross-section photomicrograph in Figure 26a. The upper layers above metal 2, where the CBRAM cells are place can be seen in Figure 26b. The image was provided by one to the current manufacturers of commercial available CBRAM, Adesto Technologies.



(a) (b)

Figure 26. (a) Cross-section of an IC implemented in a 45 nm process, with the FEOL part and BEOL part identified and (b) CBRAM BEOL integration by Adesto Technologies

2.2.3.1. CBRAM process development for BEOL integration

A processing flow needs to conform to standard BEOL processing/manufacturing. This requires the CBRAM structures to be fabricated with processing tools currently running in foundry partners that specialize in split wafer fab manufacturing. As a results of this program Arizona State University (ASU, Arizona) is working with a potential BEOL foundry, BRIDG (Florida), to define an acceptable processing flow and to optimize it. The effort is targeting the use of plasma enhanced chemical vapor deposition CVD (PECVD) thin-films as the solid-state electrolytes for CBRAM devices.

An initial flow has been proposed and is under investigation. It includes over 80 manufacturing steps including chemical mechanical polishing (CMP) and dual-damascene processing to enable planarization and Cu interconnects to be implemented with five photolithography masks. Evolution/modifications of the processing flow will be made once the first batches of devices are produced, to further reduce the number of masks, number of processing steps, or improve alignments and the use of processing tools.

Five processing masks are used to build CBRAM device arrays. In a full split-fab manufacturing flow, fewer steps would be required since some of the front-end-of-line (FEOL) masks would be reused in the BEOL process.

A cross-section of the initial CBRAM device design is illustrated in Figure 27. Process control steps have been included in the processing flow with the goal of developing a qualified, 'fab' ready process. This processing flow is the first attempt at incorporation our CBRAM technology in an industrial BEOL process, at BRIDG. Discussions with BRIDG are ongoing to support the identification candidate selector device types (e.g., transistors) that may be included in the memory ICs.

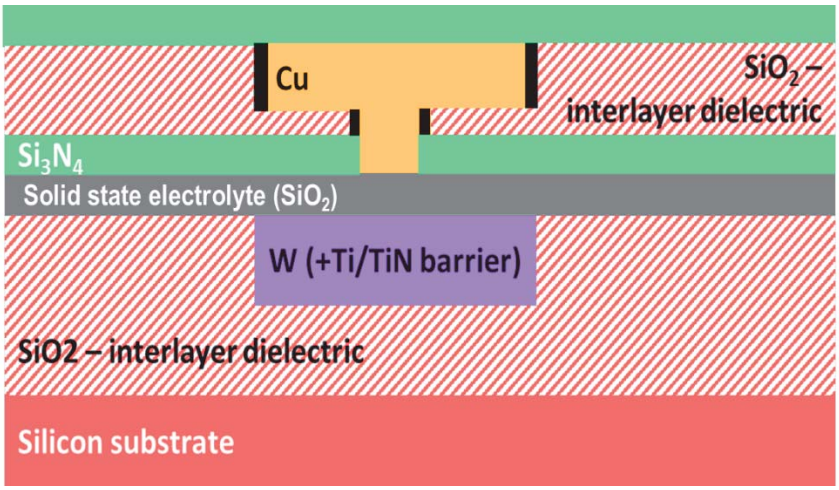


Figure 27. Illustration of RRAM device cross-section defining the material stack

2.2.3.2. Reticle design/Mask design

As mentioned above the process flow for the CBRAM devices require five masks. A 2cm by 2cm reticle has been designed with several structures printed with an i-line stepper. Standard alignment marks for i-line stepper tools have been added, as well as control features for checks occurring after every processing step. A description of test structures and arrays is provided below along a brief discussion of how higher density arrays may be manufactured.

The reticle, shown in Figure 28, consists of 16 different tiles of area 5mm by 5mm. Structures on the tile set, which are listed on Table 2, include: RRAM test structures, processing test structures, and arrays of RRAM devices.

Table 2. Description of reticle tiles

Tile	Description	Tile	Description
1	Test structure	9	Reduced cross-point array
2	cross-point array	10	Test arrays - small
3	cross-point array	11	cross-point array
4	cross-point array	12	cross-point array
5	Test structure	13	Multi cross-point array
6	cross-point array	14	Multi cross-point array
7	cross-point array	15	cross-point array
8	cross-point array	16	cross-point array

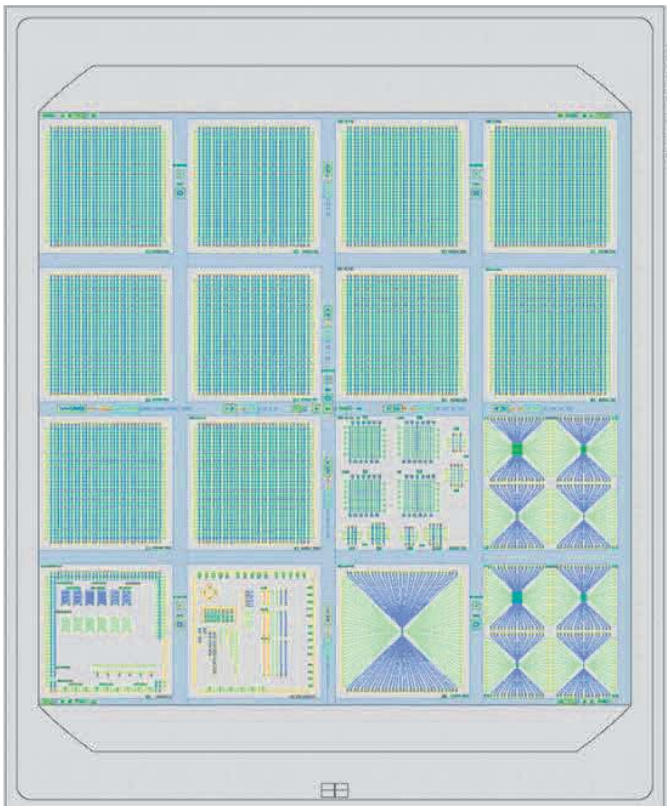


Figure 28. 2cm by 2cm reticle designed with 16 5mm by 5mm tiles consisting of various RRAM array and device geometries and process monitor structures

Two tiles are dedicated to stand-alone RRAM test structures implemented among others single RRAM devices. The remaining tiles consist of RRAM crosspoint arrays of different dimensions (number of rows and columns) and sizes, which define active RRAM device area, pitch between and width of metal lines. Arrays with the smallest metal pitch and metal width will enable us to assess the manufacturing capability at BRIDG and the foundry's maximum density achievable to meet targeted yields. It should be noted that measurements currently being conducted on wafers recently received from BRIDG (as of October 2018) represent the first lot though the foundry and likely do not represent the anticipated yields for future lots.

Figure 29 provides the layout of the corner of a representative RRAM crosspoint array. As the figure shows, the RRAM devices are defined by the via (CR) located at the intersection of a metal 1 (M1 in blue) and metal 2 (M2 in green) layer. Different feature sizes (pitch, metal and via dimensions) on the reticle tiles are given in Table 3. Dimensions are defined graphically in Figure 30. It should be noted that dimensions B and E are equal, A and G are equal, and all dimensions reported are in microns.

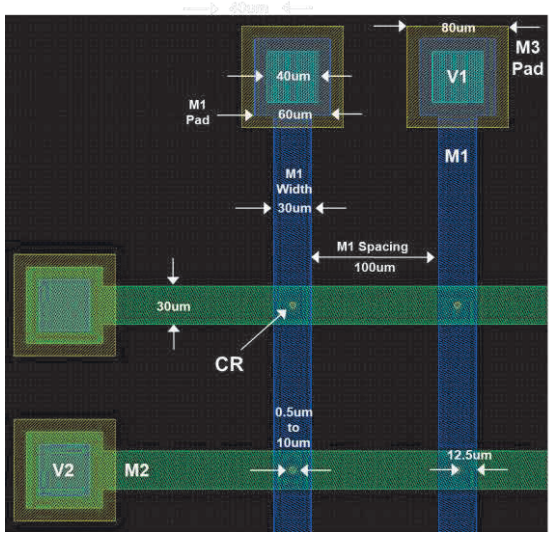


Figure 29. Layout of the corner of a representative RRAM crosspoint array

Table 3. Pitch, metal, and via dimensions of RRAM arrays on reticle tiles (all sizes in μm)

Cell (all sizes um)	Via Size (layer 12): D	Metal Width(M1 and M2): A and G	Metal Beyond Via: C	Metal Space / pitch: B and E
1st	10	14	2	10
2nd	5	7	1	5
3rd	2	4	1	2
4th	1	2	0.5	1
5th	0.5	0.9	0.2	0.5

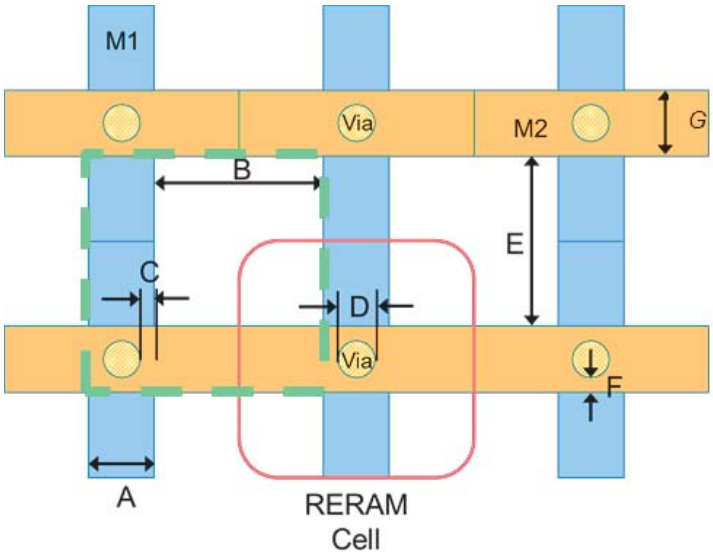


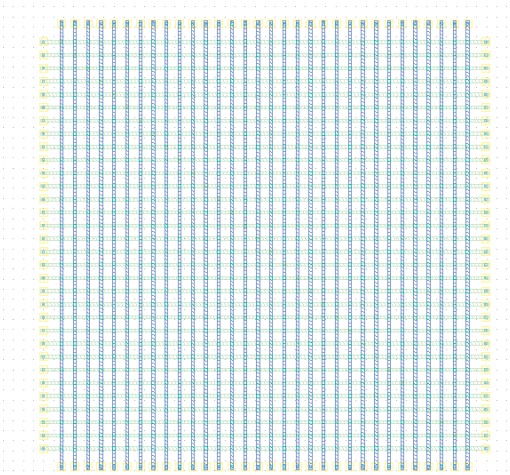
Figure 30. Graphical definition of of a RRAM array dimensions

The unit area for each RRAM device in an array cell is defined by the green dashed box in Figure 30. This area can be computed as (A+B)*(G+E) where if G=A and E=B equals $(A+B)^2$. The minimum A equals D+2C. Thus the areas per bit (the green square) are provided in Table 4 for the different arrays on the reticle (see Table 2). Table 3 reports the area per RRAM device (bit) in μm^2 and cm^2. This enables a straightforward computation of area (in cm^2) necessary to fabricate a 100Mb density array. For the minimal dimensions used in this design (via=500nm diameter = minimal feature size) the area of a 100 Mb RRAM array would be 1.96 cm^2.

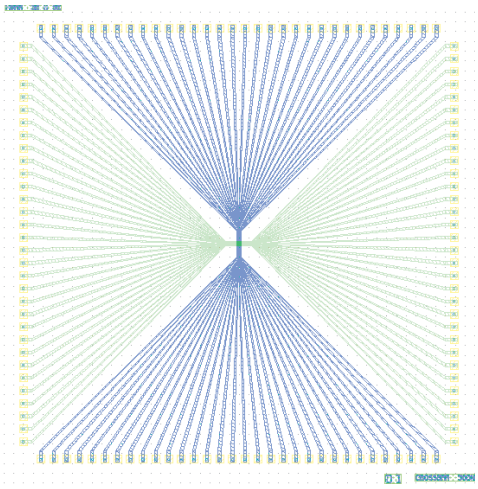
A closer view of some of the arrays is shown in Figure 31, where a relaxed sized array is illustrated in Figure 31a, an array with minimal dimensions is illustrated in Figure 31b, and array design to assess BRIDG manufacturing capabilities is illustrated in Figure 31c. The density increase obtained through array scaling is clearly visible when comparing Figures 31a and 31b.

Table 4. Cell area and array area for different sizing available on the reticle

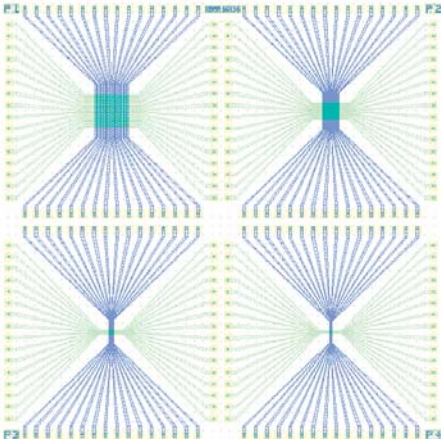
	Area (μm^2)/bit	cm^2/bit	cm^2/100Mbit
1st	$(14+10)^2=576$	$576\ 10^{-8}$	576
2nd	$(7+5)^2=144$	$144\ 10^{-8}$	144
3rd	$(4+2)^2=36$	$36\ 10^{-8}$	36
4th	$(2+1)^2=9$	$9\ 10^{-8}$	9
5th	$(0.9+0.5)^2=1.96$	$1.96\ 10^{-8}$	1.96



(a)



(b)



(c)

Figure 31. Illustration of different type of arrays available on the reticle: (a) relaxed sized array; (b) array with smaller dimensions; (c) series of arrays scaled down to towards minimal sizing

The design of this reticle mask is a first step towards the design and fabrication of a non-volatile, radiation hard, RRAM crosspoint memory. The same design and manufacturing tools needed to develop crosspoint arrays can be used for selector-based RRAM memories built with one transistor-one RRAM device (1T-1R) architectures NVM. For the 1T-1R memory we estimate the total area of the IC would be set by an array RRAM cells occupying 60% of the total IC area and control logic occupying close to 40% of the area, as illustrated in Figure 32.

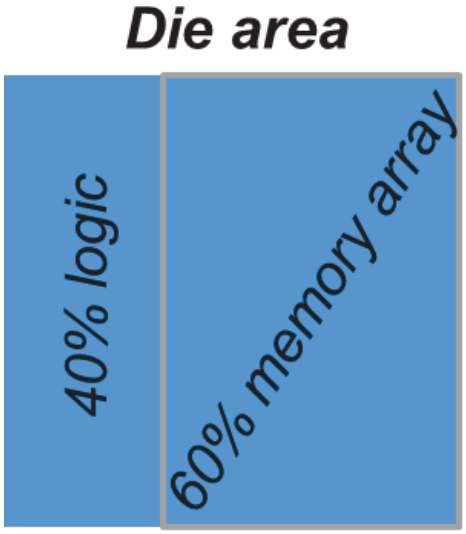


Figure 32. Estimated area partitioning in a RRAM based 1T-1R NVM memory

Using these estimates, a 100Mb NVM RRAM IC memory fabricated with a 500 nm pitch in upper metal layers require a die area of 3.3cm^2. This is set by the sum of the areas for the memory array occupying 60% of the area (2cm^2 for a 100Mb array) and an additional area for the control logic and I/O (1.3cm2 for CMOS). By the same calculation, a 64Mb NVM memory would be at 2.08cm^2. Processing was started at BRIDG in the summer of 2018. The first wafer lots were receive by ASU in October 2018. Figure 33 show one of the eight inches wafers fabricated by BRIDG and deliver to ASU.

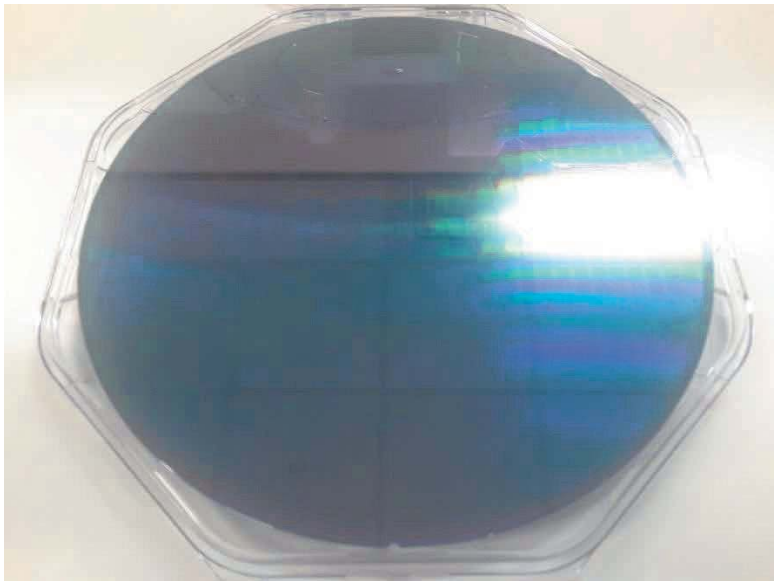


Figure 33. Photograph of wafers fabricated at BRIDG. Wafers lot pulled at photolithography mask 2 level

2.2.3.3. Technology transfer – process development

ASU has begun transferring technology to BRIDG. The RRAM process that is being delivered is a Cu-SiO_2 PECVD process. BRIDG has incorporated the process into its wafer line. Evaluations of materials, electrical operation, endurance, retention and yield of the RRAM technology are ongoing at ASU. Arrays of RRAM cells on 2 inch wafers manufactured at ASU and the 8 inch wafer fabricated by BRIDG are the test coupons currently being tested.

2.2.4. Cumulative Radiation Damage of High Density RRAM Arrays (Task 8)

Heavy ion irradiations were performed at the Ion Beam Laboratory (IBL) at Sandia National Laboratories. $Ge_{30}Se_{70}$ CBRAM crossbar 5 μm diameter devices were irradiated with 100 keV Li^+ ions using the NanoImplanter (NI) raster scanning focused ion beam. Similar studies are planned for the Cu-SiO_2 PECVD process in the coming year if yields are high enough. Prior to exposure the $Ge_{30}Se_{70}$ devices were placed under vacuum in the NI and probed. The devices were cycled with a DC current-voltage (I-V) sweep using an Agilent B1500 to verify that the devices operated correctly. Each device was programmed with a 10 mV staircase sweep from 0 V to 0.5 V and back to 0 V and erased with a sweep from 0 V to -0.8 V back to 0V. Three devices were erased into an HRS and three were programmed to an LRS with a 10 μA compliance current. A small (sub programming threshold) DC I-V read sweep from 0 V to 30 mV was used to sample the resistive state of the device before irradiation. Each device was exposed and tested individually. The 40 nm diameter Li beam was raster scanned in 40 nm steps over a 25 μm × 25 μm area over a device to a fluence of 10^{11} ions/cm^2. The device remained probed during irradiation with no bias applied. After irradiation, the 30 mV read sweep was applied to measure the state of the device. Exposures were continued in 10^{11} ions/cm^2 fluence steps to 10^{12} ions/cm^2 where the fluence was increased to 10^{12} ions/cm^2 steps and at 10^{13} ions/cm^2 the step was increased to 10^{13} ions/cm^2. A read sweep was performed on the device after each fluence step. The devices were irradiated up to a total fluence of 5×10^{13} ions/cm^2 or until the device shorted.

Three devices were irradiated with Tandem accelerated 1 MeV Ta ions. The devices tested have an Al contact offset from the area of the CBRAM cell; as depicted in the inset of Figure 34. The devices were wire bonded in a 24 pin DIP and placed on a circuit board inside the beam line with BNC accessible connections to an Agilent 4155 parameter analyzer. Two of the devices were DC cycled and erased into an HRS while the third device was cycled and programmed into an LRS with a 10 μA compliance current. The Ta ion beam was approximately 500 μm × 1000 μm and fully covered the device area, as shown in the beam profile overlay in Figure 34. During each exposure, a 50 mV read bias was applied to the anode contact with the cathode grounded.

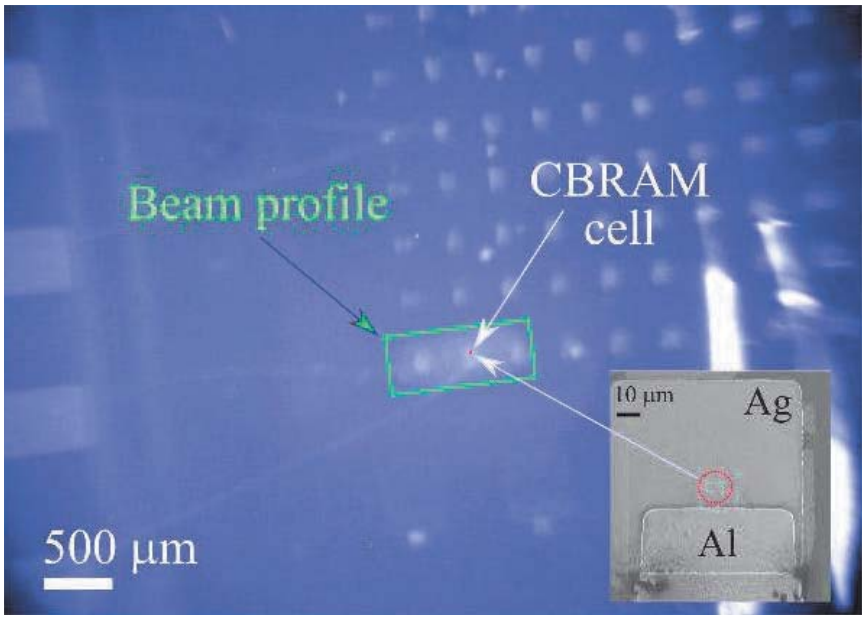


Figure 34. Overlay of the Ta-ion beam profile on exposed CBRAM device

The Stopping and Range of Ions in Materials (SRIM) calculator was used to estimate the TID deposited and the DD dose in the switching layer of the CBRAM devices. The linear energy transfer (LET) and non-ionizing energy loss (NIEL) values generated from SRIM were converted to TID and DD using the following equation:

$$TID\ [\text{rad}] = \text{LET} \cdot \Phi \cdot K \tag{16}$$

$$DD\ [\text{MeV} \cdot \text{g}^{(-1)}] = NIEL \cdot \Phi \tag{17}$$

where $K = 1.6 \times 10^{-8}\ \text{rad} \cdot \text{g} \cdot \text{MeV}^{-1}$ and Φ is the fluence in ions/cm^2.

For the Li ion exposure three devices were initially set to an HRS while three others were set to an LRS. The resistance state of the six devices versus the accumulative Li ion fluence is shown in Figure 35. The TID calculated using SRIM is marked on the top x-axis. Devices programmed to an HRS are plotted with dotted lines while the devices set to an LRS are solid lines. Of the devices programmed to an LRS only device 3 shorted after a fluence of 3×10^{13} ions/cm2. Devices 1 and 2 failed to retain their initial state after a fluence of 10^{13} ions/cm2 but they did not short. For the three devices programmed to an HRS devices 5 and 6 were shorted to an LRS. Device 5 shorted at a fluence of 2×10^{13} ions/cm2. Device 6 decreased in resistance after a fluence of 3×10^{12} ions/cm^2 and shorted after 3×10^{12} ions/cm^2. Device 4 did not transition to an LRS but decreased slightly in resistance after a fluence of 10^{13} ions/cm^2.

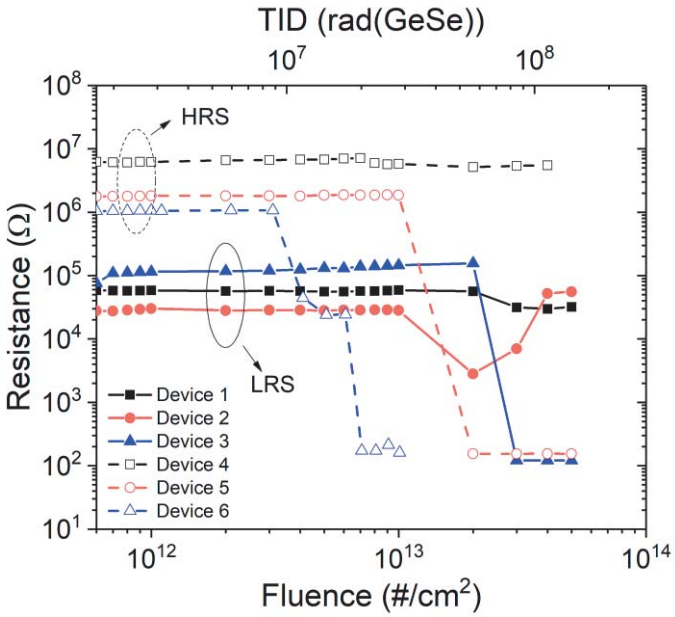


Figure 35. Resistive state of CBRAM devices during 100 keV Li bombardment

The post resistance state after each pulse versus accumulative fluence is plotted in Figure 36 for the 1 MeV Ta-ion exposure. Devices 1 and 2 were set to an HRS prior to exposure and device 3 was set to the LRS. Both devices in the HRS transitioned to a lower resistance after a fluence of 10^{12} ions/cm^2 and $3x10^{12}$ ions/cm^2 for devices 2 and 1, respectively. The device in an LRS was only tested up to 6×10^{11} ions/cm^2 with no significant change in resistance observed.

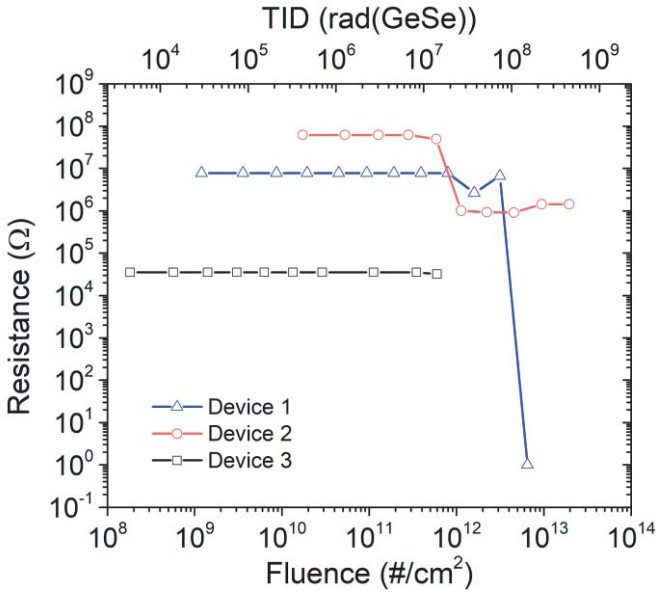


Figure 36. Resistive state of CBRAM devices during 1 MeV Ta-ion bombardment

$Ge_{30}Se_{70}$ CBRAM devices were also bombarded with 200 keV Si ions. In that experiment, a fluence was selected such that the resistance state decreased during each beam scan and was

measured *in situ* during the scan with a 30 mV read bias applied to the anode. The initial resistance state along with the final resistance state of each scan was extracted and plotted in Figure 37 versus ion fluence. It should be noted that the fluence used in these earlier Si ion measurements were significantly larger than the Li and Ta tests.

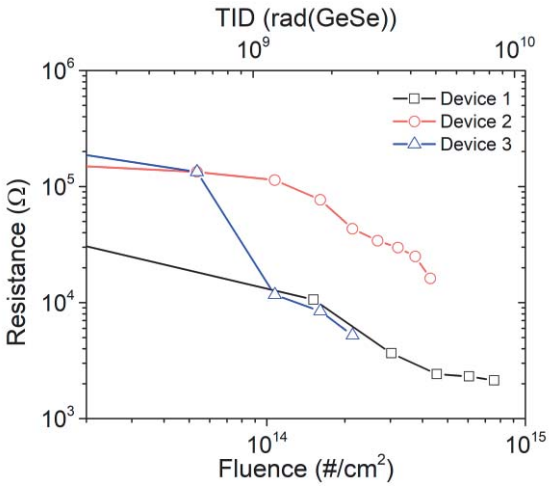


Figure 37. Resistive state of CBRAM devices during 200 keV Si-ion bombardment

The calculated TID is also plotted on the top x-axis. Using the TID and DD values of the 100 keV Li, 1 MeV Ta, and 200 keV Si irradiations, Figure 38 was constructed to assess if TID or DD played the greater role in the observed radiation effects. This figure reports the TID and DD value at the fluence of the last stable resistance state prior to the resistance decreasing. The 1 MeV Ta ions are shown to produce 10 times the DD as the 100 keV Li ions but both sets of devices experienced resistance decreases within the same magnitude of TID.

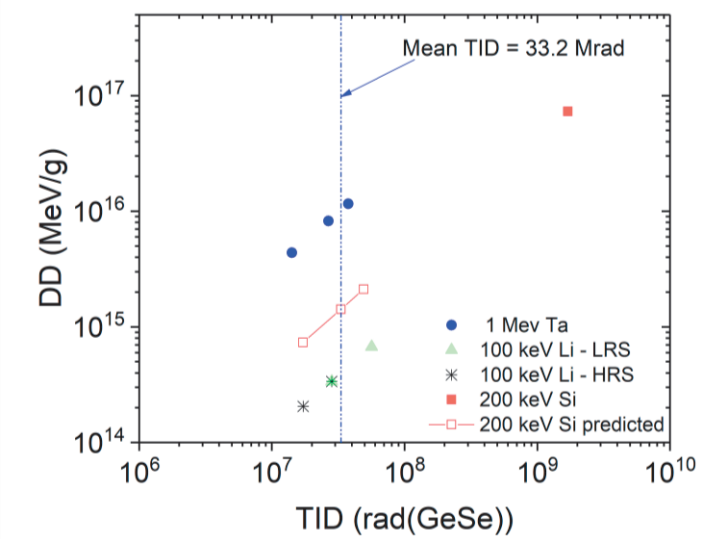


Figure 38. Displacement damage and TID in devices. TID has the most significant impact, with a mean threshold (blue dotted line) of 33.2 Mrad (GeSe)

This analysis suggests that the observed changes were in fact an ionization effect, although this is still under investigation. Based on the results of the Ta and Li exposures, the mean TID threshold for resistance change was found to be 33.2 Mrad(GeSe). In the case of the 200 keV Si tests, the first exposure resulted in a decrease in resistance state. Though the fluence threshold for a resistance change was not captured with the experiments, these data are included to verify that the TID and DD received falls above the predicted TID threshold for resistance change. In combination with the Ta and Li data the 33.2 Mrad(GeSe) threshold result can be used to predict the approximate fluence of 200 keV Si ions necessary to observe a resistance change. Based on the results of Figure 13, resistance changes due to 200 keV Si bombardment are expected to occur between 10^{12} ions/cm^2 to 4×10^{12} ions/cm^2. Future work on Cu-SiO2 RRAM will be conducted to assess whether similar cumulative damage response characteristics will hold for a different material system.

2.2.5. Electrical Experiments on High Density RRAM Arrays (Task 9)

We conducted electrical testing on Cu-SiO_2 RRAM arrays fabricated at both ASU and BRIDG. These results of these tests are discussed in year 3 section reporting.

2.2.6. Heavy Ion Testing/SEE Characterizations of RRAM Arrays (Task 10)

2.2.6.1. 1T1R and Crossbar Design

In general, there are two types of integrated RRAM array architectures. The first configuration is the 1T1R array. In this configuration each RRAM device is in series with a cell selection transistor. The bit lines (BLs) are connected to the RRAM anodes (top electrodes) and the drain contacts of the selection transistors are connected to the RRAM cathodes (bottom electrodes). The word lines (WLs) control the gates of the selection transistors. The use of selection transistors in the 1T1R enable the electrical isolation of RRAM devices from one to another (see Figure 39(a)). The minimum cell area for the 1T1R architecture is $6F^2$ (F is the lithography feature size) if a minimum size transistor is used with aggressive borderless DRAM design rules. If standard RHBD techniques are applied, we would expect an increase in 1T1R to be less that 12F2 consisted with the standard < 2X penalty specified for RHBD CMOS. However, it should be noted that this 2X penalty may be significantly less given the fact that the BEOL RRAM geometry is likely the limiting factor in 1T1R sizing.

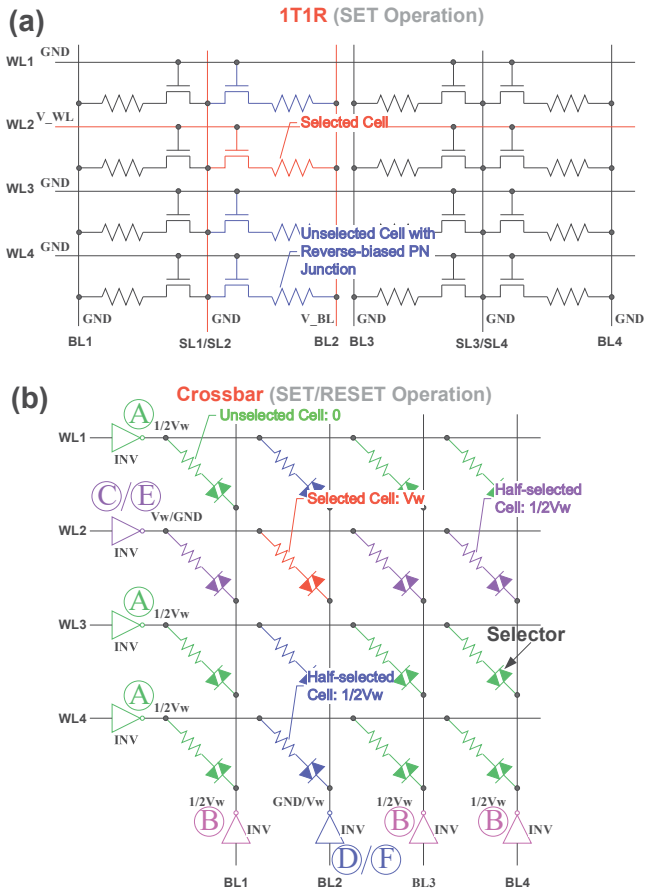


Figure 39. (a) Schematic of the 1T1R architecture and (b) of 1/2 bias scheme in the crossbar architecture

The second configuration is the crossbar array, which consists of rows and columns perpendicular to each other with RRAM cells sandwiched in between (see Figure 39(b)).

The crossbar architecture can achieve a smaller footprint of $4F^2$, thus it can support a higher integration density. Crossbar architecture consists of only RRAM devices without selection transistors in the array. At the edge of the array, RRAM devices on the same word line (WL) or bit line (BL) share a common driver (e.g. CMOS inverter). A simple crossbar array suffers from a problem known as "sneak paths" that limits the array size, increases power consumption, and degrades write/read margins. Therefore, today's crossbar designs typically use stacked cell structures composed of 1-selector and 1-resistor (1S1R) in series. The use of two-terminal selector devices with strong I-V nonlinearity has been shown to significantly suppress sneak currents. In the recent years, industrial development has led to various prototype chips, e.g. ITRI's 4Mb HfOx 1T1R array, Panasonic's 8Mb TaOx crossbar array and SanDisk/Toshiba's 32Gb MeOx crossbar array. Figure 39(b) shows a schematic of 4×4 1S1R crossbar array architecture, with the word lines (WLs) connected to the RRAM anodes (top electrodes) and bit lines (BLs) connected to the RRAM cathodes (bottom electrodes). We have already reported test results on the Panasonci technology (see AY2016 report). We have yet to get access to the SanDisk/Toshiba technology.

2.2.6.2. Programming Scheme

The write operation includes two processes, SET and RESET. In the 1T1R architecture, the WL of the selected cells are set to a positive voltage (i.e. V_WL) to make sure the selection transistor is "ON" when a cell is being written (SET) or erased (RESET). In the SET operation, the selected BL is fixed to a positive voltage of V_BL and source line (SL) is grounded (Figure 39(a)). In the RESET operation, the selected BL is grounded and the selected SL are biased by a positive voltage of V_SL. The other unselected WL, SL and BL are all grounded. In the crossbar architecture, the 1/2 bias scheme is usually employed. In this scheme, unselected WLs and BLs are all biased to half write voltage Vw/2, while the selected WL and BL are biased to full write voltage Vw and 0 V for the SET operation, 0 V and Vw for the RESET operation, respectively. Therefore, during either SET or RESET, some cells share either WL or BL signals with the selected cell. These "half-selected" cells are colored as purple (WL shared) or blue (BL shared) in Figure 39(b). As these "half-selected" cells are biased, they suffer certain degree of undesired write disturbance. All the unselected cells sharing neither WL nor BL with the selected cell will have 0 V applied across the electrodes if neglecting the interconnect wire resistance. In this work, we will focus on the 1/2 bias scheme for the crossbar architecture.

2.2.6.3. Susceptibility Analysis

It is known that the transistor's reverse biased drain to body PN junction is the most sensitive strike location in bulk CMOS technology. When the junction is struck by a high energy particle, electron/hole pairs generated in this sensitive region will cause photo-current flow.

In the 1T1R architecture, each RRAM device has a selection transistor in series. The susceptible RRAM are the cells in blue in the same column as the selected cells being written (see Figure 39(a)). In the SET operation, the sensitive locations are the drain-body junctions tied through unselected RRAM devices to the selected BL. The generated holes will sink to the body of the transistor, while the electrons will be collected to the drain of the transistor. Therefore, ion-induced positive photo-current will flow through the RRAM cell from anode to cathode. Depending on the magnitude of current, voltage on the cathode might be pulled down even to a negative potential. This could cause a suitably high positive voltage differential between anode and cathode thereby making an RRAM cell susceptible to HRS to LRS flipping. However, in the RESET operation, the sensitive locations are source-body junctions tied to the selected SL. A negative photocurrent is generated only for the angular strike. This is because there is a parasitic bipolar effect caused by the forward biasing of body-drain junction. This may cause a spurious transition from LRS to HRS under extreme circumstances. No LRS to HRS upset was shown in experiments. This suggests the flipping from LRS to HRS has a very small possibility in the 1T1R structure. Therefore, in this work, only HRS to LRS transition with normal incidence strike is considered for the 1T1R architecture at the system level analysis.

Table 5. Sensitive Transistors and Potential Upset Types

Process	Driver (Inverter)	Bias	Off Transistor	Upset Type	Upset Bits
SET	A	1/2Vw	NMOS	LRS -> HRS	P_A(LET)
	B	1/2Vw	NMOS	HRS -> LRS	P_B(LET)
	C	Vw	NMOS	LRS -> HRS	P_C(LET)
	D	GND	PMOS	LRS -> HRS	P_D(LET)
RESET	A	1/2Vw	NMOS	LRS -> HRS	P_A (LET)
	B	1/2Vw	NMOS	HRS -> LRS	P_B (LET)
	E	GND	PMOS	HRS -> LRS	P_E(LET)
	F	Vw	NMOS	HRS -> LRS	P_F(LET)

In the crossbar array, there are drivers (CMOS inverters) at the edge of the array to drive WLs and BLs. Any "OFF" transistor of the driver has a reversed biased PN junction that may be struck by an incident ion. If an incident particle strikes the drain of the "OFF" transistor (PMOS or NMOS), a transient voltage spike is generated at the output of the driver. This voltage spike may propagate along the WL or BL since there is no isolation between RRAM cells in the crossbar array. The net voltage difference across RRAM cells can be either positive or negative depending on whether the PMOS or the NMOS of the driver is struck. This means both HRS to LRS and LRS to HRS upsets can occur with roughly the same probability. Table 5 summarizes all possible sensitive transistors ("OFF" transistors) and upset types during SET or RESET operation in the crossbar architecture. Drivers A and B are the drivers with outputs of Vw/2 on the rows (WL) and columns (BL), respectively, in both SET and RESET operations. Drivers C and E are WL drivers with outputs of Vw in SET and ground in RESET, respectively. Drivers D and F are BL drivers with output of ground in SET and Vw in RESET, respectively. The descriptions of the driver categories can be referred to Figure 39(b). As the generated voltage transient propagates across all the cells along a given WL or BL, it has the possibility to cause multiple-bit upsets (MBUs). However, due to parasitic capacitances, wire resistances and the loading effects of other cells, the generated spike amplitude attenuates as it propagates. Thus only the cells that are close to the driver from the edge are susceptible to the upset. Depending on the incident ion LET, different numbers of cells may experience upsets, namely, from PA (LET) for Driver A to PF (LET) for Driver F.

In order to investigate the dependence of the numbers of upset cells on the incident ion LET, the predictive technology model (PTM) for the 45nm bulk transistors is used to simulate the transistors in the drivers at the edge of the array. A physics-based RRAM SPICE model and radiation-induced photocurrent model used in prior work is employed to perform the circuit simulations. As the MBU effect only occurs in the low-voltage operation, the write voltage (Vw) is designed to be 1 V by changing the activation energy of an oxide material in the RRAM SPICE model. Table 6 shows the voltage biases with same RRAM oxide material during SET and RESET operations in the 1T1R and crossbar architectures.

Table 6. Voltage Biases in Each Architecture

	1T1R			Crossbar
Process	V_WL (V)	V_BL (V)	V_SL (V)	VDD (V)
SET	0.7	1.0	0	1.0
RESET	1.6	0	1.1	1.0

As mentioned above, only SBUs are assumed to occur when a heavy ion strikes the cathode node of RRAM during the SET operation in a 1T1R structure. Figure 40(a) presents the simulated single cell upset probability for HRS to LRS flipping as a function of the incident ion LET. The threshold LET is found to be 1.8 MeV*cm2/mg from the SPICE simulations. The threshold LET is generally affected by a few factors in RRAM memory: 1) the sensitive area, which decides the magnitude of ion-induced photo-current and the net voltage differential across RRAM; 2) the intrinsic switching voltage of RRAM, which determines how much net voltage across RRAM can flip its desired state; 3) the applied voltage on BL, which will determine how much voltage transient is required to cause enough voltage difference on the RRAM. Our prior work presented a larger LET at a given applied voltage on BL. For example, the threshold LET of 1T1R was around 4 MeV*cm2/mg in our prior work and it might be less than 1 MeV*cm2/mg at a given BL voltage of 2 V. This is because the sensitive area or size of access transistor used in our work (i.e. W = 135 nm, L = 45 nm) is much smaller than that in previous work (i.e. W = 1 μm, L = 100 nm). The threshold LET in this work (1.8 MeV*cm^2/mg) is decreased from our prior work. The reason is that the RRAM switching voltage is reduced by changing the activation energy of an oxide material in the RRAM SPICE model.

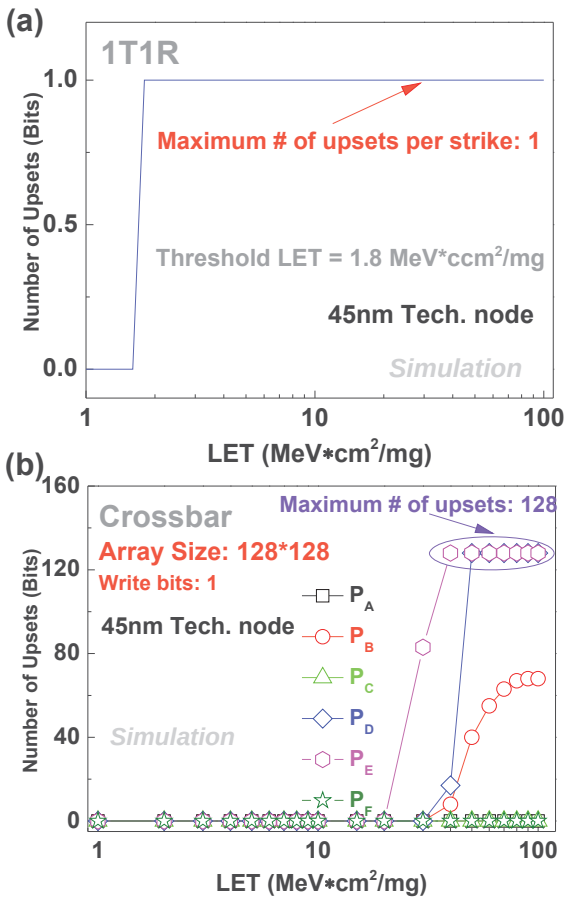


Figure 40. (a) Single bit upset from HRS to LRS due to SEE in 1T1R array and (b) MBUs from HRS to LRS or from LRS to HRS

For the crossbar architecture, a state-of-the-art FAST selector, which shows excellent nonlinear I-V characteristics, is chosen to suppress parasitic sneak paths in unselected cells. With the help of the selector, the off-resistance (ROFF) of the "half selected" cells is assumed to be 109 Ω in the SPICE simulation. As mentioned earlier, both HRS to LRS and LRS to HRS flipping can occur in the crossbar architecture. In order to quantify the number of upsets of either type that may occur, SPICE simulations were performed on arrays programed with two data patterns. One array was preprogrammed with all the cells in LRS (~100 kΩ) to get the number of upsets from LRS to HRS. The other one was preprogrammed with all the cells in HRS (~1 MΩ) to obtain the number of upsets from HRS to LRS. In the crossbar array simulation, the parasitic capacitances and wire resistances (for 45nm node) are taken into consideration. Figure 40(b) shows the MBU effect simulation result for a 128 × 128 array when only one bit is written into the array. It indicates that the number of upsets increases as the incident ion LET increases. This can be attributed to the larger voltage spike generated at the output of the driver when the incident ion LET is larger. It also suggests that the number of upsets strongly varies with the types of drivers being struck. First, Drivers A and B (Figure 39(b) and Table V) have the same output voltage of 1/2 Vw and sensitive transistor (i.e. NMOS). A strike on the NMOS drain of driver A on the row

can cause LRS to HRS upset. However, a strike on the NMOS drain of driver B on the column can cause HRS to LRS upset. The number of upsets, PA, is smaller than PB for a given LET due to a lower switching voltage from HRS to LRS in the RRAM model. The difference between PD and PE has a similar explanation. Compared to PB, PE presents more upsets because the drain area of PMOS is larger than that of NMOS which results in larger photocurrent and larger voltage spike. Finally, PF has a smaller number of upsets compared to PB for a given LET because higher WL voltage (i.e. Vw) requires higher photocurrent to pull it down to a certain voltage.

In addition, we found that the quality of selector will also affect the number of upsets in the crossbar architecture. Figure 41 shows the number of upsets under the PB condition for different threshold selector with different ROFF resistances. The result suggests that a selector with higher off-resistance is desired in the design of crossbar memory for stronger radiation hardness. If we compare the 1T1R and the crossbar architectures, the crossbar architecture generally presents a higher threshold LET than the 1T1R architecture.

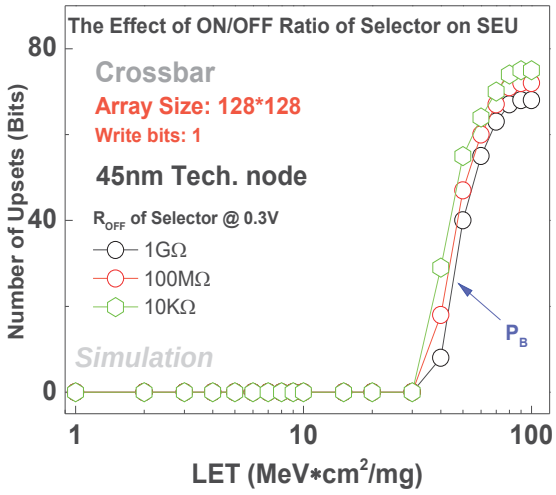


Figure 41. The number of upset bits increases as the lower quality threshold selector with lower OFF resistance is employed

2.2.6.4. Single Event Upset (SEU) Rate

Since the number of upsets varies significantly with the types and locations of transistors being struck and the states of RRAM cells, especially in the crossbar architecture, we have to consider all the strike scenarios. In order to obtain an "expected" number of upset cells when an incident ion strikes a sensitive transistor, the average number of upsets is calculated by considering the probability of each strike.

In the 1T1R architecture, it has been assumed that an SEU only occurs during the SET operation. Due to the selection transistor, only one bit may be flipped when a heavy ion strikes one of the sensitive locations. Then the average SEU rate (number of upsets) is

$$R_{SEU} = P_{SEU\_SET}\rho_{HRS}\rho_{SET}W_B \quad (18)$$

where P_{SEU_SET} is the number of bits, either zero or one, flipped for a given ion LET (see Figure 40a), ρ_{HRS} is the probability that a RRAM cell not accessed and in the same column is in HRS, ρ_{SET} is the probability that a cell programming process is performing the SET operation, and W_B is the number of bits to be written in parallel into the array in each address loop. The value for W_B determines the number of BLs being activated in the SET operation. The average SEU rate for the 1T1R architecture is not dependent on the sub-array size because it only involves SBUs.

In the crossbar architecture, an SEU can occur during both SET and RESET operations. Due to the MBUs, the number of upsets is dependent on the size of sub-array (i.e. N × N) and the number of activated BLs (i.e. W_B) in both SET and RESET operations. During SET operation, when an ion hits one of the "OFF" transistors, the average SEU rate in an N × N array is

$$R_{SEU\_SET} = [(N-1)P_A\rho_{LRS} + (N-W_B)P_B\rho_{HRS} + P_C\rho_{LRS} + W_BP_D\rho_{LRS}]/2N \quad (19)$$

where ρ_{LRS} is the probability of a RRAM cell in LRS. Similarly, the average SEU rate for the RESET operation is

$$R_{SEU\_RESET} = [(N-1)P_A\rho_{LRS} + (N-W_B)P_B\rho_{HRS} + P_E\rho_{HRS} + W_BP_F\rho_{HRS}]/2N \quad (20)$$

If the probability of a write process performing SET is ρ_{SET} and performing RESET is ρ_{RESET}, then the average SEU rate in a write process in the crossbar architecture is

$$R_{SEU} = R_{SEU\_SET}\rho_{SET} + R_{SEU\_RESET}\rho_{RESET} \quad (21)$$

where,

$$\rho_{LRS} + \rho_{HRS} = 1 \quad (22)$$

$$\rho_{SET} + \rho_{RESET} = 1 \quad (23)$$

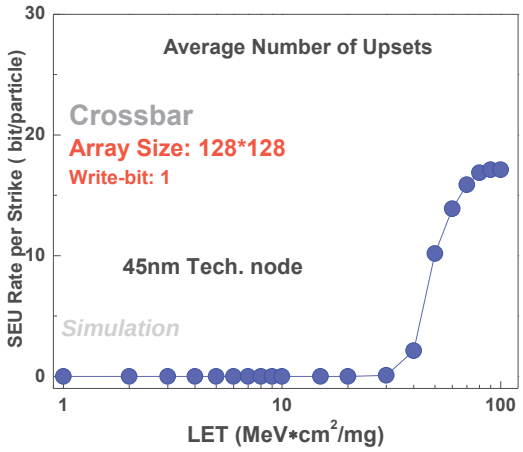


Figure 42. Average SEU rate in a 128 × 128 array with one bit written in the crossbar architecture

We assume that RRAM cells have the equal probability to be in HRS and LRS and the SET operation has the same frequency as the RESET operation. Thus, the average SEU rate in the 1T1R and in the crossbar can be determined using the above equations. Figure 42 shows the average SEU rate of a crossbar array with a size of 128 × 128 when only one bit is written into the array. In practice, the size of the driver is varied with array size and the number of bits to be written into an array simultaneously in one address loop. Table 7 shows the size of the NMOS of the driver for crossbar arrays with different array size and different numbers of bits to be written in parallel into an array. The PMOS of the driver is twice as large as the NMOS. In the photocurrent model, the photocurrent will scale with drain area of the device when the drain width and length are smaller than 200 nm, which is comparable with the ion radius (~100 nm). Figure 43(a) shows that the SEU rate increases with more bits written into an array in parallel. This is mainly because a larger driver is used to provide enough drive current when more bits are written into an array simultaneously. For a given incident ion LET, the larger driver can generate larger photocurrent and incur larger transient voltage on the output of the driver, resulting in more upsets. The driver size may also be increased with larger array size. However, the parasitic resistances and capacitances of the wires and the loading effect of other cells increase with the array size as well. As a result, the generated spike attenuates faster as it propagates along WL or BL in a larger array than that in a smaller array. Therefore, a trade-off exists between SEU rate and array size in the crossbar architecture. The 256 × 256 array presents the lowest SEU rate, as shown in Figure 43(b).

Table 7. Sizing the Drivers of Crossbar with Various Array Size at 45nm

Array Size	Number of Activated Cells in an Array	W/L of NMOS
128 × 128	1	1
	4	1
	16	3
256 × 256	1	1
	4	2
	16	4
512 × 512	1	2
	4	3
	16	6

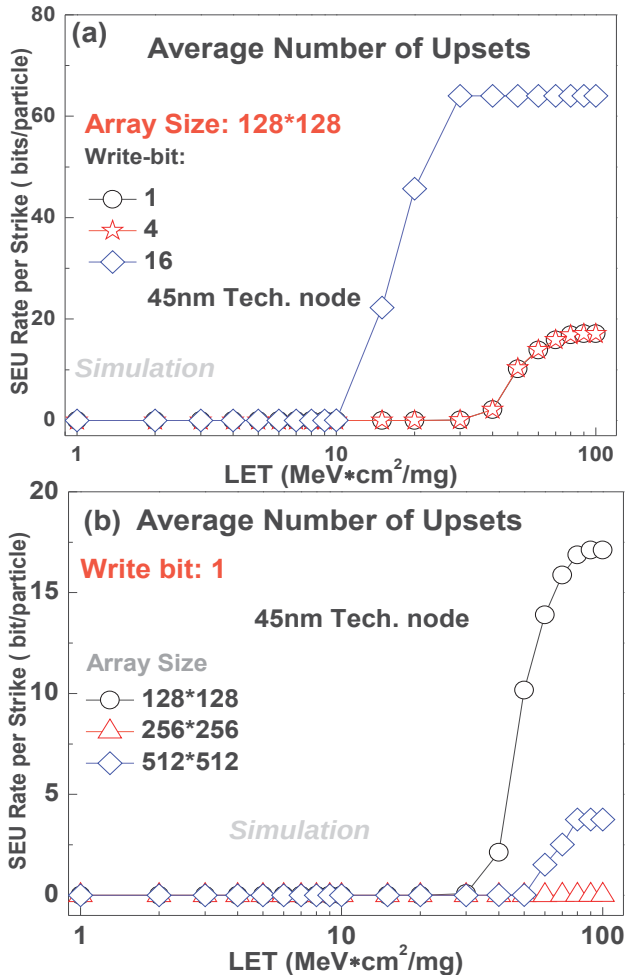


Figure 43. (a) Average SEU rate increases with increasing the number of bits to be written in the 128 × 128 array and (b) average SEU rate varies with array size for given number of bits written

2.2.6.5. Bit-Error-Rate/Day Calculation

Bit-Error-Rate (BER) per day at the system level caused by SEU can be calculated by integrating the SEU rate, the ion flux, the sensitive area and the susceptible time window as

$$BER.Day(LET) = \iint R_{SEU}(LET)\phi(LET)dAdt \quad (24)$$

where $R_{SEU}(LET)$ is the SEU rate (from Eq. (18) for 1T1R or (21) for crossbar), $\phi(LET)$ is the integral ion flux. The susceptible time window is only when the programming operation (either SET or RESET) is performed in the RRAM system. In this work, we employed an integral LET spectra for galactic cosmic rays during solar minimum to calculate the SEU-induced BER in the RRAM system (Figure 44). For the 1T1R architecture, as mentioned above, the sensitive locations are the drain-body junctions of the "OFF" transistors tied to the selected BL in SET operation. Therefore, the sensitive area is the total area of the drains of the "OFF" transistors connected to the selected BL. Then for an N × N array with W_B bits to be written simultaneously, the sensitive area can be calculated as

$$Area_{1T1R} = A_{D\_N}(N-1)W_B n \quad (25)$$

where $N-1$ is number of "OFF" transistors tied to a selected BL, and W_B is number of selected BLs, and n is the number of activated arrays in the RRAM system. If I/O bit width of the system is N_{IO}, then

$$n = N_{IO}/W_B \quad (26)$$

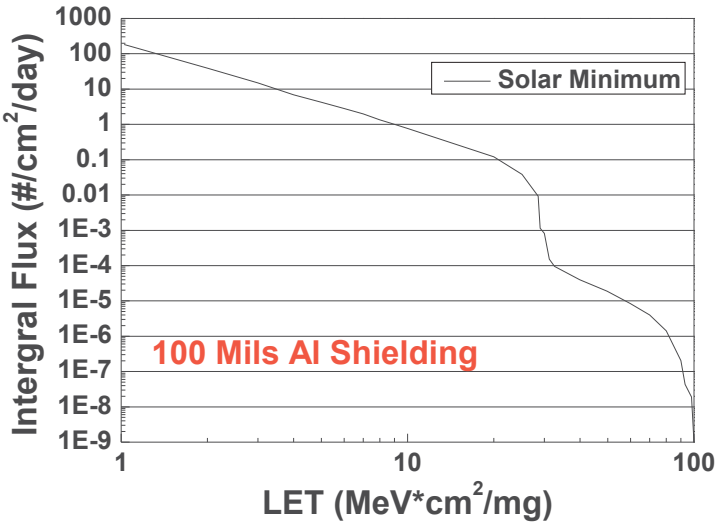


Figure 44. An integral LET spectra for galactic cosmic rays during solar minimum

Thus the sensitive area of the 1T1R becomes

$$Area_{1T1R} = A_{D_N}(N-1)N_{IO} \quad (27)$$

which is only determined by the I/O width no matter how many sub-arrays are activated. For the crossbar architecture, in contrast, the sensitive area is the total area of the drains of the both N-type and P-type "OFF" transistors of the edge drivers. For a N × N crossbar array, the total number of drivers is 2N. In the SET operation, all the WL are biased to Vw or 1/2Vw and all the N-type transistors are "OFF"; W_B of BLs are grounded if W_B bits are written into simultaneously, hence there are $N - W_B$ N-type and W_B P-type "OFF" transistors on the BL. In total, $2N - W_B$ N-type and W_B P-type "OFF" transistors in SET operation. The analysis is similar in the RESET operation. Thus the sensitive area is calculated as

$$Area_{crossbar} = \begin{cases} \left[\left(A_{D_N}(2N - W_B) + A_{D_P}W_B\right)\rho_{SET}\right] + \left[\left(A_{D_N}(2N-1) + A_{D_P}\right)\rho_{RESET}\right] \\ N_{IO}/W_B \end{cases} \quad (28)$$

which is not only determined by the I/O width but also how many sub-arrays are activated. For example, for the 64 bits I/O used in the system, if we write 8 bits into one sub-array in parallel, we need to activate 8 sub-arrays.

In this work, we assume the RRAM cell write latency is 20 ns. In addition, the most write-intensive workload in a solid-state-drive (SSD) is used to calculate the total write time window for the system, which is 308.9 s/day. Taking those assumptions into account, Figure 45(a) and (b) show the maximum BER/day for the 1T1R array and the crossbar array, respectively. In the 1T1R architecture, it indicates that the maximum BER per day is exponentially increased with the sub-array size. However, it has no dependency on the bits to be written simultaneously in a sub-array (Figure 45(a)). The reason is that the sensitive area is only as a function of I/O bit width of a system (from Eq. (10)). In the crossbar architecture, however, both the number of bits to be written in one sub-array and the array size can affect the maximum BER per day even for a given I/O bit width (i.e. 64 bit) and total write time window (i.e. 308.9 s/day). It suggests that array size of 256 × 256 has the lowest maximum BER per day if a single bit is written into one array as shown in Figure 45(b).

If we compare the 1T1R and the crossbar architectures, the crossbar array does not have transistor in the array (only at the edge), thus it has smaller sensitive area than the 1T1R array. On the other hand, the 1T1R only shows SBU, the crossbar array may have MBUs, thus once the crossbar is struck, it would generate more bit errors. However, the threshold LET of the crossbar structure is much higher than that of the 1T1R structure as discussed in section II. In addition, the integral LET spectra for galactic cosmic rays is decreased exponentially with ion LET (Figure 44). As a result of all the aforementioned factors, our analysis shows that the crossbar architecture still has a smaller maximum BER/day as compared to the 1T1R architecture.

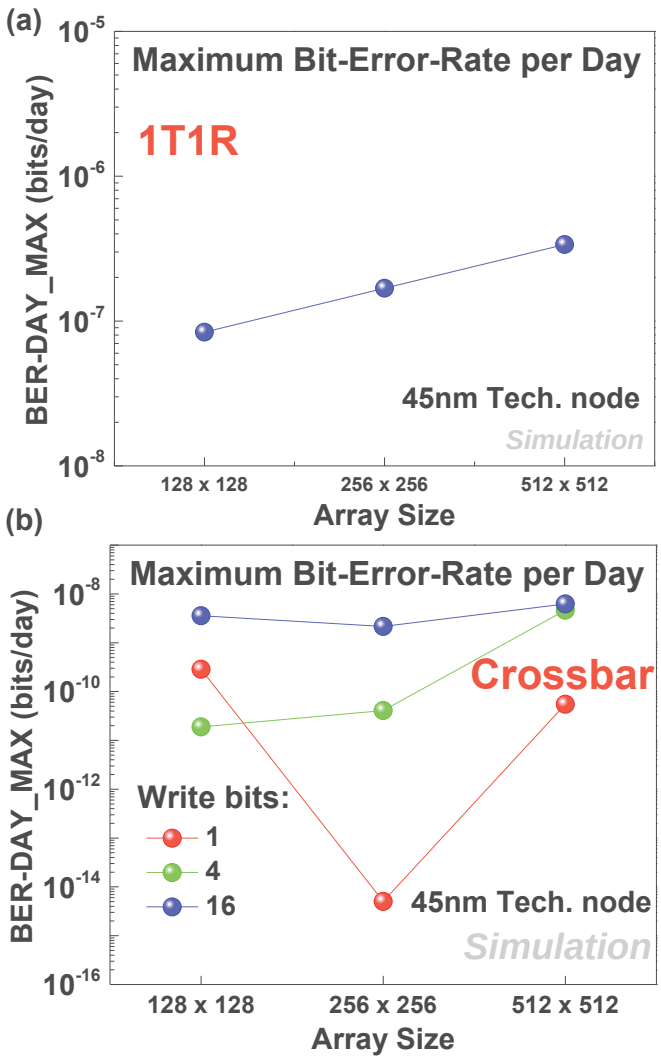


Figure 45. (a) An integral LET spectra for galactic cosmic rays during solar minimum and (b) calculated Bit-Error-Rate per day for various array sizes and numbers of bits written in one array

3. PROGRAM RESULTS FOR YEAR 3

3.1. Summary of Year 3 Results

Task 7 - Designed and fabricated (at BRIDG) arrays of CBRAM variants that meet these density requirements.

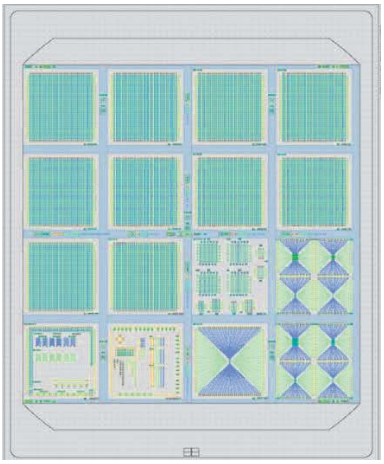
Task 9 – Conducted electrical experiments on CBRAM arrays

Tasks 11,12 – Use d multiplie split lots for process and design optimization

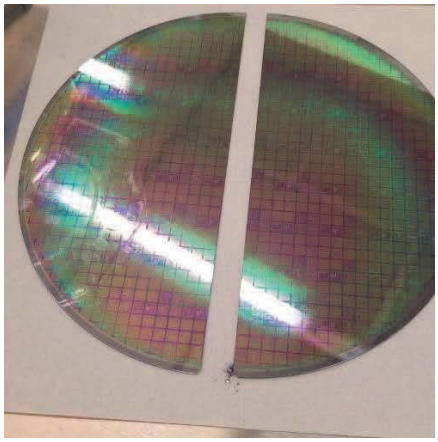
3.2. Detailed Results in Year 3

3.2.1. RRAM Array Fabrication, Process and Design Optimization (Tasks 7,11, 12)

In the previous reporting period, we presented the effort conducted in order to establish and conduct technology transfer of oxide-based CBRAM technology to a pilot line such as BRIDG-Florida. The effort developed: 1) a manufacturing process (BEOL compatible, planarized process) as well as 2) the mask-set needed for implementation of CBRAM devices, CBRAM arrays as well as test structures. A brief reminder of such effort is shown here in Figure 46, where the top view of the reticle implementing the different tiles is illustrated, as well as a top view photograph of a wafer implemented through the pilot line.



(a)



(b)

Figure 46. (a) mask-set reticle layout implementing different tiles of arrays, CBRAM cells and test structures, (b) example of one processed 8-inch wafer

An illustration of some of the test structures and devices is provided in Figure 47 and 48, where top view microphotographs of crossbar arrays as well as a top view of PMCs/CBRAM cells and resistivity test structures are provided. The arrays are 32 by 32 crossbar arrays, and the photographs illustrate the impact of pitch reduction since all have been acquired at the same magnification but have decreasing feature dimensions.

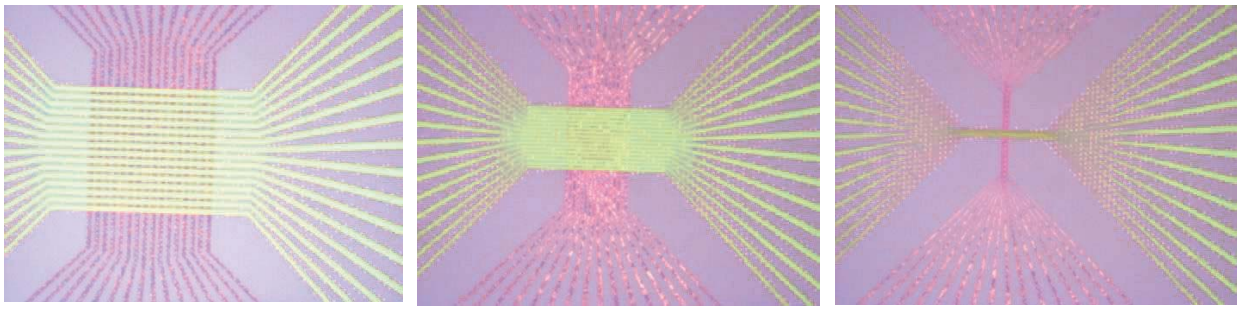


Figure 47. Illustration of some of the 32 by 32 crossbar arrays implemented through the pilot line, with different metal pitch: from larger to smaller feature dimensions. (images are acquired at the same magnification)

The resistivity test structures are useful to gather information with respect to the "access resistors" that PMC devices are seeing.

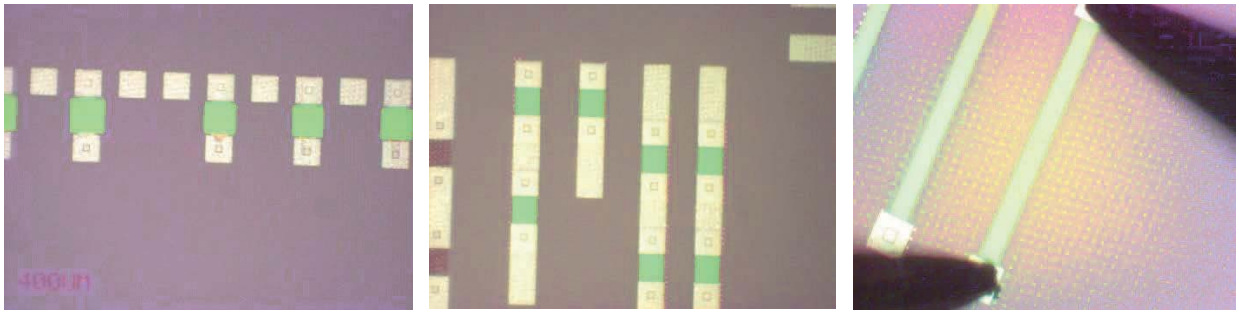


Figure 48. Illustration of some of the test structure available on the test-chip: (a) large PMC cells, (b) contact resistance test structure, (c) resistivity test structures

In Figure 49, some of the additional arrays implemented within the test-chip are also illustrated, among which, small crossbar arrays, large arrays as well as arrays with devices implemented solely on the diagonal of the crossbar structure, enabling to obtain a test structure where no sneak-path to ease electrical testing.

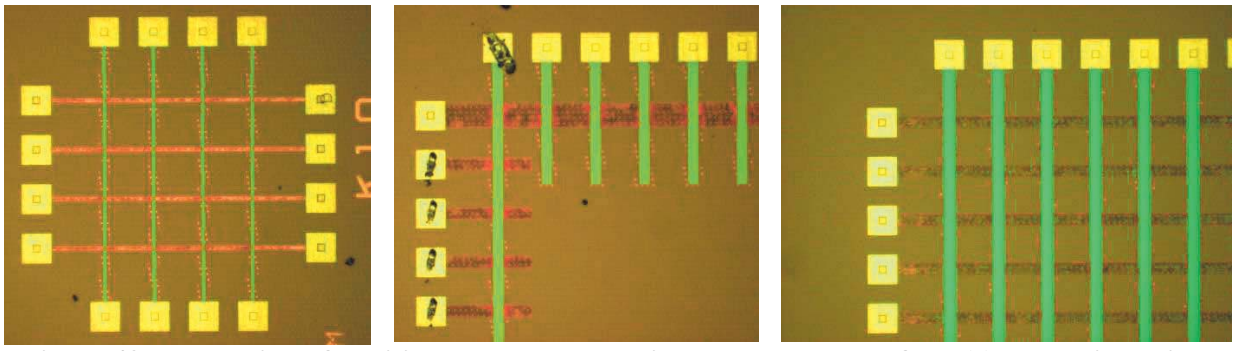


Figure 49. Illustration of additional structures available on the test wafers: (a) small dimension array, (b) single column array, (c) array with device located on the diagonal

3.2.1.1. Processing splits for CBRAM resistance switching investigations.

In order to investigate the Cu-SiO_x CBRAM device properties obtained through the technology transfer process a series of processing splits have been fabricated. This technology transfer

intends to transfer the “operating devices”, i.e. devices exhibiting a repetitive resistance switching manufactured at the ASU NanoFab to the fabrication line at BRIDG. Cu-SiO_x devices made at ASU that have been shown to exhibit resistance switching have been manufactured using SiO_x thin-films deposited using electron-beam evaporation and plasma-enhanced chemical vapor deposition (PECVD). For this research and technology transfer, a back-end-of-the-line compatibility goal pushes the effort towards the PECVD films, since PECVD dielectrics are commonly used in CMOS BEOL layers. The overall objective is also to be able to fabricate thin-films which exhibit the adequate porosity level to enable the Cu cations to be transported throughout the thin-film, enabling the formation of functional materials providing the desired resistance switching behavior. As such, the porosity of the films can be varied by modifying typical PECVD deposition parameters such as the temperature deposition, the pressure deposition or also the ratio of reactants in the PECVD chamber.

The present effort has investigated a total of nine different processing splits with the goal of identifying deposition parameters enabling to obtain operational devices. Such parameters are not definitive but constitute a first path/iteration in the methodology of “process optimization”.

Table 8. Process splits labels

RERAM wafer	Pattern
A	-+-
B	---
C	--+
D	-++
E	+-+
F	+--
G	0
H	++-
I	+++

Since 9 processing batches constitute a very large set of samples, we have decided to conduct first a forming study on the processing splits. Since devices that do not exhibit some type of forming are found to be non-operational, such forming study has been shown to enable a first down-selection of the samples. This also sets the bounding limits for resistance switching operation by revealing the lower limit of current at which electrical characterization can be conducted.

3.2.2. Experiments on High Density RRAM Arrays (Task 9)

3.2.2.1. Forming Study of different Cu-SiO_x CBRAM processing splits

In this forming study, we present data of the forming process conducted on Cu-SiOx CBRAM devices (PMCs) with different dimensions: devices with via diameters of 2um, 5um and 10um

are used. The forming process is usually the first step in ReRAM/CBRAM device operation, where the initial forming occurs at a higher voltage than the subsequent programming/set voltage.

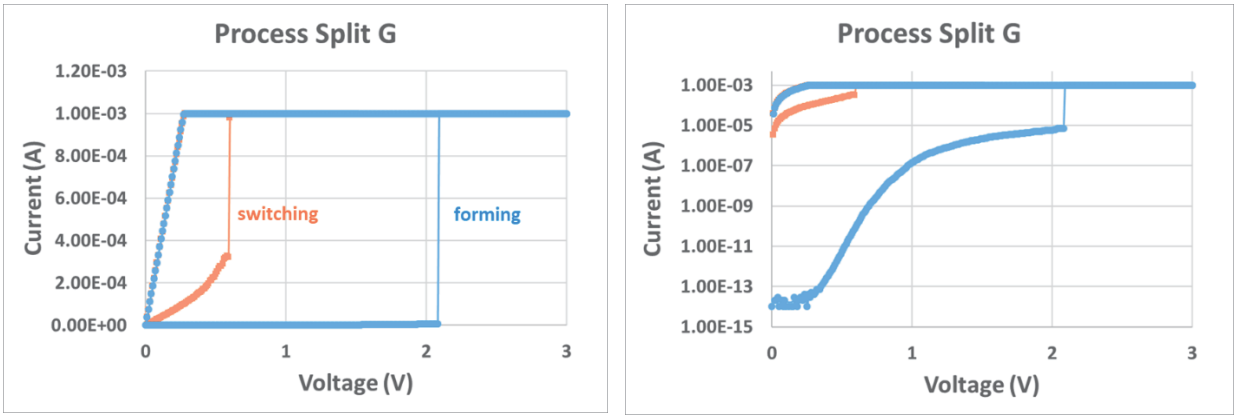


Figure 50. Illustration of typically observed behavior on ReRAM cells. A forming step has a higher characteristic voltage than the subsequent set voltage characterizing the resistance switching operation, (a) linear y-axis, (b) logarithmic y-axis

The forming study was in part completed to reduce the number of splits that would undergo lengthy and time-consuming electrical characterization. Typical forming curves obtained during this study are presented in this section, and a full presentation of the data is also provided as an appendix since the presentation of the data would be quite repetitive.

The results obtained are illustrated and summarized in the next following figures, where forming data in the form of current-voltage (IV) characteristics is presented as well as a summary of such IVs is provided as $I_{forming}$-$V_{forming}$ curves. Those I_{form}-V_{form} curves summarize the data by presenting the extracted forming voltage as V_{form}, and the current level at which forming occurs as I_{form}. In Figure 51 three IV forming curves are presented for 2um, 5um and 10um diameter devices from processing split A. IV characteristics can be obtained at two different "integration times" which basically enables to modify the voltage sweep-rate during the electrical test. In Figure 51d the I_{form}-V_{form} extracted from Figure 51a to Figure 51c data is summarized, where the purple points represent the data extracted at the fast sweep-rate (i.e. short integration time). In the I_{form}-V_{form} graph, a set of points (black) are also added for the IV obtained with a slower sweep-rate (medium integration time). As can be seen in Figure 51, some of the devices exhibit a formin at approximately 2V whereas some other already exhibit a low resistance (high-current levels even at low voltages). Such devices with low resistance are observed to be devices with the larger diameters. This can be seen in Figure 51c, where in the case of the 10um diameter device, only 2 CBRAM effectively undergo forming. In Figure 51d, the data points corresponding to the devices exhibiting low resistance can be seen on the I_{form}-V_{form} chart as the point located on the top left of the chart, which exhibit high current at low applied voltages.

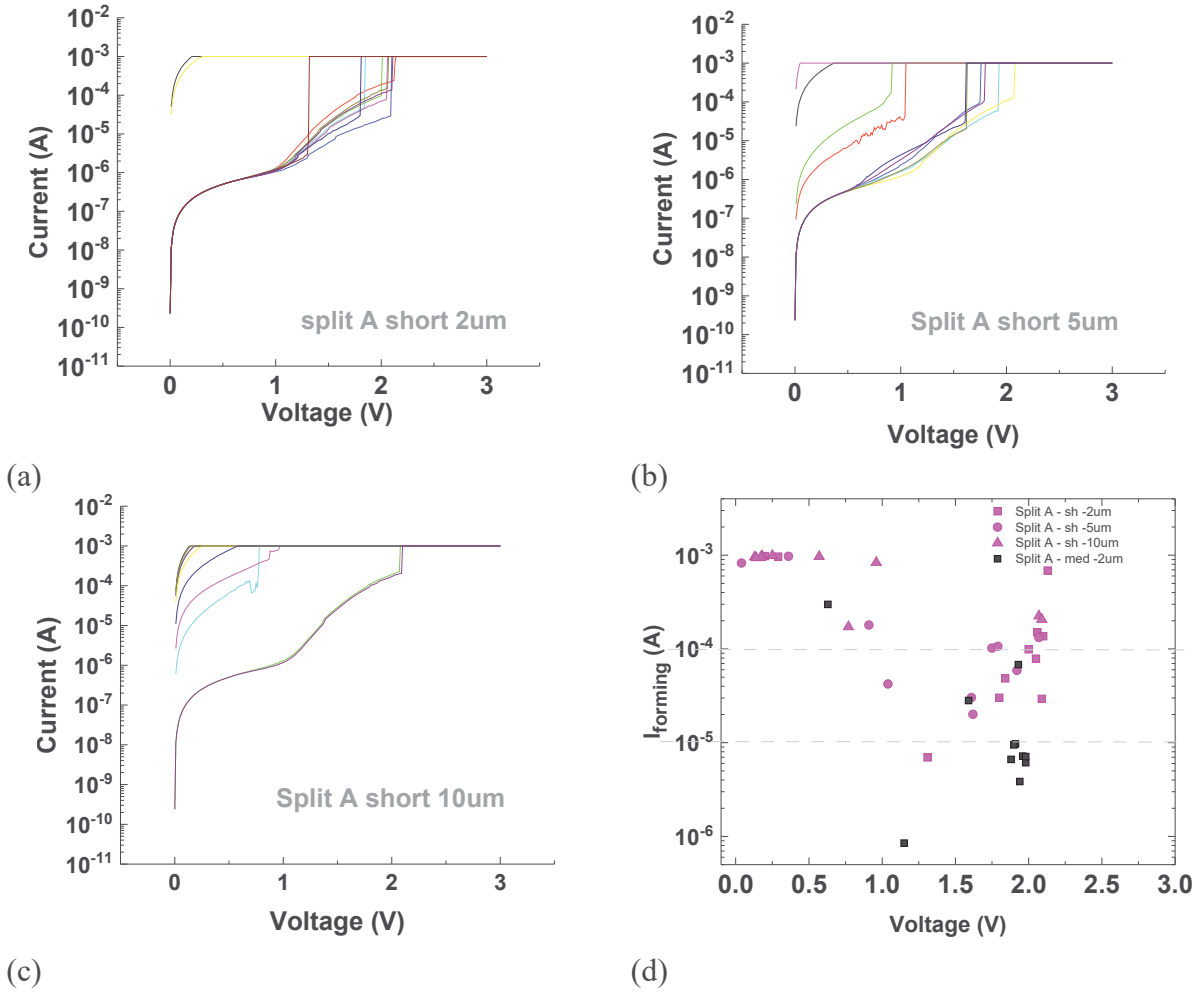


Figure 51. Forming behavior of CBRAM cells from process split A: IV characteristic of (a) 2um diameter devices, (b) 5um diameter devices, (c) 10um diameter devices, (d) I_{form}-V_{form} chart extracted from IV characteristics for 2 different sweep rates

In Figure 52 an additional illustration of the type of response observed on the processing splits is presented. In this case, split C is presented. It can be seen that for this processing split, in the case of devices with diameter of 10um we observe devices with low resistance similarly to what was observed on split A, but we also observe samples for which the current flowing through the CBRAM before forming is non-monotonic (i.e. current increases and then decreases with the increasing applied voltage). Such behavior is "hardly" represented in the I_{form}-V_{form} charts, and that is why IV forming characteristics are presented.

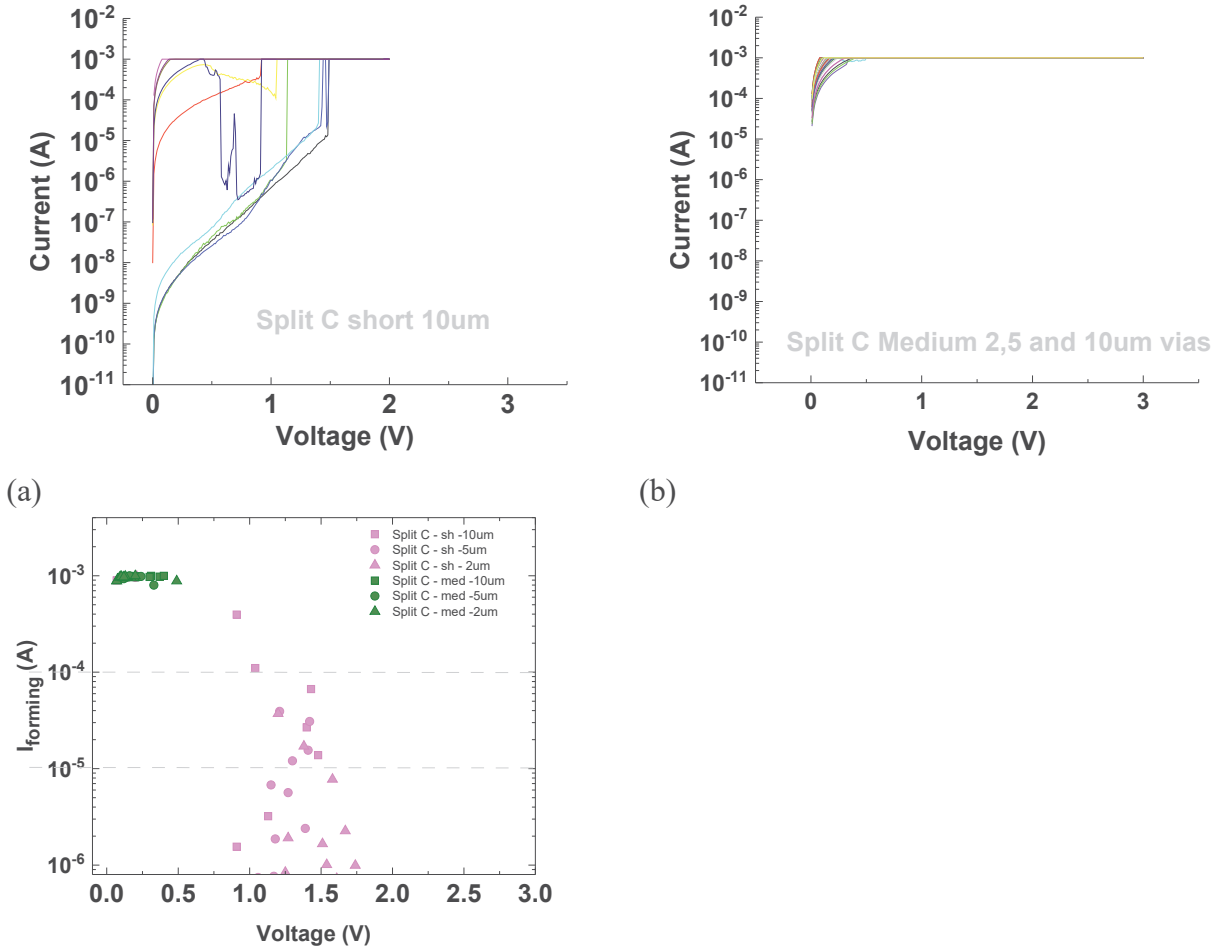


Figure 52. Forming behavior of CBRAM cells from process split C: IV characteristics of (a) 10um diameter devices at short integration times, (b) 2um, 5um and 10um diameter devices at medium integration, (c) I_{form}-V_{form} chart

An additional case is presented in Figure 53 with the data obtained on process split H where data for both short integration and medium integration are presented. In this case this dataset reveals that the non-monotonic behavior of the current can exist at both fast and slow sweep-rate. Here, again the devices with a diameter of 10um are the ones exhibited the highest degree of variability.

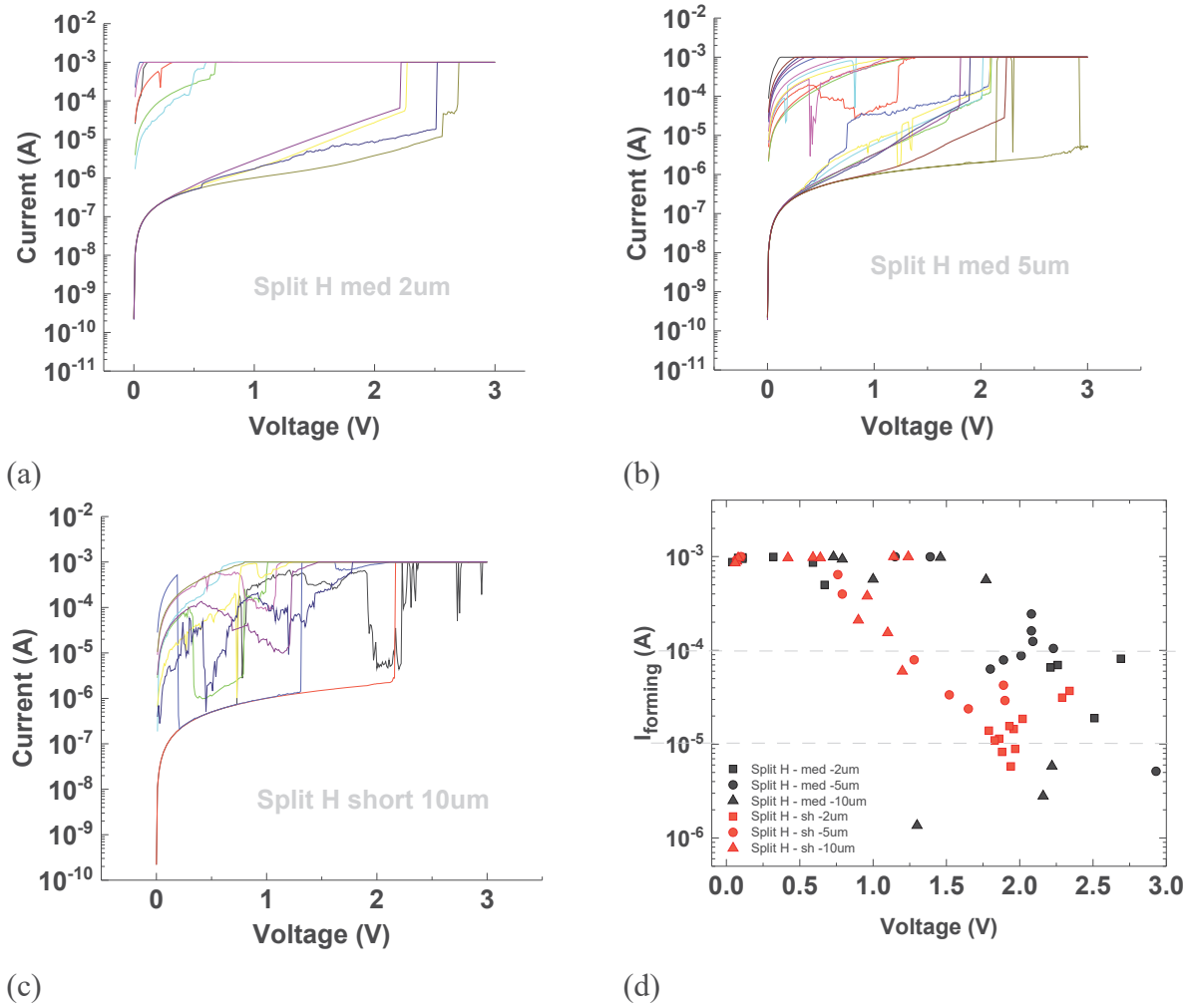


Figure 53. Split H IV characteristics of (a) 2um diameter devices at medium integration times, (b) 5um diameter devices at medium integration times, (c) 10um diameter devices at short integration times, (d) I_{form}-V_{form} chart

In the following graphs of Figure 54, the case of process split I is presented. The observation observed on devices from split I constitute a 'golden standard' for forming behavior. Forming IV characteristic obtained with a medium integration time are presented in graph a through c. The typical I_{form}-V_{form} curve obtained at short and medium integration time are then presented. Devices from split I present forming for both the 2, 5 and 10 um diameter devices (when many of the previous had few 10um diameter devices exhibiting forming). Very few of the devices form this split exhibit low resistance state. Additionally it can be observed that the variability of the V_{form} values is lower than the one presented in previous illustration for other process splits. From the I_{form}-V_{form} curve it is also clear the V_{form} is lower for slow sweep-rates, as well as I_{form} is lower for the slow sweep-rate. This is illustrated in Figure 54f where the full IV are presented for short and medium integration on the 2um diameter devices. Additionally, in this present case, it can be seen that the current flowing through the devices scales with area before forming, as the IV for different diameter are shown in Figure 54e.

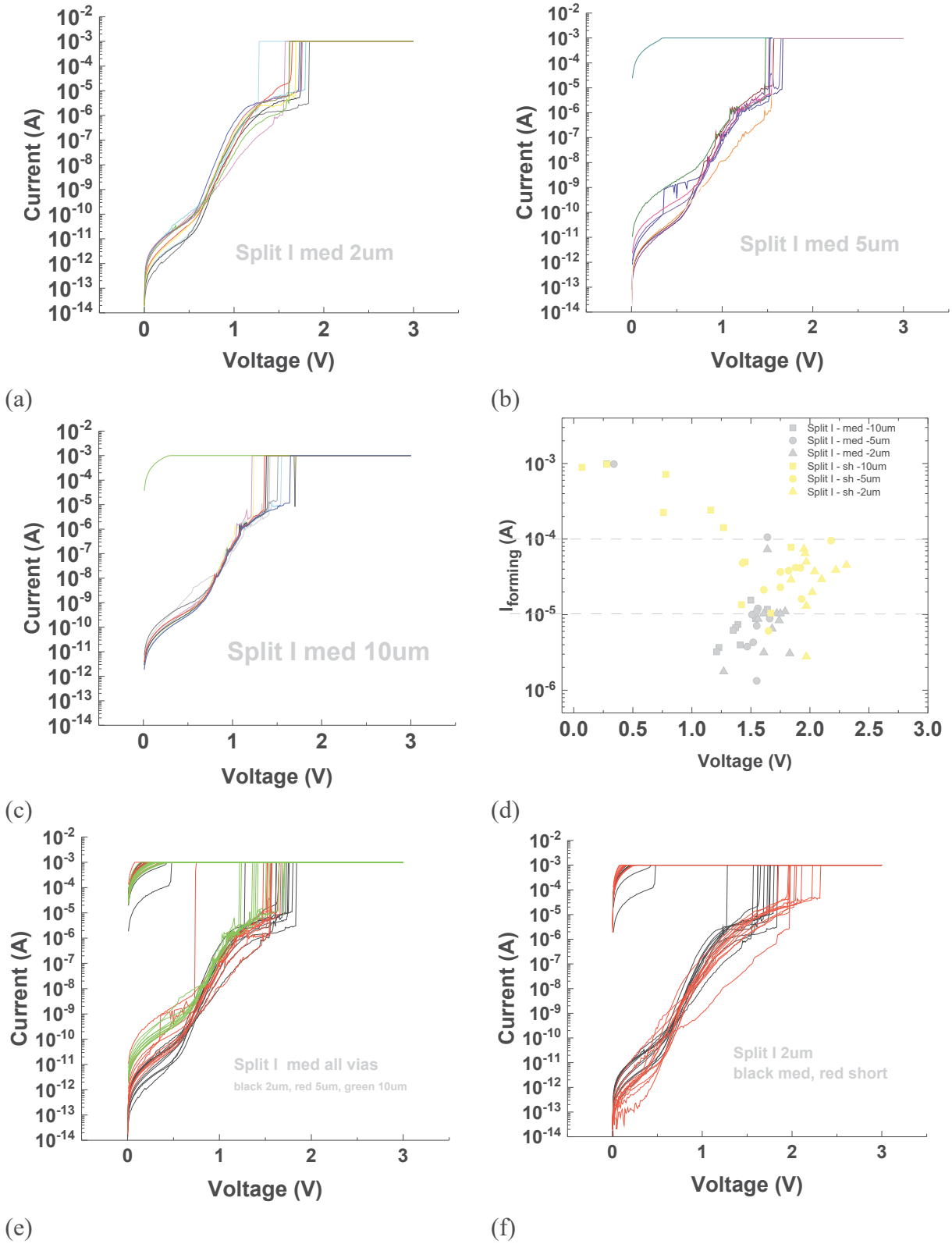


Figure 54: Split I IV characteristics of (a) 2um, (b) 5um, and (c) 10um diameter devices at medium integration times, (d) I_{form}-V_{form} for 2 different sweep rates, (e) comparison of 2um, 5um and 10um diameter device data, (f) comparison of 2um devices at 2 different sweep-rates

These observations are the ones typically reported in most of the literature on RRAM/CBRAM devices, and as a consequence process split I constitutes a processing split of particular interest.

A summary of all the I_{form}-V_{form} datasets obtained on the additional process splits is presented in the following Figure 55, which has all the dataset plotted. It can be seen that depending on the process split, a variation of V_{form} and its standard-deviation (variation/variability) can be observed, and similarly a variation of I_{form} and its standard-deviation is also observed.

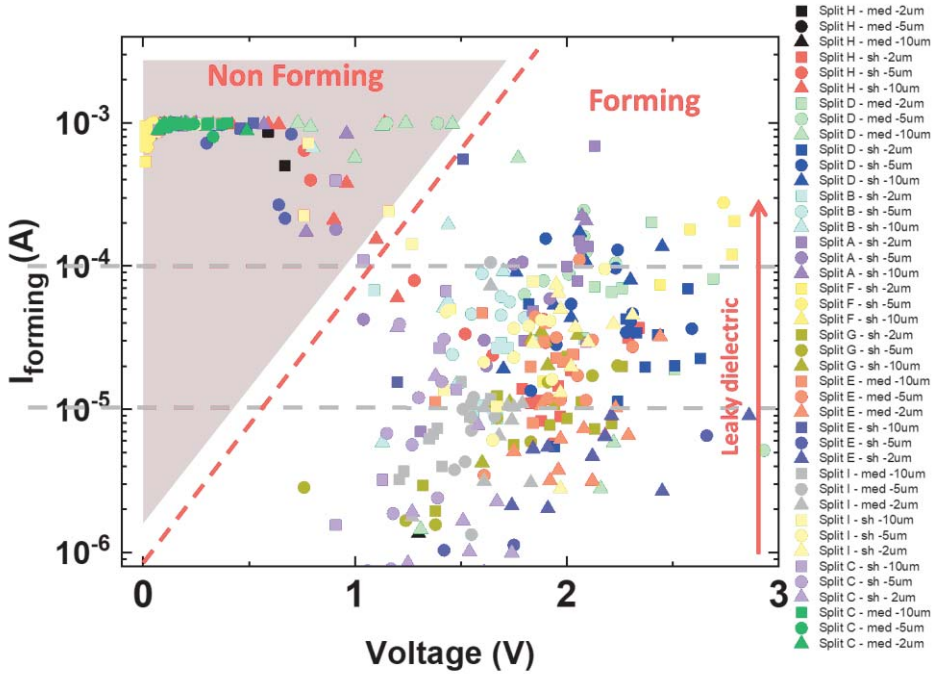


Figure 55. Dataset of I_{form}-V_{form} pairs obtained though the forming study

The higher the I_{form}, the "leakier" the SiO_x dielectric layer is, and it can be hypothesized that such behavior is related to the porosity of the films. Porosity would have to be evaluated in future works to be able to relate such parameter to functionality of the material.

In the case of the devices exhibiting low resistance from the beginning and the tendency to observe such low resistance levels on 10um diameter devices, processing yield might be a factor, since defects density would be higher on larger area devices.

Table 9 summarizes the observations made during the study providing the forming voltage ranges and forming current ranges as well as the summary of observations. Split E, G and I are observed to have the best "forming behavior/properties" with good yield of devices exhibiting forming as well as reproducible values within a given split. It is interesting to note that split G constitutes the baseline of the design of experiment matrix (0 in the pattern column) and split process E and I, which also exhibit promising forming behavior both exhibit higher processing temperature and higher reactant ratio than the baseline process split.

Table 9. Overall summary of the forming study

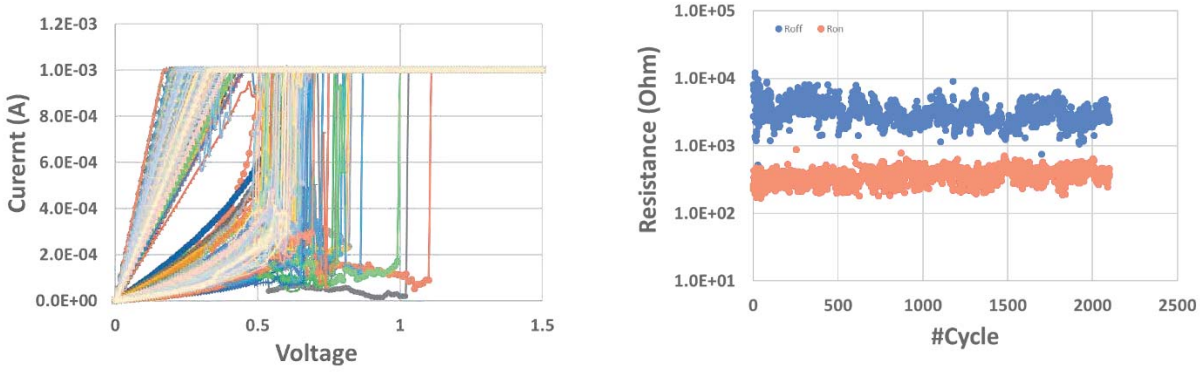
CBRAM Wafers	Pattern (T,P,Ratio)	$V_{forming}$ (V)	$I_{forming}$ (uA)	Summary
A	-+-	~ 2	~100u	10um highly conductive, 2um best
B	---	1.5-1.7	<100u	10um highly conductive, 2um best
C	--+	1.25 - 1.6	1u -20u	No forming in MED, short has high HRS
D	-++	XX	XX	No forming in MED, short has high HRS, 2um best
E	+-+	2 - 2.5	<100u	MED best, 2um best, reproducible, scaling with via diameter, very high HRS, good yield
F	+--	1.7 - 2.5	<60u	Bad yield, few 2um formed, shorted 10um
G	0	~ 2.7	>100u	good yield
H	++-	1.5-2.3	<50u	2um short good, lots of current peaks, i.e redox?
I	+++	1.7 - 2.5	<100u	MED best, MED <10uA, short <100uA, good yield, reproducible and scaling

3.2.2.2. Resistance Switching of Cu-SiO_x CBRAM cell from selected processing splits

In this section, we present the resistance switching characteristics obtained on several of the processing splits. This section will illustrate that the CBRAM cells from process split E, G and I are indeed the most promising since they are the ones that will be shown to exhibit resistance switching.

Among the different processing splits, split E, G and I are the ones that do show consistent forming, capability to be erased after forming, and capability to be repeatedly switched after forming. An illustration of the switching characteristic obtained on those process splits is summarized in this section. Results are obtained by conducted DC-IV testing.

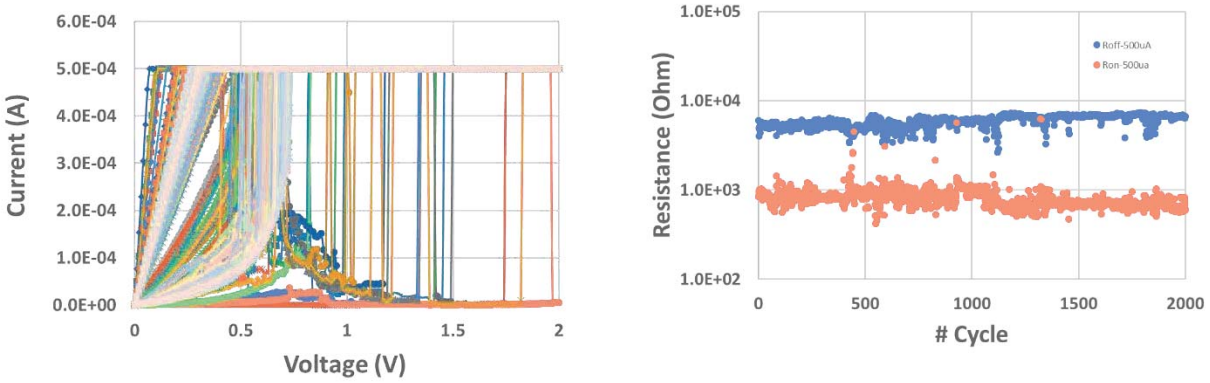
Split E



(a) (b)

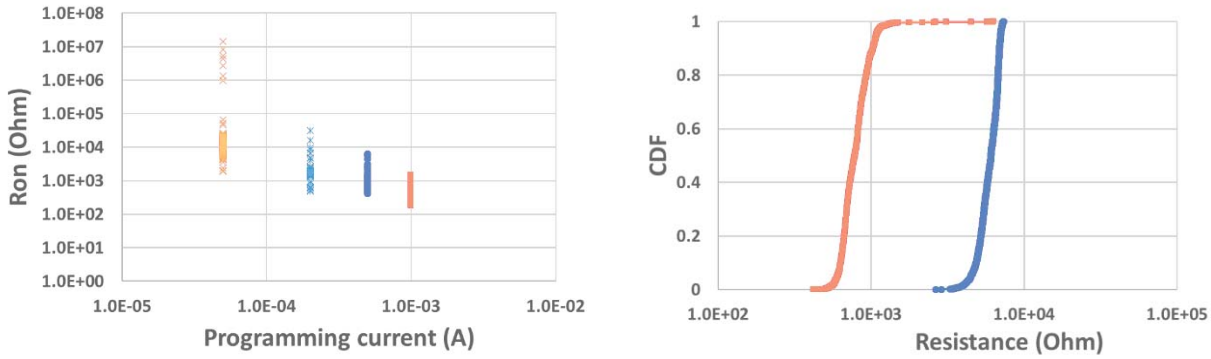
Figure 56. Illustration of repeated resistance switching conducted on devices from split E. (a) repeated DC-IV programming curve, (b) cycling curve

Split G

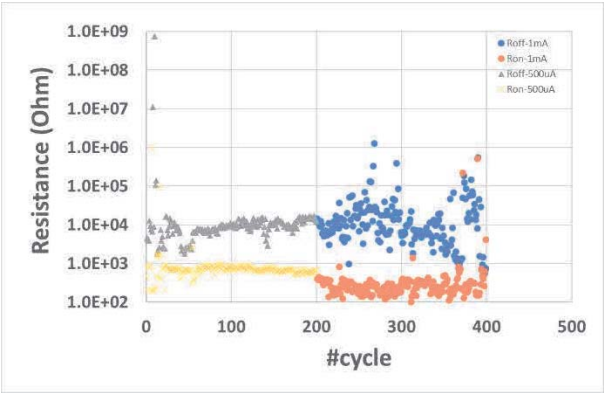


(a) (b)

Figure 57. Illustration of repeated resistance switching conducted on devices from split G. (a) repeated DC-IV programming curve, (b) cycling curve



(a) (b)



(c)

Figure 58. Split G (a) Ron vs Iprog curve, (b) cdf obtained for the HRS and LRS of cycled device, (c) cycling obtained with different Iprog

Split I

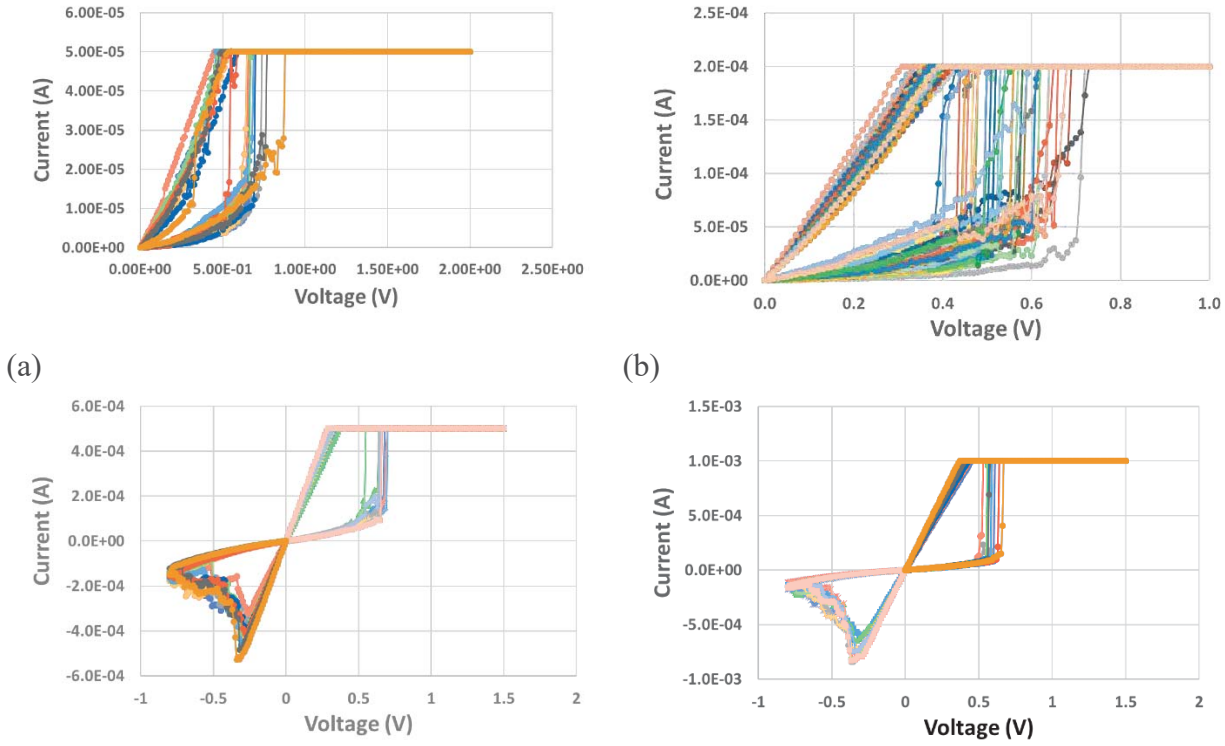


Figure 59. Illustration of repeated resistance switching conducted on devices from split I (a) with Iprog=50uA, (b) Iprog=200uA, (c) Iprog=500uA, (d) Iprog=1mA

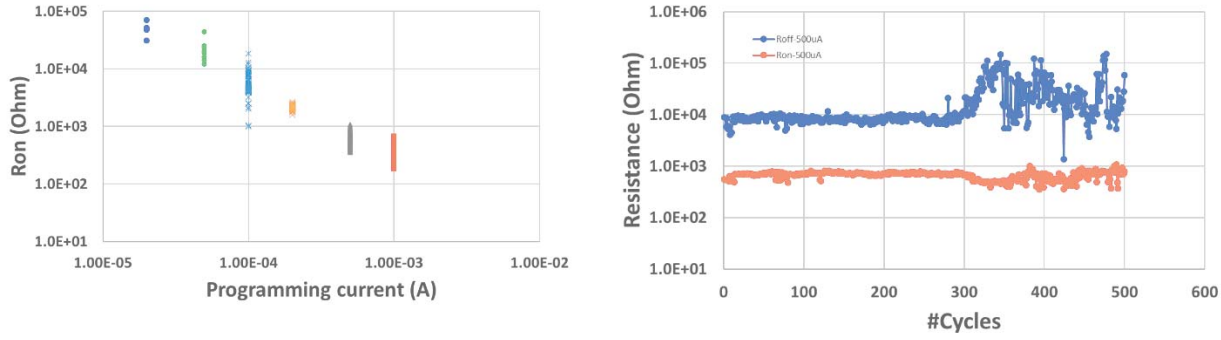


Figure 60. Split I (a) Ron vs Iprog curve, (b) cycling

These 3 different splits exhibit difference in their characteristic that have been to observed as such:

In general after cycling, non-monotonic current is observed on the case of devices from split E and split G with split G being the process split which exhibited the largest non-monotonicity. Process G is capable of exhibiting resistive switching for lower programming currents (Iprog, i.e. compliance) than process splits E and G, however process G seems to not withstand DC cycling as well as devices obtained from split E, and G. In order to be able to provide a better understanding of the variability of the HRS and LRS effectively programmed, additional cycling would have to be carried, however pulse-based cycling will be implemented to also minimize the stress related to the DC based testing.

The results presented in this report demonstrate the successful technology transfert of a Cu-SiOx based CBRAM processing capability as well as operating device to a pilot line. It is obtained that the devices with processing using the high temperature paths provide operational devices which will have to be characterized further for cycling and retention. It is worth to mention that this is unique capability: No university research group has developed a Cu-SiOx CBRAM technology that is fully CMOS compatible such as this one, and it is also worth noting that no university has also presented data on planarized CBRAM process, which are the study case that should be investigated, since E-Field effect could be at ply in non-planarized cells, making the transfer of technology more complex and the experimental results between planarized and non-planarized different.

3.2.2.3. Additional IV forming data for the remaining splits.

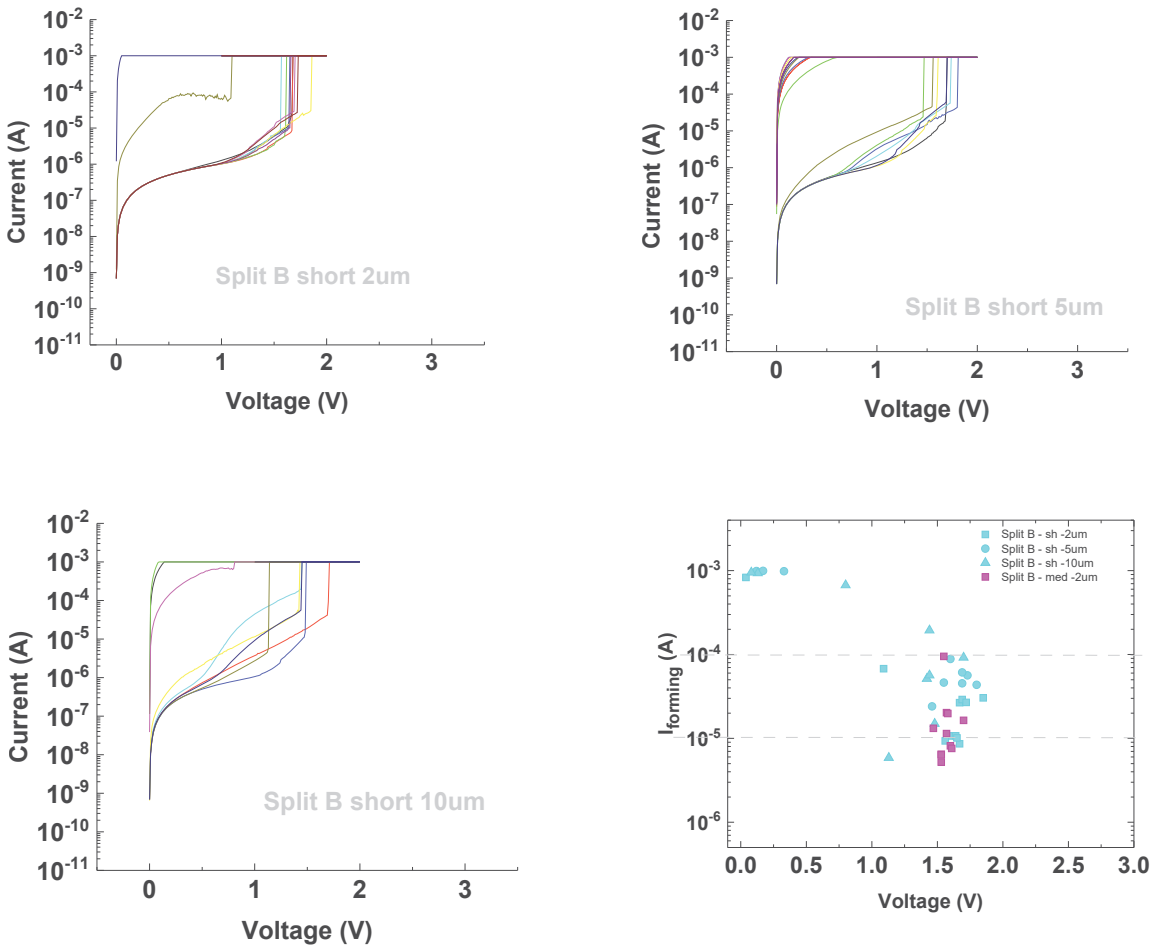


Figure 61. Forming behavior of CBRAM cells from process split B – short integration time

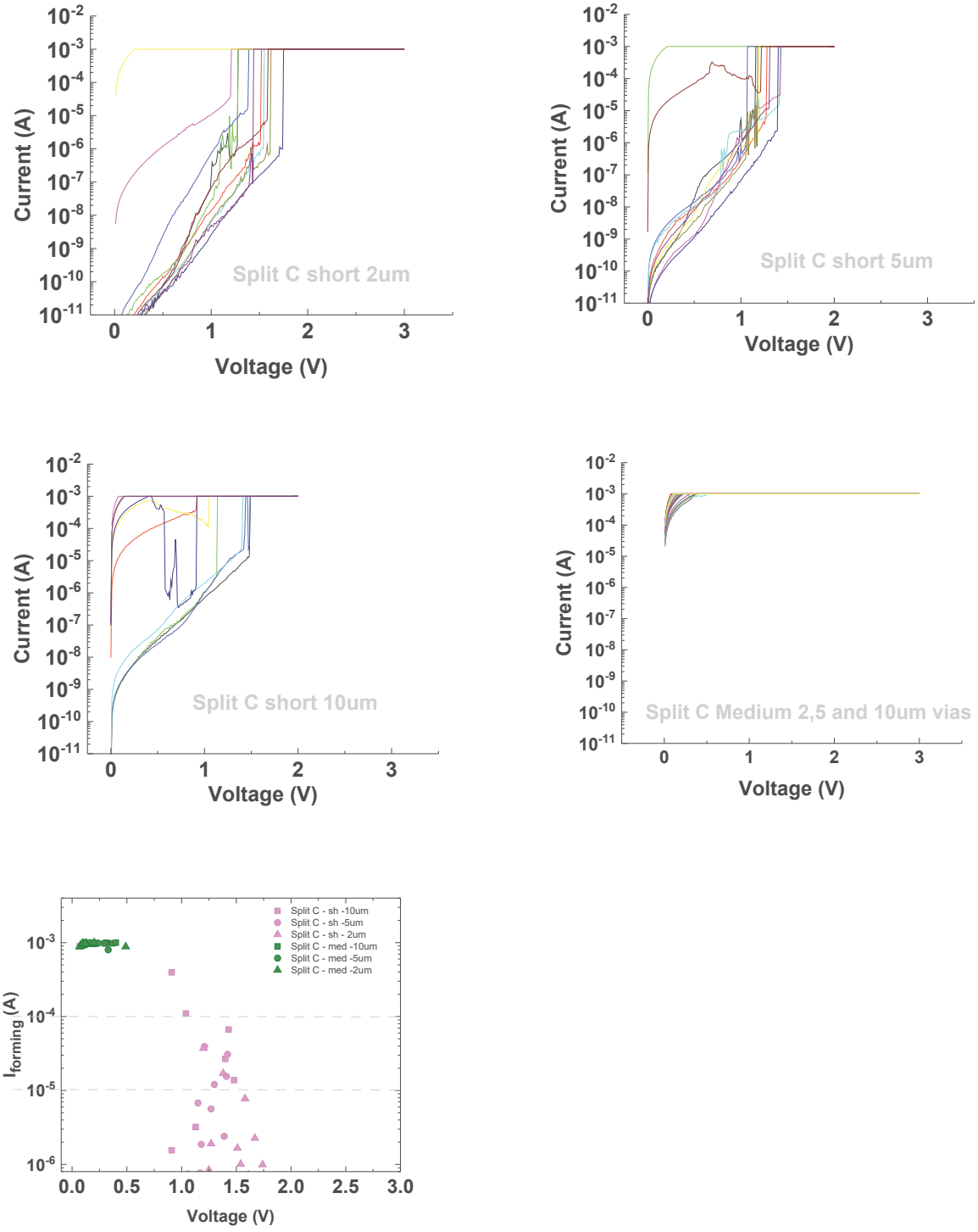


Figure 62. Forming behavior of CBRAM cells from process split C – short and medium integration time

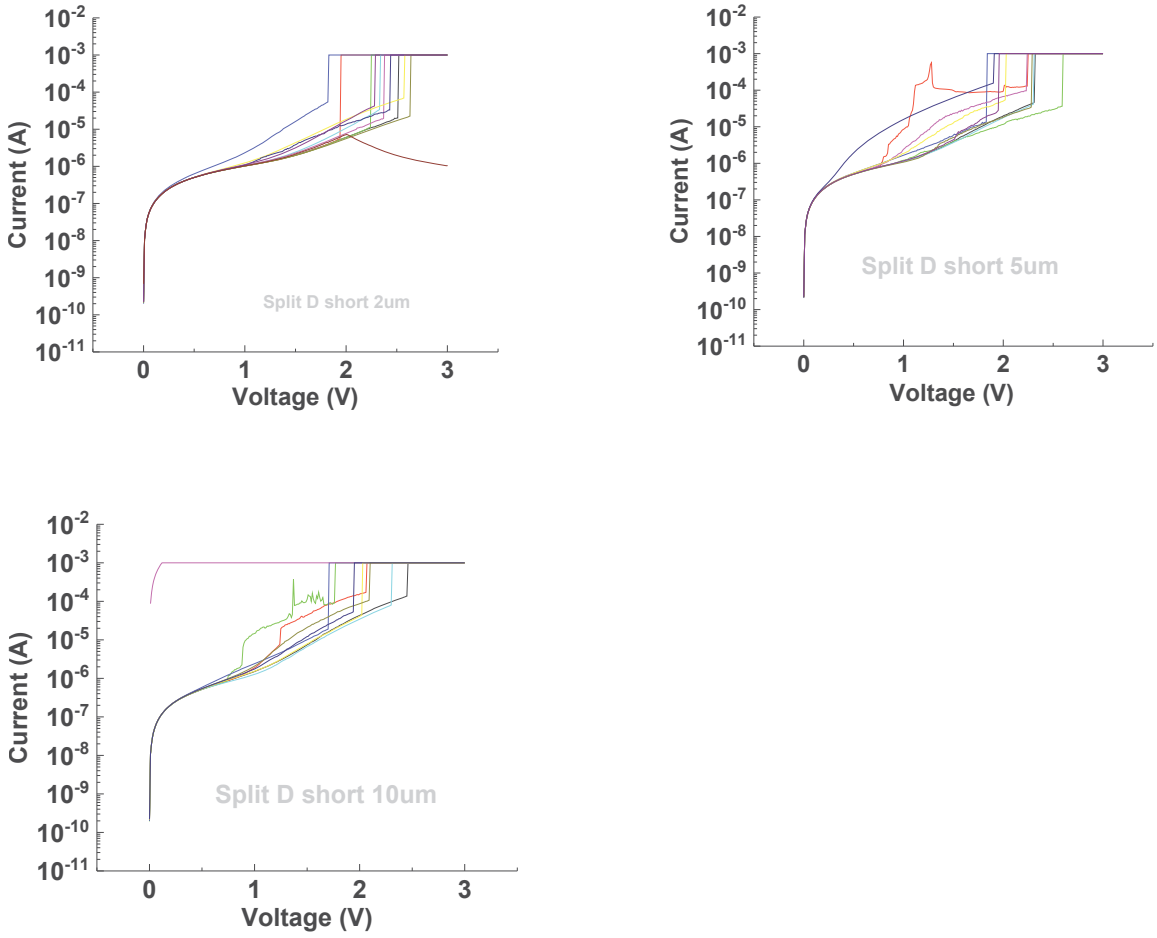


Figure 63. Forming behavior of CBRAM cells from process split D – short integration time

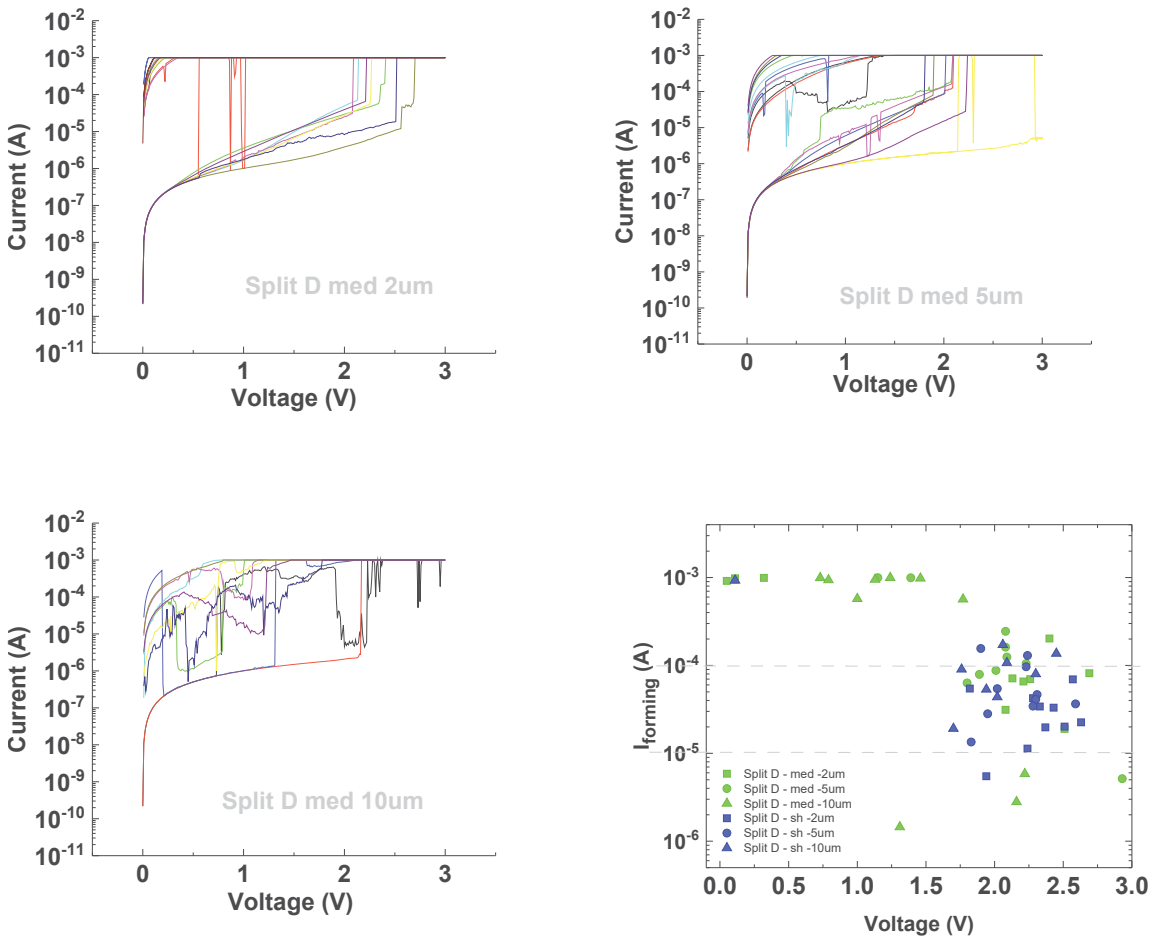


Figure 64. Forming behavior of CBRAM cells from process split D – medium integration time

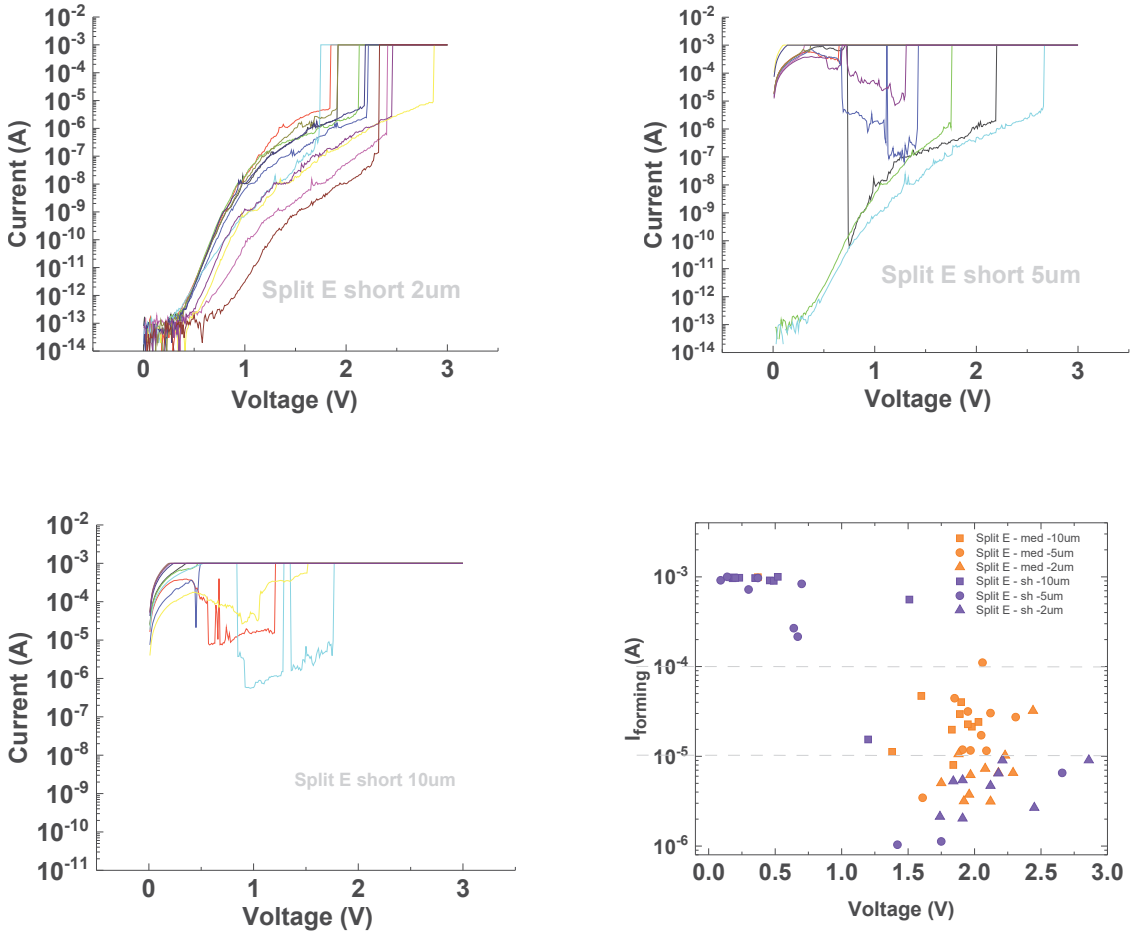


Figure 65. Forming behavior of CBRAM cells from process split E – short integration time

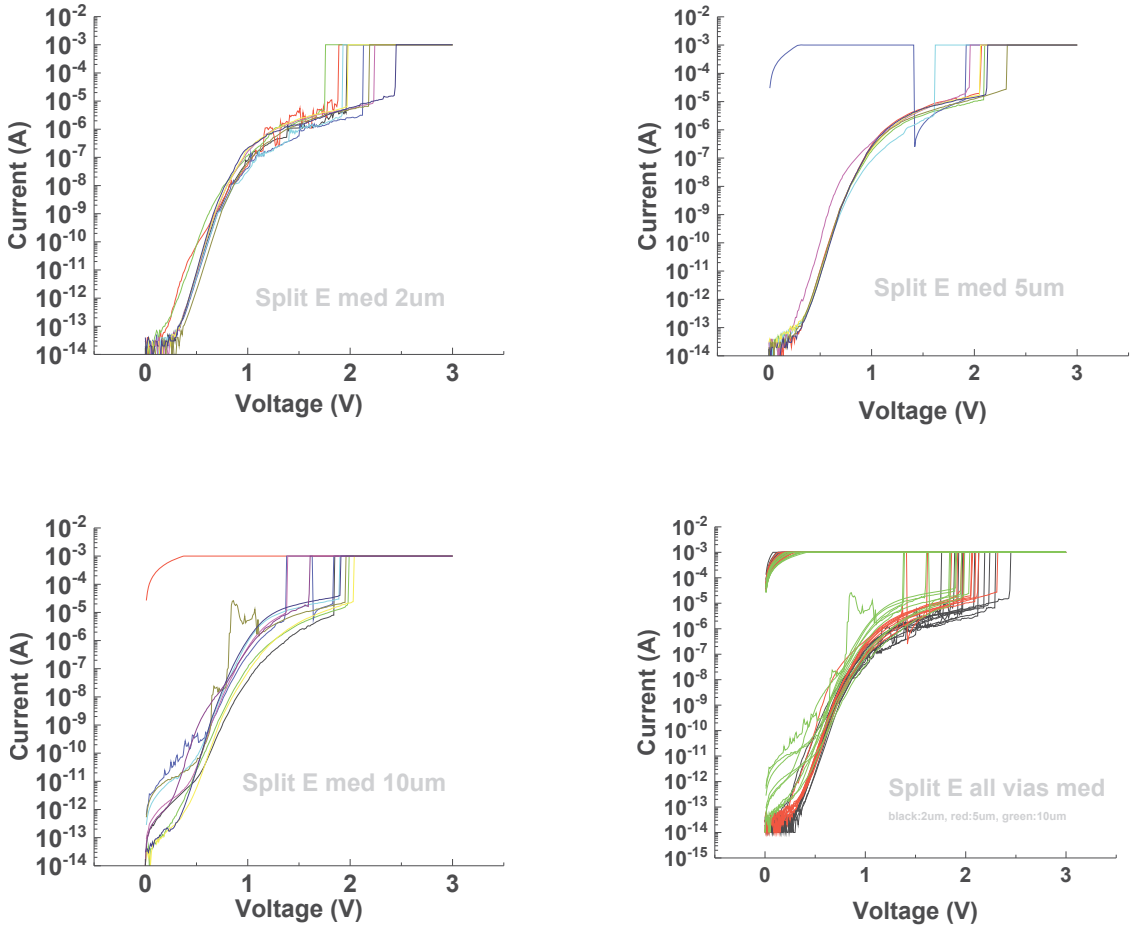


Figure 66. Forming behavior of CBRAM cells from process split E – medium integration time

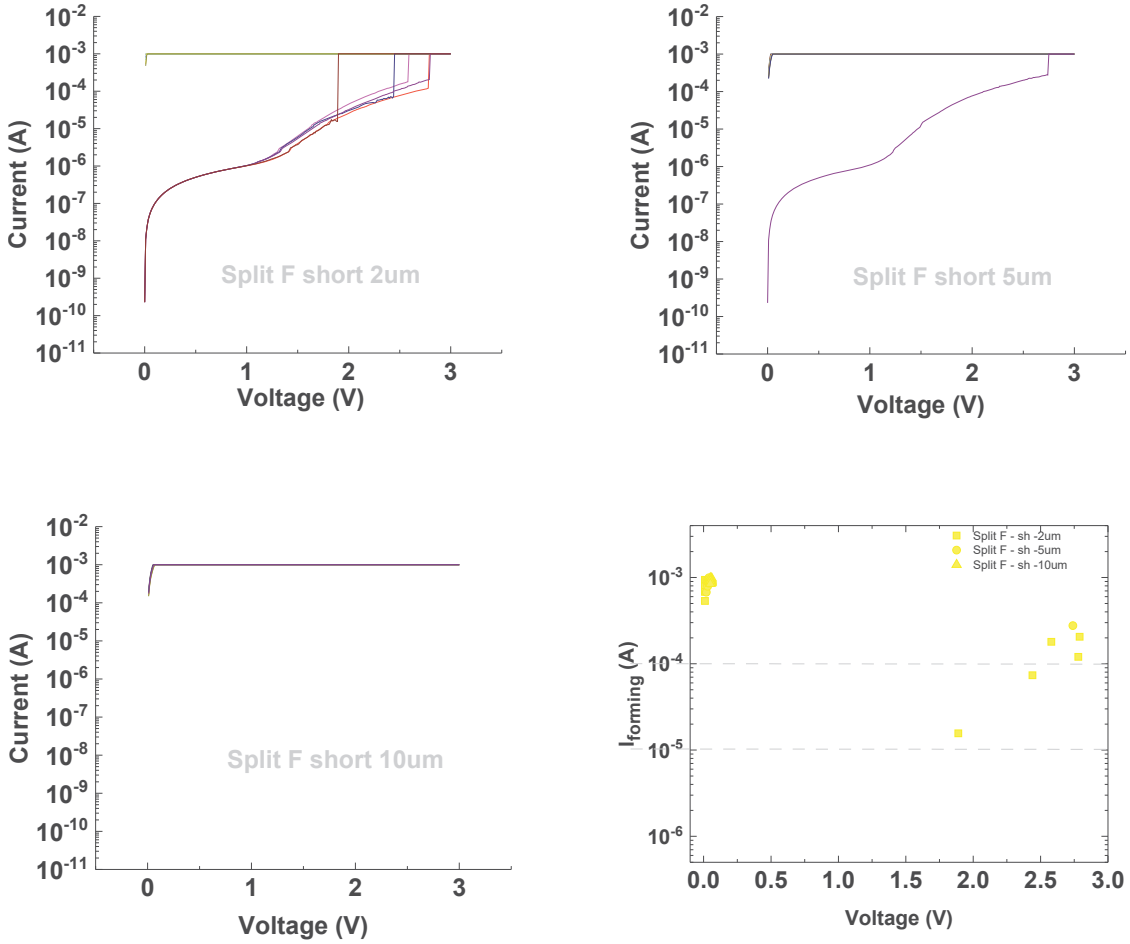


Figure 67. Forming behavior of CBRAM cells from process split F – short integration time

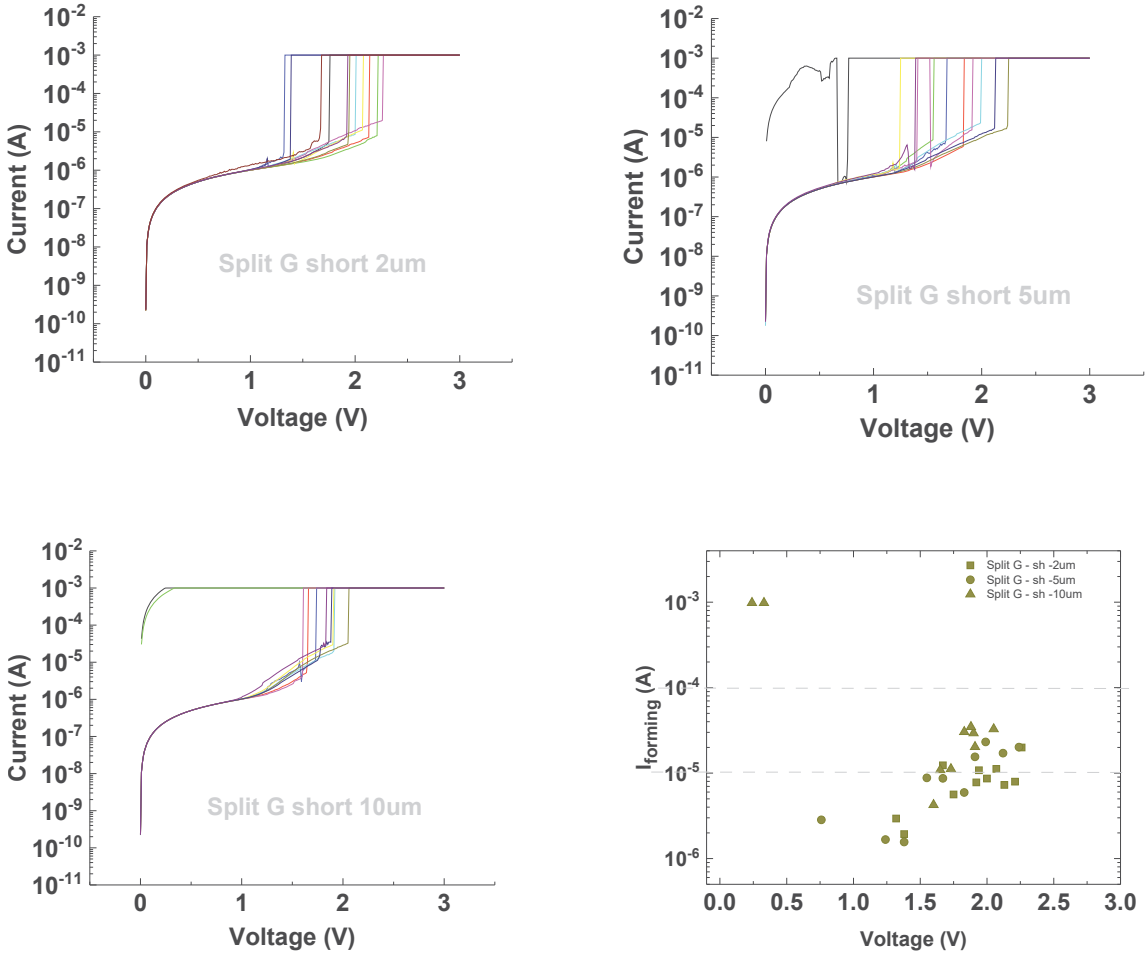


Figure 68. Forming behavior of CBRAM cells from process split G – short integration time

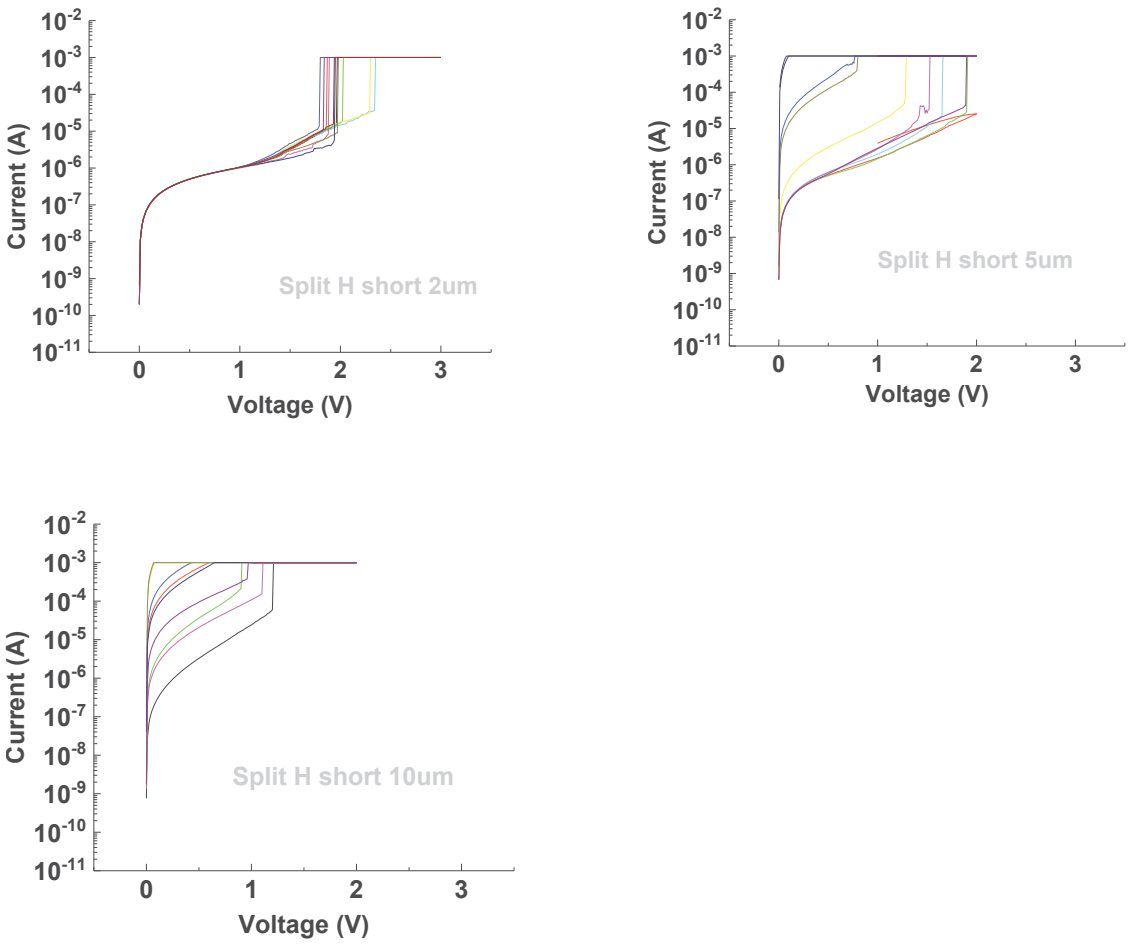


Figure 69. Forming behavior of CBRAM cells from process split H – short integration time

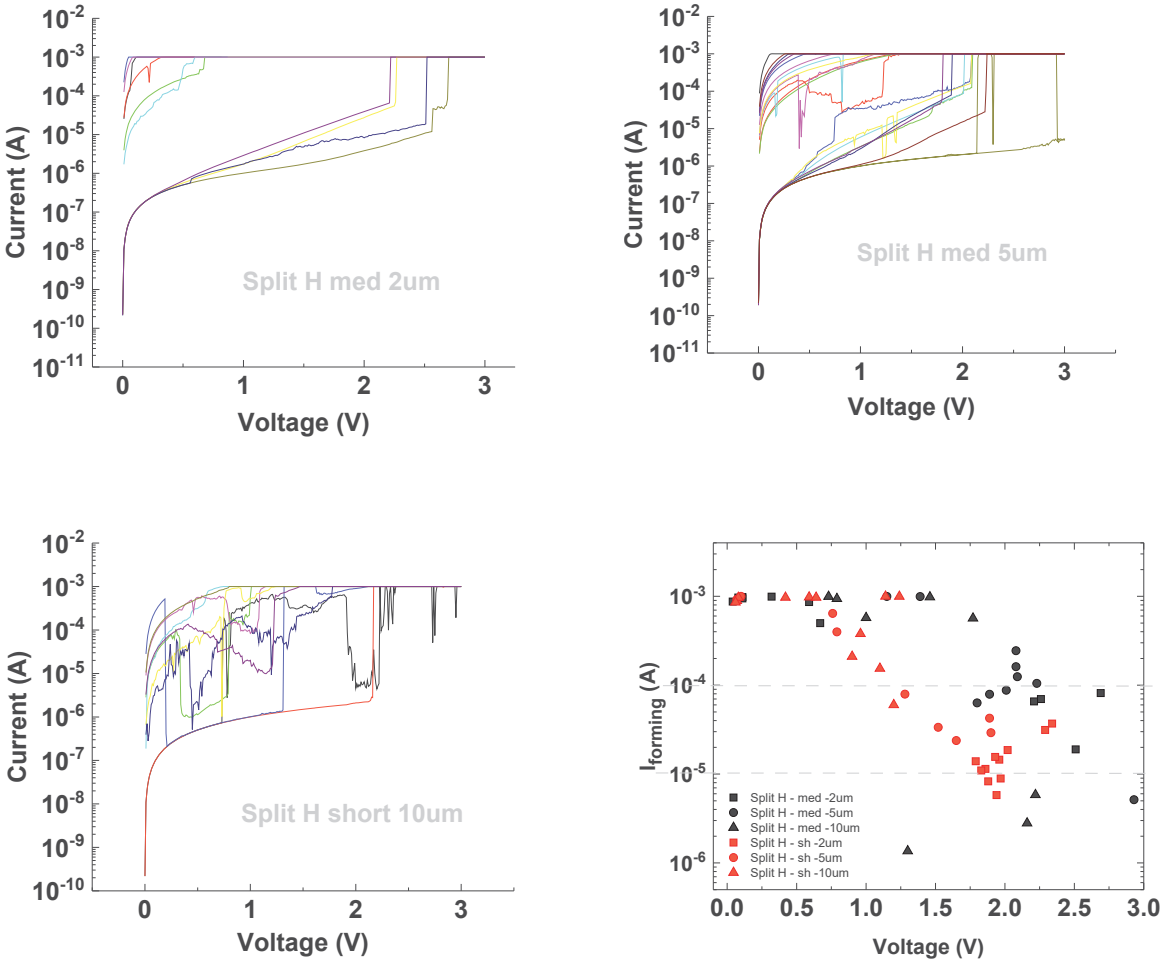


Figure 70. Forming behavior of CBRAM cells from process split H – medium integration time

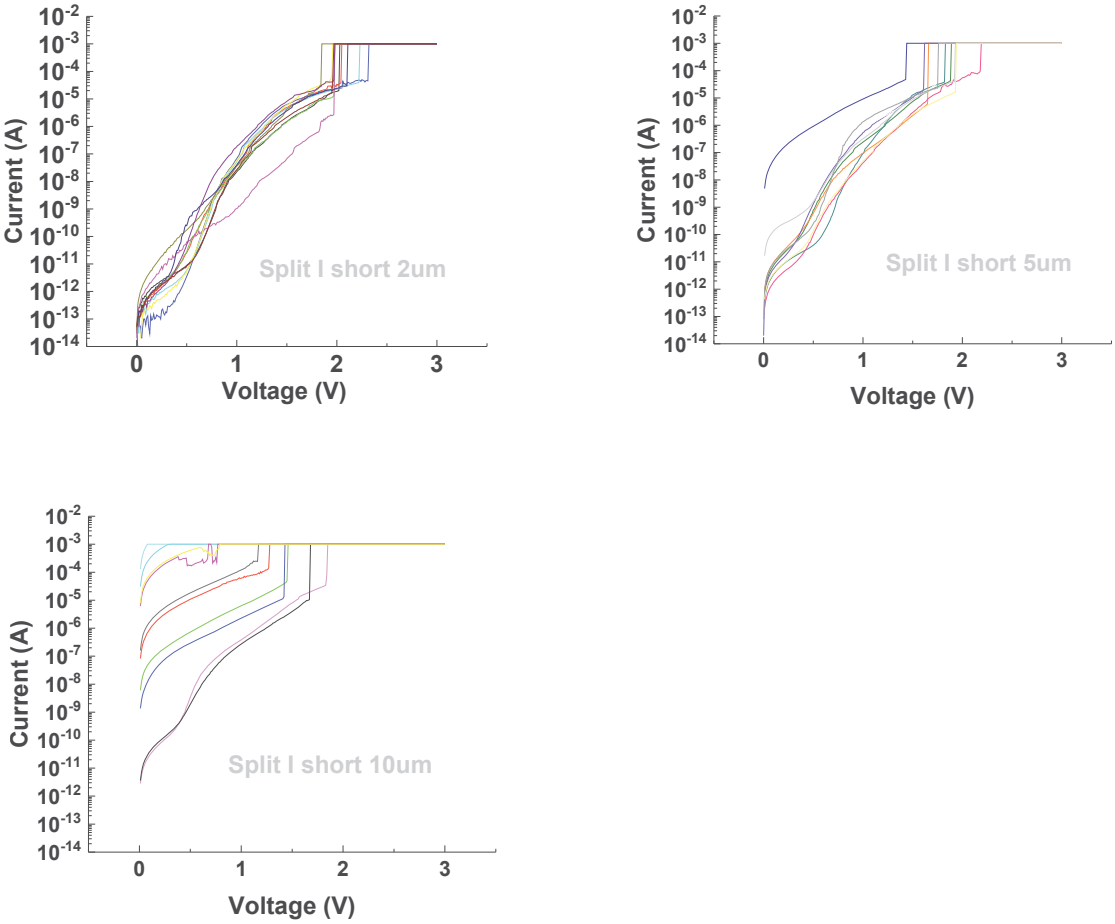


Figure 71. Forming behavior of CBRAM cells from process split I – short integration time

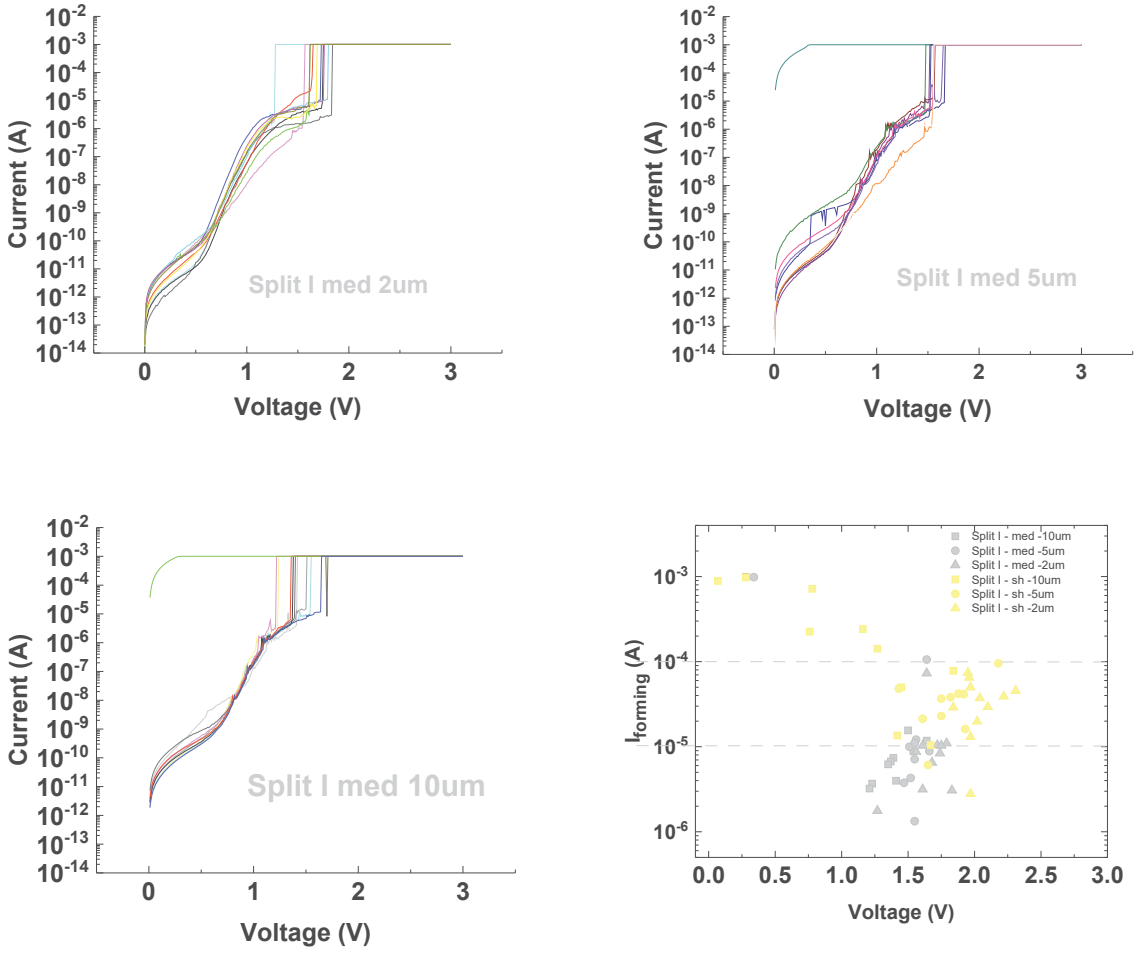


Figure 72. Forming behavior of CBRAM cells from process split I – medium integration time

4. FUTURE WORK

As part of the future work to be conducted on this CBRAM NVM memory cell, we believe that analyzing the current mechanisms at play during forming as well as during resistance switching will be of interest to understand the importance of cations and/or electron transport.

Additionally, since the porosity of the SiOx is thought to be a key parameter for designing a functional material, it will be interesting to characterize the porosity of the SiOx films obtained by PECVD for different processing conditions, and be able to justify the evolution of porosity with such conditions.

Different splits have demonstrated a cycling capability well beyond the 2000 DC cycles. DC cycling is understood as being a “high stress” switching, and pulse switching will have to be carried to asses the cycling well switching is conducted with voltage pulses.

Last but not least, retention on the presented splits has been recorded for over 48 hours at room temperature. The measurements being carried at room temperature as of now, the retention is not assessed as of now. Such retention will be part of the next steps of work on these down selected processing splits, and particularly high temperature retention o be able to obtain an accelerated estimate of the retention.

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

Acronym/ Abbreviation	Description
1T1R	One Transistor,One Resistor
AFRL	Air Force Research Laboratory
BEOL	Back-End-Of-Line
CBRAM	Conductive Bridge Random Access Memory
CF	Conductive Filament
CHG	Chalcogenide Glass
CMOS	Complementary Metal-Oxide-Semicondutor
CSSER	Center for Solid State Electronics Research
Cu	Copper
DFT	Density Functional Theory
DC	Direct Current
EDS	Energy Dispersive X-ray Scattering
GIF	Gamma Irradiation Facility
HRS	High Resistance State
IC	Integrated Circuit
IV	Current Voltage
ITRS	International Technology Roadmap for Semiconductors
LE-CSSS	LeRoy Eyring Center of Solid State Science
LET	Linear Energy Transfer
LRS	Low Resistance State
MBU	Multi-bit Upset
MEM	Metal–Electrolyte–Metal
NIEL	Non-ionizing Energy Loss
NVM	Non-volatile Memory
PECVD	Plasma-enhanced Chemical Vapor Deposition
PMC	Programmable Metallization Cell
QFL	Quasi-Fermi Level
REDOX	Reduction/Oxidation
RRAM	Resisitive Random Access Memory
SEE	Single Event Effect
SEU	Single Event Upset
SiOx	Silicon Oxide
SMU	Source Monitor Unit
SRIM	Stopping and Range of Ions in Materials
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose

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