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Superjunction Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) as a Pulsed Constant-current Load

by Timothy E. Griffin

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14. ABSTRACT

In this effort, I designed and tested a gate drive to pulse partly on a silicon (Si) superjunction high-voltage power metal-oxide-semiconductor field effect transistor (MOSFET) as a constant-current load. This load is for use in a reverse-recovery measurement circuit and is pulsed partly on during, up to 1 ms, and from just before the device-under-test (DUT) MOSFET is conducting until just after the DUT is off. Some measurements want a constant I_D; the load MOSFET had its initial partly on V_{GS} fine-tuned to select I_D up to 20 A, which is constant with load V_{DS} from a small value up to much of its rating. During the pulse, our control circuit measured I_D and maintained it somewhat constant, with feedback reducing the V_{GS}. I_D through the load's V_{DS} generated heat that reduced $V_{GS(th)}$, thus needing our feedback. This initial investigation found oscillations that made analog control not ideal to keep the load MOSFET I_D constant.

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1. Introduction

A reverse-recovery circuit for a device under test (DUT) such as a 4*H*-silicon carbide (SiC) power metal-oxide-semiconductor field effect transistor (MOSFET) needs a load to limit its I_D acceptably, and preferably, keep it at a constant value. Such a load would be located between the power supply and the reverse-recovery circuit's inductor, as shown in figure 1.

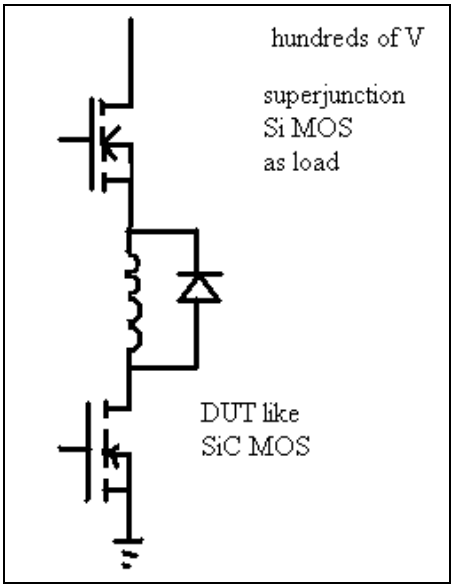

Figure 1. Reverse-recovery circuit with an Si MOSFET as a constant-current load.

The inductor and then the V_{DS} across the load limit the rate of building up inductor I_L. This setup provides more of a fail-safe and is simpler than limiting the DUT conduction time. For reverse-recovery measurements, the DUT would be double-pulsed to turn it on fully and build I_I nearly linearly with time rapidly, turn it off to measure its turn-off, and turn it on again to measure its turn-on for reverse-recovery testing. Choosing our load to be on for less total time, like 100 μs, would permit more I_D. The DUT would be ramped on for Q_{GS} measurement.

For the DUT with a resistor load, increased V_{DS} reduces I_D. Some uses of DUTs prefer or need measurement for a specific value of on-state I_D; for example, a pulse width modulation (PWM) motor drive controls the motor current. I used this Si MOSFET load pulsed on with a fairly constant I_D in a large range of V_{DS} from beyond the pinch-off point up to ¾ of its V_{DS} rating. For a given pulse time and V_{DS}, its datasheet had an I_D limit; I used up to 2/3 of that I_D. This is limited by junction temperatures like 150 °C and can lead to possible damage. When I_I approaches the load's limiting constant value, the $V_{DS\ load}$ rises rapidly to ($V_{supply} - V_{DS\ test,\ on}$). The DUT SiC MOSFET, starting at its low $V_{DS\ DUT,\ on}$, is turned off so its $V_{DS\ DUT}$ rises to V_{supply} while the I_I free-wheels through the anti-parallel diode. Then the DUT is turned on to conduct I_I

and the $V_{DS\ load}$ rises to ($V_{supply} - V_{DS\ DUT,\ on}$). The load's I_D through its V_{DS} gives heating and a temperature rise, during which I intend to control the load's V_{GS} properly for constant I_D (sensitive to small variations in V_{GS}). I worked with a circuit without the DUT, inductor, or flyback diode.

2. Material Thermal Considerations

The pulsed load needs adequate thermal conductivity of materials between the case and the hydroblok chill plate, 5.7 cm^2. Our first load MOSFET had its metal back connected to its drain, so it was on an electrically insulating ceramic aluminum nitride (AlN) 0.0635-cm thick and a heat sink compound on the chill plate. The AlN lists an electrical insulation of more than 10^{14} Ωcm and a typical thermal conductivity of 1.8 W cm^{-1} °C^{-1} at 25 °C, 1.33 W cm^{-1} at 100 °C, and 1.1 W cm^{-1} at 200 °C. Chemical vapor deposited diamond has a larger mismatch of coefficient of thermal expansion with copper, and it does not have proven good bonding with it (*1*). For SiC, the *n*-type low-doped Cree lists, at 25 °C, a large thermal conductivity 3–3.8 and 645.4 W cm^{-1} (T - 132.8 K) $^{-1}$ (*2*), and its high-doped value is 1669.1 W cm^{-1} (T + 627.3 K) $^{-1}$, which is higher than silicon's 1.5 W cm^{-1}.

For the electrically insulating heat sink compound, AI Technology Inc.'s Cool Silver, continuous to 150 °C at 0.12 W cm^{-1} °C^{-1}, was previously unknown. Given that I planned to use the compound for a brief time at a limited backside temperature, instead of using Electrolube HTSP (to 200 °C at 0.03 W cm^{-1} °C^{-1}), I used Arctic Silver 5, which has a thermal conductivity greater than 0.089 W cm^{-1} °C^{-1}, but withstands long-term to merely 130 °C and for peak to above 180 °C. Arctic Silver 5 consists, by weight, of more than 86% thermally conductive sub-micron zinc oxide (ZnO), aluminum oxide (Al_2O_3), and boron nitride (BN) ceramic particles of unique shape and size, in polysynthetic oils with no silicone oil. The compound at silicon microprocessor temperatures (less than 125 °C) initially thins out for contact and then thickens slightly over 50 to 200 h and several thermal cycles for maximum particle-to-particle conduction. Testing beyond the needs of this effort, it was cycled a few times to 180 °C then held at 200 °C for 17 h, after which it became dried up, flakey, and caked, and did not adhere to the AlN when that was lifted off, which is unacceptable. Replaced with new compound, after 170 °C for 2 h or after 200 °C for 10 min, it maintained its original appearance, ability to be moved, and adhesion; hence, it was acceptable for this effort. Thus, a transistor with an isolated baseplate could be placed on an electrically conductive surface, but to achieve a more direct connection to water-cooling, as by soldering, would be complex.

A Julabo recirculating chiller could begin the load near 0 °C, which would allow for an much increased rise in the load's junction temperature, but this process would condense atmospheric moisture, a condition which might be tolerable. Cooling details cannot further optimize the load.

3. Rejection of an Insulated Gate Bipolar Transistor (IGBT) as a Pulsed Load

As a pulsed load, an IGBT, even with a much larger I_G than a MOSFET, takes too many microseconds to switch. From our floating analog V_{GS}, this I_G is prohibitive, or even inconceivable. Using it as our load would heat the junction near to its limit, which would increase the turn-on rise time plus the turn-off fall time.

An IGBT simplifies as a MOSFET with its drain connected to a bipolar junction transistor's collector and with the MOSFET source going into the bipolar junction transistor (BJT) base. For Si, the V_{CE} of 1−1.5 V for an I_C of merely 1 A and around 10 V for constant maximum current is larger than for a MOSFET and our load's preferred need. In the usual switch-mode fully on, the conductivity modulation injects into the drift region minority carriers typically 100 to 1000 times the n^- doping (*5*); injection is slow, microseconds, and the turn-off current tail slowly removes carriers. An IGBT pulsed slightly above its $V_{GE(th)}$ in a rare linear mode for constant I_C is not necessarily faster due to reduced injection. Although a large enough IGBT has desirable ratings of thousands of volts, plenty of amperes, and for 1 ms pulse, a low thermal impedance, even for amperes of I_G the listed switching is too slow, several microseconds for a 6300-V Powerex CM600HG-130HF. An Advanced Power Technology 1200-V APT75GP120JDQ3 to 57 A emphasizes speed; with a 50 Ω generator, I directly drove 6.3 V into the V_{GE} for beginning I_C. I observed a too-slow turn-on of a 1-μs delay plus a 3-μs rise time; the I_C fall time was 200 ns. An IGBT lists its off-state leakage as being small, but it is larger than what is found in MOSFETs.

A Si MOSFET rated similarly to an IGBT can usually handle higher dI_D/dt, but perhaps lower dV_{DS}/dt. For the MOSFET, the external R_g controls these. I found minor Si IGBT future improvements, such as, at more than 3300 V (*3*), the emitter side has an enhanced planar gate cell and the collector side has light punch-through; the n^- drift is thinner for less loss; and it has a positive temperature coefficient for $V_{CE(sat)}$, a reduced tail current, a much lower junction leakage to 150 °C, and no snapback below 25 °C. A carrier stored trench bipolar transistor (*4*) now has a thin wafer, optimized backside collector profile in the high-voltage region, and an optimized *p*-base. A narrower trench pitch would reduce turn-off losses, and a retrograde doping for channel stop with negligible channel surface concentration could control the $V_{GE(th)}$.

4. SiC Power MOSFET

A large enough SiC MOSFET with adequate design, processing, and specifications for a pulsed load is not in production. Within its $I_D(V_{DS}, T)$ operating area, it needs adequate uniformity, durability, and stability with fewer nanopipes, basal plane dislocations, and other crystal defects. Temperature increase causes a decrease in mobility and slightly in $V_{GS(th)}$ to turn the MOSFET further on, nearing its maximum, and perhaps giving unwanted leakage or even turn-on (*6*). Others recommend not injecting minority carriers into a majority carrier SiC device, to avoid stacking fault growth. SiC MOSFETs have switching losses smaller than conduction losses to at least 10 kHz, and 100-kHz switching is considered (*7*). High frequency permits more ability for the PWM and a smaller transformer for a DC-DC converter, and prefers, for up to 2 kV, a SiC MOSFET over a SiC IGBT (which will emphasize several to 15 kV).

5. Superjunction Si MOSFET

A superjunction MOSFET has a more complex design including chip thinning for some improvements. If visualized as lying horizontally, it has very highly doped columns of *p*-type Si and *n*-type, laterally side-by-side, each having majority carrier conduction. The columns' height-to-width ratio may be up to 25 with trench filling by anisotropic epitaxial growth (*8*). A beginning superjunction SiC MOSFET is many years away but would need a much shallower required doping depth.

Superjunction MOSFETs list to 900 V with a fairly high I_D. Current density is notably higher, so the chip is smaller, but may suggest a short-circuit detection monitor of V_{DS} to turn it off. Instead, I control the I_D. The columns block lateral current, and hence, latch-up of the parasitic *npn*-bipolar transistor; their lateral pitch has become smaller over the years for smaller R_{DSon}. The charge-compensated columns have a difficult-to-fabricate, nearly perfect charge balance. These columns, when depleted of carrier charge starting at the *p*-*n* junction lines, block V_{DS} (rating desirably rising with temperature). Their R_{DSon} is dominated by the drift zone, and when not depleted of carriers, is lower than for a planar junction's lighter-doped Si (with voltage-driven vertical expansion of its space charge layer to block V_{DS}). For an Infineon 2008 coolMOS design, at MOSFET turn-on, the I_D neutralizes the charge in the *n*-columns and a voltage-driven drift current neutralizes the *p*-columns, at low forward V_{DS}. Column fabrication may have six cycles of epitaxial deposition then ion implantation, ending with diffusion. Turn-off is by the sudden, nearly intrinsic depletion of these columns. The *n*-columns are doped about 10 times more than in a non-superjunction MOSFET (*9*). The MOSFET antiparallel diode has a large surface, and so, a very low forward voltage drop, but has rapid reverse recovery at a high peak

current. For a V_{DS} above about 50 V C_{DS}, although increased by this large area, it is reduced by the depletion of the columns and wider space charge layer to below that of a non-superjunction MOSFET; the C_{GD} Miller capacitance decreases much faster. During turn-off, no carriers flow in the high field region, so there is no second breakdown phenomenon and the MOSFET can switch at high dV_{DS}/dt.

Si coolMOS 2005 designs can have dI_D/dt several hundred A/μs without dI_D/dt being dependent on I_D (*10*); 2000 A/μs (*11*) is not ultra-fast. For superjunction, the C_{oss} and its switching output energy loss for significant V_{DS} is only about half or less of other MOSFETs; for a similar $R_{DS(on)}$, the total gate charge is now 25% less than previous coolMOSs.

The R_{gate}, and not I_D and C_{oss}, should control dV_{DS}/dt (*10*). The coolMOS in 1998 included low R_{DSon} (*7*) and in 2001 lowered the $V_{GS(th)}$ to 3±0.5 V and lowered the internal MOSFET R_{gate}; rise and fall times were symmetrical. In 2004 the body diode had 1/10 the Q_{rr}. In 2005 the $R_{DS(on)}$, Q_{gate}, and switching time became ultra-small, then in 2008 they became small and V_{DS} = 900 V became available. R_{DSon} scaled as $V_{BDS}^{1.3}$ (no longer linear) and not as a non-superjunction's $V_{BDS}^{2.4}$ or $V_{BDS}^{2.6}$, so conduction losses scaled as $P_{out}^{2}V^{-0.7}$. For the same P_{out}, a larger V_{BDS} rating reduces conduction losses. Future stacking of Y-shaped field plates (YFET) gives the trench superjunction a compensation process window seven times that of oxide filled trenches (*12*), permitting much higher doping concentrations for specific R_{DSon} of 0.65 Ωcm^2 at a breakdown voltage of 680 V with a cell pitch of 4 μm. Since each superjunction MOSFET p^+ column does not conduct in the on-state, a charge sheet superjunction MOSFET (*13*) would replace the column by a thinner (for more conduction area) vertical sheet of insulator like Al_2O_3 containing fixed negative charge, around $-\varepsilon_s E_{Crit}/q$ or for Si, -2×10^{12} cm^{-2}.

The limit for our load MOSFET datasheet safe-operating area varies as $V_{DS}I_D(t\text{pulse})^{-1/2}$. Our first load was an Infineon IPW60R045CP, rated 45 mΩ, 50 V/ns for 1 ms at 600 V and 13 A; with our 300 Ω gate resistor, I_D rose in 20 ns or more and the speed was acceptable. Among MOSFETs, the IPW90R120C3 for 900 V and 1 ms is rated 3 A; a larger area would have been preferred. ST's MDmesh V STY112N65M5, rated 650 V, has a better (19 to) 22 mΩ. The IXYS IXFN32N120 has, for 1 ms, 0.01 °C W–1, implying at 1200 V, 10 A.

6. Superjunction MOSFET as a Pulsed Constant-current Load

In our reverse-recovery circuit, I preferred as a load a superjunction MOSFET singly pulsed, partly on for constant current. This setup has a better combination of small switching time, enough pulse time and I_D at V_{DS}, and low I_G for the floating drive. A level 50 to 67 A of I_I would have been preferred. The load needed to be verified as workable with any ringing, as from pulsing the DUT. The first load MOSFET IPW60R045CP had a single pulse of V_{GS} at about

4.1 V, below the 5 V of a plateau in Q_{gate} from 32 to 85 nC. Leakage I_D was minor for the junction temperature and off-state negative V_{GS}. I later limited the load's V_{DS} to about 2/3 of the rating so I_D did not begin to oscillate significantly.

Since the V_{GS} is less than 5.6 V, there is not an increase of the load MOSFET on-resistance with junction temperature to decrease the listed I_D, stop current localizations, and enable the parallel MOSFETs to share current. Hence, the load MOSFETs could not be in parallel without individual control of the I_D.

The development circuit had a DC link V_{supply} 0 to 1000 V Glassman, rated 8 A. Stiffening capacitors included two in series of electrolytic Cornell-Dubilier 550C, 500 V of 2700 μF having a resonance frequency 1300 Hz. Two in series of 3500 μF, three polypropylene 3 μF SCD305K122C3Z25, and a ceramic 0.1 μF 10GAP10 were in parallel. I did not use a segmented metalized polypropylene film, such as 1000 V and 470 μF, which would not dry out and has lower equivalent series resistance (ESR).

An Avago isolating linear sensing integrated circuit HCPL-7520 had an internal analog-to-digital converter. The 7520 analog output was from 0 V to well above 4 V, and through a resistor, drove the load MOSFET V_{GS}. More than its optical isolation of 891 V was preferred, since the load MOSFET V_S was at the sum of the tested MOSFET V_{DS}, preferably to 1200 V, plus the voltage across the inductor. The 7520 performance was not enough to justify a V_{GS} low-parasitic custom circuit board. For durability, the 7520 output I_G needed to be through 300 Ω, which was perhaps not ideally rapid for larger load MOSFETs. At the resulting speed, the feedback made V_{GS}, and hence I_D, prone to oscillations. Analog HCNR201 with light-emitting diodes (LEDs) illuminating two matched photodiodes would need a circuit of transistors and multiple supplies without clear performance. The load MOSFET gate drive in use would need an isolated power supply Pico DC linear TLAC5/300D, presenting two 5 V in series, with 1 mV rms ripple; the dummy minimum load used could select a 4.5 to 5.5 V supply to the 7520's $V_{(out\ VDD)}$ to adjust its V_{OUT}.

The gate supply's minimum load of small power could be a novel use of SiC junction barrier Schottky diodes. These below the designed voltage conduct little, but above that voltage conduct increasingly more, hence stiffening the supply. I could visually choose near where all the diode $I(V)$ curves for 25 °C through 150 °C changed little with temperature to select our diode current and its voltage; diodes in series would give the desired load voltage. The Cree 1 A, 600 V CSD01060 has a point at 1.1 V and 0.3 A; a halfwave surge could be 5.5 A for 10 ms. For a 20 A CSD20060 to 175 °C, I could choose 3 A at 1.1 V, with a low DC thermal impedance 1 °C W^{-1}. For the IPW60R045CP load MOSFET for 1 ms with 6 A, I limited it to 400 V to reduce oscillations.

In figure 2, the 33220A's pulse went to the 7520's V_{in+}, from which 10 nF goes to its input ground. Two of the current probes, TCP305 through its TCPA300 at 10 A/V, measured the I_D at 0.1 V/A to give V_{Id}, one went to the TDS5104 oscilloscope and the other to the V_{Id} from its BNC

output having 50 Ω to ground. That other V_{Id}, through a resistive divider of (2700 Ω in parallel with a 1N4148) to (47 Ω in parallel with 50 nF), went to the 7520's V_{in-}, from which 10 nF goes to its input ground. This V_{in-} decreased the load MOSFET V_{GS}, to make I_D more constant with time. V_{out} can swing to $V_{out\ GND}$ + 5 V. The 7520 amplifies $V_{in+} - V_{in-}$ as within –0.2 to 0.2 V by 9.8, to give V_{out}, supplying up to 11 mA. To filter input transients, from the 7520's V_{in+} to $V_{in\ GND}$ is 10 nF, and from V_{in-} to $V_{in\ GND}$ 47 Ω, later 75 Ω, in parallel with 10 nF. From the 7520's V_{out} went 300 Ω to V_{GS} and from that V_{out} went 30 nF (finally 120 nF) to the 7520's output ground to reduce ringing in the rise of V_{GS} seen in I_D.

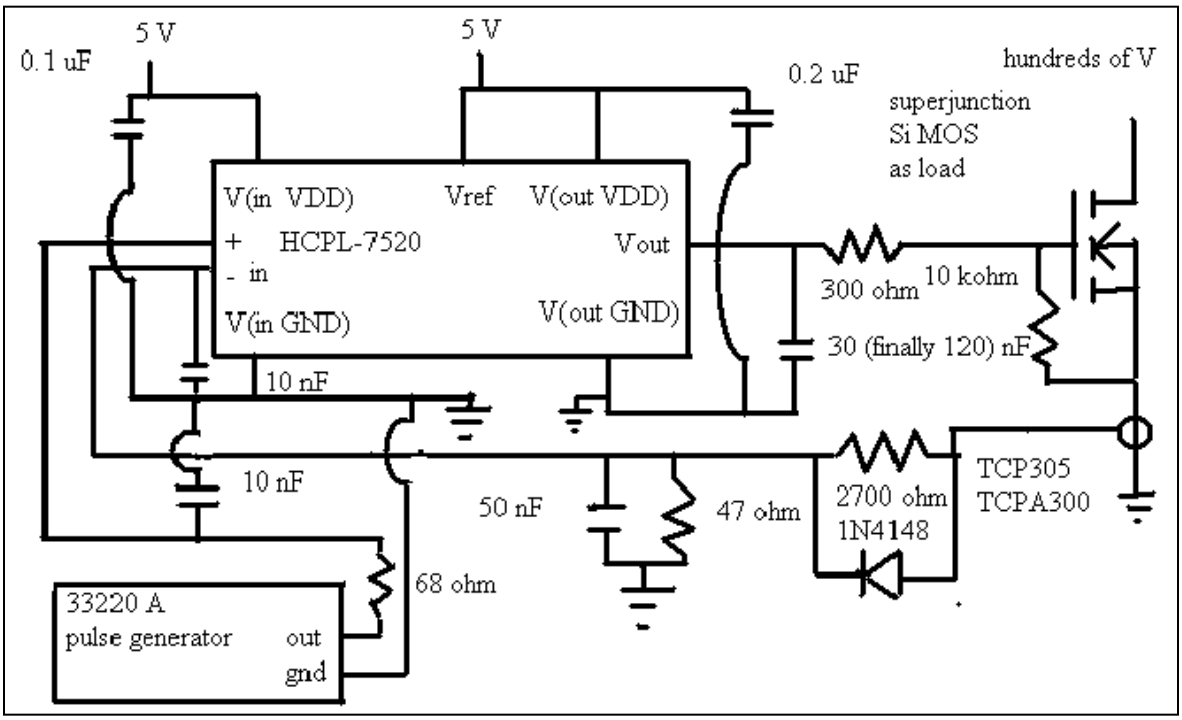

Figure 2. Gate control circuit for the load MOSFET.

Increasing to 450 V, the I_D late in the pulse oscillated too much. Figure 3 shows channel 3, the top line V_{GS}, decreasing; channel 1, the line one-from-top $I_{D;}$ channel 4, the flat line $V_{main\ supply}$ 450 V; and channel 3, the bottom line V_{in-} of 7520's with oscillation.

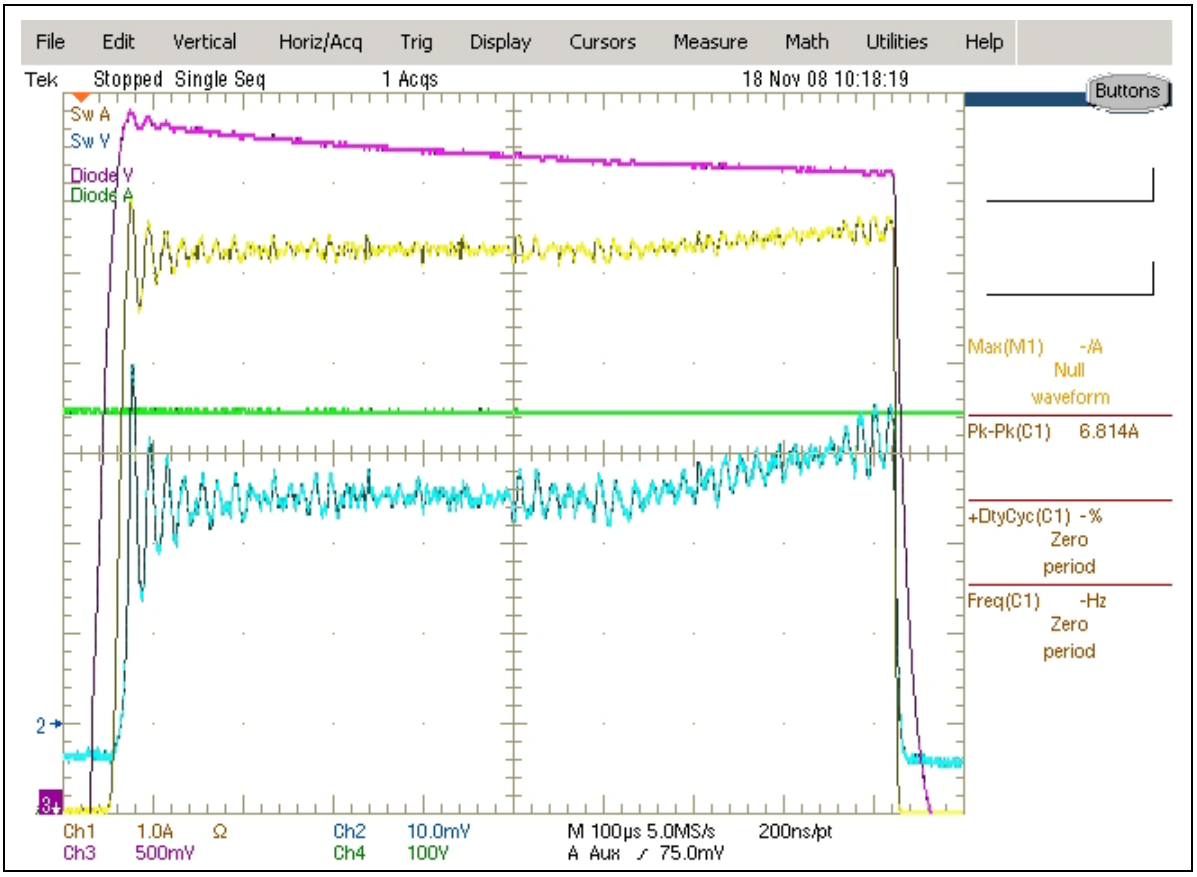

Figure 3. Oscilloscope trace of pulsed load MOSFET IPW60R045CP.

I changed to a load MOSFET ST STE40NK90ZD with a rating larger than 900 V, but to a mid-2006 design that was not as advanced. Its 3.8 cm by 2.5 cm copper case bottom was electrically isolated, so it was mounted with Arctic Silver 5 to the chill plate, now with flowing lab-chilled water. The junction-to-case thermal resistance was for DC, 0.2 °C W^{-1}, and for 1 ms, 0.014; within the safe operating area for 1 ms at 600 V is 17 A, and at 300 V, 34 A. $V_{GS(th)}$ is typically 3.75 V, decreasing with temperature to 0.56 times at 150 °C. It lists $R_{DS(on)}$ 0.14 to 0.18 Ω, increasing 2.25 times at 150 °C (STE45NK80ZD 800 V has a smaller value of 0.11 to 0.13 Ω). Listing with a 4.7 Ω gate resistor, a turn-off delay 450 ns, and then fall time 200 ns, it was fast enough with our 300 Ω gate resistor. Our Agilent 33220A linearly interpolated waveform was customized initially smaller to avoid initial overshoot from the 7520 and in I_D.

With a slightly slower rise, figure 4 shows channel 1, the top line $I_{D;}$ channel 2, the line rapidly increasing to one-from-top at right as 7520's V_{in-} to reduce V_{GS}; channel 4, the flat line V_{main} supply 300 V; and near it channel 3, V_{GS} gradually decreasing.

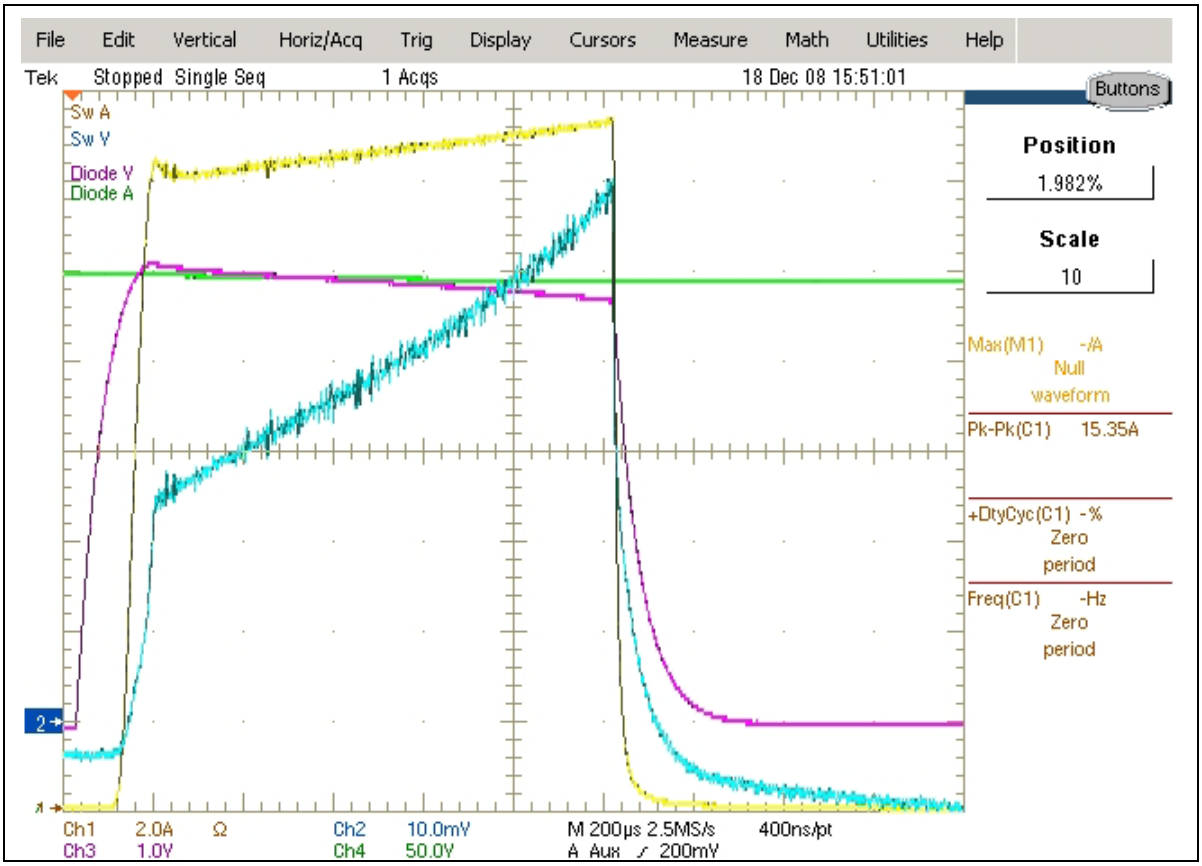

Figure 4. Oscilloscope trace of pulsed load MOSFET STE40NK90ZD.

I finally tried using V_{Id} as a divider (2700 Ω in parallel with two in series of a leg of Cree SiC C2D20120D Schottky diode) to 7520's V_{in-} and to (75 Ω in parallel with (0.56 µF to 300 Ω)) to $V_{input\ GND}$. The Schottkys were used seeking to reduce capacitance and oscillation.

The I_D feedback to decrease V_{GS} for the STE40NK90ZD had been reduced to control oscillation. Having I_D increasing notably is unstable; with I_D increasing above 16 A at 350 V and near 1 ms, this MOSFET blew even though it was supposedly rated 26 A. The future control circuit will be digital with transistor-transistor logic, through optocouplers HCNW-2611 for a 1414-V isolation. This would be to a floating DAC811 digital-to-analog converter, giving V_{GS} with more I_G. Initial work looked promising.

7. Conclusion

I tested a gate drive for a superjunction MOSFET as a pulsed constant-current load up to 1 ms. Heating decreased $V_{GS(th)}$ with time, so a measurement of I_D went through closed-loop control and reduced our floating V_{GS} to seek the needed, precise value for constant I_D. The MOSFET available as the load had a limited rating. The idea worked, but an analog optocoupler HCPL-7520 had problems with stability. A floating DAC811 digital-to-analog converter is planned for future testing.

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List of Symbols, Abbreviations, and Acronyms

Al_2O_3	aluminum oxide
AlN	aluminum nitride
BJT	bipolar junction transistor
BN	boron nitride
DUT	device under test
ESR	equivalent series resistance
IGBT	insulated gate bipolar transistor
LEDs	light-emitting diodes
MOSFET	metal-oxide-semiconductor field effect transistor
PWM	pulse width modulation
SiC	silicon carbide
YFET	Y-shaped field plates
ZnO	zinc oxide

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1 CD	US ARMY INFO SYS ENGRG CMND ATTN AMSEL IE TD A RIVERA FT HUACHUCA AZ 85613-5300
1 CD	COMMANDER US ARMY RDECOM ATTN AMSRD AMR W C MCCORKLE 5400 FOWLER RD REDSTONE ARSENAL AL 35898-5000
4 CDS 1 HC	US ARMY RSRCH LAB ATTN IMNE ALC HRR MAIL & RECORDS MGMT (1 CD) ATTN RDRL CIM L TECHL LIB (1 CD) ATTN RDRL CIM P TECHL PUB (1 HD) ATTN T GRIFFIN RDRL SED P (1 CD) ADELPHI MD 20783-1197

TOTAL: 11 (1 ELEC, 9 CDS, 1 HD)