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14. ABSTRACT

Silicon carbide (SiC) is a wide bandgap semiconductor with a power figure-of-merit ~400x higher than silicon. SiC power MOSFETs have been in commercial production since 2011, but they are still far from their ultimate limits of performance. The main limitations are the resistances of the MOS channel, the drift region, and the substrate. In this program we address all three resistances. To reduce the channel resistance, we introduce two new trench MOSFET structures. The tri-gate (3G) MOSFET applies FinFET geometry to vertical power devices for the first time, and the IMOSFET implements a deeply-scaled trench MOSFET using a fully-self-aligned approach. Both structures can reduce the channel resistance by 5 – 10x. To reduce the substrate resistance we etch a waffle pattern of depressions that penetrate 90% of the way through a thinned 200 µm substrate, and back-fill with electroplated copper for low thermal and electrical resistance. We have demonstrated substrate resistances ~3x lower than that of a substrate uniformly thinned to 110 µm, the process currently used in industry. To reduce the drift layer resistance we first evaluated superjunction structures, but the benefit in the presence of realistic charge imbalance was insufficient to justify the complexity of fabrication. Instead, we elected to use conductivity modulation by implementing an n-channel IGBT on an n+ substrate, where the buried p+ anode layer is contacted using our waffle substrate technology. In addition, we addressed the problem of limited short-circuit withstand time (SCWT) by introducing the concept of gate-charge scaling, wherein we reduce the oxide thickness and gate drive by the same factor. This increases the SCWT by that factor, with no impact on the on-state or blocking operation. At the time of this writing, the waffle substrate development has been completed, the first 3G-MOSFETs are being tested, and the IMOSFET and n-IGBT devices are still in fabrication. This project has resulted in two issued patents with two additional patents pending, six conference presentations, five journal papers, and a plenary talk at ICSCRM 2019 in Kyoto, Japan.

15. SUBJECT TERMS

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Dear Sirs:

As required by our contract, I am enclosing a copy of our final report on Army Research Laboratory Cooperative Agreement W911NF-15-2-0041.

Regards,

James A. Cooper
President

Revolutionary Innovation in SiC Power Devices

Cooperative Agreement No. W911NF-15-2-0041
Army Research Laboratory – Sonrisa Research, Inc.

Final Report
July 17, 2019

Executive Summary

Our program began by confronting the three main limitations to the performance of SiC power MOSFETs: (a) the MOS channel resistance, (b) drift region resistance, and (c) substrate resistance. Although our work is not finished, we have introduced new ideas and created new avenues for progress in all three areas, and we are close to first demonstration devices in all three areas. The progress and current status in each area are summarized in the next few paragraphs, with details provided in the body of this report.

Table 1 shows the different tasks and their time evolution during this project. Task 3.3 on superjunction (SJ) drift regions was discontinued following a pessimistic assessment of their cost/benefit ratio in SiC, and our approach to the drift resistance shifted to new Task 7.2 based on conductivity modulation of the drift region. The discontinuation of Task 3.3 also terminated Task 5. Our success in process development under Task 2 led us to propose a new Task 7.1 on fully self-aligned, deeply-scaled UMOSFETs. The work under Tasks 3.1, 4, and 7.1 will be continued under ARPA-E grant DE-AR0001009 that commenced on June 13, 2019. Task 7.2 will be continued under ARL cooperative agreement W911NF-19-2-0213 that began on August 8, 2019.

On the next four pages we summarize the progress under Tasks 3.1, 3.2, and 3.3, with details provided in the body of this report.

Table 1. Evolution of tasks during this project. Green shading indicates a high level of activity, and dots ••• indicate a continuing lower level of activity.

Task	Description		Year 1	Year 2	Year 3	Year 4
1	Perform 3-D Simulations					•••••
2	Develop New Unit Processes				•••••	•••••
3.1	Design & Fabricate 3G-MOSFETs					
3.2	Fabricate Waffle Substrates					
3.3	Design & Fabricate SJ Drift Regions				X	X
4	Fabricate 3G-WS MOSFETs					
5	Fabricate 3G-SJ-WS MOSFETs				X	X
6	Education, Collaboration, and Tech Transfer					
7.1	Develop Other Novel Devices	Design & Fabricate IMOSFETs				
7.2		Design & Fabricate WS-IGBTs				

Task 3.1: Addressing the Channel Resistance

FinFET or Tri-Gate (3G) MOSFETs

We began this project by proposing that the FinFET (or tri-gate) geometry used in silicon VLSI could be adapted to vertical SiC power MOSFETs. The resulting structure can be thought of as a conventional DMOSFET with trenches running perpendicular to the gate and source fingers, so that the sidewalls of the trenches provide additional current-carrying paths for the MOS channel without increasing die area. Our 3G-MOSFETs currently in fabrication have trenches that are 0.5 μm wide and 0.5 μm apart, with depths of 1.5 and 2 μm. These structures have deeper source and base regions that require MeV implantation energies and new masking technology. The trenches are coated with a deposited gate oxide and filled with polysilicon gate material. Simulations indicate that these structures reduce the channel resistance by between 7 and 9×, depending on trench depth. This will have the same effect as increasing the channel mobility by 7 – 9×.

During Years 1 and 2 of this project we developed etching, masking, and patterning technology for this novel structure. During Years 3 and 4 we fabricated demonstration devices for process verification and performance evaluation. We are working on eight quarter-wafers: two with 2-μm trenches and V_B of 900 V; two others with 2-μm trenches and V_B of 650 V; two with 1.5-μm trenches and V_B of 900 V; and two others with 1.5-μm trenches and V_B of 650 V. The first quarter-wafer having 2-μm trenches and V_B of 650 V completed processing in August, but suffers from gate-drain shorts believed caused by over-etching of the ILD window at the gate bonding pad. Seven other quarter-wafers are nearing completion but have not passed the critical oxide-etch step, so the etching issue can be corrected on those samples. We expect to finish processing the next quarter-wafer within the next eight weeks, followed shortly thereafter by the remaining six quarter-wafers.

Self-aligned, deeply-scaled trench MOSFETs (new Task 7.1)

In June 2016 we began to explore a fully self-aligned, deeply-scaled UMOSFET (IMOSFET) structure that uses fabrication technology already developed for the 3G-MOSFET. Simulations indicate that the IMOSFET should have similar on-state performance to the 3G-MOSFET, but it may be simpler to fabricate, potentially making it more manufacturable. Work on the IMOSFET has proceeded in parallel to the 3G-MOSFET. We are processing four quarter-wafers with epilayers to block 950 V (650 V rating), two with channel lengths of 0.53 μm and two with channel lengths of 0.70 μm. Included are devices with trench widths of 0.4, 0.5, and 0.6 μm on both the *a*- and *m*-planes of 4H-SiC. The samples have received all implants except the trench field-shield implant [1], which occurs after trench etch. We will perform the trench etch next, and we expect that fabrication will be completed during the first half of 2020.

Task 3.2: Addressing the Substrate Resistance

The resistance of the *n*+ substrate is the third major limitation of SiC power MOSFETs. *n*+ wafers of 4H-SiC have resistivities in the 18 – 27 mΩ-cm range and a thickness of 350 μm, giving them a specific resistance of 0.6 – 0.9 mΩ-cm^2. One approach to reduce this value is thinning the substrate at the end of the fabrication process. In their production MOSFETs, Infineon thins their substrate to 110 μm, reducing the resistance to ~0.3 mΩ-cm^2. Since our 3G-MOSFETs and IMOSFETs have channel resistance as low as 0.15 – 0.2 mΩ-cm^2, the resistance of an Infineon thinned substrate is still dominant, and needs to be reduced further. In the waffle substrate approach we first thin the substrate uniformly to 200 μm, then etch a waffle pattern with depressions that extend through all but 20 μm of the *n*+ substrate. Electrical calculations show this can reduce the substrate resistance to 0.075 – 0.10 mΩ-cm^2.

The waffle structure is intended to provide structural support while reducing the electrical resistance. We studied various waffle patterns using used 2-D Ansys™ simulations. A 200 μm thick substrate having waffle depressions 180 μm deep and area 200×200 μm, surrounded by unetched ridges 200 μm thick and 50 μm wide, has equivalent stiffness to that of a uniformly-thinned Infineon substrate, while reducing the resistance by >3×. The simulations have been calibrated by mechanical bending measurements on actual thinned substrates.

We have developed etching procedures using electroplated Ni as an etch mask that produce depressions with vertical sidewalls, no micro-trenching and minimal bowing at the bottom. Experiments on several wafers (24 discrete measurements) show a statistical variation in etch depth across a 100-mm wafer and from run-to-run of only ±5 μm for a 180 μm deep etch.

To reduce the thermal resistance, we developed a procedure for filling the depressions with electroplated copper that is planarized even with the tops of the SiC ridges. The one step that remains to be developed is bask-side laser annealing to form ohmic contacts prior to copper electroplating. Purdue does not have laser annealing equipment at the present time, and to date we have been unable to locate a vendor capable of handling 100-mm wafers.

Task 3.3 Addressing the Drift Resistance

Superjunction drift regions

In SiC power MOSFETs, the drift region resistance increases roughly as the square of the blocking voltage and becomes the dominant resistance in the device at $V_B > 1700$ V. In silicon MOSFET technology, the uniformly-doped drift region is replaced by a "superjunction" consisting of alternating pillars of *n* and *p*- doping. During the first 18 months of this project, we explored the idea of implementing superjunction drift regions in SiC. In addition to being difficult to fabricate, we evaluated their characteristics under varying degrees of charge imbalance between *n* and *p* pillars. The results are discouraging. If any degree of charge imbalance is present the drift resistance increases as the *square* of blocking voltage, just as a conventional drift region. The reduction in resistance is ~3× for a charge imbalance of 20%, and ~5× for an imbalance of 10%. While these reductions are desirable, in our judgment the

difficulty in fabricating superjunctions of sufficient thickness to be useful in SiC outweighed the potential benefits. Consequently, we suggested that the drift resistance problem could be more easily addressed using conductivity modulation, i.e. by fabricating an IGBT. This change in direction was approved in July 2017.

Waffle-substrate n-channel IGBTs (new Task 7.2)

Silicon IGBTs are the most effective power switches in the voltage range above 1 kV because their drift resistance increases as the *square root* of blocking voltage. This is due to conductivity modulation of the drift region by carriers injected from the substrate. IGBTs have two drawbacks: an additional voltage drop due to the forward-biased substrate / drift-region junction, and large switching loss due to the slow removal of minority carriers from the drift region. The added V_F in SiC IGBTs is ~3V, whereas it is ~0.7 V in silicon IGBTs. Nevertheless, IGBTs are attractive options for SiC at blocking voltages above 4 – 5 kV.

n-channel IGBTs are preferred because the electron mobility in 4H-SiC is ~9× higher than the hole mobility. However, *n*-IGBTs must be fabricated on *p*-type substrates, and *p*-type substrates in 4H-SiC are highly resistive. This has restricted *n*-IGBTs in SiC to blocking voltages ≥15 kV where the drift region is sufficiently thick to allow removal of the *n*-type substrate. In this program we are removing this limitation by inserting a thin *p*+ epilayer above the *n*+ substrate and contacting this epilayer by etching through the *n*+ substrate in a waffle pattern, as will be described below. We began the design, process development, and initial fabrication of a 10 kV *n*-channel DMOS-IGBT based on waffle substrate technology in July 2017. We are currently processing four quarter-wafers, two with lifetime enhancement of the drift region by interstitial diffusion of implanted carbon, and two without lifetime enhancement. The non-enhanced quarter-wafers have completed base and source implantation and are ready for base-contact implantation. The two lifetime-enhanced quarter-wafers have finished base implantation and are ready for source implantation. The fabrication procedure is the same as a conventional short-channel MOSFET except for the final step to etch a waffle pattern on the back side. We expect the first experimental devices to be completed by May 2020, with characterization completed by August 2020.

Task 6 Education, Collaboration, and Technology Transfer

Under this task we created an online process "cookbook" with detailed recipes for the various processes used to fabricate our devices. This resource is accessible on the web at *http://nanohub.org/groups.wbg/wiki/SiCCookbook.*

Under technology transfer, Sonrisa was approached by X-FAB Texas to assist in developing a production process module for (i) etching trenches in SiC suitable for use with trench MOSFETs, (ii) deposition and annealing conformal gate oxides in the trenches, (iii) filling the trenches with doped polysilicon, (iv) planarization of the upper surface of the polysilicon, and (v) deep *p*+ ion implantation to create and contact *p*+ field shields. These modules will enable X-FAB to fabricate either 3G-MOSFET or IMOSFET structures, as well as proprietary

UMOSFET structures of clients. A proposal has been submitted to the PowerAmerica Open Innovation Fund (OIF), and decisions will be announced in time for an October 1 start date.

Journal Publications and Conference Presentations

[1] Md. M. Alam, D. T. Morisette, and J. A. Cooper, "Practical Design of 4H-SiC Superjuction Devices in the Presence of Charge Imbalance," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2017)*, Washington, DC, September 17 - 22, 2017; *Materials Science Forum*, Vol. 924, pp. 563-567, 2018.

[2] M. Sampath, D. T. Morisette, and J. A. Cooper, "Comparison of Single- and Double-Trench UMOSFETs in 4H-SiC," poster presentation at the *International Conference on Silicon Carbide and Related Materials (ICSCRM-2017)*, Washington, DC, September 17 - 22, 2017; *Materials Science Forum*, Vol. 924, pp. 752-755, 2018.

[3] J. A. Cooper, N. Islam, R. P Ramamurthy, M. Sampath, and D. T. Morisette, "Vertical Tri-Gate Power MOSFETs in 4H-SiC," poster presentation at the *International Conference on Silicon Carbide and Related Materials (ICSCRM-2017)*, Washington, DC, September 17 - 22, 2017; *Materials Science Forum*, Vol. 924, pp. 680-683, 2018.

[4] M. Alam, D. T. Morisette, and J. A. Cooper, "Design Guidelines for Superjunction Devices in the Presence of Charge Imbalance," *IEEE Transactions on Electron Devices*, Vol. 65, No. 8, pp. 3345 – 3351, August 2018.

[5] J. A. Cooper, "Progress is Impossible Without Change: Innovation as a Driver of SiC Technological Evolution," [PLENARY] *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.

[6] J. A. Cooper, D. T. Morisette, and M. Sampath, "Increased Short-Circuit Withstand Time and Reduced DIBL by Constant-Gate-Charge Scaling in SiC Power MOSFETs, *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.

[7] M. Sampath, A. Salemi, D. T. Morisette, and J. A. Cooper, "The IMOSFET: A Deeply-Scaled, Fully-Self-Aligned Trench MOSFET," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.

[8] N. Opondo, J. A. Cooper, H. Liao, W. W. Chen, and D. T. Morisette, "The Waffle Substrate: A Novel Approach to Reducing Substrate Resistance in SiC Power Devices," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.

Patents and Patent Applications

[1] J. A. Cooper, "Methods of Reducing the Electrical and Thermal Resistance of SiC Substrates and Devices Made Thereby," U.S. Patent # 9,780,206, October 2, 2017.

[2] J. A. Cooper, "MOS-Based Power Semiconductor Device Having Increased Current Carrying Area and Method of Fabricating Same," U.S. Patent #9,997,599, June 12, 2018.

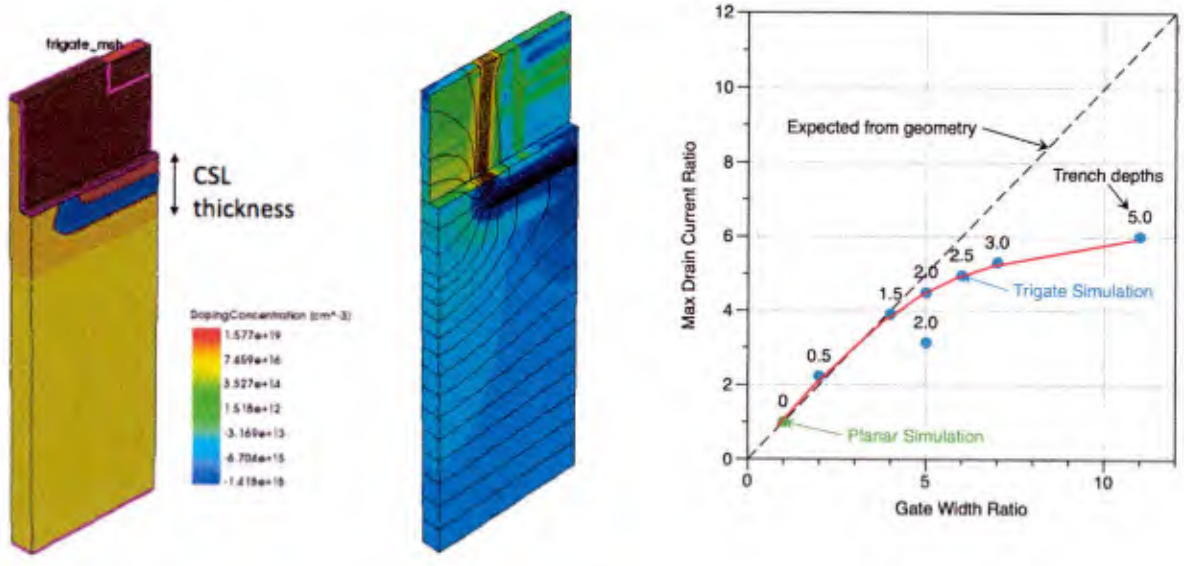
[3] J. A. Cooper, D. T. Morisette, and M. Sampath, "MOS Devices with Increased Short Circuit Robustness," U.S. Patent Application, submitted June 11, 2019.

1. Technical Progress Report

Task 1a: Tri-Gate MOSFET Simulations (Madan Sampath)

We have developed a flexible, 3D numerical simulation framework for optimization of the tri-gate structure using *Sentaurus Device* and related tools from Synopsis, Inc. There are several areas we investigated, including the influence of trench depth, JFET width, and JFET doping on the total specific on-resistance and blocking voltage of a tri-gate MOSFET.

Figure 1(a) shows the unit cell of the tri-gate simulation and Figure 1(c) shows the drain current ratio as a function of the gate width ratio (assuming equal mobilities on the sidewalls and horizontal surfaces). The drain current ratio is the factor by which the on-resistance is reduced compared to a planar DMOSFET. The drain current ratio follows the gate width ratio (dashed line) up to trench depths of ~ 2 μm. For deeper trenches the JFET resistance begins to dominate the on-resistance, and the improvement tapers off. This result is encouraging, and confirms our original estimate of a 2 μm optimal trench depth. Note that this analysis assumes *equal mobilities* on the sidewalls and horizontal surfaces, whereas in real devices we expect 2 – 3x higher mobility on the a-axis sidewalls. This will result in an even greater reduction in on-resistance.



(a) *(b)* *(c)*

Figure 1: (a) Simulated unit cell. (b) Unit cell in the on-state; color indicates current density and contours are electron quasi-Fermi levels. The gate oxide thickness is 40 nm. The applied gate voltage is VT + 6 V, and the drain bias is 0.2 V (b) Drain current ratio vs. gate width ratio as trench depth is increased from zero (a planar device) to 5 μm. The JFET width is 3 μm for all points except the lower point at a trench depth of 2 μm. For this point the JFET half-width is 1 μm. Any current ratio greater than unity represents an improvement over the conventional planar DMOSFET.

Another critical dimension that requires careful optimization is the JFET width. The simulation results shown in Figure 1(c) assume a JFET width of 3 μm except for the lower data point at a trench depth of 2.0 μm, which results from a JFET width of 1 μm. As the JFET width is reduced, the region becomes pinched-off by depletion regions surrounding the adjacent p-wells, thus increasing the JFET resistance. On the other hand, as the JFET width is increased, the area consumed also increases, again increasing the specific on resistance (resistance-area

product). There is an optimum point between these extremes where the contribution of the JFET region to the overall specific on-resistance is minimized, as illustrated in Figure 2. This minimum occurs at a JFET width of approximately 3.5 μm for this JFET doping. We will fabricate devices with several JFET widths to experimentally confirm the best JFET width.

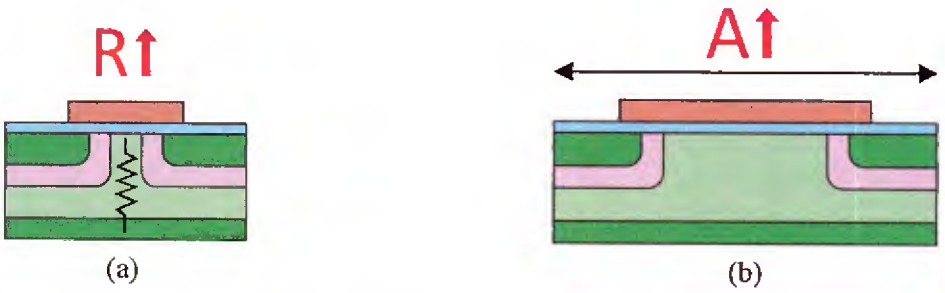


Figure 2: Specific on-resistance due to non-optimum JFET region widths: (a) too narrow leads to high resistance (b) too wide leads to large area.

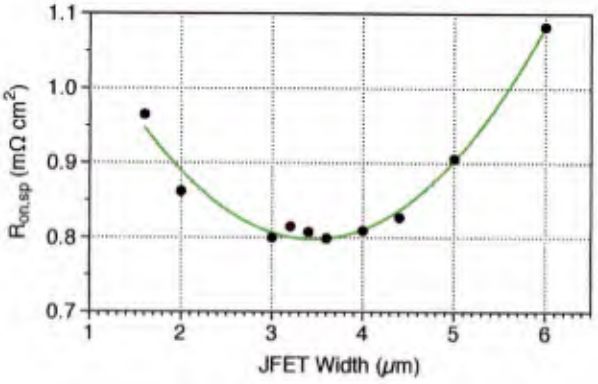


Figure 3: 3D simulation of the 3G-MOSFET specific on-resistance vs. JFET width.

After developing a 3-D Sentaurus Device simulation of the 3G-MOSFET, we simulated the half unit cell to identify the optimum design in terms of specific on-resistance and blocking voltage. We are using the approximate breakdown analysis model available in Sentaurus Device for calculating the blocking voltage of the 3G-MOSFET. This model solves Poisson's equation and calculates the resulting ionization integral, and produces reasonably accurate results with dramatic reductions in computation time. We have verified the accuracy by comparison with simulations which include the hole and electron continuity equations.

We found that the *n*-type current spreading layer (CSL) plays an important role in determining the blocking voltage of the MOSFET. The unit cell in Figure 1(a) should have a breakdown voltage of 930 V based on a planar one-sided step junction model, but the simulated breakdown voltage is only 640 V. However, when we reduce the thickness of the CSL layer so it doesn't extend below the *p*-base implant, the blocking voltage rises to 900 V, and when we remove the CSL layer entirely it becomes 950 V. The higher doping of the CSL layer produces a steeper gradient in the electric field just below the *p*-base junction, resulting in a lower breakdown voltage.

However, the purpose of the CSL layer is to spread the current from the JFET region more efficiently into the drift region, so reducing the CSL thickness also increases the specific on-resistance. We investigated this trade-off to find the optimum thickness of the CSL layer by maximizing the figure-of-merit $V_{BR}^2/R_{on,sp}$. Figure 4 shows the variation of $V_{BR}^2/R_{on,sp}$ vs. JFET width for different CSL thicknesses. A CSL that extends 0.6 μm below the trench bottom provides the highest figure of merit for nearly all JFET widths.

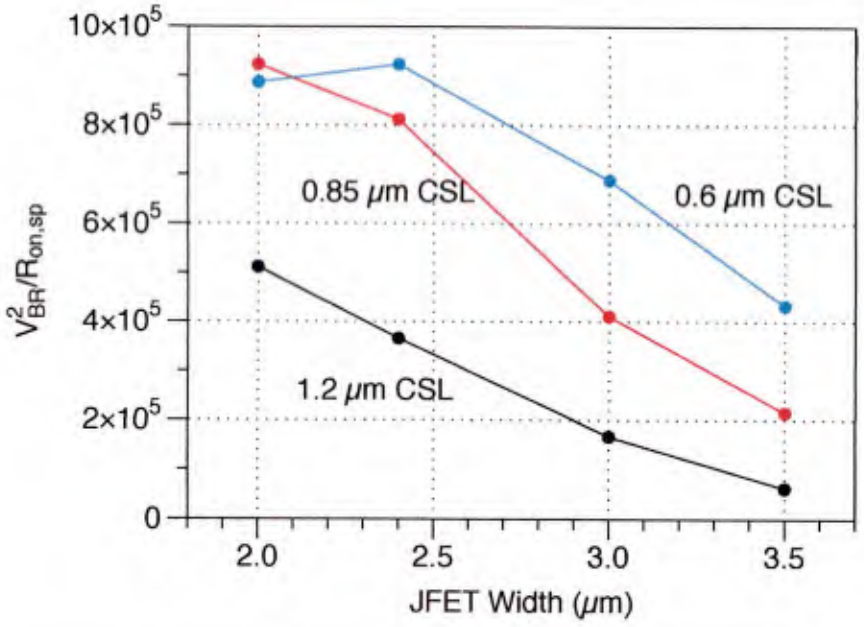


Figure 4: Figure of merit vs. JFET width for different CSL thicknesses.

To investigate further, we fix the JFET width at 2 μm and vary the CSL thickness. Figure 5 shows the variation of specific on-resistance, blocking voltage, and figure of merit as a function of CSL thickness. The plot shows that the maximum figure of merit occurs at a thickness of 0.85 μm, but in this region the blocking voltage is very sensitive to CSL thickness. Therefore, it is better to select 0.6 μm, giving up a slight increase in figure of merit to make the blocking voltage less sensitive to variations in CSL thickness that may occur in a real device. These optimizations were incorporated into the prototype tri-gate MOSFETs which are currently nearing completion.

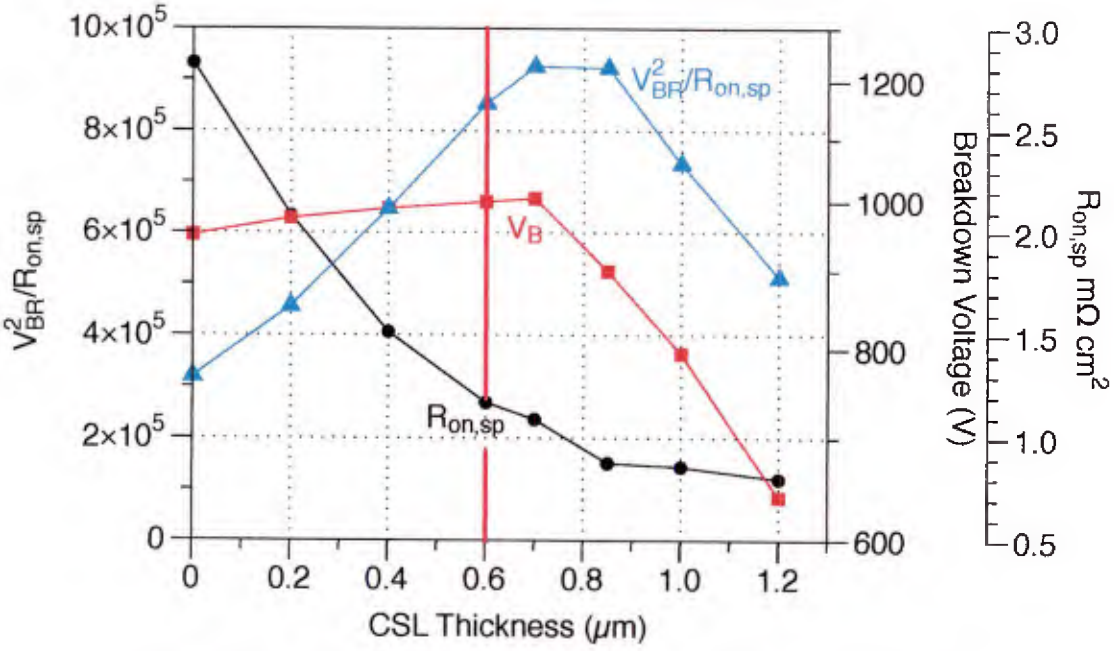


Figure 5: Performance vs CSL thickness for a JFET width of 2.0 μm. The red line is the selected design point.

Task 1b: IMOSFET Simulations (Madan Sampath)

Ultra-Scaled IMOSFET vs. Commercial UMOSFET Performance

Commercial trench MOSFETs from both Rohm and Infineon incorporate field shields for gate oxide protection, but both have only one MOSFET channel per trench, so we refer to them as "single-channel" UMOSFETs. By comparison, the IMOSFET has two channels per trench and the self-aligned field shield provides more complete oxide protection than either the Rohm or Infineon designs. In 2012, ROHM Semiconductor reported a novel double-trench UMOSFET with separate gate and field-protection trenches [2]. Their simulations predicted a specific on-resistance $R_{on,sp}$ of 0.79 mΩ-cm^2 at 630 V, and 1.41 mΩ-cm^2 at 1260 V, although these predictions did not include substrate resistance. An alternative, the single-trench oxide-protected UMOSFET, was first reported in 1998 by Purdue. These two structures are illustrated in Figure 6, and based on common design rules, the cell pitch for double trench is ~2.5x larger than the single trench alternative. Since UMOSFET specific on-resistance is proportional to cell pitch, one would expect the single trench alternative to be clearly preferable. However, we undertook a simulation study to verify this expectation and to understand whether or not the double trench concept had other unforeseen benefits.

A current spreading layer (CSL) has been added below the base in both structures to prevent JFET pinch-off and promote lateral current spreading and fully optimize both designs. The CSL can extend deeper in the single-trench device because this structure provides greater protection of the gate oxide, as will be discussed below.

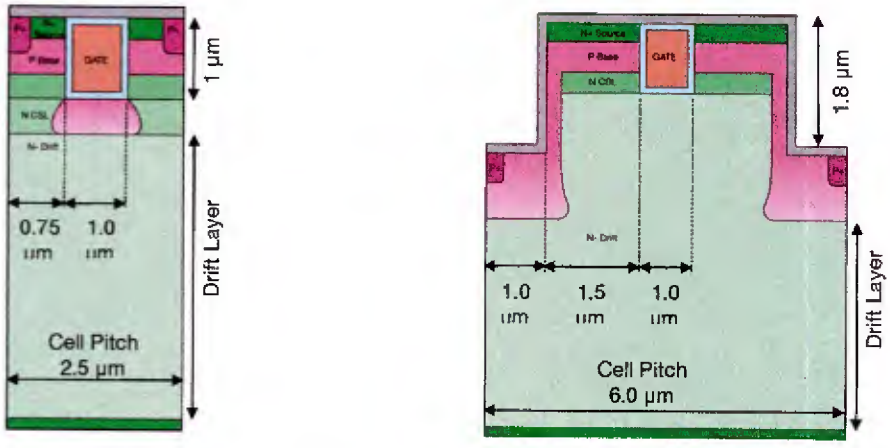


Figure 6: Simulated single-trench (a) and double-trench (b) UMOSFET structures

Figure 7 shows the simulated electric field plot for both devices at $V_{DS} = 600$ V and $V_{GS} = 0$ with the same scale. The source trench requires a deeper implant than the gate trench to adequately shield the gate oxide in the double trench design. In the expanded view, we can see the oxide electric field is much higher in the double trench, because in the single trench protects the oxide completely. The maximum oxide field in the single-trench device is 2.0 MV/cm, whereas in the double-trench it is 3.9 MV/cm. The lower oxide field leads to much higher oxide reliability under operational conditions.

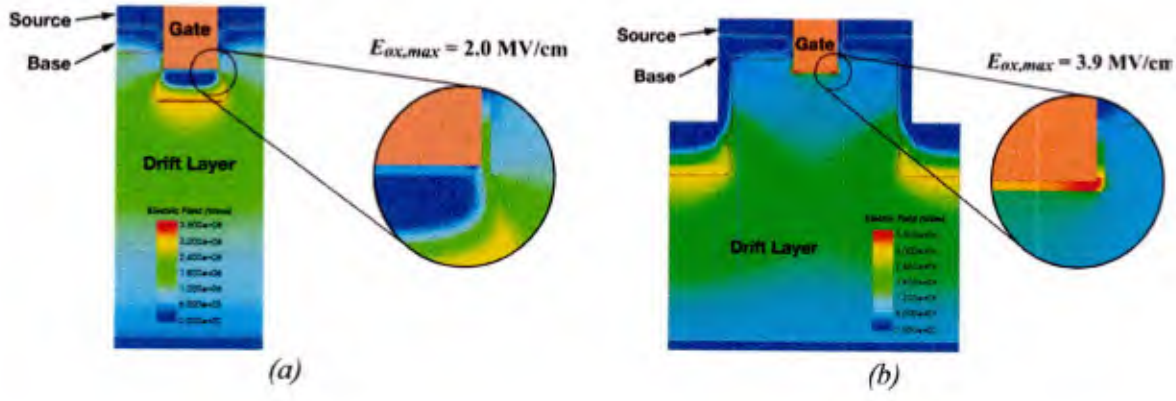


Figure 7: Simulated electric field distribution at breakdown for (a) single-trench and (b) double-trench UMOSFETs

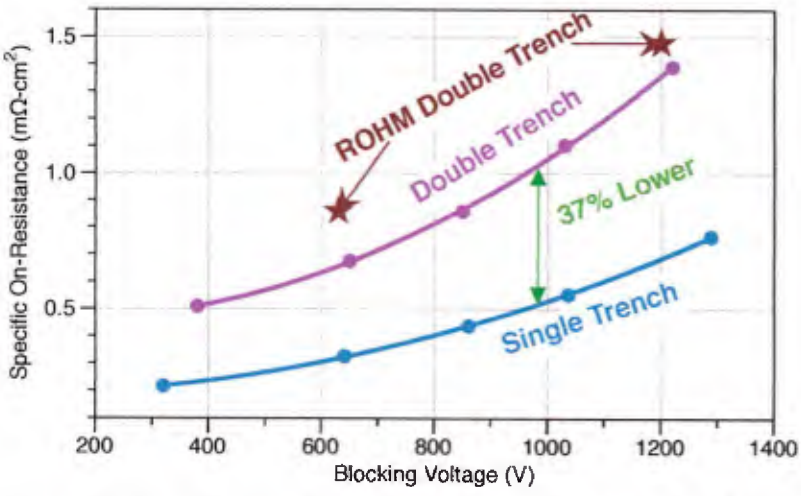


Figure 8: Ron,sp vs. V_B for single- and double-trench UMOSFETs

Figure 8 shows the simulated specific on-resistance $R_{on,sp}$ *vs.* V_{BR} for single- and double-trench UMOSFETs, and it can be seen that the oxide protected single-trench design has lower $R_{on,sp}$ than the double trench structure by ~37%. The $R_{on,sp}$ calculations include a substrate resistance of 0.069 mΩ-cm^2 in both devices, which corresponds to the expected resistance of a waffle substrate. As expected, the major factor in the lower $R_{on,sp}$ of the single-trench device is the lower cell pitch, which permits more cells in a given area.

Optimization of the Ultra-Scaled IMOSFET

In this section, we present results of simulations performed to determine the practicality and expected performance of an oxide protected UMOSFET scaled down to dimensions similar to that of the 3G-MOSFET, as depicted in Figure 9(a). These devices, with a cell pitch of 0.5 µm, can be fabricated from the same unit processes used in the 3G-MOSFET. The doping of CSL layer is 1.2 x 10^{17} cm^{-3}. The total dose of the implant is selected such that the electric field does not punch through to the oxide. The UMOSFET will be fabricated in a stripe geometry, and will have P+ contacts in a separate plane than the one shown in the figure. Figure 9(b) shows the forward bias plot for V_{DS} = 0.2 V and V_{GS} = 12 V. The colour depicts the current density, and the line contours represent 20 equally spaced electron quasi-fermi levels spaced 10 mV apart, which help illustrate where the dominant potential drops occur within the device. Figure 9(c) shows the simulated electric field at breakdown (V_{DS} = 600 V, V_{GS} = 0 V), which shows that the trench implant completely protects the oxide and prevents base punch through.

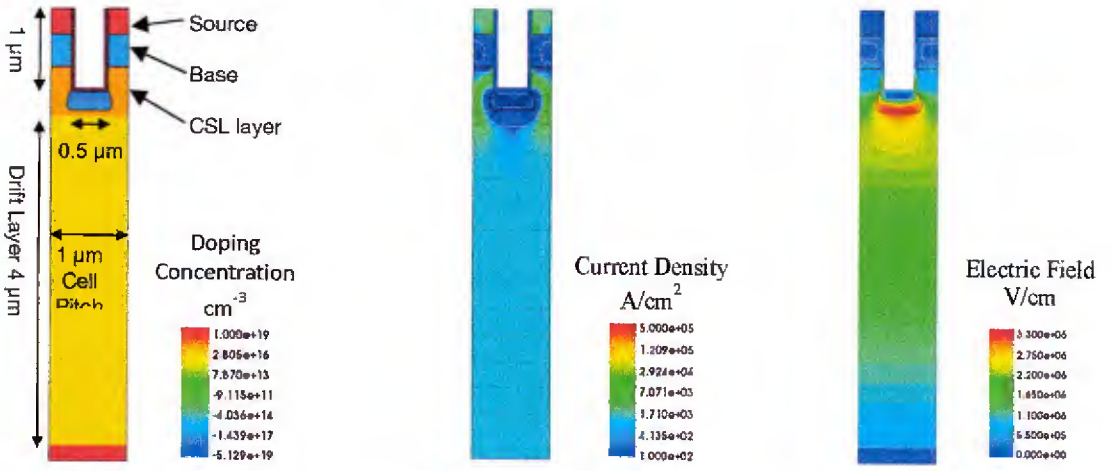


Figure 9 (a) Scaled UMOSFET (IMOSFET) simulated structure in (b) forward bias (c) reverse bias

Figure 10 compares the specific on-resistance of a Rohm single-channel UMOSFET on a 100 µm thick substrate to an IMOSFET on a 100 µm substrate, and to an IMOSFET on a waffle substrate. An IMOSFET on a 100 µm substrate has less than half the resistance of a single-channel UMOSFET. Combining the IMOSFET with a waffle substrate yields a specific on-resistance up to 5x lower than that of a single-channel UMOSFET. As $R_{on,sp}$ is reduced, the absolute resistance specification can be met with smaller die and the number of die per wafer increases. More die per wafer means lower die cost, making SiC MOSFETs more competitive with silicon MOSFETs and IGBTs at blocking voltages as low as 400 V.

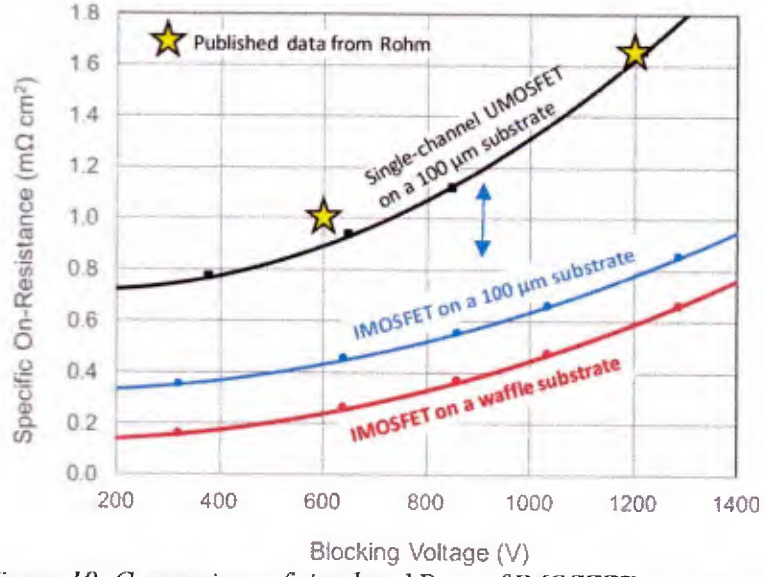


Figure 10: Comparison of simulated $R_{on,sp}$ of IMOSFETs compared to existing commercial trench MOSFETs

We continue to work on how far we can push the UMOSFET scaling limit to reduce cell pitch as far as possible. However, scaling beyond the 0.5 µm cell pitch depicted above becomes difficult due to pinch-off at the trench implant junction from one cell to the next, which requires an increase in CSL layer doping. This in turn causes premature breakdown due to field crowding

at the corner. However, we have several ideas in development to solve these problems and permit scaling well below 0.5 µm cell pitch.

Task 3.1a: Trigate MOSFET (Naeem Islam, Rahul Ramamurthy)

Tri-gate Device Design and Mask Layout

The trigate MOSFET can be visualized as a standard planar DMOSFET with trenches etched perpendicular to the source regions. The sidewalls and upper and lower surfaces of the trenches form the inversion channel for the MOSFET. Two important cross sections through the trigate MOSFET, along with some of the key dimensions are shown in Figure 11. Two blocking voltages are targeted where the trigate MOSFET will have a significant impact: (a) 650 V specification (930 V breakdown), and (b) 930 V specification (1,300 V breakdown). The corresponding drift regions will be (a) 5.4 µm, doped 1.4 x 10^{16}cm^{-3}, and (b) 8.4 µm, doped 1 x 10^{16} cm^{-3}. In both cases, the JFET region and current spreading layer will be doped 1 x 10^{17} cm^{-3}, with the latter extending 0.5 µm below the bottom of the p-base implant.

The devices are fabricated on one quarter of a 4 inch SiC wafer, which was purchased from Cree, Inc. A single die is 1.04 cm square, and a matrix of 11 die is included in each quarter. Every die contains two modules: Device Module and a Process Control Module (PCM). The features in the device module can be classified into two broad categories. The areas containing features with minimum dimensions less than 2 µm are considered "fine" category and will be written by e-beam lithography. All other areas will be defined by optical lithography. The overall layout of die is shown in Figure 12.

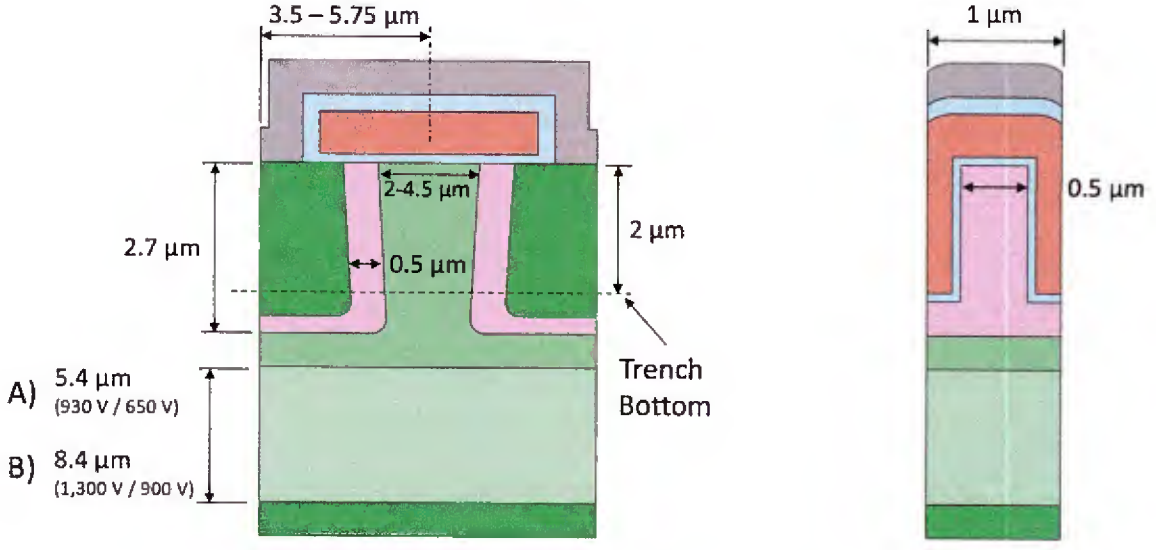


Figure 11: Cross sections of the 3G-MOSFET (a) through the fin centerline and (b) perpendicular to the fin through the channel region

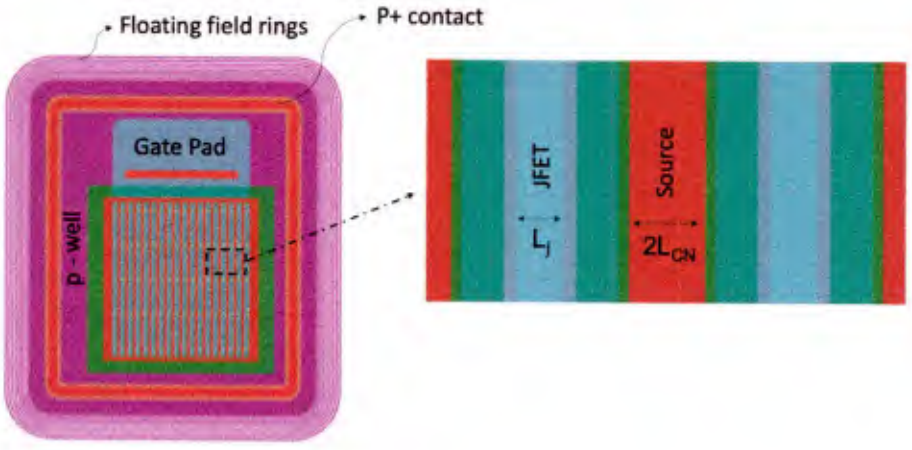


Figure 12: JFET length (L_J) and source contact length (L_{CN})

Based on 3-D simulations of the trigate described in a previous section, the optimum JFET width W_J is approximately 3.5 µm. To verify this experimentally six devices with JFET widths ranging between 2.0 and 4.5 µm, in steps of 0.5 µm are included in the device module. Based our previous experience with NiSi contacts to SiC, 3D simulations, and from recent test runs, we believe that a 0.5 µm source ohmic contact width L_{CN} will provide sufficiently low contact resistance. The resulting cell pitch will range from 3.5 to 5.75 µm. The process control module (PCM) consists of test device structures that are each uniquely designed to verify a particular step in the trigate MOSFET fabrication process. The 3D geometry of the trigate structure requires test devices on the top, bottom, and sidewall surfaces to extract information such as mobility and contact resistance. The PCM includes TLM, MOSCAP, MOSFET, interlayer dielectric (ILD) breakdown, and p-well spacing test devices.

Tri-gate MOSFET Process Development and Fabrication

Implementing the layout plan described above and the realization of the trigate MOSFET requires rigorous development of process technology, some of which have never been applied to power MOSFETs before. The main fabrication steps of the trigate MOSFET process are depicted in Figure 13.

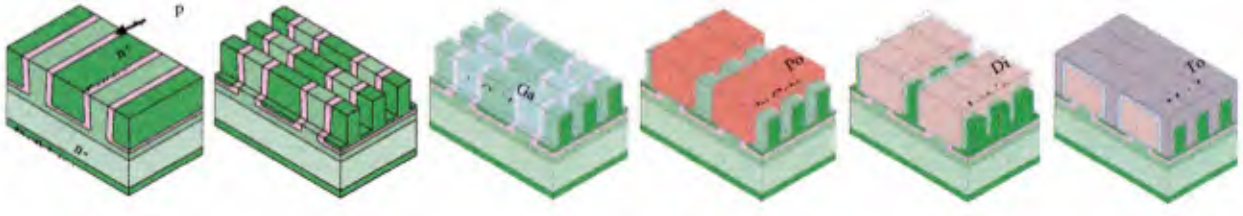


Figure 13: Steps in the fabrication of the trigate power MOSFET: (a) implant p-base and n+ source using a self-aligned process; (b) etch trenches perpendicular to the source stripes; (c) deposit gate oxide and anneal; (d) deposit and dope polysilicon gates to fill the trenches, then pattern poly into stripes; (e) form a thick oxide over the gates by thermal oxidation and clear the oxide over the exposed SiC by a short BHF dip; (f) deposit ohmic metal and anneal to form source and base contacts, then deposit top metal over entire active area.

The goal is to develop a unified process for the trigate MOSFET that is manufacturable with high yield and at low cost. The approach taken was to first identify, develop and demonstrate the critical unit processes. Once demonstrated, these processes are integrated together into a single process for the complete device.

Self-aligned, short-channel base and source implants

Fabrication of the tri-gate MOSFET requires high-energy implants to form the source and base regions of the transistor. A self-aligned process is used to define the channel of the device, using polysilicon as an implant mask. A polysilicon film of 4.8 μm thickness is required to block the base implant, and this is deposited by LPCVD. The first step is to etch windows in the polysilicon layer to allow the Al implant to form the base region. Such high aspect ratio, highly anisotropic etching of polysilicon is challenging. In the original plan, this step involved two lithography steps: 1) e-beam liftoff lithography to pattern a metal mask over the JFET regions and floating field rings (FFR), and 2) an optical liftoff lithography step to define a metal mask over the inactive field area of the device and form the larger, less critical test structures. The metal, in this case a 200 nm bi-layer of Ti and Ni, would act as a mask during RIE etching of the underlying polysilicon film. This process was successfully developed on small test samples without micro-masking. However, when the same process was carried out on the larger area 3G-MOSFET samples, we observed severe micromasking in the etched region.

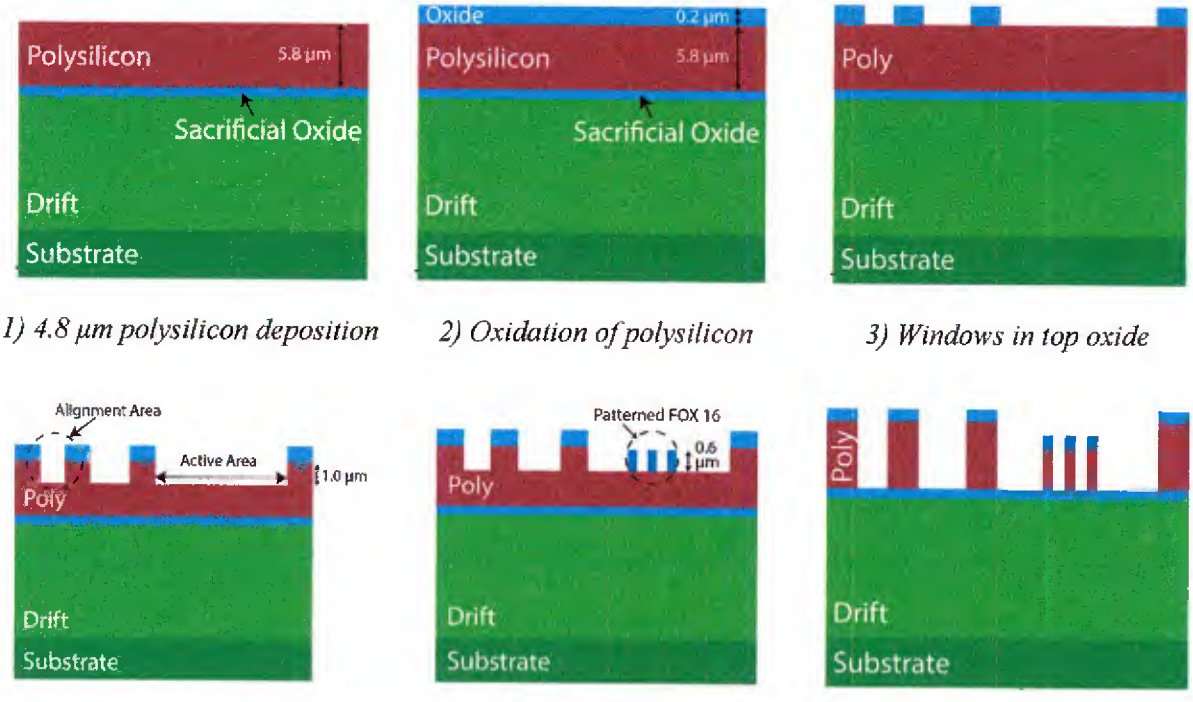
To avoid micromasking during the etching of the polysilicon implant mask, we developed an oxide masking process that is compatible with commercial Si production facilities. The process requires a reversal in the sequence of the lithography and the tone of the resist compared to the previous process. E-beam lithography is used in the active area. Here an HSQ (hydrogen silsesquioxane) resist known as FOX 16 us used to mask the polysilicon implant mask. In the larger, non-critical areas an optically-defined thermally-grown oxide layer is used to mask the polysilicon implant masking layer. FOX 16 is an inorganic compound composed of $[HSiO_{3/2}]_n$ clusters, and is a negative-tone resist. Under electron irradiation, the material converts to SiO_2, thus resulting in an all-oxide mask for the polysilicon etch. This process can use the existing mask design with no increase in e-beam exposure time.

Figure 14 illustrates the flow of the new oxide-only process. First, the deposited polysilicon is oxidized to form a 200 nm film of SiO_2. Windows around the device active area, process control modules, and alignment marks are opened in the oxide using photolithography and wet etching in BOE. In order to align the subsequent e-beam lithography step that forms the JFET and FFR regions, alignment marks ~ 1 μm deep are etched into polysilicon layer. This etch is carried out in a Cl_2-based plasma at 175 watts rf power and 50 watt bias power under 1.5 Pa pressure in a Panasonic E620 ICP-RIE etching system. Following this etch, FOX 16 e-beam resist is deposited and exposed in areas of the JFET fingers and the FFR gaps to form an oxide layer, protecting the polysilicon implant mask underneath.

The oxide-masked polysilicon etch was then attempted in the same system under a similar chlorine-based recipe as described above. However, even after changing the mask material, the micromasking issue persisted, though to a lesser degree. The problem is apparently more fundamental, and one potential reason is the non-spontaneous nature of the reaction between the adsorbed Cl layer and the polysilicon surface. In addition, the major byproduct in a Cl-based

RIE of silicon is $SiCl_4$, which has a boiling point of 57.4°C [3]. This results in a relatively low vapor pressure, and thus the byproducts are only moderately volatile. The etching mechanism of polysilicon by Cl is therefore dominated by ion bombardment rather than chemical reaction. Thus the process provides very anisotropic etching, which is desirable. However, the combination of a moderately-volatile byproduct and the saturation of the surface with adsorbed Cl due to the limited reaction rate may lead to non-uniform etching and micromasking. The problem also seems to be more pronounced in polysilicon compared to crystalline silicon, due to the increased surface roughness.

To solve this issue, a change to a different etchant species was needed. An obvious candidate is SF_6. The major byproduct formed during polysilicon etching with a fluorinated gas is SiF_4, which has a low boiling point of -87°C [3], and is therefore highly volatile. In addition, a spontaneous reaction occurs at the polysilicon surface, although this leads to isotropic etching, and thus undercutting of the mask. To realize an anisotropic etch, a passivation layer is needed to protect the sidewalls. This is the basis of the Bosch process, which is available in our STS ASE ICP-RIE system using C_4F_8 as the passivating species and SF_6 as the etching species.



1) 4.8 µm polysilicon deposition *2) Oxidation of polysilicon* *3) Windows in top oxide*

4) Alignment mark etch *5) E-beam lithography with FOX-16 resist* *6) Polysilicon etch*

Figure 14: Oxide-only polysilicon implant mask etch process sequence.

The process starts with the deposition of a polymeric passivation layer of C_4F_8 at 600 W RF power for 5 sec. This is then followed by an etching step with SF_6 and O_2 at 500 W RF power and 20 W platen power for 5 sec. The directionality of the radicals etches the polymer and polysilicon on the horizontal surfaces, but the etch remains inhibited on the sidewalls due to the polymer protection. The cycle then repeats as many times as required to perform the desired etch. The pressure during both the deposition and etching steps is maintained at 18 mTorr with

an automatic pressure control position. The etch rate of polysilicon under this recipe is 1.5 μm/min, with a selectivity over an oxide mask greater than 25. The etched polysilicon pillars are found to be highly anisotropic under scanning electron microscopy (SEM), with a 100 nm undercut and scalloped sidewall, typical of the Bosch process. An SEM image of the etched polysilicon after the Bosch process is shown in Figure 15. Despite having undercut and scalloping sidewall, the features are satisfactory for use as an implant mask and subsequent processing. Further optimization to reduce and compensate for the undercut will be conducted in future.

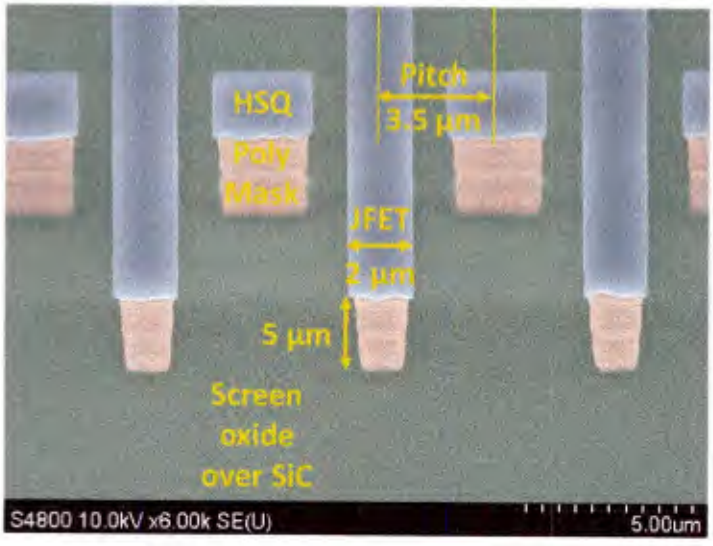


Figure 15: False color SEM image of polysilicon etch in the Bosch process.

A self-aligned process is then used to form the channel region by blocking the high energy n^+ implant that forms the source regions. A sidewall spacer is formed by thermal oxidation of the polysilicon implant mask pillars, creating a gap between the *p*-type base implant and the subsequent n^+ source implant and defining the channel length of the MOSFET. A pyrogenic wet thermal oxidation at 1100° C and atmospheric pressure is employed to create a 0.5 μm lateral expansion of the polysilicon implant mask. During development of the process, a crystalline silicon sample and a patterned polysilicon test sample were loaded together to calibrate the oxidation rate. As seen in Figure 16, the oxidation rate of polysilicon is slightly higher than crystalline silicon, as expected. The low oxidation rate of polysilicon at the initial stages could be due to the presence of polymer residue from the Bosch process used to etch the polysilicon. Figure 17 shows the same polysilicon features before and after the thermal oxidation. An expansion of the polysilicon by 0.5μm can clearly be seen in the figure.

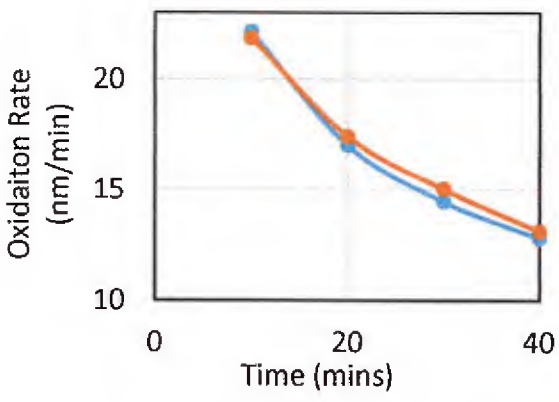


Figure 16: Pyrogenic oxidation of polysilicon at 1100° C.

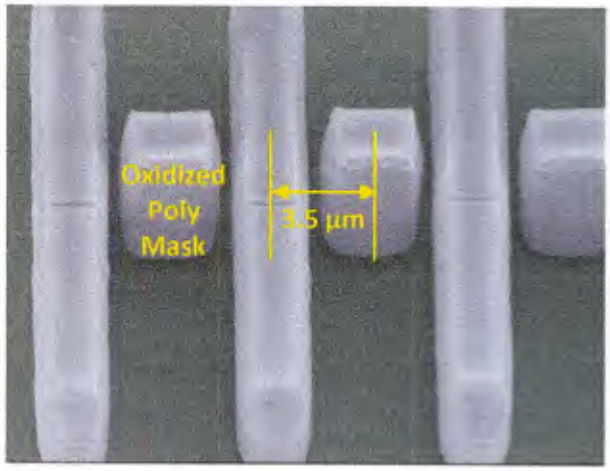
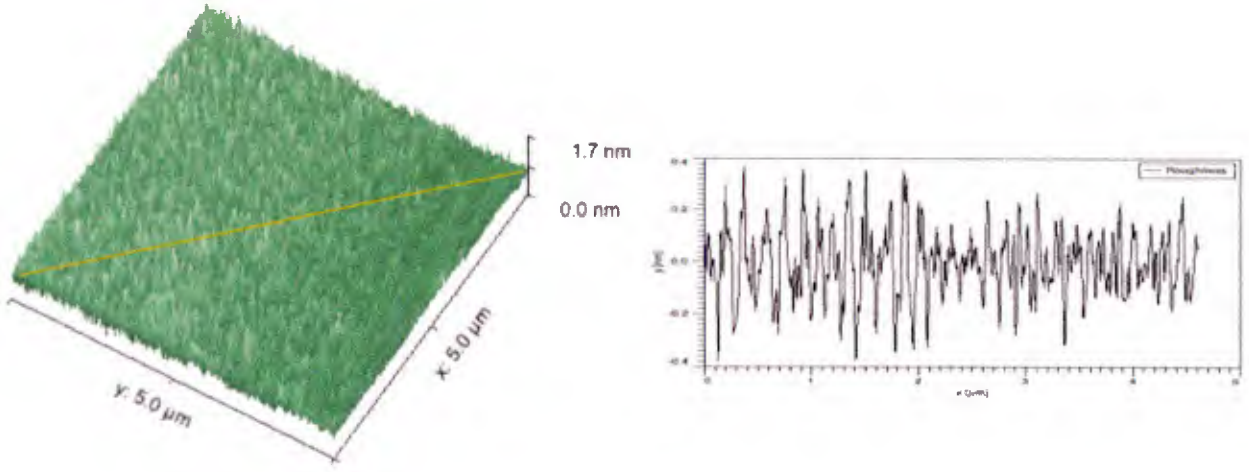


Figure 17: SEM image after polysilicon expansion by oxidation using the self-aligned short-channel process.

The trigate device structure involves trenches that run perpendicular to the source regions. The formation of 2 µm deep trenches in lot A requires deep base and source junctions (2.70 and 2.25 µm respectively), and thus high energy ion implantation in the range of 3-4 MeV. This is one of the major challenges in the trigate device fabrication. All the above implantation including the shallow P+ region to contact the base has been successfully completed. A high temperature anneal (> 1600°C) was then performed to activate the dopants in the implanted regions, and the results from this process are described below.

The SiC surface must be protected from migration of surface atoms and Si sublimation during the high temperature activation anneal. This is typically done by using a carbon capping layer. To do this, the samples were first spin coated with 2.5 µm of positive photoresist (AZ1518). An anneal in argon at 650°C for 20 minutes was then done to pyrolyze the photoresist film and form a carbon cap. The implant activation anneal was done in a hot wall reactor at a temperature of 1700°C in argon at 400 mbar for 10 mins. After this anneal, the carbon cap film was black, mirror like, and 5 times thinner than the original photoresist film. The carbon cap was removed by oxidation and the surface morphology and roughness were measured using atomic force microscopy to determine the effect of the high temperature anneal on the SiC surface. Figure 18 shows the 3D plot and a 2D cross section image of the measurement. The surface roughness is below 1 nm which corresponds to a smooth SiC surface without any damage from the high energy ion implantation.

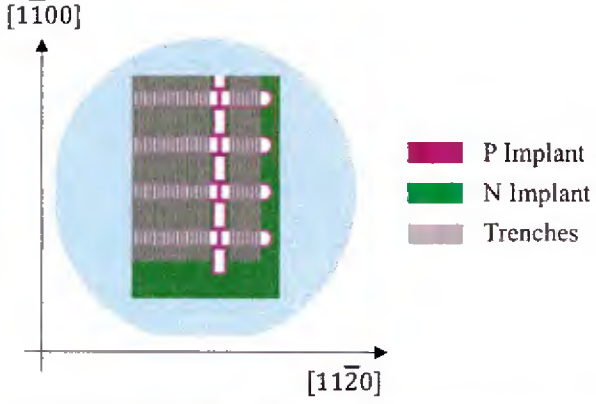


(a) *(b)*

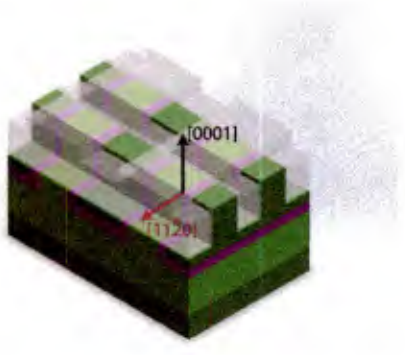
Figure 18: 3D AFM image of across the source and base regions after high energy implantation and activation anneal. The roughness along the cutline (a) is shown in (b). A smooth SiC surface is recovered after the activation anneal process with a surface roughness of RQ of 0.24 nm.

Sub-micron Gate Trenches

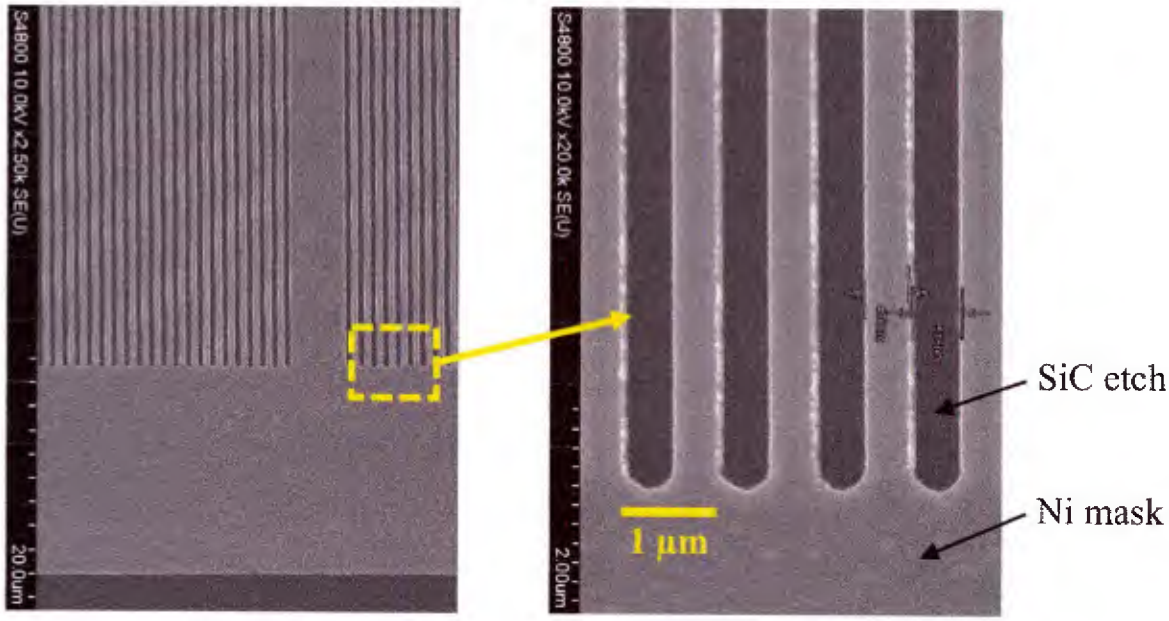
The trigate device fabrication is conducted on a n-type 4° off-cut 4H-SiC with 1×10^{16} cm^{-3} substrate doping concentration. In P base implant lithography process, the JFET fingers are aligned parallel to the primary flat of the wafer along the $[11\bar{2}0]$ direction in crystallographic orientation. This also ensures the self-aligned source fingers run parallel to the major axis with high accuracy. Figure 18(a) shows the source finger with respect to the crystallographic orientation in the wafer. SiC trenches are etched perpendicular to the source fingers which opens the $\{11\bar{2}0\}$ face, or a-face, for current conduction on the trench sidewalls as shown in Figure 18(b). The electron mobility on the a-face in 4H SiC is reported almost double compared to the {0001} or Si-face, which contributes to reduced specific on-resistance.



(a) JFET, source and trench finger orientation with respect to the wafer



(b) 3D isometric view of the current paths along the sidewall $\{11\bar{2}0\}$ plane



(c) Top view SEM image of the trench etch lithography

(d) Close-up top view SEM image of trench etch lithography

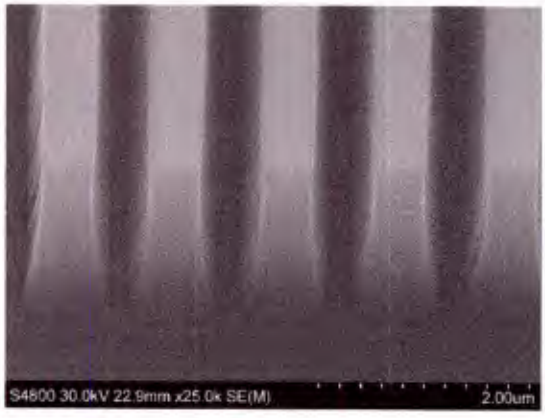
Figure 19: Mask layout and SEM image of SiC trench etch lithography

SiC trenches created by defining a high-resolution Nickel (Ni) hard mask. The width of the fins and trenches are 0.5 µm, making 1 µm pitch in a unit cell. The lithography is done in our JEOL JBX 8100 FS, a new e-beam lithography system at Purdue University. Since our old system, a Vistec VB6 has been decommissioned, a new optimized recipe for the trench lithography was successfully developed in the new e-beam system to lift off a 200 nm thick Ni metal layer. A conventional bilayer of PMMA resist is used, combining highly sensitive 495 PMMA as the bottom layer, and high resolution 950 PMMA as the top layer. After developing the resist in PMMA developer (MIBK:IPA 1:3) for 45 seconds, the samples are loaded into an e-beam evaporation system. A bilayer of 10 nm Ti and 200 nm Ni is evaporated and lifted off in PG remover in a hot bath at 60°C. The patterned metal layer is used as the hard mask during the trench etch. Once again, the e-beam lithography is followed by optical lithography and a lift off process to protect large field areas, and to minimize the required e-beam write time. Figure 19(c) and (d) show SEM images of the trench e-beam lithography in the active area of the device with the Ni hard mask lifted off.

A major challenge in the development of this fabrication process was to identify a successful trench etch recipe with no micro trenching nor any other undesirable secondary effects. A recipe was developed in the Birck Center's Panasonic E620 ICP-RIE etching system two years ago, and was described in previous reports. However, the etching system went down 3 months ago due to a mechanical failure for an indefinite time. Therefore we pursued an alternative option to use the Oxford Plasmalab 100 ICP-RIE etching system at nearby Notre Dame University. After a detailed study and varying different process parameters, we have developed an improved SiC etching recipe in that system. SiC is etched in a 5 mTorr sulphur hexafluoride (SF_6) ambient at 2500 W ICP power and 0.6 W/cm^2 bias power density. This produces a SiC etch rate of approximately 0.5 µm/min. Figure 20(a) and (b) shows the SEM

image of SiC trench etch with 0.5 μm trench and fin widths in Oxford Plasma Lab ICP-RIE and Panasonic E620 ICP-RIE system, respectively.

(a) SEM image of the recently developed SiC trench etch in Notre Dame's Oxford Plasma Lab 100 ICP-RIE



(b) SEM image of previously reported SiC trench etch in Purdue's Panasonic E620 ICP-RIE

Figure 20: SEM image of SiC trenches in different ICP-RIE systems. The fin and trench widths are each 0.5 μm.

Conformal Gate Oxide

The formation of a reliable, high-quality gate oxide wrapped uniformly around the transistor fins is one of the keys to successful fabrication of the tri-gate MOSFETs. Thermal oxidation cannot be used for this purpose due to the different oxidation rates of the top and sidewall of the trench. We have developed a *poly-oxidation* process that involves thermal oxidation of an LPCVD-deposited conformal polysilicon film. A TEOS-based LPCVD SiO_2 deposition and a TDMAS-based ALD SiO_2 deposition are also being investigated as alternatives.

During device operation, a positive voltage is applied on the gate to turn on the transistor, and the electric field in the oxide is expected to be the highest at the top and bottom corners of the trench due to field crowding. In the blocking state, some part of the electric field is expected to terminate in the oxide at the bottom of the trench. Thinning of the oxide near these corners could lead to premature failure of the device. In addition, the resulting channel includes regions on the top, sides, and bottom of the fins, and it is important that these regions have similar threshold voltages. Conformal deposition of the oxide on the trench geometry is therefore crucial. To determine the uniformity of the resulting oxide thickness, we took several cross-sectional SEM images. First, trenches were etched in SiC using an e-beam-defined metal mask and an ICP-RIE process using an SF_6-based chemistry. The trenches were 2 μm deep and 0.5 μm wide, with a pitch of 1 μm. The samples were then cleaned using the standard wet chemical RCA process. Gate oxide was formed using both poly-ox and TEOS processes.

The trenched area was milled on a test sample to create a cross-section using FIB, after filling the trenches with polysilicon. The ion beam energy and accelerating voltage was carefully adjusted to ensure the integrity of the SiC/SiO_2 interface. Figure 21 shows SEM images of the resulting cross-sections taken using a cold field-emission microscope at a rotation angle of 70°. To obtain good contrast during imaging, the samples were subjected to a 30 sec HF dip to

recess the oxide under the gate. As seen in the figure, the coverage of the poly-ox and TEOS oxides are both 100%, and both the top and bottom of the trench seem to be well protected by the oxide. The oxide thickness at the top and bottom of the trench are equal for both poly-ox and TEOS, but the oxide thickness of the sidewall is slightly lower. The ratio of the oxide thickness at the top and sidewall of the trench is 1.30 for the poly-ox process and 1.17 for the TEOS process.

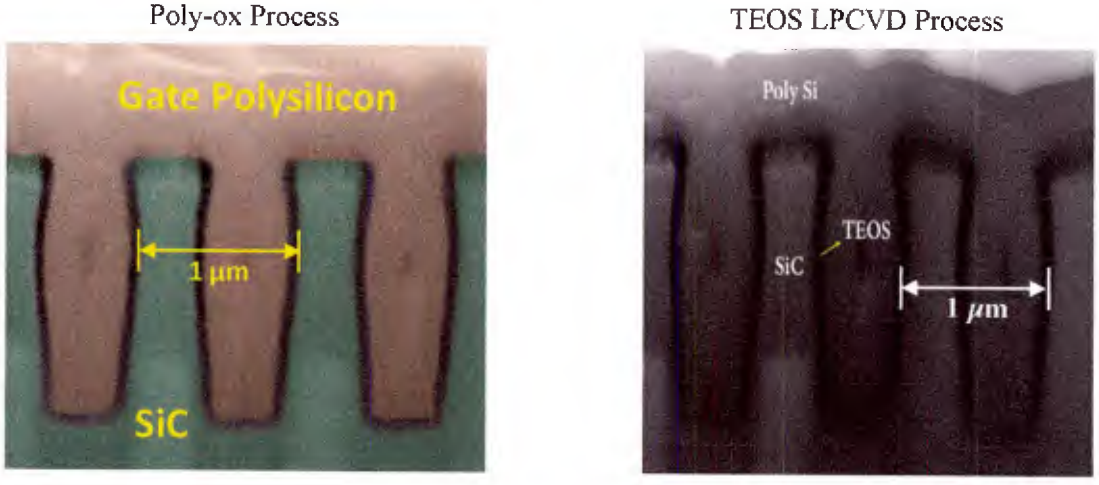


Figure 21: Cross sectional SEM images of the SiC / SiO_2 / polysilicon stack.

Gate Polysilicon Trench Fill, Patterning, and Interlayer Dielectric

After formation of the conformal gate oxide deposition, a 0.5 µm thick polysilicon layer was then conformally deposited on the samples using an LPCVD process, and doped using an N-type (phosphorous) spin-on-dopant (SOD) process, forming the wrap-around gate of the trigate devices. A SIMS analysis on polysilicon test samples with this process yielded a doping of $5x10^{18}$ cm^{-3} at a depth of 2 µm. An additional 0.6 µm thick polysilicon film is then deposited and doped using the same SOD process. Next, the gate fingers were patterned by use of a polysilicon RIE etch in the active areas as part of the self-aligned source contact process. The polysilicon in the source regions are etched down to the N-implanted SiC surface on top of the trigate fin, leaving a plug of polysilicon in the trenches. The gate polysilicon was then thermally oxidized to form an SiO_2 interlayer dielectric (ILD).

Ohmic Contacts and Power Metal

The next step is the contact anneal process to create ohmic contacts in the source and drain regions. First, a 20 seconds dip in BOE was performed to remove the oxide in the source windows that would have formed during ILD formation process. This is followed with a short SF_6/Ar RIE etch to roughen up the SiC surface and then O_2 ashing to remove any hydrocarbon slag that may have formed during the RIE etch. Another 20 second BOE etch was done to ensure no oxide in the source windows before a 200 nm film of nickel was evaporated onto the sample. The ohmic anneal process is done in two steps. The sample is first annealed at 750°C for 3 minutes in argon using a rapid thermal anneal (RTA) process at atmospheric pressure. At this step, the nickel-silicide is formed in the source windows. A piranha etch is then performed to remove the unreacted nickel over the ILD and field oxide regions. Next, the front of the sample

was protected by photoresist while the Ni was evaporated on the back side. The sample is then subjected to an anneal at 1000°C with all other parameters remaining the same as before. The high temperature anneal is done to achieve low specific contact resistance of $< 3 \times 10^{-6}$ Ωcm^{-2} as verified by test samples using the same process. Microscope images of the active area is shown in Figure 22. The next step is the create opening in the ILD to contact the gate and then finally deposit top metal.

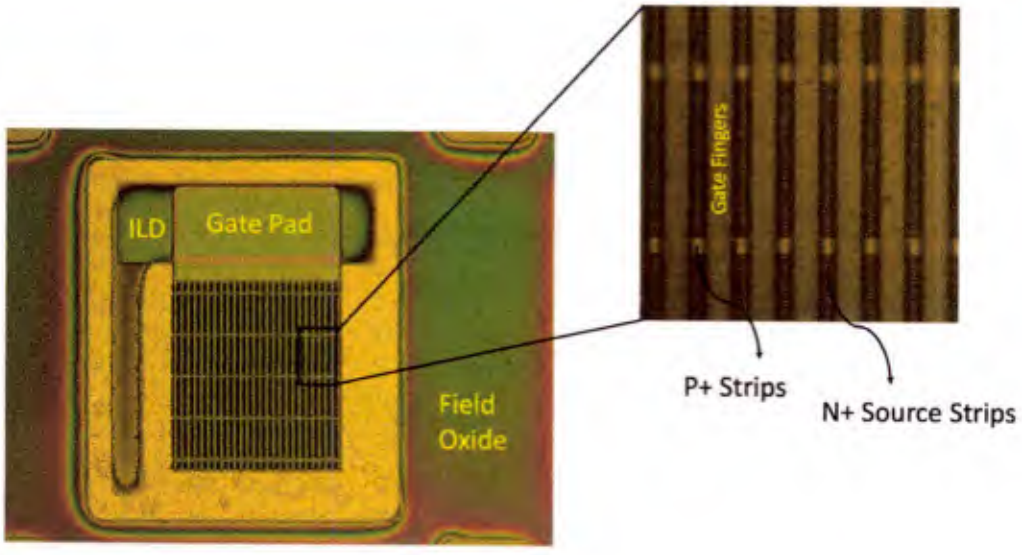


Figure 22: Ohmic contact anneal of Generation 1 (Device 4Q2) trigate MOSFET at 1000°C for 3 minutes in argon ambient.

Fabrication Status

The fabrication effort is being carried out in two waves: generation 1 (Gen 1) and generation 2 (Gen 2). The Gen 1 lot is comprised of four samples, which are fabricated in a staggered manner, providing backup samples in the case of an unrecoverable failure in any single process step. As of this report, the first sample of the Gen 1 lot has been completed, but during electrical testing a gate-drain short was discovered. A failure analysis determined the likely cause to be over-etching during the ILD patterning. Electrical measurements of test MOSCAP structures prior to this etch confirmed the integrity of the gate oxide. The three other Gen 1 samples are ready for field oxide deposition and patterning, followed by the gate stack process, and experiments are underway to refine the etching process to eliminate the fault. We expect completion of the next sample within the next eight weeks.

The tri-gate Gen 2 devices are focused on a shallower 1 μm trench, which reduces fabrication complexity but retains most of the benefit of the 2 μm trench. The p-type aluminum base implantation has been completed and the samples were processed to define the self-aligned channel and source implantation mask using nickel electroplating. The samples were then sent back to mi2 GmbH in Germany for nitrogen implantation. The source implantation is designed to have a 1.25 μm junction depth, with high doping near the surface to produce low resistance ohmic contacts. The highest implantation energy of the profile is 1.3 MeV. Once these samples were received from the source implant, the polysilicon mask was stripped, and the samples were

cleaned using the RCA process in preparation for the p+ implant mask. The p+ implant mask process used for Gen 1 consisted of a combination of optical lithography for the testers and e-beam lithography for the in the active area where the critical dimension is 2 µm. However, the complete process can now be accomplished using a single photo-lithography step with the newly installed Heidelberg direct write system in our cleanroom. Dose-test and process optimization runs were carried out and features down to 1 µm were achieved with excellent alignment. This system was then used to define the p+ implant metal mask and samples have been sent out for the final p+ implant. This step will be followed by the implant anneal, gate trench etch, gate stack, and metallization steps. We expect completion of the first Gen 2 devices by the end of 2019.

Task 3.1b: Deeply-scaled UMOSFET (IMOSFET) (Madan Sampath, Dr. Arash Salemi)

SiC power MOSFETs have made great progress since the first commercial devices were introduced in 2011, but they are still far from their theoretical limits of performance. Above ~1200 V the specific on-resistance is limited by the drift region, but below 1200 V the resistance is dominated by the channel and the substrate, with smaller contributions from the source and JFET regions. The source, channel, and JFET resistances are all proportional to unit cell area. Trench MOSFETs have smaller cell area than planar DMOSFETs, and are inherently more scalable. In this paper we describe a highly self-aligned fabrication process to realize deeply-scaled trench MOSFETs with a cell pitch of 0.5 µm per channel. Since the narrow gate trench is shaped like a letter "I", we refer to these devices as "IMOSFETs," illustrated in cross-section in Figure 23.

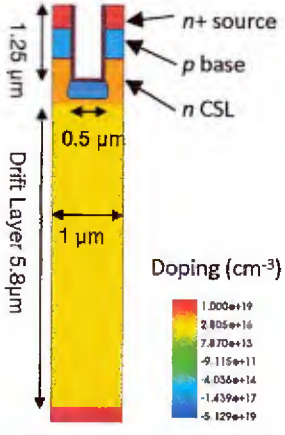


Figure 23: Final IMOSFET device

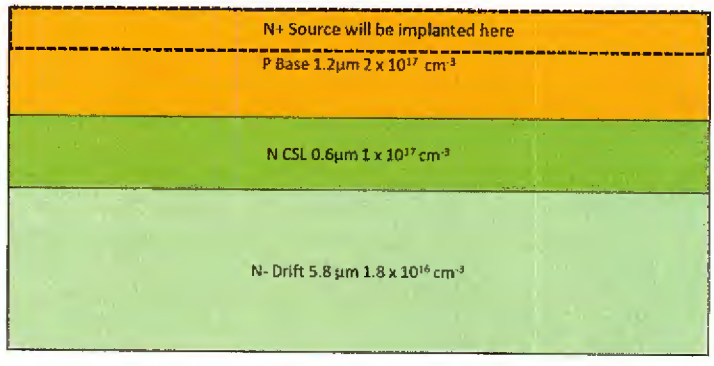


Figure 24: Initial IMOSFET epitaxial wafer structure.

The epilayer structure used in the fabrication of the first IMOSFET prototype devices is shown in Figure 24. The total base thickness is 1.2 µm, which is the sum of the *n*+ source thickness and *p* base thickness. Since the source layer is formed by ion implantation, we can vary the effective channel length (thickness of the remaining *p* base) by adjusting the depth of the source implant profile, without having to purchase additional wafers.

IMOS Process Development

The major steps in the fabrication process of the deeply-scaled IMOSFET is illustrated in Figure 25.

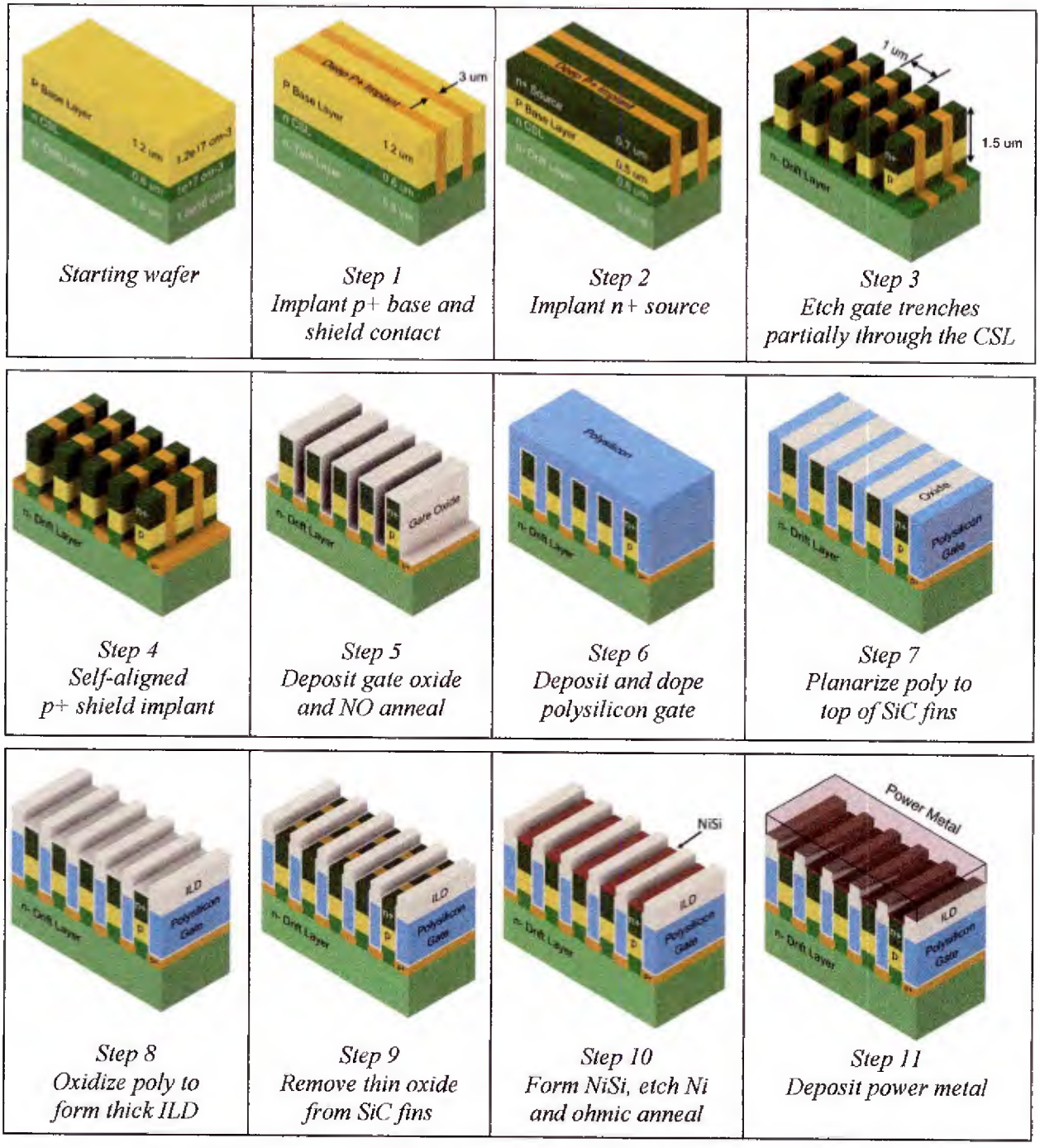


Figure 25: Illustration of the major steps in the deeply-scaled IMOSFET fabrication process

The first step in the fabrication of an IMOSFET is a deep P+ implant, which acts as both a top base contact and as a floating field ring (FFR) edge termination. The profile for this implant is shown in Figure 26. The top section of the profile is heavily doped for a good P+ ohmic contact, while the bottom profile is optimized for the FFR near breakdown. The FFR region will be etched to the active device trench level of 1.5 µm to remove the p-base epitaxial layer which would otherwise short the floating field rings together. The line indicates the gate trench etch depth, below which the dose should be sufficient to prevent punch-through in reverse bias. The red line shows the background N-type epilayer doping below 1.2 µm. Above this depth the epilayer is P-type, as illustrated in Figure 23.

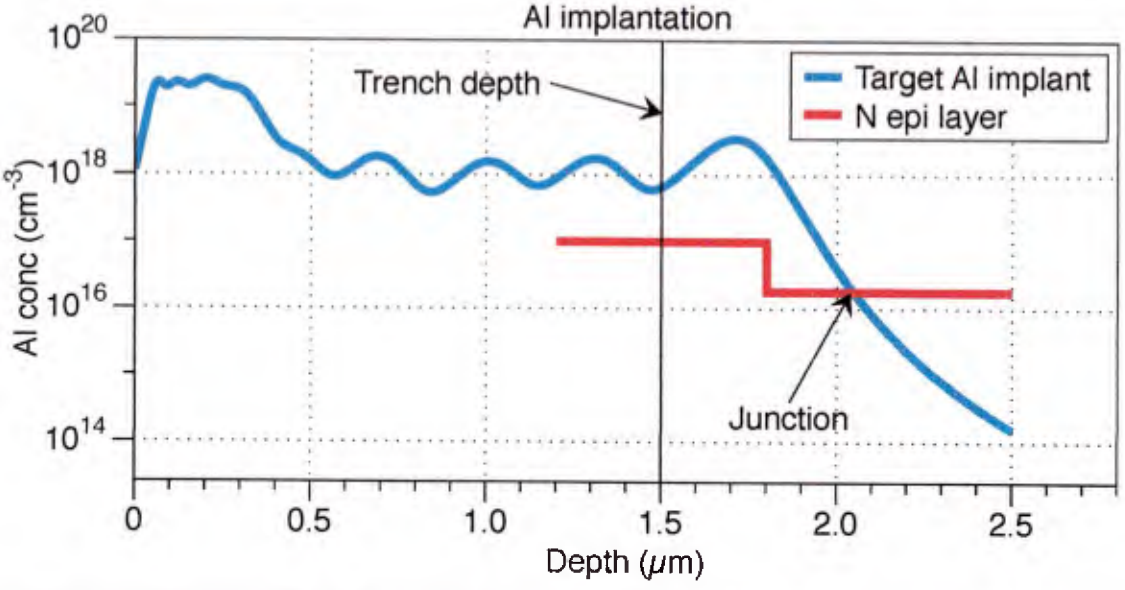
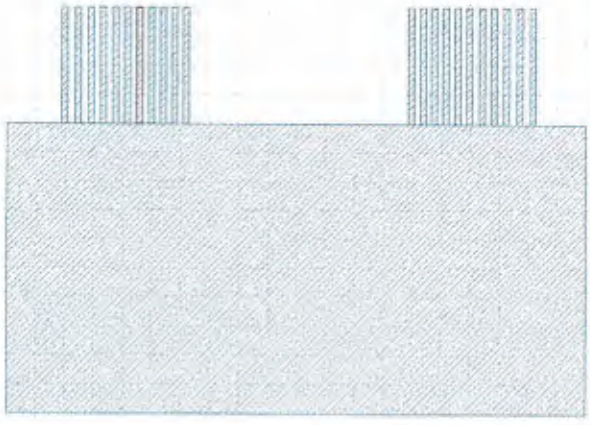


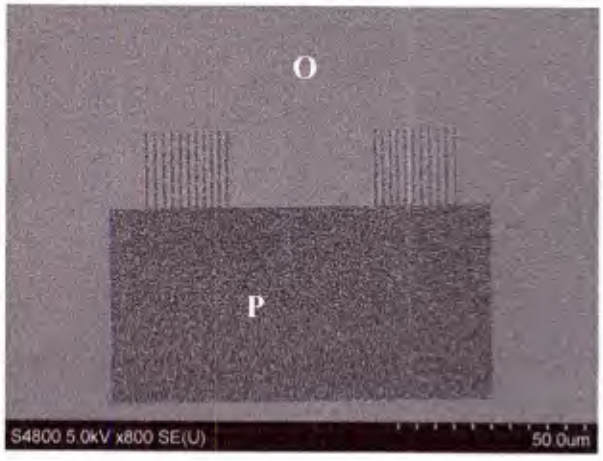
Figure 26: Deep P+ implant profile vs. depth, predicted using range and straggle data from [4]

The implant mask is a thick polysilicon film patterned by e-beam lithography. First a screen oxide was grown on the IMOS wafers, followed by polysilicon deposition and oxidation. The measured polysilicon thickness was 4.3 µm and oxide thickness is 170 nm. Electron beam photoresist was used to pattern the oxide since the patterns in FFR are less than 1µm, and the oxide was then used as a hard mask during the polysilicon etch. The IMOS process leverages the same BOSCH RIE process we developed for the trigate MOSFET deep implant mask.

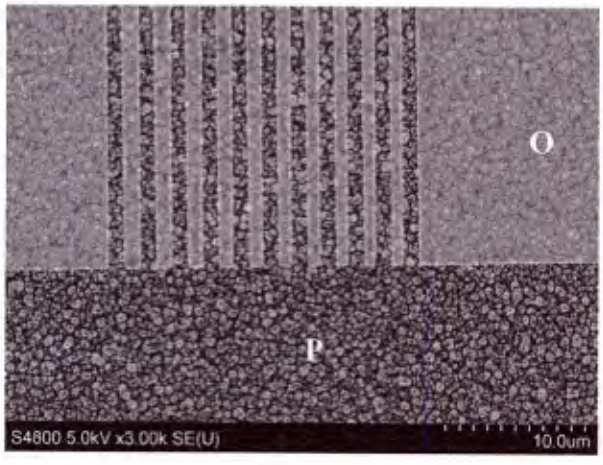
The suggested dose for ZEP resist was 245 µC/cm^2 and we can see that doses from 225 to 275 give good results. Thus, we use 250 µC/cm^2 for our exposure dose. The oxide is etched in our STS ASE ICP-RIE tool using SF_6 and O_2 gases at 600 W RF power and 30 W platen power for 4 minutes. The oxide etch rate was found to be 32.5 nm/min and the e-beam resist etch rate is 120-130 nm/min. Therefore, to etch 170 nm of oxide, at least 680 nm of resist is required. This is achieved using ZEP 520A resist spun at 1000 rpm for 60 seconds, providing a thickness of 800 nm. This process was used to successfully form the oxide test patterns shown in Figure 27.



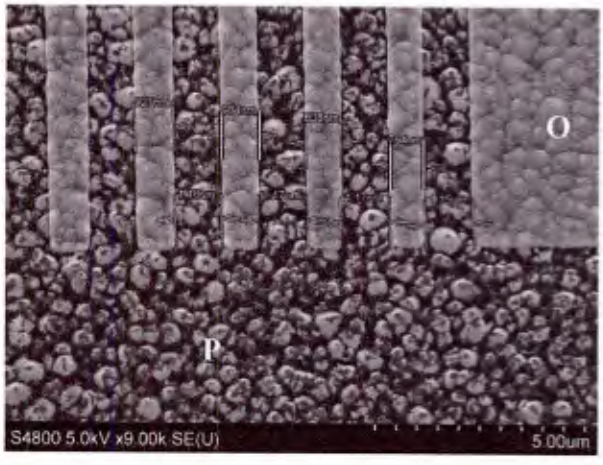
(a) GDS pattern to be written in E-Beam



(b) Top view of etched oxide



(c) Sample tilted at 31°



(d) Tilted view with dimensions

Figure 27: Test patterns formed by ICP-RIE in an SiO_2 hard-mask on a thick polysilicon implant mask.

To etch the polysilicon implant mask, we use the Bosch RIE process, which uses alternating passivation and etching steps to minimize lateral etching and achieve high aspect ratio structures. It begins with the deposition of a polymeric passivation layer of C_4F_8 at 600 W RF power for 5 sec. This is followed by an etching step with SF_6 and O_2 at 500 W RF power and 20 W platen power for 5 sec. The directionality of the radicals quickly etches the polymer subsequently the underlying polysilicon on the horizontal surfaces, but the etch reaction remains inhibited on the sidewalls due to the polymer protection. The cycle then repeats as many times as required to perform the desired etch. The pressure during both the deposition and etching steps is maintained at 18 mTorr with an automatic pressure control system. The etch rate of polysilicon under this recipe is 610 nm/min, with a selectivity over an oxide mask greater than 25 : 1. An SEM image of the etched polysilicon after the Bosch process is shown in Figure 28 - Figure 31.

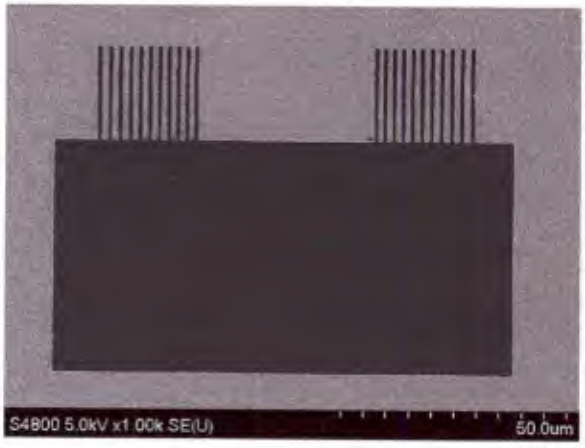


Figure 28: Top view of Polysilicon etch

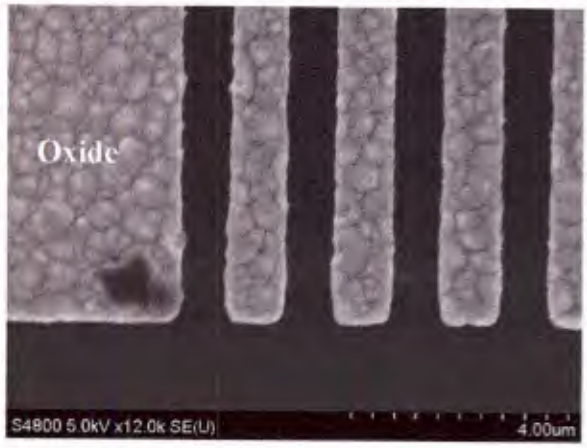


Figure 29: Zoomed top view

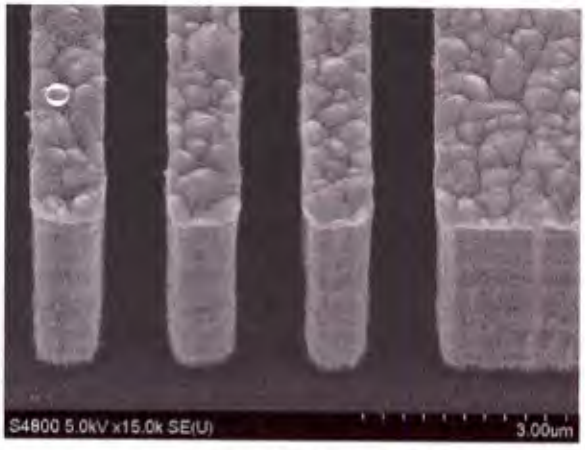


Figure 30: SEM tilted at 31°

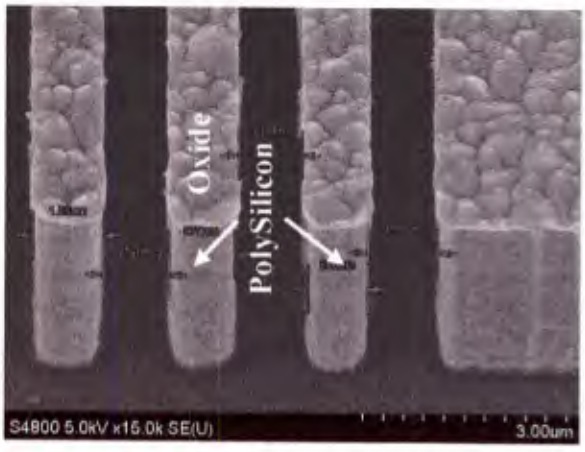


Figure 31: SEM tilted at 31°

Table 2: Channel length variations included in initial IMOSFET fabrication run

Channel	Channel length	Highest Energy	Range (SRIM)	Straggle (SRIM)
Short	0.53 μm	380 keV	335 nm	103 nm
Long	0.70 μm	246 keV	239 nm	87 nm

Table shows the two variations which we will be targeting for this IMOS fabrication run. TRIM simulations were performed to confirm the required Ni implant mask thickness. As shown in Figure 32, we can see that 600 nm of Ni mask is required to block the source implant, and this needs to be done by e-beam lithography. The CSAR 62 e-beam resist has a thickness of 800 nm when spun at 1000 rpm speed. We have done several test runs to confirm that this thick metal mask can be lifted off with the e-beam resist.

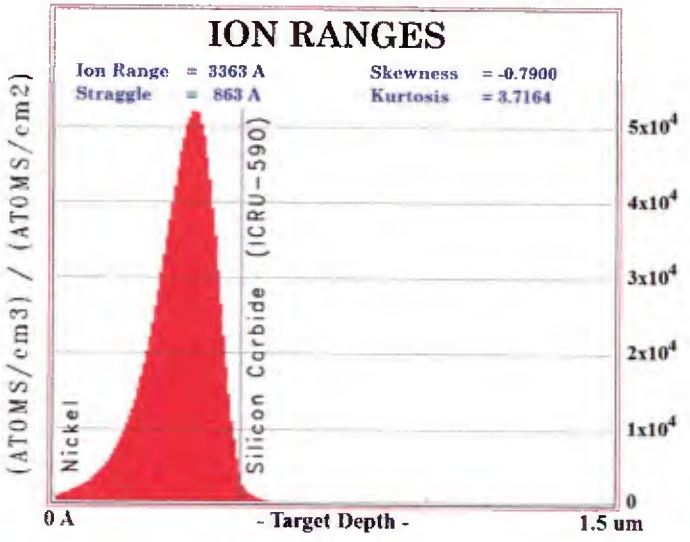


Figure 32: TRIM simulation for source implant of short channel

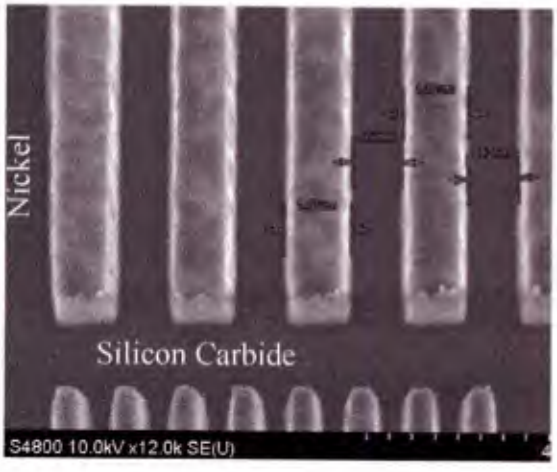


Figure 33: 30 ° tilted SEM image

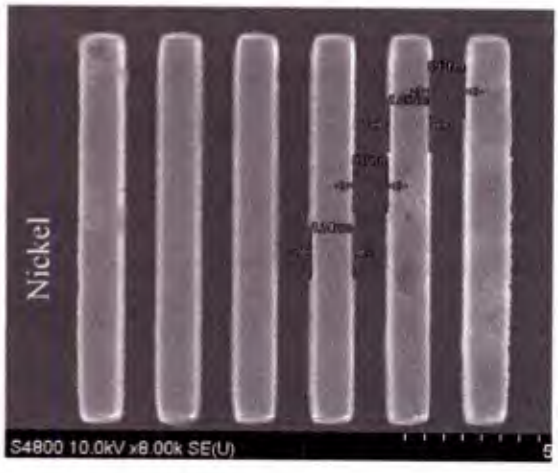


Figure 34: SEM image of light field pattern

First, a dose and alignment test was performed, and the optimal dose was found to be 330 μC/cm^2 at 100 nA current for Ni lift off with the CSAR resist. The above figures show the results of a 600 nm Ni liftoff process with 1 μm features, which are the smallest features on this mask.

All ion implantations except the p+ trench shield implant are complete, and the next step in fabricating the first prototype IMOSFETs is the gate trench etch. This etch is performed in two steps. The field area is etched first, followed by the active gate area. This is required because the etch rate in high-aspect-ratio areas, such as the gate trenches, is lower than in the field area. The trench pattern is done by e-beam lithography, as shown in Figure 35. An optical photoresist pattern is then used to cover the active device area, limiting the first 1.5 μm etch to the field area only.

Figure 35: E-beam Ni mask for Gate trench

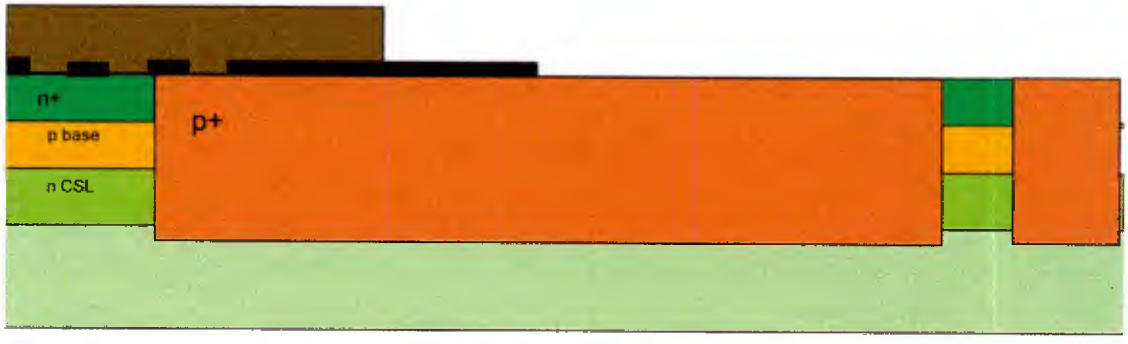


Figure 36: Optical mask to protect active area etch

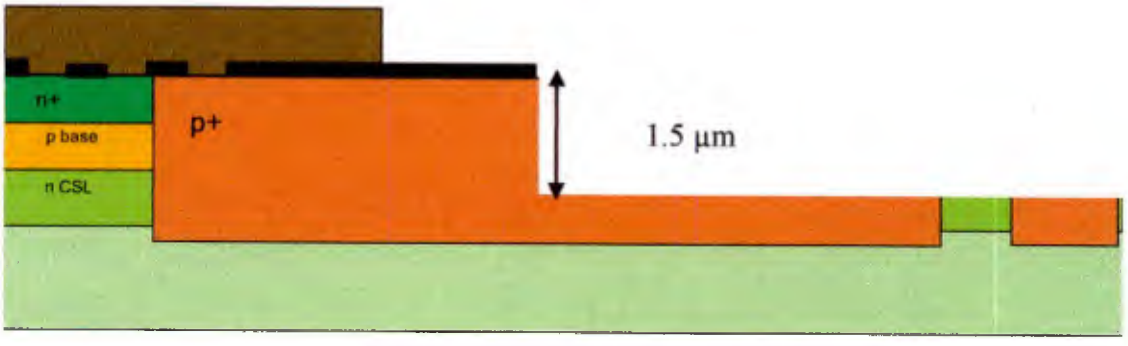


Figure 37: Etch field area

The nominal trench and mesa widths are both 0.5 µm, but since there are uncertainties in the processes, we have added several variations, including trench / mesa widths of 0.4 µm / 0.4 µm, 0.6 µm / 0.4 µm, 0.4 µm / 0.6 µm and 0.6 µm / 0.6 µm. The completed nickel masks created by e-beam lithography are shown in Figure 38 – Figure 41.

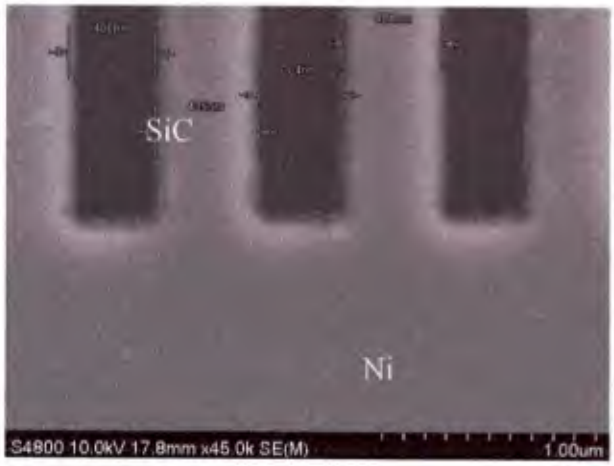


Figure 38: Mesa-Trench 0.4 x 0.4 μm

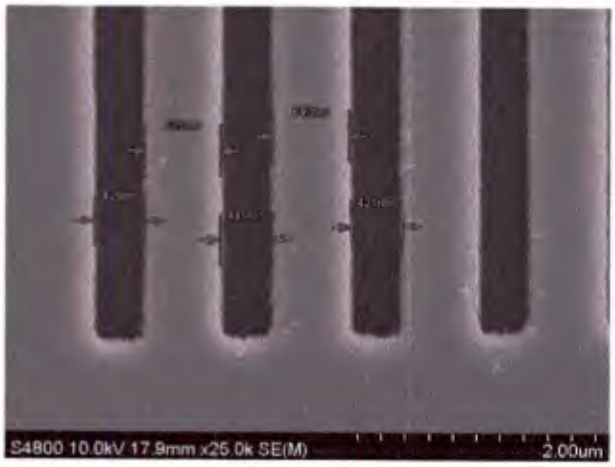


Figure 39: Mesa-Trench 0.6 x 0.4 μm

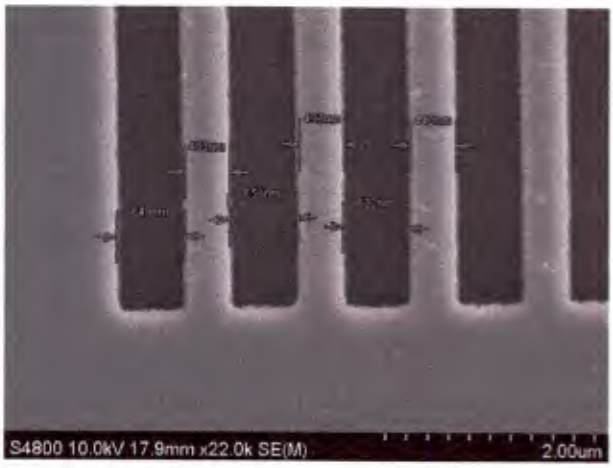


Figure 40: Mesa-Trench 0.4 x 0.6 μm

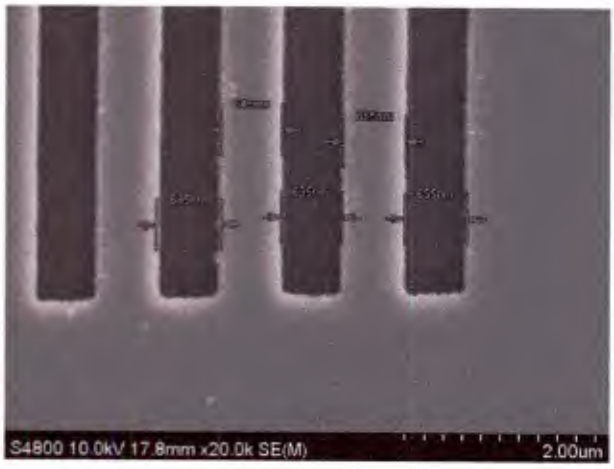


Figure 41: Mesa-Trench 0.6 x 0.6 μm

The etch is done at Purdue in an STS AOE ICP-RIE tool. Our optimized recipe uses 3 kW ICP power, 250 W bias power, an SF_6 flow rate of 20 sccm, and pressure of 10 mTorr. The etch rates and selectivity are shown below:

SiC Etch rate = 809.6 nm
Ni Etch rate = 20.8 nm
Selectivity (SiC/Ni) = 38.9

The SEM images from the etch are shown below:

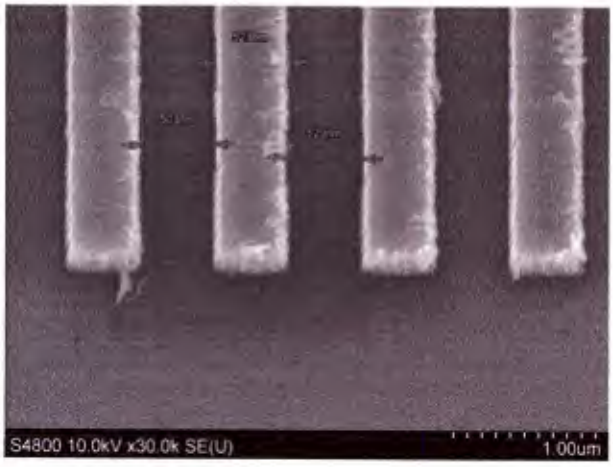


Figure 42: SEM image of Ni mask before etching

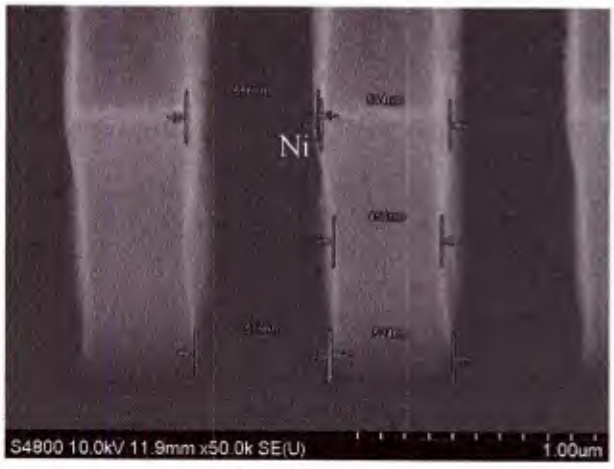


Figure 43: Zoomed image of etched sample

We next implant the p+ trench field shield, self-aligned to the trench. The gate oxide is then deposited and NO annealed, and polysilicon is deposited and doped to form gate electrodes. The polysilicon is planarized by a blanket dry etch, and a FIB cross-section of the device completed up to this step is shown in Figure 44.

The gate polysilicon is then thermally oxidized to form an intermediate-layer dielectric. The thin oxide formed on the SiC fins during this step is removed by a short BHF dip. Self-aligned source contacts are formed by depositing Ni and annealing at 700° C to form NiSi on the exposed SiC. The remaining unannealed Ni is removed by a wet etch, Ni is deposited on the back side, and the ohmic contact anneal is performed. The active area is then covered by thick power metal, completing the fabrication. The key to scaling the IMOSFET to sub-micron dimensions is that ***no alignments are required within the unit cell.***

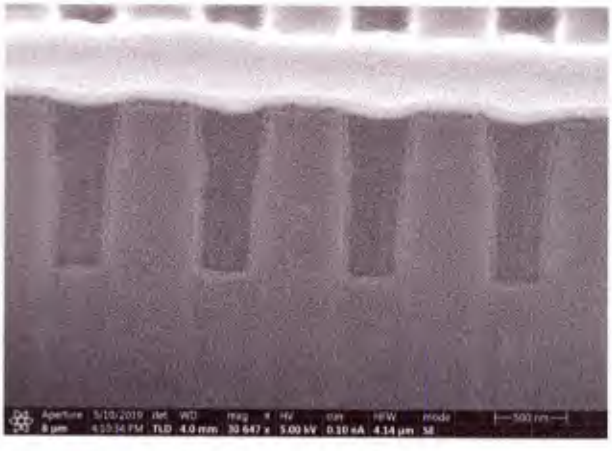


Figure 44: FIB cross-section of poly filled trenches

The spacing between p+ contact stripes in the IMOSFET is adjusted to achieve the desired trade-off between low on-resistance (wide separation) and increased avalanche ruggedness (narrow separation).

Task 3.2: Waffle Substrate (Dr. Noah Opondo)

Note: this section is excerpted from a manuscript currently in preparation for publication

The most important performance metrics for power devices are the specific on-resistance, the blocking voltage V_B, and the high-frequency figure-of-merit $V_B^2/R_{ON,SP}$. $R_{ON,SP}$ has contributions from the MOS channel, the drift layer, and the substrate. For power devices with blocking voltages between 400 - 900 V, where most applications lie, the substrate is a major contributor to the total on-resistance. One way to reduce the substrate resistance is to mechanically thin the substrate, and this is currently employed in the most advanced production devices [5]. However, back-grinding can introduce surface damage such as scratches, dislocations, and cracks that reduce the mechanical strength of the wafer. In addition, wafer warp and bow may be exacerbated on thinned wafers during subsequent processing. Back-side polishing restores some of the intrinsic strength by reducing the concentration of surface defects [6], but the reduced mechanical strength can pose challenges during fabrication. Thinning is therefore carried out after most front-side processing is done, to minimize the chance of breakage.

To further reduce the substrate resistance, we form deep depressions in a repeating or "waffle" pattern on the backside of the substrate. The waffle structure provides mechanical support while reducing the effective electrical thickness of the substrate. Let us assume a substrate of thickness t_1 and resistivity ρ, and consider a square area having side length $d_1 \times d_1$. We perform an anisotropic etch in a square subsection of the area with side length $d_2 < d_1$, leaving thickness $t_2 << t_1$ remaining as shown in the inset to Figure 45. We can obtain a conservative upper bound on the specific resistance of the $d_1 \times d_1$ region by neglecting conduction in the un-etched fins and assuming conduction only occurs through the thinned depressions. In this case we can write

$$R_{SUB,SP} \leq \rho t_2 (\frac{d_1}{d_2})^2$$

This relationship is plotted in Figure 45, assuming a substrate resistivity of 25 mΩ cm. The horizontal dashed line is the specific resistance of a substrate uniformly thinned to 110 μm. We note that if ohmic contacts are also established on the vertical sidewalls and top surfaces of the fins, the actual resistance will be somewhat lower than that shown in Figure 45.

For a d_2/d_1 ratio of 0.8 with the substrate etched to a final thickness t_2 of 20 μm, the resistance reduction factor with respect to a thinned wafer of 110 μm is 3.5×. For a practical process, waffle substrate fabrication must exhibit good uniformity, repeatability and control. The results depend on the choice of masking material, deposition techniques, etch chemistry, and the lack of micro-masking and micro-trenching [7].

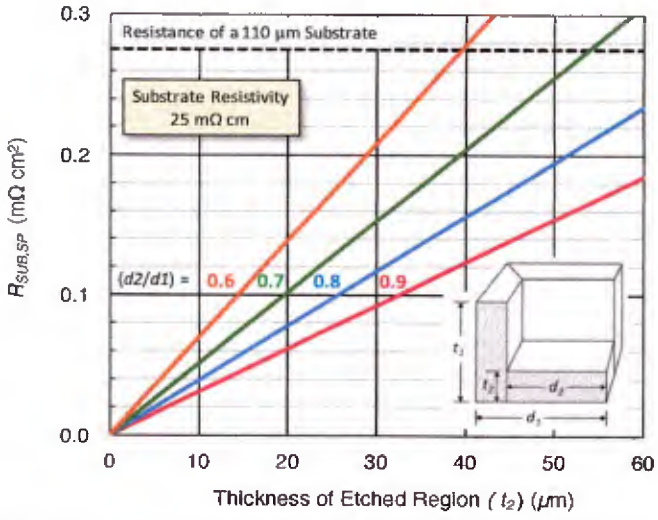


Figure 45: Specific resistance of a waffle substrate assuming no conduction in the un-etched fins. The specific resistance of an un-etched substrate of thickness 110 µm is shown dashed.

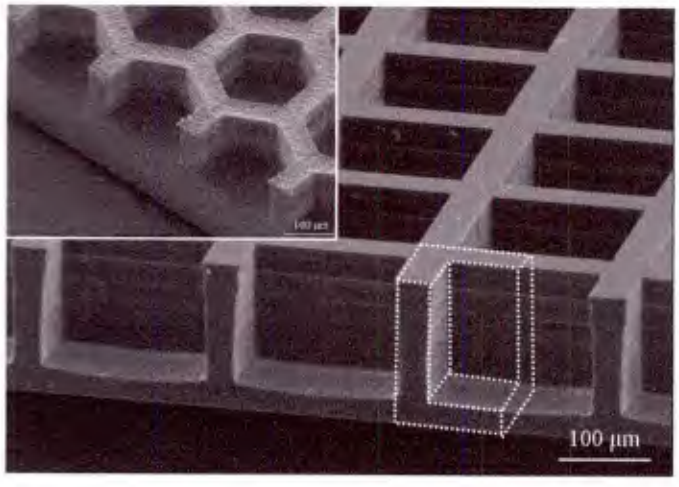


Figure 46: SEM image of trenches forming the waffle pattern from the top view. No micro-masking is observed. The nickel etch mask is still in place in the inset. The dotted lines indicate a single cell from which the resistance reduction factor is derived in Figure 45.

To gain insight into the relationship between the vertical and horizontal dimensions of the waffle pattern and the resulting stiffness and strength of the final wafer, finite-element analysis (FEA) are performed using the ANSYS^{TM} structural simulation tool. The results are used to obtain optimal values of thickness and waffle pattern dimensions to reduce the electrical resistance while retaining sufficient mechanical strength and stiffness. The simulation results are calibrated by mechanical tests using the ball-on-ring (BOR) test technique. The BOR test eliminates contributions from the periphery of the wafer, since the applied force has a radial symmetry [8].

In the next sections, we describe the process to form a waffle substrate using established processing capabilities. The waffle-etch process uses standard contact photolithography, metal mask deposition, and inductively coupled plasma (ICP) etching. SEM image of the waffle

pattern with square, and hexagonal pattern in the inset is shown in Figure 46. We then obtain mechanical stiffness data on thinned wafers using BOR test measurements. This forms the basis for the overall substrate reduction that will be reported in the second part of the work.

ANSYS Simulations

Mechanical simulations are performed on cantilever samples using ANSYS™ FEA to investigate the effect of uniform thinning and waffle pattern etching on stiffness. Figure 47 plots stiffness as a function of wafer thickness following uniform thinning for both thinned and thinned-plus-waffle-patterned samples. The waffle pattern dimensions are illustrated in the inset of Figure 47. The waffle patterns have depressions that penetrate to within 20 μm of the total thickness. Using structural mechanics, the maximum principal stress, tensile stress distribution, deformation, and displacement of the structure are obtained upon application of a force. Wafer thicknesses of 110, 150, 200, and 250 μm are simulated using cantilever geometry, both with and without waffle patterns. Simulations reveal that the stiffness of a substrate uniformly thinned to 110 μm, reported by Infineon to be their production process [9], is comparable to the stiffness of a wafer thinned to 180 - 200 μm and waffle-etched so that only 20 μm remains in the depressions.

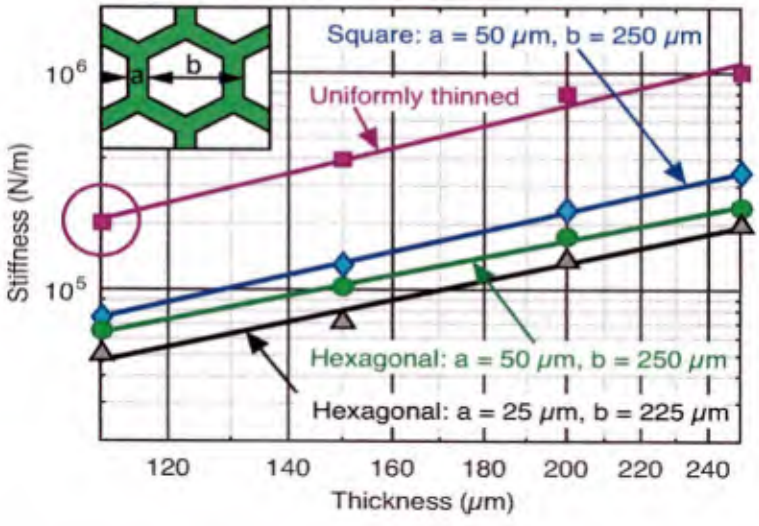


Figure 47: ANSYS simulation results of patterned and unpatterned 4H-SiC substrates of different dimensions. The circle represents the uniformly-thinned 110 μm substrate reported by Infineon as their production process. Waffle substrates on a wafer thinned to 200 μm would exhibit comparable stiffness.

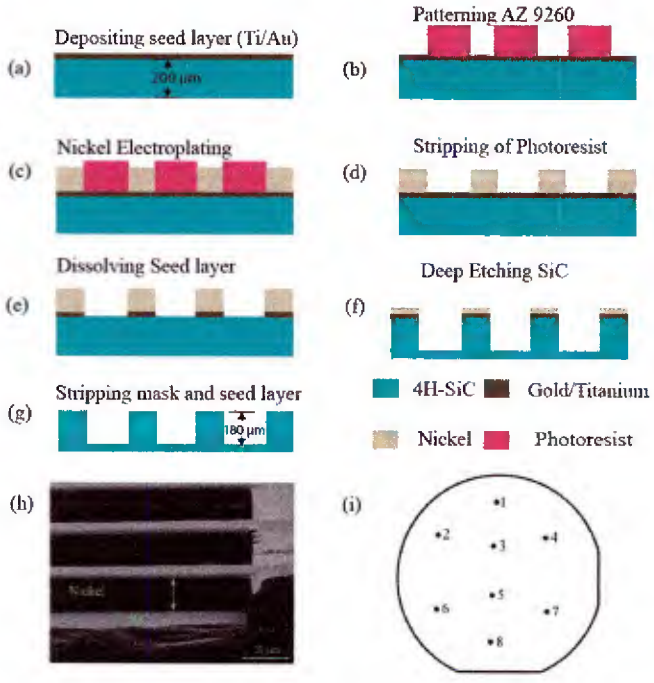


Figure 48: a) Sample is solvent cleaned followed by seed layer deposition of Ti/Au (15/40 nm) b) Photolithography to pattern the seed layer c) Electroplating of nickel to fill mold d) Photoresist dissolved in PRS 2000 e) Seed layer stripped in gold etchant f) ICP etching of SiC, g) Stripping of the remaining mask and the seed layer, h) SEM image showing the nickel mask and SiC before RIE, and (i) Approximate location of measurement points on the backside (carbon face) of the wafer.

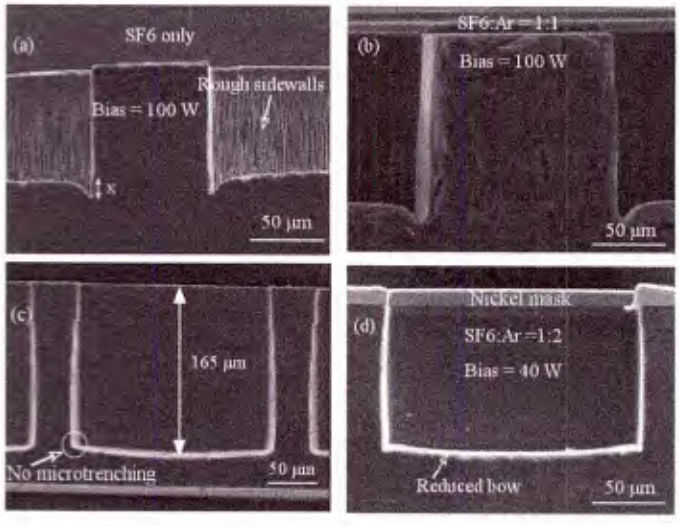


Figure 49: a) Cross section of a sample etched in SF_6. Micro-trenching of 15% and rough sidewalls are observed. The percentage of micro-trenching is defined as the ratio of the over-etch at the base (labeled X) to the total etch depth × 100. b) Cross-section of a sample etched in SF_6:Ar 1:1 at 100 W RF power, with micro-trenching reduced to 8%. c) A sample etched in SF_6:Ar 1:2 at 100 W RF power, exhibiting no micro-trenching and smooth sidewalls, but with a slight bow in the bottom. d) Reducing the RF power to 40 W reduces the bowing.

Fabrication Procedure

We use 100 mm diameter n-type 4H-SiC wafers with a resistivity 14-25 mΩ-cm and nominal thickness of 350 μm purchased from Dow Corning, with the surface tilted 4° towards <1 1 $\bar{2}$ 0>. The wafers are first thinned by NOVASiC in a two step process using High Rigid Grinder (HRG 300) from ACCRETECH. First the wafers are rough-ground from nominal thickness to 20 μm above the final thickness at a rate of 1 μm/s, then fine-ground to the desired final thickness of 150, 200, and 250 μm at a grinding rate of 0.3 μm/s. Wafer thickness is measured at various points on each wafer, and exhibits a standard-deviation-to-mean-ratio of 1-2%.

The 4H-SiC wafers are then RCA and solvent cleaned, followed by deposition of a 15 nm/40 nm Ti/Au seed layer by electron beam evaporation at a base pressure of 10^{-6} Torr. A double-layer spin-and-bake process is used to form an thick film of AZ9260 photoresist, which is then patterned by contact photolithography. After developing, the wafers are post-baked at 90 °C for 30 min and etched in Ar plasma for 1 min at 100 W RF power and 1 Torr pressure. A nickel etch mask is then formed by electroplating in a nickel sulfamate bath at 40 °C and a current density of 10 mA/cm^2. The bath is stirred continuously throughout the process, and is maintained at a pH of 4.8. The nickel deposition rate varies between due to non-uniformities in the electroplating process but a minimum of 10 μm of Ni is deposited in all cases.

After electroplating, the wafers are rinsed in DI water and the photoresist is removed by soaking in Baker PRS 2000, at 60 °C for 20 min, followed by rinsing in isopropyl alcohol and drying with N_2. The seed layer is then stripped in a nickel compatible Au etchant from Sigma Aldrich. Waffle patterns are etched in either a Surface Technology Systems (STS) AOE ICP-RIE or a Panasonic E620 ICP-RIE system. During the etch in the STS AOE, the 100 mm diameter SiC wafers are attached to a carrier wafer using Santovac 5 to provide good thermal contact, and clamped to a chuck with an eight-finger ceramic holder bearing on the wafer at the edge. Samples in the Panasonic E620 are secured using an electrostatic chuck. The wafers are cooled during etching using He back-side flow. Figure 48 shows the schematic flow of the process and a Hitachi S4800 SEM image of the nickel etch mask after the electroplating process.

The waffle substrate process requires deep trenches etched in 4H-SiC without micro-trenching or micro-masking, with smooth sidewalls and good uniformity and repeatability. Several papers have reported etching SiC in SF_6 and O_2 [10, 11, 12], SF_6 and Ar [7, 13,], SF_6 alone [14], and a combination of Ar, O_2, and SF_6 chemistry [15, 16]. Addition of O_2 to the etch chemistry enhances ion reflection and sidewall charging that exacerbates micro-trenching. This work, therefore, investigates 4H-SiC etching in SF_6 and Ar only. Etch recipes involving SF_6 and Ar gases at different ratios are investigated. The process pressure, RF source power and platen power are all kept constant at 15 mTorr, and 100 W respectively. Etching is carried out in two-hour steps, with the etch depth measured using a stylus type AlphaStep surface profiler and confirmed using a Bruker GT-K1 optical profilometer. After etching, the wafers are diced using a Disco DAD dicing saw and imaged by SEM to evaluate the etch profile and to check for micro-trenching. With SF_6 as the only etch gas, the etch rate is 80 μm/hr with micro-trenching of 15% of the etch depth, and rough sidewalls are observed as shown in Figure 49a). Using a (1:1) SF_6:Ar mixture, the etch rate is 49 μm/hr with 8% micro-trenching and the selectivity to nickel mask is 33:1. With a (1:2) SF_6:Ar mixture, the etch rate is reduced to 30 μm/hr with a selectivity

of 25:1. Micro-trenching is completely eliminated with this recipe, but a slight bow is observed in the trench bottom as shown in Figure 49c). A higher proportion of Ar results in more physical sputtering than reactive ion etching. Low pressure insures heavy Ar ions are attracted to the SiC surface with high directionality, so there are few sidewall reflections resulting in the elimination of micro-trenching. By reducing the platen power to 40 W, the bow is reduced significantly and the selectivity increases to 30:1 as shown in Figure 49d). Reducing the platen power reduces the energy of the incident etching species improving the uniformity of the etch at the bottom of the trench and the etch selectivity of SiC to the Ni mask. The etch rate reduction can be attributed to the reduced concentration of SF_6 providing fewer fluorine radicals in the ion-assisted etching. The introduction of Ar into the gas mixture results in smoother sidewalls. This may be due to the sputtering and removal of etch resistant by-products from the sidewalls, and the formation of a passivation layer (C_xF_y) that coats the surface, preventing additional etching that might roughen the sidewalls (c.f. Figure 49 and Figure 46). This passivation layer would also promote the anisotropic etching of 4H-SiC.

Micro-masking is avoided by having a clean, particle-free wafer surface at the beginning of the etch process, and by insuring that the pumping rate of the etch byproducts from the chamber is faster than the rate at which they are re-deposited on the wafer during etching. Nickel masks are known to be susceptible to micro-masking, especially at high power and pressure where etch byproducts may be redeposited on the wafer surface. This can be avoided by using low pressure (a benefit of ICP) and increasing the pumping rate of byproducts from the chamber. We chose Ni as an etch mask because of the ease and convenience of electroplating more than 10 μm of mask material and its compatibility with SiC etch chemistry. The pumping rate of the etch by-products was 1000 l/s at a pressure of 15 mTorr. No micro-masking is observed on the wafers under these conditions.

The etch is evaluated by depth measurements at eight points on the wafer, as shown in Figure 48, after every two hours of etching until the desired depth is obtained. Intermediate etch-depth checks are used to adjust the process if the etch rate drifts during an etch. For a target etch depth of 180 μm, the average etch depth across the Panasonic etched samples are 177.8 μm and with a range of $\pm$ 3.0 μm and , while for the STS AOE sample, the average etch is 172 μm with a max - min range of $\pm$ 5.6 μm. Two runs are done in the Panasonic system while a single run is done in the STS AOE. These results indicate good uniformity across all samples and are within the expectation of one standard deviation of our target of 180 μm. The etch depth at eight different points across the wafer for two different etching systems are shown in Figure 48 showing that run-to-run variations in the same system are small and the recipe requires little modification when moving from one system to another.

Table 3: Etch depth (μm) variation for points 1-8 in Figure 48(i) using Panasonic and STS AOE. The table shows repeatable and stable results for 2 different etch systems.

	Panasonic	Panasonic	STS AOE
	Run 1	Run 2	Run 3
Position	Etch depth	Etch depth	Etch depth
1	178.1	176.7	170.6
2	179.1	176.7	169.3
3	178.6	178.1	173.5
4	176.8	179.6	168.3
5	180.8	179.3	179.5
6	176.1	177.6	171.3
7	174.8	180	173.7
8	178.4	181.5	171.4
Average (μm)	177.8	178.5	172.2
Target Thickness (μm)	180	180	180
Max (μm)	180.8	181.5	179.5
Min (μm)	174.8	176.7	168.3
Difference (μm)	±3.0	±2.4	±5.6

Mechanical Testing

The strength of SiC wafers is strongly influenced by the flaws on the surface introduced by sawing and polishing during wafer production. Different methods have been used to determine the strength of brittle materials. These include the 3-point bending test (3PBT) and 4-Point Bending Test (4PBT) [17], the Ball on Ring (BOR) test [18], and the Ring-on-Ring (ROR) test [19]. The 3PBT and 4PBT can be influenced by edge defects due to the uniaxial nature of the applied force. Biaxial strength tests such as BOR and ROR minimize stress at the periphery of the sample, provided the samples are much larger than the ball and ring fixtures. If edge effects are mitigated, surface preparation and surface defects become key factors in determining the strength of the wafers. In the next paragraphs we report the results of mechanical tests on 4H-SiC samples using ball on ring test.

The mechanical tests on 4H-SiC samples were done using a BOR fixture mounted on the Material Testing System model 810 mechanical characterization system. The 1 mm diameter ball is made of tungsten carbide, and the rings made of brass of inner diameter 2.25 mm and outer diameter 3.25 mm. Tungsten carbide is chosen because of its high stiffness. The ring is placed on a lower cylindrical plate fixed on the 810 MTS system, while the tungsten carbide ball is placed on an upper cylindrical piece machined with a hemispherical depression of radius 0.5 mm to hold the ball in position during the experiment. The ball is affixed with Vaseline to prevent it from slipping out of the depression. The two cylindrical pieces are machined from A2 steel heat treated to a hardness of 62 RC on the Rockwell Scale. The MTS system is aligned to make the upper and lower fixtures parallel and flat. Before each experiment, the test fixture including the ball and ring are cleaned of any debris that could cause premature breakage of the sample. Samples for the experiment are diced from a 100 mm, 4H-SiC wafer with dimensions of 10 mm

by 10 mm with measured thicknesses of 144 μm, 188 μm, 240 μm and 350 μm. Before dicing, the samples are coated with photoresist and mounted on tape to minimize the chances of debris from the dicing saw being deposited on the wafers. No difference in stiffness is observed by placing the sample with ball either on the Si-face or the C-face. Calibration of the tool is performed by the manufacturer, Material Testing System Corporation, prior to the experiment. A load cell of maximum force 100 kN (MTS Model 661.20) is used to acquire the force history. The displacement history δ is recorded using a built-in linearly-variable displacement transducer (LVDT) with a maximum range of 381 mm. The applied force is increased until the sample fails, with a nominal strain rate of 0.01/s.

The raw data is post-processed by fitting the displacement δ as a function of the force F to the following second order equation to determine the compliance,

$$\Delta\delta = \alpha F^2 + \beta F + c$$

where α, β, and c are constants to be determined. These values are identified for each individual fixture component and used to subtract out the compliance as a result of the displacement of the component parts, leaving only the displacement associated with the 4H-SiC pieces. The stiffness of each specimen is then calculated from the force versus displacement values. The stiffness values obtained closely match the ANSYS simulation values as shown in Figure 50, which plots stiffness versus sample thickness for the ball-on-ring configuration. For this configuration, the theoretical stiffness is proportional to the product of Young's modulus times the sample thickness squared. The solid lines in Figure 50 have a slope of 2.0, and Young's modulus extracted from the experimental data is 403 GPa. This is within the range 390 – 690 GPa typically reported in the literature for SiC [20,21]. A slightly higher value of 474 GPa was assumed in the simulations.

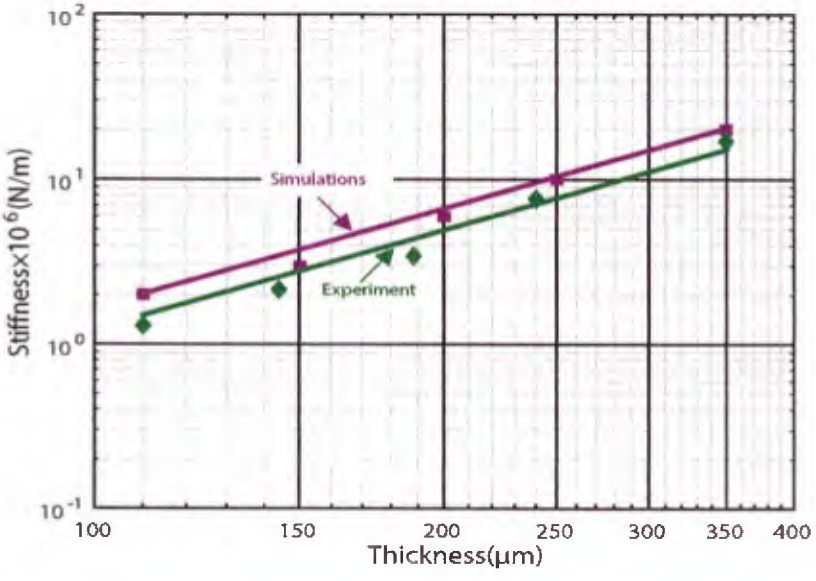


Figure 50: Comparison of simulated and measured stiffness as a function of thickness for un-etched 4H-SiC samples. The experimental data are obtained using the ball-on-ring configuration, as described in section IV.

We have demonstrated wafer-scale deep-trench patterned etching of 4H-SiC substrates of up to 180 μm with good uniformity, repeatability and control and without micro-trenching and micro-masking. ANSYS simulations reveal that the stiffness of the trench-etched-patterned pieces of wafers thinned to 200 - 250 μm is comparable to the wafers uniformly thinned to 110 μm that are presently used in commercial production. This process can be applied to any SiC device for which substrate resistance is a limitation. We currently have three separate projects which will leverage this method of substrate reduction, both for substrate resistance reduction (our 3G-MOSFET and IMOSFET projects), and as a novel means for accessing the p-type collector of an IGBT fabricated on the more readily available n-type 4H-SiC substrates. These projects are described in more detail in other sections of this report.

Task 3.3a: Superjunction Drift Regions (Monzurul Alam)

Superjunction (SJ) drift regions, as shown in Figure 51, were introduced in late 1990's. The theoretical foundation of SJ devices was first described by Fujihira in 1997 [22]. The model presented therein is based on a quasi-one-dimensional electrostatics analysis, and predicts a significant reduction in the drift layer specific on-resistance ($R_{ON,SP}$). Silicon superjunction MOSFETS, such as Infineon's CoolMOS product line, have already enjoyed significant commercial success. However, to date there have been no SiC Superjunction MOSFETs available. This task explores the feasibility of applying this concept to SiC power devices.

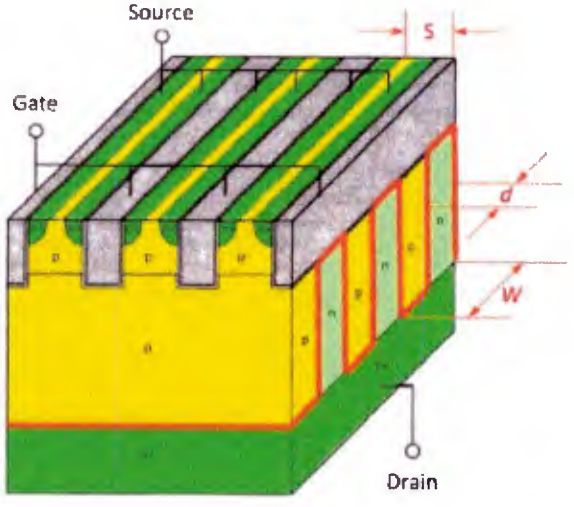


Figure 51: A superjunction drift region, as implemented in a silicon UMOSFET.

Superjunction Design and Simulation

Blocking voltage depends on the drift layer thickness t_{drift} for both planar and SJ devices. As described in Kimoto & Cooper, the optimum $R_{ON,SP}$ of a planar device with a blocking voltage, V_B can be estimated using the empirical equation

$$R_{ON,SP}(opt) = 2.8 \times 10^{-8} \times (T/300)^{2.8} \times V_B^{2.29} (m\Omega.cm^2)$$

where T is the absolute temperature. In contrast, Fujihira predicted that the optimum $R_{ON,SP}$ for a SJ device would be given by

$$R_{ON,SP}(opt) = 4 \times d \times V_B/(\mu \times \varepsilon_s \times E_c^2)$$

where d is the width of the p and n pillars. Two important features of SJ devices are apparent from this expression. First, the specific on-resistance of a SJ drift region increases linearly with blocking voltage, rather than as the square of blocking voltage as in a conventional drift region. Second, the specific on-resistance decreases with decreasing pillar width.

Since the Fujihira model is based on a simple 1-D analysis of the device, we studied the 2-D analytical model as outlined in Wang, et.al, 2009 [23]. While this model helped us develop better insight into SJ performance tradeoffs, it did not allow us to consider all the possible non-ideal scenarios that can arise in practical devices. Therefore we quickly moved to perform 2-D device simulations using *Sentaurus Device*. The simulations primarily varied three parameters: drift layer thickness (t_{drift}), pillar width (d), and pillar doping (N_D, N_A), which lead to corresponding blocking voltages (V_B). Then $R_{ON,SP}$ is calculated by using the formula

$$R_{ON,SP} = 2 \times t_{drift} / (q \times \mu_n \times N_D)$$

The factor of 2 arises because only half of the drift layer is comprised of conducting n-pillars. When the doping×width product of the two pillars is equal ($d_n N_D = d_p N_A$), the drift layer is said to be "balanced." This condition is assumed in the Fujihira model and in our initial simulations. Figure 7 compares $R_{ON,SP}$ of an optimized planar device to the Fujihira model, as well as to the results of our simulations. The 2-D simulation is in good agreement with the Fujihira model. The significant improvement at higher blocking voltages comes from the linear relationship between $R_{ON,SP}$ and V_B, while it is quadratic for planar devices. For example, at a blocking voltage (V_B) of 2000 V, a SJ device would have a 2-10x lower $R_{ON,SP}$ than a planar device for pillar widths from $d = 4$ μm to 1 μm.

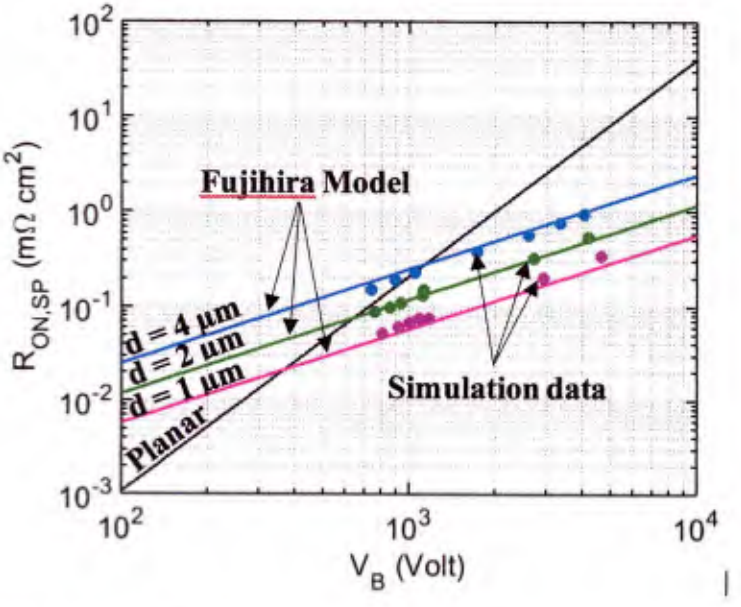


Figure 52: Comparison of the specific on-resistance of a conventional drift region and an optimal superjunction drift region as predicted by the Fujihira model (colored lines) and by Sentaurus Device simulations (points) for various pillar widths.

One of the major challenges in fabricating a SJ drift region is maintaining perfect charge balance between the *n* and *p* pillars. The degree of charge imbalance is defined as $(N_A - N_D)/N_D \times 100\%$, and we assumed without loss of generality that the p pillar doping (N_A) is below nominal in our simulations. Figure 53(a) shows the results of our simulations assuming a -20% imbalance for pillar widths of 1, 2, and 4 μm, compared with the balanced SJ Fujihira model. Assuming perfect charge balance, the blocking voltage is essentially proportional to the SJ drift layer thickness for a given pillar width. However, in the presence of significant imbalance, a portion of the more heavily-doped pillar remains undepleted. This limits the blocking voltage that can be achieved for a particular pillar width. Beyond this limit, any increase in thickness only serves to increase the specific on-resistance. This limiting blocking voltage increases with pillar width, and decreases with increasing levels of imbalance.

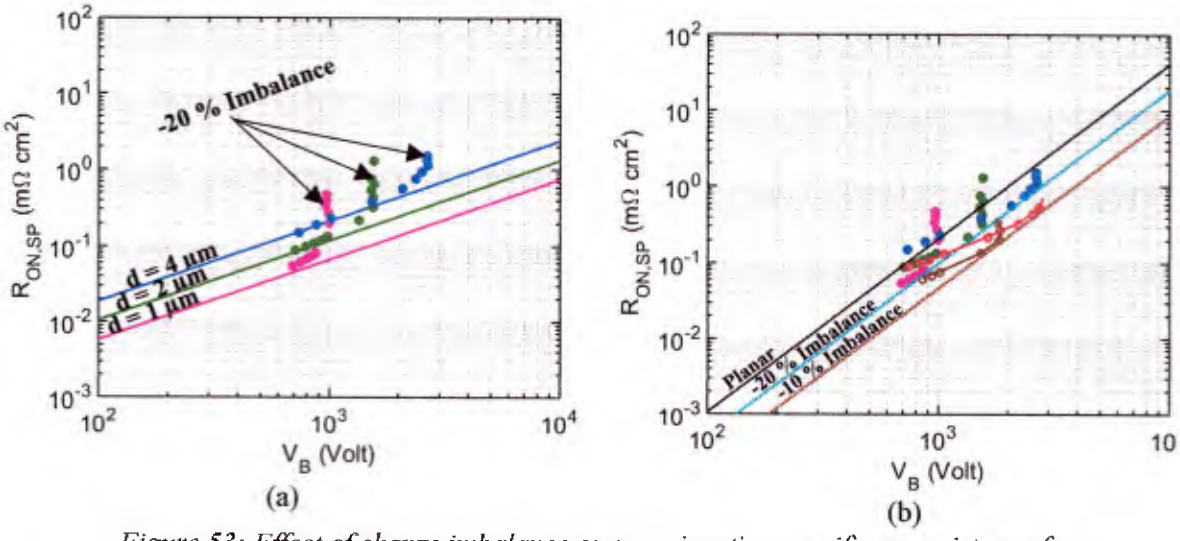


Figure 53: Effect of charge imbalance on superjunction specific on resistance for (a) balanced (lines) and -20% imbalanced (points) SJ devices and pillar widths of 1, 2, and 4 μm (b) -10% (open circles with lines) and -20% (solid circles) imbalanced SJ devices.

Figure 53(b) shows the simulation results for -20% (solid circles) and -10% (open circles with lines) imbalanced SJ devices for various pillar widths. The unipolar power device figure-of-merit is defined as $V_b^2/R_{on,sp}$. The highest possible FOM for a given level of imbalance can be represented by a line with slope V_b^2 tangent to this data, as illustrated in Figure 53(b) by blue (-20%) and brown (-10%) dotted lines. It is apparent from this plot that the specific on-resistance of SJ devices with charge imbalance increases with the ***square*** of V_b, just as in conventional devices, although up to a 5x reduction is possible if imbalance can be kept below 10%.

The previous simulation results were based on simple box profiles with constant pillar dopings. However, if the multicycle implant-epi-implant process is used, the doping profiles will not be constant, and this could lead to another source of imbalance, at least on a local scale. Therefore we simulated devices with a more realistic implanted profile to determine the extent to which this could further limit device performance. According to our constant doping simulation an optimum pillar doping ($N_{D,opt}$) of 8×10^{16} cm^{-3} is necessary for a pillar width (d) of 2 μm. Therefore, multi-energy implant schedules were developed using the analytical doping models of Janson, et al. [5] (which we have previously verified by experiment) to create a SJ drift layer as shown in Figure 10(a). The model shows that a drift layer thickness of 2.5 μm is possible by

single step multi-energy implant schedules of Al and N with highest energy of 4.4 MeV and 4 MeV respectively. The number of implants per cycle required for Al and N are 13 and 16 respectively to minimize ripple in the profile. Eight successive epi-implant cycles are required to form a drift layer thickness (t_{drift}) of 20 µm. A typical simulated SJ drift layer is shown in Figure 54(a) and corresponding performance is compared with planar device and a SJ with constant doping in Figure 54(b). This shows that the performance of the SJ device by the multicycle implant-epi regrowth method is almost identical as that of an idealized constant doping SJ device.

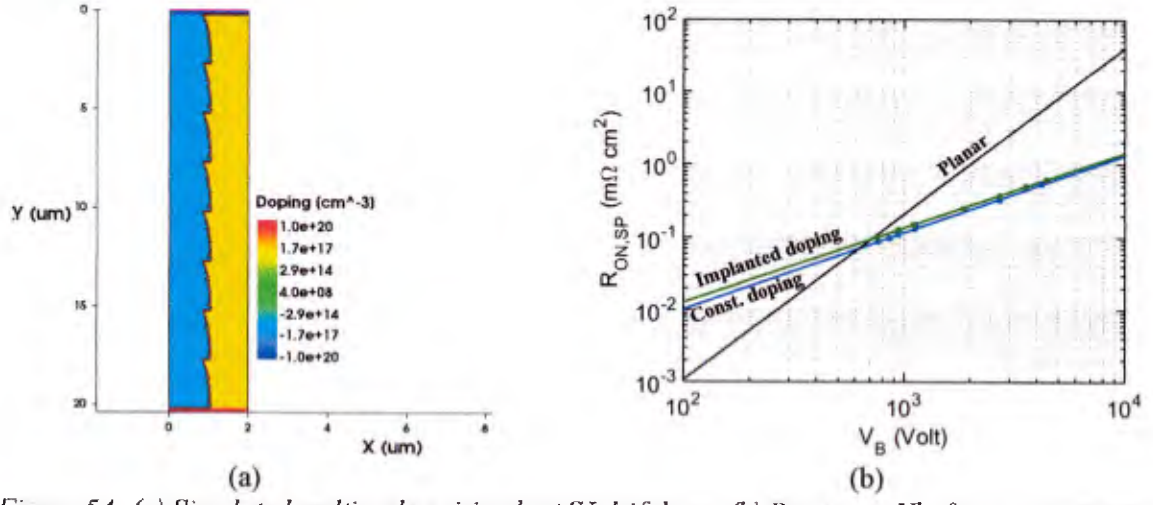


Figure 54: (a) Simulated multicycle epi-implant SJ drift layer (b) Ron,sp vs. Vb for a conventional drift region, an ideal uniformly-doped SJ, and a multicycle epi-implant SJ.

In the section above, we discussed in detail the limitations of superjunction performance caused by the lack of perfect charge balance between the *n* and *p* pillars. The specific on-resistance ($R_{on,sp}$) of an imbalanced superjunction follows a quadratic relationship with blocking voltage (V_{BR}), instead of a linear relation as outlined in [6].

Figure 55 shows the performance limit of a superjunction having -20% charge imbalance, obtained by reducing the dose ($d*N_D$) to $\approx 7.0\times10^{12}$ cm^{-2}. A unique choice of dose and drift layer thickness (t_{drift}) is necessary to achieve any particular blocking voltage for the expected degree of charge imbalance. The imbalanced limit line is almost parallel to that of a conventional limit. Therefore, a fixed margin of improvement over the conventional structure is possible for a given degree of imbalance. For example, in the case of -20% charge imbalance, approximately 3~3.5x improvement is feasible, and a lower-than-expected charge imbalance will improve the performance margin.

Figure 55 also presents the performance limit for -10%, and -5% charge imbalance. These limit lines are also essentially parallel to the conventional limit. The limit for -5% charge imbalance shows an improvement of about 10 ~ 12x over a conventional drift layer. After a careful study of silicon superjunction physics and literature, it is clear that charge imbalance is inevitable.

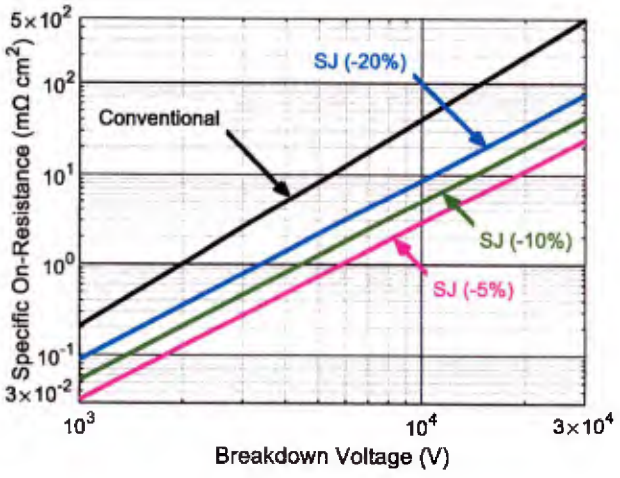


Figure 55: Performance limits of SiC superjunction drift layers in the presence of charge imbalance.

In summary, we have found that in the presence of charge imbalance, superjunction drift regions exhibit a quadratic dependence of specific on-resistance on blocking voltage, similar to conventional drift regions. This is in contrast to the commonly-accepted *linear* dependence, which can only be realized under conditions of perfect charge balance. To minimize the effect of imbalance, we developed a design methodology that produces the maximum figure-of-merit under an anticipated percentage charge imbalance, which we described in detail in a recent publication.

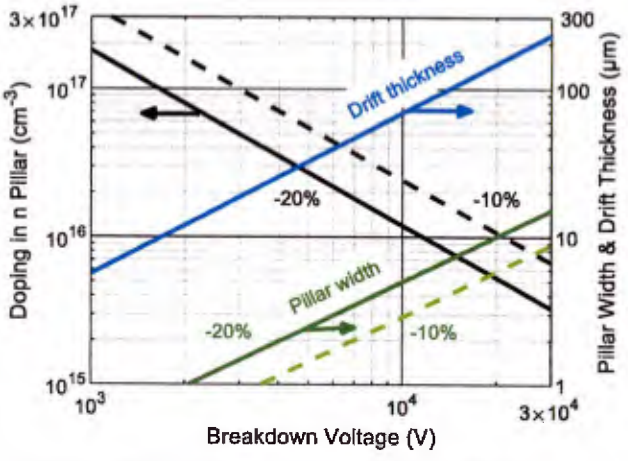


Figure 56: Optimum design parameters for SJ's in 4H-SiC as a function of V_{BR} for charge imbalances of -20% (solid lines) and-10% (dashed lines).

The optimum pillar doping, pillar width, and drift layer thickness were determined for different anticipated levels of charge imbalance. Figure 56 shows the optimum SJ parameters for 4H-SiC as a function of design blocking voltage for two levels of charge imbalance, -10% and -20%. The lines in Figure 56 are obtained by fitting to data points between $d = 1$ and $d = 6$ μm. The optimum drift layer thickness is the same for both -10% and -20% imbalance. Likewise, the aspect ratio t/d is nearly constant over the V_{BR} range for a given imbalance, around 14:1 for -20% imbalance and 24:1 for -10% imbalance. Superjunction devices designed using this

guidance can have lower specific on-resistance than conventional drift regions, even in the presence of realistic levels of charge imbalance.

Statistical Performance Analysis in the Presence of Random Imbalance

Inevitable random variations in the pillar width or doping arising from the imperfection of the fabrication process will necessarily result in a varying degree of imbalance, which generally degrades blocking voltage and alters the specific on-resistance. We have applied a Monte-Carlo analysis to study the effect of these variations on device performance. We start by assigning a Gaussian probability distribution to each of the device design parameters: pillar width, epilayer thickness, and pillar doping, each with the standard deviation-to-mean ratios shown in Figure 57.

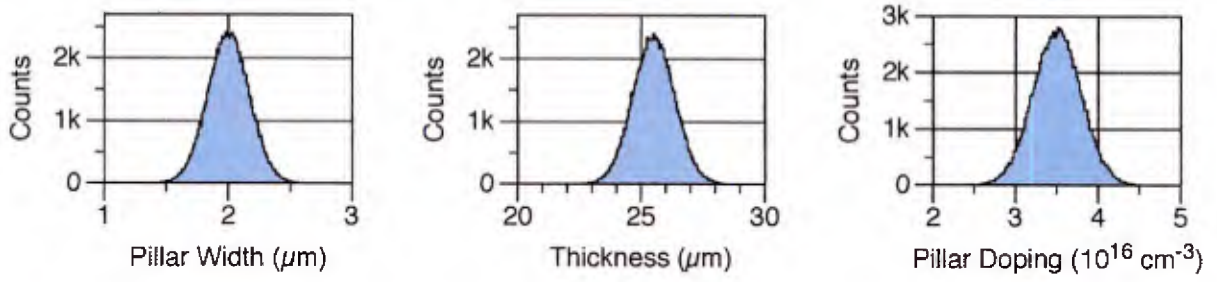


Figure 57: Gaussian probability distributions for pillar width, epilayer thickness, and pillar doping.

As a demonstration of this technique, we applied the analysis to two design cases targeted at 4 kV, one corresponding to the naive assumption of a perfectly balanced, Fujihira model optimum for pillar width $d = 2\ \mu m$, and the other using the parameters optimized for -20% imbalance. These distributions are sampled to generate a random population of 100,000 designs. Then using the Wang model (including ionization integrals), we calculate the blocking voltage and on-resistance of each.

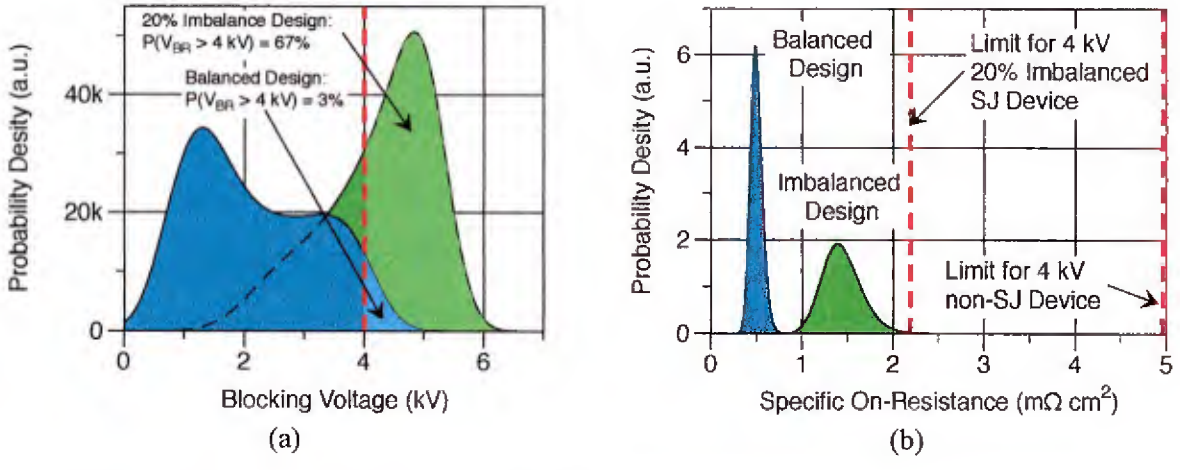


Figure 57: Probability distributions for (a) blocking voltage and (b) specific on-resistance for a 4 kV balanced SJ design (blue), and a design optimized for 20% charge imbalance (green), subject to the random parameter variations documented at the bottom of the previous page.

The results are striking, particularly for the balanced design (see Figure 57). There is a broad distribution of blocking voltage, peaking at about 1,300 V, and only 3% of the results are greater than the desired 4 kV. This is not surprising, however, since the design assumed perfect balance, and nearly all random combinations of the varied parameters result in at least some imbalance, which always leads to a reduction in blocking voltage. The reason there are any samples at all with blocking voltages > 4 kV is that half the samples have thicker-than-nominal drift layers, and a few of these are nearly balanced, leading to slightly higher-than-nominal blocking voltages.

The case is decidedly better for the SJ devices designed with 20% imbalance in mind, at least in terms of blocking voltage, with 67% of the devices exhibiting a blocking voltage above the desired 4 kV. To achieve this improvement, the specific on-resistance increases by approximately a factor of 3x and the distribution widens slightly, but still retains a 3x improvement over conventional drift regions.

These results can be illustrated in an even more compact manner using a traditional plot of $R_{on,sp}$ vs. V_{BR}, as shown in Figure 58. The black diagonal line shows the limit for conventional drift layers, and the dotted line indicates the design blocking voltage. The contour plots show the distribution of results for both SJ designs. Each contour represents the boundary within which 10%, 50%, or 90% of the results are found.

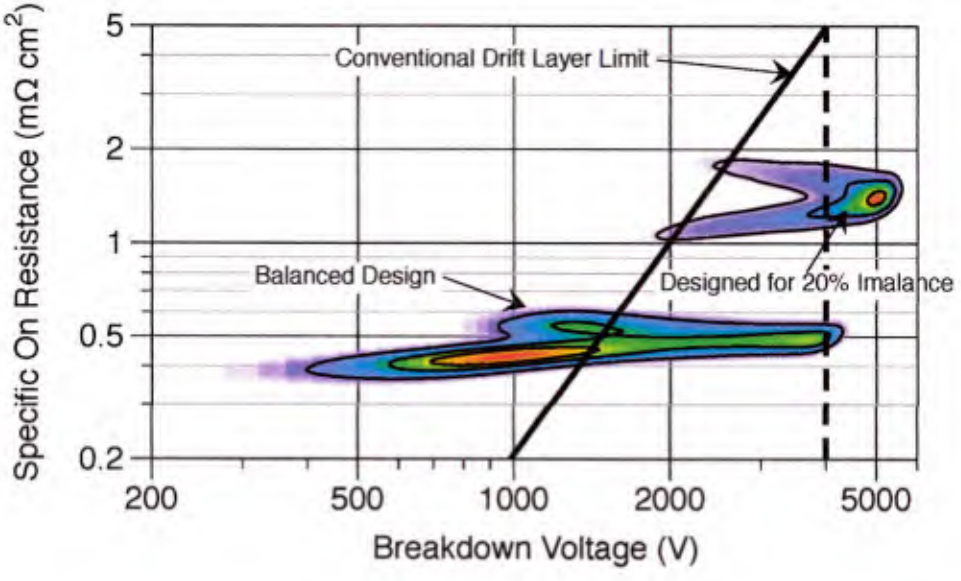


Figure 58: Contour plots of $R_{on,sp}$ vs. V_{BR} for balanced SJ designs and designs optimized for 20% charge imbalance and a target blocking voltage of 4 kV. The contours enclose 10%, 50%, and 90% of the devices. The lower contour plot assumes a balanced nominal design, and the upper contour plot is for a SJ design optimized for 20% imbalance.

The results of this section should not be interpreted as a fully-optimized SJ design, since we still fail to achieve our target of 4 kV in approximately 1/3 of the possible cases. However, the Monte Carlo statistical analysis method described in this case study is extremely valuable in helping us select a target design that has a high probability of success in meeting both the targeted blocking voltage and a significant reduction in on-resistance compared with conventional devices.

Potential Superjunction Fabrication Methods

The fabrication of superjuction devices is straightforward in theory, but challenging in practice, especially in terms of maintaining pillar symmetry and charge balance. The pillars can be formed using one of two basic methods: (i) ion implantation, or (ii) trench etch + epitaxial re-fill. Ion implantation has the advantage of excellent dose control, which helps achieve low levels of imbalance. To minimize charge imbalance, we would start with a very lightly doped epilayer and perform a blanket implant of nitrogen to form the *n* pillars. The *p* pillars would then be formed by selective counter-doping with an aluminum implant. This method does not require alignment of the *n* and *p* pillars, and benefits from the excellent dose control of ion implanation for both *n* and *p* pillars. Figure 59(a) shows a schematic diagram of a SJ drift layer formed by implant-epi regrowth method.

The blocking voltage of implanted SJ devices is limited by the implant depth that can be achieved by the maximum implant energy available. Using the maximum energy of 5 MeV available from our vendor, Ion Beam Services of Peynier, France, we can expect to achieve a drift layer thickness of ~ 2.65 µm from a single implant, which would provide a V_b of only ~ 430 V. To achieve higher blocking voltages, multiple implant / epitaxy / implant cycles would be required, with each subsequent implant step requiring an alignment to the previous implant. SiC superjunctions become useful well above 4 kV, where the drift region dominates the on-resistance, but this requires *at least **nine** epi / implant cycles.*

The trench-refill process would start with a nitrogen-doped epilayer that will form the *n* pillars. The *p* pillars are then formed etching a deep trench by anisotropic RIE, then filling the trench by an epitaxial regrowth of p-type SiC . This allows the entire structure to be formed in a single step, but relies on tight control of doping concentrations during epitaxy and accurate lithography to achieve low imbalance levels. Recently published work on SiC trench fill epitaxy suggests that this method may one day become a practical reality. Figure 59(b) shows a cross-section of a 48 µm thick SiC trench refill, with a 6:1 aspect ratio. [24]. However, the aspect ratio required to achieve optimal performance in the presence of ~20% charge imbalance is approximately 13:1, and the high level of doping control required to achieve adequate charge balance has yet to be adequately demonstrated.

We contacted Ascatron AB as a potential vendor for such refill epitaxy. After reviewing our requirements, they informed us that for practical reasons their process is limited to a 2.5 µm wide trench, 12 µm deep, corresponding to an aspect ratio of only ~5. In addition, our discussions with Ascatron revealed that doping control within such refilled structures is currently too poor to achieve even this modest level of balance.

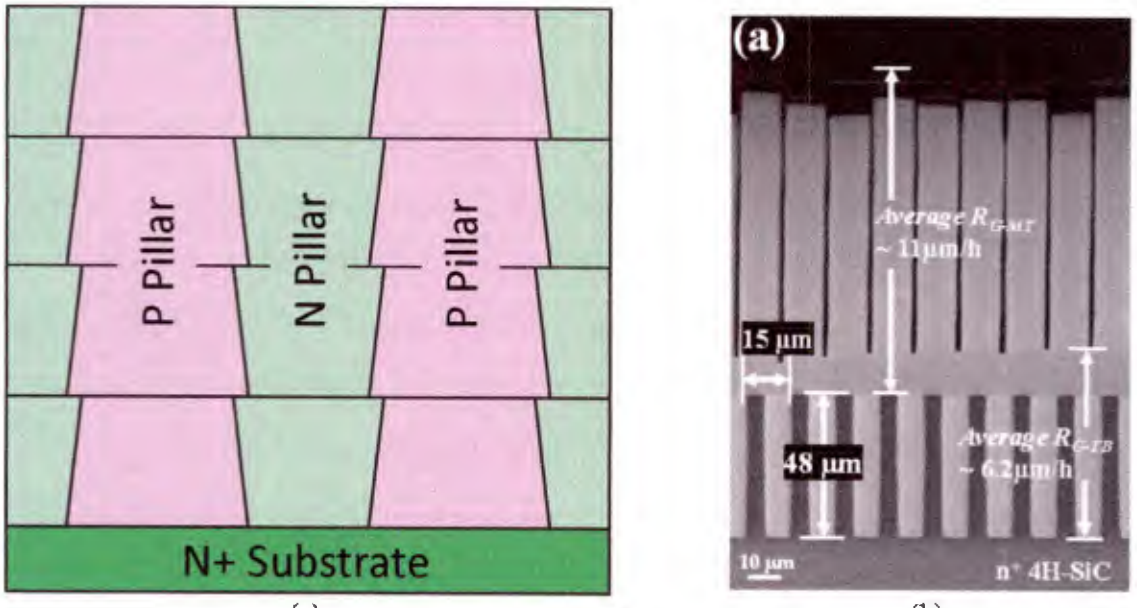


Figure 59: Fabrication of superjunction drift layer: (a) Illustration of Multicycle implant / epitaxial regrowth method, (b) SEM cross-section of trench-refill method of Ji, et al., before planarization.

Task 3.3b: Waffle-Substrate *n*-IGBT (Monzurul Alam)

Overview

In high-voltage power devices, the drift region typically limits on-state performance because of its high resistance compared with other parts of the device structure. As described in the previous section, we conducted a detailed study on SiC superjunction (SJ) drift regions to determine whether or not this technology would provide a significant benefit, while taking into consideration the current state-of-the-art in SiC fabrication technology. After rigorous study, we concluded that the inevitable charge imbalance present in all practical SJ structures imposes substantial limitations on the improvements which can be achieved, and that current SiC fabrication technology must be significantly advanced before SJ devices become practical.

We thus shifted our focus to the insulated gate bipolar transistor (IGBT) as an alternative solution for high-voltage devices. In an IGBT, conductivity modulation in the drift region overcomes the high resistivity problem. An n-channel IGBT is preferable over a p-channel IGBT because the SiC channel mobility for electrons is nearly an order of magnitude higher than for holes. On the contrary, an n-channel IGBT requires a p-type substrate which is highly resistive. Therefore, fabrication of an n-channel IGBT is limited to the ultra-high voltage (V_{BR} > 15 kV) where the epitaxially grown p+ anode layer is sufficiently thick to be free-standing after removal of the substrate.

However, the innovative waffle substrate concept, also described in this report, can be used to develop an n-channel IGBT for medium voltage applications (< 15 kV). Figure 60 shows an n-channel IGBT with a thick free-standing drift layer suitable for ultra-high voltages, and a waffle substrate n-channel IGBT suitable for medium voltages.

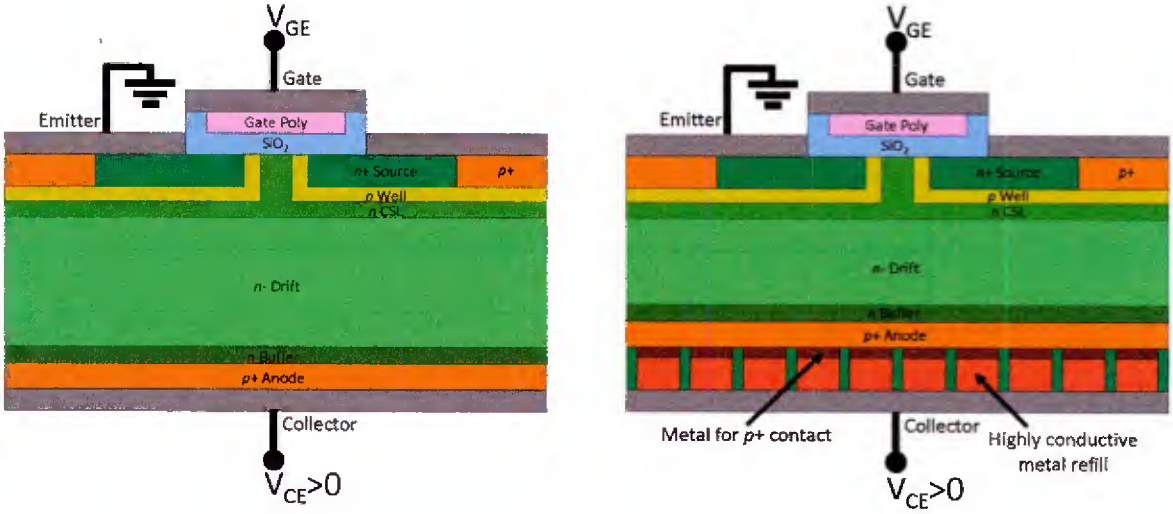


Figure 60: (a) Ultra high voltage n-channel IGBT without the substrate (b) moderately high voltage n-channel IGBT with waffle like substrate

We derived a 1-D analytical model to determine the range of voltages where the IGBT is superior in performance to an equivalent *n*-channel DMOFET. The model is derived excluding the CSL and buffer layer shown in Figure 60. As illustrated in illustrated in Figure 61, this first order calculation shows that *n*-channel IGBT should exhibit superior performance in low frequency applications for a blocking voltage $V_{BR} > 6$ kV at 175°C, assuming a maximum power dissipation of 200 W/cm^2. Based on this analysis we to fabricate an *n*-channel waffle substrate IGBT with a blocking capability of 12.5 kV, where the improvement factor could be as high as 2.5x at 200 W/cm^2 power dissipation.

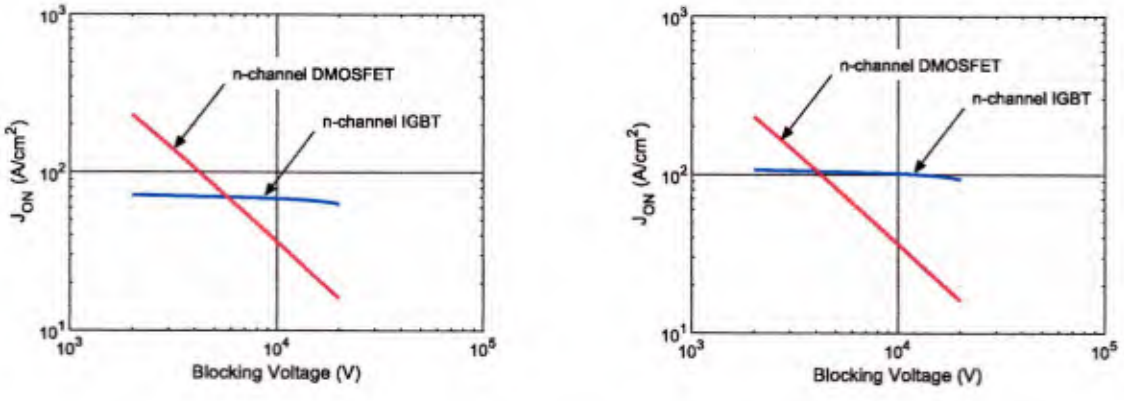


Figure 61:On-current vs. blocking voltage for an n-channel IGBT and an n-channel DMOSFET at 175°C for power dissipation limits of (a) 200 W/cm^2 (b) 300 W/cm^2

Design parameters and on-state performance

While first order calculations using analytical models helped guided us to an appropriate application for the *n*-channel waffle substrate IGBT, 2D numerical simulation using Sentaurus™ Device is required to optimize design parameters shown in the cross section of Figure 62. The top part of the device is obtained by ion implantation, and to keep the fabrication as simple as possible, we are using contact optical lithography throughout, except for the edge termination which requires higher tolerances. The doping profiles used in the numerical simulation are shown in Figure 63. The dose of the base underneath the source is about 4.1×10^{13} cm^{-2}, sufficient to prevent the punch through of the base region the off-state.

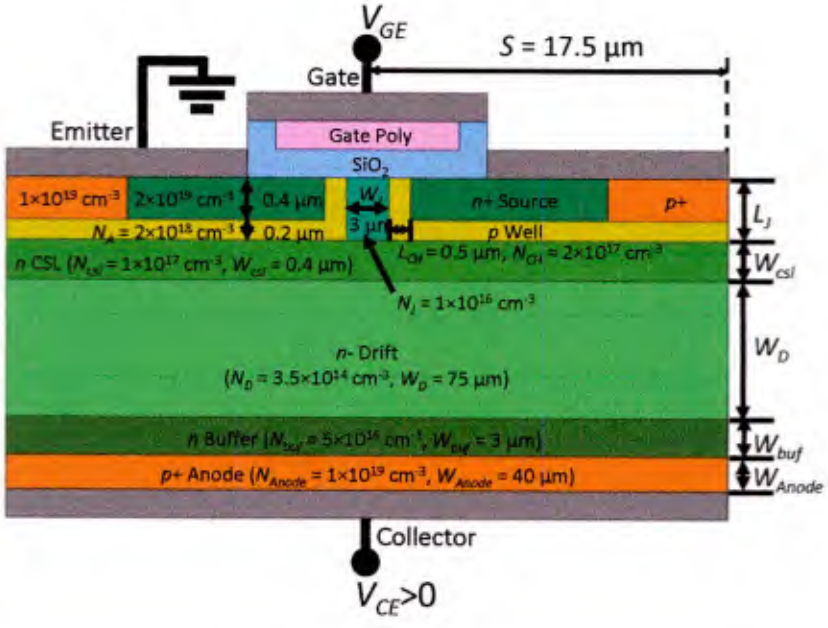


Figure 62: Cross section of an n-channel IGBT, highlighting relevant design parameters

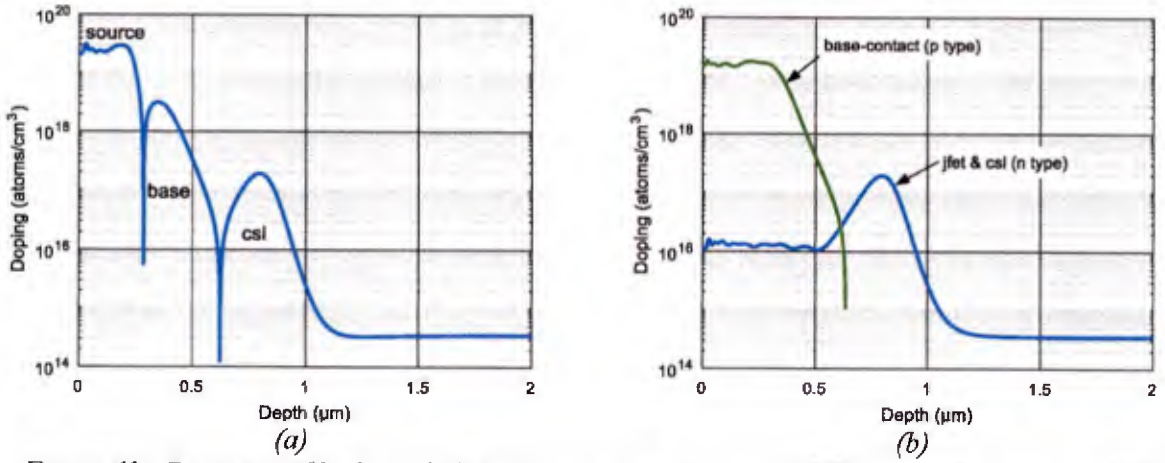


Figure 63: Doping profile through the source and base (a) and JFET (b) regions based on implant range and straggle models found in [4]

The use of contact optical lithography imposes a fairly large cell pitch (17.5 μm), but does not significantly impact performance since the current rating will be limited primarily by the ~ 3 V forward diode drop intrinsic to all SiC IGBTs. The simulated on-state current density is plotted as a function of applied voltage in Figure 64(a), compared with the simplified one-dimensional dc analysis of the IGBT presented in [25]. At a power density limit of 200 W/cm^{2}and a junction temperature of 175°C, the expected current density is 60 A/cm^2 at a forward voltage of 3.3 V, while a comparable n-channel DMOSFET would be limited to 28 A/cm^2 at 7.1 V.

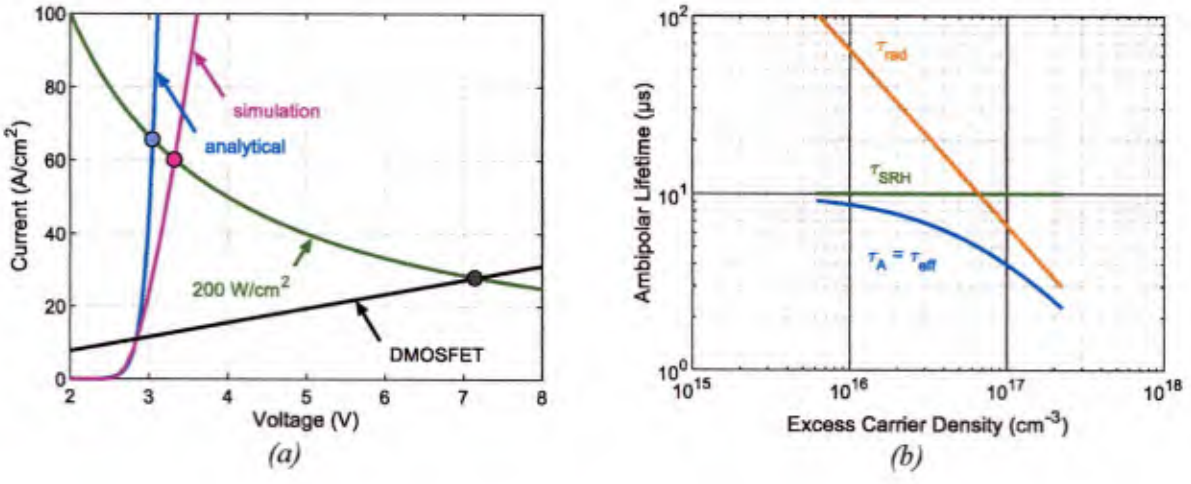


Figure 64: (a) Simulated I-V characteristics of a 12.5 kV n-channel IGBT and a comparable n-channel DMOSFET (b) Ambipolar lifetime as a function of excess carrier density

The ambipolar lifetime of the carriers in the drift region determines the degree of conductivity modulation in an IGBT. We considered Shockley-Read-Hall (SRH) lifetime of the carrier to be 10 μs in both our simulation and analytical calculations. However, other mechanisms like radiative and Auger recombination also affect the ambipolar lifetime of the carriers. Fortunately, the lifetime due to auger recombination has negligible impact on the net lifetime, but radiative recombination is important at high temperatures and at high carrier concentrations. We have extracted the ambipolar lifetime profile in the drift layer as a function of carrier density from the simulation and presented it in Figure 64(b). An average value of the ambipolar lifetime is ~ 5 μs, or about 50% of the SRH lifetime.

Design of edge termination

We have also simulated a floating field ring (FFR) edge termination structure to determine suitable parameters. This simulation is very time consuming because a large number of floating field rings is required to obtain such high blocking voltages. At least eighty rings are required, with an initial spacing s_0 = 1 μm, and an initial ring width w_0 = 1 μm. The total FFR width would be 388 μm to block 10 kV (80% of 12.5 kV). The spacing and the widths are be increased by 2% from one ring to the next from the main junction outward. An alternative design with a blocking voltage requires 90 rings in 371 μm with s_0 = 0.75 μm, w_0 = 0.75 μm and an increment of 2%, but requires slightly higher resolution lithography. In either case, the *p*+ implanted edge

termination rings will be achieved by e-beam lithography, due to the small dimensions and high tolerances required.

Mask Layout

The fabrication of the proposed *n*-channel IGBT requires 11 lithography masks. We have three device types, denoted as A, B, and C, having cell pitches 17.5 μm, 21.5 μm, and 27 μm respectively. The differences in cell pitch arise from different alignment tolerances and minimum feature sizes. In our design, the expected on-state current density is 60 A/cm^2 at a maximum power density of 200 W/cm^2. There are three different sizes of the devices included in the mask set, with active areas of 0.25 mm^2, 1.69 mm^2, and 13.4 mm^2, referred to as small (0.15 A), medium (1 A), and large (8 A), respectively. A representative device from the mask layout is shown in Figure 65.

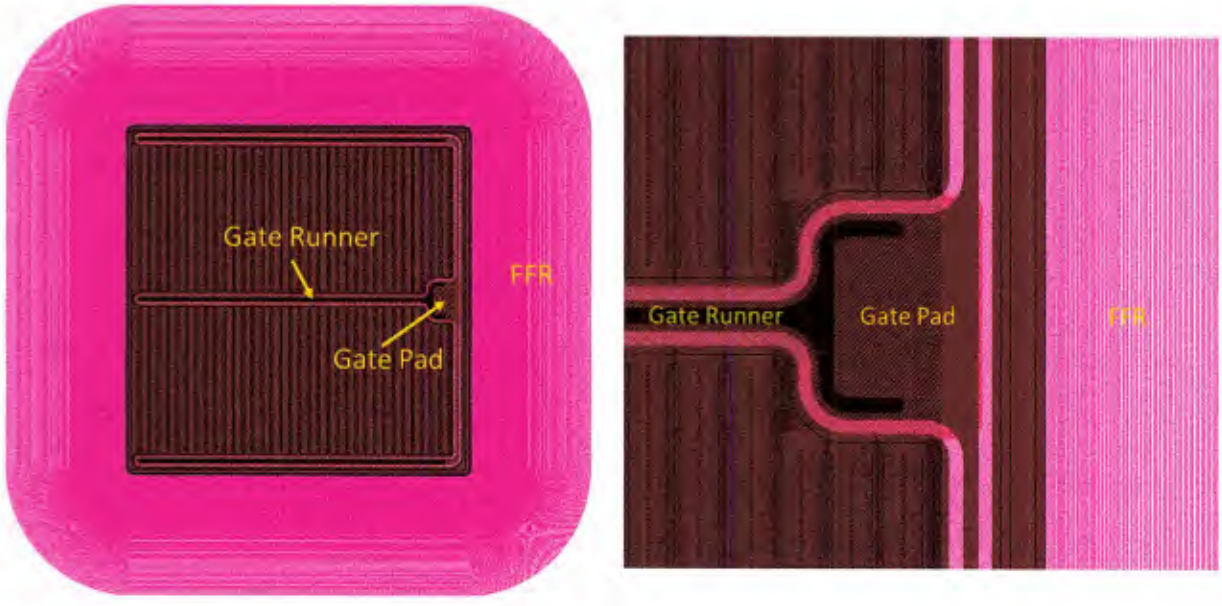
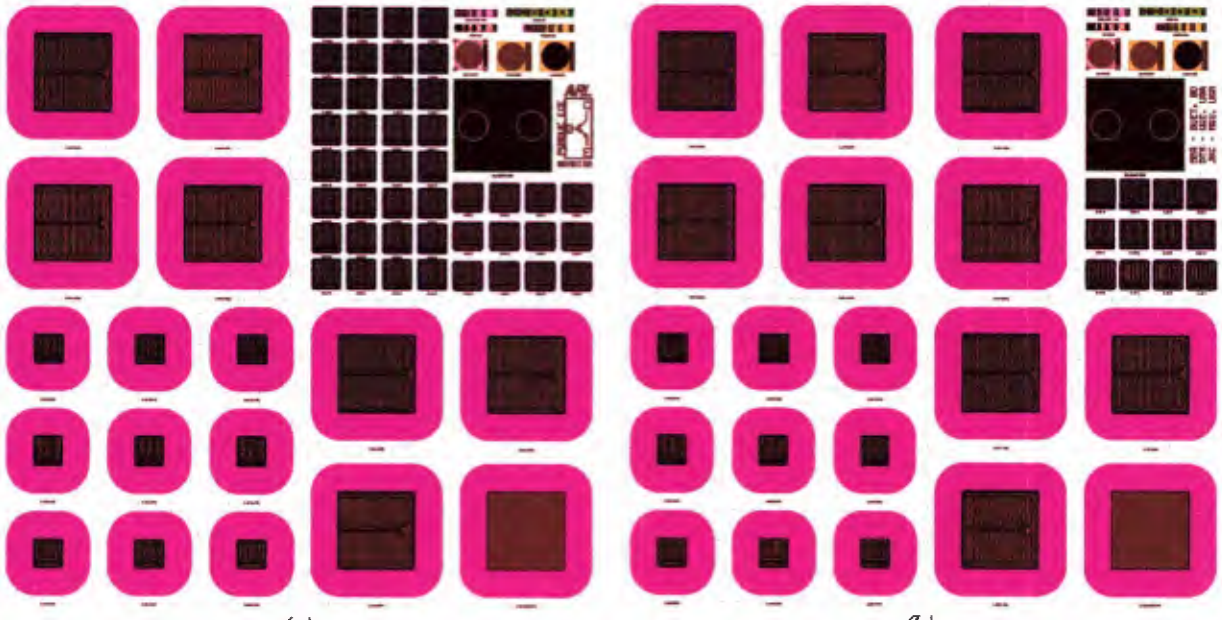


Figure 65: Sample IGBT from the mask design

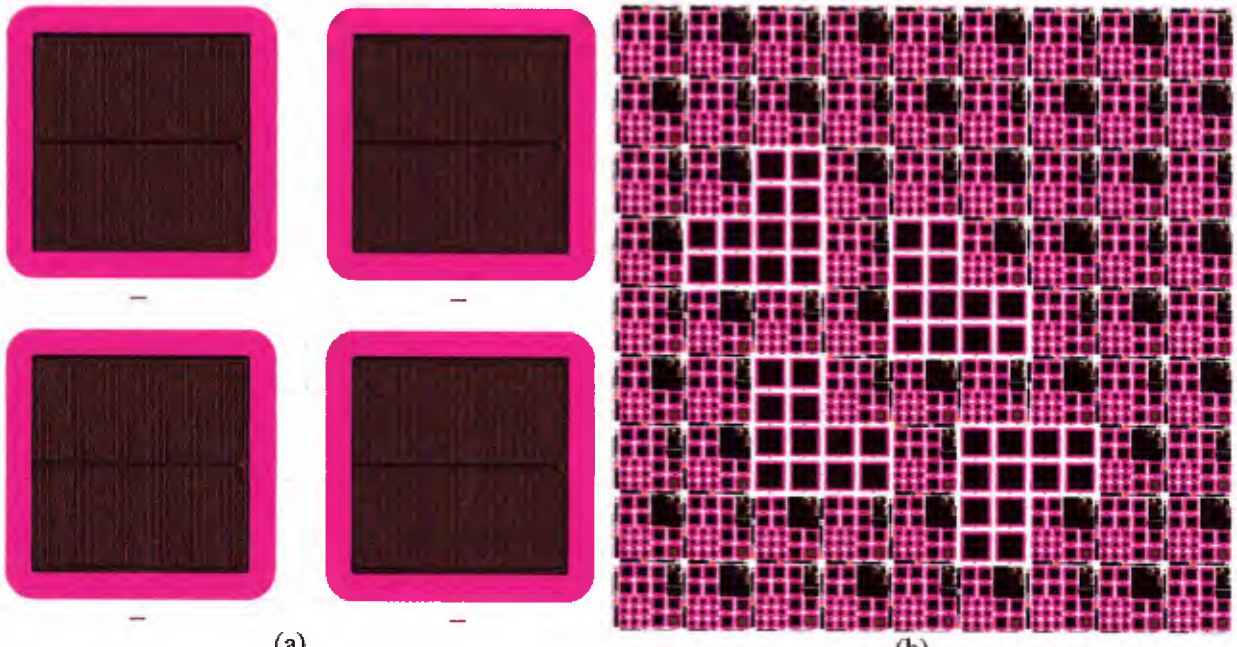
The overall layout consists of three different types of die, each 10.8 mm × 10.8 mm. Type-I and type-II die are shown in Figure 66. Each die is divided into four quadrants, and all quadrants of type-I and type-II are identical except the first quadrant. In this first quadrant, we have placed several small devices without floating field rings, as well test structures such as TLMs and MOSCAPs. In the type-II die, some of the small devices in the first quadrant are replaced by two medium sized devices, one type A and one type B. There are nine small devices with floating field rings in the third quadrant of these die.



(a) *(b)*

Figure 66: Layout of (a) Type-I (b) Type-II die

Figure 67(a) shows the type-III die where we have placed four large devices of type B which are expected to carry 8 A. The overall layout for a full wafer is shown in Figure 67(b).



(a) (b)

Figure 67: Layout of the (a) type-III die, and (b) full wafer

Fabrication

The fabrication process will be carried out using four quarter wafer samples. Two of these samples will receive a carbon implantation and anneal lifetime enhancement process, while the other two control samples will not. The four samples will be processed as two lots in series, with one enhanced lifetime sample and one control sample in each lot. The design of the layout is such that there are five type-I die, five type-II die, and three type-III die. There are total 457 devices in a quarter wafer, with 42% of the devices having floating field ring edge terminations. The twelve large devices are placed in the layout such that they will be close to the center of the quarter wafer.

We have implemented a lifetime enhancement procedure suggested by Miyazawa and Tsuchida [26], whereby a high dose (1.35×10^{16} cm^{-2}) of carbon is implanted in four samples (PU435Q1, PU435Q3, PU436Q1 and PU436Q3). This implant creates a high concentration of carbon interstitials through impacts with the lattice. The samples are then annealed at 1600°C for 30 min to diffuse these carbon atoms into the drift layer where they recombine with carbon vacancies, which have been shown to be the dominant lifetime degrading defect. This process therefore increases the minority carrier lifetime. All four samples are then etched using RIE to remove the area damaged by the high dose implantation. Finally a sacrificial oxide is grown by a 10 hr wet oxidation to reduce the resulting surface roughness.

Fabrication of the proposed *n*-channel waffle-substrate IGBT is currently underway, and the current status is summarized in Table 4. We have identified following major steps to complete the IGBT fabrication, not including the waffle substrate.

Table 4: Fabrication progress of an n-channel IGBT with waffle substrate

<table>
<tr><td colspan="2">Purpose</td><td colspan="4">IGBT Device Fabrication</td><td colspan="4">Lifetime Measurement</td></tr>
<tr><td colspan="2">Sample ID</td><td>PU435Q2</td><td>PU436Q2</td><td>PU435Q3</td><td>PU436Q3</td><td>PU435Q1</td><td>PU436Q1</td><td>PU435Q4</td><td>PU436Q4</td></tr>
<tr><td rowspan="10">Active Device Fabrication</td><td>Lifetime enhancement</td><td>N/A</td><td>N/A</td><td>done</td><td>done</td><td>done</td><td>done</td><td>N/A</td><td>N/A</td></tr>
<tr><td>N implantation for JFET & CSL</td><td>done</td><td>done</td><td>done</td><td>done</td><td rowspan="10" colspan="4">N/A</td></tr>
<tr><td>Al implantation for base</td><td>done</td><td>done</td><td>In progress</td><td>In progress</td></tr>
<tr><td>N implantation for source</td><td>done</td><td>done</td><td rowspan="9">not started</td><td rowspan="9">not started</td></tr>
<tr><td>Al implantation for base contact</td><td>In progress</td><td>In progress</td></tr>
<tr><td>Field oxide deposition</td><td rowspan="8">not started</td><td rowspan="8">not started</td></tr>
<tr><td>Poly Si gate formation</td></tr>
<tr><td>Gate metallization</td></tr>
<tr><td>Source & base metallization</td></tr>
<tr><td>Top layer metallization</td></tr>
<tr><td>Back-side Fabrication</td><td>Waffle Substrate</td></tr>
</table>

Addendum: The Concept of Gate-Charge Scaling (James Cooper)

It was pointed out by Dr. Allen Hefner at one of our program reviews that decreasing the specific on-resistance of a SiC power MOSFET automatically decreases its short-circuit withstand time (SCWT). Since the goal of this project is to decrease the specific on-resistance, it is important to find a way to break the connection between on-resistance and SCWT. Our proposal involves what we term *constant-gate-charge scaling*, as will be described below.

The specific on-resistance of a power MOSFET can be written

$$R_{CH,SP} = \frac{L_{CH}(WS)}{\mu_{CH} W_{CH} C_{OX}(V_G - V_T)}$$

where L_{CH} and W_{CH} are channel length and width, μ_{CH} is channel mobility, C_{OX} is oxide capacitance, V_G and V_T are the gate and threshold voltages, and W and S are the width and pitch of a MOSFET unit cell. Any decrease in channel resistance causes a proportional increase in saturation current, given by

$$J_{D,SAT} = \frac{1}{2}\left[\frac{\mu_{CH} W_{CH} C_{OX}(V_G - V_T)}{L_{CH}(WS)}\right](V_G - V_T) = \frac{(V_G - V_T)}{2R_{CH,SP}}$$

Assuming adiabatic heating during the short-circuit event, the SCWT at half the rated voltage can be approximated by

$$SCWT = (4\rho C_p \Delta T)/(E_C J_{D,SAT})$$

where ρ is the material density, C_p is the specific heat, ΔT is the maximum allowable temperature rise, and E_C is the critical field. Clearly, any increase in saturation current directly reduces SCWT.

We propose to break the connection between channel resistance, saturation current, and SCWT by reducing both the oxide thickness and on-state gate voltage, keeping the gate charge (and oxide field) constant, as described below.

The gate charge in inversion can be approximated by $Q_G \approx C_{OX}(V_G - V_T)$. If we reduce both oxide thickness and $(V_G - V_T)$ by the factor α, the gate charge, oxide field, and specific on-resistance remain constant, but the saturation current is reduced by the factor α. This reduces the power dissipation and lengthens SCWT by the factor α, *with no degradation in either on-state or blocking performance.*

Figure 69 illustrates this concept using the analytical bulk-charge MOSFET equation. Here the saturation current is reduced by >3× as the oxide thickness is scaled from 50 nm to 10 nm with the oxide field held constant at 4 MV/cm. Figure 70 expands the origin of Figure 69, showing curves of constant power dissipation. Clearly the on-state performance (slope of the I-V curves) is unaffected by this scaling. Figure 71 shows 2-D simulations of a short-channel

trench MOSFET subject to constant-gate-charge scaling. Not only is the saturation current reduced, but the output conductance in saturation is also largely eliminated. This is because the thinner gate oxide reinforces gate control over the potential barrier at the source, reducing drain-induced barrier lowering (DIBL). In this case, scaling the oxide thickness from 50 nm to 10 nm reduces saturation current (and increases SCWT) by almost 5×.

As oxide thickness is reduced, we scale the on-state gate voltage to maintain the same gate charge and oxide field. A careful analysis shows that the required gate voltage does not depend on threshold voltage, since we can write

$$Q_g = \varepsilon_{ox} E_{ox} = \varepsilon_{ox} \left(V_g - \varphi_{ms} - 2\psi_F \right) / t_{ox}$$

where φ_{ms} is the gate-semiconductor work function and ψ_F is the bulk Fermi potential. This makes it easy to select the on-state gate voltage corresponding to a given oxide thickness and desired oxide field.

Constant-gate-charge scaling can be applied to existing production devices, both planar DMOSFETs and trench MOSFETs, simply by reducing the oxide thickness. No other process changes are required, and existing mask sets can be used without modification. If desired, the reduced DIBL may also permit the use of shorter channels, further improving the performance.

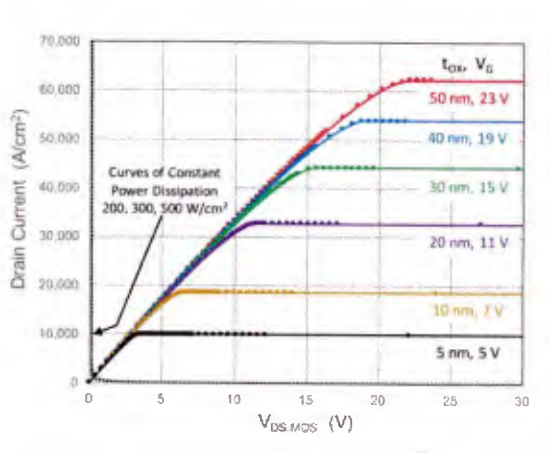


Figure 69. I-V characteristics computed using the bulk-charge equation. Oxide thickness and gate voltage are scaled to keep the oxide field constant at 4 MV/cm (Q_g = 1.38 μC/cm²).

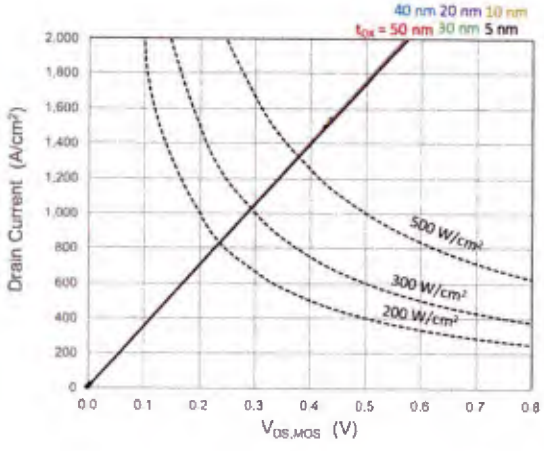


Figure 70. Expanded view of Figure 69 near the origin, showing constant power contours. The on-resistance, given by the inverse slope of the I-V characteristics, is the same for all curves.

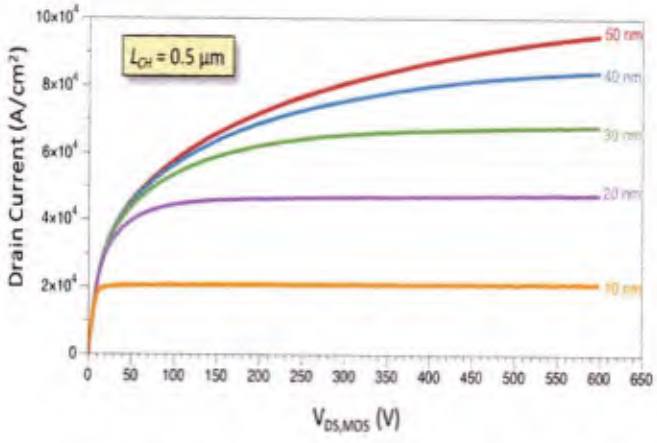


Figure 71. I-V characteristics of a 1,200 V trench MOSFET from 2D simulations. Gate voltage is adjusted to keep the oxide field at 4 MV/cm for all curves. The output conductance arising from DIBL is reduced for the thin-oxide devices. At V_{DS} = 600 V the saturation current decreases by 4.7× as oxide thickness is reduced from 50 to 10 nm. This increases the SCWT by approximately 4.7×, while the slope of the characteristics near the origin (the specific on-resistance) is unchanged.

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3. Financial Report

We have operated for the past year under a 12-month no-cost extension (NCE) with an end date of July 16, 2019. In late 2018 we were awarded a three-year cooperative agreement under the 2018 ARPA-E OPEN FOA to continue development of the tri-gate MOSFET and IMOSFET. Although the start date for the ARPA-E grant is June 2019, we are allowed to charge for work up to 90 days prior to the start date. In April 2019 we reduced our senior salary charges to the ARL NCE, and from May1 through July 16 we shifted three of our four graduate students, their associated lab and outside processing charges, and 75% of our senior salary charges to our new ARPA-E cooperative agreement. This left a graduate student working on waffle-substrate IGBTs and 25% of the original senior salaries on the ARL NCE. With these adjustments we were able to continue supporting this project through the July 16 end date.

The table below shows the total grant amount of $3,029,346.86, a projection of the amount expended by the end of the project on July 16, 2019 ($3,023,145.92), and projection of the remaining unspent balance ($6,201.43). The next page lists the expense categories underlying this projection (valid as of August 27, 2019). The column labeled Cost-Share on the next page captures senior salary expenses in April 2019 that were not charged to this grant.

It is important to note that **the books have not yet been closed**, since we have not received final invoices from our subcontractor Purdue University. Purdue lab charges for a given month are not included in the Purdue invoice to Sonrisa until the following month. Hence, lab charges for July are included in the August invoice to Sonrisa, which is submitted by the second week in September. In addition, final salary charges for Prof. Dallas Morisette will not be available until early October. The summaries on these pages therefore represent **projections** of our financial position as of the end of the NCE on July 16, 2019, based on **estimates** of lab and salary charges from Purdue. If any unspent balance remains after the final invoice is submitted by Purdue, we will shift some or all of the senior salary cost-share from April 2019 to the FEDERAL column so as to reduce the unspent balance to zero.

TOTAL PER GRANT AWARD	3,029,346.86	
TOTAL EXPENDED	3,023,145.92	
Difference	6,200.94	
PER NCE REMAINING	6,201.43	
	(0.49)	ROUNDING

Sonrisa Research Inc.
Statement of Activities by Class
ARL 2015-2019

	FEDERAL	COST-SHARE	TOTAL
Income			
4000 Grant Income	3,023,145.92		3,023,145.92
4200 Cost Share Match - In-Kind		11,336.87	11,336.87
Total Income	$ 3,023,145.92	$ 11,336.87	$ 3,034,482.79
Gross Profit	$ 3,023,145.92	$ 11,336.87	$ 3,034,482.79
Expenses			
5000 Salary & Wages	265,189.02	7,388.97	272,577.99
5050 Payroll Expenditures			0.00
5200 Travel	26,561.78		26,561.78
5300 Materials & Supplies			0.00
5325 Wafers -SiC	81,444.15		81,444.15
5350 Photomasks	22,421.02		22,421.02
Total 5300 Materials & Supplies	$ 103,865.17	$ 0.00	$ 103,865.17
5400 Contractual Costs			0.00
5405 Salary - Faculty	452,992.50		452,992.50
5410 Fringe - Faculty	128,386.08		128,386.08
5415 Salaries - Students	348,252.85		348,252.85
5420 Fringe - Students	21,266.26		21,266.26
5425 Student Fee Remissions	150,322.67		150,322.67
5430 Supplies - Student	257,115.77		257,115.77
5435 Travel, Domestic	18,177.99		18,177.99
5440 Indirect Cost - 55% PU	725,329.49		725,329.49
5445 Equipment - Scientific PU	177,906.96		177,906.96
Total 5400 Contractual Costs	$ 2,279,750.57	$ 0.00	$ 2,279,750.57
5450 Consultant Services - G4 LLC	34,000.00		34,000.00
5500 Processing Services			0.00
5510 Hot-Stage Ion Implantation	55,510.24		55,510.24
5540 Wafer Thinning	11,650.00		11,650.00
Total 5500 Processing Services	$ 67,160.24	$ 0.00	$ 67,160.24
6000 G&A Costs			0.00
5100 Fringe Benefits	66,296.72	1,847.24	68,143.96
6050 Salaries-Pres/Treas	59,185.98	1,157.48	60,343.46
6100 Fringe Benefits & Payroll Taxes	40,702.01	943.18	41,645.19
6150 Accounting & Audit Services	66,553.75		66,553.75
6200 Legal Services	2,121.00		2,121.00
6250 Office Expenses	514.82		514.82
6260 Bank Charges	78.86		78.86
6300 Insurance	10,284.00		10,284.00
6400 Filing Fees & Licenses	882.00		882.00
6500 Fines & Penalities			0.00
Total 6000 G&A Costs	$ 246,619.14	$ 3,947.90	$ 250,567.04
6999 Miscelleous Expenditure			0.00
Purchases	0.00		0.00
Total Expenses	$ 3,023,145.92	$ 11,336.87	$ 3,034,482.79
Net Operating Income	$ 0.00	$ 0.00	$ 0.00

Tuesday, Aug 27, 2019 05:30:29 PM GMT-7 - Accrual Basis