ARL-TR-8771 ● AUG 2019

DEVCOM ARMY RESEARCH LABORATORY

Design Comparison of Silicon Carbide (SiC) Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) for Linear-Mode Operation

by Heather O'Brien, Damian Urciuoli, Aderinto Ogunniyi, and Brett Hull

Disclaimers

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

ARL-TR-8771 ● AUG 2019

Design Comparison of Silicon Carbide (SiC) Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) for Linear-Mode Operation

by **Heather O'Brien, Damian Urciuoli, and Aderinto Ogunniyi**
Sensors and Electron Devices Directorate, CCDC Army Research Laboratory

Brett Hull
Wolfspeed, a Cree Company, Research Triangle Park, NC

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
August 2019	Technical Report	January–December 2018

4. TITLE AND SUBTITLE
Design Comparison of Silicon Carbide (SiC) Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) for Linear-Mode Operation

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Heather O'Brien, Damian Urciuoli, Aderinto Ogunniyi, and Brett Hull

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
CCDC Army Research Laboratory
ATTN: FCDD-RLS-DP
2800 Powder Mill Road, Adelphi, MD 20783-1138.

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TR-8771

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
ORCID IDs: Heather O'Brien, 0000-0003-4726-1593; Brett Hull, 0000-0003-0512-7476

14. ABSTRACT
Silicon carbide metal-oxide semiconductor field-effect transistors (MOSFETs) were designed and fabricated for linear-mode applications. The MOSFETs have a chip area of 3.3 × 3.3 mm and a voltage-blocking rating up to 1200 V. The device design parameters, such as channel length, gate oxide thickness, and implantation process, were varied to study the effects on operation in the saturation region. The MOSFETs were evaluated in a pulse circuit at pulse widths ranging from 250 μs to 40 ms. The MOSFETs with the thicker oxide (625 Å) sustained greater pulsed energy dissipation (over 130 J/cm^2) than those with thinner oxide. Results suggest that linear-mode silicon carbide MOSFETs with thick oxide can dissipate five times greater pulsed energy density than their commercial silicon counterparts.

15. SUBJECT TERMS
power MOSFET, power semiconductor switches, silicon carbide, gate oxide, pulsed power

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Heather O'Brien
Unclassified	Unclassified	Unclassified	UU	18	19b. TELEPONE NUMBER (Include area code) 301-394-5545

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

Contents

List of Figures iv

List of Tables iv

Acknowledgment v

1. Introduction 1

2. Device Design 1

3. Evaluations and Results 3

3.1 Circuitry 3

3.2 Results 4

3.3 Discussion 7

4. Conclusion 8

5. References 9

List of Symbols, Abbreviations, and Acronyms 10

Distribution List 11

List of Figures

Fig. 1 One of the 3.3- × 3.3-mm test chips packaged in a TO-247-3. Pins (left to right) are gate, drain, and source..... 2

Fig. 2 On-state curves for the MOSFET fabricated with 1.5-µm channel, 445-Å oxide thickness..... 2

Fig. 3 On-state curves for the MOSFET fabricated with 1.5-µm channel, 625-Å oxide thickness..... 3

Fig. 4 On-state curves for the MOSFET fabricated with 2.0-µm channel, 625-Å oxide thickness, and standard implantation process..... 3

Fig. 5 Simplified schematic of the pulse circuit used for MOSFET evaluation..... 4

Fig. 6 Average survived energy dissipation of 14.0 J at 16.5-ms pulse width for the MOSFET fabricated with 1.5-µm channel and 445-Å oxide.... 5

Fig. 7 Average survived energy dissipation of 15.1 J at 16.5-ms pulse width for the MOSFET fabricated with 1.5-µm channel and 625-Å oxide.... 5

Fig. 8 Average survived energy dissipation of 14.7 J at 16.5-ms pulse width for the MOSFET fabricated with 2.0-µm channel and 625-Å oxide. The waveforms for peak energy dissipation greater than 15 J are shown. 5

Fig. 9 Subsequent failure of MOSFET with 2.0-µm channel when attempting to increase the energy to near 16 J..... 6

Fig. 10 Typical state of the MOSFETs after they were stressed to failure at high-energy density. Extreme local heating appears to originate below the wire bonds on the source contact. 6

Fig. 11 Energy sustained over the 40-ms pulse was 19.4 J. The MOSFET was not stressed to failure at this pulse width. 7

List of Tables

Table 1 Measured pulse energy dissipation for pulse width = 16.5 ms..... 8

Acknowledgment

The authors thank Q Jon Zhang, formerly of Wolfspeed, for the design, processing, and initial measurements of the metal-oxide semiconductor field-effect transistors (MOSFETs).

1. Introduction

In linear-mode applications, transistors are required to operate in the saturation region. Devices may operate in linear mode at appreciable currents for a brief period (100 µs–100 ms) for applications such as current-limited power charging, electronic loads, and transient suppression during soft start. Challenges of functioning in linear mode include staying within semiconductor material thermal limits and optimizing designs to avoid thermal instability and thermal runaway. Most commercial power transistors are optimized for fast switching transitions and low on-state resistance, and thus not designed for operation in the saturation region. The failure mechanism of transistors operated in saturation has been observed as thermal runaway in a hot spot causing localized turn-on and localized shorting. Thermal instability increases with greater device gain and greater deviation in threshold voltage with temperature.[1] Recent design research to optimize linear-mode performance of transistors includes investigation of novel cell layouts[2] and introduction of local gain variation in the active area.[3]

This report describes linear-mode operation for recently developed experimental silicon carbide (SiC) vertical metal-oxide semiconductor field-effect transistors (MOSFETs). The first motivation of the research is to determine whether 4H-SiC material's large bandgap and high thermal conductivity enable SiC devices to sustain greater pulsed energy density than commercial Si devices. The second motivation is to study how different MOSFET design parameters chosen for these SiC devices, such as channel length and oxide thickness, contribute to defining the safe operating area.

2. Device Design

The SiC linear MOSFETs have a chip area of 3.3 × 3.3 mm (active area of 0.068 cm^2) and a voltage-blocking rating up to 1200 V. Two primary design parameters are varied in this research: channel length and oxide thickness. The channel lengths considered are 1.5 µm (with 10.1-µm cell pitch) and 2.0 µm (with 11.1-µm cell pitch). The oxide thicknesses are 445 and 625 Å. The MOSFETs are individually packaged in open TO-247-3 packages (Fig. 1). Each chip was soldered using a eutectic gold–tin preform to contact the drain. The gold-finished gate and source pads on the top side of the chip are connected to the pins of the package by 0.25-mm-diameter aluminum bond wires.

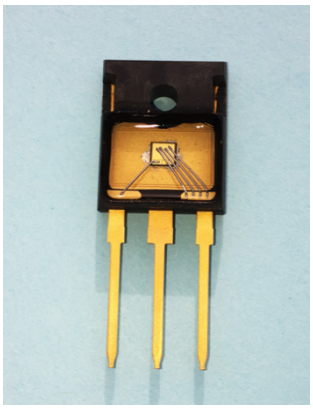

Fig. 1 One of the 3.3- × 3.3-mm test chips packaged in a TO-247-3. Pins (left to right) are gate, drain, and source.

The on-state performance of the packaged MOSFETs was characterized at ambient temperature. Typical drain-to-source voltage (V_{DS}) versus drain-to-source current (I_{DS}) sets of on-state curves are shown in Figs. 2–4 for different fabricated combinations of channel length and oxide thickness. The V_{DS} versus I_{DS} on-state curves for the longer channel and thicker oxide (Fig. 4) imply that drain current amplitude would be more consistent and controllable over a wide range of applied drain voltages, and thus more thermally stable.

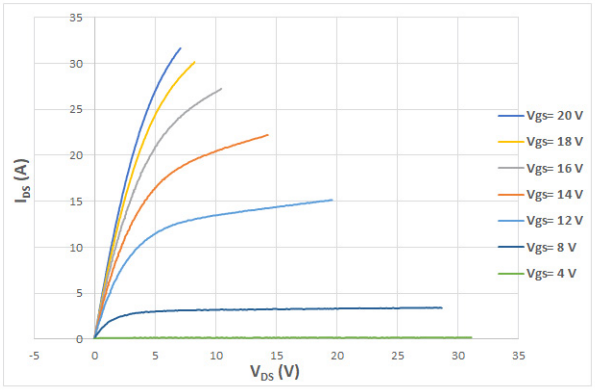

Fig. 2 On-state curves for the MOSFET fabricated with 1.5-µm channel, 445-Å oxide thickness

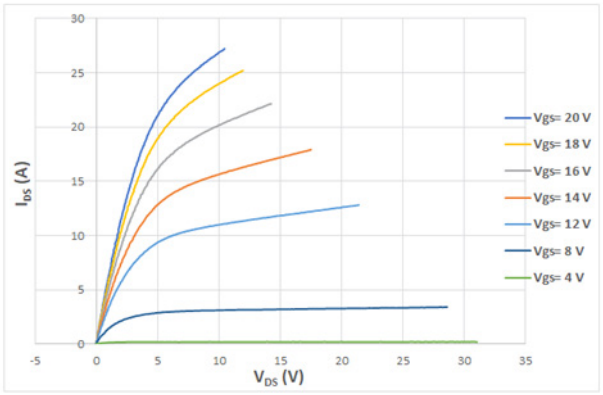

Fig. 3 On-state curves for the MOSFET fabricated with 1.5-µm channel, 625-Å oxide thickness

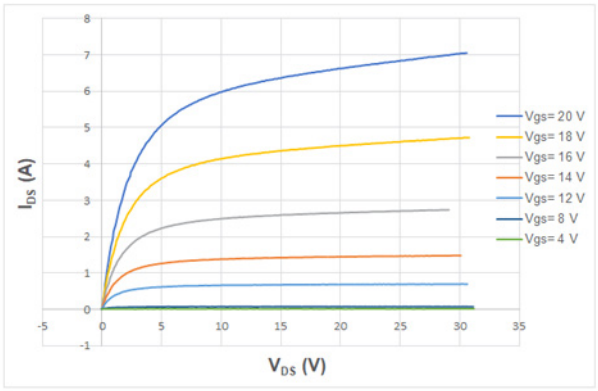

Fig. 4 On-state curves for the MOSFET fabricated with 2.0-µm channel, 625-Å oxide thickness, and standard implantation process

3. Evaluations and Results

3.1 Circuitry

The pulsed evaluation circuit is a capacitor-based discharge circuit in which the MOSFET sees full capacitor voltage and current when it is switched (Fig. 5). Several capacitors are paralleled to provide a total capacitance of 8000 µF. Each MOSFET was switched for a selected current amplitude at gradually increasing total pulsed energy until failure. The pulse widths ranged from 250 µs to 40 ms. The majority of switching was at a pulse width of 16.5 ms. The initial capacitor voltage ranged from 20 to 200 V.

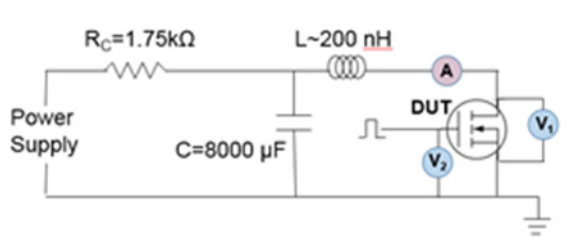

Fig. 5 Simplified schematic of the pulse circuit used for MOSFET evaluation

The gate driver for the MOSFET incorporates feedback control to continuously monitor and regulate the drain current through the MOSFET. This control scheme maintains the amplitude of the pulsed current even as the charge on the capacitor bank falls.[4]

3.2 Results

The maximum survivable single pulse energy for each MOSFET design was evaluated at a pulse width of 16.5 ms and a current amplitude of approximately 8.5 A (125 A/cm^2 over the active area) (Figs. 6–8). The drain-source voltage was gradually increased for each individual pulse, increasing overall pulsed energy, until the MOSFET failed. Catastrophic failure occurred late in the pulse, as shown in Figs. 9–10. Failure appeared to originate beneath the source wire bonds, where current density and temperature would be highest.[5] A few MOSFETs were also switched at lower (4.9 A) or higher (15.5 A) current amplitude at the same pulse width, and they also failed at approximately the same total dissipated energy. The 1.5-µm channel MOSFETs with the oxide thickness of 445 Å survived an average of 14.0 J, and the devices with 625 Å oxide survived an average of 15.1 J. All devices failed during subsequent pulses at slightly higher dissipated energy. For this channel length, the MOSFETs with 40% thicker oxide withstood at least 8% greater energy dissipation. The hypothesis is that the greater oxide thickness provides additional heat capacity at the surface of the device. These results support an argument for greater research in the area of thicker oxide or new oxide materials for high-power and high-temperature semiconductors.

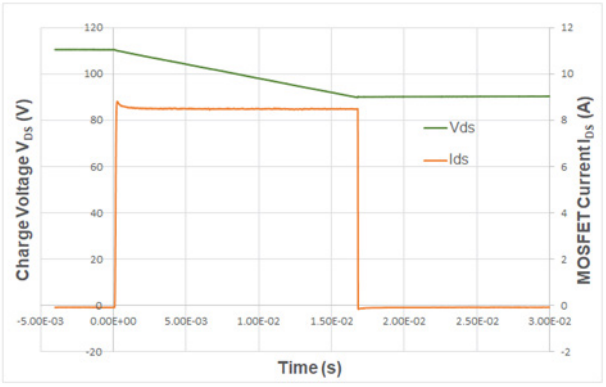

Fig. 6 Average survived energy dissipation of 14.0 J at 16.5-ms pulse width for the MOSFET fabricated with 1.5-µm channel and 445-Å oxide

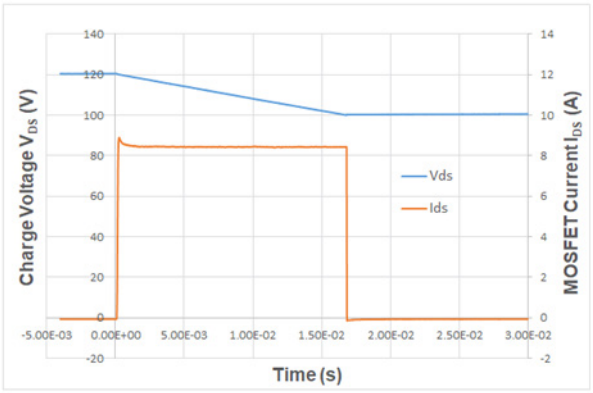

Fig. 7 Average survived energy dissipation of 15.1 J at 16.5-ms pulse width for the MOSFET fabricated with 1.5-µm channel and 625-Å oxide

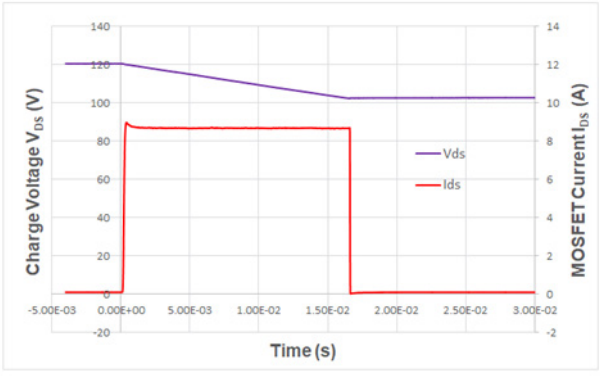

Fig. 8 Average survived energy dissipation of 14.7 J at 16.5-ms pulse width for the MOSFET fabricated with 2.0-µm channel and 625-Å oxide. The waveforms for peak energy dissipation greater than 15 J are shown.

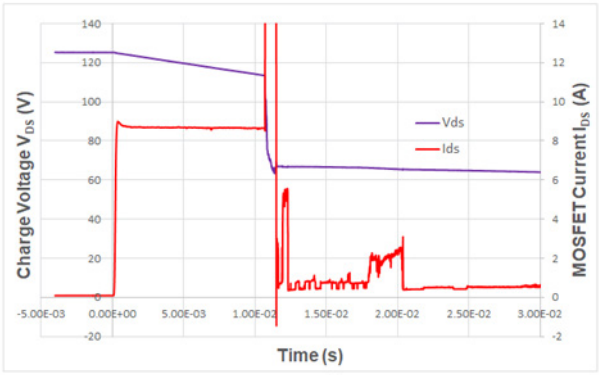

Fig. 9 Subsequent failure of MOSFET with 2.0-µm channel when attempting to increase the energy to near 16 J

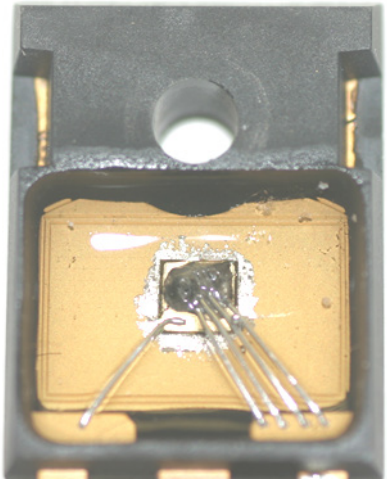

Fig. 10 Typical state of the MOSFETs after they were stressed to failure at high-energy density. Extreme local heating appears to originate below the wire bonds on the source contact.

The 2.0-µm channel MOSFETs with the oxide thickness of 625 Å survived an average of 14.7 J (Fig. 8), similar to the results of the thick oxide, 1.5-µm channel MOSFETs. The similarity in pulse energy between these two designs suggests that increasing the channel length from 1.5 to 2.0 µm did not affect the sustainable pulse energy at this time scale, though the longer channel was expected to be more thermally stable. Longer-channel MOSFETs fabricated with the thinner oxide were not available for evaluation to further substantiate how much oxide thickness enables energy dissipation.

The 2.0-µm channel, 625-Å oxide MOSFETs were additionally switched at increasing pulse width out to 40 ms (Fig. 11). The corresponding energy dissipated over the 40-ms pulse was 19.4 J. The MOSFET was not stressed to failure at this pulse width. The power supply and capacitance of the circuit need to be modified

to support full voltage and current at wider pulse widths. With the present pulse circuit configuration, the dissipated power at the front end of the pulse is significantly higher than the power at t = 40 ms.

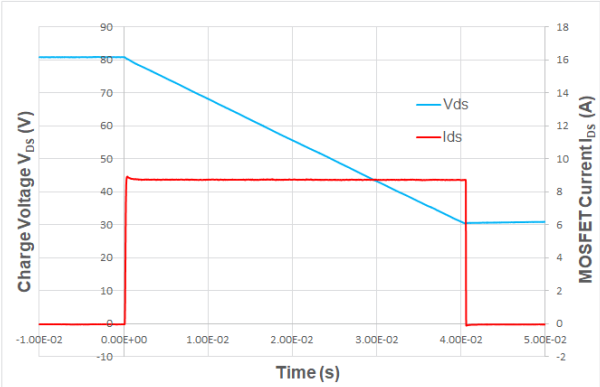

Fig. 11 Energy sustained over the 40-ms pulse was 19.4 J. The MOSFET was not stressed to failure at this pulse width.

3.3 Discussion

The saturation current, I_{Dsat}, of a MOSFET can be described by Eq. 1, where Z is the channel width, μ_n is the effective electron mobility, C_o is the oxide capacitance, L is the channel length, V_G is the gate voltage, and V_T is the threshold voltage.[6]

$$I_{Dsat} = \frac{Z\mu_n C_o}{2L}(V_G - V_T)^2 \quad . \qquad (1)$$

The SiC linear-mode MOSFETs were designed with relatively large channel lengths (>1 µm) in order to increase the on-resistance and minimize the change in I_{Dsat} over the full range of drain-source voltages.[7] Thick oxide was grown to enable finer control of the drain current amplitude, while also increasing thermal capacitance at the surface of the device.

Evaluations of sustainable pulsed energy were also conducted with larger, low-drain-to-source resistance (R_{DS}) SiC MOSFETs and commercially available Si linear-mode MOSFETs. Relative to the low-resistance SiC power MOSFETs (chip area of 31.65 mm^2), which survived 85 J/cm^2, the thick-oxide SiC linear-mode MOSFETs survived 138 J/cm^2. The thick-oxide SiC MOSFETs also survived greater than five times the energy density of the commercially available Si linear-mode MOSFETs (IXTX22N100L and APL502) evaluated under the same 16.5-ms pulsed conditions (Table 1).

Table 1 Measured pulse energy dissipation for pulse width = 16.5 ms

Device	Chip area (cm^2)	Average survivable pulse energy (J)	Specific energy (J/cm^2)
New SiC MOSFET with thick oxide	0.1089	15.1	138
New SiC MOSFET with standard oxide	0.1089	14.0	128.5
Low-R_{DS} SiC MOSFET	0.3165	27	85
Si APL 502	1.41	>34.2[a]	>24.3
Si IXTX22N100L	1.305	19.9	15.2

[a] This device did not fail at energy up to 34.2 J.

4. Conclusion

The conclusion of this research is that the oxide thickness had greater effect on the linear MOSFET's survivable pulsed energy than did the range of fabricated channel lengths. Increasing oxide thickness by 40% resulted in greater than 8% higher pulsed energy dissipated without failure at a pulse width of 16.5 ms. At extreme pulsed energy, the MOSFET's failure appeared in the area of the source pad below the wire bonds. Future work will include investigating an alternative method of source contact to better spread the current and transfer the heat at the top side of the chip.

5. References

1. Dodge J. How to make linear mode work. Bend (OR): Microsemi Corporation; n.d. [accessed 2019 Aug 19]. https://www.digikey.com/en/pdf/m/microsemi-power-products-group/microsemi-make-linear-mode-work.

2. Su Y, Bobde M, Lui S, Chang H, Jin Q, Zhang L. A comparison of close-cell, stripe-cell, and orthogonal-cell low voltage superjunction trench power MOSFETs for linear mode application. Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD); 2018 May 13–17; Chicago, IL. p. 327–330.

3. Chang M-H, Rutter P. Optimizing the trade-off between the RDS(on) of power MOSFETs and linear mode performance by local modification of MOSFET gain. Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD); 2016 June 12–16; Prague, Czech Republic. p. 379–382.

4. O'Brien H, Ogunniyi A, Urciuoli D, Zhang QJ, Hull B. SiC MOSFETs designed and evaluated for linear mode operation. Proceedings of the 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA); 2017 Oct 30–Nov 1; Albuquerque, NM. p. 153–157.

5. Van Brunt E, Barbieri T, Barkley A, Solovey J, Richmond J, Hull B. Surge current failure mechanisms in 4H-SiC JBS rectifiers. Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD); 2018 May 13–17; Chicago, IL. p. 415–418.

6. Pierret RF. Field effect devices, modular series on solid state devices. Reading (MA): Addison-Wesley; 1990. Vol. 4.

7. Chen W-K, editor. The electrical engineering handbook. Burlington (MA): Elsevier; 2005.

List of Symbols, Abbreviations, and Acronyms

ARL	Army Research Laboratory
CCDC	US Army Combat Capabilities Development Command
I_{DS}	drain-to-source current
MOSFET	metal–oxide–semiconductor field-effect transistor
R_{DS}	drain-to-source resistance
SiC	silicon carbide
V_{DS}	drain-to-source voltage

1 (PDF)	DEFENSE TECHNICAL INFORMATION CTR DTIC OCA
1 (PDF)	CCDC ARL FCDD RLD CL TECH LIB
1 (PDF)	GOVT PRINTG OFC A MALHOTRA
3 (PDF)	CCDC ARL FCDD RLS DP H O'BRIEN A OGUNNIYI D URCIUOLI