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DIGITAL LOGIC GATE CHARACTERIZATION WITH GALLIUM NITRIDE TRANSISTOR

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14. ABSTRACT
This thesis presents work on the development of digital logic gates using Gallium Nitride (GaN) transistors in a 0.25µm process. The allowed minimum width of 12 µm is reduced to 5 µm in order to observe scalability and to measure the performance benets of smaller device sizes in the GaN process. Due to poor modeling, the designed Buffered FET Logic INV, NOR2, and NAND2 are designed for functionality over performance, resulting from the risk of failure without proper simulations. A preliminary test plan was developed and executed to prove the functionality of the devices across varying temperatures, voltages, and input frequencies, with initial tests indicating that the devices are fully functional across these parameters.

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Digital Logic Gate Characterization with Gallium Nitride Transistors

A Thesis

Presented in Partial Fulfillment of the Requirements for the Degree Master of Science in the Graduate School of The Ohio State University

By

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2019

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Abstract

This thesis presents work on the development of digital logic gates using Gallium Nitride (GaN) transistors in a 0.25μm process. The allowed minimum width of 12 μm is reduced to 5 μm in order to observe scalability and to measure the performance benefits of smaller device sizes in the GaN process. Due to poor modeling, the designed Buffered FET Logic INV, NOR2, and NAND2 are designed for functionality over performance, resulting from the risk of failure without proper simulations. A preliminary test plan was developed and executed to prove the functionality of the devices across varying temperatures, voltages, and input frequencies, with initial tests indicating that the devices are fully functional across these parameters.

This thesis is dedicated to my mom whose encouragement and support made this all possible.

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Chapter 1: Introduction

Gallium Nitride (GaN) processes present several improvements in both RF and analog design spaces, compared to Silicon (Si) process nodes. This includes higher operating temperatures and higher power densities made possible by the larger bandgap [7], [23],[13]. As shown in Figure 1.1, the increase in bandgap stretches from 1.1eV to 3.4eV. Despite the improvements that GaN technology offers in the analog and RF design spaces, Si processes still comprise the majority of digital circuits that are developed due to their already prolific presence, large volume capabilities, and process maturity.

In Radio Frequency (RF) systems which use GaN technologies, added design complexity, such as the addition of buffers/drivers for the logic levels, is required in order to interface with traditional digital blocks (I2C, SPI). This is apparent in reconfigurable analog circuits, which require digital control, as shown in Figure 1.2. In this figure, switch capacitors are enabled to modulate the gain of the amplifier.

Furthermore, keeping up with Moore's Law has forced scalability to be paramount in the advancement of digital integrated circuits (ICs), made evident by the constant development of Si processes [6]. Unfortunately, Si is approaching the theoretical limit as sub 10 nm are developed, driving a need for alternative technologies [6].

The added design complexity that Si interfaces require, as well as the need to advance GaN technologies, is paving the way for rapidly expanding research on digital

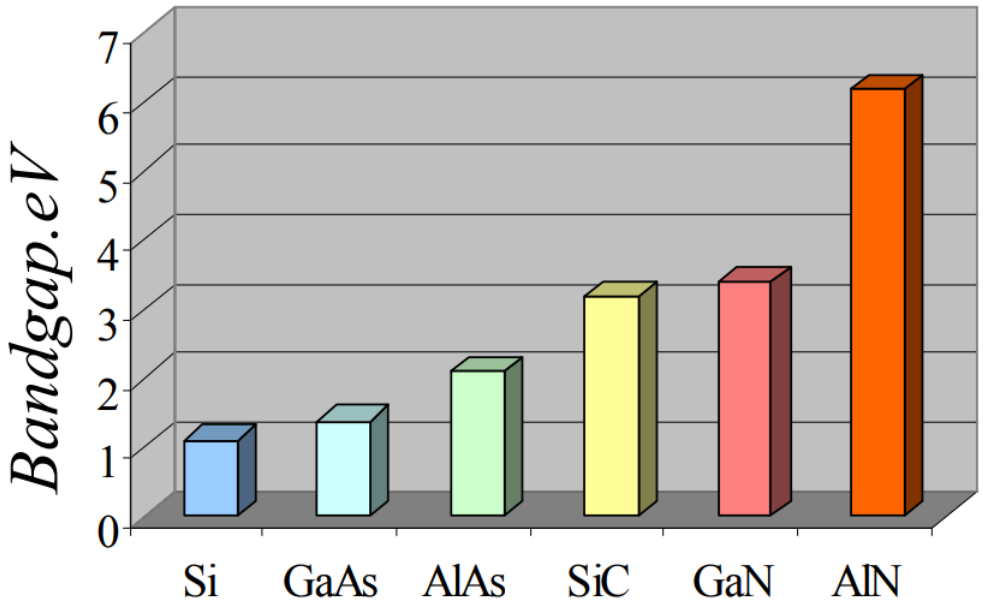

Figure 1.1: Bandgap of Semiconductor Materials [7]

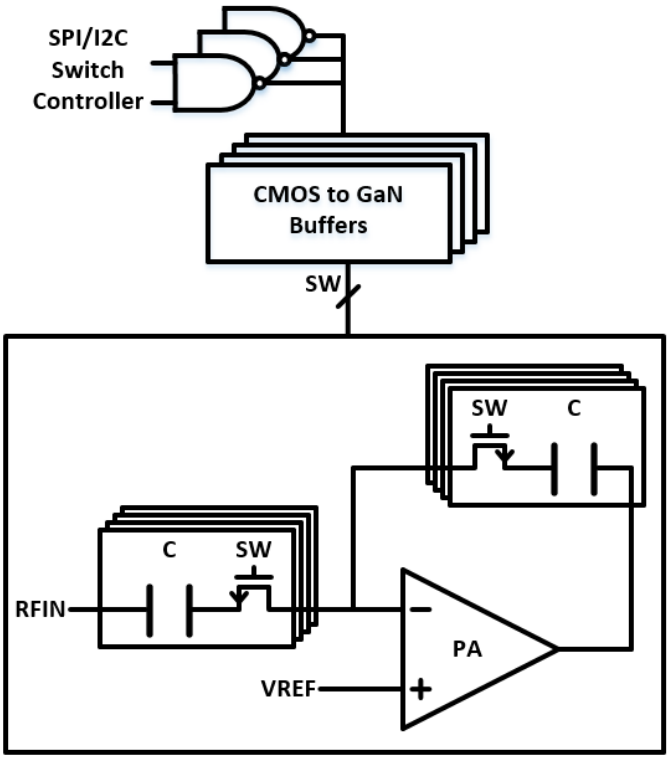

Figure 1.2: Demonstration of Variable Gain Control Requiring GaN Drivers

2

GaN circuits. Traditiona-channelMOS logic circuits are fabricated using enhancement P-channel and N-channel devices; however, the GaN technologies consist of only N-channel depletion mode transistors and lack P-channel devices, caused by the poor hole mobility inherent to GaN. Development of digital logic gates with GaN is constrained by these device limitations. Unbuffered FET Logic (UFL), Schottky Diode FET Logic (SDFL), Capacitor Diode FET Logic (CDFL), and Buffered FET Logic (BFL) are the presented depletion only N-channel logic families.

1.1 Past Advancements in N-channel Logic

In the 1980s, GaAs N-channel logic was in tight contest with Si CMOS processes for position as the dominate logic family in terms of scalability and performance. There was expansive research on both enhancement/depletion (E/D) mode and depletion only N-channel logic families, all of which were designed using Gallium Arsenide (GaAs) MESFET devices [1],[15],[22],[4],[3],[24],[9]. The availability of operational enhancement devices naturally caused more emphasis to be placed on the E/D mode logic variants, but there still are reported cases of depletion only logic variants. From that era, GaAs SDFL [4],[3], CDFL, [9], and BFL [19] families were all implemented and proven to be both operational and viable options for LSI design. Present day reports of depletion only GaN logic, however, are in short supply due to the developing interest in its future capabilities [5]. Table 1.1 details the performance metrics of logic families from past GaAs and present GaN structures. The results presented in this thesis are highlighted in blue. For comparison, the capacitive loading of the pads and interfacing equipment, such as the oscilloscope, result in propagation delays that are magnitudes larger, which is shown in Table 1.1.

Table 1.1: Depletion Mode Logic Family Metrics

Logic Family	V_{DD}/V_{SS}	GND	Logic	Process	L_{MIN}	T_{PROP}
SDFL [4]	2 V / -1.5 V	0 V	NOR4	GaAs	1 μm	82 ps
CDFL [9]	5 V / NA	0 V	INV	GaAs	1.5 μm	200 ps
BFL [19]	2.5 V / $\sim$-1.5	0 V	IN	GaAs	N/A	N/A
BFL [5]	0 V / -12 V	-6 V	Ring Osc	GaN	1 mm	172 ps
BFL (Presented)	12 V / -4 V	0 V	INV NOR2 NAND2	GaN	0.25 μm	172 ns

* The decoupling capacitors on the needle probes, as well as the capacitive loading from the test equipment limited the measurement capabilities.

1.2 Organization of Thesis

This thesis covers three primary categories:

1. GaN Device Characterization

2. Operation of CMOS and depletion N-Channel Logic Families

3. Design and Test of Digital Gates using 0.25μm Process

Chapter 2 discusses the development of the GaN HEMT used for the N-channel logic families, as well as the history of N-channel logic families. Chapter 3 focuses on the operation of the proposed depletion only N-channel logic families. Chapter 4 details the design process and decisions for the Buffered FET Logic gates that are designed in the GaN technology. Chapter 5 covers the testing procedures and results of the implemented BFL logic structures. Chapter 6 details the future work and concludes the analysis.

Chapter 2: Background

2.1 Development of GaN HEMT/ pHEMT Device Structures

Over the past few decades, there is increasing demand for high performance microwave transistors resulting from ever increasing data rates and broadband wireless internet connections [14]. It is well established that the increased electron mobility, bandgap, and large breakdown voltages in GaN and GaAs technologies (Figure 2.2) make them prime candidates for applications which require high power, wide bandwidth, high efficiency, and high linearity [20].

Presented in 1979, the HEMT device was conceived while working towards high speed GaAs MESFETs [12]. The HEMT device structures are formed by creating a heterojunction with a highly doped material on the substrate and an undoped material underneath the device passivation, as shown in Figure 2.1. Since different materials have different band gaps, the valence band and conduction bands at the heterojunction interface of the HEMT bend to a continuous level. Ideally, the heterojunction formed in HEMTs would share the same lattice constant between the two materials; however, this is not the case. The BFL gates are designed using GaN pHEMT devices which account for the deep traps within the material by limiting the

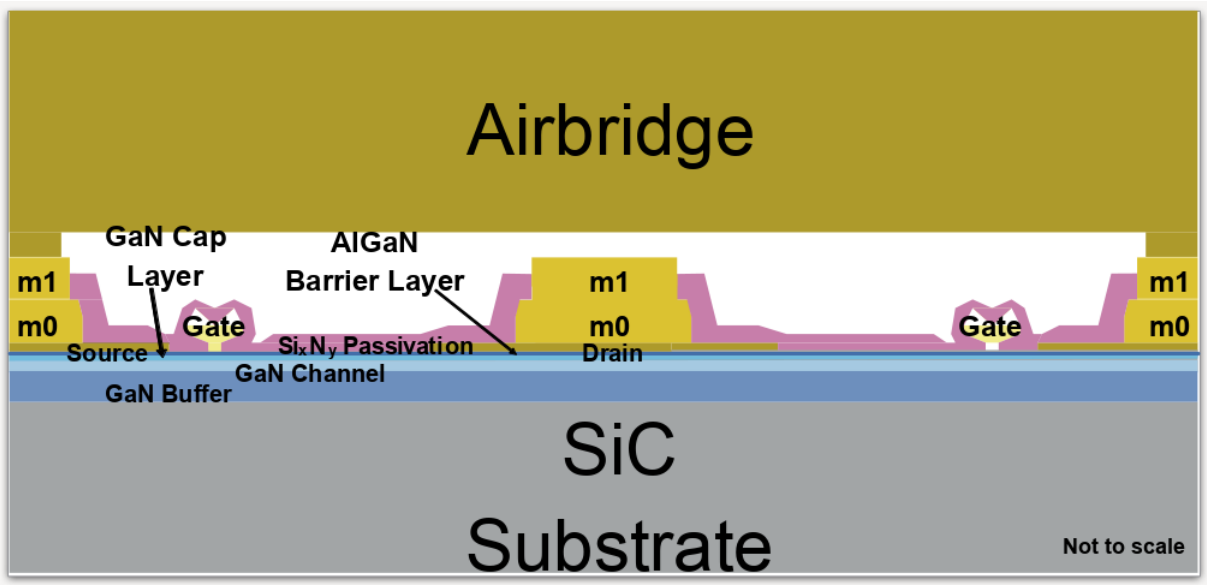

Figure 2.1: GaN Process pHEMT Topology

Material	Mobility, μ, $cm^2/V.s$	Dielectric Constant, ε	Bandgap, Eg, eV	Break down field, Eb $10^6 V/cm$	BFOM Ratio	Tmax, ^OC
Si	1300	11.9	1.12	0.3	1.0	300
GaAs	5000	12.5	1.42	0.4	9.6	300
4H-SiC	260	10	3.2	3.5	3.1	600
GaN	1500	9.5	3.4	2	24.6	700

Figure 2.2: Baliga Figure of Merit (BFOM) for Transistor Performance [18]

thickness of the AlGaN layer, allowing the crystal lattice structure to stretch. This provides a larger bandgap and effectively improves performance [17],[13],[16].

As previously mentioned, GaN pHEMT device structures are key in high frequency and large gain applications. The benefits of these devices drive a need to incorporate digital reconfigurability and to mature the digital GaN logic gates for both RF/analog and digital device integration.

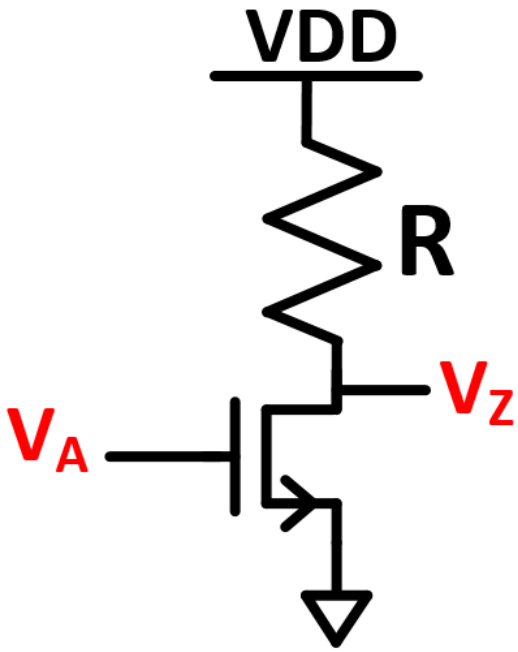

Figure 2.3: N-Channel Only Inverter with Pull Up Resistor

2.2 Digital Logic Development and Classification for GaN Transistors

Complementary logic is unavailable in the GaN process due to the complexity of designing and maturing P-channel and enhancement mode devices [21],[26],[8],[2]. Thus, forward development is limited to the design and implementation of N-channel only logic families for GaN technologies.

2.2.1 N-Channel Logic Family

The simplest form of N-channel logic is comprised of a strong pull up network, often loaded by a resistor. Figure 2.3 is a simple N-channel inverter with resistance R as the pull up resistance. The weak pull down of the inverter is due to the voltage divider created between the load resistance and N-channel device. If we assume the input transistor is turned on when input V_A is logic high, a path to ground is created.

This causes the output node, V_Z, to pull low. The output node voltage is determined by a voltage divider with resistive load R and the on-resistance, R_{ON}, of the transistor, as described in equation 2.1.

$$V_Z = V_{DD}(\frac{R_{ON}}{R + R_{ON}}) \tag{2.1}$$

When V_A is pulled low, the input transistor turns off, and V_Z is pulled high as set by equation 2.2. Because no current flows into the gate of the next stage, V_Z pulls high to V_{DD}.

$$V_Z = V_{DD} \tag{2.2}$$

The pull up and pull down speeds are drastically different since the R_{ON} of the transistor is substantially smaller than the pull up resistor.

In practice, the load resistance requires large area and therefore is inefficient for VLSI design. More practical N-channel logic families are available, and the following chapter details the alternative depletion only N-channel families presented in the following list:

- 1: Schottky Diode FET Logic (SDFL)
- 2: Unbuffered FET Logic (UFL)
- 3: Capacitor Diode FET Logic (CDFL)
- 4: Buffered FET Logic (BFL)

Chapter 3: N-channel Logic Families

Because there are no enhancement mode GaN transistors in the available processes, four depletion mode N-channel families are analyzed [25],[11]. These families are known for large voltage swings, increased noise margins, large power consumption, and added complexity from dual power supplies [24]. Due to the HEMT device structure, there is also a limitation due to the schottky diodes of the transistors. This limiting voltage, specified as V_{DROP} in Table 3.1, limits the output range and is used as a boundary condition for the logic swing. Table 3.1 details the relevant logic parameters used to characterize the logic families of the following subsections.

Table 3.1: Logic Parameters for N-channel Logic Families

V_T	Threshold Voltage
V_H	Logic High Input
V_L	Logic Low Input
V_{DIODES}	Voltage Drop Across Level Shifting Diodes
V_{DROP}	Schottky Diode Forward Bias Voltage

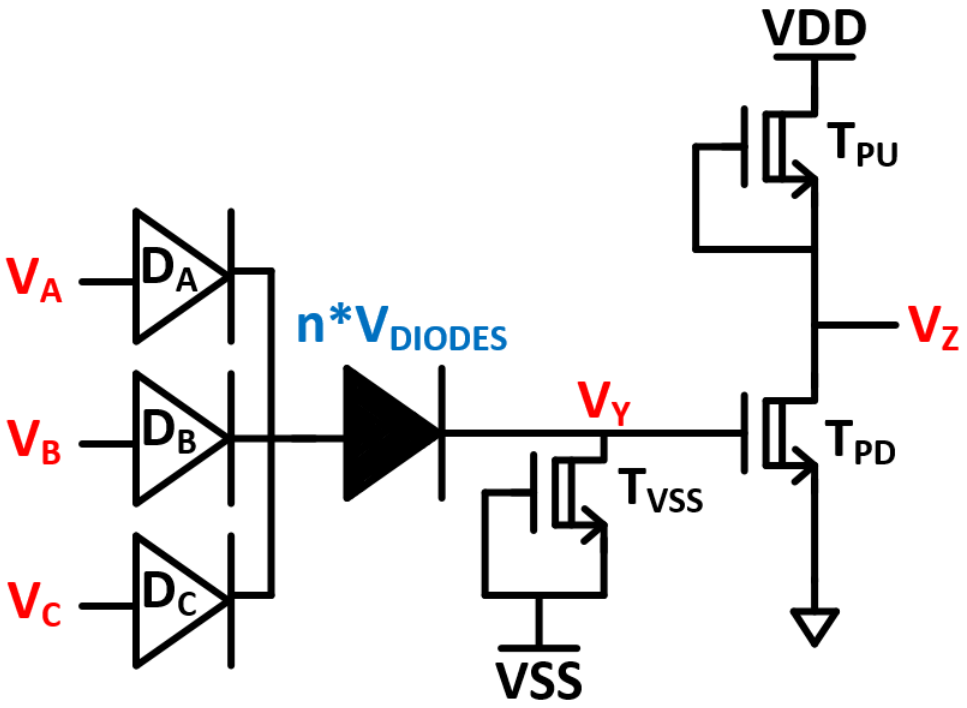

Figure 3.1: SDFL NOR3 Logic Gate

3.1 Schottky Diode FET Logic

SDFL logic gates use schottky diodes not only for level shifting, but also as the switching elements to form the gate. In comparison to transistors, the diodes have low capacitance, low series resistance, and there are no minority carrier charge storage issues caused by the pn junctions in FETs [10]. The primary benefit of the SDFL structure is the reduced area from the schottky diodes. Figure 3.1 demonstrates a NOR3 gate implemented with SDFL logic. The pull down and pull up output transistors, respectively labeled as T_{PD} and T_{PU}, serve as an inverter to restore the output to the proper logic high and logic low levels.

Before illustrating the operation of the three input SDFL NOR gate, the boundary conditions for V_L and V_H are set. If we assume that $V_Z = V_H$, then the output level

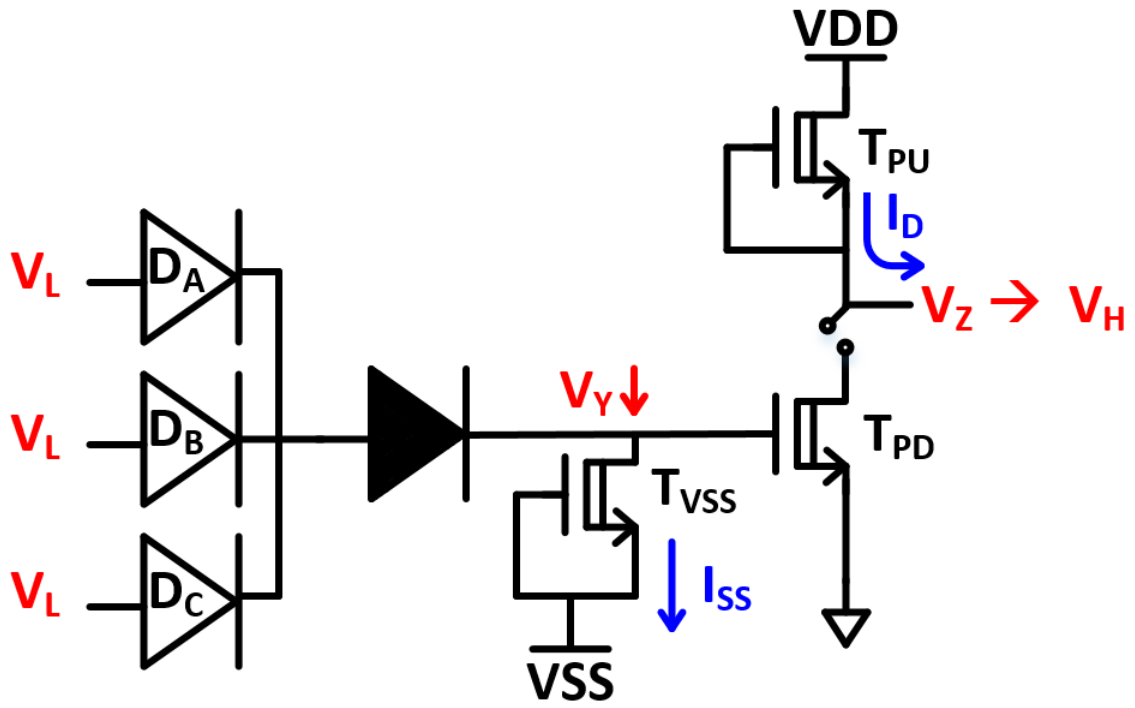

Figure 3.2: SDFL NOR3 Logic Gate with Low Inputs

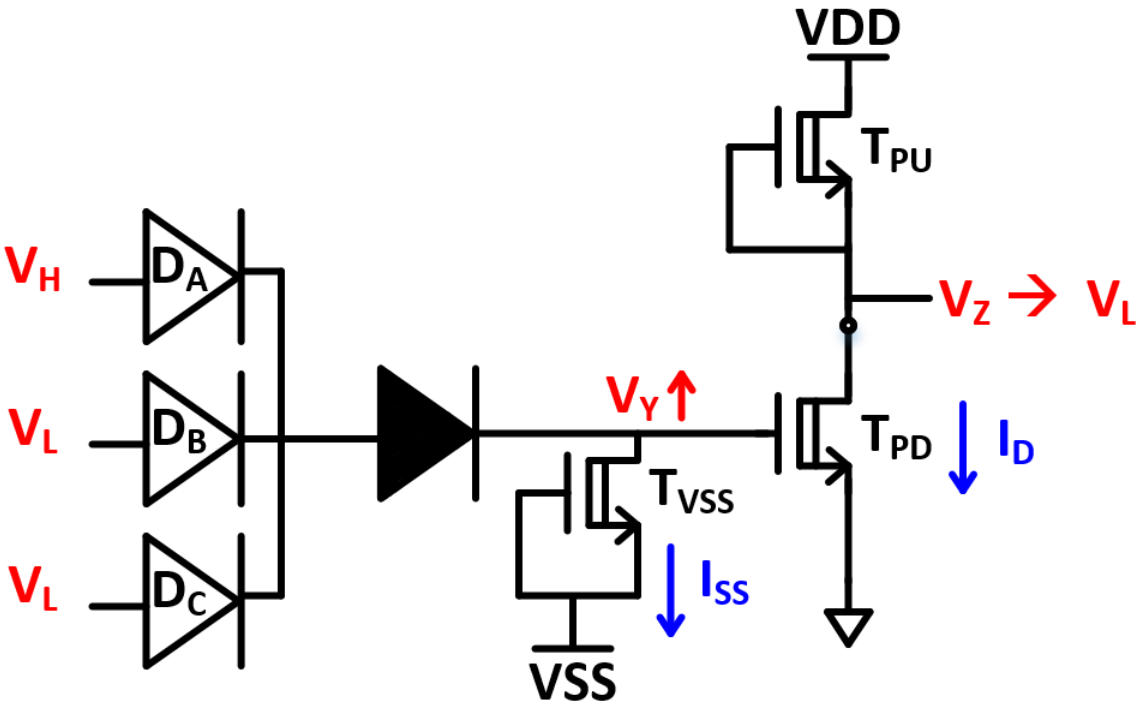

Figure 3.3: SDFL NOR3 Logic Gate with One High Input

is limited by V_{DROP} as seen in equation 3.1. Under the case that $V_Z = V_L$, equation 3.2 constrains the minimum output low value. In the low case, V_Y is also bound by equation 3.3 to guarantee that the drain to gate schottky diode of T_{VSS} is deep reverse biased.

$$V_H < V_{DD} - V_{DROP} \tag{3.1}$$

$$V_L > V_Y + V_{DROP} \tag{3.2}$$

$$V_Y > V_{SS} + V_{DROP} \tag{3.3}$$

Now, assume that the inputs to the diodes D_A, D_B, and D_C are set where (V_A, V_B, V_C) = 000, such as in Figure 3.2. In this case, V_Z rises to V_H, requiring T_{PD} to turn off. T_{PD} is off if the V_{GS} of T_{PD}, which is V_Y, is less than V_T. Based on the logic low inputs, $V_Y = V_L - n \cdot V_{DIODES}$, with equation 3.3 limiting the level of V_Y. The number of level shifts needed are selected to ensure that T_{PD} is turned off during this logical state.

If we assume that the input voltages transition to (V_A, V_B, V_C) = 100, such as in Figure 3.3, then the output voltage V_Z transitions to V_L. This requires T_{PD} to be turned on, creating a path to GND. This occurs once the input to diode D_A is large enough to increase V_Y greater than V_T. At a minimum, equation 3.4 sets V_H to be a magnitude such that $V_Y = V_T$. V_Y' is the previous value when $V_Z = V_L$. In practice, V_H is chosen larger so that T_{PD} is strongly ON with a V_{GS} sufficiently larger than V_T. As a result, equations 3.3, 3.1, and 3.4 are used to determine both V_{DD} and V_{SS}.

$$V_H > (V_T - V_Y') + n \cdot V_{DIODES} \tag{3.4}$$

These boundary conditions indicate that both logic high and logic low both are greater than GND, allowing the inputs and outputs to the logic gates to be positive values. In conclusion, schottky diode logic is considered to be fast and area efficient due to the low capacitance and reduced area of the schottky diodes, but SDFL lacks the drive strength of other N-channel logic families due to the fixed currents from the diode connected transistors [10].

3.2 Unbuffered FET Logic

Of the depletion mode logic families available, UFL logic is lower power and slower when driving large loads, compared to BFL and CDFL logic. As seen in Figure 3.4, a UFL inverter is comprised of T_{PU} as the pull up, T_{PD} as the active pull down, and T_A as the input transistor. The output node V_Z is equal to equation 3.5. Similar to SDFL, equations 3.6, 3.7, 3.8, and 3.9 are the boundary conditions for V_Z and V_X. Equation 3.7 only applies in the case that a logic high is applied at the input transistor T_A.

$$V_Z = V_X - n \cdot V_{DIODES} \tag{3.5}$$

$$V_X < V_{DD} - V_{DROP} \tag{3.6}$$

$$V_X > V_H + V_{DROP} \tag{3.7}$$

$$V_Z > V_{VSS} + V_{DROP} \tag{3.8}$$

$$V_H < V_{DROP} \tag{3.9}$$

In order to illustrate the operation, assume that the input is initialized such that $V_A = V_L$, as shown in Figure 3.5. In this state, T_A turns off, forcing the output V_Z to increase such that $V_Z = V_X - n \cdot V_{DIODES}$, with V_X limited by equation 3.6. Turning off T_A requires that $V_L < V_T$. Because $V_Z = V_H$ and $V_Z = V_X - n \cdot V_{DIODES}$, the level shifting diodes are selected to ensure a V_Z high enough to turn on the next stage of logic. At a minimum, the input to the next stage must exceed V_T such that $V_H > V_T$.

If the input transitions such that $V_A = V_H$, V_Z falls to V_L. The output node is still $V_Z = V_X - n \cdot V_{DIODES}$, but V_X is now equal to a value closer to GND due to transistor T_A turning on, as shown in Figure 3.6. V_X is now bound by equation 3.7, and the magnitude of V_X is set by the drive strength ratio of T_A and T_{PU}. Because V_X is driven towards GND, T_A is sized bigger, relative to T_{PU}, to reduce the magnitude of V_X.

Ultimately, the performance of UFL is bottlenecked by the drive capability [10]. Larger fanouts directly increase the load capacitance in the latter stages, demanding more current to charge the larger load capacitance. This is a problem in UFL logic, since the current drive is set depending on the values of V_{SS} and V_{DD}. Solutions to increase the charge and discharge speeds, and therefore drive capabilities, are proposed in the next two logic families.

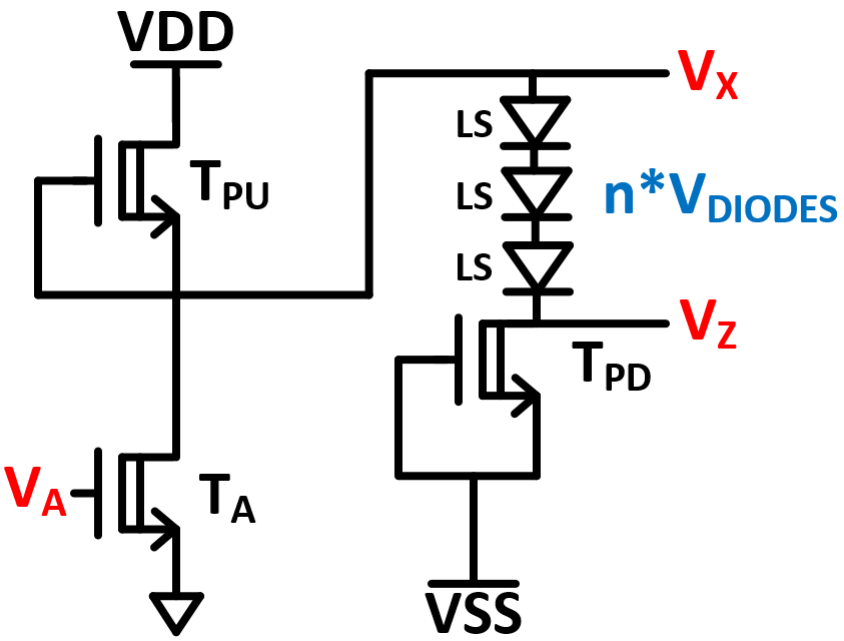

Figure 3.4: UFL INV Logic Gate

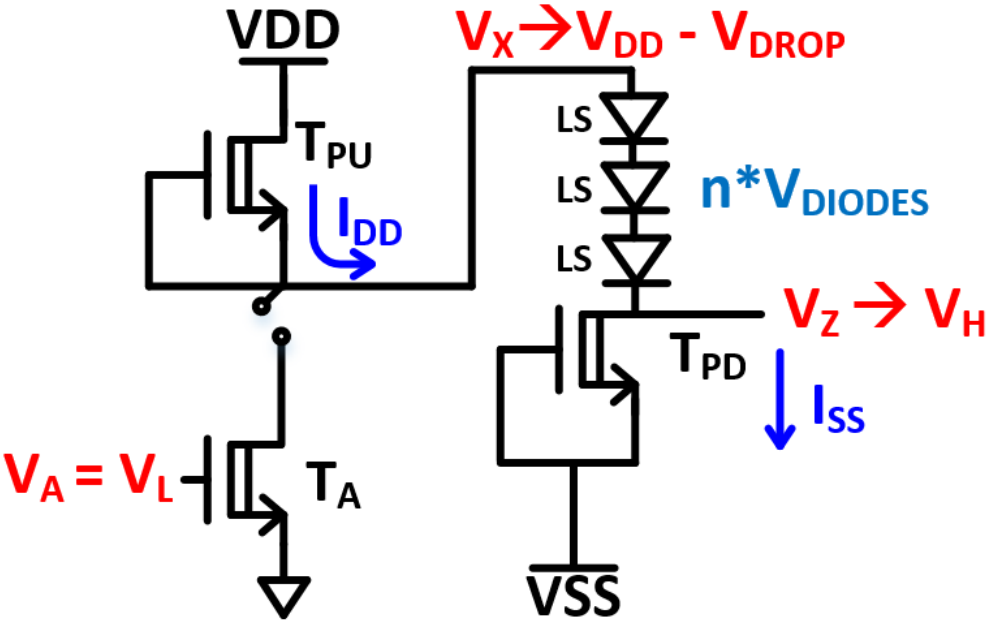

Figure 3.5: UFL INV Gate with $V_A = V_L$

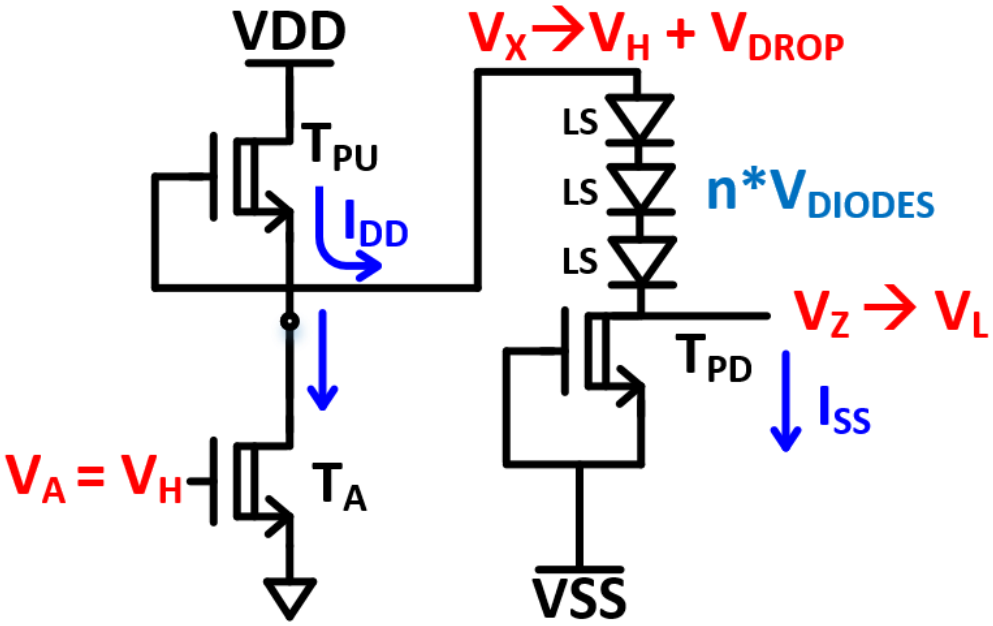

Figure 3.6: UFL INV Gate with $V_A = V_H$

3.3 Capacitor Diode FET Logic

CDFL is an extension of UFL, meaning that the boundary conditions for CDFL logic are the same as in UFL logic. Architecturally, the CDFL family uses the same UFL structure but with a capacitor in parallel with the level shifting diodes. The added capacitor in CDFL is frequently replaced with a reverse biased schottky diode due to process compatibility [9], as shown in Figure 3.7. The benefit of CDFL is apparent primarily when the output node V_Z begins to fall to V_L. In this state, the load capacitance, C_{LOAD}, begins to discharge through T_{PD} and through the additional diode, as seen in Figure 3.8. The added current path allows V_Z to transition from V_H to V_L much faster.

The primary disadvantage to the capacitive feed forward path is that the capacitance from the additional diode must be large relative to the load capacitance of the

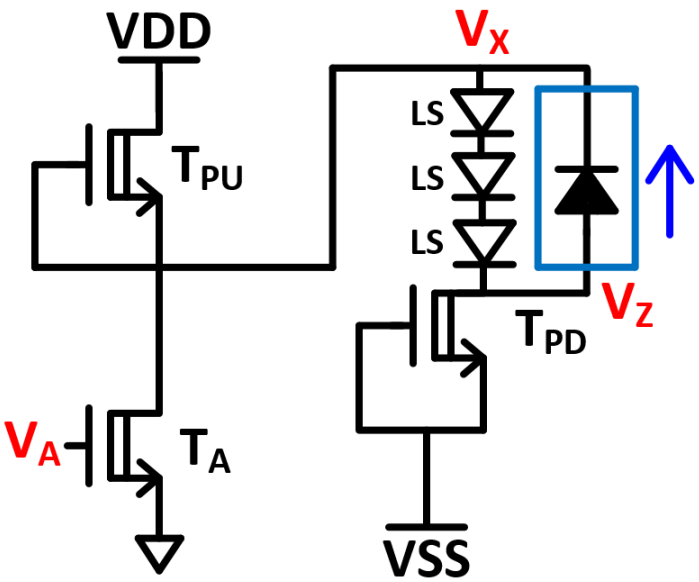

Figure 3.7: CDFL INV Gate with Capacitive Feedforward Reverse Biased Diode

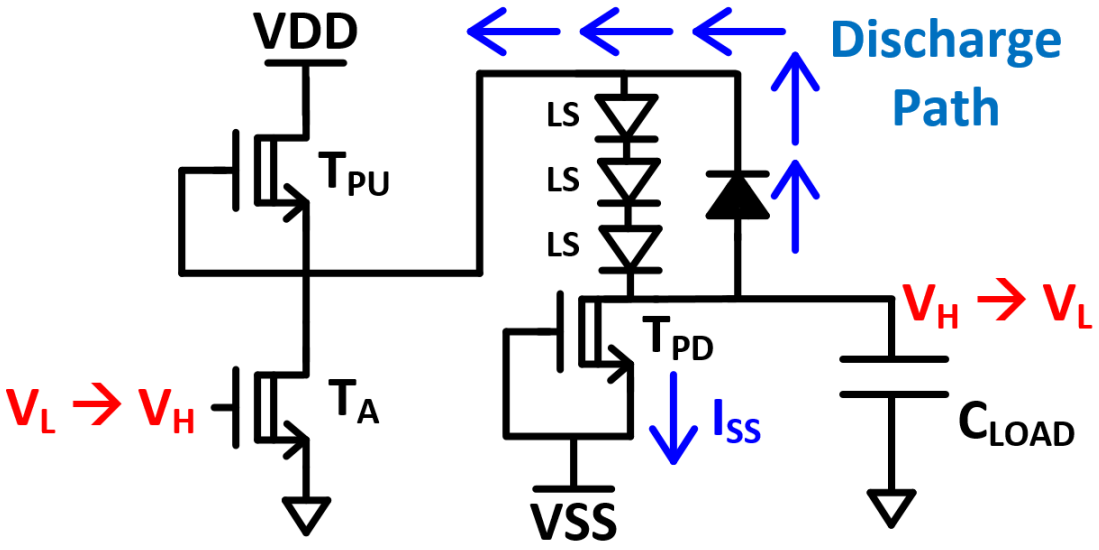

Figure 3.8: CDFL INV Gate with Output Discharge through Feedforward Diode

following stages due to the capacitive voltage divider created at the output node, V_Z. Despite this, the total area of CDFL logic is an overall reduction, compared to SDFL and UFL, due to the coupling from the added feedforward diode, causing CDFL to consume less total power of the presented N-channel logic families [10].

3.4 Buffered FET Logic

Unlike the other proposed logic families, BFL gates account for the reduced drive strength from UFL logic by adding a source follower transistor, as shown in Figure 3.9. The output node V_Z rises quickly due to the large V_{GS} seen at T_{SF} when the input V_A transitions from V_H to V_L. As a result, BFL gates can drive larger loads by increasing the drive strength of T_{SF}. The driving capabilities at V_Z are now set by the large current gain from the T_{SF}, effectively decoupling the drive strength of transistors T_A and T_{PU} from the output. This allows designers to reduce the total area of both T_A and T_{PU} [10]. The current drive of the BFL gate, as a result, depends on the aspect ratio of the source follower transistor. The primary concern would be to select V_{DD} and V_{SS} so that T_{SF} and T_{PD} are both in saturation. The logical operation and analysis of BFL are completed in the subsequent chapter.

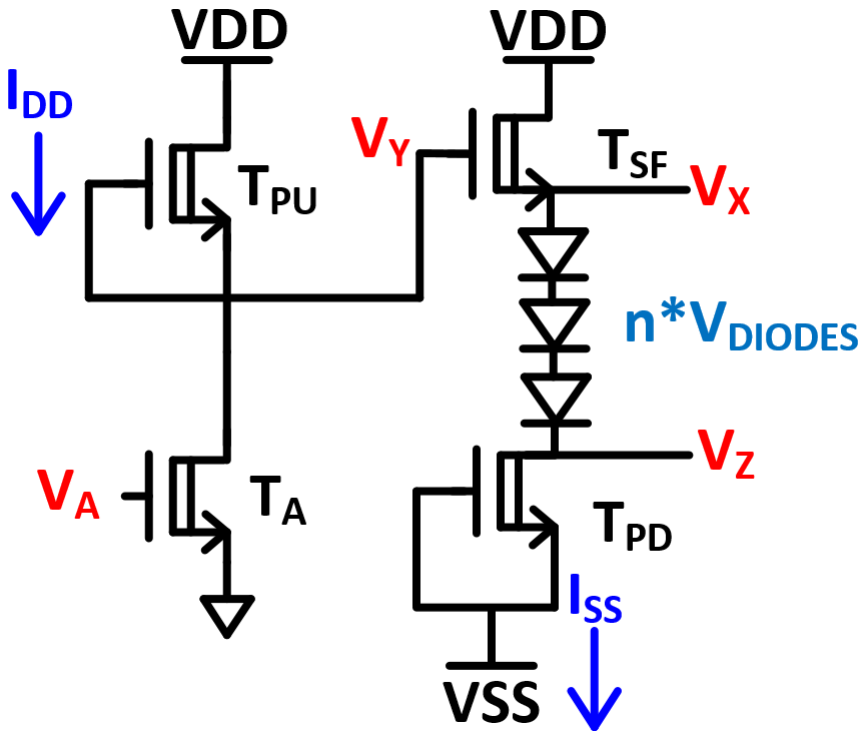

Figure 3.9: BFL INV Gate using Source Follower Buffer

3.5 Performance Tradeoffs

SDFL is fast due to the low capacitance values of the input diodes. It also requires less area than the other families because of the use of diodes at the inputs. CDFL logic consumes the least amount of power because of the compensating feedforward path from the additional diode, and it is a speed improvement on UFL. The increased drive strength from BFL makes it the fastest of all four logic families, while also consuming larger area and naturally more power. Table 3.2 demonstrates these advantages and disadvantages of the four logic families.

Table 3.2: Depletion Mode Logic Family General Comparison

Logic Family	Power / Area	Speed / Fanout
SDFL	Semi-Low / Low	High / High
CDFL	Low / Low	High / Low
UFL	Semi-Low / High	Low / Low
BFL	High / High	High / High

Chapter 4: Design and Implementation

The GaN process used to design the logic gates is a 0.25 μm process with minimum width of 12 μm. The designed logic gates are implemented with a minimum width of 5 μm by modifying the layout of the transistors, despite going against design rules. Because GaN models are typically developed for specific widths and lengths, none are available for the custom sized minimum width of 5 μm. The lack of models also makes predicting the operating characteristics, such as the threshold voltage, difficult as it can vary upwards of 1 Volt in some cases. As a result, the designed logic gates are designed for functionality over performance due to the lack of simulation models. Without these models, general design rules for the chosen logic family can be used to design the gates. The following section details the BFL design methodology used to build the logic gates.

4.1 Digital GaN Buffered FET Logic Design Process

As stated in Chapter 3, BFL is a modification of UFL due to the added source follower transistor. The same logic values from Table 3.1, as well as careful consideration of V_{DD} and V_{SS} are required, for the full logic swing to ensure that transistors T_{SF} and T_{PD} are both in saturation. Once again, boundary conditions are placed on V_Y, V_A, and V_Z to ensure that the schottky diode between the drain and gate is

sufficiently reverse biased. Equations 4.2, 4.3, and 4.4 represent the boundary limits on these nodes.

By substituting equation 4.2 into equation 4.3, it is apparent that, at a minimum, the input to a logic gate must follow $V_A < V_{DD} - 2 \cdot V_{DROP}$ to have enough margin for sufficient reverse bias of the schottky diodes. To illustrate the operation, assume that the input to T_A is initialized to logic low such that $V_A = V_L$ and $V_Z = V_H$ as shown in Figure 4.1. In this steady state, transistor T_A turns off, and V_Y is pulled to V_{DD}. V_Y is permitted to violate the boundary condition presented in equation 4.2 because there is no current path from drain to gate. If no current can flow into the gate of T_{SF}, T_{PU} can be approximated as a open with V_Y rising to V_{DD}.

As seen in Figure 4.1, $V_Y >> V_X$, such that $V_{GS} = V_Y - V_Z >> V_T$, creating large current drive from T_{SF}. This surge of current charges V_Z to logic high, requiring that $V_Z > V_T$ to ensure that the following logic stage input is turned ON. In the case that level shifting diodes are added, such as in Figure 4.2, equation 4.5 can be substituted into $V_Z = V_X - n \cdot V_{DIODES}$ to show that $V_Z = V_{DD} - V_{DROP} - n \cdot V_{DIODES}$, presented in equation 4.1. The following list acts as the boundary conditions for $V_A = V_L$.

- $V_Z < V_{DD} - V_{DROP} - n \cdot V_{DIODES}$
- $V_H = V_Z > V_T$
- $V_Z > V_{SS} + V_{DROP}$

$$V_Z = V_{DD} - V_{DROP} - n \cdot V_{DIODES} \tag{4.1}$$

$$V_Y < V_{DD} - V_{DROP} \tag{4.2}$$

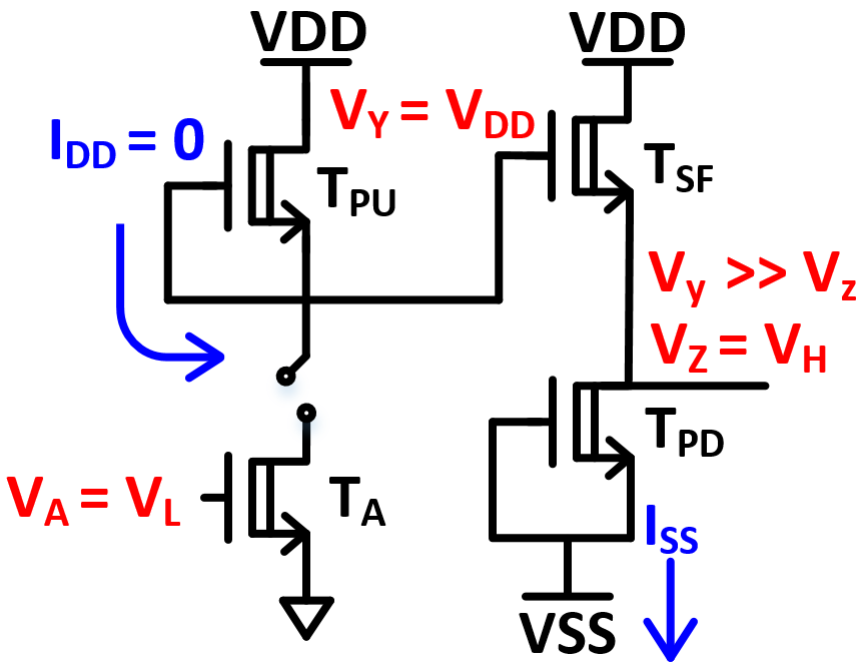

Figure 4.1: BFL INV Gate without Level Shifting Diodes

$$V_A < V_Y - V_{DROP} \tag{4.3}$$

$$V_Z > V_{SS} + V_{DROP} \tag{4.4}$$

$$V_X < V_{DD} - V_{DROP} \tag{4.5}$$

Now, assume that V_A transitions from low to high, such that $V_A = V_H$, as shown in Figure 4.3. T_A turns on, and a path to GND is created. Current now passes from T_{PU} to T_A, with V_Y set by the effective resistances of both transistors. Because Both T_{PU} and T_A have a constant V_{GS}, both can be modeled as resistors with values R_{PU} and R_A, as shown in Figure 4.4. In order to pull V_Y towards GND, R_A is set low

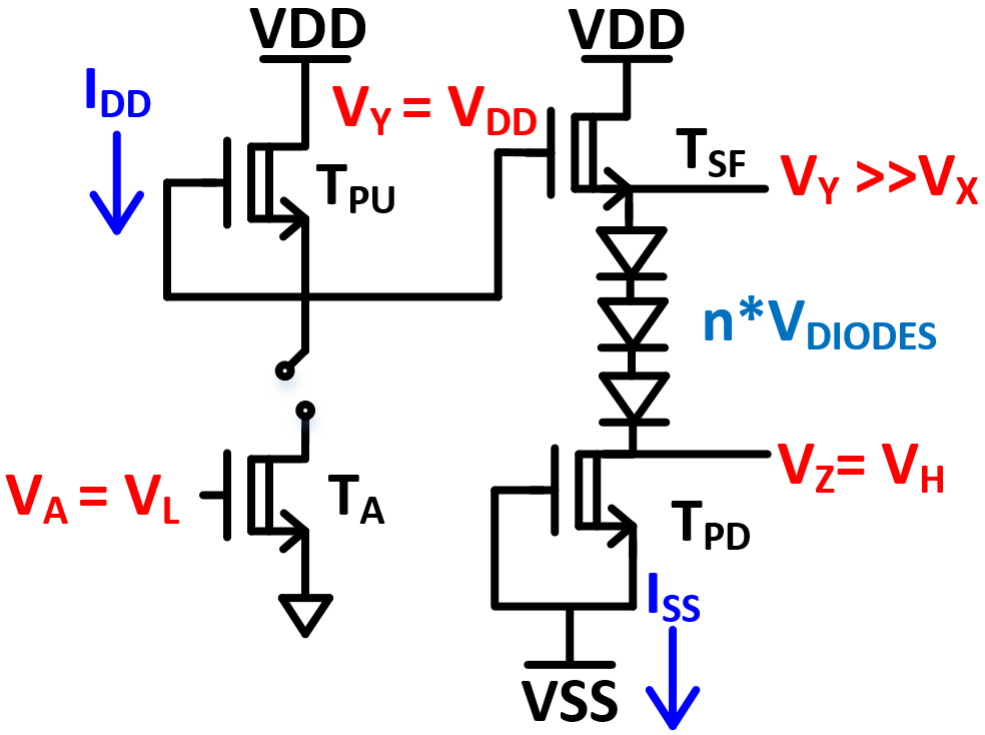

Figure 4.2: BFL INV Gate with Logic Low Input

relative to R_{PU}. By decreasing R_A, V_Y falls to a lower voltage, as seen in equation 4.6.

As V_Y falls, T_{SF} sees a $V_Y - V_X << V_T$, cutting off the channel of T_{SF}. T_{SF} turning off during the low to high transition of V_A is an operational requirement to ensure that V_Z can discharge to V_{SS}. If this condition is not met, level shifting diodes are added such that $V_X = V_Z + n \cdot V_{DIODES}$, where $V_Y - V_X << V_T$, as presented in Figure 4.4. This guarantees that T_{SF} turns off, allowing V_Z to discharge through T_{PD}. In order to turn off the inputs to the next stage, V_Z must discharge to a magnitude below V_T. As a result, V_{SS} is selected to satisfy equation 4.4. While V_Z discharges, V_X slowly drops until $V_Y - V_X > V_T$, dissipating current through T_{SF}, directly slowing the discharge of V_Z.

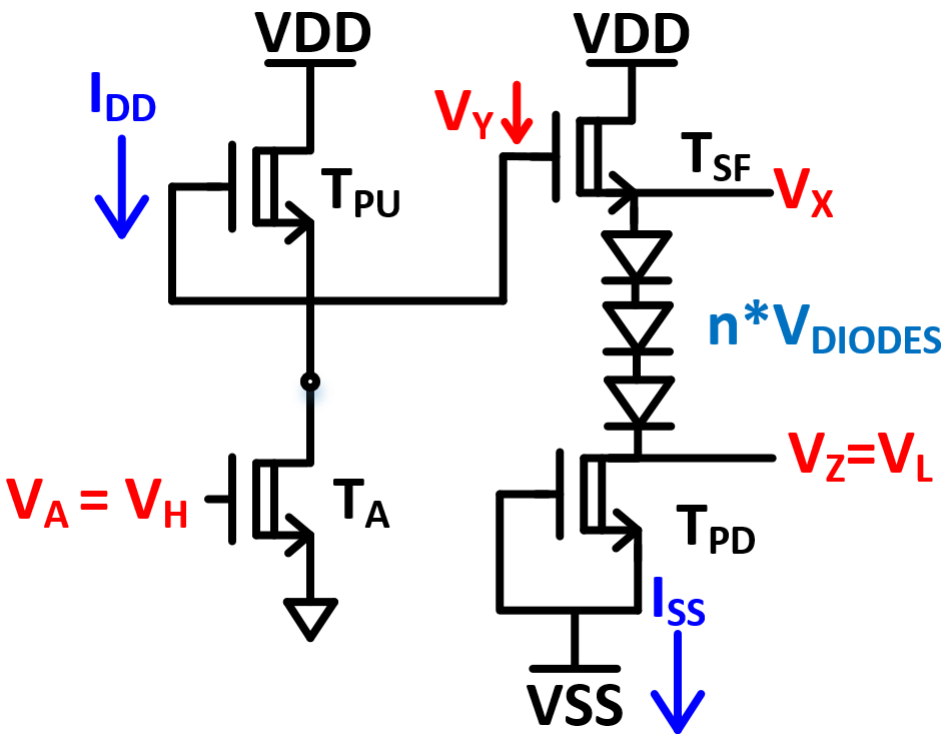

Figure 4.3: BFL INV Gate with Logic High Input

$$V_Y = V_{DD}(\frac{R_A}{R_{PU} + R_A}) \tag{4.6}$$

The boundary conditions for $V_A = V_H$ are in the following list.

- $V_Y - V_{X_{(V_A=V_L)}} << V_T$
- $V_L = V_Z > V_{SS} + V_{DROP}$
- $V_{SS} < V_T - V_{DROP}$

Using the boundary conditions of both $V_A = V_L$ and the transition to $V_A = V_H$, minimum V_{DD} and V_{SS} are obtained. V_{SS} is set based on the V_T and V_L. V_{SS} is

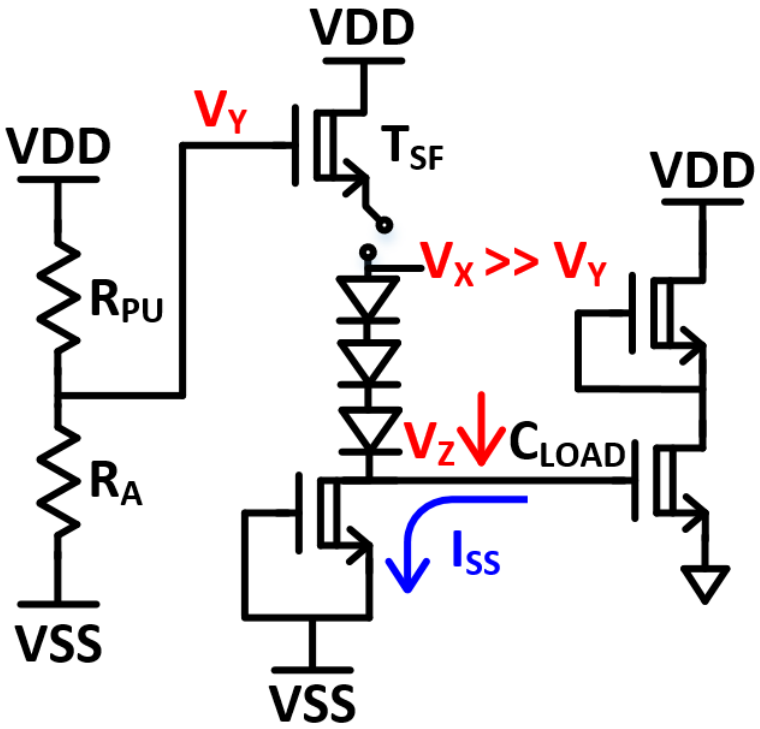

Figure 4.4: BFL INV Gate with Resistor Divider at Gate of T_{SF}

bounded by both $V_{SS} < V_T - V_{DROP}$ and $V_L > V_{SS} + V_{DROP}$. Assuming that $V_L = V_T$ to turn off the following logic stages, V_{SS} is solved to be equation 4.7.

$$\begin{aligned} V_{SS} &< V_L - V_{DROP} \\ V_L &< V_T \end{aligned} \tag{4.7}$$

A more negative V_L puts the following logic stages in the deep cut off region, reducing current in the channel. If V_L is barely less than V_T, the channel is weakly cut off. This indicates that lower V_L values are ideal. Defining V_{DD} requires more analysis. In the $V_A = V_L$ case, V_{DD} is bound such that $V_X < V_{DD} - V_{DROP}$. When V_A transitions to V_H, the source follower, T_{SF} turns off. For this to happen $V_Y - V_{X_{(V_A=V_L)}} << V_T$. If transistors T_A and T_{PU} are designed with a given V_{DD} such that equation 4.6 resolves to $V_Y = V_H + V_{DROP}$, then V_Y is the minimum allowable value. This is designed for

by setting $R_A << R_{PU}$. Substituting $V_Y = V_H + V_{DROP}$ into V_Y and equation 4.5 as V_X, the minimum allowable V_{DD} needed to turn off T_{SF} and level shift to logic V_H can be solved, as presented in equation 4.8.

$$\begin{aligned} V_Y = V_{DD}\frac{R_A}{R_A + R_{PU}} &= V_H + V_{DROP} \\ V_X &= V_{DD} - V_{DROP} \\ V_{DD} &> V_H + 2 \cdot V_{DROP} - V_T \end{aligned} \tag{4.8}$$

From V_{DD}, the number of level shifting diodes are determined to shift V_Z to V_H, presented in equation 4.9.

$$n = \frac{V_{DD} - V_{DROP} - V_H}{V_{DIODES}} \tag{4.9}$$

To demonstrate, assume the following process parameters: $V_H = 0$ V, $V_L = -4$ V, $V_T = -3.5$ V, $V_{DIODES} = 1.5$ V, and $V_{DROP} = 1.1$ V. Substituting into equations 4.8, 4.9, and 4.7 provides $V_{DD} = 5.7$ V, $n = 3.06$, and $V_{SS} = -4.6$ V.

If $V_A = V_L$, then $V_Y = 5.7$ V, $V_X = 4.6$ V, and $V_Z = 0.1$ V. When $V_A = V_H$, we note that $V_Y = 1.1$ and $V_Y - V_X = -3.5$ V, turning off T_{SF}. This causes V_Z to discharge to $V_{SS} + V_{DROP} = -3.5$ V. In practice, V_{DD} should be increased larger than 5.7 V to turn off T_{SF} for longer, increasing the discharge time of V_Z. Decreasing V_{SS} provides a more negative V_{GS} to the next stage input transistors, putting them deeper in the cutoff region, impeding the flow of current.

4.2 Implemented BFL Logic Gates

Designing and implementing this logic family without simulation models requires intuition and a fundamental understanding of the logic operation. Using the proposed

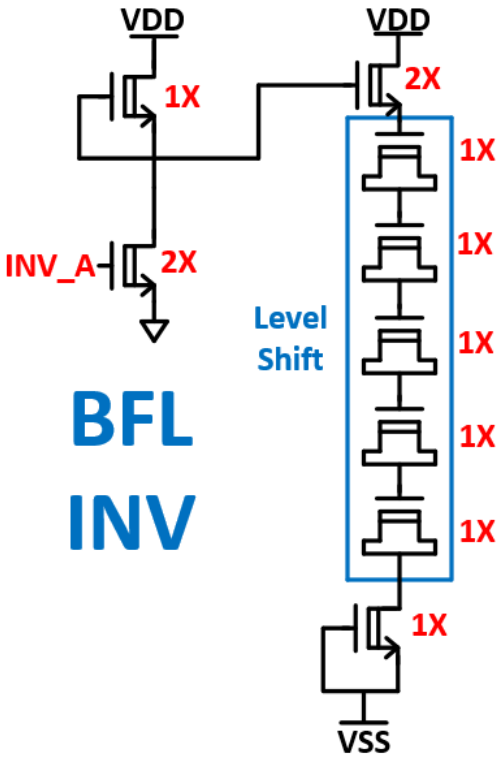

Figure 4.5: BFL Inverter with Diode Connected Level Shifting

design process, an inverter, 2 input NAND gate, and 2 input NOR gate are designed into separate groups, one with $W_{MIN} = 5\,\mu$m and one with $W_{MIN} = 12\,\mu$m. The threshold voltage, diode drop, and forward bias voltage of the schottky are estimated to be $-3.5\,$V, $1.5\,$V, and $1.1\,$V, respectively. Using these approximate values, V_{DD} and V_{SS} are selected as $12\,$V and $-4\,$V, as detailed in Table 4.1. The selected rails permit the source follower to both generate large current for rising outputs and turn off the source follower for falling outputs. The designed gates are shown in Figures 4.5, 4.6, and 4.7. The input transistors are sized twice the W_{MIN} to increase the pull down strength such that the gate of the source follower can be biased at $V_H + V_{DROP}$. The source follower is also doubled to increase the current that is driving the next logic stages.

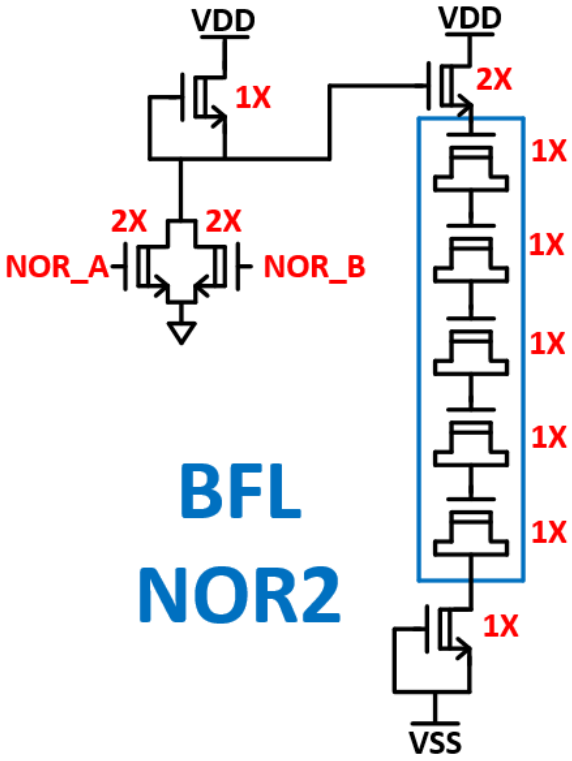

Figure 4.6: BFL NOR2 with Diode Connected Level Shifting

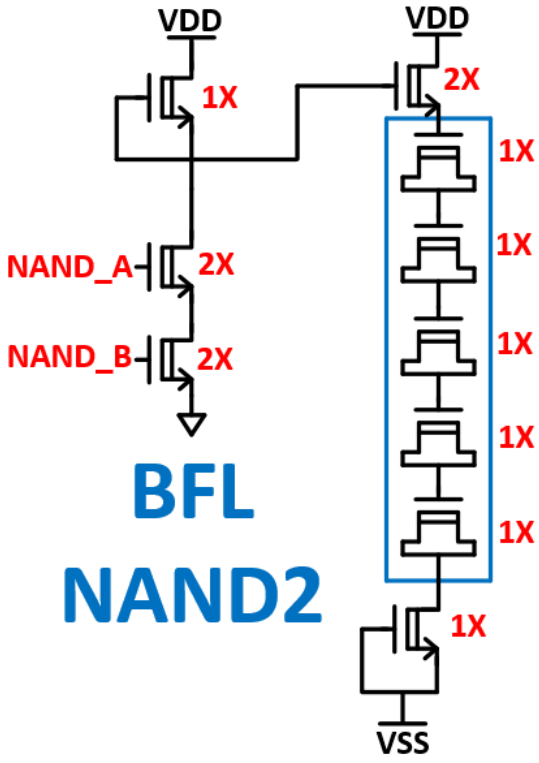

Figure 4.7: BFL NAND2 with Diode Connected Level Shifting

Table 4.1: Digital GaN Fixed Design Parameters

V_{DD}	V_{SS}	GND	V_T	V_{DROP}	V_{DIODE}
12 V	-4 V	0 V	-4 V	1.1 V	1.5 V

Chapter 5: Buffered FET Logic GaN Testing and Results

5.1 Fabrication and Test Setup

After designing the GaN logic gates, they are fabricated on a gold plated copper tungsten carrier (Figure 5.1) and are placed in logical configurations as seen in Figures 5.2 and 5.3. Groups A and B/C have minimum gate widths of $W_{MIN} = 12\,\mu$m and $W_{MIN} = 5\,\mu$m, respectively. In order to probe the inputs and outputs of the logic structures, ten pads are added for each logic bank, specified in Table 5.1. These pads are interfaced to the testing equipment using a probe station with custom ordered probes with a pitch of $100\,\mu$m, as seen in Figure 5.4. Each probe is attached to a banana cable which is connected to the testing equipment.

The base equipment needed to test the logic gates are an oscilloscope, arbitrary waveform generator (AWG), DC power supply, and probe station with thermal chucks for testing across temperatures. In order to characterize the BFL logic gates, it is imperative to identify the critical performance parameters, which are detailed in the following list. These are characterized across varying power supply rails (V_{DD} only), temperature, and input frequencies F_{IN}.

- V_{DD}/V_{SS}

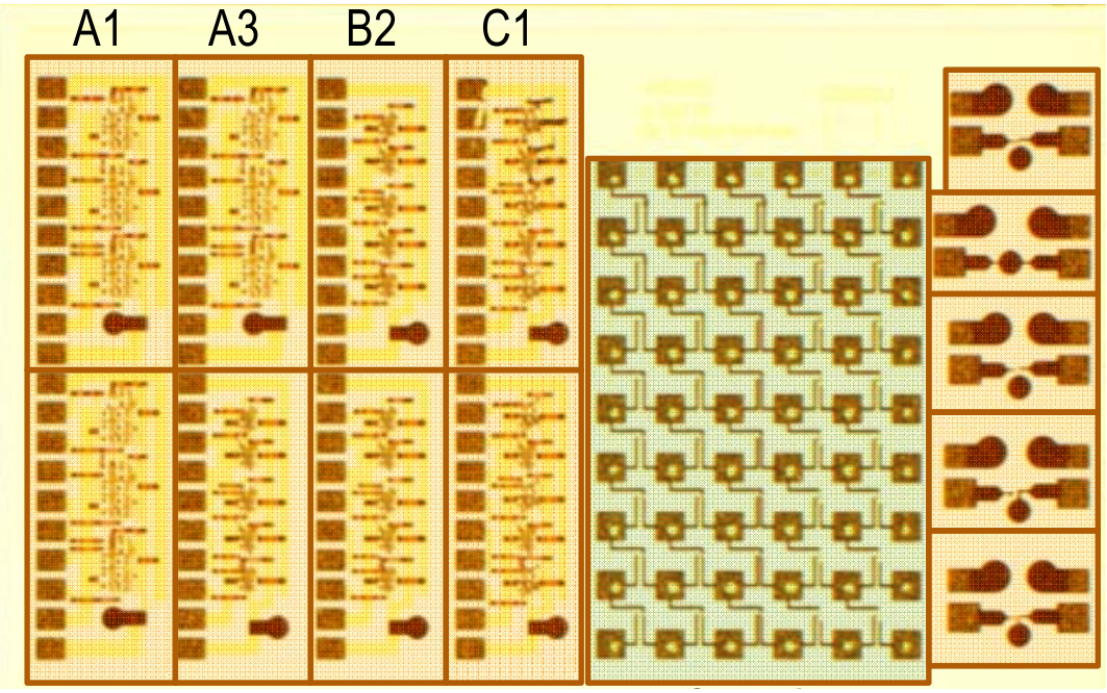

Figure 5.1: Designed Logic Gates on Gold-Plated Copper Tungsten Carrier

- Input Frequency (F_{IN})
- V_{HIGH}/V_{LOW}
- Rise Time (T_{RISE}) / Fall Time (T_{FALL})
- Positive P_{HIGH} / Negative P_{LOW} Pulse Widths
- $T_{PROPFALL}$ and $T_{PROPRISE}$

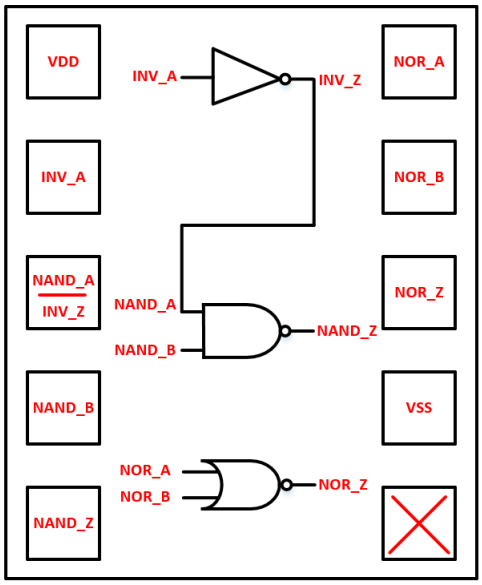

Figure 5.2: Gate Structure of A1/A3 Logic Banks

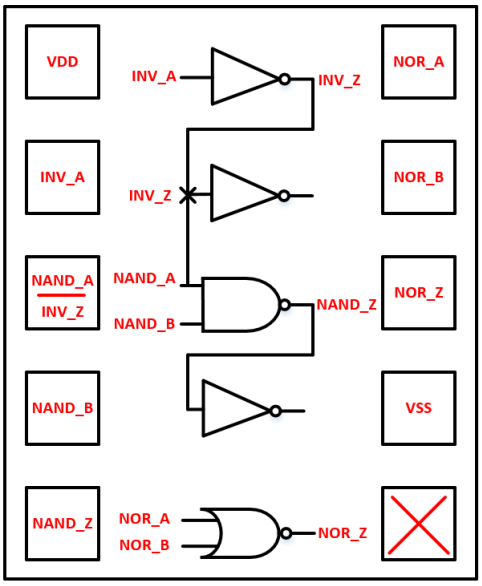

Figure 5.3: Gate Structure of A1/A3 Logic Banks

Table 5.1: Pin Configuration for Pads in Figure 5.1

Probe Pin	Signal
1	VDD
2	INVA
3	NANDA/INVZ
4	NANDB
5	NANDZ
6	NORA
7	NORB
8	NORZ
9	VSS
10	GND

5.2 Testing Procedure

The following equipment is used to test the GaN logic gates:

- Agilent Infiniium DS09204H Oscilloscope (2 GHz)
- Keysight E3631A Power Supply
- Keysight 811150A Pulse Function AWG (120 MHz)

All measurements with the equipment are completed using standard GPIB connectors with LabView as the interfacing software. The AWG provides the input signals to the logic gates by connecting the banana jacks from the probes to the AWG, while the input, along with the outputs from the logic gates, are connected to the oscilloscope for measurement. All of the calculations and data processing are completed in LabView and Matlab to generate the resulting data plots.

The test plan itself is a dynamic characterization of the logic gates across three variables: temperature, voltage, and input frequency. The swept parameters are

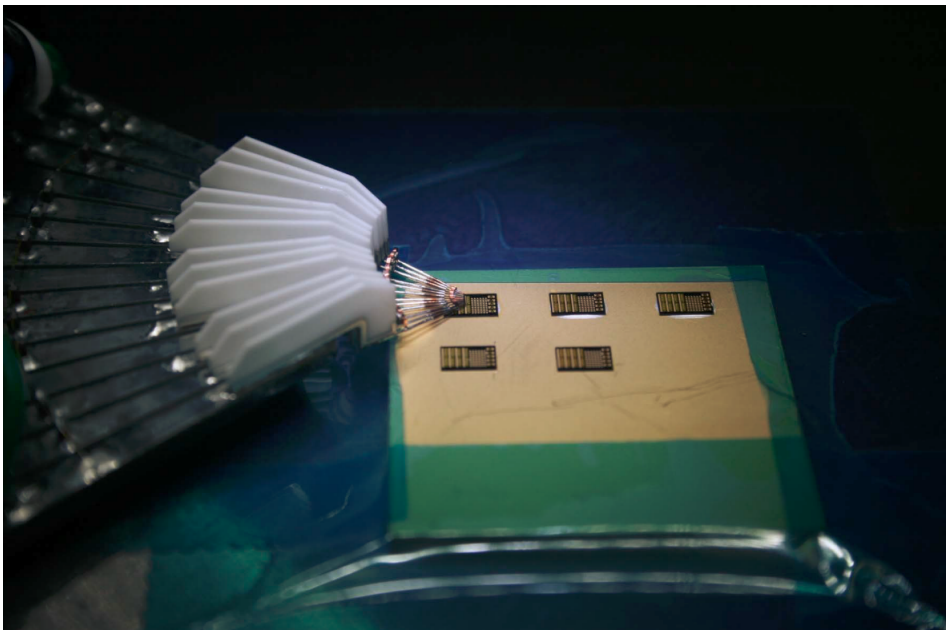

Figure 5.4: 10 Pin Probe Interfacing with GaN Logic Gates

included in Table 5.2. Testing for operation across V_{DD} and temperature characterizes the devices across dynamic operating conditions, while sweeping the input frequency qualifies the maximum speed of the gates. In the test setup, the probes are loaded with decoupling capacitors, increasing the time constant at the output of the gates. The decoupling capacitors on the probes, as well as the GaN IO pads, directly limit the maximum achievable input frequency before too much noise interferes with valid readings from the output.

Table 5.2: Variable Sweep

V_{DD}	F_{IN}	T
12:0.5:10 V	1kHz-25kHz	18C, 175C V

After attaching the probes to the oscilloscope, data measurements are taken across the variable sweep. Propagation delays $T_{PROPFALL}$ and $T_{PROPRISE}$ are calculated by taking the difference between the time stamps of the 50% points of T_{RISE} and T_{FALL}. Both T_{RISE} and T_{FALL} are calculated by taking the time difference between the 90% and 10% points of the logic high and logic low values. During the dynamic voltage scaling of V_{DD}, the 90% and 10% voltage points change based on the levels that the output gate values are swinging between. V_{HIGH} and V_{LOW} are the stable logic high and logic low values measured on the oscilloscope. Finally, P_{HIGH} and P_{LOW} are the pulse widths of the logic high and logic low states. These parameters are detailed in Figure 5.5.

5.3 Results

The swept results are presented in the appendix. It is important to note that the NAND gate fails to function correctly at $V_{DD} = 10$ V. In the results, the performance of the NAND gate at $V_{DD} = 10$ V is held constant to the previous state, as a result. The NAND at 175C also fails to operate at $V_{DD} = 10.5$ V, which is why it is held constant after $V_{DD} = 11$ V. In cases where there is no data point, the data is an outlier and is removed. Based on the sampled results, the rise times, fall times, and propagation delays do not vary across input frequency. At higher frequencies, there would be a visible change in these parameters. The results across the input frequencies are averaged so that a single value is plotted for given temperatures across a voltage sweep.

5.3.1 Results Analysis

Between the minimum sized gates (Group B) at $W_{MIN} = 5\,\mu$m (asterisk / squares) and the larger devices (Group A) $W_{MIN} = 12\,\mu$m (circle / star) of the resulting plots, there is an apparent 1.5 to 2.5 times speed increase in the larger sized devices. The rise times of Group A inverters is approximately 150 ns, while the rise times of Group B inverters are close to 400 ns. As V_{DD} scales down, the rise times and fall times respectively decrease. Power consumed from I_{SS} is relatively constant since V_{SS} remains the same, while I_{DD} shows a decrease as voltage drops. The propagation delays drop as V_{DD} decreases and are much larger at higher temperatures. In the case that the falling edge of the output is longer, the rising to falling edge propagation delay is increased. Ideally, the BFL logic gate would not drop to V_{SS}, causing the large fall times, as this requires a long discharge time. This results in an effective increase in propagation delay.

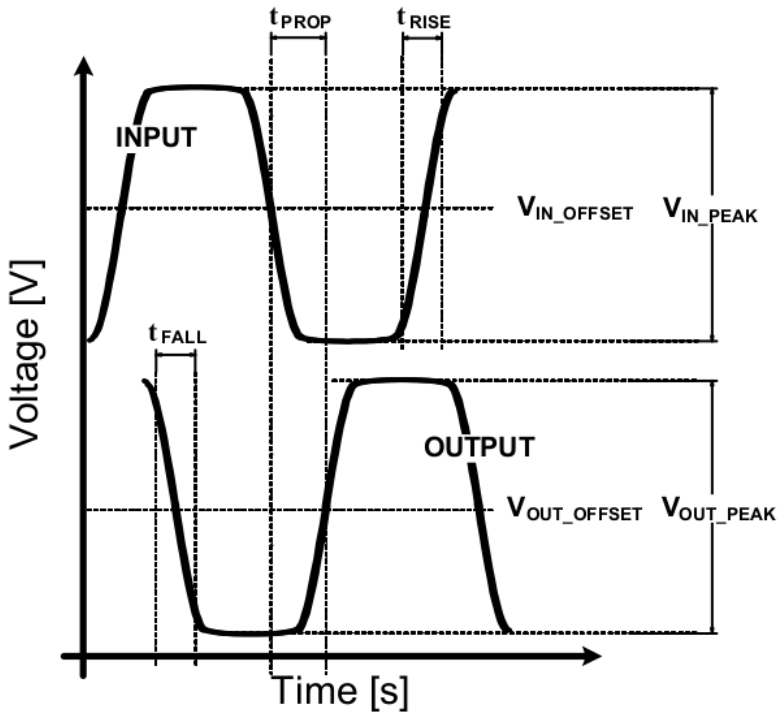

Figure 5.5: Digital Logic Performance Metrics for Gate Level Devices

Chapter 6: Conclusion and Future Work

The designed GaN BFL logic gates are proved functional and operational across voltage, temperature, and input frequency. This is also the case in which the minimum width is scaled down, despite going against design rules for the given process. These both demonstrate that BFL in GaN is functional and scalable for future designs, especially as models and design kits become more available. For the future work, the remaining depletion logic families (CDFL, UFL, SDFL) need to be implemented and characterized across voltage, temperature, and frequency, as well as bench marked against each other for optimum performance. The current BFL gates also need to be characterized at higher input frequencies to determine maximum operating conditions. Contingent on the remaining tasks, GaN logic proves to be a viable option in digital systems and integrated circuits and will see expanding development in the following years.

Appendix A: Digital Logic Gate Measured Results

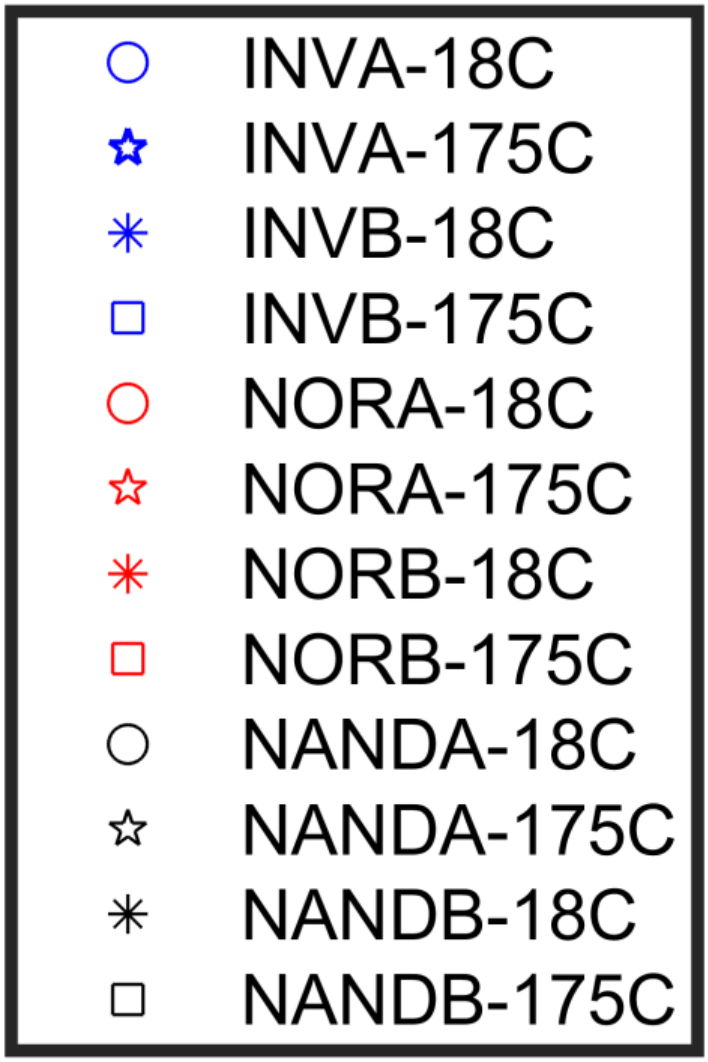

Figure A.1: Legend with Nomenclature for Sampled Data

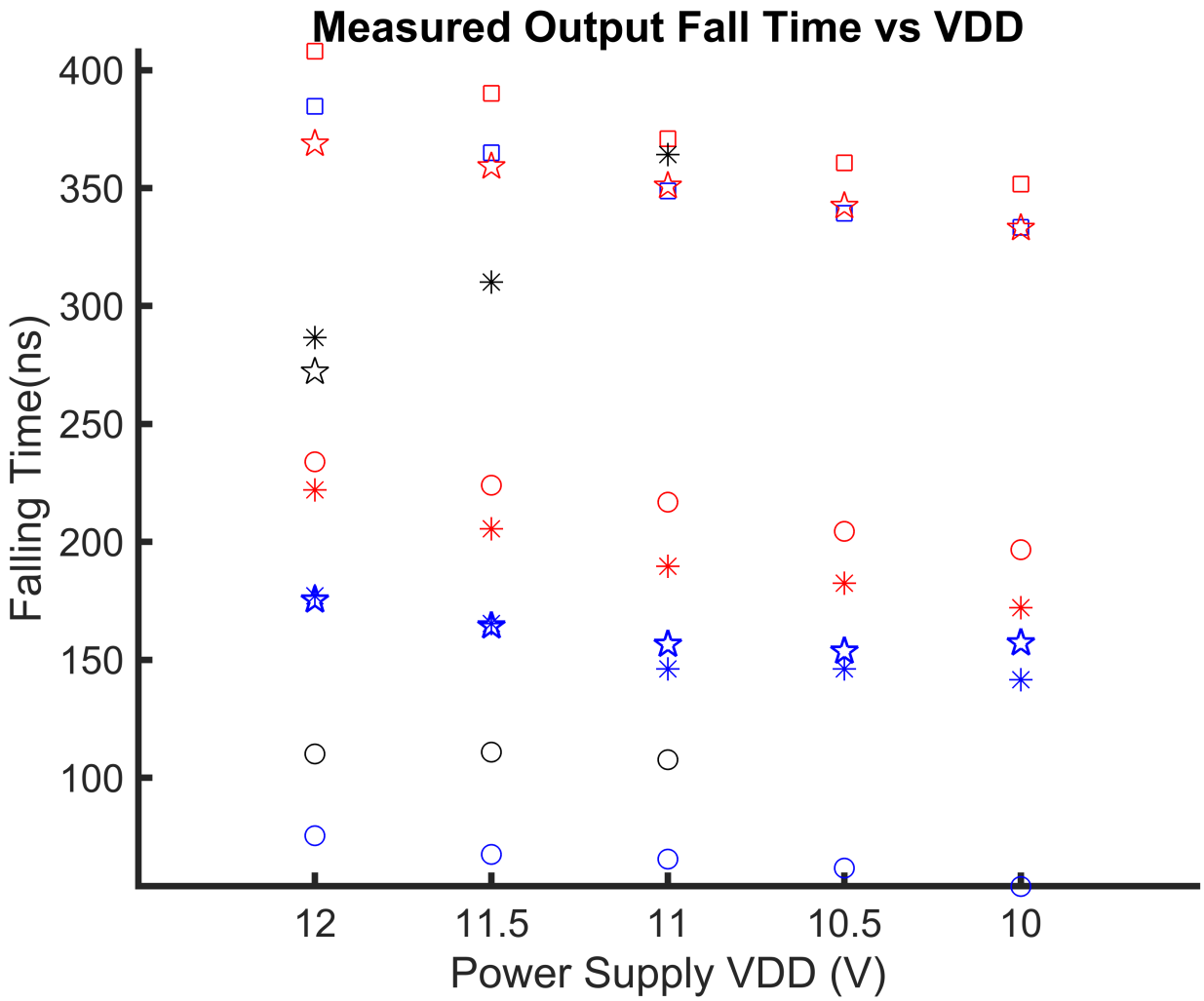

Figure A.2: Measured Output Fall Time

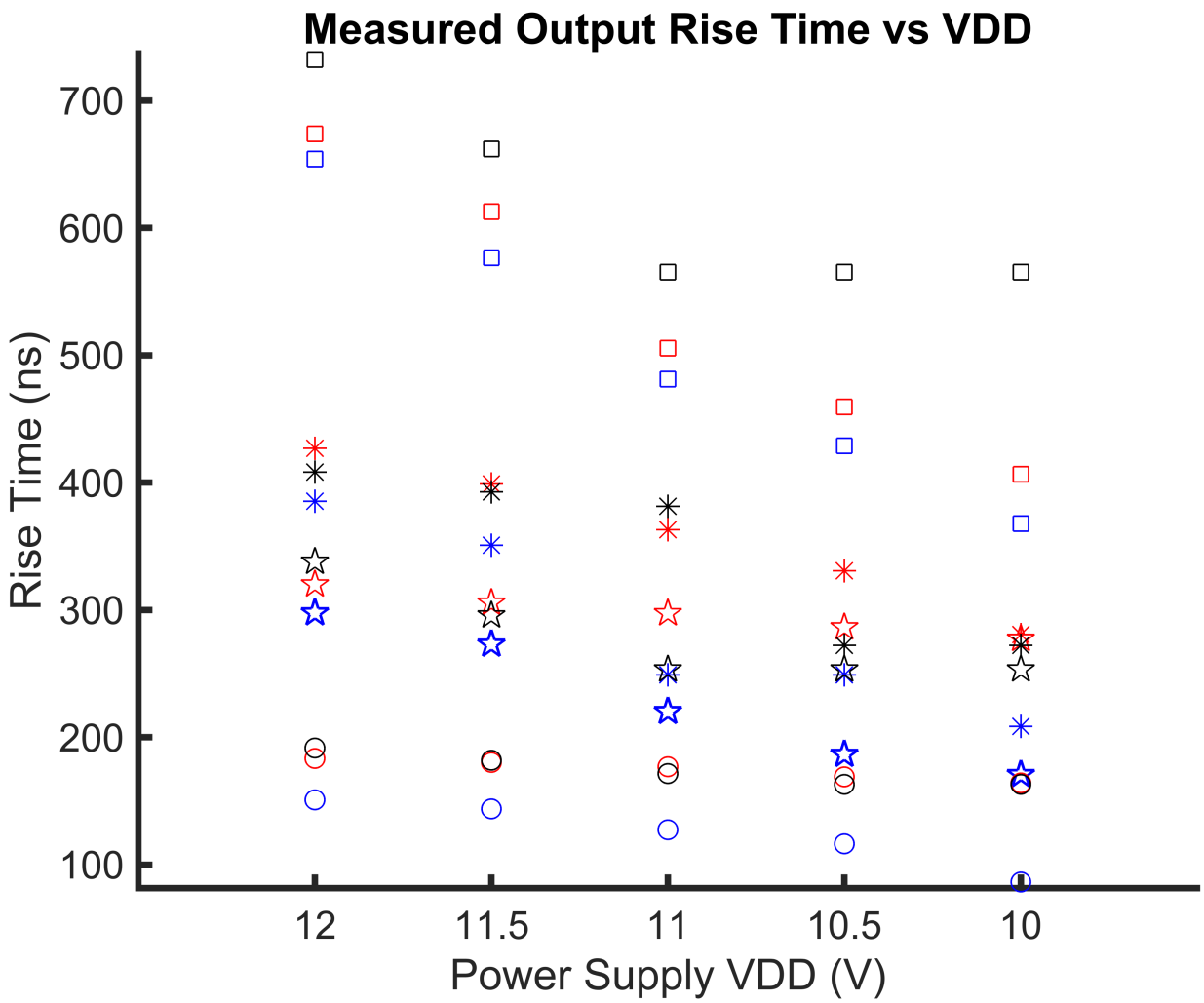

Figure A.3: Measured Output Rise Time

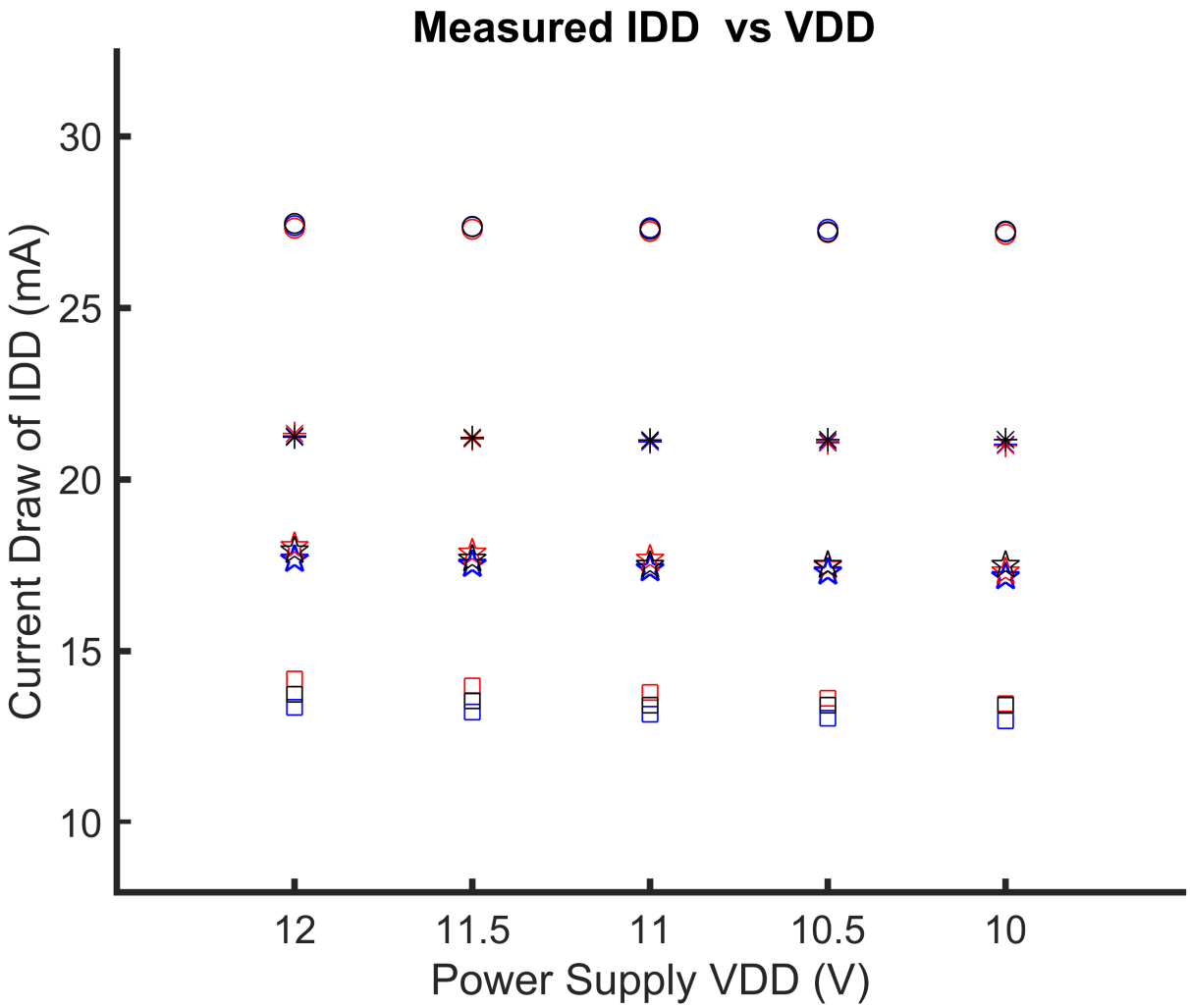

Figure A.4: Measured Current Consumed from V_{DD}

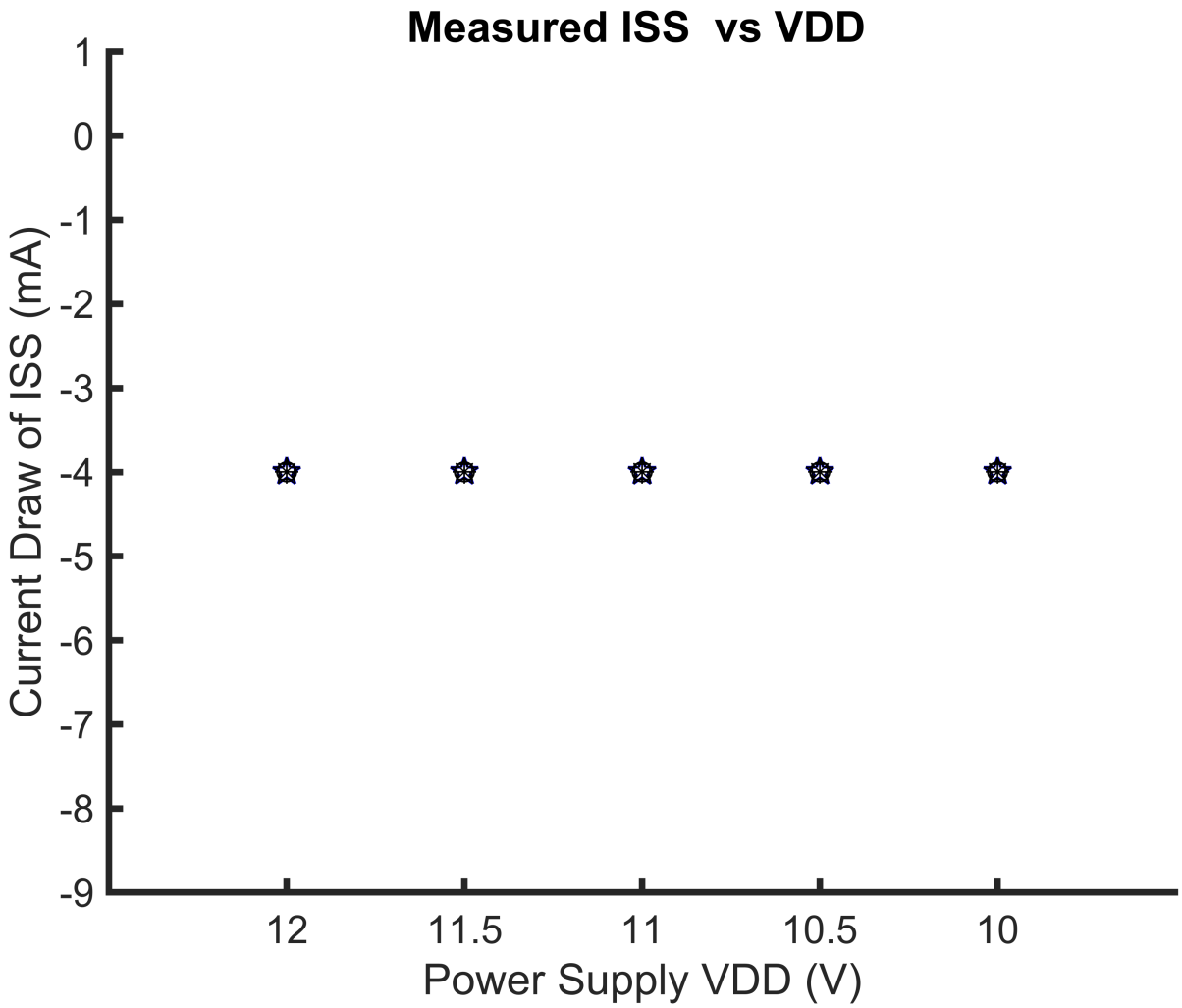

Figure A.5: Measured Current Consumed from V_{SS}

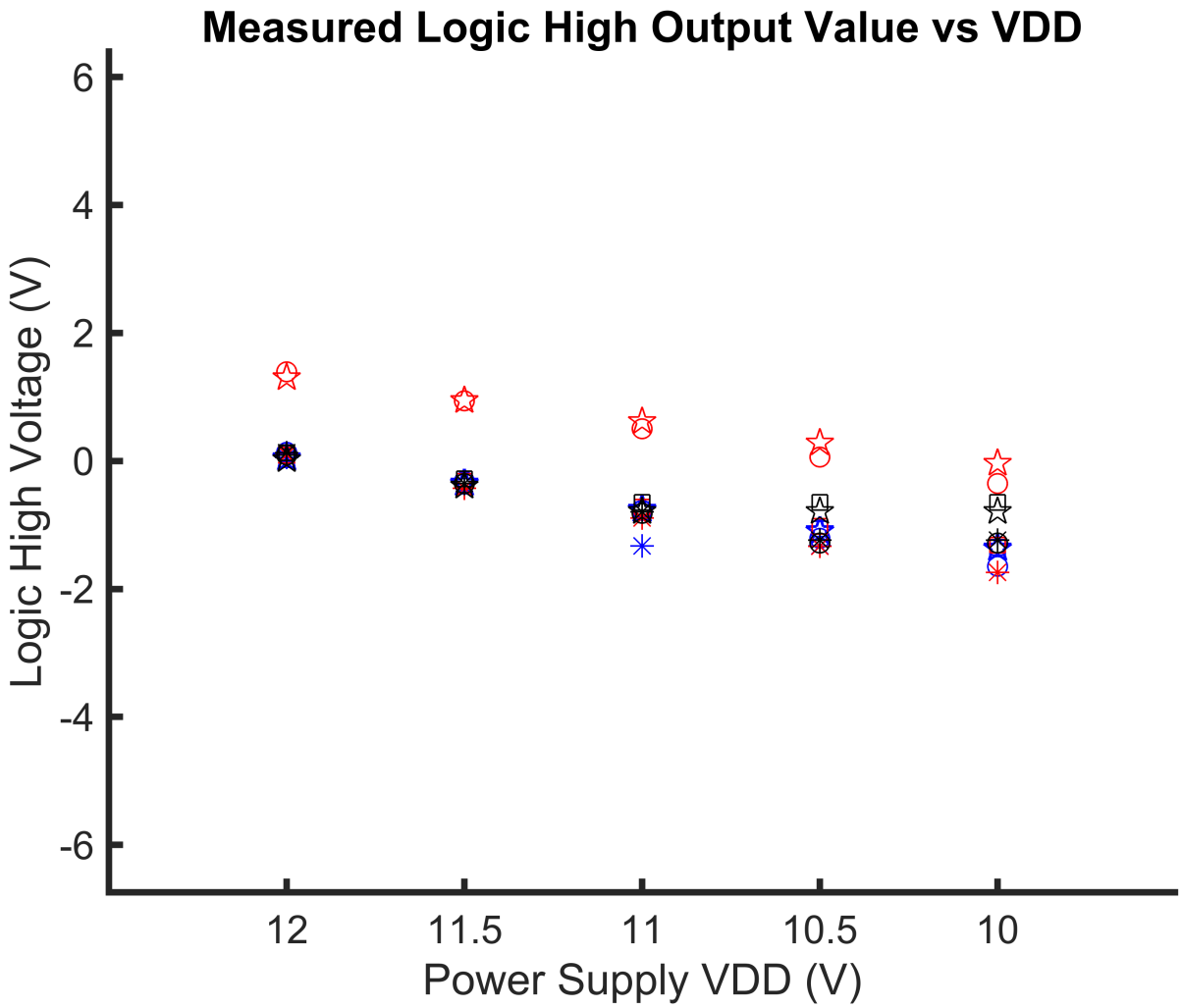

Figure A.6: Measured Logic High Value

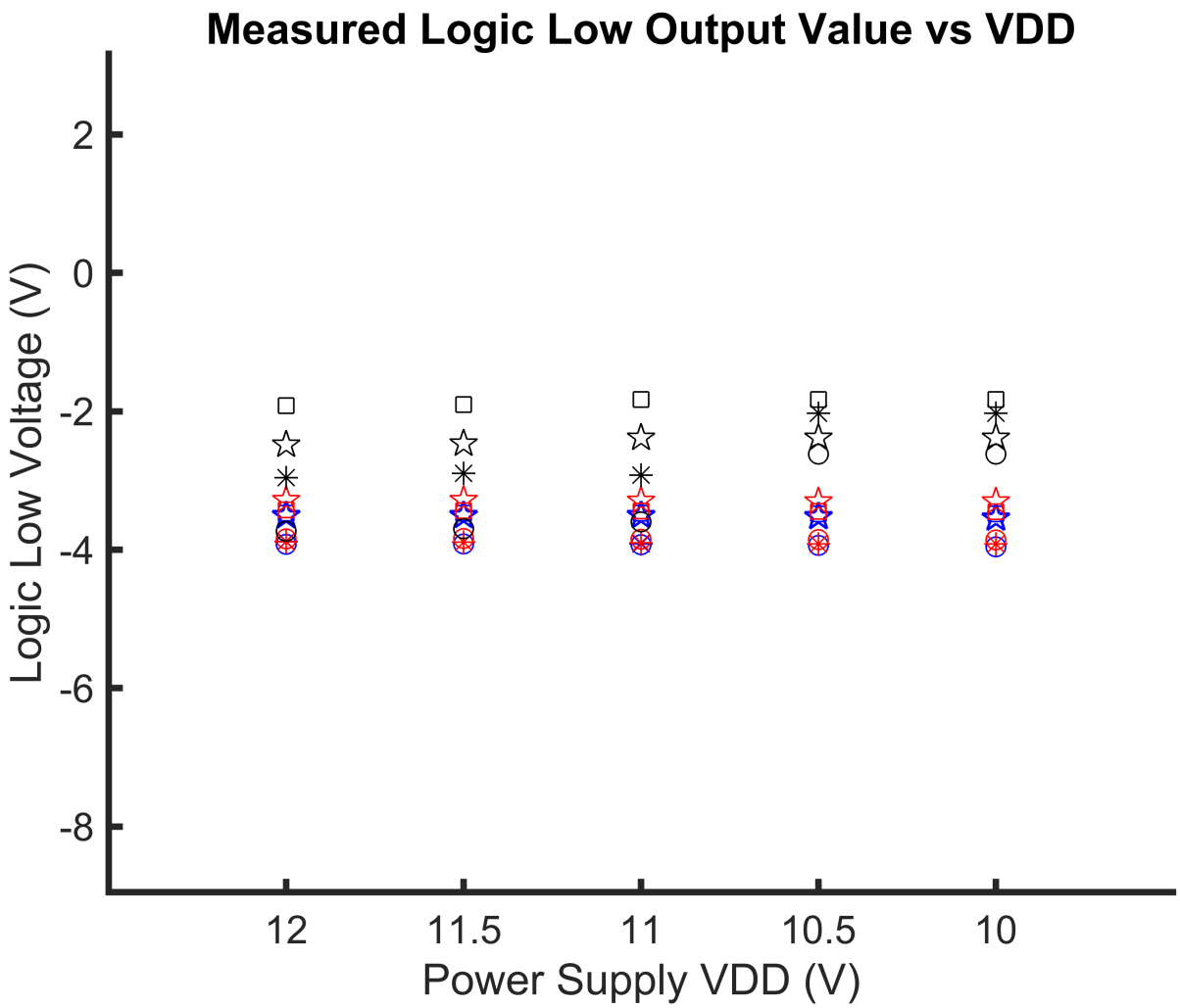

Figure A.7: Measured Logic Low Value

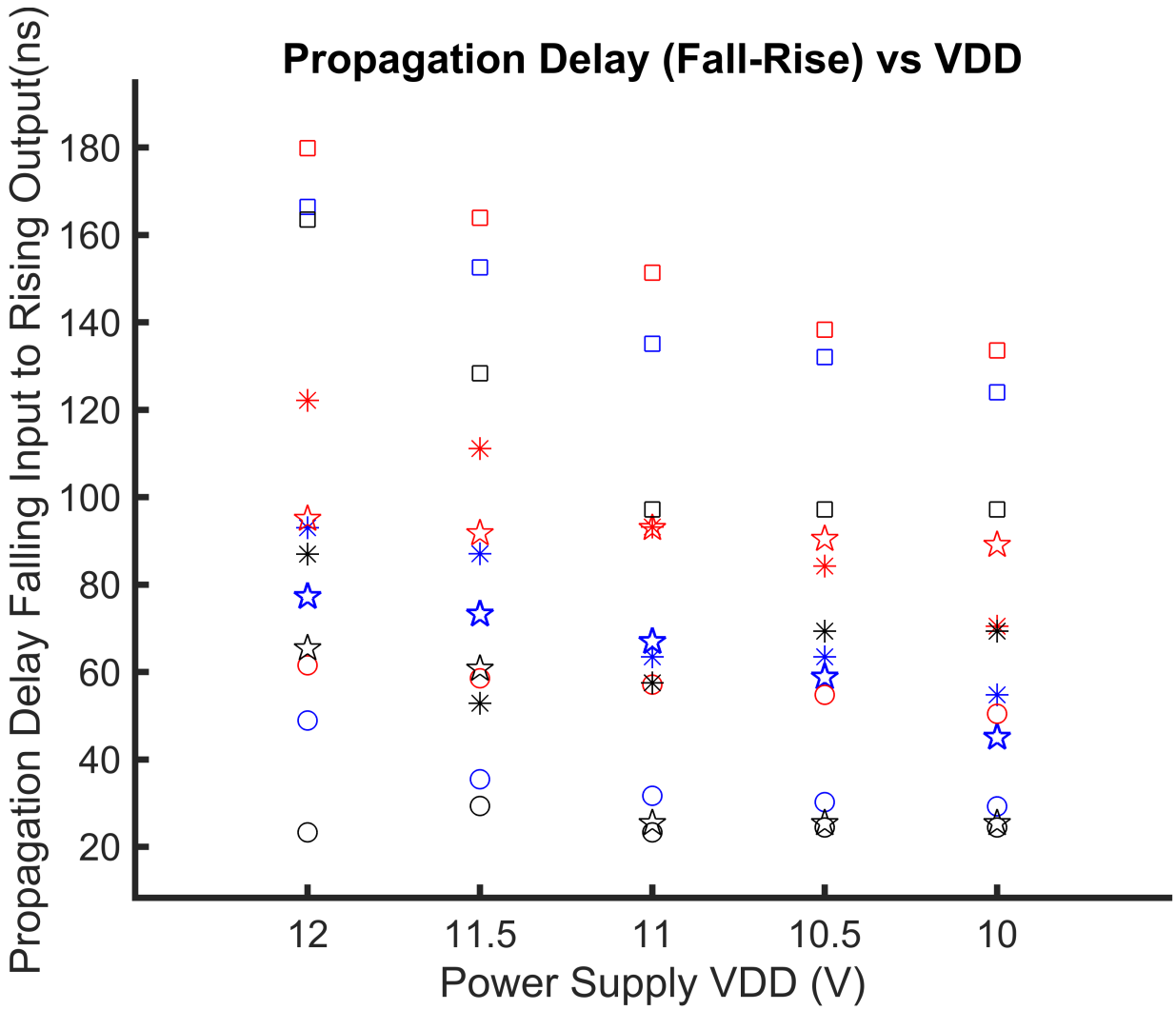

Figure A.8: Input Fall to Output Rise Propagation Delay

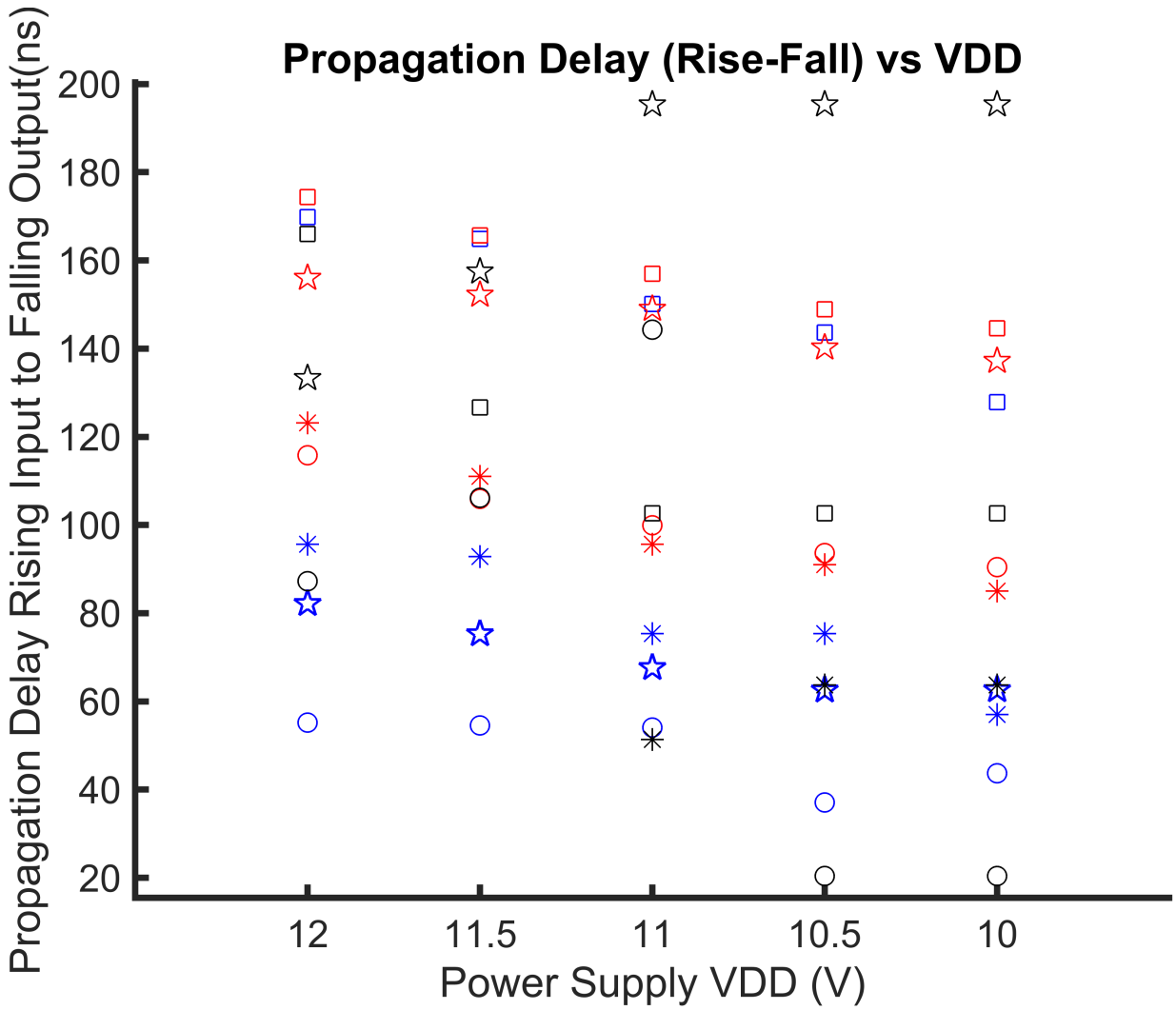

Figure A.9: Input Rise to Output Fall Propagation Delay

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