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Transient Simulation of High-Voltage Silicon Carbide Super-Gate Turn-off Thyristors (SGTOs) under Extreme Narrow Pulsed Conditions

by Aderinto Ogunniyi, James Schrock, Heather O'Brien, and Stephen Bayne

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14. ABSTRACT

This report discusses the failure mechanism of 15-kV silicon carbide super-gate turn-off thyristors (SGTOs) during extreme high current density (3.85 kA/cm^2) pulsed operation. It is believed that the failure mechanism of the devices evaluated is attributed to recombination-induced stacking fault (SF) formation due to the insufficient buffer layer thickness. The SF failure mechanism is supported experimentally by forward voltage degradation observed during long-term pulse evaluation of the SGTO devices during high-current narrow pulse evaluation performed at 0.5 Hz. The report implements technology computer-aided design simulation at the experimental narrow pulse evaluation previously stated. The results reveal a significant level of (~10^{14} cm^{-3}) minority carrier injection in the buffer layer that penetrates into the substrate region of the device, which could potentially affect the long-term reliability and pulse performance. A model of a high-power SGTO was developed in the Silvaco Atlas software to better understand the extreme electrical stresses in the SGTO when subjected to a high-current pulse. Simulation of the on-state current and device forward voltage drop closely matches measured data. Current density distribution through the device was analyzed, and areas of high minority carrier injection at elevated high current operation were identified.

15. SUBJECT TERMS
silicon carbide, SiC, gate turn-off thyristor, GTO, pulsed power, stacking faults, SFs, anode current, carrier injection, pulse forming network, PFN

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1. Introduction

Silicon carbide (SiC) power devices are attracting great interest for next-generation pulsed-power and power electronic systems. SiC offers several material advantages over its silicon counterpart such as high critical field, fast switching, recovery time, high thermal conductivity, and large elastic modulus, making it favorable for pulse-switching systems and applications.[1–4] The US Army Research Laboratory* has developed an interest in modeling and simulation of the inner workings of high-pulsed-power SiC devices that are subjected to elevated current densities at unique timescales in the microsecond and millisecond regime. Accurate physics-based SiC models will enable better optimization of SiC device designs leading to enhanced device performance and reliability. These physics-based SiC models will also enable the prediction of device performance at various extreme pulsed conditions, expanding the application of SiC power devices. This research presents the modeling and evaluation of SiC gate turn-offs (GTOs) at extreme pulsed power densities and shows direct correlation between measured high-power characterization and simulated current and voltage waveforms.[1–4] It is speculated that recombination-induced stacking faults (SFs) are the underlying mechanism that limits the long-term reliability and peak current capability of ultra-high-voltage SiC super-gate turn-off thyristors (SGTOs) used in high-current-density pulsed applications. Although SF formation at basal plane dislocations (BPDs) is a well-known degradation mechanism of SiC bipolar devices that results in erratically increasing forward voltage drop,[5–7] SF formation has been mitigated for standard current densities (~100 A/cm^2) through advances in processing techniques.[6,7] These processing techniques include the prevention of interfacial BPDs from growth of epilayers that experience conductivity modulation by increasing the efficiency of their conversion to threading edge dislocations through potassium hydroxide etch preparation of the substrate and by growth of thick buffer layers on the top of the substrate to prevent minority carrier injection into the substrate where the high density of BPDs reside.[6,7] This research presents experimental on-state voltage degradation that is characteristic of SFs of 15-kV SiC SGTOs during narrow pulse operation. Furthermore, a technology computer-aided design (TCAD) simulation was implemented to analyze potential causes of forward voltage (V_F) drop instability in SiC GTO during extreme pulsed-power operation.

* The work outlined in this report was performed while the US Army Research Laboratory (ARL) was part of the US Army Research, Development, and Engineering Command (RDECOM). As of 31 January 2019, the organization is now part of the US Army Combat Capabilities Development Command (formerly RDECOM) and is now called CCDC Army Research Laboratory.

2. SiC GTO Structure

The 15-kV SiC SGTO presented in this report is manufactured by Wolfspeed. It has a chip area of 1.05 cm^2 and an active area normalized to the anode mesa of 0.52 cm^2. The SGTO has highly interdigitated gate-anode regions that enable the device to have an extremely fast turn-on *dI/dt* capability. Figure 1 shows a simplified schematic cross section of the 15-kV SiC SGTO with a 1-µm n+ buffer layer. The SGTO is an asymmetric device using a pnpn structure and is grown on an n+ 4H-SiC substrate as shown in Fig. 1. This is essential due to the high resistance of p-type SiC substrates. The low doped p-type blocking layer of the 15-kV SGTO is 120 µm thick. The high blocking voltage of the SGTO is enabled by this thick epilayer and multizone edge junction termination extension. The SiC SGTO displayed in this report is a current-controlled device that transitions from the OFF-state to the ON-state when a small current pulse-trigger is applied to the anode relative to the gate region. Details of the device fabrication can be found in Cheng et al.[8]

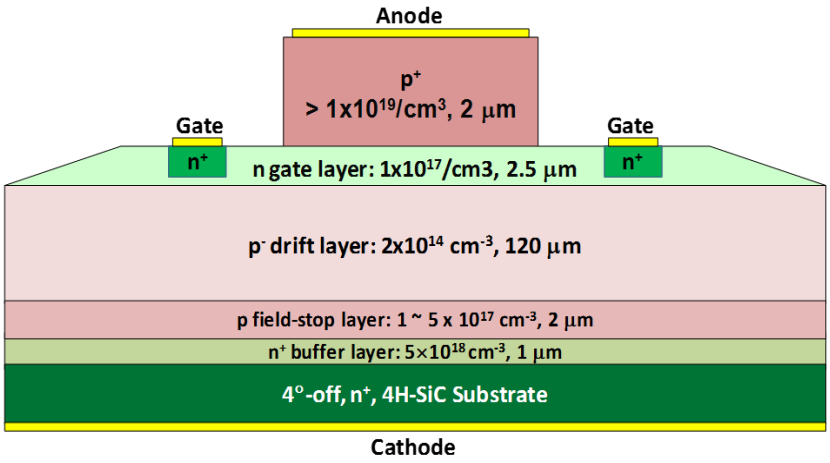

Fig. 1. Simplified schematic cross section of the 15-kV SiC SGTO (diagram not to scale)

3. Device Modeling Approach

The SiC SGTO thyristor is a bipolar device that operates at high-level injection during high-current forward conduction. It is essential to implement accurate SiC physics-based models to characterize the transient characteristics of the SiC devices appropriately under extreme pulsed conditions. It is imperative to incorporate accurate mobility and lifetime models for both the electrons and holes in order to accurately simulate the forward conduction characteristics of the device. To simulate the SiC SGTO thyristor, electron and hole physically based mobility and lifetime models were implemented in a physics-based numerical simulator called

Atlas. These models account for variations in carrier mobility and lifetime as functions of impurity concentration, carrier concentration, and temperature. The mobility models implemented in the simulation include analytic low-field, Conwell-Weisskopf, and Mattheissen's rule.[9] The analytic low-field mobility model has the dependent variables of ionized impurity concentration and lattice temperature, and it models coulombic and phonon scattering in localized sections of the device. The Conwell-Weisskopf mobility model contains the dependent variables of carrier concentration and lattice temperature, and it accounts for the contribution of carrier-carrier scattering to the overall mobility, which becomes significant during high-level injection. Finally, the overall low-field mobility is determined by Mattheissen's rule as a function of the contributions from the analytic low-field mobility and Conwell-Weisskopf model. The two primary lifetime models implemented in the simulation are the Shockley-Read-Hall (SRH) concentration-dependent lifetime model and the Auger recombination lifetime model.[10–14] The SRH model contains the dependent variables of ionized impurity concentration and lattice temperature, and it models lifetime reduction as a function of increasing doping concentration. Finally, the Auger recombination lifetime model is used for consideration of three particle transitions that occur during high-level injection.[9–14] An impact ionization model is included to account for the carrier generation due to high electric fields.[9,15] This model is essential in modeling and simulating the breakdown voltage of the 15-kV SiC SGTO. Furthermore, the temperature-dependent SiC material parameters such as thermal conductivity and volumetric specific heat were accounted for in this work to depict accurate electrothermal behavior of the device under extreme pulsed-switching conditions. The precise modeling of the material thermal conductivity is essential for steady-state simulation of the device. The accurate modeling of the volumetric specific heat is imperative for transient simulation of the device.

4. Experimental Setup and Simulation Overview

A pulse-forming network (PFN) was developed in the Atlas MixedMode module from discrete L and C components in order to simulate the 120-μs full width half maximum pulse used to evaluate the SiC SGTO's pulse-switching characteristics. The gate of the SiC SGTO was driven using a floating voltage pulse source referenced to the anode. The gate voltage pulse was implemented with 200-ns rise and fall times and a duration of 10 μs, during which it pulled 1 A out of the gate to trigger the device on. This gate drive method was used for all transient simulations presented in this work. A simplified schematic of the PFN and SiC SGTO as implemented in the Atlas MixedMode module is shown in Fig. 2.

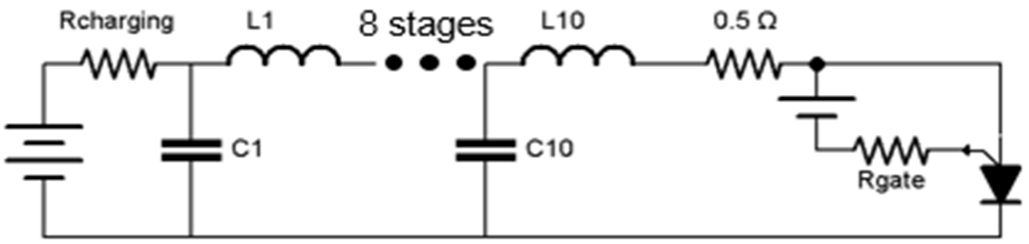

Fig. 2 MixedMode 10-stage PFN schematic for evaluating the pulsed characteristics of the SiC SGTO

A 10-stage, 0.5-Ω PFN was designed and built for determining the pulse power capability, pulse power reliability, safe operating area, and failure modes of advanced power semiconductor switches during pulse overcurrent conditions. The PFN generates a 120-µs, 2-kA (3.85 kA/cm^2) current pulse to meet power requirements for survivability and lethality applications. The pulses were applied at 0.5 Hz to allow the device to return to room temperature after each pulse by minimizing the average power dissipation. The current amplitude was chosen to be approximately 2 kA based off of prior work that determined the pulsed overcurrent safe operating area of a prior generation of SiC SGTOs.[5] The devices were triggered with a gate–anode current of 0.5 A. The transient waveforms gathered during the current pulses include the anode–cathode voltage, anode–cathode current, gate–anode current (device triggering current), and on-state voltage. The anode–cathode voltage is measured with an Agilent Technologies N2891A 70-MHz differential probe; the anode–cathode current is measured with a Power Electronic Measurements Rogowski type CWT 15B with a sensitivity of 2.00 mV/A; the gate–anode current was measured with a Pearson Current Monitor model 2877 with an output of 1.0 V/A; the on-state voltage of the device was accurately measured with an active high-voltage saturation probe. The details about this pulse power evaluation test system are described in Lacouture et al.[16] A simplified block diagram of the power stage and data acquisition is shown in Fig. 3. During the evaluation process, the device under test is removed from the high-energy testbed and its static characteristics are measured with an Agilent Technologies B1505A Power Device Analyzer/Curve Tracer. The static characteristics measured include device forward conduction, gate–anode forward conduction, and gate–anode reverse leakage. The device test procedure includes pulse switching the device to a pulse current of 2 kA for a few iterations. After a few pulsed iterations, the device static characteristics were measured to determine any subtle electrical variation or degradation. These electrical characteristics were obtained using the data acquisition platform as shown in Fig. 3.

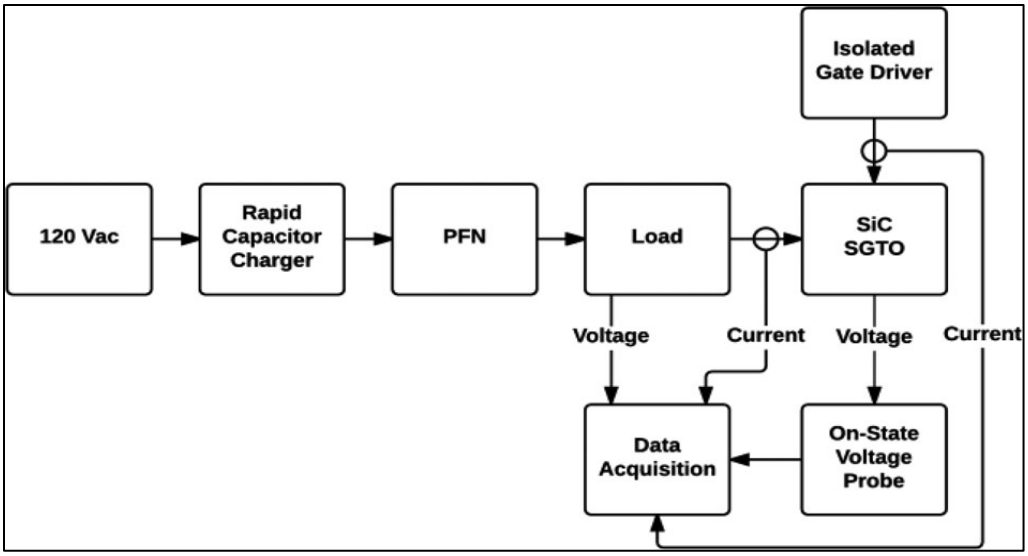

Fig. 3 Simplified block diagram of the pulse evaluation system to characterize high-voltage SiC SGTO

A simplified half-cell cross section of the device as simulated in the Silvaco Atlas numerical simulator is shown in Fig. 4. The physical device has an active conduction area between the edge terminations of 0.52 cm^2. The cell width in simulation is 23 µm and scaled in the z-direction by 2.3×10^6 µm to emulate the simulated current magnitude flowing through the physical device based on its active area. In addition, the anode mesa, n gate, p- drift, and p+ buffer layers in simulation are doped and have depths according to the device fabrication published in Cheng et al.[8]

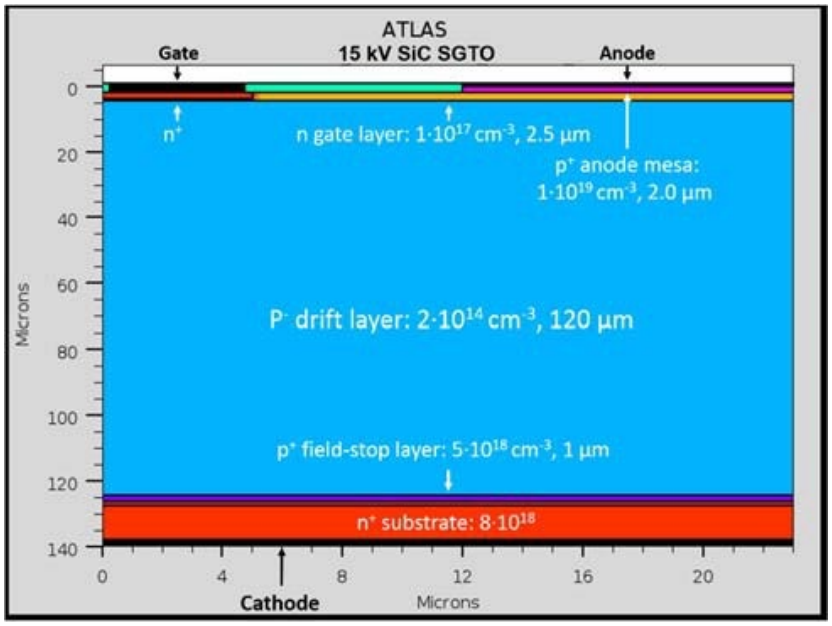

Fig. 4 SiC SGTO half unit cell as simulated in Silvaco Atlas

5. Results and Discussion

Figure 5 demonstrates the 15-kV SiC SGTO's experimentally measured and simulated current-voltage (I-V) characteristics. The experimentally measured I-V characteristics were analyzed up to 20 A, which was the maximum current capability of the Agilent B1505A used to acquire this measurement; the SiC GTO static simulation (isothermal) was implemented beyond 2 kA. In addition, the subplot of Fig. 5 shows the anode–cathode resistance corresponding to the I-V points. Figure 6 depicts a comparison of the experimental device and simulated (non-isothermal) device anode voltage and current waveforms plotted during a 2-kA PFN switching cycle.

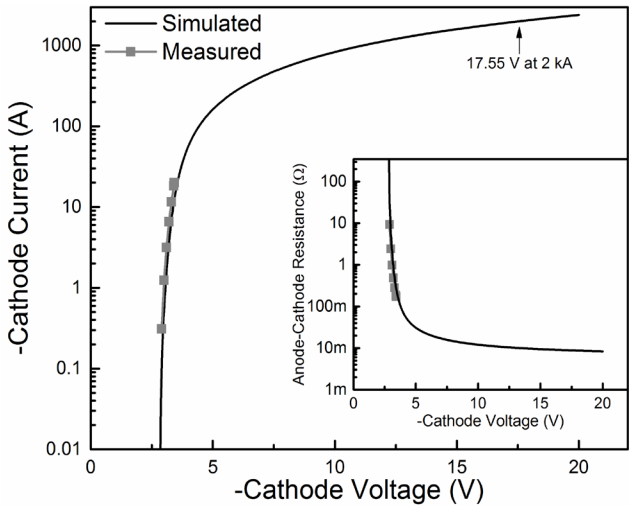

Fig. 5 Experimental and simulated (isothermal) 15-kV SiC SGTO forward characteristics displaying strong similarity

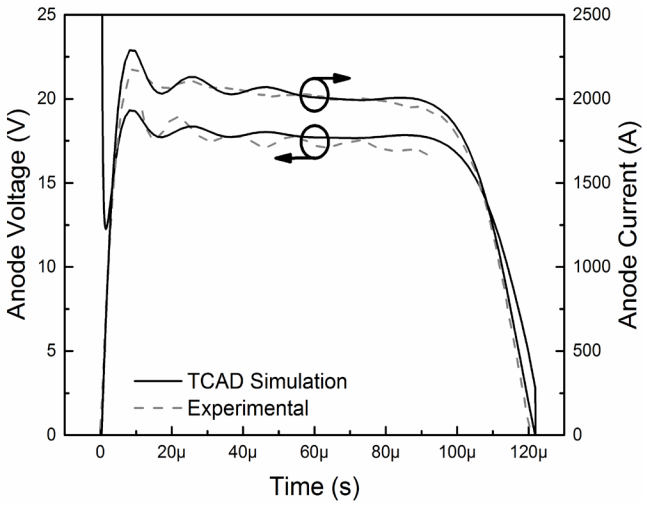

Fig. 6 Experimental and simulated (non-isothermal) 15-kV SiC SGTO anode voltage and current waveforms during a 120-µs 2-kA PFN switching cycle; the concordance between the experimental and simulated waveforms demonstrates the accuracy of the TCAD model

The simulated device peak temperature was approximately 370 K for the waveform shown in Fig. 7 and the device returned to a room termperature of 300 K after 40 ms. The subplot in Fig. 7 also depicts a peak power disspation of 45 kW from the device at 2 kA and at a 120-µs pulse width. The experimental system and TCAD simulation were used in conjunction to determine the failure mechanism of three 15-kV SiC SGTO thyristors during high-current-density (3.85 kA/cm^2) pulsed applications. Figure 7 displays the experimental V_F measured throughout the 2-kA narrow (120-µs pulse width) pulse evaluation of each device until failure. In Fig. 8 the V_F of device 1 started at the lowest level and increased until failure at pulse iteration of 72,000; the V_F of device 2 started at a higher level than device 1 and failed more rapidly with a final abrupt increase in V_F during pulse iteration of 48,470; and device 3 started with the highest V_F and failed after the fewest number of pulses with an abrupt increase in V_F during pulse interation of 9,751. Figure 7 demonstrates that each device exhibited an increasing V_F characteristic of SF formation and propagation.[17–20] The bipolar degradation mechanism of SF formation and propagation is due to minority carrier recombination at a BPD. The high SF concentration is manifested by the foward votlage increase reducing carrier lifetime and forming a potential barrier for carrier transport.[20] Based on the experimental results, it is believed that the long-term reliability and peak current capability of ultra-high-voltage SiC SGTOs for pulsed-power applications can be advanced through the utilization of buffer layers specifically designed to meet the extremely high-current-density requirements.

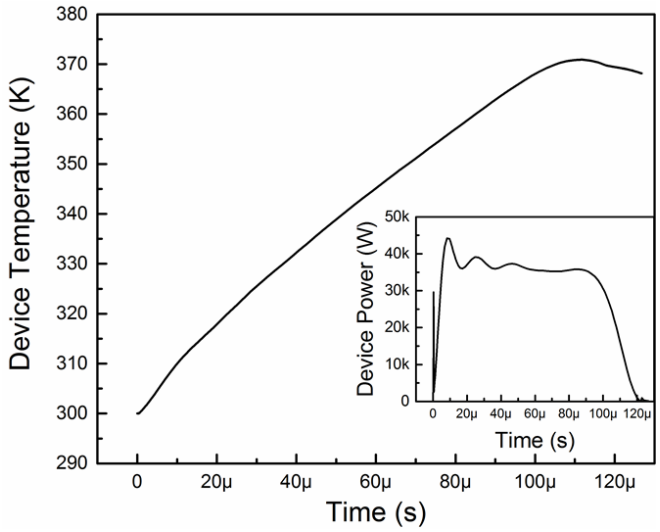

Fig. 7 Simulated temperature and dissipated power of SiC SGTO with a 120-µs pulse at 2 kA

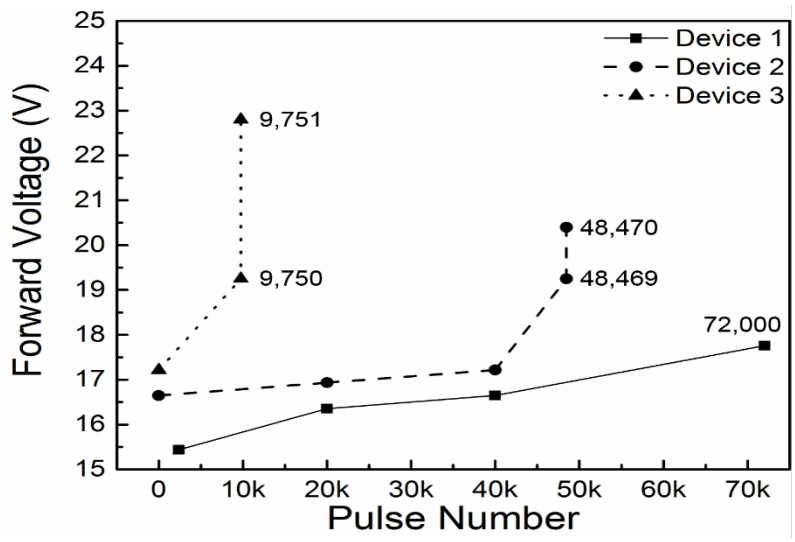

Fig. 8 Experimental V_F measured throughout the 2-kA, 120-µs pulsed evaluation of SiC GTOs until failure

Figure 9 displays the hole concentration throughout the simulated 15-kV SiC SGTO device structure at 91.3 µs into the non-isothermal 2-kA pulse shown in Fig. 6. Figure 9 demonstrates that injection of ~10^{14} cm^{-3} occurs into the substrate during the extremely high-current-density pulsed condition of 3.85 kA/cm^2. In addition, Fig. 10 displays the electron and hole concentrations along the y-axis cutline shown in Fig. 9. In Fig. 10, the x-axis origin correlates to the top of the anode, and the end of the x-axis (x = 140 µm) correlates to 12.5-µm depth into the substrate.

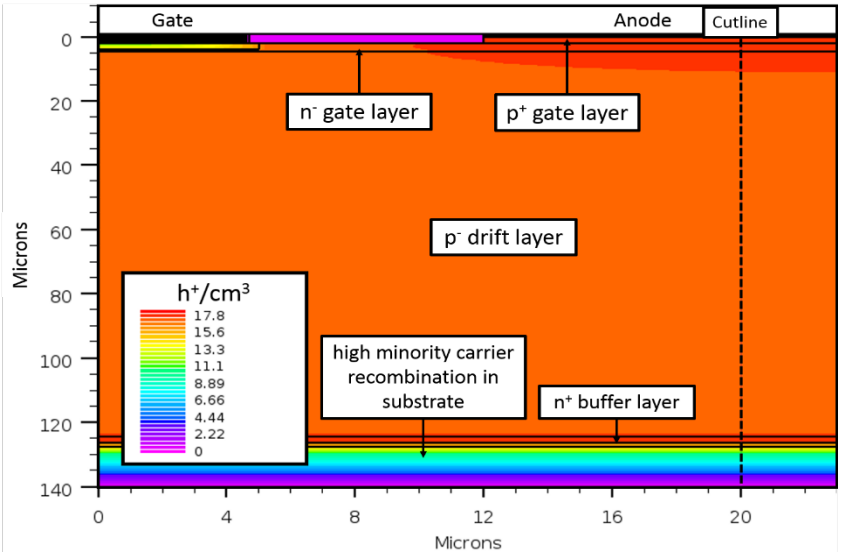

Fig. 9 Simulated hole concentration profile throughout the device structure at a narrow current pulse of 2 kA revealing the exposure of high minority carrier injection into the substrate

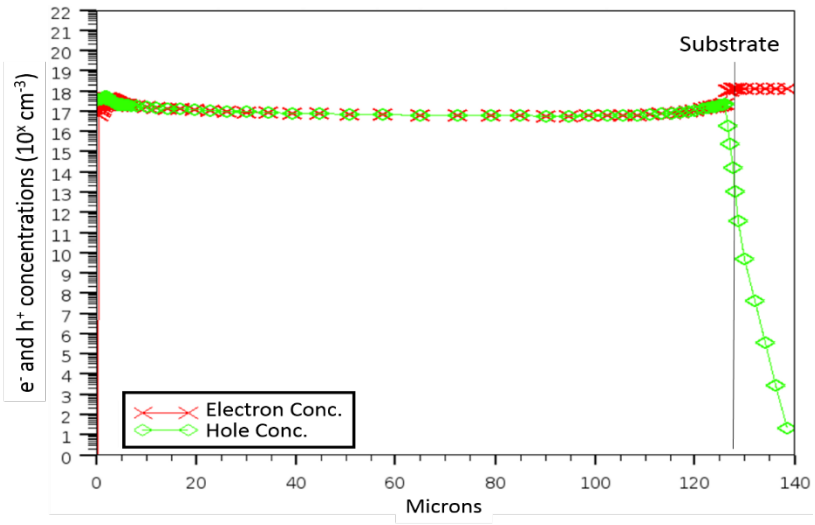

Fig. 10 Simulated electron and hole concentrations along the y-axis cutline that further demonstrates the high (~10^{14} cm^{-3}) minority carrier density injected into the substrate

It is speculated that recombination-induced SF formation occurs in SiC SGTOs operating under extremely high current density. This speculation was supported experimentally by the rapid increase and instability of the V_F drop measured during the device pulse evaluation as shown in Fig. 8. Furthermore, the device simulation results presents a significant hole injection concentration into the substrate as shown in Fig. 10, which could potentially enable the development of SF formation. After the SF formed in the substrate because of the insufficiently thick n^+ buffer layer, the minority carrier recombination would have enabled the SFs to propagate up into the epilayers operating under conductivity modulation. It is speculated that the SF formations eventually resulted in catastrophic device failure as a result of the decreasing device effective active area and corresponding localized increases in current density.[20]

6. Summary and Conclusion

This report compares experimental and simulated device behavior to aid in the failure analysis of 15-kV SiC SGTOs subjected to extreme pulsed current operation. The failure mechanism is suspected to be SF formation because of insufficiently thick buffer layers for pulsed-power application regime. This conclusion is drawn from experimental V_F degradation exhibited during narrow pulsed evaluation at 3.85 kA/cm^2; TCAD modeling and simulation of the device reveals that a fair amount of (~10^{14} cm^{-3}) minority carrier injection into the substrate could be the potential cause of foward voltage degradation in high-voltage SiC SGTO. With these simulated results, it is suspected that the long-term

reliability and peak current capability of ultra-high-voltage SiC SGTOs for pulsed-power applications can be improved by optimizing the buffer layer thickness, making these devices suitable for the extremely high current densities exceeding 100 A/cm^2.

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List of Symbols, Abbreviations, and Acronyms

BPD	basal plane dislocation
GTO	gate turn-off thyristor
I-V	current-voltage
PFN	pulse forming network
SF	stacking fault
SGTO	super-gate turn-off thyristor
SiC	silicon carbide
SRH	Shockley-Read-Hall
TCAD	technology computer-aided design
V_F	forward voltage

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